AM261x Sitara™ Microcontrollers

1 Features

Processor Cores:

- Single and Dual Arm® Cortex® R5F CPU with each core running up to 500 MHz
  - 16KB I-Cache with 64-bit ECC per CPU core
  - 16KB D-cache with 32-bit ECC per CPU core
  - 256KB Tightly Coupled Memory (TCM) per core, with 32-bit ECC
  - Lockstep or Dual core operation supported
- Trigonometric Math Unit (TMU) for accelerating trigonometric functions
  - Up to 2 × TMU, one per R5F MCU core

Memory Subsystem:

- 1.5MB of On-Chip Shared SRAM (3 banks × 512KB). ECC error protection for full 1.5MB OCSRAM.
- 256KB Remote Low latency L2 cache (RL2), software programmable, shared between all cores, allocated from SRAM

System on Chip (SoC) Services and Architecture:

- 1 × EDMA to support data movement functions
- Device Boot supported from the following interfaces:
  - UART (Primary/Backup)
  - OSPI NOR and NAND Flash (50MHz SDR and 25MHz DDR)
  - USB Peripheral boot
- Interprocessor communication modules
  - SPINLOCK module for synchronizing processes running on multiple R5F CPUs and HSM CPU
  - MAILBOX functionality implemented through CTRLMMR registers

Flash Memory Interfaces:

- 2 × Octal Serial Peripheral Interface (OSPI) at up to 133-MHz SDR and 133-MHz DDR at 1.8V and 3.3V which can be used for
  - External flash memory with full XIP (eXecute In Place) support
  - RAM expansion/FOTA
- 1 × 4-bit Multi-Media Card/Secure Digital (MMC/SD) interface
- General-Purpose Memory Controller (GPMC)
  - 16-bit parallel data bus with 22-bit address bus and 4 chip selects
  - Up to 4MB addressable memory space
  - Integrated Error Location Module (ELM) support for error checking

General Connectivity:

- 6 × Universal Asynchronous RX-TX (UART) modules
- 4 × Serial Peripheral Interface (SPI) controllers
- 3 × Local Interconnect Network (LIN) ports
- 3 × Inter-Integrated Circuit (I2C) ports
- 2 × Modular Controller Area Network (MCAN) modules with CAN-FD support
- 1 × Fast Serial Interface Transmitter (FSITX) at up to 200Mbps
- 1 × Fast Serial Interface Receiver (FSIRX) at up to 200Mbps
- Up to 140 × General Purpose I/O (GPIO)

USB 2.0

- Port configurable as USB host, USB device, or USB Dual-Role device
- USB 2.0 Host mode
  - High-Speed (HS, 480Mbps)
  - Full-Speed (FS, 12Mbps)
  - Low-Speed (LS, 1.5Mbps)
- USB 2.0 Device mode
  - High-Speed (HS, 480Mbps)
  - Full-Speed (FS, 12Mbps)

Sensing and Actuation:

- Real-time Control Subsystem (CONTROLSS)
- Flexible Input/Output Crossbars (XBAR)
- 3 × 12-bit Analog to Digital Converters (ADC) with 3 MSPS maximum sampling rate
  - Each ADC module with
    - 7× Single ended channels **OR**
    - 3 × Differential channels
  - Highly configurable ADC digital logic
    - With selectable internal or external reference
    - 4 × Post-Processing blocks for each ADC module
- 9 × Analog Comparators with internal 12-bit DAC reference (CMPSS-A)
- 1 × 12 bit Digital to Analog Converter (DAC)
- 10 × Enhanced High Resolution Pulse Width Modulation (eHRPWM) modules
  - Single or Dual PWM channels
  - Advanced PWM Configurations
  - Enhanced HRPWM extends the time resolution of the PWM compared to EPWM
- 8 × Enhanced Capture (ECAP) modules
- 2 × Enhanced Quadrature Encoder Pulse (EQEP) modules
- 2 × Sigma-Delta Filter Modules (SDFM)

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Industrial Connectivity:

- 2× Programmable Real-time Unit – Industrial Communication SubSystem(2× PRU-ICSS)
  - 2× PRU per ICSS for a total of 4 PRU cores
  - Dual core Programmable Realtime Unit Subsystem (PRU0 / PRU1)
    - Deterministic hardware
    - Dynamic firmware
  - 20-channel enhanced input (eGPI) per PRU
  - 20-channel enhanced output (eGPO) per PRU
  - Embedded Peripherals and Memory
    - 1 × UART, 1x ECAP
    - 1 × MDIO, 1x IEP
    - 1 × 32KB Shared General Purpose RAM
    - 2 × 8KB Shared Data RAM
    - 1 × 12KB IRAM per PRU
    - ScratchPad (SPAD), MAC/CRC
  - Digital encoder and sigma-delta control loops
  - The PRU-ICSS enables advanced industrial protocols including:
    - EtherCAT®, Ethernet/IP™
    - PROFINET®, IO-Link®
  - Dedicated Interrupt Controller (INTC)
  - Dynamic CONTROLSS XBAR Integration
  - Supports standard ethernet (EMAC) – up to 2 external ports

High Speed Interfaces

- Integrated Ethernet Switch(CPSW3G)
  - Supporting two external ports and one internal port with selectable MII/ RMII/ RGMII
  - IEEE 1588 (2008 Annex D, Annex E, Annex F) with 802.1AS PTP
  - Clause 45 MDIO PHY management
  - 512 × ALE engine based packet classifiers
  - Priority flow control with up to 2KB packet size
  - Four CPU hardware interrupt pacing
  - IP/ UDP/ TCP checksum offload in hardware
  - Supports TSN

Security:

- Hardware Security Module (HSM) with support for Auto SHE 1.1/EVITA
- Targeted for ISO 21434 compliance
- Secure boot support
  - Device Take Over Protection
  - Hardware enforced root-of-trust
  - Authenticated boot
  - SW Anti-rollback protection
- Debug security
  - Secure device debug only after proper authentication
  - Ability to disable device debug functionality
- Device ID and Key Management
  - Support for OTP Memory (FUSEROM)
    - Store root keys and other security fields
  - Separate EFUSE controllers and FUSE ROMs
  - Unique Device Public Identifiers
- Memory Protection Units (MPU)
  - Dedicated Arm® MPU per Cortex®-R5F core
  - System MPU - present at various interfaces in the SoC (MPU or Firewall)
  - 8 to 16 Programmable Regions
    - Enable/Privilege ID
    - Start/End Address
    - Read/Write/Cachable
    - Secure/Non-Secure
- Cryptographic acceleration
  - Cryptographic cores with DMA Support
  - AES - 128/192/256-bit key sizes
  - SHA2 - 256/384/512-bit support
  - DRBG with pseudo and true random number generator

Functional Safety:

- Enables design of systems with functional safety requirements
  - Error Signaling Module (ESM)
  - ECC or parity on calculation critical memories
  - Built-In Self-Test (BIST) on-chip RAM
  - Runtime internal diagnostic modules including voltage, temperature, and clock monitoring, windowed watchdog timers, CRC engines for memory integrity checks
- Functional Safety-Compliant targeted [Industrial]
  - Developed for functional safety applications
  - Documentation to be made available to aid IEC 61508 functional safety system design
  - Systematic capability up to SIL-3 targeted
  - Hardware integrity up to SIL-3 targeted
  - Safety-related certification
    - IEC 61508 planned
- Functional Safety-Compliant targeted [Automotive]
  - Developed for functional safety applications
  - Documentation to be made available to aid ISO 26262 functional safety system design
  - Systematic capability up to ASIL-D targeted
  - Hardware integrity up to ASIL-D targeted
  - Safety-related certification
    - ISO 26262 planned

Technology / Package:

- AEC-Q100 qualified for automotive applications
- Package options
  - Available multiple NFBGA packages (see Section 3)
  - With 0.5mm, 0.65 mm and 0.8 mm pitch options

2 Applications

- General Purpose Safety MCU
- Two axis servo drive
- AC Inverter
- Industrial Digital Power Control
  - Energy storage systems
  - EV charging
  - String Inverters
- Remote I/O
- Communication Module
- Automotive Digital Power Conversion/Control
  - On-board Chargers, DC/DC Converters
  - Battery Management Systems (BMS)
- Telematics Control Unit

3 Description

The AM261x Sitara Arm® Microcontrollers are part of Sitara AM26x real-time MCU families designed to meet the complex real-time processing needs of next generation industrial and automotive embedded products. With scalable Arm Cortex® R5F performance and an extensive set of peripherals, AM261x device is designed for a broad range of applications while offering safety features and optimized peripherals for real time control.

Key features and benefits:

- Peripherals supporting system level connectivity such as Gigabit Ethernet, USB, OSPI/QSPI, CAN, UARTs, SPI and GPIOs.
- Granular firewalls managed by Hardware Security Manager (HSM) enable developers to implement stringent security minded system design requirements.
- Up to two R5F cores in cluster with 256KB of shared Tightly Coupled Memory (TCM) per core along with 1.5MB of shared SRAM, greatly reducing the need for external memory.

Package Information

Part Number	Package	Pitch	Package Size
AM261...ZCZQ1	ZCZQ1(NFBGA, 324)	0.8mm	15 mm × 15 mm
AM261...ZFG	ZFG(NFBGA, 304)	0.65mm	13.25 mm × 13.25 mm
AM261...ZEJQ1	ZEJQ1(NFBGA, 256)	0.8mm	13 mm × 13 mm
AM261...ZNC	ZNC(NFBGA, 293)	0.5mm	10 mm × 10 mm

ADVANCE INFORMATION

3.1 Functional Block Diagram

AM261x Functional Block Diagram

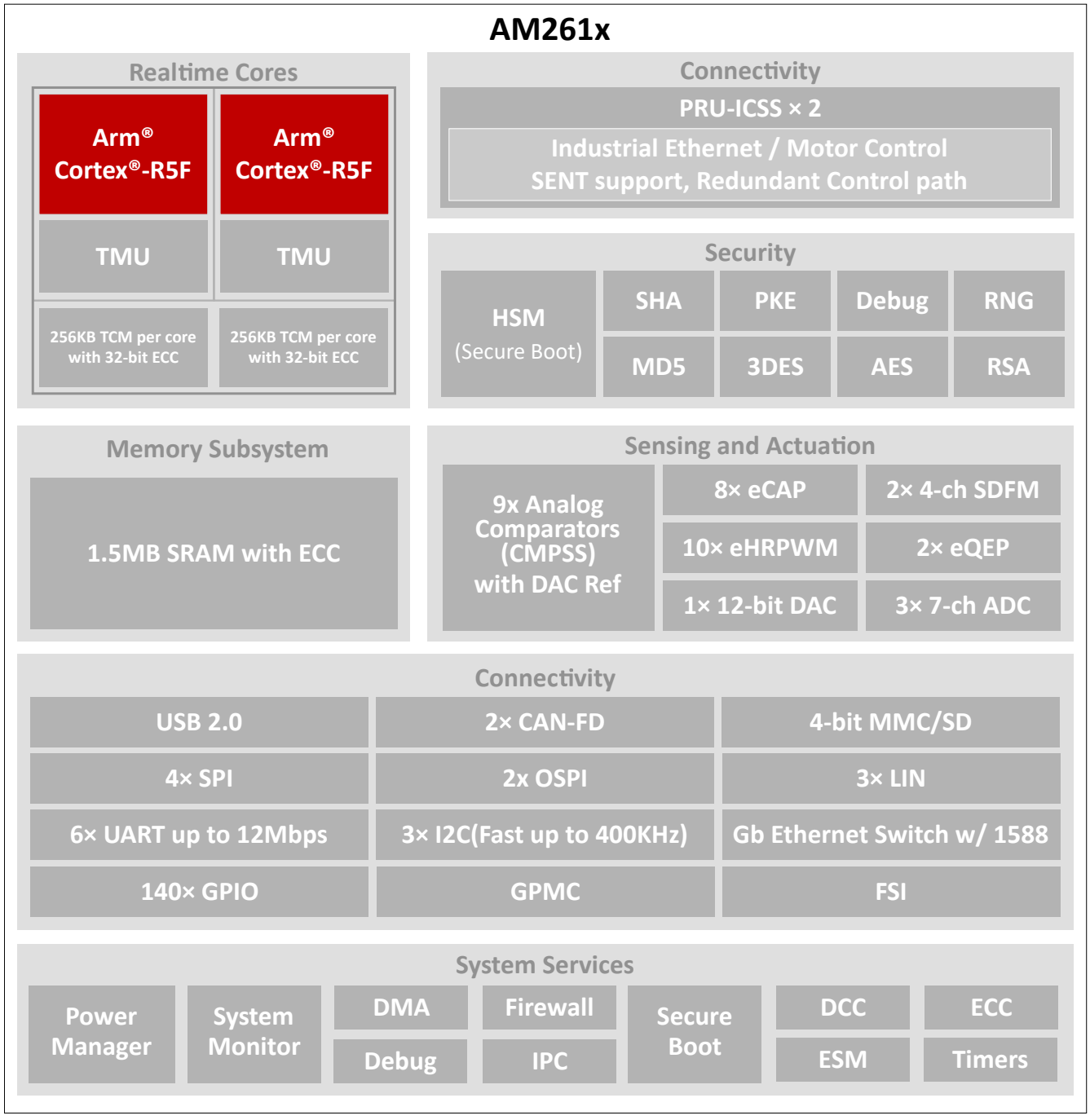

Figure 3-1. AM261x Functional Block Diagram

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4 Package Comparison

Table 4-1 shows a comparison between packages, highlighting the differences.

Table 4-1. Package Comparison

		Packages			
Features	**Reference Name**	**AM261...ZCZ-Q1**	**AM261...ZFG**	**AM261...ZEJ-Q1**	**AM261...ZNC**
JTAG DEVICE ID COMPARISON (FEATURES)					
JTAG Device ID	Industrial:	TBD	TBD	TBD	TBD
	Extended Automotive:	TBD	TBD	TBD	TBD
PROCESSORS AND ACCELERATORS					
Speed Grade		Upto 500 MHz, See Section 6.1.1 Device Naming Convention for more details			
Arm® Cortex-R5F	R5FSS	AM261**2** and AM261**2**-Q1 : 2 cores (1× Dual Core with Lockstep) AM261**1** and AM261**1**-Q1 : 1 core (Single Core)			
Trigonometric Math Unit	TMU	Yes			
Hardware Security Module	HSM	Yes			
Crypto Accelerators	Security	Yes			
PROGRAM AND DATA STORAGE					
On-Chip Shared Memory (RAM)	OCSRAM	Upto 1.5MB, See Section 6.1.1 Device Naming Convention for more details			
R5F Tightly Coupled Memory (TCM)	TCM	Up to 256KB			
PERIPHERALS AND AVAILABLE PINS					
Analog-to-Digital Converter	ADC	ADC0 with 6 channels ADC1 with 6 channels ADC2 with 6 channels ADC_CAL0	ADC0 with 7 channels ADC1 with 7 channels ADC2 with 7 channels ADC_CAL0	ADC0 with 7 channels ADC1 with 7 channels ADC2 with 7 channels ADC_CAL0	ADC0 with 7 channels ADC2 with 7 channels ADC_CAL0
Comparator Modules	CMPSS	9× CMPSS	9× CMPSS	9× CMPSS	6× CMPSS
Gigabit Ethernet Interface	CPSW	CPSW0 with RGMII1, RGMII2 CPSW0 with RMII1, RMII2 CPSW0 with MII1, MII2	CPSW0 with RGMII1, RGMII2 CPSW0 with RMII1, RMII2 CPSW0 with MII1, MII2	CPSW0 with RGMII1, RGMII2 CPSW0 with RMII1, RMII2 CPSW0 with MII1, MII2	CPSW0 with RGMII1, RGMII2 CPSW0 with RMII1, RMII2 CPSW0 with MII1
Digital-to-Analog Converter	DAC	1× DAC	1× DAC	1× DAC	1× DAC
Enhanced Capture Module	ECAP	8× ECAP	8× ECAP	8× ECAP	8× ECAP
Enhanced High Resolution Pulse Width Modulation	eHRPWM	EPWM0 EPWM1 EPWM2 EPWM3 EPWM4 EPWM5 EPWM6 EPWM7 EPWM8 EPWM9	EPWM0 EPWM1 EPWM2 EPWM3 EPWM4 EPWM5 EPWM6 EPWM7 EPWM8 EPWM9	EPWM0 EPWM1 EPWM2 EPWM3 EPWM4 EPWM5 EPWM6 EPWM7 EPWM8 EPWM9	EPWM0 EPWM1 EPWM2 EPWM3 EPWM4 EPWM5 EPWM6 EPWM7 EPWM8 EPWM9
Enhanced Quadrature Encoder Pulse Module	EQEP	EQEP0 EQEP1	EQEP0 EQEP1	EQEP0 EQEP1	EQEP0 EQEP1
Fast Serial Interface	FSI	FSIRX0 FSITX0	FSIRX0 FSITX0	FSIRX0 FSITX0	FSIRX0 FSITX0
General-Purpose I/O	GPIO	141 GPIOs	141 GPIOs	114 GPIOs	112 GPIOs
General-Purpose Memory Controller	GPMC	GPMC0	GPMC0	Not Available	Not Available
Inter-Integrated Circuit Interface	I2C	I2C0 I2C1 I2C2	I2C0 I2C1 I2C2	I2C0 I2C1 I2C2	I2C0 I2C1 I2C2
Local Interconnect Network	LIN	LIN0 LIN1 LIN2	LIN0 LIN1 LIN2	LIN0 LIN1 LIN2	LIN0 LIN1 LIN2
Modular Controller Area Network Interface	MCAN	MCAN0 MCAN1	MCAN0 MCAN1	MCAN0 MCAN1	MCAN0 MCAN1
Full CAN-FD Support	MCAN	MCAN0 MCAN1	MCAN0 MCAN1	MCAN0 MCAN1	MCAN0 MCAN1
Multi-Media Card/Secure Digital Interface	MMC-SD	MMC0	MMC0	MMC0	Not Available
Octal SPI Flash Interface	OSPI	OSPI0 OSPI1	OSPI0 OSPI1	OSPI0 OSPI1	OSPI0 OSPI1

Table 4-1. Package Comparison (continued)

		Packages			
Features	**Reference Name**	**AM261...ZCZ-Q1**	**AM261...ZFG**	**AM261...ZEJ-Q1**	**AM261...ZNC**
Programmable Real-Time Unit Subsystem	PRU-ICSS	PR0-PRU0 PR0-PRU1 PR1-PRU0 PR1-PRU1 and PR0-UART0 PR1-UART0	PR0-PRU0 PR0-PRU1 PR1-PRU0 PR1-PRU1 and PR0-UART0 PR1-UART0	PR0-PRU0 PR0-PRU1(partial) PR1-PRU0 PR1-PRU1 and PR1-UART0	PR0-PRU0(partial) PR0-PRU1(partial) PR1-PRU0(partial) PR1-PRU1(partial)
Industrial Communication Subsystem Support	PRU-ICSS	Refer PRU-ICSS section	Refer PRU-ICSS section	Refer PRU-ICSS section	Refer PRU-ICSS section
Sigma Delta Filter Module	SDFM	SDFM0 SDFM1	SDFM0 SDFM1	SDFM0	Not Available
Serial Peripheral Interface	SPI	SPI0 SPI1 SPI2 SPI3	SPI0 SPI1 SPI2 SPI3	SPI0 SPI1 SPI2 SPI3	SPI0 SPI2
Universal Asynchronous Receiver and Transmitter	UART	UART0 UART1 UART2 UART3 UART4 UART5	UART0 UART1 UART2 UART3 UART4 UART5	UART0 UART1 UART2 UART3 UART4 UART5	UART0 UART1 UART2 UART3 UART4 UART5
Universal Serial Bus	USB	USB0 with external VBUS	USB0 with external VBUS	USB0 with external VBUS	USB0 with external VBUS
Miscellaneous					
CLKOUT	CLKOUT	CLKOUT0 CLKOUT1	CLKOUT0 CLKOUT1	CLKOUT0 CLKOUT1	CLKOUT0
External Reference Clock Input	EXT_REFCLK	EXT_REFCLK0	EXT_REFCLK0	EXT_REFCLK0	EXT_REFCLK0
Junction Temperature		Extended Automotive: –40°C to 150°C	Extended Industrial: –40°C to 125°C	Extended Automotive: –40°C to 150°C	Extended Industrial: –40°C to 125°C
Automotive Qualification		AEC-Q100	-	AEC-Q100	-

ADVANCE INFORMATION

4.1 Related Products

Sitara™ Microcontrollers Family of Arm® Cortex®-R based high performance microcontrollers with advanced networking, real-time control, and signal processing accelerators to meet emerging MCU requirements for industrial and automotive applications.

Sitara™ Processors Family of broad, scalable processors based on Arm® Cortex®-A cores with flexible accelerators, peripherals, connectivity and unified software support – an excellent choice for sensors to servers. Sitara™ processors have the features and reliability necessary for the latest industrial and automotive application-level requirements.

Sitara™ Microcontrollers - Evaluation Modules TI provides device-specific Evaluation Module (EVM) designs to help kick-start product development. See the LP-AM261 for more information.

Products to complete your design The following list of products are frequently purchased or used in conjunction with the AM261x device to meet your system design requirements.

- **TPS65036x-Q1** - Functional safety-compliant multi-rail power supply for safety MCUs applications.
- **TPS3704-Q1** - Automotive multichannel window supervisor with very-high accuracy and compact form factor.
- **DP83TG720S-Q1** - 1000BASE-T1 automotive Ethernet PHY with RGMII.
- **DP83826E** - Low latency 10/100-Mbps Ethernet PHY with MII interface and enhanced mode.
- **TCAN1042H-Q1** - Automotive 70-V bus-fault-protected CAN transceiver with flexible data-rate.

5 Terminal Configuration and Functions

5.1 Pin Diagram

Note

The terms "ball", "pin", and "terminal" are used interchangeably throughout the document. An attempt is made to use "ball" only when referring to the physical package.

The diagrams in this section are used in conjunction with the other Terminal Configuration and Functions tables to locate signal names and ball grid numbers.

ADVANCE INFORMATION

5.1.1 AM261x ZCZ Pin Diagram

AM261x ZCZ Pin Diagram

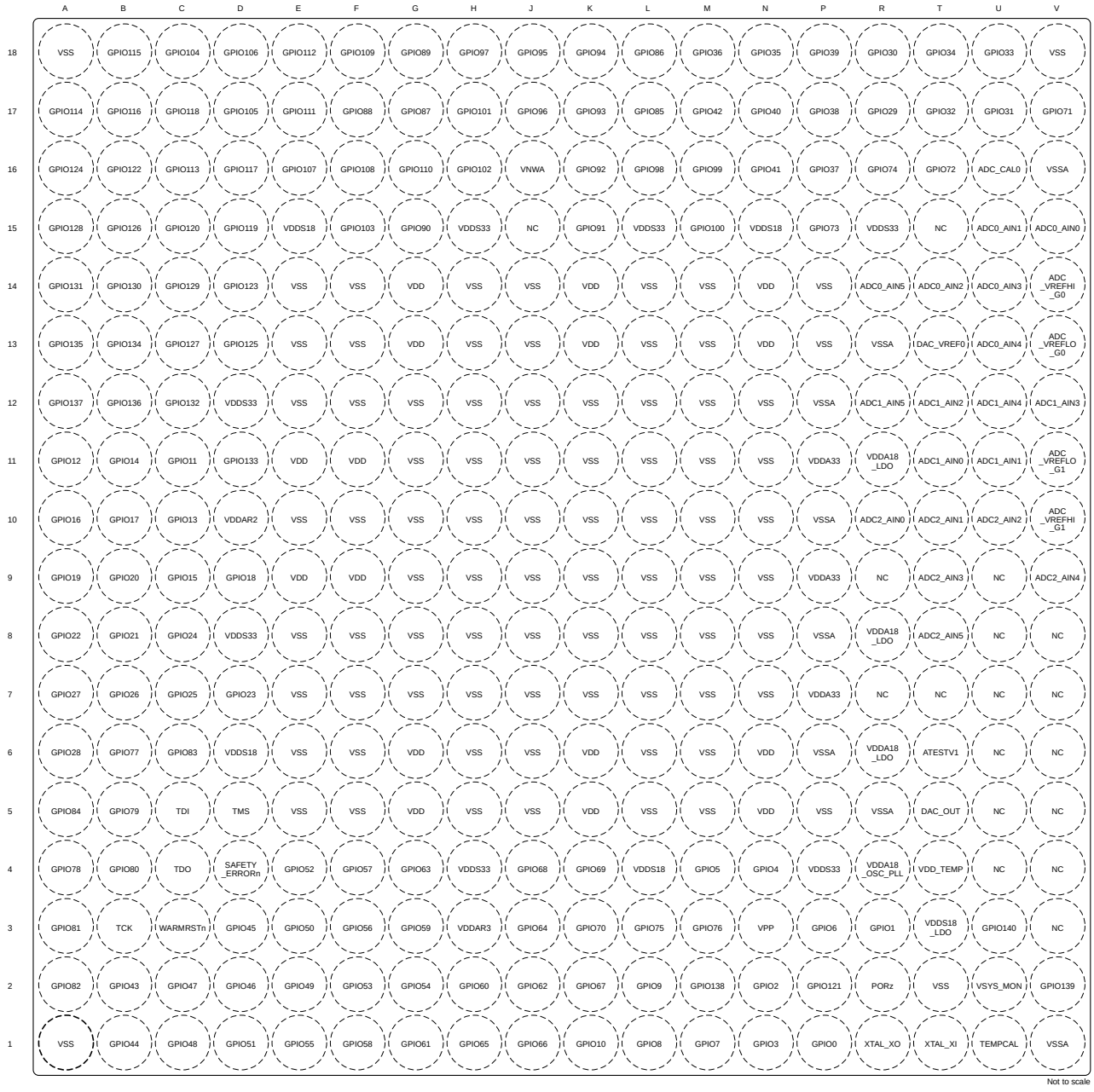

Figure 5-1. AM261x ZCZ Pin Diagram

5.1.2 AM261x ZFG Pin Diagram

AM261x ZFG Pin Diagram

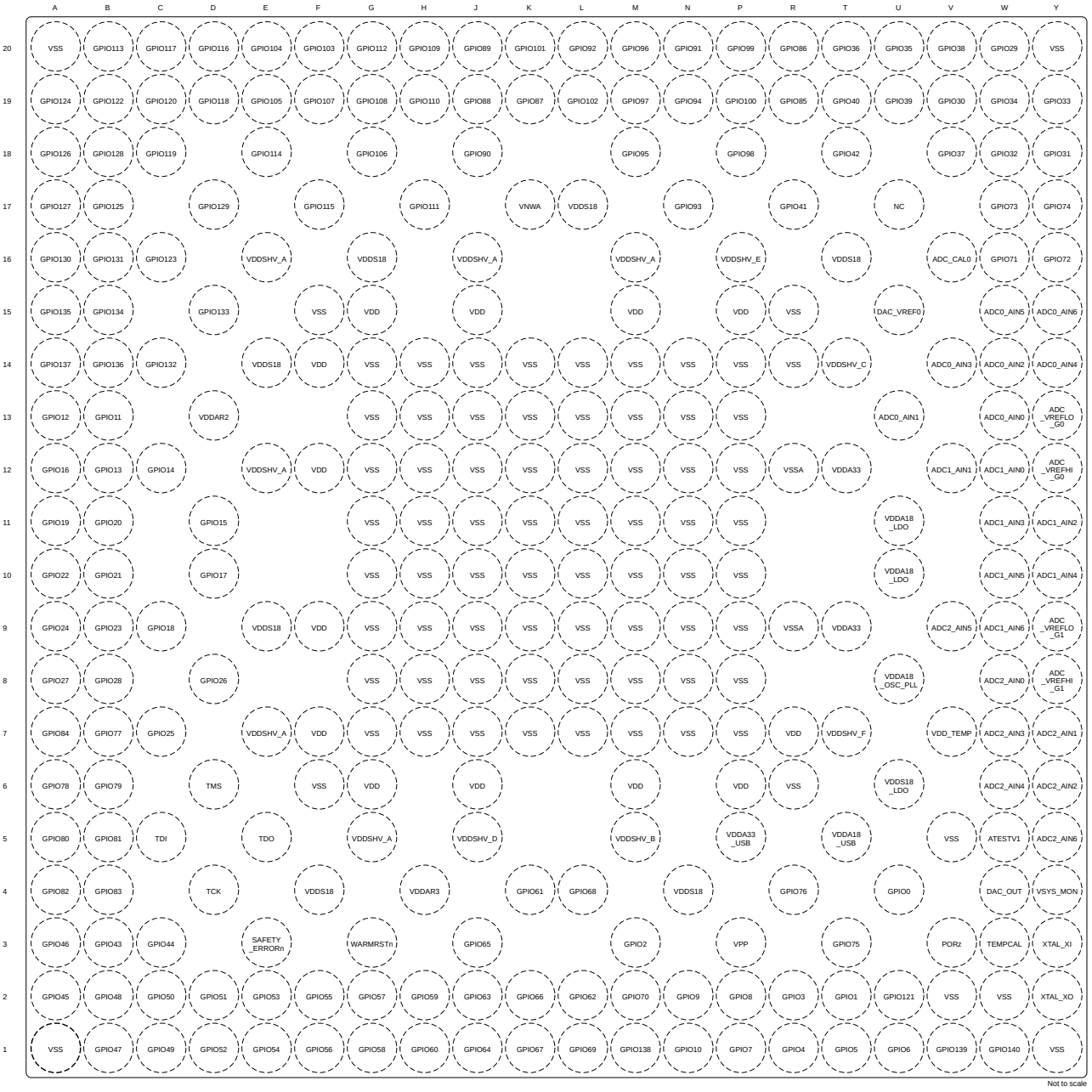

Figure 5-2. AM261x ZFG Pin Diagram

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5.1.3 AM261x ZEJ Pin Diagram

AM261x ZEJ Pin Diagram

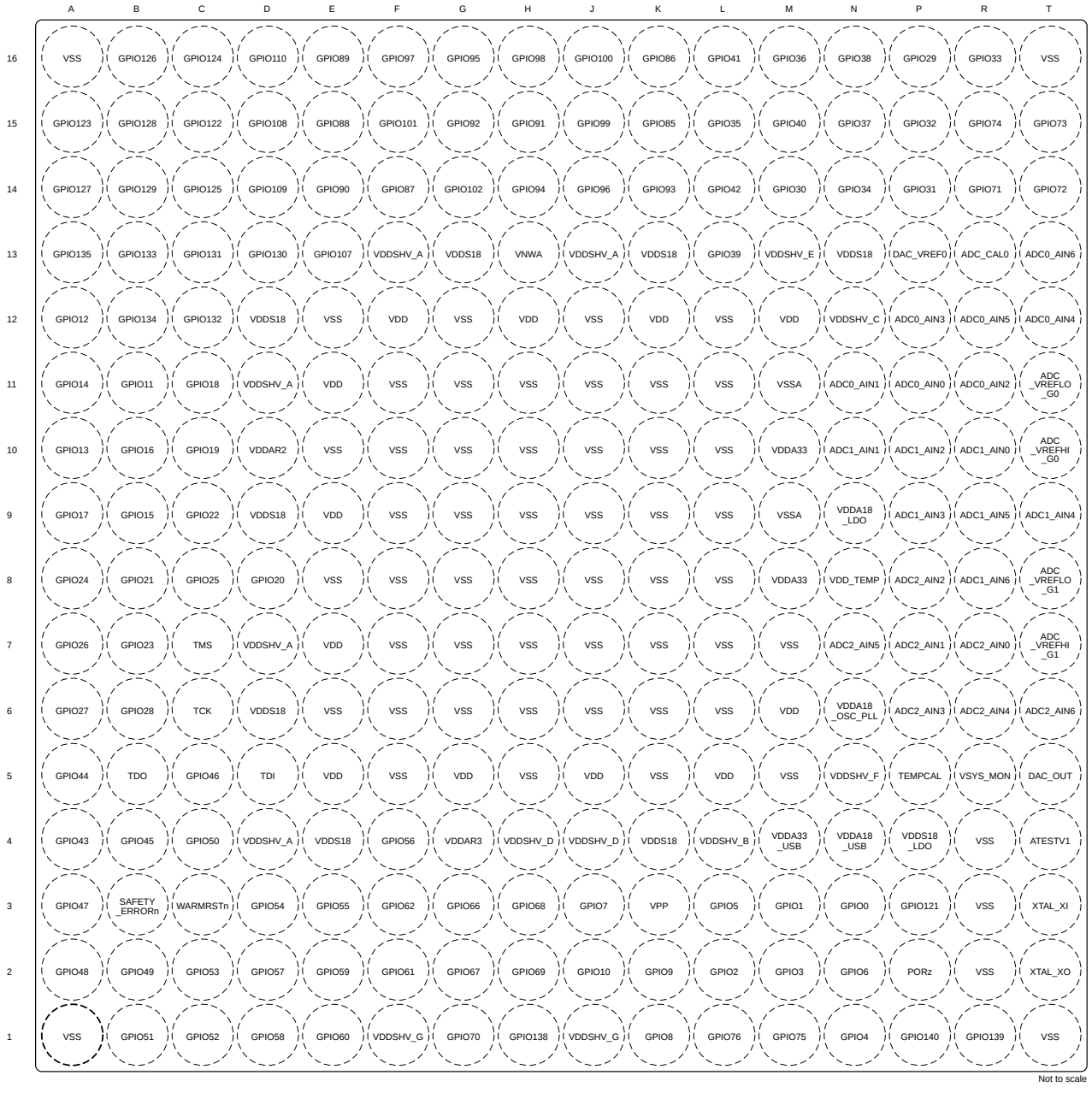

Figure 5-3. AM261x ZEJ Pin Diagram

5.1.4 AM261x ZNC Pin Diagram

AM261x ZNC Pin Diagram

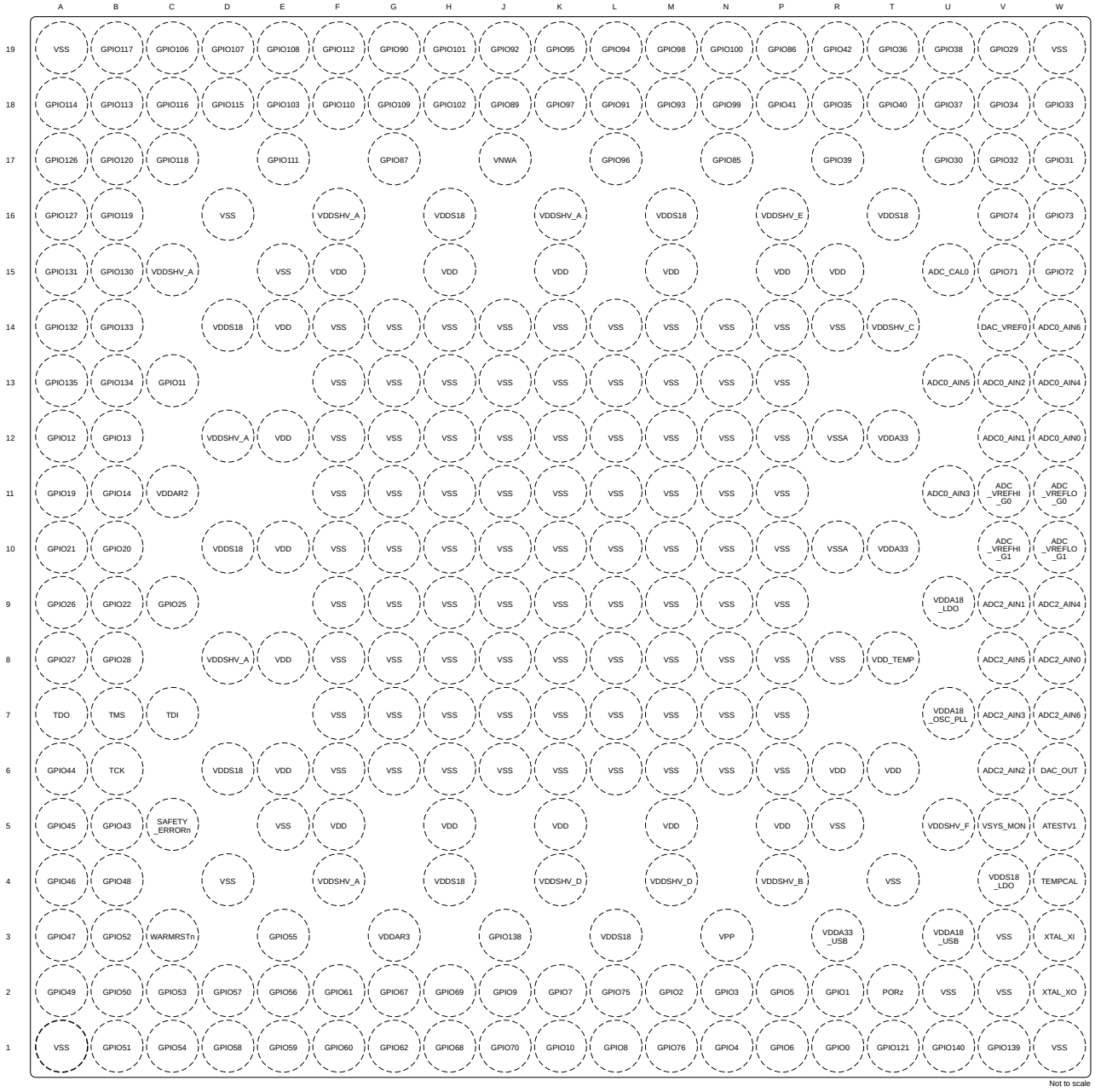

Figure 5-4. AM261x ZNC Pin Diagram

ADVANCE INFORMATION

5.2 Pin Attributes

The following list describes the contents of each column in the *Pin Attributes* table:

1. **Ball Number:** Ball numbers assigned to each terminal of the Ball Grid Array package.
2. **Ball Name:** Ball name assigned to each terminal of the Ball Grid Array package (this name is typically taken from the primary MUXMODE 0 signal function).
3. **Signal Name:** Signal name of all dedicated and pin multiplexed signal functions associated with a ball.

Note

The *Pin Attributes* table, defines the SoC pin multiplexed signal function implemented at the pin and **does not** define secondary multiplexing of signal functions implemented in device subsystems. Secondary multiplexing of signal functions are not described in this table. For more information on secondary multiplexed signal functions, see the respective peripheral chapter of the device TRM.

4. **Mux Mode:** The MUXMODE value associated with each pin multiplexed signal function:
   - MUXMODE 7 is the primary pin multiplexed signal function. However, the primary pin multiplexed signal function is not necessarily the default pin multiplexed signal function.
   - MUXMODE values 1 through 15 are possible for pin multiplexed signal functions. However, not all MUXMODE values have been implemented. The only valid MUXMODE values are those defined as pin multiplexed signal functions within the Pin Attributes table. Only defined valid values of MUXMODE can be used.
   - Bootstrap defines SOC configuration pins, where the logic state applied to each pin is latched on the rising edge of PORz. These input signal functions are fixed to their respective pins and are not programmable via MUXMODE.
   - An empty box or "-" means Not Applicable.

Note

- The value found in the MUX MODE AFTER RESET column defines the default pin multiplexed signal function selected when PORz is deasserted.
- Configuring two pins to the same pin multiplexed signal function can yield unexpected results and is not supported. This can be prevented with proper software configuration.
- Configuring a pad to an undefined multiplexing mode results in undefined behavior and must be avoided.

5. **Type:** Signal type and direction:
   - I = Input
   - O = Output
   - ID = Input, with open-drain output function
   - OD = Output, with open-drain output function
   - IO = Input, Output, or simultaneously Input and Output
   - IOD = Input, Output, or simultaneously Input and Output, with open-drain output function
   - IOZ = Input, Output, or simultaneously Input and Output, with three-state output function
   - OZ = Output with three-state output function
   - A = Analog
   - CAP = LDO capacitor
   - PWR = Power
   - GND = Ground
6. **Ball State During Reset (RX/TX/PULL):** State of the terminal while PORz is asserted, where RX defines the state of the input buffer, TX defines the state of the output buffer, and PULL defines the state of internal pull resistors:
   - RX (Input buffer)
     - Off: The input buffer is **disabled**.

  - On: The input buffer is **enabled**.
- TX (Output buffer)
  - Off: The output buffer is **disabled**.
  - Low: The output buffer is **enabled** and drives V_{OL}.
- PULL (Internal pull resistors)
  - Off: Internal pull resistors are turned **off.**
  - Up: Internal **pull-up** resistor is turned on.
  - Down: Internal **pull-down** resistor is turned on.
  - NA: No internal pull resistor.
- An empty box, or "-" means Not Applicable.

7. **Ball State After Reset (RX/TX/PULL):** State of the terminal after PORz is deasserted, where RX defines the state of the input buffer, TX defines the state of the output buffer, and PULL defines the state of internal pull resistors:
   - RX (Input buffer)
     - Off: The input buffer is **disabled**.
     - On: The input buffer is **enabled**.
   - TX (Output buffer)
     - Off: The output buffer is **disabled**.
     - SS: The subsystem selected with MUXMODE determines the output buffer state.
   - PULL (Internal pull resistors)
     - Off: Internal pull resistors are turned **off.**
     - Up: Internal **pull-up resistor** is turned on.
     - Down: Internal **pull-down resistor** is turned on.
     - NA: No internal pull resistor.
   - An empty box, NA, or "-" means Not Applicable.
8. **Mux Mode After Reset:** The value found in this column defines the **default** pin multiplexed signal function after PORz is deasserted.
   - An empty box, NA, or "-" means Not Applicable.
9. **I/O Voltage**: This column describes I/O **operating voltage** options of the respective power supply, when applicable.
   - An empty box, NA, or "-" means Not Applicable.

   For more information, see valid operating voltage range defined for each power supply in *Recommended Operating Conditions*.
10. **Power:** The power supply of the associated I/O, when applicable.
    - An empty box, NA, or "-" means Not Applicable.
11. **Hys:** Indicates if the input buffer associated with this I/O has hysteresis:
    - Yes: Hysteresis Support
    - No: **No** Hysteresis Support
    - An empty box, NA, or "-" means Not Applicable.

    For more information, see the hysteresis values in *Electrical Characteristics*.
12. **Pull Type:** Indicates the presence of an internal pull-up or pull-down resistor. Internal resistors can be enabled or disabled via software.
    - PU: Internal pull-up Only
    - PD: Internal pull-down Only
    - PU/PD: Internal pull-up and pull-down
    - An empty box, NA, or "-" means No internal pull.

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Note

Configuring two pins to the same pin multiplexed signal function is not supported as this yields unexpected results. Issues can be easily prevented with the proper software configuration.

When a pad is set into a multiplexing mode which is not defined by pin multiplexing, that pad's behavior is undefined. This must be avoided.

13. **Buffer Type:** This column defines the buffer type associated with a terminal. This information can be used to determine the applicable Electrical Characteristics table.
    - An empty box, NA, or "-" means Not Applicable.

    For electrical characteristics, refer to the appropriate buffer type table in *Electrical Characteristics*.
14. **Pad Configuration Register Name:** This is the name of the device pad/pin configuration register.
15. **Pad Configuration Register Address:** This is the memory address of the device pad/pin configuration register.
16. **Pad Configuration Register Default Value**: This is the default value of the register device pad/pin configuration register after PORz is deasserted.

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ Address[15]/ Default Value [16]	Signal Name [3]	Mux Mode [4]	Signal Type [5]	MUX Mode after Reset [7]	IO Voltage [9]	Power [10]	Buffer Type [13]
V15	W13	P11	W12	ADC0_AIN0	ADC0_AIN0		-		-	-	Analog
U15	U13	N11	V12	ADC0_AIN1	ADC0_AIN1		-		-	-	Analog
T14	W14	R11	V13	ADC0_AIN2	ADC0_AIN2		-		-	-	Analog
U14	V14	P12	U11	ADC0_AIN3	ADC0_AIN3		-		-	-	Analog
U13	Y14	T12	W13	ADC0_AIN4	ADC0_AIN4		-		-	-	Analog
R14	W15	R12	U13	ADC0_AIN5	ADC0_AIN5		-		-	-	Analog
	Y15	T13	W14	ADC0_AIN6	ADC0_AIN6		-		-	-	Analog
T11	W12	R10		ADC1_AIN0	ADC1_AIN0		-		-	-	Analog
U11	V12	N10		ADC1_AIN1	ADC1_AIN1		-		-	-	Analog
T12	Y11	P10		ADC1_AIN2	ADC1_AIN2		-		-	-	Analog
V12	W11	P9		ADC1_AIN3	ADC1_AIN3		-		-	-	Analog
U12	Y10	T9		ADC1_AIN4	ADC1_AIN4		-		-	-	Analog
R12	W10	R9		ADC1_AIN5	ADC1_AIN5		-		-	-	Analog
	W9	R8		ADC1_AIN6	ADC1_AIN6		-		-	-	Analog
R10	W8	R7	W8	ADC2_AIN0	ADC2_AIN0		-		-	-	Analog
T10	Y7	P7	V9	ADC2_AIN1	ADC2_AIN1		-		-	-	Analog
U10	Y6	P8	V6	ADC2_AIN2	ADC2_AIN2		-		-	-	Analog
T9	W7	P6	V7	ADC2_AIN3	ADC2_AIN3		-		-	-	Analog
V9	W6	R6	W9	ADC2_AIN4	ADC2_AIN4		-		-	-	Analog
T8	V9	N7	V8	ADC2_AIN5	ADC2_AIN5		-		-	-	Analog
	Y5	T6	W7	ADC2_AIN6	ADC2_AIN6		-		-	-	Analog
U16	V16	R13	U15	ADC_CAL0	ADC_CAL0		-		-	-	Analog
V14	Y12	T10	V11	ADC_VREFHI_G0	ADC_VREFHI1		-		-	-	Analog
					ADC_VREFHI0		-				
V10	Y8	T7	V10	ADC_VREFHI_G1	ADC_VREFHI2		-		-	-	Analog
V13	Y13	T11	W11	ADC_VREFLO_G0	ADC_VREFLO0		-		-	-	Analog
					ADC_VREFLO1		-				
V11	Y9	T8	W10	ADC_VREFLO_G1	ADC_VREFLO2		-		-	-	Analog
T6	W5	T4	W5	ATESTV1	ATESTV1			-		-	-
T5	W4	T5	W6	DAC_OUT	DAC_OUT		-		-	-	Analog
T13	U15	P13	V14	DAC_VREF0	DAC_VREF0		-		-	-	Analog

Analog

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Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ Address[15]/ Default Value [16]	Signal Name [3]	Mux Mode [4]	Signal Type [5]	MUX Mode after Reset [7]	IO Voltage [9]	Power [10]	Buffer Type [13]
P1	U4	N3	R1	GPIO0 GPIO0_CFG_REG 0x5310 0000 0x0000 05F7	OSPI0_CSn0	0	O	Mode7	3.3 V	GENERAL	LVCMOS
					SPI0_CS0	1	IO				
					UART3_RXD	2	I				
					OSPI0_D0	4	IO				
					GPIO0	7	IO				
R3	T2	M3	R2	GPIO1 GPIO1_CFG_REG 0x5310 0004 0x0000 05F7	OSPI0_CSn1	0	O	Mode7	3.3 V	GENERAL	LVCMOS
					SPI0_CLK	1	IO				
					UART3_TXD	2	O				
					UART2_RTSn	5	O				
					GPIO1	7	IO				
					XBAROUT0	10	O				
N2	M3	L2	M2	GPIO2 GPIO2_CFG_REG 0x5310 0008 0x0000 05F7	OSPI0_CLK	0	O	Mode7	1.8 V/3.3 V	FLASH0	LVCMOS
					OSPI0_D0	1	IO				
					UART3_CTSn	4	I				
					OSPI1_D0	5	IO				
					GPIO2	7	IO				
N1	R2	M2	N2	GPIO3 GPIO3_CFG_REG 0x5310 000C 0x0000 05D7	OSPI0_D0	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					EPWM9_A	1	O				
					PR1_PRU1_GPIO11	2	IO				
					UART1_DCDn	3	I				
					GPMC0_AD11	6	O				
					GPIO3	7	IO				
					SOP0	Bootstrap					
N4	R1	N1	N1	GPIO4 GPIO4_CFG_REG 0x5310 0010 0x0000 05D7	OSPI0_D1	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					EPWM9_B	1	O				
					PR1_PRU1_GPIO12	2	IO				
					UART1_RIn	3	I				
					GPMC0_AD12	6	O				
					GPIO4	7	IO				
					SOP1	Bootstrap					
M4	T1	L3	P2	GPIO5 GPIO5_CFG_REG 0x5310 0014 0x0000 05F7	OSPI0_D2	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					SPI0_D0	1	IO				
					OSPI0_D6	2	IO				
					GPIO5	7	IO				
					DTB_OUT_12	15	O				

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ Address[15]/ Default Value [16]	Signal Name [3]	Mux Mode [4]	Signal Type [5]	MUX Mode after Reset [7]	IO Voltage [9]	Power [10]	Buffer Type [13]
P3	U1	N2	P1	GPIO6 GPIO6_CFG_REG 0x5310 0018 0x0000 05F7	OSPI0_D3	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					SPI0_D1	1	IO				
					OSPI0_D4	2	IO				
					GPIO6	7	IO				
					DTB_INOUT_1	15	IO				
M1	P1	J3	K2	GPIO7 GPIO7_CFG_REG 0x5310 001C 0x0000 05F7	MCAN0_RX	0	I	Mode7	1.8 V/3.3 V	FLASH0	LVCMOS
					OSPI0_D4	1	IO				
					OSPI0_D2	2	IO				
					OSPI0_DQS	5	I				
					GPIO7	7	IO				
L1	P2	K1	L1	GPIO8 GPIO8_CFG_REG 0x5310 0020 0x0000 05F7	MCAN0_TX	0	O	Mode7	1.8 V/3.3 V	FLASH0	LVCMOS
					OSPI0_D5	1	IO				
					OSPI0_D6	2	IO				
					OSPI0_D2	5	IO				
					GPIO8	7	IO				
L2	N2	K2	J2	GPIO9 GPIO9_CFG_REG 0x5310 0024 0x0000 05F7	MCAN1_RX	0	I	Mode7	1.8 V/3.3 V	FLASH0	LVCMOS
					OSPI0_D6	1	IO				
					OSPI0_DQS	2	I				
					LIN1_TXD	3	IO				
					UART1_TXD	4	O				
					OSPI0_CLK	5	O				
					GPIO9	7	IO				
K1	N1	J2	K1	GPIO10 GPIO10_CFG_REG 0x5310 0028 0x0000 05F7	MCAN1_TX	0	O	Mode7	1.8 V/3.3 V	FLASH0	LVCMOS
					OSPI0_D7	1	IO				
					OSPI0_CLK	2	O				
					UART1_DTRn	3	O				
					UART3_CTSn	4	I				
					OSPI1_CLK	5	O				
					GPIO10	7	IO				

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Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ Address[15]/ Default Value [16]	Signal Name [3]	Mux Mode [4]	Signal Type [5]	MUX Mode after Reset [7]	IO Voltage [9]	Power [10]	Buffer Type [13]
C11	B13	B11	C13	GPIO11 GPIO11_CFG_REG 0x5310 002C 0x0000 05F7	SPI0_CS0	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					PR1_PRU0_GPIO2	1	IO				
					MMC0_CLK	2	IO				
					UART3_RXD	3	I				
					GPMC0_A0	6	O				
					GPIO11	7	IO				
					ADC_EXTCH_XBAROUT0	9	O				
					XBAROUT0	10	O				
					DTB_INOUT_3	15	IO				
A11	A13	A12	A12	GPIO12 GPIO12_CFG_REG 0x5310 0030 0x0000 05D7	SPI0_CLK	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					PR1_PRU0_GPIO9	1	IO				
					MMC0_CMD	2	IO				
					UART3_TXD	3	O				
					FSITX0_CLK	5	O				
					GPMC0_A7	6	O				
					GPIO12	7	IO				
					ADC_EXTCH_XBAROUT1	9	O				
					XBAROUT1	10	O				
					DTB_OUT_15	15	O				
					SOP2	Bootstrap					
C10	B12	A10	B12	GPIO13 GPIO13_CFG_REG 0x5310 0034 0x0000 05D7	SPI0_D0	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					PR1_PRU0_GPIO0	1	IO				
					MMC0_D0	2	IO				
					UART3_CTSn	3	I				
					FSITX0_DATA0	5	O				
					GPMC0_A16	6	O				
					GPIO13	7	IO				
					ADC_EXTCH_XBAROUT2	9	O				
					XBAROUT2	10	O				
					DTB_INOUT_2	15	IO				
					SOP3	Bootstrap					

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ Address[15]/ Default Value [16]	Signal Name [3]	Mux Mode [4]	Signal Type [5]	MUX Mode after Reset [7]	IO Voltage [9]	Power [10]	Buffer Type [13]
B11	C12	A11	B11	GPIO14 GPIO14_CFG_REG 0x5310 0038 0x0000 05F7	SPI0_D1	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					PR1_PRU0_GPIO1	1	IO				
					MMC0_D1	2	IO				
					UART3_RTSn	3	O				
					FSITX0_DATA1	5	O				
					GPMC0_BE1n	6	O				
					GPIO14	7	IO				
					ADC_EXTCH_XBAROUT3	9	O				
					XBAROUT3	10	O				
					DTB_INOUT_5	15	IO				
C9	D11	B9		GPIO15 GPIO15_CFG_REG 0x5310 003C 0x0000 05F7	SPI1_CS0	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					EPWM7_A	1	O				
					MMC0_D2	2	IO				
					UART4_TXD	3	O				
					PR1_PRU1_GPIO4	5	IO				
					GPIO15	7	IO				
					GPMC0_WAIT0	8	I				
					ADC_EXTCH_XBAROUT4	9	O				
					XBAROUT1	10	O				
A10	A12	B10		GPIO16 GPIO16_CFG_REG 0x5310 0040 0x0000 05F7	SPI1_CLK	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					EPWM7_B	1	O				
					MMC0_D3	2	IO				
					UART4_RXD	3	I				
					PR1_PRU1_GPIO3	5	IO				
					FSIRX0_CLK	6	I				
					GPIO16	7	IO				
					GPMC0_OEn_REn	8	O				
					ADC_EXTCH_XBAROUT5	9	O				
					XBAROUT2	10	O				

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Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ Address[15]/ Default Value [16]	Signal Name [3]	Mux Mode [4]	Signal Type [5]	MUX Mode after Reset [7]	IO Voltage [9]	Power [10]	Buffer Type [13]
B10	D10	A9		GPIO17 GPIO17_CFG_REG 0x5310 0044 0x0000 05F7	SPI1_D0	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					EPWM8_A	1	O				
					MMC0_WP	2	I				
					UART5_TXD	3	O				
					OSPI0_ECC_FAIL	4	I				
					PR1_PRU1_GPIO16	5	IO				
					FSIRX0_DATA0	6	I				
					GPIO17	7	IO				
					GPMC0_DIR	8	O				
					ADC_EXTCH_XBAROUT6	9	O				
					XBAROUT3	10	O				
D9	C9	C11		GPIO18 GPIO18_CFG_REG 0x5310 0048 0x0000 05F7	SPI1_D1	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					EPWM8_B	1	O				
					MMC0_CD	2	I				
					UART5_RXD	3	I				
					OSPI0_RESET_OUT0	4	O				
					PR1_PRU1_GPIO15	5	IO				
					FSIRX0_DATA1	6	I				
					GPIO18	7	IO				
					GPMC0_WPn	8	O				
					ADC_EXTCH_XBAROUT7	9	O				
					XBAROUT4	10	O				
A9	A11	C10	A11	GPIO19 GPIO19_CFG_REG 0x5310 004C 0x0000 05F7	LIN1_RXD	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					OSPI0_ECC_FAIL	1	I				
					SPI2_CS0	2	IO				
					PR1_PRU1_GPIO6	3	IO				
					OSPI1_ECC_FAIL	4	I				
					UART1_RXD	5	I				
					GPMC0_AD6	6	IO				
					GPIO19	7	IO				
					OSPI0_RESET_OUT1	8	O				
					XBAROUT5	10	O				
					EPWM6_B	11	O				

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Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ Address[15]/ Default Value [16]	Signal Name [3]	Mux Mode [4]	Signal Type [5]	MUX Mode after Reset [7]	IO Voltage [9]	Power [10]	Buffer Type [13]
M15	P19	J16	N19	GPIO100 GPIO100_CFG_REG 0x5310 0190 0x0000 05F7	PR0_PRU0_GPIO12	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					RMII2_TXD1	2	O				
					RGMII2_TD1	3	O				
					MII2_TXD1	4	O				
					GPIO100	7	IO				
H17	K20	F15	H19	GPIO101 GPIO101_CFG_REG 0x5310 0194 0x0000 05F7	PR0_PRU0_GPIO13	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					RGMII2_TD2	3	O				
					MII2_TXD2	4	O				
					GPIO101	7	IO				
H16	L19	G14	H18	GPIO102 GPIO102_CFG_REG 0x5310 0198 0x0000 05F7	PR0_PRU0_GPIO14	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					RGMII2_TD3	3	O				
					MII2_TXD3	4	O				
					GPIO102	7	IO				
F15	F20		E18	GPIO103 GPIO103_CFG_REG 0x5310 019C 0x0000 05F7	PR0_PRU1_GPIO5	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					RMII1_RX_ER	2	I				
					MII1_RX_ER	4	I				
					GPIO103	7	IO				
					TRC_DATA0	8	O				
					ADC_EXTCH_XBAROUT6	9	O				
C18	E20			GPIO104 GPIO104_CFG_REG 0x5310 01A0 0x0000 05F7	PR0_PRU1_GPIO9	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					PR0_UART0_RXD	1	I				
					PR0_IEP0_EDIO_DATA_IN_OUT31	3	IO				
					MII1_COL	4	I				
					GPMC0_A21	6	O				
					GPIO104	7	IO				
					TRC_DATA1	8	O				
					ADC_EXTCH_XBAROUT7	9	O				
D17	E19			GPIO105 GPIO105_CFG_REG 0x5310 01A4 0x0000 05F7	PR0_PRU1_GPIO10	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					PR0_UART0_TXD	1	O				
					RMII1_CRS_DV	2	I				
					PR0_IEP0_EDIO_DATA_IN_OUT30	3	IO				
					MII1_CRS	4	I				
					GPMC0_A20	6	O				
					GPIO105	7	IO				
					TRC_DATA2	8	O				

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Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ Address[15]/ Default Value [16]	Signal Name [3]	Mux Mode [4]	Signal Type [5]	MUX Mode after Reset [7]	IO Voltage [9]	Power [10]	Buffer Type [13]
D18	G18		C19	GPIO106 GPIO106_CFG_REG 0x5310 01A8 0x0000 05F7	PR0_PRU1_GPIO8	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					GPIO106	7	IO				
					TRC_DATA3	8	O				
E16	F19	E13	D19	GPIO107 GPIO107_CFG_REG 0x5310 01AC 0x0000 05F7	PR0_PRU1_GPIO6	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					MCAN0_RX	1	I				
					RMII1_REF_CLK	2	IO				
					RGMII1_RXC	3	I				
					MII1_RXCLK	4	I				
					GPIO107	7	IO				
					TRC_DATA4	8	O				
					DTB_INOUT_4	15	IO				
F16	G19	D15	E19	GPIO108 GPIO108_CFG_REG 0x5310 01B0 0x0000 05F7	PR0_PRU1_GPIO4	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					MCAN0_TX	1	O				
					RGMII1_RX_CTL	3	I				
					MII1_RXDV	4	I				
					GPIO108	7	IO				
					TRC_DATA5	8	O				
					DTB_OUT_9	15	O				
F18	H20	D14	G18	GPIO109 GPIO109_CFG_REG 0x5310 01B4 0x0000 05F7	PR0_PRU1_GPIO0	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					MCAN1_RX	1	I				
					RMII1_RXD0	2	I				
					RGMII1_RD0	3	I				
					MII1_RXD0	4	I				
					GPIO109	7	IO				
					TRC_DATA6	8	O				
G16	H19	D16	F18	GPIO110 GPIO110_CFG_REG 0x5310 01B8 0x0000 05F7	PR0_PRU1_GPIO1	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					MCAN1_TX	1	O				
					RMII1_RXD1	2	I				
					RGMII1_RD1	3	I				
					MII1_RXD1	4	I				
					GPIO110	7	IO				
					TRC_DATA7	8	O				
					DTB_OUT_13	15	O				

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ Address[15]/ Default Value [16]	Signal Name [3]	Mux Mode [4]	Signal Type [5]	MUX Mode after Reset [7]	IO Voltage [9]	Power [10]	Buffer Type [13]
E17	H17		E17	GPIO111 GPIO111_CFG_REG 0x5310 01BC 0x0000 05F7	PR0_PRU1_GPIO2	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					RGMII1_RD2	3	I				
					MII1_RXD2	4	I				
					GPIO111	7	IO				
					TRC_DATA8	8	O				
E18	G20		F19	GPIO112 GPIO112_CFG_REG 0x5310 01C0 0x0000 05F7	PR0_PRU1_GPIO3	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					RGMII1_RD3	3	I				
					MII1_RXD3	4	I				
					GPIO112	7	IO				
					TRC_DATA9	8	O				
C16	B20		B18	GPIO113 GPIO113_CFG_REG 0x5310 01C4 0x0000 05F7	PR0_PRU1_GPIO16	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					RGMII1_TXC	3	O				
					MII1_TXCLK	4	I				
					GPIO113	7	IO				
					TRC_DATA10	8	O				
A17	E18		A18	GPIO114 GPIO114_CFG_REG 0x5310 01C8 0x0000 05F7	PR0_PRU1_GPIO15	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					RMII1_TX_EN	2	O				
					RGMII1_TX_CTL	3	O				
					MII1_TX_EN	4	O				
					GPIO114	7	IO				
					TRC_DATA11	8	O				
B18	F17		D18	GPIO115 GPIO115_CFG_REG 0x5310 01CC 0x0000 05F7	PR0_PRU1_GPIO11	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					RMII1_TXD0	2	O				
					RGMII1_TD0	3	O				
					MII1_TXD0	4	O				
					GPIO115	7	IO				
					TRC_DATA12	8	O				
B17	D20		C18	GPIO116 GPIO116_CFG_REG 0x5310 01D0 0x0000 05F7	PR0_PRU1_GPIO12	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					RMII1_TXD1	2	O				
					RGMII1_TD1	3	O				
					MII1_TXD1	4	O				
					GPIO116	7	IO				
					TRC_DATA13	8	O				

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Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ Address[15]/ Default Value [16]	Signal Name [3]	Mux Mode [4]	Signal Type [5]	MUX Mode after Reset [7]	IO Voltage [9]	Power [10]	Buffer Type [13]
D16	C20		B19	GPIO117 GPIO117_CFG_REG 0x5310 01D4 0x0000 05F7	PR0_PRU1_GPIO13	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					RGMII1_TD2	3	O				
					MII1_TXD2	4	O				
					GPIO117	7	IO				
					TRC_DATA14	8	O				
					XBAROUT11	10	O				
C17	D19		C17	GPIO118 GPIO118_CFG_REG 0x5310 01D8 0x0000 05F7	PR0_PRU1_GPIO14	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					RGMII1_TD3	3	O				
					MII1_TXD3	4	O				
					GPIO118	7	IO				
					TRC_DATA15	8	O				
					XBAROUT12	10	O				
D15	C18		B16	GPIO119 GPIO119_CFG_REG 0x5310 01DC 0x0000 05F7	PR0_PRU1_GPIO19	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					UART3_RXD	2	I				
					PR0_IEP0_EDC_SYNC_OUT0	3	O				
					GPMC0_A19	6	O				
					GPIO119	7	IO				
					TRC_CLK	8	O				
					EQEP1_A	9	I				
					XBAROUT13	10	O				
C15	C19		B17	GPIO120 GPIO120_CFG_REG 0x5310 01E0 0x0000 05F7	PR0_PRU1_GPIO18	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					UART3_TXD	2	O				
					PR0_IEP0_EDIO_DATA_IN_OUT31	3	IO				
					GPMC0_A17	6	O				
					GPIO120	7	IO				
					TRC_CTL	8	O				
					EQEP1_B	9	I				
					XBAROUT14	10	O				
P2	U2	P3	T1	GPIO121 GPIO121_CFG_REG 0x5310 01E4 0x0000 05F7	EXT_REFCLK0	0	I	Mode7	3.3 V	GENERAL	LVCMOS
					SAFETY_ERRORn	1	IO				
					USB0_DRVVBUS	2	O				
					PR0_IEP0_EDIO_DATA_IN_OUT30	3	IO				
					GPMC0_A18	6	O				
					GPIO121	7	IO				
					EQEP1_INDEX	9	IO				
					XBAROUT15	10	O				
					DTB_OUT_14	15	O				

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ Address[15]/ Default Value [16]	Signal Name [3]	Mux Mode [4]	Signal Type [5]	MUX Mode after Reset [7]	IO Voltage [9]	Power [10]	Buffer Type [13]
B16	B19	C15		GPIO122 GPIO122_CFG_REG 0x5310 01E8 0x0000 05F7	CLKOUT1	0	O	Mode7	3.3 V	GENERAL	LVCMOS
					PR1_PRU0_GPIO7	1	IO				
					UART2_RTSn	2	O				
					PSM_CLKOUT	3	O				
					PR1_UART0_CTSn	4	I				
					GPMC0_A5	6	O				
					GPIO122	7	IO				
					SDFM0_CLK0	8	I				
					EQEP1_STROBE	9	IO				
D14	C16	A15		GPIO123 GPIO123_CFG_REG 0x5310 01EC 0x0000 05F7	PR0_ECAP0_APWM_OUT	0	O	Mode7	3.3 V	GENERAL	LVCMOS
					PR1_PRU1_GPIO10	1	IO				
					UART2_CTSn	2	I				
					PR1_ECAP0_APWM_OUT	3	O				
					PR1_UART0_RTSn	4	O				
					GPMC0_AD10	6	IO				
					GPIO123	7	IO				
					SDFM0_D0	8	I				
A16	A19	C16		GPIO124 GPIO124_CFG_REG 0x5310 01F0 0x0000 05F7	PR0_PRU1_GPIO7	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					CPTS0_TS_SYNC	1	O				
					PR1_PRU0_GPIO10	2	IO				
					PR0_IEP0_EDC_SYNC_OUT1	3	O				
					PR1_UART0_RXD	4	I				
					GPMC0_A8	6	O				
					GPIO124	7	IO				
					SDFM0_CLK1	8	I				
					SDFM1_D0	9	I				
					UART2_TXD	10	O				
					UART5_RTSn	11	O				
D13	B17	C14		GPIO125 GPIO125_CFG_REG 0x5310 01F4 0x0000 05F7	PR0_PRU1_GPIO17	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					PR1_PRU1_GPIO13	1	IO				
					UART2_RXD	2	I				
					PR0_IEP0_EDIO_DATA_IN_OUT30	3	IO				
					PR1_UART0_TXD	4	O				
					UART5_CTSn	5	I				
					GPMC0_AD13	6	IO				
					GPIO125	7	IO				
					SDFM0_D1	8	I				

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Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ Address[15]/ Default Value [16]	Signal Name [3]	Mux Mode [4]	Signal Type [5]	MUX Mode after Reset [7]	IO Voltage [9]	Power [10]	Buffer Type [13]
B15	A18	B16	A17	GPIO126 GPIO126_CFG_REG 0x5310 01F8 0x0000 05F7	UART1_CTSn	0	I	Mode7	3.3 V	GENERAL	LVCMOS
					PR1_MDIO0_MDIO	1	IO				
					SPI2_CS1	2	IO				
					PR1_IEP0_EDC_SYNC_OUT1	3	O				
					UART5_CTSn	4	I				
					UART5_TXD	5	O				
					GPMC0_CLKLB	6	IO				
					GPIO126	7	IO				
					SDFM0_CLK2	8	I				
					SDFM1_D1	9	I				
					ADC_EXTCH_XBAROUT8	10	O				
C13	A17	A14	A16	GPIO127 GPIO127_CFG_REG 0x5310 01FC 0x0000 05F7	UART2_CTSn	0	I	Mode7	3.3 V	GENERAL	LVCMOS
					PR1_MDIO0_MDC	1	O				
					SPI3_CS1	2	IO				
					UART5_RXD	5	I				
					GPMC0_BE0n_CLE	6	O				
					GPIO127	7	IO				
					SDFM0_D2	8	I				
					ADC_EXTCH_XBAROUT0	10	O				
A15	B18	B15		GPIO128 GPIO128_CFG_REG 0x5310 0200 0x0000 05F7	SPI2_D1	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					PR1_PRU1_GPIO14	1	IO				
					UART5_RXD	5	I				
					GPMC0_AD14	6	IO				
					GPIO128	7	IO				
					SDFM0_CLK3	8	I				
					SDFM1_D2	9	I				
					ADC_EXTCH_XBAROUT9	10	O				
C14	D17	B14		GPIO129 GPIO129_CFG_REG 0x5310 0204 0x0000 05F7	SPI2_CLK	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					PR1_PRU1_GPIO17	1	IO				
					UART5_TXD	5	O				
					GPMC0_WEn	6	O				
					GPIO129	7	IO				
					SDFM0_D3	8	I				
					ADC_EXTCH_XBAROUT1	10	O				

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ Address[15]/ Default Value [16]	Signal Name [3]	Mux Mode [4]	Signal Type [5]	MUX Mode after Reset [7]	IO Voltage [9]	Power [10]	Buffer Type [13]
B14	A16	D13	B15	GPIO130 GPIO130_CFG_REG 0x5310 0208 0x0000 05F7	SPI2_D0	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					PR1_PRU1_GPIO18	1	IO				
					UART4_RTSn	2	O				
					PR1_IEP0_EDC_SYNC_OUT0	3	O				
					I2C1_SDA	4	IO				
					MCAN1_RX	5	I				
					GPMC0_OEn_REn	6	O				
					GPIO130	7	IO				
					EQEP0_A	8	I				
					SDFM1_CLK0	9	I				
A14	B16	C13	A15	GPIO131 GPIO131_CFG_REG 0x5310 020C 0x0000 05F7	SPI2_CS0	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					PR1_PRU0_GPIO19	1	IO				
					UART4_CTSn	2	I				
					PR1_IEP0_EDIO_DATA_IN_OUT31	3	IO				
					I2C1_SCL	4	IO				
					MCAN1_TX	5	O				
					GPMC0_CSn0	6	O				
					GPIO131	7	IO				
					EQEP0_B	8	I				
					SDFM1_D0	9	I				
C12	C14	C12	A14	GPIO132 GPIO132_CFG_REG 0x5310 0210 0x0000 05F7	I2C2_SDA	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					PR1_PRU0_GPIO20	1	IO				
					UART4_TXD	2	O				
					PR1_IEP0_EDIO_DATA_IN_OUT30	3	IO				
					GPMC0_A15	6	O				
					GPIO132	7	IO				
					EQEP0_STROBE	8	IO				
					SDFM1_CLK1	9	I				
					ADC_EXTCH_XBAROUT2	10	O				
D11	D15	B13	B14	GPIO133 GPIO133_CFG_REG 0x5310 0214 0x0000 05F7	I2C2_SCL	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					PR1_PRU1_GPIO7	1	IO				
					UART4_RXD	2	I				
					GPMC0_AD7	6	IO				
					GPIO133	7	IO				
					EQEP0_INDEX	8	IO				
					SDFM1_D1	9	I				
					ADC_EXTCH_XBAROUT3	10	O				

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Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ Address[15]/ Default Value [16]	Signal Name [3]	Mux Mode [4]	Signal Type [5]	MUX Mode after Reset [7]	IO Voltage [9]	Power [10]	Buffer Type [13]
B13	B15	B12	B13	GPIO134 GPIO134_CFG_REG 0x5310 0218 0x0000 05F7	I2C0_SDA	0	IO	Mode7	3.3 V	GENERAL	I2C OPEN DRAIN
					GPIO134	7	IO				
					SDFM1_CLK2	9	I				
A13	A15	A13	A13	GPIO135 GPIO135_CFG_REG 0x5310 021C 0x0000 05F7	I2C0_SCL	0	IO	Mode7	3.3 V	GENERAL	I2C OPEN DRAIN
					GPIO135	7	IO				
					SDFM1_CLK3	9	I				
B12	B14			GPIO136 GPIO136_CFG_REG 0x5310 0220 0x0000 05F7	UART1_RTSn	0	O	Mode7	3.3 V	GENERAL	LVCMOS
					SPI0_CS1	1	IO				
					LIN0_RXD	2	IO				
					UART3_RXD	3	I				
					GPIO136	7	IO				
					SDFM1_D2	9	I				
A12	A14			GPIO137 GPIO137_CFG_REG 0x5310 0224 0x0000 05F7	UART2_RTSn	0	O	Mode7	3.3 V	GENERAL	LVCMOS
					EQEP1_INDEX	1	IO				
					LIN0_TXD	2	IO				
					UART3_TXD	3	O				
					GPIO137	7	IO				
					SDFM1_D3	9	I				
M2	M1	H1	J3	GPIO138 GPIO138_CFG_REG 0x5310 0228 0x0000 0570	CLKOUT0	0	O	Mode0	1.8 V/3.3 V	FLASH0	LVCMOS
					LIN1_RXD	1	IO				
					OSPI0_ECC_FAIL	2	I				
					UART1_RXD	3	I				
					SPI2_CS0	4	IO				
					OSPI1_ECC_FAIL	5	I				
					USB0_DRVVBUS	6	O				
					GPIO138	7	IO				
					SAFETY_ERRORn	8	IO				
V2	V1	R1	V1	GPIO139 GPIO139_CFG_REG 0x5310 022C 0x00 0060	USB0_DP	0	IO	Mode0 (see comment)	3.3 V	GENERAL	Analog
					UART5_RXD	1	I				
					GPIO139	7	IO				
U3	W1	P1	U1	GPIO140 GPIO140_CFG_REG 0x5310 0230 0x00 0060	USB0_DM	0	IO	Mode0 (see comment)	3.3 V	GENERAL	Analog
					UART5_TXD	1	O				
					GPIO140	7	IO				

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ Address[15]/ Default Value [16]	Signal Name [3]	Mux Mode [4]	Signal Type [5]	MUX Mode after Reset [7]	IO Voltage [9]	Power [10]	Buffer Type [13]
B9	B11	D8	B10	GPIO20 GPIO20_CFG_REG 0x5310 0050 0x0000 05F7	LIN1_TXD	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					OSPI0_RESET_OUT0	1	O				
					SPI2_CLK	2	IO				
					PR1_PRU1_GPIO8	3	IO				
					OSPI1_RESET_OUT0	4	O				
					UART1_TXD	5	O				
					GPMC0_AD8	6	IO				
					GPIO20	7	IO				
					XBAROUT6	10	O				
					EPWM6_A	11	O				
B8	B10	B8	A10	GPIO21 GPIO21_CFG_REG 0x5310 0054 0x0000 05F7	LIN2_RXD	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					UART2_RXD	1	I				
					SPI2_D0	2	IO				
					USB0_DRVVBUS	3	O				
					OSPI1_RESET_OUT1	4	O				
					OSPI0_RESET_OUT1	5	O				
					GPIO21	7	IO				
					GPMC0_CSn0	8	O				
A8	A10	C9	B9	GPIO22 GPIO22_CFG_REG 0x5310 0058 0x0000 05F7	LIN2_TXD	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					UART2_TXD	1	O				
					SPI2_D1	2	IO				
					GPIO22	7	IO				
					GPMC0_ADVn_ALE	8	O				
D7	B9	B7		GPIO23 GPIO23_CFG_REG 0x5310 005C 0x0000 05F7	I2C1_SCL	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					SPI3_CS0	2	IO				
					PR1_PRU0_GPIO17	3	IO				
					GPMC0_WEn	6	O				
					GPIO23	7	IO				
					XBAROUT7	10	O				
C8	A9	A8		GPIO24 GPIO24_CFG_REG 0x5310 0060 0x0000 05F7	I2C1_SDA	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					SPI3_CLK	2	IO				
					PR1_PRU0_GPIO18	3	IO				
					GPMC0_OEn_REn	6	O				
					GPIO24	7	IO				
					XBAROUT8	10	O				

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Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ Address[15]/ Default Value [16]	Signal Name [3]	Mux Mode [4]	Signal Type [5]	MUX Mode after Reset [7]	IO Voltage [9]	Power [10]	Buffer Type [13]
C7	C7	C8	C9	GPIO25 GPIO25_CFG_REG 0x5310 0064 0x0000 05F7	UART0_RTSn	0	O	Mode7	3.3 V	GENERAL	LVCMOS
					I2C2_SCL	1	IO				
					SPI3_D0	2	IO				
					PR1_PRU1_GPIO19	3	IO				
					PR1_PRU0_GPIO17	4	IO				
					UART3_RXD	5	I				
					GPMC0_WAIT1	6	I				
					GPIO25	7	IO				
					XBAROUT9	10	O				
					DTB_OUT_8	15	O				
B7	D8	A7	A9	GPIO26 GPIO26_CFG_REG 0x5310 0068 0x0000 05F7	UART0_CTSn	0	I	Mode7	3.3 V	GENERAL	LVCMOS
					I2C2_SDA	1	IO				
					SPI3_D1	2	IO				
					SPI0_CS1	3	IO				
					PR1_PRU0_GPIO7	4	IO				
					UART3_TXD	5	O				
					GPIO26	7	IO				
					XBAROUT10	10	O				
A7	A8	A6	A8	GPIO27 GPIO27_CFG_REG 0x5310 006C 0x0000 05F7	UART0_RXD	0	I	Mode7	3.3 V	GENERAL	LVCMOS
					LIN0_RXD	1	IO				
					GPIO27	7	IO				
					XBAROUT4	10	O				
					DTB_INOUT_6	15	IO				
A6	B8	B6	B8	GPIO28 GPIO28_CFG_REG 0x5310 0070 0x0000 05F7	UART0_TXD	0	O	Mode7	3.3 V	GENERAL	LVCMOS
					LIN0_TXD	1	IO				
					GPIO28	7	IO				
					XBAROUT5	10	O				
					DTB_INOUT_7	15	IO				
R17	W20	P16	V19	GPIO29 GPIO29_CFG_REG 0x5310 0074 0x0000 05F7	RGMII1_RXC	0	I	Mode7	1.8 V/3.3 V	FLASH1	LVCMOS
					RMII1_REF_CLK	1	IO				
					MII1_RXCLK	2	I				
					OSPI1_CLK	3	O				
					FSITX0_CLK	6	O				
					GPIO29	7	IO				

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ Address[15]/ Default Value [16]	Signal Name [3]	Mux Mode [4]	Signal Type [5]	MUX Mode after Reset [7]	IO Voltage [9]	Power [10]	Buffer Type [13]
R18	V19	M14	U17	GPIO30 GPIO30_CFG_REG 0x5310 0078 0x0000 05F7	RGMII1_RX_CTL	0	I	Mode7	1.8 V/3.3 V	FLASH1	LVCMOS
					RMII1_RX_ER	1	I				
					MII1_RXDV	2	I				
					OSPI1_D0	3	IO				
					FSITX0_DATA0	6	O				
					GPIO30	7	IO				
U17	Y18	P14	W17	GPIO31 GPIO31_CFG_REG 0x5310 007C 0x0000 05F7	RGMII1_RD0	0	I	Mode7	1.8 V/3.3 V	FLASH1	LVCMOS
					RMII1_RXD0	1	I				
					MII1_RXD0	2	I				
					OSPI1_D1	3	IO				
					FSITX0_DATA1	6	O				
					GPIO31	7	IO				
T17	W18	P15	V17	GPIO32 GPIO32_CFG_REG 0x5310 0080 0x0000 05F7	RGMII1_RD1	0	I	Mode7	1.8 V/3.3 V	FLASH1	LVCMOS
					RMII1_RXD1	1	I				
					MII1_RXD1	2	I				
					OSPI1_D2	3	IO				
					FSIRX0_CLK	6	I				
					GPIO32	7	IO				
U18	Y19	R16	W18	GPIO33 GPIO33_CFG_REG 0x5310 0084 0x0000 05F7	RGMII1_RD2	0	I	Mode7	1.8 V/3.3 V	FLASH1	LVCMOS
					PR1_IEP0_EDC_SYNC_OUT0	1	O				
					MII1_RXD2	2	I				
					OSPI1_D3	3	IO				
					UART1_RXD	4	I				
					FSIRX0_DATA0	6	I				
					GPIO33	7	IO				
					EQEP0_A	8	I				
					GPMC0_CSn2	9	O				
T18	W19	N14	V18	GPIO34 GPIO34_CFG_REG 0x5310 0088 0x0000 05F7	RGMII1_RD3	0	I	Mode7	1.8 V/3.3 V	FLASH1	LVCMOS
					PR1_IEP0_EDIO_DATA_IN_OUT31	1	IO				
					MII1_RXD3	2	I				
					OSPI1_D4	3	IO				
					UART1_TXD	4	O				
					FSIRX0_DATA1	6	I				
					GPIO34	7	IO				
					EQEP0_B	8	I				
					GPMC0_CSn3	9	O				

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Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ Address[15]/ Default Value [16]	Signal Name [3]	Mux Mode [4]	Signal Type [5]	MUX Mode after Reset [7]	IO Voltage [9]	Power [10]	Buffer Type [13]
N18	U20	L15	R18	GPIO35 GPIO35_CFG_REG 0x5310 008C 0x0000 05F7	RGMII1_TXC	0	O	Mode7	1.8 V/3.3 V	FLASH1	LVCMOS
					PR1_IEP0_EDIO_DATA_IN_OUT30	1	IO				
					MII1_TXCLK	2	I				
					OSPI1_D5	3	IO				
					UART4_RXD	4	I				
					GPIO35	7	IO				
					EQEP0_INDEX	8	IO				
M18	T20	M16	T19	GPIO36 GPIO36_CFG_REG 0x5310 0090 0x0000 05F7	RGMII1_TX_CTL	0	O	Mode7	1.8 V/3.3 V	FLASH1	LVCMOS
					RMII1_TX_EN	1	O				
					MII1_TX_EN	2	O				
					OSPI1_D6	3	IO				
					GPIO36	7	IO				
					EQEP0_STROBE	8	IO				
P16	V18	N15	U18	GPIO37 GPIO37_CFG_REG 0x5310 0094 0x0000 05F7	RGMII1_TD0	0	O	Mode7	1.8 V/3.3 V	FLASH1	LVCMOS
					RMII1_TXD0	1	O				
					MII1_TXD0	2	O				
					OSPI1_D7	3	IO				
					GPIO37	7	IO				
					EQEP1_A	8	I				
P17	V20	N16	U19	GPIO38 GPIO38_CFG_REG 0x5310 0098 0x0000 05F7	RGMII1_TD1	0	O	Mode7	1.8 V/3.3 V	FLASH1	LVCMOS
					RMII1_TXD1	1	O				
					MII1_TXD1	2	O				
					OSPI1_CSn0	3	O				
					GPIO38	7	IO				
					EQEP1_B	8	I				
P18	U19	L13	R17	GPIO39 GPIO39_CFG_REG 0x5310 009C 0x0000 05F7	RGMII1_TD2	0	O	Mode7	1.8 V/3.3 V	FLASH1	LVCMOS
					RMII1_CRS_DV	1	I				
					MII1_TXD2	2	O				
					OSPI1_DQS	3	I				
					GPIO39	7	IO				
					EQEP1_STROBE	8	IO				

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ Address[15]/ Default Value [16]	Signal Name [3]	Mux Mode [4]	Signal Type [5]	MUX Mode after Reset [7]	IO Voltage [9]	Power [10]	Buffer Type [13]
N17	T19	M15	T18	GPIO40 GPIO40_CFG_REG 0x5310 00A0 0x0000 05F7	RGMII1_TD3	0	O	Mode7	1.8 V/3.3 V	FLASH1	LVCMOS
					PR0_PRU0_GPIO7	1	IO				
					MII1_TXD3	2	O				
					OSPI1_ECC_FAIL	3	I				
					UART4_TXD	4	O				
					PR0_IEP0_EDC_SYNC_OUT1	5	O				
					PR1_IEP0_EDC_SYNC_OUT1	6	O				
					GPIO40	7	IO				
					EQEP1_INDEX	8	IO				
N16	R17	L16	P18	GPIO41 GPIO41_CFG_REG 0x5310 00A4 0x0000 05F7	MDIO0_MDIO	0	IO	Mode7	1.8 V/3.3 V	FLASH1	LVCMOS
					MCAN1_RX	1	I				
					OSPI1_RESET_OUT0	3	O				
					GPIO41	7	IO				
M17	T18	L14	R19	GPIO42 GPIO42_CFG_REG 0x5310 00A8 0x0000 05F7	MDIO0_MDC	0	O	Mode7	3.3 V	GENERAL	LVCMOS
					MCAN1_TX	1	O				
					GPIO42	7	IO				
B2	B3	A4	B5	GPIO43 GPIO43_CFG_REG 0x5310 00AC 0x0000 05F7	EPWM0_A	0	O	Mode7	3.3 V	GENERAL	LVCMOS
					PR1_PRU0_GPIO5	2	IO				
					GPMC0_A3	6	O				
					GPIO43	7	IO				
					EPWM0_A	10	O				
B1	C3	A5	A6	GPIO44 GPIO44_CFG_REG 0x5310 00B0 0x0000 05F7	EPWM0_B	0	O	Mode7	3.3 V	GENERAL	LVCMOS
					PR1_PRU0_GPIO8	2	IO				
					GPMC0_A6	6	O				
					GPIO44	7	IO				
					EPWM0_B	10	O				
D3	A2	B4	A5	GPIO45 GPIO45_CFG_REG 0x5310 00B4 0x0000 05F7	EPWM1_A	0	O	Mode7	3.3 V	GENERAL	LVCMOS
					PR1_PRU0_GPIO6	2	IO				
					GPMC0_A4	6	O				
					GPIO45	7	IO				
					EPWM1_A	10	O				
D2	A3	C5	A4	GPIO46 GPIO46_CFG_REG 0x5310 00B8 0x0000 05F7	EPWM1_B	0	O	Mode7	3.3 V	GENERAL	LVCMOS
					PR1_PRU0_GPIO4	2	IO				
					GPMC0_A2	6	O				
					GPIO46	7	IO				
					EPWM4_B	10	O				

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Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ Address[15]/ Default Value [16]	Signal Name [3]	Mux Mode [4]	Signal Type [5]	MUX Mode after Reset [7]	IO Voltage [9]	Power [10]	Buffer Type [13]
C2	B1	A3	A3	GPIO47 GPIO47_CFG_REG 0x5310 00BC 0x0000 05F7	EPWM2_A	0	O	Mode7	3.3 V	GENERAL	LVCMOS
					PR1_PRU0_GPIO3	2	IO				
					GPMC0_A1	6	O				
					GPIO47	7	IO				
					EPWM2_A	10	O				
C1	B2	A2	B4	GPIO48 GPIO48_CFG_REG 0x5310 00C0 0x0000 05F7	EPWM2_B	0	O	Mode7	3.3 V	GENERAL	LVCMOS
					PR1_PRU0_GPIO16	2	IO				
					PR1_PRU0_GPIO7	4	IO				
					GPMC0_A14	6	O				
					GPIO48	7	IO				
					EPWM2_B	10	O				
E2	C1	B2	A2	GPIO49 GPIO49_CFG_REG 0x5310 00C4 0x0000 05F7	EPWM3_A	0	O	Mode7	3.3 V	GENERAL	LVCMOS
					PR1_PRU0_GPIO15	2	IO				
					GPMC0_A13	6	O				
					GPIO49	7	IO				
					EPWM3_A	10	O				
E3	C2	C4	B2	GPIO50 GPIO50_CFG_REG 0x5310 00C8 0x0000 05F7	EPWM3_B	0	O	Mode7	3.3 V	GENERAL	LVCMOS
					PR1_PRU0_GPIO11	2	IO				
					GPMC0_A9	6	O				
					GPIO50	7	IO				
					EPWM6_A	10	O				
D1	D2	B1	B1	GPIO51 GPIO51_CFG_REG 0x5310 00CC 0x0000 05F7	EPWM4_A	0	O	Mode7	3.3 V	GENERAL	LVCMOS
					PR1_PRU0_GPIO12	2	IO				
					GPMC0_A10	6	O				
					GPIO51	7	IO				
					EPWM4_A	10	O				
E4	D1	C1	B3	GPIO52 GPIO52_CFG_REG 0x5310 00D0 0x0000 05F7	EPWM4_B	0	O	Mode7	3.3 V	GENERAL	LVCMOS
					PR1_PRU0_GPIO13	2	IO				
					GPMC0_A11	6	O				
					GPIO52	7	IO				
					EPWM1_B	10	O				
F2	E2	C2	C2	GPIO53 GPIO53_CFG_REG 0x5310 00D4 0x0000 05F7	EPWM5_A	0	O	Mode7	3.3 V	GENERAL	LVCMOS
					PR1_PRU0_GPIO14	2	IO				
					GPMC0_A12	6	O				
					GPIO53	7	IO				
					EPWM5_A	10	O				

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ Address[15]/ Default Value [16]	Signal Name [3]	Mux Mode [4]	Signal Type [5]	MUX Mode after Reset [7]	IO Voltage [9]	Power [10]	Buffer Type [13]
G2	E1	D3	C1	GPIO54 GPIO54_CFG_REG 0x5310 00D8 0x0000 05F7	EPWM5_B	0	O	Mode7	3.3 V	GENERAL	LVCMOS
					PR1_PRU1_GPIO5	2	IO				
					OSPI0_RESET_OUT0	3	O				
					GPMC0_AD5	6	IO				
					GPIO54	7	IO				
					EPWM8_B	10	O				
E1	F2	E3	E3	GPIO55 GPIO55_CFG_REG 0x5310 00DC 0x0000 05F7	EPWM6_A	0	O	Mode7	3.3 V	GENERAL	LVCMOS
					PR1_PRU1_GPIO8	1	IO				
					CLKOUT0	2	O				
					GPMC0_AD8	6	IO				
					GPIO55	7	IO				
					EPWM3_B	10	O				
F3	F1	F4	E2	GPIO56 GPIO56_CFG_REG 0x5310 00E0 0x0000 05F7	EPWM6_B	0	O	Mode7	3.3 V	GENERAL	LVCMOS
					PR1_PRU1_GPIO6	1	IO				
					UART2_RTSn	3	O				
					GPMC0_A20	6	O				
					GPIO56	7	IO				
					EPWM6_B	10	O				
F4	G2	D2	D2	GPIO57 GPIO57_CFG_REG 0x5310 00E4 0x0000 05F7	EPWM7_A	0	O	Mode7	1.8 V/3.3 V	FLASH0	LVCMOS
					PR1_PRU1_GPIO4	1	IO				
					OSPI0_CSn1	2	O				
					OSPI1_CSn1	5	O				
					GPMC0_AD4	6	IO				
					GPIO57	7	IO				
					EPWM7_A	10	O				
F1	G1	D1	D1	GPIO58 GPIO58_CFG_REG 0x5310 00E8 0x0000 05F7	EPWM7_B	0	O	Mode7	1.8 V/3.3 V	FLASH0	LVCMOS
					PR1_PRU1_GPIO3	1	IO				
					OSPI1_D1	2	IO				
					OSPI0_D1	5	IO				
					GPMC0_AD3	6	IO				
					GPIO58	7	IO				
					EPWM5_B	10	O				

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Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ Address[15]/ Default Value [16]	Signal Name [3]	Mux Mode [4]	Signal Type [5]	MUX Mode after Reset [7]	IO Voltage [9]	Power [10]	Buffer Type [13]
G3	H2	E2	E1	GPIO59 GPIO59_CFG_REG 0x5310 00EC 0x0000 05F7	EPWM8_A	0	O	Mode7	1.8 V/3.3 V	FLASH0	LVCMOS
					PR1_PRU1_GPIO16	1	IO				
					OSPI1_D0	2	IO				
					MCAN0_RX	3	I				
					PR0_PRU1_GPIO7	4	IO				
					OSPI0_D0	5	IO				
					GPMC0_CSn1	6	O				
					GPIO59	7	IO				
					UART4_TXD	8	O				
					EPWM8_A	10	O				
H2	H1	E1	F1	GPIO60 GPIO60_CFG_REG 0x5310 00F0 0x0000 05F7	EPWM8_B	0	O	Mode7	1.8 V/3.3 V	FLASH0	LVCMOS
					PR1_PRU1_GPIO15	1	IO				
					OSPI1_CLK	2	O				
					MCAN0_TX	3	O				
					OSPI0_CLK	5	O				
					GPMC0_AD15	6	IO				
					GPIO60	7	IO				
					UART4_RXD	8	I				
					EPWM9_B	10	O				
G1	K4	F2	F2	GPIO61 GPIO61_CFG_REG 0x5310 00F4 0x0000 05F7	EPWM9_A	0	O	Mode7	1.8 V/3.3 V	FLASH0	LVCMOS
					LIN1_TXD	1	IO				
					OSPI0_RESET_OUT0	2	O				
					SPI2_CLK	3	IO				
					UART1_TXD	4	O				
					OSPI1_RESET_OUT0	5	O				
					GPIO61	7	IO				
					EPWM9_A	10	O				
J2	L2	F3	G1	GPIO62 GPIO62_CFG_REG 0x5310 00F8 0x0000 05F7	EPWM9_B	0	O	Mode7	1.8 V/3.3 V	FLASH0	LVCMOS
					LIN1_RXD	1	IO				
					OSPI0_CSn0	2	O				
					UART1_RTSn	3	O				
					OSPI1_CSn0	5	O				
					GPIO62	7	IO				

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ Address[15]/ Default Value [16]	Signal Name [3]	Mux Mode [4]	Signal Type [5]	MUX Mode after Reset [7]	IO Voltage [9]	Power [10]	Buffer Type [13]
G4	J2			GPIO63 GPIO63_CFG_REG 0x5310 00FC 0x0000 05F7	LIN0_RXD	0	IO	Mode7	1.8 V/3.3 V	FLASH0	LVCMOS
					UART1_CTSn	1	I				
					I2C0_SDA	3	IO				
					UART2_TXD	4	O				
					GPIO63	7	IO				
					EPWM7_B	10	O				
J3	J1			GPIO64 GPIO64_CFG_REG 0x5310 0100 0x0000 05F7	LIN0_TXD	0	IO	Mode7	1.8 V/3.3 V	FLASH0	LVCMOS
					UART2_RTSn	1	O				
					OSPI0_RESET_OUT0	2	O				
					I2C0_SCL	3	IO				
					UART4_TXD	4	O				
					GPIO64	7	IO				
H1	J3			GPIO65 GPIO65_CFG_REG 0x5310 0104 0x0000 05F7	OSPI0_ECC_FAIL	0	I	Mode7	1.8 V/3.3 V	FLASH0	LVCMOS
					UART2_CTSn	1	I				
					OSPI0_RESET_OUT1	2	O				
					I2C1_SDA	3	IO				
					UART4_RXD	4	I				
					OSPI0_CSn0	6	O				
					GPIO65	7	IO				
J1	K2	G3		GPIO66 GPIO66_CFG_REG 0x5310 0108 0x0000 05F7	OSPI0_RESET_OUT0	0	O	Mode7	1.8 V/3.3 V	FLASH0	LVCMOS
					UART3_RTSn	1	O				
					I2C1_SCL	3	IO				
					UART2_RXD	4	I				
					OSPI0_D1	6	IO				
					GPIO66	7	IO				
K2	K1	G2	G2	GPIO67 GPIO67_CFG_REG 0x5310 010C 0x0000 05F7	PR1_PRU0_GPIO0	0	IO	Mode7	1.8 V/3.3 V	FLASH0	LVCMOS
					OSPI0_D5	2	IO				
					UART3_CTSn	3	I				
					GPIO67	7	IO				
J4	L4	H3	H1	GPIO68 GPIO68_CFG_REG 0x5310 0110 0x0000 05F7	PR1_PRU0_GPIO1	0	IO	Mode7	1.8 V/3.3 V	FLASH0	LVCMOS
					OSPI0_D7	2	IO				
					UART1_DCDn	3	I				
					GPIO68	7	IO				
K4	L1	H2	H2	GPIO69 GPIO69_CFG_REG 0x5310 0114 0x0000 05F7	PR1_PRU0_GPIO2	0	IO	Mode7	1.8 V/3.3 V	FLASH0	LVCMOS
					OSPI0_D3	2	IO				
					UART1_RIn	3	I				
					GPIO69	7	IO				

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Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ Address[15]/ Default Value [16]	Signal Name [3]	Mux Mode [4]	Signal Type [5]	MUX Mode after Reset [7]	IO Voltage [9]	Power [10]	Buffer Type [13]
K3	M2	G1	J1	GPIO70 GPIO70_CFG_REG 0x5310 0118 0x0000 05F7	PR1_PRU0_GPIO9	0	IO	Mode7	1.8 V/3.3 V	FLASH0	LVCMOS
					OSPI0_D1	2	IO				
					UART1_DTRn	3	O				
					UART3_CTSn	4	I				
					OSPI1_D1	5	IO				
					OSPI0_ECC_FAIL	6	I				
					GPIO70	7	IO				
V17	W16	R14	V15	GPIO71 GPIO71_CFG_REG 0x5310 011C 0x0000 05F7	PR1_PRU1_GPIO0	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					UART1_DSRn	1	I				
					UART4_RTSn	3	O				
					GPMC0_AD0	6	IO				
					GPIO71	7	IO				
T16	Y16	T14	W15	GPIO72 GPIO72_CFG_REG 0x5310 0120 0x0000 05F7	PR1_PRU1_GPIO1	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					MII1_RX_ER	2	I				
					UART4_CTSn	3	I				
					GPMC0_AD1	6	IO				
					GPIO72	7	IO				
P15	W17	T15	W16	GPIO73 GPIO73_CFG_REG 0x5310 0124 0x0000 05F7	PR1_PRU1_GPIO2	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					MII1_COL	2	I				
					UART5_TXD	3	O				
					GPMC0_AD2	6	IO				
					GPIO73	7	IO				
					ADC_EXTCH_XBAROUT4	9	O				
R16	Y17	R15	V16	GPIO74 GPIO74_CFG_REG 0x5310 0128 0x0000 05F7	PR1_PRU1_GPIO9	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					MII1_CRS	2	I				
					UART5_RXD	3	I				
					GPMC0_AD9	6	IO				
					GPIO74	7	IO				
					ADC_EXTCH_XBAROUT5	9	O				
L3	T3	M1	L2	GPIO75 GPIO75_CFG_REG 0x5310 012C 0x0000 05F7	UART1_RXD	0	I	Mode7	3.3 V	GENERAL	LVCMOS
					OSPI0_LBCLKO	1	O				
					LIN1_RXD	4	IO				
					OSPI1_LBCLKO	5	O				
					GPMC0_CLK	6	IO				
					GPIO75	7	IO				

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ Address[15]/ Default Value [16]	Signal Name [3]	Mux Mode [4]	Signal Type [5]	MUX Mode after Reset [7]	IO Voltage [9]	Power [10]	Buffer Type [13]
M3	R4	L1	M1	GPIO76 GPIO76_CFG_REG 0x5310 0130 0x0000 05F7	UART1_TXD	0	O	Mode7	1.8 V/3.3 V	FLASH0	LVCMOS
					OSPI0_DQS	1	I				
					OSPI0_D4	2	IO				
					LIN1_TXD	4	IO				
					GPIO76	7	IO				
B6	B7			GPIO77 GPIO77_CFG_REG 0x5310 0134 0x0000 05F7	MMC0_CLK	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					UART0_RXD	1	I				
					LIN0_RXD	2	IO				
					MCAN0_RX	3	I				
					PR1_MDIO0_MDIO	4	IO				
					GPIO77	7	IO				
					SDFM1_CLK0	8	I				
A4	A6			GPIO78 GPIO78_CFG_REG 0x5310 0138 0x0000 05F7	MMC0_CMD	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					UART0_TXD	1	O				
					LIN0_TXD	2	IO				
					MCAN0_TX	3	O				
					PR1_MDIO0_MDC	4	O				
					GPIO78	7	IO				
					SDFM1_D0	8	I				
B5	B6			GPIO79 GPIO79_CFG_REG 0x5310 013C 0x0000 05F7	MMC0_D0	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					UART2_RXD	1	I				
					I2C1_SCL	2	IO				
					MCAN1_RX	3	I				
					PR1_PRU0_GPIO10	4	IO				
					GPIO79	7	IO				
					SDFM1_CLK1	8	I				
B4	A5			GPIO80 GPIO80_CFG_REG 0x5310 0140 0x0000 05F7	MMC0_D1	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					MCAN1_TX	3	O				
					PR1_PRU0_GPIO9	4	IO				
					GPIO80	7	IO				
					SDFM1_D1	8	I				
A3	B5			GPIO81 GPIO81_CFG_REG 0x5310 0144 0x0000 05F7	MMC0_D2	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					UART2_TXD	1	O				
					I2C1_SDA	2	IO				
					PR1_PRU0_GPIO0	4	IO				
					GPIO81	7	IO				
					SDFM1_CLK2	8	I				

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Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ Address[15]/ Default Value [16]	Signal Name [3]	Mux Mode [4]	Signal Type [5]	MUX Mode after Reset [7]	IO Voltage [9]	Power [10]	Buffer Type [13]
A2	A4			GPIO82 GPIO82_CFG_REG 0x5310 0148 0x0000 05F7	MMC0_D3	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					UART3_RTSn	1	O				
					PR1_PRU0_GPIO1	4	IO				
					GPIO82	7	IO				
					SDFM1_D2	8	I				
C6	B4			GPIO83 GPIO83_CFG_REG 0x5310 014C 0x0000 05F7	MMC0_WP	0	I	Mode7	3.3 V	GENERAL	LVCMOS
					UART0_RTSn	1	O				
					I2C2_SCL	2	IO				
					PR1_PRU0_GPIO2	4	IO				
					GPIO83	7	IO				
					SDFM1_CLK3	8	I				
A5	A7			GPIO84 GPIO84_CFG_REG 0x5310 0150 0x0000 05F7	MMC0_CD	0	I	Mode7	3.3 V	GENERAL	LVCMOS
					UART0_CTSn	1	I				
					I2C2_SDA	2	IO				
					GPIO84	7	IO				
					SDFM1_D3	8	I				
L17	R19	K15	N17	GPIO85 GPIO85_CFG_REG 0x5310 0154 0x0000 05F7	PR0_MDIO0_MDIO	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					LIN0_RXD	1	IO				
					MCAN0_RX	2	I				
					GPIO85	7	IO				
					XBAROUT14	10	O				
					DTB_OUT_10	15	O				
L18	R20	K16	P19	GPIO86 GPIO86_CFG_REG 0x5310 0158 0x0000 05F7	PR0_MDIO0_MDC	0	O	Mode7	3.3 V	GENERAL	LVCMOS
					LIN0_TXD	1	IO				
					MCAN0_TX	2	O				
					GPIO86	7	IO				
					XBAROUT15	10	O				
					DTB_OUT_11	15	O				
G17	K19	F14	G17	GPIO87 GPIO87_CFG_REG 0x5310 015C 0x0000 05F7	PR0_PRU0_GPIO5	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					UART3_RTSn	1	O				
					RMII2_RX_ER	2	I				
					MII2_RX_ER	4	I				
					GPIO87	7	IO				
					TRC_CTL	8	O				
					ADC_EXTCH_XBAROUT4	9	O				
					XBAROUT6	10	O				

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ Address[15]/ Default Value [16]	Signal Name [3]	Mux Mode [4]	Signal Type [5]	MUX Mode after Reset [7]	IO Voltage [9]	Power [10]	Buffer Type [13]
F17	J19	E15		GPIO88 GPIO88_CFG_REG 0x5310 0160 0x0000 05F7	PR0_PRU0_GPIO9	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					PR1_PRU0_GPIO9	1	IO				
					PR0_IEP0_EDC_SYNC_OUT1	2	O				
					PR0_UART0_CTSn	3	I				
					MII2_COL	4	I				
					GPIO88	7	IO				
G18	J20	E16	J18	GPIO89 GPIO89_CFG_REG 0x5310 0164 0x0000 05F7	PR0_PRU0_GPIO10	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					UART3_CTSn	1	I				
					RMII2_CRS_DV	2	I				
					PR0_UART0_RTSn	3	O				
					MII2_CRS	4	I				
					GPIO89	7	IO				
G15	J18	E14	G19	GPIO90 GPIO90_CFG_REG 0x5310 0168 0x0000 05F7	PR0_PRU0_GPIO8	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					I2C0_SDA	1	IO				
					GPIO90	7	IO				
K15	N20	H15	L18	GPIO91 GPIO91_CFG_REG 0x5310 016C 0x0000 05F7	PR0_PRU0_GPIO6	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					I2C0_SCL	1	IO				
					RMII2_REF_CLK	2	IO				
					RGMII2_RXC	3	I				
					MII2_RXCLK	4	I				
					GPIO91	7	IO				
K16	L20	G15	J19	GPIO92 GPIO92_CFG_REG 0x5310 0170 0x0000 05F7	PR0_PRU0_GPIO4	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					UART3_RXD	1	I				
					RGMII2_RX_CTL	3	I				
					MII2_RXDV	4	I				
					GPIO92	7	IO				
					TRC_CLK	8	O				
					ADC_EXTCH_XBAROUT5	9	O				
					XBAROUT7	10	O				

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Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ Address[15]/ Default Value [16]	Signal Name [3]	Mux Mode [4]	Signal Type [5]	MUX Mode after Reset [7]	IO Voltage [9]	Power [10]	Buffer Type [13]
K17	N17	K14	M18	GPIO93 GPIO93_CFG_REG 0x5310 0174 0x0000 05F7	PR0_PRU0_GPIO0	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					PR1_PRU0_GPIO0	1	IO				
					RMII2_RXD0	2	I				
					RGMII2_RD0	3	I				
					MII2_RXD0	4	I				
					GPIO93	7	IO				
					TRC_DATA0	8	O				
					ADC_EXTCH_XBAROUT6	9	O				
					XBAROUT8	10	O				
K18	N19	H14	L19	GPIO94 GPIO94_CFG_REG 0x5310 0178 0x0000 05F7	PR0_PRU0_GPIO1	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					PR1_PRU0_GPIO1	1	IO				
					RMII2_RXD1	2	I				
					RGMII2_RD1	3	I				
					MII2_RXD1	4	I				
					GPIO94	7	IO				
					TRC_DATA1	8	O				
					ADC_EXTCH_XBAROUT7	9	O				
					XBAROUT11	10	O				
J18	M18	G16	K19	GPIO95 GPIO95_CFG_REG 0x5310 017C 0x0000 05F7	PR0_PRU0_GPIO2	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					PR1_PRU0_GPIO2	1	IO				
					RGMII2_RD2	3	I				
					MII2_RXD2	4	I				
					GPIO95	7	IO				
					TRC_DATA2	8	O				
					ADC_EXTCH_XBAROUT8	9	O				
					XBAROUT12	10	O				
J17	M20	J14	L17	GPIO96 GPIO96_CFG_REG 0x5310 0180 0x0000 05F7	PR0_PRU0_GPIO3	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					UART3_TXD	1	O				
					RGMII2_RD3	3	I				
					MII2_RXD3	4	I				
					GPIO96	7	IO				
					TRC_DATA3	8	O				
					ADC_EXTCH_XBAROUT9	9	O				
					XBAROUT13	10	O				
					DTB_INOUT_0	15	IO				

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ Address[15]/ Default Value [16]	Signal Name [3]	Mux Mode [4]	Signal Type [5]	MUX Mode after Reset [7]	IO Voltage [9]	Power [10]	Buffer Type [13]
H18	M19	F16	K18	GPIO97 GPIO97_CFG_REG 0x5310 0184 0x0000 05F7	PR0_PRU0_GPIO16	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					RGMII2_TXC	3	O				
					MII2_TXCLK	4	I				
					GPIO97	7	IO				
L16	P18	H16	M19	GPIO98 GPIO98_CFG_REG 0x5310 0188 0x0000 05F7	PR0_PRU0_GPIO15	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					RMII2_TX_EN	2	O				
					RGMII2_TX_CTL	3	O				
					MII2_TX_EN	4	O				
					GPIO98	7	IO				
M16	P20	J15	N18	GPIO99 GPIO99_CFG_REG 0x5310 018C 0x0000 05F7	PR0_PRU0_GPIO11	0	IO	Mode7	3.3 V	GENERAL	LVCMOS
					RMII2_TXD0	2	O				
					RGMII2_TD0	3	O				
					MII2_TXD0	4	O				
					GPIO99	7	IO				
J15, R7, R9, T15, T7, U4, U5, U6, U7, U8, U9, V3, V4, V5, V6, V7, V8	U17			NC	NC	0	NC		NA	NC	-
R2	V3	P2	T2	PORz	PORz	0	I	Mode0	3.3 V	GENERAL	HHV
D4	E3	B3	C5	SAFETY_ERRORn SAFETY_ERRORn_CFG_REG 0x5310 0238 0x0000 0410	SAFETY_ERRORn	0	IO	Mode0	3.3 V	GENERAL	LVCMOS
B3	D4	C6	B6	TCK TCK_CFG_REG 0x5310 0248 0x0000 0210	TCK	0	I	Mode0	3.3 V	GENERAL	LVCMOS
C5	C5	D5	C7	TDI TDI_CFG_REG 0x5310 023C 0x0000 06D0	TDI	0	I	Mode0	3.3 V	GENERAL	LVCMOS
C4	E5	B5	A7	TDO TDO_CFG_REG 0x5310 0240 0x0000 0630	TDO	0	O	Mode0	3.3 V	GENERAL	LVCMOS
U1	W3	P5	W4	TEMPCAL	TEMPCAL		-		-	-	Analog
D5	D6	C7	B7	TMS TMS_CFG_REG 0x5310 0244 0x0000 0610	TMS	0	IO	Mode0	3.3 V	GENERAL	LVCMOS

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Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ Address[15]/ Default Value [16]	Signal Name [3]	Mux Mode [4]	Signal Type [5]	MUX Mode after Reset [7]	IO Voltage [9]	Power [10]	Buffer Type [13]
E11, E9, F11, F9, G13, G14, G5, G6, K13, K14, K5, K6, N13, N14, N5, N6	F12, F14, F7, F9, G15, G6, J15, J6, M15, M6, P15, P6, R7	E11, E5, E7, E9, F12, G5, H12, J5, K12, L5, M12, M6	E10, E12, E14, E6, E8, F15, F5, H15, H5, K15, K5, M15, M5, P15, P5, R15, R6, T6	VDD	VDD		Power		1.2V	Power	-
R11, R6, R8	U10, U11	N9	U9	VDDA18_LDO	VDDA18_LDO		Power		1.8V	Power	-
R4	U8	N6	U7	VDDA18_OSC_PLL	VDDA18_OSC_PLL		Power		1.8V	Power	-
					VDDA18_USB		Power				
	T5	N4	U3	VDDA18_USB	VDDA18_USB		Power		1.8V	Power	-
P11, P7, P9	T12, T9	M10, M8	T10, T12	VDDA33	VDDA33		Power		3.3V	Power	-
	P5	M4	R3	VDDA33_USB	VDDA33_USB		Power		3.3V	Power	-
D10	D13	D10	C11	VDDAR2	VDDAR2		Power		1.2V	Power	-
H3	H4	G4	G3	VDDAR3	VDDAR3		Power		1.2V	Power	-
D6, E15, L4, N15	E14, E9, F4, G16, L17, N4, T16	D12, D6, D9, E4, G13, K13, K4, N13	D10, D14, D6, H16, H4, L3, M16, T16	VDDS18	VDDS18		Power		1.8V	Power	-
T3	U6	P4	V4	VDDS18_LDO	VDDS18_LDO		Power		1.8V	Power	-
D12, D8, H15, H4, L15, P4, R15				VDDS33	VDDA33_USB		Power		3.3V	Power	-
					VDDS33		Power				
	E12, E16, E7, G5, J16, M16	D11, D4, D7, F13, J13	C15, D12, D8, F16, F4, K16	VDDSHV_A	VDDS33		Power		3.3V	Power	-
	M5	L4	P4	VDDSHV_B	VDDS33		Power		3.3V	Power	-
	T14	N12	T14	VDDSHV_C	VDDS33		Power		3.3V	Power	-
	J5	H4, J4	K4, M4	VDDSHV_D	VDDS1833_FLASH0		Power		1.8V/3.3V	FLASH0 IO Power Supply	-
	P16	M13	P16	VDDSHV_E	VDDS1833_FLASH1		Power		1.8V/3.3V	FLASH1 IO Power Supply	-
	T7	N5	U5	VDDSHV_F	VDDS33		Power		3.3V	Power	-
		F1, J1		VDDSHV_G	VDDS1833_FLASH0-SIP		Power		1.8V/3.3V	FLASH0-SIP IO Power Supply	-
T4	V7	N8	T8	VDD_TEMP	VDD_TEMP		Power		1.8V	Power	-
J16	K17	H13	J17	VNWA	VNWA		Power		1.2V	Power	-
N3	P3	K3	N3	VPP	VPP		Power		VPP	Power	-

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ Address[15]/ Default Value [16]	Signal Name [3]	Mux Mode [4]	Signal Type [5]	MUX Mode after Reset [7]	IO Voltage [9]	Power [10]	Buffer Type [13]
A1, A18, E10, E12, E13, E14, E5, E6, E7, E8, F10, F12, F13, F14, F5, F6, F7, F8, G10, G11, G12, G7, G8, G9, H10, H11, H12, H13, H14, H5, H6, H7, H8, H9, J10, J11, J12, J13, J14, J5, J6, J7, J8, J9, K10, K11, K12, K7, K8, K9, L10, L11, L12, L13, L14, L5, L6, L7, L8, L9, M10, M11, M12, M13, M14, M5, M6, M7, M8, M9, N10, N11, N12, N7, N8, N9, P13, P14, P5, T2, V18	A1, A20, F15, F6, G10, G11, G12, G13, G14, G7, G8, G9, H10, H11, H12, H13, H14, H7, H8, H9, J10, J11, J12, J13, J14, J7, J8, J9, K10, K11, K12, K13, K14, K7, K8, K9, L10, L11, L12, L13, L14, L7, L8, L9, M10, M11, M12, M13, M14, M7, M8, M9, N10, N11, N12, N13, N14, N7, N8, N9, P10, P11, P12, P13, P14, P7, P8, P9, R14, R15, R6, V2, V5, W2, Y1, Y20	A1, A16, E10, E12, E6, E8, F10, F11, F5, F6, F7, F8, F9, G10, G11, G12, G6, G7, G8, G9, H10, H11, H5, H6, H7, H8, H9, J10, J11, J12, J9, K10, K11, K5, K6, K7, K8, K9, L10, L11, L12, L6, L7, L8, L9, M5, M7, R2, R3, R4, T1, T16	A1, A19, D16, D4, E15, E5, F10, F11, F12, F13, F14, F6, F7, F8, F9, G10, G11, G12, G13, G14, G6, G7, G8, G9, H10, H11, H12, H13, H14, H6, H7, H8, H9, J10, J11, J12, J13, J14, J6, J7, J8, J9, K10, K11, K12, K13, K14, K6, K7, K8, K9, L10, L11, L12, L13, L14, L6, L7, L8, L9, M10, M11, M12, M13, M14, M6, M7, M8, M9, N10, N11, N12, N13, N14, N6, N7, N8, N9, P10, P11, P12, P13, P14, P6, P7, P8, P9, R14, R5, R8, T4, U2, V2, V3, W1, W19	VSS	VSS		GND		VSS	GND	-
P10, P12, P6, P8, R13, R5, V1, V16	R12, R9	M11, M9	R10, R12	VSSA	VSSA		AGND		VSSA	AGND	-
U2	Y4	R5	V5	VSYS_MON	VSYS_MON		-		-	-	Analog
C3	G3	C3	C3	WARMRSTn WARMRSTn_CFG_REG 0x5310 0234 0x0000 0510	WARMRSTn	0	IO	Mode0	3.3 V	GENERAL	FS_OPEN_DRAIN
T1	Y3	T3	W3	XTAL_XI	XTAL_XI	0	I	Mode0	1.8V	OSC	OSC
R1	Y2	T2	W2	XTAL_XO	XTAL_XO	0	O	Mode0	1.8V	OSC	OSC

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5.3 Signal Descriptions

Many signals are available on multiple pins, according to the software configuration of the pin multiplexing options.

The following list describes the column headers:

1. **SIGNAL NAME:** The name of the signal passing through the pin.

Note

Signal names and descriptions provided in each Signal Descriptions table, represent the pin multiplexed signal function which is implemented at the pin and selected via IOMUX pad configuration registers. Some device subsystems provide secondary multiplexing of signal functions, which are not described in these tables. For more information on secondary multiplexed signal functions, see the respective peripheral chapter of the device TRM.

2. **PIN TYPE:** Signal direction and type:
   - I = Input
   - O = Output
   - IO = Input, Output, or simultaneously Input and Output
   - ID = Input with open-drain output function
   - OD = Output, with open-drain output function
   - IOD = Input, Output, or simultaneously Input and Output, with open-drain output function
   - IOZ = Input, Output, or simultaneously Input and Output, with three-state output function
   - OZ = Output with three-state output function
   - A = Analog
   - CAP = LDO capacitor
   - PWR = Power
   - GND = Ground
3. **DESCRIPTION:** Description of the signal
4. **BALL:** Associated ball number

For more information on the I/O cell configurations, see the *Pad Configuration Registers* section within the *Device Configuration* chapter of the device TRM.

5.3.1 ADC

Table 5-2. ADC0 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
ADC0_AIN0	-	ADC Analog Input 0 (+IN0) CMPSS-A: inH (+IN)	V15	W13	P11	W12
ADC0_AIN1	-	ADC Analog Input 1 (-IN0) CMPSS-A: inL (-IN)	U15	U13	N11	V12
ADC0_AIN2	-	ADC Analog Input 2 (+IN1) CMPSS-A: inH (+IN)	T14	W14	R11	V13
ADC0_AIN3	-	ADC Analog Input 3 (-IN1) CMPSS-A: inL (-IN)	U14	V14	P12	U11
ADC0_AIN4	-	ADC Analog Input 4 (+IN2) CMPSS-A: inH (+IN)	U13	Y14	T12	W13
ADC0_AIN5	-	ADC Analog Input 5 (-IN2) CMPSS-A: inL (-IN)	R14	W15	R12	U13
ADC0_AIN6	-	ADC Analog Input 6		Y15	T13	W14

Table 5-3. ADC1 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
ADC1_AIN0	-	ADC Analog Input 0 (+IN0) CMPSS-A: inH (+IN)	T11	W12	R10	
ADC1_AIN1	-	ADC Analog Input 1 (-IN0) CMPSS-A: inL (-IN)	U11	V12	N10	
ADC1_AIN2	-	ADC Analog Input 2 (+IN1) CMPSS-A: inH (+IN)	T12	Y11	P10	
ADC1_AIN3	-	ADC Analog Input 3 (-IN1) CMPSS-A: inL (-IN)	V12	W11	P9	
ADC1_AIN4	-	ADC Analog Input 4 (+IN2) CMPSS-A: inH (+IN)	U12	Y10	T9	
ADC1_AIN5	-	ADC Analog Input 5 (-IN2) CMPSS-A: inL (-IN)	R12	W10	R9	
ADC1_AIN6	-	ADC Analog Input 6		W9	R8	

Table 5-4. ADC2 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
ADC2_AIN0	-	ADC Analog Input 0 (+IN0) CMPSS-A: inH (+IN)	R10	W8	R7	W8
ADC2_AIN1	-	ADC Analog Input 1 (-IN0) CMPSS-A: inL (-IN)	T10	Y7	P7	V9
ADC2_AIN2	-	ADC Analog Input 2 (+IN1) CMPSS-A: inH (+IN)	U10	Y6	P8	V6
ADC2_AIN3	-	ADC Analog Input 3 (-IN1) CMPSS-A: inL (-IN)	T9	W7	P6	V7
ADC2_AIN4	-	ADC Analog Input 4 (+IN2) CMPSS-A: inH (+IN)	V9	W6	R6	W9
ADC2_AIN5	-	ADC Analog Input 5 (-IN2) CMPSS-A: inL (-IN)	T8	V9	N7	V8
ADC2_AIN6	-	ADC Analog Input 6		Y5	T6	W7

5.3.2 ADC_CAL

Table 5-5. ADC_CAL Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
ADC_CAL0	-	ADC Calibration Pin 0	U16	V16	R13	U15

5.3.3 ADC VREF

Table 5-6. ADC_VREF Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
ADC_VREFHI0	-	ADC Reference (Positive)				V11
ADC_VREFHI1	-	ADC Reference (Positive)	V14	Y12	T10	
ADC_VREFHI2	-	ADC Reference (Positive)	V10	Y8	T7	V10
ADC_VREFLO0	-	ADC Reference (Negative)				W11
ADC_VREFLO1	-	ADC Reference (Negative)	V13	Y13	T11	
ADC_VREFLO2	-	ADC Reference (Negative)	V11	Y9	T8	W10

5.3.4 CPSW

Table 5-7. CPSW0 RGMII1 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
RGMII1_RXC	I	RGMII Receive Clock	E16, R17	F19, W20	E13, P16	D19, V19
RGMII1_RX_CTL	I	RGMII Receive Control	F16, R18	G19, V19	D15, M14	E19, U17
RGMII1_TXC	O	RGMII Transmit Clock	C16, N18	B20, U20	L15	B18, R18
RGMII1_TX_CTL	O	RGMII Transmit Control	A17, M18	E18, T20	M16	A18, T19
RGMII1_RD0	I	RGMII Receive Data 0	F18, U17	H20, Y18	D14, P14	G18, W17
RGMII1_RD1	I	RGMII Receive Data 1	G16, T17	H19, W18	D16, P15	F18, V17
RGMII1_RD2	I	RGMII Receive Data 2	E17, U18	H17, Y19	R16	E17, W18
RGMII1_RD3	I	RGMII Receive Data 3	E18, T18	G20, W19	N14	F19, V18
RGMII1_TD0	O	RGMII Transmit Data 0	B18, P16	F17, V18	N15	D18, U18
RGMII1_TD1	O	RGMII Transmit Data 1	B17, P17	D20, V20	N16	C18, U19
RGMII1_TD2	O	RGMII Transmit Data 2	D16, P18	C20, U19	L13	B19, R17
RGMII1_TD3	O	RGMII Transmit Data 3	C17, N17	D19, T19	M15	C17, T18

Table 5-8. CPSW0 RGMII2 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
RGMII2_RXC	I	RGMII Receive Clock	K15	N20	H15	L18
RGMII2_RX_CTL	I	RGMII Receive Control	K16	L20	G15	J19
RGMII2_TXC	O	RGMII Transmit Clock	H18	M19	F16	K18
RGMII2_TX_CTL	O	RGMII Transmit Control	L16	P18	H16	M19
RGMII2_RD0	I	RGMII Receive Data 0	K17	N17	K14	M18
RGMII2_RD1	I	RGMII Receive Data 1	K18	N19	H14	L19
RGMII2_RD2	I	RGMII Receive Data 2	J18	M18	G16	K19
RGMII2_RD3	I	RGMII Receive Data 3	J17	M20	J14	L17

Table 5-8. CPSW0 RGMII2 Signal Descriptions (continued)

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
RGMII2_TD0	O	RGMII Transmit Data 0	M16	P20	J15	N18
RGMII2_TD1	O	RGMII Transmit Data 1	M15	P19	J16	N19
RGMII2_TD2	O	RGMII Transmit Data 2	H17	K20	F15	H19
RGMII2_TD3	O	RGMII Transmit Data 3	H16	L19	G14	H18

Table 5-9. CPSW0 RMII1 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
RMII1_CRS_DV	I	RMII Carrier Sense / Data Valid	D17, P18	E19, U19	L13	R17
RMII1_REF_CLK	IO	RMII Reference Clock	E16, R17	F19, W20	E13, P16	D19, V19
RMII1_RX_ER	I	RMII Receive Data Error	F15, R18	F20, V19	M14	E18, U17
RMII1_TX_EN	O	RMII Transmit Enable	A17, M18	E18, T20	M16	A18, T19
RMII1_RXD0	I	RMII Receive Data 0	F18, U17	H20, Y18	D14, P14	G18, W17
RMII1_RXD1	I	RMII Receive Data 1	G16, T17	H19, W18	D16, P15	F18, V17
RMII1_TXD0	O	RMII Transmit Data 0	B18, P16	F17, V18	N15	D18, U18
RMII1_TXD1	O	RMII Transmit Data 1	B17, P17	D20, V20	N16	C18, U19

Table 5-10. CPSW0 RMII2 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
RMII2_CRS_DV	I	RMII Carrier Sense / Data Valid	G18	J20	E16	J18
RMII2_REF_CLK	IO	RMII Reference Clock	K15	N20	H15	L18
RMII2_RX_ER	I	RMII Receive Data Error	G17	K19	F14	G17
RMII2_TX_EN	O	RMII Transmit Enable	L16	P18	H16	M19
RMII2_RXD0	I	RMII Receive Data 0	K17	N17	K14	M18
RMII2_RXD1	I	RMII Receive Data 1	K18	N19	H14	L19
RMII2_TXD0	O	RMII Transmit Data 0	M16	P20	J15	N18
RMII2_TXD1	O	RMII Transmit Data 1	M15	P19	J16	N19

Table 5-11. CPSW0 MII1 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
MII1_COL	I	MII Collision Detected	C18, P15	E20, W17	T15	W16
MII1_CRS	I	MII Carrier Sense	D17, R16	E19, Y17	R15	V16
MII1_RXCLK	I	MII Receive Clock	E16, R17	F19, W20	E13, P16	D19, V19
MII1_RXDV	I	MII Receive Data Valid	F16, R18	G19, V19	D15, M14	E19, U17
MII1_RX_ER	I	MII Receive Data Error	F15, T16	F20, Y16	T14	E18, W15
MII1_TXCLK	I	MII Transmit Clock	C16, N18	B20, U20	L15	B18, R18
MII1_TX_EN	O	MII Transmit Enable	A17, M18	E18, T20	M16	A18, T19
MII1_RXD0	I	MII Receive Data 0	F18, U17	H20, Y18	D14, P14	G18, W17
MII1_RXD1	I	MII Receive Data 1	G16, T17	H19, W18	D16, P15	F18, V17
MII1_RXD2	I	MII Receive Data 2	E17, U18	H17, Y19	R16	E17, W18
MII1_RXD3	I	MII Receive Data 3	E18, T18	G20, W19	N14	F19, V18

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Table 5-11. CPSW0 MII1 Signal Descriptions (continued)

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
MII1_TXD0	O	MII Transmit Data 0	B18, P16	F17, V18	N15	D18, U18
MII1_TXD1	O	MII Transmit Data 1	B17, P17	D20, V20	N16	C18, U19
MII1_TXD2	O	MII Transmit Data 2	D16, P18	C20, U19	L13	B19, R17
MII1_TXD3	O	MII Transmit Data 3	C17, N17	D19, T19	M15	C17, T18

Table 5-12. CPSW0 MII2 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
MII2_COL	I	MII Collision Detected	F17	J19	E15	
MII2_CRS	I	MII Carrier Sense	G18	J20	E16	J18
MII2_RXCLK	I	MII Receive Clock	K15	N20	H15	L18
MII2_RXDV	I	MII Receive Data Valid	K16	L20	G15	J19
MII2_RX_ER	I	MII Receive Error	G17	K19	F14	G17
MII2_TXCLK	I	MII Transmit Clock	H18	M19	F16	K18
MII2_TX_EN	O	MII Transmit Enable	L16	P18	H16	M19
MII2_RXD0	I	MII Receive Data 0	K17	N17	K14	M18
MII2_RXD1	I	MII Receive Data 1	K18	N19	H14	L19
MII2_RXD2	I	MII Receive Data 2	J18	M18	G16	K19
MII2_RXD3	I	MII Receive Data 3	J17	M20	J14	L17
MII2_TXD0	O	MII Transmit Data 0	M16	P20	J15	N18
MII2_TXD1	O	MII Transmit Data 1	M15	P19	J16	N19
MII2_TXD2	O	MII Transmit Data 2	H17	K20	F15	H19
MII2_TXD3	O	MII Transmit Data 3	H16	L19	G14	H18

Table 5-13. MDIO0 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
MDIO0_MDC	O	MDIO Clock	M17	T18	L14	R19
MDIO0_MDIO	IO	MDIO Data	N16	R17	L16	P18

5.3.5 CPTS

Table 5-14. CPTS0 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
CPTS0_TS_SYNC	O	CPTS Time Stamp Counter Bit Output	A16	A19	C16	

5.3.6 DAC

Table 5-15. DAC Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
DAC_OUT	-	DAC Output	T5	W4	T5	W6

Table 5-15. DAC Signal Descriptions (continued)

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
DAC_VREF0	-	DAC Voltage Reference 0	T13	U15	P13	V14

5.3.7 EPWM

Table 5-16. EPWM0 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
EPWM0_A	O	EPWM Output A	B2	B3	A4	B5
EPWM0_B	O	EPWM Output B	B1	C3	A5	A6

Table 5-17. EPWM1 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
EPWM1_A	O	EPWM Output A	D3	A2	B4	A5
EPWM1_B	O	EPWM Output B	D2, E4	A3, D1	C1, C5	A4, B3

Table 5-18. EPWM2 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
EPWM2_A	O	EPWM Output A	C2	B1	A3	A3
EPWM2_B	O	EPWM Output B	C1	B2	A2	B4

Table 5-19. EPWM3 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
EPWM3_A	O	EPWM Output A	E2	C1	B2	A2
EPWM3_B	O	EPWM Output B	E1, E3	C2, F2	C4, E3	B2, E3

Table 5-20. EPWM4 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
EPWM4_A	O	EPWM Output A	D1	D2	B1	B1
EPWM4_B	O	EPWM Output B	D2, E4	A3, D1	C1, C5	A4, B3

Table 5-21. EPWM5 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
EPWM5_A	O	EPWM Output A	F2	E2	C2	C2
EPWM5_B	O	EPWM Output B	F1, G2	E1, G1	D1, D3	C1, D1

Table 5-22. EPWM6 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
EPWM6_A	O	EPWM Output A	B9, E1, E3	B11, C2, F2	C4, D8, E3	B10, B2, E3
EPWM6_B	O	EPWM Output B	A9, F3	A11, F1	C10, F4	A11, E2

Table 5-23. EPWM7 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
EPWM7_A	O	EPWM Output A	C9, F4	D11, G2	B9, D2	D2
EPWM7_B	O	EPWM Output B	A10, F1, G4	A12, G1, J2	B10, D1	D1

Table 5-24. EPWM8 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
EPWM8_A	O	EPWM Output A	B10, G3	D10, H2	A9, E2	E1
EPWM8_B	O	EPWM Output B	D9, G2, H2	C9, E1, H1	C11, D3, E1	C1, F1

Table 5-25. EPWM9 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
EPWM9_A	O	EPWM Output A	G1, N1	K4, R2	F2, M2	F2, N2
EPWM9_B	O	EPWM Output B	H2, J2, N4	H1, L2, R1	E1, F3, N1	F1, G1, N1

5.3.8 EQEP

Table 5-26. EQEP0 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
EQEP0_A	I	EQEP Quadrature Input A	B14, U18	A16, Y19	D13, R16	B15, W18
EQEP0_B	I	EQEP Quadrature Input B	A14, T18	B16, W19	C13, N14	A15, V18
EQEP0_INDEX	IO	EQEP Index	D11, N18	D15, U20	B13, L15	B14, R18
EQEP0_STROBE	IO	EQEP Strobe	C12, M18	C14, T20	C12, M16	A14, T19

Table 5-27. EQEP1 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
EQEP1_A	I	EQEP Quadrature Input A	D15, P16	C18, V18	N15	B16, U18
EQEP1_B	I	EQEP Quadrature Input B	C15, P17	C19, V20	N16	B17, U19
EQEP1_INDEX	IO	EQEP Index	A12, N17, P2	A14, T19, U2	M15, P3	T1, T18
EQEP1_STROBE	IO	EQEP Strobe	B16, P18	B19, U19	C15, L13	R17

5.3.9 FSI

Table 5-28. FSIRX0 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
FSIRX0_CLK	I	FSI Clock	A10, T17	A12, W18	B10, P15	V17
FSIRX0_DATA0	I	FSI Data 0	B10, U18	D10, Y19	A9, R16	W18
FSIRX0_DATA1	I	FSI Data 1	D9, T18	C9, W19	C11, N14	V18

Table 5-29. FSITX0 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
FSITX0_CLK	O	FSI Clock	A11, R17	A13, W20	A12, P16	A12, V19
FSITX0_DATA0	O	FSI Data 0	C10, R18	B12, V19	A10, M14	B12, U17
FSITX0_DATA1	O	FSI Data 1	B11, U17	C12, Y18	A11, P14	B11, W17

5.3.10 GPIO

Table 5-30. GPIO Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
GPIO0	IO	General Purpose Input/Output	P1	U4	N3	R1
GPIO1	IO	General Purpose Input/Output	R3	T2	M3	R2
GPIO2	IO	General Purpose Input/Output	N2	M3	L2	M2
GPIO3	IO	General Purpose Input/Output	N1	R2	M2	N2
GPIO4	IO	General Purpose Input/Output	N4	R1	N1	N1
GPIO5	IO	General Purpose Input/Output	M4	T1	L3	P2
GPIO6	IO	General Purpose Input/Output	P3	U1	N2	P1
GPIO7	IO	General Purpose Input/Output	M1	P1	J3	K2
GPIO8	IO	General Purpose Input/Output	L1	P2	K1	L1
GPIO9	IO	General Purpose Input/Output	L2	N2	K2	J2
GPIO10	IO	General Purpose Input/Output	K1	N1	J2	K1
GPIO11	IO	General Purpose Input/Output	C11	B13	B11	C13
GPIO12	IO	General Purpose Input/Output	A11	A13	A12	A12
GPIO13	IO	General Purpose Input/Output	C10	B12	A10	B12
GPIO14	IO	General Purpose Input/Output	B11	C12	A11	B11
GPIO15	IO	General Purpose Input/Output	C9	D11	B9	
GPIO16	IO	General Purpose Input/Output	A10	A12	B10	
GPIO17	IO	General Purpose Input/Output	B10	D10	A9	
GPIO18	IO	General Purpose Input/Output	D9	C9	C11	
GPIO19	IO	General Purpose Input/Output	A9	A11	C10	A11
GPIO100	IO	General Purpose Input/Output	M15	P19	J16	N19
GPIO101	IO	General Purpose Input/Output	H17	K20	F15	H19
GPIO102	IO	General Purpose Input/Output	H16	L19	G14	H18
GPIO103	IO	General Purpose Input/Output	F15	F20		E18
GPIO104	IO	General Purpose Input/Output	C18	E20		
GPIO105	IO	General Purpose Input/Output	D17	E19		
GPIO106	IO	General Purpose Input/Output	D18	G18		C19

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Table 5-30. GPIO Signal Descriptions (continued)

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
GPIO107	IO	General Purpose Input/Output	E16	F19	E13	D19
GPIO108	IO	General Purpose Input/Output	F16	G19	D15	E19
GPIO109	IO	General Purpose Input/Output	F18	H20	D14	G18
GPIO110	IO	General Purpose Input/Output	G16	H19	D16	F18
GPIO111	IO	General Purpose Input/Output	E17	H17		E17
GPIO112	IO	General Purpose Input/Output	E18	G20		F19
GPIO113	IO	General Purpose Input/Output	C16	B20		B18
GPIO114	IO	General Purpose Input/Output	A17	E18		A18
GPIO115	IO	General Purpose Input/Output	B18	F17		D18
GPIO116	IO	General Purpose Input/Output	B17	D20		C18
GPIO117	IO	General Purpose Input/Output	D16	C20		B19
GPIO118	IO	General Purpose Input/Output	C17	D19		C17
GPIO119	IO	General Purpose Input/Output	D15	C18		B16
GPIO120	IO	General Purpose Input/Output	C15	C19		B17
GPIO121	IO	General Purpose Input/Output	P2	U2	P3	T1
GPIO122	IO	General Purpose Input/Output	B16	B19	C15	
GPIO123	IO	General Purpose Input/Output	D14	C16	A15	
GPIO124	IO	General Purpose Input/Output	A16	A19	C16	
GPIO125	IO	General Purpose Input/Output	D13	B17	C14	
GPIO126	IO	General Purpose Input/Output	B15	A18	B16	A17
GPIO127	IO	General Purpose Input/Output	C13	A17	A14	A16
GPIO128	IO	General Purpose Input/Output	A15	B18	B15	
GPIO129	IO	General Purpose Input/Output	C14	D17	B14	
GPIO130	IO	General Purpose Input/Output	B14	A16	D13	B15
GPIO131	IO	General Purpose Input/Output	A14	B16	C13	A15
GPIO132	IO	General Purpose Input/Output	C12	C14	C12	A14
GPIO133	IO	General Purpose Input/Output	D11	D15	B13	B14
GPIO134	IO	General Purpose Input/Output	B13	B15	B12	B13
GPIO135	IO	General Purpose Input/Output	A13	A15	A13	A13
GPIO136	IO	General Purpose Input/Output	B12	B14		
GPIO137	IO	General Purpose Input/Output	A12	A14		
GPIO138	IO	General Purpose Input/Output	M2	M1	H1	J3
GPIO139	IO	General Purpose Input/Output	V2	V1	R1	V1
GPIO140	IO	General Purpose Input/Output	U3	W1	P1	U1
GPIO20	IO	General Purpose Input/Output	B9	B11	D8	B10
GPIO21	IO	General Purpose Input/Output	B8	B10	B8	A10
GPIO22	IO	General Purpose Input/Output	A8	A10	C9	B9
GPIO23	IO	General Purpose Input/Output	D7	B9	B7	
GPIO24	IO	General Purpose Input/Output	C8	A9	A8	
GPIO25	IO	General Purpose Input/Output	C7	C7	C8	C9
GPIO26	IO	General Purpose Input/Output	B7	D8	A7	A9
GPIO27	IO	General Purpose Input/Output	A7	A8	A6	A8
GPIO28	IO	General Purpose Input/Output	A6	B8	B6	B8
GPIO29	IO	General Purpose Input/Output	R17	W20	P16	V19

Table 5-30. GPIO Signal Descriptions (continued)

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
GPIO30	IO	General Purpose Input/Output	R18	V19	M14	U17
GPIO31	IO	General Purpose Input/Output	U17	Y18	P14	W17
GPIO32	IO	General Purpose Input/Output	T17	W18	P15	V17
GPIO33	IO	General Purpose Input/Output	U18	Y19	R16	W18
GPIO34	IO	General Purpose Input/Output	T18	W19	N14	V18
GPIO35	IO	General Purpose Input/Output	N18	U20	L15	R18
GPIO36	IO	General Purpose Input/Output	M18	T20	M16	T19
GPIO37	IO	General Purpose Input/Output	P16	V18	N15	U18
GPIO38	IO	General Purpose Input/Output	P17	V20	N16	U19
GPIO39	IO	General Purpose Input/Output	P18	U19	L13	R17
GPIO40	IO	General Purpose Input/Output	N17	T19	M15	T18
GPIO41	IO	General Purpose Input/Output	N16	R17	L16	P18
GPIO42	IO	General Purpose Input/Output	M17	T18	L14	R19
GPIO43	IO	General Purpose Input/Output	B2	B3	A4	B5
GPIO44	IO	General Purpose Input/Output	B1	C3	A5	A6
GPIO45	IO	General Purpose Input/Output	D3	A2	B4	A5
GPIO46	IO	General Purpose Input/Output	D2	A3	C5	A4
GPIO47	IO	General Purpose Input/Output	C2	B1	A3	A3
GPIO48	IO	General Purpose Input/Output	C1	B2	A2	B4
GPIO49	IO	General Purpose Input/Output	E2	C1	B2	A2
GPIO50	IO	General Purpose Input/Output	E3	C2	C4	B2
GPIO51	IO	General Purpose Input/Output	D1	D2	B1	B1
GPIO52	IO	General Purpose Input/Output	E4	D1	C1	B3
GPIO53	IO	General Purpose Input/Output	F2	E2	C2	C2
GPIO54	IO	General Purpose Input/Output	G2	E1	D3	C1
GPIO55	IO	General Purpose Input/Output	E1	F2	E3	E3
GPIO56	IO	General Purpose Input/Output	F3	F1	F4	E2
GPIO57	IO	General Purpose Input/Output	F4	G2	D2	D2
GPIO58	IO	General Purpose Input/Output	F1	G1	D1	D1
GPIO59	IO	General Purpose Input/Output	G3	H2	E2	E1
GPIO60	IO	General Purpose Input/Output	H2	H1	E1	F1
GPIO61	IO	General Purpose Input/Output	G1	K4	F2	F2
GPIO62	IO	General Purpose Input/Output	J2	L2	F3	G1
GPIO63	IO	General Purpose Input/Output	G4	J2		
GPIO64	IO	General Purpose Input/Output	J3	J1		
GPIO65	IO	General Purpose Input/Output	H1	J3		
GPIO66	IO	General Purpose Input/Output	J1	K2	G3	
GPIO67	IO	General Purpose Input/Output	K2	K1	G2	G2
GPIO68	IO	General Purpose Input/Output	J4	L4	H3	H1
GPIO69	IO	General Purpose Input/Output	K4	L1	H2	H2
GPIO70	IO	General Purpose Input/Output	K3	M2	G1	J1
GPIO71	IO	General Purpose Input/Output	V17	W16	R14	V15
GPIO72	IO	General Purpose Input/Output	T16	Y16	T14	W15
GPIO73	IO	General Purpose Input/Output	P15	W17	T15	W16

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Table 5-30. GPIO Signal Descriptions (continued)

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
GPIO74	IO	General Purpose Input/Output	R16	Y17	R15	V16
GPIO75	IO	General Purpose Input/Output	L3	T3	M1	L2
GPIO76	IO	General Purpose Input/Output	M3	R4	L1	M1
GPIO77	IO	General Purpose Input/Output	B6	B7		
GPIO78	IO	General Purpose Input/Output	A4	A6		
GPIO79	IO	General Purpose Input/Output	B5	B6		
GPIO80	IO	General Purpose Input/Output	B4	A5		
GPIO81	IO	General Purpose Input/Output	A3	B5		
GPIO82	IO	General Purpose Input/Output	A2	A4		
GPIO83	IO	General Purpose Input/Output	C6	B4		
GPIO84	IO	General Purpose Input/Output	A5	A7		
GPIO85	IO	General Purpose Input/Output	L17	R19	K15	N17
GPIO86	IO	General Purpose Input/Output	L18	R20	K16	P19
GPIO87	IO	General Purpose Input/Output	G17	K19	F14	G17
GPIO88	IO	General Purpose Input/Output	F17	J19	E15	
GPIO89	IO	General Purpose Input/Output	G18	J20	E16	J18
GPIO90	IO	General Purpose Input/Output	G15	J18	E14	G19
GPIO91	IO	General Purpose Input/Output	K15	N20	H15	L18
GPIO92	IO	General Purpose Input/Output	K16	L20	G15	J19
GPIO93	IO	General Purpose Input/Output	K17	N17	K14	M18
GPIO94	IO	General Purpose Input/Output	K18	N19	H14	L19
GPIO95	IO	General Purpose Input/Output	J18	M18	G16	K19
GPIO96	IO	General Purpose Input/Output	J17	M20	J14	L17
GPIO97	IO	General Purpose Input/Output	H18	M19	F16	K18
GPIO98	IO	General Purpose Input/Output	L16	P18	H16	M19
GPIO99	IO	General Purpose Input/Output	M16	P20	J15	N18

5.3.11 GPMC0

Table 5-31. GPMC0 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
GPMC0_ADVn_ALE	O	GPMC Address Valid (active low) or Address Latch Enable	A8	A10	C9	B9
GPMC0_CLK	IO	GPMC Clock	L3	T3	M1	L2
GPMC0_CLKLB	IO	GPMC Clock Loopback	B15	A18	B16	A17
GPMC0_DIR	O	GPMC Data Bus Signal Direction Control	B10	D10	A9	
GPMC0_OEn_REn	O	GPMC Output Enable (active low) or Read Enable (active low)	A10, B14, C8	A12, A16, A9	A8, B10, D13	B15
GPMC0_WEn	O	GPMC Write Enable (active low)	C14, D7	B9, D17	B14, B7	
GPMC0_WPn	O	GPMC Flash Write Protect (active low)	D9	C9	C11	
GPMC0_A0	O	GPMC Address 0 Output. Only used to effectively address 8-bit data non-multiplexed memories	C11	B13	B11	C13

Table 5-31. GPMC0 Signal Descriptions (continued)

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
GPMC0_A1	O	GPMC Address 1 Output in A/D non-multiplexed mode and Address 17 in A/D multiplexed mode	C2	B1	A3	A3
GPMC0_A2	O	GPMC Address 2 Output in A/D non-multiplexed mode and Address 18 in A/D multiplexed mode	D2	A3	C5	A4
GPMC0_A3	O	GPMC Address 3 Output in A/D non-multiplexed mode and Address 19 in A/D multiplexed mode	B2	B3	A4	B5
GPMC0_A4	O	GPMC Address 4 Output in A/D non-multiplexed mode and Address 20 in A/D multiplexed mode	D3	A2	B4	A5
GPMC0_A5	O	GPMC Address 5 Output in A/D non-multiplexed mode and Address 21 in A/D multiplexed mode	B16	B19	C15	
GPMC0_A6	O	GPMC Address 6 Output in A/D non-multiplexed mode and Address 22 in A/D multiplexed mode	B1	C3	A5	A6
GPMC0_A7	O	GPMC Address 7 Output in A/D non-multiplexed mode and Address 23 in A/D multiplexed mode	A11	A13	A12	A12
GPMC0_A8	O	GPMC Address 8 Output in A/D non-multiplexed mode and Address 24 in A/D multiplexed mode	A16	A19	C16	
GPMC0_A9	O	GPMC Address 9 Output in A/D non-multiplexed mode and Address 25 in A/D multiplexed mode	E3	C2	C4	B2
GPMC0_A10	O	GPMC Address 10 Output in A/D non-multiplexed mode and Address 26 in A/D multiplexed mode	D1	D2	B1	B1
GPMC0_A11	O	GPMC Address 11 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	E4	D1	C1	B3
GPMC0_A12	O	GPMC Address 12 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	F2	E2	C2	C2
GPMC0_A13	O	GPMC Address 13 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	E2	C1	B2	A2
GPMC0_A14	O	GPMC Address 14 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	C1	B2	A2	B4
GPMC0_A15	O	GPMC Address 15 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	C12	C14	C12	A14
GPMC0_A16	O	GPMC Address 16 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	C10	B12	A10	B12
GPMC0_A17	O	GPMC Address 17 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	C15	C19		B17
GPMC0_A18	O	GPMC Address 18 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	P2	U2	P3	T1

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Table 5-31. GPMC0 Signal Descriptions (continued)

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
GPMC0_A19	O	GPMC Address 19 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	D15	C18		B16
GPMC0_A20	O	GPMC Address 20 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	D17, F3	E19, F1	F4	E2
GPMC0_A21	O	GPMC Address 21 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	C18	E20		
GPMC0_AD0	IO	GPMC Data 0 Input/Output in A/D non-multiplexed mode and additionally Address 1 Output in A/D multiplexed mode	V17	W16	R14	V15
GPMC0_AD1	IO	GPMC Data 1 Input/Output in A/D non-multiplexed mode and additionally Address 2 Output in A/D multiplexed mode	T16	Y16	T14	W15
GPMC0_AD2	IO	GPMC Data 2 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode	P15	W17	T15	W16
GPMC0_AD3	IO	GPMC Data 3 Input/Output in A/D non-multiplexed mode and additionally Address 4 Output in A/D multiplexed mode	F1	G1	D1	D1
GPMC0_AD4	IO	GPMC Data 4 Input/Output in A/D non-multiplexed mode and additionally Address 5 Output in A/D multiplexed mode	F4	G2	D2	D2
GPMC0_AD5	IO	GPMC Data 5 Input/Output in A/D non-multiplexed mode and additionally Address 6 Output in A/D multiplexed mode	G2	E1	D3	C1
GPMC0_AD6	IO	GPMC Data 6 Input/Output in A/D non-multiplexed mode and additionally Address 7 Output in A/D multiplexed mode	A9	A11	C10	A11
GPMC0_AD7	IO	GPMC Data 7 Input/Output in A/D non-multiplexed mode and additionally Address 8 Output in A/D multiplexed mode	D11	D15	B13	B14
GPMC0_AD8	IO	GPMC Data 8 Input/Output in A/D non-multiplexed mode and additionally Address 9 Output in A/D multiplexed mode	B9, E1	B11, F2	D8, E3	B10, E3
GPMC0_AD9	IO	GPMC Data 9 Input/Output in A/D non-multiplexed mode and additionally Address 10 Output in A/D multiplexed mode	R16	Y17	R15	V16
GPMC0_AD10	IO	GPMC Data 10 Input/Output in A/D non-multiplexed mode and additionally Address 11 Output in A/D multiplexed mode	D14	C16	A15	
GPMC0_AD11	O	GPMC Data 11 Input/Output in A/D non-multiplexed mode and additionally Address 12 Output in A/D multiplexed mode	N1	R2	M2	N2

Table 5-31. GPMC0 Signal Descriptions (continued)

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
GPMC0_AD12	O	GPMC Data 12 Input/Output in A/D non-multiplexed mode and additionally Address 13 Output in A/D multiplexed mode	N4	R1	N1	N1
GPMC0_AD13	IO	GPMC Data 13 Input/Output in A/D non-multiplexed mode and additionally Address 14 Output in A/D multiplexed mode	D13	B17	C14	
GPMC0_AD14	IO	GPMC Data 14 Input/Output in A/D non-multiplexed mode and additionally Address 15 Output in A/D multiplexed mode	A15	B18	B15	
GPMC0_AD15	IO	GPMC Data 15 Input/Output in A/D non-multiplexed mode and additionally Address 16 Output in A/D multiplexed mode	H2	H1	E1	F1
GPMC0_BE0n_CLE	O	GPMC Lower-Byte Enable (active low) or Command Latch Enable	C13	A17	A14	A16
GPMC0_BE1n	O	GPMC Upper-Byte Enable (active low)	B11	C12	A11	B11
GPMC0_CSn0	O	GPMC Chip Select 0 (active low)	A14, B8	B10, B16	B8, C13	A10, A15
GPMC0_CSn1	O	GPMC Chip Select 1 (active low)	G3	H2	E2	E1
GPMC0_CSn2	O	GPMC Chip Select 2 (active low)	U18	Y19	R16	W18
GPMC0_CSn3	O	GPMC Chip Select 3 (active low)	T18	W19	N14	V18
GPMC0_WAIT0	I	GPMC External Indication of Wait	C9	D11	B9	
GPMC0_WAIT1	I	GPMC External Indication of Wait	C7	C7	C8	C9

5.3.12 I2C

Table 5-32. I2C0 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
I2C0_SCL	IO	I2C Clock	A13, J3, K15	A15, J1, N20	A13, H15	A13, L18
I2C0_SDA	IO	I2C Data	B13, G15, G4	B15, J18, J2	B12, E14	B13, G19

Table 5-33. I2C1 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
I2C1_SCL	IO	I2C Clock	A14, B5, D7, J1	B16, B6, B9, K2	B7, C13, G3	A15
I2C1_SDA	IO	I2C Data	A3, B14, C8, H1	A16, A9, B5, J3	A8, D13	B15

Table 5-34. I2C2 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
I2C2_SCL	IO	I2C Clock	C6, C7, D11	B4, C7, D15	B13, C8	B14, C9
I2C2_SDA	IO	I2C Data	A5, B7, C12	A7, C14, D8	A7, C12	A14, A9

5.3.13 LIN

Table 5-35. LIN0 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
LIN0_RXD	IO	LIN Receive Data	A7, B12, B6, G4, L17	A8, B14, B7, J2, R19	A6, K15	A8, N17
LIN0_TXD	IO	LIN Transmit Data	A12, A4, A6, J3, L18	A14, A6, B8, J1, R20	B6, K16	B8, P19

Table 5-36. LIN1 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
LIN1_RXD	IO	LIN Receive Data	A9, J2, L3, M2	A11, L2, M1, T3	C10, F3, H1, M1	A11, G1, J3, L2
LIN1_TXD	IO	LIN Transmit Data	B9, G1, L2, M3	B11, K4, N2, R4	D8, F2, K2, L1	B10, F2, J2, M1

Table 5-37. LIN2 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
LIN2_RXD	IO	LIN Receive Data	B8	B10	B8	A10
LIN2_TXD	IO	LIN Transmit Data	A8	A10	C9	B9

5.3.14 MCAN

Table 5-38. MCAN0 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
MCAN0_RX	I	MCAN Receive Data	B6, E16, G3, L17, M1	B7, F19, H2, P1, R19	E13, E2, J3, K15	D19, E1, K2, N17
MCAN0_TX	O	MCAN Transmit Data	A4, F16, H2, L1, L18	A6, G19, H1, P2, R20	D15, E1, K1, K16	E19, F1, L1, P19

Table 5-39. MCAN1 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
MCAN1_RX	I	MCAN Receive Data	B14, B5, F18, L2, N16	A16, B6, H20, N2, R17	D13, D14, K2, L16	B15, G18, J2, P18
MCAN1_TX	O	MCAN Transmit Data	A14, B4, G16, K1, M17	A5, B16, H19, N1, T18	C13, D16, J2, L14	A15, F18, K1, R19

5.3.15 SPI (MCSPI)

Table 5-40. SPI0 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
SPI0_CLK	IO	SPI0 Clock (SOP2)	A11, R3	A13, T2	A12, M3	A12, R2
SPI0_CS0	IO	SPI0 Chip Select 0	C11, P1	B13, U4	B11, N3	C13, R1
SPI0_CS1	IO	SPI0 Chip Select 1	B12, B7	B14, D8	A7	A9

Table 5-40. SPI0 Signal Descriptions (continued)

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
SPI0_D0	IO	SPI0 Data 0 (SOP3)	C10, M4	B12, T1	A10, L3	B12, P2
SPI0_D1	IO	SPI0 Data 1	B11, P3	C12, U1	A11, N2	B11, P1

Table 5-41. SPI1 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
SPI1_CLK	IO	SPI1 Clock	A10	A12	B10	
SPI1_CS0	IO	SPI1 Chip Select 0	C9	D11	B9	
SPI1_D0	IO	SPI1 Data 0	B10	D10	A9	
SPI1_D1	IO	SPI1 Data 1	D9	C9	C11	

Table 5-42. SPI2 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
SPI2_CLK	IO	SPI2 Clock	B9, C14, G1	B11, D17, K4	B14, D8, F2	B10, F2
SPI2_CS0	IO	SPI2 Chip Select 0	A14, A9, M2	A11, B16, M1	C10, C13, H1	A11, A15, J3
SPI2_CS1	IO	SPI2 Chip Select 1	B15	A18	B16	A17
SPI2_D0	IO	SPI2 Data 0	B14, B8	A16, B10	B8, D13	A10, B15
SPI2_D1	IO	SPI2 Data 1	A15, A8	A10, B18	B15, C9	B9

Table 5-43. SPI3 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
SPI3_CLK	IO	SPI3 Clock	C8	A9	A8	
SPI3_CS0	IO	SPI3 Chip Select 0	D7	B9	B7	
SPI3_CS1	IO	SPI3 Chip Select 1	C13	A17	A14	A16
SPI3_D0	IO	SPI3 Data 0	C7	C7	C8	C9
SPI3_D1	IO	SPI3 Data 1	B7	D8	A7	A9

5.3.16 MMC

Table 5-44. MMC0 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
MMC0_CD	I	MMC/SD Card Detect	A5, D9	A7, C9	C11	
MMC0_CLK	IO	MMC/SD Clock	B6, C11	B13, B7	B11	C13
MMC0_CMD	IO	MMC/SD Command	A11, A4	A13, A6	A12	A12
MMC0_WP	I	MMC/SD Write Protect	B10, C6	B4, D10	A9	
MMC0_D0	IO	MMC/SD Data	B5, C10	B12, B6	A10	B12
MMC0_D1	IO	MMC/SD Data	B11, B4	A5, C12	A11	B11
MMC0_D2	IO	MMC/SD Data	A3, C9	B5, D11	B9	
MMC0_D3	IO	MMC/SD Data	A10, A2	A12, A4	B10	

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5.3.17 Power Supply

Table 5-45. Power Supply Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
VDD	Power	1.2V Core supply	E11, E9, F11, F9, G13, G14, G5, G6, K13, K14, K5, K6, N13, N14, N5, N6	F12, F14, F7, F9, G15, G6, J15, J6, M15, M6, P15, P6, R7	E11, E5, E7, E9, F12, G5, H12, J5, K12, L5, M12, M6	E10, E12, E14, E6, E8, F15, F5, H15, H5, K15, K5, M15, M5, P15, P5, R15, R6, T6
VDDA18_LDO	Power	1.8V Analog LDO Output	R11, R6, R8	U10, U11	N9	U9
VDDA18_OSC_PLL	Power	1.8V PLL supply	R4	U8	N6	U7
VDDA18_USB	Power	USB 1.8V analog supply		T5	N4	U3
VDDA33	Power	3.3V analog supply	P11, P7, P9	T12, T9	M10, M8	T10, T12
VDDA33_USB	Power	USB 3.3V analog supply		P5	M4	R3
VDDAR2	Power	SRAM Array supply	D10	D13	D10	C11
VDDAR3	Power	SRAM Array supply	H3	H4	G4	G3
VDDS18	Power	1.8V IO supply	D6, E15, L4, N15	E14, E9, F4, G16, L17, N4, T16	D12, D6, D9, E4, G13, K13, K4, N13	D10, D14, D6, H16, H4, L3, M16, T16
VDDS18_LDO	Power	1.8V Digital LDO Output	T3	U6	P4	V4
VDDS1833_FLASH0	Power	1.8V/3.3V Flash 0 IO Supply		J5	H4, J4	K4, M4
VDDS1833_FLASH1	Power	1.8V/3.3V Flash 1 IO Supply		P16	M13	P16
VDDS1833_FLASH0-SIP	Power	1.8V/3.3V SIP Flash Supply. This must be shorted to VDDSHV_D(VDDS1833_FLASH0) on board. Will be used for Flash supply in future Flash SIP packages.			F1, J1	
VDDS33	Power	3.3V IO supply	D12, H15, H4, L15, P4, R15	E12, E16, E7, G5, J16, M16, M5, T14, T7	D11, D4, D7, F13, J13, L4, N12, N5	C15, D12, D8, F16, F4, K16, P4, T14, U5
VDD_TEMP	Power	VDD Temp	T4	V7	N8	T8
VNWA	Power	1.2V N-well bias	J16	K17	H13	J17
VSSA	-	Analog Ground	P10, P12, P6, P8, R13, R5, V1, V16	R12, R9	M11, M9	R10, R12

5.3.18 PRU-ICSS

Table 5-46. PRU-ICSS ECAP Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
PR0_ECAP0_APWM_OUT	O	PRU-ICSS Enhanced Capture (ECAP) Input or ECAP Auxiliary PWM (APWM) Output	D14	C16	A15	
PR1_ECAP0_APWM_OUT	O	PRU-ICSS Enhanced Capture (ECAP) Input or ECAP Auxiliary PWM (APWM) Output	D14	C16	A15	

Table 5-47. PRU-ICSS GPIO Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
PR0_PRU0_GPIO0	IO	PRU0 General Purpose Input/Output	K17	N17	K14	M18
PR0_PRU0_GPIO1	IO	PRU0 General Purpose Input/Output	K18	N19	H14	L19
PR0_PRU0_GPIO2	IO	PRU0 General Purpose Input/Output	J18	M18	G16	K19
PR0_PRU0_GPIO3	IO	PRU0 General Purpose Input/Output	J17	M20	J14	L17
PR0_PRU0_GPIO4	IO	PRU0 General Purpose Input/Output	K16	L20	G15	J19
PR0_PRU0_GPIO5	IO	PRU0 General Purpose Input/Output	G17	K19	F14	G17
PR0_PRU0_GPIO6	IO	PRU0 General Purpose Input/Output	K15	N20	H15	L18
PR0_PRU0_GPIO7	IO	PRU0 General Purpose Input/Output	N17	T19	M15	T18
PR0_PRU0_GPIO8	IO	PRU0 General Purpose Input/Output	G15	J18	E14	G19
PR0_PRU0_GPIO9	IO	PRU0 General Purpose Input/Output	F17	J19	E15	
PR0_PRU0_GPIO10	IO	PRU0 General Purpose Input/Output	G18	J20	E16	J18
PR0_PRU0_GPIO11	IO	PRU0 General Purpose Input/Output	M16	P20	J15	N18
PR0_PRU0_GPIO12	IO	PRU0 General Purpose Input/Output	M15	P19	J16	N19
PR0_PRU0_GPIO13	IO	PRU0 General Purpose Input/Output	H17	K20	F15	H19
PR0_PRU0_GPIO14	IO	PRU0 General Purpose Input/Output	H16	L19	G14	H18
PR0_PRU0_GPIO15	IO	PRU0 General Purpose Input/Output	L16	P18	H16	M19
PR0_PRU0_GPIO16	IO	PRU0 General Purpose Input/Output	H18	M19	F16	K18
PR0_PRU1_GPIO0	IO	PRU1 General Purpose Input/Output	F18	H20	D14	G18
PR0_PRU1_GPIO1	IO	PRU1 General Purpose Input/Output	G16	H19	D16	F18
PR0_PRU1_GPIO2	IO	PRU1 General Purpose Input/Output	E17	H17		E17
PR0_PRU1_GPIO3	IO	PRU1 General Purpose Input/Output	E18	G20		F19
PR0_PRU1_GPIO4	IO	PRU1 General Purpose Input/Output	F16	G19	D15	E19
PR0_PRU1_GPIO5	IO	PRU1 General Purpose Input/Output	F15	F20		E18
PR0_PRU1_GPIO6	IO	PRU1 General Purpose Input/Output	E16	F19	E13	D19
PR0_PRU1_GPIO7	IO	PRU1 General Purpose Input/Output	A16, G3	A19, H2	C16, E2	E1
PR0_PRU1_GPIO8	IO	PRU1 General Purpose Input/Output	D18	G18		C19
PR0_PRU1_GPIO9	IO	PRU1 General Purpose Input/Output	C18	E20		
PR0_PRU1_GPIO10	IO	PRU1 General Purpose Input/Output	D17	E19		
PR0_PRU1_GPIO11	IO	PRU1 General Purpose Input/Output	B18	F17		D18
PR0_PRU1_GPIO12	IO	PRU1 General Purpose Input/Output	B17	D20		C18
PR0_PRU1_GPIO13	IO	PRU1 General Purpose Input/Output	D16	C20		B19
PR0_PRU1_GPIO14	IO	PRU1 General Purpose Input/Output	C17	D19		C17
PR0_PRU1_GPIO15	IO	PRU1 General Purpose Input/Output	A17	E18		A18
PR0_PRU1_GPIO16	IO	PRU1 General Purpose Input/Output	C16	B20		B18
PR0_PRU1_GPIO17	IO	PRU1 General Purpose Input/Output	D13	B17	C14	
PR0_PRU1_GPIO18	IO	PRU1 General Purpose Input/Output	C15	C19		B17
PR0_PRU1_GPIO19	IO	PRU1 General Purpose Input/Output	D15	C18		B16
PR1_PRU0_GPIO0	IO	PRU0 General Purpose Input/Output	A3, C10, K17, K2	B12, B5, K1, N17	A10, G2, K14	B12, G2, M18
PR1_PRU0_GPIO1	IO	PRU0 General Purpose Input/Output	A2, B11, J4, K18	A4, C12, L4, N19	A11, H14, H3	B11, H1, L19
PR1_PRU0_GPIO2	IO	PRU0 General Purpose Input/Output	C11, C6, J18, K4	B13, B4, L1, M18	B11, G16, H2	C13, H2, K19
PR1_PRU0_GPIO3	IO	PRU0 General Purpose Input/Output	C2	B1	A3	A3
PR1_PRU0_GPIO4	IO	PRU0 General Purpose Input/Output	D2	A3	C5	A4

ADVANCE INFORMATION

Table 5-47. PRU-ICSS GPIO Signal Descriptions (continued)

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
PR1_PRU0_GPIO5	IO	PRU0 General Purpose Input/Output	B2	B3	A4	B5
PR1_PRU0_GPIO6	IO	PRU0 General Purpose Input/Output	D3	A2	B4	A5
PR1_PRU0_GPIO7	IO	PRU0 General Purpose Input/Output	B16, B7, C1	B19, B2, D8	A2, A7, C15	A9, B4
PR1_PRU0_GPIO8	IO	PRU0 General Purpose Input/Output	B1	C3	A5	A6
PR1_PRU0_GPIO9	IO	PRU0 General Purpose Input/Output	A11, B4, F17, K3	A13, A5, J19, M2	A12, E15, G1	A12, J1
PR1_PRU0_GPIO10	IO	PRU0 General Purpose Input/Output	A16, B5	A19, B6	C16	
PR1_PRU0_GPIO11	IO	PRU0 General Purpose Input/Output	E3	C2	C4	B2
PR1_PRU0_GPIO12	IO	PRU0 General Purpose Input/Output	D1	D2	B1	B1
PR1_PRU0_GPIO13	IO	PRU0 General Purpose Input/Output	E4	D1	C1	B3
PR1_PRU0_GPIO14	IO	PRU0 General Purpose Input/Output	F2	E2	C2	C2
PR1_PRU0_GPIO15	IO	PRU0 General Purpose Input/Output	E2	C1	B2	A2
PR1_PRU0_GPIO16	IO	PRU0 General Purpose Input/Output	C1	B2	A2	B4
PR1_PRU0_GPIO17	IO	PRU0 General Purpose Input/Output	C7, D7	B9, C7	B7, C8	C9
PR1_PRU0_GPIO18	IO	PRU0 General Purpose Input/Output	C8	A9	A8	
PR1_PRU0_GPIO19	IO	PRU0 General Purpose Input/Output	A14	B16	C13	A15
PR1_PRU0_GPIO20	IO	PRU1 General Purpose Input/Output	C12	C14	C12	A14
PR1_PRU1_GPIO0	IO	PRU1 General Purpose Input/Output	V17	W16	R14	V15
PR1_PRU1_GPIO1	IO	PRU1 General Purpose Input/Output	T16	Y16	T14	W15
PR1_PRU1_GPIO2	IO	PRU1 General Purpose Input/Output	P15	W17	T15	W16
PR1_PRU1_GPIO3	IO	PRU1 General Purpose Input/Output	A10, F1	A12, G1	B10, D1	D1
PR1_PRU1_GPIO4	IO	PRU1 General Purpose Input/Output	C9, F4	D11, G2	B9, D2	D2
PR1_PRU1_GPIO5	IO	PRU1 General Purpose Input/Output	G2	E1	D3	C1
PR1_PRU1_GPIO6	IO	PRU1 General Purpose Input/Output	A9, F3	A11, F1	C10, F4	A11, E2
PR1_PRU1_GPIO7	IO	PRU1 General Purpose Input/Output	D11	D15	B13	B14
PR1_PRU1_GPIO8	IO	PRU1 General Purpose Input/Output	B9, E1	B11, F2	D8, E3	B10, E3
PR1_PRU1_GPIO9	IO	PRU1 General Purpose Input/Output	R16	Y17	R15	V16
PR1_PRU1_GPIO10	IO	PRU1 General Purpose Input/Output	D14	C16	A15	
PR1_PRU1_GPIO11	IO	PRU1 General Purpose Input/Output	N1	R2	M2	N2
PR1_PRU1_GPIO12	IO	PRU1 General Purpose Input/Output	N4	R1	N1	N1
PR1_PRU1_GPIO13	IO	PRU1 General Purpose Input/Output	D13	B17	C14	
PR1_PRU1_GPIO14	IO	PRU1 General Purpose Input/Output	A15	B18	B15	
PR1_PRU1_GPIO15	IO	PRU1 General Purpose Input/Output	D9, H2	C9, H1	C11, E1	F1
PR1_PRU1_GPIO16	IO	PRU1 General Purpose Input/Output	B10, G3	D10, H2	A9, E2	E1
PR1_PRU1_GPIO17	IO	PRU1 General Purpose Input/Output	C14	D17	B14	
PR1_PRU1_GPIO18	IO	PRU1 General Purpose Input/Output	B14	A16	D13	B15
PR1_PRU1_GPIO19	IO	PRU1 General Purpose Input/Output	C7	C7	C8	C9

Table 5-48. PRU-ICSS IEP Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
PR0_IEP0_EDC_SYNC_OUT0	O	PRU-ICSS Industrial Ethernet Distributed Clock Sync Output	D15	C18		B16

Table 5-48. PRU-ICSS IEP Signal Descriptions (continued)

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
PR0_IEP0_EDC_SYNC_OUT1	O	PRU-ICSS Industrial Ethernet Distributed Clock Sync Output	A16, F17, N17	A19, J19, T19	C16, E15, M15	T18
PR0_IEP0_EDIO_DATA_IN_OUT30	IO	PRU-ICSS Industrial Ethernet Digital I/O Data Input/Output	D13, D17, P2	B17, E19, U2	C14, P3	T1
PR0_IEP0_EDIO_DATA_IN_OUT31	IO	PRU-ICSS Industrial Ethernet Digital I/O Data Input/Output	C15, C18	C19, E20		B17
PR1_IEP0_EDC_SYNC_OUT0	O	PRU-ICSS Industrial Ethernet Distributed Clock Sync Output	B14, U18	A16, Y19	D13, R16	B15, W18
PR1_IEP0_EDC_SYNC_OUT1	O	PRU-ICSS Industrial Ethernet Distributed Clock Sync Output	B15, N17	A18, T19	B16, M15	A17, T18
PR1_IEP0_EDIO_DATA_IN_OUT30	IO	PRU-ICSS Industrial Ethernet Digital I/O Data Input/Output	C12, N18	C14, U20	C12, L15	A14, R18
PR1_IEP0_EDIO_DATA_IN_OUT31	IO	PRU-ICSS Industrial Ethernet Digital I/O Data Input/Output	A14, T18	B16, W19	C13, N14	A15, V18

Table 5-49. PRU-ICSS MDIO Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
PR0_MDIO0_MDC	O	PRU-ICSS MDIO Clock	L18	R20	K16	P19
PR0_MDIO0_MDIO	IO	PRU-ICSS MDIO Data	L17	R19	K15	N17
PR1_MDIO0_MDC	O	PRU-ICSS MDIO Clock	A4, C13	A17, A6	A14	A16
PR1_MDIO0_MDIO	IO	PRU-ICSS MDIO Data	B15, B6	A18, B7	B16	A17

Table 5-50. PRU-ICSS UART Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
PR0_UART0_CTSn	I	PRU-ICSS UART Clear to Send (Active Low)	F17	J19	E15	
PR0_UART0_RTSn	O	PRU-ICSS UART Request to Send (Active Low)	G18	J20	E16	J18
PR0_UART0_RXD	I	PRU-ICSS UART Receive Data	C18	E20		
PR0_UART0_TXD	O	PRU-ICSS UART Transmit Data	D17	E19		
PR1_UART0_CTSn	I	PRU-ICSS UART Clear to Send (Active Low)	B16	B19	C15	
PR1_UART0_RTSn	O	PRU-ICSS UART Request to Send (Active Low)	D14	C16	A15	
PR1_UART0_RXD	I	PRU-ICSS UART Receive Data	A16	A19	C16	
PR1_UART0_TXD	O	PRU-ICSS UART Transmit Data	D13	B17	C14	

5.3.19 OSPI

Table 5-51. OSPI0 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
OSPI0_CLK	O	OSPI0 Clock	H2, K1, L2, N2	H1, M3, N1, N2	E1, J2, K2, L2	F1, J2, K1, M2
OSPI0_DQS	I	OSPI0 Data Strobe (DQS) or Loopback Clock input	L2, M1, M3	N2, P1, R4	J3, K2, L1	J2, K2, M1

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Table 5-51. OSPI0 Signal Descriptions (continued)

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
OSPI0_ECC_FAIL	I	OSPI0 ECC Failure Status Pin	A9, B10, H1, K3, M2	A11, D10, J3, M1, M2	A9, C10, G1, H1	A11, J1, J3
OSPI0_LBCLKO	O	OSPI0 Loopback Clock output	L3	T3	M1	L2
OSPI0_CSn0	O	OSPI0 Chip Select 0	H1, J2, P1	J3, L2, U4	F3, N3	G1, R1
OSPI0_CSn1	O	OSPI0 Chip Select 1	F4, R3	G2, T2	D2, M3	D2, R2
OSPI0_D0	IO	OSPI0 Data bit 0 (SOP0)	G3, N1, N2, P1	H2, M3, R2, U4	E2, L2, M2, N3	E1, M2, N2, R1
OSPI0_D1	IO	OSPI0 Data bit 1 (SOP1)	F1, J1, K3, N4	G1, K2, M2, R1	D1, G1, G3, N1	D1, J1, N1
OSPI0_D2	IO	OSPI0 Data bit 2	L1, M1, M4	P1, P2, T1	J3, K1, L3	K2, L1, P2
OSPI0_D3	IO	OSPI0 Data bit 3	K4, P3	L1, U1	H2, N2	H2, P1
OSPI0_D4	IO	OSPI0 Data bit 4	M1, M3, P3	P1, R4, U1	J3, L1, N2	K2, M1, P1
OSPI0_D5	IO	OSPI0 Data bit 5	K2, L1	K1, P2	G2, K1	G2, L1
OSPI0_D6	IO	OSPI0 Data bit 6	L1, L2, M4	N2, P2, T1	K1, K2, L3	J2, L1, P2
OSPI0_D7	IO	OSPI0 Data bit 7	J4, K1	L4, N1	H3, J2	H1, K1
OSPI0_RESET_OUT0	O	OSPI0 Reset Out 0	B9, D9, G1, G2, J1, J3	B11, C9, E1, J1, K2, K4	C11, D3, D8, F2, G3	B10, C1, F2
OSPI0_RESET_OUT1	O	OSPI0 Reset Out 1	A9, B8, H1	A11, B10, J3	B8, C10	A10, A11

Table 5-52. OSPI1 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
OSPI1_CLK	O	OSPI1 Clock	H2, K1, R17	H1, N1, W20	E1, J2, P16	F1, K1, V19
OSPI1_DQS	I	OSPI1 Data Strobe (DQS) or Loopback Clock input	P18	U19	L13	R17
OSPI1_ECC_FAIL	I	OSPI1 ECC Failure Status Pin	A9, M2, N17	A11, M1, T19	C10, H1, M15	A11, J3, T18
OSPI1_LBCLKO	O	OSPI1 Loopback Clock output	L3	T3	M1	L2
OSPI1_CSn0	O	OSPI1 Chip Select 0	J2, P17	L2, V20	F3, N16	G1, U19
OSPI1_CSn1	O	OSPI1 Chip Select 1	F4	G2	D2	D2
OSPI1_D0	IO	OSPI1 Data bit 0 (SOP0)	G3, N2, R18	H2, M3, V19	E2, L2, M14	E1, M2, U17
OSPI1_D1	IO	OSPI1 Data bit 1 (SOP1)	F1, K3, U17	G1, M2, Y18	D1, G1, P14	D1, J1, W17
OSPI1_D2	IO	OSPI1 Data bit 2	T17	W18	P15	V17
OSPI1_D3	IO	OSPI1 Data bit 3	U18	Y19	R16	W18
OSPI1_D4	IO	OSPI1 Data bit 4	T18	W19	N14	V18
OSPI1_D5	IO	OSPI1 Data bit 5	N18	U20	L15	R18
OSPI1_D6	IO	OSPI1 Data bit 6	M18	T20	M16	T19
OSPI1_D7	IO	OSPI1 Data bit 7	P16	V18	N15	U18
OSPI1_RESET_OUT0	O	OSPI1 Reset Out 0	B9, G1, N16	B11, K4, R17	D8, F2, L16	B10, F2, P18
OSPI1_RESET_OUT1	O	OSPI1 Reset Out 1	B8	B10	B8	A10

5.3.20 SDFM

Table 5-53. SDFM0 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
SDFM0_CLK0	I	SDFM Channel 0 Clock	B16	B19	C15	

Table 5-53. SDFM0 Signal Descriptions (continued)

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
SDFM0_CLK1	I	SDFM Channel 1 Clock	A16	A19	C16	
SDFM0_CLK2	I	SDFM Channel 2 Clock	B15	A18	B16	A17
SDFM0_CLK3	I	SDFM Channel 3 Clock	A15	B18	B15	
SDFM0_D0	I	SDFM Channel 0 Data	D14	C16	A15	
SDFM0_D1	I	SDFM Channel 1 Data	D13	B17	C14	
SDFM0_D2	I	SDFM Channel 2 Data	C13	A17	A14	A16
SDFM0_D3	I	SDFM Channel 3 Data	C14	D17	B14	

Table 5-54. SDFM1 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
SDFM1_CLK0	I	SDFM Channel 0 Clock	B14, B6	A16, B7	D13	B15
SDFM1_CLK1	I	SDFM Channel 1 Clock	B5, C12	B6, C14	C12	A14
SDFM1_CLK2	I	SDFM Channel 2 Clock	A3, B13	B15, B5	B12	B13
SDFM1_CLK3	I	SDFM Channel 3 Clock	A13, C6	A15, B4	A13	A13
SDFM1_D0	I	SDFM Channel 0 Data	A14, A16, A4	A19, A6, B16	C13, C16	A15
SDFM1_D1	I	SDFM Channel 1 Data	B15, B4, D11	A18, A5, D15	B13, B16	A17, B14
SDFM1_D2	I	SDFM Channel 2 Data	A15, A2, B12	A4, B14, B18	B15	
SDFM1_D3	I	SDFM Channel 3 Data	A12, A5	A14, A7		

5.3.21 System and Miscellaneous

5.3.21.1 Boot Mode Configuration

Table 5-55. Boot Mode Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
SOP0		Boot Mode configuration bit 0 (OSPI0_D0)	N1	R2	M2	N2
SOP1		Boot Mode configuration bit 1 (OSPI0_D1)	N4	R1	N1	N1
SOP2		Boot Mode configuration bit 2 (SPI0_CLK)	A11	A13	A12	A12
SOP3		Boot Mode configuration bit 3 (SPI0_D0)	C10	B12	A10	B12

5.3.21.2 Clocking

Table 5-56. XTAL Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
XTAL_XI	I	External Crystal (XTAL) Input	T1	Y3	T3	W3
XTAL_XO	O	External Crystal (XTAL) Output	R1	Y2	T2	W2

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Table 5-57. Output Clock Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
CLKOUT0	O	Output Clock 0	E1, M2	F2, M1	E3, H1	E3, J3
CLKOUT1	O	Output Clock 1	B16	B19	C15	

Table 5-58. External Reference Clock Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
EXT_REFCLK0	I	External Reference Clock Input	P2	U2	P3	T1

5.3.21.3 Emulation and Debug

Table 5-59. Trace Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
TRC_CLK	O	Trace Clock	D15, K16	C18, L20	G15	B16, J19
TRC_CTL	O	Trace Control	C15, G17	C19, K19	F14	B17, G17
TRC_DATA0	O	Trace Data 0	F15, K17	F20, N17	K14	E18, M18
TRC_DATA1	O	Trace Data 1	C18, K18	E20, N19	H14	L19
TRC_DATA2	O	Trace Data 2	D17, J18	E19, M18	G16	K19
TRC_DATA3	O	Trace Data 3	D18, J17	G18, M20	J14	C19, L17
TRC_DATA4	O	Trace Data 4	E16	F19	E13	D19
TRC_DATA5	O	Trace Data 5	F16	G19	D15	E19
TRC_DATA6	O	Trace Data 6	F18	H20	D14	G18
TRC_DATA7	O	Trace Data 7	G16	H19	D16	F18
TRC_DATA8	O	Trace Data 8	E17	H17		E17
TRC_DATA9	O	Trace Data 9	E18	G20		F19
TRC_DATA10	O	Trace Data 10	C16	B20		B18
TRC_DATA11	O	Trace Data 11	A17	E18		A18
TRC_DATA12	O	Trace Data 12	B18	F17		D18
TRC_DATA13	O	Trace Data 13	B17	D20		C18
TRC_DATA14	O	Trace Data 14	D16	C20		B19
TRC_DATA15	O	Trace Data 15	C17	D19		C17

Table 5-60. JTAG Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
TCK	I	JTAG Test Clock Input	B3	D4	C6	B6
TDI	I	JTAG Test Data Input	C5	C5	D5	C7
TDO	O	JTAG Test Data Output	C4	E5	B5	A7
TMS	IO	JTAG Test Mode Select Input	D5	D6	C7	B7

5.3.21.4 SYSTEM

Table 5-61. System Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
PORz	I	Device Power-On (PORz) cold reset	R2	V3	P2	T2
SAFETY_ERRORn	IO	ESM Safety Error Signal	D4, M2, P2	E3, M1, U2	B3, H1, P3	C5, J3, T1
WARMRSTn	IO	Warm Reset Request (Input) / Warm Reset Status (Output)	C3	G3	C3	C3

5.3.21.5 USB0

Table 5-62. USB0 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
USB0_DM	IO	USB 2.0 Differential Data (negative)	U3	W1	P1	U1
USB0_DP	IO	USB 2.0 Differential Data (positive)	V2	V1	R1	V1
USB0_DRVVBUS	O	USB VBUS control output (active high)	B8, M2, P2	B10, M1, U2	B8, H1, P3	A10, J3, T1

5.3.21.6 VMON

Table 5-63. VMON Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
VSYS_MON	-	External Voltage Monitor with 0.9 V (+/-3%) setpoint.	U2	Y4	R5	V5

Table 5-64. No Connection Description

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
NC	NC	No Connection	J15, R7, R9, T15, T7, U4, U5, U6, U7, U8, U9, V3, V4, V5, V6, V7, V8	U17		

5.3.22 UART

Table 5-65. UART0 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
UART0_CTSn	I	UART Clear to Send (active low)	A5, B7	A7, D8	A7	A9
UART0_RTSn	O	UART Request to Send (active low)	C6, C7	B4, C7	C8	C9
UART0_RXD	I	UART Receive Data	A7, B6	A8, B7	A6	A8
UART0_TXD	O	UART Transmit Data	A4, A6	A6, B8	B6	B8

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Table 5-66. UART1 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
UART1_CTSn	I	UART Clear to Send (active low)	B15, G4	A18, J2	B16	A17
UART1_DCDn	I	UART Data Carrier Detect (Active Low)	J4, N1	L4, R2	H3, M2	H1, N2
UART1_DSRn	I	UART Data Set Ready (Active Low)	V17	W16	R14	V15
UART1_DTRn	O	UART Data Terminal Ready (Active Low)	K1, K3	M2, N1	G1, J2	J1, K1
UART1_RIn	I	UART Ring Indicator	K4, N4	L1, R1	H2, N1	H2, N1
UART1_RTSn	O	UART Request to Send (active low)	B12, J2	B14, L2	F3	G1
UART1_RXD	I	UART Receive Data	A9, L3, M2, U18	A11, M1, T3, Y19	C10, H1, M1, R16	A11, J3, L2, W18
UART1_TXD	O	UART Transmit Data	B9, G1, L2, M3, T18	B11, K4, N2, R4, W19	D8, F2, K2, L1, N14	B10, F2, J2, M1, V18

Table 5-67. UART2 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
UART2_CTSn	I	UART Clear to Send (active low)	C13, D14, H1	A17, C16, J3	A14, A15	A16
UART2_RTSn	O	UART Request to Send (active low)	A12, B16, F3, J3, R3	A14, B19, F1, J1, T2	C15, F4, M3	E2, R2
UART2_RXD	I	UART Receive Data	B5, B8, D13, J1	B10, B17, B6, K2	B8, C14, G3	A10
UART2_TXD	O	UART Transmit Data	A16, A3, A8, G4	A10, A19, B5, J2	C16, C9	B9

Table 5-68. UART3 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
UART3_CTSn	I	UART Clear to Send (active low)	C10, G18, K1, K2, K3, N2	B12, J20, K1, M2, M3, N1	A10, E16, G1, G2, J2, L2	B12, G2, J1, J18, K1, M2
UART3_RTSn	O	UART Request to Send (active low)	A2, B11, G17, J1	A4, C12, K19, K2	A11, F14, G3	B11, G17
UART3_RXD	I	UART Receive Data	B12, C11, C7, D15, K16, P1	B13, B14, C18, C7, L20, U4	B11, C8, G15, N3	B16, C13, C9, J19, R1
UART3_TXD	O	UART Transmit Data	A11, A12, B7, C15, J17, R3	A13, A14, C19, D8, M20, T2	A12, A7, J14, M3	A12, A9, B17, L17, R2

Table 5-69. UART4 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
UART4_CTSn	I	UART Clear to Send (active low)	A14, T16	B16, Y16	C13, T14	A15, W15
UART4_RTSn	O	UART Request to Send (active low)	B14, V17	A16, W16	D13, R14	B15, V15
UART4_RXD	I	UART Receive Data	A10, D11, H1, H2, N18	A12, D15, H1, J3, U20	B10, B13, E1, L15	B14, F1, R18
UART4_TXD	O	UART Transmit Data	C12, C9, G3, J3, N17	C14, D11, H2, J1, T19	B9, C12, E2, M15	A14, E1, T18

Table 5-70. UART5 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
UART5_CTSn	I	UART Clear to Send (active low)	B15, D13	A18, B17	B16, C14	A17
UART5_RTSn	O	UART Request to Send (active low)	A16	A19	C16	
UART5_RXD	I	UART Receive Data	A15, C13, D9, R16, V2	A17, B18, C9, V1, Y17	A14, B15, C11, R1, R15	A16, V1, V16
UART5_TXD	O	UART Transmit Data	B10, B15, C14, P15, U3	A18, D10, D17, W1, W17	A9, B14, B16, P1, T15	A17, U1, W16

5.3.23 XBAR

Table 5-71. Output XBAR Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
XBAROUT0	O	OUTPUTXBAR Signal 0	C11, R3	B13, T2	B11, M3	C13, R2
XBAROUT1	O	OUTPUTXBAR Signal 1	A11, C9	A13, D11	A12, B9	A12
XBAROUT2	O	OUTPUTXBAR Signal 2	A10, C10	A12, B12	A10, B10	B12
XBAROUT3	O	OUTPUTXBAR Signal 3	B10, B11	C12, D10	A11, A9	B11
XBAROUT4	O	OUTPUTXBAR Signal 4	A7, D9	A8, C9	A6, C11	A8
XBAROUT5	O	OUTPUTXBAR Signal 5	A6, A9	A11, B8	B6, C10	A11, B8
XBAROUT6	O	OUTPUTXBAR Signal 6	B9, G17	B11, K19	D8, F14	B10, G17
XBAROUT7	O	OUTPUTXBAR Signal 7	D7, K16	B9, L20	B7, G15	J19
XBAROUT8	O	OUTPUTXBAR Signal 8	C8, K17	A9, N17	A8, K14	M18
XBAROUT9	O	OUTPUTXBAR Signal 9	C7	C7	C8	C9
XBAROUT10	O	OUTPUTXBAR Signal 10	B7	D8	A7	A9
XBAROUT11	O	OUTPUTXBAR Signal 11	D16, K18	C20, N19	H14	B19, L19
XBAROUT12	O	OUTPUTXBAR Signal 12	C17, J18	D19, M18	G16	C17, K19
XBAROUT13	O	OUTPUTXBAR Signal 13	D15, J17	C18, M20	J14	B16, L17
XBAROUT14	O	OUTPUTXBAR Signal 14	C15, L17	C19, R19	K15	B17, N17
XBAROUT15	O	OUTPUTXBAR Signal 15	L18, P2	R20, U2	K16, P3	P19, T1

Table 5-72. External ADC Channel Select XBAR Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
ADC_EXTCH_XBAROUT0	O	External ADC Channel Select XBAR Signal 0	C11, C13	A17, B13	A14, B11	A16, C13
ADC_EXTCH_XBAROUT1	O	External ADC Channel Select XBAR Signal 1	A11, C14	A13, D17	A12, B14	A12
ADC_EXTCH_XBAROUT2	O	External ADC Channel Select XBAR Signal 2	C10, C12	B12, C14	A10, C12	A14, B12
ADC_EXTCH_XBAROUT3	O	External ADC Channel Select XBAR Signal 3	B11, D11	C12, D15	A11, B13	B11, B14
ADC_EXTCH_XBAROUT4	O	External ADC Channel Select XBAR Signal 4	C9, G17, P15	D11, K19, W17	B9, F14, T15	G17, W16
ADC_EXTCH_XBAROUT5	O	External ADC Channel Select XBAR Signal 5	A10, K16, R16	A12, L20, Y17	B10, G15, R15	J19, V16
ADC_EXTCH_XBAROUT6	O	External ADC Channel Select XBAR Signal 6	B10, F15, K17	D10, F20, N17	A9, K14	E18, M18

ADVANCE INFORMATION

Table 5-72. External ADC Channel Select XBAR Signal Descriptions (continued)

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
ADC_EXTCH_XBAROUT7	O	External ADC Channel Select XBAR Signal 7	C18, D9, K18	C9, E20, N19	C11, H14	L19
ADC_EXTCH_XBAROUT8	O	External ADC Channel Select XBAR Signal 8	B15, J18	A18, M18	B16, G16	A17, K19
ADC_EXTCH_XBAROUT9	O	External ADC Channel Select XBAR Signal 9	A15, J17	B18, M20	B15, J14	L17

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1) (2)

PARAMETER		MIN	MAX	UNIT
VDD	SOC VDD core supply	–0.5	1.5	V
VDDAR1	SRAM Array Supply 1	–0.5	1.5	V
VDDAR2	SRAM Array Supply 2	–0.5	1.5	V
VDDAR3	SRAM Array Supply 3	–0.5	1.5	V
VDDS18	1.8V IO Bias Supply from Bias LDO routed through Board	–0.5	2.1	V
VDDS33	3.3V IO Supply	–0.5	4.0	V
VDDA18_OSC_PLL	1.8V Analog Supply for PLL. Routed from the 1.8V Analog LDO out through Board	–0.5	2.1	V
VDDA33	Analog 3.3V Supply	–0.5	4.0	V
VDDA18	1.8V Analog Supply. Routed from the 1.8V Analog LDO out through Board	–0.5	2.1	V
IO Pin Steady State Voltage	3.3V LVCMOS IO Buffer	–0.3	VDDS33(3) + 0.3	V
	3.3V I2C Open-Drain IO Buffers	–0.3	VDDS33(3) + 0.3	V
	XTAL Pad	–0.5	2.1	V
Transient Overshoot and Undershoot	All Other IO Terminals	–0.3	VDDS33(3) + 0.2 × VDDS33(3) for up to 20% of signal period	V
	XTAL Pad 20% of VDDA18_OSC_PLL for up to 20% of signal period		0.2 × VDDA18_OSC_PLL	V
Latch Up Performance Class II (150°C)	Latch-up I-test Performance (Current-Pulse Injection on each IO pin)		±100	mA
	Latch-up Overvoltage Performance (Voltage Injection on each IO pin)		1.5 × VDDS33	V
Output current	Digital output (per pin), I_{OUT}	–20	20	mA
Storage temperature(4)	T_{stg}	–55	155	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to VSS, unless otherwise noted.
(3) VDDS33 is the voltage on the corresponding power-supply pin(s) for the IC.
(4) Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see the *Semiconductor and IC Package Thermal Metrics Application Report*.

ADVANCE INFORMATION

6.2 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION		MIN	NOM	MAX	UNIT
VDD	SOC VDD Core Supply		1.140	1.25	1.32	V
VDDAR1, VDDAR2, VDDAR3	SRAM Array Supplies		1.140	1.25	1.32	V
VDDS18	1.8V IO Bias Supply from Bias LDO routed through board		1.710	1.800	1.890	V
VDDS33	3.3V IO Supply		3.135	3.300	3.465	V
VDDA18_OSC_PLL	1.8V Analog supply for PLL. Routed from the Analog LDO out through board		1.710	1.800	1.890	V
VDDA33	Analog 3.3V Supply		3.135	3.300	3.465	V
VDDA18	1.8V Analog supply. Routed from 1.8V Analog LDO out through Board		1.710	1.800	1.890	V
Tj	Operating junction temperature range	Extended Automotive	-40		150	°C
T_J	Operating junction temperature range	Extended Industrial	–40		125	°C

ADVANCE INFORMATION

6.3 Electrical Characteristics

Note

The interfaces or signals described in Section 6.3.1 *Digital and Analog IO Electrical Characteristics* correspond to the interfaces or signals available in multiplexing mode 0 (Primary Function).

All interfaces or signals multiplexed on the balls described in these tables have the same DC electrical characteristics, unless multiplexing involves a PHY and GPIO combination, in which case different DC electrical characteristics are specified for the different multiplexing modes (Functions).

AM261x has 1.8V or 3.3V compatible IOs based on supply connected to VDDS1833_FLASH0 and VDDS1833_FLASH1. Electrical characteristics of 1.8V IOs will be updated in future revisions of this datasheet.

6.3.1 Digital and Analog IO Electrical Characteristics

over recommended operating conditions (unless otherwise noted). The below are for IOs powered at 3.3V

PARAMETER		MIN	TYP	MAX	UNIT
PORz IO					
V_{IH}	High-Level Input Voltage	1.35			V
V_{IL}	Low-Level Input Voltage			0.5	V
V_{HYS}	Hysteresis Voltage at an Input	0.070			V
I_L	Input Leakage Current	–2		2	µA
Warm Reset IO					
V_{IH}	High-Level Input Voltage	2			V
V_{IL}	Low-Level Input Voltage			0.8	V
V_{HYS}	Hysteresis Voltage at an Input	0.347			V
V_{OL}	Low Level Output Voltage, Driver Enabled : I_{OL} = 6 mA			0.45	V
I_L	Input Leakage Current, Receiver Disabled, Pull Disabled	–57			µA
TCK IO					
V_{IH}	High-Level Input Voltage	2.15			V
V_{IL}	Low-Level Input Voltage			0.55	V
V_{HYS}	Hysteresis Voltage at an Input	0.4			V
I_L	Input Leakage Current, Receiver Disabled, Pull Disabled	–3.9	8.9	17.2	µA
	Input Leakage Current, Receiver Disabled, Pullup Enabled		106.9	128.2	µA
	Input Leakage Current, Receiver Disabled, Pulldown Enabled		100.3	130.3	µA
I2C OD IOs					
V_{IH}	High-Level Input Voltage	2			V
V_{IL}	Low-Level Input Voltage			0.8	V
V_{HYS}	Hysteresis Voltage at an Input	0.165			V
I_L	Input Leakage Current, Receiver Disabled, Pull Disabled	–18		18	µA
V_{OL}	Low Level Output Voltage, Driver Enabled : I_{OL} = 3 mA			0.45	V
All Other LVCMOS					
V_{IH}	High- Level Input Voltage	2			V
V_{IL}	Low-Level Input Voltage			0.8	V
V_{HYS}	Hysteresis Voltage at an Input	0.265			V
V_{OL}	Low Level Output Voltage, Driver Enabled : I_{OL} = 6 mA			0.45	V
V_{OH}	High Level Output Voltage, Driver Enabled : I_{OH} = 6 mA	VDDS33(1) – 0.45			V

ADVANCE INFORMATION

over recommended operating conditions (unless otherwise noted). The below are for IOs powered at 3.3V

PARAMETER		MIN	TYP	MAX	UNIT
I_L	Input Leakage Current, Receiver Disabled, Pull Disabled	–18		18	µA
	Input Leakage Current, Receiver Disabled, Pullup Enabled	–243	–100	–19	µA
	Input Leakage Current, Receiver Disabled, Pulldown Enabled	51	100	210	µA

(1) VDDS33 is the voltage on the corresponding power-supply pins(VDDS33, VDDS1833_FLASH0, VDDS1833_FLASH1) on the IC.

6.4 Thermal Resistance Characteristics

This section provides the thermal resistance characteristics used on this device.

For reliability and operability concerns, the maximum junction temperature of the device has to be at or below the T_J value identified in Recommended Operating Conditions.

6.4.1 Package Thermal Characteristics

It is recommended to perform thermal simulations at the system level with the worst-case device power consumption.

PARAMETER	DESCRIPTION	°C/W(1) (2)	AIR FLOW (m/s) (3)
$R\Theta_{JC}$	Junction-to-case	TBD	N/A
$R\Theta_{JB}$	Junction-to-board	TBD	N/A
$R\Theta_{JA}$	Junction-to-free air	TBD	0
$R\Theta_{JA}$	Junction-to-moving air	TBD	1
		TBD	2
		TBD	3
Ψ_{JT}	Junction-to-package top	TBD	0
		TBD	1
		TBD	2
		TBD	3
Ψ_{JB}	Junction-to-board	TBD	0
		TBD	1
		TBD	2
		TBD	3

(1) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)
- JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-6, Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)
- JESD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-9, Test Boards for Area Array Surface Mount Packages

(2) °C/W = degrees Celsius per watt
(3) m/s = meters per second

ADVANCE INFORMATION

7 Detailed Description

7.1 Overview

The AM261x Sitara Arm® Microcontrollers are built to meet the complex real-time processing and control needs of next generation industrial and automotive embedded projects. AM261x uniquely combines advanced computing with industry leading real-time control peripherals to meet the growing performance needs of applications such as HEV/EV (on-board chargers, DC-DC converters, Battery Management Systems), Two axis Servo drive, Industrial Digital Power control(energy storage, String Inverters), and other general real-time constrained systems. AM261x combines up to two Cortex-R5F MCUs, a real-time control subsystem (CONTROLSS), a Hardware Security Module (HSM), and two instances of Sitara's TSN-enabled PRU-ICSS, making AM261x designed for advanced motor control and digital power control applications.

The R5F cores are arranged in cluster with 256KB of shared tightly coupled memory (TCM) along with 1.5MB of shared SRAM. The Arm® cores can be optionally programmed to run in lock-step option for different functional safety configurations. Extensive ECC is included on on-chip memory, peripherals, and interconnect for enhanced reliability. Cryptographic acceleration and secure boot are also available on AM261x devices in addition to granular firewalls managed by the HSM for developers to design the most secure systems.

The Real-Time Control Subsystem (CONTROLSS) is a revolutionary subsystem integrated into the device. CONTROLSS contains multiple digital and analog control peripherals including: ADC, CMPSS, EPWM, ECAP, and EQEP, among others to enable efficient execution of critical sense/process/actuate real-time signal chain control loops. The integrated crossbar (XBAR) infrastructure enables flexible configuration and routing of external signals to internal ports and internal signals to external pins.

The PRU-ICSS in AM261x provides the flexible industrial communications capability necessary to run TSN, EtherCAT®, PROFINET®, Ethernet/IP™, or for standard Ethernet connectivity and custom I/O interfacing. The PRU also enables additional interfaces in the SoC including sigma delta decimation filters and absolute encoder interfaces. The CPSW interface also provides two standard Ethernet ports.

TI provides a complete set of microcontroller software and development tools for the AM261x family of microcontrollers in addition to multiple pin-to-pin compatible devices for scalability and ease of use.

7.2 Processor Subsystems

7.2.1 Arm Cortex-R5F Subsystem

The R5FSS is a dual-core implementation of the Arm® Cortex®-R5F processor configured for dual-core (split) or lockstep modes of operation. It also includes accompanying memories (L1 caches and tightly-coupled memories), standard Arm® CoreSight™ debug and trace architecture, integrated Vectored Interrupt Manager (VIM), ECC Aggregators, and various wrappers for protocol conversion and address translation for easy integration into the SoC. The device has one R5FSS module for a total possible 2x functional cores (dual-core mode) or 1x functional cores (lockstep mode).

Note

The Arm® Cortex®-R5F processor is a Cortex-R5 processor that includes the optional Floating-point Unit (FPU) extension.

For more information, see *R5FSS* section in *Processors and Accelerators* chapter in the device TRM.

8 Applications, Implementation, and Layout

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Device Connection and Layout Fundamentals

8.1.1 External Oscillator

For more information about External Oscillators, see the *Input Clocks/Oscillators* section.

8.1.2 JTAG, EMU, and TRACE

Texas Instruments supports a variety of eXtended Development System (XDS) JTAG controllers with various debug capabilities beyond only JTAG support. A summary of this information is available in the XDS Target Connection Guide.

For recommendations on JTAG, EMU, and TRACE routing, see the Emulation and Trace Headers Technical Reference Manual

8.1.3 Hardware Reference Design and Guidelines

For details regarding creating PCB systems based on the AM261x family of MCU devices, please see the reference design LP-AM261. A Hardware design guideline document is planned for future release.

9 Device and Documentation Support

9.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microcontrollers (MCUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, XAM2612AOFFHIZFB). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

For orderable part numbers of AM261x devices , see the Package Option Addendum of this document, the TI website (ti.com), or contact your TI sales representative.

9.1.1 Device Naming Convention

Table 9-1. Nomenclature Description

FIELD PARAMETER	FIELD DESCRIPTION	VALUE	DESCRIPTION
Field Parameter	Field Description	Value	Description
a	Device evolution stage	X	Prototype
		P	Preproduction (production test flow, no reliability data)
		BLANK	Production - Released to market
BBBBBB	Base production part number	AM2612	2× R5F
		AM2611	1× R5F
r	Device revision	A	Silicon Revision 1.0
S	Special Features	TBD	Reserved
Z	Device Operating Performance Points	O	500MHz, 1.5MB (Overdrive, full mem)
f	Features(see Device Comparison, Device Comparison)	D	ICSS-PRU / No EtherCAT
		E	ICSS-PRU / EtherCAT
		F	ICSS-PRU / EtherCAT / Pre-integrated Stacks
		G	ICSS-PRU/Protocols (TBD)
Y	Functional Safety	G	Non-Functional Safety
		F	Functional Safety
s	Safety & Security	G	Non-security
		1-9	Dummy key devices
		H-Z	Production key HS devices
T	Temp (Junction)	I	-40°C to 125°C (Extended Industrial)
		M	-40°C to 150°C (Extended Automotive)
PPP	Package Designator	ZCZ	ZCZ NFBGA-N324 (15 mm × 15 mm) Package
		ZFG	ZFG NFBGA-N304 (13.25 mm × 13.25 mm) Package
		ZEJ	ZEJ NFBGA-N256 (13 mm × 13 mm) Package
		ZNC	ZNC NFBGA-N293 (10 mm × 10 mm) Package
Q1	Automotive Designator and Max Junction Temperature	Q1	Auto Qualified (AEC-Q100) -40°C to 150°C - Extended Automotive
		BLANK	Standard -40°C to 125°C - Extended Industrial
XXXXXXX			Lot Trace Code (LTC)
YYY			Production Code; For TI use only
O			Pin one designator
G1			ECAT - Green package designator

ADVANCE INFORMATION

9.2 Tools and Software

The following products support development for AM261x platforms:

Development Tools

Code Composer Studio™ Integrated Development Environment Code Composer Studio (CCS) Integrated Development Environment (IDE) is a development environment that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

SysConfig-PinMux Tool The SysConfig-PinMux Utility is a software tool which provides a Graphical User Interface for configuring pin multiplexing settings, resolving conflicts and specifying I/O cell characteristics for TI Embedded Processor devices. The tool can be used to automatically calculate the optimal pinmux configuration to satisfy entered system requirements. The tool will generate output C header/code files that can be imported into software development kits (SDKs) and used to configure customer's software to meet custom hardware requirements.

For a complete listing of development-support tools for the processor platform, visit the Texas Instruments website at ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

9.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The following documents are provided to describe the AM261x device.

AM261x Technical Reference Manual Details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the AM261x family of devices.

AM261x TRM Register Addendum Details the memory mapped register information for each peripheral and subsystem in the AM261x family of devices.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

Ethernet/IP™ is a trademark of ODVA, INC..
CoreSight™ is a trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.
Code Composer Studio™ and TI E2E™ are trademarks of Texas Instruments.
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EtherCAT® is a registered trademark of Beckhoff Automation GmbH.
PROFINET® is a registered trademark of PROFINET International.
IO-Link® is a registered trademark of PROFIBUS Nutzerorganisation e.V. eingetragener verein (e.v.) FED REP GERMANY.
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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

Changes from September 1, 2024 to November 6, 2024 (from Revision * (September 2024) to Revision A (November 2024)) **Page**

- Added Specifications, Detailed description, Applications, Implementations and Layout sections....1
- Updated Features section to mention ECC for OCSRAM, EMAC support in PRU-ICSS, TSN in CPSW....1
- Updated Device Naming Convention and Package comparison tables....6
- Updated Device junction temperature for Extended Industrial Temperature....6

ADVANCE INFORMATION

11 Mechanical, Packaging, and Orderable Information

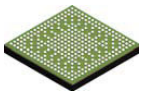
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

To learn more about TI packaging, visit the Packaging information website.

ADVANCE INFORMATION

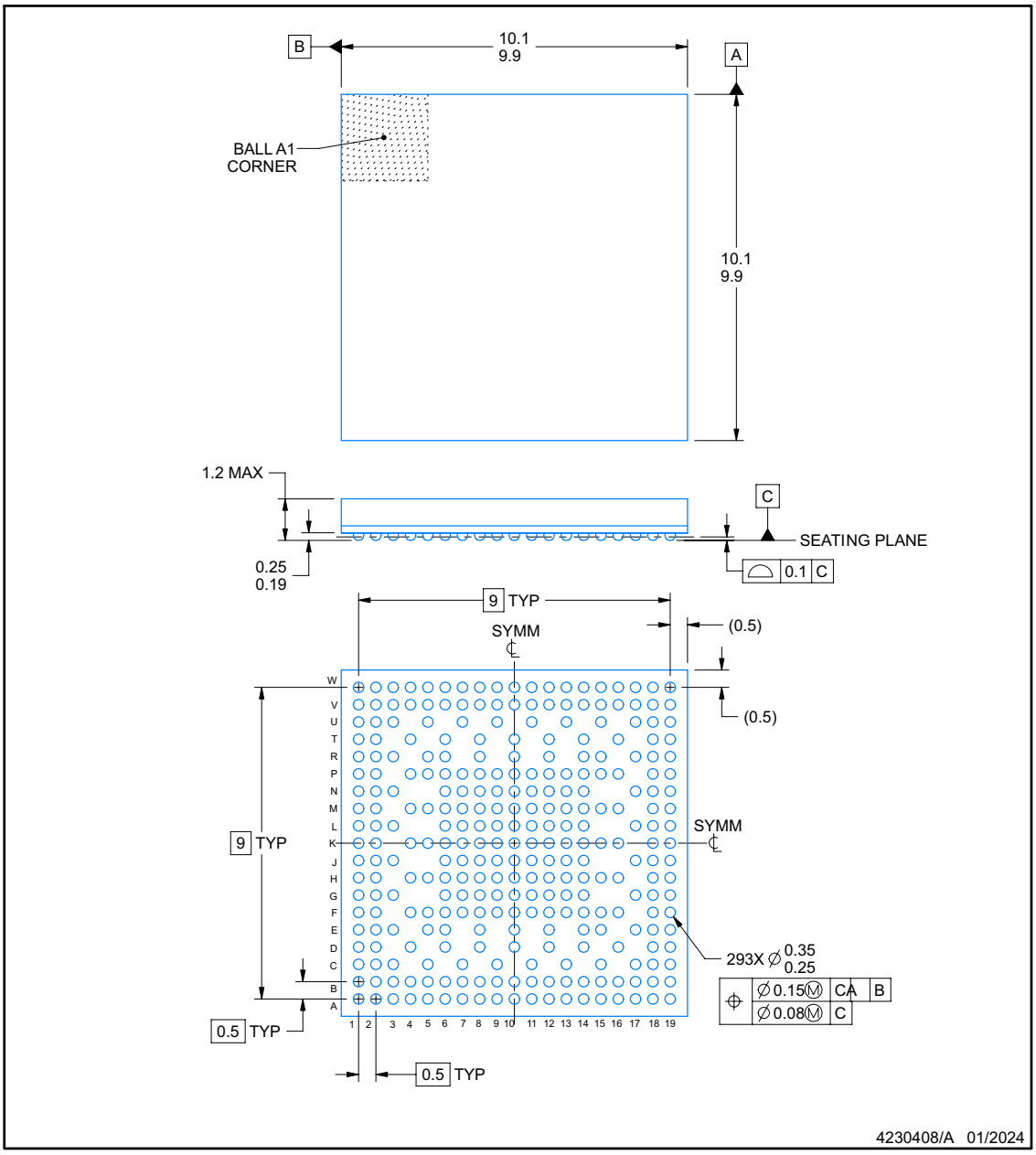
PACKAGE OUTLINE

ZNC0293A



NFBGA - 1.2 mm max height

PLASTIC BALL GRID ARRAY



NOTES:

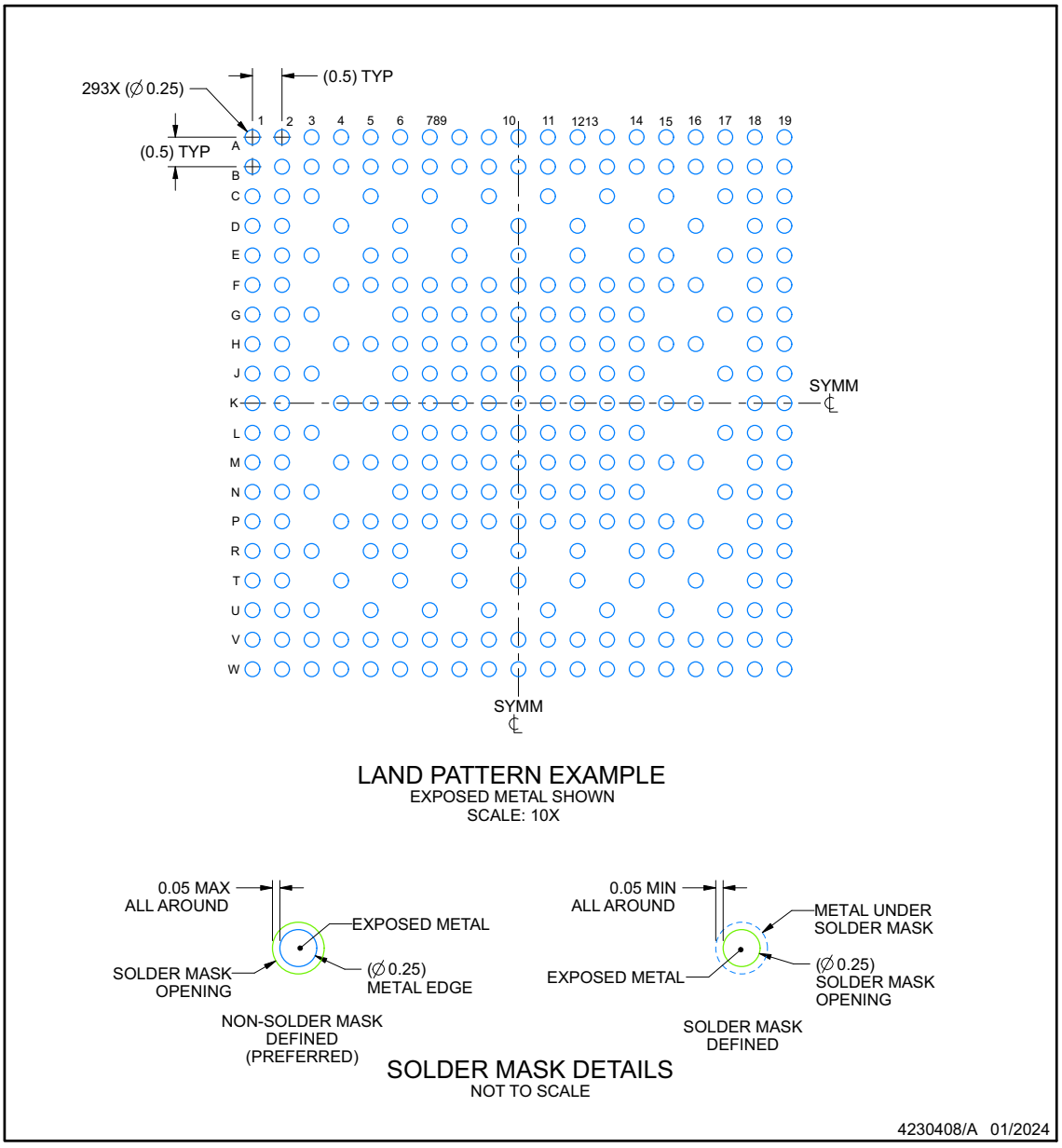
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

ZNC0293A

NFBGA - 1.2 mm max height

PLASTIC BALL GRID ARRAY



NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).

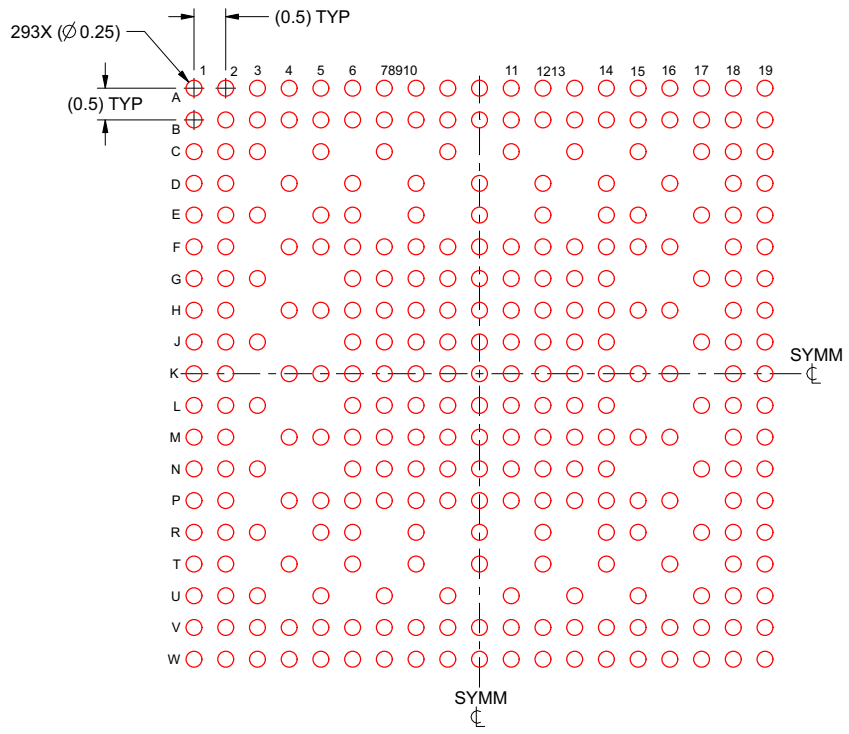
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

ZNC0293A — NFBGA - 1.2 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.100 mm THICK STENCIL
SCALE: 10X

4230408/A 01/2024

NOTES: (continued)

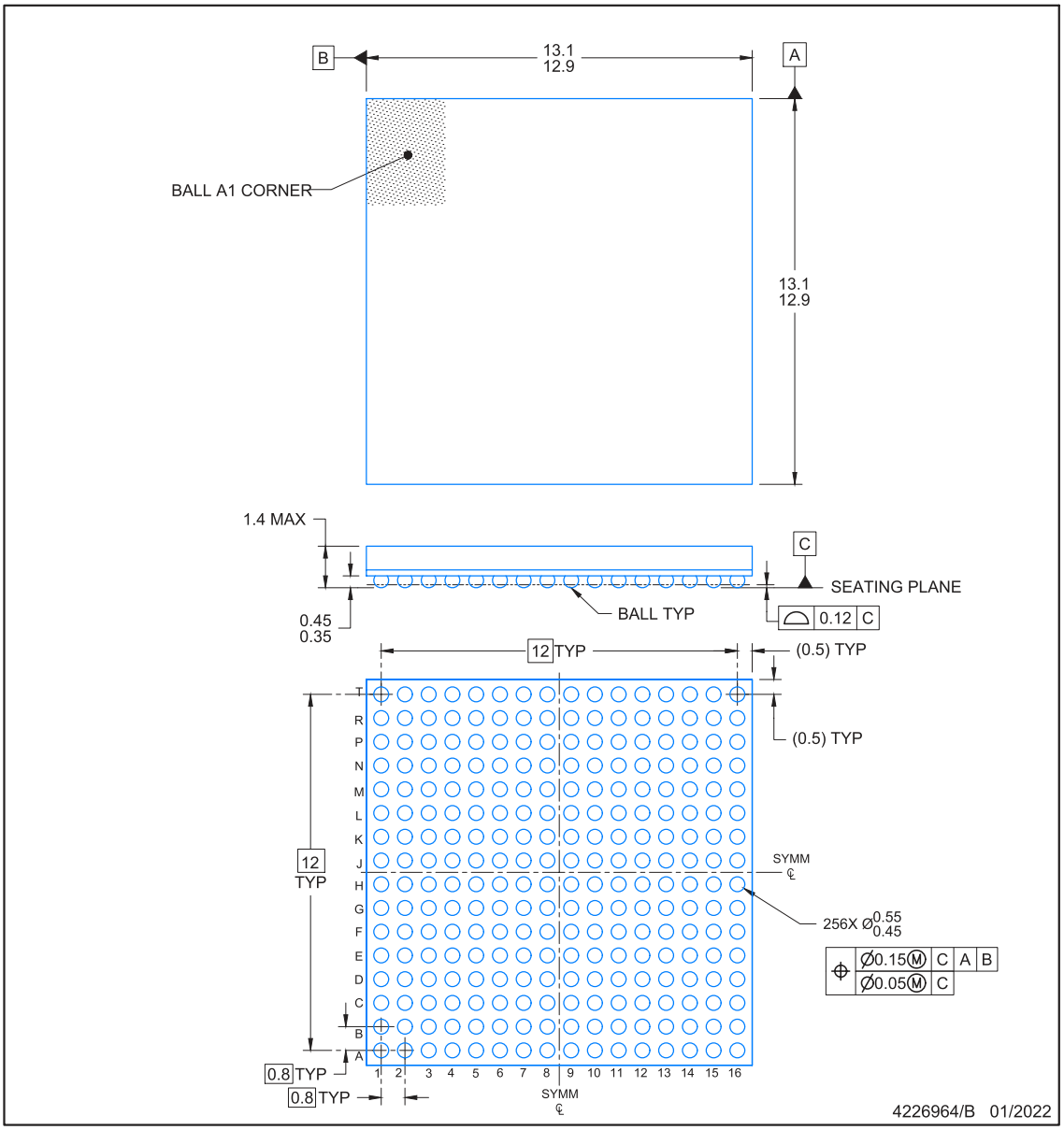
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

ZEJ0256A

NFBGA - 1.4 mm max height

PLASTIC BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

ADVANCE INFORMATION

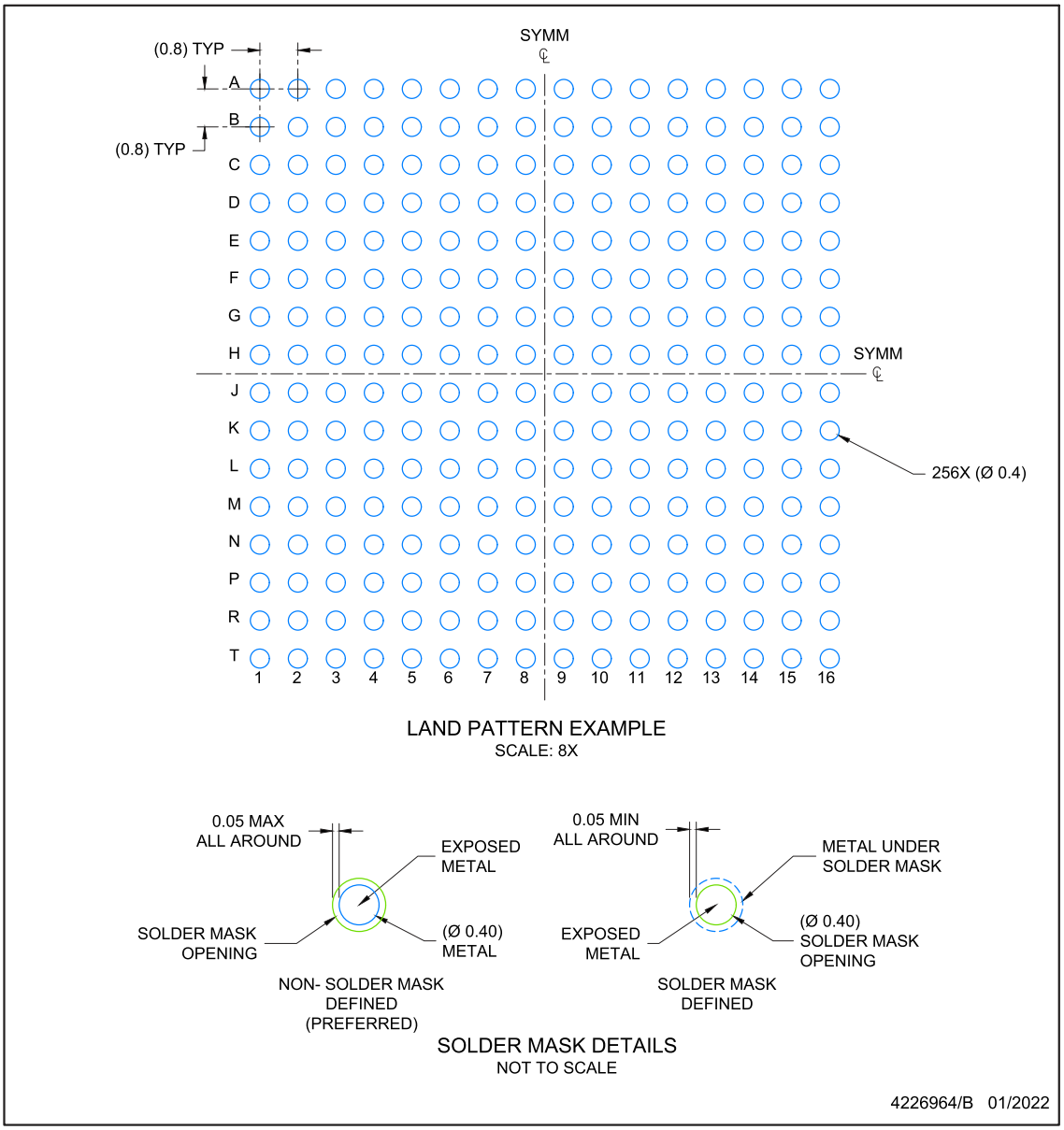
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

ZEJ0256A

NFBGA - 1.4 mm max height

PLASTIC BALL GRID ARRAY



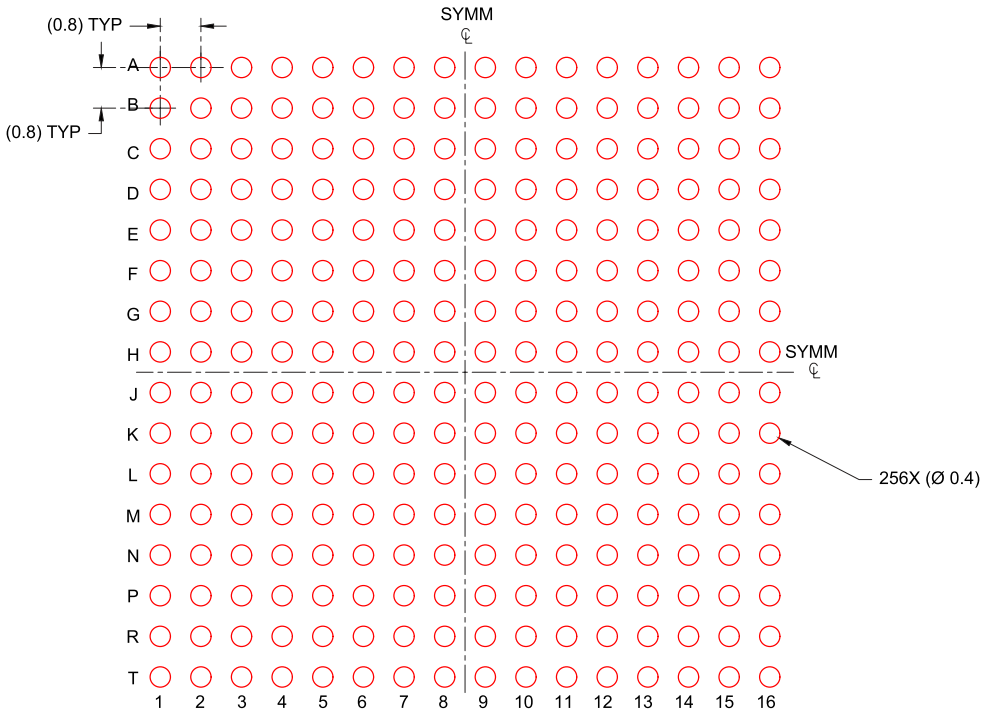
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

ZEJ0256A — **NFBGA - 1.4 mm max height**

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.150 mm THICK STENCIL
SCALE: 8X

4226964/B 01/2022

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

ADVANCE INFORMATION

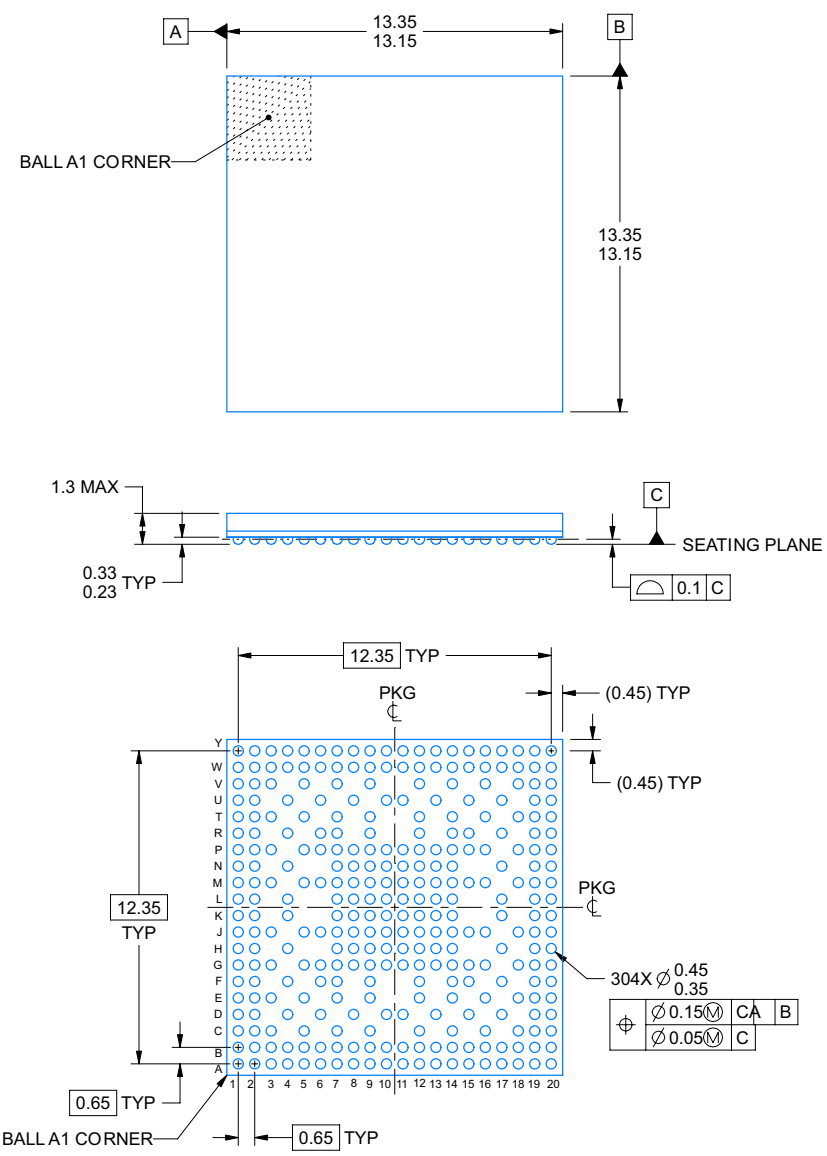
ADVANCE INFORMATION

PACKAGE OUTLINE

ZFG0304A

NFBGA - 1.3 mm max height

PLASTIC BALL GRID ARRAY



NOTES:

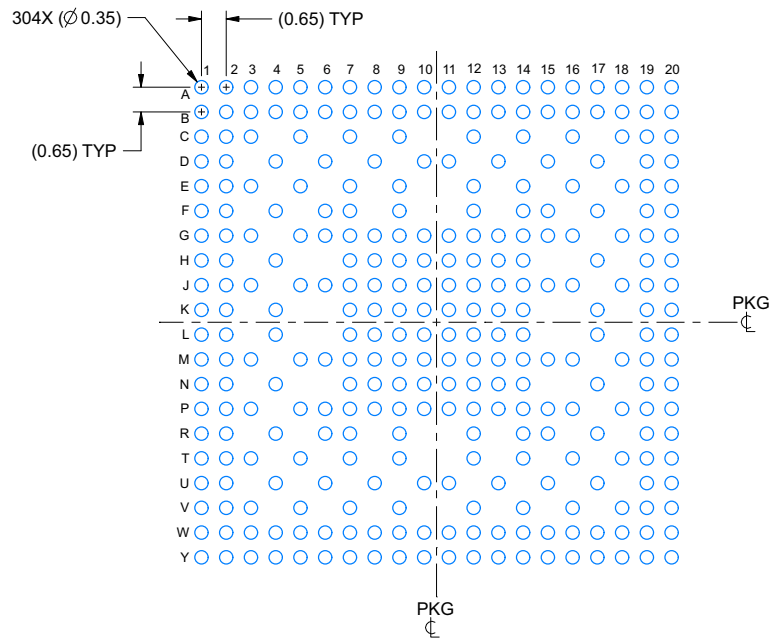
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

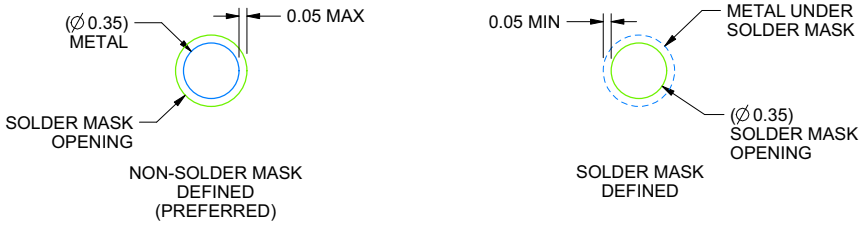
ZFG0304A

NFBGA - 1.3 mm max height

PLASTIC BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS
NOT TO SCALE

4230188/A 11/2023

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).

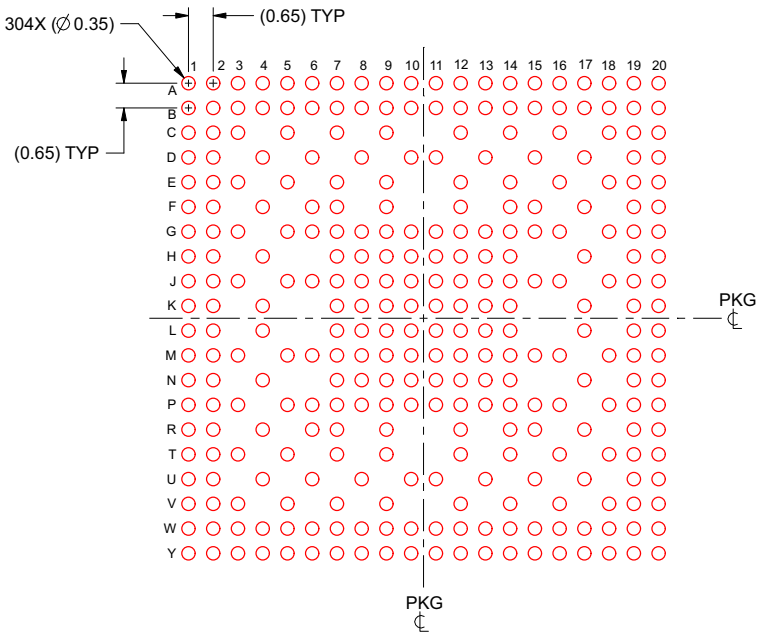
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

ZFG0304A — NFBGA - 1.3 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4230188/A 11/2023

NOTES: (continued)

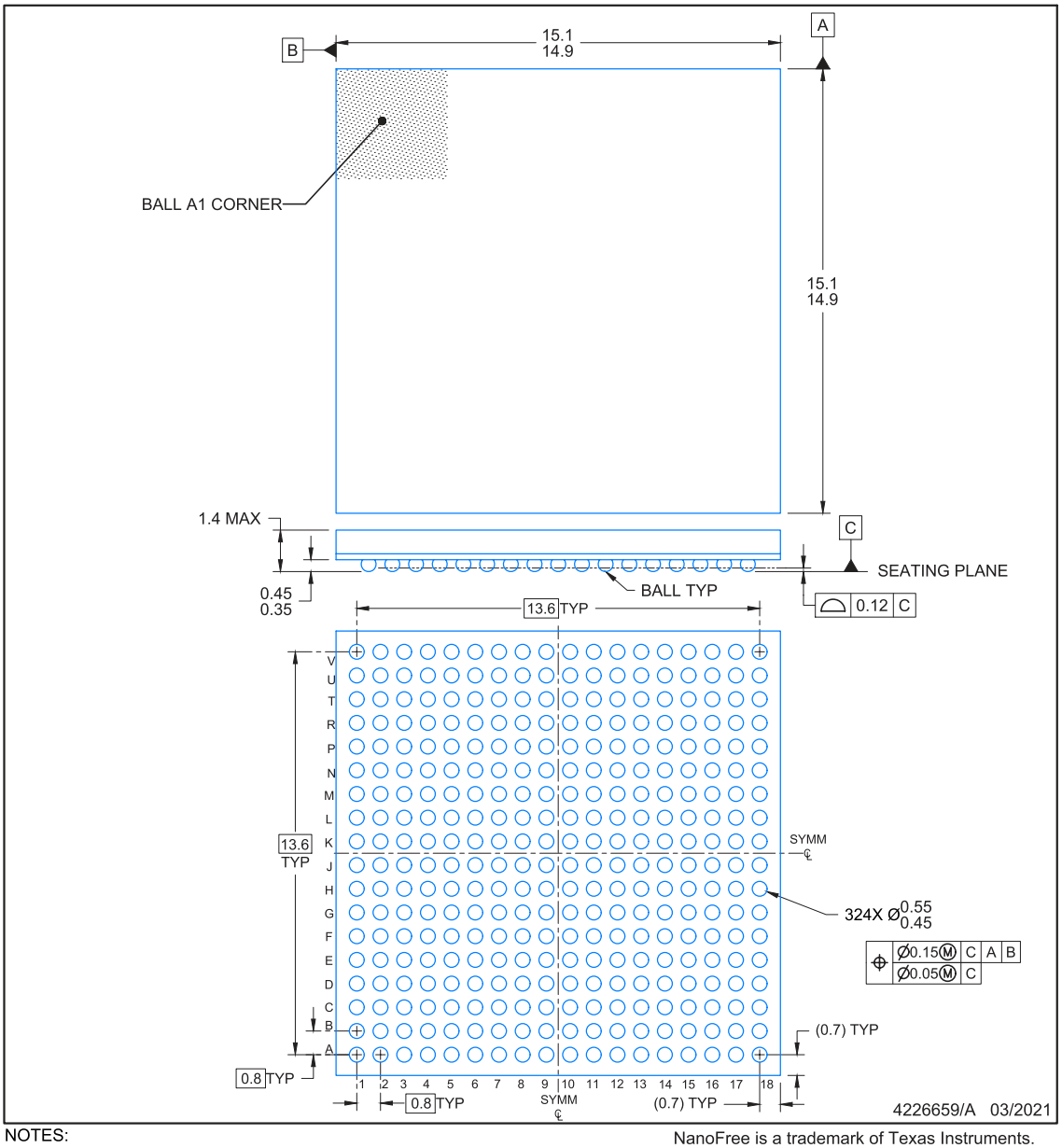
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

ZCZ0324A

NFBGA - 1.4 mm max height

PLASTIC BALL GRID ARRAY



NOTES:

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1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

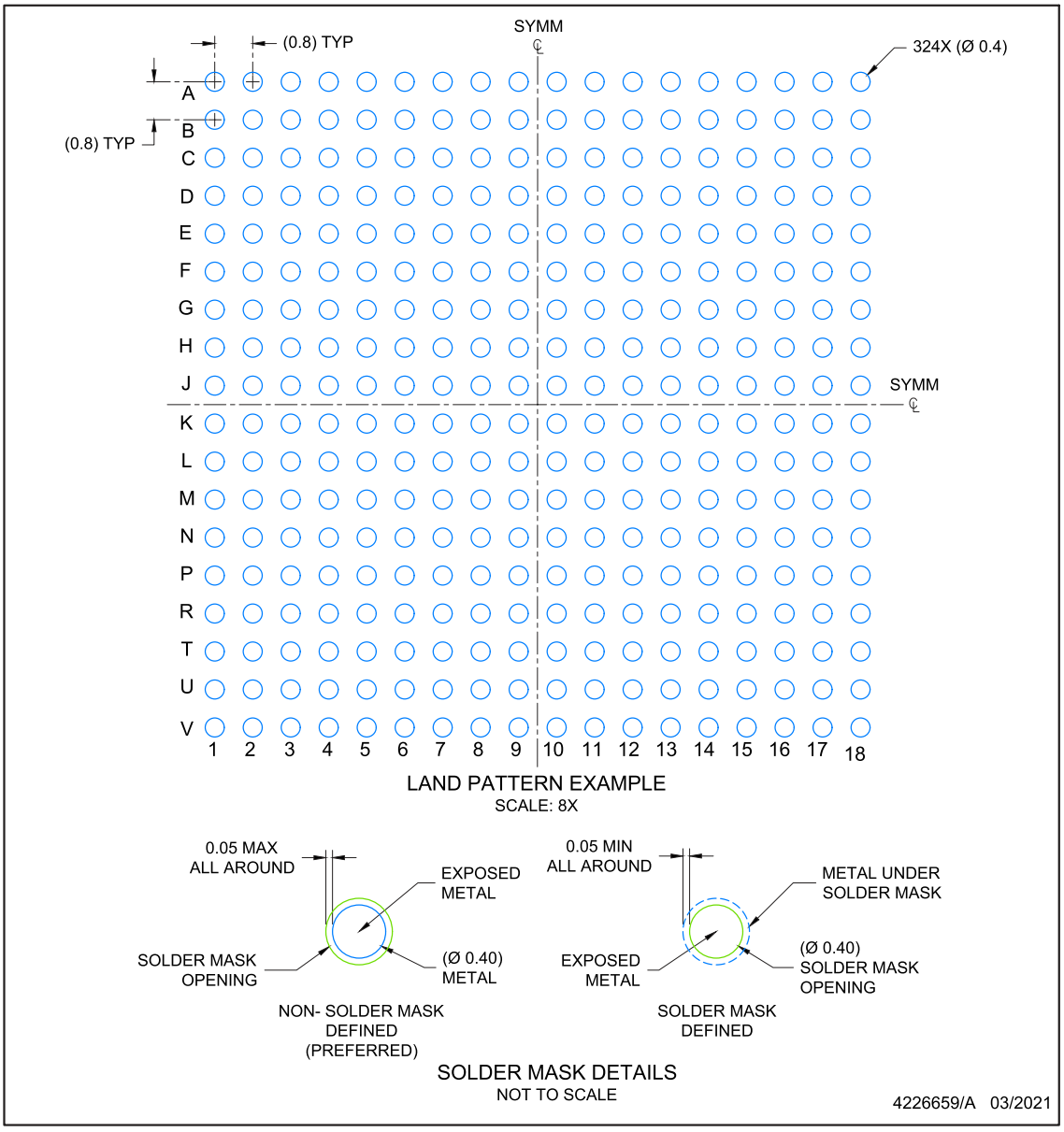
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

ZCZ0324A — NFBGA - 1.4 mm max height

PLASTIC BALL GRID ARRAY



NOTES: (continued)

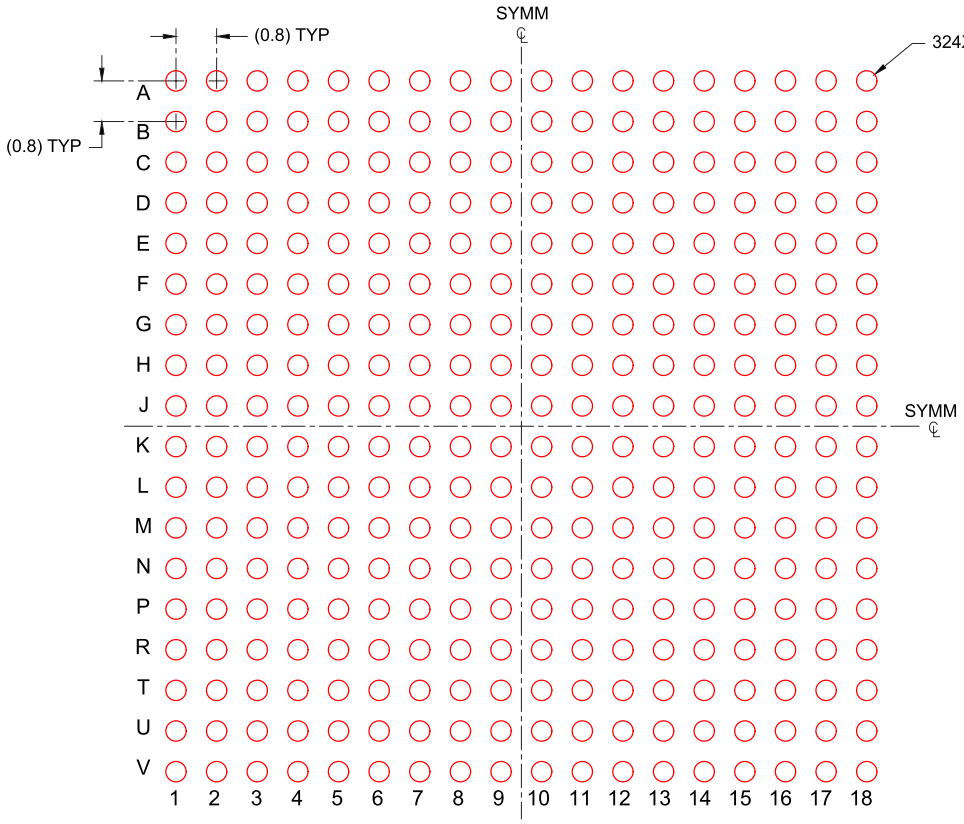
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

ZCZ0324A

NFBGA - 1.4 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.150 mm THICK STENCIL
SCALE: 8X

4226659/A 03/2021

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XAM2612AOFFHIZFG	ACTIVE	NFBGA	ZFG	304	119	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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