Technical Reference Manual

AM263x Register Addendum

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Read This First

About This Register Addendum

This Register Addendum (RA) provides detailed register references for each peripheral and subsystem in the device including:

- Register Address
- Register Name
- Register Types
- Register Reset Values
- Register Descriptions
- Bit-field Descriptions

This Register Addendum has been created in order to make the Technical Reference Manual a more effective and size-efficient collateral document. The AM263x Technical Reference Manual can be downloaded at https://www.ti.com/lit/pdf/spruj17.

Note on Register Names

Note

This sections and the examples need to be read before proceeding to other chapters

Rev D now expands upon register name by prepending additional information to show where in the IP the register is located. There are three main types of locations. Examples are described below:

- Memory Related Registers
  - These registers are prefixed with *MEM*
  - Example: MEM_QSPI0_CSN0_CFG
- Configuration Related Registers
  - These registers are prefixed with *CFG*
  - Example: CFG0_ATTR_STATUS
- Region Specific Registers
  - These registers are prefixed with a name relating to the IP
  - Example 1: CPSW_VBUSP_REGS_INT_REGS_INT_SS_C0_TH_THRESH_PULSE_EN_REG means REGS_INT_REGS_INT_SS_C0_TH_THRESH_PULSE_EN_REG is related to CPSW_NCSS_VBUSP
  - Example 2: CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ECC_REV says CPSW's ECC_REG is related to CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC. Name to be shorter and aligned in a future revision.

This change in names is also followed by sub section headers and figure titles showing different naming conventions for the registers, but the header and figure are referring to the same register. The different naming conventions help legacy users search for registers. A future revision of this document can align the registers names.

Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

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Related Documentation From Texas Instruments

For a complete listing of related documentation and development-support tools for the device, visit the Texas Instruments website at www.ti.com.

AM263x Documentation

- AM263x Data sheet
- AM263x Errata
- AM263x Technical Reference Manual
  - Technical Reference Manual contains programming guides at the end of select IPs' chapters
- AM263x Register Addendum
- AM263x Hardware Design Guidelines

AM263x Software

- Sitara MCU+ Academy for AM263x
  - Texas Instruments offers the MCU+ Academy as a resource for designing with the MCU+ software and tools on supported devices.
  - The MCU+ Academy features easy-to-use training modules that range from the basics of getting started to advanced development topics.
- MCU-PLUS-SDK-AM263x

AM263x Product Folders

- AM2634 Product Folder
- AM2632 Product Folder
- AM2631 Product Folder

AM263x Evaluation Modules

- AM263x Control Card (TMDSCNCD263)
- AM263x LaunchPad (LP-AM263)

Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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Release History (Register Addendum)

The below table summarizes Register Addendum versions and changes.

Version	Literature Number	Date	Notes
*1	SPRUJ42*1	March 2022	Initial Creation
-	SPRUJ42	April 2022	Original Release Added Read This First Content

Version	Literature Number	Date	Notes
A	SPRUJ42A	September 2022	Memory Map Updates: • Core-specific Memory Maps added Updates included for the following CTRLMMR Registers: • TOP_CTRL • MSS_CTRL • MSS_IOMUX • MSS_TOPRCM • MSS_RCM CONTROLSS_EPWM Register Descriptions Added Updates included for the following CONTROLSS Registers: • CONTROLSS_ADC* • CONTROLSS_CMPSS* • CONTROLSS_DAC • CONTROLSS_ECAP • CONTROLSS_EQEP • CONTROLSS_FSI* • CONTROLSS_GLOBAL_CTRL • CONTROLSS_*XBAR Updates included for the following SoC Registers • MSS_GPIO • MSS_LIN • MSS_SPINLOCK
B	SPRUJ42B	October 2022	Updates included for the following CTRLMMR Registers: • TOP_CTRL • MSS_CTRL • MSS_IOMUX • MSS_TOPRCM • MSS_RCM Updates included for the following CONTROLSS Registers: • CONTROLSS_CMPSS* • CONTROLSS_ECAP • CONTROLSS_EQEP • CONTROLSS_GLOBAL_CTRL • CONTROLSS_*XBAR Updates included for the following SoC Registers • XBAR and INTR Registers • MSS_*
C	SPRUJ42C	December 2022	Updates in general register description layout applied across document. PRU-ICSS Registers Added CONTROLSS_EPWM Registers Added Updates included for the following CTRLMMR Registers: • TOP_CTRL • MSS_CTRL • MSS_IOMUX • MSS_TOPRCM • MSS_RCM Updates included for the following SoC Registers • XBAR and INTR Registers • MSS_*

Version	Literature Number	Date	Notes
D	SPRUJ42D	December 2023	• Aligned register reset values in tables and images • Update register names with nomenclature used in other register addendums – Uncompressed instances and registers in EPWM. – Removed "n" variable from register nomenclature from CMPSSA, CMPSSB, ECAP, EQEP, FSI_RX, FSI_TX, OTTOCAL, R5SS, DCC, MCAN, MCRC, RTI, UART, and SDFM • Adding missing figures. ESM, GPIO, I2C, and INPUTXBAR still need missing figures added • CPSW combined into one chapter • TCM, TCMA, TCMB, CCMR, and STC moved into R5SS_Core chapter • Combined TPTC and TPCC chapter into EDAM chapter • Removed chapter CTRLMMR_CONTROLSS_GLOBAL_CTRL which was one page linking to another chapter • MCAN chapters combined into one chapter • Changed AGG to AGGR • TSXBAR_INTR renamed to SoC_TIMESYNC_XBAR0 • SOC_TSXBAR_INTR chapter renamed to SoC_TIMESYNC_XBAR1 and moved to 3.24 • TOP PBIST renamed to PBIST with instance name of PBIST0 • CMPSS instances renamed to CMPSS12B. Names to align with CMPSSA in future revision • Global Control Registers have register name changes from epwm to etpwm and cmpssb to cmpss*b0. • Added GPMC, ELM, and WDT chatpers

1 Memory Map

This chapter summarizes the memory map address regions for the device.

1.1 Device Memory Map

This section describes the device memory map.

Note

The memory locations not shown are either unallocated or reserved and not used.

Accesses to these locations are not recommended and must be avoided.

Table 1-1. AM263x Memory Map

Region Name	Start Address	End Address	Size
Core-specific Internal Memory Map[1]	0x0000 0000	0x1FFF FFFF	512MB
MCRC0	0x3500 0000	0x3500 03FF	1 KB
MPU_L2OCRAM_BANK0	0x4002 0000	0x4002 0FFF	4 KB
MPU_L2OCRAM_BANK1	0x4004 0000	0x4004 0FFF	4 KB
MPU_L2OCRAM_BANK2	0x4006 0000	0x4006 0FFF	4 KB
MPU_L2OCRAM_BANK3	0x4008 0000	0x4008 0FFF	4 KB
MPU_R5FSS0_CORE0_AXIS	0x400A 0000	0x400A 0FFF	4 KB
MPU_R5FSS0_CORE1_AXIS	0x400C 0000	0x400C 0FFF	4 KB
MPU_R5FSS1_CORE0_AXIS	0x400E 0000	0x400E 0FFF	4 KB
MPU_R5FSS1_CORE1_AXIS	0x4010 0000	0x4010 0FFF	4 KB
MPU_MBOX_SRAM	0x4014 0000	0x4014 0FFF	4 KB
MPU_QSPI0	0x4016 0000	0x4016 0FFF	4 KB
MPU_SCRM2SCRP0	0x4018 0000	0x4018 0FFF	4 KB
MPU_SCRM2SCRP1	0x401A 0000	0x401A 0FFF	4 KB
MPU_R5FSS0_CORE0_AHB	0x401C 0000	0x401C 0FFF	4 KB
MPU_R5FSS0_CORE1_AHB	0x401E 0000	0x401E 0FFF	4 KB
MPU_R5FSS1_CORE0_AHB	0x4020 0000	0x4020 0FFF	4 KB
MPU_R5FSS1_CORE1_AHB	0x4022 0000	0x4022 0FFF	4 KB
ICSSM0_INTERNAL[1]	0x4800 0000	0x4803 FFFF	256 KB
ICSSM0_ECC	0x4810 0000	0x4810 03FF	1 KB
QSPI0	0x4820 0000	0x4820 01FF	512 Bytes
MMC0	0x4830 0000	0x4830 1FFF	8 KB
GPMC0_CFG	0x4840 0000	0x4840 03FF	1 KB
CONTROLSS_G0_EPWM0	0x5000 0000	0x5000 0FFF	4 KB
CONTROLSS_G0_EPWM1	0x5000 1000	0x5000 1FFF	4 KB
CONTROLSS_G0_EPWM2	0x5000 2000	0x5000 2FFF	4 KB
CONTROLSS_G0_EPWM3	0x5000 3000	0x5000 3FFF	4 KB
CONTROLSS_G0_EPWM4	0x5000 4000	0x5000 4FFF	4 KB
CONTROLSS_G0_EPWM5	0x5000 5000	0x5000 5FFF	4 KB
CONTROLSS_G0_EPWM6	0x5000 6000	0x5000 6FFF	4 KB
CONTROLSS_G0_EPWM7	0x5000 7000	0x5000 7FFF	4 KB
CONTROLSS_G0_EPWM8	0x5000 8000	0x5000 8FFF	4 KB
CONTROLSS_G0_EPWM9	0x5000 9000	0x5000 9FFF	4 KB
CONTROLSS_G0_EPWM10	0x5000 A000	0x5000 AFFF	4 KB
CONTROLSS_G0_EPWM11	0x5000 B000	0x5000 BFFF	4 KB
CONTROLSS_G0_EPWM12	0x5000 C000	0x5000 CFFF	4 KB
CONTROLSS_G0_EPWM13	0x5000 D000	0x5000 DFFF	4 KB
CONTROLSS_G0_EPWM14	0x5000 E000	0x5000 EFFF	4 KB
CONTROLSS_G0_EPWM15	0x5000 F000	0x5000 FFFF	4 KB

Table 1-1. AM263x Memory Map (continued)

Region Name	Start Address	End Address	Size
CONTROLSS_G0_EPWM16	0x5001 0000	0x5001 0FFF	4 KB
CONTROLSS_G0_EPWM17	0x5001 1000	0x5001 1FFF	4 KB
CONTROLSS_G0_EPWM18	0x5001 2000	0x5001 2FFF	4 KB
CONTROLSS_G0_EPWM19	0x5001 3000	0x5001 3FFF	4 KB
CONTROLSS_G0_EPWM20	0x5001 4000	0x5001 4FFF	4 KB
CONTROLSS_G0_EPWM21	0x5001 5000	0x5001 5FFF	4 KB
CONTROLSS_G0_EPWM22	0x5001 6000	0x5001 6FFF	4 KB
CONTROLSS_G0_EPWM23	0x5001 7000	0x5001 7FFF	4 KB
CONTROLSS_G0_EPWM24	0x5001 8000	0x5001 8FFF	4 KB
CONTROLSS_G0_EPWM25	0x5001 9000	0x5001 9FFF	4 KB
CONTROLSS_G0_EPWM26	0x5001 A000	0x5001 AFFF	4 KB
CONTROLSS_G0_EPWM27	0x5001 B000	0x5001 BFFF	4 KB
CONTROLSS_G0_EPWM28	0x5001 C000	0x5001 CFFF	4 KB
CONTROLSS_G0_EPWM29	0x5001 D000	0x5001 DFFF	4 KB
CONTROLSS_G0_EPWM30	0x5001 E000	0x5001 EFFF	4 KB
CONTROLSS_G0_EPWM31	0x5001 F000	0x5001 FFFF	4 KB
CONTROLSS_G1_EPWM0	0x5004 0000	0x5004 0FFF	4 KB
CONTROLSS_G1_EPWM1	0x5004 1000	0x5004 1FFF	4 KB
CONTROLSS_G1_EPWM2	0x5004 2000	0x5004 2FFF	4 KB
CONTROLSS_G1_EPWM3	0x5004 3000	0x5004 3FFF	4 KB
CONTROLSS_G1_EPWM4	0x5004 4000	0x5004 4FFF	4 KB
CONTROLSS_G1_EPWM5	0x5004 5000	0x5004 5FFF	4 KB
CONTROLSS_G1_EPWM6	0x5004 6000	0x5004 6FFF	4 KB
CONTROLSS_G1_EPWM7	0x5004 7000	0x5004 7FFF	4 KB
CONTROLSS_G1_EPWM8	0x5004 8000	0x5004 8FFF	4 KB
CONTROLSS_G1_EPWM9	0x5004 9000	0x5004 9FFF	4 KB
CONTROLSS_G1_EPWM10	0x5004 A000	0x5004 AFFF	4 KB
CONTROLSS_G1_EPWM11	0x5004 B000	0x5004 BFFF	4 KB
CONTROLSS_G1_EPWM12	0x5004 C000	0x5004 CFFF	4 KB
CONTROLSS_G1_EPWM13	0x5004 D000	0x5004 DFFF	4 KB
CONTROLSS_G1_EPWM14	0x5004 E000	0x5004 EFFF	4 KB
CONTROLSS_G1_EPWM15	0x5004 F000	0x5004 FFFF	4 KB
CONTROLSS_G1_EPWM16	0x5005 0000	0x5005 0FFF	4 KB
CONTROLSS_G1_EPWM17	0x5005 1000	0x5005 1FFF	4 KB
CONTROLSS_G1_EPWM18	0x5005 2000	0x5005 2FFF	4 KB
CONTROLSS_G1_EPWM19	0x5005 3000	0x5005 3FFF	4 KB
CONTROLSS_G1_EPWM20	0x5005 4000	0x5005 4FFF	4 KB
CONTROLSS_G1_EPWM21	0x5005 5000	0x5005 5FFF	4 KB
CONTROLSS_G1_EPWM22	0x5005 6000	0x5005 6FFF	4 KB
CONTROLSS_G1_EPWM23	0x5005 7000	0x5005 7FFF	4 KB
CONTROLSS_G1_EPWM24	0x5005 8000	0x5005 8FFF	4 KB
CONTROLSS_G1_EPWM25	0x5005 9000	0x5005 9FFF	4 KB
CONTROLSS_G1_EPWM26	0x5005 A000	0x5005 AFFF	4 KB
CONTROLSS_G1_EPWM27	0x5005 B000	0x5005 BFFF	4 KB
CONTROLSS_G1_EPWM28	0x5005 C000	0x5005 CFFF	4 KB
CONTROLSS_G1_EPWM29	0x5005 D000	0x5005 DFFF	4 KB
CONTROLSS_G1_EPWM30	0x5005 E000	0x5005 EFFF	4 KB

Table 1-1. AM263x Memory Map (continued)

Region Name	Start Address	End Address	Size
CONTROLSS_G1_EPWM31	0x5005 F000	0x5005 FFFF	4 KB
CONTROLSS_G2_EPWM0	0x5008 0000	0x5008 0FFF	4 KB
CONTROLSS_G2_EPWM1	0x5008 1000	0x5008 1FFF	4 KB
CONTROLSS_G2_EPWM2	0x5008 2000	0x5008 2FFF	4 KB
CONTROLSS_G2_EPWM3	0x5008 3000	0x5008 3FFF	4 KB
CONTROLSS_G2_EPWM4	0x5008 4000	0x5008 4FFF	4 KB
CONTROLSS_G2_EPWM5	0x5008 5000	0x5008 5FFF	4 KB
CONTROLSS_G2_EPWM6	0x5008 6000	0x5008 6FFF	4 KB
CONTROLSS_G2_EPWM7	0x5008 7000	0x5008 7FFF	4 KB
CONTROLSS_G2_EPWM8	0x5008 8000	0x5008 8FFF	4 KB
CONTROLSS_G2_EPWM9	0x5008 9000	0x5008 9FFF	4 KB
CONTROLSS_G2_EPWM10	0x5008 A000	0x5008 AFFF	4 KB
CONTROLSS_G2_EPWM11	0x5008 B000	0x5008 BFFF	4 KB
CONTROLSS_G2_EPWM12	0x5008 C000	0x5008 CFFF	4 KB
CONTROLSS_G2_EPWM13	0x5008 D000	0x5008 DFFF	4 KB
CONTROLSS_G2_EPWM14	0x5008 E000	0x5008 EFFF	4 KB
CONTROLSS_G2_EPWM15	0x5008 F000	0x5008 FFFF	4 KB
CONTROLSS_G2_EPWM16	0x5009 0000	0x5009 0FFF	4 KB
CONTROLSS_G2_EPWM17	0x5009 1000	0x5009 1FFF	4 KB
CONTROLSS_G2_EPWM18	0x5009 2000	0x5009 2FFF	4 KB
CONTROLSS_G2_EPWM19	0x5009 3000	0x5009 3FFF	4 KB
CONTROLSS_G2_EPWM20	0x5009 4000	0x5009 4FFF	4 KB
CONTROLSS_G2_EPWM21	0x5009 5000	0x5009 5FFF	4 KB
CONTROLSS_G2_EPWM22	0x5009 6000	0x5009 6FFF	4 KB
CONTROLSS_G2_EPWM23	0x5009 7000	0x5009 7FFF	4 KB
CONTROLSS_G2_EPWM24	0x5009 8000	0x5009 8FFF	4 KB
CONTROLSS_G2_EPWM25	0x5009 9000	0x5009 9FFF	4 KB
CONTROLSS_G2_EPWM26	0x5009 A000	0x5009 AFFF	4 KB
CONTROLSS_G2_EPWM27	0x5009 B000	0x5009 BFFF	4 KB
CONTROLSS_G2_EPWM28	0x5009 C000	0x5009 CFFF	4 KB
CONTROLSS_G2_EPWM29	0x5009 D000	0x5009 DFFF	4 KB
CONTROLSS_G2_EPWM30	0x5009 E000	0x5009 EFFF	4 KB
CONTROLSS_G2_EPWM31	0x5009 F000	0x5009 FFFF	4 KB
CONTROLSS_G3_EPWM0	0x500C 0000	0x500C 0FFF	4 KB
CONTROLSS_G3_EPWM1	0x500C 1000	0x500C 1FFF	4 KB
CONTROLSS_G3_EPWM2	0x500C 2000	0x500C 2FFF	4 KB
CONTROLSS_G3_EPWM3	0x500C 3000	0x500C 3FFF	4 KB
CONTROLSS_G3_EPWM4	0x500C 4000	0x500C 4FFF	4 KB
CONTROLSS_G3_EPWM5	0x500C 5000	0x500C 5FFF	4 KB
CONTROLSS_G3_EPWM6	0x500C 6000	0x500C 6FFF	4 KB
CONTROLSS_G3_EPWM7	0x500C 7000	0x500C 7FFF	4 KB
CONTROLSS_G3_EPWM8	0x500C 8000	0x500C 8FFF	4 KB
CONTROLSS_G3_EPWM9	0x500C 9000	0x500C 9FFF	4 KB
CONTROLSS_G3_EPWM10	0x500C A000	0x500C AFFF	4 KB
CONTROLSS_G3_EPWM11	0x500C B000	0x500C BFFF	4 KB
CONTROLSS_G3_EPWM12	0x500C C000	0x500C CFFF	4 KB
CONTROLSS_G3_EPWM13	0x500C D000	0x500C DFFF	4 KB

Table 1-1. AM263x Memory Map (continued)

Region Name	Start Address	End Address	Size
CONTROLSS_G3_EPWM14	0x500C E000	0x500C EFFF	4 KB
CONTROLSS_G3_EPWM15	0x500C F000	0x500C FFFF	4 KB
CONTROLSS_G3_EPWM16	0x500D 0000	0x500D 0FFF	4 KB
CONTROLSS_G3_EPWM17	0x500D 1000	0x500D 1FFF	4 KB
CONTROLSS_G3_EPWM18	0x500D 2000	0x500D 2FFF	4 KB
CONTROLSS_G3_EPWM19	0x500D 3000	0x500D 3FFF	4 KB
CONTROLSS_G3_EPWM20	0x500D 4000	0x500D 4FFF	4 KB
CONTROLSS_G3_EPWM21	0x500D 5000	0x500D 5FFF	4 KB
CONTROLSS_G3_EPWM22	0x500D 6000	0x500D 6FFF	4 KB
CONTROLSS_G3_EPWM23	0x500D 7000	0x500D 7FFF	4 KB
CONTROLSS_G3_EPWM24	0x500D 8000	0x500D 8FFF	4 KB
CONTROLSS_G3_EPWM25	0x500D 9000	0x500D 9FFF	4 KB
CONTROLSS_G3_EPWM26	0x500D A000	0x500D AFFF	4 KB
CONTROLSS_G3_EPWM27	0x500D B000	0x500D BFFF	4 KB
CONTROLSS_G3_EPWM28	0x500D C000	0x500D CFFF	4 KB
CONTROLSS_G3_EPWM29	0x500D D000	0x500D DFFF	4 KB
CONTROLSS_G3_EPWM30	0x500D E000	0x500D EFFF	4 KB
CONTROLSS_G3_EPWM31	0x500D F000	0x500D FFFF	4 KB
CONTROLSS_ADC0_RESULT	0x5010 0000	0x5010 0FFF	4 KB
CONTROLSS_ADC1_RESULT	0x5010 1000	0x5010 1FFF	4 KB
CONTROLSS_ADC2_RESULT	0x5010 2000	0x5010 2FFF	4 KB
CONTROLSS_ADC3_RESULT	0x5010 3000	0x5010 3FFF	4 KB
CONTROLSS_ADC4_RESULT	0x5010 4000	0x5010 4FFF	4 KB
CONTROLSS_CMPSSA0	0x5020 0000	0x5020 0FFF	4 KB
CONTROLSS_CMPSSA1	0x5020 1000	0x5020 1FFF	4 KB
CONTROLSS_CMPSSA2	0x5020 2000	0x5020 2FFF	4 KB
CONTROLSS_CMPSSA3	0x5020 3000	0x5020 3FFF	4 KB
CONTROLSS_CMPSSA4	0x5020 4000	0x5020 4FFF	4 KB
CONTROLSS_CMPSSA5	0x5020 5000	0x5020 5FFF	4 KB
CONTROLSS_CMPSSA6	0x5020 6000	0x5020 6FFF	4 KB
CONTROLSS_CMPSSA7	0x5020 7000	0x5020 7FFF	4 KB
CONTROLSS_CMPSSA8	0x5020 8000	0x5020 8FFF	4 KB
CONTROLSS_CMPSSA9	0x5020 9000	0x5020 9FFF	4 KB
CONTROLSS_CMPSSB0	0x5022 0000	0x5022 0FFF	4 KB
CONTROLSS_CMPSSB1	0x5022 1000	0x5022 1FFF	4 KB
CONTROLSS_CMPSSB2	0x5022 2000	0x5022 2FFF	4 KB
CONTROLSS_CMPSSB3	0x5022 3000	0x5022 3FFF	4 KB
CONTROLSS_CMPSSB4	0x5022 4000	0x5022 4FFF	4 KB
CONTROLSS_CMPSSB5	0x5022 5000	0x5022 5FFF	4 KB
CONTROLSS_CMPSSB6	0x5022 6000	0x5022 6FFF	4 KB
CONTROLSS_CMPSSB7	0x5022 7000	0x5022 7FFF	4 KB
CONTROLSS_CMPSSB8	0x5022 8000	0x5022 8FFF	4 KB
CONTROLSS_CMPSSB9	0x5022 9000	0x5022 9FFF	4 KB
CONTROLSS_ECAP0	0x5024 0000	0x5024 0FFF	4 KB
CONTROLSS_ECAP1	0x5024 1000	0x5024 1FFF	4 KB
CONTROLSS_ECAP2	0x5024 2000	0x5024 2FFF	4 KB
CONTROLSS_ECAP3	0x5024 3000	0x5024 3FFF	4 KB

Table 1-1. AM263x Memory Map (continued)

Region Name	Start Address	End Address	Size
CONTROLSS_ECAP4	0x5024 4000	0x5024 4FFF	4 KB
CONTROLSS_ECAP5	0x5024 5000	0x5024 5FFF	4 KB
CONTROLSS_ECAP6	0x5024 6000	0x5024 6FFF	4 KB
CONTROLSS_ECAP7	0x5024 7000	0x5024 7FFF	4 KB
CONTROLSS_ECAP8	0x5024 8000	0x5024 8FFF	4 KB
CONTROLSS_ECAP9	0x5024 9000	0x5024 9FFF	4 KB
CONTROLSS_DAC0	0x5026 0000	0x5026 0FFF	4 KB
CONTROLSS_SDFM0	0x5026 8000	0x5026 8FFF	4 KB
CONTROLSS_SDFM1	0x5026 9000	0x5026 9FFF	4 KB
CONTROLSS_EQEP0	0x5027 0000	0x5027 0FFF	4 KB
CONTROLSS_EQEP1	0x5027 1000	0x5027 1FFF	4 KB
CONTROLSS_EQEP2	0x5027 2000	0x5027 2FFF	4 KB
CONTROLSS_FSI0_TX0	0x5028 0000	0x5028 0FFF	4 KB
CONTROLSS_FSI0_TX1	0x5028 1000	0x5028 1FFF	4 KB
CONTROLSS_FSI0_RX0	0x5029 0000	0x5029 0FFF	4 KB
CONTROLSS_FSI0_RX1	0x5029 1000	0x5029 1FFF	4 KB
CONTROLSS_FSI1_TX2	0x502A 0000	0x502A 0FFF	4 KB
CONTROLSS_FSI1_TX3	0x502A 1000	0x502A 1FFF	4 KB
CONTROLSS_FSI1_RX2	0x502B 0000	0x502B 0FFF	4 KB
CONTROLSS_FSI1_RX3	0x502B 1000	0x502B 1FFF	4 KB
CONTROLSS_ADC0_CFG	0x502C 0000	0x502C 0FFF	4 KB
CONTROLSS_ADC1_CFG	0x502C 1000	0x502C 1FFF	4 KB
CONTROLSS_ADC2_CFG	0x502C 2000	0x502C 2FFF	4 KB
CONTROLSS_ADC3_CFG	0x502C 3000	0x502C 3FFF	4 KB
CONTROLSS_ADC4_CFG	0x502C 4000	0x502C 4FFF	4 KB
CONTROLSS_INPUTXBAR	0x502D 0000	0x502D 0FFF	4 KB
CONTROLSS_PWMXBAR	0x502D 1000	0x502D 1FFF	4 KB
CONTROLSS_PWMSYNCOUTXBAR	0x502D 2000	0x502D 2FFF	4 KB
CONTROLSS_MDLXBAR	0x502D 3000	0x502D 3FFF	4 KB
CONTROLSS_ICLXBAR	0x502D 4000	0x502D 4FFF	4 KB
CONTROLSS_INTXBAR	0x502D 5000	0x502D 5FFF	4 KB
CONTROLSS_DMAXBAR	0x502D 6000	0x502D 6FFF	4 KB
CONTROLSS_OUTPUTXBAR	0x502D 8000	0x502D 8FFF	4 KB
CONTROLSS_OTTOCAL0	0x502E 0000	0x502E 0FFF	4 KB
CONTROLSS_OTTOCAL1	0x502E 1000	0x502E 1FFF	4 KB
CONTROLSS_OTTOCAL2	0x502E 2000	0x502E 2FFF	4 KB
CONTROLSS_OTTOCAL3	0x502E 3000	0x502E 3FFF	4 KB
CONTROLSS_CTRL	0x502F 0000	0x502F 7FFF	32 KB
DEBUGSS	0x5080 0000	0x508F FFFF	1024 KB
MSS_CTRL	0x50D0 0000	0x50D3 FFFF	256 KB
TOP_CTRL	0x50D8 0000	0x50D8 7FFF	32 KB
SPINLOCK0	0x50E0 0000	0x50E0 7FFF	32 KB
VIM	0x50F0 0000	0x50F0 3FFF	16 KB
GPIO0	0x5200 0000	0x5200 00FF	256 Bytes
GPIO1	0x5200 1000	0x5200 10FF	256 Bytes
GPIO2	0x5200 2000	0x5200 20FF	256 Bytes
GPIO3	0x5200 3000	0x5200 30FF	256 Bytes

Table 1-1. AM263x Memory Map (continued)

Region Name	Start Address	End Address	Size
WDT0	0x5210 0000	0x5210 00FF	256 Bytes
WDT1	0x5210 1000	0x5210 10FF	256 Bytes
WDT2	0x5210 2000	0x5210 20FF	256 Bytes
WDT3	0x5210 3000	0x5210 30FF	256 Bytes
RTI0	0x5218 0000	0x5218 03FF	1 KB
RTI1	0x5218 1000	0x5218 13FF	1 KB
RTI2	0x5218 2000	0x5218 23FF	1 KB
RTI3	0x5218 3000	0x5218 33FF	1 KB
MCSPI0	0x5220 0000	0x5220 01FF	512 Bytes
MCSPI1	0x5220 1000	0x5220 11FF	512 Bytes
MCSPI2	0x5220 2000	0x5220 21FF	512 Bytes
MCSPI3	0x5220 3000	0x5220 31FF	512 Bytes
MCSPI4	0x5220 4000	0x5220 41FF	512 Bytes
UART0	0x5230 0000	0x5230 01FF	512 Bytes
UART1	0x5230 1000	0x5230 11FF	512 Bytes
UART2	0x5230 2000	0x5230 21FF	512 Bytes
UART3	0x5230 3000	0x5230 31FF	512 Bytes
UART4	0x5230 4000	0x5230 41FF	512 Bytes
UART5	0x5230 5000	0x5230 51FF	512 Bytes
LIN0	0x5240 0000	0x5240 00FF	256 Bytes
LIN1	0x5240 1000	0x5240 10FF	256 Bytes
LIN2	0x5240 2000	0x5240 20FF	256 Bytes
LIN3	0x5240 3000	0x5240 30FF	256 Bytes
LIN4	0x5240 4000	0x5240 40FF	256 Bytes
I2C0	0x5250 0000	0x5250 00FF	256 Bytes
I2C1	0x5250 1000	0x5250 10FF	256 Bytes
I2C2	0x5250 2000	0x5250 20FF	256 Bytes
I2C3	0x5250 3000	0x5250 30FF	256 Bytes
MCAN0_MSG_RAM	0x5260 0000	0x5260 7FFF	32 KB
MCAN0_CFG	0x5260 8000	0x5260 83FF	1 KB
MCAN1_MSG_RAM	0x5261 0000	0x5261 7FFF	32 KB
MCAN1_CFG	0x5261 8000	0x5261 83FF	1 KB
MCAN2_MSG_RAM	0x5262 0000	0x5262 7FFF	32 KB
MCAN2_CFG	0x5262 8000	0x5262 83FF	1 KB
MCAN3_MSG_RAM	0x5263 0000	0x5263 7FFF	32 KB
MCAN3_CFG	0x5263 8000	0x5263 83FF	1 KB
MCAN0_ECC	0x5270 0000	0x5270 03FF	1 KB
MCAN1_ECC	0x5270 1000	0x5270 13FF	1 KB
MCAN2_ECC	0x5270 2000	0x5270 23FF	1 KB
MCAN3_ECC	0x5270 3000	0x5270 33FF	1 KB
ELM0	0x527F 0000	0x527F 0FFF	4 KB
CPSW0	0x5280 0000	0x529F FFFF	2 MB
TPCC0	0x52A0 0000	0x52A0 7FFF	32 KB
TPTC00	0x52A4 0000	0x52A4 0FFF	4 KB
TPTC01	0x52A6 0000	0x52A6 0FFF	4 KB
DCC0	0x52B0 0000	0x52B0 00FF	256 Bytes
DCC1	0x52B0 1000	0x52B0 10FF	256 Bytes

Table 1-1. AM263x Memory Map (continued)

Region Name	Start Address	End Address	Size
DCC2	0x52B0 2000	0x52B0 20FF	256 Bytes
DCC3	0x52B0 3000	0x52B0 30FF	256 Bytes
TOP_ESM	0x52D0 0000	0x52D0 0FFF	4 KB
SOC_TIMESYNC_XBAR0	0x52E0 0000	0x52E0 00FF	256 Bytes
EDMA_TRIG_XBAR	0x52E0 1000	0x52E0 11FF	512 Bytes
GPIO_INTR_XBAR	0x52E0 2000	0x52E0 23FF	1 KB
ICSSM_INTR_XBAR	0x52E0 3000	0x52E0 30FF	256 Bytes
SOC_TIMESYNC_XBAR1	0x52E0 4000	0x52E0 43FF	1 KB
ECC_AGG_R5FSS0_CORE0	0x5300 0000	0x5300 03FF	1 KB
ECC_AGG_R5FSS0_CORE1	0x5300 3000	0x5300 33FF	1 KB
ECC_AGG_R5FSS1_CORE0	0x5300 4000	0x5300 43FF	1 KB
ECC_AGG_R5FSS1_CORE1	0x5300 7000	0x5300 73FF	1 KB
ECC_AGG_TOP	0x5301 0000	0x5301 03FF	1 KB
IOMUX	0x5310 0000	0x5310 0FFF	4 KB
TOP_RCM	0x5320 0000	0x5320 7FFF	32 KB
MSS_RCM	0x5320 8000	0x5320 FFFF	32 KB
R5FSS0_CCMR	0x5321 0000	0x5321 0FFF	4 KB
R5FSS1_CCMR	0x5321 1000	0x5321 1FFF	4 KB
TOP_PBIST	0x5330 0000	0x5330 03FF	1 KB
R5FSS0_STC	0x5350 0000	0x5350 01FF	512 Bytes
R5FSS1_STC	0x5351 0000	0x5351 01FF	512 Bytes
EXT_FLASH0	0x6000 0000	0x61FF FFFF	32 MB
EXT_FLASH1	0x6200 0000	0x63FF FFFF	32 MB
GPMC0_MEM	0x6800 0000	0x6FFF FFFF	128 MB
L2OCRAM	0x7000 0000	0x701F FFFF	2 MB
MBOX_SRAM	0x7200 0000	0x7200 3FFF	16 KB
R5FSS0_CORE0_ICACHE[4]	0x7400 0000	0x747F FFFF	16 KB (8 MB)[5]
R5FSS0_CORE0_DCACHE[4]	0x7480 0000	0x74FF FFFF	16 KB (8 MB)[5]
R5FSS0_CORE1_ICACHE[2] [4]	0x7500 0000	0x757F FFFF	16 KB (8 MB)[5]
R5FSS0_CORE1_DCACHE[2] [4]	0x7580 0000	0x75FF FFFF	16 KB (8 MB)[5]
R5FSS1_CORE0_ICACHE[4]	0x7600 0000	0x767F FFFF	16 KB (8 MB)[5]
R5FSS1_CORE0_DCACHE[4]	0x7680 0000	0x76FF FFFF	16 KB (8 MB)[5]
R5FSS1_CORE1_ICACHE[2] [4]	0x7700 0000	0x777F FFFF	16 KB (8 MB)[5]
R5FSS1_CORE1_DCACHE[2] [4]	0x7780 0000	0x77FF FFFF	16 KB (8 MB)[5]
R5FSS0_CORE0_TCMA[3] [4]	0x7800 0000	0x7800 FFFF (Lockstep) 0x7800 7FFF (Dual Core)	64 KB (Lockstep) 32 KB (Dual Core)
R5FSS0_CORE0_TCMB[3] [4]	0x7810 0000	0x7810 FFFF (Lockstep) 0x7810 7FFF (Dual Core)	64 KB (Lockstep) 32 KB (Dual Core)
R5FSS0_CORE1_TCMA[2] [4]	0x7820 0000	0x7820 7FFF	32 KB
R5FSS0_CORE1_TCMB[2] [4]	0x7830 0000	0x7830 7FFF	32 KB
R5FSS1_CORE0_TCMA[3] [4]	0x7840 0000	0x7840 FFFF (Lockstep) 0x7840 7FFF (Dual Core)	64 KB (Lockstep) 32 KB (Dual Core)
R5FSS1_CORE0_TCMB[3] [4]	0x7850 0000	0x7850 FFFF (Lockstep) 0x7850 7FFF (Dual Core)	64 KB (Lockstep) 32 KB (Dual Core)
R5FSS1_CORE1_TCMA[2] [4]	0x7860 0000	0x7860 7FFF	32 KB
R5FSS1_CORE1_TCMB[2] [4]	0x7870 0000	0x7870 7FFF	32 KB

(1) See core-specific tables for the internal memory map.

(2) In Lockstep mode, the R5FSS*x* CORE**1** memory region is not accessible.
(3) The size of these memories changes based on Dual-Core vs Lockstep operation.
For more information about Dual-Core and Lockstep modes, see the *R5FSS* chapter.
For more information about ATCM and BTCM, see the *Tightly-Coupled Memories (TCM)* section within the *R5FSS* chapter.
(4) This memory region is used by each CPU core to access the TCM/Cache memory space of other CPU cores.
(5) Each R5FSS contains 16 KB i-cache and 16 KB d-cache. However, the system interconnect sees an 8 MB address range at ICACHE/DCACHE. Any core attempting to access more than 16 KB will wrap around and access the same cache multiple times.

1.2 R5FSS Memory Map

Table 1-2. R5FSS0-0 Memory Map

Region Name	Start Address	End Address	Size
R5SS0_CORE0_TCMA_ROM	0x0000 0000	0x0001 FFFF	128 KB
R5SS0_CORE0_TCMA_RAM	0x0002 0000	0x0002 FFFF (Lockstep) 0x0002 7FFF (Dual Core)	64 KB (Lockstep) 32 KB (Dual Core)
R5SS0_CORE0_TCMB_RAM	0x0008 0000	0x0008 FFFF (Lockstep) 0x0008 7FFF (Dual Core)	64 KB (Lockstep) 32 KB (Dual Core)
R5SS0_CORE0_VIM	0x50F0 0000	0x50F0 3FFF	16 KB
R5SS0_CORE0_WWDT (WDT0)	0x5210 0000	0x5210 00FF	256 Bytes
ROM to RAM Swap			
R5SS0_CORE0_TCMA_ROM	NA	NA	NA
R5SS0_CORE0_TCMA_RAM	0x0000 0000	0x0000 FFFF (Lockstep) 0x0000 7FFF (Dual Core)	64 KB (Lockstep) 32 KB (Dual Core)
R5SS0_CORE0_TCMB_RAM	0x0008 0000	0x0008 FFFF (Lockstep) 0x0008 7FFF (Dual Core)	64 KB (Lockstep) 32 KB (Dual Core)
R5SS0_CORE0_VIM	0x50F0 0000	0x50F0 3FFF	16 KB
R5SS0_CORE0_WWDT (WDT0)	0x5210 0000	0x5210 00FF	256 Bytes

Table 1-3. R5FSS0-1 Memory Map

Region Name	Start Address	End Address	Size
R5SS0_CORE1_TCMA_RAM	0x0000 0000	0x0000 7FFF	32 KB
R5SS0_CORE1_TCMB_RAM	0x0008 0000	0x0008 7FFF	32 KB
R5SS0_CORE1_VIM	0x50F0 0000	0x50F0 3FFF	16 KB
R5SS0_CORE1_WWDT (WDT1)	0x5210 1000	0x5210 10FF	256 Bytes

Table 1-4. R5FSS1-0 Memory Map

Region Name	Start Address	End Address	Size
R5SS1_CORE0_TCMA_RAM	0x0000 0000	0x0000 FFFF (Lockstep) 0x0000 7FFF (Dual Core)	64 KB (Lockstep) 32 KB (Dual Core)
R5SS1_CORE0_TCMB_RAM	0x0008 0000	0x0008 FFFF (Lockstep) 0x0008 7FFF (Dual Core)	64 KB (Lockstep) 32 KB (Dual Core)
R5SS1_CORE0_VIM	0x50F0 0000	0x50F0 3FFF	16 KB
R5SS1_CORE0_WWDT (WDT2)	0x5210 2000	0x5210 20FF	256 Bytes

Table 1-5. R5FSS1-1 Memory Map

Region Name	Start Address	End Address	Size
R5SS1_CORE1_TCMA_RAM	0x0000 0000	0x0000 7FFF	32 KB
R5SS1_CORE1_TCMB_RAM	0x0008 0000	0x0008 7FFF	32 KB
R5SS1_CORE1_VIM	0x50F0 0000	0x50F0 3FFF	16 KB
R5SS1_CORE1_WWDT (WDT3)	0x5210 3000	0x5210 30FF	256 Bytes

1.3 PRU-ICSS Memory Map

Region Name	Start Address	End Address	Size
PRU-ICSS Data RAM0 (DRAM0)	0x0000 0000	0x0000 1FFF	8 KB
PRU-ICSS Data RAM1 (DRAM1)	0x0000 2000	0x0000 3FFF	8 KB
PRU-ICSS Data RAM2 (Shared DRAM2)	0x0001 0000	0x0001 FFFF	64 KB
PRU-ICSS INTC	0x0002 0000	0x0002 1FFF	8 KB
PRU-ICSS PRU0 Control	0x0002 2000	0x0002 23FF	1 KB
PRU-ICSS PRU0 Debug	0x0002 2400	0x0002 3FFF	7 KB
PRU-ICSS PRU1 Control	0x0002 4000	0x0002 43FF	1 KB
PRU-ICSS PRU1 Debug	0x0002 4400	0x0002 5FFF	7 KB
PRU-ICSS CFG	0x0002 6000	0x0002 6FFF	4 KB
PRU-ICSS ECC_CFG	0x0002 7000	0x0002 7FFF	4 KB
PRU-ICSS UART0	0x0002 8000	0x0002 9FFF	8 KB
PRU-ICSS Reserved	0x0002 A000	0x0002 BFFF	8 KB
PRU-ICSS Reserved	0x0002 C000	0x0002 DFFF	8 KB
PRU-ICSS IEP	0x0002 E000	0x0002 EFFF	8 KB
PRU-ICSS ECAP0	0x0003 0000	0x0003 1FFF	8 KB
PRU-ICSS MII_RT_CFG	0x0003 2000	0x0003 23FF	1 KB
PRU-ICSS MII_MDIO	0x0003 2400	0x0003 3FFF	7 KB
PRU-ICSS PRU0 IRAM	0x0003 4000	0x0003 7FFF	16 KB
PRU-ICSS PRU1 IRAM	0x0003 8000	0x0003 BFFF	16 KB

2 Control Module (CTRLMMR) Registers

The control module is the main controller for top-level device behavior in various states. Module contains registers for configuration, bootstrap (SOP) signals, I/O terminal pad multiplexing, clock selection, and many others. There are various control or (CTRLMMR) modules define in this device, and those module's registers are described in the following sections.

2.1 MMR Write Protection

All Control Module MMR have a protection mechanism which prevents spurious writes from changing register values. LOCK0_KICK0 and LOCK0_KICK1 registers are used for this purpose. The sequence to unlock these MMR is as follows:

1. Write exact unlock value (Table 2-1) to <Control Module>LOCK0_KICK0:KEY field
2. Write exact unlock value (Table 2-1) to <Control Module>LOCK0_KICK1:KEY field

The sequence to lock the MMR is as follows:

1. Write zero (or anyother value other than the unlock value)Table 2-1) to <Control Module>LOCK0_KICK1:KEY field
2. Write zero (or anyother value other than the unlock value)Table 2-1) to <Control Module>LOCK0_KICK0:KEY field

- **Note**

  If the above sequence for locking the IOMUX is not followed, an AHB_WRITE_ERROR interrupt will occur (if enabled).

For example, to unlock Control Module MSS_CTRL the sequence is as below:

1. Write 0x01234567 to MSS_CTRL.LOCK0_KICK0:KEY
2. Write 0xFEDCBA8 to MSS_CTRL.LOCK0_KICK1:KEY

To lock the Control Module MSS_CTRL the sequence is as below:

1. Write 0x0 to MSS_CTRL.LOCK0_KICK1:KEY
2. Write 0x0 to MSS_CTRL.LOCK0_KICK0:KEY

Any writes to locked memory region will result in assertion of the MMR_ACCESS_ERR_WR event by the respective control modules. This assertion can be enabled or disabled by writing the appropriate value to <Control Module>.INTR_ENABLE.KICK_ERR_EN field.

The table below shows the values that must be written to the LOCK0_KICK0 and LOCK0_KICK1 registers to unlock the various Control modules' MMR.

Table 2-1. Kick Protection Register Unlock Values

Protected Register	LockKick Register	Unlock Value
TOP_CTRL	LOCK0_KICK0	0x01234567
	LOCK0_KICK1	0xFEDCBA8
MSS_CTRL	LOCK0_KICK0	0x01234567
	LOCK0_KICK1	0xFEDCBA8
CONTROLSS_CTRL	LOCK0_KICK0	0x01234567
	LOCK0_KICK1	0xFEDCBA8
TOP_RCM	LOCK0_KICK0	0x01234567
	LOCK0_KICK1	0xFEDCBA8
MSS_RCM	LOCK0_KICK0	0x01234567
	LOCK0_KICK1	0xFEDCBA8
IOMUX	LOCK0_KICK0	0x83E70B13
	LOCK0_KICK1	0x95A4F1E0

Note

To ensure that all registers from a given partition are write protected, software must always re-lock the protection mechanism after completing the register writes.

The kick protection registers described in this section are an exception and are not write protected by the protection mechanism.

2.2 TOP_CTRL Registers

Table 2-2. CFG0, CFG0 Registers, Base Address=0X0000000050D80000, Length=8192

Offset	Length	Register Name	TOP_CTRL_mmr Physical Address
10h	32	EFUSE_DIEID0	50D8 0010h
14h	32	EFUSE_DIEID1	50D8 0014h
18h	32	EFUSE_DIEID2	50D8 0018h
1Ch	32	EFUSE_DIEID3	50D8 001Ch
20h	32	EFUSE_UID0	50D8 0020h
24h	32	EFUSE_UID1	50D8 0024h
28h	32	EFUSE_UID2	50D8 0028h
2Ch	32	EFUSE_UID3	50D8 002Ch
30h	32	EFUSE_DEVICE_TYPE	50D8 0030h
34h	32	EFUSE_FROM0_CHECKSUM	50D8 0034h
38h	32	EFUSE_JTAG_USERCODE_ID	50D8 0038h
500h	32	MAC_ID0	50D8 0500h
504h	32	MAC_ID1	50D8 0504h
C00h	32	ADC_REFBUF0_CTRL	50D8 0C00h
C04h	32	ADC_REFBUF1_CTRL	50D8 0C04h
C08h	32	ADC_REF_COMP_CTRL	50D8 0C08h
C0Ch	32	ADC_REF_GOOD_STATUS	50D8 0C0Ch
C10h	32	VMON_CTRL	50D8 0C10h
C14h	32	VMON_STAT	50D8 0C14h
C18h	32	PMU_COARSE_STAT	50D8 0C18h
C20h	32	MASK_VMON_ERROR_ESM_H	50D8 0C20h
C24h	32	MASK_VMON_ERROR_ESM_L	50D8 0C24h
C34h	32	VMON_FILTER_CTRL	50D8 0C34h
D00h	32	TSENSE_CFG	50D8 0D00h
D04h	32	TSENSE_STATUS	50D8 0D04h
D08h	32	TSENSE_STATUS_RAW	50D8 0D08h
D14h	32	TSENSE0_ALERT	50D8 0D14h
D18h	32	TSENSE0_CNTL	50D8 0D18h
D1Ch	32	TSENSE0_RESULT	50D8 0D1Ch
D20h	32	TSENSE0_DATA0	50D8 0D20h
D24h	32	TSENSE0_DATA1	50D8 0D24h
D28h	32	TSENSE0_DATA2	50D8 0D28h
D2Ch	32	TSENSE0_DATA3	50D8 0D2Ch
D30h	32	TSENSE0_ACCU	50D8 0D30h
D44h	32	TSENSE1_ALERT	50D8 0D44h
D48h	32	TSENSE1_CNTL	50D8 0D48h
D4Ch	32	TSENSE1_RESULT	50D8 0D4Ch
D50h	32	TSENSE1_DATA0	50D8 0D50h
D54h	32	TSENSE1_DATA1	50D8 0D54h
D58h	32	TSENSE1_DATA2	50D8 0D58h
D5Ch	32	TSENSE1_DATA3	50D8 0D5Ch
D60h	32	TSENSE1_ACCU	50D8 0D60h
D7Ch	32	TSENSE2_RESULT	50D8 0D7Ch
DACh	32	TSENSE3_RESULT	50D8 0DACh
FF8h	32	HW_SPARE_REC0	50D8 0FF8h

Table 2-2. CFG0, CFG0 Registers, Base Address=0X0000000050D80000, Length=8192 (continued)

Offset	Length	Register Name	TOP_CTRL_mmr Physical Address
FFCh	32	HW_SPARE_REC1	50D8 0FFCh
1008h	32	LOCK0_KICK0	50D8 1008h
100Ch	32	LOCK0_KICK1	50D8 100Ch
1010h	32	intr_raw_status	50D8 1010h
1014h	32	intr_enabled_status_clear	50D8 1014h
1018h	32	intr_enable	50D8 1018h
101Ch	32	intr_enable_clear	50D8 101Ch
1020h	32	eoi	50D8 1020h
1024h	32	fault_address	50D8 1024h
1028h	32	fault_type_status	50D8 1028h
102Ch	32	fault_attr_status	50D8 102Ch
1030h	32	fault_clear	50D8 1030h

2.2.1 CFG0_EFUSE_DIEID0 Registers

2.2.1.1 CFG0_DIEID0 Register (Offset = 10h) [reset = 0h]

Short Description:

Long Description:

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Table 2-3. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0010h

Figure 2-1. EFUSE_DIEID0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EFUSE_DIEID0_VAL															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EFUSE_DIEID0_VAL															
R															
0h															

Access Types Legend

Table 2-4. EFUSE_DIEID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EFUSE_DIEID0_VAL	R	0h	EFUSE DieID[31:0] Reset Source: mod_g_rst_n

2.2.2 CFG0_EFUSE_DIEID1 Registers

2.2.2.1 CFG0_DIEID1 Register (Offset = 14h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-5. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0014h

Figure 2-2. EFUSE_DIEID1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EFUSE_DIEID1_VAL															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EFUSE_DIEID1_VAL															
R															
0h															

Access Types Legend

Table 2-6. EFUSE_DIEID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EFUSE_DIEID1_VAL	R	0h	EFUSE DieID[63:32] Reset Source: mod_g_rst_n

2.2.3 CFG0_EFUSE_DIEID2 Registers

2.2.3.1 CFG0_DIEID2 Register (Offset = 18h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-7. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0018h

Figure 2-3. EFUSE_DIEID2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EFUSE_DIEID2_VAL															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EFUSE_DIEID2_VAL															
R															
0h															

Access Types Legend

Table 2-8. EFUSE_DIEID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EFUSE_DIEID2_VAL	R	0h	EFUSE DieID[95:64] Reset Source: mod_g_rst_n

2.2.4 CFG0_EFUSE_DIEID3 Registers

2.2.4.1 CFG0_DIEID3 Register (Offset = 1Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-9. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 001Ch

Figure 2-4. EFUSE_DIEID3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EFUSE_DIEID3_VAL															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EFUSE_DIEID3_VAL															
R															
0h															

Access Types Legend

Table 2-10. EFUSE_DIEID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EFUSE_DIEID3_VAL	R	0h	EFUSE DieID[127:96] Reset Source: mod_g_rst_n

2.2.5 CFG0_EFUSE_UID0 Registers

2.2.5.1 CFG0_UID0 Register (Offset = 20h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-11. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0020h

Figure 2-5. EFUSE_UID0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EFUSE_UID0_VAL															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EFUSE_UID0_VAL															
R															
0h															

Access Types Legend

Table 2-12. EFUSE_UID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EFUSE_UID0_VAL	R	0h	EFUSE UID[31:0] Reset Source: mod_g_rst_n

2.2.6 CFG0_EFUSE_UID1 Registers

2.2.6.1 CFG0_UID1 Register (Offset = 24h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-13. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0024h

Figure 2-6. EFUSE_UID1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EFUSE_UID1_VAL															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EFUSE_UID1_VAL															
R															
0h															

Access Types Legend

Table 2-14. EFUSE_UID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EFUSE_UID1_VAL	R	0h	EFUSE UID[63:32] Reset Source: mod_g_rst_n

2.2.7 CFG0_EFUSE_UID2 Registers

2.2.7.1 CFG0_UID2 Register (Offset = 28h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-15. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0028h

Figure 2-7. EFUSE_UID2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EFUSE_UID2_VAL															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EFUSE_UID2_VAL															
R															
0h															

Access Types Legend

Table 2-16. EFUSE_UID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EFUSE_UID2_VAL	R	0h	EFUSE UID[95:64] Reset Source: mod_g_rst_n

2.2.8 CFG0_EFUSE_UID3 Registers

2.2.8.1 CFG0_UID3 Register (Offset = 2Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-17. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 002Ch

Figure 2-8. EFUSE_UID3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								EFUSE_UID3_VAL							
NONE								R							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EFUSE_UID3_VAL															
R															
0h															

Access Types Legend

Table 2-18. EFUSE_UID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	EFUSE_UID3_VAL	R	0h	EFUSE UID[120:96] Reset Source: mod_g_rst_n

2.2.9 CFG0_EFUSE_DEVICE_TYPE Registers

2.2.9.1 CFG0_DEVICE_TYPE Register (Offset = 30h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-19. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0030h

Figure 2-9. EFUSE_DEVICE_TYPE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EFUSE_DEVICE_TYPE_VAL															
R															
0h															

Access Types Legend

Table 2-20. EFUSE_DEVICE_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	EFUSE_DEVICE_TYPE_VAL	R	0h	EFUSE Device Type Reset Source: mod_g_rst_n

2.2.10 CFG0_EFUSE_FROM0_CHECKSUM Registers

2.2.10.1 CFG0_FROM0_CHECKSUM Register (Offset = 34h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-21. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0034h

Figure 2-10. EFUSE_FROM0_CHECKSUM Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EFUSE_FROM0_CHECKSUM_VAL															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EFUSE_FROM0_CHECKSUM_VAL															
R															
0h															

Access Types Legend

Table 2-22. EFUSE_FROM0_CHECKSUM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EFUSE_FROM0_CHECKSUM_VAL	R	0h	32 bit FROM0 Checksum Reset Source: mod_g_rst_n

2.2.11 CFG0_EFUSE_JTAG_USERCODE_ID Registers

2.2.11.1 CFG0_JTAG_USERCODE_ID Register (Offset = 38h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-23. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0038h

Figure 2-11. EFUSE_JTAG_USERCODE_ID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EFUSE_JTAG_USERCODE_ID_VAL															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EFUSE_JTAG_USERCODE_ID_VAL															
R															
0h															

Access Types Legend

Table 2-24. EFUSE_JTAG_USERCODE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EFUSE_JTAG_USERCODE_ID_VAL	R	0h	EFUSE JTAG_USER_CODE_ID[31:0]. Denotes part variant Reset Source: mod_g_rst_n

2.2.12 CFG0_MAC_ID0 Registers

2.2.12.1 CFG0_ID0 Register (Offset = 500h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-25. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0500h

Figure 2-12. MAC_ID0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MAC_ID0_MACID_LO															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAC_ID0_MACID_LO															
R															
0h															

Access Types Legend

Table 2-26. MAC_ID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MAC_ID0_MACID_LO	R	0h	MAC ID low [32bits] Reset Source: mod_g_rst_n

2.2.13 CFG0_MAC_ID1 Registers

2.2.13.1 CFG0_ID1 Register (Offset = 504h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-27. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0504h

Figure 2-13. MAC_ID1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAC_ID1_MACID_HI															
R															
0h															

Access Types Legend

Table 2-28. MAC_ID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	MAC_ID1_MACID_HI	R	0h	MAC ID high [16bits] Reset Source: mod_g_rst_n

2.2.14 CFG0_ADC_REFBUF0_CTRL Registers

2.2.14.1 CFG0_REFBUF0_CTRL Register (Offset = C00h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-29. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0C00h

Figure 2-14. ADC_REFBUF0_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ADC_REFBUF0_CTRL_ENABLE		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-30. ADC_REFBUF0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ADC_REFBUF0_CTRL_ENABLE	R/W	0h	Enables adc reference 0, mask hhv before enable 000: Disable 111 : Enable Reset Source: mod_g_rst_n

2.2.15 CFG0_ADC_REFBUF1_CTRL Registers

2.2.15.1 CFG0_REFBUF1_CTRL Register (Offset = C04h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-31. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0C04h

Figure 2-15. ADC_REFBUF1_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ADC_REFBUF1_CTRL_ENABLE		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-32. ADC_REFBUF1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ADC_REFBUF1_CTRL_ENABLE	R/W	0h	Enables adc reference 0, mask hhv before enable 000: Disable 111 : Enable Reset Source: mod_g_rst_n

2.2.16 CFG0_ADC_REF_COMP_CTRL Registers

2.2.16.1 CFG0_REF_COMP_CTRL Register (Offset = C08h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-33. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0C08h

Figure 2-16. ADC_REF_COMP_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					ADC_REF_COMP_CTRL_ADC34_REFOK_EN			RESERVED	ADC_REF_COMP_CTRL_ADC12_REFOK_EN			RESERVED	ADC_REF_COMP_CTRL_ADC0_REFOK_EN		
NONE					R/W			NONE	R/W			NONE	R/W		
0					0h			0	0h			0	0h		

Access Types Legend

Table 2-34. ADC_REF_COMP_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE		Reserved
10:8	ADC_REF_COMP_CTRL_ADC34_REFOK_EN	R/W	0h	enables reference comparators (ROK1). This monitors adc3 and adc4 refernc Reset Source: mod_g_rst_n
7	RESERVED	NONE		Reserved
6:4	ADC_REF_COMP_CTRL_ADC12_REFOK_EN	R/W	0h	enables reference comparators (ROK0B). This monitors adc1 and adc2 refernce Reset Source: mod_g_rst_n
3	RESERVED	NONE		Reserved
2:0	ADC_REF_COMP_CTRL_ADC0_REFOK_EN	R/W	0h	enables reference comparators (ROK0). This monitors adc0 refernce Reset Source: mod_g_rst_n

2.2.17 CFG0_ADC_REF_GOOD_STATUS Registers

2.2.17.1 CFG0_REF_GOOD_STATUS Register (Offset = C0Ch) [reset = 3fh]

Short Description:

Long Description:

Return to Summary Table

Table 2-35. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0C0Ch

Figure 2-17. ADC_REF_GOOD_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
2b67															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										ADC_REF_GOOD_STATUS_ADC34_REF_UV_GOOD	ADC_REF_GOOD_STATUS_ADC34_REF_OV_GOOD	ADC_REF_GOOD_STATUS_ADC12_REF_UV_GOOD	ADC_REF_GOOD_STATUS_ADC12_REF_OV_GOOD	ADC_REF_GOOD_STATUS_ADC0_REF_UV_GOOD	ADC_REF_GOOD_STATUS_ADC0_REF_OV_GOOD
NONE										R	R	R	R	R	R
2b67										1h	1h	1h	1h	1h	1h

Access Types Legend

Table 2-36. ADC_REF_GOOD_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE		Reserved
5	ADC_REF_GOOD_STATUS_ADC34_REF_UV_GOOD	R	1h	Under Voltage check OK Reset Source: mod_g_rst_n
4	ADC_REF_GOOD_STATUS_ADC34_REF_OV_GOOD	R	1h	Over voltage check OK Reset Source: mod_g_rst_n
3	ADC_REF_GOOD_STATUS_ADC12_REF_UV_GOOD	R	1h	Under Voltage check OK Reset Source: mod_g_rst_n
2	ADC_REF_GOOD_STATUS_ADC12_REF_OV_GOOD	R	1h	Over voltage check OK Reset Source: mod_g_rst_n
1	ADC_REF_GOOD_STATUS_ADC0_REF_UV_GOOD	R	1h	Under Voltage check OK Reset Source: mod_g_rst_n
0	ADC_REF_GOOD_STATUS_ADC0_REF_OV_GOOD	R	1h	Over voltage check OK Reset Source: mod_g_rst_n

2.2.18 CFG0_VMON_CTRL Registers

2.2.18.1 CFG0_CTRL Register (Offset = C10h) [reset = 7777777h]

Short Description:

Long Description:

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Table 2-37. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0C10h

Figure 2-18. VMON_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					VMON_CTRL_CMP8_EN			RESERVED	VMON_CTRL_CMP7_EN			RESERVED	VMON_CTRL_CMP5_EN		
NONE					R/W			NONE	R/W			NONE	R/W		
3f3					7h			1	7h			1	7h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	VMON_CTRL_CMP3_EN			RESERVED	VMON_CTRL_CMP2_EN			RESERVED	VMON_CTRL_CMP1_EN			RESERVED	VMON_CTRL_CMP0_EN		
NONE	R/W			NONE	R/W			NONE	R/W			NONE	R/W		
1	7h			1	7h			1	7h			0	7h		

Access Types Legend

Table 2-38. VMON_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE		Reserved
26:24	VMON_CTRL_CMP8_EN	R/W	7h	VMON EN Reset Source: mod_g_rst_n
23	RESERVED	NONE		Reserved
22:20	VMON_CTRL_CMP7_EN	R/W	7h	VMON EN Reset Source: mod_g_rst_n
19	RESERVED	NONE		Reserved
18:16	VMON_CTRL_CMP5_EN	R/W	7h	VMON EN Reset Source: mod_g_rst_n
15	RESERVED	NONE		Reserved
14:12	VMON_CTRL_CMP3_EN	R/W	7h	VMON EN Reset Source: mod_g_rst_n
11	RESERVED	NONE		Reserved
10:8	VMON_CTRL_CMP2_EN	R/W	7h	VMON EN Reset Source: mod_g_rst_n
7	RESERVED	NONE		Reserved
6:4	VMON_CTRL_CMP1_EN	R/W	7h	VMON EN Reset Source: mod_g_rst_n
3	RESERVED	NONE		Reserved
2:0	VMON_CTRL_CMP0_EN	R/W	7h	VMON EN Reset Source: mod_g_rst_n

2.2.19 CFG0_VMON_STAT Registers

2.2.19.1 CFG0_STAT Register (Offset = C14h) [reset = 7ffh]

Short Description:

Long Description:

Return to Summary Table

Table 2-39. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0C14h

Figure 2-19. VMON_STAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
423a35c7															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					VMON_STAT_CMP8_UV_OK	VMON_STAT_CMP7_UV_OK	VMON_STAT_CMP5_UV_OK	VMON_STAT_CMP5_OV_OK	VMON_STAT_CMP3_UV_OK	VMON_STAT_CMP3_OV_OK	VMON_STAT_CMP2_UV_OK	VMON_STAT_CMP2_OV_OK	VMON_STAT_CMP1_UV_OK	VMON_STAT_CMP1_OV_OK	VMON_STAT_CMP0_UV_OK
NONE					R	R	R	R	R	R	R	R	R	R	R
423a35c7					1h	1h	1h	1h	1h	1h	1h	1h	1h	1h	1h

Access Types Legend

Table 2-40. VMON_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE		Reserved
10	VMON_STAT_CMP8_UV_OK	R	1h	VMON OK Reset Source: mod_g_rst_n
9	VMON_STAT_CMP7_UV_OK	R	1h	VMON OK Reset Source: mod_g_rst_n
8	VMON_STAT_CMP5_UV_OK	R	1h	VMON OK Reset Source: mod_g_rst_n
7	VMON_STAT_CMP5_OV_OK	R	1h	VMON OK Reset Source: mod_g_rst_n
6	VMON_STAT_CMP3_UV_OK	R	1h	VMON OK Reset Source: mod_g_rst_n
5	VMON_STAT_CMP3_OV_OK	R	1h	VMON OK Reset Source: mod_g_rst_n
4	VMON_STAT_CMP2_UV_OK	R	1h	VMON OK Reset Source: mod_g_rst_n
3	VMON_STAT_CMP2_OV_OK	R	1h	VMON OK Reset Source: mod_g_rst_n
2	VMON_STAT_CMP1_UV_OK	R	1h	VMON OK Reset Source: mod_g_rst_n
1	VMON_STAT_CMP1_OV_OK	R	1h	VMON OK Reset Source: mod_g_rst_n
0	VMON_STAT_CMP0_UV_OK	R	1h	VMON OK Reset Source: mod_g_rst_n

2.2.20 CFG0_PMU_COARSE_STAT Registers

2.2.20.1 CFG0_COARSE_STAT Register (Offset = C18h) [reset = fh]

Short Description:

Long Description:

Return to Summary Table

Table 2-41. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0C18h

Figure 2-20. PMU_COARSE_STAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
6f															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												PMU_COARSE_STAT_VSUP18_RDY	PMU_COARSE_STAT_VCORE_RDY	PMU_COARSE_STAT_LDO_RDY	PMU_COARSE_STAT_BG_RDY
NONE												R	R	R	R
6f												1h	1h	1h	1h

Access Types Legend

Table 2-42. PMU_COARSE_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	PMU_COARSE_STAT_VSUP18_RDY	R	1h	Coarse VMON OK Reset Source: mod_g_rst_n
2	PMU_COARSE_STAT_VCORE_RDY	R	1h	Coarse VMON OK Reset Source: mod_g_rst_n
1	PMU_COARSE_STAT_LDO_RDY	R	1h	Coarse VMON OK Reset Source: mod_g_rst_n
0	PMU_COARSE_STAT_BG_RDY	R	1h	Coarse VMON OK Reset Source: mod_g_rst_n

2.2.21 CFG0_MASK_VMON_ERROR_ESM_H Registers

2.2.21.1 CFG0_VMON_ERROR_ESM_H Register (Offset = C20h) [reset = 1ffffh]

Short Description:

Long Description:

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Table 2-43. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0C20h

Figure 2-21. MASK_VMON_ERROR_ESM_H Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															MASK_VMON_ERROR_ESM_H_ADC34_REF_UV_MASK
NONE															R/W
a1b01d4b1c7															1h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK_VMON_ERROR_ESM_H_ADC34_REF_OV_MASK	MASK_VMON_ERROR_ESM_H_ADC12_REF_UV_MASK	MASK_VMON_ERROR_ESM_H_ADC12_REF_OV_MASK	MASK_VMON_ERROR_ESM_H_ADC0_REF_UV_MASK	MASK_VMON_ERROR_ESM_H_ADC0_REF_OV_MASK	MASK_VMON_ERROR_ESM_H_CMP8_UV_ERR_MASK	MASK_VMON_ERROR_ESM_H_CMP7_UV_ERR_MASK	MASK_VMON_ERROR_ESM_H_CMP5_UV_ERR_MASK	MASK_VMON_ERROR_ESM_H_CMP5_OV_ERR_MASK	MASK_VMON_ERROR_ESM_H_CMP3_UV_ERR_MASK	MASK_VMON_ERROR_ESM_H_CMP3_OV_ERR_MASK	MASK_VMON_ERROR_ESM_H_CMP2_UV_ERR_MASK	MASK_VMON_ERROR_ESM_H_CMP2_OV_ERR_MASK	MASK_VMON_ERROR_ESM_H_CMP1_UV_ERR_NASK	MASK_VMON_ERROR_ESM_H_CMP1_OV_ERR_MASK	MASK_VMON_ERROR_ESM_H_CMP0_UV_ERR_MASK
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	1h	1h	1h	1h	1h	1h	1h	1h	1h	1h	1h	1h	1h	1h	1h

Access Types Legend

Table 2-44. MASK_VMON_ERROR_ESM_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE		Reserved
16	MASK_VMON_ERROR_ESM_H_ADC34_REF_UV_MASK	R/W	1h	VMON Error Mask to ESM Reset Source: mod_g_rst_n
15	MASK_VMON_ERROR_ESM_H_ADC34_REF_OV_MASK	R/W	1h	VMON Error Mask to ESM Reset Source: mod_g_rst_n
14	MASK_VMON_ERROR_ESM_H_ADC12_REF_UV_MASK	R/W	1h	VMON Error Mask to ESM Reset Source: mod_g_rst_n
13	MASK_VMON_ERROR_ESM_H_ADC12_REF_OV_MASK	R/W	1h	VMON Error Mask to ESM Reset Source: mod_g_rst_n

Table 2-44. MASK_VMON_ERROR_ESM_H Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	MASK_VMON_ERROR_ESM_H_ADC0_REF_UV_MASK	R/W	1h	VMON Error Mask to ESM Reset Source: mod_g_rst_n
11	MASK_VMON_ERROR_ESM_H_ADC0_REF_OV_MASK	R/W	1h	VMON Error Mask to ESM Reset Source: mod_g_rst_n
10	MASK_VMON_ERROR_ESM_H_CMP8_UV_ERR_MASK	R/W	1h	VMON Error Mask to ESM Reset Source: mod_g_rst_n
9	MASK_VMON_ERROR_ESM_H_CMP7_UV_ERR_MASK	R/W	1h	VMON Error Mask to ESM Reset Source: mod_g_rst_n
8	MASK_VMON_ERROR_ESM_H_CMP5_UV_ERR_MASK	R/W	1h	VMON Error Mask to ESM Reset Source: mod_g_rst_n
7	MASK_VMON_ERROR_ESM_H_CMP5_OV_ERR_MASK	R/W	1h	VMON Error Mask to ESM Reset Source: mod_g_rst_n
6	MASK_VMON_ERROR_ESM_H_CMP3_UV_ERR_MASK	R/W	1h	VMON Error Mask to ESM Reset Source: mod_g_rst_n
5	MASK_VMON_ERROR_ESM_H_CMP3_OV_ERR_MASK	R/W	1h	VMON Error Mask to ESM Reset Source: mod_g_rst_n
4	MASK_VMON_ERROR_ESM_H_CMP2_UV_ERR_MASK	R/W	1h	VMON Error Mask to ESM Reset Source: mod_g_rst_n
3	MASK_VMON_ERROR_ESM_H_CMP2_OV_ERR_MASK	R/W	1h	VMON Error Mask to ESM Reset Source: mod_g_rst_n
2	MASK_VMON_ERROR_ESM_H_CMP1_UV_ERR_NASK	R/W	1h	VMON Error Mask to ESM Reset Source: mod_g_rst_n
1	MASK_VMON_ERROR_ESM_H_CMP1_OV_ERR_MASK	R/W	1h	VMON Error Mask to ESM Reset Source: mod_g_rst_n
0	MASK_VMON_ERROR_ESM_H_CMP0_UV_ERR_MASK	R/W	1h	VMON Error Mask to ESM Reset Source: mod_g_rst_n

2.2.22 CFG0_MASK_VMON_ERROR_ESM_L Registers

2.2.22.1 CFG0_VMON_ERROR_ESM_L Register (Offset = C24h) [reset = 1ffffh]

Short Description:

Long Description:

Return to Summary Table

Table 2-45. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0C24h

Figure 2-22. MASK_VMON_ERROR_ESM_L Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															MASK_VMON_ERROR_ESM_L_ADC34_REF_UV_MASK
NONE															R/W
a1b01d4b1c7															1h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK_VMON_ERROR_ESM_L_ADC34_REF_OV_MASK	MASK_VMON_ERROR_ESM_L_ADC12_REF_UV_MASK	MASK_VMON_ERROR_ESM_L_ADC12_REF_OV_MASK	MASK_VMON_ERROR_ESM_L_ADC0_REF_UV_MASK	MASK_VMON_ERROR_ESM_L_ADC0_REF_OV_MASK	MASK_VMON_ERROR_ESM_L_CMP8_UV_ERR_MASK	MASK_VMON_ERROR_ESM_L_CMP7_UV_ERR_MASK	MASK_VMON_ERROR_ESM_L_CMP5_UV_ERR_MASK	MASK_VMON_ERROR_ESM_L_CMP5_OV_ERR_MASK	MASK_VMON_ERROR_ESM_L_CMP3_UV_ERR_MASK	MASK_VMON_ERROR_ESM_L_CMP3_OV_ERR_MASK	MASK_VMON_ERROR_ESM_L_CMP2_UV_ERR_MASK	MASK_VMON_ERROR_ESM_L_CMP2_OV_ERR_MASK	MASK_VMON_ERROR_ESM_L_CMP1_UV_ERR_N ASK	MASK_VMON_ERROR_ESM_L_CMP1_OV_ERR_MASK	MASK_VMON_ERROR_ESM_L_CMP0_UV_ERR_MASK
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	1h	1h	1h	1h	1h	1h	1h	1h	1h	1h	1h	1h	1h	1h	1h

Access Types Legend

Table 2-46. MASK_VMON_ERROR_ESM_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE		Reserved
16	MASK_VMON_ERROR_ESM_L_ADC34_REF_UV_MASK	R/W	1h	VMON Error Mask to INTR Reset Source: mod_g_rst_n
15	MASK_VMON_ERROR_ESM_L_ADC34_REF_OV_MASK	R/W	1h	VMON Error Mask to INTR Reset Source: mod_g_rst_n
14	MASK_VMON_ERROR_ESM_L_ADC12_REF_UV_MASK	R/W	1h	VMON Error Mask to INTR Reset Source: mod_g_rst_n
13	MASK_VMON_ERROR_ESM_L_ADC12_REF_OV_MASK	R/W	1h	VMON Error Mask to INTR Reset Source: mod_g_rst_n
12	MASK_VMON_ERROR_ESM_L_ADC0_REF_UV_MASK	R/W	1h	VMON Error Mask to INTR Reset Source: mod_g_rst_n

Table 2-46. MASK_VMON_ERROR_ESM_L Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	MASK_VMON_ERROR_ESM_L_ADC0_REF_OV_MASK	R/W	1h	VMON Error Mask to INTR Reset Source: mod_g_rst_n
10	MASK_VMON_ERROR_ESM_L_CMP8_UV_ERR_MASK	R/W	1h	VMON Error Mask to INTR Reset Source: mod_g_rst_n
9	MASK_VMON_ERROR_ESM_L_CMP7_UV_ERR_MASK	R/W	1h	VMON Error Mask to INTR Reset Source: mod_g_rst_n
8	MASK_VMON_ERROR_ESM_L_CMP5_UV_ERR_MASK	R/W	1h	VMON Error Mask to INTR Reset Source: mod_g_rst_n
7	MASK_VMON_ERROR_ESM_L_CMP5_OV_ERR_MASK	R/W	1h	VMON Error Mask to INTR Reset Source: mod_g_rst_n
6	MASK_VMON_ERROR_ESM_L_CMP3_UV_ERR_MASK	R/W	1h	VMON Error Mask to INTR Reset Source: mod_g_rst_n
5	MASK_VMON_ERROR_ESM_L_CMP3_OV_ERR_MASK	R/W	1h	VMON Error Mask to INTR Reset Source: mod_g_rst_n
4	MASK_VMON_ERROR_ESM_L_CMP2_UV_ERR_MASK	R/W	1h	VMON Error Mask to INTR Reset Source: mod_g_rst_n
3	MASK_VMON_ERROR_ESM_L_CMP2_OV_ERR_MASK	R/W	1h	VMON Error Mask to INTR Reset Source: mod_g_rst_n
2	MASK_VMON_ERROR_ESM_L_CMP1_UV_ERR_NASK	R/W	1h	VMON Error Mask to INTR Reset Source: mod_g_rst_n
1	MASK_VMON_ERROR_ESM_L_CMP1_OV_ERR_MASK	R/W	1h	VMON Error Mask to INTR Reset Source: mod_g_rst_n
0	MASK_VMON_ERROR_ESM_L_CMP0_UV_ERR_MASK	R/W	1h	VMON Error Mask to INTR Reset Source: mod_g_rst_n

2.2.23 CFG0_VMON_FILTER_CTRL Registers

2.2.23.1 CFG0_FILTER_CTRL Register (Offset = C34h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-47. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0C34h

Figure 2-23. VMON_FILTER_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														VMON_FILTER_CTRL_SELECT_VALUE	
NONE														R/W	
0														0h	

Access Types Legend

Table 2-48. VMON_FILTER_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1:0	VMON_FILTER_CTRL_SELECT_VALUE	R/W	0h	VMON FILTER control select 00 : no filtering (default) 01 : filtering for 4.8us 10 : filtering for 9.6us 11 : filtering for 14.4us **Note: This bit will only be reset by PORz. Reset Source: mod_por_rst_n

2.2.24 CFG0_TSENSE_CFG Registers

2.2.24.1 CFG0_CFG Register (Offset = D00h) [reset = 11110000h]

Short Description:

Long Description:

Return to Summary Table

Table 2-49. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0D00h

Figure 2-24. TSENSE_CFG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			TSENSE_CFG_TMPSOFF	RESERVED			TSENSE_CFG_BGROFF	RESERVED			TSENSE_CFG_AIPOFF	RESERVED			TSENSE_CFG_SNSR_MX_HIZ
NONE			R/W	NONE			R/W	NONE			R/W	NONE			R/W
0			1h	0			1h	0			1h	0			1h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			TSENSE_CFG_DELAY					TSENSE_CFG_SENSOR_SEL				RESERVED			TSENSE_CFG_ENABLE
NONE			R/W					R/W				NONE			R/W
0			0h					0h				0			0h

Access Types Legend

Table 2-50. TSENSE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28	TSENSE_CFG_TMPSOFF	R/W	1h	Temperature sensor off 0 : on 1 : off **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
27:25	RESERVED	NONE		Reserved
24	TSENSE_CFG_BGROFF	R/W	1h	BandGap on/off control 1 : off 0 : on **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
23:21	RESERVED	NONE		Reserved
20	TSENSE_CFG_AIPOFF	R/W	1h	1 : iddq mode select 0 : normal mode **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
19:17	RESERVED	NONE		Reserved
16	TSENSE_CFG_SNSR_MX_HIZ	R/W	1h	sensor mux hiz control 0 : normal operation. Mux will select either one of the anlaog sensor 1 : mux will be high impedence **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
15:14	RESERVED	NONE		Reserved
13:8	TSENSE_CFG_DELAY	R/W	0h	number of wait clock cycles between each TMPS Readout. Configure a Non zero value as delay value since configuring 0 is not allowed **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
7:4	TSENSE_CFG_SENSOR_SEL	R/W	0h	Sensor Selection sensor enable bits for each sensor 0 : sensor disable 1 : sensor enable bit3: temp_sensor3 bit2: temp_sensor2 bit1: temp_sensor1 bit0: temp_sensor0 **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
3:1	RESERVED	NONE		Reserved

Table 2-50. TSENSE_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TSENSE_CFG_ENABLE	R/W	0h	Temperature controller enable **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n

2.2.25 CFG0_TSENSE_STATUS Registers

2.2.25.1 CFG0_STATUS Register (Offset = D04h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-51. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0D04h

Figure 2-25. TSENSE_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									TSENSE_STATUS_S1_COLD	TSENSE_STATUS_S1_HOT	TSENSE_STATUS_S1_LOW_THRHLD	RESERVED	TSENSE_STATUS_S0_COLD	TSENSE_STATUS_S0_HOT	TSENSE_STATUS_S0_LOW_THRHLD
NONE									R	R	R	NONE	R	R	R
0									0h	0h	0h	0	0h	0h	0h

Access Types Legend

Table 2-52. TSENSE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE		Reserved
6	TSENSE_STATUS_S1_COLD	R	0h	temperature Sensor 1 hot event detect 0 : event not occured 1 : event occurred **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
5	TSENSE_STATUS_S1_HOT	R	0h	temperature Sensor 1 cold event detect 0 : event not occured 1 : event occurred **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
4	TSENSE_STATUS_S1_LOW_THRHLD	R	0h	temperature Sensor 1 low threshold event detect 0 : event not occured 1 : event occurred **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
3	RESERVED	NONE		Reserved
2	TSENSE_STATUS_S0_COLD	R	0h	temperature Sensor 0 hot event detect 0 : event not occured 1 : event occurred **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
1	TSENSE_STATUS_S0_HOT	R	0h	temperature Sensor 0 cold event detect 0 : event not occured 1 : event occurred **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
0	TSENSE_STATUS_S0_LOW_THRHLD	R	0h	temperature Sensor 0 low threshold event detect 0 : event not occured 1 : event occurred **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n

2.2.26 CFG0_TSENSE_STATUS_RAW Registers

2.2.26.1 CFG0_STATUS_RAW Register (Offset = D08h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-53. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0D08h

Figure 2-26. TSENSE_STATUS_RAW Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									TSENSE_STATUS_RAW_S1_COLD	TSENSE_STATUS_RAW_S1_HOT	TSENSE_STATUS_RAW_S1_LOW_THRHLD	RESERVED	TSENSE_STATUS_RAW_S0_COLD	TSENSE_STATUS_RAW_S0_HOT	TSENSE_STATUS_RAW_S0_LOW_THRHLD
NONE									R	R	R	NONE	R	R	R
0									0h	0h	0h	0	0h	0h	0h

Access Types Legend

Table 2-54. TSENSE_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE		Reserved
6	TSENSE_STATUS_RAW_S1_COLD	R	0h	temperature Sensor 1 hot event detect 0 : event not occured 1 : event occurred **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
5	TSENSE_STATUS_RAW_S1_HOT	R	0h	temperature Sensor 1 cold event detect 0 : event not occured 1 : event occurred **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
4	TSENSE_STATUS_RAW_S1_LOW_THRHLD	R	0h	temperature Sensor 1 low threshold event detect 0 : event not occured 1 : event occurred **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
3	RESERVED	NONE		Reserved
2	TSENSE_STATUS_RAW_S0_COLD	R	0h	temperature Sensor 0 hot event detect 0 : event not occured 1 : event occurred **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
1	TSENSE_STATUS_RAW_S0_HOT	R	0h	temperature Sensor 0 cold event detect 0 : event not occured 1 : event occurred **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
0	TSENSE_STATUS_RAW_S0_LOW_THRHLD	R	0h	temperature Sensor 0 low threshold event detect 0 : event not occured 1 : event occurred **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n

2.2.27 CFG0_TSENSE0_ALERT Registers

2.2.27.1 CFG0_ALERT Register (Offset = D14h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-55. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0D14h

Figure 2-27. TSENSE0_ALERT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								TSENSE0_ALERT_ALERT_THRHLD_HOT							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TSENSE0_ALERT_ALERT_THRHLD_COLD							
NONE								R/W							
0								0h							

Access Types Legend

Table 2-56. TSENSE0_ALERT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	TSENSE0_ALERT_ALERT_THRHLD_HOT	R/W	0h	cold threshold/low temp threshold **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
15:8	RESERVED	NONE		Reserved
7:0	TSENSE0_ALERT_ALERT_THRHLD_COLD	R/W	0h	hot threshold/high temp threshold **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n

2.2.28 CFG0_TSENSE0_CNTL Registers

2.2.28.1 CFG0_CNTL Register (Offset = D18h) [reset = 100000h]

Short Description:

Long Description:

Return to Summary Table

Table 2-57. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0D18h

Figure 2-28. TSENSE0_CNTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							TSENSE0_CNTL_MASK_LOW_THRHLD	RESERVED			TSENSE0_CNTL_MASK_COLD	RESERVED			TSENSE0_CNTL_MASK_HOT
NONE							R/W	NONE			R/W	NONE			R/W
0							0h	0			1h	0			0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							TSENSE0_CNTL_ACCU_CLEAR	RESERVED			TSENSE0_CNTL_FIFO_FREEZE	RESERVED			TSENSE0_CNTL_FIFO_CLEAR
NONE							R/W	NONE			R/W	NONE			R/W
3e8							0h	0			0h	0			0h

Access Types Legend

Table 2-58. TSENSE0_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24	TSENSE0_CNTL_MASK_LOW_THRHLD	R/W	0h	mask low threshold comparator output **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
23:21	RESERVED	NONE		Reserved
20	TSENSE0_CNTL_MASK_COLD	R/W	1h	Mask hot comparator output **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
19:17	RESERVED	NONE		Reserved
16	TSENSE0_CNTL_MASK_HOT	R/W	0h	mask cold comparator output **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
15:9	RESERVED	NONE		Reserved
8	TSENSE0_CNTL_ACCU_CLEAR	R/W	0h	accumulator clear **Note: This bit will only be reset by PORz. Reset Source: mod_temp_sense0_accu_rst_n
7:5	RESERVED	NONE		Reserved
4	TSENSE0_CNTL_FIFO_FREEZE	R/W	0h	fifo freeze **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
3:1	RESERVED	NONE		Reserved
0	TSENSE0_CNTL_FIFO_CLEAR	R/W	0h	fifo clear **Note: This bit will only be reset by PORz. Reset Source: mod_temp_sense0_fifo_rst_n

2.2.29 CFG0_TSENSE0_RESULT Registers

2.2.29.1 CFG0_RESULT Register (Offset = D1Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-59. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0D1Ch

Figure 2-29. TSENSE0_RESULT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															TSENSE0_RESULT_ECOZ
NONE															R
0															0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TSENSE0_RESULT_DTEMP							
NONE								R							
0								0h							

Access Types Legend

Table 2-60. TSENSE0_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE		Reserved
16	TSENSE0_RESULT_ECOZ	R	0h	Conversion in Progress. 1 : Conversion on going 0 : conversion completed **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
15:8	RESERVED	NONE		Reserved
7:0	TSENSE0_RESULT_DTEMP	R	0h	Temp Code readout **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n

2.2.30 CFG0_TSENSE0_DATA0 Registers

2.2.30.1 CFG0_DATA0 Register (Offset = D20h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-61. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0D20h

Figure 2-30. TSENSE0_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TSENSE0_DATA0_TAG															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSENSE0_DATA0_TAG								TSENSE0_DATA0_DATA							
R								R							
0h								0h							

Access Types Legend

Table 2-62. TSENSE0_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	TSENSE0_DATA0_TAG	R	0h	tag 0 **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
7:0	TSENSE0_DATA0_DATA	R	0h	fifo data 0 **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n

2.2.31 CFG0_TSENSE0_DATA1 Registers

2.2.31.1 CFG0_DATA1 Register (Offset = D24h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-63. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0D24h

Figure 2-31. TSENSE0_DATA1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TSENSE0_DATA1_TAG															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSENSE0_DATA1_TAG								TSENSE0_DATA1_DATA							
R								R							
0h								0h							

Access Types Legend

Table 2-64. TSENSE0_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	TSENSE0_DATA1_TAG	R	0h	tag 1 **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
7:0	TSENSE0_DATA1_DATA	R	0h	fifo data 1 **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n

2.2.32 CFG0_TSENSE0_DATA2 Registers

2.2.32.1 CFG0_DATA2 Register (Offset = D28h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-65. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0D28h

Figure 2-32. TSENSE0_DATA2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TSENSE0_DATA2_TAG															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSENSE0_DATA2_TAG								TSENSE0_DATA2_DATA							
R								R							
0h								0h							

Access Types Legend

Table 2-66. TSENSE0_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	TSENSE0_DATA2_TAG	R	0h	tag 2 **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
7:0	TSENSE0_DATA2_DATA	R	0h	fifo data 2 **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n

2.2.33 CFG0_TSENSE0_DATA3 Registers

2.2.33.1 CFG0_DATA3 Register (Offset = D2Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-67. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0D2Ch

Figure 2-33. TSENSE0_DATA3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TSENSE0_DATA3_TAG															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSENSE0_DATA3_TAG								TSENSE0_DATA3_DATA							
R								R							
0h								0h							

Access Types Legend

Table 2-68. TSENSE0_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	TSENSE0_DATA3_TAG	R	0h	tag 3 **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
7:0	TSENSE0_DATA3_DATA	R	0h	fifo data 3 **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n

2.2.34 CFG0_TSENSE0_ACCU Registers

2.2.34.1 CFG0_ACCU Register (Offset = D30h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-69. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0D30h

Figure 2-34. TSENSE0_ACCU Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TSENSE0_ACCU_CUMUL															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSENSE0_ACCU_CUMUL															
R															
0h															

Access Types Legend

Table 2-70. TSENSE0_ACCU Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TSENSE0_ACCU_CUMUL	R	0h	cumulative sum of past DTEMPs **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n

2.2.35 CFG0_TSENSE1_ALERT Registers

2.2.35.1 CFG0_ALERT Register (Offset = D44h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-71. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0D44h

Figure 2-35. TSENSE1_ALERT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								TSENSE1_ALERT_ALERT_THRHLD_HOT							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TSENSE1_ALERT_ALERT_THRHLD_COLD							
NONE								R/W							
0								0h							

Access Types Legend

Table 2-72. TSENSE1_ALERT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	TSENSE1_ALERT_ALERT_THRHLD_HOT	R/W	0h	cold threshold/low temp threshold **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
15:8	RESERVED	NONE		Reserved
7:0	TSENSE1_ALERT_ALERT_THRHLD_COLD	R/W	0h	hot threshold/high temp threshold **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n

2.2.36 CFG0_TSENSE1_CNTL Registers

2.2.36.1 CFG0_CNTL Register (Offset = D48h) [reset = 100000h]

Short Description:

Long Description:

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Table 2-73. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0D48h

Figure 2-36. TSENSE1_CNTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							TSENSE1_CNTL_MASK_LOW_THRHLD	RESERVED			TSENSE1_CNTL_MASK_COLD	RESERVED			TSENSE1_CNTL_MASK_HOT
NONE							R/W	NONE			R/W	NONE			R/W
0							0h	0			1h	0			0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							TSENSE1_CNTL_ACCU_CLEAR	RESERVED			TSENSE1_CNTL_FIFO_FREEZE	RESERVED			TSENSE1_CNTL_FIFO_CLEAR
NONE							R/W	NONE			R/W	NONE			R/W
3e8							0h	0			0h	0			0h

Access Types Legend

Table 2-74. TSENSE1_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24	TSENSE1_CNTL_MASK_LOW_THRHLD	R/W	0h	mask low threshold comparator output **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
23:21	RESERVED	NONE		Reserved
20	TSENSE1_CNTL_MASK_COLD	R/W	1h	Mask hot comparator output **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
19:17	RESERVED	NONE		Reserved
16	TSENSE1_CNTL_MASK_HOT	R/W	0h	mask cold comparator output **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
15:9	RESERVED	NONE		Reserved
8	TSENSE1_CNTL_ACCU_CLEAR	R/W	0h	accumulator clear **Note: This bit will only be reset by PORz. Reset Source: mod_temp_sense1_accu_rst_n
7:5	RESERVED	NONE		Reserved
4	TSENSE1_CNTL_FIFO_FREEZE	R/W	0h	fifo freeze **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
3:1	RESERVED	NONE		Reserved
0	TSENSE1_CNTL_FIFO_CLEAR	R/W	0h	fifo clear **Note: This bit will only be reset by PORz. Reset Source: mod_temp_sense1_fifo_rst_n

2.2.37 CFG0_TSENSE1_RESULT Registers

2.2.37.1 CFG0_RESULT Register (Offset = D4Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-75. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0D4Ch

Figure 2-37. TSENSE1_RESULT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															TSENSE1_RESULT_ECOZ
NONE															R
0															0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TSENSE1_RESULT_DTEMP							
NONE								R							
0								0h							

Access Types Legend

Table 2-76. TSENSE1_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE		Reserved
16	TSENSE1_RESULT_ECOZ	R	0h	Conversion in Progress. 1 : Conversion on going 0 : conversion completed **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
15:8	RESERVED	NONE		Reserved
7:0	TSENSE1_RESULT_DTEMP	R	0h	Temp Code readout **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n

2.2.38 CFG0_TSENSE1_DATA0 Registers

2.2.38.1 CFG0_DATA0 Register (Offset = D50h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-77. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0D50h

Figure 2-38. TSENSE1_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TSENSE1_DATA0_TAG															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSENSE1_DATA0_TAG								TSENSE1_DATA0_DATA							
R								R							
0h								0h							

Access Types Legend

Table 2-78. TSENSE1_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	TSENSE1_DATA0_TAG	R	0h	tag 0 **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
7:0	TSENSE1_DATA0_DATA	R	0h	fifo data 0 **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n

2.2.39 CFG0_TSENSE1_DATA1 Registers

2.2.39.1 CFG0_DATA1 Register (Offset = D54h) [reset = 0h]

Short Description:

Long Description:

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Table 2-79. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0D54h

Figure 2-39. TSENSE1_DATA1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TSENSE1_DATA1_TAG															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSENSE1_DATA1_TAG								TSENSE1_DATA1_DATA							
R								R							
0h								0h							

Access Types Legend

Table 2-80. TSENSE1_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	TSENSE1_DATA1_TAG	R	0h	tag 1 **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
7:0	TSENSE1_DATA1_DATA	R	0h	fifo data 1 **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n

2.2.40 CFG0_TSENSE1_DATA2 Registers

2.2.40.1 CFG0_DATA2 Register (Offset = D58h) [reset = 0h]

Short Description:

Long Description:

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Table 2-81. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0D58h

Figure 2-40. TSENSE1_DATA2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TSENSE1_DATA2_TAG															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSENSE1_DATA2_TAG								TSENSE1_DATA2_DATA							
R								R							
0h								0h							

Access Types Legend

Table 2-82. TSENSE1_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	TSENSE1_DATA2_TAG	R	0h	tag 2 **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
7:0	TSENSE1_DATA2_DATA	R	0h	fifo data 2 **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n

2.2.41 CFG0_TSENSE1_DATA3 Registers

2.2.41.1 CFG0_DATA3 Register (Offset = D5Ch) [reset = 0h]

Short Description:

Long Description:

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Table 2-83. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0D5Ch

Figure 2-41. TSENSE1_DATA3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TSENSE1_DATA3_TAG															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSENSE1_DATA3_TAG								TSENSE1_DATA3_DATA							
R								R							
0h								0h							

Access Types Legend

Table 2-84. TSENSE1_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	TSENSE1_DATA3_TAG	R	0h	tag 3 **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
7:0	TSENSE1_DATA3_DATA	R	0h	fifo data 3 **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n

2.2.42 CFG0_TSENSE1_ACCU Registers

2.2.42.1 CFG0_ACCU Register (Offset = D60h) [reset = 0h]

Short Description:

Long Description:

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Table 2-85. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0D60h

Figure 2-42. TSENSE1_ACCU Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TSENSE1_ACCU_CUMUL															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSENSE1_ACCU_CUMUL															
R															
0h															

Access Types Legend

Table 2-86. TSENSE1_ACCU Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TSENSE1_ACCU_CUMUL	R	0h	cumulative sum of past DTEMPs **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n

2.2.43 CFG0_TSENSE2_RESULT Registers

2.2.43.1 CFG0_RESULT Register (Offset = D7Ch) [reset = 0h]

Short Description:

Long Description:

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Table 2-87. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0D7Ch

Figure 2-43. TSENSE2_RESULT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															TSENSE2_RESULT_ECOZ
NONE															R
0															0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TSENSE2_RESULT_DTEMP							
NONE								R							
0								0h							

Access Types Legend

Table 2-88. TSENSE2_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE		Reserved
16	TSENSE2_RESULT_ECOZ	R	0h	Conversion in Progress. 1 : Conversion on going 0 : conversion completed **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
15:8	RESERVED	NONE		Reserved
7:0	TSENSE2_RESULT_DTEMP	R	0h	Temp Code readout **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n

2.2.44 CFG0_TSENSE3_RESULT Registers

2.2.44.1 CFG0_RESULT Register (Offset = DACh) [reset = 0h]

Short Description:

Long Description:

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Table 2-89. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0DACh

Figure 2-44. TSENSE3_RESULT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															TSENSE3_RESULT_ECOZ
NONE															R
0															0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TSENSE3_RESULT_DTEMP							
NONE								R							
0								0h							

Access Types Legend

Table 2-90. TSENSE3_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE		Reserved
16	TSENSE3_RESULT_ECOZ	R	0h	Conversion in Progress. 1 : Conversion on going 0 : conversion completed **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n
15:8	RESERVED	NONE		Reserved
7:0	TSENSE3_RESULT_DTEMP	R	0h	Temp Code readout **Note: This bit will only be reset by PORz. Reset Source: tempsense_mmr_rst_n

2.2.45 CFG0_HW_SPARE_REC0 Registers

2.2.45.1 CFG0_SPARE_REC0 Register (Offset = FF8h) [reset = 0h]

Short Description:

Long Description:

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Table 2-91. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0FF8h

Figure 2-45. HW_SPARE_REC0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
NONE															
0															

Access Types Legend

Table 2-92. HW_SPARE_REC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE		Reserved

2.2.46 CFG0_HW_SPARE_REC1 Registers

2.2.46.1 CFG0_SPARE_REC1 Register (Offset = FFCh) [reset = 0h]

Short Description:

Long Description:

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Table 2-93. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 0FFCh

Figure 2-46. HW_SPARE_REC1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
NONE															
0															

Access Types Legend

Table 2-94. HW_SPARE_REC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE		Reserved

2.2.47 CFG0_LOCK0_KICK0 Registers

2.2.47.1 CFG0_KICK0 Register (Offset = 1008h) [reset = 0h]

Short Description: - KICK0 component

Long Description: - KICK0 component

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Table 2-95. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 1008h

Figure 2-47. LOCK0_KICK0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LOCK0_KICK0															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCK0_KICK0															
R/W															
0h															

Access Types Legend

Table 2-96. LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

2.2.48 CFG0_LOCK0_KICK1 Registers

2.2.48.1 CFG0_KICK1 Register (Offset = 100Ch) [reset = 0h]

Short Description: - KICK1 component

Long Description: - KICK1 component

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Table 2-97. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 100Ch

Figure 2-48. LOCK0_KICK1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LOCK0_KICK1															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCK0_KICK1															
R/W															
0h															

Access Types Legend

Table 2-98. LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

2.2.49 CFG0_INTR_RAW_STATUS Registers

2.2.49.1 CFG0_RAW_STATUS Register (Offset = 1010h) [reset = 0h]

Short Description: Interrupt Raw Status/Set Register

Long Description: Interrupt Raw Status/Set Register

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Table 2-99. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 1010h

Figure 2-49. INTR_RAW_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												PROXY_ERR	KICK_ERR	ADDR_ERR	PROT_ERR
NONE												R/W1TS	R/W1TS	R/W1TS	R/W1TS
0												0h	0h	0h	0h

Access Types Legend

Table 2-100. INTR_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	PROXY_ERR	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

2.2.50 CFG0_INTR_ENABLED_STATUS_CLEAR Registers

2.2.50.1 CFG0_ENABLED_STATUS_CLEAR Register (Offset = 1014h) [reset = 0h]

Short Description: Interrupt Enabled Status/Clear register

Long Description: Interrupt Enabled Status/Clear register

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Table 2-101. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 1014h

Figure 2-50. INTR_ENABLED_STATUS_CLEAR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												ENABLED_PROXY_ERR	ENABLED_KICK_ERR	ENABLED_ADDR_ERR	ENABLED_PROT_ERR
NONE												R/W1TC	R/W1TC	R/W1TC	R/W1TC
0												0h	0h	0h	0h

Access Types Legend

Table 2-102. INTR_ENABLED_STATUS_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	ENABLED_PROXY_ERR	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	ENABLED_KICK_ERR	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ENABLED_ADDR_ERR	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	ENABLED_PROT_ERR	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

2.2.51 CFG0_INTR_ENABLE Registers

2.2.51.1 CFG0_ENABLE Register (Offset = 1018h) [reset = 0h]

Short Description: Interrupt Enable register

Long Description: Interrupt Enable register

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Table 2-103. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 1018h

Figure 2-51. INTR_ENABLE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												PROXY_ERR_EN	KICK_ERR_EN	ADDR_ERR_EN	PROT_ERR_EN
NONE												R/W1TS	R/W1TS	R/W1TS	R/W1TS
0												0h	0h	0h	0h

Access Types Legend

Table 2-104. INTR_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	PROXY_ERR_EN	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

2.2.52 CFG0_INTR_ENABLE_CLEAR Registers

2.2.52.1 CFG0_ENABLE_CLEAR Register (Offset = 101Ch) [reset = 0h]

Short Description: Interrupt Enable Clear register

Long Description: Interrupt Enable Clear register

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Table 2-105. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 101Ch

Figure 2-52. INTR_ENABLE_CLEAR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												PROXY_ERR_EN_CLR	KICK_ERR_EN_CLR	ADDR_ERR_EN_CLR	PROT_ERR_EN_CLR
NONE												R/W1TC	R/W1TC	R/W1TC	R/W1TC
0												0h	0h	0h	0h

Access Types Legend

Table 2-106. INTR_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	PROXY_ERR_EN_CLR	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_CLR	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_CLR	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_CLR	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

2.2.53 CFG0_EOI Registers

2.2.53.1 CFG0_EOI Register (Offset = 1020h) [reset = 0h]

Short Description: EOI register

Long Description: EOI register

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Table 2-107. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 1020h

Figure 2-53. EOI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								EOI_VECTOR							
NONE								R/W							
0								0h							

Access Types Legend

Table 2-108. EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	EOI_VECTOR	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip. Reset Source: mod_g_rst_n

2.2.54 CFG0_FAULT_ADDRESS Registers

2.2.54.1 CFG0_ADDRESS Register (Offset = 1024h) [reset = 0h]

Short Description: Fault Address register

Long Description: Fault Address register

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Table 2-109. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 1024h

Figure 2-54. FAULT_ADDRESS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FAULT_ADDR															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FAULT_ADDR															
R															
0h															

Access Types Legend

Table 2-110. FAULT_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR	R	0h	Fault Address. Reset Source: mod_g_rst_n

2.2.55 CFG0_FAULT_TYPE_STATUS Registers

2.2.55.1 CFG0_TYPE_STATUS Register (Offset = 1028h) [reset = 0h]

Short Description: Fault Type Status register

Long Description: Fault Type Status register

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Table 2-111. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 1028h

Figure 2-55. FAULT_TYPE_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									FAULT_NS	FAULT_TYPE					
NONE									R	R					
0									0h	0h					

Access Types Legend

Table 2-112. FAULT_TYPE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE		Reserved
6	FAULT_NS	R	0h	Non-secure access. Reset Source: mod_g_rst_n
5:0	FAULT_TYPE	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype ! = 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault Reset Source: mod_g_rst_n

2.2.56 CFG0_FAULT_ATTR_STATUS Registers

2.2.56.1 CFG0_ATTR_STATUS Register (Offset = 102Ch) [reset = 0h]

Short Description: Fault Attribute Status register

Long Description: Fault Attribute Status register

Return to Summary Table

Table 2-113. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 102Ch

Figure 2-56. FAULT_ATTR_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FAULT_XID												FAULT_ROUTEID			
R												R			
0h												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FAULT_ROUTEID								FAULT_PRIVID							
R								R							
0h								0h							

Access Types Legend

Table 2-114. FAULT_ATTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID	R	0h	XID. Reset Source: mod_g_rst_n
19:8	FAULT_ROUTEID	R	0h	Route ID. Reset Source: mod_g_rst_n
7:0	FAULT_PRIVID	R	0h	Privilege ID. Reset Source: mod_g_rst_n

2.2.57 CFG0_FAULT_CLEAR Registers

2.2.57.1 CFG0_CLEAR Register (Offset = 1030h) [reset = 0h]

Short Description: Fault Clear register

Long Description: Fault Clear register

Return to Summary Table

Table 2-115. Instance Table

Instance Name	Physical Address
TOP_CTRL_MMR	50D8 1030h

Figure 2-57. FAULT_CLEAR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															FAULT_CLR
NONE															W
0															0h

Access Types Legend

Table 2-116. FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	FAULT_CLR	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. Reset Source: mod_g_rst_n

2.2.58 Access Table

Table 2-117. Access Type Codes

Access Type	Code	Description
R	R	Read
R/W	R/W	Read / Write
R/W1TC	R/W1TC	Read/Write 1 To Clear
R/W1TS	R/W1TS	Read/Write 1 To Set
W	W	Write

2.3 MSS_CTRL Registers

Table 2-118. CFG0, CFG0 Registers, Base Address=0X0000000050D00000, Length=131072

Offset	Length	Register Name	mss_ctrl_mmr Physical Address
20h	32	R5SS0_CONTROL	50D0 0020h
24h	32	R5SS0_CORE0_HALT	50D0 0024h
28h	32	R5SS0_CORE1_HALT	50D0 0028h
2Ch	32	R5SS0_STATUS_REG	50D0 002Ch
30h	32	R5SS0_CORE0_STAT	50D0 0030h
34h	32	R5SS0_CORE1_STAT	50D0 0034h
38h	32	R5SS0_FORCE_WFI	50D0 0038h
40h	32	R5SS1_CONTROL	50D0 0040h
44h	32	R5SS1_CORE0_HALT	50D0 0044h
48h	32	R5SS1_CORE1_HALT	50D0 0048h
4Ch	32	R5SS1_STATUS_REG	50D0 004Ch
50h	32	R5SS1_CORE0_STAT	50D0 0050h
54h	32	R5SS1_CORE1_STAT	50D0 0054h
58h	32	R5SS1_FORCE_WFI	50D0 0058h
80h	32	R5SS0_ROM_ECLIPSE	50D0 0080h
90h	32	R5SS0_TEINIT	50D0 0090h
94h	32	R5SS1_TEINIT	50D0 0094h
A0h	32	R5SS0_CORE0_AHB_BASE	50D0 00A0h
A4h	32	R5SS1_CORE0_AHB_BASE	50D0 00A4h
A8h	32	R5SS0_CORE0_AHB_SIZE	50D0 00A8h
ACh	32	R5SS1_CORE0_AHB_SIZE	50D0 00ACh
B0h	32	R5SS0_CORE1_AHB_BASE	50D0 00B0h
B4h	32	R5SS1_CORE1_AHB_BASE	50D0 00B4h
B8h	32	R5SS0_CORE1_AHB_SIZE	50D0 00B8h
BCh	32	R5SS1_CORE1_AHB_SIZE	50D0 00BCh
D8h	32	R5SS0_TCM_ECC_WRENZ_EN	50D0 00D8h
DCh	32	R5SS1_TCM_ECC_WRENZ_EN	50D0 00DCh
100h	32	BOOT_INFO_REG0	50D0 0100h
104h	32	BOOT_INFO_REG1	50D0 0104h
108h	32	BOOT_INFO_REG2	50D0 0108h
10Ch	32	BOOT_INFO_REG3	50D0 010Ch
110h	32	BOOT_INFO_REG4	50D0 0110h
114h	32	BOOT_INFO_REG5	50D0 0114h
118h	32	BOOT_INFO_REG6	50D0 0118h
11Ch	32	BOOT_INFO_REG7	50D0 011Ch
200h	32	R5SS0_ATCM_MEM_INIT	50D0 0200h
204h	32	R5SS0_ATCM_MEM_INIT_DONE	50D0 0204h
208h	32	R5SS0_ATCM_MEM_INIT_STATUS	50D0 0208h
210h	32	R5SS0_BTCM_MEM_INIT	50D0 0210h
214h	32	R5SS0_BTCM_MEM_INIT_DONE	50D0 0214h
218h	32	R5SS0_BTCM_MEM_INIT_STATUS	50D0 0218h
220h	32	R5SS1_ATCM_MEM_INIT	50D0 0220h
224h	32	R5SS1_ATCM_MEM_INIT_DONE	50D0 0224h
228h	32	R5SS1_ATCM_MEM_INIT_STATUS	50D0 0228h
230h	32	R5SS1_BTCM_MEM_INIT	50D0 0230h

Table 2-118. CFG0, CFG0 Registers, Base Address=0X0000000050D00000, Length=131072 (continued)

Offset	Length	Register Name	mss_ctrl_mmr Physical Address
234h	32	R5SS1_BTCM_MEM_INIT_DONE	50D0 0234h
238h	32	R5SS1_BTCM_MEM_INIT_STATUS	50D0 0238h
240h	32	L2IOCRAM_MEM_INIT	50D0 0240h
244h	32	L2OCRAM_MEM_INIT_DONE	50D0 0244h
248h	32	L2OCRAM_MEM_INIT_STATUS	50D0 0248h
250h	32	MAILBOXRAM_MEM_INIT	50D0 0250h
254h	32	MAILBOXRAM_MEM_INIT_DONE	50D0 0254h
258h	32	MAILBOXRAM_MEM_INIT_STATUS	50D0 0258h
260h	32	TPCC_MEM_INIT	50D0 0260h
264h	32	TPCC_MEM_INIT_DONE	50D0 0264h
268h	32	TPCC_MEMINIT_STATUS	50D0 0268h
300h	32	TOP_PBIST_KEY_RST	50D0 0300h
304h	32	TOP_PBIST_REG0	50D0 0304h
308h	32	TOP_PBIST_REG1	50D0 0308h
30Ch	32	TOP_PBIST_REG2	50D0 030Ch
400h	32	R5SS0_CTI_TRIG_SEL	50D0 0400h
404h	32	R5SS1_CTI_TRIG_SEL	50D0 0404h
408h	32	DBGSS_CTI_TRIG_SEL	50D0 0408h
420h	32	MCAN0_HALTEN	50D0 0420h
424h	32	MCAN1_HALTEN	50D0 0424h
428h	32	MCAN2_HALTEN	50D0 0428h
42Ch	32	MCAN3_HALTEN	50D0 042Ch
430h	32	LIN0_HALTEN	50D0 0430h
434h	32	LIN1_HALTEN	50D0 0434h
438h	32	LIN2_HALTEN	50D0 0438h
43Ch	32	LIN3_HALTEN	50D0 043Ch
440h	32	LIN4_HALTEN	50D0 0440h
444h	32	I2C0_HALTEN	50D0 0444h
448h	32	I2C1_HALTEN	50D0 0448h
44Ch	32	I2C2_HALTEN	50D0 044Ch
450h	32	I2C3_HALTEN	50D0 0450h
454h	32	RTI0_HALTEN	50D0 0454h
458h	32	RTI1_HALTEN	50D0 0458h
45Ch	32	RTI2_HALTEN	50D0 045Ch
460h	32	RTI3_HALTEN	50D0 0460h
474h	32	CPSW_HALTEN	50D0 0474h
478h	32	MCRC0_HALTEN	50D0 0478h
800h	32	TPTC_DBS_CONFIG	50D0 0800h
804h	32	TPTC_BOUNDARY_CFG	50D0 0804h
808h	32	TPTC_XID_REORDER_CFG	50D0 0808h
810h	32	CPSW_CONTROL	50D0 0810h
814h	32	QSPI_CONFIG	50D0 0814h
818h	32	ICSSM_IDLE_CONTROL	50D0 0818h
81Ch	32	PRU-ICSS_PRU0_GPI_SEL	50D0 081Ch
820h	32	PRU-ICSS_PRU1_GPI_SEL	50D0 0820h
824h	32	PRU-ICSS_PRU0_GPIO_OUT_CTRL	50D0 0824h
828h	32	PRU-ICSS_PRU1_GPIO_OUT_CTRL	50D0 0828h

Table 2-118. CFG0, CFG0 Registers, Base Address=0X0000000050D00000, Length=131072 (continued)

Offset	Length	Register Name	mss_ctrl_mmr Physical Address
82Ch	32	GPMC_CONTROL	50D0 082Ch
830h	32	TPCC0_INTAGG_MASK	50D0 0830h
834h	32	TPCC0_INTAGG_STATUS	50D0 0834h
838h	32	TPCC0_INTAGG_STATUS_RAW	50D0 0838h
1008h	32	LOCK0_KICK0	50D0 1008h
100Ch	32	LOCK0_KICK1	50D0 100Ch
1010h	32	intr_raw_status	50D0 1010h
1014h	32	intr_enabled_status_clear	50D0 1014h
1018h	32	intr_enable	50D0 1018h
101Ch	32	intr_enable_clear	50D0 101Ch
1020h	32	eoi	50D0 1020h
1024h	32	fault_address	50D0 1024h
1028h	32	fault_type_status	50D0 1028h
102Ch	32	fault_attr_status	50D0 102Ch
1030h	32	fault_clear	50D0 1030h
4000h	32	R5SS0_CORE0_MBOX_WRITE_DONE	50D0 4000h
4004h	32	R5SS0_CORE0_MBOX_READ_REQ	50D0 4004h
4008h	32	R5SS0_CORE0_MBOX_READ_DONE_ACK	50D0 4008h
400Ch	32	R5SS0_CORE0_MBOX_READ_DONE	50D0 400Ch
4010h	32	R5SS0_CORE0_SW_INT	50D0 4010h
4020h	32	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK	50D0 4020h
4024h	32	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS	50D0 4024h
4028h	32	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW	50D0 4028h
4030h	32	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK	50D0 4030h
4034h	32	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS	50D0 4034h
4038h	32	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW	50D0 4038h
8000h	32	R5SS0_CORE1_MBOX_WRITE_DONE	50D0 8000h
8004h	32	R5SS0_CORE1_MBOX_READ_REQ	50D0 8004h
8008h	32	R5SS0_CORE1_MBOX_READ_DONE_ACK	50D0 8008h
800Ch	32	R5SS0_CORE1_MBOX_READ_DONE	50D0 800Ch
8010h	32	R5SS0_CORE1_SW_INT	50D0 8010h
8020h	32	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK	50D0 8020h
8024h	32	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS	50D0 8024h
8028h	32	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW	50D0 8028h
8030h	32	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK	50D0 8030h
8034h	32	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS	50D0 8034h
8038h	32	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW	50D0 8038h
C000h	32	R5SS1_CORE0_MBOX_WRITE_DONE	50D0 C000h
C004h	32	R5SS1_CORE0_MBOX_READ_REQ	50D0 C004h
C008h	32	R5SS1_CORE0_MBOX_READ_DONE_ACK	50D0 C008h
C00Ch	32	R5SS1_CORE0_MBOX_READ_DONE	50D0 C00Ch
C010h	32	R5SS1_CORE0_SW_INT	50D0 C010h
C020h	32	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK	50D0 C020h
C024h	32	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS	50D0 C024h
C028h	32	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW	50D0 C028h
C030h	32	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK	50D0 C030h
C034h	32	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS	50D0 C034h

Table 2-118. CFG0, CFG0 Registers, Base Address=0X0000000050D00000, Length=131072 (continued)

Offset	Length	Register Name	mss_ctrl_mmr Physical Address
C038h	32	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW	50D0 C038h
10000h	32	R5SS1_CORE1_MBOX_WRITE_DONE	50D1 0000h
10004h	32	R5SS1_CORE1_MBOX_READ_REQ	50D1 0004h
10008h	32	R5SS1_CORE1_MBOX_READ_DONE_ACK	50D1 0008h
1000Ch	32	R5SS1_CORE1_MBOX_READ_DONE	50D1 000Ch
10010h	32	R5SS1_CORE1_SW_INT	50D1 0010h
10020h	32	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK	50D1 0020h
10024h	32	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS	50D1 0024h
10028h	32	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW	50D1 0028h
10030h	32	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK	50D1 0030h
10034h	32	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS	50D1 0034h
10038h	32	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW	50D1 0038h
14000h	32	PRU-ICSS_PRU0_MBOX_WRITE_DONE	50D1 4000h
14004h	32	PRU-ICSS_PRU0_MBOX_READ_REQ	50D1 4004h
14008h	32	PRU-ICSS_PRU0_MBOX_READ_DONE_ACK	50D1 4008h
1400Ch	32	PRU-ICSS_PRU0_MBOX_READ_DONE	50D1 400Ch
14010h	32	PRU-ICSS_PRU1_MBOX_WRITE_DONE	50D1 4010h
14014h	32	PRU-ICSS_PRU1_MBOX_READ_REQ	50D1 4014h
14018h	32	PRU-ICSS_PRU1_MBOX_READ_DONE_ACK	50D1 4018h
1401Ch	32	PRU-ICSS_PRU1_MBOX_READ_DONE	50D1 401Ch
18000h	32	TPCC0_ERRAGG_MASK	50D1 8000h
18004h	32	TPCC0_ERRAGG_STATUS	50D1 8004h
18008h	32	TPCC0_ERRAGG_STATUS_RAW	50D1 8008h
18010h	32	MMR_ACCESS_ERRAGG_MASK0	50D1 8010h
18014h	32	MMR_ACCESS_ERRAGG_STATUS0	50D1 8014h
18018h	32	MMR_ACCESS_ERRAGG_STATUS_RAW0	50D1 8018h
18080h	32	R5SS0_CPU0_ECC_CORR_ERRAGG_MASK	50D1 8080h
18084h	32	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS	50D1 8084h
18088h	32	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW	50D1 8088h
18090h	32	R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK	50D1 8090h
18094h	32	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS	50D1 8094h
18098h	32	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW	50D1 8098h
180A0h	32	R5SS0_CPU1_ECC_CORR_ERRAGG_MASK	50D1 80A0h
180A4h	32	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS	50D1 80A4h
180A8h	32	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW	50D1 80A8h
180B0h	32	R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK	50D1 80B0h
180B4h	32	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS	50D1 80B4h
180B8h	32	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW	50D1 80B8h
180C0h	32	R5SS1_CPU0_ECC_CORR_ERRAGG_MASK	50D1 80C0h
180C4h	32	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS	50D1 80C4h
180C8h	32	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW	50D1 80C8h
180D0h	32	R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK	50D1 80D0h
180D4h	32	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS	50D1 80D4h
180D8h	32	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW	50D1 80D8h
180E0h	32	R5SS1_CPU1_ECC_CORR_ERRAGG_MASK	50D1 80E0h
180E4h	32	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS	50D1 80E4h
180E8h	32	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW	50D1 80E8h

Table 2-118. CFG0, CFG0 Registers, Base Address=0X0000000050D00000, Length=131072 (continued)

Offset	Length	Register Name	mss_ctrl_mmr Physical Address
180F0h	32	R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK	50D1 80F0h
180F4h	32	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS	50D1 80F4h
180F8h	32	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW	50D1 80F8h
18100h	32	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_MASK	50D1 8100h
18104h	32	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS	50D1 8104h
18108h	32	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW	50D1 8108h
18110h	32	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_MASK	50D1 8110h
18114h	32	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS	50D1 8114h
18118h	32	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW	50D1 8118h
18120h	32	R5SS0_TCM_ADDRPARITY_CLR	50D1 8120h
18124h	32	R5SS0_CORE0_ADDRPARITY_ERR_ATCM	50D1 8124h
18128h	32	R5SS0_CORE1_ADDRPARITY_ERR_ATCM	50D1 8128h
1812Ch	32	R5SS0_CORE0_ERR_ADDRPARITY_B0TCM	50D1 812Ch
18130h	32	R5SS0_CORE1_ERR_ADDRPARITY_B0TCM	50D1 8130h
18134h	32	R5SS0_CORE0_ERR_ADDRPARITY_B1TCM	50D1 8134h
18138h	32	R5SS0_CORE1_ERR_ADDRPARITY_B1TCM	50D1 8138h
1813Ch	32	R5SS0_TCM_ADDRPARITY_ERRFORCE	50D1 813Ch
18140h	32	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_MASK	50D1 8140h
18144h	32	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS	50D1 8144h
18148h	32	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW	50D1 8148h
18150h	32	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_MASK	50D1 8150h
18154h	32	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS	50D1 8154h
18158h	32	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW	50D1 8158h
18160h	32	R5SS1_TCM_ADDRPARITY_CLR	50D1 8160h
18164h	32	R5SS1_CORE0_ADDRPARITY_ERR_ATCM	50D1 8164h
18168h	32	R5SS1_CORE1_ADDRPARITY_ERR_ATCM	50D1 8168h
1816Ch	32	R5SS1_CORE0_ERR_ADDRPARITY_B0TCM	50D1 816Ch
18170h	32	R5SS1_CORE1_ERR_ADDRPARITY_B0TCM	50D1 8170h
18174h	32	R5SS1_CORE0_ERR_ADDRPARITY_B1TCM	50D1 8174h
18178h	32	R5SS1_CORE1_ERR_ADDRPARITY_B1TCM	50D1 8178h
1817Ch	32	R5SS1_TCM_ADDRPARITY_ERRFORCE	50D1 817Ch
18180h	32	TPCC0_PARITY_CTRL	50D1 8180h
18184h	32	TPCC0_PARITY_STATUS	50D1 8184h
18200h	32	BUS_SAFETY_CTRL	50D1 8200h
18220h	32	R5SS0_CORE0_AXI_RD_BUS_SAFETY_CTRL	50D1 8220h
18224h	32	R5SS0_CORE0_AXI_RD_BUS_SAFETY_FI	50D1 8224h
18228h	32	R5SS0_CORE0_AXI_RD_BUS_SAFETY_ERR	50D1 8228h
1822Ch	32	R5SS0_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0	50D1 822Ch
18230h	32	R5SS0_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_CMD	50D1 8230h
18234h	32	R5SS0_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_READ	50D1 8234h
18240h	32	R5SS0_CORE1_AXI_RD_BUS_SAFETY_CTRL	50D1 8240h
18244h	32	R5SS0_CORE1_AXI_RD_BUS_SAFETY_FI	50D1 8244h

Table 2-118. CFG0, CFG0 Registers, Base Address=0X0000000050D00000, Length=131072 (continued)

Offset	Length	Register Name	mss_ctrl_mmr Physical Address
18248h	32	R5SS0_CORE1_AXI_RD_BUS_SAFETY_ERR	50D1 8248h
1824Ch	32	R5SS0_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0	50D1 824Ch
18250h	32	R5SS0_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_CMD	50D1 8250h
18254h	32	R5SS0_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_READ	50D1 8254h
18260h	32	R5SS1_CORE0_AXI_RD_BUS_SAFETY_CTRL	50D1 8260h
18264h	32	R5SS1_CORE0_AXI_RD_BUS_SAFETY_FI	50D1 8264h
18268h	32	R5SS1_CORE0_AXI_RD_BUS_SAFETY_ERR	50D1 8268h
1826Ch	32	R5SS1_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0	50D1 826Ch
18270h	32	R5SS1_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_CMD	50D1 8270h
18274h	32	R5SS1_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_READ	50D1 8274h
18280h	32	R5SS1_CORE1_AXI_RD_BUS_SAFETY_CTRL	50D1 8280h
18284h	32	R5SS1_CORE1_AXI_RD_BUS_SAFETY_FI	50D1 8284h
18288h	32	R5SS1_CORE1_AXI_RD_BUS_SAFETY_ERR	50D1 8288h
1828Ch	32	R5SS1_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0	50D1 828Ch
18290h	32	R5SS1_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_CMD	50D1 8290h
18294h	32	R5SS1_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_READ	50D1 8294h
182A0h	32	R5SS0_CORE0_AXI_WR_BUS_SAFETY_CTRL	50D1 82A0h
182A4h	32	R5SS0_CORE0_AXI_WR_BUS_SAFETY_FI	50D1 82A4h
182A8h	32	R5SS0_CORE0_AXI_WR_BUS_SAFETY_ERR	50D1 82A8h
182ACh	32	R5SS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0	50D1 82ACh
182B0h	32	R5SS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_CMD	50D1 82B0h
182B4h	32	R5SS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE	50D1 82B4h
182B8h	32	R5SS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP	50D1 82B8h
182C0h	32	R5SS0_CORE1_AXI_WR_BUS_SAFETY_CTRL	50D1 82C0h
182C4h	32	R5SS0_CORE1_AXI_WR_BUS_SAFETY_FI	50D1 82C4h
182C8h	32	R5SS0_CORE1_AXI_WR_BUS_SAFETY_ERR	50D1 82C8h
182CCh	32	R5SS0_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0	50D1 82CCh
182D0h	32	R5SS0_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_CMD	50D1 82D0h
182D4h	32	R5SS0_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE	50D1 82D4h
182D8h	32	R5SS0_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP	50D1 82D8h
182E0h	32	R5SS1_CORE0_AXI_WR_BUS_SAFETY_CTRL	50D1 82E0h
182E4h	32	R5SS1_CORE0_AXI_WR_BUS_SAFETY_FI	50D1 82E4h
182E8h	32	R5SS1_CORE0_AXI_WR_BUS_SAFETY_ERR	50D1 82E8h
182ECh	32	R5SS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0	50D1 82ECh

Table 2-118. CFG0, CFG0 Registers, Base Address=0X0000000050D00000, Length=131072 (continued)

Offset	Length	Register Name	mss_ctrl_mmr Physical Address
182F0h	32	R5SS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_CMD	50D1 82F0h
182F4h	32	R5SS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE	50D1 82F4h
182F8h	32	R5SS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP	50D1 82F8h
18300h	32	R5SS1_CORE1_AXI_WR_BUS_SAFETY_CTRL	50D1 8300h
18304h	32	R5SS1_CORE1_AXI_WR_BUS_SAFETY_FI	50D1 8304h
18308h	32	R5SS1_CORE1_AXI_WR_BUS_SAFETY_ERR	50D1 8308h
1830Ch	32	R5SS1_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0	50D1 830Ch
18310h	32	R5SS1_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_CMD	50D1 8310h
18314h	32	R5SS1_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE	50D1 8314h
18318h	32	R5SS1_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP	50D1 8318h
18320h	32	R5SS0_CORE0_AXI_S_BUS_SAFETY_CTRL	50D1 8320h
18324h	32	R5SS0_CORE0_AXI_S_BUS_SAFETY_FI	50D1 8324h
18328h	32	R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR	50D1 8328h
1832Ch	32	R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_DATA0	50D1 832Ch
18330h	32	R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_CMD	50D1 8330h
18334h	32	R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITE	50D1 8334h
18338h	32	R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_READ	50D1 8338h
1833Ch	32	R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP	50D1 833Ch
18340h	32	R5SS0_CORE1_AXI_S_BUS_SAFETY_CTRL	50D1 8340h
18344h	32	R5SS0_CORE1_AXI_S_BUS_SAFETY_FI	50D1 8344h
18348h	32	R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR	50D1 8348h
1834Ch	32	R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_DATA0	50D1 834Ch
18350h	32	R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_CMD	50D1 8350h
18354h	32	R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_WRITE	50D1 8354h
18358h	32	R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_READ	50D1 8358h
1835Ch	32	R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP	50D1 835Ch
18360h	32	R5SS1_CORE0_AXI_S_BUS_SAFETY_CTRL	50D1 8360h
18364h	32	R5SS1_CORE0_AXI_S_BUS_SAFETY_FI	50D1 8364h
18368h	32	R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR	50D1 8368h
1836Ch	32	R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_DATA0	50D1 836Ch
18370h	32	R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_CMD	50D1 8370h
18374h	32	R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITE	50D1 8374h
18378h	32	R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_READ	50D1 8378h
1837Ch	32	R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP	50D1 837Ch
18380h	32	R5SS1_CORE1_AXI_S_BUS_SAFETY_CTRL	50D1 8380h
18384h	32	R5SS1_CORE1_AXI_S_BUS_SAFETY_FI	50D1 8384h

Table 2-118. CFG0, CFG0 Registers, Base Address=0X0000000050D00000, Length=131072 (continued)

Offset	Length	Register Name	mss_ctrl_mmr Physical Address
18388h	32	R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR	50D1 8388h
1838Ch	32	R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_DATA0	50D1 838Ch
18390h	32	R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_CMD	50D1 8390h
18394h	32	R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_WRITE	50D1 8394h
18398h	32	R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_READ	50D1 8398h
1839Ch	32	R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP	50D1 839Ch
183A0h	32	TPTC00_RD_BUS_SAFETY_CTRL	50D1 83A0h
183A4h	32	TPTC00_RD_BUS_SAFETY_FI	50D1 83A4h
183A8h	32	TPTC00_RD_BUS_SAFETY_ERR	50D1 83A8h
183ACh	32	TPTC00_RD_BUS_SAFETY_ERR_STAT_DATA0	50D1 83ACh
183B0h	32	TPTC00_RD_BUS_SAFETY_ERR_STAT_CMD	50D1 83B0h
183B4h	32	TPTC00_RD_BUS_SAFETY_ERR_STAT_READ	50D1 83B4h
183C0h	32	TPTC01_RD_BUS_SAFETY_CTRL	50D1 83C0h
183C4h	32	TPTC01_RD_BUS_SAFETY_FI	50D1 83C4h
183C8h	32	TPTC01_RD_BUS_SAFETY_ERR	50D1 83C8h
183CCh	32	TPTC01_RD_BUS_SAFETY_ERR_STAT_DATA0	50D1 83CCh
183D0h	32	TPTC01_RD_BUS_SAFETY_ERR_STAT_CMD	50D1 83D0h
183D4h	32	TPTC01_RD_BUS_SAFETY_ERR_STAT_READ	50D1 83D4h
183E0h	32	TPTC00_WR_BUS_SAFETY_CTRL	50D1 83E0h
183E4h	32	TPTC00_WR_BUS_SAFETY_FI	50D1 83E4h
183E8h	32	TPTC00_WR_BUS_SAFETY_ERR	50D1 83E8h
183ECh	32	TPTC00_WR_BUS_SAFETY_ERR_STAT_DATA0	50D1 83ECh
183F0h	32	TPTC00_WR_BUS_SAFETY_ERR_STAT_CMD	50D1 83F0h
183F4h	32	TPTC00_WR_BUS_SAFETY_ERR_STAT_WRITE	50D1 83F4h
183F8h	32	TPTC00_WR_BUS_SAFETY_ERR_STAT_WRITERESP	50D1 83F8h
18400h	32	TPTC01_WR_BUS_SAFETY_CTRL	50D1 8400h
18404h	32	TPTC01_WR_BUS_SAFETY_FI	50D1 8404h
18408h	32	TPTC01_WR_BUS_SAFETY_ERR	50D1 8408h
1840Ch	32	TPTC01_WR_BUS_SAFETY_ERR_STAT_DATA0	50D1 840Ch
18410h	32	TPTC01_WR_BUS_SAFETY_ERR_STAT_CMD	50D1 8410h
18414h	32	TPTC01_WR_BUS_SAFETY_ERR_STAT_WRITE	50D1 8414h
18418h	32	TPTC01_WR_BUS_SAFETY_ERR_STAT_WRITERESP	50D1 8418h
18420h	32	HSM_TPTC0_RD_BUS_SAFETY_CTRL	50D1 8420h
18424h	32	HSM_TPTC0_RD_BUS_SAFETY_FI	50D1 8424h
18428h	32	HSM_TPTC0_RD_BUS_SAFETY_ERR	50D1 8428h
1842Ch	32	HSM_TPTC0_RD_BUS_SAFETY_ERR_STAT_DATA0	50D1 842Ch
18430h	32	HSM_TPTC0_RD_BUS_SAFETY_ERR_STAT_CMD	50D1 8430h
18434h	32	HSM_TPTC0_RD_BUS_SAFETY_ERR_STAT_READ	50D1 8434h
18440h	32	HSM_TPTC1_RD_BUS_SAFETY_CTRL	50D1 8440h
18444h	32	HSM_TPTC1_RD_BUS_SAFETY_FI	50D1 8444h
18448h	32	HSM_TPTC1_RD_BUS_SAFETY_ERR	50D1 8448h
1844Ch	32	HSM_TPTC1_RD_BUS_SAFETY_ERR_STAT_DATA0	50D1 844Ch
18450h	32	HSM_TPTC1_RD_BUS_SAFETY_ERR_STAT_CMD	50D1 8450h
18454h	32	HSM_TPTC1_RD_BUS_SAFETY_ERR_STAT_READ	50D1 8454h
18460h	32	HSM_TPTC0_WR_BUS_SAFETY_CTRL	50D1 8460h

Table 2-118. CFG0, CFG0 Registers, Base Address=0X0000000050D00000, Length=131072 (continued)

Offset	Length	Register Name	mss_ctrl_mmr Physical Address
18464h	32	HSM_TPTC0_WR_BUS_SAFETY_FI	50D1 8464h
18468h	32	HSM_TPTC0_WR_BUS_SAFETY_ERR	50D1 8468h
1846Ch	32	HSM_TPTC0_WR_BUS_SAFETY_ERR_STAT_DATA0	50D1 846Ch
18470h	32	HSM_TPTC0_WR_BUS_SAFETY_ERR_STAT_CMD	50D1 8470h
18474h	32	HSM_TPTC0_WR_BUS_SAFETY_ERR_STAT_WRITE	50D1 8474h
18478h	32	HSM_TPTC0_WR_BUS_SAFETY_ERR_STAT_WRITERESP	50D1 8478h
18480h	32	HSM_TPTC1_WR_BUS_SAFETY_CTRL	50D1 8480h
18484h	32	HSM_TPTC1_WR_BUS_SAFETY_FI	50D1 8484h
18488h	32	HSM_TPTC1_WR_BUS_SAFETY_ERR	50D1 8488h
1848Ch	32	HSM_TPTC1_WR_BUS_SAFETY_ERR_STAT_DATA0	50D1 848Ch
18490h	32	HSM_TPTC1_WR_BUS_SAFETY_ERR_STAT_CMD	50D1 8490h
18494h	32	HSM_TPTC1_WR_BUS_SAFETY_ERR_STAT_WRITE	50D1 8494h
18498h	32	HSM_TPTC1_WR_BUS_SAFETY_ERR_STAT_WRITERESP	50D1 8498h
184A0h	32	QSPI0_BUS_SAFETY_CTRL	50D1 84A0h
184A4h	32	QSPI0_BUS_SAFETY_FI	50D1 84A4h
184A8h	32	QSPI0_BUS_SAFETY_ERR	50D1 84A8h
184ACh	32	QSPI0_BUS_SAFETY_ERR_STAT_DATA0	50D1 84ACh
184B0h	32	QSPI0_BUS_SAFETY_ERR_STAT_CMD	50D1 84B0h
184B4h	32	QSPI0_BUS_SAFETY_ERR_STAT_WRITE	50D1 84B4h
184B8h	32	QSPI0_BUS_SAFETY_ERR_STAT_READ	50D1 84B8h
184BCh	32	QSPI0_BUS_SAFETY_ERR_STAT_WRITERESP	50D1 84BCh
18540h	32	MCRC0_BUS_SAFETY_CTRL	50D1 8540h
18544h	32	MCRC0_BUS_SAFETY_FI	50D1 8544h
18548h	32	MCRC0_BUS_SAFETY_ERR	50D1 8548h
1854Ch	32	MCRC0_BUS_SAFETY_ERR_STAT_DATA0	50D1 854Ch
18550h	32	MCRC0_BUS_SAFETY_ERR_STAT_CMD	50D1 8550h
18554h	32	MCRC0_BUS_SAFETY_ERR_STAT_WRITE	50D1 8554h
18558h	32	MCRC0_BUS_SAFETY_ERR_STAT_READ	50D1 8558h
1855Ch	32	MCRC0_BUS_SAFETY_ERR_STAT_WRITERESP	50D1 855Ch
185E0h	32	PRU-ICSSSLAVE_BUS_SAFETY_CTRL	50D1 85E0h
185E4h	32	PRU-ICSSSLAVE_BUS_SAFETY_FI	50D1 85E4h
185E8h	32	PRU-ICSSSLAVE_BUS_SAFETY_ERR	50D1 85E8h
185ECh	32	PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_DATA0	50D1 85ECh
185F0h	32	PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_CMD	50D1 85F0h
185F4h	32	PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_WRITE	50D1 85F4h
185F8h	32	PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_READ	50D1 85F8h
185FCh	32	PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_WRITERESP	50D1 85FCh
18620h	32	L2OCRAM_BANK0_BUS_SAFETY_CTRL	50D1 8620h
18624h	32	L2OCRAM_BANK0_BUS_SAFETY_FI	50D1 8624h
18628h	32	L2OCRAM_BANK0_BUS_SAFETY_ERR	50D1 8628h
1862Ch	32	L2OCRAM_BANK0_BUS_SAFETY_ERR_STAT_DATA0	50D1 862Ch
18630h	32	L2OCRAM_BANK0_BUS_SAFETY_ERR_STAT_CMD	50D1 8630h
18634h	32	L2OCRAM_BANK0_BUS_SAFETY_ERR_STAT_WRITE	50D1 8634h
18638h	32	L2OCRAM_BANK0_BUS_SAFETY_ERR_STAT_READ	50D1 8638h

Table 2-118. CFG0, CFG0 Registers, Base Address=0X0000000050D00000, Length=131072 (continued)

Offset	Length	Register Name	mss_ctrl_mmr Physical Address
1863Ch	32	L2OCRAM_BANK0_BUS_SAFETY_ERR_STAT_WRITERESP	50D1 863Ch
18640h	32	L2OCRAM_BANK1_BUS_SAFETY_CTRL	50D1 8640h
18644h	32	L2OCRAM_BANK1_BUS_SAFETY_FI	50D1 8644h
18648h	32	L2OCRAM_BANK1_BUS_SAFETY_ERR	50D1 8648h
1864Ch	32	L2OCRAM_BANK1_BUS_SAFETY_ERR_STAT_DATA0	50D1 864Ch
18650h	32	L2OCRAM_BANK1_BUS_SAFETY_ERR_STAT_CMD	50D1 8650h
18654h	32	L2OCRAM_BANK1_BUS_SAFETY_ERR_STAT_WRITE	50D1 8654h
18658h	32	L2OCRAM_BANK1_BUS_SAFETY_ERR_STAT_READ	50D1 8658h
1865Ch	32	L2OCRAM_BANK1_BUS_SAFETY_ERR_STAT_WRITERESP	50D1 865Ch
18660h	32	L2OCRAM_BANK2_BUS_SAFETY_CTRL	50D1 8660h
18664h	32	L2OCRAM_BANK2_BUS_SAFETY_FI	50D1 8664h
18668h	32	L2OCRAM_BANK2_BUS_SAFETY_ERR	50D1 8668h
1866Ch	32	L2OCRAM_BANK2_BUS_SAFETY_ERR_STAT_DATA0	50D1 866Ch
18670h	32	L2OCRAM_BANK2_BUS_SAFETY_ERR_STAT_CMD	50D1 8670h
18674h	32	L2OCRAM_BANK2_BUS_SAFETY_ERR_STAT_WRITE	50D1 8674h
18678h	32	L2OCRAM_BANK2_BUS_SAFETY_ERR_STAT_READ	50D1 8678h
1867Ch	32	L2OCRAM_BANK2_BUS_SAFETY_ERR_STAT_WRITERESP	50D1 867Ch
18680h	32	L2OCRAM_BANK3_BUS_SAFETY_CTRL	50D1 8680h
18684h	32	L2OCRAM_BANK3_BUS_SAFETY_FI	50D1 8684h
18688h	32	L2OCRAM_BANK3_BUS_SAFETY_ERR	50D1 8688h
1868Ch	32	L2OCRAM_BANK3_BUS_SAFETY_ERR_STAT_DATA0	50D1 868Ch
18690h	32	L2OCRAM_BANK3_BUS_SAFETY_ERR_STAT_CMD	50D1 8690h
18694h	32	L2OCRAM_BANK3_BUS_SAFETY_ERR_STAT_WRITE	50D1 8694h
18698h	32	L2OCRAM_BANK3_BUS_SAFETY_ERR_STAT_READ	50D1 8698h
1869Ch	32	L2OCRAM_BANK3_BUS_SAFETY_ERR_STAT_WRITERESP	50D1 869Ch
186A0h	32	MBOX_SRAM_BUS_SAFETY_CTRL	50D1 86A0h
186A4h	32	MBOX_SRAM_BUS_SAFETY_FI	50D1 86A4h
186A8h	32	MBOX_SRAM_BUS_SAFETY_ERR	50D1 86A8h
186ACh	32	MBOX_SRAM_BUS_SAFETY_ERR_STAT_DATA0	50D1 86ACh
186B0h	32	MBOX_SRAM_BUS_SAFETY_ERR_STAT_CMD	50D1 86B0h
186B4h	32	MBOX_SRAM_BUS_SAFETY_ERR_STAT_WRITE	50D1 86B4h
186B8h	32	MBOX_SRAM_BUS_SAFETY_ERR_STAT_READ	50D1 86B8h
186BCh	32	MBOX_SRAM_BUS_SAFETY_ERR_STAT_WRITERESP	50D1 86BCh
186C0h	32	STM_STIM_BUS_SAFETY_CTRL	50D1 86C0h
186C4h	32	STM_STIM_BUS_SAFETY_FI	50D1 86C4h
186C8h	32	STM_STIM_BUS_SAFETY_ERR	50D1 86C8h
186CCh	32	STM_STIM_BUS_SAFETY_ERR_STAT_DATA0	50D1 86CCh
186D0h	32	STM_STIM_BUS_SAFETY_ERR_STAT_CMD	50D1 86D0h
186D4h	32	STM_STIM_BUS_SAFETY_ERR_STAT_WRITE	50D1 86D4h
186D8h	32	STM_STIM_BUS_SAFETY_ERR_STAT_READ	50D1 86D8h
186DCh	32	STM_STIM_BUS_SAFETY_ERR_STAT_WRITERESP	50D1 86DCh
186E0h	32	MMC0_BUS_SAFETY_CTRL	50D1 86E0h
186E4h	32	MMC0_BUS_SAFETY_FI	50D1 86E4h
186E8h	32	MMC0_BUS_SAFETY_ERR	50D1 86E8h

Table 2-118. CFG0, CFG0 Registers, Base Address=0X0000000050D00000, Length=131072 (continued)

Offset	Length	Register Name	mss_ctrl_mmr Physical Address
186ECh	32	MMC0_BUS_SAFETY_ERR_STAT_DATA0	50D1 86ECh
186F0h	32	MMC0_BUS_SAFETY_ERR_STAT_CMD	50D1 86F0h
186F4h	32	MMC0_BUS_SAFETY_ERR_STAT_WRITE	50D1 86F4h
186F8h	32	MMC0_BUS_SAFETY_ERR_STAT_READ	50D1 86F8h
186FCh	32	MMC0_BUS_SAFETY_ERR_STAT_WRITERESP	50D1 86FCh
18700h	32	GPMC0_BUS_SAFETY_CTRL	50D1 8700h
18704h	32	GPMC0_BUS_SAFETY_FI	50D1 8704h
18708h	32	GPMC0_BUS_SAFETY_ERR	50D1 8708h
1870Ch	32	GPMC0_BUS_SAFETY_ERR_STAT_DATA0	50D1 870Ch
18710h	32	GPMC0_BUS_SAFETY_ERR_STAT_CMD	50D1 8710h
18714h	32	GPMC0_BUS_SAFETY_ERR_STAT_WRITE	50D1 8714h
18718h	32	GPMC0_BUS_SAFETY_ERR_STAT_READ	50D1 8718h
1871Ch	32	GPMC0_BUS_SAFETY_ERR_STAT_WRITERESP	50D1 871Ch
18740h	32	R5SS0_CORE0_AHB_BUS_SAFETY_CTRL	50D1 8740h
18744h	32	R5SS0_CORE0_AHB_BUS_SAFETY_FI	50D1 8744h
18748h	32	R5SS0_CORE0_AHB_BUS_SAFETY_ERR	50D1 8748h
1874Ch	32	R5SS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_DATA0	50D1 874Ch
18750h	32	R5SS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_CMD	50D1 8750h
18754h	32	R5SS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITE	50D1 8754h
18758h	32	R5SS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_READ	50D1 8758h
1875Ch	32	R5SS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITE RESP	50D1 875Ch
18760h	32	R5SS0_CORE1_AHB_BUS_SAFETY_CTRL	50D1 8760h
18764h	32	R5SS0_CORE1_AHB_BUS_SAFETY_FI	50D1 8764h
18768h	32	R5SS0_CORE1_AHB_BUS_SAFETY_ERR	50D1 8768h
1876Ch	32	R5SS0_CORE1_AHB_BUS_SAFETY_ERR_STAT_DATA0	50D1 876Ch
18770h	32	R5SS0_CORE1_AHB_BUS_SAFETY_ERR_STAT_CMD	50D1 8770h
18774h	32	R5SS0_CORE1_AHB_BUS_SAFETY_ERR_STAT_WRITE	50D1 8774h
18778h	32	R5SS0_CORE1_AHB_BUS_SAFETY_ERR_STAT_READ	50D1 8778h
1877Ch	32	R5SS0_CORE1_AHB_BUS_SAFETY_ERR_STAT_WRITE RESP	50D1 877Ch
18780h	32	R5SS1_CORE0_AHB_BUS_SAFETY_CTRL	50D1 8780h
18784h	32	R5SS1_CORE0_AHB_BUS_SAFETY_FI	50D1 8784h
18788h	32	R5SS1_CORE0_AHB_BUS_SAFETY_ERR	50D1 8788h
1878Ch	32	R5SS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_DATA0	50D1 878Ch
18790h	32	R5SS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_CMD	50D1 8790h
18794h	32	R5SS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITE	50D1 8794h
18798h	32	R5SS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_READ	50D1 8798h
1879Ch	32	R5SS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITE RESP	50D1 879Ch
187A0h	32	R5SS1_CORE1_AHB_BUS_SAFETY_CTRL	50D1 87A0h
187A4h	32	R5SS1_CORE1_AHB_BUS_SAFETY_FI	50D1 87A4h
187A8h	32	R5SS1_CORE1_AHB_BUS_SAFETY_ERR	50D1 87A8h
187ACh	32	R5SS1_CORE1_AHB_BUS_SAFETY_ERR_STAT_DATA0	50D1 87ACh
187B0h	32	R5SS1_CORE1_AHB_BUS_SAFETY_ERR_STAT_CMD	50D1 87B0h
187B4h	32	R5SS1_CORE1_AHB_BUS_SAFETY_ERR_STAT_WRITE	50D1 87B4h
187B8h	32	R5SS1_CORE1_AHB_BUS_SAFETY_ERR_STAT_READ	50D1 87B8h

Table 2-118. CFG0, CFG0 Registers, Base Address=0X0000000050D00000, Length=131072 (continued)

Offset	Length	Register Name	mss_ctrl_mmr Physical Address
187BCh	32	R5SS1_CORE1_AHB_BUS_SAFETY_ERR_STAT_WRITE RESP	50D1 87BCh
18834h	32	MSS_VBUSM_SAFETY_H_ERRAGG_MASK0	50D1 8834h
18838h	32	MSS_VBUSM_SAFETY_H_ERRAGG_STATUS0	50D1 8838h
1883Ch	32	MSS_VBUSM_SAFETY_H_ERRAGG_STATUS_RAW0	50D1 883Ch
18844h	32	MSS_VBUSM_SAFETY_H_ERRAGG_MASK1	50D1 8844h
18848h	32	MSS_VBUSM_SAFETY_H_ERRAGG_STATUS1	50D1 8848h
1884Ch	32	MSS_VBUSM_SAFETY_H_ERRAGG_STATUS_RAW1	50D1 884Ch
18854h	32	MSS_VBUSM_SAFETY_L_ERRAGG_MASK0	50D1 8854h
18858h	32	MSS_VBUSM_SAFETY_L_ERRAGG_STATUS0	50D1 8858h
1885Ch	32	MSS_VBUSM_SAFETY_L_ERRAGG_STATUS_RAW0	50D1 885Ch
18864h	32	MSS_VBUSM_SAFETY_L_ERRAGG_MASK1	50D1 8864h
18868h	32	MSS_VBUSM_SAFETY_L_ERRAGG_STATUS1	50D1 8868h
1886Ch	32	MSS_VBUSM_SAFETY_L_ERRAGG_STATUS_RAW1	50D1 886Ch

2.3.1 CFG0_R5SS0_CONTROL Registers

2.3.1.1 CFG0_CONTROL Register (Offset = 20h) [reset = 707h]

Short Description:

Long Description:

Return to Summary Table

Table 2-119. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0020h

Figure 2-58. R5SS0_CONTROL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					R5SS0_CONTROL_ROM_WAIT_STATE			RESERVED					R5SS0_CONTROL_RESET_FSM_TRIGGER		
NONE					R/W			NONE					R/W		
b					0h			b					0h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					R5SS0_CONTROL_LOCK_STEP_SWITCH_WAIT			RESERVED					R5SS0_CONTROL_LOCK_STEP		
NONE					R/W			NONE					R/W		
0					7h			0					7h		

Access Types Legend

Table 2-120. R5SS0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE		Reserved
26:24	R5SS0_CONTROL_ROM_WAIT_STATE	R/W	0h	writing '111' enables a single cycle wait state with respect to CR5A_clk for rom access. This needs to be set when R5 clock is at 400MHZ and Interconnect-clk is at 200MHZ. (because it is a timing issue in this scenario) Reset Source: mod_g_rst_n
23:19	RESERVED	NONE		Reserved
18:16	R5SS0_CONTROL_RESET_FSM_TRIGGER	R/W	0h	Write pulse bit field: writing 3'b111 will trigger the reset FSM. Reset FSM ensures reset to R5SS and inturn ensures the latching of lock_step and also mem_swap bit Reset Source: mod_g_rst_n
15:11	RESERVED	NONE		Reserved
10:8	R5SS0_CONTROL_LOCK_STEP_SWITCH_WAIT	R/W	7h	writing 3'b111 ensures switch happens only after R5SS reset. Orelse it will be a immediate switch. Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	R5SS0_CONTROL_LOCK_STEP	R/W	7h	writing 3'b000 ensures R5 to be in Dual-Core mode. Note: The change happens after the R5SS reset assertion if R5_CONTROL_lock_step_switch_wait is set. Or else the switiching to Dual-core happens on the fly. Reset Source: mod_g_rst_n

2.3.2 CFG0_R5SS0_CORE0_HALT Registers

2.3.2.1 CFG0_CORE0_HALT Register (Offset = 24h) [reset = 7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-121. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0024h

Figure 2-59. R5SS0_CORE0_HALT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
b															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													R5SS0_COREA_HALT_HALT		
NONE													R/W		
b													7h		

Access Types Legend

Table 2-122. R5SS0_CORE0_HALT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	R5SS0_COREA_HALT_HALT	R/W	7h	writing '000' will unhalt CR5A. This register should be written only once. Reset Source: mod_g_rst_n

2.3.3 CFG0_R5SS0_CORE1_HALT Registers

2.3.3.1 CFG0_CORE1_HALT Register (Offset = 28h) [reset = 7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-123. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0028h

Figure 2-60. R5SS0_CORE1_HALT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
b															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													R5SS0_COREB_HALT_HALT		
NONE													R/W		
b													7h		

Access Types Legend

Table 2-124. R5SS0_CORE1_HALT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	R5SS0_COREB_HALT_HALT	R/W	7h	writing '000' will unhalt for CR5B. This register should be written only once. Reset Source: mod_g_rst_n

2.3.4 CFG0_R5SS0_STATUS_REG Registers

2.3.4.1 CFG0_STATUS_REG Register (Offset = 2Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-125. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 002Ch

Figure 2-61. R5SS0_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							R5SS0_STATUS_REG_LOCK_STEP	RESERVED							R5SS0_STATUS_REG_MEMSWAP
NONE							R	NONE							R
0							0h	0							0h

Access Types Legend

Table 2-126. R5SS0_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE		Reserved
8	R5SS0_STATUS_REG_LOCK_STEP	R	0h	Reading 1: confirms R5SS is in lockstep mode. Reading 0: confirms R5SS is in Dual-core mode. Reset Source: mod_g_rst_n
7:1	RESERVED	NONE		Reserved
0	R5SS0_STATUS_REG_MEMSWAP	R	0h	reading 1: confirms ROM is Eclipsed from with RAM for R5. Reset Source: mod_g_rst_n

2.3.5 CFG0_R5SS0_CORE0_STAT Registers

2.3.5.1 CFG0_CORE0_STAT Register (Offset = 30h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-127. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0030h

Figure 2-62. R5SS0_CORE0_STAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											R5SS0_CORE0_STAT_WFE_STAT	RESERVED			R5SS0_CORE0_STAT_WFI_STAT
NONE											R	NONE			R
0											0h	0			0h

Access Types Legend

Table 2-128. R5SS0_CORE0_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4	R5SS0_CORE0_STAT_WFE_STAT	R	0h	WFE Status Reset Source: mod_g_rst_n
3:1	RESERVED	NONE		Reserved
0	R5SS0_CORE0_STAT_WFI_STAT	R	0h	WFI Status Reset Source: mod_g_rst_n

2.3.6 CFG0_R5SS0_CORE1_STAT Registers

2.3.6.1 CFG0_CORE1_STAT Register (Offset = 34h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-129. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0034h

Figure 2-63. R5SS0_CORE1_STAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											R5SS0_CORE1_STAT_WFE_STAT	RESERVED			R5SS0_CORE1_STAT_WFI_STAT
NONE											R	NONE			R
0											0h	0			0h

Access Types Legend

Table 2-130. R5SS0_CORE1_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4	R5SS0_CORE1_STAT_WFE_STAT	R	0h	WFE Status Reset Source: mod_g_rst_n
3:1	RESERVED	NONE		Reserved
0	R5SS0_CORE1_STAT_WFI_STAT	R	0h	WFI Status Reset Source: mod_g_rst_n

2.3.7 CFG0_R5SS0_FORCE_WFI Registers

2.3.7.1 CFG0_FORCE_WFI Register (Offset = 38h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-131. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0038h

Figure 2-64. R5SS0_FORCE_WFI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_STC_CONTROL0_CR5_WFI_OVERIDE		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-132. R5SS0_FORCE_WFI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_STC_CONTROL0_CR5_WFI_OVERIDE	R/W	0h	writing 3'b111 will force the wfi signals of R5SS to 1 Reset Source: mod_g_rst_n

2.3.8 CFG0_R5SS1_CONTROL Registers

2.3.8.1 CFG0_CONTROL Register (Offset = 40h) [reset = 707h]

Short Description:

Long Description:

Return to Summary Table

Table 2-133. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0040h

Figure 2-65. R5SS1_CONTROL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED													R5SS1_CONTROL_RESET_FSM_TRIGGER		
NONE													R/W		
4229418b													0h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					R5SS1_CONTROL_LOCK_STEP_SWITCH_WAIT			RESERVED					R5SS1_CONTROL_LOCK_STEP		
NONE					R/W			NONE					R/W		
0					7h			0					7h		

Access Types Legend

Table 2-134. R5SS1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE		Reserved
18:16	R5SS1_CONTROL_RESET_FSM_TRIGGER	R/W	0h	Write pulse bit field: writing 3'b111 will trigger the reset FSM. Reset FSM ensures reset to R5SS and inturn ensures the latching of lock_step and also mem_swap bit Reset Source: mod_g_rst_n
15:11	RESERVED	NONE		Reserved
10:8	R5SS1_CONTROL_LOCK_STEP_SWITCH_WAIT	R/W	7h	writing 3'b111 ensures switch happens only after R5SS reset. Orelse it will be a immediate switch. Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	R5SS1_CONTROL_LOCK_STEP	R/W	7h	writing 3'b000 ensures R5 to be in Dual-Core mode. Note: The change happens after the R5SS reset assertion if R5_CONTROL_lock_step_switch_wait is set. Or else the switiching to Dual-core happens on the fly. Reset Source: mod_g_rst_n

2.3.9 CFG0_R5SS1_CORE0_HALT Registers

2.3.9.1 CFG0_CORE0_HALT Register (Offset = 44h) [reset = 7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-135. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0044h

Figure 2-66. R5SS1_CORE0_HALT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
b															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													R5SS1_COREA_HALT_HALT		
NONE													R/W		
b													7h		

Access Types Legend

Table 2-136. R5SS1_CORE0_HALT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	R5SS1_COREA_HALT_HALT	R/W	7h	writing '000' will unhalt CR5A. This register should be written only once. Reset Source: mod_g_rst_n

2.3.10 CFG0_R5SS1_CORE1_HALT Registers

2.3.10.1 CFG0_CORE1_HALT Register (Offset = 48h) [reset = 7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-137. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0048h

Figure 2-67. R5SS1_CORE1_HALT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
b															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													R5SS1_COREB_HALT_HALT		
NONE													R/W		
b													7h		

Access Types Legend

Table 2-138. R5SS1_CORE1_HALT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	R5SS1_COREB_HALT_HALT	R/W	7h	writing '000' will unhalt for CR5B. This register should be written only once. Reset Source: mod_g_rst_n

2.3.11 CFG0_R5SS1_STATUS_REG Registers

2.3.11.1 CFG0_STATUS_REG Register (Offset = 4Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-139. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 004Ch

Figure 2-68. R5SS1_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							R5SS1_STATUS_REG_LOCK_STEP	RESERVED							
NONE							R	NONE							
0							0h	0							

Access Types Legend

Table 2-140. R5SS1_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE		Reserved
8	R5SS1_STATUS_REG_LOCK_STEP	R	0h	Reading 1: confirms R5SS is in lockstep mode. Reading 0: confirms R5SS is in Dual-core mode. Reset Source: mod_g_rst_n
7:0	RESERVED	NONE		Reserved

2.3.12 CFG0_R5SS1_CORE0_STAT Registers

2.3.12.1 CFG0_CORE0_STAT Register (Offset = 50h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-141. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0050h

Figure 2-69. R5SS1_CORE0_STAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											R5SS1_CORE0_STAT_WFE_STAT	RESERVED			R5SS1_CORE0_STAT_WFI_STAT
NONE											R	NONE			R
0											0h	0			0h

Access Types Legend

Table 2-142. R5SS1_CORE0_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4	R5SS1_CORE0_STAT_WFE_STAT	R	0h	WFE Status Reset Source: mod_g_rst_n
3:1	RESERVED	NONE		Reserved
0	R5SS1_CORE0_STAT_WFI_STAT	R	0h	WFI Status Reset Source: mod_g_rst_n

2.3.13 CFG0_R5SS1_CORE1_STAT Registers

2.3.13.1 CFG0_CORE1_STAT Register (Offset = 54h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-143. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0054h

Figure 2-70. R5SS1_CORE1_STAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											R5SS1_CORE1_STAT_WFE_STAT	RESERVED			R5SS1_CORE1_STAT_WFI_STAT
NONE											R	NONE			R
0											0h	0			0h

Access Types Legend

Table 2-144. R5SS1_CORE1_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4	R5SS1_CORE1_STAT_WFE_STAT	R	0h	WFE Status Reset Source: mod_g_rst_n
3:1	RESERVED	NONE		Reserved
0	R5SS1_CORE1_STAT_WFI_STAT	R	0h	WFI Status Reset Source: mod_g_rst_n

2.3.14 CFG0_R5SS1_FORCE_WFI Registers

2.3.14.1 CFG0_FORCE_WFI Register (Offset = 58h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-145. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0058h

Figure 2-71. R5SS1_FORCE_WFI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_STC_CONTROL1_CR5_WFI_OVERIDE		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-146. R5SS1_FORCE_WFI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_STC_CONTROL1_CR5_WFI_OVERIDE	R/W	0h	writing 3'b111 will force the wfi signals of R5SS to 1 Reset Source: mod_g_rst_n

2.3.15 CFG0_R5SS0_ROM_ECLIPSE Registers

2.3.15.1 CFG0_ROM_ECLIPSE Register (Offset = 80h) [reset = 700h]

Short Description:

Long Description:

Return to Summary Table

Table 2-147. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0080h

Figure 2-72. R5SS0_ROM_ECLIPSE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
42294180															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					R5SS0_ROM_ECLIPSE_MEMSWAP_WAIT			RESERVED					R5SS0_ROM_ECLIPSE_MEMSWAP		
NONE					R/W			NONE					R/W		
42294180					7h			0					0h		

Access Types Legend

Table 2-148. R5SS0_ROM_ECLIPSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE		Reserved
10:8	R5SS0_ROM_ECLIPSE_MEMSWAP_WAIT	R/W	7h	writing 3'b111 ensures ROM-Eclipsing happens only after R5SS reset. Orelse it will be a immediate change. Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	R5SS0_ROM_ECLIPSE_MEMSWAP	R/W	0h	writing '111' ensures eclipsing of CR5A_ROM immediately if memswap_wait is not set. If memswap_wait is set then ROM is eclipsed after R5SS reset assertion. Reset Source: mod_g_rst_n

2.3.16 CFG0_R5SS0_TEINIT Registers

2.3.16.1 CFG0_TEINIT Register (Offset = 90h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-149. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0090h

Figure 2-73. R5SS0_TEINIT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															R5SS0_GLOBAL_CONFIG_TEINIT
NONE															R/W
0															0h

Access Types Legend

Table 2-150. R5SS0_TEINIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	R5SS0_GLOBAL_CONFIG_TEINIT	R/W	0h	Exception handling state at reset. 0-ARM 1-Thumb Reset Source: mod_g_rst_n

2.3.17 CFG0_R5SS1_TEINIT Registers

2.3.17.1 CFG0_TEINIT Register (Offset = 94h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-151. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0094h

Figure 2-74. R5SS1_TEINIT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															R5SS1_GLOBAL_CONFIG_TEINIT
NONE															R/W
0															0h

Access Types Legend

Table 2-152. R5SS1_TEINIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	R5SS1_GLOBAL_CONFIG_TEINIT	R/W	0h	Exception handling state at reset. 0-ARM 1-Thumb Reset Source: mod_g_rst_n

2.3.18 CFG0_R5SS0_CORE0_AHB_BASE Registers

2.3.18.1 CFG0_CORE0_AHB_BASE Register (Offset = A0h) [reset = 50000h]

Short Description:

Long Description:

Return to Summary Table

Table 2-153. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 00A0h

Figure 2-75. R5SS0_CORE0_AHB_BASE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												R5A0_AHB_BASE_AHB_BASE			
NONE												R/W			
0												50000h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R5A0_AHB_BASE_AHB_BASE															
R/W															
50000h															

Access Types Legend

Table 2-154. R5SS0_CORE0_AHB_BASE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	R5A0_AHB_BASE_AHB_BASE	R/W	50000h	Ti internal Register. Modifying this register is not recommended Decides the base address of ahb region Reset Source: mod_g_rst_n

2.3.19 CFG0_R5SS1_CORE0_AHB_BASE Registers

2.3.19.1 CFG0_CORE0_AHB_BASE Register (Offset = A4h) [reset = 50000h]

Short Description:

Long Description:

Return to Summary Table

Table 2-155. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 00A4h

Figure 2-76. R5SS1_CORE0_AHB_BASE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												R5A1_AHB_BASE_AHB_BASE			
NONE												R/W			
0												50000h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R5A1_AHB_BASE_AHB_BASE															
R/W															
50000h															

Access Types Legend

Table 2-156. R5SS1_CORE0_AHB_BASE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	R5A1_AHB_BASE_AHB_BASE	R/W	50000h	Ti internal Register. Modifying this register is not recommended Decides the base address of ahb region Reset Source: mod_g_rst_n

2.3.20 CFG0_R5SS0_CORE0_AHB_SIZE Registers

2.3.20.1 CFG0_CORE0_AHB_SIZE Register (Offset = A8h) [reset = 13h]

Short Description:

Long Description:

Return to Summary Table

Table 2-157. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 00A8h

Figure 2-77. R5SS0_CORE0_AHB_SIZE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
3e9															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											R5A0_AHB_SIZE_AHB_SIZE				
NONE											R/W				
3e9											13h				

Access Types Legend

Table 2-158. R5SS0_CORE0_AHB_SIZE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	R5A0_AHB_SIZE_AHB_SIZE	R/W	13h	Ti internal Register. Modifying this register is not recommended Code for selecting size for ahb. b00011 4KB b00100 8KB b00101 16KB b00110 32KB b00111 64KB b01000 128KB b01001 256KB b01010 512KB b01011 1MB b01100 2MB b01101 4MB b01110 8MB b01111 16MB b10000 32MB b10001 64MB b10010 128MB b10011 256MB b10100 512MB b10101 1GB b10110 2GB b10111 4GB Reset Source: mod_g_rst_n

2.3.21 CFG0_R5SS1_CORE0_AHB_SIZE Registers

2.3.21.1 CFG0_CORE0_AHB_SIZE Register (Offset = ACh) [reset = 13h]

Short Description:

Long Description:

Return to Summary Table

Table 2-159. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 00ACh

Figure 2-78. R5SS1_CORE0_AHB_SIZE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
3e9															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											R5A1_AHB_SIZE_AHB_SIZE				
NONE											R/W				
3e9											13h				

Access Types Legend

Table 2-160. R5SS1_CORE0_AHB_SIZE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	R5A1_AHB_SIZE_AHB_SIZE	R/W	13h	Ti internal Register. Modifying this register is not recommended Code for selecting size for ahb. b00011 4KB b00100 8KB b00101 16KB b00110 32KB b00111 64KB b01000 128KB b01001 256KB b01010 512KB b01011 1MB b01100 2MB b01101 4MB b01110 8MB b01111 16MB b10000 32MB b10001 64MB b10010 128MB b10011 256MB b10100 512MB b10101 1GB b10110 2GB b10111 4GB Reset Source: mod_g_rst_n

2.3.22 CFG0_R5SS0_CORE1_AHB_BASE Registers

2.3.22.1 CFG0_CORE1_AHB_BASE Register (Offset = B0h) [reset = 50000h]

Short Description:

Long Description:

Return to Summary Table

Table 2-161. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 00B0h

Figure 2-79. R5SS0_CORE1_AHB_BASE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												R5B0_AHB_BASE_AHB_BASE			
NONE												R/W			
0												50000h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R5B0_AHB_BASE_AHB_BASE															
R/W															
50000h															

Access Types Legend

Table 2-162. R5SS0_CORE1_AHB_BASE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	R5B0_AHB_BASE_AHB_BASE	R/W	50000h	Ti internal Register. Modifying this register is not recommended Decides the base address of ahb region Reset Source: mod_g_rst_n

2.3.23 CFG0_R5SS1_CORE1_AHB_BASE Registers

2.3.23.1 CFG0_CORE1_AHB_BASE Register (Offset = B4h) [reset = 50000h]

Short Description:

Long Description:

Return to Summary Table

Table 2-163. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 00B4h

Figure 2-80. R5SS1_CORE1_AHB_BASE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												R5B1_AHB_BASE_AHB_BASE			
NONE												R/W			
0												50000h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R5B1_AHB_BASE_AHB_BASE															
R/W															
50000h															

Access Types Legend

Table 2-164. R5SS1_CORE1_AHB_BASE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	R5B1_AHB_BASE_AHB_BASE	R/W	50000h	Ti internal Register. Modifying this register is not recommended Decides the base address of ahb region Reset Source: mod_g_rst_n

2.3.24 CFG0_R5SS0_CORE1_AHB_SIZE Registers

2.3.24.1 CFG0_CORE1_AHB_SIZE Register (Offset = B8h) [reset = 13h]

Short Description:

Long Description:

Return to Summary Table

Table 2-165. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 00B8h

Figure 2-81. R5SS0_CORE1_AHB_SIZE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
3e9															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											R5B0_AHB_SIZE_AHB_SIZE				
NONE											R/W				
3e9											13h				

Access Types Legend

Table 2-166. R5SS0_CORE1_AHB_SIZE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	R5B0_AHB_SIZE_AHB_SIZE	R/W	13h	Ti internal Register. Modifying this register is not recommended Code for selecting size for ahb. b00011 4KB b00100 8KB b00101 16KB b00110 32KB b00111 64KB b01000 128KB b01001 256KB b01010 512KB b01011 1MB b01100 2MB b01101 4MB b01110 8MB b01111 16MB b10000 32MB b10001 64MB b10010 128MB b10011 256MB b10100 512MB b10101 1GB b10110 2GB b10111 4GB Reset Source: mod_g_rst_n

2.3.25 CFG0_R5SS1_CORE1_AHB_SIZE Registers

2.3.25.1 CFG0_CORE1_AHB_SIZE Register (Offset = BCh) [reset = 13h]

Short Description:

Long Description:

Return to Summary Table

Table 2-167. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 00BCh

Figure 2-82. R5SS1_CORE1_AHB_SIZE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
3e9															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											R5B1_AHB_SIZE_AHB_SIZE				
NONE											R/W				
3e9											13h				

Access Types Legend

Table 2-168. R5SS1_CORE1_AHB_SIZE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	R5B1_AHB_SIZE_AHB_SIZE	R/W	13h	Ti internal Register. Modifying this register is not recommended Code for selecting size for ahb. b00011 4KB b00100 8KB b00101 16KB b00110 32KB b00111 64KB b01000 128KB b01001 256KB b01010 512KB b01011 1MB b01100 2MB b01101 4MB b01110 8MB b01111 16MB b10000 32MB b10001 64MB b10010 128MB b10011 256MB b10100 512MB b10101 1GB b10110 2GB b10111 4GB Reset Source: mod_g_rst_n

2.3.26 CFG0_R5SS0_TCM_ECC_WRENZ_EN Registers

2.3.26.1 CFG0_TCM_ECC_WRENZ_EN Register (Offset = D8h) [reset = 777777h]

Short Description:

Long Description:

Return to Summary Table

Table 2-169. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 00D8h

Figure 2-83. R5SS0_TCM_ECC_WRENZ_EN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED									R5SS0_TCM_ECC_WRENZ_EN_CPU1_TCMB1_WRENZ_EN			RESERVED	R5SS0_TCM_ECC_WRENZ_EN_CPU1_TCMB0_WRENZ_EN		
NONE									R/W			NONE	R/W		
9a4823									7h			1	7h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	R5SS0_TCM_ECC_WRENZ_EN_CPU1_TCMA_WRENZ_EN			RESERVED	R5SS0_TCM_ECC_WRENZ_EN_CPU0_TCMB1_WRENZ_EN			RESERVED	R5SS0_TCM_ECC_WRENZ_EN_CPU0_TCMB0_WRENZ_EN			RESERVED	R5SS0_TCM_ECC_WRENZ_EN_CPU0_TCMA_WRENZ_EN		
NONE	R/W			NONE	R/W			NONE	R/W			NONE	R/W		
1	7h			1	7h			0	7h			0	7h		

Access Types Legend

Table 2-170. R5SS0_TCM_ECC_WRENZ_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE		Reserved
22:20	R5SS0_TCM_ECC_WRENZ_EN_CPU1_TCMB1_WRENZ_EN	R/W	7h	writing '000' blocks the writes to ECC-bits of TCMB0-RAM of CR5B. Writing '111' unblocks the writes to ECC-bits of TCMB1-RAM of CR5B Reset Source: mod_g_rst_n
19	RESERVED	NONE		Reserved
18:16	R5SS0_TCM_ECC_WRENZ_EN_CPU1_TCMB0_WRENZ_EN	R/W	7h	writing '000' blocks the writes to ECC-bits of TCMB0-RAM of CR5B. Writing '111' unblocks the writes to ECC-bits of TCMB0-RAM of CR5B Reset Source: mod_g_rst_n
15	RESERVED	NONE		Reserved
14:12	R5SS0_TCM_ECC_WRENZ_EN_CPU1_TCMA_WRENZ_EN	R/W	7h	writing '000' blocks the writes to ECC-bits of TCMA-RAM of CR5B. Writing '111' unblocks the writes to ECC-bits of TCMA-RAM of CR5B Reset Source: mod_g_rst_n
11	RESERVED	NONE		Reserved
10:8	R5SS0_TCM_ECC_WRENZ_EN_CPU0_TCMB1_WRENZ_EN	R/W	7h	writing '000' blocks the writes to ECC-bits of TCMB0-RAM of CR5A. Writing '111' unblocks the writes to ECC-bits of TCMB1-RAM of CR5A Reset Source: mod_g_rst_n
7	RESERVED	NONE		Reserved
6:4	R5SS0_TCM_ECC_WRENZ_EN_CPU0_TCMB0_WRENZ_EN	R/W	7h	writing '000' blocks the writes to ECC-bits of TCMB0-RAM of CR5A. Writing '111' unblocks the writes to ECC-bits of TCMB0-RAM of CR5A Reset Source: mod_g_rst_n
3	RESERVED	NONE		Reserved
2:0	R5SS0_TCM_ECC_WRENZ_EN_CPU0_TCMA_WRENZ_EN	R/W	7h	writing '000' blocks the writes to ECC-bits of TCMA-RAM of CR5A. Writing '111' unblocks the writes to ECC-bits of TCMA-RAM of CR5A Reset Source: mod_g_rst_n

2.3.27 CFG0_R5SS1_TCM_ECC_WRENZ_EN Registers

2.3.27.1 CFG0_TCM_ECC_WRENZ_EN Register (Offset = DCh) [reset = 777777h]

Short Description:

Long Description:

Return to Summary Table

Table 2-171. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 00DCh

Figure 2-84. R5SS1_TCM_ECC_WRENZ_EN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED									R5SS1_TCM_ECC_WRENZ_EN_CPU1_TCMB1_WRENZ_EN			RESERVED	R5SS1_TCM_ECC_WRENZ_EN_CPU1_TCMB0_WRENZ_EN		
NONE									R/W			NONE	R/W		
9a4823									7h			1	7h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	R5SS1_TCM_ECC_WRENZ_EN_CPU1_TCMA_WRENZ_EN			RESERVED	R5SS1_TCM_ECC_WRENZ_EN_CPU0_TCMB1_WRENZ_EN			RESERVED	R5SS1_TCM_ECC_WRENZ_EN_CPU0_TCMB0_WRENZ_EN			RESERVED	R5SS1_TCM_ECC_WRENZ_EN_CPU0_TCMA_WRENZ_EN		
NONE	R/W			NONE	R/W			NONE	R/W			NONE	R/W		
1	7h			1	7h			0	7h			0	7h		

Access Types Legend

Table 2-172. R5SS1_TCM_ECC_WRENZ_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE		Reserved
22:20	R5SS1_TCM_ECC_WRENZ_EN_CPU1_TCMB1_WRENZ_EN	R/W	7h	writing '000' blocks the writes to ECC-bits of TCMB0-RAM of CR5B. Writing '111' unblocks the writes to ECC-bits of TCMB1-RAM of CR5B Reset Source: mod_g_rst_n
19	RESERVED	NONE		Reserved
18:16	R5SS1_TCM_ECC_WRENZ_EN_CPU1_TCMB0_WRENZ_EN	R/W	7h	writing '000' blocks the writes to ECC-bits of TCMB0-RAM of CR5B. Writing '111' unblocks the writes to ECC-bits of TCMB0-RAM of CR5B Reset Source: mod_g_rst_n
15	RESERVED	NONE		Reserved
14:12	R5SS1_TCM_ECC_WRENZ_EN_CPU1_TCMA_WRENZ_EN	R/W	7h	writing '000' blocks the writes to ECC-bits of TCMA-RAM of CR5B. Writing '111' unblocks the writes to ECC-bits of TCMA-RAM of CR5B Reset Source: mod_g_rst_n
11	RESERVED	NONE		Reserved
10:8	R5SS1_TCM_ECC_WRENZ_EN_CPU0_TCMB1_WRENZ_EN	R/W	7h	writing '000' blocks the writes to ECC-bits of TCMB0-RAM of CR5A. Writing '111' unblocks the writes to ECC-bits of TCMB1-RAM of CR5A Reset Source: mod_g_rst_n
7	RESERVED	NONE		Reserved
6:4	R5SS1_TCM_ECC_WRENZ_EN_CPU0_TCMB0_WRENZ_EN	R/W	7h	writing '000' blocks the writes to ECC-bits of TCMB0-RAM of CR5A. Writing '111' unblocks the writes to ECC-bits of TCMB0-RAM of CR5A Reset Source: mod_g_rst_n
3	RESERVED	NONE		Reserved
2:0	R5SS1_TCM_ECC_WRENZ_EN_CPU0_TCMA_WRENZ_EN	R/W	7h	writing '000' blocks the writes to ECC-bits of TCMA-RAM of CR5A. Writing '111' unblocks the writes to ECC-bits of TCMA-RAM of CR5A Reset Source: mod_g_rst_n

2.3.28 CFG0_BOOT_INFO_REG0 Registers

2.3.28.1 CFG0_INFO_REG0 Register (Offset = 100h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-173. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0100h

Figure 2-85. BOOT_INFO_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_BOOT_INFO_REG0_CONFIG															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_BOOT_INFO_REG0_CONFIG															
R/W															
0h															

Access Types Legend

Table 2-174. BOOT_INFO_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_BOOT_INFO_REG0_CONFIG	R/W	0h	Reserved Register for Software use **Note: This bit will only be reset by PORz. Reset Source: mod_por_rst_n

2.3.29 CFG0_BOOT_INFO_REG1 Registers

2.3.29.1 CFG0_INFO_REG1 Register (Offset = 104h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-175. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0104h

Figure 2-86. BOOT_INFO_REG1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_BOOT_INFO_REG1_CONFIG															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_BOOT_INFO_REG1_CONFIG															
R/W															
0h															

Access Types Legend

Table 2-176. BOOT_INFO_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_BOOT_INFO_REG1_CONFIG	R/W	0h	Reserved Register for Software use **Note: This bit will only be reset by PORz. Reset Source: mod_por_rst_n

2.3.30 CFG0_BOOT_INFO_REG2 Registers

2.3.30.1 CFG0_INFO_REG2 Register (Offset = 108h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-177. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0108h

Figure 2-87. BOOT_INFO_REG2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_BOOT_INFO_REG2_CONFIG															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_BOOT_INFO_REG2_CONFIG															
R/W															
0h															

Access Types Legend

Table 2-178. BOOT_INFO_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_BOOT_INFO_REG2_CONFIG	R/W	0h	Reserved Register for Software use **Note: This bit will only be reset by PORz. Reset Source: mod_por_rst_n

2.3.31 CFG0_BOOT_INFO_REG3 Registers

2.3.31.1 CFG0_INFO_REG3 Register (Offset = 10Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-179. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 010Ch

Figure 2-88. BOOT_INFO_REG3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_BOOT_INFO_REG3_CONFIG															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_BOOT_INFO_REG3_CONFIG															
R/W															
0h															

Access Types Legend

Table 2-180. BOOT_INFO_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_BOOT_INFO_REG3_CONFIG	R/W	0h	Reserved Register for Software use **Note: This bit will only be reset by PORz. Reset Source: mod_por_rst_n

2.3.32 CFG0_BOOT_INFO_REG4 Registers

2.3.32.1 CFG0_INFO_REG4 Register (Offset = 110h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-181. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0110h

Figure 2-89. BOOT_INFO_REG4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_BOOT_INFO_REG4_CONFIG															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_BOOT_INFO_REG4_CONFIG															
R/W															
0h															

Access Types Legend

Table 2-182. BOOT_INFO_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_BOOT_INFO_REG4_CONFIG	R/W	0h	Reserved Register for Software use **Note: This bit will only be reset by PORz. Reset Source: mod_por_rst_n

2.3.33 CFG0_BOOT_INFO_REG5 Registers

2.3.33.1 CFG0_INFO_REG5 Register (Offset = 114h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-183. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0114h

Figure 2-90. BOOT_INFO_REG5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_BOOT_INFO_REG5_CONFIG															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_BOOT_INFO_REG5_CONFIG															
R/W															
0h															

Access Types Legend

Table 2-184. BOOT_INFO_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_BOOT_INFO_REG5_CONFIG	R/W	0h	Reserved Register for Software use **Note: This bit will only be reset by PORz. Reset Source: mod_por_rst_n

2.3.34 CFG0_BOOT_INFO_REG6 Registers

2.3.34.1 CFG0_INFO_REG6 Register (Offset = 118h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-185. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0118h

Figure 2-91. BOOT_INFO_REG6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_BOOT_INFO_REG6_CONFIG															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_BOOT_INFO_REG6_CONFIG															
R/W															
0h															

Access Types Legend

Table 2-186. BOOT_INFO_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_BOOT_INFO_REG6_CONFIG	R/W	0h	Reserved Register for Software use **Note: This bit will only be reset by PORz. Reset Source: mod_por_rst_n

2.3.35 CFG0_BOOT_INFO_REG7 Registers

2.3.35.1 CFG0_INFO_REG7 Register (Offset = 11Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-187. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 011Ch

Figure 2-92. BOOT_INFO_REG7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_BOOT_INFO_REG7_CONFIG															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_BOOT_INFO_REG7_CONFIG															
R/W															
0h															

Access Types Legend

Table 2-188. BOOT_INFO_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_BOOT_INFO_REG7_CONFIG	R/W	0h	Reserved Register for Software use **Note: This bit will only be reset by PORz. Reset Source: mod_por_rst_n

2.3.36 CFG0_R5SS0_ATCM_MEM_INIT Registers

2.3.36.1 CFG0_ATCM_MEM_INIT Register (Offset = 200h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-189. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0200h

Figure 2-93. R5SS0_ATCM_MEM_INIT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															MSS_ATCM0_MEM_INIT_MEM_INIT
NONE															R/W
0															0h

Access Types Legend

Table 2-190. R5SS0_ATCM_MEM_INIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	MSS_ATCM0_MEM_INIT_MEM_INIT	R/W	0h	Write_pulse bit field: Writing 1'b1 will start initializing the ATCM banks of CR5A/B. Value in each row is initialized to 0x0C_0000_0000 Reset Source: mod_g_rst_n

2.3.37 CFG0_R5SS0_ATCM_MEM_INIT_DONE Registers

2.3.37.1 CFG0_ATCM_MEM_INIT_DONE Register (Offset = 204h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-191. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0204h

Figure 2-94. R5SS0_ATCM_MEM_INIT_DONE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															MSS_ATCM0_MEM_INIT_DONE_MEM_INIT_DONE
NONE															R/W1TC
0															0h

Access Types Legend

Table 2-192. R5SS0_ATCM_MEM_INIT_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	MSS_ATCM0_MEM_INIT_DONE_MEM_INIT_DONE	R/W1TC	0h	This field will be high once initialization of ATCM banks is finished. Writing '1' would clear the bit. Reset Source: mod_g_rst_n

2.3.38 CFG0_R5SS0_ATCM_MEM_INIT_STATUS Registers

2.3.38.1 CFG0_ATCM_MEM_INIT_STATUS Register (Offset = 208h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-193. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0208h

Figure 2-95. R5SS0_ATCM_MEM_INIT_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															MSS_ATCM0_MEM_INIT_STATUS_MEM_STATUS
NONE															R
0															0h

Access Types Legend

Table 2-194. R5SS0_ATCM_MEM_INIT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	MSS_ATCM0_MEM_INIT_STATUS_MEM_STATUS	R	0h	1'b0: No initialization is happening for ATCM banks of CR5A/B 1'b1: Initialization is in progress for ATCM banks of CR5A/B Reset Source: mod_g_rst_n

2.3.39 CFG0_R5SS0_BTCM_MEM_INIT Registers

2.3.39.1 CFG0_BTCM_MEM_INIT Register (Offset = 210h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-195. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0210h

Figure 2-96. R5SS0_BTCM_MEM_INIT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															MSS_BTCM0_MEM_INIT_MEM_INIT
NONE															R/W
0															0h

Access Types Legend

Table 2-196. R5SS0_BTCM_MEM_INIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	MSS_BTCM0_MEM_INIT_MEM_INIT	R/W	0h	Write_pulse bit field: Writing 1'b1 will start initializing the B0/1TCM banks of CR5A/B Reset Source: mod_g_rst_n

2.3.40 CFG0_R5SS0_BTCM_MEM_INIT_DONE Registers

2.3.40.1 CFG0_BTCM_MEM_INIT_DONE Register (Offset = 214h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-197. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0214h

Figure 2-97. R5SS0_BTCM_MEM_INIT_DONE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															MSS_BTCM0_MEM_INIT_DONE_MEM_INIT_DONE
NONE															R/W1TC
0															0h

Access Types Legend

Table 2-198. R5SS0_BTCM_MEM_INIT_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	MSS_BTCM0_MEM_INIT_DONE_MEM_INIT_DONE	R/W1TC	0h	This field will be high once initialization of B0/1TCM banks is finished. Writing '1' would clear the bit. Reset Source: mod_g_rst_n

2.3.41 CFG0_R5SS0_BTCM_MEM_INIT_STATUS Registers

2.3.41.1 CFG0_BTCM_MEM_INIT_STATUS Register (Offset = 218h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-199. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0218h

Figure 2-98. R5SS0_BTCM_MEM_INIT_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															MSS_BTCM0_MEM_INIT_STATUS_MEM_STATUS
NONE															R
0															0h

Access Types Legend

Table 2-200. R5SS0_BTCM_MEM_INIT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	MSS_BTCM0_MEM_INIT_STATUS_MEM_STATUS	R	0h	1'b0: No initialization is happening for B0/1TCM banks of CR5A/B 1'b1: Initialization is in progress for B0/1TCM banks of CR5A/B Reset Source: mod_g_rst_n

2.3.42 CFG0_R5SS1_ATCM_MEM_INIT Registers

2.3.42.1 CFG0_ATCM_MEM_INIT Register (Offset = 220h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-201. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0220h

Figure 2-99. R5SS1_ATCM_MEM_INIT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															MSS_ATCM1_MEM_INIT_MEM_INIT
NONE															R/W
0															0h

Access Types Legend

Table 2-202. R5SS1_ATCM_MEM_INIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	MSS_ATCM1_MEM_INIT_MEM_INIT	R/W	0h	Write_pulse bit field: Writing 1'b1 will start initializing the ATCM banks of CR5A/B. Value in each row is initialized to 0x0C_0000_0000 Reset Source: mod_g_rst_n

2.3.43 CFG0_R5SS1_ATCM_MEM_INIT_DONE Registers

2.3.43.1 CFG0_ATCM_MEM_INIT_DONE Register (Offset = 224h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-203. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0224h

Figure 2-100. R5SS1_ATCM_MEM_INIT_DONE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															MSS_ATCM1_MEM_INIT_DONE_MEM_INIT_DONE
NONE															R/W1TC
0															0h

Access Types Legend

Table 2-204. R5SS1_ATCM_MEM_INIT_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	MSS_ATCM1_MEM_INIT_DONE_MEM_INIT_DONE	R/W1TC	0h	This field will be high once initialization of ATCM banks is finished. Writing '1' would clear the bit. Reset Source: mod_g_rst_n

2.3.44 CFG0_R5SS1_ATCM_MEM_INIT_STATUS Registers

2.3.44.1 CFG0_ATCM_MEM_INIT_STATUS Register (Offset = 228h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-205. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0228h

Figure 2-101. R5SS1_ATCM_MEM_INIT_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															MSS_ATCM1_MEM_INIT_STATUS_MEM_STATUS
NONE															R
0															0h

Access Types Legend

Table 2-206. R5SS1_ATCM_MEM_INIT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	MSS_ATCM1_MEM_INIT_STATUS_MEM_STATUS	R	0h	1'b0: No initialization is happening for ATCM banks of CR5A/B 1'b1: Initialization is in progress for ATCM banks of CR5A/B Reset Source: mod_g_rst_n

2.3.45 CFG0_R5SS1_BTCM_MEM_INIT Registers

2.3.45.1 CFG0_BTCM_MEM_INIT Register (Offset = 230h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-207. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0230h

Figure 2-102. R5SS1_BTCM_MEM_INIT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															MSS_BTCM1_MEM_INIT_MEM_INIT
NONE															R/W
0															0h

Access Types Legend

Table 2-208. R5SS1_BTCM_MEM_INIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	MSS_BTCM1_MEM_INIT_MEM_INIT	R/W	0h	Write_pulse bit field: Writing 1'b1 will start initializing the B0/1TCM banks of CR5A/B Reset Source: mod_g_rst_n

2.3.46 CFG0_R5SS1_BTCM_MEM_INIT_DONE Registers

2.3.46.1 CFG0_BTCM_MEM_INIT_DONE Register (Offset = 234h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-209. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0234h

Figure 2-103. R5SS1_BTCM_MEM_INIT_DONE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															MSS_BTCM1_MEM_INIT_DONE_MEM_INIT_DONE
NONE															R/W1TC
0															0h

Access Types Legend

Table 2-210. R5SS1_BTCM_MEM_INIT_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	MSS_BTCM1_MEM_INIT_DONE_MEM_INIT_DONE	R/W1TC	0h	This field will be high once initialization of B0/1TCM banks is finished. Writing '1' would clear the bit. Reset Source: mod_g_rst_n

2.3.47 CFG0_R5SS1_BTCM_MEM_INIT_STATUS Registers

2.3.47.1 CFG0_BTCM_MEM_INIT_STATUS Register (Offset = 238h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-211. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0238h

Figure 2-104. R5SS1_BTCM_MEM_INIT_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															MSS_BTCM1_MEM_INIT_STATUS_MEM_STATUS
NONE															R
0															0h

Access Types Legend

Table 2-212. R5SS1_BTCM_MEM_INIT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	MSS_BTCM1_MEM_INIT_STATUS_MEM_STATUS	R	0h	1'b0: No initialization is happening for B0/1TCM banks of CR5A/B 1'b1: Initialization is in progress for B0/1TCM banks of CR5A/B Reset Source: mod_g_rst_n

2.3.48 CFG0_L2IOCRAM_MEM_INIT Registers

2.3.48.1 CFG0_MEM_INIT Register (Offset = 240h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-213. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0240h

Figure 2-105. L2IOCRAM_MEM_INIT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												MSS_L2_MEM_INIT_PARTITION3	MSS_L2_MEM_INIT_PARTITION2	MSS_L2_MEM_INIT_PARTITION1	MSS_L2_MEM_INIT_PARTITION0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 2-214. L2IOCRAM_MEM_INIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	MSS_L2_MEM_INIT_PARTITION3	R/W	0h	Write_pulse bit field: Writing 1'b1 will start initializing the L2 Bank3. Value in each row is initialized to 0x0 Reset Source: mod_g_rst_n
2	MSS_L2_MEM_INIT_PARTITION2	R/W	0h	Write_pulse bit field: Writing 1'b1 will start initializing the L2 Bank2. Value in each row is initialized to 0x0 Reset Source: mod_g_rst_n
1	MSS_L2_MEM_INIT_PARTITION1	R/W	0h	Write_pulse bit field: Writing 1'b1 will start initializing the L2 Bank1. Value in each row is initialized to 0x0 Reset Source: mod_g_rst_n
0	MSS_L2_MEM_INIT_PARTITION0	R/W	0h	Write_pulse bit field: Writing 1'b1 will start initializing the L2 Bank0. Value in each row is initialized to 0x0 Reset Source: mod_g_rst_n

2.3.49 CFG0_L2OCRAM_MEM_INIT_DONE Registers

2.3.49.1 CFG0_MEM_INIT_DONE Register (Offset = 244h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-215. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0244h

Figure 2-106. L2OCRAM_MEM_INIT_DONE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												MSS_L2_MEM_INIT_DONE_PARTITION3	MSS_L2_MEM_INIT_DONE_PARTITION2	MSS_L2_MEM_INIT_DONE_PARTITION1	MSS_L2_MEM_INIT_DONE_PARTITION0
NONE												R/W1TC	R/W1TC	R/W1TC	R/W1TC
0												0h	0h	0h	0h

Access Types Legend

Table 2-216. L2OCRAM_MEM_INIT_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	MSS_L2_MEM_INIT_DONE_PARTITION3	R/W1TC	0h	This field will be high once intialization of L2 bank3 is finished. Writing '1' would clear the bit Reset Source: mod_g_rst_n
2	MSS_L2_MEM_INIT_DONE_PARTITION2	R/W1TC	0h	This field will be high once intialization of L2 bank2 is finished. Writing '1' would clear the bit Reset Source: mod_g_rst_n
1	MSS_L2_MEM_INIT_DONE_PARTITION1	R/W1TC	0h	This field will be high once intialization of L2 bank1 is finished. Writing '1' would clear the bit Reset Source: mod_g_rst_n
0	MSS_L2_MEM_INIT_DONE_PARTITION0	R/W1TC	0h	This field will be high once intialization of L2 bank0 is finished. Writing '1' would clear the bit Reset Source: mod_g_rst_n

2.3.50 CFG0_L2OCRAM_MEM_INIT_STATUS Registers

2.3.50.1 CFG0_MEM_INIT_STATUS Register (Offset = 248h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-217. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0248h

Figure 2-107. L2OCRAM_MEM_INIT_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												MSS_L2_MEM_INIT_STATUS_PARTITION3	MSS_L2_MEM_INIT_STATUS_PARTITION2	MSS_L2_MEM_INIT_STATUS_PARTITION1	MSS_L2_MEM_INIT_STATUS_PARTITION0
NONE												R	R	R	R
0												0h	0h	0h	0h

Access Types Legend

Table 2-218. L2OCRAM_MEM_INIT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	MSS_L2_MEM_INIT_STATUS_PARTITION3	R	0h	1'b0: No initialization is happening for L2 bank3 1'b1: Initialization is in progress for L2 bank3 Reset Source: mod_g_rst_n
2	MSS_L2_MEM_INIT_STATUS_PARTITION2	R	0h	1'b0: No initialization is happening for L2 bank2 1'b1: Initialization is in progress for L2 bank2 Reset Source: mod_g_rst_n
1	MSS_L2_MEM_INIT_STATUS_PARTITION1	R	0h	1'b0: No initialization is happening for L2 bank1 1'b1: Initialization is in progress for L2 bank1 Reset Source: mod_g_rst_n
0	MSS_L2_MEM_INIT_STATUS_PARTITION0	R	0h	1'b0: No initialization is happening for L2 bank0 1'b1: Initialization is in progress for L2 bank0 Reset Source: mod_g_rst_n

2.3.51 CFG0_MAILBOXRAM_MEM_INIT Registers

2.3.51.1 CFG0_MEM_INIT Register (Offset = 250h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-219. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0250h

Figure 2-108. MAILBOXRAM_MEM_INIT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															MSS_MAILBOX_MEM_INIT_MEM0_INIT
NONE															R/W
0															0h

Access Types Legend

Table 2-220. MAILBOXRAM_MEM_INIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	MSS_MAILBOX_MEM_INIT_MEM0_INIT	R/W	0h	Write_pulse bit field: Writing 1'b1 will start initializing the MSS_MBOX. Value in each row is initialized to 0x0 Reset Source: mod_g_rst_n

2.3.52 CFG0_MAILBOXRAM_MEM_INIT_DONE Registers

2.3.52.1 CFG0_MEM_INIT_DONE Register (Offset = 254h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-221. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0254h

Figure 2-109. MAILBOXRAM_MEM_INIT_DONE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															MSS_MAILBOX_MEM_INIT_DONE_MEM0_DONE
NONE															R/W1TC
0															0h

Access Types Legend

Table 2-222. MAILBOXRAM_MEM_INIT_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	MSS_MAILBOX_MEM_INIT_DONE_MEM0_DONE	R/W1TC	0h	This field will be high once intialization of MSS_MBOX is finished. Writing '1' would clear the bit Reset Source: mod_g_rst_n

2.3.53 CFG0_MAILBOXRAM_MEM_INIT_STATUS Registers

2.3.53.1 CFG0_MEM_INIT_STATUS Register (Offset = 258h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-223. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0258h

Figure 2-110. MAILBOXRAM_MEM_INIT_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															MSS_MAILBOX_MEM_INIT_STATUS_MEM0_STATUS
NONE															R
0															0h

Access Types Legend

Table 2-224. MAILBOXRAM_MEM_INIT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	MSS_MAILBOX_MEM_INIT_STATUS_MEM0_STATUS	R	0h	1'b0: No initialization is happening for MSS_MBOX 1'b1: Initialization is in progress for MSS_MBOX Reset Source: mod_g_rst_n

2.3.54 CFG0_TPCC_MEM_INIT Registers

2.3.54.1 CFG0_MEM_INIT Register (Offset = 260h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-225. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0260h

Figure 2-111. TPCC_MEM_INIT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															MSS_TPCC_MEMINIT_START_TPCC_A_MEMINIT_START
NONE															R/W
0															0h

Access Types Legend

Table 2-226. TPCC_MEM_INIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	MSS_TPCC_MEMINIT_START_TPCC_A_MEMINIT_START	R/W	0h	Write_pulse bit field: Writing 1'b1 will start initializing the MSS_TPCCA Reset Source: mod_g_rst_n

2.3.55 CFG0_TPCC_MEM_INIT_DONE Registers

2.3.55.1 CFG0_MEM_INIT_DONE Register (Offset = 264h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-227. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0264h

Figure 2-112. TPCC_MEM_INIT_DONE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															MSS_TPCC_MEMINIT_DONE_TPCC_A_MEMINIT_DONE
NONE															R/W1TC
0															0h

Access Types Legend

Table 2-228. TPCC_MEM_INIT_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	MSS_TPCC_MEMINIT_DONE_TPCC_A_MEMINIT_DONE	R/W1TC	0h	This field will be high once intialization of MSS_TPCCA is finished. Writing '1' would clear the bit Reset Source: mod_g_rst_n

2.3.56 CFG0_TPCC_MEMINIT_STATUS Registers

2.3.56.1 CFG0_MEMINIT_STATUS Register (Offset = 268h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-229. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0268h

Figure 2-113. TPCC_MEMINIT_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															MSS_TPCC_MEMINIT_STATUS_TPCC_A_MEMINIT_STATUS
NONE															R
0															0h

Access Types Legend

Table 2-230. TPCC_MEMINIT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	MSS_TPCC_MEMINIT_STATUS_TPCC_A_MEMINIT_STATUS	R	0h	1'b0: No initialization is happening for MSS_TPCCA 1'b1: Initialization is in progress for MSS_TPCCB Reset Source: mod_g_rst_n

2.3.57 CFG0_TOP_PBIST_KEY_RST Registers

2.3.57.1 CFG0_PBIST_KEY_RST Register (Offset = 300h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-231. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0300h

Figure 2-114. TOP_PBIST_KEY_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MSS_PBIST_KEY_RST_PBIST_ST_RST				MSS_PBIST_KEY_RST_PBIST_ST_KEY			
NONE								R/W				R/W			
0								0h				0h			

Access Types Legend

Table 2-232. TOP_PBIST_KEY_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:4	MSS_PBIST_KEY_RST_PBIST_ST_RST	R/W	0h	MSS PBIST controller will be brought out of reset when value is 0xA Reset Source: mod_g_rst_n
3:0	MSS_PBIST_KEY_RST_PBIST_ST_KEY	R/W	0h	Top PBIST Selftest Key. Valid value is 0x5 Reset Source: mod_g_rst_n

2.3.58 CFG0_TOP_PBIST_REG0 Registers

2.3.58.1 CFG0_PBIST_REG0 Register (Offset = 304h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-233. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0304h

Figure 2-115. TOP_PBIST_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_PBIST_REG0_PBIST_REG															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_PBIST_REG0_PBIST_REG															
R/W															
0h															

Access Types Legend

Table 2-234. TOP_PBIST_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_PBIST_REG0_PBIST_REG	R/W	0h	Reset Source: mod_g_rst_n

2.3.59 CFG0_TOP_PBIST_REG1 Registers

2.3.59.1 CFG0_PBIST_REG1 Register (Offset = 308h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-235. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0308h

Figure 2-116. TOP_PBIST_REG1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_PBIST_REG1_PBIST_REG															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_PBIST_REG1_PBIST_REG															
R/W															
0h															

Access Types Legend

Table 2-236. TOP_PBIST_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_PBIST_REG1_PBIST_REG	R/W	0h	Reset Source: mod_g_rst_n

2.3.60 CFG0_TOP_PBIST_REG2 Registers

2.3.60.1 CFG0_PBIST_REG2 Register (Offset = 30Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-237. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 030Ch

Figure 2-117. TOP_PBIST_REG2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_PBIST_REG2_PBIST_REG															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_PBIST_REG2_PBIST_REG															
R/W															
0h															

Access Types Legend

Table 2-238. TOP_PBIST_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_PBIST_REG2_PBIST_REG	R/W	0h	Reset Source: mod_g_rst_n

2.3.61 CFG0_R5SS0_CTI_TRIG_SEL Registers

2.3.61.1 CFG0_CTI_TRIG_SEL Register (Offset = 400h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-239. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0400h

Figure 2-118. R5SS0_CTI_TRIG_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5SS0_CTI_TRIG_SEL_TRIG1								MSS_R5SS0_CTI_TRIG_SEL_TRIG0							
R/W								R/W							
0h								0h							

Access Types Legend

Table 2-240. R5SS0_CTI_TRIG_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_R5SS0_CTI_TRIG_SEL_TRIG1	R/W	0h	Used for selecting the trigger source for 1st trigger of MSS_R5SS Reset Source: mod_g_rst_n
7:0	MSS_R5SS0_CTI_TRIG_SEL_TRIG0	R/W	0h	Used for selecting the trigger source for 0th trigger of MSS_R5SS Reset Source: mod_g_rst_n

2.3.62 CFG0_R5SS1_CTI_TRIG_SEL Registers

2.3.62.1 CFG0_CTI_TRIG_SEL Register (Offset = 404h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-241. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0404h

Figure 2-119. R5SS1_CTI_TRIG_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5SS1_CTI_TRIG_SEL_TRIG1								MSS_R5SS1_CTI_TRIG_SEL_TRIG0							
R/W								R/W							
0h								0h							

Access Types Legend

Table 2-242. R5SS1_CTI_TRIG_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_R5SS1_CTI_TRIG_SEL_TRIG1	R/W	0h	Used for selecting the trigger source for 1st trigger of MSS_R5SS Reset Source: mod_g_rst_n
7:0	MSS_R5SS1_CTI_TRIG_SEL_TRIG0	R/W	0h	Used for selecting the trigger source for 0th trigger of MSS_R5SS Reset Source: mod_g_rst_n

2.3.63 CFG0_DBGSS_CTI_TRIG_SEL Registers

2.3.63.1 CFG0_CTI_TRIG_SEL Register (Offset = 408h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-243. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0408h

Figure 2-120. DBGSS_CTI_TRIG_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_DBGSS_CTI_TRIG_SEL_TRIG3								MSS_DBGSS_CTI_TRIG_SEL_TRIG2							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_DBGSS_CTI_TRIG_SEL_TRIG1								MSS_DBGSS_CTI_TRIG_SEL_TRIG0							
R/W								R/W							
0h								0h							

Access Types Legend

Table 2-244. DBGSS_CTI_TRIG_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_DBGSS_CTI_TRIG_SEL_TRIG3	R/W	0h	Used for selecting the trigger source for 3rd trigger of ONE_MCU_CTI Reset Source: mod_g_rst_n
23:16	MSS_DBGSS_CTI_TRIG_SEL_TRIG2	R/W	0h	Used for selecting the trigger source for 2nd trigger of ONE_MCU_CTI Reset Source: mod_g_rst_n
15:8	MSS_DBGSS_CTI_TRIG_SEL_TRIG1	R/W	0h	Used for selecting the trigger source for 1st trigger of ONE_MCU_CTI Reset Source: mod_g_rst_n
7:0	MSS_DBGSS_CTI_TRIG_SEL_TRIG0	R/W	0h	Used for selecting the trigger source for 0th trigger of ONE_MCU_CTI Reset Source: mod_g_rst_n

2.3.64 CFG0_MCAN0_HALTEN Registers

2.3.64.1 CFG0_HALTEN Register (Offset = 420h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-245. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0420h

Figure 2-121. MCAN0_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												CAN0_HALTEN_R5FSS11_HALTEN	CAN0_HALTEN_R5FSS0_CORE1_HALTEN	CAN0_HALTEN_R5FSS1_CORE0_HALTEN	CAN0_HALTEN_R5FSS0_CORE0_HALTEN
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 2-246. MCAN0_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	CAN0_HALTEN_R5FSS11_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
2	CAN0_HALTEN_R5FSS0_CORE1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
1	CAN0_HALTEN_R5FSS1_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
0	CAN0_HALTEN_R5FSS0_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n

2.3.65 CFG0_MCAN1_HALTEN Registers

2.3.65.1 CFG0_HALTEN Register (Offset = 424h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-247. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0424h

Figure 2-122. MCAN1_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												CAN1_HALTEN_R5FSS11_HALTEN	CAN1_HALTEN_R5FSS0_CORE1_HALTEN	CAN1_HALTEN_R5FSS1_CORE0_HALTEN	CAN1_HALTEN_R5FSS0_CORE0_HALTEN
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 2-248. MCAN1_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	CAN1_HALTEN_R5FSS11_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
2	CAN1_HALTEN_R5FSS0_CORE1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
1	CAN1_HALTEN_R5FSS1_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
0	CAN1_HALTEN_R5FSS0_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n

2.3.66 CFG0_MCAN2_HALTEN Registers

2.3.66.1 CFG0_HALTEN Register (Offset = 428h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-249. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0428h

Figure 2-123. MCAN2_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												CAN2_HALTEN_R5FSS11_HALTEN	CAN2_HALTEN_R5FSS0_CORE1_HALTEN	CAN2_HALTEN_R5FSS1_CORE0_HALTEN	CAN2_HALTEN_R5FSS0_CORE0_HALTEN
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 2-250. MCAN2_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	CAN2_HALTEN_R5FSS11_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
2	CAN2_HALTEN_R5FSS0_CORE1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
1	CAN2_HALTEN_R5FSS1_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
0	CAN2_HALTEN_R5FSS0_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n

2.3.67 CFG0_MCAN3_HALTEN Registers

2.3.67.1 CFG0_HALTEN Register (Offset = 42Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-251. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 042Ch

Figure 2-124. MCAN3_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												CAN3_HALTEN_R5FSS11_HALTEN	CAN3_HALTEN_R5FSS0_CORE1_HALTEN	CAN3_HALTEN_R5FSS1_CORE0_HALTEN	CAN3_HALTEN_R5FSS0_CORE0_HALTEN
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 2-252. MCAN3_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	CAN3_HALTEN_R5FSS11_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
2	CAN3_HALTEN_R5FSS0_CORE1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
1	CAN3_HALTEN_R5FSS1_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
0	CAN3_HALTEN_R5FSS0_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n

2.3.68 CFG0_LIN0_HALTEN Registers

2.3.68.1 CFG0_HALTEN Register (Offset = 430h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-253. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0430h

Figure 2-125. LIN0_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												LIN0_HALTEN_R5FSS11_HALTEN	LIN0_HALTEN_R5FSS0_CORE1_HALTEN	LIN0_HALTEN_R5FSS1_CORE0_HALTEN	LIN0_HALTEN_R5FSS0_CORE0_HALTEN
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 2-254. LIN0_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	LIN0_HALTEN_R5FSS11_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
2	LIN0_HALTEN_R5FSS0_CORE1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
1	LIN0_HALTEN_R5FSS1_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
0	LIN0_HALTEN_R5FSS0_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n

2.3.69 CFG0_LIN1_HALTEN Registers

2.3.69.1 CFG0_HALTEN Register (Offset = 434h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-255. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0434h

Figure 2-126. LIN1_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												LIN1_HALTEN_R5FSS11_HALTEN	LIN1_HALTEN_R5FSS0_CORE1_HALTEN	LIN1_HALTEN_R5FSS1_CORE0_HALTEN	LIN1_HALTEN_R5FSS0_CORE0_HALTEN
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 2-256. LIN1_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	LIN1_HALTEN_R5FSS11_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
2	LIN1_HALTEN_R5FSS0_CORE1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
1	LIN1_HALTEN_R5FSS1_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
0	LIN1_HALTEN_R5FSS0_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n

2.3.70 CFG0_LIN2_HALTEN Registers

2.3.70.1 CFG0_HALTEN Register (Offset = 438h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-257. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0438h

Figure 2-127. LIN2_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												LIN2_HALTEN_R5FSS11_HALTEN	LIN2_HALTEN_R5FSS0_CORE1_HALTEN	LIN2_HALTEN_R5FSS1_CORE0_HALTEN	LIN2_HALTEN_R5FSS0_CORE0_HALTEN
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 2-258. LIN2_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	LIN2_HALTEN_R5FSS11_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
2	LIN2_HALTEN_R5FSS0_CORE1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
1	LIN2_HALTEN_R5FSS1_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
0	LIN2_HALTEN_R5FSS0_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n

2.3.71 CFG0_LIN3_HALTEN Registers

2.3.71.1 CFG0_HALTEN Register (Offset = 43Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-259. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 043Ch

Figure 2-128. LIN3_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												LIN3_HALTEN_R5FSS11_HALTEN	LIN3_HALTEN_R5FSS0_CORE1_HALTEN	LIN3_HALTEN_R5FSS1_CORE0_HALTEN	LIN3_HALTEN_R5FSS0_CORE0_HALTEN
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 2-260. LIN3_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	LIN3_HALTEN_R5FSS11_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
2	LIN3_HALTEN_R5FSS0_CORE1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
1	LIN3_HALTEN_R5FSS1_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
0	LIN3_HALTEN_R5FSS0_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n

2.3.72 CFG0_LIN4_HALTEN Registers

2.3.72.1 CFG0_HALTEN Register (Offset = 440h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-261. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0440h

Figure 2-129. LIN4_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												LIN4_HALTEN_R5FSS11_HALTEN	LIN4_HALTEN_R5FSS0_CORE1_HALTEN	LIN4_HALTEN_R5FSS1_CORE0_HALTEN	LIN4_HALTEN_R5FSS0_CORE0_HALTEN
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 2-262. LIN4_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	LIN4_HALTEN_R5FSS11_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
2	LIN4_HALTEN_R5FSS0_CORE1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
1	LIN4_HALTEN_R5FSS1_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
0	LIN4_HALTEN_R5FSS0_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n

2.3.73 CFG0_I2C0_HALTEN Registers

2.3.73.1 CFG0_HALTEN Register (Offset = 444h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-263. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0444h

Figure 2-130. I2C0_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												I2C0_HALTEN_R5FSS11_HALTEN	I2C0_HALTEN_R5FSS0_CORE1_HALTEN	I2C0_HALTEN_R5FSS1_CORE0_HALTEN	I2C0_HALTEN_R5FSS0_CORE0_HALTEN
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 2-264. I2C0_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	I2C0_HALTEN_R5FSS11_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
2	I2C0_HALTEN_R5FSS0_CORE1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
1	I2C0_HALTEN_R5FSS1_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
0	I2C0_HALTEN_R5FSS0_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n

2.3.74 CFG0_I2C1_HALTEN Registers

2.3.74.1 CFG0_HALTEN Register (Offset = 448h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-265. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0448h

Figure 2-131. I2C1_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												I2C1_HALTEN_R5FSS11_HALTEN	I2C1_HALTEN_R5FSS0_CORE1_HALTEN	I2C1_HALTEN_R5FSS1_CORE0_HALTEN	I2C1_HALTEN_R5FSS0_CORE0_HALTEN
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 2-266. I2C1_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	I2C1_HALTEN_R5FSS11_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
2	I2C1_HALTEN_R5FSS0_CORE1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
1	I2C1_HALTEN_R5FSS1_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
0	I2C1_HALTEN_R5FSS0_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n

2.3.75 CFG0_I2C2_HALTEN Registers

2.3.75.1 CFG0_HALTEN Register (Offset = 44Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-267. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 044Ch

Figure 2-132. I2C2_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												I2C2_HALTEN_R5FSS11_HALTEN	I2C2_HALTEN_R5FSS0_CORE1_HALTEN	I2C2_HALTEN_R5FSS1_CORE0_HALTEN	I2C2_HALTEN_R5FSS0_CORE0_HALTEN
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 2-268. I2C2_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	I2C2_HALTEN_R5FSS11_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
2	I2C2_HALTEN_R5FSS0_CORE1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
1	I2C2_HALTEN_R5FSS1_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
0	I2C2_HALTEN_R5FSS0_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n

2.3.76 CFG0_I2C3_HALTEN Registers

2.3.76.1 CFG0_HALTEN Register (Offset = 450h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-269. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0450h

Figure 2-133. I2C3_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												I2C3_HALTEN_R5FSS11_HALTEN	I2C3_HALTEN_R5FSS0_CORE1_HALTEN	I2C3_HALTEN_R5FSS1_CORE0_HALTEN	I2C3_HALTEN_R5FSS0_CORE0_HALTEN
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 2-270. I2C3_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	I2C3_HALTEN_R5FSS11_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
2	I2C3_HALTEN_R5FSS0_CORE1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
1	I2C3_HALTEN_R5FSS1_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
0	I2C3_HALTEN_R5FSS0_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n

2.3.77 CFG0_RTI0_HALTEN Registers

2.3.77.1 CFG0_HALTEN Register (Offset = 454h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-271. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0454h

Figure 2-134. RTI0_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												RTI0_HALTEN_R5FSS11_HALTEN	RTI0_HALTEN_R5FSS0_CORE1_HALTEN	RTI0_HALTEN_R5FSS1_CORE0_HALTEN	RTI0_HALTEN_R5FSS0_CORE0_HALTEN
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 2-272. RTI0_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	RTI0_HALTEN_R5FSS11_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
2	RTI0_HALTEN_R5FSS0_CORE1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
1	RTI0_HALTEN_R5FSS1_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
0	RTI0_HALTEN_R5FSS0_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n

2.3.78 CFG0_RTI1_HALTEN Registers

2.3.78.1 CFG0_HALTEN Register (Offset = 458h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-273. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0458h

Figure 2-135. RTI1_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												RTI1_HALTEN_R5FSS11_HALTEN	RTI1_HALTEN_R5FSS0_CORE1_HALTEN	RTI1_HALTEN_R5FSS1_CORE0_HALTEN	RTI1_HALTEN_R5FSS0_CORE0_HALTEN
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 2-274. RTI1_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	RTI1_HALTEN_R5FSS11_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
2	RTI1_HALTEN_R5FSS0_CORE1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
1	RTI1_HALTEN_R5FSS1_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
0	RTI1_HALTEN_R5FSS0_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n

2.3.79 CFG0_RTI2_HALTEN Registers

2.3.79.1 CFG0_HALTEN Register (Offset = 45Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-275. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 045Ch

Figure 2-136. RTI2_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												RTI2_HALTEN_R5FSS11_HALTEN	RTI2_HALTEN_R5FSS0_CORE1_HALTEN	RTI2_HALTEN_R5FSS1_CORE0_HALTEN	RTI2_HALTEN_R5FSS0_CORE0_HALTEN
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 2-276. RTI2_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	RTI2_HALTEN_R5FSS11_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
2	RTI2_HALTEN_R5FSS0_CORE1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
1	RTI2_HALTEN_R5FSS1_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
0	RTI2_HALTEN_R5FSS0_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n

2.3.80 CFG0_RTI3_HALTEN Registers

2.3.80.1 CFG0_HALTEN Register (Offset = 460h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-277. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0460h

Figure 2-137. RTI3_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												RTI3_HALTEN_R5FSS11_HALTEN	RTI3_HALTEN_R5FSS0_CORE1_HALTEN	RTI3_HALTEN_R5FSS1_CORE0_HALTEN	RTI3_HALTEN_R5FSS0_CORE0_HALTEN
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 2-278. RTI3_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	RTI3_HALTEN_R5FSS11_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
2	RTI3_HALTEN_R5FSS0_CORE1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
1	RTI3_HALTEN_R5FSS1_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
0	RTI3_HALTEN_R5FSS0_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n

2.3.81 CFG0_CPSW_HALTEN Registers

2.3.81.1 CFG0_HALTEN Register (Offset = 474h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-279. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0474h

Figure 2-138. CPSW_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												CPSW_HALTEN_R5FSS11_HALTEN	CPSW_HALTEN_R5FSS0_CORE1_HALTEN	CPSW_HALTEN_R5FSS1_CORE0_HALTEN	CPSW_HALTEN_R5FSS0_CORE0_HALTEN
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 2-280. CPSW_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	CPSW_HALTEN_R5FSS11_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
2	CPSW_HALTEN_R5FSS0_CORE1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
1	CPSW_HALTEN_R5FSS1_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
0	CPSW_HALTEN_R5FSS0_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n

2.3.82 CFG0_MCRC0_HALTEN Registers

2.3.82.1 CFG0_HALTEN Register (Offset = 478h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-281. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0478h

Figure 2-139. MCRC0_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												CRC_HALTEN_R5FSS11_HALTEN	CRC_HALTEN_R5FSS0_CORE1_HALTEN	CRC_HALTEN_R5FSS1_CORE0_HALTEN	CRC_HALTEN_R5FSS0_CORE0_HALTEN
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 2-282. MCRC0_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	CRC_HALTEN_R5FSS11_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
2	CRC_HALTEN_R5FSS0_CORE1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
1	CRC_HALTEN_R5FSS1_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n
0	CRC_HALTEN_R5FSS0_CORE0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: mod_g_rst_n

2.3.83 CFG0_TPTC_DBS_CONFIG Registers

2.3.83.1 CFG0_DBS_CONFIG Register (Offset = 800h) [reset = 11h]

Short Description:

Long Description:

Return to Summary Table

Table 2-283. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0800h

Figure 2-140. TPTC_DBS_CONFIG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
3e8															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										TPTC_DBS_CONFIG_TPTC_A1		RESERVED		TPTC_DBS_CONFIG_TPTC_A0	
NONE										R/W		NONE		R/W	
3e8										1h		0		1h	

Access Types Legend

Table 2-284. TPTC_DBS_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE		Reserved
5:4	TPTC_DBS_CONFIG_TPTC_A1	R/W	1h	Default burst size tieoff value for TPTC_A1 Reset Source: mod_g_rst_n
3:2	RESERVED	NONE		Reserved
1:0	TPTC_DBS_CONFIG_TPTC_A0	R/W	1h	Default burst size tieoff value for TPTC_A0 Reset Source: mod_g_rst_n

2.3.84 CFG0_TPTC_BOUNDARY_CFG Registers

2.3.84.1 CFG0_BOUNDARY_CFG Register (Offset = 804h) [reset = 1313h]

Short Description:

Long Description:

Return to Summary Table

Table 2-285. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0804h

Figure 2-141. TPTC_BOUNDARY_CFG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
174f056369															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		MSS_TPTC_BOUNDARY_CFG_TPTC_A1_SIZE						RESERVED		MSS_TPTC_BOUNDARY_CFG_TPTC_A0_SIZE					
NONE		R/W						NONE		R/W					
174f056369		13h						0		13h					

Access Types Legend

Table 2-286. TPTC_BOUNDARY_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE		Reserved
13:8	MSS_TPTC_BOUNDARY_CFG_TPTC_A1_SIZE	R/W	13h	6 bit signal used for deciding the boundary crossing size for CID-RID-SID reordering of MSS_TPTC_A1 Example: writing 6'd19 decidies boundary to be 2^19 i.e. 512 KB Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5:0	MSS_TPTC_BOUNDARY_CFG_TPTC_A0_SIZE	R/W	13h	6 bit signal used for deciding the boundary crossing size for CID-RID-SID reordering of MSS_TPTC_A0 Example: writing 6'd19 decidies boundary to be 2^19 i.e. 512 KB Reset Source: mod_g_rst_n

2.3.85 CFG0_TPTC_XID_REORDER_CFG Registers

2.3.85.1 CFG0_XID_REORDER_CFG Register (Offset = 808h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-287. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0808h

Figure 2-142. TPTC_XID_REORDER_CFG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							MSS_TPTC_XID_REORDER_CFG_TPTC_A1_DISABLE	RESERVED							MSS_TPTC_XID_REORDER_CFG_TPTC_A0_DISABLE
NONE							R/W	NONE							R/W
0							0h	0							0h

Access Types Legend

Table 2-288. TPTC_XID_REORDER_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE		Reserved
8	MSS_TPTC_XID_REORDER_CFG_TPTC_A1_DISABLE	R/W	0h	writing 1'b1 will disable the CID-RID-SID reodering feature for MSS_TPTC_A1 Reset Source: mod_g_rst_n
7:1	RESERVED	NONE		Reserved
0	MSS_TPTC_XID_REORDER_CFG_TPTC_A0_DISABLE	R/W	0h	writing 1'b1 will disable the CID-RID-SID reodering feature for MSS_TPTC_A0 Reset Source: mod_g_rst_n

2.3.86 CFG0_CPSW_CONTROL Registers

2.3.86.1 CFG0_CONTROL Register (Offset = 810h) [reset = 1000100h]

Short Description:

Long Description:

Return to Summary Table

Table 2-289. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0810h

Figure 2-143. CPSW_CONTROL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							CPSW_CONTROL_RGMII2_ID_MODE	RESERVED	CPSW_CONTROL_RMII2_REF_CLK_SEL	RESERVED	CPSW_CONTROL_RMII2_REF_CLK_OE_N	RESERVED	CPSW_CONTROL_PORT2_MODE_SEL		
NONE							R/W	NONE	R/W	NONE	R/W	NONE	R/W		
0							1h	1	0h	0	0h	0	0h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CPSW_CONTROL_RGMII1_ID_MODE	RESERVED	CPSW_CONTROL_RMII1_REF_CLK_SEL	RESERVED	CPSW_CONTROL_RMII1_REF_CLK_OE_N	RESERVED	CPSW_CONTROL_PORT1_MODE_SEL		
NONE							R/W	NONE	R/W	NONE	R/W	NONE	R/W		
0							1h	1	0h	0	0h	0	0h		

Access Types Legend

Table 2-290. CPSW_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24	CPSW_CONTROL_RGMII2_ID_MODE	R/W	1h	Internal delay mode for port 2. Only for TX 0 : ID mode is disabled 1 : ID mode is enabled Reset Source: mod_g_rst_n
23	RESERVED	NONE		Reserved
22	CPSW_CONTROL_RMII2_REF_CLK_SEL	R/W	0h	To select the rmii_ref_clk loopback mux output either from PAD or from MSS_RCM. Write 0 to get clock will be from IO pad(pad loopback). Write 1 to get clock from internal loopback. Reset Source: mod_g_rst_n
21	RESERVED	NONE		Reserved
20	CPSW_CONTROL_RMII2_REF_CLK_OE_N	R/W	0h	RMII_REF_CLK IO Output enable control 0: Output enable 1: Output Disable Reset Source: mod_g_rst_n
19	RESERVED	NONE		Reserved
18:16	CPSW_CONTROL_PORT2_MODE_SEL	R/W	0h	Port 2 Interface 000 = MII 001 = RMII 010 = RGMII 011 - 111 = Not Supported Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	CPSW_CONTROL_RGMII1_ID_MODE	R/W	1h	Internal delay mode for port 1. Only for TX 0 : ID mode is disabled 1 : ID mode is enabled Reset Source: mod_g_rst_n
7	RESERVED	NONE		Reserved

Table 2-290. CPSW_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CPSW_CONTROL_RMII1_REF_CLK_SEL	R/W	0h	To select the rmii_ref_clk loopback mux output either from PAD or from MSS_RCM. Write 0 to get clock will be from IO pad(pad loopback). Write 1 to get clock from internal source Reset Source: mod_g_rst_n
5	RESERVED	NONE		Reserved
4	CPSW_CONTROL_RMII1_REF_CLK_OE_N	R/W	0h	RMII_REF_CLK IO Output enable control 0: Output enable 1: Output Disable Reset Source: mod_g_rst_n
3	RESERVED	NONE		Reserved
2:0	CPSW_CONTROL_PORT1_MODE_SEL	R/W	0h	Port 1 Interface 000 = MII 001 = RMII 010 = RGMII 011 - 111 = Not Supported Reset Source: mod_g_rst_n

2.3.87 CFG0_QSPI_CONFIG Registers

2.3.87.1 CFG0_CONFIG Register (Offset = 814h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-291. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0814h

Figure 2-144. QSPI_CONFIG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_QSPI_CONFIG_EXT_CLK		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-292. QSPI_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_QSPI_CONFIG_EXT_CLK	R/W	0h	Write 3'b111 to external clock as QSPI baud clock source needed for DFT IO char. Reset Source: mod_g_rst_n

2.3.88 CFG0_ICSSM_IDLE_CONTROL Registers

2.3.88.1 CFG0_IDLE_CONTROL Register (Offset = 818h) [reset = 1h]

Short Description:

Long Description:

Return to Summary Table

Table 2-293. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0818h

Figure 2-145. ICSSM_IDLE_CONTROL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															GLOBAL_CONTROLS_NOGATE
NONE															R/W
0															1h

Access Types Legend

Table 2-294. ICSSM_IDLE_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	GLOBAL_CONTROLS_NOGATE	R/W	1h	Writing 1'b0 will enable local auto-clock gating (lower power) at IP level with increase in access/functional latency. Following IPs are controlled with this signal ICSSM Reset Source: mod_g_rst_n

2.3.89 CFG0_PRU-ICSS_PRU0_GPI_SEL Registers

2.3.89.1 CFG0_PRU0_GPI_SEL Register (Offset = 81Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-295. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 081Ch

Figure 2-146. PRU-ICSS_PRU0_GPI_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		PRU-ICSS_PRU0_GPI_SEL_SEL													
NONE		R/W													
0		0h													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRU-ICSS_PRU0_GPI_SEL_SEL															
R/W															
0h															

Access Types Legend

Table 2-296. PRU-ICSS_PRU0_GPI_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE		Reserved
29:0	PRU-ICSS_PRU0_GPI_SEL_SEL	R/W	0h	GPI or PWMXBar select for ICSM Port0 0: GPI 1: PWMXBAR Reset Source: mod_g_rst_n

2.3.90 CFG0_PRU-ICSS_PRU1_GPI_SEL Registers

2.3.90.1 CFG0_PRU1_GPI_SEL Register (Offset = 820h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-297. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0820h

Figure 2-147. PRU-ICSS_PRU1_GPI_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		PRU-ICSS_PRU1_GPI_SEL_SEL													
NONE		R/W													
0		0h													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRU-ICSS_PRU1_GPI_SEL_SEL															
R/W															
0h															

Access Types Legend

Table 2-298. PRU-ICSS_PRU1_GPI_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE		Reserved
29:0	PRU-ICSS_PRU1_GPI_SEL_SEL	R/W	0h	GPI or PWMXBar select for ICSM Port0 0: GPI 1: PWMXBAR Reset Source: mod_g_rst_n

2.3.91 CFG0_PRU-ICSS_PRU0_GPIO_OUT_CTRL Registers

2.3.91.1 CFG0_PRU0_GPIO_OUT_CTRL Register (Offset = 824h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-299. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0824h

Figure 2-148. PRU-ICSS_PRU0_GPIO_OUT_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		PRU-ICSS_PRU0_GPIO_OUT_CTRL_OUTDISABLE													
NONE		R/W													
0		0h													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRU-ICSS_PRU0_GPIO_OUT_CTRL_OUTDISABLE															
R/W															
0h															

Access Types Legend

Table 2-300. PRU-ICSS_PRU0_GPIO_OUT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE		Reserved
29:0	PRU-ICSS_PRU0_GPIO_OUT_CTRL_OUTDISABLE	R/W	0h	GPO output disable for ICSSM Port 0 IO. Disable output for using the pin as input. Each Bit maps to the corresponding bit in the IO 0: Output Enable 1: Output Disable Reset Source: mod_g_rst_n

2.3.92 CFG0_PRU-ICSS_PRU1_GPIO_OUT_CTRL Registers

2.3.92.1 CFG0_PRU1_GPIO_OUT_CTRL Register (Offset = 828h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-301. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0828h

Figure 2-149. PRU-ICSS_PRU1_GPIO_OUT_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		PRU-ICSS_PRU1_GPIO_OUT_CTRL_OUTDISABLE													
NONE		R/W													
0		0h													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRU-ICSS_PRU1_GPIO_OUT_CTRL_OUTDISABLE															
R/W															
0h															

Access Types Legend

Table 2-302. PRU-ICSS_PRU1_GPIO_OUT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE		Reserved
29:0	PRU-ICSS_PRU1_GPIO_OUT_CTRL_OUTDISABLE	R/W	0h	GPO output disable for ICSSM Port 1 IO. Disable output for using the pin as input. Each Bit maps to the corresponding bit in the IO 0: Output Enable 1: Output Disable Reset Source: mod_g_rst_n

2.3.93 CFG0_GPMC_CONTROL Registers

2.3.93.1 CFG0_CONTROL Register (Offset = 82Ch) [reset = 100h]

Short Description:

Long Description:

Return to Summary Table

Table 2-303. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 082Ch

Figure 2-150. GPMC_CONTROL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
989680															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			GPMC_CONTROL_CLK_LB_OE_N	RESERVED			GPMC_CONTROL_CLK_OE_N	RESERVED			GPMC_CONTROL_CLK_LB_SEL	RESERVED			GPMC_CONTROL_CLKOUT_SEL
NONE			R/W	NONE			R/W	NONE			R/W	NONE			R/W
989680			0h	0			1h	0			0h	0			0h

Access Types Legend

Table 2-304. GPMC_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE		Reserved
12	GPMC_CONTROL_CLK_LB_OE_N	R/W	0h	GPMC_CLK_LB oe_n 1: GPMC_dev_clk is driven to pad 0: GPMC_dev_clk is not driven to pad Reset Source: mod_g_rst_n
11:9	RESERVED	NONE		Reserved
8	GPMC_CONTROL_CLK_OE_N	R/W	1h	GPMC_CLKOUT oe_n 1: GPMC_dev_clk mux output is driven to pad 0: GPMC_dev_clk mux output is not driven to pad Reset Source: mod_g_rst_n
7:5	RESERVED	NONE		Reserved
4	GPMC_CONTROL_CLK_LB_SEL	R/W	0h	GPMC_CLK_LB sel 0: GPMC_CLK_LB pad clock 1: GPMC_CLK pad clock Reset Source: mod_g_rst_n
3:1	RESERVED	NONE		Reserved
0	GPMC_CONTROL_CLKOUT_SEL	R/W	0h	GPMC_CLKOUT sel 0: GPMC_func_clock 1: GPMC_dev clock Reset Source: mod_g_rst_n

2.3.94 CFG0_TPCC0_INTAGG_MASK Registers

2.3.94.1 CFG0_INTAGG_MASK Register (Offset = 830h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-305. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0830h

Figure 2-151. TPCC0_INTAGG_MASK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														MSS_TPCC_A_INTAGG_MASK_TPTC_A1	MSS_TPCC_A_INTAGG_MASK_TPTC_A0
NONE														R/W	R/W
0														0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							MSS_TPCC_A_INTAGG_MASK_TPCC_A_INT7	MSS_TPCC_A_INTAGG_MASK_TPCC_A_INT6	MSS_TPCC_A_INTAGG_MASK_TPCC_A_INT5	MSS_TPCC_A_INTAGG_MASK_TPCC_A_INT4	MSS_TPCC_A_INTAGG_MASK_TPCC_A_INT3	MSS_TPCC_A_INTAGG_MASK_TPCC_A_INT2	MSS_TPCC_A_INTAGG_MASK_TPCC_A_INT1	MSS_TPCC_A_INTAGG_MASK_TPCC_A_INTG	
NONE							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0							0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-306. TPCC0_INTAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE		Reserved
17	MSS_TPCC_A_INTAGG_MASK_TPTC_A1	R/W	0h	Mask Interrupt from TPTC A1 to aggregated Interrupt MSS_TPCC_A_INTAGG 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
16	MSS_TPCC_A_INTAGG_MASK_TPTC_A0	R/W	0h	Mask Interrupt from TPTC A0 to aggregated Interrupt MSS_TPCC_A_INTAGG 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	MSS_TPCC_A_INTAGG_MASK_TPCC_A_INT7	R/W	0h	Mask Interrupt from MSS_TPCC_A to aggregated Interrupt MSS_TPCC_A_INTAGG 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
7	MSS_TPCC_A_INTAGG_MASK_TPCC_A_INT6	R/W	0h	Mask Interrupt from MSS_TPCC_A to aggregated Interrupt MSS_TPCC_A_INTAGG 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
6	MSS_TPCC_A_INTAGG_MASK_TPCC_A_INT5	R/W	0h	Mask Interrupt from MSS_TPCC_A to aggregated Interrupt MSS_TPCC_A_INTAGG 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
5	MSS_TPCC_A_INTAGG_MASK_TPCC_A_INT4	R/W	0h	Mask Interrupt from MSS_TPCC_A to aggregated Interrupt MSS_TPCC_A_INTAGG 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n

Table 2-306. TPCC0_INTAGG_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	MSS_TPCC_A_INTAGG_MASK_TPCC_A_INT3	R/W	0h	Mask Interrupt from MSS_TPCC_A to aggregated Interrupt MSS_TPCC_A_INTAGG 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
3	MSS_TPCC_A_INTAGG_MASK_TPCC_A_INT2	R/W	0h	Mask Interrupt from MSS_TPCC_A to aggregated Interrupt MSS_TPCC_A_INTAGG 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
2	MSS_TPCC_A_INTAGG_MASK_TPCC_A_INT1	R/W	0h	Mask Interrupt from MSS_TPCC_A to aggregated Interrupt MSS_TPCC_A_INTAGG 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
1	MSS_TPCC_A_INTAGG_MASK_TPCC_A_INT0	R/W	0h	Mask Interrupt from TPCC A to aggregated Interrupt MSS_TPCC_A_INTAGG 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
0	MSS_TPCC_A_INTAGG_MASK_TPCC_A_INTG	R/W	0h	Mask Interrupt from MSS_TPCC_A to aggregated Interrupt MSS_TPCC_A_INTAGG 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n

2.3.95 CFG0_TPCC0_INTAGG_STATUS Registers

2.3.95.1 CFG0_INTAGG_STATUS Register (Offset = 834h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-307. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0834h

Figure 2-152. TPCC0_INTAGG_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														MSS_TPCC_A_INTAGG_STATUS_TPTC_A1	MSS_TPCC_A_INTAGG_STATUS_TPTC_A0
NONE														R/W1TC	R/W1TC
0														0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							MSS_TPCC_A_INTAGG_STATUS_TPCC_A_INT7	MSS_TPCC_A_INTAGG_STATUS_TPCC_A_INT6	MSS_TPCC_A_INTAGG_STATUS_TPCC_A_INT5	MSS_TPCC_A_INTAGG_STATUS_TPCC_A_INT4	MSS_TPCC_A_INTAGG_STATUS_TPCC_A_INT3	MSS_TPCC_A_INTAGG_STATUS_TPCC_A_INT2	MSS_TPCC_A_INTAGG_STATUS_TPCC_A_INT1	MSS_TPCC_A_INTAGG_STATUS_TPCC_A_INT0	MSS_TPCC_A_INTAGG_STATUS_TPCC_A_INTG
NONE							R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0							0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-308. TPCC0_INTAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE		Reserved
17	MSS_TPCC_A_INTAGG_STATUS_TPTC_A1	R/W1TC	0h	Status of Interrupt from TPTC A1. Set only if Interupt is unmasked in MSS_TPCC_A_INTAGG_MASK Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
16	MSS_TPCC_A_INTAGG_STATUS_TPTC_A0	R/W1TC	0h	Status of Interrupt from TPTC A0. Set only if Interupt is unmasked in MSS_TPCC_A_INTAGG_MASK Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	MSS_TPCC_A_INTAGG_STATUS_TPCC_A_INT7	R/W1TC	0h	Status of Interrupt from MSS_TPCC_A. Set only if Interupt is unmasked in MSS_TPCC_A_INTAGG_MASK Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
7	MSS_TPCC_A_INTAGG_STATUS_TPCC_A_INT6	R/W1TC	0h	Status of Interrupt from MSS_TPCC_A. Set only if Interupt is unmasked in MSS_TPCC_A_INTAGG_MASK Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
6	MSS_TPCC_A_INTAGG_STATUS_TPCC_A_INT5	R/W1TC	0h	Status of Interrupt from MSS_TPCC_A. Set only if Interupt is unmasked in MSS_TPCC_A_INTAGG_MASK Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

Table 2-308. TPCC0_INTAGG_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MSS_TPCC_A_INTAGG_STATUS_TPCC_A_INT4	R/W1TC	0h	Status of Interrupt from MSS_TPCC_A. Set only if Interupt is unmasked in MSS_TPCC_A_INTAGG_MASK Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
4	MSS_TPCC_A_INTAGG_STATUS_TPCC_A_INT3	R/W1TC	0h	Status of Interrupt from MSS_TPCC_A. Set only if Interupt is unmasked in MSS_TPCC_A_INTAGG_MASK Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
3	MSS_TPCC_A_INTAGG_STATUS_TPCC_A_INT2	R/W1TC	0h	Status of Interrupt from MSS_TPCC_A. Set only if Interupt is unmasked in MSS_TPCC_A_INTAGG_MASK Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
2	MSS_TPCC_A_INTAGG_STATUS_TPCC_A_INT1	R/W1TC	0h	Status of Interrupt from MSS_TPCC_A. Set only if Interupt is unmasked in MSS_TPCC_A_INTAGG_MASK Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
1	MSS_TPCC_A_INTAGG_STATUS_TPCC_A_INT0	R/W1TC	0h	Status of Interrupt from TPCC A Set only if Interupt is unmasked in MSS_TPCC_A_INTAGG_MASK Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
0	MSS_TPCC_A_INTAGG_STATUS_TPCC_A_INTG	R/W1TC	0h	Status of Interrupt from MSS_TPCC_A. Set only if Interupt is unmasked in MSS_TPCC_A_INTAGG_MASK Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

2.3.96 CFG0_TPCC0_INTAGG_STATUS_RAW Registers

2.3.96.1 CFG0_INTAGG_STATUS_RAW Register (Offset = 838h) [reset = 0h]

Short Description:

Long Description:

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Table 2-309. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 0838h

Figure 2-153. TPCC0_INTAGG_STATUS_RAW Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														MSS_TPCC_A_INTAGG_STATUS_RAW_TPTC_A1	MSS_TPCC_A_INTAGG_STATUS_RAW_TPTC_A0
NONE														R/W1TC	R/W1TC
0														0h	0h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							MSS_TPCC_A_INTAGG_STATUS_RAW_TPCC_A_INT7	MSS_TPCC_A_INTAGG_STATUS_RAW_TPCC_A_INT6	MSS_TPCC_A_INTAGG_STATUS_RAW_TPCC_A_INT5	MSS_TPCC_A_INTAGG_STATUS_RAW_TPCC_A_INT4	MSS_TPCC_A_INTAGG_STATUS_RAW_TPCC_A_INT3	MSS_TPCC_A_INTAGG_STATUS_RAW_TPCC_A_INT2	MSS_TPCC_A_INTAGG_STATUS_RAW_TPCC_A_INT1	MSS_TPCC_A_INTAGG_STATUS_RAW_TPCC_A_INT0	MSS_TPCC_A_INTAGG_STATUS_RAW_TPCC_A_INTG
NONE							R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0							0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-310. TPCC0_INTAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE		Reserved
17	MSS_TPCC_A_INTAGG_STATUS_RAW_TPTC_A1	R/W1TC	0h	Raw Status of Interrupt from TPTC A1. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_A_INTAGG_MASK Reset Source: mod_g_rst_n
16	MSS_TPCC_A_INTAGG_STATUS_RAW_TPTC_A0	R/W1TC	0h	Raw Status of Interrupt from TPTC A0. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_A_INTAGG_MASK Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	MSS_TPCC_A_INTAGG_STATUS_RAW_TPCC_A_INT7	R/W1TC	0h	Raw Status of Interrupt from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_C_INTAGG_MASK Reset Source: mod_g_rst_n
7	MSS_TPCC_A_INTAGG_STATUS_RAW_TPCC_A_INT6	R/W1TC	0h	Raw Status of Interrupt from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_C_INTAGG_MASK Reset Source: mod_g_rst_n

Table 2-310. TPCC0_INTAGG_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	MSS_TPCC_A_INTAGG_STATUS_RAW_TPCC_A_INT5	R/W1TC	0h	Raw Status of Interrupt from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_C_INTAGG_MASK Reset Source: mod_g_rst_n
5	MSS_TPCC_A_INTAGG_STATUS_RAW_TPCC_A_INT4	R/W1TC	0h	Raw Status of Interrupt from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_C_INTAGG_MASK Reset Source: mod_g_rst_n
4	MSS_TPCC_A_INTAGG_STATUS_RAW_TPCC_A_INT3	R/W1TC	0h	Raw Status of Interrupt from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_C_INTAGG_MASK Reset Source: mod_g_rst_n
3	MSS_TPCC_A_INTAGG_STATUS_RAW_TPCC_A_INT2	R/W1TC	0h	Raw Status of Interrupt from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_C_INTAGG_MASK Reset Source: mod_g_rst_n
2	MSS_TPCC_A_INTAGG_STATUS_RAW_TPCC_A_INT1	R/W1TC	0h	Raw Status of Interrupt from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_C_INTAGG_MASK Reset Source: mod_g_rst_n
1	MSS_TPCC_A_INTAGG_STATUS_RAW_TPCC_A_INT0	R/W1TC	0h	Raw Status of Interrupt from TPCC A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_A_INTAGG_MASK Reset Source: mod_g_rst_n
0	MSS_TPCC_A_INTAGG_STATUS_RAW_TPCC_A_INTG	R/W1TC	0h	Raw Status of Interrupt from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_C_INTAGG_MASK Reset Source: mod_g_rst_n

2.3.97 CFG0_LOCK0_KICK0 Registers

2.3.97.1 CFG0_KICK0 Register (Offset = 1008h) [reset = 0h]

Short Description: - KICK0 component

Long Description: - KICK0 component

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Table 2-311. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 1008h

Figure 2-154. LOCK0_KICK0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LOCK0_KICK0															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCK0_KICK0															
R/W															
0h															

Access Types Legend

Table 2-312. LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

2.3.98 CFG0_LOCK0_KICK1 Registers

2.3.98.1 CFG0_KICK1 Register (Offset = 100Ch) [reset = 0h]

Short Description: - KICK1 component

Long Description: - KICK1 component

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Table 2-313. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 100Ch

Figure 2-155. LOCK0_KICK1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LOCK0_KICK1															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCK0_KICK1															
R/W															
0h															

Access Types Legend

Table 2-314. LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

2.3.99 CFG0_INTR_RAW_STATUS Registers

2.3.99.1 CFG0_RAW_STATUS Register (Offset = 1010h) [reset = 0h]

Short Description: Interrupt Raw Status/Set Register

Long Description: Interrupt Raw Status/Set Register

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Table 2-315. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 1010h

Figure 2-156. INTR_RAW_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												PROXY_ERR	KICK_ERR	ADDR_ERR	PROT_ERR
NONE												R/W1TS	R/W1TS	R/W1TS	R/W1TS
0												0h	0h	0h	0h

Access Types Legend

Table 2-316. INTR_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	PROXY_ERR	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

2.3.100 CFG0_INTR_ENABLED_STATUS_CLEAR Registers

2.3.100.1 CFG0_ENABLED_STATUS_CLEAR Register (Offset = 1014h) [reset = 0h]

Short Description: Interrupt Enabled Status/Clear register

Long Description: Interrupt Enabled Status/Clear register

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Table 2-317. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 1014h

Figure 2-157. INTR_ENABLED_STATUS_CLEAR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												ENABLED_PROXY_ERR	ENABLED_KICK_ERR	ENABLED_ADDR_ERR	ENABLED_PROT_ERR
NONE												R/W1TC	R/W1TC	R/W1TC	R/W1TC
0												0h	0h	0h	0h

Access Types Legend

Table 2-318. INTR_ENABLED_STATUS_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	ENABLED_PROXY_ERR	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	ENABLED_KICK_ERR	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ENABLED_ADDR_ERR	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	ENABLED_PROT_ERR	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

2.3.101 CFG0_INTR_ENABLE Registers

2.3.101.1 CFG0_ENABLE Register (Offset = 1018h) [reset = 0h]

Short Description: Interrupt Enable register

Long Description: Interrupt Enable register

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Table 2-319. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 1018h

Figure 2-158. INTR_ENABLE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												PROXY_ERR_EN	KICK_ERR_EN	ADDR_ERR_EN	PROT_ERR_EN
NONE												R/W1TS	R/W1TS	R/W1TS	R/W1TS
0												0h	0h	0h	0h

Access Types Legend

Table 2-320. INTR_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	PROXY_ERR_EN	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

2.3.102 CFG0_INTR_ENABLE_CLEAR Registers

2.3.102.1 CFG0_ENABLE_CLEAR Register (Offset = 101Ch) [reset = 0h]

Short Description: Interrupt Enable Clear register

Long Description: Interrupt Enable Clear register

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Table 2-321. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 101Ch

Figure 2-159. INTR_ENABLE_CLEAR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												PROXY_ERR_EN_CLR	KICK_ERR_EN_CLR	ADDR_ERR_EN_CLR	PROT_ERR_EN_CLR
NONE												R/W1TC	R/W1TC	R/W1TC	R/W1TC
0												0h	0h	0h	0h

Access Types Legend

Table 2-322. INTR_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	PROXY_ERR_EN_CLR	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_CLR	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_CLR	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_CLR	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

2.3.103 CFG0_EOI Registers

2.3.103.1 CFG0_EOI Register (Offset = 1020h) [reset = 0h]

Short Description: EOI register

Long Description: EOI register

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Table 2-323. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 1020h

Figure 2-160. EOI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								EOI_VECTOR							
NONE								R/W							
0								0h							

Access Types Legend

Table 2-324. EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	EOI_VECTOR	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip. Reset Source: mod_g_rst_n

2.3.104 CFG0_FAULT_ADDRESS Registers

2.3.104.1 CFG0_ADDRESS Register (Offset = 1024h) [reset = 0h]

Short Description: Fault Address register

Long Description: Fault Address register

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Table 2-325. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 1024h

Figure 2-161. FAULT_ADDRESS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FAULT_ADDR															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FAULT_ADDR															
R															
0h															

Access Types Legend

Table 2-326. FAULT_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR	R	0h	Fault Address. Reset Source: mod_g_rst_n

2.3.105 CFG0_FAULT_TYPE_STATUS Registers

2.3.105.1 CFG0_TYPE_STATUS Register (Offset = 1028h) [reset = 0h]

Short Description: Fault Type Status register

Long Description: Fault Type Status register

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Table 2-327. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 1028h

Figure 2-162. FAULT_TYPE_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									FAULT_NS	FAULT_TYPE					
NONE									R	R					
0									0h	0h					

Access Types Legend

Table 2-328. FAULT_TYPE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE		Reserved
6	FAULT_NS	R	0h	Non-secure access. Reset Source: mod_g_rst_n
5:0	FAULT_TYPE	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype ! = 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault Reset Source: mod_g_rst_n

2.3.106 CFG0_FAULT_ATTR_STATUS Registers

2.3.106.1 CFG0_ATTR_STATUS Register (Offset = 102Ch) [reset = 0h]

Short Description: Fault Attribute Status register

Long Description: Fault Attribute Status register

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Table 2-329. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 102Ch

Figure 2-163. FAULT_ATTR_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FAULT_XID												FAULT_ROUTEID			
R												R			
0h												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FAULT_ROUTEID								FAULT_PRIVID							
R								R							
0h								0h							

Access Types Legend

Table 2-330. FAULT_ATTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID	R	0h	XID. Reset Source: mod_g_rst_n
19:8	FAULT_ROUTEID	R	0h	Route ID. Reset Source: mod_g_rst_n
7:0	FAULT_PRIVID	R	0h	Privilege ID. Reset Source: mod_g_rst_n

2.3.107 CFG0_FAULT_CLEAR Registers

2.3.107.1 CFG0_CLEAR Register (Offset = 1030h) [reset = 0h]

Short Description: Fault Clear register

Long Description: Fault Clear register

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Table 2-331. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 1030h

Figure 2-164. FAULT_CLEAR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															FAULT_CLR
NONE															W
0															0h

Access Types Legend

Table 2-332. FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	FAULT_CLR	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. Reset Source: mod_g_rst_n

2.3.108 CFG0_R5SS0_CORE0_MBOX_WRITE_DONE Registers

2.3.108.1 CFG0_CORE0_MBOX_WRITE_DONE Register (Offset = 4000h) [reset = 0h]

Short Description:

Long Description:

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Table 2-333. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 4000h

Figure 2-165. R5SS0_CORE0_MBOX_WRITE_DONE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			MSS_R5FSS0_CORE0_MBOX_WRITE_DONE_PROC_7	RESERVED			MSS_R5FSS0_CORE0_MBOX_WRITE_DONE_PROC_6	RESERVED			MSS_R5FSS0_CORE0_MBOX_WRITE_DONE_PROC_5	RESERVED			MSS_R5FSS0_CORE0_MBOX_WRITE_DONE_PROC_4
NONE			R/W	NONE			R/W	NONE			R/W	NONE			R/W
0			0h	0			0h	0			0h	0			0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			MSS_R5FSS0_CORE0_MBOX_WRITE_DONE_PROC_3	RESERVED			MSS_R5FSS0_CORE0_MBOX_WRITE_DONE_PROC_2	RESERVED			MSS_R5FSS0_CORE0_MBOX_WRITE_DONE_PROC_1	RESERVED			MSS_R5FSS0_CORE0_MBOX_WRITE_DONE_PROC_0
NONE			R/W	NONE			R/W	NONE			R/W	NONE			R/W
0			0h	0			0h	0			0h	0			0h

Access Types Legend

Table 2-334. R5SS0_CORE0_MBOX_WRITE_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28	MSS_R5FSS0_CORE0_MBOX_WRITE_DONE_PROC_7	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 7 Reset Source: mod_g_rst_n
27:25	RESERVED	NONE		Reserved
24	MSS_R5FSS0_CORE0_MBOX_WRITE_DONE_PROC_6	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 6 Reset Source: mod_g_rst_n
23:21	RESERVED	NONE		Reserved
20	MSS_R5FSS0_CORE0_MBOX_WRITE_DONE_PROC_5	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 5 Reset Source: mod_g_rst_n
19:17	RESERVED	NONE		Reserved
16	MSS_R5FSS0_CORE0_MBOX_WRITE_DONE_PROC_4	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 4 Reset Source: mod_g_rst_n

Table 2-334. R5SS0_CORE0_MBOX_WRITE_DONE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:13	RESERVED	NONE		Reserved
12	MSS_R5FSS0_CORE0_MBOX_WRITE_DONE_PROC_3	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 3 Reset Source: mod_g_rst_n
11:9	RESERVED	NONE		Reserved
8	MSS_R5FSS0_CORE0_MBOX_WRITE_DONE_PROC_2	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 2 Reset Source: mod_g_rst_n
7:5	RESERVED	NONE		Reserved
4	MSS_R5FSS0_CORE0_MBOX_WRITE_DONE_PROC_1	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 1 Reset Source: mod_g_rst_n
3:1	RESERVED	NONE		Reserved
0	MSS_R5FSS0_CORE0_MBOX_WRITE_DONE_PROC_0	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 0 Reset Source: mod_g_rst_n

2.3.109 CFG0_R5SS0_CORE0_MBOX_READ_REQ Registers

2.3.109.1 CFG0_CORE0_MBOX_READ_REQ Register (Offset = 4004h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-335. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 4004h

Figure 2-166. R5SS0_CORE0_MBOX_READ_REQ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			MSS_R5FSS0_CORE0_MBOX_READ_REQ_PROC_7	RESERVED			MSS_R5FSS0_CORE0_MBOX_READ_REQ_PROC_6	RESERVED			MSS_R5FSS0_CORE0_MBOX_READ_REQ_PROC_5	RESERVED			MSS_R5FSS0_CORE0_MBOX_READ_REQ_PROC_4
NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC
0			0h	0			0h	0			0h	0			0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			MSS_R5FSS0_CORE0_MBOX_READ_REQ_PROC_3	RESERVED			MSS_R5FSS0_CORE0_MBOX_READ_REQ_PROC_2	RESERVED			MSS_R5FSS0_CORE0_MBOX_READ_REQ_PROC_1	RESERVED			MSS_R5FSS0_CORE0_MBOX_READ_REQ_PROC_0
NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC
0			0h	0			0h	0			0h	0			0h

Access Types Legend

Table 2-336. R5SS0_CORE0_MBOX_READ_REQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28	MSS_R5FSS0_CORE0_MBOX_READ_REQ_PROC_7	R/W1TC	0h	This is request from processor 7 to mss_cr5a. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
27:25	RESERVED	NONE		Reserved
24	MSS_R5FSS0_CORE0_MBOX_READ_REQ_PROC_6	R/W1TC	0h	This is request from processor 6 to mss_cr5a. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
23:21	RESERVED	NONE		Reserved
20	MSS_R5FSS0_CORE0_MBOX_READ_REQ_PROC_5	R/W1TC	0h	This is request from processor 5 to mss_cr5a. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
19:17	RESERVED	NONE		Reserved
16	MSS_R5FSS0_CORE0_MBOX_READ_REQ_PROC_4	R/W1TC	0h	This is request from processor 4 to mss_cr5a. Requesting it to read from mailbox. Reset Source: mod_g_rst_n

Table 2-336. R5SS0_CORE0_MBOX_READ_REQ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:13	RESERVED	NONE		Reserved
12	MSS_R5FSS0_CORE0_MBOX_READ_REQ_PROC_3	R/W1TC	0h	This is request from processor 3 to mss_cr5a. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
11:9	RESERVED	NONE		Reserved
8	MSS_R5FSS0_CORE0_MBOX_READ_REQ_PROC_2	R/W1TC	0h	This is request from processor 2 to mss_cr5a. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
7:5	RESERVED	NONE		Reserved
4	MSS_R5FSS0_CORE0_MBOX_READ_REQ_PROC_1	R/W1TC	0h	This is request from processor 1 to mss_cr5a. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
3:1	RESERVED	NONE		Reserved
0	MSS_R5FSS0_CORE0_MBOX_READ_REQ_PROC_0	R/W1TC	0h	This is request from processor 0 to mss_cr5a. Requesting it to read from mailbox. Reset Source: mod_g_rst_n

2.3.110 CFG0_R5SS0_CORE0_MBOX_READ_DONE_ACK Registers

2.3.110.1 CFG0_CORE0_MBOX_READ_DONE_ACK Register (Offset = 4008h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-337. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 4008h

Figure 2-167. R5SS0_CORE0_MBOX_READ_DONE_ACK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MSS_R5FSS0_CORE0_MBOX_READ_DONE_ACK_PROC							
NONE								R/W							
0								0h							

Access Types Legend

Table 2-338. R5SS0_CORE0_MBOX_READ_DONE_ACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	MSS_R5FSS0_CORE0_MBOX_READ_DONE_ACK_PROC	R/W	0h	Write pulse bit field: For bits 0 to 7: Wrting 1'b1 : Generates pulse interrupt to corresponding proc from MSS_CR5 Reset Source: mod_g_rst_n

2.3.111 CFG0_R5SS0_CORE0_MBOX_READ_DONE Registers

2.3.111.1 CFG0_CORE0_MBOX_READ_DONE Register (Offset = 400Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-339. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 400Ch

Figure 2-168. R5SS0_CORE0_MBOX_READ_DONE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			MSS_R5FSS0_CORE0_MBOX_READ_DONE_PROC_7	RESERVED			MSS_R5FSS0_CORE0_MBOX_READ_DONE_PROC_6	RESERVED			MSS_R5FSS0_CORE0_MBOX_READ_DONE_PROC_5	RESERVED			MSS_R5FSS0_CORE0_MBOX_READ_DONE_PROC_4
NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC
0			0h	0			0h	0			0h	0			0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			MSS_R5FSS0_CORE0_MBOX_READ_DONE_PROC_3	RESERVED			MSS_R5FSS0_CORE0_MBOX_READ_DONE_PROC_2	RESERVED			MSS_R5FSS0_CORE0_MBOX_READ_DONE_PROC_1	RESERVED			MSS_R5FSS0_CORE0_MBOX_READ_DONE_PROC_0
NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC
0			0h	0			0h	0			0h	0			0h

Access Types Legend

Table 2-340. R5SS0_CORE0_MBOX_READ_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28	MSS_R5FSS0_CORE0_MBOX_READ_DONE_PROC_7	R/W1TC	0h	This register should be written once finishing reading from CR5A's mailbox written by proc 7 Reset Source: mod_g_rst_n
27:25	RESERVED	NONE		Reserved
24	MSS_R5FSS0_CORE0_MBOX_READ_DONE_PROC_6	R/W1TC	0h	This register should be written once finishing reading from CR5A's mailbox written by proc 6 Reset Source: mod_g_rst_n
23:21	RESERVED	NONE		Reserved
20	MSS_R5FSS0_CORE0_MBOX_READ_DONE_PROC_5	R/W1TC	0h	This register should be written once finishing reading from CR5A's mailbox written by proc 5 Reset Source: mod_g_rst_n
19:17	RESERVED	NONE		Reserved

Table 2-340. R5SS0_CORE0_MBOX_READ_DONE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	MSS_R5FSS0_CORE0_MBOX_READ_DONE_PROC_4	R/W1TC	0h	This register should be written once finishing reading from CR5A's mailbox written by proc 4 Reset Source: mod_g_rst_n
15:13	RESERVED	NONE		Reserved
12	MSS_R5FSS0_CORE0_MBOX_READ_DONE_PROC_3	R/W1TC	0h	This register should be written once finishing reading from CR5A's mailbox written by proc 3 Reset Source: mod_g_rst_n
11:9	RESERVED	NONE		Reserved
8	MSS_R5FSS0_CORE0_MBOX_READ_DONE_PROC_2	R/W1TC	0h	This register should be written once finishing reading from CR5A's mailbox written by proc 2 Reset Source: mod_g_rst_n
7:5	RESERVED	NONE		Reserved
4	MSS_R5FSS0_CORE0_MBOX_READ_DONE_PROC_1	R/W1TC	0h	This register should be written once finishing reading from CR5A's mailbox written by proc 1 Reset Source: mod_g_rst_n
3:1	RESERVED	NONE		Reserved
0	MSS_R5FSS0_CORE0_MBOX_READ_DONE_PROC_0	R/W1TC	0h	This register should be written once finishing reading from CR5A's mailbox written by proc 0 Reset Source: mod_g_rst_n

2.3.112 CFG0_R5SS0_CORE0_SW_INT Registers

2.3.112.1 CFG0_CORE0_SW_INT Register (Offset = 4010h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-341. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 4010h

Figure 2-169. R5SS0_CORE0_SW_INT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															MSS_SW_INT_R5SS0_CORE0_PULSE
NONE															R/W
0															0h

Access Types Legend

Table 2-342. R5SS0_CORE0_SW_INT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	MSS_SW_INT_R5SS0_CORE0_PULSE	R/W	0h	Write_pulse bit field: writing 1'b1 to each bit will trigger MSS_SW_INT respectively to CR5A/B. Reset Source: mod_g_rst_n

2.3.113 CFG0_MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK Registers

2.3.113.1 CFG0_ADDR_ERRAGG_R5SS0_CPU0_MASK Register (Offset = 4020h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-343. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 4020h

Figure 2-170. MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														MPU_ADDR_INTR_ERRAGG0_MASK_MPU_HSM_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_MASK_MPU_R5FSS11_AHB_ADDR_ERR0
NONE														R/W	R/W
0														0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPU_ADDR_INTR_ERRAGG0_MASK_MPU_R5FSS0_CORE1_AHB_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_MASK_MPU_R5FSS1_CORE0_AHB_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_MASK_MPU_R5FSS0_CORE0_AHB_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_MASK_MPU_SCRM2SCRP1_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_MASK_MPU_SCRM2SCRP0_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_MASK_MPU_QSPI_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_MASK_MPU_MBOX_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_MASK_MPU_DTHE_A_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_MASK_MPU_R5FSS11_AXIS_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_MASK_MPU_R5FSS0_CORE1_AXIS_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_MASK_MPU_R5FSS1_CORE0_AXIS_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_MASK_MPU_R5FSS0_CORE0_AXIS_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_MASK_MPU_L2_BANK_D_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_MASK_MPU_L2_BANK_C_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_MASK_MPU_L2_BANK_B_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_MASK_MPU_L2_BANK_A_ADDR_ERR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-344. MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE		Reserved
17	MPU_ADDR_INTR_ERRAGG0_MASK_MPU_HSM_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
16	MPU_ADDR_INTR_ERRAGG0_MASK_MPU_R5FSS11_AHB_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
15	MPU_ADDR_INTR_ERRAGG0_MASK_MPU_R5FSS0_CORE1_AHB_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n

Table 2-344. MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	MPU_ADDR_INTR_ERRAGG0_MASK_MPU_R5FSS1_CORE0_AHB_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
13	MPU_ADDR_INTR_ERRAGG0_MASK_MPU_R5FSS0_CORE0_AHB_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
12	MPU_ADDR_INTR_ERRAGG0_MASK_MPU_SCRM2SCRP1_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
11	MPU_ADDR_INTR_ERRAGG0_MASK_MPU_SCRM2SCRP0_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
10	MPU_ADDR_INTR_ERRAGG0_MASK_MPU_QSPI_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
9	MPU_ADDR_INTR_ERRAGG0_MASK_MPU_MBOX_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
8	MPU_ADDR_INTR_ERRAGG0_MASK_MPU_DTHE_A_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
7	MPU_ADDR_INTR_ERRAGG0_MASK_MPU_R5FSS11_AXIS_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
6	MPU_ADDR_INTR_ERRAGG0_MASK_MPU_R5FSS0_CORE1_AXIS_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
5	MPU_ADDR_INTR_ERRAGG0_MASK_MPU_R5FSS1_CORE0_AXIS_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
4	MPU_ADDR_INTR_ERRAGG0_MASK_MPU_R5FSS0_CORE0_AXIS_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
3	MPU_ADDR_INTR_ERRAGG0_MASK_MPU_L2_BANK_D_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
2	MPU_ADDR_INTR_ERRAGG0_MASK_MPU_L2_BANK_C_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
1	MPU_ADDR_INTR_ERRAGG0_MASK_MPU_L2_BANK_B_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
0	MPU_ADDR_INTR_ERRAGG0_MASK_MPU_L2_BANK_A_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n

2.3.114 CFG0_MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS Registers

2.3.114.1 CFG0_ADDR_ERRAGG_R5SS0_CPU0_STATUS Register (Offset = 4024h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-345. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 4024h

Figure 2-171. MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_HSM_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_R5FSS11_AHB_ADDR_ERR0
NONE														R/W1TC	R/W1TC
0														0h	0h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_R5FSS0_CORE1_AHB_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_R5FSS1_CORE0_AHB_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_R5FSS0_CORE0_AHB_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_SCRM2SCRP1_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_SCRM2SCRP0_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_QSPI_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_MBOX_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_DTHE_A_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_R5FSS11_AXIS_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_R5FSS0_CORE1_AXIS_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_R5FSS1_CORE0_AXIS_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_R5FSS0_CORE0_AXIS_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_L2_BANK_D_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_L2_BANK_C_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_L2_BANK_B_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_L2_BANK_A_ADDR_ERR0
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-346. MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE		Reserved
17	MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_HSM_ADDR_ERR0	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
16	MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_R5FSS11_AHB_ADDR_ERR0	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n

Table 2-346. MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_R5FSS0_CORE1_AHB_ADDR_ERR0	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
14	MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_R5FSS1_CORE0_AHB_ADDR_ERR0	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
13	MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_R5FSS0_CORE0_AHB_ADDR_ERR0	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
12	MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_SCRM2SCRP1_ADDR_ERR0	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
11	MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_SCRM2SCRP0_ADDR_ERR0	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
10	MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_QSPI_ADDR_ERR0	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
9	MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_MBOX_ADDR_ERR0	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
8	MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_DTHE_A_ADDR_ERR0	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
7	MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_R5FSS11_AXIS_ADDR_ERR0	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
6	MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_R5FSS0_CORE1_AXIS_ADDR_ERR0	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
5	MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_R5FSS1_CORE0_AXIS_ADDR_ERR0	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
4	MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_R5FSS0_CORE0_AXIS_ADDR_ERR0	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
3	MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_L2_BANK_D_ADDR_ERR0	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
2	MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_L2_BANK_C_ADDR_ERR0	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
1	MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_L2_BANK_B_ADDR_ERR0	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
0	MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_L2_BANK_A_ADDR_ERR0	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n

2.3.115 CFG0_MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW Registers

2.3.115.1 CFG0_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW Register (Offset = 4028h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-347. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 4028h

Figure 2-172. MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_HSM_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_R5FSS11_AHB_ADDR_ERR0
NONE														R/W1TC	R/W1TC
0														0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_R5FSS0_CORE1_AHB_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_R5FSS1_CORE0_AHB_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_R5FSS0_CORE0_AHB_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_SCRM2SCRP1_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_SCRM2SCRP0_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_QSPI_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_MBOX_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_DTHE_A_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_R5FSS11_AXIS_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_R5FSS0_CORE1_AXIS_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_R5FSS1_CORE0_AXIS_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_R5FSS0_CORE0_AXIS_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_L2_BANK_D_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_L2_BANK_C_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_L2_BANK_B_ADDR_ERR0	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_L2_BANK_A_ADDR_ERR0
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-348. MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE		Reserved
17	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_HSM_ADDR_ERR0	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n

Table 2-348. MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_R5FSS11_AHB_ADDR_ERR0	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
15	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_R5FSS0_CORE1_AHB_ADDR_ERR0	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
14	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_R5FSS1_CORE0_AHB_ADDR_ERR0	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
13	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_R5FSS0_CORE0_AHB_ADDR_ERR0	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
12	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_SCRM2SCRP1_ADDR_ERR0	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
11	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_SCRM2SCRP0_ADDR_ERR0	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
10	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_QSPI_ADDR_ERR0	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
9	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_MBOX_ADDR_ERR0	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
8	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_DTHE_A_ADDR_ERR0	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
7	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_R5FSS11_AXIS_ADDR_ERR0	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
6	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_R5FSS0_CORE1_AXIS_ADDR_ERR0	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
5	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_R5FSS1_CORE0_AXIS_ADDR_ERR0	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
4	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_R5FSS0_CORE0_AXIS_ADDR_ERR0	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
3	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_L2_BANK_D_ADDR_ERR0	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
2	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_L2_BANK_C_ADDR_ERR0	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
1	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_L2_BANK_B_ADDR_ERR0	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n

Table 2-348. MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_L2_BANK_A_ADDR_ERR0	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n

2.3.116 CFG0_MPU_PROT_ERRAGG_R5SS0_CPU0_MASK Registers

2.3.116.1 CFG0_PROT_ERRAGG_R5SS0_CPU0_MASK Register (Offset = 4030h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-349. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 4030h

Figure 2-173. MPU_PROT_ERRAGG_R5SS0_CPU0_MASK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														MPU_PROT_INTR_ERRAGG0_MASK_MPU_HSM_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_MASK_MPU_R5FSS11_AHB_PROT_ERR0
NONE														R/W	R/W
0														0h	0h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPU_PROT_INTR_ERRAGG0_MASK_MPU_R5FSS0_CORE1_AHB_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_MASK_MPU_R5FSS1_CORE0_AHB_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_MASK_MPU_R5FSS0_CORE0_AHB_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_MASK_MPU_SCRM2SCRP1_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_MASK_MPU_SCRM2SCRP0_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_MASK_MPU_QSPI_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_MASK_MPU_MBOX_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_MASK_MPU_DTHE_A_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_MASK_MPU_R5FSS11_AXIS_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_MASK_MPU_R5FSS0_CORE1_AXIS_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_MASK_MPU_R5FSS1_CORE0_AXIS_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_MASK_MPU_R5FSS0_CORE0_AXIS_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_MASK_MPU_L2_BANK_D_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_MASK_MPU_L2_BANK_C_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_MASK_MPU_L2_BANK_B_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_MASK_MPU_L2_BANK_A_PROT_ERR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-350. MPU_PROT_ERRAGG_R5SS0_CPU0_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE		Reserved
17	MPU_PROT_INTR_ERRAGG0_MASK_MPU_HSM_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
16	MPU_PROT_INTR_ERRAGG0_MASK_MPU_R5FSS11_AHB_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
15	MPU_PROT_INTR_ERRAGG0_MASK_MPU_R5FSS0_CORE1_AHB_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n

Table 2-350. MPU_PROT_ERRAGG_R5SS0_CPU0_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	MPU_PROT_INTR_ERRAGG0_MASK_MPU_R5FSS1_CORE0_AHB_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
13	MPU_PROT_INTR_ERRAGG0_MASK_MPU_R5FSS0_CORE0_AHB_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
12	MPU_PROT_INTR_ERRAGG0_MASK_MPU_SCRM2SCRP1_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
11	MPU_PROT_INTR_ERRAGG0_MASK_MPU_SCRM2SCRP0_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
10	MPU_PROT_INTR_ERRAGG0_MASK_MPU_QSPI_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
9	MPU_PROT_INTR_ERRAGG0_MASK_MPU_MBOX_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
8	MPU_PROT_INTR_ERRAGG0_MASK_MPU_DTHE_A_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
7	MPU_PROT_INTR_ERRAGG0_MASK_MPU_R5FSS11_AXIS_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
6	MPU_PROT_INTR_ERRAGG0_MASK_MPU_R5FSS0_CORE1_AXIS_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
5	MPU_PROT_INTR_ERRAGG0_MASK_MPU_R5FSS1_CORE0_AXIS_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
4	MPU_PROT_INTR_ERRAGG0_MASK_MPU_R5FSS0_CORE0_AXIS_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
3	MPU_PROT_INTR_ERRAGG0_MASK_MPU_L2_BANK_D_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
2	MPU_PROT_INTR_ERRAGG0_MASK_MPU_L2_BANK_C_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
1	MPU_PROT_INTR_ERRAGG0_MASK_MPU_L2_BANK_B_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
0	MPU_PROT_INTR_ERRAGG0_MASK_MPU_L2_BANK_A_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n

2.3.117 CFG0_MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS Registers

2.3.117.1 CFG0_PROT_ERRAGG_R5SS0_CPU0_STATUS Register (Offset = 4034h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-351. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 4034h

Figure 2-174. MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														MPU_PROT_INTR_ERRAGG0_STATUS_MPU_HSM_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_STATUS_MPU_R5FSS11_AHB_PROT_ERR0
NONE														R/W1TC	R/W1TC
0														0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPU_PROT_INTR_ERRAGG0_STATUS_MPU_R5FSS0_CORE1_AHB_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_STATUS_MPU_R5FSS1_CORE0_AHB_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_STATUS_MPU_R5FSS0_CORE0_AHB_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_STATUS_MPU_SCRM2SCRP1_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_STATUS_MPU_SCRM2SCRP0_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_STATUS_MPU_QSPI_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_STATUS_MPU_MBOX_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_STATUS_MPU_DTHE_A_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_STATUS_MPU_R5FSS11_AXIS_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_STATUS_MPU_R5FSS0_CORE1_AXIS_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_STATUS_MPU_R5FSS1_CORE0_AXIS_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_STATUS_MPU_R5FSS0_CORE0_AXIS_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_STATUS_MPU_L2_BANK_D_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_STATUS_MPU_L2_BANK_C_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_STATUS_MPU_L2_BANK_B_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_STATUS_MPU_L2_BANK_A_PROT_ERR0
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-352. MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE		Reserved
17	MPU_PROT_INTR_ERRAGG0_STATUS_MPU_HSM_PROT_ERR0	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
16	MPU_PROT_INTR_ERRAGG0_STATUS_MPU_R5FSS11_AHB_PROT_ERR0	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n

Table 2-352. MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	MPU_PROT_INTR_ERRAGG0_STATUS_MPU_R5FSS0_CORE1_AHB_PROT_ERR0	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
14	MPU_PROT_INTR_ERRAGG0_STATUS_MPU_R5FSS1_CORE0_AHB_PROT_ERR0	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
13	MPU_PROT_INTR_ERRAGG0_STATUS_MPU_R5FSS0_CORE0_AHB_PROT_ERR0	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
12	MPU_PROT_INTR_ERRAGG0_STATUS_MPU_SCRM2SCRP1_PROT_ERR0	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
11	MPU_PROT_INTR_ERRAGG0_STATUS_MPU_SCRM2SCRP0_PROT_ERR0	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
10	MPU_PROT_INTR_ERRAGG0_STATUS_MPU_QSPI_PROT_ERR0	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
9	MPU_PROT_INTR_ERRAGG0_STATUS_MPU_MBOX_PROT_ERR0	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
8	MPU_PROT_INTR_ERRAGG0_STATUS_MPU_DTHE_A_PROT_ERR0	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
7	MPU_PROT_INTR_ERRAGG0_STATUS_MPU_R5FSS11_AXIS_PROT_ERR0	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
6	MPU_PROT_INTR_ERRAGG0_STATUS_MPU_R5FSS0_CORE1_AXIS_PROT_ERR0	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
5	MPU_PROT_INTR_ERRAGG0_STATUS_MPU_R5FSS1_CORE0_AXIS_PROT_ERR0	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
4	MPU_PROT_INTR_ERRAGG0_STATUS_MPU_R5FSS0_CORE0_AXIS_PROT_ERR0	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
3	MPU_PROT_INTR_ERRAGG0_STATUS_MPU_L2_BANK_D_PROT_ERR0	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
2	MPU_PROT_INTR_ERRAGG0_STATUS_MPU_L2_BANK_C_PROT_ERR0	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
1	MPU_PROT_INTR_ERRAGG0_STATUS_MPU_L2_BANK_B_PROT_ERR0	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
0	MPU_PROT_INTR_ERRAGG0_STATUS_MPU_L2_BANK_A_PROT_ERR0	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n

2.3.118 CFG0_MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW Registers

2.3.118.1 CFG0_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW Register (Offset = 4038h) [reset = 0h]

Short Description:

Long Description:

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Table 2-353. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 4038h

Figure 2-175. MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_HSM_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_R5FSS11_AHB_PROT_ERR0
NONE														R/W1TC	R/W1TC
0														0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_R5FSS0_CORE1_AHB_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_R5FSS1_CORE0_AHB_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_R5FSS0_CORE0_AHB_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_SCRM2SCRP1_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_SCRM2SCRP0_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_QSPI_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_MBOX_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_DTHE_A_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_R5FSS11_AXIS_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_R5FSS0_CORE1_AXIS_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_R5FSS1_CORE0_AXIS_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_R5FSS0_CORE0_AXIS_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_L2_BANK_D_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_L2_BANK_C_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_L2_BANK_B_PROT_ERR0	MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_L2_BANK_A_PROT_ERR0
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-354. MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE		Reserved
17	MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_HSM_PROT_ERR0	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n

Table 2-354. MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_R5FSS11_AHB_PROT_ERR0	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
15	MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_R5FSS0_CORE1_AHB_PROT_ERR0	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
14	MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_R5FSS1_CORE0_AHB_PROT_ERR0	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
13	MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_R5FSS0_CORE0_AHB_PROT_ERR0	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
12	MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_SCRM2SCRP1_PROT_ERR0	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
11	MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_SCRM2SCRP0_PROT_ERR0	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
10	MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_QSPI_PROT_ERR0	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
9	MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_MBOX_PROT_ERR0	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
8	MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_DTHE_A_PROT_ERR0	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
7	MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_R5FSS11_AXIS_PROT_ERR0	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
6	MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_R5FSS0_CORE1_AXIS_PROT_ERR0	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
5	MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_R5FSS1_CORE0_AXIS_PROT_ERR0	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
4	MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_R5FSS0_CORE0_AXIS_PROT_ERR0	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
3	MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_L2_BANK_D_PROT_ERR0	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
2	MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_L2_BANK_C_PROT_ERR0	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
1	MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_L2_BANK_B_PROT_ERR0	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n

Table 2-354. MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_L2_BANK_A_PROT_ERR0	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n

2.3.119 CFG0_R5SS0_CORE1_MBOX_WRITE_DONE Registers

2.3.119.1 CFG0_CORE1_MBOX_WRITE_DONE Register (Offset = 8000h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-355. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 8000h

Figure 2-176. R5SS0_CORE1_MBOX_WRITE_DONE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			MSS_R5FSS1_CORE0_MBOX_WRITE_DONE_PROC_7	RESERVED			MSS_R5FSS1_CORE0_MBOX_WRITE_DONE_PROC_6	RESERVED			MSS_R5FSS1_CORE0_MBOX_WRITE_DONE_PROC_5	RESERVED			MSS_R5FSS1_CORE0_MBOX_WRITE_DONE_PROC_4
NONE			R/W	NONE			R/W	NONE			R/W	NONE			R/W
0			0h	0			0h	0			0h	0			0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			MSS_R5FSS1_CORE0_MBOX_WRITE_DONE_PROC_3	RESERVED			MSS_R5FSS1_CORE0_MBOX_WRITE_DONE_PROC_2	RESERVED			MSS_R5FSS1_CORE0_MBOX_WRITE_DONE_PROC_1	RESERVED			MSS_R5FSS1_CORE0_MBOX_WRITE_DONE_PROC_0
NONE			R/W	NONE			R/W	NONE			R/W	NONE			R/W
0			0h	0			0h	0			0h	0			0h

Access Types Legend

Table 2-356. R5SS0_CORE1_MBOX_WRITE_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28	MSS_R5FSS1_CORE0_MBOX_WRITE_DONE_PROC_7	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 7 Reset Source: mod_g_rst_n
27:25	RESERVED	NONE		Reserved
24	MSS_R5FSS1_CORE0_MBOX_WRITE_DONE_PROC_6	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 6 Reset Source: mod_g_rst_n
23:21	RESERVED	NONE		Reserved
20	MSS_R5FSS1_CORE0_MBOX_WRITE_DONE_PROC_5	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 5 Reset Source: mod_g_rst_n
19:17	RESERVED	NONE		Reserved
16	MSS_R5FSS1_CORE0_MBOX_WRITE_DONE_PROC_4	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 4 Reset Source: mod_g_rst_n

Table 2-356. R5SS0_CORE1_MBOX_WRITE_DONE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:13	RESERVED	NONE		Reserved
12	MSS_R5FSS1_CORE0_MBOX_WRITE_DONE_PROC_3	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 3 Reset Source: mod_g_rst_n
11:9	RESERVED	NONE		Reserved
8	MSS_R5FSS1_CORE0_MBOX_WRITE_DONE_PROC_2	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 2 Reset Source: mod_g_rst_n
7:5	RESERVED	NONE		Reserved
4	MSS_R5FSS1_CORE0_MBOX_WRITE_DONE_PROC_1	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 1 Reset Source: mod_g_rst_n
3:1	RESERVED	NONE		Reserved
0	MSS_R5FSS1_CORE0_MBOX_WRITE_DONE_PROC_0	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 0 Reset Source: mod_g_rst_n

2.3.120 CFG0_R5SS0_CORE1_MBOX_READ_REQ Registers

2.3.120.1 CFG0_CORE1_MBOX_READ_REQ Register (Offset = 8004h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-357. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 8004h

Figure 2-177. R5SS0_CORE1_MBOX_READ_REQ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			MSS_R5FSS1_CORE0_MBOX_READ_REQ_PROC_7	RESERVED			MSS_R5FSS1_CORE0_MBOX_READ_REQ_PROC_6	RESERVED			MSS_R5FSS1_CORE0_MBOX_READ_REQ_PROC_5	RESERVED			MSS_R5FSS1_CORE0_MBOX_READ_REQ_PROC_4
NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC
0			0h	0			0h	0			0h	0			0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			MSS_R5FSS1_CORE0_MBOX_READ_REQ_PROC_3	RESERVED			MSS_R5FSS1_CORE0_MBOX_READ_REQ_PROC_2	RESERVED			MSS_R5FSS1_CORE0_MBOX_READ_REQ_PROC_1	RESERVED			MSS_R5FSS1_CORE0_MBOX_READ_REQ_PROC_0
NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC
0			0h	0			0h	0			0h	0			0h

Access Types Legend

Table 2-358. R5SS0_CORE1_MBOX_READ_REQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28	MSS_R5FSS1_CORE0_MBOX_READ_REQ_PROC_7	R/W1TC	0h	This is request from processor 7 to mss_CR5B. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
27:25	RESERVED	NONE		Reserved
24	MSS_R5FSS1_CORE0_MBOX_READ_REQ_PROC_6	R/W1TC	0h	This is request from processor 6 to mss_CR5B. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
23:21	RESERVED	NONE		Reserved
20	MSS_R5FSS1_CORE0_MBOX_READ_REQ_PROC_5	R/W1TC	0h	This is request from processor 5 to mss_CR5B. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
19:17	RESERVED	NONE		Reserved
16	MSS_R5FSS1_CORE0_MBOX_READ_REQ_PROC_4	R/W1TC	0h	This is request from processor 4 to mss_CR5B. Requesting it to read from mailbox. Reset Source: mod_g_rst_n

Table 2-358. R5SS0_CORE1_MBOX_READ_REQ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:13	RESERVED	NONE		Reserved
12	MSS_R5FSS1_CORE0_MBOX_READ_REQ_PROC_3	R/W1TC	0h	This is request from processor 3 to mss_CR5B. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
11:9	RESERVED	NONE		Reserved
8	MSS_R5FSS1_CORE0_MBOX_READ_REQ_PROC_2	R/W1TC	0h	This is request from processor 2 to mss_CR5B. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
7:5	RESERVED	NONE		Reserved
4	MSS_R5FSS1_CORE0_MBOX_READ_REQ_PROC_1	R/W1TC	0h	This is request from processor 1 to mss_CR5B. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
3:1	RESERVED	NONE		Reserved
0	MSS_R5FSS1_CORE0_MBOX_READ_REQ_PROC_0	R/W1TC	0h	This is request from processor 0 to mss_CR5B. Requesting it to read from mailbox. Reset Source: mod_g_rst_n

2.3.121 CFG0_R5SS0_CORE1_MBOX_READ_DONE_ACK Registers

2.3.121.1 CFG0_CORE1_MBOX_READ_DONE_ACK Register (Offset = 8008h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-359. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 8008h

Figure 2-178. R5SS0_CORE1_MBOX_READ_DONE_ACK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MSS_R5FSS1_CORE0_MBOX_READ_DONE_ACK_PROC							
NONE								R/W							
0								0h							

Access Types Legend

Table 2-360. R5SS0_CORE1_MBOX_READ_DONE_ACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	MSS_R5FSS1_CORE0_MBOX_READ_DONE_ACK_PROC	R/W	0h	Write pulse bit field: For bits 0 to 7: Wrting 1'b1 : Generates pulse interrupt to corresponding proc from MSS_CR5 Reset Source: mod_g_rst_n

2.3.122 CFG0_R5SS0_CORE1_MBOX_READ_DONE Registers

2.3.122.1 CFG0_CORE1_MBOX_READ_DONE Register (Offset = 800Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-361. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 800Ch

Figure 2-179. R5SS0_CORE1_MBOX_READ_DONE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			MSS_R5FSS1_CORE0_MBOX_READ_DONE_PROC_7	RESERVED			MSS_R5FSS1_CORE0_MBOX_READ_DONE_PROC_6	RESERVED			MSS_R5FSS1_CORE0_MBOX_READ_DONE_PROC_5	RESERVED			MSS_R5FSS1_CORE0_MBOX_READ_DONE_PROC_4
NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC
0			0h	0			0h	0			0h	0			0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			MSS_R5FSS1_CORE0_MBOX_READ_DONE_PROC_3	RESERVED			MSS_R5FSS1_CORE0_MBOX_READ_DONE_PROC_2	RESERVED			MSS_R5FSS1_CORE0_MBOX_READ_DONE_PROC_1	RESERVED			MSS_R5FSS1_CORE0_MBOX_READ_DONE_PROC_0
NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC
0			0h	0			0h	0			0h	0			0h

Access Types Legend

Table 2-362. R5SS0_CORE1_MBOX_READ_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28	MSS_R5FSS1_CORE0_MBOX_READ_DONE_PROC_7	R/W1TC	0h	This register should be written once finishing reading from CR5B's mailbox written by proc 7 Reset Source: mod_g_rst_n
27:25	RESERVED	NONE		Reserved
24	MSS_R5FSS1_CORE0_MBOX_READ_DONE_PROC_6	R/W1TC	0h	This register should be written once finishing reading from CR5B's mailbox written by proc 6 Reset Source: mod_g_rst_n
23:21	RESERVED	NONE		Reserved
20	MSS_R5FSS1_CORE0_MBOX_READ_DONE_PROC_5	R/W1TC	0h	This register should be written once finishing reading from CR5B's mailbox written by proc 5 Reset Source: mod_g_rst_n
19:17	RESERVED	NONE		Reserved

Table 2-362. R5SS0_CORE1_MBOX_READ_DONE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	MSS_R5FSS1_CORE0_MBOX_READ_DONE_PROC_4	R/W1TC	0h	This register should be written once finishing reading from CR5B's mailbox written by proc 4 Reset Source: mod_g_rst_n
15:13	RESERVED	NONE		Reserved
12	MSS_R5FSS1_CORE0_MBOX_READ_DONE_PROC_3	R/W1TC	0h	This register should be written once finishing reading from CR5B's mailbox written by proc 3 Reset Source: mod_g_rst_n
11:9	RESERVED	NONE		Reserved
8	MSS_R5FSS1_CORE0_MBOX_READ_DONE_PROC_2	R/W1TC	0h	This register should be written once finishing reading from CR5B's mailbox written by proc 2 Reset Source: mod_g_rst_n
7:5	RESERVED	NONE		Reserved
4	MSS_R5FSS1_CORE0_MBOX_READ_DONE_PROC_1	R/W1TC	0h	This register should be written once finishing reading from CR5B's mailbox written by proc 1 Reset Source: mod_g_rst_n
3:1	RESERVED	NONE		Reserved
0	MSS_R5FSS1_CORE0_MBOX_READ_DONE_PROC_0	R/W1TC	0h	This register should be written once finishing reading from CR5B's mailbox written by proc 0 Reset Source: mod_g_rst_n

2.3.123 CFG0_R5SS0_CORE1_SW_INT Registers

2.3.123.1 CFG0_CORE1_SW_INT Register (Offset = 8010h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-363. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 8010h

Figure 2-180. R5SS0_CORE1_SW_INT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															MSS_SW_INT_R5SS0_CORE1_PULSE
NONE															R/W
0															0h

Access Types Legend

Table 2-364. R5SS0_CORE1_SW_INT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	MSS_SW_INT_R5SS0_CORE1_PULSE	R/W	0h	Write_pulse bit field: writing 1'b1 to each bit will trigger MSS_SW_INT respectively to CR5A/B. Reset Source: mod_g_rst_n

2.3.124 CFG0_MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK Registers

2.3.124.1 CFG0_ADDR_ERRAGG_R5SS0_CPU1_MASK Register (Offset = 8020h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-365. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 8020h

Figure 2-181. MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														MPU_ADDR_INTR_ERRAGG1_MASK_MPU_HSM_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_MASK_MPU_R5FSS11_AHB_ADDR_ERR1
NONE														R/W	R/W
0														0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPU_ADDR_INTR_ERRAGG1_MASK_MPU_R5FSS0_CORE1_AHB_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_MASK_MPU_R5FSS1_CORE0_AHB_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_MASK_MPU_R5FSS0_CORE0_AHB_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_MASK_MPU_SCRM2SCRP1_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_MASK_MPU_SCRM2SCRP0_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_MASK_MPU_QSPI_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_MASK_MPU_MBOX_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_MASK_MPU_DTHE_A_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_MASK_MPU_R5FSS11_AXIS_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_MASK_MPU_R5FSS0_CORE1_AXIS_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_MASK_MPU_R5FSS1_CORE0_AXIS_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_MASK_MPU_R5FSS0_CORE0_AXIS_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_MASK_MPU_L2_BANK_D_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_MASK_MPU_L2_BANK_C_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_MASK_MPU_L2_BANK_B_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_MASK_MPU_L2_BANK_A_ADDR_ERR1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-366. MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE		Reserved
17	MPU_ADDR_INTR_ERRAGG1_MASK_MPU_HSM_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
16	MPU_ADDR_INTR_ERRAGG1_MASK_MPU_R5FSS11_AHB_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
15	MPU_ADDR_INTR_ERRAGG1_MASK_MPU_R5FSS0_CORE1_AHB_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n

Table 2-366. MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	MPU_ADDR_INTR_ERRAGG1_MASK_MPU_R5FSS1_CORE0_AHB_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
13	MPU_ADDR_INTR_ERRAGG1_MASK_MPU_R5FSS0_CORE0_AHB_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
12	MPU_ADDR_INTR_ERRAGG1_MASK_MPU_SCRM2SCRP1_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
11	MPU_ADDR_INTR_ERRAGG1_MASK_MPU_SCRM2SCRP0_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
10	MPU_ADDR_INTR_ERRAGG1_MASK_MPU_QSPI_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
9	MPU_ADDR_INTR_ERRAGG1_MASK_MPU_MBOX_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
8	MPU_ADDR_INTR_ERRAGG1_MASK_MPU_DTHE_A_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
7	MPU_ADDR_INTR_ERRAGG1_MASK_MPU_R5FSS11_AXIS_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
6	MPU_ADDR_INTR_ERRAGG1_MASK_MPU_R5FSS0_CORE1_AXIS_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
5	MPU_ADDR_INTR_ERRAGG1_MASK_MPU_R5FSS1_CORE0_AXIS_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
4	MPU_ADDR_INTR_ERRAGG1_MASK_MPU_R5FSS0_CORE0_AXIS_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
3	MPU_ADDR_INTR_ERRAGG1_MASK_MPU_L2_BANK_D_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
2	MPU_ADDR_INTR_ERRAGG1_MASK_MPU_L2_BANK_C_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
1	MPU_ADDR_INTR_ERRAGG1_MASK_MPU_L2_BANK_B_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
0	MPU_ADDR_INTR_ERRAGG1_MASK_MPU_L2_BANK_A_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n

2.3.125 CFG0_MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS Registers

2.3.125.1 CFG0_ADDR_ERRAGG_R5SS0_CPU1_STATUS Register (Offset = 8024h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-367. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 8024h

Figure 2-182. MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_HSM_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_R5FSS11_AHB_ADDR_ERR1
NONE														R/W1TC	R/W1TC
0														0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_R5FSS0_CORE1_AHB_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_R5FSS1_CORE0_AHB_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_R5FSS0_CORE0_AHB_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_SCRM2SCRP1_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_SCRM2SCRP0_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_QSPI_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_MBOX_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_DTHE_A_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_R5FSS11_AXIS_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_R5FSS0_CORE1_AXIS_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_R5FSS1_CORE0_AXIS_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_R5FSS0_CORE0_AXIS_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_L2_BANK_D_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_L2_BANK_C_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_L2_BANK_B_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_L2_BANK_A_ADDR_ERR1
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-368. MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE		Reserved
17	MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_HSM_ADDR_ERR1	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
16	MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_R5FSS11_AHB_ADDR_ERR1	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n

Table 2-368. MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_R5FSS0_CORE1_AHB_ADDR_ERR1	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
14	MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_R5FSS1_CORE0_AHB_ADDR_ERR1	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
13	MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_R5FSS0_CORE0_AHB_ADDR_ERR1	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
12	MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_SCRM2SCRP1_ADDR_ERR1	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
11	MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_SCRM2SCRP0_ADDR_ERR1	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
10	MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_QSPI_ADDR_ERR1	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
9	MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_MBOX_ADDR_ERR1	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
8	MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_DTHE_A_ADDR_ERR1	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
7	MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_R5FSS11_AXIS_ADDR_ERR1	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
6	MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_R5FSS0_CORE1_AXIS_ADDR_ERR1	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
5	MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_R5FSS1_CORE0_AXIS_ADDR_ERR1	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
4	MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_R5FSS0_CORE0_AXIS_ADDR_ERR1	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
3	MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_L2_BANK_D_ADDR_ERR1	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
2	MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_L2_BANK_C_ADDR_ERR1	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
1	MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_L2_BANK_B_ADDR_ERR1	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
0	MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_L2_BANK_A_ADDR_ERR1	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n

2.3.126 CFG0_MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW Registers

2.3.126.1 CFG0_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW Register (Offset = 8028h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-369. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 8028h

Figure 2-183. MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_HSM_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_R5FSS11_AHB_ADDR_ERR1
NONE														R/W1TC	R/W1TC
0														0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_R5FSS0_CORE1_AHB_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_R5FSS1_CORE0_AHB_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_R5FSS0_CORE0_AHB_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_SCRM2SCRP1_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_SCRM2SCRP0_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_QSPI_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_MBOX_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_DTHE_A_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_R5FSS11_AXIS_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_R5FSS0_CORE1_AXIS_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_R5FSS1_CORE0_AXIS_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_R5FSS0_CORE0_AXIS_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_L2_BANK_D_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_L2_BANK_C_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_L2_BANK_B_ADDR_ERR1	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_L2_BANK_A_ADDR_ERR1
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-370. MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE		Reserved
17	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_HSM_ADDR_ERR1	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n

Table 2-370. MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_R5FSS11_AHB_ADDR_ERR1	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
15	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_R5FSS0_CORE1_AHB_ADDR_ERR1	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
14	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_R5FSS1_CORE0_AHB_ADDR_ERR1	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
13	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_R5FSS0_CORE0_AHB_ADDR_ERR1	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
12	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_SCRM2SCRP1_ADDR_ERR1	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
11	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_SCRM2SCRP0_ADDR_ERR1	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
10	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_QSPI_ADDR_ERR1	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
9	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_MBOX_ADDR_ERR1	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
8	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_DTHE_A_ADDR_ERR1	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
7	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_R5FSS11_AXIS_ADDR_ERR1	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
6	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_R5FSS0_CORE1_AXIS_ADDR_ERR1	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
5	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_R5FSS1_CORE0_AXIS_ADDR_ERR1	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
4	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_R5FSS0_CORE0_AXIS_ADDR_ERR1	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
3	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_L2_BANK_D_ADDR_ERR1	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
2	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_L2_BANK_C_ADDR_ERR1	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
1	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_L2_BANK_B_ADDR_ERR1	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n

Table 2-370. MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_L2_BANK_A_ADDR_ERR1	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n

2.3.127 CFG0_MPU_PROT_ERRAGG_R5SS0_CPU1_MASK Registers

2.3.127.1 CFG0_PROT_ERRAGG_R5SS0_CPU1_MASK Register (Offset = 8030h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-371. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 8030h

Figure 2-184. MPU_PROT_ERRAGG_R5SS0_CPU1_MASK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														MPU_PROT_INTR_ERRAGG1_MASK_MPU_HSM_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_MASK_MPU_R5FSS11_AHB_PROT_ERR1
NONE														R/W	R/W
0														0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPU_PROT_INTR_ERRAGG1_MASK_MPU_R5FSS0_CORE1_AHB_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_MASK_MPU_R5FSS1_CORE0_AHB_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_MASK_MPU_R5FSS0_CORE0_AHB_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_MASK_MPU_SCRM2SCRP1_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_MASK_MPU_SCRM2SCRP0_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_MASK_MPU_QSPI_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_MASK_MPU_MBOX_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_MASK_MPU_DTHE_A_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_MASK_MPU_R5FSS11_AXIS_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_MASK_MPU_R5FSS0_CORE1_AXIS_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_MASK_MPU_R5FSS1_CORE0_AXIS_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_MASK_MPU_R5FSS0_CORE0_AXIS_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_MASK_MPU_L2_BANK_D_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_MASK_MPU_L2_BANK_C_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_MASK_MPU_L2_BANK_B_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_MASK_MPU_L2_BANK_A_PROT_ERR1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-372. MPU_PROT_ERRAGG_R5SS0_CPU1_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE		Reserved
17	MPU_PROT_INTR_ERRAGG1_MASK_MPU_HSM_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
16	MPU_PROT_INTR_ERRAGG1_MASK_MPU_R5FSS11_AHB_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
15	MPU_PROT_INTR_ERRAGG1_MASK_MPU_R5FSS0_CORE1_AHB_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n

Table 2-372. MPU_PROT_ERRAGG_R5SS0_CPU1_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	MPU_PROT_INTR_ERRAGG1_MASK_MPU_R5FSS1_CORE0_AHB_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
13	MPU_PROT_INTR_ERRAGG1_MASK_MPU_R5FSS0_CORE0_AHB_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
12	MPU_PROT_INTR_ERRAGG1_MASK_MPU_SCRM2SCRP1_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
11	MPU_PROT_INTR_ERRAGG1_MASK_MPU_SCRM2SCRP0_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
10	MPU_PROT_INTR_ERRAGG1_MASK_MPU_QSPI_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
9	MPU_PROT_INTR_ERRAGG1_MASK_MPU_MBOX_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
8	MPU_PROT_INTR_ERRAGG1_MASK_MPU_DTHE_A_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
7	MPU_PROT_INTR_ERRAGG1_MASK_MPU_R5FSS11_AXIS_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
6	MPU_PROT_INTR_ERRAGG1_MASK_MPU_R5FSS0_CORE1_AXIS_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
5	MPU_PROT_INTR_ERRAGG1_MASK_MPU_R5FSS1_CORE0_AXIS_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
4	MPU_PROT_INTR_ERRAGG1_MASK_MPU_R5FSS0_CORE0_AXIS_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
3	MPU_PROT_INTR_ERRAGG1_MASK_MPU_L2_BANK_D_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
2	MPU_PROT_INTR_ERRAGG1_MASK_MPU_L2_BANK_C_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
1	MPU_PROT_INTR_ERRAGG1_MASK_MPU_L2_BANK_B_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
0	MPU_PROT_INTR_ERRAGG1_MASK_MPU_L2_BANK_A_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n

2.3.128 CFG0_MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS Registers

2.3.128.1 CFG0_PROT_ERRAGG_R5SS0_CPU1_STATUS Register (Offset = 8034h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-373. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 8034h

Figure 2-185. MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														MPU_PROT_INTR_ERRAGG1_STATUS_MPU_HSM_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_STATUS_MPU_R5FSS11_AHB_PROT_ERR1
NONE														R/W1TC	R/W1TC
0														0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPU_PROT_INTR_ERRAGG1_STATUS_MPU_R5FSS0_CORE1_AHB_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_STATUS_MPU_R5FSS1_CORE0_AHB_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_STATUS_MPU_R5FSS0_CORE0_AHB_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_STATUS_MPU_SCRM2SCRP1_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_STATUS_MPU_SCRM2SCRP0_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_STATUS_MPU_QSPI_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_STATUS_MPU_MBOX_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_STATUS_MPU_DTHE_A_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_STATUS_MPU_R5FSS11_AXIS_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_STATUS_MPU_R5FSS0_CORE1_AXIS_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_STATUS_MPU_R5FSS1_CORE0_AXIS_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_STATUS_MPU_R5FSS0_CORE0_AXIS_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_STATUS_MPU_L2_BANK_D_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_STATUS_MPU_L2_BANK_C_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_STATUS_MPU_L2_BANK_B_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_STATUS_MPU_L2_BANK_A_PROT_ERR1
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-374. MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE		Reserved
17	MPU_PROT_INTR_ERRAGG1_STATUS_MPU_HSM_PROT_ERR1	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
16	MPU_PROT_INTR_ERRAGG1_STATUS_MPU_R5FSS11_AHB_PROT_ERR1	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n

Table 2-374. MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	MPU_PROT_INTR_ERRAGG1_STATUS_MPU_R5FSS0_CORE1_AHB_PROT_ERR1	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
14	MPU_PROT_INTR_ERRAGG1_STATUS_MPU_R5FSS1_CORE0_AHB_PROT_ERR1	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
13	MPU_PROT_INTR_ERRAGG1_STATUS_MPU_R5FSS0_CORE0_AHB_PROT_ERR1	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
12	MPU_PROT_INTR_ERRAGG1_STATUS_MPU_SCRM2SCRP1_PROT_ERR1	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
11	MPU_PROT_INTR_ERRAGG1_STATUS_MPU_SCRM2SCRP0_PROT_ERR1	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
10	MPU_PROT_INTR_ERRAGG1_STATUS_MPU_QSPI_PROT_ERR1	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
9	MPU_PROT_INTR_ERRAGG1_STATUS_MPU_MBOX_PROT_ERR1	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
8	MPU_PROT_INTR_ERRAGG1_STATUS_MPU_DTHE_A_PROT_ERR1	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
7	MPU_PROT_INTR_ERRAGG1_STATUS_MPU_R5FSS11_AXIS_PROT_ERR1	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
6	MPU_PROT_INTR_ERRAGG1_STATUS_MPU_R5FSS0_CORE1_AXIS_PROT_ERR1	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
5	MPU_PROT_INTR_ERRAGG1_STATUS_MPU_R5FSS1_CORE0_AXIS_PROT_ERR1	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
4	MPU_PROT_INTR_ERRAGG1_STATUS_MPU_R5FSS0_CORE0_AXIS_PROT_ERR1	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
3	MPU_PROT_INTR_ERRAGG1_STATUS_MPU_L2_BANK_D_PROT_ERR1	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
2	MPU_PROT_INTR_ERRAGG1_STATUS_MPU_L2_BANK_C_PROT_ERR1	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
1	MPU_PROT_INTR_ERRAGG1_STATUS_MPU_L2_BANK_B_PROT_ERR1	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
0	MPU_PROT_INTR_ERRAGG1_STATUS_MPU_L2_BANK_A_PROT_ERR1	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n

2.3.129 CFG0_MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW Registers

2.3.129.1 CFG0_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW Register (Offset = 8038h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-375. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 8038h

Figure 2-186. MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_HSM_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_R5FSS11_AHB_PROT_ERR1
NONE														R/W1TC	R/W1TC
0														0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_R5FSS0_CORE1_AHB_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_R5FSS1_CORE0_AHB_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_R5FSS0_CORE0_AHB_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_SCRM2SCRP1_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_SCRM2SCRP0_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_QSPI_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_MBOX_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_DTHE_A_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_R5FSS11_AXIS_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_R5FSS0_CORE1_AXIS_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_R5FSS1_CORE0_AXIS_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_R5FSS0_CORE0_AXIS_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_L2_BANK_D_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_L2_BANK_C_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_L2_BANK_B_PROT_ERR1	MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_L2_BANK_A_PROT_ERR1
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-376. MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE		Reserved
17	MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_HSM_PROT_ERR1	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n

Table 2-376. MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_R5FSS11_AHB_PROT_ERR1	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
15	MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_R5FSS0_CORE1_AHB_PROT_ERR1	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
14	MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_R5FSS1_CORE0_AHB_PROT_ERR1	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
13	MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_R5FSS0_CORE0_AHB_PROT_ERR1	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
12	MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_SCRM2SCRP1_PROT_ERR1	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
11	MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_SCRM2SCRP0_PROT_ERR1	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
10	MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_QSPI_PROT_ERR1	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
9	MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_MBOX_PROT_ERR1	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
8	MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_DTHE_A_PROT_ERR1	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
7	MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_R5FSS11_AXIS_PROT_ERR1	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
6	MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_R5FSS0_CORE1_AXIS_PROT_ERR1	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
5	MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_R5FSS1_CORE0_AXIS_PROT_ERR1	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
4	MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_R5FSS0_CORE0_AXIS_PROT_ERR1	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
3	MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_L2_BANK_D_PROT_ERR1	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
2	MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_L2_BANK_C_PROT_ERR1	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
1	MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_L2_BANK_B_PROT_ERR1	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n

Table 2-376. MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_L2_BANK_A_PROT_ERR1	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n

2.3.130 CFG0_R5SS1_CORE0_MBOX_WRITE_DONE Registers

2.3.130.1 CFG0_CORE0_MBOX_WRITE_DONE Register (Offset = C000h) [reset = 0h]

Short Description:

Long Description:

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Table 2-377. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 C000h

Figure 2-187. R5SS1_CORE0_MBOX_WRITE_DONE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			MSS_R5FSS01_MBOX_WRITE_DONE_PROC_7	RESERVED			MSS_R5FSS01_MBOX_WRITE_DONE_PROC_6	RESERVED			MSS_R5FSS01_MBOX_WRITE_DONE_PROC_5	RESERVED			MSS_R5FSS01_MBOX_WRITE_DONE_PROC_4
NONE			R/W	NONE			R/W	NONE			R/W	NONE			R/W
0			0h	0			0h	0			0h	0			0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			MSS_R5FSS01_MBOX_WRITE_DONE_PROC_3	RESERVED			MSS_R5FSS01_MBOX_WRITE_DONE_PROC_2	RESERVED			MSS_R5FSS01_MBOX_WRITE_DONE_PROC_1	RESERVED			MSS_R5FSS01_MBOX_WRITE_DONE_PROC_0
NONE			R/W	NONE			R/W	NONE			R/W	NONE			R/W
0			0h	0			0h	0			0h	0			0h

Access Types Legend

Table 2-378. R5SS1_CORE0_MBOX_WRITE_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28	MSS_R5FSS01_MBOX_WRITE_DONE_PROC_7	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 7 Reset Source: mod_g_rst_n
27:25	RESERVED	NONE		Reserved
24	MSS_R5FSS01_MBOX_WRITE_DONE_PROC_6	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 6 Reset Source: mod_g_rst_n
23:21	RESERVED	NONE		Reserved
20	MSS_R5FSS01_MBOX_WRITE_DONE_PROC_5	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 5 Reset Source: mod_g_rst_n
19:17	RESERVED	NONE		Reserved
16	MSS_R5FSS01_MBOX_WRITE_DONE_PROC_4	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 4 Reset Source: mod_g_rst_n
15:13	RESERVED	NONE		Reserved

Table 2-378. R5SS1_CORE0_MBOX_WRITE_DONE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	MSS_R5FSS01_MBOX_WRITE_DONE_PROC_3	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 3 Reset Source: mod_g_rst_n
11:9	RESERVED	NONE		Reserved
8	MSS_R5FSS01_MBOX_WRITE_DONE_PROC_2	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 2 Reset Source: mod_g_rst_n
7:5	RESERVED	NONE		Reserved
4	MSS_R5FSS01_MBOX_WRITE_DONE_PROC_1	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 1 Reset Source: mod_g_rst_n
3:1	RESERVED	NONE		Reserved
0	MSS_R5FSS01_MBOX_WRITE_DONE_PROC_0	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 0 Reset Source: mod_g_rst_n

2.3.131 CFG0_R5SS1_CORE0_MBOX_READ_REQ Registers

2.3.131.1 CFG0_CORE0_MBOX_READ_REQ Register (Offset = C004h) [reset = 0h]

Short Description:

Long Description:

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Table 2-379. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 C004h

Figure 2-188. R5SS1_CORE0_MBOX_READ_REQ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			MSS_R5FSS01_MBOX_READ_REQ_PROC_7	RESERVED			MSS_R5FSS01_MBOX_READ_REQ_PROC_6	RESERVED			MSS_R5FSS01_MBOX_READ_REQ_PROC_5	RESERVED			MSS_R5FSS01_MBOX_READ_REQ_PROC_4
NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC
0			0h	0			0h	0			0h	0			0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			MSS_R5FSS01_MBOX_READ_REQ_PROC_3	RESERVED			MSS_R5FSS01_MBOX_READ_REQ_PROC_2	RESERVED			MSS_R5FSS01_MBOX_READ_REQ_PROC_1	RESERVED			MSS_R5FSS01_MBOX_READ_REQ_PROC_0
NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC
0			0h	0			0h	0			0h	0			0h

Access Types Legend

Table 2-380. R5SS1_CORE0_MBOX_READ_REQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28	MSS_R5FSS01_MBOX_READ_REQ_PROC_7	R/W1TC	0h	This is request from processor 7 to mss_cr5a. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
27:25	RESERVED	NONE		Reserved
24	MSS_R5FSS01_MBOX_READ_REQ_PROC_6	R/W1TC	0h	This is request from processor 6 to mss_cr5a. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
23:21	RESERVED	NONE		Reserved
20	MSS_R5FSS01_MBOX_READ_REQ_PROC_5	R/W1TC	0h	This is request from processor 5 to mss_cr5a. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
19:17	RESERVED	NONE		Reserved
16	MSS_R5FSS01_MBOX_READ_REQ_PROC_4	R/W1TC	0h	This is request from processor 4 to mss_cr5a. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
15:13	RESERVED	NONE		Reserved
12	MSS_R5FSS01_MBOX_READ_REQ_PROC_3	R/W1TC	0h	This is request from processor 3 to mss_cr5a. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
11:9	RESERVED	NONE		Reserved

Table 2-380. R5SS1_CORE0_MBOX_READ_REQ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	MSS_R5FSS01_MBOX_READ_REQ_PROC_2	R/W1TC	0h	This is request from processor 2 to mss_cr5a. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
7:5	RESERVED	NONE		Reserved
4	MSS_R5FSS01_MBOX_READ_REQ_PROC_1	R/W1TC	0h	This is request from processor 1 to mss_cr5a. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
3:1	RESERVED	NONE		Reserved
0	MSS_R5FSS01_MBOX_READ_REQ_PROC_0	R/W1TC	0h	This is request from processor 0 to mss_cr5a. Requesting it to read from mailbox. Reset Source: mod_g_rst_n

2.3.132 CFG0_R5SS1_CORE0_MBOX_READ_DONE_ACK Registers

2.3.132.1 CFG0_CORE0_MBOX_READ_DONE_ACK Register (Offset = C008h) [reset = 0h]

Short Description:

Long Description:

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Table 2-381. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 C008h

Figure 2-189. R5SS1_CORE0_MBOX_READ_DONE_ACK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MSS_R5FSS01_MBOX_READ_DONE_ACK_PROC							
NONE								R/W							
0								0h							

Access Types Legend

Table 2-382. R5SS1_CORE0_MBOX_READ_DONE_ACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	MSS_R5FSS01_MBOX_READ_DONE_ACK_PROC	R/W	0h	Write pulse bit field: For bits 0 to 7: Wrting 1'b1 : Generates pulse interrupt to corresponding proc from MSS_CR5 Reset Source: mod_g_rst_n

2.3.133 CFG0_R5SS1_CORE0_MBOX_READ_DONE Registers

2.3.133.1 CFG0_CORE0_MBOX_READ_DONE Register (Offset = C00Ch) [reset = 0h]

Short Description:

Long Description:

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Table 2-383. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 C00Ch

Figure 2-190. R5SS1_CORE0_MBOX_READ_DONE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			MSS_R5FSS01_MBOX_READ_DONE_PROC_7	RESERVED			MSS_R5FSS01_MBOX_READ_DONE_PROC_6	RESERVED			MSS_R5FSS01_MBOX_READ_DONE_PROC_5	RESERVED			MSS_R5FSS01_MBOX_READ_DONE_PROC_4
NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC
0			0h	0			0h	0			0h	0			0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			MSS_R5FSS01_MBOX_READ_DONE_PROC_3	RESERVED			MSS_R5FSS01_MBOX_READ_DONE_PROC_2	RESERVED			MSS_R5FSS01_MBOX_READ_DONE_PROC_1	RESERVED			MSS_R5FSS01_MBOX_READ_DONE_PROC_0
NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC
0			0h	0			0h	0			0h	0			0h

Access Types Legend

Table 2-384. R5SS1_CORE0_MBOX_READ_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28	MSS_R5FSS01_MBOX_READ_DONE_PROC_7	R/W1TC	0h	This register should be written once finishing reading from CR5A's mailbox written by proc 7 Reset Source: mod_g_rst_n
27:25	RESERVED	NONE		Reserved
24	MSS_R5FSS01_MBOX_READ_DONE_PROC_6	R/W1TC	0h	This register should be written once finishing reading from CR5A's mailbox written by proc 6 Reset Source: mod_g_rst_n
23:21	RESERVED	NONE		Reserved
20	MSS_R5FSS01_MBOX_READ_DONE_PROC_5	R/W1TC	0h	This register should be written once finishing reading from CR5A's mailbox written by proc 5 Reset Source: mod_g_rst_n
19:17	RESERVED	NONE		Reserved
16	MSS_R5FSS01_MBOX_READ_DONE_PROC_4	R/W1TC	0h	This register should be written once finishing reading from CR5A's mailbox written by proc 4 Reset Source: mod_g_rst_n
15:13	RESERVED	NONE		Reserved
12	MSS_R5FSS01_MBOX_READ_DONE_PROC_3	R/W1TC	0h	This register should be written once finishing reading from CR5A's mailbox written by proc 3 Reset Source: mod_g_rst_n

Table 2-384. R5SS1_CORE0_MBOX_READ_DONE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:9	RESERVED	NONE		Reserved
8	MSS_R5FSS01_MBOX_READ_DONE_PROC_2	R/W1TC	0h	This register should be written once finishing reading from CR5A's mailbox written by proc 2 Reset Source: mod_g_rst_n
7:5	RESERVED	NONE		Reserved
4	MSS_R5FSS01_MBOX_READ_DONE_PROC_1	R/W1TC	0h	This register should be written once finishing reading from CR5A's mailbox written by proc 1 Reset Source: mod_g_rst_n
3:1	RESERVED	NONE		Reserved
0	MSS_R5FSS01_MBOX_READ_DONE_PROC_0	R/W1TC	0h	This register should be written once finishing reading from CR5A's mailbox written by proc 0 Reset Source: mod_g_rst_n

2.3.134 CFG0_R5SS1_CORE0_SW_INT Registers

2.3.134.1 CFG0_CORE0_SW_INT Register (Offset = C010h) [reset = 0h]

Short Description:

Long Description:

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Table 2-385. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 C010h

Figure 2-191. R5SS1_CORE0_SW_INT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															MSS_SW_INT_R5SS1_CORE0_PULSE
NONE															R/W
0															0h

Access Types Legend

Table 2-386. R5SS1_CORE0_SW_INT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	MSS_SW_INT_R5SS1_CORE0_PULSE	R/W	0h	Write_pulse bit field: writing 1'b1 to each bit will trigger MSS_SW_INT respectively to CR5A/B. Reset Source: mod_g_rst_n

2.3.135 CFG0_MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK Registers

2.3.135.1 CFG0_ADDR_ERRAGG_R5SS1_CPU0_MASK Register (Offset = C020h) [reset = 0h]

Short Description:

Long Description:

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Table 2-387. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 C020h

Figure 2-192. MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														MPU_ADDR_INTR_ERRAGG2_MASK_MPU_HSM_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_MASK_MPU_R5FSS11_AHB_ADDR_ERR2
NONE														R/W	R/W
0														0h	0h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPU_ADDR_INTR_ERRAGG2_MASK_MPU_R5FSS0_CORE1_AHB_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_MASK_MPU_R5FSS1_CORE0_AHB_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_MASK_MPU_R5FSS0_CORE0_AHB_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_MASK_MPU_SCRM2SCRP1_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_MASK_MPU_SCRM2SCRP0_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_MASK_MPU_QSPI_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_MASK_MPU_MBOX_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_MASK_MPU_DTHE_A_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_MASK_MPU_R5FSS11_AXIS_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_MASK_MPU_R5FSS0_CORE1_AXIS_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_MASK_MPU_R5FSS1_CORE0_AXIS_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_MASK_MPU_R5FSS0_CORE0_AXIS_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_MASK_MPU_L2_BANK_D_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_MASK_MPU_L2_BANK_C_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_MASK_MPU_L2_BANK_B_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_MASK_MPU_L2_BANK_A_ADDR_ERR2
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-388. MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE		Reserved
17	MPU_ADDR_INTR_ERRAGG2_MASK_MPU_HSM_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
16	MPU_ADDR_INTR_ERRAGG2_MASK_MPU_R5FSS11_AHB_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
15	MPU_ADDR_INTR_ERRAGG2_MASK_MPU_R5FSS0_CORE1_AHB_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n

Table 2-388. MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	MPU_ADDR_INTR_ERRAGG2_MASK_MPU_R5FSS1_CORE0_AHB_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
13	MPU_ADDR_INTR_ERRAGG2_MASK_MPU_R5FSS0_CORE0_AHB_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
12	MPU_ADDR_INTR_ERRAGG2_MASK_MPU_SCRM2SCRP1_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
11	MPU_ADDR_INTR_ERRAGG2_MASK_MPU_SCRM2SCRP0_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
10	MPU_ADDR_INTR_ERRAGG2_MASK_MPU_QSPI_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
9	MPU_ADDR_INTR_ERRAGG2_MASK_MPU_MBOX_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
8	MPU_ADDR_INTR_ERRAGG2_MASK_MPU_DTHE_A_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
7	MPU_ADDR_INTR_ERRAGG2_MASK_MPU_R5FSS11_AXIS_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
6	MPU_ADDR_INTR_ERRAGG2_MASK_MPU_R5FSS0_CORE1_AXIS_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
5	MPU_ADDR_INTR_ERRAGG2_MASK_MPU_R5FSS1_CORE0_AXIS_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
4	MPU_ADDR_INTR_ERRAGG2_MASK_MPU_R5FSS0_CORE0_AXIS_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
3	MPU_ADDR_INTR_ERRAGG2_MASK_MPU_L2_BANK_D_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
2	MPU_ADDR_INTR_ERRAGG2_MASK_MPU_L2_BANK_C_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
1	MPU_ADDR_INTR_ERRAGG2_MASK_MPU_L2_BANK_B_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
0	MPU_ADDR_INTR_ERRAGG2_MASK_MPU_L2_BANK_A_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n

2.3.136 CFG0_MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS Registers

2.3.136.1 CFG0_ADDR_ERRAGG_R5SS1_CPU0_STATUS Register (Offset = C024h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-389. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 C024h

Figure 2-193. MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_HSM_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_R5FSS11_AHB_ADDR_ERR2
NONE														R/W1TC	R/W1TC
0														0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_R5FSS0_CORE1_AHB_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_R5FSS1_CORE0_AHB_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_R5FSS0_CORE0_AHB_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_SCRM2SCRP1_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_SCRM2SCRP0_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_QSPI_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_MBOX_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_DTHE_A_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_R5FSS11_AXIS_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_R5FSS0_CORE1_AXIS_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_R5FSS1_CORE0_AXIS_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_R5FSS0_CORE0_AXIS_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_L2_BANK_D_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_L2_BANK_C_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_L2_BANK_B_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_L2_BANK_A_ADDR_ERR2
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-390. MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE		Reserved
17	MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_HSM_ADDR_ERR2	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
16	MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_R5FSS11_AHB_ADDR_ERR2	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n

Table 2-390. MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_R5FSS0_CORE1_AHB_ADDR_ERR2	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
14	MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_R5FSS1_CORE0_AHB_ADDR_ERR2	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
13	MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_R5FSS0_CORE0_AHB_ADDR_ERR2	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
12	MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_SCRM2SCRP1_ADDR_ERR2	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
11	MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_SCRM2SCRP0_ADDR_ERR2	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
10	MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_QSPI_ADDR_ERR2	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
9	MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_MBOX_ADDR_ERR2	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
8	MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_DTHE_A_ADDR_ERR2	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
7	MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_R5FSS11_AXIS_ADDR_ERR2	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
6	MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_R5FSS0_CORE1_AXIS_ADDR_ERR2	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
5	MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_R5FSS1_CORE0_AXIS_ADDR_ERR2	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
4	MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_R5FSS0_CORE0_AXIS_ADDR_ERR2	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
3	MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_L2_BANK_D_ADDR_ERR2	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
2	MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_L2_BANK_C_ADDR_ERR2	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
1	MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_L2_BANK_B_ADDR_ERR2	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
0	MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_L2_BANK_A_ADDR_ERR2	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n

2.3.137 CFG0_MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW Registers

2.3.137.1 CFG0_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW Register (Offset = C028h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-391. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 C028h

Figure 2-194. MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_HSM_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_R5FSS11_AHB_ADDR_ERR2
NONE														R/W1TC	R/W1TC
0														0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_R5FSS0_CORE1_AHB_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_R5FSS1_CORE0_AHB_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_R5FSS0_CORE0_AHB_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_SCRM2SCRP1_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_SCRM2SCRP0_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_QSPI_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_MBOX_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_DTHE_A_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_R5FSS11_AXIS_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_R5FSS0_CORE1_AXIS_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_R5FSS1_CORE0_AXIS_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_R5FSS0_CORE0_AXIS_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_L2_BANK_D_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_L2_BANK_C_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_L2_BANK_B_ADDR_ERR2	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_L2_BANK_A_ADDR_ERR2
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-392. MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE		Reserved
17	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_HSM_ADDR_ERR2	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n

Table 2-392. MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_R5FSS11_AHB_ADDR_ERR2	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
15	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_R5FSS0_CORE1_AHB_ADDR_ERR2	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
14	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_R5FSS1_CORE0_AHB_ADDR_ERR2	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
13	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_R5FSS0_CORE0_AHB_ADDR_ERR2	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
12	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_SCRM2SCRP1_ADDR_ERR2	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
11	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_SCRM2SCRP0_ADDR_ERR2	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
10	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_QSPI_ADDR_ERR2	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
9	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_MBOX_ADDR_ERR2	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
8	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_DTHE_A_ADDR_ERR2	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
7	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_R5FSS11_AXIS_ADDR_ERR2	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
6	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_R5FSS0_CORE1_AXIS_ADDR_ERR2	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
5	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_R5FSS1_CORE0_AXIS_ADDR_ERR2	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
4	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_R5FSS0_CORE0_AXIS_ADDR_ERR2	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
3	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_L2_BANK_D_ADDR_ERR2	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
2	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_L2_BANK_C_ADDR_ERR2	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
1	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_L2_BANK_B_ADDR_ERR2	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n

Table 2-392. MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_L2_BANK_A_ADDR_ERR2	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n

2.3.138 CFG0_MPU_PROT_ERRAGG_R5SS1_CPU0_MASK Registers

2.3.138.1 CFG0_PROT_ERRAGG_R5SS1_CPU0_MASK Register (Offset = C030h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-393. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 C030h

Figure 2-195. MPU_PROT_ERRAGG_R5SS1_CPU0_MASK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														MPU_PROT_INTR_ERRAGG2_MASK_MPU_HSM_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_MASK_MPU_R5FSS11_AHB_PROT_ERR2
NONE														R/W	R/W
0														0h	0h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPU_PROT_INTR_ERRAGG2_MASK_MPU_R5FSS0_CORE1_AHB_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_MASK_MPU_R5FSS1_CORE0_AHB_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_MASK_MPU_R5FSS0_CORE0_AHB_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_MASK_MPU_SCRM2SCRP1_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_MASK_MPU_SCRM2SCRP0_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_MASK_MPU_QSPI_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_MASK_MPU_MBOX_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_MASK_MPU_DTHE_A_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_MASK_MPU_R5FSS11_AXIS_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_MASK_MPU_R5FSS0_CORE1_AXIS_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_MASK_MPU_R5FSS1_CORE0_AXIS_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_MASK_MPU_R5FSS0_CORE0_AXIS_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_MASK_MPU_L2_BANK_D_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_MASK_MPU_L2_BANK_C_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_MASK_MPU_L2_BANK_B_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_MASK_MPU_L2_BANK_A_PROT_ERR2
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-394. MPU_PROT_ERRAGG_R5SS1_CPU0_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE		Reserved
17	MPU_PROT_INTR_ERRAGG2_MASK_MPU_HSM_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
16	MPU_PROT_INTR_ERRAGG2_MASK_MPU_R5FSS11_AHB_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
15	MPU_PROT_INTR_ERRAGG2_MASK_MPU_R5FSS0_CORE1_AHB_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n

Table 2-394. MPU_PROT_ERRAGG_R5SS1_CPU0_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	MPU_PROT_INTR_ERRAGG2_MASK_MPU_R5FSS1_CORE0_AHB_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
13	MPU_PROT_INTR_ERRAGG2_MASK_MPU_R5FSS0_CORE0_AHB_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
12	MPU_PROT_INTR_ERRAGG2_MASK_MPU_SCRM2SCRP1_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
11	MPU_PROT_INTR_ERRAGG2_MASK_MPU_SCRM2SCRP0_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
10	MPU_PROT_INTR_ERRAGG2_MASK_MPU_QSPI_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
9	MPU_PROT_INTR_ERRAGG2_MASK_MPU_MBOX_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
8	MPU_PROT_INTR_ERRAGG2_MASK_MPU_DTHE_A_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
7	MPU_PROT_INTR_ERRAGG2_MASK_MPU_R5FSS11_AXIS_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
6	MPU_PROT_INTR_ERRAGG2_MASK_MPU_R5FSS0_CORE1_AXIS_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
5	MPU_PROT_INTR_ERRAGG2_MASK_MPU_R5FSS1_CORE0_AXIS_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
4	MPU_PROT_INTR_ERRAGG2_MASK_MPU_R5FSS0_CORE0_AXIS_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
3	MPU_PROT_INTR_ERRAGG2_MASK_MPU_L2_BANK_D_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
2	MPU_PROT_INTR_ERRAGG2_MASK_MPU_L2_BANK_C_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
1	MPU_PROT_INTR_ERRAGG2_MASK_MPU_L2_BANK_B_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
0	MPU_PROT_INTR_ERRAGG2_MASK_MPU_L2_BANK_A_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n

2.3.139 CFG0_MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS Registers

2.3.139.1 CFG0_PROT_ERRAGG_R5SS1_CPU0_STATUS Register (Offset = C034h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-395. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 C034h

Figure 2-196. MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														MPU_PROT_INTR_ERRAGG2_STATUS_MPU_HSM_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_STATUS_MPU_R5FSS11_AHB_PROT_ERR2
NONE														R/W1TC	R/W1TC
0														0h	0h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPU_PROT_INTR_ERRAGG2_STATUS_MPU_R5FSS0_CORE1_AHB_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_STATUS_MPU_R5FSS1_CORE0_AHB_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_STATUS_MPU_R5FSS0_CORE0_AHB_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_STATUS_MPU_SCRM2SCRP1_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_STATUS_MPU_SCRM2SCRP0_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_STATUS_MPU_QSPI_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_STATUS_MPU_MBOX_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_STATUS_MPU_DTHE_A_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_STATUS_MPU_R5FSS11_AXIS_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_STATUS_MPU_R5FSS0_CORE1_AXIS_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_STATUS_MPU_R5FSS1_CORE0_AXIS_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_STATUS_MPU_R5FSS0_CORE0_AXIS_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_STATUS_MPU_L2_BANK_D_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_STATUS_MPU_L2_BANK_C_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_STATUS_MPU_L2_BANK_B_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_STATUS_MPU_L2_BANK_A_PROT_ERR2
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-396. MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE		Reserved
17	MPU_PROT_INTR_ERRAGG2_STATUS_MPU_HSM_PROT_ERR2	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
16	MPU_PROT_INTR_ERRAGG2_STATUS_MPU_R5FSS11_AHB_PROT_ERR2	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n

Table 2-396. MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	MPU_PROT_INTR_ERRAGG2_STATUS_MPU_R5FSS0_CORE1_AHB_PROT_ERR2	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
14	MPU_PROT_INTR_ERRAGG2_STATUS_MPU_R5FSS1_CORE0_AHB_PROT_ERR2	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
13	MPU_PROT_INTR_ERRAGG2_STATUS_MPU_R5FSS0_CORE0_AHB_PROT_ERR2	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
12	MPU_PROT_INTR_ERRAGG2_STATUS_MPU_SCRM2SCRP1_PROT_ERR2	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
11	MPU_PROT_INTR_ERRAGG2_STATUS_MPU_SCRM2SCRP0_PROT_ERR2	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
10	MPU_PROT_INTR_ERRAGG2_STATUS_MPU_QSPI_PROT_ERR2	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
9	MPU_PROT_INTR_ERRAGG2_STATUS_MPU_MBOX_PROT_ERR2	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
8	MPU_PROT_INTR_ERRAGG2_STATUS_MPU_DTHE_A_PROT_ERR2	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
7	MPU_PROT_INTR_ERRAGG2_STATUS_MPU_R5FSS11_AXIS_PROT_ERR2	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
6	MPU_PROT_INTR_ERRAGG2_STATUS_MPU_R5FSS0_CORE1_AXIS_PROT_ERR2	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
5	MPU_PROT_INTR_ERRAGG2_STATUS_MPU_R5FSS1_CORE0_AXIS_PROT_ERR2	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
4	MPU_PROT_INTR_ERRAGG2_STATUS_MPU_R5FSS0_CORE0_AXIS_PROT_ERR2	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
3	MPU_PROT_INTR_ERRAGG2_STATUS_MPU_L2_BANK_D_PROT_ERR2	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
2	MPU_PROT_INTR_ERRAGG2_STATUS_MPU_L2_BANK_C_PROT_ERR2	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
1	MPU_PROT_INTR_ERRAGG2_STATUS_MPU_L2_BANK_B_PROT_ERR2	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
0	MPU_PROT_INTR_ERRAGG2_STATUS_MPU_L2_BANK_A_PROT_ERR2	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n

2.3.140 CFG0_MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW Registers

2.3.140.1 CFG0_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW Register (Offset = C038h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-397. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D0 C038h

Figure 2-197. MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_HSM_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_R5FSS11_AHB_PROT_ERR2
NONE														R/W1TC	R/W1TC
0														0h	0h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_R5FSS0_CORE1_AHB_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_R5FSS1_CORE0_AHB_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_R5FSS0_CORE0_AHB_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_SCRM2SCRP1_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_SCRM2SCRP0_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_QSPI_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_MBOX_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_DTHE_A_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_R5FSS11_AXIS_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_R5FSS0_CORE1_AXIS_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_R5FSS1_CORE0_AXIS_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_R5FSS0_CORE0_AXIS_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_L2_BANK_D_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_L2_BANK_C_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_L2_BANK_B_PROT_ERR2	MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_L2_BANK_A_PROT_ERR2
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-398. MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE		Reserved
17	MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_HSM_PROT_ERR2	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n

Table 2-398. MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_R5FSS11_AHB_PROT_ERR2	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
15	MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_R5FSS0_CORE1_AHB_PROT_ERR2	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
14	MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_R5FSS1_CORE0_AHB_PROT_ERR2	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
13	MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_R5FSS0_CORE0_AHB_PROT_ERR2	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
12	MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_SCRM2SCRP1_PROT_ERR2	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
11	MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_SCRM2SCRP0_PROT_ERR2	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
10	MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_QSPI_PROT_ERR2	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
9	MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_MBOX_PROT_ERR2	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
8	MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_DTHE_A_PROT_ERR2	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
7	MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_R5FSS11_AXIS_PROT_ERR2	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
6	MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_R5FSS0_CORE1_AXIS_PROT_ERR2	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
5	MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_R5FSS1_CORE0_AXIS_PROT_ERR2	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
4	MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_R5FSS0_CORE0_AXIS_PROT_ERR2	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
3	MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_L2_BANK_D_PROT_ERR2	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
2	MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_L2_BANK_C_PROT_ERR2	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
1	MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_L2_BANK_B_PROT_ERR2	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n

Table 2-398. MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_L2_BANK_A_PROT_ERR2	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n

2.3.141 CFG0_R5SS1_CORE1_MBOX_WRITE_DONE Registers

2.3.141.1 CFG0_CORE1_MBOX_WRITE_DONE Register (Offset = 10000h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-399. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 0000h

Figure 2-198. R5SS1_CORE1_MBOX_WRITE_DONE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			MSS_R5FSS11_MBOX_WRITE_DONE_PROC_7	RESERVED			MSS_R5FSS11_MBOX_WRITE_DONE_PROC_6	RESERVED			MSS_R5FSS11_MBOX_WRITE_DONE_PROC_5	RESERVED			MSS_R5FSS11_MBOX_WRITE_DONE_PROC_4
NONE			R/W	NONE			R/W	NONE			R/W	NONE			R/W
0			0h	0			0h	0			0h	0			0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			MSS_R5FSS11_MBOX_WRITE_DONE_PROC_3	RESERVED			MSS_R5FSS11_MBOX_WRITE_DONE_PROC_2	RESERVED			MSS_R5FSS11_MBOX_WRITE_DONE_PROC_1	RESERVED			MSS_R5FSS11_MBOX_WRITE_DONE_PROC_0
NONE			R/W	NONE			R/W	NONE			R/W	NONE			R/W
0			0h	0			0h	0			0h	0			0h

Access Types Legend

Table 2-400. R5SS1_CORE1_MBOX_WRITE_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28	MSS_R5FSS11_MBOX_WRITE_DONE_PROC_7	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 7 Reset Source: mod_g_rst_n
27:25	RESERVED	NONE		Reserved
24	MSS_R5FSS11_MBOX_WRITE_DONE_PROC_6	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 6 Reset Source: mod_g_rst_n
23:21	RESERVED	NONE		Reserved
20	MSS_R5FSS11_MBOX_WRITE_DONE_PROC_5	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 5 Reset Source: mod_g_rst_n
19:17	RESERVED	NONE		Reserved
16	MSS_R5FSS11_MBOX_WRITE_DONE_PROC_4	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 4 Reset Source: mod_g_rst_n
15:13	RESERVED	NONE		Reserved

Table 2-400. R5SS1_CORE1_MBOX_WRITE_DONE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	MSS_R5FSS11_MBOX_WRITE_DONE_PROC_3	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 3 Reset Source: mod_g_rst_n
11:9	RESERVED	NONE		Reserved
8	MSS_R5FSS11_MBOX_WRITE_DONE_PROC_2	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 2 Reset Source: mod_g_rst_n
7:5	RESERVED	NONE		Reserved
4	MSS_R5FSS11_MBOX_WRITE_DONE_PROC_1	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 1 Reset Source: mod_g_rst_n
3:1	RESERVED	NONE		Reserved
0	MSS_R5FSS11_MBOX_WRITE_DONE_PROC_0	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 0 Reset Source: mod_g_rst_n

2.3.142 CFG0_R5SS1_CORE1_MBOX_READ_REQ Registers

2.3.142.1 CFG0_CORE1_MBOX_READ_REQ Register (Offset = 10004h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-401. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 0004h

Figure 2-199. R5SS1_CORE1_MBOX_READ_REQ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			MSS_R5FSS11_MBOX_READ_REQ_PROC_7	RESERVED			MSS_R5FSS11_MBOX_READ_REQ_PROC_6	RESERVED			MSS_R5FSS11_MBOX_READ_REQ_PROC_5	RESERVED			MSS_R5FSS11_MBOX_READ_REQ_PROC_4
NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC
0			0h	0			0h	0			0h	0			0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			MSS_R5FSS11_MBOX_READ_REQ_PROC_3	RESERVED			MSS_R5FSS11_MBOX_READ_REQ_PROC_2	RESERVED			MSS_R5FSS11_MBOX_READ_REQ_PROC_1	RESERVED			MSS_R5FSS11_MBOX_READ_REQ_PROC_0
NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC
0			0h	0			0h	0			0h	0			0h

Access Types Legend

Table 2-402. R5SS1_CORE1_MBOX_READ_REQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28	MSS_R5FSS11_MBOX_READ_REQ_PROC_7	R/W1TC	0h	This is request from processor 7 to mss_CR5B. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
27:25	RESERVED	NONE		Reserved
24	MSS_R5FSS11_MBOX_READ_REQ_PROC_6	R/W1TC	0h	This is request from processor 6 to mss_CR5B. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
23:21	RESERVED	NONE		Reserved
20	MSS_R5FSS11_MBOX_READ_REQ_PROC_5	R/W1TC	0h	This is request from processor 5 to mss_CR5B. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
19:17	RESERVED	NONE		Reserved
16	MSS_R5FSS11_MBOX_READ_REQ_PROC_4	R/W1TC	0h	This is request from processor 4 to mss_CR5B. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
15:13	RESERVED	NONE		Reserved
12	MSS_R5FSS11_MBOX_READ_REQ_PROC_3	R/W1TC	0h	This is request from processor 3 to mss_CR5B. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
11:9	RESERVED	NONE		Reserved

Table 2-402. R5SS1_CORE1_MBOX_READ_REQ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	MSS_R5FSS11_MBOX_READ_REQ_PROC_2	R/W1TC	0h	This is request from processor 2 to mss_CR5B. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
7:5	RESERVED	NONE		Reserved
4	MSS_R5FSS11_MBOX_READ_REQ_PROC_1	R/W1TC	0h	This is request from processor 1 to mss_CR5B. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
3:1	RESERVED	NONE		Reserved
0	MSS_R5FSS11_MBOX_READ_REQ_PROC_0	R/W1TC	0h	This is request from processor 0 to mss_CR5B. Requesting it to read from mailbox. Reset Source: mod_g_rst_n

2.3.143 CFG0_R5SS1_CORE1_MBOX_READ_DONE_ACK Registers

2.3.143.1 CFG0_CORE1_MBOX_READ_DONE_ACK Register (Offset = 10008h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-403. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 0008h

Figure 2-200. R5SS1_CORE1_MBOX_READ_DONE_ACK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MSS_R5FSS11_MBOX_READ_DONE_ACK_PROC							
NONE								R/W							
0								0h							

Access Types Legend

Table 2-404. R5SS1_CORE1_MBOX_READ_DONE_ACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	MSS_R5FSS11_MBOX_READ_DONE_ACK_PROC	R/W	0h	Write pulse bit field: For bits 0 to 7: Wrting 1'b1 : Generates pulse interrupt to corresponding proc from MSS_CR5 Reset Source: mod_g_rst_n

2.3.144 CFG0_R5SS1_CORE1_MBOX_READ_DONE Registers

2.3.144.1 CFG0_CORE1_MBOX_READ_DONE Register (Offset = 1000Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-405. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 000Ch

Figure 2-201. R5SS1_CORE1_MBOX_READ_DONE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			MSS_R5FSS11_MBOX_READ_DONE_PROC_7	RESERVED			MSS_R5FSS11_MBOX_READ_DONE_PROC_6	RESERVED			MSS_R5FSS11_MBOX_READ_DONE_PROC_5	RESERVED			MSS_R5FSS11_MBOX_READ_DONE_PROC_4
NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC
0			0h	0			0h	0			0h	0			0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			MSS_R5FSS11_MBOX_READ_DONE_PROC_3	RESERVED			MSS_R5FSS11_MBOX_READ_DONE_PROC_2	RESERVED			MSS_R5FSS11_MBOX_READ_DONE_PROC_1	RESERVED			MSS_R5FSS11_MBOX_READ_DONE_PROC_0
NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC
0			0h	0			0h	0			0h	0			0h

Access Types Legend

Table 2-406. R5SS1_CORE1_MBOX_READ_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28	MSS_R5FSS11_MBOX_READ_DONE_PROC_7	R/W1TC	0h	This register should be written once finishing reading from CR5B's mailbox written by proc 7 Reset Source: mod_g_rst_n
27:25	RESERVED	NONE		Reserved
24	MSS_R5FSS11_MBOX_READ_DONE_PROC_6	R/W1TC	0h	This register should be written once finishing reading from CR5B's mailbox written by proc 6 Reset Source: mod_g_rst_n
23:21	RESERVED	NONE		Reserved
20	MSS_R5FSS11_MBOX_READ_DONE_PROC_5	R/W1TC	0h	This register should be written once finishing reading from CR5B's mailbox written by proc 5 Reset Source: mod_g_rst_n
19:17	RESERVED	NONE		Reserved
16	MSS_R5FSS11_MBOX_READ_DONE_PROC_4	R/W1TC	0h	This register should be written once finishing reading from CR5B's mailbox written by proc 4 Reset Source: mod_g_rst_n
15:13	RESERVED	NONE		Reserved
12	MSS_R5FSS11_MBOX_READ_DONE_PROC_3	R/W1TC	0h	This register should be written once finishing reading from CR5B's mailbox written by proc 3 Reset Source: mod_g_rst_n

Table 2-406. R5SS1_CORE1_MBOX_READ_DONE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:9	RESERVED	NONE		Reserved
8	MSS_R5FSS11_MBOX_READ_DONE_PROC_2	R/W1TC	0h	This register should be written once finishing reading from CR5B's mailbox written by proc 2 Reset Source: mod_g_rst_n
7:5	RESERVED	NONE		Reserved
4	MSS_R5FSS11_MBOX_READ_DONE_PROC_1	R/W1TC	0h	This register should be written once finishing reading from CR5B's mailbox written by proc 1 Reset Source: mod_g_rst_n
3:1	RESERVED	NONE		Reserved
0	MSS_R5FSS11_MBOX_READ_DONE_PROC_0	R/W1TC	0h	This register should be written once finishing reading from CR5B's mailbox written by proc 0 Reset Source: mod_g_rst_n

2.3.145 CFG0_R5SS1_CORE1_SW_INT Registers

2.3.145.1 CFG0_CORE1_SW_INT Register (Offset = 10010h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-407. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 0010h

Figure 2-202. R5SS1_CORE1_SW_INT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															MSS_SW_INT_R5SS1_CORE1_PULSE
NONE															R/W
0															0h

Access Types Legend

Table 2-408. R5SS1_CORE1_SW_INT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	MSS_SW_INT_R5SS1_CORE1_PULSE	R/W	0h	Write_pulse bit field: writing 1'b1 to each bit will trigger MSS_SW_INT respectively to CR5A/B. Reset Source: mod_g_rst_n

2.3.146 CFG0_MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK Registers

2.3.146.1 CFG0_ADDR_ERRAGG_R5SS1_CPU1_MASK Register (Offset = 10020h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-409. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 0020h

Figure 2-203. MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														MPU_ADDR_INTR_ERRAGG3_MASK_MPU_HSM_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_MASK_MPU_R5FSS11_AHB_ADDR_ERR3
NONE														R/W	R/W
0														0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPU_ADDR_INTR_ERRAGG3_MASK_MPU_R5FSS0_CORE1_AHB_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_MASK_MPU_R5FSS1_CORE0_AHB_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_MASK_MPU_R5FSS0_CORE0_AHB_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_MASK_MPU_SCRM2SCRP1_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_MASK_MPU_SCRM2SCRP0_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_MASK_MPU_QSPI_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_MASK_MPU_MBOX_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_MASK_MPU_DTHE_A_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_MASK_MPU_R5FSS11_AXIS_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_MASK_MPU_R5FSS0_CORE1_AXIS_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_MASK_MPU_R5FSS1_CORE0_AXIS_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_MASK_MPU_R5FSS0_CORE0_AXIS_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_MASK_MPU_L2_BANK_D_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_MASK_MPU_L2_BANK_C_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_MASK_MPU_L2_BANK_B_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_MASK_MPU_L2_BANK_A_ADDR_ERR3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-410. MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE		Reserved
17	MPU_ADDR_INTR_ERRAGG3_MASK_MPU_HSM_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
16	MPU_ADDR_INTR_ERRAGG3_MASK_MPU_R5FSS11_AHB_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
15	MPU_ADDR_INTR_ERRAGG3_MASK_MPU_R5FSS0_CORE1_AHB_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n

Table 2-410. MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	MPU_ADDR_INTR_ERRAGG3_MASK_MPU_R5FSS1_CORE0_AHB_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
13	MPU_ADDR_INTR_ERRAGG3_MASK_MPU_R5FSS0_CORE0_AHB_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
12	MPU_ADDR_INTR_ERRAGG3_MASK_MPU_SCRM2SCRP1_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
11	MPU_ADDR_INTR_ERRAGG3_MASK_MPU_SCRM2SCRP0_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
10	MPU_ADDR_INTR_ERRAGG3_MASK_MPU_QSPI_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
9	MPU_ADDR_INTR_ERRAGG3_MASK_MPU_MBOX_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
8	MPU_ADDR_INTR_ERRAGG3_MASK_MPU_DTHE_A_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
7	MPU_ADDR_INTR_ERRAGG3_MASK_MPU_R5FSS11_AXIS_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
6	MPU_ADDR_INTR_ERRAGG3_MASK_MPU_R5FSS0_CORE1_AXIS_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
5	MPU_ADDR_INTR_ERRAGG3_MASK_MPU_R5FSS1_CORE0_AXIS_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
4	MPU_ADDR_INTR_ERRAGG3_MASK_MPU_R5FSS0_CORE0_AXIS_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
3	MPU_ADDR_INTR_ERRAGG3_MASK_MPU_L2_BANK_D_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
2	MPU_ADDR_INTR_ERRAGG3_MASK_MPU_L2_BANK_C_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
1	MPU_ADDR_INTR_ERRAGG3_MASK_MPU_L2_BANK_B_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
0	MPU_ADDR_INTR_ERRAGG3_MASK_MPU_L2_BANK_A_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n

2.3.147 CFG0_MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS Registers

2.3.147.1 CFG0_ADDR_ERRAGG_R5SS1_CPU1_STATUS Register (Offset = 10024h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-411. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 0024h

Figure 2-204. MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_HSM_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_R5FSS11_AHB_ADDR_ERR3
NONE														R/W1TC	R/W1TC
0														0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_R5FSS0_CORE1_AHB_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_R5FSS1_CORE0_AHB_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_R5FSS0_CORE0_AHB_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_SCRM2SCRP1_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_SCRM2SCRP0_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_QSPI_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_MBOX_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_DTHE_A_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_R5FSS11_AXIS_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_R5FSS0_CORE1_AXIS_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_R5FSS1_CORE0_AXIS_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_R5FSS0_CORE0_AXIS_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_L2_BANK_D_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_L2_BANK_C_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_L2_BANK_B_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_L2_BANK_A_ADDR_ERR3
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-412. MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE		Reserved
17	MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_HSM_ADDR_ERR3	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
16	MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_R5FSS11_AHB_ADDR_ERR3	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n

Table 2-412. MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_R5FSS0_CORE1_AHB_ADDR_ERR3	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
14	MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_R5FSS1_CORE0_AHB_ADDR_ERR3	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
13	MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_R5FSS0_CORE0_AHB_ADDR_ERR3	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
12	MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_SCRM2SCRP1_ADDR_ERR3	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
11	MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_SCRM2SCRP0_ADDR_ERR3	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
10	MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_QSPI_ADDR_ERR3	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
9	MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_MBOX_ADDR_ERR3	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
8	MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_DTHE_A_ADDR_ERR3	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
7	MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_R5FSS11_AXIS_ADDR_ERR3	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
6	MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_R5FSS0_CORE1_AXIS_ADDR_ERR3	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
5	MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_R5FSS1_CORE0_AXIS_ADDR_ERR3	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
4	MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_R5FSS0_CORE0_AXIS_ADDR_ERR3	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
3	MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_L2_BANK_D_ADDR_ERR3	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
2	MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_L2_BANK_C_ADDR_ERR3	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
1	MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_L2_BANK_B_ADDR_ERR3	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
0	MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_L2_BANK_A_ADDR_ERR3	R/W1TC	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n

2.3.148 CFG0_MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW Registers

2.3.148.1 CFG0_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW Register (Offset = 10028h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-413. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 0028h

Figure 2-205. MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_HSM_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_R5FSS11_AHB_ADDR_ERR3
NONE														R/W1TC	R/W1TC
0														0h	0h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_R5FSS0_CORE1_AHB_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_R5FSS1_CORE0_AHB_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_R5FSS0_CORE0_AHB_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_SCRM2SCRP1_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_SCRM2SCRP0_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_QSPI_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_MBOX_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_DTHE_A_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_R5FSS11_AXIS_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_R5FSS0_CORE1_AXIS_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_R5FSS1_CORE0_AXIS_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_R5FSS0_CORE0_AXIS_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_L2_BANK_D_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_L2_BANK_C_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_L2_BANK_B_ADDR_ERR3	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_L2_BANK_A_ADDR_ERR3
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-414. MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE		Reserved
17	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_HSM_ADDR_ERR3	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n

Table 2-414. MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_R5FSS11_AHB_ADDR_ERR3	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
15	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_R5FSS0_CORE1_AHB_ADDR_ERR3	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
14	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_R5FSS1_CORE0_AHB_ADDR_ERR3	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
13	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_R5FSS0_CORE0_AHB_ADDR_ERR3	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
12	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_SCRM2SCRP1_ADDR_ERR3	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
11	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_SCRM2SCRP0_ADDR_ERR3	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
10	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_QSPI_ADDR_ERR3	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
9	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_MBOX_ADDR_ERR3	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
8	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_DTHE_A_ADDR_ERR3	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
7	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_R5FSS11_AXIS_ADDR_ERR3	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
6	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_R5FSS0_CORE1_AXIS_ADDR_ERR3	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
5	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_R5FSS1_CORE0_AXIS_ADDR_ERR3	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
4	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_R5FSS0_CORE0_AXIS_ADDR_ERR3	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
3	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_L2_BANK_D_ADDR_ERR3	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
2	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_L2_BANK_C_ADDR_ERR3	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
1	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_L2_BANK_B_ADDR_ERR3	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n

Table 2-414. MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_L2_BANK_A_ADDR_ERR3	R/W1TC	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n

2.3.149 CFG0_MPU_PROT_ERRAGG_R5SS1_CPU1_MASK Registers

2.3.149.1 CFG0_PROT_ERRAGG_R5SS1_CPU1_MASK Register (Offset = 10030h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-415. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 0030h

Figure 2-206. MPU_PROT_ERRAGG_R5SS1_CPU1_MASK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														MPU_PROT_INTR_ERRAGG3_MASK_MPU_HSM_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_MASK_MPU_R5FSS11_AHB_PROT_ERR3
NONE														R/W	R/W
0														0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPU_PROT_INTR_ERRAGG3_MASK_MPU_R5FSS0_CORE1_AHB_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_MASK_MPU_R5FSS1_CORE0_AHB_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_MASK_MPU_R5FSS0_CORE0_AHB_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_MASK_MPU_SCRM2SCRP1_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_MASK_MPU_SCRM2SCRP0_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_MASK_MPU_QSPI_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_MASK_MPU_MBOX_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_MASK_MPU_DTHE_A_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_MASK_MPU_R5FSS11_AXIS_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_MASK_MPU_R5FSS0_CORE1_AXIS_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_MASK_MPU_R5FSS1_CORE0_AXIS_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_MASK_MPU_R5FSS0_CORE0_AXIS_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_MASK_MPU_L2_BANK_D_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_MASK_MPU_L2_BANK_C_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_MASK_MPU_L2_BANK_B_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_MASK_MPU_L2_BANK_A_PROT_ERR3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-416. MPU_PROT_ERRAGG_R5SS1_CPU1_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE		Reserved
17	MPU_PROT_INTR_ERRAGG3_MASK_MPU_HSM_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
16	MPU_PROT_INTR_ERRAGG3_MASK_MPU_R5FSS11_AHB_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
15	MPU_PROT_INTR_ERRAGG3_MASK_MPU_R5FSS0_CORE1_AHB_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n

Table 2-416. MPU_PROT_ERRAGG_R5SS1_CPU1_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	MPU_PROT_INTR_ERRAGG3_MASK_MPU_R5FSS1_CORE0_AHB_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
13	MPU_PROT_INTR_ERRAGG3_MASK_MPU_R5FSS0_CORE0_AHB_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
12	MPU_PROT_INTR_ERRAGG3_MASK_MPU_SCRM2SCRP1_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
11	MPU_PROT_INTR_ERRAGG3_MASK_MPU_SCRM2SCRP0_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
10	MPU_PROT_INTR_ERRAGG3_MASK_MPU_QSPI_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
9	MPU_PROT_INTR_ERRAGG3_MASK_MPU_MBOX_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
8	MPU_PROT_INTR_ERRAGG3_MASK_MPU_DTHE_A_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
7	MPU_PROT_INTR_ERRAGG3_MASK_MPU_R5FSS11_AXIS_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
6	MPU_PROT_INTR_ERRAGG3_MASK_MPU_R5FSS0_CORE1_AXIS_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
5	MPU_PROT_INTR_ERRAGG3_MASK_MPU_R5FSS1_CORE0_AXIS_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
4	MPU_PROT_INTR_ERRAGG3_MASK_MPU_R5FSS0_CORE0_AXIS_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
3	MPU_PROT_INTR_ERRAGG3_MASK_MPU_L2_BANK_D_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
2	MPU_PROT_INTR_ERRAGG3_MASK_MPU_L2_BANK_C_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
1	MPU_PROT_INTR_ERRAGG3_MASK_MPU_L2_BANK_B_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
0	MPU_PROT_INTR_ERRAGG3_MASK_MPU_L2_BANK_A_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n

2.3.150 CFG0_MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS Registers

2.3.150.1 CFG0_PROT_ERRAGG_R5SS1_CPU1_STATUS Register (Offset = 10034h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-417. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 0034h

Figure 2-207. MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														MPU_PROT_INTR_ERRAGG3_STATUS_MPU_HSM_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_STATUS_MPU_R5FSS11_AHB_PROT_ERR3
NONE														R/W1TC	R/W1TC
0														0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPU_PROT_INTR_ERRAGG3_STATUS_MPU_R5FSS0_CORE1_AHB_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_STATUS_MPU_R5FSS1_CORE0_AHB_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_STATUS_MPU_R5FSS0_CORE0_AHB_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_STATUS_MPU_SCRM2SCRP1_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_STATUS_MPU_SCRM2SCRP0_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_STATUS_MPU_QSPI_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_STATUS_MPU_MBOX_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_STATUS_MPU_DTHE_A_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_STATUS_MPU_R5FSS11_AXIS_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_STATUS_MPU_R5FSS0_CORE1_AXIS_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_STATUS_MPU_R5FSS1_CORE0_AXIS_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_STATUS_MPU_R5FSS0_CORE0_AXIS_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_STATUS_MPU_L2_BANK_D_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_STATUS_MPU_L2_BANK_C_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_STATUS_MPU_L2_BANK_B_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_STATUS_MPU_L2_BANK_A_PROT_ERR3
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-418. MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE		Reserved
17	MPU_PROT_INTR_ERRAGG3_STATUS_MPU_HSM_PROT_ERR3	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
16	MPU_PROT_INTR_ERRAGG3_STATUS_MPU_R5FSS11_AHB_PROT_ERR3	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n

Table 2-418. MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	MPU_PROT_INTR_ERRAGG3_STATUS_MPU_R5FSS0_CORE1_AHB_PROT_ERR3	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
14	MPU_PROT_INTR_ERRAGG3_STATUS_MPU_R5FSS1_CORE0_AHB_PROT_ERR3	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
13	MPU_PROT_INTR_ERRAGG3_STATUS_MPU_R5FSS0_CORE0_AHB_PROT_ERR3	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
12	MPU_PROT_INTR_ERRAGG3_STATUS_MPU_SCRM2SCRP1_PROT_ERR3	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
11	MPU_PROT_INTR_ERRAGG3_STATUS_MPU_SCRM2SCRP0_PROT_ERR3	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
10	MPU_PROT_INTR_ERRAGG3_STATUS_MPU_QSPI_PROT_ERR3	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
9	MPU_PROT_INTR_ERRAGG3_STATUS_MPU_MBOX_PROT_ERR3	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
8	MPU_PROT_INTR_ERRAGG3_STATUS_MPU_DTHE_A_PROT_ERR3	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
7	MPU_PROT_INTR_ERRAGG3_STATUS_MPU_R5FSS11_AXIS_PROT_ERR3	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
6	MPU_PROT_INTR_ERRAGG3_STATUS_MPU_R5FSS0_CORE1_AXIS_PROT_ERR3	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
5	MPU_PROT_INTR_ERRAGG3_STATUS_MPU_R5FSS1_CORE0_AXIS_PROT_ERR3	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
4	MPU_PROT_INTR_ERRAGG3_STATUS_MPU_R5FSS0_CORE0_AXIS_PROT_ERR3	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
3	MPU_PROT_INTR_ERRAGG3_STATUS_MPU_L2_BANK_D_PROT_ERR3	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
2	MPU_PROT_INTR_ERRAGG3_STATUS_MPU_L2_BANK_C_PROT_ERR3	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
1	MPU_PROT_INTR_ERRAGG3_STATUS_MPU_L2_BANK_B_PROT_ERR3	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
0	MPU_PROT_INTR_ERRAGG3_STATUS_MPU_L2_BANK_A_PROT_ERR3	R/W1TC	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n

2.3.151 CFG0_MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW Registers

2.3.151.1 CFG0_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW Register (Offset = 10038h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-419. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 0038h

Figure 2-208. MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_HSM_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_R5FSS11_AHB_PROT_ERR3
NONE														R/W1TC	R/W1TC
0														0h	0h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_R5FSS0_CORE1_AHB_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_R5FSS1_CORE0_AHB_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_R5FSS0_CORE0_AHB_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_SCRM2SCRP1_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_SCRM2SCRP0_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_QSPI_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_MBOX_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_DTHE_A_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_R5FSS11_AXIS_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_R5FSS0_CORE1_AXIS_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_R5FSS1_CORE0_AXIS_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_R5FSS0_CORE0_AXIS_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_L2_BANK_D_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_L2_BANK_C_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_L2_BANK_B_PROT_ERR3	MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_L2_BANK_A_PROT_ERR3
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-420. MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE		Reserved
17	MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_HSM_PROT_ERR3	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n

Table 2-420. MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_R5FSS11_AHB_PROT_ERR3	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
15	MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_R5FSS0_CORE1_AHB_PROT_ERR3	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
14	MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_R5FSS1_CORE0_AHB_PROT_ERR3	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
13	MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_R5FSS0_CORE0_AHB_PROT_ERR3	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
12	MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_SCRM2SCRP1_PROT_ERR3	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
11	MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_SCRM2SCRP0_PROT_ERR3	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
10	MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_QSPI_PROT_ERR3	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
9	MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_MBOX_PROT_ERR3	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
8	MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_DTHE_A_PROT_ERR3	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
7	MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_R5FSS11_AXIS_PROT_ERR3	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
6	MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_R5FSS0_CORE1_AXIS_PROT_ERR3	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
5	MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_R5FSS1_CORE0_AXIS_PROT_ERR3	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
4	MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_R5FSS0_CORE0_AXIS_PROT_ERR3	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
3	MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_L2_BANK_D_PROT_ERR3	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
2	MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_L2_BANK_C_PROT_ERR3	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n
1	MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_L2_BANK_B_PROT_ERR3	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n

Table 2-420. MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_L2_BANK_A_PROT_ERR3	R/W1TC	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK Reset Source: mod_g_rst_n

2.3.152 CFG0_PRU-ICSS_PRU0_MBOX_WRITE_DONE Registers

2.3.152.1 CFG0_PRU0_MBOX_WRITE_DONE Register (Offset = 14000h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-421. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 4000h

Figure 2-209. PRU-ICSS_PRU0_MBOX_WRITE_DONE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRU-ICSS_PRU0_MBOX_WRITE_DONE_PROC_7	RESERVED			PRU-ICSS_PRU0_MBOX_WRITE_DONE_PROC_6	RESERVED			PRU-ICSS_PRU0_MBOX_WRITE_DONE_PROC_5	RESERVED			PRU-ICSS_PRU0_MBOX_WRITE_DONE_PROC_4
NONE			R/W	NONE			R/W	NONE			R/W	NONE			R/W
0			0h	0			0h	0			0h	0			0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRU-ICSS_PRU0_MBOX_WRITE_DONE_PROC_3	RESERVED			PRU-ICSS_PRU0_MBOX_WRITE_DONE_PROC_2	RESERVED			PRU-ICSS_PRU0_MBOX_WRITE_DONE_PROC_1	RESERVED			PRU-ICSS_PRU0_MBOX_WRITE_DONE_PROC_0
NONE			R/W	NONE			R/W	NONE			R/W	NONE			R/W
0			0h	0			0h	0			0h	0			0h

Access Types Legend

Table 2-422. PRU-ICSS_PRU0_MBOX_WRITE_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28	PRU-ICSS_PRU0_MBOX_WRITE_DONE_PROC_7	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 7 Reset Source: mod_g_rst_n
27:25	RESERVED	NONE		Reserved
24	PRU-ICSS_PRU0_MBOX_WRITE_DONE_PROC_6	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 6 Reset Source: mod_g_rst_n
23:21	RESERVED	NONE		Reserved
20	PRU-ICSS_PRU0_MBOX_WRITE_DONE_PROC_5	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 5 Reset Source: mod_g_rst_n
19:17	RESERVED	NONE		Reserved
16	PRU-ICSS_PRU0_MBOX_WRITE_DONE_PROC_4	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 4 Reset Source: mod_g_rst_n
15:13	RESERVED	NONE		Reserved

Table 2-422. PRU-ICSS_PRU0_MBOX_WRITE_DONE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	PRU-ICSS_PRU0_MBOX_WRITE_DONE_PROC_3	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 3 Reset Source: mod_g_rst_n
11:9	RESERVED	NONE		Reserved
8	PRU-ICSS_PRU0_MBOX_WRITE_DONE_PROC_2	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 2 Reset Source: mod_g_rst_n
7:5	RESERVED	NONE		Reserved
4	PRU-ICSS_PRU0_MBOX_WRITE_DONE_PROC_1	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 1 Reset Source: mod_g_rst_n
3:1	RESERVED	NONE		Reserved
0	PRU-ICSS_PRU0_MBOX_WRITE_DONE_PROC_0	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 0 Reset Source: mod_g_rst_n

2.3.153 CFG0_PRU-ICSS_PRU0_MBOX_READ_REQ Registers

2.3.153.1 CFG0_PRU0_MBOX_READ_REQ Register (Offset = 14004h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-423. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 4004h

Figure 2-210. PRU-ICSS_PRU0_MBOX_READ_REQ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRU-ICSS_PRU0_MBOX_READ_REQ_PROC_7	RESERVED			PRU-ICSS_PRU0_MBOX_READ_REQ_PROC_6	RESERVED			PRU-ICSS_PRU0_MBOX_READ_REQ_PROC_5	RESERVED			PRU-ICSS_PRU0_MBOX_READ_REQ_PROC_4
NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC
0			0h	0			0h	0			0h	0			0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRU-ICSS_PRU0_MBOX_READ_REQ_PROC_3	RESERVED			PRU-ICSS_PRU0_MBOX_READ_REQ_PROC_2	RESERVED			PRU-ICSS_PRU0_MBOX_READ_REQ_PROC_1	RESERVED			PRU-ICSS_PRU0_MBOX_READ_REQ_PROC_0
NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC
0			0h	0			0h	0			0h	0			0h

Access Types Legend

Table 2-424. PRU-ICSS_PRU0_MBOX_READ_REQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28	PRU-ICSS_PRU0_MBOX_READ_REQ_PROC_7	R/W1TC	0h	This is request from processor 7 to corresponding ICSSM_PRU. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
27:25	RESERVED	NONE		Reserved
24	PRU-ICSS_PRU0_MBOX_READ_REQ_PROC_6	R/W1TC	0h	This is request from processor 6 to corresponding ICSSM_PRU. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
23:21	RESERVED	NONE		Reserved
20	PRU-ICSS_PRU0_MBOX_READ_REQ_PROC_5	R/W1TC	0h	This is request from processor 5 to corresponding ICSSM_PRU. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
19:17	RESERVED	NONE		Reserved
16	PRU-ICSS_PRU0_MBOX_READ_REQ_PROC_4	R/W1TC	0h	This is request from processor 4 to corresponding ICSSM_PRU. Requesting it to read from mailbox. Reset Source: mod_g_rst_n

Table 2-424. PRU-ICSS_PRU0_MBOX_READ_REQ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:13	RESERVED	NONE		Reserved
12	PRU-ICSS_PRU0_MBOX_READ_REQ_PROC_3	R/W1TC	0h	This is request from processor 3 to corresponding ICSSM_PRU. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
11:9	RESERVED	NONE		Reserved
8	PRU-ICSS_PRU0_MBOX_READ_REQ_PROC_2	R/W1TC	0h	This is request from processor 2 to corresponding ICSSM_PRU. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
7:5	RESERVED	NONE		Reserved
4	PRU-ICSS_PRU0_MBOX_READ_REQ_PROC_1	R/W1TC	0h	This is request from processor 1 to corresponding ICSSM_PRU. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
3:1	RESERVED	NONE		Reserved
0	PRU-ICSS_PRU0_MBOX_READ_REQ_PROC_0	R/W1TC	0h	This is request from processor 0 to corresponding ICSSM_PRU. Requesting it to read from mailbox. Reset Source: mod_g_rst_n

2.3.154 CFG0_PRU-ICSS_PRU0_MBOX_READ_DONE_ACK Registers

2.3.154.1 CFG0_PRU0_MBOX_READ_DONE_ACK Register (Offset = 14008h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-425. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 4008h

Figure 2-211. PRU-ICSS_PRU0_MBOX_READ_DONE_ACK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRU-ICSS_PRU0_MBOX_READ_DONE_ACK_PROC							
NONE								R/W							
0								0h							

Access Types Legend

Table 2-426. PRU-ICSS_PRU0_MBOX_READ_DONE_ACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	PRU-ICSS_PRU0_MBOX_READ_DONE_ACK_PROC	R/W	0h	Write pulse bit field: For bits 0 to 7: Wrting 1'b1 : Generates pulse interrupt to corresponding proc from ICSSM_PRU0. For bits 8 to 15: Wrting 1'b1 : Generates pulse interrupt to corresponding proc from ICSSM_PRU1. Reset Source: mod_g_rst_n

2.3.155 CFG0_PRU-ICSS_PRU0_MBOX_READ_DONE Registers

2.3.155.1 CFG0_PRU0_MBOX_READ_DONE Register (Offset = 1400Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-427. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 400Ch

Figure 2-212. PRU-ICSS_PRU0_MBOX_READ_DONE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRU-ICSS_PRU0_MBOX_READ_DONE_PROC_7	RESERVED			PRU-ICSS_PRU0_MBOX_READ_DONE_PROC_6	RESERVED			PRU-ICSS_PRU0_MBOX_READ_DONE_PROC_5	RESERVED			PRU-ICSS_PRU0_MBOX_READ_DONE_PROC_4
NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC
0			0h	0			0h	0			0h	0			0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRU-ICSS_PRU0_MBOX_READ_DONE_PROC_3	RESERVED			PRU-ICSS_PRU0_MBOX_READ_DONE_PROC_2	RESERVED			PRU-ICSS_PRU0_MBOX_READ_DONE_PROC_1	RESERVED			PRU-ICSS_PRU0_MBOX_READ_DONE_PROC_0
NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC
0			0h	0			0h	0			0h	0			0h

Access Types Legend

Table 2-428. PRU-ICSS_PRU0_MBOX_READ_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28	PRU-ICSS_PRU0_MBOX_READ_DONE_PROC_7	R/W1TC	0h	This register should be written once finishing reading from corresponding ICSSM_PRU's mailbox written by proc 7 Reset Source: mod_g_rst_n
27:25	RESERVED	NONE		Reserved
24	PRU-ICSS_PRU0_MBOX_READ_DONE_PROC_6	R/W1TC	0h	This register should be written once finishing reading from corresponding ICSSM_PRU's mailbox written by proc 6 Reset Source: mod_g_rst_n
23:21	RESERVED	NONE		Reserved
20	PRU-ICSS_PRU0_MBOX_READ_DONE_PROC_5	R/W1TC	0h	This register should be written once finishing reading from corresponding ICSSM_PRU's mailbox written by proc 5 Reset Source: mod_g_rst_n
19:17	RESERVED	NONE		Reserved
16	PRU-ICSS_PRU0_MBOX_READ_DONE_PROC_4	R/W1TC	0h	This register should be written once finishing reading from corresponding ICSSM_PRU's mailbox written by proc 4 Reset Source: mod_g_rst_n

Table 2-428. PRU-ICSS_PRU0_MBOX_READ_DONE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:13	RESERVED	NONE		Reserved
12	PRU-ICSS_PRU0_MBOX_READ_DONE_PROC_3	R/W1TC	0h	This register should be written once finishing reading from corresponding ICSSM_PRU's mailbox written by proc 3 Reset Source: mod_g_rst_n
11:9	RESERVED	NONE		Reserved
8	PRU-ICSS_PRU0_MBOX_READ_DONE_PROC_2	R/W1TC	0h	This register should be written once finishing reading from corresponding ICSSM_PRU's mailbox written by proc 2 Reset Source: mod_g_rst_n
7:5	RESERVED	NONE		Reserved
4	PRU-ICSS_PRU0_MBOX_READ_DONE_PROC_1	R/W1TC	0h	This register should be written once finishing reading from corresponding ICSSM_PRU's mailbox written by proc 1 Reset Source: mod_g_rst_n
3:1	RESERVED	NONE		Reserved
0	PRU-ICSS_PRU0_MBOX_READ_DONE_PROC_0	R/W1TC	0h	This register should be written once finishing reading from corresponding ICSSM_PRU's mailbox written by proc 0 Reset Source: mod_g_rst_n

2.3.156 CFG0_PRU-ICSS_PRU1_MBOX_WRITE_DONE Registers

2.3.156.1 CFG0_PRU1_MBOX_WRITE_DONE Register (Offset = 14010h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-429. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 4010h

Figure 2-213. PRU-ICSS_PRU1_MBOX_WRITE_DONE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRU-ICSS_PRU1_MBOX_WRITE_DONE_PROC_7	RESERVED			PRU-ICSS_PRU1_MBOX_WRITE_DONE_PROC_6	RESERVED			PRU-ICSS_PRU1_MBOX_WRITE_DONE_PROC_5	RESERVED			PRU-ICSS_PRU1_MBOX_WRITE_DONE_PROC_4
NONE			R/W	NONE			R/W	NONE			R/W	NONE			R/W
0			0h	0			0h	0			0h	0			0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRU-ICSS_PRU1_MBOX_WRITE_DONE_PROC_3	RESERVED			PRU-ICSS_PRU1_MBOX_WRITE_DONE_PROC_2	RESERVED			PRU-ICSS_PRU1_MBOX_WRITE_DONE_PROC_1	RESERVED			PRU-ICSS_PRU1_MBOX_WRITE_DONE_PROC_0
NONE			R/W	NONE			R/W	NONE			R/W	NONE			R/W
0			0h	0			0h	0			0h	0			0h

Access Types Legend

Table 2-430. PRU-ICSS_PRU1_MBOX_WRITE_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28	PRU-ICSS_PRU1_MBOX_WRITE_DONE_PROC_7	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 7 Reset Source: mod_g_rst_n
27:25	RESERVED	NONE		Reserved
24	PRU-ICSS_PRU1_MBOX_WRITE_DONE_PROC_6	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 6 Reset Source: mod_g_rst_n
23:21	RESERVED	NONE		Reserved
20	PRU-ICSS_PRU1_MBOX_WRITE_DONE_PROC_5	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 5 Reset Source: mod_g_rst_n
19:17	RESERVED	NONE		Reserved
16	PRU-ICSS_PRU1_MBOX_WRITE_DONE_PROC_4	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 4 Reset Source: mod_g_rst_n
15:13	RESERVED	NONE		Reserved

Table 2-430. PRU-ICSS_PRU1_MBOX_WRITE_DONE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	PRU-ICSS_PRU1_MBOX_WRITE_DONE_PROC_3	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 3 Reset Source: mod_g_rst_n
11:9	RESERVED	NONE		Reserved
8	PRU-ICSS_PRU1_MBOX_WRITE_DONE_PROC_2	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 2 Reset Source: mod_g_rst_n
7:5	RESERVED	NONE		Reserved
4	PRU-ICSS_PRU1_MBOX_WRITE_DONE_PROC_1	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 1 Reset Source: mod_g_rst_n
3:1	RESERVED	NONE		Reserved
0	PRU-ICSS_PRU1_MBOX_WRITE_DONE_PROC_0	R/W	0h	Write pulse bit field: This register should be written once finishing writing into the mailbox memory of processor 0 Reset Source: mod_g_rst_n

2.3.157 CFG0_PRU-ICSS_PRU1_MBOX_READ_REQ Registers

2.3.157.1 CFG0_PRU1_MBOX_READ_REQ Register (Offset = 14014h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-431. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 4014h

Figure 2-214. PRU-ICSS_PRU1_MBOX_READ_REQ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRU-ICSS_PRU1_MBOX_READ_REQ_PROC_7	RESERVED			PRU-ICSS_PRU1_MBOX_READ_REQ_PROC_6	RESERVED			PRU-ICSS_PRU1_MBOX_READ_REQ_PROC_5	RESERVED			PRU-ICSS_PRU1_MBOX_READ_REQ_PROC_4
NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC
0			0h	0			0h	0			0h	0			0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRU-ICSS_PRU1_MBOX_READ_REQ_PROC_3	RESERVED			PRU-ICSS_PRU1_MBOX_READ_REQ_PROC_2	RESERVED			PRU-ICSS_PRU1_MBOX_READ_REQ_PROC_1	RESERVED			PRU-ICSS_PRU1_MBOX_READ_REQ_PROC_0
NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC
0			0h	0			0h	0			0h	0			0h

Access Types Legend

Table 2-432. PRU-ICSS_PRU1_MBOX_READ_REQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28	PRU-ICSS_PRU1_MBOX_READ_REQ_PROC_7	R/W1TC	0h	This is request from processor 7 to corresponding ICSSM_PRU. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
27:25	RESERVED	NONE		Reserved
24	PRU-ICSS_PRU1_MBOX_READ_REQ_PROC_6	R/W1TC	0h	This is request from processor 6 to corresponding ICSSM_PRU. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
23:21	RESERVED	NONE		Reserved
20	PRU-ICSS_PRU1_MBOX_READ_REQ_PROC_5	R/W1TC	0h	This is request from processor 5 to corresponding ICSSM_PRU. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
19:17	RESERVED	NONE		Reserved
16	PRU-ICSS_PRU1_MBOX_READ_REQ_PROC_4	R/W1TC	0h	This is request from processor 4 to corresponding ICSSM_PRU. Requesting it to read from mailbox. Reset Source: mod_g_rst_n

Table 2-432. PRU-ICSS_PRU1_MBOX_READ_REQ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:13	RESERVED	NONE		Reserved
12	PRU-ICSS_PRU1_MBOX_READ_REQ_PROC_3	R/W1TC	0h	This is request from processor 3 to corresponding ICSSM_PRU. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
11:9	RESERVED	NONE		Reserved
8	PRU-ICSS_PRU1_MBOX_READ_REQ_PROC_2	R/W1TC	0h	This is request from processor 2 to corresponding ICSSM_PRU. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
7:5	RESERVED	NONE		Reserved
4	PRU-ICSS_PRU1_MBOX_READ_REQ_PROC_1	R/W1TC	0h	This is request from processor 1 to corresponding ICSSM_PRU. Requesting it to read from mailbox. Reset Source: mod_g_rst_n
3:1	RESERVED	NONE		Reserved
0	PRU-ICSS_PRU1_MBOX_READ_REQ_PROC_0	R/W1TC	0h	This is request from processor 0 to corresponding ICSSM_PRU. Requesting it to read from mailbox. Reset Source: mod_g_rst_n

2.3.158 CFG0_PRU-ICSS_PRU1_MBOX_READ_DONE_ACK Registers

2.3.158.1 CFG0_PRU1_MBOX_READ_DONE_ACK Register (Offset = 14018h) [reset = 0h]

Short Description:

Long Description:

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Table 2-433. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 4018h

Figure 2-215. PRU-ICSS_PRU1_MBOX_READ_DONE_ACK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRU-ICSS_PRU1_MBOX_READ_DONE_ACK_PROC							
NONE								R/W							
0								0h							

Access Types Legend

Table 2-434. PRU-ICSS_PRU1_MBOX_READ_DONE_ACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	PRU-ICSS_PRU1_MBOX_READ_DONE_ACK_PROC	R/W	0h	Write pulse bit field: For bits 0 to 7: Wrting 1'b1 : Generates pulse interrupt to corresponding proc from ICSSM_PRU0. For bits 8 to 15: Wrting 1'b1 : Generates pulse interrupt to corresponding proc from ICSSM_PRU1. Reset Source: mod_g_rst_n

2.3.159 CFG0_PRU-ICSS_PRU1_MBOX_READ_DONE Registers

2.3.159.1 CFG0_PRU1_MBOX_READ_DONE Register (Offset = 1401Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-435. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 401Ch

Figure 2-216. PRU-ICSS_PRU1_MBOX_READ_DONE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRU-ICSS_PRU1_MBOX_READ_DONE_PROC_7	RESERVED			PRU-ICSS_PRU1_MBOX_READ_DONE_PROC_6	RESERVED			PRU-ICSS_PRU1_MBOX_READ_DONE_PROC_5	RESERVED			PRU-ICSS_PRU1_MBOX_READ_DONE_PROC_4
NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC
0			0h	0			0h	0			0h	0			0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRU-ICSS_PRU1_MBOX_READ_DONE_PROC_3	RESERVED			PRU-ICSS_PRU1_MBOX_READ_DONE_PROC_2	RESERVED			PRU-ICSS_PRU1_MBOX_READ_DONE_PROC_1	RESERVED			PRU-ICSS_PRU1_MBOX_READ_DONE_PROC_0
NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC	NONE			R/W1TC
0			0h	0			0h	0			0h	0			0h

Access Types Legend

Table 2-436. PRU-ICSS_PRU1_MBOX_READ_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28	PRU-ICSS_PRU1_MBOX_READ_DONE_PROC_7	R/W1TC	0h	This register should be written once finishing reading from corresponding ICSSM_PRU's mailbox written by proc 7 Reset Source: mod_g_rst_n
27:25	RESERVED	NONE		Reserved
24	PRU-ICSS_PRU1_MBOX_READ_DONE_PROC_6	R/W1TC	0h	This register should be written once finishing reading from corresponding ICSSM_PRU's mailbox written by proc 6 Reset Source: mod_g_rst_n
23:21	RESERVED	NONE		Reserved
20	PRU-ICSS_PRU1_MBOX_READ_DONE_PROC_5	R/W1TC	0h	This register should be written once finishing reading from corresponding ICSSM_PRU's mailbox written by proc 5 Reset Source: mod_g_rst_n
19:17	RESERVED	NONE		Reserved
16	PRU-ICSS_PRU1_MBOX_READ_DONE_PROC_4	R/W1TC	0h	This register should be written once finishing reading from corresponding ICSSM_PRU's mailbox written by proc 4 Reset Source: mod_g_rst_n

Table 2-436. PRU-ICSS_PRU1_MBOX_READ_DONE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:13	RESERVED	NONE		Reserved
12	PRU-ICSS_PRU1_MBOX_READ_DONE_PROC_3	R/W1TC	0h	This register should be written once finishing reading from corresponding ICSSM_PRU's mailbox written by proc 3 Reset Source: mod_g_rst_n
11:9	RESERVED	NONE		Reserved
8	PRU-ICSS_PRU1_MBOX_READ_DONE_PROC_2	R/W1TC	0h	This register should be written once finishing reading from corresponding ICSSM_PRU's mailbox written by proc 2 Reset Source: mod_g_rst_n
7:5	RESERVED	NONE		Reserved
4	PRU-ICSS_PRU1_MBOX_READ_DONE_PROC_1	R/W1TC	0h	This register should be written once finishing reading from corresponding ICSSM_PRU's mailbox written by proc 1 Reset Source: mod_g_rst_n
3:1	RESERVED	NONE		Reserved
0	PRU-ICSS_PRU1_MBOX_READ_DONE_PROC_0	R/W1TC	0h	This register should be written once finishing reading from corresponding ICSSM_PRU's mailbox written by proc 0 Reset Source: mod_g_rst_n

2.3.160 CFG0_TPCC0_ERRAGG_MASK Registers

2.3.160.1 CFG0_ERRAGG_MASK Register (Offset = 18000h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-437. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8000h

Figure 2-217. TPCC0_ERRAGG_MASK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					MSS_TPCC_A_ERRAGG_MASK_TPTC_A1_READ_ACCESS_ERROR	MSS_TPCC_A_ERRAGG_MASK_TPTC_A0_READ_ACCESS_ERROR	MSS_TPCC_A_ERRAGG_MASK_TPCC_A_READ_ACCESS_ERROR	RESERVED					MSS_TPCC_A_ERRAGG_MASK_TPTC_A1_WRITE_ACCESS_ERROR	MSS_TPCC_A_ERRAGG_MASK_TPTC_A0_WRITE_ACCESS_ERROR	MSS_TPCC_A_ERRAGG_MASK_TPCC_A_WRITE_ACCESS_ERROR
NONE					R/W	R/W	R/W	NONE					R/W	R/W	R/W
0					0h	0h	0h	0					0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											MSS_TPCC_A_ERRAGG_MASK_TPCC_A_PAR_ERR	MSS_TPCC_A_ERRAGG_MASK_TPTC_A1_ERR	MSS_TPCC_A_ERRAGG_MASK_TPTC_A0_ERR	MSS_TPCC_A_ERRAGG_MASK_TPCC_A_MPINT	MSS_TPCC_A_ERRAGG_MASK_TPCC_A_ERRINT
NONE											R/W	R/W	R/W	R/W	R/W
0											0h	0h	0h	0h	0h

Access Types Legend

Table 2-438. TPCC0_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE		Reserved
26	MSS_TPCC_A_ERRAGG_MASK_TPTC_A1_READ_ACCESS_ERROR	R/W	0h	Mask Error from MSS_TPTC_A1 to aggregated Error MSS_TPCC_A_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
25	MSS_TPCC_A_ERRAGG_MASK_TPTC_A0_READ_ACCESS_ERROR	R/W	0h	Mask Error from MSS_TPTC_A0 to aggregated Error MSS_TPCC_A_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
24	MSS_TPCC_A_ERRAGG_MASK_TPCC_A_READ_ACCESS_ERROR	R/W	0h	Mask Error from MSS_TPCC_A to aggregated Error MSS_TPCC_A_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
23:19	RESERVED	NONE		Reserved
18	MSS_TPCC_A_ERRAGG_MASK_TPTC_A1_WRITE_ACCESS_ERROR	R/W	0h	Mask Error from MSS_TPTC_A1 to aggregated Error MSS_TPCC_A_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n

Table 2-438. TPCC0_ERRAGG_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	MSS_TPCC_A_ERRAGG_MASK_TPTC_A0_WRITE_ACCESS_ERROR	R/W	0h	Mask Error from MSS_TPTC_A0 to aggregated Error MSS_TPCC_A_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
16	MSS_TPCC_A_ERRAGG_MASK_TPCC_A_WRITE_ACCESS_ERROR	R/W	0h	Mask Error from MSS_TPCC_A to aggregated Error MSS_TPCC_A_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
15:5	RESERVED	NONE		Reserved
4	MSS_TPCC_A_ERRAGG_MASK_TPCC_A_PAR_ERR	R/W	0h	Mask Error from MSS_TPCC_A to aggregated Error MSS_TPCC_A_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
3	MSS_TPCC_A_ERRAGG_MASK_TPTC_A1_ERR	R/W	0h	Mask Error from MSS_TPTC_A1 to aggregated Error MSS_TPCC_A_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
2	MSS_TPCC_A_ERRAGG_MASK_TPTC_A0_ERR	R/W	0h	Mask Error from MSS_TPTC_A0 to aggregated Error MSS_TPCC_A_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
1	MSS_TPCC_A_ERRAGG_MASK_TPCC_A_MPINT	R/W	0h	Mask Error from MSS_TPCC_A to aggregated Error MSS_TPCC_A_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
0	MSS_TPCC_A_ERRAGG_MASK_TPCC_A_ERRINT	R/W	0h	Mask Error from MSS_TPCC_A to aggregated Error MSS_TPCC_A_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n

2.3.161 CFG0_TPCC0_ERRAGG_STATUS Registers

2.3.161.1 CFG0_ERRAGG_STATUS Register (Offset = 18004h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-439. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8004h

Figure 2-218. TPCC0_ERRAGG_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					MSS_TPCC_A_ERRAGG_STATUS_TPTC_A1_READ_ACCESS_ERROR	MSS_TPCC_A_ERRAGG_STATUS_TPTC_A0_READ_ACCESS_ERROR	MSS_TPCC_A_ERRAGG_STATUS_TPCC_A_READ_ACCESS_ERROR	RESERVED					MSS_TPCC_A_ERRAGG_STATUS_TPTC_A1_WRITE_ACCESS_ERROR	MSS_TPCC_A_ERRAGG_STATUS_TPTC_A0_WRITE_ACCESS_ERROR	MSS_TPCC_A_ERRAGG_STATUS_TPCC_A_WRITE_ACCESS_ERROR
NONE					R/W1TC	R/W1TC	R/W1TC	NONE					R/W1TC	R/W1TC	R/W1TC
0					0h	0h	0h	0					0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											MSS_TPCC_A_ERRAGG_STATUS_TPCC_A_PAR_ERR	MSS_TPCC_A_ERRAGG_STATUS_TPTC_A1_ERR	MSS_TPCC_A_ERRAGG_STATUS_TPTC_A0_ERR	MSS_TPCC_A_ERRAGG_STATUS_TPCC_A_MPINT	MSS_TPCC_A_ERRAGG_STATUS_TPCC_A_ERRINT
NONE											R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0											0h	0h	0h	0h	0h

Access Types Legend

Table 2-440. TPCC0_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE		Reserved
26	MSS_TPCC_A_ERRAGG_STATUS_TPTC_A1_READ_ACCESS_ERROR	R/W1TC	0h	Status of Error from MSS_TPTC_A1. Set only if Interupt is unmasked in MSS_TPCC_A_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
25	MSS_TPCC_A_ERRAGG_STATUS_TPTC_A0_READ_ACCESS_ERROR	R/W1TC	0h	Status of Error from MSS_TPTC_A0. Set only if Interupt is unmasked in MSS_TPCC_A_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
24	MSS_TPCC_A_ERRAGG_STATUS_TPCC_A_READ_ACCESS_ERROR	R/W1TC	0h	Status of Error from MSS_TPCC_A. Set only if Interupt is unmasked in MSS_TPCC_A_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
23:19	RESERVED	NONE		Reserved

Table 2-440. TPCC0_ERRAGG_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	MSS_TPCC_A_ERRAGG_STATUS_TPTC_A1_WRITE_ACCESS_ERROR	R/W1TC	0h	Status of Error from MSS_TPTC_A1. Set only if Interupt is unmasked in MSS_TPCC_A_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
17	MSS_TPCC_A_ERRAGG_STATUS_TPTC_A0_WRITE_ACCESS_ERROR	R/W1TC	0h	Status of Error from MSS_TPTC_A0. Set only if Interupt is unmasked in MSS_TPCC_A_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
16	MSS_TPCC_A_ERRAGG_STATUS_TPCC_A_WRITE_ACCESS_ERROR	R/W1TC	0h	Status of Error from MSS_TPCC_A. Set only if Interupt is unmasked in MSS_TPCC_A_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
15:5	RESERVED	NONE		Reserved
4	MSS_TPCC_A_ERRAGG_STATUS_TPCC_A_PAR_ERR	R/W1TC	0h	Status of Error from MSS_TPCC_A. Set only if Interupt is unmasked in MSS_TPCC_A_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
3	MSS_TPCC_A_ERRAGG_STATUS_TPTC_A1_ERR	R/W1TC	0h	Status of Error from MSS_TPTC_A1. Set only if Interupt is unmasked in MSS_TPCC_A_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
2	MSS_TPCC_A_ERRAGG_STATUS_TPTC_A0_ERR	R/W1TC	0h	Status of Error from MSS_TPTC_A0. Set only if Interupt is unmasked in MSS_TPCC_A_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
1	MSS_TPCC_A_ERRAGG_STATUS_TPCC_A_MPINT	R/W1TC	0h	Status of Error from MSS_TPCC_A. Set only if Interupt is unmasked in MSS_TPCC_A_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
0	MSS_TPCC_A_ERRAGG_STATUS_TPCC_A_ERRINT	R/W1TC	0h	Status of Error from MSS_TPCC_A. Set only if Interupt is unmasked in MSS_TPCC_A_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n

2.3.162 CFG0_TPCC0_ERRAGG_STATUS_RAW Registers

2.3.162.1 CFG0_ERRAGG_STATUS_RAW Register (Offset = 18008h) [reset = 0h]

Short Description:

Long Description:

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Table 2-441. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8008h

Figure 2-219. TPCC0_ERRAGG_STATUS_RAW Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					MSS_TPCC_A_ERRAGG_STATUS_RAW_TPTC_A1_READ_ACCESS_ERROR	MSS_TPCC_A_ERRAGG_STATUS_RAW_TPTC_A0_READ_ACCESS_ERROR	MSS_TPCC_A_ERRAGG_STATUS_RAW_TPCC_A_READ_ACCESS_ERROR	RESERVED					MSS_TPCC_A_ERRAGG_STATUS_RAW_TPTC_A1_WRITE_ACCESS_ERROR	MSS_TPCC_A_ERRAGG_STATUS_RAW_TPTC_A0_WRITE_ACCESS_ERROR	MSS_TPCC_A_ERRAGG_STATUS_RAW_TPCC_A_WRITE_ACCESS_ERROR
NONE					R/W1TC	R/W1TC	R/W1TC	NONE					R/W1TC	R/W1TC	R/W1TC
0					0h	0h	0h	0					0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											MSS_TPCC_A_ERRAGG_STATUS_RAW_TPCC_A_PAR_ERR	MSS_TPCC_A_ERRAGG_STATUS_RAW_TPTC_A1_ERR	MSS_TPCC_A_ERRAGG_STATUS_RAW_TPTC_A0_ERR	MSS_TPCC_A_ERRAGG_STATUS_RAW_TPCC_A_MPINT	MSS_TPCC_A_ERRAGG_STATUS_RAW_TPCC_A_ERRINT
NONE											R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0											0h	0h	0h	0h	0h

Access Types Legend

Table 2-442. TPCC0_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE		Reserved
26	MSS_TPCC_A_ERRAGG_STATUS_RAW_TPTC_A1_READ_ACCESS_ERROR	R/W1TC	0h	Raw Status of Error from MSS_TPTC_A1. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_A_ERRAGG_MASK Reset Source: mod_g_rst_n
25	MSS_TPCC_A_ERRAGG_STATUS_RAW_TPTC_A0_READ_ACCESS_ERROR	R/W1TC	0h	Raw Status of Error from MSS_TPTC_A0. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_A_ERRAGG_MASK Reset Source: mod_g_rst_n

Table 2-442. TPCC0_ERRAGG_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	MSS_TPCC_A_ERRAGG_STATUS_RAW_TPCC_A_READ_ACCESS_ERROR	R/W1TC	0h	Raw Status of Error from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_A_ERRAGG_MASK Reset Source: mod_g_rst_n
23:19	RESERVED	NONE		Reserved
18	MSS_TPCC_A_ERRAGG_STATUS_RAW_TPTC_A1_WRITE_ACCESS_ERROR	R/W1TC	0h	Raw Status of Error from MSS_TPTC_A1. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_A_ERRAGG_MASK Reset Source: mod_g_rst_n
17	MSS_TPCC_A_ERRAGG_STATUS_RAW_TPTC_A0_WRITE_ACCESS_ERROR	R/W1TC	0h	Raw Status of Error from MSS_TPTC_A0. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_A_ERRAGG_MASK Reset Source: mod_g_rst_n
16	MSS_TPCC_A_ERRAGG_STATUS_RAW_TPCC_A_WRITE_ACCESS_ERROR	R/W1TC	0h	Raw Status of Error from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_A_ERRAGG_MASK Reset Source: mod_g_rst_n
15:5	RESERVED	NONE		Reserved
4	MSS_TPCC_A_ERRAGG_STATUS_RAW_TPCC_A_PAR_ERR	R/W1TC	0h	Raw Status of Error from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_A_ERRAGG_MASK Reset Source: mod_g_rst_n
3	MSS_TPCC_A_ERRAGG_STATUS_RAW_TPTC_A1_ERR	R/W1TC	0h	Raw Status of Error from MSS_TPTC_A1. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_A_ERRAGG_MASK Reset Source: mod_g_rst_n
2	MSS_TPCC_A_ERRAGG_STATUS_RAW_TPTC_A0_ERR	R/W1TC	0h	Raw Status of Error from MSS_TPTC_A0. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_A_ERRAGG_MASK Reset Source: mod_g_rst_n
1	MSS_TPCC_A_ERRAGG_STATUS_RAW_TPCC_A_MPINT	R/W1TC	0h	Raw Status of Error from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_A_ERRAGG_MASK Reset Source: mod_g_rst_n
0	MSS_TPCC_A_ERRAGG_STATUS_RAW_TPCC_A_ERRINT	R/W1TC	0h	Raw Status of Error from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_A_ERRAGG_MASK Reset Source: mod_g_rst_n

2.3.163 CFG0_MMR_ACCESS_ERRAGG_MASK0 Registers

2.3.163.1 CFG0_ACCESS_ERRAGG_MASK0 Register (Offset = 18010h) [reset = 0h]

Short Description:

Long Description:

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Table 2-443. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8010h

Figure 2-220. MMR_ACCESS_ERRAGG_MASK0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_PERIPH_ERRAGG_MASK0_HSM_CTRL_WR	MSS_PERIPH_ERRAGG_MASK0_HSM_CTRL_RD	MSS_PERIPH_ERRAGG_MASK0_HSM_SOC_CTRL_WR	MSS_PERIPH_ERRAGG_MASK0_HSM_SOC_CTRL_RD	MSS_PERIPH_ERRAGG_MASK0_TOP_RCM_WR	MSS_PERIPH_ERRAGG_MASK0_TOP_RCM_RD	MSS_PERIPH_ERRAGG_MASK0_TOP_CTRL_WR	MSS_PERIPH_ERRAGG_MASK0_TOP_CTRL_RD	MSS_PERIPH_ERRAGG_MASK0_MSS_RCM_WR	MSS_PERIPH_ERRAGG_MASK0_MSS_RCM_RD	MSS_PERIPH_ERRAGG_MASK0_MSS_CTRL_WR	MSS_PERIPH_ERRAGG_MASK0_MSS_CTRL_RD
NONE				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0				0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-444. MMR_ACCESS_ERRAGG_MASK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11	MSS_PERIPH_ERRAGG_MASK0_HSM_CTRL_WR	R/W	0h	Mask Interrupt from HSM_CTRL to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
10	MSS_PERIPH_ERRAGG_MASK0_HSM_CTRL_RD	R/W	0h	Mask Interrupt from HSM_CTRL to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
9	MSS_PERIPH_ERRAGG_MASK0_HSM_SOC_CTRL_WR	R/W	0h	Mask Interrupt from HSM_SOC_CTRL to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
8	MSS_PERIPH_ERRAGG_MASK0_HSM_SOC_CTRL_RD	R/W	0h	Mask Interrupt from HSM_SOC_CTRL to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
7	MSS_PERIPH_ERRAGG_MASK0_TOP_RCM_WR	R/W	0h	Mask Interrupt from TOP_RCM to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
6	MSS_PERIPH_ERRAGG_MASK0_TOP_RCM_RD	R/W	0h	Mask Interrupt from TOP_RCM to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
5	MSS_PERIPH_ERRAGG_MASK0_TOP_CTRL_WR	R/W	0h	Mask Interrupt from TOP_CTRL to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n

Table 2-444. MMR_ACCESS_ERRAGG_MASK0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	MSS_PERIPH_ERRAGG_MASK0_TOP_CTRL_RD	R/W	0h	Mask Interrupt from TOP_CTRL to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
3	MSS_PERIPH_ERRAGG_MASK0_MSS_RCM_WR	R/W	0h	Mask Interrupt from MSS_RCM to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
2	MSS_PERIPH_ERRAGG_MASK0_MSS_RCM_RD	R/W	0h	Mask Interrupt from MSS_RCM to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
1	MSS_PERIPH_ERRAGG_MASK0_MSS_CTRL_WR	R/W	0h	Mask Interrupt from MSS_CTRL to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
0	MSS_PERIPH_ERRAGG_MASK0_MSS_CTRL_RD	R/W	0h	Mask Interrupt from MSS_CTRL to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n

2.3.164 CFG0_MMR_ACCESS_ERRAGG_STATUS0 Registers

2.3.164.1 CFG0_ACCESS_ERRAGG_STATUS0 Register (Offset = 18014h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-445. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8014h

Figure 2-221. MMR_ACCESS_ERRAGG_STATUS0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_PERIPH_ERRAGG_STATUS0_HSM_CTRL_WR	MSS_PERIPH_ERRAGG_STATUS0_HSM_CTRL_RD	MSS_PERIPH_ERRAGG_STATUS0_HSM_SOC_CTRL_WR	MSS_PERIPH_ERRAGG_STATUS0_HSM_SOC_CTRL_RD	MSS_PERIPH_ERRAGG_STATUS0_TOP_RCM_WR	MSS_PERIPH_ERRAGG_STATUS0_TOP_RCM_RD	MSS_PERIPH_ERRAGG_STATUS0_TOP_CTRL_WR	MSS_PERIPH_ERRAGG_STATUS0_TOP_CTRL_RD	MSS_PERIPH_ERRAGG_STATUS0_MSS_RCM_WR	MSS_PERIPH_ERRAGG_STATUS0_MSS_RCM_RD	MSS_PERIPH_ERRAGG_STATUS0_MSS_CTRL_WR	MSS_PERIPH_ERRAGG_STATUS0_MSS_CTRL_RD
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0				0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-446. MMR_ACCESS_ERRAGG_STATUS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11	MSS_PERIPH_ERRAGG_STATUS0_HSM_CTRL_WR	R/W1TC	0h	Status of Interrupt from HSM_CTRL Set only if Interupt is unmasked in MSS_PERIPH_ERRAGG_MASK0 Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
10	MSS_PERIPH_ERRAGG_STATUS0_HSM_CTRL_RD	R/W1TC	0h	Status of Interrupt from HSM_CTRL Set only if Interupt is unmasked in MSS_PERIPH_ERRAGG_MASK0 Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
9	MSS_PERIPH_ERRAGG_STATUS0_HSM_SOC_CTRL_WR	R/W1TC	0h	Status of Interrupt from HSM_SOC_CTRL Set only if Interupt is unmasked in MSS_PERIPH_ERRAGG_MASK0 Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
8	MSS_PERIPH_ERRAGG_STATUS0_HSM_SOC_CTRL_RD	R/W1TC	0h	Status of Interrupt from HSM_SOC_CTRL Set only if Interupt is unmasked in MSS_PERIPH_ERRAGG_MASK0 Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
7	MSS_PERIPH_ERRAGG_STATUS0_TOP_RCM_WR	R/W1TC	0h	Status of Interrupt from TOP_RCM Set only if Interupt is unmasked in MSS_PERIPH_ERRAGG_MASK0 Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
6	MSS_PERIPH_ERRAGG_STATUS0_TOP_RCM_RD	R/W1TC	0h	Status of Interrupt from TOP_RCM Set only if Interupt is unmasked in MSS_PERIPH_ERRAGG_MASK0 Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
5	MSS_PERIPH_ERRAGG_STATUS0_TOP_CTRL_WR	R/W1TC	0h	Status of Interrupt from TOP_CTRL Set only if Interupt is unmasked in MSS_PERIPH_ERRAGG_MASK0 Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

Table 2-446. MMR_ACCESS_ERRAGG_STATUS0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	MSS_PERIPH_ERRAGG_STATUS0_TOP_CTRL_RD	R/W1TC	0h	Status of Interrupt from TOP_CTRL Set only if Interupt is unmasked in MSS_PERIPH_ERRAGG_MASK0 Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
3	MSS_PERIPH_ERRAGG_STATUS0_MSS_RCM_WR	R/W1TC	0h	Status of Interrupt from MSS_RCM Set only if Interupt is unmasked in MSS_PERIPH_ERRAGG_MASK0 Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
2	MSS_PERIPH_ERRAGG_STATUS0_MSS_RCM_RD	R/W1TC	0h	Status of Interrupt from MSS_RCM Set only if Interupt is unmasked in MSS_PERIPH_ERRAGG_MASK0 Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
1	MSS_PERIPH_ERRAGG_STATUS0_MSS_CTRL_WR	R/W1TC	0h	Status of Interrupt from MSS_CTRL Set only if Interupt is unmasked in MSS_PERIPH_ERRAGG_MASK0 Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
0	MSS_PERIPH_ERRAGG_STATUS0_MSS_CTRL_RD	R/W1TC	0h	Status of Interrupt from MSS_CTRL Set only if Interupt is unmasked in MSS_PERIPH_ERRAGG_MASK0 Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

2.3.165 CFG0_MMR_ACCESS_ERRAGG_STATUS_RAW0 Registers

2.3.165.1 CFG0_ACCESS_ERRAGG_STATUS_RAW0 Register (Offset = 18018h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-447. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8018h

Figure 2-222. MMR_ACCESS_ERRAGG_STATUS_RAW0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_PERIPH_ERRAGG_STATUS_RAW0_HSM_CTRL_WR	MSS_PERIPH_ERRAGG_STATUS_RAW0_HSM_CTRL_RD	MSS_PERIPH_ERRAGG_STATUS_RAW0_HSM_SOC_CTRL_WR	MSS_PERIPH_ERRAGG_STATUS_RAW0_HSM_SOC_CTRL_RD	MSS_PERIPH_ERRAGG_STATUS_RAW0_TOP_RCM_WR	MSS_PERIPH_ERRAGG_STATUS_RAW0_TOP_RCM_RD	MSS_PERIPH_ERRAGG_STATUS_RAW0_TOP_CTRL_WR	MSS_PERIPH_ERRAGG_STATUS_RAW0_TOP_CTRL_RD	MSS_PERIPH_ERRAGG_STATUS_RAW0_MSS_RCM_WR	MSS_PERIPH_ERRAGG_STATUS_RAW0_MSS_RCM_RD	MSS_PERIPH_ERRAGG_STATUS_RAW0_MSS_CTRL_WR	MSS_PERIPH_ERRAGG_STATUS_RAW0_MSS_CTRL_RD
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0				0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-448. MMR_ACCESS_ERRAGG_STATUS_RAW0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11	MSS_PERIPH_ERRAGG_STATUS_RAW0_HSM_CTRL_WR	R/W1TC	0h	Raw Status of Interrupt from HSM_CTRL. Set irrespective if the Interupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0 Reset Source: mod_g_rst_n
10	MSS_PERIPH_ERRAGG_STATUS_RAW0_HSM_CTRL_RD	R/W1TC	0h	Raw Status of Interrupt from HSM_CTRL. Set irrespective if the Interupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0 Reset Source: mod_g_rst_n
9	MSS_PERIPH_ERRAGG_STATUS_RAW0_HSM_SOC_CTRL_WR	R/W1TC	0h	Raw Status of Interrupt from HSM_SOC_CTRL. Set irrespective if the Interupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0 Reset Source: mod_g_rst_n
8	MSS_PERIPH_ERRAGG_STATUS_RAW0_HSM_SOC_CTRL_RD	R/W1TC	0h	Raw Status of Interrupt from HSM_SOC_CTRL. Set irrespective if the Interupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0 Reset Source: mod_g_rst_n
7	MSS_PERIPH_ERRAGG_STATUS_RAW0_TOP_RCM_WR	R/W1TC	0h	Raw Status of Interrupt from TOP_RCM. Set irrespective if the Interupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0 Reset Source: mod_g_rst_n
6	MSS_PERIPH_ERRAGG_STATUS_RAW0_TOP_RCM_RD	R/W1TC	0h	Raw Status of Interrupt from TOP_RCM. Set irrespective if the Interupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0 Reset Source: mod_g_rst_n

Table 2-448. MMR_ACCESS_ERRAGG_STATUS_RAW0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MSS_PERIPH_ERRAGG_STATUS_RAW0_TOP_CTRL_WR	R/W1TC	0h	Raw Status of Interrupt from TOP_CTRL. Set irrespective if the Interupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0 Reset Source: mod_g_rst_n
4	MSS_PERIPH_ERRAGG_STATUS_RAW0_TOP_CTRL_RD	R/W1TC	0h	Raw Status of Interrupt from TOP_CTRL. Set irrespective if the Interupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0 Reset Source: mod_g_rst_n
3	MSS_PERIPH_ERRAGG_STATUS_RAW0_MSS_RCM_WR	R/W1TC	0h	Raw Status of Interrupt from MSS_RCM. Set irrespective if the Interupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0 Reset Source: mod_g_rst_n
2	MSS_PERIPH_ERRAGG_STATUS_RAW0_MSS_RCM_RD	R/W1TC	0h	Raw Status of Interrupt from MSS_RCM. Set irrespective if the Interupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0 Reset Source: mod_g_rst_n
1	MSS_PERIPH_ERRAGG_STATUS_RAW0_MSS_CTRL_WR	R/W1TC	0h	Raw Status of Interrupt from MSS_CTRL. Set irrespective if the Interupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0 Reset Source: mod_g_rst_n
0	MSS_PERIPH_ERRAGG_STATUS_RAW0_MSS_CTRL_RD	R/W1TC	0h	Raw Status of Interrupt from MSS_CTRL. Set irrespective if the Interupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0 Reset Source: mod_g_rst_n

2.3.166 CFG0_R5SS0_CPU0_ECC_CORR_ERRAGG_MASK Registers

2.3.166.1 CFG0_CPU0_ECC_CORR_ERRAGG_MASK Register (Offset = 18080h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-449. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8080h

Figure 2-223. R5SS0_CPU0_ECC_CORR_ERRAGG_MASK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_IDATA_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_ITAG_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_DDATA_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_DTAG_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_B0TCM_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_B1TCM_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_ATCM_CORR_ERR
NONE									R/W	R/W	R/W	R/W	R/W	R/W	R/W
0									0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-450. R5SS0_CPU0_ECC_CORR_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE		Reserved
6	R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_IDATA_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
5	R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_ITAG_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
4	R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_DDATA_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
3	R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_DTAG_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
2	R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_B0TCM_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n

Table 2-450. R5SS0_CPU0_ECC_CORR_ERRAGG_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_B1TCM_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
0	R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_ATCM_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n

2.3.167 CFG0_R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS Registers

2.3.167.1 CFG0_CPU0_ECC_CORR_ERRAGG_STATUS Register (Offset = 18084h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-451. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8084h

Figure 2-224. R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_IDATA_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_ITAG_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_DDATA_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_DTAG_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_B0TCM_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_B1TCM_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_ATCM_CORR_ERR
NONE									R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0									0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-452. R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE		Reserved
6	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_IDATA_CORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
5	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_ITAG_CORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
4	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_DDATA_CORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
3	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_DTAG_CORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

Table 2-452. R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_B0TCM_CORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
1	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_B1TCM_CORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
0	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_ATCM_CORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

2.3.168 CFG0_R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW Registers

2.3.168.1 CFG0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW Register (Offset = 18088h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-453. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8088h

Figure 2-225. R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_IDATA_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_ITAG_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_DDATA_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_DTAG_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_B0TCM_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_B1TCM_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_ATCM_CORR_ERR
NONE									R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0									0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-454. R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE		Reserved
6	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_IDATA_CORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
5	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_ITAG_CORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
4	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_DDATA_CORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
3	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_DTAG_CORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

Table 2-454. R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_B0TCM_CORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
1	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_B1TCM_CORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
0	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_ATCM_CORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

2.3.169 CFG0_R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK Registers

2.3.169.1 CFG0_CPU0_ECC_UNCORR_ERRAGG_MASK Register (Offset = 18090h) [reset = 0h]

Short Description:

Long Description:

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Table 2-455. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8090h

Figure 2-226. R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU0_DDATA_UNCORR_ERR	R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU0_DTAG_UNCORR_ERR	R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU0_B0TCM_UNCORR_ERR	R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU0_B1TCM_UNCORR_ERR	R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU0_ATCM_UNCORR_ERR
NONE											R/W	R/W	R/W	R/W	R/W
0											0h	0h	0h	0h	0h

Access Types Legend

Table 2-456. R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4	R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU0_DDATA_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
3	R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU0_DTAG_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
2	R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU0_B0TCM_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
1	R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU0_B1TCM_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n

Table 2-456. R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU0_ATCM_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n

2.3.170 CFG0_R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS Registers

2.3.170.1 CFG0_CPU0_ECC_UNCORR_ERRAGG_STATUS Register (Offset = 18094h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-457. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8094h

Figure 2-227. R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU0_DDATA_UNCORR_ERR	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU0_DTAG_UNCORR_ERR	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU0_B0TCM_UNCORR_ERR	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU0_B1TCM_UNCORR_ERR	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU0_ATCM_UNCORR_ERR
NONE											R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0											0h	0h	0h	0h	0h

Access Types Legend

Table 2-458. R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU0_DDATA_UNCORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
3	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU0_DTAG_UNCORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
2	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU0_B0TCM_UNCORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
1	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU0_B1TCM_UNCORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

Table 2-458. R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU0_ATCM_UNCORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

2.3.171 CFG0_R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW Registers

2.3.171.1 CFG0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW Register (Offset = 18098h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-459. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8098h

Figure 2-228. R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_DDATA_UNCORR_ERR	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_DTAG_UNCORR_ERR	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_B0TCM_UNCORR_ERR	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_B1TCM_UNCORR_ERR	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_ATCM_UNCORR_ERR
NONE											R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0											0h	0h	0h	0h	0h

Access Types Legend

Table 2-460. R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_DDATA_UNCORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
3	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_DTAG_UNCORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
2	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_B0TCM_UNCORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
1	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_B1TCM_UNCORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

Table 2-460. R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_ATCM_UNCORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

2.3.172 CFG0_R5SS0_CPU1_ECC_CORR_ERRAGG_MASK Registers

2.3.172.1 CFG0_CPU1_ECC_CORR_ERRAGG_MASK Register (Offset = 180A0h) [reset = 0h]

Short Description:

Long Description:

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Table 2-461. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 80A0h

Figure 2-229. R5SS0_CPU1_ECC_CORR_ERRAGG_MASK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_IDATA_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_ITAG_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_DDATA_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_DTAG_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_B0TCM_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_B1TCM_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_ATCM_CORR_ERR
NONE									R/W	R/W	R/W	R/W	R/W	R/W	R/W
0									0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-462. R5SS0_CPU1_ECC_CORR_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE		Reserved
6	R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_IDATA_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
5	R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_ITAG_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
4	R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_DDATA_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
3	R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_DTAG_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
2	R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_B0TCM_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n

Table 2-462. R5SS0_CPU1_ECC_CORR_ERRAGG_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_B1TCM_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
0	R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_ATCM_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n

2.3.173 CFG0_R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS Registers

2.3.173.1 CFG0_CPU1_ECC_CORR_ERRAGG_STATUS Register (Offset = 180A4h) [reset = 0h]

Short Description:

Long Description:

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Table 2-463. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 80A4h

Figure 2-230. R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_IDATA_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_ITAG_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_DDATA_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_DTAG_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_B0TCM_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_B1TCM_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_ATCM_CORR_ERR
NONE									R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0									0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-464. R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE		Reserved
6	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_IDATA_CORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
5	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_ITAG_CORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
4	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_DDATA_CORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
3	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_DTAG_CORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

Table 2-464. R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_B0TCM_CORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
1	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_B1TCM_CORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
0	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_ATCM_CORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

2.3.174 CFG0_R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW Registers

2.3.174.1 CFG0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW Register (Offset = 180A8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-465. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 80A8h

Figure 2-231. R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_IDATA_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_ITAG_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_DDATA_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_DTAG_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_B0TCM_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_B1TCM_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_ATCM_CORR_ERR
NONE									R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0									0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-466. R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE		Reserved
6	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_IDATA_CORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
5	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_ITAG_CORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
4	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_DDATA_CORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
3	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_DTAG_CORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

Table 2-466. R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_B0TCM_CORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
1	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_B1TCM_CORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
0	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_ATCM_CORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

2.3.175 CFG0_R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK Registers

2.3.175.1 CFG0_CPU1_ECC_UNCORR_ERRAGG_MASK Register (Offset = 180B0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-467. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 80B0h

Figure 2-232. R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU1_DDATA_UNCORR_ERR	R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU1_DTAG_UNCORR_ERR	R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU1_B0TCM_UNCORR_ERR	R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU1_B1TCM_UNCORR_ERR	R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU1_ATCM_UNCORR_ERR
NONE											R/W	R/W	R/W	R/W	R/W
0											0h	0h	0h	0h	0h

Access Types Legend

Table 2-468. R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4	R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU1_DDATA_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
3	R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU1_DTAG_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
2	R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU1_B0TCM_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
1	R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU1_B1TCM_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n

Table 2-468. R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU1_ATCM_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n

2.3.176 CFG0_R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS Registers

2.3.176.1 CFG0_CPU1_ECC_UNCORR_ERRAGG_STATUS Register (Offset = 180B4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-469. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 80B4h

Figure 2-233. R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU1_DDATA_UNCORR_ERR	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU1_DTAG_UNCORR_ERR	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU1_B0TCM_UNCORR_ERR	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU1_B1TCM_UNCORR_ERR	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU1_ATCM_UNCORR_ERR
NONE											R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0											0h	0h	0h	0h	0h

Access Types Legend

Table 2-470. R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU1_DDATA_UNCORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
3	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU1_DTAG_UNCORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
2	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU1_B0TCM_UNCORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
1	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU1_B1TCM_UNCORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

Table 2-470. R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU1_ATCM_UNCORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

2.3.177 CFG0_R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW Registers

2.3.177.1 CFG0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW Register (Offset = 180B8h) [reset = 0h]

Short Description:

Long Description:

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Table 2-471. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 80B8h

Figure 2-234. R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_DDATA_UNCORR_ERR	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_DTAG_UNCORR_ERR	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_B0TCM_UNCORR_ERR	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_B1TCM_UNCORR_ERR	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_ATCM_UNCORR_ERR
NONE											R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0											0h	0h	0h	0h	0h

Access Types Legend

Table 2-472. R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_DDATA_UNCORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
3	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_DTAG_UNCORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
2	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_B0TCM_UNCORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
1	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_B1TCM_UNCORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

Table 2-472. R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_ATCM_UNCORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

2.3.178 CFG0_R5SS1_CPU0_ECC_CORR_ERRAGG_MASK Registers

2.3.178.1 CFG0_CPU0_ECC_CORR_ERRAGG_MASK Register (Offset = 180C0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-473. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 80C0h

Figure 2-235. R5SS1_CPU0_ECC_CORR_ERRAGG_MASK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_IDATA_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_ITAG_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_DDATA_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_DTAG_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_B0TCM_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_B1TCM_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_ATCM_CORR_ERR
NONE									R/W	R/W	R/W	R/W	R/W	R/W	R/W
0									0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-474. R5SS1_CPU0_ECC_CORR_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE		Reserved
6	R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_IDATA_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
5	R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_ITAG_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
4	R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_DDATA_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
3	R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_DTAG_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
2	R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_B0TCM_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n

Table 2-474. R5SS1_CPU0_ECC_CORR_ERRAGG_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_B1TCM_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
0	R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_ATCM_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n

2.3.179 CFG0_R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS Registers

2.3.179.1 CFG0_CPU0_ECC_CORR_ERRAGG_STATUS Register (Offset = 180C4h) [reset = 0h]

Short Description:

Long Description:

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Table 2-475. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 80C4h

Figure 2-236. R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_IDATA_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_ITAG_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_DDATA_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_DTAG_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_B0TCM_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_B1TCM_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_ATCM_CORR_ERR
NONE									R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0									0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-476. R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE		Reserved
6	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_IDATA_CORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
5	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_ITAG_CORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
4	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_DDATA_CORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
3	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_DTAG_CORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

Table 2-476. R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_B0TCM_CORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
1	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_B1TCM_CORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
0	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_ATCM_CORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

2.3.180 CFG0_R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW Registers

2.3.180.1 CFG0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW Register (Offset = 180C8h) [reset = 0h]

Short Description:

Long Description:

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Table 2-477. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 80C8h

Figure 2-237. R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_IDATA_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_ITAG_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_DDATA_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_DTAG_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_B0TCM_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_B1TCM_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_ATCM_CORR_ERR
NONE									R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0									0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-478. R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE		Reserved
6	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_IDATA_CORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
5	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_ITAG_CORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
4	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_DDATA_CORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
3	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_DTAG_CORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

Table 2-478. R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_B0TCM_CORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
1	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_B1TCM_CORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
0	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_ATCM_CORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

2.3.181 CFG0_R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK Registers

2.3.181.1 CFG0_CPU0_ECC_UNCORR_ERRAGG_MASK Register (Offset = 180D0h) [reset = 0h]

Short Description:

Long Description:

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Table 2-479. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 80D0h

Figure 2-238. R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU0_DDATA_UNCORR_ERR	R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU0_DTAG_UNCORR_ERR	R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU0_B0TCM_UNCORR_ERR	R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU0_B1TCM_UNCORR_ERR	R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU0_ATCM_UNCORR_ERR
NONE											R/W	R/W	R/W	R/W	R/W
0											0h	0h	0h	0h	0h

Access Types Legend

Table 2-480. R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4	R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU0_DDATA_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
3	R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU0_DTAG_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
2	R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU0_B0TCM_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
1	R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU0_B1TCM_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n

Table 2-480. R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU0_ATCM_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n

2.3.182 CFG0_R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS Registers

2.3.182.1 CFG0_CPU0_ECC_UNCORR_ERRAGG_STATUS Register (Offset = 180D4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-481. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 80D4h

Figure 2-239. R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU0_DDATA_UNCORR_ERR	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU0_DTAG_UNCORR_ERR	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU0_B0TCM_UNCORR_ERR	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU0_B1TCM_UNCORR_ERR	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU0_ATCM_UNCORR_ERR
NONE											R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0											0h	0h	0h	0h	0h

Access Types Legend

Table 2-482. R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU0_DDATA_UNCORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
3	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU0_DTAG_UNCORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
2	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU0_B0TCM_UNCORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
1	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU0_B1TCM_UNCORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

Table 2-482. R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU0_ATCM_UNCORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

2.3.183 CFG0_R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW Registers

2.3.183.1 CFG0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW Register (Offset = 180D8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-483. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 80D8h

Figure 2-240. R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_DDATA_UNCORR_ERR	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_DTAG_UNCORR_ERR	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_B0TCM_UNCORR_ERR	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_B1TCM_UNCORR_ERR	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_ATCM_UNCORR_ERR
NONE											R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0											0h	0h	0h	0h	0h

Access Types Legend

Table 2-484. R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_DDATA_UNCORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
3	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_DTAG_UNCORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
2	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_B0TCM_UNCORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
1	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_B1TCM_UNCORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

Table 2-484. R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_ATCM_UNCORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

2.3.184 CFG0_R5SS1_CPU1_ECC_CORR_ERRAGG_MASK Registers

2.3.184.1 CFG0_CPU1_ECC_CORR_ERRAGG_MASK Register (Offset = 180E0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-485. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 80E0h

Figure 2-241. R5SS1_CPU1_ECC_CORR_ERRAGG_MASK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_IDATA_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_ITAG_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_DDATA_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_DTAG_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_B0TCM_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_B1TCM_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_ATCM_CORR_ERR
NONE									R/W	R/W	R/W	R/W	R/W	R/W	R/W
0									0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-486. R5SS1_CPU1_ECC_CORR_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE		Reserved
6	R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_IDATA_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
5	R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_ITAG_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
4	R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_DDATA_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
3	R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_DTAG_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
2	R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_B0TCM_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n

Table 2-486. R5SS1_CPU1_ECC_CORR_ERRAGG_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_B1TCM_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
0	R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_ATCM_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n

2.3.185 CFG0_R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS Registers

2.3.185.1 CFG0_CPU1_ECC_CORR_ERRAGG_STATUS Register (Offset = 180E4h) [reset = 0h]

Short Description:

Long Description:

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Table 2-487. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 80E4h

Figure 2-242. R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_IDATA_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_ITAG_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_DDATA_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_DTAG_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_B0TCM_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_B1TCM_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_ATCM_CORR_ERR
NONE									R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0									0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-488. R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE		Reserved
6	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_IDATA_CORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
5	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_ITAG_CORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
4	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_DDATA_CORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
3	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_DTAG_CORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

Table 2-488. R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_B0TCM_CORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
1	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_B1TCM_CORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
0	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_ATCM_CORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

2.3.186 CFG0_R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW Registers

2.3.186.1 CFG0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW Register (Offset = 180E8h) [reset = 0h]

Short Description:

Long Description:

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Table 2-489. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 80E8h

Figure 2-243. R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_IDATA_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_ITAG_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_DDATA_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_DTAG_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_B0TCM_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_B1TCM_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_ATCM_CORR_ERR
NONE									R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0									0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-490. R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE		Reserved
6	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_IDATA_CORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
5	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_ITAG_CORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
4	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_DDATA_CORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
3	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_DTAG_CORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

Table 2-490. R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_B0TCM_CORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
1	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_B1TCM_CORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
0	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_ATCM_CORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

2.3.187 CFG0_R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK Registers

2.3.187.1 CFG0_CPU1_ECC_UNCORR_ERRAGG_MASK Register (Offset = 180F0h) [reset = 0h]

Short Description:

Long Description:

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Table 2-491. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 80F0h

Figure 2-244. R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU1_DDATA_UNCORR_ERR	R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU1_DTAG_UNCORR_ERR	R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU1_B0TCM_UNCORR_ERR	R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU1_B1TCM_UNCORR_ERR	R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU1_ATCM_UNCORR_ERR
NONE											R/W	R/W	R/W	R/W	R/W
0											0h	0h	0h	0h	0h

Access Types Legend

Table 2-492. R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4	R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU1_DDATA_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
3	R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU1_DTAG_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
2	R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU1_B0TCM_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
1	R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU1_B1TCM_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n

Table 2-492. R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU1_ATCM_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n

2.3.188 CFG0_R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS Registers

2.3.188.1 CFG0_CPU1_ECC_UNCORR_ERRAGG_STATUS Register (Offset = 180F4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-493. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 80F4h

Figure 2-245. R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU1_DDATA_UNCORR_ERR	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU1_DTAG_UNCORR_ERR	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU1_B0TCM_UNCORR_ERR	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU1_B1TCM_UNCORR_ERR	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU1_ATCM_UNCORR_ERR
NONE											R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0											0h	0h	0h	0h	0h

Access Types Legend

Table 2-494. R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU1_DDATA_UNCORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
3	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU1_DTAG_UNCORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
2	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU1_B0TCM_UNCORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
1	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU1_B1TCM_UNCORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

Table 2-494. R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU1_ATCM_UNCORR_ERR	R/W1TC	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

2.3.189 CFG0_R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW Registers

2.3.189.1 CFG0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW Register (Offset = 180F8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-495. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 80F8h

Figure 2-246. R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_DDATA_UNCORR_ERR	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_DTAG_UNCORR_ERR	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_B0TCM_UNCORR_ERR	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_B1TCM_UNCORR_ERR	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_ATCM_UNCORR_ERR
NONE											R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0											0h	0h	0h	0h	0h

Access Types Legend

Table 2-496. R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_DDATA_UNCORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
3	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_DTAG_UNCORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
2	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_B0TCM_UNCORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
1	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_B1TCM_UNCORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

Table 2-496. R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_ATCM_UNCORR_ERR	R/W1TC	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

2.3.190 CFG0_R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_MASK Registers

2.3.190.1 CFG0_CPU0_TCM_ADDRPARITY_ERRAGG_MASK Register (Offset = 18100h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-497. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8100h

Figure 2-247. R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_MASK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU0_B1TCM0_PARITY_ERR	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU0_B0TCM0_PARITY_ERR	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU0_ATCM0_PARITY_ERR
NONE													R/W	R/W	R/W
0													0h	0h	0h

Access Types Legend

Table 2-498. R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU0_B1TCM0_PARITY_ERR	R/W	0h	Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
1	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU0_B0TCM0_PARITY_ERR	R/W	0h	Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
0	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU0_ATCM0_PARITY_ERR	R/W	0h	Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n

2.3.191 CFG0_R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS Registers

2.3.191.1 CFG0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS Register (Offset = 18104h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-499. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8104h

Figure 2-248. R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS0_CPU0_B1TCM0_PARITY_ERR	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS0_CPU0_B0TCM0_PARITY_ERR	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS0_CPU0_ATCM0_PARITY_ERR
NONE													R/W1TC	R/W1TC	R/W1TC
0													0h	0h	0h

Access Types Legend

Table 2-500. R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS0_CPU0_B1TCM0_PARITY_ERR	R/W1TC	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
1	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS0_CPU0_B0TCM0_PARITY_ERR	R/W1TC	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
0	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS0_CPU0_ATCM0_PARITY_ERR	R/W1TC	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

2.3.192 CFG0_R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Registers

2.3.192.1 CFG0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Register (Offset = 18108h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-501. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8108h

Figure 2-249. R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU0_B1TCM0_PARITY_ERR	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU0_B0TCM0_PARITY_ERR	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU0_ATCM0_PARITY_ERR
NONE													R/W1TC	R/W1TC	R/W1TC
0													0h	0h	0h

Access Types Legend

Table 2-502. R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU0_B1TCM0_PARITY_ERR	R/W1TC	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
1	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU0_B0TCM0_PARITY_ERR	R/W1TC	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
0	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU0_ATCM0_PARITY_ERR	R/W1TC	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

2.3.193 CFG0_R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_MASK Registers

2.3.193.1 CFG0_CPU1_TCM_ADDRPARITY_ERRAGG_MASK Register (Offset = 18110h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-503. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8110h

Figure 2-250. R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_MASK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU1_B1TCM1_PARITY_ERR	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU1_B1TCM0_PARITY_ERR	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU1_ATCM1_PARITY_ERR
NONE													R/W	R/W	R/W
0													0h	0h	0h

Access Types Legend

Table 2-504. R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU1_B1TCM1_PARITY_ERR	R/W	0h	Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
1	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU1_B1TCM0_PARITY_ERR	R/W	0h	Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
0	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU1_ATCM1_PARITY_ERR	R/W	0h	Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n

2.3.194 CFG0_R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS Registers

2.3.194.1 CFG0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS Register (Offset = 18114h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-505. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8114h

Figure 2-251. R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS0_CPU1_B1TCM1_PARITY_ERR	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS0_CPU1_B0TCM1_PARITY_ERR	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS0_CPU1_ATCM1_PARITY_ERR
NONE													R/W1TC	R/W1TC	R/W1TC
0													0h	0h	0h

Access Types Legend

Table 2-506. R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS0_CPU1_B1TCM1_PARITY_ERR	R/W1TC	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
1	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS0_CPU1_B0TCM1_PARITY_ERR	R/W1TC	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
0	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS0_CPU1_ATCM1_PARITY_ERR	R/W1TC	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

2.3.195 CFG0_R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Registers

2.3.195.1 CFG0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Register (Offset = 18118h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-507. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8118h

Figure 2-252. R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU1_B1TCM1_PARITY_ERR	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU1_B0TCM1_PARITY_ERR	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU1_ATCM1_PARITY_ERR
NONE													R/W1TC	R/W1TC	R/W1TC
0													0h	0h	0h

Access Types Legend

Table 2-508. R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU1_B1TCM1_PARITY_ERR	R/W1TC	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
1	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU1_B0TCM1_PARITY_ERR	R/W1TC	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
0	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU1_ATCM1_PARITY_ERR	R/W1TC	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

2.3.196 CFG0_R5SS0_TCM_ADDRPARITY_CLR Registers

2.3.196.1 CFG0_TCM_ADDRPARITY_CLR Register (Offset = 18120h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-509. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8120h

Figure 2-253. R5SS0_TCM_ADDRPARITY_CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED									TCM0_PARITY_CTRL_B1TCM1_ERRADDR_CLR			RESERVED	TCM0_PARITY_CTRL_B1TCM0_ERRADDR_CLR		
NONE									R/W			NONE	R/W		
0									0h			0	0h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	TCM0_PARITY_CTRL_B0CM1_ERRADDR_CLR			RESERVED	TCM0_PARITY_CTRL_B0TCM0_ERRADDR_CLR			RESERVED	TCM0_PARITY_CTRL_ATCM1_ERRADDR_CLR			RESERVED	TCM0_PARITY_CTRL_ATCM0_ERRADDR_CLR		
NONE	R/W			NONE	R/W			NONE	R/W			NONE	R/W		
0	0h			0	0h			0	0h			0	0h		

Access Types Legend

Table 2-510. R5SS0_TCM_ADDRPARITY_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE		Reserved
22:20	TCM0_PARITY_CTRL_B1TCM1_ERRADDR_CLR	R/W	0h	Write pulse bit field: writing 3'b111 clears the Address latched after parity error for B1TCM of CR5B Reset Source: mod_g_rst_n
19	RESERVED	NONE		Reserved
18:16	TCM0_PARITY_CTRL_B1TCM0_ERRADDR_CLR	R/W	0h	Write pulse bit field: writing 3'b111 clears the Address latched after parity error for B1TCM of CR5A Reset Source: mod_g_rst_n
15	RESERVED	NONE		Reserved
14:12	TCM0_PARITY_CTRL_B0CM1_ERRADDR_CLR	R/W	0h	Write pulse bit field: writing 3'b111 clears the Address latched after parity error for B0TCM of CR5B Reset Source: mod_g_rst_n
11	RESERVED	NONE		Reserved
10:8	TCM0_PARITY_CTRL_B0TCM0_ERRADDR_CLR	R/W	0h	Write pulse bit field: writing 3'b111 clears the Address latched after parity error for B0TCM of CR5A Reset Source: mod_g_rst_n
7	RESERVED	NONE		Reserved
6:4	TCM0_PARITY_CTRL_ATCM1_ERRADDR_CLR	R/W	0h	Write pulse bit field: writing 3'b111 clears the Address latched after parity error for ATCM of CR5B Reset Source: mod_g_rst_n
3	RESERVED	NONE		Reserved
2:0	TCM0_PARITY_CTRL_ATCM0_ERRADDR_CLR	R/W	0h	Pulse bit-field writing 3'b111 clears the Address latched after parity error for ATCM of CR5A Reset Source: mod_g_rst_n

2.3.197 CFG0_R5SS0_CORE0_ADDRPARITY_ERR_ATCM Registers

2.3.197.1 CFG0_CORE0_ADDRPARITY_ERR_ATCM Register (Offset = 18124h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-511. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8124h

Figure 2-254. R5SS0_CORE0_ADDRPARITY_ERR_ATCM Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												ERR_PARITY_ATCM0_R5SS0_ADDR			
NONE												R			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR_PARITY_ATCM0_R5SS0_ADDR															
R															
0h															

Access Types Legend

Table 2-512. R5SS0_CORE0_ADDRPARITY_ERR_ATCM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	ERR_PARITY_ATCM0_R5SS0_ADDR	R	0h	Address lathched when parity error is occurred for ATCM of CR5A Reset Source: mod_g_rst_n

2.3.198 CFG0_R5SS0_CORE1_ADDRPARITY_ERR_ATCM Registers

2.3.198.1 CFG0_CORE1_ADDRPARITY_ERR_ATCM Register (Offset = 18128h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-513. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8128h

Figure 2-255. R5SS0_CORE1_ADDRPARITY_ERR_ATCM Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												ERR_PARITY_ATCM1_R5SS0_ADDR			
NONE												R			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR_PARITY_ATCM1_R5SS0_ADDR															
R															
0h															

Access Types Legend

Table 2-514. R5SS0_CORE1_ADDRPARITY_ERR_ATCM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	ERR_PARITY_ATCM1_R5SS0_ADDR	R	0h	Address lathched when parity error is occurred for ATCM of CR5B Reset Source: mod_g_rst_n

2.3.199 CFG0_R5SS0_CORE0_ERR_ADDRPARITY_B0TCM Registers

2.3.199.1 CFG0_CORE0_ERR_ADDRPARITY_B0TCM Register (Offset = 1812Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-515. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 812Ch

Figure 2-256. R5SS0_CORE0_ERR_ADDRPARITY_B0TCM Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												ERR_PARITY_B0TCM0_R5SS0_ADDR			
NONE												R			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR_PARITY_B0TCM0_R5SS0_ADDR															
R															
0h															

Access Types Legend

Table 2-516. R5SS0_CORE0_ERR_ADDRPARITY_B0TCM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	ERR_PARITY_B0TCM0_R5SS0_ADDR	R	0h	Address lathched when parity error is occurred for B0TCM of CR5A Reset Source: mod_g_rst_n

2.3.200 CFG0_R5SS0_CORE1_ERR_ADDRPARITY_B0TCM Registers

2.3.200.1 CFG0_CORE1_ERR_ADDRPARITY_B0TCM Register (Offset = 18130h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-517. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8130h

Figure 2-257. R5SS0_CORE1_ERR_ADDRPARITY_B0TCM Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												ERR_PARITY_B0TCM1_R5SS0_ADDR			
NONE												R			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR_PARITY_B0TCM1_R5SS0_ADDR															
R															
0h															

Access Types Legend

Table 2-518. R5SS0_CORE1_ERR_ADDRPARITY_B0TCM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	ERR_PARITY_B0TCM1_R5SS0_ADDR	R	0h	Address lathched when parity error is occurred for B0TCM of CR5B Reset Source: mod_g_rst_n

2.3.201 CFG0_R5SS0_CORE0_ERR_ADDRPARITY_B1TCM Registers

2.3.201.1 CFG0_CORE0_ERR_ADDRPARITY_B1TCM Register (Offset = 18134h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-519. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8134h

Figure 2-258. R5SS0_CORE0_ERR_ADDRPARITY_B1TCM Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												ERR_PARITY_B1TCM0_R5SS0_ADDR			
NONE												R			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR_PARITY_B1TCM0_R5SS0_ADDR															
R															
0h															

Access Types Legend

Table 2-520. R5SS0_CORE0_ERR_ADDRPARITY_B1TCM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	ERR_PARITY_B1TCM0_R5SS0_ADDR	R	0h	Address lathched when parity error is occurred for B1TCM of CR5A Reset Source: mod_g_rst_n

2.3.202 CFG0_R5SS0_CORE1_ERR_ADDRPARITY_B1TCM Registers

2.3.202.1 CFG0_CORE1_ERR_ADDRPARITY_B1TCM Register (Offset = 18138h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-521. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8138h

Figure 2-259. R5SS0_CORE1_ERR_ADDRPARITY_B1TCM Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												ERR_PARITY_B1TCM1_R5SS0_ADDR			
NONE												R			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR_PARITY_B1TCM1_R5SS0_ADDR															
R															
0h															

Access Types Legend

Table 2-522. R5SS0_CORE1_ERR_ADDRPARITY_B1TCM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	ERR_PARITY_B1TCM1_R5SS0_ADDR	R	0h	Address lathched when parity error is occurred for B1TCM of CR5B Reset Source: mod_g_rst_n

2.3.203 CFG0_R5SS0_TCM_ADDRPARITY_ERRFORCE Registers

2.3.203.1 CFG0_TCM_ADDRPARITY_ERRFORCE Register (Offset = 1813Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-523. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 813Ch

Figure 2-260. R5SS0_TCM_ADDRPARITY_ERRFORCE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED									TCM0_PARITY_ERRFRC_B1TCM1			RESERVED	TCM0_PARITY_ERRFRC_B1TCM0		
NONE									R/W			NONE	R/W		
0									0h			0	0h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	TCM0_PARITY_ERRFRC_B0TCM1			RESERVED	TCM0_PARITY_ERRFRC_B0TCM0			RESERVED	TCM0_PARITY_ERRFRC_ATCM1			RESERVED	TCM0_PARITY_ERRFRC_ATCM0		
NONE	R/W			NONE	R/W			NONE	R/W			NONE	R/W		
0	0h			0	0h			0	0h			0	0h		

Access Types Legend

Table 2-524. R5SS0_TCM_ADDRPARITY_ERRFORCE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE		Reserved
22:20	TCM0_PARITY_ERRFRC_B1TCM1	R/W	0h	Write pulse bit field: writing 3'b111 forces a parity error for B1TCM of CR5B Reset Source: mod_g_rst_n
19	RESERVED	NONE		Reserved
18:16	TCM0_PARITY_ERRFRC_B1TCM0	R/W	0h	Write pulse bit field: writing 3'b111 forces a parity error for B1TCM of CR5A Reset Source: mod_g_rst_n
15	RESERVED	NONE		Reserved
14:12	TCM0_PARITY_ERRFRC_B0TCM1	R/W	0h	Write pulse bit field: writing 3'b111 forces a parity error for B0TCM of CR5B Reset Source: mod_g_rst_n
11	RESERVED	NONE		Reserved
10:8	TCM0_PARITY_ERRFRC_B0TCM0	R/W	0h	Write pulse bit field: writing 3'b111 forces a parity error for B0TCM of CR5A Reset Source: mod_g_rst_n
7	RESERVED	NONE		Reserved
6:4	TCM0_PARITY_ERRFRC_ATCM1	R/W	0h	Write pulse bit field: writing 3'b111 forces a parity error for ATCM of CR5B Reset Source: mod_g_rst_n
3	RESERVED	NONE		Reserved
2:0	TCM0_PARITY_ERRFRC_ATCM0	R/W	0h	Write pulse bit field: writing 3'b111 forces a parity error for ATCM of CR5A Reset Source: mod_g_rst_n

2.3.204 CFG0_R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_MASK Registers

2.3.204.1 CFG0_CPU0_TCM_ADDRPARITY_ERRAGG_MASK Register (Offset = 18140h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-525. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8140h

Figure 2-261. R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_MASK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU0_B1TCM0_PARITY_ERR	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU0_B0TCM0_PARITY_ERR	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU0_ATCM0_PARITY_ERR
NONE													R/W	R/W	R/W
0													0h	0h	0h

Access Types Legend

Table 2-526. R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU0_B1TCM0_PARITY_ERR	R/W	0h	Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
1	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU0_B0TCM0_PARITY_ERR	R/W	0h	Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
0	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU0_ATCM0_PARITY_ERR	R/W	0h	Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n

2.3.205 CFG0_R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS Registers

2.3.205.1 CFG0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS Register (Offset = 18144h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-527. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8144h

Figure 2-262. R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS1_CPU0_B1TCM0_PARITY_ERR	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS1_CPU0_B0TCM0_PARITY_ERR	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS1_CPU0_ATCM0_PARITY_ERR
NONE													R/W1TC	R/W1TC	R/W1TC
0													0h	0h	0h

Access Types Legend

Table 2-528. R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS1_CPU0_B1TCM0_PARITY_ERR	R/W1TC	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
1	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS1_CPU0_B0TCM0_PARITY_ERR	R/W1TC	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
0	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS1_CPU0_ATCM0_PARITY_ERR	R/W1TC	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

2.3.206 CFG0_R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Registers

2.3.206.1 CFG0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Register (Offset = 18148h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-529. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8148h

Figure 2-263. R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU0_B1TCM0_PARITY_ERR	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU0_B0TCM0_PARITY_ERR	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU0_ATCM0_PARITY_ERR
NONE													R/W1TC	R/W1TC	R/W1TC
0													0h	0h	0h

Access Types Legend

Table 2-530. R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU0_B1TCM0_PARITY_ERR	R/W1TC	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
1	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU0_B0TCM0_PARITY_ERR	R/W1TC	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
0	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU0_ATCM0_PARITY_ERR	R/W1TC	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

2.3.207 CFG0_R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_MASK Registers

2.3.207.1 CFG0_CPU1_TCM_ADDRPARITY_ERRAGG_MASK Register (Offset = 18150h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-531. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8150h

Figure 2-264. R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_MASK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU1_B1TCM1_PARITY_ERR	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU1_B0TCM1_PARITY_ERR	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU1_ATCM1_PARITY_ERR
NONE													R/W	R/W	R/W
0													0h	0h	0h

Access Types Legend

Table 2-532. R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU1_B1TCM1_PARITY_ERR	R/W	0h	Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
1	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU1_B0TCM1_PARITY_ERR	R/W	0h	Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n
0	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU1_ATCM1_PARITY_ERR	R/W	0h	Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU 1 : Interrupt is Masked 0 : Interrupt is Unmasked Reset Source: mod_g_rst_n

2.3.208 CFG0_R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS Registers

2.3.208.1 CFG0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS Register (Offset = 18154h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-533. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8154h

Figure 2-265. R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS1_CPU1_B1TCM1_PARITY_ERR	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS1_CPU1_B0TCM1_PARITY_ERR	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS1_CPU1_ATCM1_PARITY_ERR
NONE													R/W1TC	R/W1TC	R/W1TC
0													0h	0h	0h

Access Types Legend

Table 2-534. R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS1_CPU1_B1TCM1_PARITY_ERR	R/W1TC	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
1	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS1_CPU1_B0TCM1_PARITY_ERR	R/W1TC	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
0	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS1_CPU1_ATCM1_PARITY_ERR	R/W1TC	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

2.3.209 CFG0_R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Registers

2.3.209.1 CFG0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Register (Offset = 18158h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-535. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8158h

Figure 2-266. R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU1_B1TCM1_PARITY_ERR	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU1_B0TCM1_PARITY_ERR	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU1_ATCM1_PARITY_ERR
NONE													R/W1TC	R/W1TC	R/W1TC
0													0h	0h	0h

Access Types Legend

Table 2-536. R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU1_B1TCM1_PARITY_ERR	R/W1TC	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
1	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU1_B0TCM1_PARITY_ERR	R/W1TC	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n
0	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU1_ATCM1_PARITY_ERR	R/W1TC	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt. Reset Source: mod_g_rst_n

2.3.210 CFG0_R5SS1_TCM_ADDRPARITY_CLR Registers

2.3.210.1 CFG0_TCM_ADDRPARITY_CLR Register (Offset = 18160h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-537. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8160h

Figure 2-267. R5SS1_TCM_ADDRPARITY_CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED									TCM1_PARITY_CTRL_B1TCM1_ERRADDR_CLR			RESERVED	TCM1_PARITY_CTRL_B1TCM0_ERRADDR_CLR		
NONE									R/W			NONE	R/W		
0									0h			0	0h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	TCM1_PARITY_CTRL_B0CM1_ERRADDR_CLR			RESERVED	TCM1_PARITY_CTRL_B0TCM0_ERRADDR_CLR			RESERVED	TCM1_PARITY_CTRL_ATCM1_ERRADDR_CLR			RESERVED	TCM1_PARITY_CTRL_ATCM0_ERRADDR_CLR		
NONE	R/W			NONE	R/W			NONE	R/W			NONE	R/W		
0	0h			0	0h			0	0h			0	0h		

Access Types Legend

Table 2-538. R5SS1_TCM_ADDRPARITY_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE		Reserved
22:20	TCM1_PARITY_CTRL_B1TCM1_ERRADDR_CLR	R/W	0h	Write pulse bit field: writing 3'b111 clears the Address latched after parity error for B1TCM of CR5B Reset Source: mod_g_rst_n
19	RESERVED	NONE		Reserved
18:16	TCM1_PARITY_CTRL_B1TCM0_ERRADDR_CLR	R/W	0h	Write pulse bit field: writing 3'b111 clears the Address latched after parity error for B1TCM of CR5A Reset Source: mod_g_rst_n
15	RESERVED	NONE		Reserved
14:12	TCM1_PARITY_CTRL_B0CM1_ERRADDR_CLR	R/W	0h	Write pulse bit field: writing 3'b111 clears the Address latched after parity error for B0TCM of CR5B Reset Source: mod_g_rst_n
11	RESERVED	NONE		Reserved
10:8	TCM1_PARITY_CTRL_B0TCM0_ERRADDR_CLR	R/W	0h	Write pulse bit field: writing 3'b111 clears the Address latched after parity error for B0TCM of CR5A Reset Source: mod_g_rst_n
7	RESERVED	NONE		Reserved
6:4	TCM1_PARITY_CTRL_ATCM1_ERRADDR_CLR	R/W	0h	Write pulse bit field: writing 3'b111 clears the Address latched after parity error for ATCM of CR5B Reset Source: mod_g_rst_n
3	RESERVED	NONE		Reserved
2:0	TCM1_PARITY_CTRL_ATCM0_ERRADDR_CLR	R/W	0h	Pulse bit-field writing 3'b111 clears the Address latched after parity error for ATCM of CR5A Reset Source: mod_g_rst_n

2.3.211 CFG0_R5SS1_CORE0_ADDRPARITY_ERR_ATCM Registers

2.3.211.1 CFG0_CORE0_ADDRPARITY_ERR_ATCM Register (Offset = 18164h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-539. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8164h

Figure 2-268. R5SS1_CORE0_ADDRPARITY_ERR_ATCM Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												ERR_PARITY_ATCM0_R5SS1_ADDR			
NONE												R			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR_PARITY_ATCM0_R5SS1_ADDR															
R															
0h															

Access Types Legend

Table 2-540. R5SS1_CORE0_ADDRPARITY_ERR_ATCM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	ERR_PARITY_ATCM0_R5SS1_ADDR	R	0h	Address lathched when parity error is occurred for ATCM of CR5A Reset Source: mod_g_rst_n

2.3.212 CFG0_R5SS1_CORE1_ADDRPARITY_ERR_ATCM Registers

2.3.212.1 CFG0_CORE1_ADDRPARITY_ERR_ATCM Register (Offset = 18168h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-541. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8168h

Figure 2-269. R5SS1_CORE1_ADDRPARITY_ERR_ATCM Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												ERR_PARITY_ATCM1_R5SS1_ADDR			
NONE												R			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR_PARITY_ATCM1_R5SS1_ADDR															
R															
0h															

Access Types Legend

Table 2-542. R5SS1_CORE1_ADDRPARITY_ERR_ATCM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	ERR_PARITY_ATCM1_R5SS1_ADDR	R	0h	Address lathched when parity error is occurred for ATCM of CR5B Reset Source: mod_g_rst_n

2.3.213 CFG0_R5SS1_CORE0_ERR_ADDRPARITY_B0TCM Registers

2.3.213.1 CFG0_CORE0_ERR_ADDRPARITY_B0TCM Register (Offset = 1816Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-543. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 816Ch

Figure 2-270. R5SS1_CORE0_ERR_ADDRPARITY_B0TCM Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												ERR_PARITY_B0TCM0_R5SS1_ADDR			
NONE												R			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR_PARITY_B0TCM0_R5SS1_ADDR															
R															
0h															

Access Types Legend

Table 2-544. R5SS1_CORE0_ERR_ADDRPARITY_B0TCM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	ERR_PARITY_B0TCM0_R5SS1_ADDR	R	0h	Address lathched when parity error is occurred for B0TCM of CR5A Reset Source: mod_g_rst_n

2.3.214 CFG0_R5SS1_CORE1_ERR_ADDRPARITY_B0TCM Registers

2.3.214.1 CFG0_CORE1_ERR_ADDRPARITY_B0TCM Register (Offset = 18170h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-545. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8170h

Figure 2-271. R5SS1_CORE1_ERR_ADDRPARITY_B0TCM Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												ERR_PARITY_B0TCM1_R5SS1_ADDR			
NONE												R			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR_PARITY_B0TCM1_R5SS1_ADDR															
R															
0h															

Access Types Legend

Table 2-546. R5SS1_CORE1_ERR_ADDRPARITY_B0TCM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	ERR_PARITY_B0TCM1_R5SS1_ADDR	R	0h	Address lathched when parity error is occurred for B0TCM of CR5B Reset Source: mod_g_rst_n

2.3.215 CFG0_R5SS1_CORE0_ERR_ADDRPARITY_B1TCM Registers

2.3.215.1 CFG0_CORE0_ERR_ADDRPARITY_B1TCM Register (Offset = 18174h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-547. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8174h

Figure 2-272. R5SS1_CORE0_ERR_ADDRPARITY_B1TCM Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												ERR_PARITY_B1TCM0_R5SS1_ADDR			
NONE												R			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR_PARITY_B1TCM0_R5SS1_ADDR															
R															
0h															

Access Types Legend

Table 2-548. R5SS1_CORE0_ERR_ADDRPARITY_B1TCM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	ERR_PARITY_B1TCM0_R5SS1_ADDR	R	0h	Address lathched when parity error is occurred for B1TCM of CR5A Reset Source: mod_g_rst_n

2.3.216 CFG0_R5SS1_CORE1_ERR_ADDRPARITY_B1TCM Registers

2.3.216.1 CFG0_CORE1_ERR_ADDRPARITY_B1TCM Register (Offset = 18178h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-549. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8178h

Figure 2-273. R5SS1_CORE1_ERR_ADDRPARITY_B1TCM Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												ERR_PARITY_B1TCM1_R5SS1_ADDR			
NONE												R			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR_PARITY_B1TCM1_R5SS1_ADDR															
R															
0h															

Access Types Legend

Table 2-550. R5SS1_CORE1_ERR_ADDRPARITY_B1TCM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	ERR_PARITY_B1TCM1_R5SS1_ADDR	R	0h	Address lathched when parity error is occurred for B1TCM of CR5B Reset Source: mod_g_rst_n

2.3.217 CFG0_R5SS1_TCM_ADDRPARITY_ERRFORCE Registers

2.3.217.1 CFG0_TCM_ADDRPARITY_ERRFORCE Register (Offset = 1817Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-551. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 817Ch

Figure 2-274. R5SS1_TCM_ADDRPARITY_ERRFORCE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED									TCM1_PARITY_ERRFRC_B1TCM1			RESERVED	TCM1_PARITY_ERRFRC_B1TCM0		
NONE									R/W			NONE	R/W		
0									0h			0	0h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	TCM1_PARITY_ERRFRC_B0TCM1			RESERVED	TCM1_PARITY_ERRFRC_B0TCM0			RESERVED	TCM1_PARITY_ERRFRC_ATCM1			RESERVED	TCM1_PARITY_ERRFRC_ATCM0		
NONE	R/W			NONE	R/W			NONE	R/W			NONE	R/W		
0	0h			0	0h			0	0h			0	0h		

Access Types Legend

Table 2-552. R5SS1_TCM_ADDRPARITY_ERRFORCE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE		Reserved
22:20	TCM1_PARITY_ERRFRC_B1TCM1	R/W	0h	Write pulse bit field: writing 3'b111 forces a parity error for B1TCM of CR5B Reset Source: mod_g_rst_n
19	RESERVED	NONE		Reserved
18:16	TCM1_PARITY_ERRFRC_B1TCM0	R/W	0h	Write pulse bit field: writing 3'b111 forces a parity error for B1TCM of CR5A Reset Source: mod_g_rst_n
15	RESERVED	NONE		Reserved
14:12	TCM1_PARITY_ERRFRC_B0TCM1	R/W	0h	Write pulse bit field: writing 3'b111 forces a parity error for B0TCM of CR5B Reset Source: mod_g_rst_n
11	RESERVED	NONE		Reserved
10:8	TCM1_PARITY_ERRFRC_B0TCM0	R/W	0h	Write pulse bit field: writing 3'b111 forces a parity error for B0TCM of CR5A Reset Source: mod_g_rst_n
7	RESERVED	NONE		Reserved
6:4	TCM1_PARITY_ERRFRC_ATCM1	R/W	0h	Write pulse bit field: writing 3'b111 forces a parity error for ATCM of CR5B Reset Source: mod_g_rst_n
3	RESERVED	NONE		Reserved
2:0	TCM1_PARITY_ERRFRC_ATCM0	R/W	0h	Write pulse bit field: writing 3'b111 forces a parity error for ATCM of CR5A Reset Source: mod_g_rst_n

2.3.218 CFG0_TPCC0_PARITY_CTRL Registers

2.3.218.1 CFG0_PARITY_CTRL Register (Offset = 18180h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-553. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8180h

Figure 2-275. TPCC0_PARITY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															TPCC_PARITY_CTRL_TPCC_A_PARITY_ERR_CLR
NONE															R/W
0															0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											TPCC_PARITY_CTRL_TPCC_A_PARITY_TESTEN	RESERVED			TPCC_PARITY_CTRL_TPCC_A_PARITY_EN
NONE											R/W	NONE			R/W
0											0h	0			0h

Access Types Legend

Table 2-554. TPCC0_PARITY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE		Reserved
16	TPCC_PARITY_CTRL_TPCC_A_PARITY_ERR_CLR	R/W	0h	Write pulse bit field: parity clear bit. Writing 1'b1 will clear the tpcc_a_parity_addr Reset Source: mod_g_rst_n
15:5	RESERVED	NONE		Reserved
4	TPCC_PARITY_CTRL_TPCC_A_PARITY_TESTEN	R/W	0h	parity test enable for tpcc a Reset Source: mod_g_rst_n
3:1	RESERVED	NONE		Reserved
0	TPCC_PARITY_CTRL_TPCC_A_PARITY_EN	R/W	0h	writing 1'b1 enables parity for TPCC_A Reset Source: mod_g_rst_n

2.3.219 CFG0_TPCC0_PARITY_STATUS Registers

2.3.219.1 CFG0_PARITY_STATUS Register (Offset = 18184h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-555. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8184h

Figure 2-276. TPCC0_PARITY_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							TPCC_PARITY_STATUS_TPCC_A_PARITY_ADDR								
NONE							R								
0							0h								

Access Types Legend

Table 2-556. TPCC0_PARITY_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE		Reserved
8:0	TPCC_PARITY_STATUS_TPCC_A_PARITY_ADDR	R	0h	address where parity error happened for tpcca Reset Source: mod_g_rst_n

2.3.220 CFG0_BUS_SAFETY_CTRL Registers

2.3.220.1 CFG0_SAFETY_CTRL Register (Offset = 18200h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-557. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8200h

Figure 2-277. BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_BUS_SAFETY_CTRL_ENABLE		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-558. BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_BUS_SAFETY_CTRL_ENABLE	R/W	0h	Reset Source: mod_g_rst_n

2.3.221 CFG0_R5SS0_CORE0_AXI_RD_BUS_SAFETY_CTRL Registers

2.3.221.1 CFG0_CORE0_AXI_RD_BUS_SAFETY_CTRL Register (Offset = 18220h) [reset = 7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-559. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8220h

Figure 2-278. R5SS0_CORE0_AXI_RD_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_CTRL_TYPE							
NONE								R							
b								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_CTRL_ERR_CLEAR	RESERVED					MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_CTRL_ENABLE		
NONE							R/W	NONE					R/W		
0							0h	0					7h		

Access Types Legend

Table 2-560. R5SS0_CORE0_AXI_RD_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_CTRL_TYPE	R	0h	Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Reset Source: mod_g_rst_n

2.3.222 CFG0_R5SS0_CORE0_AXI_RD_BUS_SAFETY_FI Registers

2.3.222.1 CFG0_CORE0_AXI_RD_BUS_SAFETY_FI Register (Offset = 18224h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-561. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8224h

Figure 2-279. R5SS0_CORE0_AXI_RD_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_FI_SAFE								MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_FI_MAIN							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_FI_DATA								RESERVED		MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_FI_DED	MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_FI_SEC	MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_FI_GLOBAL_SAFE	MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_FI_GLOBAL_MAIN
R/W								NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h								0		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-562. R5SS0_CORE0_AXI_RD_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_FI_SAFE	R/W	0h	Reset Source: mod_g_rst_n
23:16	MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_FI_MAIN	R/W	0h	Reset Source: mod_g_rst_n
15:8	MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_FI_DATA	R/W	0h	Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_FI_DED	R/W	0h	Reset Source: mod_g_rst_n
4	MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_FI_SEC	R/W	0h	Reset Source: mod_g_rst_n
3	MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Reset Source: mod_g_rst_n
2	MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Reset Source: mod_g_rst_n

Table 2-562. R5SS0_CORE0_AXI_RD_BUS_SAFETY_FI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	Reset Source: mod_g_rst_n
0	MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	Reset Source: mod_g_rst_n

2.3.223 CFG0_R5SS0_CORE0_AXI_RD_BUS_SAFETY_ERR Registers

2.3.223.1 CFG0_CORE0_AXI_RD_BUS_SAFETY_ERR Register (Offset = 18228h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-563. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8228h

Figure 2-280. R5SS0_CORE0_AXI_RD_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_ERR_DED								MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_ERR_SEC							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_ERR_COMP_CHECK								MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_ERR_COMP_ERR							
R								R							
0h								0h							

Access Types Legend

Table 2-564. R5SS0_CORE0_AXI_RD_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_ERR_DED	R	0h	Reset Source: mod_g_rst_n
23:16	MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_ERR_SEC	R	0h	Reset Source: mod_g_rst_n
15:8	MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_ERR_COMP_CHECK	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_ERR_COMP_ERR	R	0h	Reset Source: mod_g_rst_n

2.3.224 CFG0_R5SS0_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0 Registers

2.3.224.1 CFG0_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 1822Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-565. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 822Ch

Figure 2-281. R5SS0_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0_D1								MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0_D0							
R								R							
0h								0h							

Access Types Legend

Table 2-566. R5SS0_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Reset Source: mod_g_rst_n

2.3.225 CFG0_R5SS0_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_CMD Registers

2.3.225.1 CFG0_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 18230h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-567. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8230h

Figure 2-282. R5SS0_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															

Access Types Legend

Table 2-568. R5SS0_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.226 CFG0_R5SS0_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_READ Registers

2.3.226.1 CFG0_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_READ Register (Offset = 18234h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-569. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8234h

Figure 2-283. R5SS0_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_READ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															

Access Types Legend

Table 2-570. R5SS0_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_READ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS0_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_READ_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.227 CFG0_R5SS0_CORE1_AXI_RD_BUS_SAFETY_CTRL Registers

2.3.227.1 CFG0_CORE1_AXI_RD_BUS_SAFETY_CTRL Register (Offset = 18240h) [reset = 7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-571. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8240h

Figure 2-284. R5SS0_CORE1_AXI_RD_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_CTRL_TYPE							
NONE								R							
b								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_CTRL_ERR_CLEAR	RESERVED					MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_CTRL_ENABLE		
NONE							R/W	NONE					R/W		
0							0h	0					7h		

Access Types Legend

Table 2-572. R5SS0_CORE1_AXI_RD_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_CTRL_TYPE	R	0h	Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Reset Source: mod_g_rst_n

2.3.228 CFG0_R5SS0_CORE1_AXI_RD_BUS_SAFETY_FI Registers

2.3.228.1 CFG0_CORE1_AXI_RD_BUS_SAFETY_FI Register (Offset = 18244h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-573. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8244h

Figure 2-285. R5SS0_CORE1_AXI_RD_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_FI_SAFE								MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_FI_MAIN							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_FI_DATA								RESERVED		MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_FI_DED	MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_FI_SEC	MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_FI_GLOBAL_SAFE	MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_FI_GLOBAL_MAIN
R/W								NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h								0		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-574. R5SS0_CORE1_AXI_RD_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_FI_SAFE	R/W	0h	Reset Source: mod_g_rst_n
23:16	MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_FI_MAIN	R/W	0h	Reset Source: mod_g_rst_n
15:8	MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_FI_DATA	R/W	0h	Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_FI_DED	R/W	0h	Reset Source: mod_g_rst_n
4	MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_FI_SEC	R/W	0h	Reset Source: mod_g_rst_n
3	MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Reset Source: mod_g_rst_n
2	MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Reset Source: mod_g_rst_n

Table 2-574. R5SS0_CORE1_AXI_RD_BUS_SAFETY_FI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	Reset Source: mod_g_rst_n
0	MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	Reset Source: mod_g_rst_n

2.3.229 CFG0_R5SS0_CORE1_AXI_RD_BUS_SAFETY_ERR Registers

2.3.229.1 CFG0_CORE1_AXI_RD_BUS_SAFETY_ERR Register (Offset = 18248h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-575. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8248h

Figure 2-286. R5SS0_CORE1_AXI_RD_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_ERR_DED								MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_ERR_SEC							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_ERR_COMP_CHECK								MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_ERR_COMP_ERR							
R								R							
0h								0h							

Access Types Legend

Table 2-576. R5SS0_CORE1_AXI_RD_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_ERR_DED	R	0h	Reset Source: mod_g_rst_n
23:16	MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_ERR_SEC	R	0h	Reset Source: mod_g_rst_n
15:8	MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_ERR_COMP_CHECK	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_ERR_COMP_ERR	R	0h	Reset Source: mod_g_rst_n

2.3.230 CFG0_R5SS0_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0 Registers

2.3.230.1 CFG0_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 1824Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-577. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 824Ch

Figure 2-287. R5SS0_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0_D1								MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0_D0							
R								R							
0h								0h							

Access Types Legend

Table 2-578. R5SS0_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Reset Source: mod_g_rst_n

2.3.231 CFG0_R5SS0_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_CMD Registers

2.3.231.1 CFG0_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 18250h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-579. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8250h

Figure 2-288. R5SS0_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															

Access Types Legend

Table 2-580. R5SS0_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.232 CFG0_R5SS0_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_READ Registers

2.3.232.1 CFG0_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_READ Register (Offset = 18254h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-581. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8254h

Figure 2-289. R5SS0_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_READ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															

Access Types Legend

Table 2-582. R5SS0_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_READ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_READ_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.233 CFG0_R5SS1_CORE0_AXI_RD_BUS_SAFETY_CTRL Registers

2.3.233.1 CFG0_CORE0_AXI_RD_BUS_SAFETY_CTRL Register (Offset = 18260h) [reset = 7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-583. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8260h

Figure 2-290. R5SS1_CORE0_AXI_RD_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MSS_R5FSS01_AXI_RD_BUS_SAFETY_CTRL_TYPE							
NONE								R							
b								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							MSS_R5FSS01_AXI_RD_BUS_SAFETY_CTRL_ERR_CLEAR	RESERVED					MSS_R5FSS01_AXI_RD_BUS_SAFETY_CTRL_ENABLE		
NONE							R/W	NONE					R/W		
0							0h	0					7h		

Access Types Legend

Table 2-584. R5SS1_CORE0_AXI_RD_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	MSS_R5FSS01_AXI_RD_BUS_SAFETY_CTRL_TYPE	R	0h	Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	MSS_R5FSS01_AXI_RD_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	MSS_R5FSS01_AXI_RD_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Reset Source: mod_g_rst_n

2.3.234 CFG0_R5SS1_CORE0_AXI_RD_BUS_SAFETY_FI Registers

2.3.234.1 CFG0_CORE0_AXI_RD_BUS_SAFETY_FI Register (Offset = 18264h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-585. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8264h

Figure 2-291. R5SS1_CORE0_AXI_RD_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS01_AXI_RD_BUS_SAFETY_FI_SAFE								MSS_R5FSS01_AXI_RD_BUS_SAFETY_FI_MAIN							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS01_AXI_RD_BUS_SAFETY_FI_DATA								RESERVED		MSS_R5FSS01_AXI_RD_BUS_SAFETY_FI_DED	MSS_R5FSS01_AXI_RD_BUS_SAFETY_FI_SEC	MSS_R5FSS01_AXI_RD_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	MSS_R5FSS01_AXI_RD_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	MSS_R5FSS01_AXI_RD_BUS_SAFETY_FI_GLOBAL_SAFE	MSS_R5FSS01_AXI_RD_BUS_SAFETY_FI_GLOBAL_MAIN
R/W								NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h								0		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-586. R5SS1_CORE0_AXI_RD_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_R5FSS01_AXI_RD_BUS_SAFETY_FI_SAFE	R/W	0h	Reset Source: mod_g_rst_n
23:16	MSS_R5FSS01_AXI_RD_BUS_SAFETY_FI_MAIN	R/W	0h	Reset Source: mod_g_rst_n
15:8	MSS_R5FSS01_AXI_RD_BUS_SAFETY_FI_DATA	R/W	0h	Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	MSS_R5FSS01_AXI_RD_BUS_SAFETY_FI_DED	R/W	0h	Reset Source: mod_g_rst_n
4	MSS_R5FSS01_AXI_RD_BUS_SAFETY_FI_SEC	R/W	0h	Reset Source: mod_g_rst_n
3	MSS_R5FSS01_AXI_RD_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Reset Source: mod_g_rst_n
2	MSS_R5FSS01_AXI_RD_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Reset Source: mod_g_rst_n
1	MSS_R5FSS01_AXI_RD_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	Reset Source: mod_g_rst_n

Table 2-586. R5SS1_CORE0_AXI_RD_BUS_SAFETY_FI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MSS_R5FSS01_AXI_RD_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	Reset Source: mod_g_rst_n

2.3.235 CFG0_R5SS1_CORE0_AXI_RD_BUS_SAFETY_ERR Registers

2.3.235.1 CFG0_CORE0_AXI_RD_BUS_SAFETY_ERR Register (Offset = 18268h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-587. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8268h

Figure 2-292. R5SS1_CORE0_AXI_RD_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS01_AXI_RD_BUS_SAFETY_ERR_DED								MSS_R5FSS01_AXI_RD_BUS_SAFETY_ERR_SEC							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS01_AXI_RD_BUS_SAFETY_ERR_COMP_CHECK								MSS_R5FSS01_AXI_RD_BUS_SAFETY_ERR_COMP_ERR							
R								R							
0h								0h							

Access Types Legend

Table 2-588. R5SS1_CORE0_AXI_RD_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_R5FSS01_AXI_RD_BUS_SAFETY_ERR_DED	R	0h	Reset Source: mod_g_rst_n
23:16	MSS_R5FSS01_AXI_RD_BUS_SAFETY_ERR_SEC	R	0h	Reset Source: mod_g_rst_n
15:8	MSS_R5FSS01_AXI_RD_BUS_SAFETY_ERR_COMP_CHECK	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_R5FSS01_AXI_RD_BUS_SAFETY_ERR_COMP_ERR	R	0h	Reset Source: mod_g_rst_n

2.3.236 CFG0_R5SS1_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0 Registers

2.3.236.1 CFG0_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 1826Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-589. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 826Ch

Figure 2-293. R5SS1_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS01_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0_D1								MSS_R5FSS01_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0_D0							
R								R							
0h								0h							

Access Types Legend

Table 2-590. R5SS1_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_R5FSS01_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_R5FSS01_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Reset Source: mod_g_rst_n

2.3.237 CFG0_R5SS1_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_CMD Registers

2.3.237.1 CFG0_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 18270h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-591. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8270h

Figure 2-294. R5SS1_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS01_AXI_RD_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS01_AXI_RD_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															

Access Types Legend

Table 2-592. R5SS1_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS01_AXI_RD_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.238 CFG0_R5SS1_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_READ Registers

2.3.238.1 CFG0_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_READ Register (Offset = 18274h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-593. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8274h

Figure 2-295. R5SS1_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_READ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS01_AXI_RD_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS01_AXI_RD_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															

Access Types Legend

Table 2-594. R5SS1_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_READ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS01_AXI_RD_BUS_SAFETY_ERR_STAT_READ_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.239 CFG0_R5SS1_CORE1_AXI_RD_BUS_SAFETY_CTRL Registers

2.3.239.1 CFG0_CORE1_AXI_RD_BUS_SAFETY_CTRL Register (Offset = 18280h) [reset = 7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-595. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8280h

Figure 2-296. R5SS1_CORE1_AXI_RD_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MSS_R5FSS11_AXI_RD_BUS_SAFETY_CTRL_TYPE							
NONE								R							
b								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							MSS_R5FSS11_AXI_RD_BUS_SAFETY_CTRL_ERR_CLEAR	RESERVED					MSS_R5FSS11_AXI_RD_BUS_SAFETY_CTRL_ENABLE		
NONE							R/W	NONE					R/W		
0							0h	0					7h		

Access Types Legend

Table 2-596. R5SS1_CORE1_AXI_RD_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	MSS_R5FSS11_AXI_RD_BUS_SAFETY_CTRL_TYPE	R	0h	Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	MSS_R5FSS11_AXI_RD_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	MSS_R5FSS11_AXI_RD_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Reset Source: mod_g_rst_n

2.3.240 CFG0_R5SS1_CORE1_AXI_RD_BUS_SAFETY_FI Registers

2.3.240.1 CFG0_CORE1_AXI_RD_BUS_SAFETY_FI Register (Offset = 18284h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-597. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8284h

Figure 2-297. R5SS1_CORE1_AXI_RD_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS11_AXI_RD_BUS_SAFETY_FI_SAFE								MSS_R5FSS11_AXI_RD_BUS_SAFETY_FI_MAIN							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS11_AXI_RD_BUS_SAFETY_FI_DATA								RESERVED		MSS_R5FSS11_AXI_RD_BUS_SAFETY_FI_DED	MSS_R5FSS11_AXI_RD_BUS_SAFETY_FI_SEC	MSS_R5FSS11_AXI_RD_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	MSS_R5FSS11_AXI_RD_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	MSS_R5FSS11_AXI_RD_BUS_SAFETY_FI_GLOBAL_SAFE	MSS_R5FSS11_AXI_RD_BUS_SAFETY_FI_GLOBAL_MAIN
R/W								NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h								0		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-598. R5SS1_CORE1_AXI_RD_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_R5FSS11_AXI_RD_BUS_SAFETY_FI_SAFE	R/W	0h	Reset Source: mod_g_rst_n
23:16	MSS_R5FSS11_AXI_RD_BUS_SAFETY_FI_MAIN	R/W	0h	Reset Source: mod_g_rst_n
15:8	MSS_R5FSS11_AXI_RD_BUS_SAFETY_FI_DATA	R/W	0h	Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	MSS_R5FSS11_AXI_RD_BUS_SAFETY_FI_DED	R/W	0h	Reset Source: mod_g_rst_n
4	MSS_R5FSS11_AXI_RD_BUS_SAFETY_FI_SEC	R/W	0h	Reset Source: mod_g_rst_n
3	MSS_R5FSS11_AXI_RD_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Reset Source: mod_g_rst_n
2	MSS_R5FSS11_AXI_RD_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Reset Source: mod_g_rst_n
1	MSS_R5FSS11_AXI_RD_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	Reset Source: mod_g_rst_n

Table 2-598. R5SS1_CORE1_AXI_RD_BUS_SAFETY_FI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MSS_R5FSS11_AXI_RD_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	Reset Source: mod_g_rst_n

2.3.241 CFG0_R5SS1_CORE1_AXI_RD_BUS_SAFETY_ERR Registers

2.3.241.1 CFG0_CORE1_AXI_RD_BUS_SAFETY_ERR Register (Offset = 18288h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-599. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8288h

Figure 2-298. R5SS1_CORE1_AXI_RD_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS11_AXI_RD_BUS_SAFETY_ERR_DED								MSS_R5FSS11_AXI_RD_BUS_SAFETY_ERR_SEC							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS11_AXI_RD_BUS_SAFETY_ERR_COMP_CHECK								MSS_R5FSS11_AXI_RD_BUS_SAFETY_ERR_COMP_ERR							
R								R							
0h								0h							

Access Types Legend

Table 2-600. R5SS1_CORE1_AXI_RD_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_R5FSS11_AXI_RD_BUS_SAFETY_ERR_DED	R	0h	Reset Source: mod_g_rst_n
23:16	MSS_R5FSS11_AXI_RD_BUS_SAFETY_ERR_SEC	R	0h	Reset Source: mod_g_rst_n
15:8	MSS_R5FSS11_AXI_RD_BUS_SAFETY_ERR_COMP_CHECK	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_R5FSS11_AXI_RD_BUS_SAFETY_ERR_COMP_ERR	R	0h	Reset Source: mod_g_rst_n

2.3.242 CFG0_R5SS1_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0 Registers

2.3.242.1 CFG0_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 1828Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-601. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 828Ch

Figure 2-299. R5SS1_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS11_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0_D1								MSS_R5FSS11_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0_D0							
R								R							
0h								0h							

Access Types Legend

Table 2-602. R5SS1_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_R5FSS11_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_R5FSS11_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Reset Source: mod_g_rst_n

2.3.243 CFG0_R5SS1_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_CMD Registers

2.3.243.1 CFG0_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 18290h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-603. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8290h

Figure 2-300. R5SS1_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS11_AXI_RD_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS11_AXI_RD_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															

Access Types Legend

Table 2-604. R5SS1_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS11_AXI_RD_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.244 CFG0_R5SS1_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_READ Registers

2.3.244.1 CFG0_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_READ Register (Offset = 18294h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-605. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8294h

Figure 2-301. R5SS1_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_READ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS11_AXI_RD_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS11_AXI_RD_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															

Access Types Legend

Table 2-606. R5SS1_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_READ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS11_AXI_RD_BUS_SAFETY_ERR_STAT_READ_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.245 CFG0_R5SS0_CORE0_AXI_WR_BUS_SAFETY_CTRL Registers

2.3.245.1 CFG0_CORE0_AXI_WR_BUS_SAFETY_CTRL Register (Offset = 182A0h) [reset = 7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-607. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 82A0h

Figure 2-302. R5SS0_CORE0_AXI_WR_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_CTRL_TYPE							
NONE								R							
b								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_CTRL_ERR_CLEAR	RESERVED					MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_CTRL_ENABLE		
NONE							R/W	NONE					R/W		
0							0h	0					7h		

Access Types Legend

Table 2-608. R5SS0_CORE0_AXI_WR_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_CTRL_TYPE	R	0h	Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Reset Source: mod_g_rst_n

2.3.246 CFG0_R5SS0_CORE0_AXI_WR_BUS_SAFETY_FI Registers

2.3.246.1 CFG0_CORE0_AXI_WR_BUS_SAFETY_FI Register (Offset = 182A4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-609. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 82A4h

Figure 2-303. R5SS0_CORE0_AXI_WR_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_FI_SAFE								MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_FI_MAIN							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_FI_DATA								RESERVED		MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_FI_DED	MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_FI_SEC	MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_FI_GLOBAL_SAFE	MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_FI_GLOBAL_MAIN
R/W								NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h								0		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-610. R5SS0_CORE0_AXI_WR_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_FI_SAFE	R/W	0h	Reset Source: mod_g_rst_n
23:16	MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_FI_MAIN	R/W	0h	Reset Source: mod_g_rst_n
15:8	MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_FI_DATA	R/W	0h	Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_FI_DED	R/W	0h	Reset Source: mod_g_rst_n
4	MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_FI_SEC	R/W	0h	Reset Source: mod_g_rst_n
3	MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Reset Source: mod_g_rst_n
2	MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Reset Source: mod_g_rst_n

Table 2-610. R5SS0_CORE0_AXI_WR_BUS_SAFETY_FI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	Reset Source: mod_g_rst_n
0	MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	Reset Source: mod_g_rst_n

2.3.247 CFG0_R5SS0_CORE0_AXI_WR_BUS_SAFETY_ERR Registers

2.3.247.1 CFG0_CORE0_AXI_WR_BUS_SAFETY_ERR Register (Offset = 182A8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-611. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 82A8h

Figure 2-304. R5SS0_CORE0_AXI_WR_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_ERR_DED								MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_ERR_SEC							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_ERR_COMP_CHECK								MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_ERR_COMP_ERR							
R								R							
0h								0h							

Access Types Legend

Table 2-612. R5SS0_CORE0_AXI_WR_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_ERR_DED	R	0h	Reset Source: mod_g_rst_n
23:16	MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_ERR_SEC	R	0h	Reset Source: mod_g_rst_n
15:8	MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_ERR_COMP_CHECK	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_ERR_COMP_ERR	R	0h	Reset Source: mod_g_rst_n

2.3.248 CFG0_R5SS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0 Registers

2.3.248.1 CFG0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 182ACh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-613. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 82ACh

Figure 2-305. R5SS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0_D1								MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0_D0							
R								R							
0h								0h							

Access Types Legend

Table 2-614. R5SS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Reset Source: mod_g_rst_n

2.3.249 CFG0_R5SS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_CMD Registers

2.3.249.1 CFG0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 182B0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-615. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 82B0h

Figure 2-306. R5SS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															

Access Types Legend

Table 2-616. R5SS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.250 CFG0_R5SS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE Registers

2.3.250.1 CFG0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE Register (Offset = 182B4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-617. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 82B4h

Figure 2-307. R5SS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															

Access Types Legend

Table 2-618. R5SS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.251 CFG0_R5SS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP Registers

2.3.251.1 CFG0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP Register (Offset = 182B8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-619. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 82B8h

Figure 2-308. R5SS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															

Access Types Legend

Table 2-620. R5SS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.252 CFG0_R5SS0_CORE1_AXI_WR_BUS_SAFETY_CTRL Registers

2.3.252.1 CFG0_CORE1_AXI_WR_BUS_SAFETY_CTRL Register (Offset = 182C0h) [reset = 7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-621. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 82C0h

Figure 2-309. R5SS0_CORE1_AXI_WR_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_CTRL_TYPE							
NONE								R							
b								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_CTRL_ERR_CLEAR	RESERVED					MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_CTRL_ENABLE		
NONE							R/W	NONE					R/W		
0							0h	0					7h		

Access Types Legend

Table 2-622. R5SS0_CORE1_AXI_WR_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_CTRL_TYPE	R	0h	Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Reset Source: mod_g_rst_n

2.3.253 CFG0_R5SS0_CORE1_AXI_WR_BUS_SAFETY_FI Registers

2.3.253.1 CFG0_CORE1_AXI_WR_BUS_SAFETY_FI Register (Offset = 182C4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-623. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 82C4h

Figure 2-310. R5SS0_CORE1_AXI_WR_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_FI_SAFE								MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_FI_MAIN							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_FI_DATA								RESERVED		MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_FI_DED	MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_FI_SEC	MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_FI_GLOBAL_SAFE	MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_FI_GLOBAL_MAIN
R/W								NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h								0		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-624. R5SS0_CORE1_AXI_WR_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_FI_SAFE	R/W	0h	Reset Source: mod_g_rst_n
23:16	MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_FI_MAIN	R/W	0h	Reset Source: mod_g_rst_n
15:8	MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_FI_DATA	R/W	0h	Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_FI_DED	R/W	0h	Reset Source: mod_g_rst_n
4	MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_FI_SEC	R/W	0h	Reset Source: mod_g_rst_n
3	MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Reset Source: mod_g_rst_n
2	MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Reset Source: mod_g_rst_n

Table 2-624. R5SS0_CORE1_AXI_WR_BUS_SAFETY_FI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	Reset Source: mod_g_rst_n
0	MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	Reset Source: mod_g_rst_n

2.3.254 CFG0_R5SS0_CORE1_AXI_WR_BUS_SAFETY_ERR Registers

2.3.254.1 CFG0_CORE1_AXI_WR_BUS_SAFETY_ERR Register (Offset = 182C8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-625. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 82C8h

Figure 2-311. R5SS0_CORE1_AXI_WR_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_ERR_DED								MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_ERR_SEC							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_ERR_COMP_CHECK								MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_ERR_COMP_ERR							
R								R							
0h								0h							

Access Types Legend

Table 2-626. R5SS0_CORE1_AXI_WR_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_ERR_DED	R	0h	Reset Source: mod_g_rst_n
23:16	MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_ERR_SEC	R	0h	Reset Source: mod_g_rst_n
15:8	MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_ERR_COMP_CHECK	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_ERR_COMP_ERR	R	0h	Reset Source: mod_g_rst_n

2.3.255 CFG0_R5SS0_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0 Registers

2.3.255.1 CFG0_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 182CCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-627. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 82CCh

Figure 2-312. R5SS0_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0_D1								MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0_D0							
R								R							
0h								0h							

Access Types Legend

Table 2-628. R5SS0_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Reset Source: mod_g_rst_n

2.3.256 CFG0_R5SS0_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_CMD Registers

2.3.256.1 CFG0_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 182D0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-629. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 82D0h

Figure 2-313. R5SS0_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															

Access Types Legend

Table 2-630. R5SS0_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.257 CFG0_R5SS0_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE Registers

2.3.257.1 CFG0_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE Register (Offset = 182D4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-631. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 82D4h

Figure 2-314. R5SS0_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															

Access Types Legend

Table 2-632. R5SS0_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.258 CFG0_R5SS0_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP Registers

2.3.258.1 CFG0_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP Register (Offset = 182D8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-633. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 82D8h

Figure 2-315. R5SS0_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															

Access Types Legend

Table 2-634. R5SS0_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.259 CFG0_R5SS1_CORE0_AXI_WR_BUS_SAFETY_CTRL Registers

2.3.259.1 CFG0_CORE0_AXI_WR_BUS_SAFETY_CTRL Register (Offset = 182E0h) [reset = 7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-635. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 82E0h

Figure 2-316. R5SS1_CORE0_AXI_WR_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MSS_R5FSS01_AXI_WR_BUS_SAFETY_CTRL_TYPE							
NONE								R							
b								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							MSS_R5FSS01_AXI_WR_BUS_SAFETY_CTRL_ERR_CLEAR	RESERVED					MSS_R5FSS01_AXI_WR_BUS_SAFETY_CTRL_ENABLE		
NONE							R/W	NONE					R/W		
0							0h	0					7h		

Access Types Legend

Table 2-636. R5SS1_CORE0_AXI_WR_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	MSS_R5FSS01_AXI_WR_BUS_SAFETY_CTRL_TYPE	R	0h	Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	MSS_R5FSS01_AXI_WR_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	MSS_R5FSS01_AXI_WR_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Reset Source: mod_g_rst_n

2.3.260 CFG0_R5SS1_CORE0_AXI_WR_BUS_SAFETY_FI Registers

2.3.260.1 CFG0_CORE0_AXI_WR_BUS_SAFETY_FI Register (Offset = 182E4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-637. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 82E4h

Figure 2-317. R5SS1_CORE0_AXI_WR_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS01_AXI_WR_BUS_SAFETY_FI_SAFE								MSS_R5FSS01_AXI_WR_BUS_SAFETY_FI_MAIN							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS01_AXI_WR_BUS_SAFETY_FI_DATA								RESERVED		MSS_R5FSS01_AXI_WR_BUS_SAFETY_FI_DED	MSS_R5FSS01_AXI_WR_BUS_SAFETY_FI_SEC	MSS_R5FSS01_AXI_WR_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	MSS_R5FSS01_AXI_WR_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	MSS_R5FSS01_AXI_WR_BUS_SAFETY_FI_GLOBAL_SAFE	MSS_R5FSS01_AXI_WR_BUS_SAFETY_FI_GLOBAL_MAIN
R/W								NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h								0		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-638. R5SS1_CORE0_AXI_WR_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_R5FSS01_AXI_WR_BUS_SAFETY_FI_SAFE	R/W	0h	Reset Source: mod_g_rst_n
23:16	MSS_R5FSS01_AXI_WR_BUS_SAFETY_FI_MAIN	R/W	0h	Reset Source: mod_g_rst_n
15:8	MSS_R5FSS01_AXI_WR_BUS_SAFETY_FI_DATA	R/W	0h	Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	MSS_R5FSS01_AXI_WR_BUS_SAFETY_FI_DED	R/W	0h	Reset Source: mod_g_rst_n
4	MSS_R5FSS01_AXI_WR_BUS_SAFETY_FI_SEC	R/W	0h	Reset Source: mod_g_rst_n
3	MSS_R5FSS01_AXI_WR_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Reset Source: mod_g_rst_n
2	MSS_R5FSS01_AXI_WR_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Reset Source: mod_g_rst_n
1	MSS_R5FSS01_AXI_WR_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	Reset Source: mod_g_rst_n

Table 2-638. R5SS1_CORE0_AXI_WR_BUS_SAFETY_FI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MSS_R5FSS01_AXI_WR_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	Reset Source: mod_g_rst_n

2.3.261 CFG0_R5SS1_CORE0_AXI_WR_BUS_SAFETY_ERR Registers

2.3.261.1 CFG0_CORE0_AXI_WR_BUS_SAFETY_ERR Register (Offset = 182E8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-639. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 82E8h

Figure 2-318. R5SS1_CORE0_AXI_WR_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS01_AXI_WR_BUS_SAFETY_ERR_DED								MSS_R5FSS01_AXI_WR_BUS_SAFETY_ERR_SEC							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS01_AXI_WR_BUS_SAFETY_ERR_COMP_CHECK								MSS_R5FSS01_AXI_WR_BUS_SAFETY_ERR_COMP_ERR							
R								R							
0h								0h							

Access Types Legend

Table 2-640. R5SS1_CORE0_AXI_WR_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_R5FSS01_AXI_WR_BUS_SAFETY_ERR_DED	R	0h	Reset Source: mod_g_rst_n
23:16	MSS_R5FSS01_AXI_WR_BUS_SAFETY_ERR_SEC	R	0h	Reset Source: mod_g_rst_n
15:8	MSS_R5FSS01_AXI_WR_BUS_SAFETY_ERR_COMP_CHECK	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_R5FSS01_AXI_WR_BUS_SAFETY_ERR_COMP_ERR	R	0h	Reset Source: mod_g_rst_n

2.3.262 CFG0_R5SS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0 Registers

2.3.262.1 CFG0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 182ECh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-641. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 82ECh

Figure 2-319. R5SS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS01_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0_D1								MSS_R5FSS01_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0_D0							
R								R							
0h								0h							

Access Types Legend

Table 2-642. R5SS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_R5FSS01_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_R5FSS01_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Reset Source: mod_g_rst_n

2.3.263 CFG0_R5SS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_CMD Registers

2.3.263.1 CFG0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 182F0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-643. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 82F0h

Figure 2-320. R5SS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS01_AXI_WR_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS01_AXI_WR_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															

Access Types Legend

Table 2-644. R5SS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS01_AXI_WR_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.264 CFG0_R5SS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE Registers

2.3.264.1 CFG0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE Register (Offset = 182F4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-645. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 82F4h

Figure 2-321. R5SS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS01_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS01_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															

Access Types Legend

Table 2-646. R5SS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS01_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.265 CFG0_R5SS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP Registers

2.3.265.1 CFG0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP Register (Offset = 182F8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-647. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 82F8h

Figure 2-322. R5SS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS01_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS01_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															

Access Types Legend

Table 2-648. R5SS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS01_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.266 CFG0_R5SS1_CORE1_AXI_WR_BUS_SAFETY_CTRL Registers

2.3.266.1 CFG0_CORE1_AXI_WR_BUS_SAFETY_CTRL Register (Offset = 18300h) [reset = 7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-649. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8300h

Figure 2-323. R5SS1_CORE1_AXI_WR_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MSS_R5FSS11_AXI_WR_BUS_SAFETY_CTRL_TYPE							
NONE								R							
b								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							MSS_R5FSS11_AXI_WR_BUS_SAFETY_CTRL_ERR_CLEAR	RESERVED					MSS_R5FSS11_AXI_WR_BUS_SAFETY_CTRL_ENABLE		
NONE							R/W	NONE					R/W		
0							0h	0					7h		

Access Types Legend

Table 2-650. R5SS1_CORE1_AXI_WR_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	MSS_R5FSS11_AXI_WR_BUS_SAFETY_CTRL_TYPE	R	0h	Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	MSS_R5FSS11_AXI_WR_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	MSS_R5FSS11_AXI_WR_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Reset Source: mod_g_rst_n

2.3.267 CFG0_R5SS1_CORE1_AXI_WR_BUS_SAFETY_FI Registers

2.3.267.1 CFG0_CORE1_AXI_WR_BUS_SAFETY_FI Register (Offset = 18304h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-651. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8304h

Figure 2-324. R5SS1_CORE1_AXI_WR_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS11_AXI_WR_BUS_SAFETY_FI_SAFE								MSS_R5FSS11_AXI_WR_BUS_SAFETY_FI_MAIN							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS11_AXI_WR_BUS_SAFETY_FI_DATA								RESERVED		MSS_R5FSS11_AXI_WR_BUS_SAFETY_FI_DED	MSS_R5FSS11_AXI_WR_BUS_SAFETY_FI_SEC	MSS_R5FSS11_AXI_WR_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	MSS_R5FSS11_AXI_WR_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	MSS_R5FSS11_AXI_WR_BUS_SAFETY_FI_GLOBAL_SAFE	MSS_R5FSS11_AXI_WR_BUS_SAFETY_FI_GLOBAL_MAIN
R/W								NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h								0		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-652. R5SS1_CORE1_AXI_WR_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_R5FSS11_AXI_WR_BUS_SAFETY_FI_SAFE	R/W	0h	Reset Source: mod_g_rst_n
23:16	MSS_R5FSS11_AXI_WR_BUS_SAFETY_FI_MAIN	R/W	0h	Reset Source: mod_g_rst_n
15:8	MSS_R5FSS11_AXI_WR_BUS_SAFETY_FI_DATA	R/W	0h	Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	MSS_R5FSS11_AXI_WR_BUS_SAFETY_FI_DED	R/W	0h	Reset Source: mod_g_rst_n
4	MSS_R5FSS11_AXI_WR_BUS_SAFETY_FI_SEC	R/W	0h	Reset Source: mod_g_rst_n
3	MSS_R5FSS11_AXI_WR_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Reset Source: mod_g_rst_n
2	MSS_R5FSS11_AXI_WR_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Reset Source: mod_g_rst_n
1	MSS_R5FSS11_AXI_WR_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	Reset Source: mod_g_rst_n

Table 2-652. R5SS1_CORE1_AXI_WR_BUS_SAFETY_FI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MSS_R5FSS11_AXI_WR_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	Reset Source: mod_g_rst_n

2.3.268 CFG0_R5SS1_CORE1_AXI_WR_BUS_SAFETY_ERR Registers

2.3.268.1 CFG0_CORE1_AXI_WR_BUS_SAFETY_ERR Register (Offset = 18308h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-653. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8308h

Figure 2-325. R5SS1_CORE1_AXI_WR_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS11_AXI_WR_BUS_SAFETY_ERR_DED								MSS_R5FSS11_AXI_WR_BUS_SAFETY_ERR_SEC							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS11_AXI_WR_BUS_SAFETY_ERR_COMP_CHECK								MSS_R5FSS11_AXI_WR_BUS_SAFETY_ERR_COMP_ERR							
R								R							
0h								0h							

Access Types Legend

Table 2-654. R5SS1_CORE1_AXI_WR_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_R5FSS11_AXI_WR_BUS_SAFETY_ERR_DED	R	0h	Reset Source: mod_g_rst_n
23:16	MSS_R5FSS11_AXI_WR_BUS_SAFETY_ERR_SEC	R	0h	Reset Source: mod_g_rst_n
15:8	MSS_R5FSS11_AXI_WR_BUS_SAFETY_ERR_COMP_CHECK	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_R5FSS11_AXI_WR_BUS_SAFETY_ERR_COMP_ERR	R	0h	Reset Source: mod_g_rst_n

2.3.269 CFG0_R5SS1_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0 Registers

2.3.269.1 CFG0_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 1830Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-655. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 830Ch

Figure 2-326. R5SS1_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS11_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0_D1								MSS_R5FSS11_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0_D0							
R								R							
0h								0h							

Access Types Legend

Table 2-656. R5SS1_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_R5FSS11_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_R5FSS11_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Reset Source: mod_g_rst_n

2.3.270 CFG0_R5SS1_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_CMD Registers

2.3.270.1 CFG0_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 18310h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-657. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8310h

Figure 2-327. R5SS1_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS11_AXI_WR_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS11_AXI_WR_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															

Access Types Legend

Table 2-658. R5SS1_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS11_AXI_WR_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.271 CFG0_R5SS1_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE Registers

2.3.271.1 CFG0_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE Register (Offset = 18314h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-659. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8314h

Figure 2-328. R5SS1_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS11_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS11_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															

Access Types Legend

Table 2-660. R5SS1_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS11_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.272 CFG0_R5SS1_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP Registers

2.3.272.1 CFG0_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP Register (Offset = 18318h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-661. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8318h

Figure 2-329. R5SS1_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS11_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS11_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															

Access Types Legend

Table 2-662. R5SS1_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS11_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.273 CFG0_R5SS0_CORE0_AXI_S_BUS_SAFETY_CTRL Registers

2.3.273.1 CFG0_CORE0_AXI_S_BUS_SAFETY_CTRL Register (Offset = 18320h) [reset = 7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-663. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8320h

Figure 2-330. R5SS0_CORE0_AXI_S_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_CTRL_TYPE							
NONE								R							
b								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_CTRL_ERR_CLEAR	RESERVED					MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_CTRL_ENABLE		
NONE							R/W	NONE					R/W		
0							0h	0					7h		

Access Types Legend

Table 2-664. R5SS0_CORE0_AXI_S_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_CTRL_TYPE	R	0h	Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Reset Source: mod_g_rst_n

2.3.274 CFG0_R5SS0_CORE0_AXI_S_BUS_SAFETY_FI Registers

2.3.274.1 CFG0_CORE0_AXI_S_BUS_SAFETY_FI Register (Offset = 18324h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-665. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8324h

Figure 2-331. R5SS0_CORE0_AXI_S_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_FI_SAFE								MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_FI_MAIN							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_FI_DATA								RESERVED		MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_FI_DED	MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_FI_SEC	MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_FI_GLOBAL_SAFE	MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_FI_GLOBAL_MAIN
R/W								NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h								0		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-666. R5SS0_CORE0_AXI_S_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_FI_SAFE	R/W	0h	Reset Source: mod_g_rst_n
23:16	MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_FI_MAIN	R/W	0h	Reset Source: mod_g_rst_n
15:8	MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_FI_DATA	R/W	0h	Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_FI_DED	R/W	0h	Reset Source: mod_g_rst_n
4	MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_FI_SEC	R/W	0h	Reset Source: mod_g_rst_n
3	MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Reset Source: mod_g_rst_n
2	MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Reset Source: mod_g_rst_n

Table 2-666. R5SS0_CORE0_AXI_S_BUS_SAFETY_FI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	Reset Source: mod_g_rst_n
0	MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	Reset Source: mod_g_rst_n

2.3.275 CFG0_R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR Registers

2.3.275.1 CFG0_CORE0_AXI_S_BUS_SAFETY_ERR Register (Offset = 18328h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-667. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8328h

Figure 2-332. R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_ERR_DED								MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_ERR_SEC							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_ERR_COMP_CHECK								MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_ERR_COMP_ERR							
R								R							
0h								0h							

Access Types Legend

Table 2-668. R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_ERR_DED	R	0h	Reset Source: mod_g_rst_n
23:16	MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_ERR_SEC	R	0h	Reset Source: mod_g_rst_n
15:8	MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_ERR_COMP_CHECK	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_ERR_COMP_ERR	R	0h	Reset Source: mod_g_rst_n

2.3.276 CFG0_R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_DATA0 Registers

2.3.276.1 CFG0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 1832Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-669. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 832Ch

Figure 2-333. R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_DATA0_D1								MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_DATA0_D0							
R								R							
0h								0h							

Access Types Legend

Table 2-670. R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Reset Source: mod_g_rst_n

2.3.277 CFG0_R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_CMD Registers

2.3.277.1 CFG0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 18330h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-671. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8330h

Figure 2-334. R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															

Access Types Legend

Table 2-672. R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.278 CFG0_R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITE Registers

2.3.278.1 CFG0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITE Register (Offset = 18334h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-673. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8334h

Figure 2-335. R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															

Access Types Legend

Table 2-674. R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITE_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.279 CFG0_R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_READ Registers

2.3.279.1 CFG0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_READ Register (Offset = 18338h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-675. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8338h

Figure 2-336. R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_READ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															

Access Types Legend

Table 2-676. R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_READ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_READ_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.280 CFG0_R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP Registers

2.3.280.1 CFG0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP Register (Offset = 1833Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-677. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 833Ch

Figure 2-337. R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															

Access Types Legend

Table 2-678. R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.281 CFG0_R5SS0_CORE1_AXI_S_BUS_SAFETY_CTRL Registers

2.3.281.1 CFG0_CORE1_AXI_S_BUS_SAFETY_CTRL Register (Offset = 18340h) [reset = 7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-679. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8340h

Figure 2-338. R5SS0_CORE1_AXI_S_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_CTRL_TYPE							
NONE								R							
b								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_CTRL_ERR_CLEAR	RESERVED					MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_CTRL_ENABLE		
NONE							R/W	NONE					R/W		
0							0h	0					7h		

Access Types Legend

Table 2-680. R5SS0_CORE1_AXI_S_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_CTRL_TYPE	R	0h	Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Reset Source: mod_g_rst_n

2.3.282 CFG0_R5SS0_CORE1_AXI_S_BUS_SAFETY_FI Registers

2.3.282.1 CFG0_CORE1_AXI_S_BUS_SAFETY_FI Register (Offset = 18344h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-681. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8344h

Figure 2-339. R5SS0_CORE1_AXI_S_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_FI_SAFE								MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_FI_MAIN							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_FI_DATA								RESERVED		MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_FI_DED	MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_FI_SEC	MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_FI_GLOBAL_SAFE	MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_FI_GLOBAL_MAIN
R/W								NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h								0		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-682. R5SS0_CORE1_AXI_S_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_FI_SAFE	R/W	0h	Reset Source: mod_g_rst_n
23:16	MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_FI_MAIN	R/W	0h	Reset Source: mod_g_rst_n
15:8	MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_FI_DATA	R/W	0h	Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_FI_DED	R/W	0h	Reset Source: mod_g_rst_n
4	MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_FI_SEC	R/W	0h	Reset Source: mod_g_rst_n
3	MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Reset Source: mod_g_rst_n
2	MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Reset Source: mod_g_rst_n

Table 2-682. R5SS0_CORE1_AXI_S_BUS_SAFETY_FI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	Reset Source: mod_g_rst_n
0	MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	Reset Source: mod_g_rst_n

2.3.283 CFG0_R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR Registers

2.3.283.1 CFG0_CORE1_AXI_S_BUS_SAFETY_ERR Register (Offset = 18348h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-683. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8348h

Figure 2-340. R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_ERR_DED								MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_ERR_SEC							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_ERR_COMP_CHECK								MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_ERR_COMP_ERR							
R								R							
0h								0h							

Access Types Legend

Table 2-684. R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_ERR_DED	R	0h	Reset Source: mod_g_rst_n
23:16	MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_ERR_SEC	R	0h	Reset Source: mod_g_rst_n
15:8	MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_ERR_COMP_CHECK	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_ERR_COMP_ERR	R	0h	Reset Source: mod_g_rst_n

2.3.284 CFG0_R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_DATA0 Registers

2.3.284.1 CFG0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 1834Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-685. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 834Ch

Figure 2-341. R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_DATA0_D1								MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_DATA0_D0							
R								R							
0h								0h							

Access Types Legend

Table 2-686. R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Reset Source: mod_g_rst_n

2.3.285 CFG0_R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_CMD Registers

2.3.285.1 CFG0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 18350h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-687. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8350h

Figure 2-342. R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															

Access Types Legend

Table 2-688. R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.286 CFG0_R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_WRITE Registers

2.3.286.1 CFG0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_WRITE Register (Offset = 18354h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-689. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8354h

Figure 2-343. R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_WRITE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															

Access Types Legend

Table 2-690. R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_WRITE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITE_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.287 CFG0_R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_READ Registers

2.3.287.1 CFG0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_READ Register (Offset = 18358h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-691. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8358h

Figure 2-344. R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_READ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															

Access Types Legend

Table 2-692. R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_READ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_READ_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.288 CFG0_R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP Registers

2.3.288.1 CFG0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP Register (Offset = 1835Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-693. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 835Ch

Figure 2-345. R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															

Access Types Legend

Table 2-694. R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.289 CFG0_R5SS1_CORE0_AXI_S_BUS_SAFETY_CTRL Registers

2.3.289.1 CFG0_CORE0_AXI_S_BUS_SAFETY_CTRL Register (Offset = 18360h) [reset = 7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-695. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8360h

Figure 2-346. R5SS1_CORE0_AXI_S_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MSS_R5FSS01_AXI_S_BUS_SAFETY_CTRL_TYPE							
NONE								R							
b								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							MSS_R5FSS01_AXI_S_BUS_SAFETY_CTRL_ERR_CLEAR	RESERVED					MSS_R5FSS01_AXI_S_BUS_SAFETY_CTRL_ENABLE		
NONE							R/W	NONE					R/W		
0							0h	0					7h		

Access Types Legend

Table 2-696. R5SS1_CORE0_AXI_S_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	MSS_R5FSS01_AXI_S_BUS_SAFETY_CTRL_TYPE	R	0h	Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	MSS_R5FSS01_AXI_S_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	MSS_R5FSS01_AXI_S_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Reset Source: mod_g_rst_n

2.3.290 CFG0_R5SS1_CORE0_AXI_S_BUS_SAFETY_FI Registers

2.3.290.1 CFG0_CORE0_AXI_S_BUS_SAFETY_FI Register (Offset = 18364h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-697. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8364h

Figure 2-347. R5SS1_CORE0_AXI_S_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS01_AXI_S_BUS_SAFETY_FI_SAFE								MSS_R5FSS01_AXI_S_BUS_SAFETY_FI_MAIN							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS01_AXI_S_BUS_SAFETY_FI_DATA								RESERVED		MSS_R5FSS01_AXI_S_BUS_SAFETY_FI_DED	MSS_R5FSS01_AXI_S_BUS_SAFETY_FI_SEC	MSS_R5FSS01_AXI_S_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	MSS_R5FSS01_AXI_S_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	MSS_R5FSS01_AXI_S_BUS_SAFETY_FI_GLOBAL_SAFE	MSS_R5FSS01_AXI_S_BUS_SAFETY_FI_GLOBAL_MAIN
R/W								NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h								0		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-698. R5SS1_CORE0_AXI_S_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_R5FSS01_AXI_S_BUS_SAFETY_FI_SAFE	R/W	0h	Reset Source: mod_g_rst_n
23:16	MSS_R5FSS01_AXI_S_BUS_SAFETY_FI_MAIN	R/W	0h	Reset Source: mod_g_rst_n
15:8	MSS_R5FSS01_AXI_S_BUS_SAFETY_FI_DATA	R/W	0h	Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	MSS_R5FSS01_AXI_S_BUS_SAFETY_FI_DED	R/W	0h	Reset Source: mod_g_rst_n
4	MSS_R5FSS01_AXI_S_BUS_SAFETY_FI_SEC	R/W	0h	Reset Source: mod_g_rst_n
3	MSS_R5FSS01_AXI_S_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Reset Source: mod_g_rst_n
2	MSS_R5FSS01_AXI_S_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Reset Source: mod_g_rst_n
1	MSS_R5FSS01_AXI_S_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	Reset Source: mod_g_rst_n

Table 2-698. R5SS1_CORE0_AXI_S_BUS_SAFETY_FI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MSS_R5FSS01_AXI_S_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	Reset Source: mod_g_rst_n

2.3.291 CFG0_R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR Registers

2.3.291.1 CFG0_CORE0_AXI_S_BUS_SAFETY_ERR Register (Offset = 18368h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-699. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8368h

Figure 2-348. R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS01_AXI_S_BUS_SAFETY_ERR_DED								MSS_R5FSS01_AXI_S_BUS_SAFETY_ERR_SEC							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS01_AXI_S_BUS_SAFETY_ERR_COMP_CHECK								MSS_R5FSS01_AXI_S_BUS_SAFETY_ERR_COMP_ERR							
R								R							
0h								0h							

Access Types Legend

Table 2-700. R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_R5FSS01_AXI_S_BUS_SAFETY_ERR_DED	R	0h	Reset Source: mod_g_rst_n
23:16	MSS_R5FSS01_AXI_S_BUS_SAFETY_ERR_SEC	R	0h	Reset Source: mod_g_rst_n
15:8	MSS_R5FSS01_AXI_S_BUS_SAFETY_ERR_COMP_CHECK	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_R5FSS01_AXI_S_BUS_SAFETY_ERR_COMP_ERR	R	0h	Reset Source: mod_g_rst_n

2.3.292 CFG0_R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_DATA0 Registers

2.3.292.1 CFG0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 1836Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-701. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 836Ch

Figure 2-349. R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS01_AXI_S_BUS_SAFETY_ERR_STAT_DATA0_D1								MSS_R5FSS01_AXI_S_BUS_SAFETY_ERR_STAT_DATA0_D0							
R								R							
0h								0h							

Access Types Legend

Table 2-702. R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_R5FSS01_AXI_S_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_R5FSS01_AXI_S_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Reset Source: mod_g_rst_n

2.3.293 CFG0_R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_CMD Registers

2.3.293.1 CFG0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 18370h) [reset = 0h]

Short Description:

Long Description:

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Table 2-703. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8370h

Figure 2-350. R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS01_AXI_S_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS01_AXI_S_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															

Access Types Legend

Table 2-704. R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS01_AXI_S_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.294 CFG0_R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITE Registers

2.3.294.1 CFG0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITE Register (Offset = 18374h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-705. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8374h

Figure 2-351. R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS01_AXI_S_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS01_AXI_S_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															

Access Types Legend

Table 2-706. R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS01_AXI_S_BUS_SAFETY_ERR_STAT_WRITE_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.295 CFG0_R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_READ Registers

2.3.295.1 CFG0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_READ Register (Offset = 18378h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-707. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8378h

Figure 2-352. R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_READ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS01_AXI_S_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS01_AXI_S_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															

Access Types Legend

Table 2-708. R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_READ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS01_AXI_S_BUS_SAFETY_ERR_STAT_READ_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.296 CFG0_R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP Registers

2.3.296.1 CFG0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP Register (Offset = 1837Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-709. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 837Ch

Figure 2-353. R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS01_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS01_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															

Access Types Legend

Table 2-710. R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS01_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.297 CFG0_R5SS1_CORE1_AXI_S_BUS_SAFETY_CTRL Registers

2.3.297.1 CFG0_CORE1_AXI_S_BUS_SAFETY_CTRL Register (Offset = 18380h) [reset = 7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-711. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8380h

Figure 2-354. R5SS1_CORE1_AXI_S_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MSS_R5FSS11_AXI_S_BUS_SAFETY_CTRL_TYPE							
NONE								R							
b								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							MSS_R5FSS11_AXI_S_BUS_SAFETY_CTRL_ERR_CLEAR	RESERVED					MSS_R5FSS11_AXI_S_BUS_SAFETY_CTRL_ENABLE		
NONE							R/W	NONE					R/W		
0							0h	0					7h		

Access Types Legend

Table 2-712. R5SS1_CORE1_AXI_S_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	MSS_R5FSS11_AXI_S_BUS_SAFETY_CTRL_TYPE	R	0h	Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	MSS_R5FSS11_AXI_S_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	MSS_R5FSS11_AXI_S_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Reset Source: mod_g_rst_n

2.3.298 CFG0_R5SS1_CORE1_AXI_S_BUS_SAFETY_FI Registers

2.3.298.1 CFG0_CORE1_AXI_S_BUS_SAFETY_FI Register (Offset = 18384h) [reset = 0h]

Short Description:

Long Description:

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Table 2-713. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8384h

Figure 2-355. R5SS1_CORE1_AXI_S_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS11_AXI_S_BUS_SAFETY_FI_SAFE								MSS_R5FSS11_AXI_S_BUS_SAFETY_FI_MAIN							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS11_AXI_S_BUS_SAFETY_FI_DATA								RESERVED		MSS_R5FSS11_AXI_S_BUS_SAFETY_FI_DED	MSS_R5FSS11_AXI_S_BUS_SAFETY_FI_SEC	MSS_R5FSS11_AXI_S_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	MSS_R5FSS11_AXI_S_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	MSS_R5FSS11_AXI_S_BUS_SAFETY_FI_GLOBAL_SAFE	MSS_R5FSS11_AXI_S_BUS_SAFETY_FI_GLOBAL_MAIN
R/W								NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h								0		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-714. R5SS1_CORE1_AXI_S_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_R5FSS11_AXI_S_BUS_SAFETY_FI_SAFE	R/W	0h	Reset Source: mod_g_rst_n
23:16	MSS_R5FSS11_AXI_S_BUS_SAFETY_FI_MAIN	R/W	0h	Reset Source: mod_g_rst_n
15:8	MSS_R5FSS11_AXI_S_BUS_SAFETY_FI_DATA	R/W	0h	Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	MSS_R5FSS11_AXI_S_BUS_SAFETY_FI_DED	R/W	0h	Reset Source: mod_g_rst_n
4	MSS_R5FSS11_AXI_S_BUS_SAFETY_FI_SEC	R/W	0h	Reset Source: mod_g_rst_n
3	MSS_R5FSS11_AXI_S_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Reset Source: mod_g_rst_n
2	MSS_R5FSS11_AXI_S_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Reset Source: mod_g_rst_n
1	MSS_R5FSS11_AXI_S_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	Reset Source: mod_g_rst_n

Table 2-714. R5SS1_CORE1_AXI_S_BUS_SAFETY_FI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MSS_R5FSS11_AXI_S_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	Reset Source: mod_g_rst_n

2.3.299 CFG0_R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR Registers

2.3.299.1 CFG0_CORE1_AXI_S_BUS_SAFETY_ERR Register (Offset = 18388h) [reset = 0h]

Short Description:

Long Description:

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Table 2-715. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8388h

Figure 2-356. R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS11_AXI_S_BUS_SAFETY_ERR_DED								MSS_R5FSS11_AXI_S_BUS_SAFETY_ERR_SEC							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS11_AXI_S_BUS_SAFETY_ERR_COMP_CHECK								MSS_R5FSS11_AXI_S_BUS_SAFETY_ERR_COMP_ERR							
R								R							
0h								0h							

Access Types Legend

Table 2-716. R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_R5FSS11_AXI_S_BUS_SAFETY_ERR_DED	R	0h	Reset Source: mod_g_rst_n
23:16	MSS_R5FSS11_AXI_S_BUS_SAFETY_ERR_SEC	R	0h	Reset Source: mod_g_rst_n
15:8	MSS_R5FSS11_AXI_S_BUS_SAFETY_ERR_COMP_CHECK	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_R5FSS11_AXI_S_BUS_SAFETY_ERR_COMP_ERR	R	0h	Reset Source: mod_g_rst_n

2.3.300 CFG0_R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_DATA0 Registers

2.3.300.1 CFG0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 1838Ch) [reset = 0h]

Short Description:

Long Description:

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Table 2-717. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 838Ch

Figure 2-357. R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS11_AXI_S_BUS_SAFETY_ERR_STAT_DATA0_D1								MSS_R5FSS11_AXI_S_BUS_SAFETY_ERR_STAT_DATA0_D0							
R								R							
0h								0h							

Access Types Legend

Table 2-718. R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_R5FSS11_AXI_S_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_R5FSS11_AXI_S_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Reset Source: mod_g_rst_n

2.3.301 CFG0_R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_CMD Registers

2.3.301.1 CFG0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 18390h) [reset = 0h]

Short Description:

Long Description:

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Table 2-719. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8390h

Figure 2-358. R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS11_AXI_S_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS11_AXI_S_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															

Access Types Legend

Table 2-720. R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS11_AXI_S_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.302 CFG0_R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_WRITE Registers

2.3.302.1 CFG0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_WRITE Register (Offset = 18394h) [reset = 0h]

Short Description:

Long Description:

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Table 2-721. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8394h

Figure 2-359. R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_WRITE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS11_AXI_S_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS11_AXI_S_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															

Access Types Legend

Table 2-722. R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_WRITE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS11_AXI_S_BUS_SAFETY_ERR_STAT_WRITE_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.303 CFG0_R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_READ Registers

2.3.303.1 CFG0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_READ Register (Offset = 18398h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-723. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8398h

Figure 2-360. R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_READ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS11_AXI_S_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS11_AXI_S_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															

Access Types Legend

Table 2-724. R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_READ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS11_AXI_S_BUS_SAFETY_ERR_STAT_READ_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.304 CFG0_R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP Registers

2.3.304.1 CFG0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP Register (Offset = 1839Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-725. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 839Ch

Figure 2-361. R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS11_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS11_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															

Access Types Legend

Table 2-726. R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS11_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.305 CFG0_TPTC00_RD_BUS_SAFETY_CTRL Registers

2.3.305.1 CFG0_RD_BUS_SAFETY_CTRL Register (Offset = 183A0h) [reset = 7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-727. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 83A0h

Figure 2-362. TPTC00_RD_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MSS_TPTC_A0_RD_BUS_SAFETY_CTRL_TYPE							
NONE								R							
b								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							MSS_TPTC_A0_RD_BUS_SAFETY_CTRL_ERR_CLEAR	RESERVED					MSS_TPTC_A0_RD_BUS_SAFETY_CTRL_ENABLE		
NONE							R/W	NONE					R/W		
0							0h	0					7h		

Access Types Legend

Table 2-728. TPTC00_RD_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	MSS_TPTC_A0_RD_BUS_SAFETY_CTRL_TYPE	R	0h	Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	MSS_TPTC_A0_RD_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	MSS_TPTC_A0_RD_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Reset Source: mod_g_rst_n

2.3.306 CFG0_TPTC00_RD_BUS_SAFETY_FI Registers

2.3.306.1 CFG0_RD_BUS_SAFETY_FI Register (Offset = 183A4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-729. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 83A4h

Figure 2-363. TPTC00_RD_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_TPTC_A0_RD_BUS_SAFETY_FI_SAFE								MSS_TPTC_A0_RD_BUS_SAFETY_FI_MAIN							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_TPTC_A0_RD_BUS_SAFETY_FI_DATA								RESERVED		MSS_TPTC_A0_RD_BUS_SAFETY_FI_DED	MSS_TPTC_A0_RD_BUS_SAFETY_FI_SEC	MSS_TPTC_A0_RD_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	MSS_TPTC_A0_RD_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	MSS_TPTC_A0_RD_BUS_SAFETY_FI_GLOBAL_SAFE	MSS_TPTC_A0_RD_BUS_SAFETY_FI_GLOBAL_MAIN
R/W								NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h								0		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-730. TPTC00_RD_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_TPTC_A0_RD_BUS_SAFETY_FI_SAFE	R/W	0h	Reset Source: mod_g_rst_n
23:16	MSS_TPTC_A0_RD_BUS_SAFETY_FI_MAIN	R/W	0h	Reset Source: mod_g_rst_n
15:8	MSS_TPTC_A0_RD_BUS_SAFETY_FI_DATA	R/W	0h	Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	MSS_TPTC_A0_RD_BUS_SAFETY_FI_DED	R/W	0h	Reset Source: mod_g_rst_n
4	MSS_TPTC_A0_RD_BUS_SAFETY_FI_SEC	R/W	0h	Reset Source: mod_g_rst_n
3	MSS_TPTC_A0_RD_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Reset Source: mod_g_rst_n
2	MSS_TPTC_A0_RD_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Reset Source: mod_g_rst_n
1	MSS_TPTC_A0_RD_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	Reset Source: mod_g_rst_n

Table 2-730. TPTC00_RD_BUS_SAFETY_FI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MSS_TPTC_A0_RD_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	Reset Source: mod_g_rst_n

2.3.307 CFG0_TPTC00_RD_BUS_SAFETY_ERR Registers

2.3.307.1 CFG0_RD_BUS_SAFETY_ERR Register (Offset = 183A8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-731. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 83A8h

Figure 2-364. TPTC00_RD_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_TPTC_A0_RD_BUS_SAFETY_ERR_DED								MSS_TPTC_A0_RD_BUS_SAFETY_ERR_SEC							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_TPTC_A0_RD_BUS_SAFETY_ERR_COMP_CHECK								MSS_TPTC_A0_RD_BUS_SAFETY_ERR_COMP_ERR							
R								R							
0h								0h							

Access Types Legend

Table 2-732. TPTC00_RD_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_TPTC_A0_RD_BUS_SAFETY_ERR_DED	R	0h	Reset Source: mod_g_rst_n
23:16	MSS_TPTC_A0_RD_BUS_SAFETY_ERR_SEC	R	0h	Reset Source: mod_g_rst_n
15:8	MSS_TPTC_A0_RD_BUS_SAFETY_ERR_COMP_CHECK	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_TPTC_A0_RD_BUS_SAFETY_ERR_COMP_ERR	R	0h	Reset Source: mod_g_rst_n

2.3.308 CFG0_TPTC00_RD_BUS_SAFETY_ERR_STAT_DATA0 Registers

2.3.308.1 CFG0_RD_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 183ACh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-733. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 83ACh

Figure 2-365. TPTC00_RD_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_DATA0_D1								MSS_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_DATA0_D0							
R								R							
0h								0h							

Access Types Legend

Table 2-734. TPTC00_RD_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Reset Source: mod_g_rst_n

2.3.309 CFG0_TPTC00_RD_BUS_SAFETY_ERR_STAT_CMD Registers

2.3.309.1 CFG0_RD_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 183B0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-735. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 83B0h

Figure 2-366. TPTC00_RD_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															

Access Types Legend

Table 2-736. TPTC00_RD_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.310 CFG0_TPTC00_RD_BUS_SAFETY_ERR_STAT_READ Registers

2.3.310.1 CFG0_RD_BUS_SAFETY_ERR_STAT_READ Register (Offset = 183B4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-737. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 83B4h

Figure 2-367. TPTC00_RD_BUS_SAFETY_ERR_STAT_READ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															

Access Types Legend

Table 2-738. TPTC00_RD_BUS_SAFETY_ERR_STAT_READ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_READ_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.311 CFG0_TPTC01_RD_BUS_SAFETY_CTRL Registers

2.3.311.1 CFG0_RD_BUS_SAFETY_CTRL Register (Offset = 183C0h) [reset = 7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-739. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 83C0h

Figure 2-368. TPTC01_RD_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MSS_TPTC_A1_RD_BUS_SAFETY_CTRL_TYPE							
NONE								R							
b								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							MSS_TPTC_A1_RD_BUS_SAFETY_CTRL_ERR_CLEAR	RESERVED					MSS_TPTC_A1_RD_BUS_SAFETY_CTRL_ENABLE		
NONE							R/W	NONE					R/W		
0							0h	0					7h		

Access Types Legend

Table 2-740. TPTC01_RD_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	MSS_TPTC_A1_RD_BUS_SAFETY_CTRL_TYPE	R	0h	Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	MSS_TPTC_A1_RD_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	MSS_TPTC_A1_RD_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Reset Source: mod_g_rst_n

2.3.312 CFG0_TPTC01_RD_BUS_SAFETY_FI Registers

2.3.312.1 CFG0_RD_BUS_SAFETY_FI Register (Offset = 183C4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-741. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 83C4h

Figure 2-369. TPTC01_RD_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_TPTC_A1_RD_BUS_SAFETY_FI_SAFE								MSS_TPTC_A1_RD_BUS_SAFETY_FI_MAIN							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_TPTC_A1_RD_BUS_SAFETY_FI_DATA								RESERVED		MSS_TPTC_A1_RD_BUS_SAFETY_FI_DED	MSS_TPTC_A1_RD_BUS_SAFETY_FI_SEC	MSS_TPTC_A1_RD_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	MSS_TPTC_A1_RD_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	MSS_TPTC_A1_RD_BUS_SAFETY_FI_GLOBAL_SAFE	MSS_TPTC_A1_RD_BUS_SAFETY_FI_GLOBAL_MAIN
R/W								NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h								0		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-742. TPTC01_RD_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_TPTC_A1_RD_BUS_SAFETY_FI_SAFE	R/W	0h	Reset Source: mod_g_rst_n
23:16	MSS_TPTC_A1_RD_BUS_SAFETY_FI_MAIN	R/W	0h	Reset Source: mod_g_rst_n
15:8	MSS_TPTC_A1_RD_BUS_SAFETY_FI_DATA	R/W	0h	Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	MSS_TPTC_A1_RD_BUS_SAFETY_FI_DED	R/W	0h	Reset Source: mod_g_rst_n
4	MSS_TPTC_A1_RD_BUS_SAFETY_FI_SEC	R/W	0h	Reset Source: mod_g_rst_n
3	MSS_TPTC_A1_RD_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Reset Source: mod_g_rst_n
2	MSS_TPTC_A1_RD_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Reset Source: mod_g_rst_n
1	MSS_TPTC_A1_RD_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	Reset Source: mod_g_rst_n

Table 2-742. TPTC01_RD_BUS_SAFETY_FI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MSS_TPTC_A1_RD_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	Reset Source: mod_g_rst_n

2.3.313 CFG0_TPTC01_RD_BUS_SAFETY_ERR Registers

2.3.313.1 CFG0_RD_BUS_SAFETY_ERR Register (Offset = 183C8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-743. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 83C8h

Figure 2-370. TPTC01_RD_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_TPTC_A1_RD_BUS_SAFETY_ERR_DED								MSS_TPTC_A1_RD_BUS_SAFETY_ERR_SEC							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_TPTC_A1_RD_BUS_SAFETY_ERR_COMP_CHECK								MSS_TPTC_A1_RD_BUS_SAFETY_ERR_COMP_ERR							
R								R							
0h								0h							

Access Types Legend

Table 2-744. TPTC01_RD_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_TPTC_A1_RD_BUS_SAFETY_ERR_DED	R	0h	Reset Source: mod_g_rst_n
23:16	MSS_TPTC_A1_RD_BUS_SAFETY_ERR_SEC	R	0h	Reset Source: mod_g_rst_n
15:8	MSS_TPTC_A1_RD_BUS_SAFETY_ERR_COMP_CHECK	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_TPTC_A1_RD_BUS_SAFETY_ERR_COMP_ERR	R	0h	Reset Source: mod_g_rst_n

2.3.314 CFG0_TPTC01_RD_BUS_SAFETY_ERR_STAT_DATA0 Registers

2.3.314.1 CFG0_RD_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 183CCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-745. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 83CCh

Figure 2-371. TPTC01_RD_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_DATA0_D1								MSS_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_DATA0_D0							
R								R							
0h								0h							

Access Types Legend

Table 2-746. TPTC01_RD_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Reset Source: mod_g_rst_n

2.3.315 CFG0_TPTC01_RD_BUS_SAFETY_ERR_STAT_CMD Registers

2.3.315.1 CFG0_RD_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 183D0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-747. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 83D0h

Figure 2-372. TPTC01_RD_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															

Access Types Legend

Table 2-748. TPTC01_RD_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.316 CFG0_TPTC01_RD_BUS_SAFETY_ERR_STAT_READ Registers

2.3.316.1 CFG0_RD_BUS_SAFETY_ERR_STAT_READ Register (Offset = 183D4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-749. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 83D4h

Figure 2-373. TPTC01_RD_BUS_SAFETY_ERR_STAT_READ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															

Access Types Legend

Table 2-750. TPTC01_RD_BUS_SAFETY_ERR_STAT_READ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_READ_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.317 CFG0_TPTC00_WR_BUS_SAFETY_CTRL Registers

2.3.317.1 CFG0_WR_BUS_SAFETY_CTRL Register (Offset = 183E0h) [reset = 7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-751. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 83E0h

Figure 2-374. TPTC00_WR_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MSS_TPTC_A0_WR_BUS_SAFETY_CTRL_TYPE							
NONE								R							
b								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							MSS_TPTC_A0_WR_BUS_SAFETY_CTRL_ERR_CLEAR	RESERVED					MSS_TPTC_A0_WR_BUS_SAFETY_CTRL_ENABLE		
NONE							R/W	NONE					R/W		
0							0h	0					7h		

Access Types Legend

Table 2-752. TPTC00_WR_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	MSS_TPTC_A0_WR_BUS_SAFETY_CTRL_TYPE	R	0h	Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	MSS_TPTC_A0_WR_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	MSS_TPTC_A0_WR_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Reset Source: mod_g_rst_n

2.3.318 CFG0_TPTC00_WR_BUS_SAFETY_FI Registers

2.3.318.1 CFG0_WR_BUS_SAFETY_FI Register (Offset = 183E4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-753. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 83E4h

Figure 2-375. TPTC00_WR_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_TPTC_A0_WR_BUS_SAFETY_FI_SAFE								MSS_TPTC_A0_WR_BUS_SAFETY_FI_MAIN							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_TPTC_A0_WR_BUS_SAFETY_FI_DATA								RESERVED		MSS_TPTC_A0_WR_BUS_SAFETY_FI_DED	MSS_TPTC_A0_WR_BUS_SAFETY_FI_SEC	MSS_TPTC_A0_WR_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	MSS_TPTC_A0_WR_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	MSS_TPTC_A0_WR_BUS_SAFETY_FI_GLOBAL_SAFE	MSS_TPTC_A0_WR_BUS_SAFETY_FI_GLOBAL_MAIN
R/W								NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h								0		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-754. TPTC00_WR_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_TPTC_A0_WR_BUS_SAFETY_FI_SAFE	R/W	0h	Reset Source: mod_g_rst_n
23:16	MSS_TPTC_A0_WR_BUS_SAFETY_FI_MAIN	R/W	0h	Reset Source: mod_g_rst_n
15:8	MSS_TPTC_A0_WR_BUS_SAFETY_FI_DATA	R/W	0h	Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	MSS_TPTC_A0_WR_BUS_SAFETY_FI_DED	R/W	0h	Reset Source: mod_g_rst_n
4	MSS_TPTC_A0_WR_BUS_SAFETY_FI_SEC	R/W	0h	Reset Source: mod_g_rst_n
3	MSS_TPTC_A0_WR_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Reset Source: mod_g_rst_n
2	MSS_TPTC_A0_WR_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Reset Source: mod_g_rst_n
1	MSS_TPTC_A0_WR_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	Reset Source: mod_g_rst_n

Table 2-754. TPTC00_WR_BUS_SAFETY_FI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MSS_TPTC_A0_WR_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	Reset Source: mod_g_rst_n

2.3.319 CFG0_TPTC00_WR_BUS_SAFETY_ERR Registers

2.3.319.1 CFG0_WR_BUS_SAFETY_ERR Register (Offset = 183E8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-755. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 83E8h

Figure 2-376. TPTC00_WR_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_TPTC_A0_WR_BUS_SAFETY_ERR_DED								MSS_TPTC_A0_WR_BUS_SAFETY_ERR_SEC							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_TPTC_A0_WR_BUS_SAFETY_ERR_COMP_CHECK								MSS_TPTC_A0_WR_BUS_SAFETY_ERR_COMP_ERR							
R								R							
0h								0h							

Access Types Legend

Table 2-756. TPTC00_WR_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_TPTC_A0_WR_BUS_SAFETY_ERR_DED	R	0h	Reset Source: mod_g_rst_n
23:16	MSS_TPTC_A0_WR_BUS_SAFETY_ERR_SEC	R	0h	Reset Source: mod_g_rst_n
15:8	MSS_TPTC_A0_WR_BUS_SAFETY_ERR_COMP_CHECK	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_TPTC_A0_WR_BUS_SAFETY_ERR_COMP_ERR	R	0h	Reset Source: mod_g_rst_n

2.3.320 CFG0_TPTC00_WR_BUS_SAFETY_ERR_STAT_DATA0 Registers

2.3.320.1 CFG0_WR_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 183ECh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-757. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 83ECh

Figure 2-377. TPTC00_WR_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_DATA0_D1								MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_DATA0_D0							
R								R							
0h								0h							

Access Types Legend

Table 2-758. TPTC00_WR_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Reset Source: mod_g_rst_n

2.3.321 CFG0_TPTC00_WR_BUS_SAFETY_ERR_STAT_CMD Registers

2.3.321.1 CFG0_WR_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 183F0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-759. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 83F0h

Figure 2-378. TPTC00_WR_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															

Access Types Legend

Table 2-760. TPTC00_WR_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.322 CFG0_TPTC00_WR_BUS_SAFETY_ERR_STAT_WRITE Registers

2.3.322.1 CFG0_WR_BUS_SAFETY_ERR_STAT_WRITE Register (Offset = 183F4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-761. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 83F4h

Figure 2-379. TPTC00_WR_BUS_SAFETY_ERR_STAT_WRITE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															

Access Types Legend

Table 2-762. TPTC00_WR_BUS_SAFETY_ERR_STAT_WRITE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.323 CFG0_TPTC00_WR_BUS_SAFETY_ERR_STAT_WRITERESP Registers

2.3.323.1 CFG0_WR_BUS_SAFETY_ERR_STAT_WRITERESP Register (Offset = 183F8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-763. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 83F8h

Figure 2-380. TPTC00_WR_BUS_SAFETY_ERR_STAT_WRITERESP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															

Access Types Legend

Table 2-764. TPTC00_WR_BUS_SAFETY_ERR_STAT_WRITERESP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.324 CFG0_TPTC01_WR_BUS_SAFETY_CTRL Registers

2.3.324.1 CFG0_WR_BUS_SAFETY_CTRL Register (Offset = 18400h) [reset = 7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-765. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8400h

Figure 2-381. TPTC01_WR_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MSS_TPTC_A1_WR_BUS_SAFETY_CTRL_TYPE							
NONE								R							
b								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							MSS_TPTC_A1_WR_BUS_SAFETY_CTRL_ERR_CLEAR	RESERVED					MSS_TPTC_A1_WR_BUS_SAFETY_CTRL_ENABLE		
NONE							R/W	NONE					R/W		
0							0h	0					7h		

Access Types Legend

Table 2-766. TPTC01_WR_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	MSS_TPTC_A1_WR_BUS_SAFETY_CTRL_TYPE	R	0h	Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	MSS_TPTC_A1_WR_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	MSS_TPTC_A1_WR_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Reset Source: mod_g_rst_n

2.3.325 CFG0_TPTC01_WR_BUS_SAFETY_FI Registers

2.3.325.1 CFG0_WR_BUS_SAFETY_FI Register (Offset = 18404h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-767. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8404h

Figure 2-382. TPTC01_WR_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_TPTC_A1_WR_BUS_SAFETY_FI_SAFE								MSS_TPTC_A1_WR_BUS_SAFETY_FI_MAIN							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_TPTC_A1_WR_BUS_SAFETY_FI_DATA								RESERVED		MSS_TPTC_A1_WR_BUS_SAFETY_FI_DED	MSS_TPTC_A1_WR_BUS_SAFETY_FI_SEC	MSS_TPTC_A1_WR_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	MSS_TPTC_A1_WR_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	MSS_TPTC_A1_WR_BUS_SAFETY_FI_GLOBAL_SAFE	MSS_TPTC_A1_WR_BUS_SAFETY_FI_GLOBAL_MAIN
R/W								NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h								0		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-768. TPTC01_WR_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_TPTC_A1_WR_BUS_SAFETY_FI_SAFE	R/W	0h	Reset Source: mod_g_rst_n
23:16	MSS_TPTC_A1_WR_BUS_SAFETY_FI_MAIN	R/W	0h	Reset Source: mod_g_rst_n
15:8	MSS_TPTC_A1_WR_BUS_SAFETY_FI_DATA	R/W	0h	Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	MSS_TPTC_A1_WR_BUS_SAFETY_FI_DED	R/W	0h	Reset Source: mod_g_rst_n
4	MSS_TPTC_A1_WR_BUS_SAFETY_FI_SEC	R/W	0h	Reset Source: mod_g_rst_n
3	MSS_TPTC_A1_WR_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Reset Source: mod_g_rst_n
2	MSS_TPTC_A1_WR_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Reset Source: mod_g_rst_n
1	MSS_TPTC_A1_WR_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	Reset Source: mod_g_rst_n

Table 2-768. TPTC01_WR_BUS_SAFETY_FI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MSS_TPTC_A1_WR_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	Reset Source: mod_g_rst_n

2.3.326 CFG0_TPTC01_WR_BUS_SAFETY_ERR Registers

2.3.326.1 CFG0_WR_BUS_SAFETY_ERR Register (Offset = 18408h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-769. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8408h

Figure 2-383. TPTC01_WR_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_TPTC_A1_WR_BUS_SAFETY_ERR_DED								MSS_TPTC_A1_WR_BUS_SAFETY_ERR_SEC							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_TPTC_A1_WR_BUS_SAFETY_ERR_COMP_CHECK								MSS_TPTC_A1_WR_BUS_SAFETY_ERR_COMP_ERR							
R								R							
0h								0h							

Access Types Legend

Table 2-770. TPTC01_WR_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_TPTC_A1_WR_BUS_SAFETY_ERR_DED	R	0h	Reset Source: mod_g_rst_n
23:16	MSS_TPTC_A1_WR_BUS_SAFETY_ERR_SEC	R	0h	Reset Source: mod_g_rst_n
15:8	MSS_TPTC_A1_WR_BUS_SAFETY_ERR_COMP_CHECK	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_TPTC_A1_WR_BUS_SAFETY_ERR_COMP_ERR	R	0h	Reset Source: mod_g_rst_n

2.3.327 CFG0_TPTC01_WR_BUS_SAFETY_ERR_STAT_DATA0 Registers

2.3.327.1 CFG0_WR_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 1840Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-771. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 840Ch

Figure 2-384. TPTC01_WR_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_DATA0_D1								MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_DATA0_D0							
R								R							
0h								0h							

Access Types Legend

Table 2-772. TPTC01_WR_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Reset Source: mod_g_rst_n

2.3.328 CFG0_TPTC01_WR_BUS_SAFETY_ERR_STAT_CMD Registers

2.3.328.1 CFG0_WR_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 18410h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-773. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8410h

Figure 2-385. TPTC01_WR_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															

Access Types Legend

Table 2-774. TPTC01_WR_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.329 CFG0_TPTC01_WR_BUS_SAFETY_ERR_STAT_WRITE Registers

2.3.329.1 CFG0_WR_BUS_SAFETY_ERR_STAT_WRITE Register (Offset = 18414h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-775. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8414h

Figure 2-386. TPTC01_WR_BUS_SAFETY_ERR_STAT_WRITE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															

Access Types Legend

Table 2-776. TPTC01_WR_BUS_SAFETY_ERR_STAT_WRITE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.330 CFG0_TPTC01_WR_BUS_SAFETY_ERR_STAT_WRITERESP Registers

2.3.330.1 CFG0_WR_BUS_SAFETY_ERR_STAT_WRITERESP Register (Offset = 18418h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-777. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8418h

Figure 2-387. TPTC01_WR_BUS_SAFETY_ERR_STAT_WRITERESP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															

Access Types Legend

Table 2-778. TPTC01_WR_BUS_SAFETY_ERR_STAT_WRITERESP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.331 CFG0_HSM_TPTC0_RD_BUS_SAFETY_CTRL Registers

2.3.331.1 CFG0_TPTC0_RD_BUS_SAFETY_CTRL Register (Offset = 18420h) [reset = 7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-779. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8420h

Figure 2-388. HSM_TPTC0_RD_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								HSM_TPTC_A0_RD_BUS_SAFETY_CTRL_TYPE							
NONE								R							
b								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							HSM_TPTC_A0_RD_BUS_SAFETY_CTRL_ERR_CLEAR	RESERVED					HSM_TPTC_A0_RD_BUS_SAFETY_CTRL_ENABLE		
NONE							R/W	NONE					R/W		
0							0h	0					7h		

Access Types Legend

Table 2-780. HSM_TPTC0_RD_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	HSM_TPTC_A0_RD_BUS_SAFETY_CTRL_TYPE	R	0h	Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	HSM_TPTC_A0_RD_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	HSM_TPTC_A0_RD_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Reset Source: mod_g_rst_n

2.3.332 CFG0_HSM_TPTC0_RD_BUS_SAFETY_FI Registers

2.3.332.1 CFG0_TPTC0_RD_BUS_SAFETY_FI Register (Offset = 18424h) [reset = 0h]

Short Description:

Long Description:

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Table 2-781. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8424h

Figure 2-389. HSM_TPTC0_RD_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSM_TPTC_A0_RD_BUS_SAFETY_FI_SAFE								HSM_TPTC_A0_RD_BUS_SAFETY_FI_MAIN							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSM_TPTC_A0_RD_BUS_SAFETY_FI_DATA								RESERVED		HSM_TPTC_A0_RD_BUS_SAFETY_FI_DED	HSM_TPTC_A0_RD_BUS_SAFETY_FI_SEC	HSM_TPTC_A0_RD_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	HSM_TPTC_A0_RD_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	HSM_TPTC_A0_RD_BUS_SAFETY_FI_GLOBAL_SAFE	HSM_TPTC_A0_RD_BUS_SAFETY_FI_GLOBAL_MAIN
R/W								NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h								0		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-782. HSM_TPTC0_RD_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	HSM_TPTC_A0_RD_BUS_SAFETY_FI_SAFE	R/W	0h	Reset Source: mod_g_rst_n
23:16	HSM_TPTC_A0_RD_BUS_SAFETY_FI_MAIN	R/W	0h	Reset Source: mod_g_rst_n
15:8	HSM_TPTC_A0_RD_BUS_SAFETY_FI_DATA	R/W	0h	Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	HSM_TPTC_A0_RD_BUS_SAFETY_FI_DED	R/W	0h	Reset Source: mod_g_rst_n
4	HSM_TPTC_A0_RD_BUS_SAFETY_FI_SEC	R/W	0h	Reset Source: mod_g_rst_n
3	HSM_TPTC_A0_RD_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Reset Source: mod_g_rst_n
2	HSM_TPTC_A0_RD_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Reset Source: mod_g_rst_n
1	HSM_TPTC_A0_RD_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	Reset Source: mod_g_rst_n

Table 2-782. HSM_TPTC0_RD_BUS_SAFETY_FI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HSM_TPTC_A0_RD_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	Reset Source: mod_g_rst_n

2.3.333 CFG0_HSM_TPTC0_RD_BUS_SAFETY_ERR Registers

2.3.333.1 CFG0_TPTC0_RD_BUS_SAFETY_ERR Register (Offset = 18428h) [reset = 0h]

Short Description:

Long Description:

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Table 2-783. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8428h

Figure 2-390. HSM_TPTC0_RD_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSM_TPTC_A0_RD_BUS_SAFETY_ERR_DED								HSM_TPTC_A0_RD_BUS_SAFETY_ERR_SEC							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSM_TPTC_A0_RD_BUS_SAFETY_ERR_COMP_CHECK								HSM_TPTC_A0_RD_BUS_SAFETY_ERR_COMP_ERR							
R								R							
0h								0h							

Access Types Legend

Table 2-784. HSM_TPTC0_RD_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	HSM_TPTC_A0_RD_BUS_SAFETY_ERR_DED	R	0h	Reset Source: mod_g_rst_n
23:16	HSM_TPTC_A0_RD_BUS_SAFETY_ERR_SEC	R	0h	Reset Source: mod_g_rst_n
15:8	HSM_TPTC_A0_RD_BUS_SAFETY_ERR_COMP_CHECK	R	0h	Reset Source: mod_g_rst_n
7:0	HSM_TPTC_A0_RD_BUS_SAFETY_ERR_COMP_ERR	R	0h	Reset Source: mod_g_rst_n

2.3.334 CFG0_HSM_TPTC0_RD_BUS_SAFETY_ERR_STAT_DATA0 Registers

2.3.334.1 CFG0_TPTC0_RD_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 1842Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-785. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 842Ch

Figure 2-391. HSM_TPTC0_RD_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSM_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_DATA0_D1								HSM_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_DATA0_D0							
R								R							
0h								0h							

Access Types Legend

Table 2-786. HSM_TPTC0_RD_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	HSM_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Reset Source: mod_g_rst_n
7:0	HSM_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Reset Source: mod_g_rst_n

2.3.335 CFG0_HSM_TPTC0_RD_BUS_SAFETY_ERR_STAT_CMD Registers

2.3.335.1 CFG0_TPTC0_RD_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 18430h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-787. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8430h

Figure 2-392. HSM_TPTC0_RD_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSM_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSM_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															

Access Types Legend

Table 2-788. HSM_TPTC0_RD_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HSM_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.336 CFG0_HSM_TPTC0_RD_BUS_SAFETY_ERR_STAT_READ Registers

2.3.336.1 CFG0_TPTC0_RD_BUS_SAFETY_ERR_STAT_READ Register (Offset = 18434h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-789. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8434h

Figure 2-393. HSM_TPTC0_RD_BUS_SAFETY_ERR_STAT_READ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSM_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSM_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															

Access Types Legend

Table 2-790. HSM_TPTC0_RD_BUS_SAFETY_ERR_STAT_READ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HSM_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_READ_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.337 CFG0_HSM_TPTC1_RD_BUS_SAFETY_CTRL Registers

2.3.337.1 CFG0_TPTC1_RD_BUS_SAFETY_CTRL Register (Offset = 18440h) [reset = 7h]

Short Description:

Long Description:

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Table 2-791. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8440h

Figure 2-394. HSM_TPTC1_RD_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								HSM_TPTC_A1_RD_BUS_SAFETY_CTRL_TYPE							
NONE								R							
b								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							HSM_TPTC_A1_RD_BUS_SAFETY_CTRL_ERR_CLEAR	RESERVED					HSM_TPTC_A1_RD_BUS_SAFETY_CTRL_ENABLE		
NONE							R/W	NONE					R/W		
0							0h	0					7h		

Access Types Legend

Table 2-792. HSM_TPTC1_RD_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	HSM_TPTC_A1_RD_BUS_SAFETY_CTRL_TYPE	R	0h	Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	HSM_TPTC_A1_RD_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	HSM_TPTC_A1_RD_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Reset Source: mod_g_rst_n

2.3.338 CFG0_HSM_TPTC1_RD_BUS_SAFETY_FI Registers

2.3.338.1 CFG0_TPTC1_RD_BUS_SAFETY_FI Register (Offset = 18444h) [reset = 0h]

Short Description:

Long Description:

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Table 2-793. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8444h

Figure 2-395. HSM_TPTC1_RD_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSM_TPTC_A1_RD_BUS_SAFETY_FI_SAFE								HSM_TPTC_A1_RD_BUS_SAFETY_FI_MAIN							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSM_TPTC_A1_RD_BUS_SAFETY_FI_DATA								RESERVED		HSM_TPTC_A1_RD_BUS_SAFETY_FI_DED	HSM_TPTC_A1_RD_BUS_SAFETY_FI_SEC	HSM_TPTC_A1_RD_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	HSM_TPTC_A1_RD_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	HSM_TPTC_A1_RD_BUS_SAFETY_FI_GLOBAL_SAFE	HSM_TPTC_A1_RD_BUS_SAFETY_FI_GLOBAL_MAIN
R/W								NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h								0		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-794. HSM_TPTC1_RD_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	HSM_TPTC_A1_RD_BUS_SAFETY_FI_SAFE	R/W	0h	Reset Source: mod_g_rst_n
23:16	HSM_TPTC_A1_RD_BUS_SAFETY_FI_MAIN	R/W	0h	Reset Source: mod_g_rst_n
15:8	HSM_TPTC_A1_RD_BUS_SAFETY_FI_DATA	R/W	0h	Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	HSM_TPTC_A1_RD_BUS_SAFETY_FI_DED	R/W	0h	Reset Source: mod_g_rst_n
4	HSM_TPTC_A1_RD_BUS_SAFETY_FI_SEC	R/W	0h	Reset Source: mod_g_rst_n
3	HSM_TPTC_A1_RD_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Reset Source: mod_g_rst_n
2	HSM_TPTC_A1_RD_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Reset Source: mod_g_rst_n
1	HSM_TPTC_A1_RD_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	Reset Source: mod_g_rst_n

Table 2-794. HSM_TPTC1_RD_BUS_SAFETY_FI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HSM_TPTC_A1_RD_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	Reset Source: mod_g_rst_n

2.3.339 CFG0_HSM_TPTC1_RD_BUS_SAFETY_ERR Registers

2.3.339.1 CFG0_TPTC1_RD_BUS_SAFETY_ERR Register (Offset = 18448h) [reset = 0h]

Short Description:

Long Description:

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Table 2-795. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8448h

Figure 2-396. HSM_TPTC1_RD_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSM_TPTC_A1_RD_BUS_SAFETY_ERR_DED								HSM_TPTC_A1_RD_BUS_SAFETY_ERR_SEC							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSM_TPTC_A1_RD_BUS_SAFETY_ERR_COMP_CHECK								HSM_TPTC_A1_RD_BUS_SAFETY_ERR_COMP_ERR							
R								R							
0h								0h							

Access Types Legend

Table 2-796. HSM_TPTC1_RD_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	HSM_TPTC_A1_RD_BUS_SAFETY_ERR_DED	R	0h	Reset Source: mod_g_rst_n
23:16	HSM_TPTC_A1_RD_BUS_SAFETY_ERR_SEC	R	0h	Reset Source: mod_g_rst_n
15:8	HSM_TPTC_A1_RD_BUS_SAFETY_ERR_COMP_CHECK	R	0h	Reset Source: mod_g_rst_n
7:0	HSM_TPTC_A1_RD_BUS_SAFETY_ERR_COMP_ERR	R	0h	Reset Source: mod_g_rst_n

2.3.340 CFG0_HSM_TPTC1_RD_BUS_SAFETY_ERR_STAT_DATA0 Registers

2.3.340.1 CFG0_TPTC1_RD_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 1844Ch) [reset = 0h]

Short Description:

Long Description:

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Table 2-797. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 844Ch

Figure 2-397. HSM_TPTC1_RD_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSM_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_DATA0_D1								HSM_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_DATA0_D0							
R								R							
0h								0h							

Access Types Legend

Table 2-798. HSM_TPTC1_RD_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	HSM_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Reset Source: mod_g_rst_n
7:0	HSM_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Reset Source: mod_g_rst_n

2.3.341 CFG0_HSM_TPTC1_RD_BUS_SAFETY_ERR_STAT_CMD Registers

2.3.341.1 CFG0_TPTC1_RD_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 18450h) [reset = 0h]

Short Description:

Long Description:

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Table 2-799. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8450h

Figure 2-398. HSM_TPTC1_RD_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSM_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSM_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															

Access Types Legend

Table 2-800. HSM_TPTC1_RD_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HSM_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.342 CFG0_HSM_TPTC1_RD_BUS_SAFETY_ERR_STAT_READ Registers

2.3.342.1 CFG0_TPTC1_RD_BUS_SAFETY_ERR_STAT_READ Register (Offset = 18454h) [reset = 0h]

Short Description:

Long Description:

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Table 2-801. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8454h

Figure 2-399. HSM_TPTC1_RD_BUS_SAFETY_ERR_STAT_READ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSM_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSM_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															

Access Types Legend

Table 2-802. HSM_TPTC1_RD_BUS_SAFETY_ERR_STAT_READ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HSM_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_READ_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.343 CFG0_HSM_TPTC0_WR_BUS_SAFETY_CTRL Registers

2.3.343.1 CFG0_TPTC0_WR_BUS_SAFETY_CTRL Register (Offset = 18460h) [reset = 7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-803. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8460h

Figure 2-400. HSM_TPTC0_WR_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								HSM_TPTC_A0_WR_BUS_SAFETY_CTRL_TYPE							
NONE								R							
b								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							HSM_TPTC_A0_WR_BUS_SAFETY_CTRL_ERR_CLEAR	RESERVED					HSM_TPTC_A0_WR_BUS_SAFETY_CTRL_ENABLE		
NONE							R/W	NONE					R/W		
0							0h	0					7h		

Access Types Legend

Table 2-804. HSM_TPTC0_WR_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	HSM_TPTC_A0_WR_BUS_SAFETY_CTRL_TYPE	R	0h	Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	HSM_TPTC_A0_WR_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	HSM_TPTC_A0_WR_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Reset Source: mod_g_rst_n

2.3.344 CFG0_HSM_TPTC0_WR_BUS_SAFETY_FI Registers

2.3.344.1 CFG0_TPTC0_WR_BUS_SAFETY_FI Register (Offset = 18464h) [reset = 0h]

Short Description:

Long Description:

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Table 2-805. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8464h

Figure 2-401. HSM_TPTC0_WR_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSM_TPTC_A0_WR_BUS_SAFETY_FI_SAFE								HSM_TPTC_A0_WR_BUS_SAFETY_FI_MAIN							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSM_TPTC_A0_WR_BUS_SAFETY_FI_DATA								RESERVED		HSM_TPTC_A0_WR_BUS_SAFETY_FI_DED	HSM_TPTC_A0_WR_BUS_SAFETY_FI_SEC	HSM_TPTC_A0_WR_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	HSM_TPTC_A0_WR_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	HSM_TPTC_A0_WR_BUS_SAFETY_FI_GLOBAL_SAFE	HSM_TPTC_A0_WR_BUS_SAFETY_FI_GLOBAL_MAIN
R/W								NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h								0		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-806. HSM_TPTC0_WR_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	HSM_TPTC_A0_WR_BUS_SAFETY_FI_SAFE	R/W	0h	Reset Source: mod_g_rst_n
23:16	HSM_TPTC_A0_WR_BUS_SAFETY_FI_MAIN	R/W	0h	Reset Source: mod_g_rst_n
15:8	HSM_TPTC_A0_WR_BUS_SAFETY_FI_DATA	R/W	0h	Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	HSM_TPTC_A0_WR_BUS_SAFETY_FI_DED	R/W	0h	Reset Source: mod_g_rst_n
4	HSM_TPTC_A0_WR_BUS_SAFETY_FI_SEC	R/W	0h	Reset Source: mod_g_rst_n
3	HSM_TPTC_A0_WR_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Reset Source: mod_g_rst_n
2	HSM_TPTC_A0_WR_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Reset Source: mod_g_rst_n
1	HSM_TPTC_A0_WR_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	Reset Source: mod_g_rst_n

Table 2-806. HSM_TPTC0_WR_BUS_SAFETY_FI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HSM_TPTC_A0_WR_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	Reset Source: mod_g_rst_n

2.3.345 CFG0_HSM_TPTC0_WR_BUS_SAFETY_ERR Registers

2.3.345.1 CFG0_TPTC0_WR_BUS_SAFETY_ERR Register (Offset = 18468h) [reset = 0h]

Short Description:

Long Description:

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Table 2-807. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8468h

Figure 2-402. HSM_TPTC0_WR_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSM_TPTC_A0_WR_BUS_SAFETY_ERR_DED								HSM_TPTC_A0_WR_BUS_SAFETY_ERR_SEC							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSM_TPTC_A0_WR_BUS_SAFETY_ERR_COMP_CHECK								HSM_TPTC_A0_WR_BUS_SAFETY_ERR_COMP_ERR							
R								R							
0h								0h							

Access Types Legend

Table 2-808. HSM_TPTC0_WR_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	HSM_TPTC_A0_WR_BUS_SAFETY_ERR_DED	R	0h	Reset Source: mod_g_rst_n
23:16	HSM_TPTC_A0_WR_BUS_SAFETY_ERR_SEC	R	0h	Reset Source: mod_g_rst_n
15:8	HSM_TPTC_A0_WR_BUS_SAFETY_ERR_COMP_CHECK	R	0h	Reset Source: mod_g_rst_n
7:0	HSM_TPTC_A0_WR_BUS_SAFETY_ERR_COMP_ERR	R	0h	Reset Source: mod_g_rst_n

2.3.346 CFG0_HSM_TPTC0_WR_BUS_SAFETY_ERR_STAT_DATA0 Registers

2.3.346.1 CFG0_TPTC0_WR_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 1846Ch) [reset = 0h]

Short Description:

Long Description:

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Table 2-809. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 846Ch

Figure 2-403. HSM_TPTC0_WR_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_DATA0_D1								HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_DATA0_D0							
R								R							
0h								0h							

Access Types Legend

Table 2-810. HSM_TPTC0_WR_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Reset Source: mod_g_rst_n
7:0	HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Reset Source: mod_g_rst_n

2.3.347 CFG0_HSM_TPTC0_WR_BUS_SAFETY_ERR_STAT_CMD Registers

2.3.347.1 CFG0_TPTC0_WR_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 18470h) [reset = 0h]

Short Description:

Long Description:

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Table 2-811. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8470h

Figure 2-404. HSM_TPTC0_WR_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															

Access Types Legend

Table 2-812. HSM_TPTC0_WR_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.348 CFG0_HSM_TPTC0_WR_BUS_SAFETY_ERR_STAT_WRITE Registers

2.3.348.1 CFG0_TPTC0_WR_BUS_SAFETY_ERR_STAT_WRITE Register (Offset = 18474h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-813. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8474h

Figure 2-405. HSM_TPTC0_WR_BUS_SAFETY_ERR_STAT_WRITE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															

Access Types Legend

Table 2-814. HSM_TPTC0_WR_BUS_SAFETY_ERR_STAT_WRITE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.349 CFG0_HSM_TPTC0_WR_BUS_SAFETY_ERR_STAT_WRITERESP Registers

2.3.349.1 CFG0_TPTC0_WR_BUS_SAFETY_ERR_STAT_WRITERESP Register (Offset = 18478h) [reset = 0h]

Short Description:

Long Description:

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Table 2-815. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8478h

Figure 2-406. HSM_TPTC0_WR_BUS_SAFETY_ERR_STAT_WRITERESP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															

Access Types Legend

Table 2-816. HSM_TPTC0_WR_BUS_SAFETY_ERR_STAT_WRITERESP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.350 CFG0_HSM_TPTC1_WR_BUS_SAFETY_CTRL Registers

2.3.350.1 CFG0_TPTC1_WR_BUS_SAFETY_CTRL Register (Offset = 18480h) [reset = 7h]

Short Description:

Long Description:

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Table 2-817. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8480h

Figure 2-407. HSM_TPTC1_WR_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								HSM_TPTC_A1_WR_BUS_SAFETY_CTRL_TYPE							
NONE								R							
b								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							HSM_TPTC_A1_WR_BUS_SAFETY_CTRL_ERR_CLEAR	RESERVED					HSM_TPTC_A1_WR_BUS_SAFETY_CTRL_ENABLE		
NONE							R/W	NONE					R/W		
0							0h	0					7h		

Access Types Legend

Table 2-818. HSM_TPTC1_WR_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	HSM_TPTC_A1_WR_BUS_SAFETY_CTRL_TYPE	R	0h	Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	HSM_TPTC_A1_WR_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	HSM_TPTC_A1_WR_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Reset Source: mod_g_rst_n

2.3.351 CFG0_HSM_TPTC1_WR_BUS_SAFETY_FI Registers

2.3.351.1 CFG0_TPTC1_WR_BUS_SAFETY_FI Register (Offset = 18484h) [reset = 0h]

Short Description:

Long Description:

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Table 2-819. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8484h

Figure 2-408. HSM_TPTC1_WR_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSM_TPTC_A1_WR_BUS_SAFETY_FI_SAFE								HSM_TPTC_A1_WR_BUS_SAFETY_FI_MAIN							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSM_TPTC_A1_WR_BUS_SAFETY_FI_DATA								RESERVED		HSM_TPTC_A1_WR_BUS_SAFETY_FI_DED	HSM_TPTC_A1_WR_BUS_SAFETY_FI_SEC	HSM_TPTC_A1_WR_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	HSM_TPTC_A1_WR_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	HSM_TPTC_A1_WR_BUS_SAFETY_FI_GLOBAL_SAFE	HSM_TPTC_A1_WR_BUS_SAFETY_FI_GLOBAL_MAIN
R/W								NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h								0		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-820. HSM_TPTC1_WR_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	HSM_TPTC_A1_WR_BUS_SAFETY_FI_SAFE	R/W	0h	Reset Source: mod_g_rst_n
23:16	HSM_TPTC_A1_WR_BUS_SAFETY_FI_MAIN	R/W	0h	Reset Source: mod_g_rst_n
15:8	HSM_TPTC_A1_WR_BUS_SAFETY_FI_DATA	R/W	0h	Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	HSM_TPTC_A1_WR_BUS_SAFETY_FI_DED	R/W	0h	Reset Source: mod_g_rst_n
4	HSM_TPTC_A1_WR_BUS_SAFETY_FI_SEC	R/W	0h	Reset Source: mod_g_rst_n
3	HSM_TPTC_A1_WR_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Reset Source: mod_g_rst_n
2	HSM_TPTC_A1_WR_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Reset Source: mod_g_rst_n
1	HSM_TPTC_A1_WR_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	Reset Source: mod_g_rst_n

Table 2-820. HSM_TPTC1_WR_BUS_SAFETY_FI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HSM_TPTC_A1_WR_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	Reset Source: mod_g_rst_n

2.3.352 CFG0_HSM_TPTC1_WR_BUS_SAFETY_ERR Registers

2.3.352.1 CFG0_TPTC1_WR_BUS_SAFETY_ERR Register (Offset = 18488h) [reset = 0h]

Short Description:

Long Description:

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Table 2-821. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8488h

Figure 2-409. HSM_TPTC1_WR_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSM_TPTC_A1_WR_BUS_SAFETY_ERR_DED								HSM_TPTC_A1_WR_BUS_SAFETY_ERR_SEC							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSM_TPTC_A1_WR_BUS_SAFETY_ERR_COMP_CHECK								HSM_TPTC_A1_WR_BUS_SAFETY_ERR_COMP_ERR							
R								R							
0h								0h							

Access Types Legend

Table 2-822. HSM_TPTC1_WR_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	HSM_TPTC_A1_WR_BUS_SAFETY_ERR_DED	R	0h	Reset Source: mod_g_rst_n
23:16	HSM_TPTC_A1_WR_BUS_SAFETY_ERR_SEC	R	0h	Reset Source: mod_g_rst_n
15:8	HSM_TPTC_A1_WR_BUS_SAFETY_ERR_COMP_CHECK	R	0h	Reset Source: mod_g_rst_n
7:0	HSM_TPTC_A1_WR_BUS_SAFETY_ERR_COMP_ERR	R	0h	Reset Source: mod_g_rst_n

2.3.353 CFG0_HSM_TPTC1_WR_BUS_SAFETY_ERR_STAT_DATA0 Registers

2.3.353.1 CFG0_TPTC1_WR_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 1848Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-823. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 848Ch

Figure 2-410. HSM_TPTC1_WR_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_DATA0_D1								HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_DATA0_D0							
R								R							
0h								0h							

Access Types Legend

Table 2-824. HSM_TPTC1_WR_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Reset Source: mod_g_rst_n
7:0	HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Reset Source: mod_g_rst_n

2.3.354 CFG0_HSM_TPTC1_WR_BUS_SAFETY_ERR_STAT_CMD Registers

2.3.354.1 CFG0_TPTC1_WR_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 18490h) [reset = 0h]

Short Description:

Long Description:

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Table 2-825. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8490h

Figure 2-411. HSM_TPTC1_WR_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															

Access Types Legend

Table 2-826. HSM_TPTC1_WR_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.355 CFG0_HSM_TPTC1_WR_BUS_SAFETY_ERR_STAT_WRITE Registers

2.3.355.1 CFG0_TPTC1_WR_BUS_SAFETY_ERR_STAT_WRITE Register (Offset = 18494h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-827. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8494h

Figure 2-412. HSM_TPTC1_WR_BUS_SAFETY_ERR_STAT_WRITE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															

Access Types Legend

Table 2-828. HSM_TPTC1_WR_BUS_SAFETY_ERR_STAT_WRITE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.356 CFG0_HSM_TPTC1_WR_BUS_SAFETY_ERR_STAT_WRITERESP Registers

2.3.356.1 CFG0_TPTC1_WR_BUS_SAFETY_ERR_STAT_WRITERESP Register (Offset = 18498h) [reset = 0h]

Short Description:

Long Description:

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Table 2-829. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8498h

Figure 2-413. HSM_TPTC1_WR_BUS_SAFETY_ERR_STAT_WRITERESP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															

Access Types Legend

Table 2-830. HSM_TPTC1_WR_BUS_SAFETY_ERR_STAT_WRITERESP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.357 CFG0_QSPI0_BUS_SAFETY_CTRL Registers

2.3.357.1 CFG0_BUS_SAFETY_CTRL Register (Offset = 184A0h) [reset = 7h]

Short Description:

Long Description:

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Table 2-831. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 84A0h

Figure 2-414. QSPI0_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MSS_QSPI_BUS_SAFETY_CTRL_TYPE							
NONE								R							
b								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							MSS_QSPI_BUS_SAFETY_CTRL_ERR_CLEAR	RESERVED					MSS_QSPI_BUS_SAFETY_CTRL_ENABLE		
NONE							R/W	NONE					R/W		
0							0h	0					7h		

Access Types Legend

Table 2-832. QSPI0_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	MSS_QSPI_BUS_SAFETY_CTRL_TYPE	R	0h	Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	MSS_QSPI_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	MSS_QSPI_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Reset Source: mod_g_rst_n

2.3.358 CFG0_QSPI0_BUS_SAFETY_FI Registers

2.3.358.1 CFG0_BUS_SAFETY_FI Register (Offset = 184A4h) [reset = 0h]

Short Description:

Long Description:

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Table 2-833. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 84A4h

Figure 2-415. QSPI0_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_QSPI_BUS_SAFETY_FI_SAFE								MSS_QSPI_BUS_SAFETY_FI_MAIN							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_QSPI_BUS_SAFETY_FI_DATA								RESERVED		MSS_QSPI_BUS_SAFETY_FI_DED	MSS_QSPI_BUS_SAFETY_FI_SEC	MSS_QSPI_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	MSS_QSPI_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	MSS_QSPI_BUS_SAFETY_FI_GLOBAL_SAFE	MSS_QSPI_BUS_SAFETY_FI_GLOBAL_MAIN
R/W								NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h								0		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-834. QSPI0_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_QSPI_BUS_SAFETY_FI_SAFE	R/W	0h	Reset Source: mod_g_rst_n
23:16	MSS_QSPI_BUS_SAFETY_FI_MAIN	R/W	0h	Reset Source: mod_g_rst_n
15:8	MSS_QSPI_BUS_SAFETY_FI_DATA	R/W	0h	Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	MSS_QSPI_BUS_SAFETY_FI_DED	R/W	0h	Reset Source: mod_g_rst_n
4	MSS_QSPI_BUS_SAFETY_FI_SEC	R/W	0h	Reset Source: mod_g_rst_n
3	MSS_QSPI_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Reset Source: mod_g_rst_n
2	MSS_QSPI_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Reset Source: mod_g_rst_n
1	MSS_QSPI_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	Reset Source: mod_g_rst_n
0	MSS_QSPI_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	Reset Source: mod_g_rst_n

2.3.359 CFG0_QSPI0_BUS_SAFETY_ERR Registers

2.3.359.1 CFG0_BUS_SAFETY_ERR Register (Offset = 184A8h) [reset = 0h]

Short Description:

Long Description:

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Table 2-835. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 84A8h

Figure 2-416. QSPI0_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_QSPI_BUS_SAFETY_ERR_DED								MSS_QSPI_BUS_SAFETY_ERR_SEC							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_QSPI_BUS_SAFETY_ERR_COMP_CHECK								MSS_QSPI_BUS_SAFETY_ERR_COMP_ERR							
R								R							
0h								0h							

Access Types Legend

Table 2-836. QSPI0_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_QSPI_BUS_SAFETY_ERR_DED	R	0h	Reset Source: mod_g_rst_n
23:16	MSS_QSPI_BUS_SAFETY_ERR_SEC	R	0h	Reset Source: mod_g_rst_n
15:8	MSS_QSPI_BUS_SAFETY_ERR_COMP_CHECK	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_QSPI_BUS_SAFETY_ERR_COMP_ERR	R	0h	Reset Source: mod_g_rst_n

2.3.360 CFG0_QSPI0_BUS_SAFETY_ERR_STAT_DATA0 Registers

2.3.360.1 CFG0_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 184ACh) [reset = 0h]

Short Description:

Long Description:

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Table 2-837. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 84ACh

Figure 2-417. QSPI0_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_QSPI_BUS_SAFETY_ERR_STAT_DATA0_D1								MSS_QSPI_BUS_SAFETY_ERR_STAT_DATA0_D0							
R								R							
0h								0h							

Access Types Legend

Table 2-838. QSPI0_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_QSPI_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_QSPI_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Reset Source: mod_g_rst_n

2.3.361 CFG0_QSPI0_BUS_SAFETY_ERR_STAT_CMD Registers

2.3.361.1 CFG0_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 184B0h) [reset = 0h]

Short Description:

Long Description:

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Table 2-839. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 84B0h

Figure 2-418. QSPI0_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_QSPI_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_QSPI_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															

Access Types Legend

Table 2-840. QSPI0_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_QSPI_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.362 CFG0_QSPI0_BUS_SAFETY_ERR_STAT_WRITE Registers

2.3.362.1 CFG0_BUS_SAFETY_ERR_STAT_WRITE Register (Offset = 184B4h) [reset = 0h]

Short Description:

Long Description:

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Table 2-841. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 84B4h

Figure 2-419. QSPI0_BUS_SAFETY_ERR_STAT_WRITE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_QSPI_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_QSPI_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															

Access Types Legend

Table 2-842. QSPI0_BUS_SAFETY_ERR_STAT_WRITE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_QSPI_BUS_SAFETY_ERR_STAT_WRITE_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.363 CFG0_QSPI0_BUS_SAFETY_ERR_STAT_READ Registers

2.3.363.1 CFG0_BUS_SAFETY_ERR_STAT_READ Register (Offset = 184B8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-843. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 84B8h

Figure 2-420. QSPI0_BUS_SAFETY_ERR_STAT_READ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_QSPI_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_QSPI_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															

Access Types Legend

Table 2-844. QSPI0_BUS_SAFETY_ERR_STAT_READ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_QSPI_BUS_SAFETY_ERR_STAT_READ_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.364 CFG0_QSPI0_BUS_SAFETY_ERR_STAT_WRITERESP Registers

2.3.364.1 CFG0_BUS_SAFETY_ERR_STAT_WRITERESP Register (Offset = 184BCh) [reset = 0h]

Short Description:

Long Description:

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Table 2-845. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 84BCh

Figure 2-421. QSPI0_BUS_SAFETY_ERR_STAT_WRITERESP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_QSPI_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_QSPI_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															

Access Types Legend

Table 2-846. QSPI0_BUS_SAFETY_ERR_STAT_WRITERESP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_QSPI_BUS_SAFETY_ERR_STAT_WRITERESP_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.365 CFG0_MCRC0_BUS_SAFETY_CTRL Registers

2.3.365.1 CFG0_BUS_SAFETY_CTRL Register (Offset = 18540h) [reset = 7h]

Short Description:

Long Description:

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Table 2-847. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8540h

Figure 2-422. MCRC0_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MSS_MCRC_BUS_SAFETY_CTRL_TYPE							
NONE								R							
b								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							MSS_MCRC_BUS_SAFETY_CTRL_ERR_CLEAR	RESERVED					MSS_MCRC_BUS_SAFETY_CTRL_ENABLE		
NONE							R/W	NONE					R/W		
0							0h	0					7h		

Access Types Legend

Table 2-848. MCRC0_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	MSS_MCRC_BUS_SAFETY_CTRL_TYPE	R	0h	Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	MSS_MCRC_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	MSS_MCRC_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Reset Source: mod_g_rst_n

2.3.366 CFG0_MCRC0_BUS_SAFETY_FI Registers

2.3.366.1 CFG0_BUS_SAFETY_FI Register (Offset = 18544h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-849. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8544h

Figure 2-423. MCRC0_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_MCRC_BUS_SAFETY_FI_SAFE								MSS_MCRC_BUS_SAFETY_FI_MAIN							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_MCRC_BUS_SAFETY_FI_DATA								RESERVED		MSS_MCRC_BUS_SAFETY_FI_DED	MSS_MCRC_BUS_SAFETY_FI_SEC	MSS_MCRC_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	MSS_MCRC_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	MSS_MCRC_BUS_SAFETY_FI_GLOBAL_SAFE	MSS_MCRC_BUS_SAFETY_FI_GLOBAL_MAIN
R/W								NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h								0		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-850. MCRC0_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_MCRC_BUS_SAFETY_FI_SAFE	R/W	0h	Reset Source: mod_g_rst_n
23:16	MSS_MCRC_BUS_SAFETY_FI_MAIN	R/W	0h	Reset Source: mod_g_rst_n
15:8	MSS_MCRC_BUS_SAFETY_FI_DATA	R/W	0h	Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	MSS_MCRC_BUS_SAFETY_FI_DED	R/W	0h	Reset Source: mod_g_rst_n
4	MSS_MCRC_BUS_SAFETY_FI_SEC	R/W	0h	Reset Source: mod_g_rst_n
3	MSS_MCRC_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Reset Source: mod_g_rst_n
2	MSS_MCRC_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Reset Source: mod_g_rst_n
1	MSS_MCRC_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	Reset Source: mod_g_rst_n
0	MSS_MCRC_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	Reset Source: mod_g_rst_n

2.3.367 CFG0_MCRC0_BUS_SAFETY_ERR Registers

2.3.367.1 CFG0_BUS_SAFETY_ERR Register (Offset = 18548h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-851. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8548h

Figure 2-424. MCRC0_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_MCRC_BUS_SAFETY_ERR_DED								MSS_MCRC_BUS_SAFETY_ERR_SEC							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_MCRC_BUS_SAFETY_ERR_COMP_CHECK								MSS_MCRC_BUS_SAFETY_ERR_COMP_ERR							
R								R							
0h								0h							

Access Types Legend

Table 2-852. MCRC0_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_MCRC_BUS_SAFETY_ERR_DED	R	0h	Reset Source: mod_g_rst_n
23:16	MSS_MCRC_BUS_SAFETY_ERR_SEC	R	0h	Reset Source: mod_g_rst_n
15:8	MSS_MCRC_BUS_SAFETY_ERR_COMP_CHECK	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_MCRC_BUS_SAFETY_ERR_COMP_ERR	R	0h	Reset Source: mod_g_rst_n

2.3.368 CFG0_MCRC0_BUS_SAFETY_ERR_STAT_DATA0 Registers

2.3.368.1 CFG0_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 1854Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-853. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 854Ch

Figure 2-425. MCRC0_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_MCRC_BUS_SAFETY_ERR_STAT_DATA0_D1								MSS_MCRC_BUS_SAFETY_ERR_STAT_DATA0_D0							
R								R							
0h								0h							

Access Types Legend

Table 2-854. MCRC0_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_MCRC_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_MCRC_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Reset Source: mod_g_rst_n

2.3.369 CFG0_MCRC0_BUS_SAFETY_ERR_STAT_CMD Registers

2.3.369.1 CFG0_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 18550h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-855. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8550h

Figure 2-426. MCRC0_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_MCRC_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_MCRC_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															

Access Types Legend

Table 2-856. MCRC0_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_MCRC_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.370 CFG0_MCRC0_BUS_SAFETY_ERR_STAT_WRITE Registers

2.3.370.1 CFG0_BUS_SAFETY_ERR_STAT_WRITE Register (Offset = 18554h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-857. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8554h

Figure 2-427. MCRC0_BUS_SAFETY_ERR_STAT_WRITE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_MCRC_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_MCRC_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															

Access Types Legend

Table 2-858. MCRC0_BUS_SAFETY_ERR_STAT_WRITE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_MCRC_BUS_SAFETY_ERR_STAT_WRITE_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.371 CFG0_MCRC0_BUS_SAFETY_ERR_STAT_READ Registers

2.3.371.1 CFG0_BUS_SAFETY_ERR_STAT_READ Register (Offset = 18558h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-859. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8558h

Figure 2-428. MCRC0_BUS_SAFETY_ERR_STAT_READ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_MCRC_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_MCRC_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															

Access Types Legend

Table 2-860. MCRC0_BUS_SAFETY_ERR_STAT_READ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_MCRC_BUS_SAFETY_ERR_STAT_READ_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.372 CFG0_MCRC0_BUS_SAFETY_ERR_STAT_WRITERESP Registers

2.3.372.1 CFG0_BUS_SAFETY_ERR_STAT_WRITERESP Register (Offset = 1855Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-861. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 855Ch

Figure 2-429. MCRC0_BUS_SAFETY_ERR_STAT_WRITERESP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_MCRC_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_MCRC_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															

Access Types Legend

Table 2-862. MCRC0_BUS_SAFETY_ERR_STAT_WRITERESP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_MCRC_BUS_SAFETY_ERR_STAT_WRITERESP_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.373 CFG0_PRU-ICSSSLAVE_BUS_SAFETY_CTRL Registers

2.3.373.1 CFG0_BUS_SAFETY_CTRL Register (Offset = 185E0h) [reset = 7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-863. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 85E0h

Figure 2-430. PRU-ICSSSLAVE_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PRU-ICSSSLAVE_BUS_SAFETY_CTRL_TYPE							
NONE								R							
b								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							PRU-ICSSSLAVE_BUS_SAFETY_CTRL_ERR_CLEAR	RESERVED					PRU-ICSSSLAVE_BUS_SAFETY_CTRL_ENABLE		
NONE							R/W	NONE					R/W		
0							0h	0					7h		

Access Types Legend

Table 2-864. PRU-ICSSSLAVE_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	PRU-ICSSSLAVE_BUS_SAFETY_CTRL_TYPE	R	0h	Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	PRU-ICSSSLAVE_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	PRU-ICSSSLAVE_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Reset Source: mod_g_rst_n

2.3.374 CFG0_PRU-ICSSSLAVE_BUS_SAFETY_FI Registers

2.3.374.1 CFG0_BUS_SAFETY_FI Register (Offset = 185E4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-865. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 85E4h

Figure 2-431. PRU-ICSSSLAVE_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRU-ICSSSLAVE_BUS_SAFETY_FI_SAFE								PRU-ICSSSLAVE_BUS_SAFETY_FI_MAIN							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRU-ICSSSLAVE_BUS_SAFETY_FI_DATA								RESERVED		PRU-ICSSSLAVE_BUS_SAFETY_FI_DED	PRU-ICSSSLAVE_BUS_SAFETY_FI_SEC	PRU-ICSSSLAVE_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	PRU-ICSSSLAVE_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	PRU-ICSSSLAVE_BUS_SAFETY_FI_GLOBAL_SAFE	PRU-ICSSSLAVE_BUS_SAFETY_FI_GLOBAL_MAIN
R/W								NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h								0		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-866. PRU-ICSSSLAVE_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PRU-ICSSSLAVE_BUS_SAFETY_FI_SAFE	R/W	0h	Reset Source: mod_g_rst_n
23:16	PRU-ICSSSLAVE_BUS_SAFETY_FI_MAIN	R/W	0h	Reset Source: mod_g_rst_n
15:8	PRU-ICSSSLAVE_BUS_SAFETY_FI_DATA	R/W	0h	Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	PRU-ICSSSLAVE_BUS_SAFETY_FI_DED	R/W	0h	Reset Source: mod_g_rst_n
4	PRU-ICSSSLAVE_BUS_SAFETY_FI_SEC	R/W	0h	Reset Source: mod_g_rst_n
3	PRU-ICSSSLAVE_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Reset Source: mod_g_rst_n
2	PRU-ICSSSLAVE_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Reset Source: mod_g_rst_n

Table 2-866. PRU-ICSSSLAVE_BUS_SAFETY_FI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	PRU-ICSSSLAVE_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	Reset Source: mod_g_rst_n
0	PRU-ICSSSLAVE_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	Reset Source: mod_g_rst_n

2.3.375 CFG0_PRU-ICSSSLAVE_BUS_SAFETY_ERR Registers

2.3.375.1 CFG0_BUS_SAFETY_ERR Register (Offset = 185E8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-867. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 85E8h

Figure 2-432. PRU-ICSSSLAVE_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRU-ICSSSLAVE_BUS_SAFETY_ERR_DED								PRU-ICSSSLAVE_BUS_SAFETY_ERR_SEC							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRU-ICSSSLAVE_BUS_SAFETY_ERR_COMP_CHECK								PRU-ICSSSLAVE_BUS_SAFETY_ERR_COMP_ERR							
R								R							
0h								0h							

Access Types Legend

Table 2-868. PRU-ICSSSLAVE_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PRU-ICSSSLAVE_BUS_SAFETY_ERR_DED	R	0h	Reset Source: mod_g_rst_n
23:16	PRU-ICSSSLAVE_BUS_SAFETY_ERR_SEC	R	0h	Reset Source: mod_g_rst_n
15:8	PRU-ICSSSLAVE_BUS_SAFETY_ERR_COMP_CHECK	R	0h	Reset Source: mod_g_rst_n
7:0	PRU-ICSSSLAVE_BUS_SAFETY_ERR_COMP_ERR	R	0h	Reset Source: mod_g_rst_n

2.3.376 CFG0_PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_DATA0 Registers

2.3.376.1 CFG0_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 185ECh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-869. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 85ECh

Figure 2-433. PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_DATA0_D1								PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_DATA0_D0							
R								R							
0h								0h							

Access Types Legend

Table 2-870. PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Reset Source: mod_g_rst_n
7:0	PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Reset Source: mod_g_rst_n

2.3.377 CFG0_PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_CMD Registers

2.3.377.1 CFG0_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 185F0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-871. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 85F0h

Figure 2-434. PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															

Access Types Legend

Table 2-872. PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.378 CFG0_PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_WRITE Registers

2.3.378.1 CFG0_BUS_SAFETY_ERR_STAT_WRITE Register (Offset = 185F4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-873. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 85F4h

Figure 2-435. PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_WRITE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															

Access Types Legend

Table 2-874. PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_WRITE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_WRITE_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.379 CFG0_PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_READ Registers

2.3.379.1 CFG0_BUS_SAFETY_ERR_STAT_READ Register (Offset = 185F8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-875. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 85F8h

Figure 2-436. PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_READ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															

Access Types Legend

Table 2-876. PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_READ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_READ_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.380 CFG0_PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_WRITERESP Registers

2.3.380.1 CFG0_BUS_SAFETY_ERR_STAT_WRITERESP Register (Offset = 185FCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-877. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 85FCh

Figure 2-437. PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_WRITERESP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															

Access Types Legend

Table 2-878. PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_WRITERESP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PRU-ICSSSLAVE_BUS_SAFETY_ERR_STAT_WRITERESP_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.381 CFG0_L2OCRAM_BANK0_BUS_SAFETY_CTRL Registers

2.3.381.1 CFG0_BANK0_BUS_SAFETY_CTRL Register (Offset = 18620h) [reset = 7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-879. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8620h

Figure 2-438. L2OCRAM_BANK0_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MSS_L2_A_BUS_SAFETY_CTRL_TYPE							
NONE								R							
b								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							MSS_L2_A_BUS_SAFETY_CTRL_ERR_CLEAR	RESERVED					MSS_L2_A_BUS_SAFETY_CTRL_ENABLE		
NONE							R/W	NONE					R/W		
0							0h	0					7h		

Access Types Legend

Table 2-880. L2OCRAM_BANK0_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	MSS_L2_A_BUS_SAFETY_CTRL_TYPE	R	0h	Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	MSS_L2_A_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	MSS_L2_A_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Reset Source: mod_g_rst_n

2.3.382 CFG0_L2OCRAM_BANK0_BUS_SAFETY_FI Registers

2.3.382.1 CFG0_BANK0_BUS_SAFETY_FI Register (Offset = 18624h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-881. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8624h

Figure 2-439. L2OCRAM_BANK0_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_L2_A_BUS_SAFETY_FI_SAFE								MSS_L2_A_BUS_SAFETY_FI_MAIN							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_L2_A_BUS_SAFETY_FI_DATA								RESERVED		MSS_L2_A_BUS_SAFETY_FI_DED	MSS_L2_A_BUS_SAFETY_FI_SEC	MSS_L2_A_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	MSS_L2_A_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	MSS_L2_A_BUS_SAFETY_FI_GLOBAL_SAFE	MSS_L2_A_BUS_SAFETY_FI_GLOBAL_MAIN
R/W								NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h								0		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-882. L2OCRAM_BANK0_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_L2_A_BUS_SAFETY_FI_SAFE	R/W	0h	Reset Source: mod_g_rst_n
23:16	MSS_L2_A_BUS_SAFETY_FI_MAIN	R/W	0h	Reset Source: mod_g_rst_n
15:8	MSS_L2_A_BUS_SAFETY_FI_DATA	R/W	0h	Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	MSS_L2_A_BUS_SAFETY_FI_DED	R/W	0h	Reset Source: mod_g_rst_n
4	MSS_L2_A_BUS_SAFETY_FI_SEC	R/W	0h	Reset Source: mod_g_rst_n
3	MSS_L2_A_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Reset Source: mod_g_rst_n
2	MSS_L2_A_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Reset Source: mod_g_rst_n
1	MSS_L2_A_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	Reset Source: mod_g_rst_n
0	MSS_L2_A_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	Reset Source: mod_g_rst_n

2.3.383 CFG0_L2OCRAM_BANK0_BUS_SAFETY_ERR Registers

2.3.383.1 CFG0_BANK0_BUS_SAFETY_ERR Register (Offset = 18628h) [reset = 0h]

Short Description:

Long Description:

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Table 2-883. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8628h

Figure 2-440. L2OCRAM_BANK0_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_L2_A_BUS_SAFETY_ERR_DED								MSS_L2_A_BUS_SAFETY_ERR_SEC							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_L2_A_BUS_SAFETY_ERR_COMP_CHECK								MSS_L2_A_BUS_SAFETY_ERR_COMP_ERR							
R								R							
0h								0h							

Access Types Legend

Table 2-884. L2OCRAM_BANK0_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_L2_A_BUS_SAFETY_ERR_DED	R	0h	Reset Source: mod_g_rst_n
23:16	MSS_L2_A_BUS_SAFETY_ERR_SEC	R	0h	Reset Source: mod_g_rst_n
15:8	MSS_L2_A_BUS_SAFETY_ERR_COMP_CHECK	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_L2_A_BUS_SAFETY_ERR_COMP_ERR	R	0h	Reset Source: mod_g_rst_n

2.3.384 CFG0_L2OCRAM_BANK0_BUS_SAFETY_ERR_STAT_DATA0 Registers

2.3.384.1 CFG0_BANK0_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 1862Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-885. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 862Ch

Figure 2-441. L2OCRAM_BANK0_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_L2_A_BUS_SAFETY_ERR_STAT_DATA0_D1								MSS_L2_A_BUS_SAFETY_ERR_STAT_DATA0_D0							
R								R							
0h								0h							

Access Types Legend

Table 2-886. L2OCRAM_BANK0_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_L2_A_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_L2_A_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Reset Source: mod_g_rst_n

2.3.385 CFG0_L2OCRAM_BANK0_BUS_SAFETY_ERR_STAT_CMD Registers

2.3.385.1 CFG0_BANK0_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 18630h) [reset = 0h]

Short Description:

Long Description:

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Table 2-887. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8630h

Figure 2-442. L2OCRAM_BANK0_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_L2_A_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_L2_A_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															

Access Types Legend

Table 2-888. L2OCRAM_BANK0_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_L2_A_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.386 CFG0_L2OCRAM_BANK0_BUS_SAFETY_ERR_STAT_WRITE Registers

2.3.386.1 CFG0_BANK0_BUS_SAFETY_ERR_STAT_WRITE Register (Offset = 18634h) [reset = 0h]

Short Description:

Long Description:

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Table 2-889. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8634h

Figure 2-443. L2OCRAM_BANK0_BUS_SAFETY_ERR_STAT_WRITE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_L2_A_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_L2_A_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															

Access Types Legend

Table 2-890. L2OCRAM_BANK0_BUS_SAFETY_ERR_STAT_WRITE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_L2_A_BUS_SAFETY_ERR_STAT_WRITE_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.387 CFG0_L2OCRAM_BANK0_BUS_SAFETY_ERR_STAT_READ Registers

2.3.387.1 CFG0_BANK0_BUS_SAFETY_ERR_STAT_READ Register (Offset = 18638h) [reset = 0h]

Short Description:

Long Description:

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Table 2-891. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8638h

Figure 2-444. L2OCRAM_BANK0_BUS_SAFETY_ERR_STAT_READ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_L2_A_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_L2_A_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															

Access Types Legend

Table 2-892. L2OCRAM_BANK0_BUS_SAFETY_ERR_STAT_READ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_L2_A_BUS_SAFETY_ERR_STAT_READ_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.388 CFG0_L2OCRAM_BANK0_BUS_SAFETY_ERR_STAT_WRITERESP Registers

2.3.388.1 CFG0_BANK0_BUS_SAFETY_ERR_STAT_WRITERESP Register (Offset = 1863Ch) [reset = 0h]

Short Description:

Long Description:

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Table 2-893. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 863Ch

Figure 2-445. L2OCRAM_BANK0_BUS_SAFETY_ERR_STAT_WRITERESP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_L2_A_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_L2_A_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															

Access Types Legend

Table 2-894. L2OCRAM_BANK0_BUS_SAFETY_ERR_STAT_WRITERESP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_L2_A_BUS_SAFETY_ERR_STAT_WRITERESP_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.389 CFG0_L2OCRAM_BANK1_BUS_SAFETY_CTRL Registers

2.3.389.1 CFG0_BANK1_BUS_SAFETY_CTRL Register (Offset = 18640h) [reset = 7h]

Short Description:

Long Description:

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Table 2-895. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8640h

Figure 2-446. L2OCRAM_BANK1_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MSS_L2_B_BUS_SAFETY_CTRL_TYPE							
NONE								R							
b								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							MSS_L2_B_BUS_SAFETY_CTRL_ERR_CLEAR	RESERVED					MSS_L2_B_BUS_SAFETY_CTRL_ENABLE		
NONE							R/W	NONE					R/W		
0							0h	0					7h		

Access Types Legend

Table 2-896. L2OCRAM_BANK1_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	MSS_L2_B_BUS_SAFETY_CTRL_TYPE	R	0h	Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	MSS_L2_B_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	MSS_L2_B_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Reset Source: mod_g_rst_n

2.3.390 CFG0_L2OCRAM_BANK1_BUS_SAFETY_FI Registers

2.3.390.1 CFG0_BANK1_BUS_SAFETY_FI Register (Offset = 18644h) [reset = 0h]

Short Description:

Long Description:

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Table 2-897. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8644h

Figure 2-447. L2OCRAM_BANK1_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_L2_B_BUS_SAFETY_FI_SAFE								MSS_L2_B_BUS_SAFETY_FI_MAIN							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_L2_B_BUS_SAFETY_FI_DATA								RESERVED		MSS_L2_B_BUS_SAFETY_FI_DED	MSS_L2_B_BUS_SAFETY_FI_SEC	MSS_L2_B_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	MSS_L2_B_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	MSS_L2_B_BUS_SAFETY_FI_GLOBAL_SAFE	MSS_L2_B_BUS_SAFETY_FI_GLOBAL_MAIN
R/W								NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h								0		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-898. L2OCRAM_BANK1_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_L2_B_BUS_SAFETY_FI_SAFE	R/W	0h	Reset Source: mod_g_rst_n
23:16	MSS_L2_B_BUS_SAFETY_FI_MAIN	R/W	0h	Reset Source: mod_g_rst_n
15:8	MSS_L2_B_BUS_SAFETY_FI_DATA	R/W	0h	Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	MSS_L2_B_BUS_SAFETY_FI_DED	R/W	0h	Reset Source: mod_g_rst_n
4	MSS_L2_B_BUS_SAFETY_FI_SEC	R/W	0h	Reset Source: mod_g_rst_n
3	MSS_L2_B_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Reset Source: mod_g_rst_n
2	MSS_L2_B_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Reset Source: mod_g_rst_n
1	MSS_L2_B_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	Reset Source: mod_g_rst_n
0	MSS_L2_B_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	Reset Source: mod_g_rst_n

2.3.391 CFG0_L2OCRAM_BANK1_BUS_SAFETY_ERR Registers

2.3.391.1 CFG0_BANK1_BUS_SAFETY_ERR Register (Offset = 18648h) [reset = 0h]

Short Description:

Long Description:

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Table 2-899. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8648h

Figure 2-448. L2OCRAM_BANK1_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_L2_B_BUS_SAFETY_ERR_DED								MSS_L2_B_BUS_SAFETY_ERR_SEC							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_L2_B_BUS_SAFETY_ERR_COMP_CHECK								MSS_L2_B_BUS_SAFETY_ERR_COMP_ERR							
R								R							
0h								0h							

Access Types Legend

Table 2-900. L2OCRAM_BANK1_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_L2_B_BUS_SAFETY_ERR_DED	R	0h	Reset Source: mod_g_rst_n
23:16	MSS_L2_B_BUS_SAFETY_ERR_SEC	R	0h	Reset Source: mod_g_rst_n
15:8	MSS_L2_B_BUS_SAFETY_ERR_COMP_CHECK	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_L2_B_BUS_SAFETY_ERR_COMP_ERR	R	0h	Reset Source: mod_g_rst_n

2.3.392 CFG0_L2OCRAM_BANK1_BUS_SAFETY_ERR_STAT_DATA0 Registers

2.3.392.1 CFG0_BANK1_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 1864Ch) [reset = 0h]

Short Description:

Long Description:

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Table 2-901. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 864Ch

Figure 2-449. L2OCRAM_BANK1_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_L2_B_BUS_SAFETY_ERR_STAT_DATA0_D1								MSS_L2_B_BUS_SAFETY_ERR_STAT_DATA0_D0							
R								R							
0h								0h							

Access Types Legend

Table 2-902. L2OCRAM_BANK1_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_L2_B_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_L2_B_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Reset Source: mod_g_rst_n

2.3.393 CFG0_L2OCRAM_BANK1_BUS_SAFETY_ERR_STAT_CMD Registers

2.3.393.1 CFG0_BANK1_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 18650h) [reset = 0h]

Short Description:

Long Description:

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Table 2-903. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8650h

Figure 2-450. L2OCRAM_BANK1_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_L2_B_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_L2_B_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															

Access Types Legend

Table 2-904. L2OCRAM_BANK1_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_L2_B_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.394 CFG0_L2OCRAM_BANK1_BUS_SAFETY_ERR_STAT_WRITE Registers

2.3.394.1 CFG0_BANK1_BUS_SAFETY_ERR_STAT_WRITE Register (Offset = 18654h) [reset = 0h]

Short Description:

Long Description:

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Table 2-905. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8654h

Figure 2-451. L2OCRAM_BANK1_BUS_SAFETY_ERR_STAT_WRITE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_L2_B_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_L2_B_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															

Access Types Legend

Table 2-906. L2OCRAM_BANK1_BUS_SAFETY_ERR_STAT_WRITE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_L2_B_BUS_SAFETY_ERR_STAT_WRITE_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.395 CFG0_L2OCRAM_BANK1_BUS_SAFETY_ERR_STAT_READ Registers

2.3.395.1 CFG0_BANK1_BUS_SAFETY_ERR_STAT_READ Register (Offset = 18658h) [reset = 0h]

Short Description:

Long Description:

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Table 2-907. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8658h

Figure 2-452. L2OCRAM_BANK1_BUS_SAFETY_ERR_STAT_READ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_L2_B_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_L2_B_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															

Access Types Legend

Table 2-908. L2OCRAM_BANK1_BUS_SAFETY_ERR_STAT_READ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_L2_B_BUS_SAFETY_ERR_STAT_READ_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.396 CFG0_L2OCRAM_BANK1_BUS_SAFETY_ERR_STAT_WRITERESP Registers

2.3.396.1 CFG0_BANK1_BUS_SAFETY_ERR_STAT_WRITERESP Register (Offset = 1865Ch) [reset = 0h]

Short Description:

Long Description:

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Table 2-909. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 865Ch

Figure 2-453. L2OCRAM_BANK1_BUS_SAFETY_ERR_STAT_WRITERESP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_L2_B_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_L2_B_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															

Access Types Legend

Table 2-910. L2OCRAM_BANK1_BUS_SAFETY_ERR_STAT_WRITERESP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_L2_B_BUS_SAFETY_ERR_STAT_WRITERESP_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.397 CFG0_L2OCRAM_BANK2_BUS_SAFETY_CTRL Registers

2.3.397.1 CFG0_BANK2_BUS_SAFETY_CTRL Register (Offset = 18660h) [reset = 7h]

Short Description:

Long Description:

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Table 2-911. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8660h

Figure 2-454. L2OCRAM_BANK2_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MSS_L2_C_BUS_SAFETY_CTRL_TYPE							
NONE								R							
b								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							MSS_L2_C_BUS_SAFETY_CTRL_ERR_CLEAR	RESERVED					MSS_L2_C_BUS_SAFETY_CTRL_ENABLE		
NONE							R/W	NONE					R/W		
0							0h	0					7h		

Access Types Legend

Table 2-912. L2OCRAM_BANK2_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	MSS_L2_C_BUS_SAFETY_CTRL_TYPE	R	0h	Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	MSS_L2_C_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	MSS_L2_C_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Reset Source: mod_g_rst_n

2.3.398 CFG0_L2OCRAM_BANK2_BUS_SAFETY_FI Registers

2.3.398.1 CFG0_BANK2_BUS_SAFETY_FI Register (Offset = 18664h) [reset = 0h]

Short Description:

Long Description:

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Table 2-913. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8664h

Figure 2-455. L2OCRAM_BANK2_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_L2_C_BUS_SAFETY_FI_SAFE								MSS_L2_C_BUS_SAFETY_FI_MAIN							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_L2_C_BUS_SAFETY_FI_DATA								RESERVED		MSS_L2_C_BUS_SAFETY_FI_DED	MSS_L2_C_BUS_SAFETY_FI_SEC	MSS_L2_C_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	MSS_L2_C_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	MSS_L2_C_BUS_SAFETY_FI_GLOBAL_SAFE	MSS_L2_C_BUS_SAFETY_FI_GLOBAL_MAIN
R/W								NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h								0		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-914. L2OCRAM_BANK2_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_L2_C_BUS_SAFETY_FI_SAFE	R/W	0h	Reset Source: mod_g_rst_n
23:16	MSS_L2_C_BUS_SAFETY_FI_MAIN	R/W	0h	Reset Source: mod_g_rst_n
15:8	MSS_L2_C_BUS_SAFETY_FI_DATA	R/W	0h	Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	MSS_L2_C_BUS_SAFETY_FI_DED	R/W	0h	Reset Source: mod_g_rst_n
4	MSS_L2_C_BUS_SAFETY_FI_SEC	R/W	0h	Reset Source: mod_g_rst_n
3	MSS_L2_C_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Reset Source: mod_g_rst_n
2	MSS_L2_C_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Reset Source: mod_g_rst_n
1	MSS_L2_C_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	Reset Source: mod_g_rst_n
0	MSS_L2_C_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	Reset Source: mod_g_rst_n

2.3.399 CFG0_L2OCRAM_BANK2_BUS_SAFETY_ERR Registers

2.3.399.1 CFG0_BANK2_BUS_SAFETY_ERR Register (Offset = 18668h) [reset = 0h]

Short Description:

Long Description:

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Table 2-915. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8668h

Figure 2-456. L2OCRAM_BANK2_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_L2_C_BUS_SAFETY_ERR_DED								MSS_L2_C_BUS_SAFETY_ERR_SEC							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_L2_C_BUS_SAFETY_ERR_COMP_CHECK								MSS_L2_C_BUS_SAFETY_ERR_COMP_ERR							
R								R							
0h								0h							

Access Types Legend

Table 2-916. L2OCRAM_BANK2_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_L2_C_BUS_SAFETY_ERR_DED	R	0h	Reset Source: mod_g_rst_n
23:16	MSS_L2_C_BUS_SAFETY_ERR_SEC	R	0h	Reset Source: mod_g_rst_n
15:8	MSS_L2_C_BUS_SAFETY_ERR_COMP_CHECK	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_L2_C_BUS_SAFETY_ERR_COMP_ERR	R	0h	Reset Source: mod_g_rst_n

2.3.400 CFG0_L2OCRAM_BANK2_BUS_SAFETY_ERR_STAT_DATA0 Registers

2.3.400.1 CFG0_BANK2_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 1866Ch) [reset = 0h]

Short Description:

Long Description:

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Table 2-917. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 866Ch

Figure 2-457. L2OCRAM_BANK2_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_L2_C_BUS_SAFETY_ERR_STAT_DATA0_D1								MSS_L2_C_BUS_SAFETY_ERR_STAT_DATA0_D0							
R								R							
0h								0h							

Access Types Legend

Table 2-918. L2OCRAM_BANK2_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_L2_C_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_L2_C_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Reset Source: mod_g_rst_n

2.3.401 CFG0_L2OCRAM_BANK2_BUS_SAFETY_ERR_STAT_CMD Registers

2.3.401.1 CFG0_BANK2_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 18670h) [reset = 0h]

Short Description:

Long Description:

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Table 2-919. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8670h

Figure 2-458. L2OCRAM_BANK2_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_L2_C_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_L2_C_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															

Access Types Legend

Table 2-920. L2OCRAM_BANK2_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_L2_C_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.402 CFG0_L2OCRAM_BANK2_BUS_SAFETY_ERR_STAT_WRITE Registers

2.3.402.1 CFG0_BANK2_BUS_SAFETY_ERR_STAT_WRITE Register (Offset = 18674h) [reset = 0h]

Short Description:

Long Description:

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Table 2-921. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8674h

Figure 2-459. L2OCRAM_BANK2_BUS_SAFETY_ERR_STAT_WRITE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_L2_C_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_L2_C_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															

Access Types Legend

Table 2-922. L2OCRAM_BANK2_BUS_SAFETY_ERR_STAT_WRITE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_L2_C_BUS_SAFETY_ERR_STAT_WRITE_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.403 CFG0_L2OCRAM_BANK2_BUS_SAFETY_ERR_STAT_READ Registers

2.3.403.1 CFG0_BANK2_BUS_SAFETY_ERR_STAT_READ Register (Offset = 18678h) [reset = 0h]

Short Description:

Long Description:

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Table 2-923. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8678h

Figure 2-460. L2OCRAM_BANK2_BUS_SAFETY_ERR_STAT_READ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_L2_C_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_L2_C_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															

Access Types Legend

Table 2-924. L2OCRAM_BANK2_BUS_SAFETY_ERR_STAT_READ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_L2_C_BUS_SAFETY_ERR_STAT_READ_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.404 CFG0_L2OCRAM_BANK2_BUS_SAFETY_ERR_STAT_WRITERESP Registers

2.3.404.1 CFG0_BANK2_BUS_SAFETY_ERR_STAT_WRITERESP Register (Offset = 1867Ch) [reset = 0h]

Short Description:

Long Description:

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Table 2-925. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 867Ch

Figure 2-461. L2OCRAM_BANK2_BUS_SAFETY_ERR_STAT_WRITERESP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_L2_C_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_L2_C_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															

Access Types Legend

Table 2-926. L2OCRAM_BANK2_BUS_SAFETY_ERR_STAT_WRITERESP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_L2_C_BUS_SAFETY_ERR_STAT_WRITERESP_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.405 CFG0_L2OCRAM_BANK3_BUS_SAFETY_CTRL Registers

2.3.405.1 CFG0_BANK3_BUS_SAFETY_CTRL Register (Offset = 18680h) [reset = 7h]

Short Description:

Long Description:

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Table 2-927. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8680h

Figure 2-462. L2OCRAM_BANK3_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MSS_L2_D_BUS_SAFETY_CTRL_TYPE							
NONE								R							
b								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							MSS_L2_D_BUS_SAFETY_CTRL_ERR_CLEAR	RESERVED					MSS_L2_D_BUS_SAFETY_CTRL_ENABLE		
NONE							R/W	NONE					R/W		
0							0h	0					7h		

Access Types Legend

Table 2-928. L2OCRAM_BANK3_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	MSS_L2_D_BUS_SAFETY_CTRL_TYPE	R	0h	Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	MSS_L2_D_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	MSS_L2_D_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Reset Source: mod_g_rst_n

2.3.406 CFG0_L2OCRAM_BANK3_BUS_SAFETY_FI Registers

2.3.406.1 CFG0_BANK3_BUS_SAFETY_FI Register (Offset = 18684h) [reset = 0h]

Short Description:

Long Description:

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Table 2-929. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8684h

Figure 2-463. L2OCRAM_BANK3_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_L2_D_BUS_SAFETY_FI_SAFE								MSS_L2_D_BUS_SAFETY_FI_MAIN							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_L2_D_BUS_SAFETY_FI_DATA								RESERVED		MSS_L2_D_BUS_SAFETY_FI_DED	MSS_L2_D_BUS_SAFETY_FI_SEC	MSS_L2_D_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	MSS_L2_D_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	MSS_L2_D_BUS_SAFETY_FI_GLOBAL_SAFE	MSS_L2_D_BUS_SAFETY_FI_GLOBAL_MAIN
R/W								NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h								0		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-930. L2OCRAM_BANK3_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_L2_D_BUS_SAFETY_FI_SAFE	R/W	0h	Reset Source: mod_g_rst_n
23:16	MSS_L2_D_BUS_SAFETY_FI_MAIN	R/W	0h	Reset Source: mod_g_rst_n
15:8	MSS_L2_D_BUS_SAFETY_FI_DATA	R/W	0h	Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	MSS_L2_D_BUS_SAFETY_FI_DED	R/W	0h	Reset Source: mod_g_rst_n
4	MSS_L2_D_BUS_SAFETY_FI_SEC	R/W	0h	Reset Source: mod_g_rst_n
3	MSS_L2_D_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Reset Source: mod_g_rst_n
2	MSS_L2_D_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Reset Source: mod_g_rst_n
1	MSS_L2_D_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	Reset Source: mod_g_rst_n
0	MSS_L2_D_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	Reset Source: mod_g_rst_n

2.3.407 CFG0_L2OCRAM_BANK3_BUS_SAFETY_ERR Registers

2.3.407.1 CFG0_BANK3_BUS_SAFETY_ERR Register (Offset = 18688h) [reset = 0h]

Short Description:

Long Description:

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Table 2-931. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8688h

Figure 2-464. L2OCRAM_BANK3_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_L2_D_BUS_SAFETY_ERR_DED								MSS_L2_D_BUS_SAFETY_ERR_SEC							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_L2_D_BUS_SAFETY_ERR_COMP_CHECK								MSS_L2_D_BUS_SAFETY_ERR_COMP_ERR							
R								R							
0h								0h							

Access Types Legend

Table 2-932. L2OCRAM_BANK3_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_L2_D_BUS_SAFETY_ERR_DED	R	0h	Reset Source: mod_g_rst_n
23:16	MSS_L2_D_BUS_SAFETY_ERR_SEC	R	0h	Reset Source: mod_g_rst_n
15:8	MSS_L2_D_BUS_SAFETY_ERR_COMP_CHECK	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_L2_D_BUS_SAFETY_ERR_COMP_ERR	R	0h	Reset Source: mod_g_rst_n

2.3.408 CFG0_L2OCRAM_BANK3_BUS_SAFETY_ERR_STAT_DATA0 Registers

2.3.408.1 CFG0_BANK3_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 1868Ch) [reset = 0h]

Short Description:

Long Description:

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Table 2-933. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 868Ch

Figure 2-465. L2OCRAM_BANK3_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_L2_D_BUS_SAFETY_ERR_STAT_DATA0_D1								MSS_L2_D_BUS_SAFETY_ERR_STAT_DATA0_D0							
R								R							
0h								0h							

Access Types Legend

Table 2-934. L2OCRAM_BANK3_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_L2_D_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_L2_D_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Reset Source: mod_g_rst_n

2.3.409 CFG0_L2OCRAM_BANK3_BUS_SAFETY_ERR_STAT_CMD Registers

2.3.409.1 CFG0_BANK3_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 18690h) [reset = 0h]

Short Description:

Long Description:

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Table 2-935. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8690h

Figure 2-466. L2OCRAM_BANK3_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_L2_D_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_L2_D_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															

Access Types Legend

Table 2-936. L2OCRAM_BANK3_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_L2_D_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.410 CFG0_L2OCRAM_BANK3_BUS_SAFETY_ERR_STAT_WRITE Registers

2.3.410.1 CFG0_BANK3_BUS_SAFETY_ERR_STAT_WRITE Register (Offset = 18694h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-937. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8694h

Figure 2-467. L2OCRAM_BANK3_BUS_SAFETY_ERR_STAT_WRITE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_L2_D_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_L2_D_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															

Access Types Legend

Table 2-938. L2OCRAM_BANK3_BUS_SAFETY_ERR_STAT_WRITE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_L2_D_BUS_SAFETY_ERR_STAT_WRITE_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.411 CFG0_L2OCRAM_BANK3_BUS_SAFETY_ERR_STAT_READ Registers

2.3.411.1 CFG0_BANK3_BUS_SAFETY_ERR_STAT_READ Register (Offset = 18698h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-939. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8698h

Figure 2-468. L2OCRAM_BANK3_BUS_SAFETY_ERR_STAT_READ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_L2_D_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_L2_D_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															

Access Types Legend

Table 2-940. L2OCRAM_BANK3_BUS_SAFETY_ERR_STAT_READ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_L2_D_BUS_SAFETY_ERR_STAT_READ_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.412 CFG0_L2OCRAM_BANK3_BUS_SAFETY_ERR_STAT_WRITERESP Registers

2.3.412.1 CFG0_BANK3_BUS_SAFETY_ERR_STAT_WRITERESP Register (Offset = 1869Ch) [reset = 0h]

Short Description:

Long Description:

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Table 2-941. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 869Ch

Figure 2-469. L2OCRAM_BANK3_BUS_SAFETY_ERR_STAT_WRITERESP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_L2_D_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_L2_D_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															

Access Types Legend

Table 2-942. L2OCRAM_BANK3_BUS_SAFETY_ERR_STAT_WRITERESP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_L2_D_BUS_SAFETY_ERR_STAT_WRITERESP_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.413 CFG0_MBOX_SRAM_BUS_SAFETY_CTRL Registers

2.3.413.1 CFG0_SRAM_BUS_SAFETY_CTRL Register (Offset = 186A0h) [reset = 7h]

Short Description:

Long Description:

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Table 2-943. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 86A0h

Figure 2-470. MBOX_SRAM_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MSS_MBOX_BUS_SAFETY_CTRL_TYPE							
NONE								R							
b								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							MSS_MBOX_BUS_SAFETY_CTRL_ERR_CLEAR	RESERVED					MSS_MBOX_BUS_SAFETY_CTRL_ENABLE		
NONE							R/W	NONE					R/W		
0							0h	0					7h		

Access Types Legend

Table 2-944. MBOX_SRAM_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	MSS_MBOX_BUS_SAFETY_CTRL_TYPE	R	0h	Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	MSS_MBOX_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	MSS_MBOX_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Reset Source: mod_g_rst_n

2.3.414 CFG0_MBOX_SRAM_BUS_SAFETY_FI Registers

2.3.414.1 CFG0_SRAM_BUS_SAFETY_FI Register (Offset = 186A4h) [reset = 0h]

Short Description:

Long Description:

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Table 2-945. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 86A4h

Figure 2-471. MBOX_SRAM_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_MBOX_BUS_SAFETY_FI_SAFE								MSS_MBOX_BUS_SAFETY_FI_MAIN							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_MBOX_BUS_SAFETY_FI_DATA								RESERVED		MSS_MBOX_BUS_SAFETY_FI_DED	MSS_MBOX_BUS_SAFETY_FI_SEC	MSS_MBOX_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	MSS_MBOX_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	MSS_MBOX_BUS_SAFETY_FI_GLOBAL_SAFE	MSS_MBOX_BUS_SAFETY_FI_GLOBAL_MAIN
R/W								NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h								0		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-946. MBOX_SRAM_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_MBOX_BUS_SAFETY_FI_SAFE	R/W	0h	Reset Source: mod_g_rst_n
23:16	MSS_MBOX_BUS_SAFETY_FI_MAIN	R/W	0h	Reset Source: mod_g_rst_n
15:8	MSS_MBOX_BUS_SAFETY_FI_DATA	R/W	0h	Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	MSS_MBOX_BUS_SAFETY_FI_DED	R/W	0h	Reset Source: mod_g_rst_n
4	MSS_MBOX_BUS_SAFETY_FI_SEC	R/W	0h	Reset Source: mod_g_rst_n
3	MSS_MBOX_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Reset Source: mod_g_rst_n
2	MSS_MBOX_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Reset Source: mod_g_rst_n
1	MSS_MBOX_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	Reset Source: mod_g_rst_n
0	MSS_MBOX_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	Reset Source: mod_g_rst_n

2.3.415 CFG0_MBOX_SRAM_BUS_SAFETY_ERR Registers

2.3.415.1 CFG0_SRAM_BUS_SAFETY_ERR Register (Offset = 186A8h) [reset = 0h]

Short Description:

Long Description:

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Table 2-947. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 86A8h

Figure 2-472. MBOX_SRAM_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_MBOX_BUS_SAFETY_ERR_DED								MSS_MBOX_BUS_SAFETY_ERR_SEC							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_MBOX_BUS_SAFETY_ERR_COMP_CHECK								MSS_MBOX_BUS_SAFETY_ERR_COMP_ERR							
R								R							
0h								0h							

Access Types Legend

Table 2-948. MBOX_SRAM_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_MBOX_BUS_SAFETY_ERR_DED	R	0h	Reset Source: mod_g_rst_n
23:16	MSS_MBOX_BUS_SAFETY_ERR_SEC	R	0h	Reset Source: mod_g_rst_n
15:8	MSS_MBOX_BUS_SAFETY_ERR_COMP_CHECK	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_MBOX_BUS_SAFETY_ERR_COMP_ERR	R	0h	Reset Source: mod_g_rst_n

2.3.416 CFG0_MBOX_SRAM_BUS_SAFETY_ERR_STAT_DATA0 Registers

2.3.416.1 CFG0_SRAM_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 186ACh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-949. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 86ACh

Figure 2-473. MBOX_SRAM_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_MBOX_BUS_SAFETY_ERR_STAT_DATA0_D1								MSS_MBOX_BUS_SAFETY_ERR_STAT_DATA0_D0							
R								R							
0h								0h							

Access Types Legend

Table 2-950. MBOX_SRAM_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_MBOX_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_MBOX_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Reset Source: mod_g_rst_n

2.3.417 CFG0_MBOX_SRAM_BUS_SAFETY_ERR_STAT_CMD Registers

2.3.417.1 CFG0_SRAM_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 186B0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-951. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 86B0h

Figure 2-474. MBOX_SRAM_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_MBOX_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_MBOX_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															

Access Types Legend

Table 2-952. MBOX_SRAM_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_MBOX_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.418 CFG0_MBOX_SRAM_BUS_SAFETY_ERR_STAT_WRITE Registers

2.3.418.1 CFG0_SRAM_BUS_SAFETY_ERR_STAT_WRITE Register (Offset = 186B4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-953. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 86B4h

Figure 2-475. MBOX_SRAM_BUS_SAFETY_ERR_STAT_WRITE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_MBOX_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_MBOX_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															

Access Types Legend

Table 2-954. MBOX_SRAM_BUS_SAFETY_ERR_STAT_WRITE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_MBOX_BUS_SAFETY_ERR_STAT_WRITE_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.419 CFG0_MBOX_SRAM_BUS_SAFETY_ERR_STAT_READ Registers

2.3.419.1 CFG0_SRAM_BUS_SAFETY_ERR_STAT_READ Register (Offset = 186B8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-955. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 86B8h

Figure 2-476. MBOX_SRAM_BUS_SAFETY_ERR_STAT_READ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_MBOX_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_MBOX_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															

Access Types Legend

Table 2-956. MBOX_SRAM_BUS_SAFETY_ERR_STAT_READ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_MBOX_BUS_SAFETY_ERR_STAT_READ_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.420 CFG0_MBOX_SRAM_BUS_SAFETY_ERR_STAT_WRITERESP Registers

2.3.420.1 CFG0_SRAM_BUS_SAFETY_ERR_STAT_WRITERESP Register (Offset = 186BCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-957. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 86BCh

Figure 2-477. MBOX_SRAM_BUS_SAFETY_ERR_STAT_WRITERESP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_MBOX_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_MBOX_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															

Access Types Legend

Table 2-958. MBOX_SRAM_BUS_SAFETY_ERR_STAT_WRITERESP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_MBOX_BUS_SAFETY_ERR_STAT_WRITERESP_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.421 CFG0_STM_STIM_BUS_SAFETY_CTRL Registers

2.3.421.1 CFG0_STIM_BUS_SAFETY_CTRL Register (Offset = 186C0h) [reset = 7h]

Short Description:

Long Description:

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Table 2-959. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 86C0h

Figure 2-478. STM_STIM_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MSS_STM_STIM_BUS_SAFETY_CTRL_TYPE							
NONE								R							
b								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							MSS_STM_STIM_BUS_SAFETY_CTRL_ERR_CLEAR	RESERVED					MSS_STM_STIM_BUS_SAFETY_CTRL_ENABLE		
NONE							R/W	NONE					R/W		
0							0h	0					7h		

Access Types Legend

Table 2-960. STM_STIM_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	MSS_STM_STIM_BUS_SAFETY_CTRL_TYPE	R	0h	Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	MSS_STM_STIM_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	MSS_STM_STIM_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Reset Source: mod_g_rst_n

2.3.422 CFG0_STM_STIM_BUS_SAFETY_FI Registers

2.3.422.1 CFG0_STM_STIM_BUS_SAFETY_FI Register (Offset = 186C4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-961. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 86C4h

Figure 2-479. STM_STIM_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_STM_STIM_BUS_SAFETY_FI_SAFE								MSS_STM_STIM_BUS_SAFETY_FI_MAIN							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_STM_STIM_BUS_SAFETY_FI_DATA								RESERVED		MSS_STM_STIM_BUS_SAFETY_FI_DED	MSS_STM_STIM_BUS_SAFETY_FI_SEC	MSS_STM_STIM_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	MSS_STM_STIM_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	MSS_STM_STIM_BUS_SAFETY_FI_GLOBAL_SAFE	MSS_STM_STIM_BUS_SAFETY_FI_GLOBAL_MAIN
R/W								NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h								0		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-962. STM_STIM_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_STM_STIM_BUS_SAFETY_FI_SAFE	R/W	0h	Reset Source: mod_g_rst_n
23:16	MSS_STM_STIM_BUS_SAFETY_FI_MAIN	R/W	0h	Reset Source: mod_g_rst_n
15:8	MSS_STM_STIM_BUS_SAFETY_FI_DATA	R/W	0h	Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	MSS_STM_STIM_BUS_SAFETY_FI_DED	R/W	0h	Reset Source: mod_g_rst_n
4	MSS_STM_STIM_BUS_SAFETY_FI_SEC	R/W	0h	Reset Source: mod_g_rst_n
3	MSS_STM_STIM_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Reset Source: mod_g_rst_n
2	MSS_STM_STIM_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Reset Source: mod_g_rst_n
1	MSS_STM_STIM_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	Reset Source: mod_g_rst_n

Table 2-962. STM_STIM_BUS_SAFETY_FI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MSS_STM_STIM_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	Reset Source: mod_g_rst_n

2.3.423 CFG0_STM_STIM_BUS_SAFETY_ERR Registers

2.3.423.1 CFG0_STM_STIM_BUS_SAFETY_ERR Register (Offset = 186C8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-963. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 86C8h

Figure 2-480. STM_STIM_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_STM_STIM_BUS_SAFETY_ERR_DED								MSS_STM_STIM_BUS_SAFETY_ERR_SEC							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_STM_STIM_BUS_SAFETY_ERR_COMP_CHECK								MSS_STM_STIM_BUS_SAFETY_ERR_COMP_ERR							
R								R							
0h								0h							

Access Types Legend

Table 2-964. STM_STIM_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_STM_STIM_BUS_SAFETY_ERR_DED	R	0h	Reset Source: mod_g_rst_n
23:16	MSS_STM_STIM_BUS_SAFETY_ERR_SEC	R	0h	Reset Source: mod_g_rst_n
15:8	MSS_STM_STIM_BUS_SAFETY_ERR_COMP_CHECK	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_STM_STIM_BUS_SAFETY_ERR_COMP_ERR	R	0h	Reset Source: mod_g_rst_n

2.3.424 CFG0_STM_STIM_BUS_SAFETY_ERR_STAT_DATA0 Registers

2.3.424.1 CFG0_STIM_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 186CCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-965. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 86CCh

Figure 2-481. STM_STIM_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_STM_STIM_BUS_SAFETY_ERR_STAT_DATA0_D1								MSS_STM_STIM_BUS_SAFETY_ERR_STAT_DATA0_D0							
R								R							
0h								0h							

Access Types Legend

Table 2-966. STM_STIM_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_STM_STIM_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_STM_STIM_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Reset Source: mod_g_rst_n

2.3.425 CFG0_STM_STIM_BUS_SAFETY_ERR_STAT_CMD Registers

2.3.425.1 CFG0_STIM_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 186D0h) [reset = 0h]

Short Description:

Long Description:

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Table 2-967. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 86D0h

Figure 2-482. STM_STIM_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_STM_STIM_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_STM_STIM_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															

Access Types Legend

Table 2-968. STM_STIM_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_STM_STIM_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.426 CFG0_STM_STIM_BUS_SAFETY_ERR_STAT_WRITE Registers

2.3.426.1 CFG0_STM_STIM_BUS_SAFETY_ERR_STAT_WRITE Register (Offset = 186D4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-969. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 86D4h

Figure 2-483. STM_STIM_BUS_SAFETY_ERR_STAT_WRITE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_STM_STIM_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_STM_STIM_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															

Access Types Legend

Table 2-970. STM_STIM_BUS_SAFETY_ERR_STAT_WRITE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_STM_STIM_BUS_SAFETY_ERR_STAT_WRITE_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.427 CFG0_STM_STIM_BUS_SAFETY_ERR_STAT_READ Registers

2.3.427.1 CFG0_STM_STIM_BUS_SAFETY_ERR_STAT_READ Register (Offset = 186D8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-971. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 86D8h

Figure 2-484. STM_STIM_BUS_SAFETY_ERR_STAT_READ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_STM_STIM_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_STM_STIM_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															

Access Types Legend

Table 2-972. STM_STIM_BUS_SAFETY_ERR_STAT_READ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_STM_STIM_BUS_SAFETY_ERR_STAT_READ_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.428 CFG0_STM_STIM_BUS_SAFETY_ERR_STAT_WRITERESP Registers

2.3.428.1 CFG0_STM_STIM_BUS_SAFETY_ERR_STAT_WRITERESP Register (Offset = 186DCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-973. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 86DCh

Figure 2-485. STM_STIM_BUS_SAFETY_ERR_STAT_WRITERESP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_STM_STIM_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_STM_STIM_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															

Access Types Legend

Table 2-974. STM_STIM_BUS_SAFETY_ERR_STAT_WRITERESP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_STM_STIM_BUS_SAFETY_ERR_STAT_WRITERESP_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.429 CFG0_MMC0_BUS_SAFETY_CTRL Registers

2.3.429.1 CFG0_BUS_SAFETY_CTRL Register (Offset = 186E0h) [reset = 7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-975. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 86E0h

Figure 2-486. MMC0_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MSS_MMC_BUS_SAFETY_CTRL_TYPE							
NONE								R							
b								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							MSS_MMC_BUS_SAFETY_CTRL_ERR_CLEAR	RESERVED					MSS_MMC_BUS_SAFETY_CTRL_ENABLE		
NONE							R/W	NONE					R/W		
0							0h	0					7h		

Access Types Legend

Table 2-976. MMC0_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	MSS_MMC_BUS_SAFETY_CTRL_TYPE	R	0h	Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	MSS_MMC_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	MSS_MMC_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Reset Source: mod_g_rst_n

2.3.430 CFG0_MMC0_BUS_SAFETY_FI Registers

2.3.430.1 CFG0_BUS_SAFETY_FI Register (Offset = 186E4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-977. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 86E4h

Figure 2-487. MMC0_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_MMC_BUS_SAFETY_FI_SAFE								MSS_MMC_BUS_SAFETY_FI_MAIN							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_MMC_BUS_SAFETY_FI_DATA								RESERVED		MSS_MMC_BUS_SAFETY_FI_DED	MSS_MMC_BUS_SAFETY_FI_SEC	MSS_MMC_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	MSS_MMC_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	MSS_MMC_BUS_SAFETY_FI_GLOBAL_SAFE	MSS_MMC_BUS_SAFETY_FI_GLOBAL_MAIN
R/W								NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h								0		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-978. MMC0_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_MMC_BUS_SAFETY_FI_SAFE	R/W	0h	Reset Source: mod_g_rst_n
23:16	MSS_MMC_BUS_SAFETY_FI_MAIN	R/W	0h	Reset Source: mod_g_rst_n
15:8	MSS_MMC_BUS_SAFETY_FI_DATA	R/W	0h	Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	MSS_MMC_BUS_SAFETY_FI_DED	R/W	0h	Reset Source: mod_g_rst_n
4	MSS_MMC_BUS_SAFETY_FI_SEC	R/W	0h	Reset Source: mod_g_rst_n
3	MSS_MMC_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Reset Source: mod_g_rst_n
2	MSS_MMC_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Reset Source: mod_g_rst_n
1	MSS_MMC_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	Reset Source: mod_g_rst_n
0	MSS_MMC_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	Reset Source: mod_g_rst_n

2.3.431 CFG0_MMC0_BUS_SAFETY_ERR Registers

2.3.431.1 CFG0_BUS_SAFETY_ERR Register (Offset = 186E8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-979. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 86E8h

Figure 2-488. MMC0_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_MMC_BUS_SAFETY_ERR_DED								MSS_MMC_BUS_SAFETY_ERR_SEC							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_MMC_BUS_SAFETY_ERR_COMP_CHECK								MSS_MMC_BUS_SAFETY_ERR_COMP_ERR							
R								R							
0h								0h							

Access Types Legend

Table 2-980. MMC0_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_MMC_BUS_SAFETY_ERR_DED	R	0h	Reset Source: mod_g_rst_n
23:16	MSS_MMC_BUS_SAFETY_ERR_SEC	R	0h	Reset Source: mod_g_rst_n
15:8	MSS_MMC_BUS_SAFETY_ERR_COMP_CHECK	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_MMC_BUS_SAFETY_ERR_COMP_ERR	R	0h	Reset Source: mod_g_rst_n

2.3.432 CFG0_MMC0_BUS_SAFETY_ERR_STAT_DATA0 Registers

2.3.432.1 CFG0_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 186ECh) [reset = 0h]

Short Description:

Long Description:

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Table 2-981. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 86ECh

Figure 2-489. MMC0_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_MMC_BUS_SAFETY_ERR_STAT_DATA0_D1								MSS_MMC_BUS_SAFETY_ERR_STAT_DATA0_D0							
R								R							
0h								0h							

Access Types Legend

Table 2-982. MMC0_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_MMC_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_MMC_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Reset Source: mod_g_rst_n

2.3.433 CFG0_MMC0_BUS_SAFETY_ERR_STAT_CMD Registers

2.3.433.1 CFG0_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 186F0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-983. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 86F0h

Figure 2-490. MMC0_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_MMC_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_MMC_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															

Access Types Legend

Table 2-984. MMC0_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_MMC_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.434 CFG0_MMC0_BUS_SAFETY_ERR_STAT_WRITE Registers

2.3.434.1 CFG0_BUS_SAFETY_ERR_STAT_WRITE Register (Offset = 186F4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-985. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 86F4h

Figure 2-491. MMC0_BUS_SAFETY_ERR_STAT_WRITE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_MMC_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_MMC_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															

Access Types Legend

Table 2-986. MMC0_BUS_SAFETY_ERR_STAT_WRITE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_MMC_BUS_SAFETY_ERR_STAT_WRITE_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.435 CFG0_MMC0_BUS_SAFETY_ERR_STAT_READ Registers

2.3.435.1 CFG0_BUS_SAFETY_ERR_STAT_READ Register (Offset = 186F8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-987. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 86F8h

Figure 2-492. MMC0_BUS_SAFETY_ERR_STAT_READ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_MMC_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_MMC_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															

Access Types Legend

Table 2-988. MMC0_BUS_SAFETY_ERR_STAT_READ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_MMC_BUS_SAFETY_ERR_STAT_READ_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.436 CFG0_MMC0_BUS_SAFETY_ERR_STAT_WRITERESP Registers

2.3.436.1 CFG0_BUS_SAFETY_ERR_STAT_WRITERESP Register (Offset = 186FCh) [reset = 0h]

Short Description:

Long Description:

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Table 2-989. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 86FCh

Figure 2-493. MMC0_BUS_SAFETY_ERR_STAT_WRITERESP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_MMC_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_MMC_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															

Access Types Legend

Table 2-990. MMC0_BUS_SAFETY_ERR_STAT_WRITERESP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_MMC_BUS_SAFETY_ERR_STAT_WRITERESP_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.437 CFG0_GPMC0_BUS_SAFETY_CTRL Registers

2.3.437.1 CFG0_BUS_SAFETY_CTRL Register (Offset = 18700h) [reset = 7h]

Short Description:

Long Description:

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Table 2-991. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8700h

Figure 2-494. GPMC0_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MSS_GPMC_BUS_SAFETY_CTRL_TYPE							
NONE								R							
b								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							MSS_GPMC_BUS_SAFETY_CTRL_ERR_CLEAR	RESERVED					MSS_GPMC_BUS_SAFETY_CTRL_ENABLE		
NONE							R/W	NONE					R/W		
0							0h	0					7h		

Access Types Legend

Table 2-992. GPMC0_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	MSS_GPMC_BUS_SAFETY_CTRL_TYPE	R	0h	Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	MSS_GPMC_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	MSS_GPMC_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Reset Source: mod_g_rst_n

2.3.438 CFG0_GPMC0_BUS_SAFETY_FI Registers

2.3.438.1 CFG0_BUS_SAFETY_FI Register (Offset = 18704h) [reset = 0h]

Short Description:

Long Description:

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Table 2-993. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8704h

Figure 2-495. GPMC0_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_GPMC_BUS_SAFETY_FI_SAFE								MSS_GPMC_BUS_SAFETY_FI_MAIN							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_GPMC_BUS_SAFETY_FI_DATA								RESERVED		MSS_GPMC_BUS_SAFETY_FI_DED	MSS_GPMC_BUS_SAFETY_FI_SEC	MSS_GPMC_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	MSS_GPMC_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	MSS_GPMC_BUS_SAFETY_FI_GLOBAL_SAFE	MSS_GPMC_BUS_SAFETY_FI_GLOBAL_MAIN
R/W								NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h								0		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-994. GPMC0_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_GPMC_BUS_SAFETY_FI_SAFE	R/W	0h	Reset Source: mod_g_rst_n
23:16	MSS_GPMC_BUS_SAFETY_FI_MAIN	R/W	0h	Reset Source: mod_g_rst_n
15:8	MSS_GPMC_BUS_SAFETY_FI_DATA	R/W	0h	Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	MSS_GPMC_BUS_SAFETY_FI_DED	R/W	0h	Reset Source: mod_g_rst_n
4	MSS_GPMC_BUS_SAFETY_FI_SEC	R/W	0h	Reset Source: mod_g_rst_n
3	MSS_GPMC_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Reset Source: mod_g_rst_n
2	MSS_GPMC_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Reset Source: mod_g_rst_n
1	MSS_GPMC_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	Reset Source: mod_g_rst_n
0	MSS_GPMC_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	Reset Source: mod_g_rst_n

2.3.439 CFG0_GPMC0_BUS_SAFETY_ERR Registers

2.3.439.1 CFG0_BUS_SAFETY_ERR Register (Offset = 18708h) [reset = 0h]

Short Description:

Long Description:

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Table 2-995. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8708h

Figure 2-496. GPMC0_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_GPMC_BUS_SAFETY_ERR_DED								MSS_GPMC_BUS_SAFETY_ERR_SEC							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_GPMC_BUS_SAFETY_ERR_COMP_CHECK								MSS_GPMC_BUS_SAFETY_ERR_COMP_ERR							
R								R							
0h								0h							

Access Types Legend

Table 2-996. GPMC0_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_GPMC_BUS_SAFETY_ERR_DED	R	0h	Reset Source: mod_g_rst_n
23:16	MSS_GPMC_BUS_SAFETY_ERR_SEC	R	0h	Reset Source: mod_g_rst_n
15:8	MSS_GPMC_BUS_SAFETY_ERR_COMP_CHECK	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_GPMC_BUS_SAFETY_ERR_COMP_ERR	R	0h	Reset Source: mod_g_rst_n

2.3.440 CFG0_GPMC0_BUS_SAFETY_ERR_STAT_DATA0 Registers

2.3.440.1 CFG0_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 1870Ch) [reset = 0h]

Short Description:

Long Description:

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Table 2-997. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 870Ch

Figure 2-497. GPMC0_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_GPMC_BUS_SAFETY_ERR_STAT_DATA0_D1								MSS_GPMC_BUS_SAFETY_ERR_STAT_DATA0_D0							
R								R							
0h								0h							

Access Types Legend

Table 2-998. GPMC0_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_GPMC_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_GPMC_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Reset Source: mod_g_rst_n

2.3.441 CFG0_GPMC0_BUS_SAFETY_ERR_STAT_CMD Registers

2.3.441.1 CFG0_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 18710h) [reset = 0h]

Short Description:

Long Description:

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Table 2-999. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8710h

Figure 2-498. GPMC0_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_GPMC_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_GPMC_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															

Access Types Legend

Table 2-1000. GPMC0_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_GPMC_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.442 CFG0_GPMC0_BUS_SAFETY_ERR_STAT_WRITE Registers

2.3.442.1 CFG0_BUS_SAFETY_ERR_STAT_WRITE Register (Offset = 18714h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1001. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8714h

Figure 2-499. GPMC0_BUS_SAFETY_ERR_STAT_WRITE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_GPMC_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_GPMC_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															

Access Types Legend

Table 2-1002. GPMC0_BUS_SAFETY_ERR_STAT_WRITE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_GPMC_BUS_SAFETY_ERR_STAT_WRITE_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.443 CFG0_GPMC0_BUS_SAFETY_ERR_STAT_READ Registers

2.3.443.1 CFG0_BUS_SAFETY_ERR_STAT_READ Register (Offset = 18718h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1003. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8718h

Figure 2-500. GPMC0_BUS_SAFETY_ERR_STAT_READ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_GPMC_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_GPMC_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															

Access Types Legend

Table 2-1004. GPMC0_BUS_SAFETY_ERR_STAT_READ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_GPMC_BUS_SAFETY_ERR_STAT_READ_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.444 CFG0_GPMC0_BUS_SAFETY_ERR_STAT_WRITERESP Registers

2.3.444.1 CFG0_BUS_SAFETY_ERR_STAT_WRITERESP Register (Offset = 1871Ch) [reset = 0h]

Short Description:

Long Description:

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Table 2-1005. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 871Ch

Figure 2-501. GPMC0_BUS_SAFETY_ERR_STAT_WRITERESP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_GPMC_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_GPMC_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															

Access Types Legend

Table 2-1006. GPMC0_BUS_SAFETY_ERR_STAT_WRITERESP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_GPMC_BUS_SAFETY_ERR_STAT_WRITERESP_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.445 CFG0_R5SS0_CORE0_AHB_BUS_SAFETY_CTRL Registers

2.3.445.1 CFG0_CORE0_AHB_BUS_SAFETY_CTRL Register (Offset = 18740h) [reset = 7h]

Short Description:

Long Description:

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Table 2-1007. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8740h

Figure 2-502. R5SS0_CORE0_AHB_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_CTRL_TYPE							
NONE								R							
b								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_CTRL_ERR_CLEAR	RESERVED					MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_CTRL_ENABLE		
NONE							R/W	NONE					R/W		
0							0h	0					7h		

Access Types Legend

Table 2-1008. R5SS0_CORE0_AHB_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_CTRL_TYPE	R	0h	Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Reset Source: mod_g_rst_n

2.3.446 CFG0_R5SS0_CORE0_AHB_BUS_SAFETY_FI Registers

2.3.446.1 CFG0_CORE0_AHB_BUS_SAFETY_FI Register (Offset = 18744h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1009. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8744h

Figure 2-503. R5SS0_CORE0_AHB_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_FI_SAFE								MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_FI_MAIN							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_FI_DATA								RESERVED		MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_FI_DED	MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_FI_SEC	MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_FI_GLOBAL_SAFE	MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_FI_GLOBAL_MAIN
R/W								NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h								0		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-1010. R5SS0_CORE0_AHB_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_FI_SAFE	R/W	0h	Reset Source: mod_g_rst_n
23:16	MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_FI_MAIN	R/W	0h	Reset Source: mod_g_rst_n
15:8	MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_FI_DATA	R/W	0h	Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_FI_DED	R/W	0h	Reset Source: mod_g_rst_n
4	MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_FI_SEC	R/W	0h	Reset Source: mod_g_rst_n
3	MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Reset Source: mod_g_rst_n
2	MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Reset Source: mod_g_rst_n

Table 2-1010. R5SS0_CORE0_AHB_BUS_SAFETY_FI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	Reset Source: mod_g_rst_n
0	MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	Reset Source: mod_g_rst_n

2.3.447 CFG0_R5SS0_CORE0_AHB_BUS_SAFETY_ERR Registers

2.3.447.1 CFG0_CORE0_AHB_BUS_SAFETY_ERR Register (Offset = 18748h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1011. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8748h

Figure 2-504. R5SS0_CORE0_AHB_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_ERR_DED								MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_ERR_SEC							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_ERR_COMP_CHECK								MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_ERR_COMP_ERR							
R								R							
0h								0h							

Access Types Legend

Table 2-1012. R5SS0_CORE0_AHB_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_ERR_DED	R	0h	Reset Source: mod_g_rst_n
23:16	MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_ERR_SEC	R	0h	Reset Source: mod_g_rst_n
15:8	MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_ERR_COMP_CHECK	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_ERR_COMP_ERR	R	0h	Reset Source: mod_g_rst_n

2.3.448 CFG0_R5SS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_DATA0 Registers

2.3.448.1 CFG0_CORE0_AHB_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 1874Ch) [reset = 0h]

Short Description:

Long Description:

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Table 2-1013. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 874Ch

Figure 2-505. R5SS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_DATA0_D1								MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_DATA0_D0							
R								R							
0h								0h							

Access Types Legend

Table 2-1014. R5SS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Reset Source: mod_g_rst_n

2.3.449 CFG0_R5SS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_CMD Registers

2.3.449.1 CFG0_CORE0_AHB_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 18750h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1015. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8750h

Figure 2-506. R5SS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															

Access Types Legend

Table 2-1016. R5SS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.450 CFG0_R5SS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITE Registers

2.3.450.1 CFG0_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITE Register (Offset = 18754h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1017. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8754h

Figure 2-507. R5SS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															

Access Types Legend

Table 2-1018. R5SS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITE_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.451 CFG0_R5SS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_READ Registers

2.3.451.1 CFG0_CORE0_AHB_BUS_SAFETY_ERR_STAT_READ Register (Offset = 18758h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1019. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8758h

Figure 2-508. R5SS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_READ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															

Access Types Legend

Table 2-1020. R5SS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_READ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_READ_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.452 CFG0_R5SS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITERESP Registers

2.3.452.1 CFG0_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITERESP Register (Offset = 1875Ch) [reset = 0h]

Short Description:

Long Description:

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Table 2-1021. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 875Ch

Figure 2-509. R5SS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITERESP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															

Access Types Legend

Table 2-1022. R5SS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITERESP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITERESP_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.453 CFG0_R5SS0_CORE1_AHB_BUS_SAFETY_CTRL Registers

2.3.453.1 CFG0_CORE1_AHB_BUS_SAFETY_CTRL Register (Offset = 18760h) [reset = 7h]

Short Description:

Long Description:

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Table 2-1023. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8760h

Figure 2-510. R5SS0_CORE1_AHB_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_CTRL_TYPE							
NONE								R							
b								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_CTRL_ERR_CLEAR	RESERVED					MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_CTRL_ENABLE		
NONE							R/W	NONE					R/W		
0							0h	0					7h		

Access Types Legend

Table 2-1024. R5SS0_CORE1_AHB_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_CTRL_TYPE	R	0h	Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Reset Source: mod_g_rst_n

2.3.454 CFG0_R5SS0_CORE1_AHB_BUS_SAFETY_FI Registers

2.3.454.1 CFG0_CORE1_AHB_BUS_SAFETY_FI Register (Offset = 18764h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1025. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8764h

Figure 2-511. R5SS0_CORE1_AHB_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_FI_SAFE								MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_FI_MAIN							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_FI_DATA								RESERVED		MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_FI_DED	MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_FI_SEC	MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_FI_GLOBAL_SAFE	MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_FI_GLOBAL_MAIN
R/W								NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h								0		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-1026. R5SS0_CORE1_AHB_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_FI_SAFE	R/W	0h	Reset Source: mod_g_rst_n
23:16	MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_FI_MAIN	R/W	0h	Reset Source: mod_g_rst_n
15:8	MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_FI_DATA	R/W	0h	Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_FI_DED	R/W	0h	Reset Source: mod_g_rst_n
4	MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_FI_SEC	R/W	0h	Reset Source: mod_g_rst_n
3	MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Reset Source: mod_g_rst_n
2	MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Reset Source: mod_g_rst_n

Table 2-1026. R5SS0_CORE1_AHB_BUS_SAFETY_FI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	Reset Source: mod_g_rst_n
0	MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	Reset Source: mod_g_rst_n

2.3.455 CFG0_R5SS0_CORE1_AHB_BUS_SAFETY_ERR Registers

2.3.455.1 CFG0_CORE1_AHB_BUS_SAFETY_ERR Register (Offset = 18768h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1027. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8768h

Figure 2-512. R5SS0_CORE1_AHB_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_ERR_DED								MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_ERR_SEC							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_ERR_COMP_CHECK								MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_ERR_COMP_ERR							
R								R							
0h								0h							

Access Types Legend

Table 2-1028. R5SS0_CORE1_AHB_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_ERR_DED	R	0h	Reset Source: mod_g_rst_n
23:16	MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_ERR_SEC	R	0h	Reset Source: mod_g_rst_n
15:8	MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_ERR_COMP_CHECK	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_ERR_COMP_ERR	R	0h	Reset Source: mod_g_rst_n

2.3.456 CFG0_R5SS0_CORE1_AHB_BUS_SAFETY_ERR_STAT_DATA0 Registers

2.3.456.1 CFG0_CORE1_AHB_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 1876Ch) [reset = 0h]

Short Description:

Long Description:

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Table 2-1029. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 876Ch

Figure 2-513. R5SS0_CORE1_AHB_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_DATA0_D1								MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_DATA0_D0							
R								R							
0h								0h							

Access Types Legend

Table 2-1030. R5SS0_CORE1_AHB_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Reset Source: mod_g_rst_n

2.3.457 CFG0_R5SS0_CORE1_AHB_BUS_SAFETY_ERR_STAT_CMD Registers

2.3.457.1 CFG0_CORE1_AHB_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 18770h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1031. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8770h

Figure 2-514. R5SS0_CORE1_AHB_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															

Access Types Legend

Table 2-1032. R5SS0_CORE1_AHB_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.458 CFG0_R5SS0_CORE1_AHB_BUS_SAFETY_ERR_STAT_WRITE Registers

2.3.458.1 CFG0_CORE1_AHB_BUS_SAFETY_ERR_STAT_WRITE Register (Offset = 18774h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1033. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8774h

Figure 2-515. R5SS0_CORE1_AHB_BUS_SAFETY_ERR_STAT_WRITE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															

Access Types Legend

Table 2-1034. R5SS0_CORE1_AHB_BUS_SAFETY_ERR_STAT_WRITE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITE_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.459 CFG0_R5SS0_CORE1_AHB_BUS_SAFETY_ERR_STAT_READ Registers

2.3.459.1 CFG0_CORE1_AHB_BUS_SAFETY_ERR_STAT_READ Register (Offset = 18778h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1035. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8778h

Figure 2-516. R5SS0_CORE1_AHB_BUS_SAFETY_ERR_STAT_READ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															

Access Types Legend

Table 2-1036. R5SS0_CORE1_AHB_BUS_SAFETY_ERR_STAT_READ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_READ_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.460 CFG0_R5SS0_CORE1_AHB_BUS_SAFETY_ERR_STAT_WRITERESP Registers

2.3.460.1 CFG0_CORE1_AHB_BUS_SAFETY_ERR_STAT_WRITERESP Register (Offset = 1877Ch) [reset = 0h]

Short Description:

Long Description:

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Table 2-1037. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 877Ch

Figure 2-517. R5SS0_CORE1_AHB_BUS_SAFETY_ERR_STAT_WRITERESP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															

Access Types Legend

Table 2-1038. R5SS0_CORE1_AHB_BUS_SAFETY_ERR_STAT_WRITERESP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITERESP_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.461 CFG0_R5SS1_CORE0_AHB_BUS_SAFETY_CTRL Registers

2.3.461.1 CFG0_CORE0_AHB_BUS_SAFETY_CTRL Register (Offset = 18780h) [reset = 7h]

Short Description:

Long Description:

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Table 2-1039. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8780h

Figure 2-518. R5SS1_CORE0_AHB_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MSS_R5FSS01_AHB_BUS_SAFETY_CTRL_TYPE							
NONE								R							
b								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							MSS_R5FSS01_AHB_BUS_SAFETY_CTRL_ERR_CLEAR	RESERVED					MSS_R5FSS01_AHB_BUS_SAFETY_CTRL_ENABLE		
NONE							R/W	NONE					R/W		
0							0h	0					7h		

Access Types Legend

Table 2-1040. R5SS1_CORE0_AHB_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	MSS_R5FSS01_AHB_BUS_SAFETY_CTRL_TYPE	R	0h	Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	MSS_R5FSS01_AHB_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	MSS_R5FSS01_AHB_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Reset Source: mod_g_rst_n

2.3.462 CFG0_R5SS1_CORE0_AHB_BUS_SAFETY_FI Registers

2.3.462.1 CFG0_CORE0_AHB_BUS_SAFETY_FI Register (Offset = 18784h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1041. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8784h

Figure 2-519. R5SS1_CORE0_AHB_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS01_AHB_BUS_SAFETY_FI_SAFE								MSS_R5FSS01_AHB_BUS_SAFETY_FI_MAIN							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS01_AHB_BUS_SAFETY_FI_DATA								RESERVED		MSS_R5FSS01_AHB_BUS_SAFETY_FI_DED	MSS_R5FSS01_AHB_BUS_SAFETY_FI_SEC	MSS_R5FSS01_AHB_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	MSS_R5FSS01_AHB_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	MSS_R5FSS01_AHB_BUS_SAFETY_FI_GLOBAL_SAFE	MSS_R5FSS01_AHB_BUS_SAFETY_FI_GLOBAL_MAIN
R/W								NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h								0		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-1042. R5SS1_CORE0_AHB_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_R5FSS01_AHB_BUS_SAFETY_FI_SAFE	R/W	0h	Reset Source: mod_g_rst_n
23:16	MSS_R5FSS01_AHB_BUS_SAFETY_FI_MAIN	R/W	0h	Reset Source: mod_g_rst_n
15:8	MSS_R5FSS01_AHB_BUS_SAFETY_FI_DATA	R/W	0h	Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	MSS_R5FSS01_AHB_BUS_SAFETY_FI_DED	R/W	0h	Reset Source: mod_g_rst_n
4	MSS_R5FSS01_AHB_BUS_SAFETY_FI_SEC	R/W	0h	Reset Source: mod_g_rst_n
3	MSS_R5FSS01_AHB_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Reset Source: mod_g_rst_n
2	MSS_R5FSS01_AHB_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Reset Source: mod_g_rst_n
1	MSS_R5FSS01_AHB_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	Reset Source: mod_g_rst_n

Table 2-1042. R5SS1_CORE0_AHB_BUS_SAFETY_FI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MSS_R5FSS01_AHB_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	Reset Source: mod_g_rst_n

2.3.463 CFG0_R5SS1_CORE0_AHB_BUS_SAFETY_ERR Registers

2.3.463.1 CFG0_CORE0_AHB_BUS_SAFETY_ERR Register (Offset = 18788h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1043. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8788h

Figure 2-520. R5SS1_CORE0_AHB_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS01_AHB_BUS_SAFETY_ERR_DED								MSS_R5FSS01_AHB_BUS_SAFETY_ERR_SEC							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS01_AHB_BUS_SAFETY_ERR_COMP_CHECK								MSS_R5FSS01_AHB_BUS_SAFETY_ERR_COMP_ERR							
R								R							
0h								0h							

Access Types Legend

Table 2-1044. R5SS1_CORE0_AHB_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_R5FSS01_AHB_BUS_SAFETY_ERR_DED	R	0h	Reset Source: mod_g_rst_n
23:16	MSS_R5FSS01_AHB_BUS_SAFETY_ERR_SEC	R	0h	Reset Source: mod_g_rst_n
15:8	MSS_R5FSS01_AHB_BUS_SAFETY_ERR_COMP_CHECK	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_R5FSS01_AHB_BUS_SAFETY_ERR_COMP_ERR	R	0h	Reset Source: mod_g_rst_n

2.3.464 CFG0_R5SS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_DATA0 Registers

2.3.464.1 CFG0_CORE0_AHB_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 1878Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1045. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 878Ch

Figure 2-521. R5SS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS01_AHB_BUS_SAFETY_ERR_STAT_DATA0_D1								MSS_R5FSS01_AHB_BUS_SAFETY_ERR_STAT_DATA0_D0							
R								R							
0h								0h							

Access Types Legend

Table 2-1046. R5SS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_R5FSS01_AHB_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_R5FSS01_AHB_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Reset Source: mod_g_rst_n

2.3.465 CFG0_R5SS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_CMD Registers

2.3.465.1 CFG0_CORE0_AHB_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 18790h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1047. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8790h

Figure 2-522. R5SS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS01_AHB_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS01_AHB_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															

Access Types Legend

Table 2-1048. R5SS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS01_AHB_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.466 CFG0_R5SS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITE Registers

2.3.466.1 CFG0_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITE Register (Offset = 18794h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1049. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8794h

Figure 2-523. R5SS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS01_AHB_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS01_AHB_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															

Access Types Legend

Table 2-1050. R5SS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS01_AHB_BUS_SAFETY_ERR_STAT_WRITE_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.467 CFG0_R5SS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_READ Registers

2.3.467.1 CFG0_CORE0_AHB_BUS_SAFETY_ERR_STAT_READ Register (Offset = 18798h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1051. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8798h

Figure 2-524. R5SS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_READ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS01_AHB_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS01_AHB_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															

Access Types Legend

Table 2-1052. R5SS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_READ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS01_AHB_BUS_SAFETY_ERR_STAT_READ_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.468 CFG0_R5SS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITERESP Registers

2.3.468.1 CFG0_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITERESP Register (Offset = 1879Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1053. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 879Ch

Figure 2-525. R5SS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITERESP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS01_AHB_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS01_AHB_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															

Access Types Legend

Table 2-1054. R5SS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITERESP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS01_AHB_BUS_SAFETY_ERR_STAT_WRITERESP_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.469 CFG0_R5SS1_CORE1_AHB_BUS_SAFETY_CTRL Registers

2.3.469.1 CFG0_CORE1_AHB_BUS_SAFETY_CTRL Register (Offset = 187A0h) [reset = 7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1055. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 87A0h

Figure 2-526. R5SS1_CORE1_AHB_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MSS_R5FSS11_AHB_BUS_SAFETY_CTRL_TYPE							
NONE								R							
b								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							MSS_R5FSS11_AHB_BUS_SAFETY_CTRL_ERR_CLEAR	RESERVED					MSS_R5FSS11_AHB_BUS_SAFETY_CTRL_ENABLE		
NONE							R/W	NONE					R/W		
0							0h	0					7h		

Access Types Legend

Table 2-1056. R5SS1_CORE1_AHB_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	MSS_R5FSS11_AHB_BUS_SAFETY_CTRL_TYPE	R	0h	Reset Source: mod_g_rst_n
15:9	RESERVED	NONE		Reserved
8	MSS_R5FSS11_AHB_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	MSS_R5FSS11_AHB_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Reset Source: mod_g_rst_n

2.3.470 CFG0_R5SS1_CORE1_AHB_BUS_SAFETY_FI Registers

2.3.470.1 CFG0_CORE1_AHB_BUS_SAFETY_FI Register (Offset = 187A4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1057. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 87A4h

Figure 2-527. R5SS1_CORE1_AHB_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS11_AHB_BUS_SAFETY_FI_SAFE								MSS_R5FSS11_AHB_BUS_SAFETY_FI_MAIN							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS11_AHB_BUS_SAFETY_FI_DATA								RESERVED		MSS_R5FSS11_AHB_BUS_SAFETY_FI_DED	MSS_R5FSS11_AHB_BUS_SAFETY_FI_SEC	MSS_R5FSS11_AHB_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	MSS_R5FSS11_AHB_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	MSS_R5FSS11_AHB_BUS_SAFETY_FI_GLOBAL_SAFE	MSS_R5FSS11_AHB_BUS_SAFETY_FI_GLOBAL_MAIN
R/W								NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h								0		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-1058. R5SS1_CORE1_AHB_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_R5FSS11_AHB_BUS_SAFETY_FI_SAFE	R/W	0h	Reset Source: mod_g_rst_n
23:16	MSS_R5FSS11_AHB_BUS_SAFETY_FI_MAIN	R/W	0h	Reset Source: mod_g_rst_n
15:8	MSS_R5FSS11_AHB_BUS_SAFETY_FI_DATA	R/W	0h	Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	MSS_R5FSS11_AHB_BUS_SAFETY_FI_DED	R/W	0h	Reset Source: mod_g_rst_n
4	MSS_R5FSS11_AHB_BUS_SAFETY_FI_SEC	R/W	0h	Reset Source: mod_g_rst_n
3	MSS_R5FSS11_AHB_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Reset Source: mod_g_rst_n
2	MSS_R5FSS11_AHB_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Reset Source: mod_g_rst_n
1	MSS_R5FSS11_AHB_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	Reset Source: mod_g_rst_n

Table 2-1058. R5SS1_CORE1_AHB_BUS_SAFETY_FI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MSS_R5FSS11_AHB_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	Reset Source: mod_g_rst_n

2.3.471 CFG0_R5SS1_CORE1_AHB_BUS_SAFETY_ERR Registers

2.3.471.1 CFG0_CORE1_AHB_BUS_SAFETY_ERR Register (Offset = 187A8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1059. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 87A8h

Figure 2-528. R5SS1_CORE1_AHB_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS11_AHB_BUS_SAFETY_ERR_DED								MSS_R5FSS11_AHB_BUS_SAFETY_ERR_SEC							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS11_AHB_BUS_SAFETY_ERR_COMP_CHECK								MSS_R5FSS11_AHB_BUS_SAFETY_ERR_COMP_ERR							
R								R							
0h								0h							

Access Types Legend

Table 2-1060. R5SS1_CORE1_AHB_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MSS_R5FSS11_AHB_BUS_SAFETY_ERR_DED	R	0h	Reset Source: mod_g_rst_n
23:16	MSS_R5FSS11_AHB_BUS_SAFETY_ERR_SEC	R	0h	Reset Source: mod_g_rst_n
15:8	MSS_R5FSS11_AHB_BUS_SAFETY_ERR_COMP_CHECK	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_R5FSS11_AHB_BUS_SAFETY_ERR_COMP_ERR	R	0h	Reset Source: mod_g_rst_n

2.3.472 CFG0_R5SS1_CORE1_AHB_BUS_SAFETY_ERR_STAT_DATA0 Registers

2.3.472.1 CFG0_CORE1_AHB_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 187ACh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1061. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 87ACh

Figure 2-529. R5SS1_CORE1_AHB_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS11_AHB_BUS_SAFETY_ERR_STAT_DATA0_D1								MSS_R5FSS11_AHB_BUS_SAFETY_ERR_STAT_DATA0_D0							
R								R							
0h								0h							

Access Types Legend

Table 2-1062. R5SS1_CORE1_AHB_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_R5FSS11_AHB_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Reset Source: mod_g_rst_n
7:0	MSS_R5FSS11_AHB_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Reset Source: mod_g_rst_n

2.3.473 CFG0_R5SS1_CORE1_AHB_BUS_SAFETY_ERR_STAT_CMD Registers

2.3.473.1 CFG0_CORE1_AHB_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 187B0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1063. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 87B0h

Figure 2-530. R5SS1_CORE1_AHB_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS11_AHB_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS11_AHB_BUS_SAFETY_ERR_STAT_CMD_STAT															
R															
0h															

Access Types Legend

Table 2-1064. R5SS1_CORE1_AHB_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS11_AHB_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.474 CFG0_R5SS1_CORE1_AHB_BUS_SAFETY_ERR_STAT_WRITE Registers

2.3.474.1 CFG0_CORE1_AHB_BUS_SAFETY_ERR_STAT_WRITE Register (Offset = 187B4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1065. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 87B4h

Figure 2-531. R5SS1_CORE1_AHB_BUS_SAFETY_ERR_STAT_WRITE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS11_AHB_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS11_AHB_BUS_SAFETY_ERR_STAT_WRITE_STAT															
R															
0h															

Access Types Legend

Table 2-1066. R5SS1_CORE1_AHB_BUS_SAFETY_ERR_STAT_WRITE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS11_AHB_BUS_SAFETY_ERR_STAT_WRITE_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.475 CFG0_R5SS1_CORE1_AHB_BUS_SAFETY_ERR_STAT_READ Registers

2.3.475.1 CFG0_CORE1_AHB_BUS_SAFETY_ERR_STAT_READ Register (Offset = 187B8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1067. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 87B8h

Figure 2-532. R5SS1_CORE1_AHB_BUS_SAFETY_ERR_STAT_READ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS11_AHB_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS11_AHB_BUS_SAFETY_ERR_STAT_READ_STAT															
R															
0h															

Access Types Legend

Table 2-1068. R5SS1_CORE1_AHB_BUS_SAFETY_ERR_STAT_READ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS11_AHB_BUS_SAFETY_ERR_STAT_READ_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.476 CFG0_R5SS1_CORE1_AHB_BUS_SAFETY_ERR_STAT_WRITERESP Registers

2.3.476.1 CFG0_CORE1_AHB_BUS_SAFETY_ERR_STAT_WRITERESP Register (Offset = 187BCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1069. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 87BCh

Figure 2-533. R5SS1_CORE1_AHB_BUS_SAFETY_ERR_STAT_WRITERESP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_R5FSS11_AHB_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_R5FSS11_AHB_BUS_SAFETY_ERR_STAT_WRITERESP_STAT															
R															
0h															

Access Types Legend

Table 2-1070. R5SS1_CORE1_AHB_BUS_SAFETY_ERR_STAT_WRITERESP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSS_R5FSS11_AHB_BUS_SAFETY_ERR_STAT_WRITERESP_STAT	R	0h	Reset Source: mod_g_rst_n

2.3.477 CFG0_MSS_VBUSM_SAFETY_H_ERRAGG_MASK0 Registers

2.3.477.1 CFG0_VBUSM_SAFETY_H_ERRAGG_MASK0 Register (Offset = 18834h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1071. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8834h

Figure 2-534. MSS_VBUSM_SAFETY_H_ERRAGG_MASK0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_DTHE_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_MCRC_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_QSPI_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_ICSSM_PDSP1_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_ICSSM_PDSP0_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_HSM_TPTC1_WR_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_HSM_TPTC1_RD_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_HSM_TPTC0_WR_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_HSM_TPTC0_RD_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_TPTC1_WR_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_TPTC0_WR_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_TPTC1_RD_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_TPTC0_RD_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_L2RAM3_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_L2RAM2_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_L2RAM1_VBUSM_ERRH
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_L2RAM0_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_CPSW_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_HSM_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_DAP_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_R5FSS11_SLV_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_R5FSS0_CORE1_SLV_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_R5FSS11_WR_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_R5FSS0_CORE1_WR_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_R5FSS11_RD_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_R5FSS0_CORE1_RD_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_R5FSS1_CORE0_SLV_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_R5FSS0_CORE0_SLV_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_R5FSS1_CORE0_WR_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_R5FSS0_CORE0_WR_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_R5FSS1_CORE0_RD_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_R5FSS0_CORE0_RD_VBUSM_ERRH
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-1072. MSS_VBUSM_SAFETY_H_ERRAGG_MASK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_DTHE_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
30	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_MCRC_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n

Table 2-1072. MSS_VBUSM_SAFETY_H_ERRAGG_MASK0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_QSPI_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
28	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_ICSSM_PDSP1_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
27	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_ICSSM_PDSP0_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
26	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_HSM_TPTC1_WR_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
25	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_HSM_TPTC1_RD_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
24	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_HSM_TPTC0_WR_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
23	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_HSM_TPTC0_RD_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
22	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_TPTC1_WR_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
21	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_TPTC0_WR_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
20	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_TPTC1_RD_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
19	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_TPTC0_RD_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
18	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_L2RAM3_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
17	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_L2RAM2_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
16	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_L2RAM1_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
15	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_L2RAM0_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n

Table 2-1072. MSS_VBUSM_SAFETY_H_ERRAGG_MASK0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_CPSW_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
13	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_HSM_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
12	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_DAP_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
11	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_R5FSS11_SLV_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
10	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_R5FSS0_CORE1_SLV_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
9	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_R5FSS11_WR_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
8	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_R5FSS0_CORE1_WR_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
7	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_R5FSS11_RD_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
6	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_R5FSS0_CORE1_RD_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
5	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_R5FSS1_CORE0_SLV_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
4	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_R5FSS0_CORE0_SLV_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
3	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_R5FSS1_CORE0_WR_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
2	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_R5FSS0_CORE0_WR_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
1	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_R5FSS1_CORE0_RD_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
0	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK_R5FSS0_CORE0_RD_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n

2.3.478 CFG0_MSS_VBUSM_SAFETY_H_ERRAGG_STATUS0 Registers

2.3.478.1 CFG0_VBUSM_SAFETY_H_ERRAGG_STATUS0 Register (Offset = 18838h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1073. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8838h

Figure 2-535. MSS_VBUSM_SAFETY_H_ERRAGG_STATUS0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_DTHE_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_MCRC_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_QSPI_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_ICSSM_PDSP1_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_ICSSM_PDSP0_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_HSM_TPTC1_WR_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_HSM_TPTC1_RD_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_HSM_TPTC0_WR_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_HSM_TPTC0_RD_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_TPTC1_WR_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_TPTC0_WR_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_TPTC1_RD_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_TPTC0_RD_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_L2RAM3_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_L2RAM2_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_L2RAM1_VBUSM_ERRH
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_L2RAM0_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_CPSW_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_HSM_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_DAP_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_R5FSS11_SLV_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_R5FSS0_CORE1_SLV_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_R5FSS11_WR_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_R5FSS0_CORE1_WR_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_R5FSS11_RD_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_R5FSS0_CORE1_RD_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_R5FSS1_CORE0_SLV_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_R5FSS0_CORE0_SLV_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_R5FSS1_CORE0_WR_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_R5FSS0_CORE0_WR_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_R5FSS1_CORE0_RD_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_R5FSS0_CORE0_RD_VBUSM_ERRH
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-1074. MSS_VBUSM_SAFETY_H_ERRAGG_STATUS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_DTHE_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
30	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_MCRC_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n

Table 2-1074. MSS_VBUSM_SAFETY_H_ERRAGG_STATUS0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_QSPI_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
28	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_ICSSM_PDSP1_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
27	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_ICSSM_PDSP0_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
26	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_HSM_TPTC1_WR_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
25	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_HSM_TPTC1_RD_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
24	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_HSM_TPTC0_WR_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
23	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_HSM_TPTC0_RD_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
22	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_TPTC1_WR_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
21	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_TPTC0_WR_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
20	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_TPTC1_RD_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
19	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_TPTC0_RD_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
18	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_L2RAM3_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
17	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_L2RAM2_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
16	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_L2RAM1_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
15	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_L2RAM0_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n

Table 2-1074. MSS_VBUSM_SAFETY_H_ERRAGG_STATUS0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_CPSW_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
13	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_HSM_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
12	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_DAP_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
11	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_R5FSS11_SLV_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
10	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_R5FSS0_CORE1_SLV_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
9	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_R5FSS11_WR_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
8	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_R5FSS0_CORE1_WR_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
7	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_R5FSS11_RD_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
6	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_R5FSS0_CORE1_RD_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
5	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_R5FSS1_CORE0_SLV_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
4	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_R5FSS0_CORE0_SLV_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
3	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_R5FSS1_CORE0_WR_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
2	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_R5FSS0_CORE0_WR_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
1	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_R5FSS1_CORE0_RD_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
0	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_R5FSS0_CORE0_RD_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n

2.3.479 CFG0_MSS_VBUSM_SAFETY_H_ERRAGG_STATUS_RAW0 Registers

2.3.479.1 CFG0_VBUSM_SAFETY_H_ERRAGG_STATUS_RAW0 Register (Offset = 1883Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1075. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 883Ch

Figure 2-536. MSS_VBUSM_SAFETY_H_ERRAGG_STATUS_RAW0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_DTHE_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_MCRC_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_QSPI_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_ICSSM_PDSP1_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_ICSSM_PDSP0_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_HSM_TPTC1_WR_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_HSM_TPTC1_RD_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_HSM_TPTC0_WR_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_HSM_TPTC0_RD_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_TPTC1_WR_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_TPTC0_WR_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_TPTC1_RD_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_TPTC0_RD_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_L2RAM3_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_L2RAM2_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_L2RAM1_VBUSM_ERRH
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_L2RAM0_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_CPSW_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_HSM_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_DAP_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_R5FSS11_SLV_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_R5FSS0_CORE1_SLV_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_R5FSS11_WR_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_R5FSS0_CORE1_WR_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_R5FSS11_RD_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_R5FSS0_CORE1_RD_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_R5FSS1_CORE0_SLV_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_R5FSS0_CORE0_SLV_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_R5FSS1_CORE0_WR_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_R5FSS0_CORE0_WR_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_R5FSS1_CORE0_RD_VBUSM_ERRH	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_R5FSS0_CORE0_RD_VBUSM_ERRH
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-1076. MSS_VBUSM_SAFETY_H_ERRAGG_STATUS_RAW0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_DTHE_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n

Table 2-1076. MSS_VBUSM_SAFETY_H_ERRAGG_STATUS_RAW0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_MCRC_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
29	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_QSPI_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
28	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_ICSSM_PDSP1_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
27	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_ICSSM_PDSP0_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
26	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_HSM_TPTC1_WR_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
25	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_HSM_TPTC1_RD_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
24	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_HSM_TPTC0_WR_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
23	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_HSM_TPTC0_RD_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
22	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_TPTC1_WR_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
21	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_TPTC0_WR_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
20	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_TPTC1_RD_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
19	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_TPTC0_RD_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
18	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_L2RAM3_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
17	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_L2RAM2_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
16	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_L2RAM1_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n

Table 2-1076. MSS_VBUSM_SAFETY_H_ERRAGG_STATUS_RAW0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_L2RAM0_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
14	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_CPSW_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
13	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_HSM_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
12	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_DAP_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
11	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_R5FSS11_SLV_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
10	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_R5FSS0_CORE1_SLV_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
9	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_R5FSS11_WR_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
8	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_R5FSS0_CORE1_WR_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
7	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_R5FSS11_RD_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
6	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_R5FSS0_CORE1_RD_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
5	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_R5FSS1_CORE0_SLV_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
4	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_R5FSS0_CORE0_SLV_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
3	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_R5FSS1_CORE0_WR_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
2	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_R5FSS0_CORE0_WR_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
1	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_R5FSS1_CORE0_RD_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n

Table 2-1076. MSS_VBUSM_SAFETY_H_ERRAGG_STATUS_RAW0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW_R5FSS0_CORE0_RD_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n

2.3.480 CFG0_MSS_VBUSM_SAFETY_H_ERRAGG_MASK1 Registers

2.3.480.1 CFG0_VBUSM_SAFETY_H_ERRAGG_MASK1 Register (Offset = 18844h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1077. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8844h

Figure 2-537. MSS_VBUSM_SAFETY_H_ERRAGG_MASK1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MSS_VBUSM_SAFETY_H1_ERRAGG_MASK_GPMC_VBUSM_ERRH	MSS_VBUSM_SAFETY_H1_ERRAGG_MASK_MMC_VBUSM_ERRH	MSS_VBUSM_SAFETY_H1_ERRAGG_MASK_STM_STIM_VBUSM_ERRH	MSS_VBUSM_SAFETY_H1_ERRAGG_MASK_MSS_MBOX_VBUSM_ERRH	MSS_VBUSM_SAFETY_H1_ERRAGG_MASK_ICSSMSLAVE_VBUSM_ERRH	MSS_VBUSM_SAFETY_H1_ERRAGG_MASK_HSM_S_VBUSM_ERRH	MSS_VBUSM_SAFETY_H1_ERRAGG_MASK_SCRM2SCRP_1_VBUSM_ERRH	MSS_VBUSM_SAFETY_H1_ERRAGG_MASK_SCRM2SCRP_0_VBUSM_ERRH
NONE								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-1078. MSS_VBUSM_SAFETY_H_ERRAGG_MASK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7	MSS_VBUSM_SAFETY_H1_ERRAGG_MASK_GPMC_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H1_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H1_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
6	MSS_VBUSM_SAFETY_H1_ERRAGG_MASK_MMC_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H1_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H1_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
5	MSS_VBUSM_SAFETY_H1_ERRAGG_MASK_STM_STIM_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H1_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H1_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
4	MSS_VBUSM_SAFETY_H1_ERRAGG_MASK_MSS_MBOX_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H1_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H1_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
3	MSS_VBUSM_SAFETY_H1_ERRAGG_MASK_ICSSMSLAVE_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H1_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H1_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n

Table 2-1078. MSS_VBUSM_SAFETY_H_ERRAGG_MASK1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	MSS_VBUSM_SAFETY_H1_ERRAGG_MASK_HSM_S_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H1_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H1_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
1	MSS_VBUSM_SAFETY_H1_ERRAGG_MASK_SCRM2SCRP_1_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H1_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H1_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
0	MSS_VBUSM_SAFETY_H1_ERRAGG_MASK_SCRM2SCRP_0_VBUSM_ERRH	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_H1_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_H1_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n

2.3.481 CFG0_MSS_VBUSM_SAFETY_H_ERRAGG_STATUS1 Registers

2.3.481.1 CFG0_VBUSM_SAFETY_H_ERRAGG_STATUS1 Register (Offset = 18848h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1079. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8848h

Figure 2-538. MSS_VBUSM_SAFETY_H_ERRAGG_STATUS1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS_GPMC_VBUSM_ERRH	MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS_MMC_VBUSM_ERRH	MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS_STM_STIM_VBUSM_ERRH	MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS_MSS_MBOX_VBUSM_ERRH	MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS_ICSSMSLAVE_VBUSM_ERRH	MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS_HSM_S_VBUSM_ERRH	MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS_SCRM2SCRP_1_VBUSM_ERRH	MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS_SCRM2SCRP_0_VBUSM_ERRH
NONE								R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-1080. MSS_VBUSM_SAFETY_H_ERRAGG_STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7	MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS_GPMC_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H1_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H1_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
6	MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS_MMC_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H1_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H1_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
5	MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS_STM_STIM_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H1_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H1_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
4	MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS_MSS_MBOX_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H1_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H1_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n

Table 2-1080. MSS_VBUSM_SAFETY_H_ERRAGG_STATUS1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS_ICSSMSLAVE_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H1_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H1_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
2	MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS_HSM_S_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H1_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H1_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
1	MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS_SCRM2SCRP_1_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H1_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H1_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
0	MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS_SCRM2SCRP_0_VBUSM_ERRH	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_H1_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_H1_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n

2.3.482 CFG0_MSS_VBUSM_SAFETY_H_ERRAGG_STATUS_RAW1 Registers

2.3.482.1 CFG0_VBUSM_SAFETY_H_ERRAGG_STATUS_RAW1 Register (Offset = 1884Ch) [reset = 0h]

Short Description:

Long Description:

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Table 2-1081. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 884Ch

Figure 2-539. MSS_VBUSM_SAFETY_H_ERRAGG_STATUS_RAW1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS_RAW_GPMC_VBUSM_ERRH	MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS_RAW_MMC_VBUSM_ERRH	MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS_RAW_STM_STIM_VBUSM_ERRH	MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS_RAW_MSS_MBOX_VBUSM_ERRH	MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS_RAW_ICSSMSLAVE_VBUSM_ERRH	MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS_RAW_HSM_S_VBUSM_ERRH	MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS_RAW_SCRM2SCRP_1_VBUSM_ERRH	MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS_RAW_SCRM2SCRP_0_VBUSM_ERRH
NONE								R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-1082. MSS_VBUSM_SAFETY_H_ERRAGG_STATUS_RAW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7	MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS_RAW_GPMC_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H1_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H1_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
6	MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS_RAW_MMC_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H1_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H1_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
5	MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS_RAW_STM_STIM_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H1_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H1_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
4	MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS_RAW_MSS_MBOX_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H1_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H1_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n

Table 2-1082. MSS_VBUSM_SAFETY_H_ERRAGG_STATUS_RAW1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS_RAW_ICSSMSLAVE_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H1_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H1_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
2	MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS_RAW_HSM_S_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H1_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H1_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
1	MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS_RAW_SCRM2SCRP_1_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H1_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H1_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
0	MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS_RAW_SCRM2SCRP_0_VBUSM_ERRH	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_H1_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_H1_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n

2.3.483 CFG0_MSS_VBUSM_SAFETY_L_ERRAGG_MASK0 Registers

2.3.483.1 CFG0_VBUSM_SAFETY_L_ERRAGG_MASK0 Register (Offset = 18854h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1083. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8854h

Figure 2-540. MSS_VBUSM_SAFETY_L_ERRAGG_MASK0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_DTHE_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_MCRC_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_QSPI_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_ICSSM_PDSP1_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_ICSSM_PDSP0_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_HSM_TPTC1_WR_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_HSM_TPTC1_RD_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_HSM_TPTC0_WR_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_HSM_TPTC0_RD_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_TPTC1_WR_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_TPTC0_WR_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_TPTC1_RD_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_TPTC0_RD_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_L2RAM3_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_L2RAM2_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_L2RAM1_VBUSM_ERRL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_L2RAM0_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_CPSW_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_HSM_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_DAP_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_R5FSS11_SLV_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_R5FSS0_CORE1_SLV_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_R5FSS11_WR_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_R5FSS0_CORE1_WR_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_R5FSS11_RD_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_R5FSS0_CORE1_RD_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_R5FSS1_CORE0_SLV_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_R5FSS0_CORE0_SLV_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_R5FSS1_CORE0_WR_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_R5FSS0_CORE0_WR_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_R5FSS1_CORE0_RD_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_R5FSS0_CORE0_RD_VBUSM_ERRL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-1084. MSS_VBUSM_SAFETY_L_ERRAGG_MASK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_DTHE_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
30	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_MCRC_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n

Table 2-1084. MSS_VBUSM_SAFETY_L_ERRAGG_MASK0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_QSPI_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
28	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_ICSSM_PDSP1_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
27	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_ICSSM_PDSP0_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
26	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_HSM_TPTC1_WR_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
25	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_HSM_TPTC1_RD_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
24	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_HSM_TPTC0_WR_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
23	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_HSM_TPTC0_RD_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
22	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_TPTC1_WR_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
21	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_TPTC0_WR_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
20	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_TPTC1_RD_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
19	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_TPTC0_RD_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
18	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_L2RAM3_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
17	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_L2RAM2_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
16	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_L2RAM1_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
15	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_L2RAM0_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n

Table 2-1084. MSS_VBUSM_SAFETY_L_ERRAGG_MASK0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_CPSW_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
13	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_HSM_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
12	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_DAP_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
11	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_R5FSS11_SLV_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
10	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_R5FSS0_CORE1_SLV_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
9	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_R5FSS11_WR_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
8	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_R5FSS0_CORE1_WR_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
7	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_R5FSS11_RD_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
6	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_R5FSS0_CORE1_RD_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
5	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_R5FSS1_CORE0_SLV_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
4	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_R5FSS0_CORE0_SLV_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
3	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_R5FSS1_CORE0_WR_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
2	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_R5FSS0_CORE0_WR_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
1	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_R5FSS1_CORE0_RD_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
0	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK_R5FSS0_CORE0_RD_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L0_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n

2.3.484 CFG0_MSS_VBUSM_SAFETY_L_ERRAGG_STATUS0 Registers

2.3.484.1 CFG0_VBUSM_SAFETY_L_ERRAGG_STATUS0 Register (Offset = 18858h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1085. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8858h

Figure 2-541. MSS_VBUSM_SAFETY_L_ERRAGG_STATUS0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_DTHE_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_MCRC_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_QSPI_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_ICSSM_PDSP1_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_ICSSM_PDSP0_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_HSM_TPTC1_WR_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_HSM_TPTC1_RD_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_HSM_TPTC0_WR_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_HSM_TPTC0_RD_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_TPTC1_WR_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_TPTC0_WR_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_TPTC1_RD_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_TPTC0_RD_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_L2RAM3_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_L2RAM2_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_L2RAM1_VBUSM_ERRL
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_L2RAM0_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_CPSW_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_HSM_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_DAP_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_R5FSS11_SLV_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_R5FSS0_CORE1_SLV_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_R5FSS11_WR_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_R5FSS0_CORE1_WR_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_R5FSS11_RD_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_R5FSS0_CORE1_RD_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_R5FSS1_CORE0_SLV_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_R5FSS0_CORE0_SLV_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_R5FSS1_CORE0_WR_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_R5FSS0_CORE0_WR_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_R5FSS1_CORE0_RD_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_R5FSS0_CORE0_RD_VBUSM_ERRL
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-1086. MSS_VBUSM_SAFETY_L_ERRAGG_STATUS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_DTHE_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
30	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_MCRC_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n

Table 2-1086. MSS_VBUSM_SAFETY_L_ERRAGG_STATUS0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_QSPI_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
28	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_ICSSM_PDSP1_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
27	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_ICSSM_PDSP0_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
26	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_HSM_TPTC1_WR_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
25	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_HSM_TPTC1_RD_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
24	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_HSM_TPTC0_WR_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
23	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_HSM_TPTC0_RD_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
22	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_TPTC1_WR_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
21	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_TPTC0_WR_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
20	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_TPTC1_RD_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
19	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_TPTC0_RD_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
18	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_L2RAM3_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
17	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_L2RAM2_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
16	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_L2RAM1_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
15	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_L2RAM0_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n

Table 2-1086. MSS_VBUSM_SAFETY_L_ERRAGG_STATUS0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_CPSW_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
13	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_HSM_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
12	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_DAP_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
11	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_R5FSS11_SLV_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
10	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_R5FSS0_CORE1_SLV_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
9	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_R5FSS11_WR_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
8	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_R5FSS0_CORE1_WR_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
7	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_R5FSS11_RD_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
6	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_R5FSS0_CORE1_RD_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
5	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_R5FSS1_CORE0_SLV_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
4	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_R5FSS0_CORE0_SLV_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
3	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_R5FSS1_CORE0_WR_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
2	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_R5FSS0_CORE0_WR_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
1	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_R5FSS1_CORE0_RD_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
0	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_R5FSS0_CORE0_RD_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n

2.3.485 CFG0_MSS_VBUSM_SAFETY_L_ERRAGG_STATUS_RAW0 Registers

2.3.485.1 CFG0_VBUSM_SAFETY_L_ERRAGG_STATUS_RAW0 Register (Offset = 1885Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1087. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 885Ch

Figure 2-542. MSS_VBUSM_SAFETY_L_ERRAGG_STATUS_RAW0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_DTHE_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_MCRC_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_QSPI_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_ICSSM_PDSP1_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_ICSSM_PDSP0_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_HSM_TPTC1_WR_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_HSM_TPTC1_RD_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_HSM_TPTC0_WR_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_HSM_TPTC0_RD_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_TPTC1_WR_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_TPTC0_WR_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_TPTC1_RD_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_TPTC0_RD_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_L2RAM3_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_L2RAM2_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_L2RAM1_VBUSM_ERRL
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_L2RAM0_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_CPSW_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_HSM_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_DAP_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_R5FSS11_SLV_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_R5FSS0_CORE1_SLV_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_R5FSS11_WR_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_R5FSS0_CORE1_WR_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_R5FSS11_RD_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_R5FSS0_CORE1_RD_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_R5FSS1_CORE0_SLV_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_R5FSS0_CORE0_SLV_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_R5FSS1_CORE0_WR_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_R5FSS0_CORE0_WR_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_R5FSS1_CORE0_RD_VBUSM_ERRL	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_R5FSS0_CORE0_RD_VBUSM_ERRL
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-1088. MSS_VBUSM_SAFETY_L_ERRAGG_STATUS_RAW0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_DTHE_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n

Table 2-1088. MSS_VBUSM_SAFETY_L_ERRAGG_STATUS_RAW0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_MCRC_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
29	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_QSPI_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
28	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_ICSSM_PDSP1_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
27	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_ICSSM_PDSP0_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
26	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_HSM_TPTC1_WR_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
25	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_HSM_TPTC1_RD_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
24	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_HSM_TPTC0_WR_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
23	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_HSM_TPTC0_RD_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
22	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_TPTC1_WR_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
21	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_TPTC0_WR_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
20	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_TPTC1_RD_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
19	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_TPTC0_RD_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
18	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_L2RAM3_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
17	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_L2RAM2_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
16	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_L2RAM1_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n

Table 2-1088. MSS_VBUSM_SAFETY_L_ERRAGG_STATUS_RAW0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_L2RAM0_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
14	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_CPSW_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
13	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_HSM_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
12	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_DAP_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
11	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_R5FSS11_SLV_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
10	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_R5FSS0_CORE1_SLV_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
9	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_R5FSS11_WR_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
8	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_R5FSS0_CORE1_WR_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
7	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_R5FSS11_RD_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
6	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_R5FSS0_CORE1_RD_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
5	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_R5FSS1_CORE0_SLV_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
4	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_R5FSS0_CORE0_SLV_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
3	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_R5FSS1_CORE0_WR_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
2	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_R5FSS0_CORE0_WR_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
1	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_R5FSS1_CORE0_RD_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n

Table 2-1088. MSS_VBUSM_SAFETY_L_ERRAGG_STATUS_RAW0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW_R5FSS0_CORE0_RD_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L0_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L0_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n

2.3.486 CFG0_MSS_VBUSM_SAFETY_L_ERRAGG_MASK1 Registers

2.3.486.1 CFG0_VBUSM_SAFETY_L_ERRAGG_MASK1 Register (Offset = 18864h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1089. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8864h

Figure 2-543. MSS_VBUSM_SAFETY_L_ERRAGG_MASK1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MSS_VBUSM_SAFETY_L1_ERRAGG_MASK_GPMC_VBUSM_ERRL	MSS_VBUSM_SAFETY_L1_ERRAGG_MASK_MMC_VBUSM_ERRL	MSS_VBUSM_SAFETY_L1_ERRAGG_MASK_STM_STIM_VBUSM_ERRL	MSS_VBUSM_SAFETY_L1_ERRAGG_MASK_MSS_MBOX_VBUSM_ERRL	MSS_VBUSM_SAFETY_L1_ERRAGG_MASK_ICSSMSLAVE_VBUSM_ERRL	MSS_VBUSM_SAFETY_L1_ERRAGG_MASK_HSM_S_VBUSM_ERRL	MSS_VBUSM_SAFETY_L1_ERRAGG_MASK_SCRM2SCRP_1_VBUSM_ERRL	MSS_VBUSM_SAFETY_L1_ERRAGG_MASK_SCRM2SCRP_0_VBUSM_ERRL
NONE								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-1090. MSS_VBUSM_SAFETY_L_ERRAGG_MASK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7	MSS_VBUSM_SAFETY_L1_ERRAGG_MASK_GPMC_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L1_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L1_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
6	MSS_VBUSM_SAFETY_L1_ERRAGG_MASK_MMC_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L1_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L1_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
5	MSS_VBUSM_SAFETY_L1_ERRAGG_MASK_STM_STIM_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L1_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L1_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
4	MSS_VBUSM_SAFETY_L1_ERRAGG_MASK_MSS_MBOX_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L1_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L1_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
3	MSS_VBUSM_SAFETY_L1_ERRAGG_MASK_ICSSMSLAVE_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L1_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L1_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n

Table 2-1090. MSS_VBUSM_SAFETY_L_ERRAGG_MASK1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	MSS_VBUSM_SAFETY_L1_ERRAGG_MASK_HSM_S_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L1_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L1_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
1	MSS_VBUSM_SAFETY_L1_ERRAGG_MASK_SCRM2SCRP_1_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L1_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L1_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n
0	MSS_VBUSM_SAFETY_L1_ERRAGG_MASK_SCRM2SCRP_0_VBUSM_ERRL	R/W	0h	Mask Error from MSS_VBUSM_SAFETY_L1_ERRAGG to aggregated Error MSS_VBUSM_SAFETY_L1_ERRAGG_ERRAGG 1 : Error is Masked 0 : Error is Unmasked Reset Source: mod_g_rst_n

2.3.487 CFG0_MSS_VBUSM_SAFETY_L_ERRAGG_STATUS1 Registers

2.3.487.1 CFG0_VBUSM_SAFETY_L_ERRAGG_STATUS1 Register (Offset = 18868h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1091. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 8868h

Figure 2-544. MSS_VBUSM_SAFETY_L_ERRAGG_STATUS1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS_GPMC_VBUSM_ERRL	MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS_MMC_VBUSM_ERRL	MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS_STM_STIM_VBUSM_ERRL	MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS_MSS_MBOX_VBUSM_ERRL	MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS_ICSSMSLAVE_VBUSM_ERRL	MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS_HSM_S_VBUSM_ERRL	MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS_SCRM2SCRP_1_VBUSM_ERRL	MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS_SCRM2SCRP_0_VBUSM_ERRL
NONE								R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-1092. MSS_VBUSM_SAFETY_L_ERRAGG_STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7	MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS_GPMC_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L1_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L1_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
6	MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS_MMC_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L1_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L1_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
5	MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS_STM_STIM_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L1_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L1_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
4	MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS_MSS_MBOX_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L1_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L1_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n

Table 2-1092. MSS_VBUSM_SAFETY_L_ERRAGG_STATUS1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS_ICSSMSLAVE_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L1_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L1_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
2	MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS_HSM_S_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L1_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L1_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
1	MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS_SCRM2SCRP_1_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L1_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L1_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n
0	MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS_SCRM2SCRP_0_VBUSM_ERRL	R/W1TC	0h	Status of Error from MSS_VBUSM_SAFETY_L1_ERRAGG. Set only if Interupt is unmasked in MSS_VBUSM_SAFETY_L1_ERRAGG_ERRAGG_MASK Wrie 0x1 to clear this Error. Reset Source: mod_g_rst_n

2.3.488 CFG0_MSS_VBUSM_SAFETY_L_ERRAGG_STATUS_RAW1 Registers

2.3.488.1 CFG0_VBUSM_SAFETY_L_ERRAGG_STATUS_RAW1 Register (Offset = 1886Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1093. Instance Table

Instance Name	Physical Address
MSS_CTRL_MMR	50D1 886Ch

Figure 2-545. MSS_VBUSM_SAFETY_L_ERRAGG_STATUS_RAW1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS_RAW_GPMC_VBUSM_ERRL	MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS_RAW_MMC_VBUSM_ERRL	MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS_RAW_STM_STIM_VBUSM_ERRL	MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS_RAW_MSS_MBOX_VBUSM_ERRL	MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS_RAW_ICSSMSLAVE_VBUSM_ERRL	MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS_RAW_HSM_S_VBUSM_ERRL	MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS_RAW_SCRM2SCRP_1_VBUSM_ERRL	MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS_RAW_SCRM2SCRP_0_VBUSM_ERRL
NONE								R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-1094. MSS_VBUSM_SAFETY_L_ERRAGG_STATUS_RAW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7	MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS_RAW_GPMC_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L1_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L1_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
6	MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS_RAW_MMC_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L1_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L1_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
5	MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS_RAW_STM_STIM_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L1_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L1_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
4	MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS_RAW_MSS_MBOX_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L1_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L1_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n

Table 2-1094. MSS_VBUSM_SAFETY_L_ERRAGG_STATUS_RAW1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS_RAW_ICSSMSLAVE_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L1_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L1_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
2	MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS_RAW_HSM_S_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L1_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L1_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
1	MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS_RAW_SCRM2SCRP_1_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L1_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L1_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n
0	MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS_RAW_SCRM2SCRP_0_VBUSM_ERRL	R/W1TC	0h	Raw Status of Error from MSS_VBUSM_SAFETY_L1_ERRAGG. Set irrespective if the Interupt is masked or unmasked in MSS_VBUSM_SAFETY_L1_ERRAGG_ERRAGG_MASK Reset Source: mod_g_rst_n

2.3.489 Access Table

Table 2-1095. Access Type Codes

Access Type	Code	Description
R	R	Read
R/W	R/W	Read / Write
R/W1TC	R/W1TC	Read/Write 1 To Clear
R/W1TS	R/W1TS	Read/Write 1 To Set
W	W	Write

2.4 MSS_IOMUX Registers

Table 2-1096. MEM, MEM Registers, Base Address=0X0000000053100000, Length=4096

Offset	Length	Register Name	MSS_IOMUX Physical Address
0h	32	QSPI0_CSn0_CFG_REG	5310 0000h
4h	32	QSPI0_CSn1_CFG_REG	5310 0004h
8h	32	QSPI0_CLK_CFG_REG	5310 0008h
Ch	32	QSPI0_D0_CFG_REG	5310 000Ch
10h	32	QSPI0_D1_CFG_REG	5310 0010h
14h	32	QSPI0_D2_CFG_REG	5310 0014h
18h	32	QSPI0_D3_CFG_REG	5310 0018h
1Ch	32	MCAN0_RX_CFG_REG	5310 001Ch
20h	32	MCAN0_TX_CFG_REG	5310 0020h
24h	32	MCAN1_RX_CFG_REG	5310 0024h
28h	32	MCAN1_TX_CFG_REG	5310 0028h
2Ch	32	SPI0_CS0_CFG_REG	5310 002Ch
30h	32	SPI0_CLK_CFG_REG	5310 0030h
34h	32	SPI0_D0_CFG_REG	5310 0034h
38h	32	SPI0_D1_CFG_REG	5310 0038h
3Ch	32	SPI1_CS0_CFG_REG	5310 003Ch
40h	32	SPI1_CLK_CFG_REG	5310 0040h
44h	32	SPI1_D0_CFG_REG	5310 0044h
48h	32	SPI1_D1_CFG_REG	5310 0048h
4Ch	32	LIN1_RXD_CFG_REG	5310 004Ch
50h	32	LIN1_TXD_CFG_REG	5310 0050h
54h	32	LIN2_RXD_CFG_REG	5310 0054h
58h	32	LIN2_TXD_CFG_REG	5310 0058h
5Ch	32	I2C1_SCL_CFG_REG	5310 005Ch
60h	32	I2C1_SDA_CFG_REG	5310 0060h
64h	32	UART0_RTSn_CFG_REG	5310 0064h
68h	32	UART0_CTSn_CFG_REG	5310 0068h
6Ch	32	UART0_RXD_CFG_REG	5310 006Ch
70h	32	UART0_TXD_CFG_REG	5310 0070h
74h	32	RGMII1_RXC_CFG_REG	5310 0074h
78h	32	RGMII1_RX_CTL_CFG_REG	5310 0078h
7Ch	32	RGMII1_RD0_CFG_REG	5310 007Ch
80h	32	RGMII1_RD1_CFG_REG	5310 0080h
84h	32	RGMII1_RD2_CFG_REG	5310 0084h
88h	32	RGMII1_RD3_CFG_REG	5310 0088h
8Ch	32	RGMII1_TXC_CFG_REG	5310 008Ch
90h	32	RGMII1_TX_CTL_CFG_REG	5310 0090h
94h	32	RGMII1_TD0_CFG_REG	5310 0094h
98h	32	RGMII1_TD1_CFG_REG	5310 0098h
9Ch	32	RGMII1_TD2_CFG_REG	5310 009Ch
A0h	32	RGMII1_TD3_CFG_REG	5310 00A0h
A4h	32	MDIO0_MDIO_CFG_REG	5310 00A4h
A8h	32	MDIO0_MDC_CFG_REG	5310 00A8h
ACh	32	EPWM0_A_CFG_REG	5310 00ACh
B0h	32	EPWM0_B_CFG_REG	5310 00B0h

Table 2-1096. MEM, MEM Registers, Base Address=0X0000000053100000, Length=4096 (continued)

Offset	Length	Register Name	MSS_IOMUX Physical Address
B4h	32	EPWM1_A_CFG_REG	5310 00B4h
B8h	32	EPWM1_B_CFG_REG	5310 00B8h
BCh	32	EPWM2_A_CFG_REG	5310 00BCh
C0h	32	EPWM2_B_CFG_REG	5310 00C0h
C4h	32	EPWM3_A_CFG_REG	5310 00C4h
C8h	32	EPWM3_B_CFG_REG	5310 00C8h
CCh	32	EPWM4_A_CFG_REG	5310 00CCh
D0h	32	EPWM4_B_CFG_REG	5310 00D0h
D4h	32	EPWM5_A_CFG_REG	5310 00D4h
D8h	32	EPWM5_B_CFG_REG	5310 00D8h
DCh	32	EPWM6_A_CFG_REG	5310 00DCh
E0h	32	EPWM6_B_CFG_REG	5310 00E0h
E4h	32	EPWM7_A_CFG_REG	5310 00E4h
E8h	32	EPWM7_B_CFG_REG	5310 00E8h
ECh	32	EPWM8_A_CFG_REG	5310 00ECh
F0h	32	EPWM8_B_CFG_REG	5310 00F0h
F4h	32	EPWM9_A_CFG_REG	5310 00F4h
F8h	32	EPWM9_B_CFG_REG	5310 00F8h
FCh	32	EPWM10_A_CFG_REG	5310 00FCh
100h	32	EPWM10_B_CFG_REG	5310 0100h
104h	32	EPWM11_A_CFG_REG	5310 0104h
108h	32	EPWM11_B_CFG_REG	5310 0108h
10Ch	32	EPWM12_A_CFG_REG	5310 010Ch
110h	32	EPWM12_B_CFG_REG	5310 0110h
114h	32	EPWM13_A_CFG_REG	5310 0114h
118h	32	EPWM13_B_CFG_REG	5310 0118h
11Ch	32	EPWM14_A_CFG_REG	5310 011Ch
120h	32	EPWM14_B_CFG_REG	5310 0120h
124h	32	EPWM15_A_CFG_REG	5310 0124h
128h	32	EPWM15_B_CFG_REG	5310 0128h
12Ch	32	UART1_RXD_CFG_REG	5310 012Ch
130h	32	UART1_TXD_CFG_REG	5310 0130h
134h	32	MMC0_CLK_CFG_REG	5310 0134h
138h	32	MMC0_CMD_CFG_REG	5310 0138h
13Ch	32	MMC0_D0_CFG_REG	5310 013Ch
140h	32	MMC0_D1_CFG_REG	5310 0140h
144h	32	MMC0_D2_CFG_REG	5310 0144h
148h	32	MMC0_D3_CFG_REG	5310 0148h
14Ch	32	MMC0_WP_CFG_REG	5310 014Ch
150h	32	MMC0_CD_CFG_REG	5310 0150h
154h	32	PR0_MDIO0_MDIO_CFG_REG	5310 0154h
158h	32	PR0_MDIO0_MDC_CFG_REG	5310 0158h
15Ch	32	PR0_PRU0_GPO5_CFG_REG	5310 015Ch
160h	32	PR0_PRU0_GPO9_CFG_REG	5310 0160h
164h	32	PR0_PRU0_GPO10_CFG_REG	5310 0164h
168h	32	PR0_PRU0_GPO8_CFG_REG	5310 0168h
16Ch	32	PR0_PRU0_GPO6_CFG_REG	5310 016Ch

Table 2-1096. MEM, MEM Registers, Base Address=0X0000000053100000, Length=4096 (continued)

Offset	Length	Register Name	MSS_IOMUX Physical Address
170h	32	PR0_PRU0_GPO4_CFG_REG	5310 0170h
174h	32	PR0_PRU0_GPO0_CFG_REG	5310 0174h
178h	32	PR0_PRU0_GPO1_CFG_REG	5310 0178h
17Ch	32	PR0_PRU0_GPO2_CFG_REG	5310 017Ch
180h	32	PR0_PRU0_GPO3_CFG_REG	5310 0180h
184h	32	PR0_PRU0_GPO16_CFG_REG	5310 0184h
188h	32	PR0_PRU0_GPO15_CFG_REG	5310 0188h
18Ch	32	PR0_PRU0_GPO11_CFG_REG	5310 018Ch
190h	32	PR0_PRU0_GPO12_CFG_REG	5310 0190h
194h	32	PR0_PRU0_GPO13_CFG_REG	5310 0194h
198h	32	PR0_PRU0_GPO14_CFG_REG	5310 0198h
19Ch	32	PR0_PRU1_GPO5_CFG_REG	5310 019Ch
1A0h	32	PR0_PRU1_GPO9_CFG_REG	5310 01A0h
1A4h	32	PR0_PRU1_GPO10_CFG_REG	5310 01A4h
1A8h	32	PR0_PRU1_GPO8_CFG_REG	5310 01A8h
1ACh	32	PR0_PRU1_GPO6_CFG_REG	5310 01ACh
1B0h	32	PR0_PRU1_GPO4_CFG_REG	5310 01B0h
1B4h	32	PR0_PRU1_GPO0_CFG_REG	5310 01B4h
1B8h	32	PR0_PRU1_GPO1_CFG_REG	5310 01B8h
1BCh	32	PR0_PRU1_GPO2_CFG_REG	5310 01BCh
1C0h	32	PR0_PRU1_GPO3_CFG_REG	5310 01C0h
1C4h	32	PR0_PRU1_GPO16_CFG_REG	5310 01C4h
1C8h	32	PR0_PRU1_GPO15_CFG_REG	5310 01C8h
1CCh	32	PR0_PRU1_GPO11_CFG_REG	5310 01CCh
1D0h	32	PR0_PRU1_GPO12_CFG_REG	5310 01D0h
1D4h	32	PR0_PRU1_GPO13_CFG_REG	5310 01D4h
1D8h	32	PR0_PRU1_GPO14_CFG_REG	5310 01D8h
1DCh	32	PR0_PRU1_GPO19_CFG_REG	5310 01DCh
1E0h	32	PR0_PRU1_GPO18_CFG_REG	5310 01E0h
1E4h	32	EXT_REFCLK0_CFG_REG	5310 01E4h
1E8h	32	SDFM0_CLK0_CFG_REG	5310 01E8h
1ECh	32	SDFM0_D0_CFG_REG	5310 01ECh
1F0h	32	SDFM0_CLK1_CFG_REG	5310 01F0h
1F4h	32	SDFM0_D1_CFG_REG	5310 01F4h
1F8h	32	SDFM0_CLK2_CFG_REG	5310 01F8h
1FCh	32	SDFM0_D2_CFG_REG	5310 01FCh
200h	32	SDFM0_CLK3_CFG_REG	5310 0200h
204h	32	SDFM0_D3_CFG_REG	5310 0204h
208h	32	EQEP0_A_CFG_REG	5310 0208h
20Ch	32	EQEP0_B_CFG_REG	5310 020Ch
210h	32	EQEP0_STROBE_CFG_REG	5310 0210h
214h	32	EQEP0_INDEX_CFG_REG	5310 0214h
218h	32	I2C0_SDA_CFG_REG	5310 0218h
21Ch	32	I2C0_SCL_CFG_REG	5310 021Ch
220h	32	MCAN2_TX_CFG_REG	5310 0220h
224h	32	MCAN2_RX_CFG_REG	5310 0224h
228h	32	CLKOUT0_CFG_REG	5310 0228h

Table 2-1096. MEM, MEM Registers, Base Address=0X0000000053100000, Length=4096 (continued)

Offset	Length	Register Name	MSS_IOMUX Physical Address
22Ch	32	WARMRSTn_CFG_REG	5310 022Ch
230h	32	SAFETY_ERRORn_CFG_REG	5310 0230h
234h	32	TDI_CFG_REG	5310 0234h
238h	32	TDO_CFG_REG	5310 0238h
23Ch	32	TMS_CFG_REG	5310 023Ch
240h	32	TCK_CFG_REG	5310 0240h
244h	32	QSPI0_CLKLB_CFG_REG	5310 0244h
248h	32	QUAL_GRP_0_CFG_REG	5310 0248h
24Ch	32	QUAL_GRP_1_CFG_REG	5310 024Ch
250h	32	QUAL_GRP_2_CFG_REG	5310 0250h
254h	32	QUAL_GRP_3_CFG_REG	5310 0254h
258h	32	QUAL_GRP_4_CFG_REG	5310 0258h
25Ch	32	QUAL_GRP_5_CFG_REG	5310 025Ch
260h	32	QUAL_GRP_6_CFG_REG	5310 0260h
264h	32	QUAL_GRP_7_CFG_REG	5310 0264h
268h	32	QUAL_GRP_8_CFG_REG	5310 0268h
26Ch	32	QUAL_GRP_9_CFG_REG	5310 026Ch
270h	32	QUAL_GRP_10_CFG_REG	5310 0270h
274h	32	QUAL_GRP_11_CFG_REG	5310 0274h
278h	32	QUAL_GRP_12_CFG_REG	5310 0278h
27Ch	32	QUAL_GRP_13_CFG_REG	5310 027Ch
280h	32	QUAL_GRP_14_CFG_REG	5310 0280h
284h	32	QUAL_GRP_15_CFG_REG	5310 0284h
288h	32	QUAL_GRP_16_CFG_REG	5310 0288h
28Ch	32	QUAL_GRP_17_CFG_REG	5310 028Ch
290h	32	USER_MODE_EN	5310 0290h
294h	32	PADGLBL_CFG_REG	5310 0294h
298h	32	IO_CFG_KICK0	5310 0298h
29Ch	32	IO_CFG_KICK1	5310 029Ch

2.4.1 MEM_QSPI0_CSN0_CFG_REG Registers

2.4.1.1 MEM_CSN0_CFG_REG Register (Offset = 0h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1097. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0000h

Figure 2-546. QSPI0_CSN0_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1098. QSPI0_CSN0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.2 MEM_QSPI0_CSN1_CFG_REG Registers

2.4.2.1 MEM_CSN1_CFG_REG Register (Offset = 4h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1099. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0004h

Figure 2-547. QSPI0_CSN1_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1100. QSPI0_CSN1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.3 MEM_QSPI0_CLK_CFG_REG Registers

2.4.3.1 MEM_CLK_CFG_REG Register (Offset = 8h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1101. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0008h

Figure 2-548. QSPI0_CLK_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1102. QSPI0_CLK_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.4 MEM_QSPI0_D0_CFG_REG Registers

2.4.4.1 MEM_D0_CFG_REG Register (Offset = Ch) [reset = 5d7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1103. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 000Ch

Figure 2-549. QSPI0_D0_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4822									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	0h	1h	7h			

Access Types Legend

Table 2-1104. QSPI0_D0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	0h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.5 MEM_QSPI0_D1_CFG_REG Registers

2.4.5.1 MEM_D1_CFG_REG Register (Offset = 10h) [reset = 5d7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1105. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0010h

Figure 2-550. QSPI0_D1_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4822									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	0h	1h	7h			

Access Types Legend

Table 2-1106. QSPI0_D1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	0h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.6 MEM_QSPI0_D2_CFG_REG Registers

2.4.6.1 MEM_D2_CFG_REG Register (Offset = 14h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1107. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0014h

Figure 2-551. QSPI0_D2_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1108. QSPI0_D2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.7 MEM_QSPI0_D3_CFG_REG Registers

2.4.7.1 MEM_D3_CFG_REG Register (Offset = 18h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1109. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0018h

Figure 2-552. QSPI0_D3_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1110. QSPI0_D3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.8 MEM_MCAN0_RX_CFG_REG Registers

2.4.8.1 MEM_RX_CFG_REG Register (Offset = 1Ch) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1111. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 001Ch

Figure 2-553. MCAN0_RX_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1112. MCAN0_RX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.9 MEM_MCAN0_TX_CFG_REG Registers

2.4.9.1 MEM_TX_CFG_REG Register (Offset = 20h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1113. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0020h

Figure 2-554. MCAN0_TX_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1114. MCAN0_TX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.10 MEM_MCAN1_RX_CFG_REG Registers

2.4.10.1 MEM_RX_CFG_REG Register (Offset = 24h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1115. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0024h

Figure 2-555. MCAN1_RX_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1116. MCAN1_RX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.11 MEM_MCAN1_TX_CFG_REG Registers

2.4.11.1 MEM_TX_CFG_REG Register (Offset = 28h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1117. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0028h

Figure 2-556. MCAN1_TX_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1118. MCAN1_TX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.12 MEM_SPI0_CS0_CFG_REG Registers

2.4.12.1 MEM_CS0_CFG_REG Register (Offset = 2Ch) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1119. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 002Ch

Figure 2-557. SPI0_CS0_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1120. SPI0_CS0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.13 MEM_SPI0_CLK_CFG_REG Registers

2.4.13.1 MEM_CLK_CFG_REG Register (Offset = 30h) [reset = 5d7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1121. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0030h

Figure 2-558. SPI0_CLK_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4822									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	0h	1h	7h			

Access Types Legend

Table 2-1122. SPI0_CLK_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	0h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.14 MEM_SPI0_D0_CFG_REG Registers

2.4.14.1 MEM_D0_CFG_REG Register (Offset = 34h) [reset = 5d7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1123. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0034h

Figure 2-559. SPI0_D0_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4822									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	0h	1h	7h			

Access Types Legend

Table 2-1124. SPI0_D0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	0h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.15 MEM_SPI0_D1_CFG_REG Registers

2.4.15.1 MEM_D1_CFG_REG Register (Offset = 38h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1125. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0038h

Figure 2-560. SPI0_D1_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1126. SPI0_D1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.16 MEM_SPI1_CS0_CFG_REG Registers

2.4.16.1 MEM_CS0_CFG_REG Register (Offset = 3Ch) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1127. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 003Ch

Figure 2-561. SPI1_CS0_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1128. SPI1_CS0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.17 MEM_SPI1_CLK_CFG_REG Registers

2.4.17.1 MEM_CLK_CFG_REG Register (Offset = 40h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1129. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0040h

Figure 2-562. SPI1_CLK_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1130. SPI1_CLK_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.18 MEM_SPI1_D0_CFG_REG Registers

2.4.18.1 MEM_D0_CFG_REG Register (Offset = 44h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1131. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0044h

Figure 2-563. SPI1_D0_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1132. SPI1_D0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.19 MEM_SPI1_D1_CFG_REG Registers

2.4.19.1 MEM_D1_CFG_REG Register (Offset = 48h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1133. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0048h

Figure 2-564. SPI1_D1_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1134. SPI1_D1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.20 MEM_LIN1_RXD_CFG_REG Registers

2.4.20.1 MEM_RXD_CFG_REG Register (Offset = 4Ch) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1135. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 004Ch

Figure 2-565. LIN1_RXD_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1136. LIN1_RXD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.21 MEM_LIN1_TXD_CFG_REG Registers

2.4.21.1 MEM_TXD_CFG_REG Register (Offset = 50h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1137. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0050h

Figure 2-566. LIN1_TXD_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1138. LIN1_TXD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.22 MEM_LIN2_RXD_CFG_REG Registers

2.4.22.1 MEM_RXD_CFG_REG Register (Offset = 54h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1139. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0054h

Figure 2-567. LIN2_RXD_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1140. LIN2_RXD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.23 MEM_LIN2_TXD_CFG_REG Registers

2.4.23.1 MEM_TXD_CFG_REG Register (Offset = 58h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1141. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0058h

Figure 2-568. LIN2_TXD_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1142. LIN2_TXD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.24 MEM_I2C1_SCL_CFG_REG Registers

2.4.24.1 MEM_SCL_CFG_REG Register (Offset = 5Ch) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1143. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 005Ch

Figure 2-569. I2C1_SCL_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1144. I2C1_SCL_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.25 MEM_I2C1_SDA_CFG_REG Registers

2.4.25.1 MEM_SDA_CFG_REG Register (Offset = 60h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1145. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0060h

Figure 2-570. I2C1_SDA_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1146. I2C1_SDA_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.26 MEM_UART0_RTSN_CFG_REG Registers

2.4.26.1 MEM_RTSN_CFG_REG Register (Offset = 64h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1147. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0064h

Figure 2-571. UART0_RTSN_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1148. UART0_RTSN_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.27 MEM_UART0_CTSN_CFG_REG Registers

2.4.27.1 MEM_CTSN_CFG_REG Register (Offset = 68h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1149. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0068h

Figure 2-572. UART0_CTSN_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1150. UART0_CTSN_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.28 MEM_UART0_RXD_CFG_REG Registers

2.4.28.1 MEM_RXD_CFG_REG Register (Offset = 6Ch) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1151. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 006Ch

Figure 2-573. UART0_RXD_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1152. UART0_RXD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.29 MEM_UART0_TXD_CFG_REG Registers

2.4.29.1 MEM_TXD_CFG_REG Register (Offset = 70h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1153. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0070h

Figure 2-574. UART0_TXD_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1154. UART0_TXD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.30 MEM_RGMII1_RXC_CFG_REG Registers

2.4.30.1 MEM_RXC_CFG_REG Register (Offset = 74h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1155. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0074h

Figure 2-575. RGMII1_RXC_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1156. RGMII1_RXC_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.31 MEM_RGMII1_RX_CTL_CFG_REG Registers

2.4.31.1 MEM_RX_CTL_CFG_REG Register (Offset = 78h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1157. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0078h

Figure 2-576. RGMII1_RX_CTL_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1158. RGMII1_RX_CTL_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.32 MEM_RGMII1_RD0_CFG_REG Registers

2.4.32.1 MEM_RD0_CFG_REG Register (Offset = 7Ch) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1159. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 007Ch

Figure 2-577. RGMII1_RD0_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1160. RGMII1_RD0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.33 MEM_RGMII1_RD1_CFG_REG Registers

2.4.33.1 MEM_RD1_CFG_REG Register (Offset = 80h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1161. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0080h

Figure 2-578. RGMII1_RD1_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1162. RGMII1_RD1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.34 MEM_RGMII1_RD2_CFG_REG Registers

2.4.34.1 MEM_RD2_CFG_REG Register (Offset = 84h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1163. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0084h

Figure 2-579. RGMII1_RD2_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1164. RGMII1_RD2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.35 MEM_RGMII1_RD3_CFG_REG Registers

2.4.35.1 MEM_RD3_CFG_REG Register (Offset = 88h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1165. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0088h

Figure 2-580. RGMII1_RD3_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1166. RGMII1_RD3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.36 MEM_RGMII1_TXC_CFG_REG Registers

2.4.36.1 MEM_TXC_CFG_REG Register (Offset = 8Ch) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1167. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 008Ch

Figure 2-581. RGMII1_TXC_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1168. RGMII1_TXC_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.37 MEM_RGMII1_TX_CTL_CFG_REG Registers

2.4.37.1 MEM_TX_CTL_CFG_REG Register (Offset = 90h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1169. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0090h

Figure 2-582. RGMII1_TX_CTL_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1170. RGMII1_TX_CTL_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.38 MEM_RGMII1_TD0_CFG_REG Registers

2.4.38.1 MEM_TD0_CFG_REG Register (Offset = 94h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1171. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0094h

Figure 2-583. RGMII1_TD0_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1172. RGMII1_TD0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.39 MEM_RGMII1_TD1_CFG_REG Registers

2.4.39.1 MEM_TD1_CFG_REG Register (Offset = 98h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1173. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0098h

Figure 2-584. RGMII1_TD1_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1174. RGMII1_TD1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.40 MEM_RGMII1_TD2_CFG_REG Registers

2.4.40.1 MEM_TD2_CFG_REG Register (Offset = 9Ch) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1175. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 009Ch

Figure 2-585. RGMII1_TD2_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1176. RGMII1_TD2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.41 MEM_RGMII1_TD3_CFG_REG Registers

2.4.41.1 MEM_TD3_CFG_REG Register (Offset = A0h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1177. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00A0h

Figure 2-586. RGMII1_TD3_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1178. RGMII1_TD3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.42 MEM_MDIO0_MDIO_CFG_REG Registers

2.4.42.1 MEM_MDIO_CFG_REG Register (Offset = A4h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1179. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00A4h

Figure 2-587. MDIO0_MDIO_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1180. MDIO0_MDIO_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.43 MEM_MDIO0_MDC_CFG_REG Registers

2.4.43.1 MEM_MDC_CFG_REG Register (Offset = A8h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1181. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00A8h

Figure 2-588. MDIO0_MDC_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1182. MDIO0_MDC_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.44 MEM_EPWM0_A_CFG_REG Registers

2.4.44.1 MEM_A_CFG_REG Register (Offset = ACh) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1183. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00ACh

Figure 2-589. EPWM0_A_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1184. EPWM0_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.45 MEM_EPWM0_B_CFG_REG Registers

2.4.45.1 MEM_B_CFG_REG Register (Offset = B0h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1185. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00B0h

Figure 2-590. EPWM0_B_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1186. EPWM0_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.46 MEM_EPWM1_A_CFG_REG Registers

2.4.46.1 MEM_A_CFG_REG Register (Offset = B4h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1187. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00B4h

Figure 2-591. EPWM1_A_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1188. EPWM1_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.47 MEM_EPWM1_B_CFG_REG Registers

2.4.47.1 MEM_B_CFG_REG Register (Offset = B8h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1189. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00B8h

Figure 2-592. EPWM1_B_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1190. EPWM1_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.48 MEM_EPWM2_A_CFG_REG Registers

2.4.48.1 MEM_A_CFG_REG Register (Offset = BCh) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1191. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00BCh

Figure 2-593. EPWM2_A_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1192. EPWM2_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.49 MEM_EPWM2_B_CFG_REG Registers

2.4.49.1 MEM_B_CFG_REG Register (Offset = C0h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1193. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00C0h

Figure 2-594. EPWM2_B_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1194. EPWM2_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.50 MEM_EPWM3_A_CFG_REG Registers

2.4.50.1 MEM_A_CFG_REG Register (Offset = C4h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1195. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00C4h

Figure 2-595. EPWM3_A_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1196. EPWM3_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.51 MEM_EPWM3_B_CFG_REG Registers

2.4.51.1 MEM_B_CFG_REG Register (Offset = C8h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1197. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00C8h

Figure 2-596. EPWM3_B_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1198. EPWM3_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.52 MEM_EPWM4_A_CFG_REG Registers

2.4.52.1 MEM_A_CFG_REG Register (Offset = CCh) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1199. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00CCh

Figure 2-597. EPWM4_A_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1200. EPWM4_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.53 MEM_EPWM4_B_CFG_REG Registers

2.4.53.1 MEM_B_CFG_REG Register (Offset = D0h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1201. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00D0h

Figure 2-598. EPWM4_B_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1202. EPWM4_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.54 MEM_EPWM5_A_CFG_REG Registers

2.4.54.1 MEM_A_CFG_REG Register (Offset = D4h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1203. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00D4h

Figure 2-599. EPWM5_A_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1204. EPWM5_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.55 MEM_EPWM5_B_CFG_REG Registers

2.4.55.1 MEM_B_CFG_REG Register (Offset = D8h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1205. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00D8h

Figure 2-600. EPWM5_B_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1206. EPWM5_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.56 MEM_EPWM6_A_CFG_REG Registers

2.4.56.1 MEM_A_CFG_REG Register (Offset = DCh) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1207. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00DCh

Figure 2-601. EPWM6_A_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1208. EPWM6_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.57 MEM_EPWM6_B_CFG_REG Registers

2.4.57.1 MEM_B_CFG_REG Register (Offset = E0h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1209. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00E0h

Figure 2-602. EPWM6_B_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1210. EPWM6_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.58 MEM_EPWM7_A_CFG_REG Registers

2.4.58.1 MEM_A_CFG_REG Register (Offset = E4h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1211. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00E4h

Figure 2-603. EPWM7_A_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1212. EPWM7_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.59 MEM_EPWM7_B_CFG_REG Registers

2.4.59.1 MEM_B_CFG_REG Register (Offset = E8h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1213. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00E8h

Figure 2-604. EPWM7_B_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1214. EPWM7_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.60 MEM_EPWM8_A_CFG_REG Registers

2.4.60.1 MEM_A_CFG_REG Register (Offset = ECh) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1215. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00ECh

Figure 2-605. EPWM8_A_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1216. EPWM8_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.61 MEM_EPWM8_B_CFG_REG Registers

2.4.61.1 MEM_B_CFG_REG Register (Offset = F0h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1217. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00F0h

Figure 2-606. EPWM8_B_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1218. EPWM8_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.62 MEM_EPWM9_A_CFG_REG Registers

2.4.62.1 MEM_A_CFG_REG Register (Offset = F4h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1219. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00F4h

Figure 2-607. EPWM9_A_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1220. EPWM9_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.63 MEM_EPWM9_B_CFG_REG Registers

2.4.63.1 MEM_B_CFG_REG Register (Offset = F8h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1221. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00F8h

Figure 2-608. EPWM9_B_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1222. EPWM9_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.64 MEM_EPWM10_A_CFG_REG Registers

2.4.64.1 MEM_A_CFG_REG Register (Offset = FCh) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1223. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00FCh

Figure 2-609. EPWM10_A_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1224. EPWM10_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.65 MEM_EPWM10_B_CFG_REG Registers

2.4.65.1 MEM_B_CFG_REG Register (Offset = 100h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1225. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0100h

Figure 2-610. EPWM10_B_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1226. EPWM10_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.66 MEM_EPWM11_A_CFG_REG Registers

2.4.66.1 MEM_A_CFG_REG Register (Offset = 104h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1227. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0104h

Figure 2-611. EPWM11_A_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1228. EPWM11_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.67 MEM_EPWM11_B_CFG_REG Registers

2.4.67.1 MEM_B_CFG_REG Register (Offset = 108h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1229. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0108h

Figure 2-612. EPWM11_B_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1230. EPWM11_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.68 MEM_EPWM12_A_CFG_REG Registers

2.4.68.1 MEM_A_CFG_REG Register (Offset = 10Ch) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1231. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 010Ch

Figure 2-613. EPWM12_A_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1232. EPWM12_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.69 MEM_EPWM12_B_CFG_REG Registers

2.4.69.1 MEM_B_CFG_REG Register (Offset = 110h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1233. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0110h

Figure 2-614. EPWM12_B_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1234. EPWM12_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.70 MEM_EPWM13_A_CFG_REG Registers

2.4.70.1 MEM_A_CFG_REG Register (Offset = 114h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1235. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0114h

Figure 2-615. EPWM13_A_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1236. EPWM13_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.71 MEM_EPWM13_B_CFG_REG Registers

2.4.71.1 MEM_B_CFG_REG Register (Offset = 118h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1237. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0118h

Figure 2-616. EPWM13_B_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1238. EPWM13_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.72 MEM_EPWM14_A_CFG_REG Registers

2.4.72.1 MEM_A_CFG_REG Register (Offset = 11Ch) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1239. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 011Ch

Figure 2-617. EPWM14_A_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1240. EPWM14_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.73 MEM_EPWM14_B_CFG_REG Registers

2.4.73.1 MEM_B_CFG_REG Register (Offset = 120h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1241. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0120h

Figure 2-618. EPWM14_B_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1242. EPWM14_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.74 MEM_EPWM15_A_CFG_REG Registers

2.4.74.1 MEM_A_CFG_REG Register (Offset = 124h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1243. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0124h

Figure 2-619. EPWM15_A_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1244. EPWM15_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.75 MEM_EPWM15_B_CFG_REG Registers

2.4.75.1 MEM_B_CFG_REG Register (Offset = 128h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1245. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0128h

Figure 2-620. EPWM15_B_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1246. EPWM15_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.76 MEM_UART1_RXD_CFG_REG Registers

2.4.76.1 MEM_RXD_CFG_REG Register (Offset = 12Ch) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1247. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 012Ch

Figure 2-621. UART1_RXD_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1248. UART1_RXD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.77 MEM_UART1_TXD_CFG_REG Registers

2.4.77.1 MEM_TXD_CFG_REG Register (Offset = 130h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1249. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0130h

Figure 2-622. UART1_TXD_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1250. UART1_TXD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.78 MEM_MMC0_CLK_CFG_REG Registers

2.4.78.1 MEM_CLK_CFG_REG Register (Offset = 134h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1251. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0134h

Figure 2-623. MMC0_CLK_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1252. MMC0_CLK_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.79 MEM_MMC0_CMD_CFG_REG Registers

2.4.79.1 MEM_CMD_CFG_REG Register (Offset = 138h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1253. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0138h

Figure 2-624. MMC0_CMD_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1254. MMC0_CMD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.80 MEM_MMC0_D0_CFG_REG Registers

2.4.80.1 MEM_D0_CFG_REG Register (Offset = 13Ch) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1255. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 013Ch

Figure 2-625. MMC0_D0_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1256. MMC0_D0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.81 MEM_MMC0_D1_CFG_REG Registers

2.4.81.1 MEM_D1_CFG_REG Register (Offset = 140h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1257. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0140h

Figure 2-626. MMC0_D1_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1258. MMC0_D1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.82 MEM_MMC0_D2_CFG_REG Registers

2.4.82.1 MEM_D2_CFG_REG Register (Offset = 144h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1259. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0144h

Figure 2-627. MMC0_D2_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1260. MMC0_D2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.83 MEM_MMC0_D3_CFG_REG Registers

2.4.83.1 MEM_D3_CFG_REG Register (Offset = 148h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1261. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0148h

Figure 2-628. MMC0_D3_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1262. MMC0_D3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.84 MEM_MMC0_WP_CFG_REG Registers

2.4.84.1 MEM_WP_CFG_REG Register (Offset = 14Ch) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1263. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 014Ch

Figure 2-629. MMC0_WP_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1264. MMC0_WP_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.85 MEM_MMC0_CD_CFG_REG Registers

2.4.85.1 MEM_CD_CFG_REG Register (Offset = 150h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1265. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0150h

Figure 2-630. MMC0_CD_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1266. MMC0_CD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.86 MEM_PR0_MDIO0_MDIO_CFG_REG Registers

2.4.86.1 MEM_MDIO0_MDIO_CFG_REG Register (Offset = 154h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1267. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0154h

Figure 2-631. PR0_MDIO0_MDIO_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1268. PR0_MDIO0_MDIO_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.87 MEM_PR0_MDIO0_MDC_CFG_REG Registers

2.4.87.1 MEM_MDIO0_MDC_CFG_REG Register (Offset = 158h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1269. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0158h

Figure 2-632. PR0_MDIO0_MDC_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1270. PR0_MDIO0_MDC_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.88 MEM_PR0_PRU0_GPO5_CFG_REG Registers

2.4.88.1 MEM_PRU0_GPO5_CFG_REG Register (Offset = 15Ch) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1271. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 015Ch

Figure 2-633. PR0_PRU0_GPO5_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1272. PR0_PRU0_GPO5_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.89 MEM_PR0_PRU0_GPO9_CFG_REG Registers

2.4.89.1 MEM_PRU0_GPO9_CFG_REG Register (Offset = 160h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1273. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0160h

Figure 2-634. PR0_PRU0_GPO9_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1274. PR0_PRU0_GPO9_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.90 MEM_PR0_PRU0_GPO10_CFG_REG Registers

2.4.90.1 MEM_PRU0_GPO10_CFG_REG Register (Offset = 164h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1275. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0164h

Figure 2-635. PR0_PRU0_GPO10_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1276. PR0_PRU0_GPO10_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.91 MEM_PR0_PRU0_GPO8_CFG_REG Registers

2.4.91.1 MEM_PRU0_GPO8_CFG_REG Register (Offset = 168h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1277. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0168h

Figure 2-636. PR0_PRU0_GPO8_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1278. PR0_PRU0_GPO8_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.92 MEM_PR0_PRU0_GPO6_CFG_REG Registers

2.4.92.1 MEM_PRU0_GPO6_CFG_REG Register (Offset = 16Ch) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1279. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 016Ch

Figure 2-637. PR0_PRU0_GPO6_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1280. PR0_PRU0_GPO6_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.93 MEM_PR0_PRU0_GPO4_CFG_REG Registers

2.4.93.1 MEM_PRU0_GPO4_CFG_REG Register (Offset = 170h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1281. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0170h

Figure 2-638. PR0_PRU0_GPO4_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1282. PR0_PRU0_GPO4_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.94 MEM_PR0_PRU0_GPO0_CFG_REG Registers

2.4.94.1 MEM_PRU0_GPO0_CFG_REG Register (Offset = 174h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1283. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0174h

Figure 2-639. PR0_PRU0_GPO0_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1284. PR0_PRU0_GPO0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.95 MEM_PR0_PRU0_GPO1_CFG_REG Registers

2.4.95.1 MEM_PRU0_GPO1_CFG_REG Register (Offset = 178h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1285. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0178h

Figure 2-640. PR0_PRU0_GPO1_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1286. PR0_PRU0_GPO1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.96 MEM_PR0_PRU0_GPO2_CFG_REG Registers

2.4.96.1 MEM_PRU0_GPO2_CFG_REG Register (Offset = 17Ch) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1287. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 017Ch

Figure 2-641. PR0_PRU0_GPO2_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1288. PR0_PRU0_GPO2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.97 MEM_PR0_PRU0_GPO3_CFG_REG Registers

2.4.97.1 MEM_PRU0_GPO3_CFG_REG Register (Offset = 180h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1289. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0180h

Figure 2-642. PR0_PRU0_GPO3_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1290. PR0_PRU0_GPO3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.98 MEM_PR0_PRU0_GPO16_CFG_REG Registers

2.4.98.1 MEM_PRU0_GPO16_CFG_REG Register (Offset = 184h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1291. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0184h

Figure 2-643. PR0_PRU0_GPO16_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1292. PR0_PRU0_GPO16_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.99 MEM_PR0_PRU0_GPO15_CFG_REG Registers

2.4.99.1 MEM_PRU0_GPO15_CFG_REG Register (Offset = 188h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1293. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0188h

Figure 2-644. PR0_PRU0_GPO15_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1294. PR0_PRU0_GPO15_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.100 MEM_PR0_PRU0_GPO11_CFG_REG Registers

2.4.100.1 MEM_PRU0_GPO11_CFG_REG Register (Offset = 18Ch) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1295. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 018Ch

Figure 2-645. PR0_PRU0_GPO11_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1296. PR0_PRU0_GPO11_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.101 MEM_PR0_PRU0_GPO12_CFG_REG Registers

2.4.101.1 MEM_PRU0_GPO12_CFG_REG Register (Offset = 190h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1297. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0190h

Figure 2-646. PR0_PRU0_GPO12_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1298. PR0_PRU0_GPO12_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.102 MEM_PR0_PRU0_GPO13_CFG_REG Registers

2.4.102.1 MEM_PRU0_GPO13_CFG_REG Register (Offset = 194h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1299. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0194h

Figure 2-647. PR0_PRU0_GPO13_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1300. PR0_PRU0_GPO13_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.103 MEM_PR0_PRU0_GPO14_CFG_REG Registers

2.4.103.1 MEM_PRU0_GPO14_CFG_REG Register (Offset = 198h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1301. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0198h

Figure 2-648. PR0_PRU0_GPO14_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1302. PR0_PRU0_GPO14_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.104 MEM_PR0_PRU1_GPO5_CFG_REG Registers

2.4.104.1 MEM_PRU1_GPO5_CFG_REG Register (Offset = 19Ch) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1303. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 019Ch

Figure 2-649. PR0_PRU1_GPO5_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1304. PR0_PRU1_GPO5_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.105 MEM_PR0_PRU1_GPO9_CFG_REG Registers

2.4.105.1 MEM_PRU1_GPO9_CFG_REG Register (Offset = 1A0h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1305. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01A0h

Figure 2-650. PR0_PRU1_GPO9_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1306. PR0_PRU1_GPO9_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.106 MEM_PR0_PRU1_GPO10_CFG_REG Registers

2.4.106.1 MEM_PRU1_GPO10_CFG_REG Register (Offset = 1A4h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1307. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01A4h

Figure 2-651. PR0_PRU1_GPO10_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1308. PR0_PRU1_GPO10_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.107 MEM_PR0_PRU1_GPO8_CFG_REG Registers

2.4.107.1 MEM_PRU1_GPO8_CFG_REG Register (Offset = 1A8h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1309. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01A8h

Figure 2-652. PR0_PRU1_GPO8_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1310. PR0_PRU1_GPO8_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.108 MEM_PR0_PRU1_GPO6_CFG_REG Registers

2.4.108.1 MEM_PRU1_GPO6_CFG_REG Register (Offset = 1ACh) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1311. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01ACh

Figure 2-653. PR0_PRU1_GPO6_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1312. PR0_PRU1_GPO6_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.109 MEM_PR0_PRU1_GPO4_CFG_REG Registers

2.4.109.1 MEM_PRU1_GPO4_CFG_REG Register (Offset = 1B0h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1313. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01B0h

Figure 2-654. PR0_PRU1_GPO4_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1314. PR0_PRU1_GPO4_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.110 MEM_PR0_PRU1_GPO0_CFG_REG Registers

2.4.110.1 MEM_PRU1_GPO0_CFG_REG Register (Offset = 1B4h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1315. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01B4h

Figure 2-655. PR0_PRU1_GPO0_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1316. PR0_PRU1_GPO0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.111 MEM_PR0_PRU1_GPO1_CFG_REG Registers

2.4.111.1 MEM_PRU1_GPO1_CFG_REG Register (Offset = 1B8h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1317. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01B8h

Figure 2-656. PR0_PRU1_GPO1_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1318. PR0_PRU1_GPO1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.112 MEM_PR0_PRU1_GPO2_CFG_REG Registers

2.4.112.1 MEM_PRU1_GPO2_CFG_REG Register (Offset = 1BCh) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1319. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01BCh

Figure 2-657. PR0_PRU1_GPO2_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1320. PR0_PRU1_GPO2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.113 MEM_PR0_PRU1_GPO3_CFG_REG Registers

2.4.113.1 MEM_PRU1_GPO3_CFG_REG Register (Offset = 1C0h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1321. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01C0h

Figure 2-658. PR0_PRU1_GPO3_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1322. PR0_PRU1_GPO3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.114 MEM_PR0_PRU1_GPO16_CFG_REG Registers

2.4.114.1 MEM_PRU1_GPO16_CFG_REG Register (Offset = 1C4h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1323. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01C4h

Figure 2-659. PR0_PRU1_GPO16_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1324. PR0_PRU1_GPO16_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.115 MEM_PR0_PRU1_GPO15_CFG_REG Registers

2.4.115.1 MEM_PRU1_GPO15_CFG_REG Register (Offset = 1C8h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1325. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01C8h

Figure 2-660. PR0_PRU1_GPO15_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1326. PR0_PRU1_GPO15_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.116 MEM_PR0_PRU1_GPO11_CFG_REG Registers

2.4.116.1 MEM_PRU1_GPO11_CFG_REG Register (Offset = 1CCh) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1327. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01CCh

Figure 2-661. PR0_PRU1_GPO11_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1328. PR0_PRU1_GPO11_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.117 MEM_PR0_PRU1_GPO12_CFG_REG Registers

2.4.117.1 MEM_PRU1_GPO12_CFG_REG Register (Offset = 1D0h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1329. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01D0h

Figure 2-662. PR0_PRU1_GPO12_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1330. PR0_PRU1_GPO12_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.118 MEM_PR0_PRU1_GPO13_CFG_REG Registers

2.4.118.1 MEM_PRU1_GPO13_CFG_REG Register (Offset = 1D4h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1331. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01D4h

Figure 2-663. PR0_PRU1_GPO13_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1332. PR0_PRU1_GPO13_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.119 MEM_PR0_PRU1_GPO14_CFG_REG Registers

2.4.119.1 MEM_PRU1_GPO14_CFG_REG Register (Offset = 1D8h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1333. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01D8h

Figure 2-664. PR0_PRU1_GPO14_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1334. PR0_PRU1_GPO14_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.120 MEM_PR0_PRU1_GPO19_CFG_REG Registers

2.4.120.1 MEM_PRU1_GPO19_CFG_REG Register (Offset = 1DCh) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1335. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01DCh

Figure 2-665. PR0_PRU1_GPO19_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1336. PR0_PRU1_GPO19_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.121 MEM_PR0_PRU1_GPO18_CFG_REG Registers

2.4.121.1 MEM_PRU1_GPO18_CFG_REG Register (Offset = 1E0h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1337. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01E0h

Figure 2-666. PR0_PRU1_GPO18_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1338. PR0_PRU1_GPO18_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.122 MEM_EXT_REFCLK0_CFG_REG Registers

2.4.122.1 MEM_REFCLK0_CFG_REG Register (Offset = 1E4h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1339. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01E4h

Figure 2-667. EXT_REFCLK0_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1340. EXT_REFCLK0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.123 MEM_SDFM0_CLK0_CFG_REG Registers

2.4.123.1 MEM_CLK0_CFG_REG Register (Offset = 1E8h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1341. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01E8h

Figure 2-668. SDFM0_CLK0_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1342. SDFM0_CLK0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.124 MEM_SDFM0_D0_CFG_REG Registers

2.4.124.1 MEM_D0_CFG_REG Register (Offset = 1ECh) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1343. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01ECh

Figure 2-669. SDFM0_D0_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1344. SDFM0_D0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.125 MEM_SDFM0_CLK1_CFG_REG Registers

2.4.125.1 MEM_CLK1_CFG_REG Register (Offset = 1F0h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1345. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01F0h

Figure 2-670. SDFM0_CLK1_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1346. SDFM0_CLK1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.126 MEM_SDFM0_D1_CFG_REG Registers

2.4.126.1 MEM_D1_CFG_REG Register (Offset = 1F4h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1347. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01F4h

Figure 2-671. SDFM0_D1_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1348. SDFM0_D1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.127 MEM_SDFM0_CLK2_CFG_REG Registers

2.4.127.1 MEM_CLK2_CFG_REG Register (Offset = 1F8h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1349. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01F8h

Figure 2-672. SDFM0_CLK2_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1350. SDFM0_CLK2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.128 MEM_SDFM0_D2_CFG_REG Registers

2.4.128.1 MEM_D2_CFG_REG Register (Offset = 1FCh) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1351. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01FCh

Figure 2-673. SDFM0_D2_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1352. SDFM0_D2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.129 MEM_SDFM0_CLK3_CFG_REG Registers

2.4.129.1 MEM_CLK3_CFG_REG Register (Offset = 200h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1353. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0200h

Figure 2-674. SDFM0_CLK3_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1354. SDFM0_CLK3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.130 MEM_SDFM0_D3_CFG_REG Registers

2.4.130.1 MEM_D3_CFG_REG Register (Offset = 204h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1355. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0204h

Figure 2-675. SDFM0_D3_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1356. SDFM0_D3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.131 MEM_EQEP0_A_CFG_REG Registers

2.4.131.1 MEM_A_CFG_REG Register (Offset = 208h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1357. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0208h

Figure 2-676. EQEP0_A_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1358. EQEP0_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.132 MEM_EQEP0_B_CFG_REG Registers

2.4.132.1 MEM_B_CFG_REG Register (Offset = 20Ch) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1359. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 020Ch

Figure 2-677. EQEP0_B_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1360. EQEP0_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.133 MEM_EQEP0_STROBE_CFG_REG Registers

2.4.133.1 MEM_STROBE_CFG_REG Register (Offset = 210h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1361. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0210h

Figure 2-678. EQEP0_STROBE_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1362. EQEP0_STROBE_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.134 MEM_EQEP0_INDEX_CFG_REG Registers

2.4.134.1 MEM_INDEX_CFG_REG Register (Offset = 214h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1363. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0214h

Figure 2-679. EQEP0_INDEX_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1364. EQEP0_INDEX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.135 MEM_I2C0_SDA_CFG_REG Registers

2.4.135.1 MEM_SDA_CFG_REG Register (Offset = 218h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1365. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0218h

Figure 2-680. I2C0_SDA_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1366. I2C0_SDA_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.136 MEM_I2C0_SCL_CFG_REG Registers

2.4.136.1 MEM_SCL_CFG_REG Register (Offset = 21Ch) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1367. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 021Ch

Figure 2-681. I2C0_SCL_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1368. I2C0_SCL_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.137 MEM_MCAN2_TX_CFG_REG Registers

2.4.137.1 MEM_TX_CFG_REG Register (Offset = 220h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1369. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0220h

Figure 2-682. MCAN2_TX_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1370. MCAN2_TX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.138 MEM_MCAN2_RX_CFG_REG Registers

2.4.138.1 MEM_RX_CFG_REG Register (Offset = 224h) [reset = 5f7h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1371. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0224h

Figure 2-683. MCAN2_RX_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a4886									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	1h	1h	1h	1h	7h			

Access Types Legend

Table 2-1372. MCAN2_RX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

2.4.139 MEM_CLKOUT0_CFG_REG Registers

2.4.139.1 MEM_CFG_REG Register (Offset = 228h) [reset = 570h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1373. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0228h

Figure 2-684. CLKOUT0_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
R/W	R/W	NONE									R/W	R/W		R/W	
0h	0h	9a2176									0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0					1h	0h	1h	0h	1h	1h	1h	0h			

Access Types Legend

Table 2-1374. CLKOUT0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	R/W	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	R/W	0h	MMR bits for HSMODE pin incase of true I2C pads
29:21	RESERVED	NONE		Reserved
20	INP_INV_SEL	R/W	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	0h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	0h	Function select

2.4.140 MEM_WARMRSTN_CFG_REG Registers

2.4.140.1 MEM_CFG_REG Register (Offset = 22Ch) [reset = 510h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1375. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 022Ch

Figure 2-685. WARMRSTN_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	RESERVED														
R	NONE														
0h	60523a4														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	RESERVED			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	NONE			
60523a4					1h	0h	1h	0h	0h	0h	1h	0			

Access Types Legend

Table 2-1376. WARMRSTN_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R		Reserved
30:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	0h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	0h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	0h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	RESERVED	NONE		Reserved

2.4.141 MEM_SAFETY_ERRORN_CFG_REG Registers

2.4.141.1 MEM_ERRORN_CFG_REG Register (Offset = 230h) [reset = 410h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1377. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0230h

Figure 2-686. SAFETY_ERRORN_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	RESERVED														
R	NONE														
0h	5f5e164														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	RESERVED			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	NONE			
5f5e164					1h	0h	0h	0h	0h	0h	1h	0			

Access Types Legend

Table 2-1378. SAFETY_ERRORN_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R		Reserved
30:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	0h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	0h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	0h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	0h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	RESERVED	NONE		Reserved

2.4.142 MEM_TDI_CFG_REG Registers

2.4.142.1 MEM_CFG_REG Register (Offset = 234h) [reset = 6d0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1379. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0234h

Figure 2-687. TDI_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	RESERVED														
R	NONE														
0h	6902594														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	RESERVED			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	NONE			
6902594					1h	1h	0h	1h	1h	0h	1h	0			

Access Types Legend

Table 2-1380. TDI_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R		Reserved
30:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	1h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	0h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	0h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	RESERVED	NONE		Reserved

2.4.143 MEM_TDO_CFG_REG Registers

2.4.143.1 MEM_CFG_REG Register (Offset = 238h) [reset = 630h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1381. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0238h

Figure 2-688. TDO_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	RESERVED														
R	NONE														
0h	68e7bcc														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	RESERVED			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	NONE			
68e7bcc					1h	1h	0h	0h	0h	1h	1h	0			

Access Types Legend

Table 2-1382. TDO_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R		Reserved
30:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	1h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	0h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	0h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	0h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	RESERVED	NONE		Reserved

2.4.144 MEM_TMS_CFG_REG Registers

2.4.144.1 MEM_CFG_REG Register (Offset = 23Ch) [reset = 610h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1383. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 023Ch

Figure 2-689. TMS_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	RESERVED														
R	NONE														
0h	68e77e4														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	RESERVED			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	NONE			
68e77e4					1h	1h	0h	0h	0h	0h	1h	0			

Access Types Legend

Table 2-1384. TMS_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R		Reserved
30:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	1h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	0h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	0h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	0h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	0h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	RESERVED	NONE		Reserved

2.4.145 MEM_TCK_CFG_REG Registers

2.4.145.1 MEM_CFG_REG Register (Offset = 240h) [reset = 210h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1385. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0240h

Figure 2-690. TCK_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	RESERVED														
R	NONE														
0h	9896e4														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	RESERVED			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	NONE			
9896e4					0h	1h	0h	0h	0h	0h	1h	0			

Access Types Legend

Table 2-1386. TCK_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R		Reserved
30:11	RESERVED	NONE		Reserved
10	SC1	R/W	0h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	1h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	0h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	0h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	0h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	0h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	RESERVED	NONE		Reserved

2.4.146 MEM_QSPI0_CLKLB_CFG_REG Registers

2.4.146.1 MEM_CLKLB_CFG_REG Register (Offset = 244h) [reset = 5f0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1387. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0244h

Figure 2-691. QSPI0_CLKLB_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	RESERVED														
R	NONE														
0h	606d53c														

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	RESERVED			
NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	NONE			
606d53c					1h	0h	1h	1h	1h	1h	1h	0			

Access Types Legend

Table 2-1388. QSPI0_CLKLB_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R		Reserved
30:11	RESERVED	NONE		Reserved
10	SC1	R/W	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	R/W	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	R/W	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	R/W	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	RESERVED	NONE		Reserved

2.4.147 MEM_QUAL_GRP_0_CFG_REG Registers

2.4.147.1 MEM_GRP_0_CFG_REG Register (Offset = 248h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1389. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0248h

Figure 2-692. QUAL_GRP_0_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	RESERVED														
R	NONE														
0h	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								R/W							
0								0h							

Access Types Legend

Table 2-1390. QUAL_GRP_0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R		Reserved
30:8	RESERVED	NONE		Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

2.4.148 MEM_QUAL_GRP_1_CFG_REG Registers

2.4.148.1 MEM_GRP_1_CFG_REG Register (Offset = 24Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1391. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 024Ch

Figure 2-693. QUAL_GRP_1_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	RESERVED														
R	NONE														
0h	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								R/W							
0								0h							

Access Types Legend

Table 2-1392. QUAL_GRP_1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R		Reserved
30:8	RESERVED	NONE		Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

2.4.149 MEM_QUAL_GRP_2_CFG_REG Registers

2.4.149.1 MEM_GRP_2_CFG_REG Register (Offset = 250h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1393. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0250h

Figure 2-694. QUAL_GRP_2_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	RESERVED														
R	NONE														
0h	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								R/W							
0								0h							

Access Types Legend

Table 2-1394. QUAL_GRP_2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R		Reserved
30:8	RESERVED	NONE		Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

2.4.150 MEM_QUAL_GRP_3_CFG_REG Registers

2.4.150.1 MEM_GRP_3_CFG_REG Register (Offset = 254h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1395. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0254h

Figure 2-695. QUAL_GRP_3_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	RESERVED														
R	NONE														
0h	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								R/W							
0								0h							

Access Types Legend

Table 2-1396. QUAL_GRP_3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R		Reserved
30:8	RESERVED	NONE		Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

2.4.151 MEM_QUAL_GRP_4_CFG_REG Registers

2.4.151.1 MEM_GRP_4_CFG_REG Register (Offset = 258h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1397. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0258h

Figure 2-696. QUAL_GRP_4_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	RESERVED														
R	NONE														
0h	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								R/W							
0								0h							

Access Types Legend

Table 2-1398. QUAL_GRP_4_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R		Reserved
30:8	RESERVED	NONE		Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

2.4.152 MEM_QUAL_GRP_5_CFG_REG Registers

2.4.152.1 MEM_GRP_5_CFG_REG Register (Offset = 25Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1399. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 025Ch

Figure 2-697. QUAL_GRP_5_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	RESERVED														
R	NONE														
0h	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								R/W							
0								0h							

Access Types Legend

Table 2-1400. QUAL_GRP_5_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R		Reserved
30:8	RESERVED	NONE		Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

2.4.153 MEM_QUAL_GRP_6_CFG_REG Registers

2.4.153.1 MEM_GRP_6_CFG_REG Register (Offset = 260h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1401. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0260h

Figure 2-698. QUAL_GRP_6_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	RESERVED														
R	NONE														
0h	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								R/W							
0								0h							

Access Types Legend

Table 2-1402. QUAL_GRP_6_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R		Reserved
30:8	RESERVED	NONE		Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

2.4.154 MEM_QUAL_GRP_7_CFG_REG Registers

2.4.154.1 MEM_GRP_7_CFG_REG Register (Offset = 264h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1403. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0264h

Figure 2-699. QUAL_GRP_7_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	RESERVED														
R	NONE														
0h	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								R/W							
0								0h							

Access Types Legend

Table 2-1404. QUAL_GRP_7_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R		Reserved
30:8	RESERVED	NONE		Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

2.4.155 MEM_QUAL_GRP_8_CFG_REG Registers

2.4.155.1 MEM_GRP_8_CFG_REG Register (Offset = 268h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1405. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0268h

Figure 2-700. QUAL_GRP_8_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	RESERVED														
R	NONE														
0h	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								R/W							
0								0h							

Access Types Legend

Table 2-1406. QUAL_GRP_8_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R		Reserved
30:8	RESERVED	NONE		Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

2.4.156 MEM_QUAL_GRP_9_CFG_REG Registers

2.4.156.1 MEM_GRP_9_CFG_REG Register (Offset = 26Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1407. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 026Ch

Figure 2-701. QUAL_GRP_9_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	RESERVED														
R	NONE														
0h	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								R/W							
0								0h							

Access Types Legend

Table 2-1408. QUAL_GRP_9_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R		Reserved
30:8	RESERVED	NONE		Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

2.4.157 MEM_QUAL_GRP_10_CFG_REG Registers

2.4.157.1 MEM_GRP_10_CFG_REG Register (Offset = 270h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1409. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0270h

Figure 2-702. QUAL_GRP_10_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	RESERVED														
R	NONE														
0h	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								R/W							
0								0h							

Access Types Legend

Table 2-1410. QUAL_GRP_10_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R		Reserved
30:8	RESERVED	NONE		Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

2.4.158 MEM_QUAL_GRP_11_CFG_REG Registers

2.4.158.1 MEM_GRP_11_CFG_REG Register (Offset = 274h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1411. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0274h

Figure 2-703. QUAL_GRP_11_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	RESERVED														
R	NONE														
0h	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								R/W							
0								0h							

Access Types Legend

Table 2-1412. QUAL_GRP_11_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R		Reserved
30:8	RESERVED	NONE		Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

2.4.159 MEM_QUAL_GRP_12_CFG_REG Registers

2.4.159.1 MEM_GRP_12_CFG_REG Register (Offset = 278h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1413. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0278h

Figure 2-704. QUAL_GRP_12_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	RESERVED														
R	NONE														
0h	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								R/W							
0								0h							

Access Types Legend

Table 2-1414. QUAL_GRP_12_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R		Reserved
30:8	RESERVED	NONE		Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

2.4.160 MEM_QUAL_GRP_13_CFG_REG Registers

2.4.160.1 MEM_GRP_13_CFG_REG Register (Offset = 27Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1415. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 027Ch

Figure 2-705. QUAL_GRP_13_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	RESERVED														
R	NONE														
0h	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								R/W							
0								0h							

Access Types Legend

Table 2-1416. QUAL_GRP_13_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R		Reserved
30:8	RESERVED	NONE		Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

2.4.161 MEM_QUAL_GRP_14_CFG_REG Registers

2.4.161.1 MEM_GRP_14_CFG_REG Register (Offset = 280h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1417. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0280h

Figure 2-706. QUAL_GRP_14_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	RESERVED														
R	NONE														
0h	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								R/W							
0								0h							

Access Types Legend

Table 2-1418. QUAL_GRP_14_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R		Reserved
30:8	RESERVED	NONE		Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

2.4.162 MEM_QUAL_GRP_15_CFG_REG Registers

2.4.162.1 MEM_GRP_15_CFG_REG Register (Offset = 284h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1419. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0284h

Figure 2-707. QUAL_GRP_15_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	RESERVED														
R	NONE														
0h	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								R/W							
0								0h							

Access Types Legend

Table 2-1420. QUAL_GRP_15_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R		Reserved
30:8	RESERVED	NONE		Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

2.4.163 MEM_QUAL_GRP_16_CFG_REG Registers

2.4.163.1 MEM_GRP_16_CFG_REG Register (Offset = 288h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1421. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0288h

Figure 2-708. QUAL_GRP_16_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	RESERVED														
R	NONE														
0h	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								R/W							
0								0h							

Access Types Legend

Table 2-1422. QUAL_GRP_16_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R		Reserved
30:8	RESERVED	NONE		Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

2.4.164 MEM_QUAL_GRP_17_CFG_REG Registers

2.4.164.1 MEM_GRP_17_CFG_REG Register (Offset = 28Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1423. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 028Ch

Figure 2-709. QUAL_GRP_17_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	RESERVED														
R	NONE														
0h	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								R/W							
0								0h							

Access Types Legend

Table 2-1424. QUAL_GRP_17_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R		Reserved
30:8	RESERVED	NONE		Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

2.4.165 MEM_USER_MODE_EN Registers

2.4.165.1 MEM_MODE_EN Register (Offset = 290h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1425. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0290h

Figure 2-710. USER_MODE_EN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
USER_MODE_EN															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USER_MODE_EN															
R/W															
0h															

Access Types Legend

Table 2-1426. USER_MODE_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	USER_MODE_EN	R/W	0h	Write 0XADADADAD to enable user mode write access to IO CFG space

2.4.166 MEM_PADGLBL_CFG_REG Registers

2.4.166.1 MEM_CFG_REG Register (Offset = 294h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1427. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0294h

Figure 2-711. PADGLBL_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PADGLBL_CFG_REG															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PADGLBL_CFG_REG															
R/W															
0h															

Access Types Legend

Table 2-1428. PADGLBL_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PADGLBL_CFG_REG	R/W	0h	2:0 : global_ie_n_ctl - Write 3'b111 to pass global_ie_n_val to IE_N/ RXACTIVE_N pin of all the IOs. 3 : global_ie_n_val - Active low 10:8 : global_oe_n_ctl - Write 3'b111 to pass global_oe_n_val to OE_N/GZ pin of all the IOs. 11 : global_oe_n_val - Active low 18:16 : global_pi_ctl - Write 3'b111 to pass global_pi_val and global_pu_val to all the IOs 19 : global_pi_val 20 : global_pu_val

2.4.167 MEM_IO_CFG_KICK0 Registers

2.4.167.1 MEM_CFG_KICK0 Register (Offset = 298h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1429. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0298h

Figure 2-712. IO_CFG_KICK0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IO_CFG_KICK0															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IO_CFG_KICK0															
R/W															
0h															

Access Types Legend

Table 2-1430. IO_CFG_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IO_CFG_KICK0	R/W	0h	Kicker 0 Register. The value 83E7 0B13h must be written to KICK0 as part of the process to unlock the CPU.write access to the above PIN MUX registers [including IOCFGKICK1]

2.4.168 MEM_IO_CFG_KICK1 Registers

2.4.168.1 MEM_CFG_KICK1 Register (Offset = 29Ch) [reset = c1h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1431. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 029Ch

Figure 2-713. IO_CFG_KICK1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IO_CFG_KICK1															
R/W															
c1h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IO_CFG_KICK1															
R/W															
c1h															

Access Types Legend

Table 2-1432. IO_CFG_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IO_CFG_KICK1	R/W	C1h	Kicker 1 Register. The value 95A4 F1E0h must be written to the KICK1 as part of the process to unlock the CPU write access to above PINMUX registers [excluding IOCFGKICK0]. IOCFGKICK0 has to be written with 83E70B13h to enable access to IOCFGKICK1.

2.4.169 Access Table

Table 2-1433. Access Type Codes

Access Type	Code	Description
R/W	R/W	Read / Write
R	R	Read

2.5 TOP_RCM Registers

Table 2-1434. CFG0, CFG0 Registers, Base Address=0X0000000053200000, Length=8192

Offset	Length	Register Name	top_rcm_mmr0 Physical Address
0h	32	PID	5320 0000h
4h	32	WARM_RESET_CONFIG	5320 0004h
8h	32	WARM_RESET_REQ	5320 0008h
Ch	32	WARM_RST_CAUSE	5320 000Ch
10h	32	WARM_RST_CAUSE_CLR	5320 0010h
14h	32	RCOSC32K_CTRL	5320 0014h
18h	32	LIMP_MODE_EN	5320 0018h
1Ch	32	PLL_REF_CLK_SRC_SEL	5320 001Ch
20h	32	PAD_XTAL_CTRL	5320 0020h
24h	32	SOP_MODE_VALUE	5320 0024h
28h	32	CLK_LOSS_STATUS	5320 0028h
30h	32	WARM_RSTTIME1	5320 0030h
34h	32	WARM_RSTTIME2	5320 0034h
38h	32	WARM_RSTTIME3	5320 0038h
3Ch	32	WARM_RESET_CONFIG_OV	5320 003Ch
40h	32	WARM_RESET_CONFIG_UV	5320 0040h
44h	32	WARM_RESET_CONFIG_MISC	5320 0044h
400h	32	PLL_CORE_PWRCTRL	5320 0400h
404h	32	PLL_CORE_CLKCTRL	5320 0404h
408h	32	PLL_CORE_TENABLE	5320 0408h
40Ch	32	PLL_CORE_TENABLEDIV	5320 040Ch
410h	32	PLL_CORE_M2NDIV	5320 0410h
414h	32	PLL_CORE_MN2DIV	5320 0414h
418h	32	PLL_CORE_FRACDIV	5320 0418h
41Ch	32	PLL_CORE_BWCTRL	5320 041Ch
420h	32	PLL_CORE_FRACCTRL	5320 0420h
424h	32	PLL_CORE_STATUS	5320 0424h
428h	32	PLL_CORE_HSDIVIDER	5320 0428h
42Ch	32	PLL_CORE_HSDIVIDER_CLKOUT0	5320 042Ch
430h	32	PLL_CORE_HSDIVIDER_CLKOUT1	5320 0430h
434h	32	PLL_CORE_HSDIVIDER_CLKOUT2	5320 0434h
438h	32	PLL_CORE_HSDIVIDER_CLKOUT3	5320 0438h
43Ch	32	PLL_CORE_RSTCTRL	5320 043Ch
440h	32	PLL_CORE_HSDIVIDER_RSTCTRL	5320 0440h
500h	32	R5SS_CLK_SRC_SEL	5320 0500h
504h	32	R5SS_CLK_STATUS	5320 0504h
510h	32	R5SS0_CLK_DIV_SEL	5320 0510h
514h	32	R5SS1_CLK_DIV_SEL	5320 0514h
518h	32	R5SS0_CLK_GATE	5320 0518h
51Ch	32	R5SS1_CLK_GATE	5320 051Ch
520h	32	SYS_CLK_DIV_VAL	5320 0520h
524h	32	SYS_CLK_GATE	5320 0524h
528h	32	SYS_CLK_STATUS	5320 0528h
800h	32	PLL_PER_PWRCTRL	5320 0800h
804h	32	PLL_PER_CLKCTRL	5320 0804h

Table 2-1434. CFG0, CFG0 Registers, Base Address=0X0000000053200000, Length=8192 (continued)

Offset	Length	Register Name	top_rcm_mmr0 Physical Address
808h	32	PLL_PER_TENABLE	5320 0808h
80Ch	32	PLL_PER_TENABLEDIV	5320 080Ch
810h	32	PLL_PER_M2NDIV	5320 0810h
814h	32	PLL_PER_MN2DIV	5320 0814h
818h	32	PLL_PER_FRACDIV	5320 0818h
81Ch	32	PLL_PER_BWCTRL	5320 081Ch
820h	32	PLL_PER_FRACCTRL	5320 0820h
824h	32	PLL_PER_STATUS	5320 0824h
828h	32	PLL_PER_HSDIVIDER	5320 0828h
82Ch	32	PLL_PER_HSDIVIDER_CLKOUT0	5320 082Ch
830h	32	PLL_PER_HSDIVIDER_CLKOUT1	5320 0830h
834h	32	PLL_PER_HSDIVIDER_CLKOUT2	5320 0834h
83Ch	32	PLL_PER_RSTCTRL	5320 083Ch
840h	32	PLL_PER_HSDIVIDER_RSTCTRL	5320 0840h
C00h	32	CLKOUT0_CLK_SRC_SEL	5320 0C00h
C04h	32	CLKOUT1_CLK_SRC_SEL	5320 0C04h
C08h	32	CLKOUT0_DIV_VAL	5320 0C08h
C0Ch	32	CLKOUT1_DIV_VAL	5320 0C0Ch
C10h	32	CLKOUT0_CLK_GATE	5320 0C10h
C14h	32	CLKOUT1_CLK_GATE	5320 0C14h
C18h	32	CLKOUT0_CLK_STATUS	5320 0C18h
C1Ch	32	CLKOUT1_CLK_STATUS	5320 0C1Ch
C20h	32	TRCCLKOUT_CLK_SRC_SEL	5320 0C20h
C24h	32	TRCCLKOUT_DIV_VAL	5320 0C24h
C28h	32	TRCCLKOUT_CLK_GATE	5320 0C28h
C2Ch	32	TRCCLKOUT_CLK_STATUS	5320 0C2Ch
D00h	32	DFT_DMLED_EXEC	5320 0D00h
D04h	32	DFT_DMLED_STATUS	5320 0D04h
E00h	32	HW_REG0	5320 0E00h
E04h	32	HW_REG1	5320 0E04h
E08h	32	HW_REG2	5320 0E08h
E0Ch	32	HW_REG3	5320 0E0Ch
FD0h	32	HW_SPARE_RW0	5320 0FD0h
FD4h	32	HW_SPARE_RW1	5320 0FD4h
FD8h	32	HW_SPARE_RW2	5320 0FD8h
FDCh	32	HW_SPARE_RW3	5320 0FDCh
FE0h	32	HW_SPARE_RO0	5320 0FE0h
FE4h	32	HW_SPARE_RO1	5320 0FE4h
FE8h	32	HW_SPARE_RO2	5320 0FE8h
FECh	32	HW_SPARE_RO3	5320 0FECh
FF0h	32	HW_SPARE_WPH	5320 0FF0h
FF4h	32	HW_SPARE_REC	5320 0FF4h
1008h	32	LOCK0_KICK0	5320 1008h
100Ch	32	LOCK0_KICK1	5320 100Ch
1010h	32	intr_raw_status	5320 1010h
1014h	32	intr_enabled_status_clear	5320 1014h
1018h	32	intr_enable	5320 1018h

Table 2-1434. CFG0, CFG0 Registers, Base Address=0X0000000053200000, Length=8192 (continued)

Offset	Length	Register Name	top_rcm_mmr0 Physical Address
101Ch	32	intr_enable_clear	5320 101Ch
1020h	32	eoi	5320 1020h
1024h	32	fault_address	5320 1024h
1028h	32	fault_type_status	5320 1028h
102Ch	32	fault_attr_status	5320 102Ch
1030h	32	fault_clear	5320 1030h

2.5.1 CFG0_PID Registers

2.5.1.1 CFG0_PID Register (Offset = 0h) [reset = 61800215h]

Short Description: PID register

Long Description: PID register

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Table 2-1435. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0000h

Figure 2-714. PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PID_MSB16															
R															
6180h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_MISC					PID_MAJOR			PID_CUSTOM		PID_MINOR					
R					R			R		R					
0h					2h			0h		15h					

Access Types Legend

Table 2-1436. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR	R	15h	Reset Source: mod_g_rst_n

2.5.2 CFG0_WARM_RESET_CONFIG Registers

2.5.2.1 CFG0_RESET_CONFIG Register (Offset = 4h) [reset = 77770077h]

Short Description:

Long Description:

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Table 2-1437. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0004h

Figure 2-715. WARM_RESET_CONFIG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	WARM_RESET_CONFIG_WDOG3_RST_EN			RESERVED	WARM_RESET_CONFIG_WDOG2_RST_EN			RESERVED	WARM_RESET_CONFIG_WDOG1_RST_EN			RESERVED	WARM_RESET_CONFIG_WDOG0_RST_EN		
NONE	R/W			NONE	R/W			NONE	R/W			NONE	R/W		
1	7h			1	7h			0	7h			0	7h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	WARM_RESET_CONFIG_TSENSE1_RST_EN			RESERVED	WARM_RESET_CONFIG_TSENSE0_RST_EN			RESERVED	WARM_RESET_CONFIG_RST_EN			RESERVED	WARM_RESET_CONFIG_PAD_BYPASS		
NONE	R/W			NONE	R/W			NONE	R/W			NONE	R/W		
1	0h			1	0h			1	7h			1	7h		

Access Types Legend

Table 2-1438. WARM_RESET_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE		Reserved
30:28	WARM_RESET_CONFIG_WDOG3_RST_EN	R/W	7h	Enable/Disable WATCHDOG3 triggering Warm Reset Data should be loaded as multibit. Write 3b000 to disable corresponding Watchdog Write 3 b111 enable corresponding Watchdog Reset Source: mod_g_rst_n
27	RESERVED	NONE		Reserved
26:24	WARM_RESET_CONFIG_WDOG2_RST_EN	R/W	7h	Enable/Disable WATCHDOG2 triggering Warm Reset Data should be loaded as multibit. Write 3b000 to disable corresponding Watchdog Write 3 b111 enable corresponding Watchdog Reset Source: mod_g_rst_n
23	RESERVED	NONE		Reserved
22:20	WARM_RESET_CONFIG_WDOG1_RST_EN	R/W	7h	Enable/Disable WATCHDOG1 triggering Warm Reset Data should be loaded as multibit. Write 3b000 to disable corresponding Watchdog Write 3 b111 enable corresponding Watchdog Reset Source: mod_g_rst_n
19	RESERVED	NONE		Reserved
18:16	WARM_RESET_CONFIG_WDOG0_RST_EN	R/W	7h	Enable/Disable WATCHDOG0 triggering Warm Reset Data should be loaded as multibit. Write 3b000 to disable corresponding Watchdog Write 3 b111 enable corresponding Watchdog Reset Source: mod_g_rst_n
15	RESERVED	NONE		Reserved
14:12	WARM_RESET_CONFIG_TSENSE1_RST_EN	R/W	0h	Enable/Disable TEMPSENSE1 triggering Warm Reset Data should be loaded as multibit. Write 3b000 to disable temperature sensor 1 Write 3 b111 to enable temperature sensor 1 **Note: This bit will only be reset by PORz. Reset Source: mod_por_rst_n
11	RESERVED	NONE		Reserved

Table 2-1438. WARM_RESET_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10:8	WARM_RESET_CONFIG_TSENSE0_RST_EN	R/W	0h	Enable/Disable TEMPSENSE0 triggering Warm Reset Data should be loaded as multibit. Write 3b000 to disable temperature sensor 0 Write 3 b111 to enable temperature sensor 0 **Note: This bit will only be reset by PORz. Reset Source: mod_por_rst_n
7	RESERVED	NONE		Reserved
6:4	WARM_RESET_CONFIG_RST_EN	R/W	7h	Enable/Disable DEBUGSS triggering Warm Reset Data should be loaded as multibit. Write 3b000 to disable debugger Write 3 b111 enable debugger Reset Source: mod_g_rst_n
3	RESERVED	NONE		Reserved
2:0	WARM_RESET_CONFIG_PAD_BYPASS	R/W	7h	Bypass the Warm reset from Pad Input Data should be loaded as multibit. Write 3b000 : Pad Warm Reset pin has control over warm reset Write 3 b111 : Pad warm reset pin has no control on warm reset **Note: This bit will only be reset by PORz. Reset Source: mod_por_rst_n

2.5.3 CFG0_WARM_RESET_REQ Registers

2.5.3.1 CFG0_RESET_REQ Register (Offset = 8h) [reset = 7h]

Short Description:

Long Description:

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Table 2-1439. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0008h

Figure 2-716. WARM_RESET_REQ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
b															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													WARM_RESET_REQ_SW_RST		
NONE													R/W		
b													7h		

Access Types Legend

Table 2-1440. WARM_RESET_REQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	WARM_RESET_REQ_SW_RST	R/W	7h	Data should be loaded as multibit. Write 3b000 to assert warm reset from SW Write 3 b111 to deassert warm reset from SW if this is the only source of warm reset Reset Source: mod_g_rst_n

2.5.4 CFG0_WARM_RST_CAUSE Registers

2.5.4.1 CFG0_RST_CAUSE Register (Offset = Ch) [reset = 41h]

Short Description:

Long Description:

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Table 2-1441. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 000Ch

Figure 2-717. WARM_RST_CAUSE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								SYS_RST_CAUSE_CAUSE							
NONE								R							
186a0								41h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYS_RST_CAUSE_CAUSE															
R															
41h															

Access Types Legend

Table 2-1442. WARM_RST_CAUSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved

Table 2-1442. WARM_RST_CAUSE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	SYS_RST_CAUSE_CAUSE	R	41h	System Reset Cause register 24b0000_0000_0000_0000_0100_0001 - POR reset 24 b0000_0000_0000_0000_0100_0010 - Warm reset due to MSS_WDT0 24 b0000_0000_0000_0000_0100_0100 - Warm reset due to MSS_WDT1 24 b0000_0000_0000_0000_0100_1000 - Warm reset due to MSS_WDT2 24 b0000_0000_0000_0000_0101_0000 - Warm reset due to MSS_WDT3 24 b0000_0000_0000_0000_0110_0000 - Warm reset due to TOP_RMC:WARM_RESET_REQ 24 b0000_0000_0000_0000_0100_0000 - External Pad reset 24 b0000_0000_0000_0000_1100_0000 - Warm reset due to HSM_WDT 24 b0000_0000_0000_0001_0100_0000 - Warm Reset due to Deugger reset 24 b0000_0000_0000_0010_0100_0000 - Warm Reset due to Temp Sense0 Reset 24 b0000_0000_0000_0100_0100_0000 - Warm Reset due to Temp Sense1 Reset 24 b0000_0000_0000_1000_0100_0000 - Warm Reset due to vmon_cmp1_ov 24 b0000_0000_0001_0000_0100_0000 - Warm Reset due to vmon_cmp2_ov 24 b0000_0000_0010_0000_0100_0000 - Warm Reset due to vmon_cmp3_ov 24 b0000_0000_0100_0000_0100_0000 - Warm Reset due to vmon_cmp5_ov 24 b0000_0000_1000_0000_0100_0000 - Warm Reset due to vmon_cmp0_uv 24 b0000_0001_0000_0000_0100_0000 - Warm Reset due to vmon_cmp1_uv 24 b0000_0010_0000_0000_0100_0000 - Warm Reset due to vmon_cmp2_uv 24 b0000_0100_0000_0000_0100_0000 - Warm Reset due to vmon_cmp3_uv 24 b0000_1000_0000_0000_0100_0000 - Warm Reset due to vmon_cmp5_uv 24 b0001_0000_0000_0000_0100_0000 - Warm Reset due to vmon_cmp7_uv 24 b0010_0000_0000_0000_0100_0000 - Warm Reset due to vmon_cmp8_uv 24 b0100_0000_0000_0000_0100_0000 - Warm Reset due to esm 24 b1000_0000_0000_0000_0100_0000 - Warm Reset due to clk_loss on sys_clk Reset Source: mod_g_rst_n

2.5.5 CFG0_WARM_RST_CAUSE_CLR Registers

2.5.5.1 CFG0_RST_CAUSE_CLR Register (Offset = 10h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1443. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0010h

Figure 2-718. WARM_RST_CAUSE_CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													SYS_RST_CAUSE_CLR_CLEAR		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1444. WARM_RST_CAUSE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	SYS_RST_CAUSE_CLR_CLEAR	R/W	0h	Write pulse bit field: Data should be loaded as multibit. System Reset Cause register Clear Reset Source: mod_g_rst_n

2.5.6 CFG0_RCOSC32K_CTRL Registers

2.5.6.1 CFG0_CTRL Register (Offset = 14h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1445. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0014h

Figure 2-719. RCOSC32K_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													RCOSC32K_CTRL_STOPOSC		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1446. RCOSC32K_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	RCOSC32K_CTRL_STOPOSC	R/W	0h	Stop 32KHz RCOSC. Write 3b111 to stop clock Reset Source: mod_g_rst_n

2.5.7 CFG0_LIMP_MODE_EN Registers

2.5.7.1 CFG0_MODE_EN Register (Offset = 18h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1447. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0018h

Figure 2-720. LIMP_MODE_EN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					LIMP_MODE_EN_COREPLL_LOSS_EN			RESERVED	LIMP_MODE_EN_XTALCLK_LOSS_EN			RESERVED	LIMP_MODE_EN_DCC0_ERROR_EN		
NONE					R/W			NONE	R/W			NONE	R/W		
0					0h			0	0h			0	0h		

Access Types Legend

Table 2-1448. LIMP_MODE_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE		Reserved
10:8	LIMP_MODE_EN_COREPLL_LOSS_EN	R/W	0h	Enable for core pll phase lock loss to generate Limp mode 3b000: will not generate Limp mode (multibit 000) 3 b111 : will generate Limp mode (multibit 111) Reset Source: mod_g_rst_n
7	RESERVED	NONE		Reserved
6:4	LIMP_MODE_EN_XTALCLK_LOSS_EN	R/W	0h	Enable for crystal_clock_loss to generate Limp mode 3b000: will not generate Limp mode (multibit 000) 3 b111 : will generate Limp mode (multibit 111) Reset Source: mod_g_rst_n
3	RESERVED	NONE		Reserved
2:0	LIMP_MODE_EN_DCC0_ERROR_EN	R/W	0h	Enable DCC0 Error to generate Limp mode 3b000: DCC0 Error will not generate Limp mode (multibit 000) 3 b111 : DCC0 Error will generate Limp mode (multibit 111) Reset Source: mod_g_rst_n

2.5.8 CFG0_PLL_REF_CLK_SRC_SEL Registers

2.5.8.1 CFG0_REF_CLK_SRC_SEL Register (Offset = 1Ch) [reset = 0h]

Short Description:

Long Description:

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Table 2-1449. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 001Ch

Figure 2-721. PLL_REF_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									PLL_REF_CLK_SRC_SEL_PLL_PERI_REF_CLK_SRC_SEL			RESERVED	PLL_REF_CLK_SRC_SEL_PLL_CORE_REF_CLK_SRC_SEL		
NONE									R/W			NONE	R/W		
0									0h			0	0h		

Access Types Legend

Table 2-1450. PLL_REF_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE		Reserved
6:4	PLL_REF_CLK_SRC_SEL_PLL_PERI_REF_CLK_SRC_SEL	R/W	0h	Mux selct for PERI PLL REF clock Write 3b111 : to select external reference clock as PLL reference clock Write 3 b000 : to select on-die clock as PLL reference clock Reset Source: mod_g_rst_n
3	RESERVED	NONE		Reserved
2:0	PLL_REF_CLK_SRC_SEL_PLL_CORE_REF_CLK_SRC_SEL	R/W	0h	Mux selct for CORE PLL REF clock Write 3b111 : to select external reference clock as PLL reference clock Write 3 b000 : to select on-die clock as PLL reference clock Reset Source: mod_g_rst_n

2.5.9 CFG0_PAD_XTAL_CTRL Registers

2.5.9.1 CFG0_XTAL_CTRL Register (Offset = 20h) [reset = 1h]

Short Description:

Long Description:

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Table 2-1451. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0020h

Figure 2-722. PAD_XTAL_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												PAD_XTAL_CTRL_XTAL_XI_OE_N	PAD_XTAL_CTRL_XTAL_XO_RESSELECT	PAD_XTAL_CTRL_XTAL_XO_SW2	PAD_XTAL_CTRL_XTAL_XO_SW1
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	1h

Access Types Legend

Table 2-1452. PAD_XTAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	PAD_XTAL_CTRL_XTAL_XI_OE_N	R/W	0h	When gz is low, the padxo output is enabled, padxi to padxo is a single stage inverter, and the oscillator can oscillate with an external crystal plus capacitors/resistor. When gz is high, padxo is in high impedance mode, padxi and Y are driven low, and the oscillator is disabled. With gz high, the internal bias resistor between padxi and padxo is disconnected regardless of the state of resselect. Reset Source: mod_g_rst_n
2	PAD_XTAL_CTRL_XTAL_XO_RESSELECT	R/W	0h	When resselect is low, an internal 1Meg Ohm resistor is connected between padxi and padxo for oscillator bias.When resselect is asserted (high), the internal resistor is disconnected.For oscillation with a crystal while resselect is high, an external resistor must be connected between padxi and padxo to provide bias. Reset Source: mod_g_rst_n
1	PAD_XTAL_CTRL_XTAL_XO_SW2	R/W	0h	XTAL pad control bit frequency selection pin SW2 Based on table below sw2 sw1 Freq of operation 0 0 5 20 MHz 0 1 15 35 MHz 1 0 30 40 MHz 1 1 40 55 MHz Reset Source: mod_g_rst_n
0	PAD_XTAL_CTRL_XTAL_XO_SW1	R/W	1h	XTAL pad control bit frequency selection pin SW1 Based on table below sw2 sw1 Freq of operation 0 0 5 20 MHz 0 1 15 35 MHz 1 0 30 40 MHz 1 1 40 55 MHz Reset Source: mod_g_rst_n

2.5.10 CFG0_SOP_MODE_VALUE Registers

2.5.10.1 CFG0_MODE_VALUE Register (Offset = 24h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1453. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0024h

Figure 2-723. SOP_MODE_VALUE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SOP_MODE_VALUE_VAL															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOP_MODE_VALUE_VAL															
R															
0h															

Access Types Legend

Table 2-1454. SOP_MODE_VALUE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SOP_MODE_VALUE_VAL	R	0h	See below table SOP_MODE values and its corresponding mapping SOP_PAD3 SOP_PAD2 SOP_PAD1 SOP_PAD0 bootmode 0 0 0 0 QSPI Functional mode(4S) 0 0 0 1 UART Functional mode 0 0 1 0 QSPI Functional mode(1S) values from 3 to 7 is reserved for future use 1 0 0 0 THB(test) mode 1 0 0 1 ATPG mode 1 0 1 0 FLED mode (Debug SoP mode) values from B to F is reserved for future use reset value of MMR is 0 but it will latch on to the SOP mode values after reset is released. when CPU reads the MMR it will show the latched SOP mode value only Reset Source: mod_g_rst_n

2.5.11 CFG0_CLK_LOSS_STATUS Registers

2.5.11.1 CFG0_LOSS_STATUS Register (Offset = 28h) [reset = 100h]

Short Description:

Long Description:

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Table 2-1455. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0028h

Figure 2-724. CLK_LOSS_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
989680															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLK_LOSS_STATUS_RC_GOOD_BOOT	RESERVED			CLK_LOSS_STATUS_RC_CLOCK_LOSS	RESERVED			CLK_LOSS_STATUS_CRYSTAL_CLOCK_LOSS
NONE							R	NONE			R	NONE			R
989680							1h	0			0h	0			0h

Access Types Legend

Table 2-1456. CLK_LOSS_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE		Reserved
8	CLK_LOSS_STATUS_RC_GOOD_BOOT	R	1h	Clock status of RC clock at boot. Reset value will reflect the actual status 1 -- clock present at boot 0 -- clock not present at boot Reset Source: mod_g_rst_n
7:5	RESERVED	NONE		Reserved
4	CLK_LOSS_STATUS_RC_CLOCK_LOSS	R	0h	Coarse detection clock loss status for RC clock. Reset value will reflect the actual status 1 -- clock lost 0 -- clock good Reset Source: mod_g_rst_n
3:1	RESERVED	NONE		Reserved
0	CLK_LOSS_STATUS_CRYSTAL_CLOCK_LOSS	R	0h	Coarse detection clock loss status for Crystal clock. Reset value will reflect the actual status 1 -- clock lost 0 -- clock good Reset Source: mod_g_rst_n

2.5.12 CFG0_WARM_RSTTIME1 Registers

2.5.12.1 CFG0_RSTTIME1 Register (Offset = 30h) [reset = 888h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1457. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0030h

Figure 2-725. WARM_RSTTIME1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
2541b26a4															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				WARM_RSTTIME1_DELAY											
NONE				R/W											
2541b26a4				888h											

Access Types Legend

Table 2-1458. WARM_RSTTIME1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	WARM_RSTTIME1_DELAY	R/W	888h	programing Output delay Data should be loaded as multibit. For example: if value of 0x5 should be selected then 0x555 should be configured to the register. **Note: This bit will only be reset by PORz. Reset Source: mod_por_rst_n

2.5.13 CFG0_WARM_RSTTIME2 Registers

2.5.13.1 CFG0_RSTTIME2 Register (Offset = 34h) [reset = 888h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1459. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0034h

Figure 2-726. WARM_RSTTIME2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
2541b26a4															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				WARM_RSTTIME2_DELAY											
NONE				R/W											
2541b26a4				888h											

Access Types Legend

Table 2-1460. WARM_RSTTIME2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	WARM_RSTTIME2_DELAY	R/W	888h	programing input Rise delay Data should be loaded as multibit. For example: if value of 0x5 should be selected then 0x555 should be configured to the register. **Note: This bit will only be reset by PORz. Reset Source: mod_por_rst_n

2.5.14 CFG0_WARM_RSTTIME3 Registers

2.5.14.1 CFG0_RSTTIME3 Register (Offset = 38h) [reset = 111h]

Short Description:

Long Description:

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Table 2-1461. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0038h

Figure 2-727. WARM_RSTTIME3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
989a68															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				WARM_RSTTIME3_DELAY											
NONE				R/W											
989a68				111h											

Access Types Legend

Table 2-1462. WARM_RSTTIME3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	WARM_RSTTIME3_DELAY	R/W	111h	programing Input Fall delay Data should be loaded as multibit. For example: if value of 0x5 should be selected then 0x555 should be configured to the register. **Note: This bit will only be reset by PORz. Reset Source: mod_por_rst_n

2.5.15 CFG0_WARM_RESET_CONFIG_OV Registers

2.5.15.1 CFG0_RESET_CONFIG_OV Register (Offset = 3Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1463. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 003Ch

Figure 2-728. WARM_RESET_CONFIG_OV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				WARM_RESET_CONFIG_OV_VMON_CMP5_OV_RST_EN			WARM_RESET_CONFIG_OV_VMON_CMP3_OV_RST_EN			WARM_RESET_CONFIG_OV_VMON_CMP2_OV_RST_EN			WARM_RESET_CONFIG_OV_VMON_CMP1_OV_RST_EN		
NONE				R/W			R/W			R/W			R/W		
0				0h			0h			0h			0h		

Access Types Legend

Table 2-1464. WARM_RESET_CONFIG_OV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:9	WARM_RESET_CONFIG_OV_VMON_CMP5_OV_RST_EN	R/W	0h	Enable/Disable VMON Overvoltage CMP5 triggering Warm Reset Data should be loaded as multibit. Write 3b000 to disable vmon_ov rst_en Write 3 b111 to enable vmon_ov rst_en **Note: This bit will only be reset by PORz. Reset Source: mod_por_rst_n
8:6	WARM_RESET_CONFIG_OV_VMON_CMP3_OV_RST_EN	R/W	0h	Enable/Disable VMON Overvoltage CMP3 triggering Warm Reset Data should be loaded as multibit. Write 3b000 to disable vmon_ov rst_en Write 3 b111 to enable vmon_ov rst_en **Note: This bit will only be reset by PORz. Reset Source: mod_por_rst_n
5:3	WARM_RESET_CONFIG_OV_VMON_CMP2_OV_RST_EN	R/W	0h	Enable/Disable VMON Overvoltage CMP2 triggering Warm Reset Data should be loaded as multibit. Write 3b000 to disable vmon_ov rst_en Write 3 b111 to enable vmon_ov rst_en **Note: This bit will only be reset by PORz. Reset Source: mod_por_rst_n
2:0	WARM_RESET_CONFIG_OV_VMON_CMP1_OV_RST_EN	R/W	0h	Enable/Disable VMON Overvoltage CMP1 triggering Warm Reset Data should be loaded as multibit. Write 3b000 to disable vmon_ov rst_en Write 3 b111 to enable vmon_ov rst_en **Note: This bit will only be reset by PORz. Reset Source: mod_por_rst_n

2.5.16 CFG0_WARM_RESET_CONFIG_UV Registers

2.5.16.1 CFG0_RESET_CONFIG_UV Register (Offset = 40h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1465. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0040h

Figure 2-729. WARM_RESET_CONFIG_UV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED											WARM_RESET_CONFIG_UV_VMON_CMP8_UV_RST_EN			WARM_RESET_CONFIG_UV_VMON_CMP7_UV_RST_EN	
NONE											R/W			R/W	
0											0h			0h	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WARM_RESET_CONFIG_UV_VMON_CMP7_UV_RST_EN	WARM_RESET_CONFIG_UV_VMON_CMP5_UV_RST_EN			WARM_RESET_CONFIG_UV_VMON_CMP3_UV_RST_EN			WARM_RESET_CONFIG_UV_VMON_CMP2_UV_RST_EN			WARM_RESET_CONFIG_UV_VMON_CMP1_UV_RST_EN			WARM_RESET_CONFIG_UV_VMON_CMP0_UV_RST_EN		
R/W	R/W			R/W			R/W			R/W			R/W		
0h	0h			0h			0h			0h			0h		

Access Types Legend

Table 2-1466. WARM_RESET_CONFIG_UV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE		Reserved
20:18	WARM_RESET_CONFIG_UV_VMON_CMP8_UV_RST_EN	R/W	0h	Enable/Disable VMON Undervoltage CMP8 triggering Warm Reset Data should be loaded as multibit. Write 3b000 to disable vmon_uv rst_en Write 3 b111 to enable vmon_uv rst_en **Note: This bit will only be reset by PORz. Reset Source: mod_por_rst_n
17:15	WARM_RESET_CONFIG_UV_VMON_CMP7_UV_RST_EN	R/W	0h	Enable/Disable VMON Undervoltage CMP7 triggering Warm Reset Data should be loaded as multibit. Write 3b000 to disable vmon_uv rst_en Write 3 b111 to enable vmon_uv rst_en **Note: This bit will only be reset by PORz. Reset Source: mod_por_rst_n
14:12	WARM_RESET_CONFIG_UV_VMON_CMP5_UV_RST_EN	R/W	0h	Enable/Disable VMON Undervoltage CMP5 triggering Warm Reset Data should be loaded as multibit. Write 3b000 to disable vmon_uv rst_en Write 3 b111 to enable vmon_uv rst_en **Note: This bit will only be reset by PORz. Reset Source: mod_por_rst_n
11:9	WARM_RESET_CONFIG_UV_VMON_CMP3_UV_RST_EN	R/W	0h	Enable/Disable VMON Undervoltage CMP3 triggering Warm Reset Data should be loaded as multibit. Write 3b000 to disable vmon_uv rst_en Write 3 b111 to enable vmon_uv rst_en **Note: This bit will only be reset by PORz. Reset Source: mod_por_rst_n
8:6	WARM_RESET_CONFIG_UV_VMON_CMP2_UV_RST_EN	R/W	0h	Enable/Disable VMON Undervoltage CMP2 triggering Warm Reset Data should be loaded as multibit. Write 3b000 to disable vmon_uv rst_en Write 3 b111 to enable vmon_uv rst_en **Note: This bit will only be reset by PORz. Reset Source: mod_por_rst_n

Table 2-1466. WARM_RESET_CONFIG_UV Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:3	WARM_RESET_CONFIG_UV_VMON_CMP1_UV_RST_EN	R/W	0h	Enable/Disable VMON Undervoltage CMP1 triggering Warm Reset Data should be loaded as multibit. Write 3b000 to disable vmon_uv rst_en Write 3 b111 to enable vmon_uv rst_en **Note: This bit will only be reset by PORz. Reset Source: mod_por_rst_n
2:0	WARM_RESET_CONFIG_UV_VMON_CMP0_UV_RST_EN	R/W	0h	Enable/Disable VMON Undervoltage CMP0 triggering Warm Reset Data should be loaded as multibit. Write 3b000 to disable vmon_uv rst_en Write 3 b111 to enable vmon_uv rst_en **Note: This bit will only be reset by PORz. Reset Source: mod_por_rst_n

2.5.17 CFG0_WARM_RESET_CONFIG_MISC Registers

2.5.17.1 CFG0_RESET_CONFIG_MISC Register (Offset = 44h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1467. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0044h

Figure 2-730. WARM_RESET_CONFIG_MISC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										WARM_RESET_CONFIG_MISC_CLK_LOSS_SYS_CLK_RST_EN			WARM_RESET_CONFIG_MISC_ESM_RST_EN		
NONE										R/W			R/W		
0										0h			0h		

Access Types Legend

Table 2-1468. WARM_RESET_CONFIG_MISC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE		Reserved
5:3	WARM_RESET_CONFIG_MISC_CLK_LOSS_SYS_CLK_RST_EN	R/W	0h	Enable/Disable Clock loss on SYS_CLK triggering Warm Reset Data should be loaded as multibit. Write 3b000 to disable clk_loss on sys_clk rst_en Write 3 b111 to enable clk_loss on sys_clk rst_en Reset Source: mod_g_rst_n
2:0	WARM_RESET_CONFIG_MISC_ESM_RST_EN	R/W	0h	Enable/Disable ESM triggering Warm Reset Data should be loaded as multibit. Write 3b000 to disable esm rst_en Write 3 b111 to enable esm rst_en Reset Source: mod_g_rst_n

2.5.18 CFG0_PLL_CORE_PWRCTRL Registers

2.5.18.1 CFG0_CORE_PWRCTRL Register (Offset = 400h) [reset = 30h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1469. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0400h

Figure 2-731. PLL_CORE_PWRCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
2af8															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										PLL_CORE_PWRCTRL_PONIN	PLL_CORE_PWRCTRL_PGOODIN	PLL_CORE_PWRCTRL_RET	PLL_CORE_PWRCTRL_ISORET	PLL_CORE_PWRCTRL_ISOSCAN	PLL_CORE_PWRCTRL_OFFMODE
NONE										R/W	R/W	R/W	R/W	R/W	R/W
2af8										1h	1h	0h	0h	0h	0h

Access Types Legend

Table 2-1470. PLL_CORE_PWRCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE		Reserved
5	PLL_CORE_PWRCTRL_PONIN	R/W	1h	ON/OFF control of the weak power switch digital. For functional mode it should be 1 Reset Source: mod_g_rst_n
4	PLL_CORE_PWRCTRL_PGOODIN	R/W	1h	ON/OFF control of the strong power switch digital. For functional mode it should be 1 Reset Source: mod_g_rst_n
3	PLL_CORE_PWRCTRL_RET	R/W	0h	Save/Restore control for Retention mode. For functional mode it should be 0 Reset Source: mod_g_rst_n
2	PLL_CORE_PWRCTRL_ISORET	R/W	0h	Save/Restore control for Isolation of output pins For functional mode it should be 0 Reset Source: mod_g_rst_n
1	PLL_CORE_PWRCTRL_ISOSCAN	R/W	0h	Save/Restore control for Isolation of the Scanout pins. For functional mode it should be 0 Reset Source: mod_g_rst_n
0	PLL_CORE_PWRCTRL_OFFMODE	R/W	0h	Used to switch OFF the logic on VDDA. For functional mode it should be 0 Reset Source: mod_g_rst_n

2.5.19 CFG0_PLL_CORE_CLKCTRL Registers

2.5.19.1 CFG0_CORE_CLKCTRL Register (Offset = 404h) [reset = 895000h]

Short Description:

Long Description:

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Table 2-1471. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0404h

Figure 2-732. PLL_CORE_CLKCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PLL_CORE_CLKCTRL_CYCLESLIPEN	PLL_CORE_CLKCTRL_ENSSC	PLL_CORE_CLKCTRL_CLKDCOLDOEN	RESERVED					PLL_CORE_CLKCTRL_IDLE	PLL_CORE_CLKCTRL_BYPASSACKZ	PLL_CORE_CLKCTRL_STBYRET	PLL_CORE_CLKCTRL_CLKOUTEN	PLL_CORE_CLKCTRL_CLKOUTLDOEN	PLL_CORE_CLKCTRL_ULOWCLKEN	PLL_CORE_CLKCTRL_CLKDCOLDOPWDNZ	PLL_CORE_CLKCTRL_M2PWDNZ
R/W	R/W	R/W	NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0					1h	0h	0h	0h	1h	0h	0h	1h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	PLL_CORE_CLKCTRL_STOPMODE	RESERVED	PLL_CORE_CLKCTRL_SELFREQDCO			RESERVED	PLL_CORE_CLKCTRL_RELAXED_LOCK	RESERVED						PLL_CORE_CLKCTRL_SSCTYPE	PLL_CORE_CLKCTRL_TINTZ
NONE	R/W	NONE	R/W			NONE	R/W	NONE						R/W	R/W
1	1h	0	4h			0	0h	0						0h	0h

Access Types Legend

Table 2-1472. PLL_CORE_CLKCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PLL_CORE_CLKCTRL_CYCLESLIPEN	R/W	0h	FailSafe enable to trigger re-calibration in case CycleSlip occurs between REFCLK and FBCLK. Reset Source: mod_g_rst_n
30	PLL_CORE_CLKCTRL_ENSSC	R/W	0h	Controls Clock Spreading. SSC is not supported. Should be set to 0x0 to disable clock spreading. Reset Source: mod_g_rst_n
29	PLL_CORE_CLKCTRL_CLKDCOLDOEN	R/W	0h	Synchronously enables/disables CLKDCOLDO 0x0 : synchronously disables CLKDCOLDO 0x1 : synchronously enables CLKDCOLDO Reset Source: mod_g_rst_n
28:24	RESERVED	NONE		Reserved
23	PLL_CORE_CLKCTRL_IDLE	R/W	1h	Sets PLL to Idle mode 0x0 : When SYSRESET = 0 and TINITZ = 1 IDLE = 0 PLL will go to Active and Locked 0x1 : When SYSRESET = 0 and TINITZ = 1 IDLE = 1 PLL will go to Idle Bypass low powe Reset Source: mod_g_rst_n
22	PLL_CORE_CLKCTRL_BYPASSACKZ	R/W	0h	BYPASSACKZ is a special purpose input to the module. In general this input is expected to be tied to static low. For the output clocks of the module that do not have an internal bypass mux viz. CLKDCOLDO and CLKOUTLDO, a bypass mux could be implemented external to the module. Reset Source: mod_g_rst_n
21	PLL_CORE_CLKCTRL_STBYRET	R/W	0h	Standby retention control 0x0 : prepares ADPLLLJ for relock when out of retention by removing the gating on all internal clocks. 0x1 : prepares ADPLLLJ for retention by gating all the internal clocks. Reset Source: mod_g_rst_n

Table 2-1472. PLL_CORE_CLKCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	PLL_CORE_CLKCTRL_CLKOUTEN	R/W	0h	CLKOUT enable or disable 0x0 : synchronously disables CLKOUT 0x1 : synchronously enables CLKOUT Reset Source: mod_g_rst_n
19	PLL_CORE_CLKCTRL_CLKOUTLDOEN	R/W	1h	Synchronously enables/disables CLKOUTLDO 0x0 : synchronously disables CLKOUTLDO 0x1 : synchronously enables CLKOUTLDO Reset Source: mod_g_rst_n
18	PLL_CORE_CLKCTRL_ULOWCLKEN	R/W	0h	Select CLKOUT source in bypass 0x0: When ADPLLLJ in bypass mode, CLKOUT = CLKINP/(N2+1) 0x1: When ADPLLLJ in bypass mode, CLKOUT = CLKINPULOW. Reset Source: mod_g_rst_n
17	PLL_CORE_CLKCTRL_CLKDCOLDOPWDNZ	R/W	0h	0 Asynchronous power down for CLKDCOLDO o/p. Reset Source: mod_g_rst_n
16	PLL_CORE_CLKCTRL_M2PWDNZ	R/W	1h	M2 divider power down mode 0x0: Asynchronous power down for M2 divider 0x1 : M2 divider is functional Reset Source: mod_g_rst_n
15	RESERVED	NONE		Reserved
14	PLL_CORE_CLKCTRL_STOPMODE	R/W	1h	When in Lossclk/Stbyret 0x0 : Limp mode 0x1 : Stopmode Reset Source: mod_g_rst_n
13	RESERVED	NONE		Reserved
12:10	PLL_CORE_CLKCTRL_SELFREQDCO	R/W	4h	DCO Clock (DCOCLK = CLKINP * [M/(N+1)]) frequency range selector. 0x0: Reserved 0x2: HS2 : DCOCLK range is from 500 MHz to 1000 MHz 0x3: Reserved 0x4: HS1: DCOCLK range is from 1000 MHz to 2000 MHz 0x5: Reserved Reset Source: mod_g_rst_n
9	RESERVED	NONE		Reserved
8	PLL_CORE_CLKCTRL_RELAXED_LOCK	R/W	0h	Decides when FREQLOCK asserted 0x0: FREQLOCK asserted when DC frequency error less than 1% 0x1: FREQLOCK asserted when DC frequency error less than 2% Reset Source: mod_g_rst_n
7:2	RESERVED	NONE		Reserved
1	PLL_CORE_CLKCTRL_SSCTYPE	R/W	0h	SSC Type Reset Source: mod_g_rst_n
0	PLL_CORE_CLKCTRL_TINTZ	R/W	0h	PLL core soft reset Reset Source: mod_g_rst_n

2.5.20 CFG0_PLL_CORE_TENABLE Registers

2.5.20.1 CFG0_CORE_TENABLE Register (Offset = 408h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1473. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0408h

Figure 2-733. PLL_CORE_TENABLE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															PLL_CORE_TENABLE_TENABLE
NONE															R/W
0															0h

Access Types Legend

Table 2-1474. PLL_CORE_TENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	PLL_CORE_TENABLE_TENABLE	R/W	0h	M, N. SD and SELFREQDCO latch (active rise edge) Reset Source: mod_g_rst_n

2.5.21 CFG0_PLL_CORE_TENABLEDIV Registers

2.5.21.1 CFG0_CORE_TENABLEDIV Register (Offset = 40Ch) [reset = 0h]

Short Description:

Long Description:

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Table 2-1475. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 040Ch

Figure 2-734. PLL_CORE_TENABLEDIV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															PLL_CORE_TENABLEDIV_TENABLEDIV
NONE															R/W
0															0h

Access Types Legend

Table 2-1476. PLL_CORE_TENABLEDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	PLL_CORE_TENABLEDIV_TENABLEDIV	R/W	0h	M2 and N2 latch (active rise edge) Reset Source: mod_g_rst_n

2.5.22 CFG0_PLL_CORE_M2NDIV Registers

2.5.22.1 CFG0_CORE_M2NDIV Register (Offset = 410h) [reset = 13h]

Short Description:

Long Description:

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Table 2-1477. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0410h

Figure 2-735. PLL_CORE_M2NDIV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED									PLL_CORE_M2NDIV_M2						
NONE									R/W						
3e9									0h						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PLL_CORE_M2NDIV_N							
NONE								R/W							
0								13h							

Access Types Legend

Table 2-1478. PLL_CORE_M2NDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE		Reserved
22:16	PLL_CORE_M2NDIV_M2	R/W	0h	Post-divider is REGM2 Reset Source: mod_g_rst_n
15:8	RESERVED	NONE		Reserved
7:0	PLL_CORE_M2NDIV_N	R/W	13h	Pre-divider is REGN+1 Reset Source: mod_g_rst_n

2.5.23 CFG0_PLL_CORE_MN2DIV Registers

2.5.23.1 CFG0_CORE_MN2DIV Register (Offset = 414h) [reset = 640h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1479. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0414h

Figure 2-736. PLL_CORE_MN2DIV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PLL_CORE_MN2DIV_N2			
NONE												R/W			
419231a0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PLL_CORE_MN2DIV_M											
NONE				R/W											
0				640h											

Access Types Legend

Table 2-1480. PLL_CORE_MN2DIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:16	PLL_CORE_MN2DIV_N2	R/W	0h	Bypass divider is REGN2+1 Reset Source: mod_g_rst_n
15:12	RESERVED	NONE		Reserved
11:0	PLL_CORE_MN2DIV_M	R/W	640h	Feedback Multiplier is REGM Reset Source: mod_g_rst_n

2.5.24 CFG0_PLL_CORE_FRACDIV Registers

2.5.24.1 CFG0_CORE_FRACDIV Register (Offset = 418h) [reset = 8000000h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1481. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0418h

Figure 2-737. PLL_CORE_FRACDIV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PLL_CORE_FRACDIV_REGSD								RESERVED						PLL_CORE_FRACDIV_FRACTIONALM	
R/W								NONE						R/W	
8h								0						0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_CORE_FRACDIV_FRACTIONALM															
R/W															
0h															

Access Types Legend

Table 2-1482. PLL_CORE_FRACDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PLL_CORE_FRACDIV_REGSD	R/W	8h	Sigma-Delta Divider Should be set by s/w to provide optimum jitter performance. DPLL_SD_DIV = CEILING ([DPLL_MULT/ (DPLL_DIV+1)] * CLKINP/ 250), where CLKINP is the input clock of the DPLL in MHz Reset Source: mod_g_rst_n
23:18	RESERVED	NONE		Reserved
17:0	PLL_CORE_FRACDIV_FRACTIONALM	R/W	0h	Fractional part of the M divider. Reset Source: mod_g_rst_n

2.5.25 CFG0_PLL_CORE_BWCTRL Registers

2.5.25.1 CFG0_CORE_BWCTRL Register (Offset = 41Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1483. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 041Ch

Figure 2-738. PLL_CORE_BWCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													PLL_CORE_BWCTRL_BWCONTROL		PLL_CORE_BWCTRL_BW_INCR_DECRZ
NONE													R/W		R/W
0													0h		0h

Access Types Legend

Table 2-1484. PLL_CORE_BWCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:1	PLL_CORE_BWCTRL_BWCONTROL	R/W	0h	Change Loop Bandwidth Reset Source: mod_g_rst_n
0	PLL_CORE_BWCTRL_BW_INCR_DECRZ	R/W	0h	Direction of Loop Bandwidth 0x0 : decrease BW 0x1 : increase BW Reset Source: mod_g_rst_n

2.5.26 CFG0_PLL_CORE_FRACCTRL Registers

2.5.26.1 CFG0_CORE_FRACCTRL Register (Offset = 420h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1485. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0420h

Figure 2-739. PLL_CORE_FRACCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PLL_CORE_FRACCTRL_DOWNSPREAD	PLL_CORE_FRACCTRL_MODFREQDIVIDEREXPONENT			PLL_CORE_FRACCTRL_MODFREQDIVIDERMANTISSA							PLL_CORE_FRACCTRL_DELTAMSTEPINTEGER			PLL_CORE_FRACCTRL_DELTAMSTEPFRACTION	
R/W	R/W			R/W							R/W			R/W	
0h	0h			0h							0h			0h	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_CORE_FRACCTRL_DELTAMSTEPFRACTION															
R/W															
0h															

Access Types Legend

Table 2-1486. PLL_CORE_FRACCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PLL_CORE_FRACCTRL_DOWNSPREAD	R/W	0h	Controls frequency spread 0x0 : enables both side frequency spread about the programmed frequency. 0x1 : enables low frequency spread only Reset Source: mod_g_rst_n
30:28	PLL_CORE_FRACCTRL_MODFREQDIVIDEREXPONENT	R/W	0h	Exponent of the REFCLK divider to define the modulation frequency. Reset Source: mod_g_rst_n
27:21	PLL_CORE_FRACCTRL_MODFREQDIVIDERMANTISSA	R/W	0h	Mantissa of the REFCLK divider to define the modulation frequency Reset Source: mod_g_rst_n
20:18	PLL_CORE_FRACCTRL_DELTAMSTEPINTEGER	R/W	0h	Integer part of Frequency Spread control Reset Source: mod_g_rst_n
17:0	PLL_CORE_FRACCTRL_DELTAMSTEPFRACTION	R/W	0h	The fraction part of Frequency Spread control Reset Source: mod_g_rst_n

2.5.27 CFG0_PLL_CORE_STATUS Registers

2.5.27.1 CFG0_CORE_STATUS Register (Offset = 424h) [reset = e0001141h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1487. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0424h

Figure 2-740. PLL_CORE_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PLL_CORE_STATUS_PONOUT	PLL_CORE_STATUS_PGOODOUT	PLL_CORE_STATUS_LDOPWDN	PLL_CORE_STATUS_RECAL_BSTATUS3	PLL_CORE_STATUS_RECAL_OPPIN	RESERVED										
R	R	R	R	R	NONE										
1h	1h	1h	0h	0h	f42a5										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PLL_CORE_STATUS_CLKOUTLDOENACK	PLL_CORE_STATUS_CLKDCOLDOACK	PLL_CORE_STATUS_PHASELOCK	PLL_CORE_STATUS_FREQLOCK	PLL_CORE_STATUS_BYPASSACK	PLL_CORE_STATUS_STBYRETACK	PLL_CORE_STATUS_LOSSREF	PLL_CORE_STATUS_CLKOUTENACK	PLL_CORE_STATUS_LOCK2	PLL_CORE_STATUS_M2CHANGEACK	PLL_CORE_STATUS_SSCACK	PLL_CORE_STATUS_HIGHJITTER	PLL_CORE_STATUS_BYPASS
NONE			R	R	R	R	R	R	R	R	R	R	R	R	R
f42a5			1h	0h	0h	0h	1h	0h	1h	0h	0h	0h	0h	0h	1h

Access Types Legend

Table 2-1488. PLL_CORE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PLL_CORE_STATUS_PONOUT	R	1h	Status of the weak power-switch 0x0 : indicates the/OFF status of the weak power-switch in digital to SOC. 0x1 : ndicates the ON status of the weak power-switch in digital to SOC. Reset Source: mod_g_rst_n
30	PLL_CORE_STATUS_PGOODOUT	R	1h	Status of the strong power-switch 0x0 : indicates the/OFF status of the strong power-switch in digital to SOC. 0x1 : ndicates the ON status of the strong power-switch in digital to SOC. Reset Source: mod_g_rst_n
29	PLL_CORE_STATUS_LDOPWDN	R	1h	1 indicates ADPLLLJ internal LDO is power down. VDDLDOOUT will be un-defined in this condition Reset Source: mod_g_rst_n
28	PLL_CORE_STATUS_RECAL_BSTATUS3	R	0h	Recalibration status flag. 1 ADPLLLJ requires recalibration Reset Source: mod_g_rst_n
27	PLL_CORE_STATUS_RECAL_OPPIN	R	0h	Recalibration status flag. 1 ADPLLLJ requires recalibration Reset Source: mod_g_rst_n
26:13	RESERVED	NONE		Reserved
12	PLL_CORE_STATUS_CLKOUTLDOENACK	R	1h	Indicates the enable/disable condition of CLKOUTLDOEN 0x0 = CLKOUTLDO gating completed 0x1 = CLKOUTLDO enabling completed Reset Source: mod_g_rst_n

Table 2-1488. PLL_CORE_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	PLL_CORE_STATUS_CLKDCOLDOACK	R	0h	Indicates the enable/disable condition of CLKDCOLDOEN 0x0 = CLKDCOLDO gating completed 0x1 = CLKDCOLOD enabling completed Reset Source: mod_g_rst_n
10	PLL_CORE_STATUS_PHASELOCK	R	0h	Status on PHASELOCK output pin Reset Source: mod_g_rst_n
9	PLL_CORE_STATUS_FREQLOCK	R	0h	Status on FREQLOCK output pin Reset Source: mod_g_rst_n
8	PLL_CORE_STATUS_BYPASSACK	R	1h	Status of BYPASSACK output pin Reset Source: mod_g_rst_n
7	PLL_CORE_STATUS_STBYRETACK	R	0h	Standby and retention status 0x0: indicates to SOC that all internal clocks in ADPLLLJ are active and it is starting the relock process. 0x1: indicates to SOC that all internal clocks in ADPLLLJ are gated and it is ready for retention. Reset Source: mod_g_rst_n
6	PLL_CORE_STATUS_LOSSREF	R	1h	Reference input loss Reset Source: mod_g_rst_n
5	PLL_CORE_STATUS_CLKOUTENACK	R	0h	Indicates the enable/disable condition of CLKOUTEN 0x0 = CLKOUT gating completed 0x1 = CLKOUT enabling completed Reset Source: mod_g_rst_n
4	PLL_CORE_STATUS_LOCK2	R	0h	ADPLL internal loop lock status Reset Source: mod_g_rst_n
3	PLL_CORE_STATUS_M2CHANGEACK	R	0h	Acknowledge for change to M2 divider. Toggles from 1-0 or 0-1 (depending on current value) once CLKOUT frequency change has completed. Reset Source: mod_g_rst_n
2	PLL_CORE_STATUS_SSCACK	R	0h	Spread Spectrum status 0x0 : Spread-spectrum Clocking is disabled on output clocks 0x1 : Spread-spectrum Clocking is enabled on output clocks Reset Source: mod_g_rst_n
1	PLL_CORE_STATUS_HIGHJITTER	R	0h	1 indicates jitter. After PHASELOCK is asserted high, the HIGHJITTER flag is asserted high if phase error between REFCLK and FBCLK greater than 24%. Reset Source: mod_g_rst_n
0	PLL_CORE_STATUS_BYPASS	R	1h	Bypass status signal. 1 CLKOUT in bypass Reset Source: mod_g_rst_n

2.5.28 CFG0_PLL_CORE_HSDIVIDER Registers

2.5.28.1 CFG0_CORE_HSDIVIDER Register (Offset = 428h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1489. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0428h

Figure 2-741. PLL_CORE_HSDIVIDER Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														PLL_CORE_HSDIVIDER_LDOPWDNACK	PLL_CORE_HSDIVIDER_BYPASSACKZ
NONE														R	R
0														0h	0h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													PLL_CORE_HSDIVIDER_TENABLEDIV	PLL_CORE_HSDIVIDER_LDOPWDN	PLL_CORE_HSDIVIDER_BYPASS
NONE													R/W	R/W	R/W
0													0h	0h	0h

Access Types Legend

Table 2-1490. PLL_CORE_HSDIVIDER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE		Reserved
17	PLL_CORE_HSDIVIDER_LDOPWDNACK	R	0h	LDO Power Down Ack Reset Source: mod_g_rst_n
16	PLL_CORE_HSDIVIDER_BYPASSACKZ	R	0h	HSDIVIDER Bypass Ack Reset Source: mod_g_rst_n
15:3	RESERVED	NONE		Reserved
2	PLL_CORE_HSDIVIDER_TENABLEDIV	R/W	0h	Tenable Div Reset Source: mod_g_rst_n
1	PLL_CORE_HSDIVIDER_LDOPWDN	R/W	0h	LDO Power Down Reset Source: mod_g_rst_n
0	PLL_CORE_HSDIVIDER_BYPASS	R/W	0h	HSDIVIDER Bypass Reset Source: mod_g_rst_n

2.5.29 CFG0_PLL_CORE_HSDIVIDER_CLKOUT0 Registers

2.5.29.1 CFG0_CORE_HSDIVIDER_CLKOUT0 Register (Offset = 42Ch) [reset = 4h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1491. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 042Ch

Figure 2-742. PLL_CORE_HSDIVIDER_CLKOUT0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
a															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PLL_CORE_HSDIVIDER_CLKOUT0_PWDN	RESERVED		PLL_CORE_HSDIVIDER_CLKOUT0_STATUS	PLL_CORE_HSDIVIDER_CLKOUT0_GATE_CTRL	RESERVED		PLL_CORE_HSDIVIDER_CLKOUT0_DIVCHACK	PLL_CORE_HSDIVIDER_CLKOUT0_DIV				
NONE			R/W	NONE		R	R/W	NONE		R	R/W				
a			0h	0		0h	0h	0		0h	4h				

Access Types Legend

Table 2-1492. PLL_CORE_HSDIVIDER_CLKOUT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE		Reserved
12	PLL_CORE_HSDIVIDER_CLKOUT0_PWDN	R/W	0h	Power down for HSDIVIDER M4 divider and hence CLKOUT0 output 0h (R/W) = CLKOUT0 divider active 1h (R/W) = CLKOUT0 divider is powered down Reset Source: mod_g_rst_n
11:10	RESERVED	NONE		Reserved
9	PLL_CORE_HSDIVIDER_CLKOUT0_STATUS	R	0h	HSDIVIDER CLKOUT0 status 0h (R) = The clock output is gated 1h (R) = The clock output is enabled Reset Source: mod_g_rst_n
8	PLL_CORE_HSDIVIDER_CLKOUT0_GATE_CTRL	R/W	0h	Control gating of HSDIVIDER CLKOUT0 0h (R/W) = Automatically gate this clock when there is no dependency for it 1h (R/W) = Force this clock to stay enabled even if there is no request Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	PLL_CORE_HSDIVIDER_CLKOUT0_DIVCHACK	R	0h	Toggle on this status bit after changing HSDIVIDER_CLKOUT0_DIV indicates that the change in divider value has taken effect Reset Source: mod_g_rst_n
4:0	PLL_CORE_HSDIVIDER_CLKOUT0_DIV	R/W	4h	DPLL post-divider factor, M4, for internal clock generation. Divide values from 1 to 31. 0h (R/W) = Reserved Reset Source: mod_g_rst_n

2.5.30 CFG0_PLL_CORE_HSDIVIDER_CLKOUT1 Registers

2.5.30.1 CFG0_CORE_HSDIVIDER_CLKOUT1 Register (Offset = 430h) [reset = 3h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1493. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0430h

Figure 2-743. PLL_CORE_HSDIVIDER_CLKOUT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
1															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PLL_CORE_HSDIVIDER_CLKOUT1_PWDN	RESERVED		PLL_CORE_HSDIVIDER_CLKOUT1_STATUS	PLL_CORE_HSDIVIDER_CLKOUT1_GATE_CTRL	RESERVED		PLL_CORE_HSDIVIDER_CLKOUT1_DIVCHACK	PLL_CORE_HSDIVIDER_CLKOUT1_DIV				
NONE			R/W	NONE		R	R/W	NONE		R	R/W				
1			0h	0		0h	0h	0		0h	3h				

Access Types Legend

Table 2-1494. PLL_CORE_HSDIVIDER_CLKOUT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE		Reserved
12	PLL_CORE_HSDIVIDER_CLKOUT1_PWDN	R/W	0h	Power down for HSDIVIDER M5 divider and hence CLKOUT1 output 0h (R/W) = CLKOUT1 divider active 1h (R/W) = CLKOUT1 divider is powered down Reset Source: mod_g_rst_n
11:10	RESERVED	NONE		Reserved
9	PLL_CORE_HSDIVIDER_CLKOUT1_STATUS	R	0h	HSDIVIDER CLKOUT1 status 0h (R) = The clock output is gated 1h (R) = The clock output is enabled Reset Source: mod_g_rst_n
8	PLL_CORE_HSDIVIDER_CLKOUT1_GATE_CTRL	R/W	0h	Control gating of HSDIVIDER CLKOUT1 0h (R/W) = Automatically gate this clock when there is no dependency for it 1h (R/W) = Force this clock to stay enabled even if there is no request Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	PLL_CORE_HSDIVIDER_CLKOUT1_DIVCHACK	R	0h	Toggle on this status bit after changing HSDIVIDER_CLKOUT1_DIV indicates that the change in divider value has taken effect Reset Source: mod_g_rst_n
4:0	PLL_CORE_HSDIVIDER_CLKOUT1_DIV	R/W	3h	DPLL post-divider factor, M5, for internal clock generation. Divide values from 1 to 31. 0h (R/W) = Reserved Reset Source: mod_g_rst_n

2.5.31 CFG0_PLL_CORE_HSDIVIDER_CLKOUT2 Registers

2.5.31.1 CFG0_CORE_HSDIVIDER_CLKOUT2 Register (Offset = 434h) [reset = 4h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1495. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0434h

Figure 2-744. PLL_CORE_HSDIVIDER_CLKOUT2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
a															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PLL_CORE_HSDIVIDER_CLKOUT2_PWDN	RESERVED		PLL_CORE_HSDIVIDER_CLKOUT2_STATUS	PLL_CORE_HSDIVIDER_CLKOUT2_GATE_CTRL	RESERVED		PLL_CORE_HSDIVIDER_CLKOUT2_DIVCHACK	PLL_CORE_HSDIVIDER_CLKOUT2_DIV				
NONE			R/W	NONE		R	R/W	NONE		R	R/W				
a			0h	0		0h	0h	0		0h	4h				

Access Types Legend

Table 2-1496. PLL_CORE_HSDIVIDER_CLKOUT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE		Reserved
12	PLL_CORE_HSDIVIDER_CLKOUT2_PWDN	R/W	0h	Power down for HSDIVIDER M6 divider and hence CLKOUT2 output 0h (R/W) = CLKOUT2 divider active 1h (R/W) = CLKOUT2 divider is powered down Reset Source: mod_g_rst_n
11:10	RESERVED	NONE		Reserved
9	PLL_CORE_HSDIVIDER_CLKOUT2_STATUS	R	0h	HSDIVIDER CLKOUT2 status 0h (R) = The clock output is gated 1h (R) = The clock output is enabled Reset Source: mod_g_rst_n
8	PLL_CORE_HSDIVIDER_CLKOUT2_GATE_CTRL	R/W	0h	Control gating of HSDIVIDER CLKOUT2 0h (R/W) = Automatically gate this clock when there is no dependency for it 1h (R/W) = Force this clock to stay enabled even if there is no request Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	PLL_CORE_HSDIVIDER_CLKOUT2_DIVCHACK	R	0h	Toggle on this status bit after changing HSDIVIDER_CLKOUT2_DIV indicates that the change in divider value has taken effect Reset Source: mod_g_rst_n
4:0	PLL_CORE_HSDIVIDER_CLKOUT2_DIV	R/W	4h	DPLL post-divider factor, M6, for internal clock generation. Divide values from 1 to 31. 0h (R/W) = Reserved Reset Source: mod_g_rst_n

2.5.32 CFG0_PLL_CORE_HSDIVIDER_CLKOUT3 Registers

2.5.32.1 CFG0_CORE_HSDIVIDER_CLKOUT3 Register (Offset = 438h) [reset = 9h]

Short Description:

Long Description:

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Table 2-1497. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0438h

Figure 2-745. PLL_CORE_HSDIVIDER_CLKOUT3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
64															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PLL_CORE_HSDIVIDER_CLKOUT3_PWDN	RESERVED		PLL_CORE_HSDIVIDER_CLKOUT3_STATUS	PLL_CORE_HSDIVIDER_CLKOUT3_GATE_CTRL	RESERVED		PLL_CORE_HSDIVIDER_CLKOUT3_DIVCHACK	PLL_CORE_HSDIVIDER_CLKOUT3_DIV				
NONE			R/W	NONE		R	R/W	NONE		R	R/W				
64			0h	0		0h	0h	0		0h	9h				

Access Types Legend

Table 2-1498. PLL_CORE_HSDIVIDER_CLKOUT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE		Reserved
12	PLL_CORE_HSDIVIDER_CLKOUT3_PWDN	R/W	0h	Power down for HSDIVIDER M7 divider and hence CLKOUT3 output 0h (R/W) = CLKOUT3 divider active 1h (R/W) = CLKOUT3 divider is powered down Reset Source: mod_g_rst_n
11:10	RESERVED	NONE		Reserved
9	PLL_CORE_HSDIVIDER_CLKOUT3_STATUS	R	0h	HSDIVIDER CLKOUT3 status 0h (R) = The clock output is gated 1h (R) = The clock output is enabled Reset Source: mod_g_rst_n
8	PLL_CORE_HSDIVIDER_CLKOUT3_GATE_CTRL	R/W	0h	Control gating of HSDIVIDER CLKOUT3 0h (R/W) = Automatically gate this clock when there is no dependency for it 1h (R/W) = Force this clock to stay enabled even if there is no request Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	PLL_CORE_HSDIVIDER_CLKOUT3_DIVCHACK	R	0h	Toggle on this status bit after changing HSDIVIDER_CLKOUT3_DIV indicates that the change in divider value has taken effect Reset Source: mod_g_rst_n
4:0	PLL_CORE_HSDIVIDER_CLKOUT3_DIV	R/W	9h	DPLL post-divider factor, M7, for internal clock generation. Divide values from 1 to 31. 0h (R/W) = Reserved Reset Source: mod_g_rst_n

2.5.33 CFG0_PLL_CORE_RSTCTRL Registers

2.5.33.1 CFG0_CORE_RSTCTRL Register (Offset = 43Ch) [reset = 0h]

Short Description:

Long Description:

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Table 2-1499. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 043Ch

Figure 2-746. PLL_CORE_RSTCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													PLL_CORE_RSTCTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1500. PLL_CORE_RSTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	PLL_CORE_RSTCTRL_ASSERT	R/W	0h	SW Reset override for the PLL Write 3b111 : Override is enabled and Reset is asserted Reset Source: mod_g_rst_n

2.5.34 CFG0_PLL_CORE_HSDIVIDER_RSTCTRL Registers

2.5.34.1 CFG0_CORE_HSDIVIDER_RSTCTRL Register (Offset = 440h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1501. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0440h

Figure 2-747. PLL_CORE_HSDIVIDER_RSTCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													PLL_CORE_HSDIVIDER_RSTCTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1502. PLL_CORE_HSDIVIDER_RSTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	PLL_CORE_HSDIVIDER_RSTCTRL_ASSERT	R/W	0h	SW Reset override for the HSDIVIDER Write 3b111 : Override is enabled and Reset is asserted Reset Source: mod_g_rst_n

2.5.35 CFG0_R5SS_CLK_SRC_SEL Registers

2.5.35.1 CFG0_CLK_SRC_SEL Register (Offset = 500h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1503. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0500h

Figure 2-748. R5SS_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_CR5_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1504. R5SS_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_CR5_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for MSS Coretex R5 and System bus Clock. Data should be loaded as multibit. For example: if Clock source 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.5.36 CFG0_R5SS_CLK_STATUS Registers

2.5.36.1 CFG0_CLK_STATUS Register (Offset = 504h) [reset = 1h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1505. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0504h

Figure 2-749. R5SS_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MSS_ROOT_CR5_CLK_STATUS_CLKINUSE							
NONE								R							
0								1h							

Access Types Legend

Table 2-1506. R5SS_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	MSS_ROOT_CR5_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for Root clock for CortexR5 and Sysclk Reset Source: mod_g_rst_n

2.5.37 CFG0_R5SS0_CLK_DIV_SEL Registers

2.5.37.1 CFG0_CLK_DIV_SEL Register (Offset = 510h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1507. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0510h

Figure 2-750. R5SS0_CLK_DIV_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_CR50_CLK_DIV_SEL_CLKSRCSEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1508. R5SS0_CLK_DIV_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_CR50_CLK_DIV_SEL_CLKSRCSEL	R/W	0h	writing 3b000 Sets R5 clock = R5SS Root clock Writing 3 b111 Sets R5 Clock = SYSCLK Reset Source: mod_g_rst_n

2.5.38 CFG0_R5SS1_CLK_DIV_SEL Registers

2.5.38.1 CFG0_CLK_DIV_SEL Register (Offset = 514h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1509. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0514h

Figure 2-751. R5SS1_CLK_DIV_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_CR51_CLK_DIV_SEL_CLKSRCSEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1510. R5SS1_CLK_DIV_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_CR51_CLK_DIV_SEL_CLKSRCSEL	R/W	0h	writing 3b000 Sets R5 clock = R5SS Root clock Writing 3 b111 Sets R5 Clock = SYSCLK Reset Source: mod_g_rst_n

2.5.39 CFG0_R5SS0_CLK_GATE Registers

2.5.39.1 CFG0_CLK_GATE Register (Offset = 518h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1511. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0518h

Figure 2-752. R5SS0_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_CR50_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1512. R5SS0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_CR50_CLK_GATE_GATED	R/W	0h	Only for debug- Functionality not guaranteed Clock gating config for MSS Coretex R5. Data should be loaded as multibit. Write 3b000 : Clock is ungated (multibit 000) Write 3 b111 : Clock is gated (multibit 111) Reset Source: mod_g_rst_n

2.5.40 CFG0_R5SS1_CLK_GATE Registers

2.5.40.1 CFG0_CLK_GATE Register (Offset = 51Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1513. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 051Ch

Figure 2-753. R5SS1_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_CR51_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1514. R5SS1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_CR51_CLK_GATE_GATED	R/W	0h	Only for debug- Functionality not guaranteed Clock gating config for MSS Coretex R5. Data should be loaded as multibit. Write 3b000 : Clock is ungated (multibit 000) Write 3 b111 : Clock is gated (multibit 111) Reset Source: mod_g_rst_n

2.5.41 CFG0_SYS_CLK_DIV_VAL Registers

2.5.41.1 CFG0_CLK_DIV_VAL Register (Offset = 520h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1515. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0520h

Figure 2-754. SYS_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				SYS_CLK_DIV_VAL_CLKDIV											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1516. SYS_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	SYS_CLK_DIV_VAL_CLKDIV	R/W	0h	Divider value for System Clock selected clock. Data should be loaded as multibit. For example: if divider value of 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.5.42 CFG0_SYS_CLK_GATE Registers

2.5.42.1 CFG0_CLK_GATE Register (Offset = 524h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1517. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0524h

Figure 2-755. SYS_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													SYS_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1518. SYS_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	SYS_CLK_GATE_GATED	R/W	0h	Only for debug- Functionality not guaranteed Clock gating config for System Clock Data should be loaded as multibit. Write 3b000 : Clock is ungated (multibit 000) Write 3 b111 : Clock is gated (multibit 111) Reset Source: mod_g_rst_n

2.5.43 CFG0_SYS_CLK_STATUS Registers

2.5.43.1 CFG0_CLK_STATUS Register (Offset = 528h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1519. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0528h

Figure 2-756. SYS_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYS_CLK_STATUS_CURRDIVIDER								RESERVED							
R								NONE							
0h								0							

Access Types Legend

Table 2-1520. SYS_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	SYS_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for Sys Clock Reset Source: mod_g_rst_n
7:0	RESERVED	NONE		Reserved

2.5.44 CFG0_PLL_PER_PWRCTRL Registers

2.5.44.1 CFG0_PER_PWRCTRL Register (Offset = 800h) [reset = 30h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1521. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0800h

Figure 2-757. PLL_PER_PWRCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
2af8															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										PLL_PER_PWRCTRL_PONIN	PLL_PER_PWRCTRL_PGOODIN	PLL_PER_PWRCTRL_RET	PLL_PER_PWRCTRL_ISORET	PLL_PER_PWRCTRL_ISOSCAN	PLL_PER_PWRCTRL_OFFMODE
NONE										R/W	R/W	R/W	R/W	R/W	R/W
2af8										1h	1h	0h	0h	0h	0h

Access Types Legend

Table 2-1522. PLL_PER_PWRCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE		Reserved
5	PLL_PER_PWRCTRL_PONIN	R/W	1h	ON/OFF control of the weak power switch digital. For functional mode it should be 1 Reset Source: mod_g_rst_n
4	PLL_PER_PWRCTRL_PGOODIN	R/W	1h	ON/OFF control of the strong power switch digital. For functional mode it should be 1 Reset Source: mod_g_rst_n
3	PLL_PER_PWRCTRL_RET	R/W	0h	Save/Restore control for Retention mode. For functional mode it should be 0 Reset Source: mod_g_rst_n
2	PLL_PER_PWRCTRL_ISORET	R/W	0h	Save/Restore control for Isolation of output pins For functional mode it should be 0 Reset Source: mod_g_rst_n
1	PLL_PER_PWRCTRL_ISOSCAN	R/W	0h	Save/Restore control for Isolation of the Scanout pins. For functional mode it should be 0 Reset Source: mod_g_rst_n
0	PLL_PER_PWRCTRL_OFFMODE	R/W	0h	Used to switch OFF the logic on VDDA. For functional mode it should be 0 Reset Source: mod_g_rst_n

2.5.45 CFG0_PLL_PER_CLKCTRL Registers

2.5.45.1 CFG0_PER_CLKCTRL Register (Offset = 804h) [reset = 895000h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1523. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0804h

Figure 2-758. PLL_PER_CLKCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PLL_PER_CLKCTRL_CYCLESLIPEN	PLL_PER_CLKCTRL_ENSSC	PLL_PER_CLKCTRL_CLKDCOLDOEN	RESERVED					PLL_PER_CLKCTRL_IDLE	PLL_PER_CLKCTRL_BYPASSACKZ	PLL_PER_CLKCTRL_STBYRET	PLL_PER_CLKCTRL_CLKOUTEN	PLL_PER_CLKCTRL_CLKOUTLDOEN	PLL_PER_CLKCTRL_ULOWCLKEN	PLL_PER_CLKCTRL_CLKDCOLDOPWDNZ	PLL_PER_CLKCTRL_M2PWDNZ
R/W	R/W	R/W	NONE					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0					1h	0h	0h	0h	1h	0h	0h	1h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	PLL_PER_CLKCTRL_STOPMODE	RESERVED	PLL_PER_CLKCTRL_SELFREQDCO			RESERVED	PLL_PER_CLKCTRL_RELAXED_LOCK	RESERVED						PLL_PER_CLKCTRL_SSCTYPE	PLL_PER_CLKCTRL_TINTZ
NONE	R/W	NONE	R/W			NONE	R/W	NONE						R/W	R/W
1	1h	0	4h			0	0h	0						0h	0h

Access Types Legend

Table 2-1524. PLL_PER_CLKCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PLL_PER_CLKCTRL_CYCLESLIPEN	R/W	0h	FailSafe enable to trigger re-calibration in case CycleSlip occurs between REFCLK and FBCLK. Reset Source: mod_g_rst_n
30	PLL_PER_CLKCTRL_ENSSC	R/W	0h	Controls Clock Spreading. SSC is not supported. Should be set to 0x0 to disable clock spreading. Reset Source: mod_g_rst_n
29	PLL_PER_CLKCTRL_CLKDCOLDOEN	R/W	0h	Synchronously enables/disables CLKDCOLDO 0x0 : synchronously disables CLKDCOLDO 0x1 : synchronously enables CLKDCOLDO Reset Source: mod_g_rst_n
28:24	RESERVED	NONE		Reserved
23	PLL_PER_CLKCTRL_IDLE	R/W	1h	Sets PLL to Idle mode 0x0 : When SYSRESET = 0 and TINITZ = 1 IDLE = 0 PLL will go to Active and Locked 0x1 : When SYSRESET = 0 and TINITZ = 1 IDLE = 1 PLL will go to Idle Bypass low powe Reset Source: mod_g_rst_n
22	PLL_PER_CLKCTRL_BYPASSACKZ	R/W	0h	BYPASSACKZ is a special purpose input to the module. In general this input is expected to be tied to static low. For the output clocks of the module that do not have an internal bypass mux viz. CLKDCOLDO and CLKOUTLDO, a bypass mux could be implemented external to the module. Reset Source: mod_g_rst_n
21	PLL_PER_CLKCTRL_STBYRET	R/W	0h	Standby retention control 0x0 : prepares ADPLLLJ for relock when out of retention by removing the gating on all internal clocks. 0x1 : prepares ADPLLLJ for retention by gating all the internal clocks. Reset Source: mod_g_rst_n

Table 2-1524. PLL_PER_CLKCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	PLL_PER_CLKCTRL_CLKOUTEN	R/W	0h	CLKOUT enable or disable 0x0 : synchronously disables CLKOUT 0x1 : synchronously enables CLKOUT Reset Source: mod_g_rst_n
19	PLL_PER_CLKCTRL_CLKOUTLDOEN	R/W	1h	Synchronously enables/disables CLKOUTLDO 0x0 : synchronously disables CLKOUTLDO 0x1 : synchronously enables CLKOUTLDO Reset Source: mod_g_rst_n
18	PLL_PER_CLKCTRL_ULOWCLKEN	R/W	0h	Select CLKOUT source in bypass 0x0: When ADPLLLJ in bypass mode, CLKOUT = CLKINP/(N2+1) 0x1: When ADPLLLJ in bypass mode, CLKOUT = CLKINPULOW. Reset Source: mod_g_rst_n
17	PLL_PER_CLKCTRL_CLKDCOLDOPWDNZ	R/W	0h	0 Asynchronous power down for CLKDCOLDO o/p. Reset Source: mod_g_rst_n
16	PLL_PER_CLKCTRL_M2PWDNZ	R/W	1h	M2 divider power down mode 0x0: Asynchronous power down for M2 divider 0x1 : M2 divider is functional Reset Source: mod_g_rst_n
15	RESERVED	NONE		Reserved
14	PLL_PER_CLKCTRL_STOPMODE	R/W	1h	When in Lossclk/Stbyret 0x0 : Limp mode 0x1 : Stopmode Reset Source: mod_g_rst_n
13	RESERVED	NONE		Reserved
12:10	PLL_PER_CLKCTRL_SELFREQDCO	R/W	4h	DCO Clock (DCOCLK = CLKINP * [M/(N+1)]) frequency range selector. 0x0: Reserved 0x2: HS2 : DCOCLK range is from 500 MHz to 1000 MHz 0x3: Reserved 0x4: HS1: DCOCLK range is from 1000 MHz to 2000 MHz 0x5: Reserved Reset Source: mod_g_rst_n
9	RESERVED	NONE		Reserved
8	PLL_PER_CLKCTRL_RELAXED_LOCK	R/W	0h	Decides when FREQLOCK asserted 0x0: FREQLOCK asserted when DC frequency error less than 1% 0x1: FREQLOCK asserted when DC frequency error less than 2% Reset Source: mod_g_rst_n
7:2	RESERVED	NONE		Reserved
1	PLL_PER_CLKCTRL_SSCTYPE	R/W	0h	SSC Type Reset Source: mod_g_rst_n
0	PLL_PER_CLKCTRL_TINTZ	R/W	0h	PLL core soft reset Reset Source: mod_g_rst_n

2.5.46 CFG0_PLL_PER_TENABLE Registers

2.5.46.1 CFG0_PER_TENABLE Register (Offset = 808h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1525. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0808h

Figure 2-759. PLL_PER_TENABLE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															PLL_PER_TENABLE_TENABLE
NONE															R/W
0															0h

Access Types Legend

Table 2-1526. PLL_PER_TENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	PLL_PER_TENABLE_TENABLE	R/W	0h	M, N. SD and SELFREQDCO latch (active rise edge) Reset Source: mod_g_rst_n

2.5.47 CFG0_PLL_PER_TENABLEDIV Registers

2.5.47.1 CFG0_PER_TENABLEDIV Register (Offset = 80Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1527. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 080Ch

Figure 2-760. PLL_PER_TENABLEDIV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															PLL_PER_TENABLEDIV_TENABLEDIV
NONE															R/W
0															0h

Access Types Legend

Table 2-1528. PLL_PER_TENABLEDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	PLL_PER_TENABLEDIV_TENABLEDIV	R/W	0h	M2 and N2 latch (active rise edge) Reset Source: mod_g_rst_n

2.5.48 CFG0_PLL_PER_M2NDIV Registers

2.5.48.1 CFG0_PER_M2NDIV Register (Offset = 810h) [reset = 13h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1529. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0810h

Figure 2-761. PLL_PER_M2NDIV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED									PLL_PER_M2NDIV_M2						
NONE									R/W						
3e9									0h						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PLL_PER_M2NDIV_N							
NONE								R/W							
0								13h							

Access Types Legend

Table 2-1530. PLL_PER_M2NDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE		Reserved
22:16	PLL_PER_M2NDIV_M2	R/W	0h	Post-divider is REGM2 Reset Source: mod_g_rst_n
15:8	RESERVED	NONE		Reserved
7:0	PLL_PER_M2NDIV_N	R/W	13h	Pre-divider is REGN+1 Reset Source: mod_g_rst_n

2.5.49 CFG0_PLL_PER_MN2DIV Registers

2.5.49.1 CFG0_PER_MN2DIV Register (Offset = 814h) [reset = 600h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1531. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0814h

Figure 2-762. PLL_PER_MN2DIV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PLL_PER_MN2DIV_N2			
NONE												R/W			
4190ab00												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PLL_PER_MN2DIV_M											
NONE				R/W											
0				600h											

Access Types Legend

Table 2-1532. PLL_PER_MN2DIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:16	PLL_PER_MN2DIV_N2	R/W	0h	Bypass divider is REGN2+1 Reset Source: mod_g_rst_n
15:12	RESERVED	NONE		Reserved
11:0	PLL_PER_MN2DIV_M	R/W	600h	Feedback Multiplier is REGM Reset Source: mod_g_rst_n

2.5.50 CFG0_PLL_PER_FRACDIV Registers

2.5.50.1 CFG0_PER_FRACDIV Register (Offset = 818h) [reset = 8000000h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1533. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0818h

Figure 2-763. PLL_PER_FRACDIV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PLL_PER_FRACDIV_REGSD								RESERVED						PLL_PER_FRACDIV_FRACTIONALM	
R/W								NONE						R/W	
8h								0						0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_PER_FRACDIV_FRACTIONALM															
R/W															
0h															

Access Types Legend

Table 2-1534. PLL_PER_FRACDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PLL_PER_FRACDIV_REGSD	R/W	8h	Sigma-Delta Divider Should be set by s/w to provide optimum jitter performance. DPLL_SD_DIV = CEILING ([DPLL_MULT/ (DPLL_DIV+1)] * CLKINP/ 250), where CLKINP is the input clock of the DPLL in MHz Reset Source: mod_g_rst_n
23:18	RESERVED	NONE		Reserved
17:0	PLL_PER_FRACDIV_FRACTIONALM	R/W	0h	Fractional part of the M divider. Reset Source: mod_g_rst_n

2.5.51 CFG0_PLL_PER_BWCTRL Registers

2.5.51.1 CFG0_PER_BWCTRL Register (Offset = 81Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1535. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 081Ch

Figure 2-764. PLL_PER_BWCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													PLL_PER_BWCTRL_BWCONTROL		PLL_PER_BWCTRL_BW_INCR_DECRZ
NONE													R/W		R/W
0													0h		0h

Access Types Legend

Table 2-1536. PLL_PER_BWCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:1	PLL_PER_BWCTRL_BWCONTROL	R/W	0h	Change Loop Bandwidth Reset Source: mod_g_rst_n
0	PLL_PER_BWCTRL_BW_INCR_DECRZ	R/W	0h	Direction of Loop Bandwidth 0x0 : decrease BW 0x1 : increase BW Reset Source: mod_g_rst_n

2.5.52 CFG0_PLL_PER_FRACCTRL Registers

2.5.52.1 CFG0_PER_FRACCTRL Register (Offset = 820h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1537. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0820h

Figure 2-765. PLL_PER_FRACCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PLL_PER_FRACCTRL_DOWNSPREAD	PLL_PER_FRACCTRL_MODFREQDIVIDEREXPONENT			PLL_PER_FRACCTRL_MODFREQDIVIDERMANTISSA							PLL_PER_FRACCTRL_DELTAMSTEPINTEGER			PLL_PER_FRACCTRL_DELTAMSTEPFRACTION	
R/W	R/W			R/W							R/W			R/W	
0h	0h			0h							0h			0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_PER_FRACCTRL_DELTAMSTEPFRACTION															
R/W															
0h															

Access Types Legend

Table 2-1538. PLL_PER_FRACCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PLL_PER_FRACCTRL_DOWNSPREAD	R/W	0h	Controls frequency spread 0x0 : enables both side frequency spread about the programmed frequency. 0x1 : enables low frequency spread only Reset Source: mod_g_rst_n
30:28	PLL_PER_FRACCTRL_MODFREQDIVIDEREXPONENT	R/W	0h	Exponent of the REFCLK divider to define the modulation frequency. Reset Source: mod_g_rst_n
27:21	PLL_PER_FRACCTRL_MODFREQDIVIDERMANTISSA	R/W	0h	Mantissa of the REFCLK divider to define the modulation frequency Reset Source: mod_g_rst_n
20:18	PLL_PER_FRACCTRL_DELTAMSTEPINTEGER	R/W	0h	Integer part of Frequency Spread control Reset Source: mod_g_rst_n
17:0	PLL_PER_FRACCTRL_DELTAMSTEPFRACTION	R/W	0h	The fraction part of Frequency Spread control Reset Source: mod_g_rst_n

2.5.53 CFG0_PLL_PER_STATUS Registers

2.5.53.1 CFG0_PER_STATUS Register (Offset = 824h) [reset = e0001141h]

Short Description:

Long Description:

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Table 2-1539. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0824h

Figure 2-766. PLL_PER_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PLL_PER_STATUS_PONOUT	PLL_PER_STATUS_PGOODOUT	PLL_PER_STATUS_LDOPWDN	PLL_PER_STATUS_RECAL_BSTATUS3	PLL_PER_STATUS_RECAL_OPPIN	RESERVED										
R	R	R	R	R	NONE										
1h	1h	1h	0h	0h	f42a5										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PLL_PER_STATUS_CLKOUTLDOENACK	PLL_PER_STATUS_CLKDCOLDOACK	PLL_PER_STATUS_PHASELOCK	PLL_PER_STATUS_FREQLOCK	PLL_PER_STATUS_BYPASSACK	PLL_PER_STATUS_STBYRETACK	PLL_PER_STATUS_LOSSREF	PLL_PER_STATUS_CLKOUTENACK	PLL_PER_STATUS_LOCK2	PLL_PER_STATUS_M2CHANGEACK	PLL_PER_STATUS_SSCACK	PLL_PER_STATUS_HIGHJITTER	PLL_PER_STATUS_BYPASS
NONE			R	R	R	R	R	R	R	R	R	R	R	R	R
f42a5			1h	0h	0h	0h	1h	0h	1h	0h	0h	0h	0h	0h	1h

Access Types Legend

Table 2-1540. PLL_PER_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PLL_PER_STATUS_PONOUT	R	1h	Status of the weak power-switch 0x0 : indicates the/OFF status of the weak power-switch in digital to SOC. 0x1 : ndicates the ON status of the weak power-switch in digital to SOC. Reset Source: mod_g_rst_n
30	PLL_PER_STATUS_PGOODOUT	R	1h	Status of the strong power-switch 0x0 : indicates the/OFF status of the strong power-switch in digital to SOC. 0x1 : ndicates the ON status of the strong power-switch in digital to SOC. Reset Source: mod_g_rst_n
29	PLL_PER_STATUS_LDOPWDN	R	1h	1 indicates ADPLLLJ internal LDO is power down. VDDLDOOUT will be un-defined in this condition Reset Source: mod_g_rst_n
28	PLL_PER_STATUS_RECAL_BSTATUS3	R	0h	Recalibration status flag. 1 ADPLLLJ requires recalibration Reset Source: mod_g_rst_n
27	PLL_PER_STATUS_RECAL_OPPIN	R	0h	Recalibration status flag. 1 ADPLLLJ requires recalibration Reset Source: mod_g_rst_n
26:13	RESERVED	NONE		Reserved
12	PLL_PER_STATUS_CLKOUTLDOENACK	R	1h	Indicates the enable/disable condition of CLKOUTLDOEN 0x0 = CLKOUTLDO gating completed 0x1 = CLKOUTLDO enabling completed Reset Source: mod_g_rst_n
11	PLL_PER_STATUS_CLKDCOLDOACK	R	0h	Indicates the enable/disable condition of CLKDCOLDOEN 0x0 = CLKDCOLDO gating completed 0x1 = CLKDCOLDO enabling completed Reset Source: mod_g_rst_n

Table 2-1540. PLL_PER_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	PLL_PER_STATUS_PHASELOCK	R	0h	Status on PHASELOCK output pin Reset Source: mod_g_rst_n
9	PLL_PER_STATUS_FREQLOCK	R	0h	Status on FREQLOCK output pin Reset Source: mod_g_rst_n
8	PLL_PER_STATUS_BYPASSACK	R	1h	Status of BYPASSACK output pin Reset Source: mod_g_rst_n
7	PLL_PER_STATUS_STBYRETACK	R	0h	Standby and retention status 0x0: indicates to SOC that all internal clocks in ADPLLLJ are active and it is starting the relock process. 0x1: indicates to SOC that all internal clocks in ADPLLLJ are gated and it is ready for retention. Reset Source: mod_g_rst_n
6	PLL_PER_STATUS_LOSSREF	R	1h	Reference input loss Reset Source: mod_g_rst_n
5	PLL_PER_STATUS_CLKOUTENACK	R	0h	Indicates the enable/disable condition of CLKOUTEN 0x0 = CLKOUT gating completed 0x1 = CLKOUT enabling completed Reset Source: mod_g_rst_n
4	PLL_PER_STATUS_LOCK2	R	0h	ADPLL internal loop lock status Reset Source: mod_g_rst_n
3	PLL_PER_STATUS_M2CHANGEACK	R	0h	Acknowledge for change to M2 divider. Toggles from 1-0 or 0-1 (depending on current value) once CLKOUT frequency change has completed. Reset Source: mod_g_rst_n
2	PLL_PER_STATUS_SSCACK	R	0h	Spread Spectrum status 0x0 : Spread-spectrum Clocking is disabled on output clocks 0x1 : Spread-spectrum Clocking is enabled on output clocks Reset Source: mod_g_rst_n
1	PLL_PER_STATUS_HIGHJITTER	R	0h	1 indicates jitter. After PHASELOCK is asserted high, the HIGHJITTER flag is asserted high if phase error between REFCLK and FBCLK greater than 24%. Reset Source: mod_g_rst_n
0	PLL_PER_STATUS_BYPASS	R	1h	Bypass status signal. 1 CLKOUT in bypass Reset Source: mod_g_rst_n

2.5.54 CFG0_PLL_PER_HSDIVIDER Registers

2.5.54.1 CFG0_PER_HSDIVIDER Register (Offset = 828h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1541. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0828h

Figure 2-767. PLL_PER_HSDIVIDER Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														PLL_PER_HSDIVIDER_LDOPWDNACK	PLL_PER_HSDIVIDER_BYPASSACKZ
NONE														R	R
0														0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													PLL_PER_HSDIVIDER_TENABLEDIV	PLL_PER_HSDIVIDER_LDOPWDN	PLL_PER_HSDIVIDER_BYPASS
NONE													R/W	R/W	R/W
0													0h	0h	0h

Access Types Legend

Table 2-1542. PLL_PER_HSDIVIDER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE		Reserved
17	PLL_PER_HSDIVIDER_LDOPWDNACK	R	0h	LDO Power Down Ack Reset Source: mod_g_rst_n
16	PLL_PER_HSDIVIDER_BYPASSACKZ	R	0h	HSDIVIDER Bypass Ack Reset Source: mod_g_rst_n
15:3	RESERVED	NONE		Reserved
2	PLL_PER_HSDIVIDER_TENABLEDIV	R/W	0h	Tenable Div Reset Source: mod_g_rst_n
1	PLL_PER_HSDIVIDER_LDOPWDN	R/W	0h	LDO Power Down Reset Source: mod_g_rst_n
0	PLL_PER_HSDIVIDER_BYPASS	R/W	0h	HSDIVIDER Bypass Reset Source: mod_g_rst_n

2.5.55 CFG0_PLL_PER_HSDIVIDER_CLKOUT0 Registers

2.5.55.1 CFG0_PER_HSDIVIDER_CLKOUT0 Register (Offset = 82Ch) [reset = bh]

Short Description:

Long Description:

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Table 2-1543. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 082Ch

Figure 2-768. PLL_PER_HSDIVIDER_CLKOUT0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
65															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PLL_PER_HSDIVIDER_CLKOUT0_PWDN	RESERVED		PLL_PER_HSDIVIDER_CLKOUT0_STATUS	PLL_PER_HSDIVIDER_CLKOUT0_GATE_CTRL	RESERVED		PLL_PER_HSDIVIDER_CLKOUT0_DIVCHACK	PLL_PER_HSDIVIDER_CLKOUT0_DIV				
NONE			R/W	NONE		R	R/W	NONE		R	R/W				
65			0h	0		0h	0h	0		0h	bh				

Access Types Legend

Table 2-1544. PLL_PER_HSDIVIDER_CLKOUT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE		Reserved
12	PLL_PER_HSDIVIDER_CLKOUT0_PWDN	R/W	0h	Power down for HSDIVIDER M4 divider and hence CLKOUT0 output 0h (R/W) = CLKOUT0 divider active 1h (R/W) = CLKOUT0 divider is powered down Reset Source: mod_g_rst_n
11:10	RESERVED	NONE		Reserved
9	PLL_PER_HSDIVIDER_CLKOUT0_STATUS	R	0h	HSDIVIDER CLKOUT0 status 0h (R) = The clock output is gated 1h (R) = The clock output is enabled Reset Source: mod_g_rst_n
8	PLL_PER_HSDIVIDER_CLKOUT0_GATE_CTRL	R/W	0h	Control gating of HSDIVIDER CLKOUT0 0h (R/W) = Automatically gate this clock when there is no dependency for it 1h (R/W) = Force this clock to stay enabled even if there is no request Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	PLL_PER_HSDIVIDER_CLKOUT0_DIVCHACK	R	0h	Toggle on this status bit after changing HSDIVIDER_CLKOUT0_DIV indicates that the change in divider value has taken effect Reset Source: mod_g_rst_n
4:0	PLL_PER_HSDIVIDER_CLKOUT0_DIV	R/W	Bh	DPLL post-divider factor, M4, for internal clock generation. Divide values from 1 to 31. 0h (R/W) = Reserved Reset Source: mod_g_rst_n

2.5.56 CFG0_PLL_PER_HSDIVIDER_CLKOUT1 Registers

2.5.56.1 CFG0_PER_HSDIVIDER_CLKOUT1 Register (Offset = 830h) [reset = 9h]

Short Description:

Long Description:

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Table 2-1545. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0830h

Figure 2-769. PLL_PER_HSDIVIDER_CLKOUT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
64															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PLL_PER_HSDIVIDER_CLKOUT1_PWDN	RESERVED		PLL_PER_HSDIVIDER_CLKOUT1_STATUS	PLL_PER_HSDIVIDER_CLKOUT1_GATE_CTRL	RESERVED		PLL_PER_HSDIVIDER_CLKOUT1_DIVCHACK	PLL_PER_HSDIVIDER_CLKOUT1_DIV				
NONE			R/W	NONE		R	R/W	NONE		R	R/W				
64			0h	0		0h	0h	0		0h	9h				

Access Types Legend

Table 2-1546. PLL_PER_HSDIVIDER_CLKOUT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE		Reserved
12	PLL_PER_HSDIVIDER_CLKOUT1_PWDN	R/W	0h	Power down for HSDIVIDER M5 divider and hence CLKOUT1 output 0h (R/W) = CLKOUT1 divider active 1h (R/W) = CLKOUT1 divider is powered down Reset Source: mod_g_rst_n
11:10	RESERVED	NONE		Reserved
9	PLL_PER_HSDIVIDER_CLKOUT1_STATUS	R	0h	HSDIVIDER CLKOUT1 status 0h (R) = The clock output is gated 1h (R) = The clock output is enabled Reset Source: mod_g_rst_n
8	PLL_PER_HSDIVIDER_CLKOUT1_GATE_CTRL	R/W	0h	Control gating of HSDIVIDER CLKOUT1 0h (R/W) = Automatically gate this clock when there is no dependency for it 1h (R/W) = Force this clock to stay enabled even if there is no request Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	PLL_PER_HSDIVIDER_CLKOUT1_DIVCHACK	R	0h	Toggle on this status bit after changing HSDIVIDER_CLKOUT1_DIV indicates that the change in divider value has taken effect Reset Source: mod_g_rst_n
4:0	PLL_PER_HSDIVIDER_CLKOUT1_DIV	R/W	9h	DPLL post-divider factor, M5, for internal clock generation. Divide values from 1 to 31. 0h (R/W) = Reserved Reset Source: mod_g_rst_n

2.5.57 CFG0_PLL_PER_HSDIVIDER_CLKOUT2 Registers

2.5.57.1 CFG0_PER_HSDIVIDER_CLKOUT2 Register (Offset = 834h) [reset = bh]

Short Description:

Long Description:

Return to Summary Table

Table 2-1547. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0834h

Figure 2-770. PLL_PER_HSDIVIDER_CLKOUT2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
65															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PLL_PER_HSDIVIDER_CLKOUT2_PWDN	RESERVED		PLL_PER_HSDIVIDER_CLKOUT2_STATUS	PLL_PER_HSDIVIDER_CLKOUT2_GATE_CTRL	RESERVED		PLL_PER_HSDIVIDER_CLKOUT2_DIVCHACK	PLL_PER_HSDIVIDER_CLKOUT2_DIV				
NONE			R/W	NONE		R	R/W	NONE		R	R/W				
65			0h	0		0h	0h	0		0h	bh				

Access Types Legend

Table 2-1548. PLL_PER_HSDIVIDER_CLKOUT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE		Reserved
12	PLL_PER_HSDIVIDER_CLKOUT2_PWDN	R/W	0h	Power down for HSDIVIDER M6 divider and hence CLKOUT2 output 0h (R/W) = CLKOUT2 divider active 1h (R/W) = CLKOUT2 divider is powered down Reset Source: mod_g_rst_n
11:10	RESERVED	NONE		Reserved
9	PLL_PER_HSDIVIDER_CLKOUT2_STATUS	R	0h	HSDIVIDER CLKOUT2 status 0h (R) = The clock output is gated 1h (R) = The clock output is enabled Reset Source: mod_g_rst_n
8	PLL_PER_HSDIVIDER_CLKOUT2_GATE_CTRL	R/W	0h	Control gating of HSDIVIDER CLKOUT2 0h (R/W) = Automatically gate this clock when there is no dependency for it 1h (R/W) = Force this clock to stay enabled even if there is no request Reset Source: mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5	PLL_PER_HSDIVIDER_CLKOUT2_DIVCHACK	R	0h	Toggle on this status bit after changing HSDIVIDER_CLKOUT2_DIV indicates that the change in divider value has taken effect Reset Source: mod_g_rst_n
4:0	PLL_PER_HSDIVIDER_CLKOUT2_DIV	R/W	Bh	DPLL post-divider factor, M6, for internal clock generation. Divide values from 1 to 31. 0h (R/W) = Reserved Reset Source: mod_g_rst_n

2.5.58 CFG0_PLL_PER_RSTCTRL Registers

2.5.58.1 CFG0_PER_RSTCTRL Register (Offset = 83Ch) [reset = 0h]

Short Description:

Long Description:

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Table 2-1549. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 083Ch

Figure 2-771. PLL_PER_RSTCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													PLL_PER_RSTCTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1550. PLL_PER_RSTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	PLL_PER_RSTCTRL_ASSERT	R/W	0h	SW Reset override for the PLL Write 3b111 : Override is enabled and Reset is asserted Reset Source: mod_g_rst_n

2.5.59 CFG0_PLL_PER_HSDIVIDER_RSTCTRL Registers

2.5.59.1 CFG0_PER_HSDIVIDER_RSTCTRL Register (Offset = 840h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1551. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0840h

Figure 2-772. PLL_PER_HSDIVIDER_RSTCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													PLL_PER_HSDIVIDER_RSTCTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1552. PLL_PER_HSDIVIDER_RSTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	PLL_PER_HSDIVIDER_RSTCTRL_ASSERT	R/W	0h	SW Reset override for the HSDIVIDER Write 3b111 : Override is enabled and Reset is asserted Reset Source: mod_g_rst_n

2.5.60 CFG0_CLKOUT0_CLK_SRC_SEL Registers

2.5.60.1 CFG0_CLK_SRC_SEL Register (Offset = C00h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1553. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0C00h

Figure 2-773. CLKOUT0_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CLKOUT0_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1554. CLKOUT0_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	CLKOUT0_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for MSS CLKOUT . Data should be loaded as multibit. For example: if Clock source 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.5.61 CFG0_CLKOUT1_CLK_SRC_SEL Registers

2.5.61.1 CFG0_CLK_SRC_SEL Register (Offset = C04h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1555. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0C04h

Figure 2-774. CLKOUT1_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CLKOUT1_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1556. CLKOUT1_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	CLKOUT1_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for MSS CLKOUT . Data should be loaded as multibit. For example: if Clock source 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.5.62 CFG0_CLKOUT0_DIV_VAL Registers

2.5.62.1 CFG0_DIV_VAL Register (Offset = C08h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1557. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0C08h

Figure 2-775. CLKOUT0_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CLKOUT0_DIV_VAL_CLKDIV											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1558. CLKOUT0_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	CLKOUT0_DIV_VAL_CLKDIV	R/W	0h	Divider value for CLKOUT selected clock. Data should be loaded as multibit. For example: if divider value of 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.5.63 CFG0_CLKOUT1_DIV_VAL Registers

2.5.63.1 CFG0_DIV_VAL Register (Offset = C0Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1559. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0C0Ch

Figure 2-776. CLKOUT1_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CLKOUT1_DIV_VAL_CLKDIV											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1560. CLKOUT1_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	CLKOUT1_DIV_VAL_CLKDIV	R/W	0h	Divider value for CLKOUT selected clock. Data should be loaded as multibit. For example: if divider value of 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.5.64 CFG0_CLKOUT0_CLK_GATE Registers

2.5.64.1 CFG0_CLK_GATE Register (Offset = C10h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1561. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0C10h

Figure 2-777. CLKOUT0_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													CLKOUT0_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1562. CLKOUT0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	CLKOUT0_CLK_GATE_GATED	R/W	0h	Only for debug- Functionality not guaranteed Clock gating config for MSS CLKOUT Data should be loaded as multibit. Write 3b000 : Clock is ungated (multibit 000) Write 3 b111 : Clock is gated (multibit 111) Reset Source: mod_g_rst_n

2.5.65 CFG0_CLKOUT1_CLK_GATE Registers

2.5.65.1 CFG0_CLK_GATE Register (Offset = C14h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1563. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0C14h

Figure 2-778. CLKOUT1_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													CLKOUT1_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1564. CLKOUT1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	CLKOUT1_CLK_GATE_GATED	R/W	0h	Only for debug- Functionality not guaranteed Clock gating config for MSS CLKOUT Data should be loaded as multibit. Write 3b000 : Clock is ungated (multibit 000) Write 3 b111 : Clock is gated (multibit 111) Reset Source: mod_g_rst_n

2.5.66 CFG0_CLKOUT0_CLK_STATUS Registers

2.5.66.1 CFG0_CLK_STATUS Register (Offset = C18h) [reset = 1h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1565. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0C18h

Figure 2-779. CLKOUT0_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLKOUT0_CLK_STATUS_CURRDIVIDER								CLKOUT0_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-1566. CLKOUT0_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	CLKOUT0_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for CLKOUT Clock Reset Source: mod_g_rst_n
7:0	CLKOUT0_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for CLKOUT Clock Reset Source: mod_g_rst_n

2.5.67 CFG0_CLKOUT1_CLK_STATUS Registers

2.5.67.1 CFG0_CLK_STATUS Register (Offset = C1Ch) [reset = 1h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1567. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0C1Ch

Figure 2-780. CLKOUT1_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLKOUT1_CLK_STATUS_CURRDIVIDER								CLKOUT1_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-1568. CLKOUT1_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	CLKOUT1_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for CLKOUT Clock Reset Source: mod_g_rst_n
7:0	CLKOUT1_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for CLKOUT Clock Reset Source: mod_g_rst_n

2.5.68 CFG0_TRCCLKOUT_CLK_SRC_SEL Registers

2.5.68.1 CFG0_CLK_SRC_SEL Register (Offset = C20h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1569. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0C20h

Figure 2-781. TRCCLKOUT_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				TRCCLKOUT_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1570. TRCCLKOUT_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	TRCCLKOUT_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for TRC Clkout Data should be loaded as multibit. For example: if Clock source 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.5.69 CFG0_TRCCLKOUT_DIV_VAL Registers

2.5.69.1 CFG0_DIV_VAL Register (Offset = C24h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1571. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0C24h

Figure 2-782. TRCCLKOUT_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				TRCCLKOUT_DIV_VAL_CLKDIV											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1572. TRCCLKOUT_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	TRCCLKOUT_DIV_VAL_CLKDIV	R/W	0h	Divider value for TRC Clkout selected clock. Data should be loaded as multibit. For example: if divider value of 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.5.70 CFG0_TRCCLKOUT_CLK_GATE Registers

2.5.70.1 CFG0_CLK_GATE Register (Offset = C28h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1573. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0C28h

Figure 2-783. TRCCLKOUT_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													TRCCLKOUT_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1574. TRCCLKOUT_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	TRCCLKOUT_CLK_GATE_GATED	R/W	0h	Clock gatring config for TRC Clkout Data should be loaded as multibit. Write 3b000 : Clock is ungated (multibit 000) Write 3 b111 : Clock is gated (multibit 111) Reset Source: mod_g_rst_n

2.5.71 CFG0_TRCCLKOUT_CLK_STATUS Registers

2.5.71.1 CFG0_CLK_STATUS Register (Offset = C2Ch) [reset = 1h]

Short Description:

Long Description:

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Table 2-1575. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0C2Ch

Figure 2-784. TRCCLKOUT_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRCCLKOUT_CLK_STATUS_CURRDIVIDER								TRCCLKOUT_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-1576. TRCCLKOUT_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	TRCCLKOUT_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for PMIC Clkout Clock Reset Source: mod_g_rst_n
7:0	TRCCLKOUT_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for PMIC Clkout Clock Reset Source: mod_g_rst_n

2.5.72 CFG0_DFT_DMLED_EXEC Registers

2.5.72.1 CFG0_DMLED_EXEC Register (Offset = D00h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1577. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0D00h

Figure 2-785. DFT_DMLED_EXEC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DFT_DMLED_EXEC_VAL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DFT_DMLED_EXEC_VAL															
R/W															
0h															

Access Types Legend

Table 2-1578. DFT_DMLED_EXEC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DFT_DMLED_EXEC_VAL	R/W	0h	SW mapping for DMLED Execution Bit 0 : HSM CM4 Execution Bit 1 : HWA CM4 Execution Bit 2 : MSS CR5undefined Execution Reset Source: mod_g_rst_n

2.5.73 CFG0_DFT_DMLED_STATUS Registers

2.5.73.1 CFG0_DMLED_STATUS Register (Offset = D04h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1579. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0D04h

Figure 2-786. DFT_DMLED_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DFT_DMLED_STATUS_VAL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DFT_DMLED_STATUS_VAL															
R/W															
0h															

Access Types Legend

Table 2-1580. DFT_DMLED_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DFT_DMLED_STATUS_VAL	R/W	0h	SW mapping for DMLED Status Bit 0 : HSM CM4 Status Bit 1 : HWA CM4 Status Bit 2 : MSS CR5undefined Status Reset Source: mod_g_rst_n

2.5.74 CFG0_HW_REG0 Registers

2.5.74.1 CFG0_REG0 Register (Offset = E00h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1581. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0E00h

Figure 2-787. HW_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_REG0_HWREG															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_REG0_HWREG															
R/W															
0h															

Access Types Legend

Table 2-1582. HW_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HW_REG0_HWREG	R/W	0h	HW Reserved regiser. Reserved for HW RnD Reset Source: mod_g_rst_n

2.5.75 CFG0_HW_REG1 Registers

2.5.75.1 CFG0_REG1 Register (Offset = E04h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1583. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0E04h

Figure 2-788. HW_REG1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_REG1_HWREG															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_REG1_HWREG															
R/W															
0h															

Access Types Legend

Table 2-1584. HW_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HW_REG1_HWREG	R/W	0h	HW Reserved regiser. Reserved for HW RnD Reset Source: mod_g_rst_n

2.5.76 CFG0_HW_REG2 Registers

2.5.76.1 CFG0_REG2 Register (Offset = E08h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1585. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0E08h

Figure 2-789. HW_REG2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_REG2_HWREG															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_REG2_HWREG															
R/W															
0h															

Access Types Legend

Table 2-1586. HW_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HW_REG2_HWREG	R/W	0h	HW Reserved regiser. Reserved for HW RnD Reset Source: mod_g_rst_n

2.5.77 CFG0_HW_REG3 Registers

2.5.77.1 CFG0_REG3 Register (Offset = E0Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1587. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0E0Ch

Figure 2-790. HW_REG3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_REG3_HWREG															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_REG3_HWREG															
R/W															
0h															

Access Types Legend

Table 2-1588. HW_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HW_REG3_HWREG	R/W	0h	HW Reserved regiser. Reserved for HW RnD Reset Source: mod_g_rst_n

2.5.78 CFG0_HW_SPARE_RW0 Registers

2.5.78.1 CFG0_SPARE_RW0 Register (Offset = FD0h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1589. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0FD0h

Figure 2-791. HW_SPARE_RW0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RW0_HW_SPARE_RW0															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RW0_HW_SPARE_RW0															
R/W															
0h															

Access Types Legend

Table 2-1590. HW_SPARE_RW0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HW_SPARE_RW0_HW_SPARE_RW0	R/W	0h	Reserved for HW RandD Reset Source: mod_g_rst_n

2.5.79 CFG0_HW_SPARE_RW1 Registers

2.5.79.1 CFG0_SPARE_RW1 Register (Offset = FD4h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1591. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0FD4h

Figure 2-792. HW_SPARE_RW1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RW1_HW_SPARE_RW1															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RW1_HW_SPARE_RW1															
R/W															
0h															

Access Types Legend

Table 2-1592. HW_SPARE_RW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HW_SPARE_RW1_HW_SPARE_RW1	R/W	0h	Reserved for HW RandD Reset Source: mod_g_rst_n

2.5.80 CFG0_HW_SPARE_RW2 Registers

2.5.80.1 CFG0_SPARE_RW2 Register (Offset = FD8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1593. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0FD8h

Figure 2-793. HW_SPARE_RW2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RW2_HW_SPARE_RW2															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RW2_HW_SPARE_RW2															
R/W															
0h															

Access Types Legend

Table 2-1594. HW_SPARE_RW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HW_SPARE_RW2_HW_SPARE_RW2	R/W	0h	Reserved for HW RandD Reset Source: mod_g_rst_n

2.5.81 CFG0_HW_SPARE_RW3 Registers

2.5.81.1 CFG0_SPARE_RW3 Register (Offset = FDCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1595. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0FDCh

Figure 2-794. HW_SPARE_RW3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RW3_HW_SPARE_RW3															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RW3_HW_SPARE_RW3															
R/W															
0h															

Access Types Legend

Table 2-1596. HW_SPARE_RW3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HW_SPARE_RW3_HW_SPARE_RW3	R/W	0h	Reserved for HW RandD Reset Source: mod_g_rst_n

2.5.82 CFG0_HW_SPARE_RO0 Registers

2.5.82.1 CFG0_SPARE_RO0 Register (Offset = FE0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1597. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0FE0h

Figure 2-795. HW_SPARE_RO0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RO0_HW_SPARE_RO0															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RO0_HW_SPARE_RO0															
R															
0h															

Access Types Legend

Table 2-1598. HW_SPARE_RO0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HW_SPARE_RO0_HW_SPARE_RO0	R	0h	Reserved for HW RandD Reset Source: mod_g_rst_n

2.5.83 CFG0_HW_SPARE_RO1 Registers

2.5.83.1 CFG0_SPARE_RO1 Register (Offset = FE4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1599. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0FE4h

Figure 2-796. HW_SPARE_RO1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RO1_HW_SPARE_RO1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RO1_HW_SPARE_RO1															
R															
0h															

Access Types Legend

Table 2-1600. HW_SPARE_RO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HW_SPARE_RO1_HW_SPARE_RO1	R	0h	Reserved for HW RandD Reset Source: mod_g_rst_n

2.5.84 CFG0_HW_SPARE_RO2 Registers

2.5.84.1 CFG0_SPARE_RO2 Register (Offset = FE8h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1601. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0FE8h

Figure 2-797. HW_SPARE_RO2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RO2_HW_SPARE_RO2															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RO2_HW_SPARE_RO2															
R															
0h															

Access Types Legend

Table 2-1602. HW_SPARE_RO2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HW_SPARE_RO2_HW_SPARE_RO2	R	0h	Reserved for HW RandD Reset Source: mod_g_rst_n

2.5.85 CFG0_HW_SPARE_RO3 Registers

2.5.85.1 CFG0_SPARE_RO3 Register (Offset = FECh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1603. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0FECh

Figure 2-798. HW_SPARE_RO3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RO3_HW_SPARE_RO3															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RO3_HW_SPARE_RO3															
R															
0h															

Access Types Legend

Table 2-1604. HW_SPARE_RO3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HW_SPARE_RO3_HW_SPARE_RO3	R	0h	Reserved for HW RandD Reset Source: mod_g_rst_n

2.5.86 CFG0_HW_SPARE_WPH Registers

2.5.86.1 CFG0_SPARE_WPH Register (Offset = FF0h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1605. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0FF0h

Figure 2-799. HW_SPARE_WPH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_WPH_HW_SPARE_WPH															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_WPH_HW_SPARE_WPH															
R/W															
0h															

Access Types Legend

Table 2-1606. HW_SPARE_WPH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HW_SPARE_WPH_HW_SPARE_WPH	R/W	0h	Reserved for HW RandD Reset Source: mod_g_rst_n

2.5.87 CFG0_HW_SPARE_REC Registers

2.5.87.1 CFG0_SPARE_REC Register (Offset = FF4h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1607. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 0FF4h

Figure 2-800. HW_SPARE_REC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_REC_HW_SPARE_REC31	HW_SPARE_REC_HW_SPARE_REC30	HW_SPARE_REC_HW_SPARE_REC29	HW_SPARE_REC_HW_SPARE_REC28	HW_SPARE_REC_HW_SPARE_REC27	HW_SPARE_REC_HW_SPARE_REC26	HW_SPARE_REC_HW_SPARE_REC25	HW_SPARE_REC_HW_SPARE_REC24	HW_SPARE_REC_HW_SPARE_REC23	HW_SPARE_REC_HW_SPARE_REC22	HW_SPARE_REC_HW_SPARE_REC21	HW_SPARE_REC_HW_SPARE_REC20	HW_SPARE_REC_HW_SPARE_REC19	HW_SPARE_REC_HW_SPARE_REC18	HW_SPARE_REC_HW_SPARE_REC17	HW_SPARE_REC_HW_SPARE_REC16
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_REC_HW_SPARE_REC15	HW_SPARE_REC_HW_SPARE_REC14	HW_SPARE_REC_HW_SPARE_REC13	HW_SPARE_REC_HW_SPARE_REC12	HW_SPARE_REC_HW_SPARE_REC11	HW_SPARE_REC_HW_SPARE_REC10	HW_SPARE_REC_HW_SPARE_REC9	HW_SPARE_REC_HW_SPARE_REC8	HW_SPARE_REC_HW_SPARE_REC7	HW_SPARE_REC_HW_SPARE_REC6	HW_SPARE_REC_HW_SPARE_REC5	HW_SPARE_REC_HW_SPARE_REC4	HW_SPARE_REC_HW_SPARE_REC3	HW_SPARE_REC_HW_SPARE_REC2	HW_SPARE_REC_HW_SPARE_REC1	HW_SPARE_REC_HW_SPARE_REC0
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-1608. HW_SPARE_REC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HW_SPARE_REC_HW_SPARE_REC31	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
30	HW_SPARE_REC_HW_SPARE_REC30	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
29	HW_SPARE_REC_HW_SPARE_REC29	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
28	HW_SPARE_REC_HW_SPARE_REC28	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
27	HW_SPARE_REC_HW_SPARE_REC27	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
26	HW_SPARE_REC_HW_SPARE_REC26	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
25	HW_SPARE_REC_HW_SPARE_REC25	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
24	HW_SPARE_REC_HW_SPARE_REC24	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
23	HW_SPARE_REC_HW_SPARE_REC23	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n

Table 2-1608. HW_SPARE_REC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	HW_SPARE_REC_HW_SPARE_REC22	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
21	HW_SPARE_REC_HW_SPARE_REC21	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
20	HW_SPARE_REC_HW_SPARE_REC20	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
19	HW_SPARE_REC_HW_SPARE_REC19	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
18	HW_SPARE_REC_HW_SPARE_REC18	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
17	HW_SPARE_REC_HW_SPARE_REC17	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
16	HW_SPARE_REC_HW_SPARE_REC16	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
15	HW_SPARE_REC_HW_SPARE_REC15	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
14	HW_SPARE_REC_HW_SPARE_REC14	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
13	HW_SPARE_REC_HW_SPARE_REC13	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
12	HW_SPARE_REC_HW_SPARE_REC12	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
11	HW_SPARE_REC_HW_SPARE_REC11	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
10	HW_SPARE_REC_HW_SPARE_REC10	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
9	HW_SPARE_REC_HW_SPARE_REC9	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
8	HW_SPARE_REC_HW_SPARE_REC8	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
7	HW_SPARE_REC_HW_SPARE_REC7	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
6	HW_SPARE_REC_HW_SPARE_REC6	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
5	HW_SPARE_REC_HW_SPARE_REC5	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
4	HW_SPARE_REC_HW_SPARE_REC4	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
3	HW_SPARE_REC_HW_SPARE_REC3	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
2	HW_SPARE_REC_HW_SPARE_REC2	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
1	HW_SPARE_REC_HW_SPARE_REC1	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
0	HW_SPARE_REC_HW_SPARE_REC0	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n

2.5.88 CFG0_LOCK0_KICK0 Registers

2.5.88.1 CFG0_KICK0 Register (Offset = 1008h) [reset = 0h]

Short Description: - KICK0 component

Long Description: - KICK0 component

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Table 2-1609. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 1008h

Figure 2-801. LOCK0_KICK0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LOCK0_KICK0															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCK0_KICK0															
R/W															
0h															

Access Types Legend

Table 2-1610. LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

2.5.89 CFG0_LOCK0_KICK1 Registers

2.5.89.1 CFG0_KICK1 Register (Offset = 100Ch) [reset = 0h]

Short Description: - KICK1 component

Long Description: - KICK1 component

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Table 2-1611. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 100Ch

Figure 2-802. LOCK0_KICK1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LOCK0_KICK1															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCK0_KICK1															
R/W															
0h															

Access Types Legend

Table 2-1612. LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

2.5.90 CFG0_INTR_RAW_STATUS Registers

2.5.90.1 CFG0_RAW_STATUS Register (Offset = 1010h) [reset = 0h]

Short Description: Interrupt Raw Status/Set Register

Long Description: Interrupt Raw Status/Set Register

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Table 2-1613. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 1010h

Figure 2-803. INTR_RAW_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												PROXY_ERR	KICK_ERR	ADDR_ERR	PROT_ERR
NONE												R/W1TS	R/W1TS	R/W1TS	R/W1TS
0												0h	0h	0h	0h

Access Types Legend

Table 2-1614. INTR_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	PROXY_ERR	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

2.5.91 CFG0_INTR_ENABLED_STATUS_CLEAR Registers

2.5.91.1 CFG0_ENABLED_STATUS_CLEAR Register (Offset = 1014h) [reset = 0h]

Short Description: Interrupt Enabled Status/Clear register

Long Description: Interrupt Enabled Status/Clear register

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Table 2-1615. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 1014h

Figure 2-804. INTR_ENABLED_STATUS_CLEAR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												ENABLED_PROXY_ERR	ENABLED_KICK_ERR	ENABLED_ADDR_ERR	ENABLED_PROT_ERR
NONE												R/W1TC	R/W1TC	R/W1TC	R/W1TC
0												0h	0h	0h	0h

Access Types Legend

Table 2-1616. INTR_ENABLED_STATUS_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	ENABLED_PROXY_ERR	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	ENABLED_KICK_ERR	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ENABLED_ADDR_ERR	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	ENABLED_PROT_ERR	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

2.5.92 CFG0_INTR_ENABLE Registers

2.5.92.1 CFG0_ENABLE Register (Offset = 1018h) [reset = 0h]

Short Description: Interrupt Enable register

Long Description: Interrupt Enable register

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Table 2-1617. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 1018h

Figure 2-805. INTR_ENABLE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												PROXY_ERR_EN	KICK_ERR_EN	ADDR_ERR_EN	PROT_ERR_EN
NONE												R/W1TS	R/W1TS	R/W1TS	R/W1TS
0												0h	0h	0h	0h

Access Types Legend

Table 2-1618. INTR_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	PROXY_ERR_EN	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

2.5.93 CFG0_INTR_ENABLE_CLEAR Registers

2.5.93.1 CFG0_ENABLE_CLEAR Register (Offset = 101Ch) [reset = 0h]

Short Description: Interrupt Enable Clear register

Long Description: Interrupt Enable Clear register

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Table 2-1619. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 101Ch

Figure 2-806. INTR_ENABLE_CLEAR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												PROXY_ERR_EN_CLR	KICK_ERR_EN_CLR	ADDR_ERR_EN_CLR	PROT_ERR_EN_CLR
NONE												R/W1TC	R/W1TC	R/W1TC	R/W1TC
0												0h	0h	0h	0h

Access Types Legend

Table 2-1620. INTR_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	PROXY_ERR_EN_CLR	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_CLR	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_CLR	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_CLR	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

2.5.94 CFG0_EOI Registers

2.5.94.1 CFG0_EOI Register (Offset = 1020h) [reset = 0h]

Short Description: EOI register

Long Description: EOI register

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Table 2-1621. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 1020h

Figure 2-807. EOI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								EOI_VECTOR							
NONE								R/W							
0								0h							

Access Types Legend

Table 2-1622. EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	EOI_VECTOR	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip. Reset Source: mod_g_rst_n

2.5.95 CFG0_FAULT_ADDRESS Registers

2.5.95.1 CFG0_ADDRESS Register (Offset = 1024h) [reset = 0h]

Short Description: Fault Address register

Long Description: Fault Address register

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Table 2-1623. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 1024h

Figure 2-808. FAULT_ADDRESS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FAULT_ADDR															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FAULT_ADDR															
R															
0h															

Access Types Legend

Table 2-1624. FAULT_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR	R	0h	Fault Address. Reset Source: mod_g_rst_n

2.5.96 CFG0_FAULT_TYPE_STATUS Registers

2.5.96.1 CFG0_TYPE_STATUS Register (Offset = 1028h) [reset = 0h]

Short Description: Fault Type Status register

Long Description: Fault Type Status register

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Table 2-1625. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 1028h

Figure 2-809. FAULT_TYPE_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									FAULT_NS	FAULT_TYPE					
NONE									R	R					
0									0h	0h					

Access Types Legend

Table 2-1626. FAULT_TYPE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE		Reserved
6	FAULT_NS	R	0h	Non-secure access. Reset Source: mod_g_rst_n
5:0	FAULT_TYPE	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype ! = 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault Reset Source: mod_g_rst_n

2.5.97 CFG0_FAULT_ATTR_STATUS Registers

2.5.97.1 CFG0_ATTR_STATUS Register (Offset = 102Ch) [reset = 0h]

Short Description: Fault Attribute Status register

Long Description: Fault Attribute Status register

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Table 2-1627. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 102Ch

Figure 2-810. FAULT_ATTR_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FAULT_XID												FAULT_ROUTEID			
R												R			
0h												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FAULT_ROUTEID								FAULT_PRIVID							
R								R							
0h								0h							

Access Types Legend

Table 2-1628. FAULT_ATTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID	R	0h	XID. Reset Source: mod_g_rst_n
19:8	FAULT_ROUTEID	R	0h	Route ID. Reset Source: mod_g_rst_n
7:0	FAULT_PRIVID	R	0h	Privilege ID. Reset Source: mod_g_rst_n

2.5.98 CFG0_FAULT_CLEAR Registers

2.5.98.1 CFG0_CLEAR Register (Offset = 1030h) [reset = 0h]

Short Description: Fault Clear register

Long Description: Fault Clear register

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Table 2-1629. Instance Table

Instance Name	Physical Address
TOP_RCM_MMR0	5320 1030h

Figure 2-811. FAULT_CLEAR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															FAULT_CLR
NONE															W
0															0h

Access Types Legend

Table 2-1630. FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	FAULT_CLR	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. Reset Source: mod_g_rst_n

2.5.99 Access Table

Table 2-1631. Access Type Codes

Access Type	Code	Description
R	R	Read
R/W	R/W	Read / Write
R/W1TC	R/W1TC	Read/Write 1 To Clear
R/W1TS	R/W1TS	Read/Write 1 To Set
W	W	Write

2.6 MSS_RCM Registers

Table 2-1632. CFG0, CFG0 Registers, Base Address=0X0000000053208000, Length=8192

Offset	Length	Register Name	mss_rcm_mmr0 Physical Address
0h	32	PID	5320 8000h
10h	32	R5SS0_RST_STATUS	5320 8010h
14h	32	R5SS0_RST_CAUSE_CLR	5320 8014h
18h	32	R5SS0_DBG_RST_EN	5320 8018h
1Ch	32	R5SS0_RST_ASSERDLY	5320 801Ch
20h	32	R5SS0_RST2ASSERTDLY	5320 8020h
24h	32	R5SS0_RST_WFICHECK	5320 8024h
30h	32	R5SS1_RST_STATUS	5320 8030h
34h	32	R5SS1_RST_CAUSE_CLR	5320 8034h
38h	32	R5SS1_DBG_RST_EN	5320 8038h
3Ch	32	R5SS1_RST_ASSERDLY	5320 803Ch
40h	32	R5SS1_RST2ASSERTDLY	5320 8040h
44h	32	R5SS1_RST_WFICHECK	5320 8044h
100h	32	MCAN0_CLK_SRC_SEL	5320 8100h
104h	32	MCAN1_CLK_SRC_SEL	5320 8104h
108h	32	MCAN2_CLK_SRC_SEL	5320 8108h
10Ch	32	MCAN3_CLK_SRC_SEL	5320 810Ch
110h	32	QSPI0_CLK_SRC_SEL	5320 8110h
114h	32	RTI0_CLK_SRC_SEL	5320 8114h
118h	32	RTI1_CLK_SRC_SEL	5320 8118h
11Ch	32	RTI2_CLK_SRC_SEL	5320 811Ch
120h	32	RTI3_CLK_SRC_SEL	5320 8120h
128h	32	WDT0_CLK_SRC_SEL	5320 8128h
12Ch	32	WDT1_CLK_SRC_SEL	5320 812Ch
130h	32	WDT2_CLK_SRC_SEL	5320 8130h
134h	32	WDT3_CLK_SRC_SEL	5320 8134h
13Ch	32	MCSPI0_CLK_SRC_SEL	5320 813Ch
140h	32	MCSPI1_CLK_SRC_SEL	5320 8140h
144h	32	MCSPI2_CLK_SRC_SEL	5320 8144h
148h	32	MCSPI3_CLK_SRC_SEL	5320 8148h
14Ch	32	MCSPI4_CLK_SRC_SEL	5320 814Ch
150h	32	MMC0_CLK_SRC_SEL	5320 8150h
154h	32	PRU-ICSS_UCLK_CLK_SRC_SEL	5320 8154h
158h	32	CPTS_CLK_SRC_SEL	5320 8158h
15Ch	32	GPMC_CLK_SRC_SEL	5320 815Ch
160h	32	CONTROLSS_PLL_CLK_SRC_SEL	5320 8160h
164h	32	I2C_CLK_SRC_SEL	5320 8164h
174h	32	LIN0_UART0_CLK_SRC_SEL	5320 8174h
178h	32	LIN1_UART1_CLK_SRC_SEL	5320 8178h
17Ch	32	LIN2_UART2_CLK_SRC_SEL	5320 817Ch
180h	32	LIN3_UART3_CLK_SRC_SEL	5320 8180h
184h	32	LIN4_UART4_CLK_SRC_SEL	5320 8184h
188h	32	LIN5_UART5_CLK_SRC_SEL	5320 8188h
200h	32	MCAN0_CLK_DIV_VAL	5320 8200h
204h	32	MCAN1_CLK_DIV_VAL	5320 8204h

Table 2-1632. CFG0, CFG0 Registers, Base Address=0X0000000053208000, Length=8192 (continued)

Offset	Length	Register Name	mss_rcm_mmr0 Physical Address
208h	32	MCAN2_CLK_DIV_VAL	5320 8208h
20Ch	32	MCAN3_CLK_DIV_VAL	5320 820Ch
210h	32	QSPI0_CLK_DIV_VAL	5320 8210h
214h	32	RTI0_CLK_DIV_VAL	5320 8214h
218h	32	RTI1_CLK_DIV_VAL	5320 8218h
21Ch	32	RTI2_CLK_DIV_VAL	5320 821Ch
220h	32	RTI3_CLK_DIV_VAL	5320 8220h
228h	32	WDT0_CLK_DIV_VAL	5320 8228h
22Ch	32	WDT1_CLK_DIV_VAL	5320 822Ch
230h	32	WDT2_CLK_DIV_VAL	5320 8230h
234h	32	WDT3_CLK_DIV_VAL	5320 8234h
23Ch	32	MCSPI0_CLK_DIV_VAL	5320 823Ch
240h	32	MCSPI1_CLK_DIV_VAL	5320 8240h
244h	32	MCSPI2_CLK_DIV_VAL	5320 8244h
248h	32	MCSPI3_CLK_DIV_VAL	5320 8248h
24Ch	32	MCSPI4_CLK_DIV_VAL	5320 824Ch
250h	32	MMC0_CLK_DIV_VAL	5320 8250h
254h	32	PRU-ICSS_UCLK_CLK_DIV_VAL	5320 8254h
258h	32	CPTS_CLK_DIV_VAL	5320 8258h
25Ch	32	GPMC_CLK_DIV_VAL	5320 825Ch
260h	32	CONTROLSS_PLL_CLK_DIV_VAL	5320 8260h
264h	32	I2C_CLK_DIV_VAL	5320 8264h
274h	32	LIN0_UART0_CLK_DIV_VAL	5320 8274h
278h	32	LIN1_UART1_CLK_DIV_VAL	5320 8278h
27Ch	32	LIN2_UART2_CLK_DIV_VAL	5320 827Ch
280h	32	LIN3_UART3_CLK_DIV_VAL	5320 8280h
284h	32	LIN4_UART4_CLK_DIV_VAL	5320 8284h
288h	32	LIN5_UART5_CLK_DIV_VAL	5320 8288h
28Ch	32	RGMII_250_CLK_DIV_VAL	5320 828Ch
290h	32	RGMII_50_CLK_DIV_VAL	5320 8290h
294h	32	RGMII_5_CLK_DIV_VAL	5320 8294h
298h	32	XTAL_MMC_32K_CLK_DIV_VAL	5320 8298h
29Ch	32	XTAL_TEMPSENSE_32K_CLK_DIV_VAL	5320 829Ch
2A0h	32	MSS_ELM_CLK_DIV_VAL	5320 82A0h
300h	32	MCAN0_CLK_GATE	5320 8300h
304h	32	MCAN1_CLK_GATE	5320 8304h
308h	32	MCAN2_CLK_GATE	5320 8308h
30Ch	32	MCAN3_CLK_GATE	5320 830Ch
310h	32	QSPI0_CLK_GATE	5320 8310h
314h	32	RTI0_CLK_GATE	5320 8314h
318h	32	RTI1_CLK_GATE	5320 8318h
31Ch	32	RTI2_CLK_GATE	5320 831Ch
320h	32	RTI3_CLK_GATE	5320 8320h
328h	32	WDT0_CLK_GATE	5320 8328h
32Ch	32	WDT1_CLK_GATE	5320 832Ch
330h	32	WDT2_CLK_GATE	5320 8330h
334h	32	WDT3_CLK_GATE	5320 8334h

Table 2-1632. CFG0, CFG0 Registers, Base Address=0X0000000053208000, Length=8192 (continued)

Offset	Length	Register Name	mss_rcm_mmr0 Physical Address
33Ch	32	MCSPI0_CLK_GATE	5320 833Ch
340h	32	MCSPI1_CLK_GATE	5320 8340h
344h	32	MCSPI2_CLK_GATE	5320 8344h
348h	32	MCSPI3_CLK_GATE	5320 8348h
34Ch	32	MCSPI4_CLK_GATE	5320 834Ch
350h	32	MMC0_CLK_GATE	5320 8350h
354h	32	PRU-ICSS_UCLK_CLK_GATE	5320 8354h
358h	32	CPTS_CLK_GATE	5320 8358h
35Ch	32	GPMC_CLK_GATE	5320 835Ch
360h	32	CONTROLSS_PLL_CLK_GATE	5320 8360h
364h	32	I2C0_CLK_GATE	5320 8364h
368h	32	I2C1_CLK_GATE	5320 8368h
36Ch	32	I2C2_CLK_GATE	5320 836Ch
370h	32	I2C3_CLK_GATE	5320 8370h
374h	32	LIN0_CLK_GATE	5320 8374h
378h	32	LIN1_CLK_GATE	5320 8378h
37Ch	32	LIN2_CLK_GATE	5320 837Ch
380h	32	LIN3_CLK_GATE	5320 8380h
384h	32	LIN4_CLK_GATE	5320 8384h
38Ch	32	UART0_CLK_GATE	5320 838Ch
390h	32	UART1_CLK_GATE	5320 8390h
394h	32	UART2_CLK_GATE	5320 8394h
398h	32	UART3_CLK_GATE	5320 8398h
39Ch	32	UART4_CLK_GATE	5320 839Ch
3A0h	32	UART5_CLK_GATE	5320 83A0h
3A4h	32	RGMII_250_CLK_GATE	5320 83A4h
3A8h	32	RGMII_50_CLK_GATE	5320 83A8h
3ACh	32	RGMII_5_CLK_GATE	5320 83ACh
3B0h	32	MMC0_32K_CLK_GATE	5320 83B0h
3B4h	32	TEMPSENSE_32K_CLK_GATE	5320 83B4h
3B8h	32	CPSW_CLK_GATE	5320 83B8h
3BCh	32	MSS_PRU-ICSS_IEP_CLK_GATE	5320 83BCh
3C0h	32	MSS_PRU-ICSS_CORE_CLK_GATE	5320 83C0h
3C4h	32	MSS_PRU-ICSS_SYS_CLK_GATE	5320 83C4h
3C8h	32	MSS_ELM_CLK_GATE	5320 83C8h
3CCh	32	R5SS0_CORE0_GATE	5320 83CCh
3D0h	32	R5SS1_CORE0_GATE	5320 83D0h
3D4h	32	R5SS0_CORE1_GATE	5320 83D4h
3D8h	32	R5SS1_CORE1_GATE	5320 83D8h
400h	32	MCAN0_CLK_STATUS	5320 8400h
404h	32	MCAN1_CLK_STATUS	5320 8404h
408h	32	MCAN2_CLK_STATUS	5320 8408h
40Ch	32	MCAN3_CLK_STATUS	5320 840Ch
410h	32	QSPI0_CLK_STATUS	5320 8410h
414h	32	RTI0_CLK_STATUS	5320 8414h
418h	32	RTI1_CLK_STATUS	5320 8418h
41Ch	32	RTI2_CLK_STATUS	5320 841Ch

Table 2-1632. CFG0, CFG0 Registers, Base Address=0X0000000053208000, Length=8192 (continued)

Offset	Length	Register Name	mss_rcm_mmr0 Physical Address
420h	32	RTI3_CLK_STATUS	5320 8420h
428h	32	WDT0_CLK_STATUS	5320 8428h
42Ch	32	WDT1_CLK_STATUS	5320 842Ch
430h	32	WDT2_CLK_STATUS	5320 8430h
434h	32	WDT3_CLK_STATUS	5320 8434h
43Ch	32	MCSPI0_CLK_STATUS	5320 843Ch
440h	32	MCSPI1_CLK_STATUS	5320 8440h
444h	32	MCSPI2_CLK_STATUS	5320 8444h
448h	32	MCSPI3_CLK_STATUS	5320 8448h
44Ch	32	MCSPI4_CLK_STATUS	5320 844Ch
450h	32	MMC0_CLK_STATUS	5320 8450h
454h	32	PRU-ICSS_UCLK_CLK_STATUS	5320 8454h
458h	32	CPTS_CLK_STATUS	5320 8458h
45Ch	32	GPMC_CLK_STATUS	5320 845Ch
460h	32	CONTROLSS_PLL_CLK_STATUS	5320 8460h
464h	32	I2C_CLK_STATUS	5320 8464h
474h	32	LIN0_UART0_CLK_STATUS	5320 8474h
478h	32	LIN1_UART1_CLK_STATUS	5320 8478h
47Ch	32	LIN2_UART2_CLK_STATUS	5320 847Ch
480h	32	LIN3_UART3_CLK_STATUS	5320 8480h
484h	32	LIN4_UART4_CLK_STATUS	5320 8484h
488h	32	LIN5_UART5_CLK_STATUS	5320 8488h
48Ch	32	RGMII_250_CLK_STATUS	5320 848Ch
490h	32	RGMII_50_CLK_STATUS	5320 8490h
494h	32	RGMII_5_CLK_STATUS	5320 8494h
49Ch	32	MMC0_32K_CLK_STATUS	5320 849Ch
4A0h	32	TEMPSENSE_32K_CLK_STATUS	5320 84A0h
4A4h	32	MSS_ELM_CLK_STATUS	5320 84A4h
500h	32	R5SS0_POR_RST_CTRL	5320 8500h
504h	32	R5SS1_POR_RST_CTRL	5320 8504h
508h	32	R5SS0_CORE0_GRST_CTRL	5320 8508h
50Ch	32	R5SS1_CORE0_GRST_CTRL	5320 850Ch
510h	32	R5SS0_CORE1_GRST_CTRL	5320 8510h
514h	32	R5SS1_CORE1_GRST_CTRL	5320 8514h
518h	32	R5SS0_CORE0_LRST_CTRL	5320 8518h
51Ch	32	R5SS1_CORE0_LRST_CTRL	5320 851Ch
520h	32	R5SS0_CORE1_LRST_CTRL	5320 8520h
524h	32	R5SS1_CORE1_LRST_CTRL	5320 8524h
528h	32	R5SS0_VIM0_RST_CTRL	5320 8528h
52Ch	32	R5SS1_VIM0_RST_CTRL	5320 852Ch
530h	32	R5SS0_VIM1_RST_CTRL	5320 8530h
534h	32	R5SS1_VIM1_RST_CTRL	5320 8534h
538h	32	MCRC0_RST_CTRL	5320 8538h
53Ch	32	RTI0_RST_CTRL	5320 853Ch
540h	32	RTI1_RST_CTRL	5320 8540h
544h	32	RTI2_RST_CTRL	5320 8544h
548h	32	RTI3_RST_CTRL	5320 8548h

Table 2-1632. CFG0, CFG0 Registers, Base Address=0X0000000053208000, Length=8192 (continued)

Offset	Length	Register Name	mss_rcm_mmr0 Physical Address
54Ch	32	WDT0_RST_CTRL	5320 854Ch
550h	32	WDT1_RST_CTRL	5320 8550h
554h	32	WDT2_RST_CTRL	5320 8554h
558h	32	WDT3_RST_CTRL	5320 8558h
55Ch	32	TOP_ESM_RST_CTRL	5320 855Ch
560h	32	DCC0_RST_CTRL	5320 8560h
564h	32	DCC1_RST_CTRL	5320 8564h
568h	32	DCC2_RST_CTRL	5320 8568h
56Ch	32	DCC3_RST_CTRL	5320 856Ch
570h	32	MCSPI0_RST_CTRL	5320 8570h
574h	32	MCSPI1_RST_CTRL	5320 8574h
578h	32	MCSPI2_RST_CTRL	5320 8578h
57Ch	32	MCSPI3_RST_CTRL	5320 857Ch
580h	32	MCSPI4_RST_CTRL	5320 8580h
584h	32	QSPI0_RST_CTRL	5320 8584h
588h	32	MCAN0_RST_CTRL	5320 8588h
58Ch	32	MCAN1_RST_CTRL	5320 858Ch
590h	32	MCAN2_RST_CTRL	5320 8590h
594h	32	MCAN3_RST_CTRL	5320 8594h
598h	32	I2C0_RST_CTRL	5320 8598h
59Ch	32	I2C1_RST_CTRL	5320 859Ch
5A0h	32	I2C2_RST_CTRL	5320 85A0h
5A4h	32	I2C3_RST_CTRL	5320 85A4h
5A8h	32	UART0_RST_CTRL	5320 85A8h
5ACh	32	UART1_RST_CTRL	5320 85ACh
5B0h	32	UART2_RST_CTRL	5320 85B0h
5B4h	32	UART3_RST_CTRL	5320 85B4h
5B8h	32	UART4_RST_CTRL	5320 85B8h
5BCh	32	UART5_RST_CTRL	5320 85BCh
5C0h	32	LIN0_RST_CTRL	5320 85C0h
5C4h	32	LIN1_RST_CTRL	5320 85C4h
5C8h	32	LIN2_RST_CTRL	5320 85C8h
5CCh	32	LIN3_RST_CTRL	5320 85CCh
5D0h	32	LIN4_RST_CTRL	5320 85D0h
5D8h	32	EDMA_RST_CTRL	5320 85D8h
5DCh	32	INFRA_RST_CTRL	5320 85DCh
5E0h	32	CPSW_RST_CTRL	5320 85E0h
5E4h	32	MSS_PRU-ICSS_RST_CTRL	5320 85E4h
5E8h	32	MMC0_RST_CTRL	5320 85E8h
5ECh	32	GPIO0_RST_CTRL	5320 85ECh
5F0h	32	GPIO1_RST_CTRL	5320 85F0h
5F4h	32	GPIO2_RST_CTRL	5320 85F4h
5F8h	32	GPIO3_RST_CTRL	5320 85F8h
5FCh	32	SPINLOCK0_RST_CTRL	5320 85FCh
600h	32	GPMC_RST_CTRL	5320 8600h
604h	32	TEMPSENSE_32K_RST_CTRL	5320 8604h
608h	32	MSS_ELM_RST_CTRL	5320 8608h

Table 2-1632. CFG0, CFG0 Registers, Base Address=0X0000000053208000, Length=8192 (continued)

Offset	Length	Register Name	mss_rcm_mmr0 Physical Address
700h	32	L2OCRAM_BANK0_PD_CTRL	5320 8700h
704h	32	L2OCRAM_BANK1_PD_CTRL	5320 8704h
708h	32	L2OCRAM_BANK2_PD_CTRL	5320 8708h
70Ch	32	L2OCRAM_BANK3_PD_CTRL	5320 870Ch
710h	32	L2OCRAM_BANK0_PD_STATUS	5320 8710h
714h	32	L2OCRAM_BANK1_PD_STATUS	5320 8714h
718h	32	L2OCRAM_BANK2_PD_STATUS	5320 8718h
71Ch	32	L2OCRAM_BANK3_PD_STATUS	5320 871Ch
720h	32	HW_REG0	5320 8720h
724h	32	HW_REG1	5320 8724h
728h	32	HW_REG2	5320 8728h
72Ch	32	HW_REG3	5320 872Ch
800h	32	HSM_RTIA_CLK_SRC_SEL	5320 8800h
804h	32	HSM_WDT_CLK_SRC_SEL	5320 8804h
808h	32	HSM_RTC_CLK_SRC_SEL	5320 8808h
80Ch	32	HSM_DMTA_CLK_SRC_SEL	5320 880Ch
810h	32	HSM_DMTB_CLK_SRC_SEL	5320 8810h
814h	32	HSM_RTI_CLK_DIV_VAL	5320 8814h
818h	32	HSM_WDT_CLK_DIV_VAL	5320 8818h
81Ch	32	HSM_RTC_CLK_DIV_VAL	5320 881Ch
820h	32	HSM_DMTA_CLK_DIV_VAL	5320 8820h
824h	32	HSM_DMTB_CLK_DIV_VAL	5320 8824h
828h	32	HSM_RTI_CLK_GATE	5320 8828h
82Ch	32	HSM_WDT_CLK_GATE	5320 882Ch
830h	32	HSM_RTC_CLK_GATE	5320 8830h
834h	32	HSM_DMTA_CLK_GATE	5320 8834h
838h	32	HSM_DMTB_CLK_GATE	5320 8838h
83Ch	32	HSM_RTI_CLK_STATUS	5320 883Ch
840h	32	HSM_WDT_CLK_STATUS	5320 8840h
844h	32	HSM_RTC_CLK_STATUS	5320 8844h
848h	32	HSM_DMTA_CLK_STATUS	5320 8848h
84Ch	32	HSM_DMTB_CLK_STATUS	5320 884Ch
FD0h	32	HW_SPARE_RW0	5320 8FD0h
FD4h	32	HW_SPARE_RW1	5320 8FD4h
FD8h	32	HW_SPARE_RW2	5320 8FD8h
FDCh	32	HW_SPARE_RW3	5320 8FDCh
FE0h	32	HW_SPARE_RO0	5320 8FE0h
FE4h	32	HW_SPARE_RO1	5320 8FE4h
FE8h	32	HW_SPARE_RO2	5320 8FE8h
FECh	32	HW_SPARE_RO3	5320 8FECh
FF0h	32	HW_SPARE_WPH	5320 8FF0h
FF4h	32	HW_SPARE_REC	5320 8FF4h
1008h	32	LOCK0_KICK0	5320 9008h
100Ch	32	LOCK0_KICK1	5320 900Ch
1010h	32	intr_raw_status	5320 9010h
1014h	32	intr_enabled_status_clear	5320 9014h
1018h	32	intr_enable	5320 9018h

Table 2-1632. CFG0, CFG0 Registers, Base Address=0X0000000053208000, Length=8192 (continued)

Offset	Length	Register Name	mss_rcm_mmr0 Physical Address
101Ch	32	intr_enable_clear	5320 901Ch
1020h	32	eoi	5320 9020h
1024h	32	fault_address	5320 9024h
1028h	32	fault_type_status	5320 9028h
102Ch	32	fault_attr_status	5320 902Ch
1030h	32	fault_clear	5320 9030h

2.6.1 CFG0_PID Registers

2.6.1.1 CFG0_PID Register (Offset = 0h) [reset = 61800215h]

Short Description: PID register

Long Description: PID register

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Table 2-1633. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8000h

Figure 2-812. PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PID_MSB16															
R															
6180h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_MISC					PID_MAJOR			PID_CUSTOM		PID_MINOR					
R					R			R		R					
0h					2h			0h		15h					

Access Types Legend

Table 2-1634. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR	R	15h	Reset Source: mod_g_rst_n

2.6.2 CFG0_R5SS0_RST_STATUS Registers

2.6.2.1 CFG0_RST_STATUS Register (Offset = 10h) [reset = 3h]

Short Description:

Long Description:

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Table 2-1635. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8010h

Figure 2-813. R5SS0_RST_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
1															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					R5SS0_RST_STATUS_CAUSE										
NONE					R										
1					3h										

Access Types Legend

Table 2-1636. R5SS0_RST_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE		Reserved
10:0	R5SS0_RST_STATUS_CAUSE	R	3h	Has the status because of which reset has happened. Bit0: POR Reset Bit1: Warm Reset (ALso set during POR Reset) Bit2: CR5SS0 STC Reset Bit3 Reset for CORE0 and MSS_CORE00_VIM using MSS_RCM::MSS_CR5SSA0_RST_CTRL Bit4: Reset for CORE1 and MSS_CORE10_VIM using MSS_RCM::MSS_CR5SSB0_RST_CTRL Bit5: Reset for CORE0 only using MSS_RCM::MSS_CORE00_RST_CTRL Bit6: Reset for CORE1 only using using MSS_RCM::MSS_CORE10_RST_CTRL Bit7: Reset for CORE0 and MSS_CORE00_VIM caused because of reset request by debugger in CORE00 Bit8: Reset for CORE10 and MSS_CORE10_VIM caused because of reset request by debugger in CORE10 Bit9: Reset for CR5SS0 by the RESET FSM using MSS_CTRL::R5SS0_CONTROL_RESET_FSM_TRIGGER Bit 10 : MSS_RCM.MSS_CR5SS_POR_RST_CTRL0 Reset Source: mod_g_rst_n

2.6.3 CFG0_R5SS0_RST_CAUSE_CLR Registers

2.6.3.1 CFG0_RST_CAUSE_CLR Register (Offset = 14h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1637. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8014h

Figure 2-814. R5SS0_RST_CAUSE_CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													R5SS0_RST_CAUSE_CLR_CLR		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1638. R5SS0_RST_CAUSE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	R5SS0_RST_CAUSE_CLR_CLR	R/W	0h	Write pulse bit field: Clear bit for rst cause register (writing 111 will clear the rst cause register) Reset Source: mod_g_rst_n

2.6.4 CFG0_R5SS0_DBG_RST_EN Registers

2.6.4.1 CFG0_DBG_RST_EN Register (Offset = 18h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1639. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8018h

Figure 2-815. R5SS0_DBG_RST_EN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED													SYSRST_BY_DBG_RST0_R5B		
NONE													R/W		
0													0h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													SYSRST_BY_DBG_RST0_R5A		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1640. R5SS0_DBG_RST_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE		Reserved
18:16	SYSRST_BY_DBG_RST0_R5B	R/W	0h	writing 111 will block debug reset request from CORE1 toggling reset for CORE1 of respective R5SS Reset Source: mod_g_rst_n
15:3	RESERVED	NONE		Reserved
2:0	SYSRST_BY_DBG_RST0_R5A	R/W	0h	writing 111 will block debug reset request from CORE0 toggling reset for CORE0 of respective R5SS Reset Source: mod_g_rst_n

2.6.5 CFG0_R5SS0_RST_ASSERDLY Registers

2.6.5.1 CFG0_RST_ASSERDLY Register (Offset = 1Ch) [reset = fh]

Short Description:

Long Description:

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Table 2-1641. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 801Ch

Figure 2-816. R5SS0_RST_ASSERDLY Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
6f															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RST_ASSERDLY0_COMMON							
NONE								R/W							
6f								fh							

Access Types Legend

Table 2-1642. R5SS0_RST_ASSERDLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	RST_ASSERDLY0_COMMON	R/W	Fh	Value decides number of cycles reset should be kept asserted for CR5SS related resets. Programming a value of 0xFF will keep the reset asserted untill a new value other than 0xFF is written to this register The actual duration is count + 2 cycles. S/W Recommended value for this is 0x0F The COUNT is applicable to both CPU cores Reset Source: mod_g_rst_n

2.6.6 CFG0_R5SS0_RST2ASSERTDLY Registers

2.6.6.1 CFG0_RST2ASSERTDLY Register (Offset = 20h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1643. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8020h

Figure 2-817. R5SS0_RST2ASSERTDLY Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RST2ASSERTDLY0_R5B								RST2ASSERTDLY0_R5A							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RST2ASSERTDLY0_R5SSB								RST2ASSERTDLY0_R5SSA							
R/W								R/W							
0h								0h							

Access Types Legend

Table 2-1644. R5SS0_RST2ASSERTDLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RST2ASSERTDLY0_R5B	R/W	0h	Value decides number of cycles to wait before asserting reset for local reset for CORE1 Reset Source: mod_g_rst_n
23:16	RST2ASSERTDLY0_R5A	R/W	0h	Value decides number of cycles to wait before asserting reset for local reset for CORE0. Reset Source: mod_g_rst_n
15:8	RST2ASSERTDLY0_R5SSB	R/W	0h	Value decides number of cycles to wait before asserting reset for global reset for CORE1 Reset Source: mod_g_rst_n
7:0	RST2ASSERTDLY0_R5SSA	R/W	0h	Value decides number of cycles to wait before asserting reset for global reset for CORE0. Reset Source: mod_g_rst_n

2.6.7 CFG0_R5SS0_RST_WFICHECK Registers

2.6.7.1 CFG0_RST_WFICHECK Register (Offset = 24h) [reset = 7070707h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1645. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8024h

Figure 2-818. R5SS0_RST_WFICHECK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					RST_WFICHECK0_R5B			RESERVED					RST_WFICHECK0_R5A		
NONE					R/W			NONE					R/W		
b					7h			b					7h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					RST_WFICHECK0_R5SSB			RESERVED					RST_WFICHECK0_R5SSA		
NONE					R/W			NONE					R/W		
b					7h			b					7h		

Access Types Legend

Table 2-1646. R5SS0_RST_WFICHECK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE		Reserved
26:24	RST_WFICHECK0_R5B	R/W	7h	writing 000 will disable check for WFI before local reset assertion of CORE0 Reset Source: mod_g_rst_n
23:19	RESERVED	NONE		Reserved
18:16	RST_WFICHECK0_R5A	R/W	7h	writing 000 will disable check for WFI before local reset assertion of CORE0 Reset Source: mod_g_rst_n
15:11	RESERVED	NONE		Reserved
10:8	RST_WFICHECK0_R5SSB	R/W	7h	writing 000 will disable check for WFI before global reset assertion of CORE1 Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	RST_WFICHECK0_R5SSA	R/W	7h	writing 000 will disable check for WFI before global reset assertion of CORE0 Reset Source: mod_g_rst_n

2.6.8 CFG0_R5SS1_RST_STATUS Registers

2.6.8.1 CFG0_RST_STATUS Register (Offset = 30h) [reset = 3h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1647. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8030h

Figure 2-819. R5SS1_RST_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
1															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					R5SS1_RST_STATUS_CAUSE										
NONE					R										
1					3h										

Access Types Legend

Table 2-1648. R5SS1_RST_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE		Reserved
10:0	R5SS1_RST_STATUS_CAUSE	R	3h	Has the status because of which reset has happened. Bit0: POR Reset Bit1: Warm Reset (ALso set during POR Reset) Bit2: CR5SS1 STC Reset Bit3 Reset for CORE0 and MSS_CORE00_VIM using MSS_RCM::MSS_CR5SSA0_RST_CTRL Bit4: Reset for CORE1 and MSS_CORE10_VIM using MSS_RCM::MSS_CR5SSB0_RST_CTRL Bit5: Reset for CORE0 only using MSS_RCM::MSS_CORE00_RST_CTRL Bit6: Reset for CORE1 only using using MSS_RCM::MSS_CORE10_RST_CTRL Bit7: Reset for CORE0 and MSS_CORE00_VIM caused because of reset request by debugger in CORE00 Bit8: Reset for CORE10 and MSS_CORE10_VIM caused because of reset request by debugger in CORE10 Bit9: Reset for CR5SS0 by the RESET FSM using MSS_CTRL::R5SS0_CONTROL_RESET_FSM_TRIGGER Bit 10 : MSS_RCM.MSS_CR5SS_POR_RST_CTRL0 Reset Source: mod_g_rst_n

2.6.9 CFG0_R5SS1_RST_CAUSE_CLR Registers

2.6.9.1 CFG0_RST_CAUSE_CLR Register (Offset = 34h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1649. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8034h

Figure 2-820. R5SS1_RST_CAUSE_CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													R5SS1_RST_CAUSE_CLR_CLR		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1650. R5SS1_RST_CAUSE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	R5SS1_RST_CAUSE_CLR_CLR	R/W	0h	Write pulse bit field: Clear bit for rst cause register (writing 111 will clear the rst cause register) Reset Source: mod_g_rst_n

2.6.10 CFG0_R5SS1_DBG_RST_EN Registers

2.6.10.1 CFG0_DBG_RST_EN Register (Offset = 38h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1651. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8038h

Figure 2-821. R5SS1_DBG_RST_EN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED													SYSRST_BY_DBG_RST1_R5B		
NONE													R/W		
0													0h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													SYSRST_BY_DBG_RST1_R5A		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1652. R5SS1_DBG_RST_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE		Reserved
18:16	SYSRST_BY_DBG_RST1_R5B	R/W	0h	writing 111 will block debug reset request from CORE1 toggling reset for CORE1 of respective R5SS Reset Source: mod_g_rst_n
15:3	RESERVED	NONE		Reserved
2:0	SYSRST_BY_DBG_RST1_R5A	R/W	0h	writing 111 will block debug reset request from CORE0 toggling reset for CORE0 of respective R5SS Reset Source: mod_g_rst_n

2.6.11 CFG0_R5SS1_RST_ASSERDLY Registers

2.6.11.1 CFG0_RST_ASSERDLY Register (Offset = 3Ch) [reset = fh]

Short Description:

Long Description:

Return to Summary Table

Table 2-1653. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 803Ch

Figure 2-822. R5SS1_RST_ASSERDLY Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
6f															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RST_ASSERDLY1_COMMON							
NONE								R/W							
6f								fh							

Access Types Legend

Table 2-1654. R5SS1_RST_ASSERDLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	RST_ASSERDLY1_COMMON	R/W	Fh	Value decides number of cycles reset should be kept asserted for CR5SS related resets. Programming a value of 0xFF will keep the reset asserted untill a new value other than 0xFF is written to this register The actual duration is count + 2 cycles. S/W Recommended value for this is 0x0F The COUNT is applicable to both CPU cores Reset Source: mod_g_rst_n

2.6.12 CFG0_R5SS1_RST2ASSERTDLY Registers

2.6.12.1 CFG0_RST2ASSERTDLY Register (Offset = 40h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1655. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8040h

Figure 2-823. R5SS1_RST2ASSERTDLY Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RST2ASSERTDLY1_R5B								RST2ASSERTDLY1_R5A							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RST2ASSERTDLY1_R5SSB								RST2ASSERTDLY1_R5SSA							
R/W								R/W							
0h								0h							

Access Types Legend

Table 2-1656. R5SS1_RST2ASSERTDLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RST2ASSERTDLY1_R5B	R/W	0h	Value decides number of cycles to wait before asserting reset for local reset for CORE1 Reset Source: mod_g_rst_n
23:16	RST2ASSERTDLY1_R5A	R/W	0h	Value decides number of cycles to wait before asserting reset for local reset for CORE0. Reset Source: mod_g_rst_n
15:8	RST2ASSERTDLY1_R5SSB	R/W	0h	Value decides number of cycles to wait before asserting reset for global reset for CORE1 Reset Source: mod_g_rst_n
7:0	RST2ASSERTDLY1_R5SSA	R/W	0h	Value decides number of cycles to wait before asserting reset for global reset for CORE0. Reset Source: mod_g_rst_n

2.6.13 CFG0_R5SS1_RST_WFICHECK Registers

2.6.13.1 CFG0_RST_WFICHECK Register (Offset = 44h) [reset = 7070707h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1657. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8044h

Figure 2-824. R5SS1_RST_WFICHECK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					RST_WFICHECK1_R5B			RESERVED					RST_WFICHECK1_R5A		
NONE					R/W			NONE					R/W		
b					7h			b					7h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					RST_WFICHECK1_R5SSB			RESERVED					RST_WFICHECK1_R5SSA		
NONE					R/W			NONE					R/W		
b					7h			b					7h		

Access Types Legend

Table 2-1658. R5SS1_RST_WFICHECK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE		Reserved
26:24	RST_WFICHECK1_R5B	R/W	7h	writing 000 will disable check for WFI before local reset assertion of CORE0 Reset Source: mod_g_rst_n
23:19	RESERVED	NONE		Reserved
18:16	RST_WFICHECK1_R5A	R/W	7h	writing 000 will disable check for WFI before local reset assertion of CORE0 Reset Source: mod_g_rst_n
15:11	RESERVED	NONE		Reserved
10:8	RST_WFICHECK1_R5SSB	R/W	7h	writing 000 will disable check for WFI before global reset assertion of CORE1 Reset Source: mod_g_rst_n
7:3	RESERVED	NONE		Reserved
2:0	RST_WFICHECK1_R5SSA	R/W	7h	writing 000 will disable check for WFI before global reset assertion of CORE0 Reset Source: mod_g_rst_n

2.6.14 CFG0_MCAN0_CLK_SRC_SEL Registers

2.6.14.1 CFG0_CLK_SRC_SEL Register (Offset = 100h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1659. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8100h

Figure 2-825. MCAN0_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_MCAN0_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1660. MCAN0_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_MCAN0_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for corresponding MCAN.Data should be loaded as multibit. For example: if 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.6.15 CFG0_MCAN1_CLK_SRC_SEL Registers

2.6.15.1 CFG0_CLK_SRC_SEL Register (Offset = 104h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1661. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8104h

Figure 2-826. MCAN1_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_MCAN1_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1662. MCAN1_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_MCAN1_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for corresponding MCAN.Data should be loaded as multibit. For example: if 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.6.16 CFG0_MCAN2_CLK_SRC_SEL Registers

2.6.16.1 CFG0_CLK_SRC_SEL Register (Offset = 108h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1663. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8108h

Figure 2-827. MCAN2_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_MCAN2_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1664. MCAN2_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_MCAN2_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for corresponding MCAN.Data should be loaded as multibit. For example: if 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.6.17 CFG0_MCAN3_CLK_SRC_SEL Registers

2.6.17.1 CFG0_CLK_SRC_SEL Register (Offset = 10Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1665. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 810Ch

Figure 2-828. MCAN3_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_MCAN3_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1666. MCAN3_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_MCAN3_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for corresponding MCAN.Data should be loaded as multibit. For example: if 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.6.18 CFG0_QSPI0_CLK_SRC_SEL Registers

2.6.18.1 CFG0_CLK_SRC_SEL Register (Offset = 110h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1667. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8110h

Figure 2-829. QSPI0_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_QSPI_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1668. QSPI0_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_QSPI_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for QSPI.Data should be loaded as multibit. For example: if 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.6.19 CFG0_RTI0_CLK_SRC_SEL Registers

2.6.19.1 CFG0_CLK_SRC_SEL Register (Offset = 114h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1669. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8114h

Figure 2-830. RTI0_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_RTI0_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1670. RTI0_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_RTI0_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for Corresponding RTI.Data should be loaded as multibit. For example: if 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.6.20 CFG0_RTI1_CLK_SRC_SEL Registers

2.6.20.1 CFG0_CLK_SRC_SEL Register (Offset = 118h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1671. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8118h

Figure 2-831. RTI1_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_RTI1_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1672. RTI1_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_RTI1_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for Corresponding RTI.Data should be loaded as multibit. For example: if 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.6.21 CFG0_RTI2_CLK_SRC_SEL Registers

2.6.21.1 CFG0_CLK_SRC_SEL Register (Offset = 11Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1673. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 811Ch

Figure 2-832. RTI2_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_RTI2_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1674. RTI2_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_RTI2_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for Corresponding RTI.Data should be loaded as multibit. For example: if 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.6.22 CFG0_RTI3_CLK_SRC_SEL Registers

2.6.22.1 CFG0_CLK_SRC_SEL Register (Offset = 120h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1675. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8120h

Figure 2-833. RTI3_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_RTI3_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1676. RTI3_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_RTI3_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for Corresponding RTI.Data should be loaded as multibit. For example: if 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.6.23 CFG0_WDT0_CLK_SRC_SEL Registers

2.6.23.1 CFG0_CLK_SRC_SEL Register (Offset = 128h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1677. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8128h

Figure 2-834. WDT0_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_WDT0_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1678. WDT0_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_WDT0_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for WDT.Data should be loaded as multibit. For example: if 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.6.24 CFG0_WDT1_CLK_SRC_SEL Registers

2.6.24.1 CFG0_CLK_SRC_SEL Register (Offset = 12Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1679. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 812Ch

Figure 2-835. WDT1_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_WDT1_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1680. WDT1_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_WDT1_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for WDT.Data should be loaded as multibit. For example: if 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.6.25 CFG0_WDT2_CLK_SRC_SEL Registers

2.6.25.1 CFG0_CLK_SRC_SEL Register (Offset = 130h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1681. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8130h

Figure 2-836. WDT2_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_WDT2_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1682. WDT2_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_WDT2_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for WDT.Data should be loaded as multibit. For example: if 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.6.26 CFG0_WDT3_CLK_SRC_SEL Registers

2.6.26.1 CFG0_CLK_SRC_SEL Register (Offset = 134h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1683. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8134h

Figure 2-837. WDT3_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_WDT3_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1684. WDT3_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_WDT3_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for WDT.Data should be loaded as multibit. For example: if 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.6.27 CFG0_MCSPI0_CLK_SRC_SEL Registers

2.6.27.1 CFG0_CLK_SRC_SEL Register (Offset = 13Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1685. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 813Ch

Figure 2-838. MCSPI0_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_SPI0_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1686. MCSPI0_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_SPI0_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for Corresponding SPI.Data should be loaded as multibit. For example: if 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.6.28 CFG0_MCSPI1_CLK_SRC_SEL Registers

2.6.28.1 CFG0_CLK_SRC_SEL Register (Offset = 140h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1687. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8140h

Figure 2-839. MCSPI1_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_SPI1_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1688. MCSPI1_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_SPI1_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for Corresponding SPI.Data should be loaded as multibit. For example: if 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.6.29 CFG0_MCSPI2_CLK_SRC_SEL Registers

2.6.29.1 CFG0_CLK_SRC_SEL Register (Offset = 144h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1689. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8144h

Figure 2-840. MCSPI2_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_SPI2_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1690. MCSPI2_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_SPI2_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for Corresponding SPI.Data should be loaded as multibit. For example: if 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.6.30 CFG0_MCSPI3_CLK_SRC_SEL Registers

2.6.30.1 CFG0_CLK_SRC_SEL Register (Offset = 148h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1691. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8148h

Figure 2-841. MCSPI3_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_SPI3_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1692. MCSPI3_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_SPI3_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for Corresponding SPI.Data should be loaded as multibit. For example: if 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.6.31 CFG0_MCSPI4_CLK_SRC_SEL Registers

2.6.31.1 CFG0_CLK_SRC_SEL Register (Offset = 14Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1693. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 814Ch

Figure 2-842. MCSPI4_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_SPI4_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1694. MCSPI4_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_SPI4_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for Corresponding SPI.Data should be loaded as multibit. For example: if 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.6.32 CFG0_MMC0_CLK_SRC_SEL Registers

2.6.32.1 CFG0_CLK_SRC_SEL Register (Offset = 150h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1695. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8150h

Figure 2-843. MMC0_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_MMCSD_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1696. MMC0_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_MMCSD_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for MMCSD.Data should be loaded as multibit. For example: if 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.6.33 CFG0_PRU-ICSS_UCLK_CLK_SRC_SEL Registers

2.6.33.1 CFG0_UCLK_CLK_SRC_SEL Register (Offset = 154h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1697. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8154h

Figure 2-844. PRU-ICSS_UCLK_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRU-ICSS_UCLK_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1698. PRU-ICSS_UCLK_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	PRU-ICSS_UCLK_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for ICSSM_UCLK.Data should be loaded as multibit. For example: if 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.6.34 CFG0_CPTS_CLK_SRC_SEL Registers

2.6.34.1 CFG0_CLK_SRC_SEL Register (Offset = 158h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1699. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8158h

Figure 2-845. CPTS_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_CPTS_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1700. CPTS_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_CPTS_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for CPTS.Data should be loaded as multibit. For example: if 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.6.35 CFG0_GPMC_CLK_SRC_SEL Registers

2.6.35.1 CFG0_CLK_SRC_SEL Register (Offset = 15Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1701. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 815Ch

Figure 2-846. GPMC_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				GPMC_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1702. GPMC_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	GPMC_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for GPMC. Data should be loaded as multibit. For example: if 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.6.36 CFG0_CONTROLSS_PLL_CLK_SRC_SEL Registers

2.6.36.1 CFG0_PLL_CLK_SRC_SEL Register (Offset = 160h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1703. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8160h

Figure 2-847. CONTROLSS_PLL_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CONTROLSS_PLL_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1704. CONTROLSS_PLL_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	CONTROLSS_PLL_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for CONTROLSS_PLL.Data should be loaded as multibit. For example: if 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.6.37 CFG0_I2C_CLK_SRC_SEL Registers

2.6.37.1 CFG0_CLK_SRC_SEL Register (Offset = 164h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1705. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8164h

Figure 2-848. I2C_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_I2C_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1706. I2C_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_I2C_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for I2C.Data should be loaded as multibit. For example: if 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.6.38 CFG0_LIN0_UART0_CLK_SRC_SEL Registers

2.6.38.1 CFG0_UART0_CLK_SRC_SEL Register (Offset = 174h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1707. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8174h

Figure 2-849. LIN0_UART0_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_LIN0_UART0_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1708. LIN0_UART0_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_LIN0_UART0_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for corresponding UART and LIN.Data should be loaded as multibit. For example: if 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.6.39 CFG0_LIN1_UART1_CLK_SRC_SEL Registers

2.6.39.1 CFG0_UART1_CLK_SRC_SEL Register (Offset = 178h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1709. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8178h

Figure 2-850. LIN1_UART1_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_LIN1_UART1_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1710. LIN1_UART1_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_LIN1_UART1_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for corresponding UART and LIN.Data should be loaded as multibit. For example: if 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.6.40 CFG0_LIN2_UART2_CLK_SRC_SEL Registers

2.6.40.1 CFG0_UART2_CLK_SRC_SEL Register (Offset = 17Ch) [reset = 0h]

Short Description:

Long Description:

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Table 2-1711. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 817Ch

Figure 2-851. LIN2_UART2_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_LIN2_UART2_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1712. LIN2_UART2_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_LIN2_UART2_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for corresponding UART and LIN.Data should be loaded as multibit. For example: if 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.6.41 CFG0_LIN3_UART3_CLK_SRC_SEL Registers

2.6.41.1 CFG0_UART3_CLK_SRC_SEL Register (Offset = 180h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1713. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8180h

Figure 2-852. LIN3_UART3_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_LIN3_UART3_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1714. LIN3_UART3_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_LIN3_UART3_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for corresponding UART and LIN.Data should be loaded as multibit. For example: if 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.6.42 CFG0_LIN4_UART4_CLK_SRC_SEL Registers

2.6.42.1 CFG0_UART4_CLK_SRC_SEL Register (Offset = 184h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1715. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8184h

Figure 2-853. LIN4_UART4_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_LIN4_UART4_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1716. LIN4_UART4_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_LIN4_UART4_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for corresponding UART and LIN.Data should be loaded as multibit. For example: if 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.6.43 CFG0_LIN5_UART5_CLK_SRC_SEL Registers

2.6.43.1 CFG0_UART5_CLK_SRC_SEL Register (Offset = 188h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1717. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8188h

Figure 2-854. LIN5_UART5_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_LIN5_UART5_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1718. LIN5_UART5_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_LIN5_UART5_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for corresponding UART and LIN.Data should be loaded as multibit. For example: if 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.6.44 CFG0_MCAN0_CLK_DIV_VAL Registers

2.6.44.1 CFG0_CLK_DIV_VAL Register (Offset = 200h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1719. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8200h

Figure 2-855. MCAN0_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_MCAN0_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1720. MCAN0_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_MCAN0_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value corresponding MCAN selected clock.Data should be loaded as multibit. For example: if divider value of 8(1000) should be selected then 100010001000 should be configured to the register. Reset Source: mod_g_rst_n

2.6.45 CFG0_MCAN1_CLK_DIV_VAL Registers

2.6.45.1 CFG0_CLK_DIV_VAL Register (Offset = 204h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1721. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8204h

Figure 2-856. MCAN1_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_MCAN1_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1722. MCAN1_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_MCAN1_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value corresponding MCAN selected clock.Data should be loaded as multibit. For example: if divider value of 8(1000) should be selected then 100010001000 should be configured to the register. Reset Source: mod_g_rst_n

2.6.46 CFG0_MCAN2_CLK_DIV_VAL Registers

2.6.46.1 CFG0_CLK_DIV_VAL Register (Offset = 208h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1723. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8208h

Figure 2-857. MCAN2_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_MCAN2_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1724. MCAN2_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_MCAN2_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value corresponding MCAN selected clock.Data should be loaded as multibit. For example: if divider value of 8(1000) should be selected then 100010001000 should be configured to the register. Reset Source: mod_g_rst_n

2.6.47 CFG0_MCAN3_CLK_DIV_VAL Registers

2.6.47.1 CFG0_CLK_DIV_VAL Register (Offset = 20Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1725. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 820Ch

Figure 2-858. MCAN3_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_MCAN3_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1726. MCAN3_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_MCAN3_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value corresponding MCAN selected clock.Data should be loaded as multibit. For example: if divider value of 8(1000) should be selected then 100010001000 should be configured to the register. Reset Source: mod_g_rst_n

2.6.48 CFG0_QSPI0_CLK_DIV_VAL Registers

2.6.48.1 CFG0_CLK_DIV_VAL Register (Offset = 210h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1727. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8210h

Figure 2-859. QSPI0_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_QSPI_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1728. QSPI0_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_QSPI_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value QSPI selected clock.Data should be loaded as multibit. For example: if divider value of 0x8 should be selected then 0x888 should be configured to the register. Reset Source: mod_g_rst_n

2.6.49 CFG0_RTI0_CLK_DIV_VAL Registers

2.6.49.1 CFG0_CLK_DIV_VAL Register (Offset = 214h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1729. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8214h

Figure 2-860. RTI0_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_RTI0_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1730. RTI0_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_RTI0_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value Corresponding RTI selected clock.Data should be loaded as multibit. For example: if divider value of 0x8 should be selected then 0x888 should be configured to the register. Reset Source: mod_g_rst_n

2.6.50 CFG0_RTI1_CLK_DIV_VAL Registers

2.6.50.1 CFG0_CLK_DIV_VAL Register (Offset = 218h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1731. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8218h

Figure 2-861. RTI1_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_RTI1_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1732. RTI1_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_RTI1_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value Corresponding RTI selected clock.Data should be loaded as multibit. For example: if divider value of 0x8 should be selected then 0x888 should be configured to the register. Reset Source: mod_g_rst_n

2.6.51 CFG0_RTI2_CLK_DIV_VAL Registers

2.6.51.1 CFG0_CLK_DIV_VAL Register (Offset = 21Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1733. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 821Ch

Figure 2-862. RTI2_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_RTI2_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1734. RTI2_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_RTI2_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value Corresponding RTI selected clock.Data should be loaded as multibit. For example: if divider value of 0x8 should be selected then 0x888 should be configured to the register. Reset Source: mod_g_rst_n

2.6.52 CFG0_RTI3_CLK_DIV_VAL Registers

2.6.52.1 CFG0_CLK_DIV_VAL Register (Offset = 220h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1735. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8220h

Figure 2-863. RTI3_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_RTI3_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1736. RTI3_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_RTI3_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value Corresponding RTI selected clock.Data should be loaded as multibit. For example: if divider value of 0x8 should be selected then 0x888 should be configured to the register. Reset Source: mod_g_rst_n

2.6.53 CFG0_WDT0_CLK_DIV_VAL Registers

2.6.53.1 CFG0_CLK_DIV_VAL Register (Offset = 228h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1737. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8228h

Figure 2-864. WDT0_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_WDT0_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1738. WDT0_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_WDT0_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value WDT selected clock.Data should be loaded as multibit. For example: if divider value of 0x8 should be selected then 0x888 should be configured to the register. Reset Source: mod_g_rst_n

2.6.54 CFG0_WDT1_CLK_DIV_VAL Registers

2.6.54.1 CFG0_CLK_DIV_VAL Register (Offset = 22Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1739. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 822Ch

Figure 2-865. WDT1_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_WDT1_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1740. WDT1_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_WDT1_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value WDT selected clock.Data should be loaded as multibit. For example: if divider value of 0x8 should be selected then 0x888 should be configured to the register. Reset Source: mod_g_rst_n

2.6.55 CFG0_WDT2_CLK_DIV_VAL Registers

2.6.55.1 CFG0_CLK_DIV_VAL Register (Offset = 230h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1741. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8230h

Figure 2-866. WDT2_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_WDT2_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1742. WDT2_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_WDT2_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value WDT selected clock.Data should be loaded as multibit. For example: if divider value of 0x8 should be selected then 0x888 should be configured to the register. Reset Source: mod_g_rst_n

2.6.56 CFG0_WDT3_CLK_DIV_VAL Registers

2.6.56.1 CFG0_CLK_DIV_VAL Register (Offset = 234h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1743. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8234h

Figure 2-867. WDT3_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_WDT3_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1744. WDT3_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_WDT3_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value WDT selected clock.Data should be loaded as multibit. For example: if divider value of 0x8 should be selected then 0x888 should be configured to the register. Reset Source: mod_g_rst_n

2.6.57 CFG0_MCSPI0_CLK_DIV_VAL Registers

2.6.57.1 CFG0_CLK_DIV_VAL Register (Offset = 23Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1745. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 823Ch

Figure 2-868. MCSPI0_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_SPI0_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1746. MCSPI0_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_SPI0_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value Corresponding SPI selected clock.Data should be loaded as multibit. For example: if divider value of 0x8 should be selected then 0x888 should be configured to the register. Reset Source: mod_g_rst_n

2.6.58 CFG0_MCSPI1_CLK_DIV_VAL Registers

2.6.58.1 CFG0_CLK_DIV_VAL Register (Offset = 240h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1747. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8240h

Figure 2-869. MCSPI1_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_SPI1_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1748. MCSPI1_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_SPI1_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value Corresponding SPI selected clock.Data should be loaded as multibit. For example: if divider value of 0x8 should be selected then 0x888 should be configured to the register. Reset Source: mod_g_rst_n

2.6.59 CFG0_MCSPI2_CLK_DIV_VAL Registers

2.6.59.1 CFG0_CLK_DIV_VAL Register (Offset = 244h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1749. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8244h

Figure 2-870. MCSPI2_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_SPI2_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1750. MCSPI2_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_SPI2_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value Corresponding SPI selected clock.Data should be loaded as multibit. For example: if divider value of 0x8 should be selected then 0x888 should be configured to the register. Reset Source: mod_g_rst_n

2.6.60 CFG0_MCSPI3_CLK_DIV_VAL Registers

2.6.60.1 CFG0_CLK_DIV_VAL Register (Offset = 248h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1751. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8248h

Figure 2-871. MCSPI3_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_SPI3_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1752. MCSPI3_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_SPI3_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value Corresponding SPI selected clock.Data should be loaded as multibit. For example: if divider value of 0x8 should be selected then 0x888 should be configured to the register. Reset Source: mod_g_rst_n

2.6.61 CFG0_MCSPI4_CLK_DIV_VAL Registers

2.6.61.1 CFG0_CLK_DIV_VAL Register (Offset = 24Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1753. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 824Ch

Figure 2-872. MCSPI4_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_SPI4_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1754. MCSPI4_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_SPI4_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value Corresponding SPI selected clock.Data should be loaded as multibit. For example: if divider value of 0x8 should be selected then 0x888 should be configured to the register. Reset Source: mod_g_rst_n

2.6.62 CFG0_MMC0_CLK_DIV_VAL Registers

2.6.62.1 CFG0_CLK_DIV_VAL Register (Offset = 250h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1755. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8250h

Figure 2-873. MMC0_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_MMCSD_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1756. MMC0_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_MMCSD_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value MMCSD selected clock.Data should be loaded as multibit. For example: if divider value of 0x8 should be selected then 0x888 should be configured to the register. Reset Source: mod_g_rst_n

2.6.63 CFG0_PRU-ICSS_UCLK_CLK_DIV_VAL Registers

2.6.63.1 CFG0_UCLK_CLK_DIV_VAL Register (Offset = 254h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1757. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8254h

Figure 2-874. PRU-ICSS_UCLK_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRU-ICSS_UCLK_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1758. PRU-ICSS_UCLK_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	PRU-ICSS_UCLK_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value ICSSM_UCLK selected clock.Data should be loaded as multibit. For example: if divider value of 0x8 should be selected then 0x888 should be configured to the register. Reset Source: mod_g_rst_n

2.6.64 CFG0_CPTS_CLK_DIV_VAL Registers

2.6.64.1 CFG0_CLK_DIV_VAL Register (Offset = 258h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1759. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8258h

Figure 2-875. CPTS_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_CPTS_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1760. CPTS_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_CPTS_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value CPTS selected clock.Data should be loaded as multibit. For example: if divider value of 0x8 should be selected then 0x888 should be configured to the register. Reset Source: mod_g_rst_n

2.6.65 CFG0_GPMC_CLK_DIV_VAL Registers

2.6.65.1 CFG0_CLK_DIV_VAL Register (Offset = 25Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1761. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 825Ch

Figure 2-876. GPMC_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				GPMC_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1762. GPMC_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	GPMC_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value GPMC selected clock.Data should be loaded as multibit. For example: if divider value of 0x8 should be selected then 0x888 should be configured to the register. Reset Source: mod_g_rst_n

2.6.66 CFG0_CONTROLSS_PLL_CLK_DIV_VAL Registers

2.6.66.1 CFG0_PLL_CLK_DIV_VAL Register (Offset = 260h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1763. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8260h

Figure 2-877. CONTROLSS_PLL_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CONTROLSS_PLL_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1764. CONTROLSS_PLL_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	CONTROLSS_PLL_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value CONTROLSS_PLL selected clock.Data should be loaded as multibit. For example: if divider value of 0x8 should be selected then 0x888 should be configured to the register. Reset Source: mod_g_rst_n

2.6.67 CFG0_I2C_CLK_DIV_VAL Registers

2.6.67.1 CFG0_CLK_DIV_VAL Register (Offset = 264h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1765. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8264h

Figure 2-878. I2C_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_I2C_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1766. I2C_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_I2C_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value I2C selected clock.Data should be loaded as multibit. For example: if divider value of 0x8 should be selected then 0x888 should be configured to the register. Reset Source: mod_g_rst_n

2.6.68 CFG0_LIN0_UART0_CLK_DIV_VAL Registers

2.6.68.1 CFG0_UART0_CLK_DIV_VAL Register (Offset = 274h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1767. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8274h

Figure 2-879. LIN0_UART0_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_LIN0_UART0_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1768. LIN0_UART0_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_LIN0_UART0_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value for corresponding UART and LIN selected clock.Data should be loaded as multibit. For example: if divider value of 0x8 should be selected then 0x888 should be configured to the register. Reset Source: mod_g_rst_n

2.6.69 CFG0_LIN1_UART1_CLK_DIV_VAL Registers

2.6.69.1 CFG0_UART1_CLK_DIV_VAL Register (Offset = 278h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1769. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8278h

Figure 2-880. LIN1_UART1_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_LIN1_UART1_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1770. LIN1_UART1_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_LIN1_UART1_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value for corresponding UART and LIN selected clock.Data should be loaded as multibit. For example: if divider value of 0x8 should be selected then 0x888 should be configured to the register. Reset Source: mod_g_rst_n

2.6.70 CFG0_LIN2_UART2_CLK_DIV_VAL Registers

2.6.70.1 CFG0_UART2_CLK_DIV_VAL Register (Offset = 27Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1771. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 827Ch

Figure 2-881. LIN2_UART2_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_LIN2_UART2_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1772. LIN2_UART2_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_LIN2_UART2_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value for corresponding UART and LIN selected clock.Data should be loaded as multibit. For example: if divider value of 0x8 should be selected then 0x888 should be configured to the register. Reset Source: mod_g_rst_n

2.6.71 CFG0_LIN3_UART3_CLK_DIV_VAL Registers

2.6.71.1 CFG0_UART3_CLK_DIV_VAL Register (Offset = 280h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1773. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8280h

Figure 2-882. LIN3_UART3_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_LIN3_UART3_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1774. LIN3_UART3_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_LIN3_UART3_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value for corresponding UART and LIN selected clock.Data should be loaded as multibit. For example: if divider value of 0x8 should be selected then 0x888 should be configured to the register. Reset Source: mod_g_rst_n

2.6.72 CFG0_LIN4_UART4_CLK_DIV_VAL Registers

2.6.72.1 CFG0_UART4_CLK_DIV_VAL Register (Offset = 284h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1775. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8284h

Figure 2-883. LIN4_UART4_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_LIN4_UART4_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1776. LIN4_UART4_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_LIN4_UART4_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value for corresponding UART and LIN selected clock.Data should be loaded as multibit. For example: if divider value of 0x8 should be selected then 0x888 should be configured to the register. Reset Source: mod_g_rst_n

2.6.73 CFG0_LIN5_UART5_CLK_DIV_VAL Registers

2.6.73.1 CFG0_UART5_CLK_DIV_VAL Register (Offset = 288h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1777. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8288h

Figure 2-884. LIN5_UART5_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_LIN5_UART5_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-1778. LIN5_UART5_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_LIN5_UART5_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value for corresponding UART and LIN selected clock.Data should be loaded as multibit. For example: if divider value of 0x8 should be selected then 0x888 should be configured to the register. Reset Source: mod_g_rst_n

2.6.74 CFG0_RGMII_250_CLK_DIV_VAL Registers

2.6.74.1 CFG0_250_CLK_DIV_VAL Register (Offset = 28Ch) [reset = 111h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1779. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 828Ch

Figure 2-885. RGMII_250_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
989a68															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_RGMII_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
989a68				111h											

Access Types Legend

Table 2-1780. RGMII_250_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_RGMII_CLK_DIV_VAL_CLKDIVR	R/W	111h	Divider value RGMII selected clock.Data should be loaded as multibit. For example: if divider value of 0x8 should be selected then 0x888 should be configured to the register. Reset Source: mod_g_rst_n

2.6.75 CFG0_RGMII_50_CLK_DIV_VAL Registers

2.6.75.1 CFG0_50_CLK_DIV_VAL Register (Offset = 290h) [reset = 999h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1781. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8290h

Figure 2-886. RGMII_50_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
254b3c10c															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_MII100_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
254b3c10c				999h											

Access Types Legend

Table 2-1782. RGMII_50_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_MII100_CLK_DIV_VAL_CLKDIVR	R/W	999h	Divider value MII100 selected clock.Data should be loaded as multibit. For example: if divider value of 0x8 should be selected then 0x888 should be configured to the register. Reset Source: mod_g_rst_n

2.6.76 CFG0_RGMII_5_CLK_DIV_VAL Registers

2.6.76.1 CFG0_5_CLK_DIV_VAL Register (Offset = 294h) [reset = 636363h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1783. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8294h

Figure 2-887. RGMII_5_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MSS_MII10_CLK_DIV_VAL_CLKDIVR							
NONE								R/W							
1adb1								636363h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_MII10_CLK_DIV_VAL_CLKDIVR															
R/W															
636363h															

Access Types Legend

Table 2-1784. RGMII_5_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	MSS_MII10_CLK_DIV_VAL_CLKDIVR	R/W	636363h	Divider value MII10 selected clock.Data should be loaded as multibit. For example: if divider value of 0x8 should be selected then 0x888 should be configured to the register. Reset Source: mod_g_rst_n

2.6.77 CFG0_XTAL_MMC_32K_CLK_DIV_VAL Registers

2.6.77.1 CFG0_MMC_32K_CLK_DIV_VAL Register (Offset = 298h) [reset = 30cc330ch]

Short Description:

Long Description:

Return to Summary Table

Table 2-1785. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8298h

Figure 2-888. XTAL_MMC_32K_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		MSS_XTAL_32K_CLK_DIV_VAL_CLKDIVR													
NONE		R/W													
0		30cc330ch													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_XTAL_32K_CLK_DIV_VAL_CLKDIVR															
R/W															
30cc330ch															

Access Types Legend

Table 2-1786. XTAL_MMC_32K_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE		Reserved
29:0	MSS_XTAL_32K_CLK_DIV_VAL_CLKDIVR	R/W	30CC330Ch	Divider value for XTAL_32K clock. Data should be loaded as multibit. For example: if divider value of 0x30C is required then 0x30CC330C should be configured to the register. Reset Source: mod_g_rst_n

2.6.78 CFG0_XTAL_TEMPSENSE_32K_CLK_DIV_VAL Registers

2.6.78.1 CFG0_TEMPSENSE_32K_CLK_DIV_VAL Register (Offset = 29Ch) [reset = 30cc330ch]

Short Description:

Long Description:

Return to Summary Table

Table 2-1787. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 829Ch

Figure 2-889. XTAL_TEMPSENSE_32K_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		XTAL_TEMPSENSE_32K_CLK_DIV_VAL_CLKDIVR													
NONE		R/W													
0		30cc330ch													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XTAL_TEMPSENSE_32K_CLK_DIV_VAL_CLKDIVR															
R/W															
30cc330ch															

Access Types Legend

Table 2-1788. XTAL_TEMPSENSE_32K_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE		Reserved
29:0	XTAL_TEMPSENSE_32K_CLK_DIV_VAL_CLKDIVR	R/W	30CC330Ch	Divider value for XTAL_32K clock. Data should be loaded as multibit. For example: if divider value of 0x30C is required then 0x30CC330C should be configured to the register. Reset Source: mod_g_rst_n

2.6.79 CFG0_MSS_ELM_CLK_DIV_VAL Registers

2.6.79.1 CFG0_ELM_CLK_DIV_VAL Register (Offset = 2A0h) [reset = 333h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1789. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 82A0h

Figure 2-890. MSS_ELM_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
68ea279															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MSS_ELM_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
68ea279				333h											

Access Types Legend

Table 2-1790. MSS_ELM_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	MSS_ELM_CLK_DIV_VAL_CLKDIVR	R/W	333h	Divider value ELM clock.Data should be loaded as multibit. For example: if divider value of 0x8 should be selected then 0x888 should be configured to the register. Reset Source: mod_g_rst_n

2.6.80 CFG0_MCAN0_CLK_GATE Registers

2.6.80.1 CFG0_CLK_GATE Register (Offset = 300h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1791. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8300h

Figure 2-891. MCAN0_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_MCAN0_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1792. MCAN0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_MCAN0_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for corresponding MCAN Reset Source: mod_g_rst_n

2.6.81 CFG0_MCAN1_CLK_GATE Registers

2.6.81.1 CFG0_CLK_GATE Register (Offset = 304h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1793. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8304h

Figure 2-892. MCAN1_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_MCAN1_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1794. MCAN1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_MCAN1_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for corresponding MCAN Reset Source: mod_g_rst_n

2.6.82 CFG0_MCAN2_CLK_GATE Registers

2.6.82.1 CFG0_CLK_GATE Register (Offset = 308h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1795. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8308h

Figure 2-893. MCAN2_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_MCAN2_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1796. MCAN2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_MCAN2_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for corresponding MCAN Reset Source: mod_g_rst_n

2.6.83 CFG0_MCAN3_CLK_GATE Registers

2.6.83.1 CFG0_CLK_GATE Register (Offset = 30Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1797. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 830Ch

Figure 2-894. MCAN3_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_MCAN3_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1798. MCAN3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_MCAN3_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for corresponding MCAN Reset Source: mod_g_rst_n

2.6.84 CFG0_QSPI0_CLK_GATE Registers

2.6.84.1 CFG0_CLK_GATE Register (Offset = 310h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1799. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8310h

Figure 2-895. QSPI0_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_QSPI_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1800. QSPI0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_QSPI_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for QSPI Reset Source: mod_g_rst_n

2.6.85 CFG0_RTI0_CLK_GATE Registers

2.6.85.1 CFG0_CLK_GATE Register (Offset = 314h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1801. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8314h

Figure 2-896. RTI0_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_RTI0_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1802. RTI0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_RTI0_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for Corresponding RTI Reset Source: mod_g_rst_n

2.6.86 CFG0_RTI1_CLK_GATE Registers

2.6.86.1 CFG0_CLK_GATE Register (Offset = 318h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1803. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8318h

Figure 2-897. RTI1_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_RTI1_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1804. RTI1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_RTI1_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for Corresponding RTI Reset Source: mod_g_rst_n

2.6.87 CFG0_RTI2_CLK_GATE Registers

2.6.87.1 CFG0_CLK_GATE Register (Offset = 31Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1805. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 831Ch

Figure 2-898. RTI2_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_RTI2_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1806. RTI2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_RTI2_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for Corresponding RTI Reset Source: mod_g_rst_n

2.6.88 CFG0_RTI3_CLK_GATE Registers

2.6.88.1 CFG0_CLK_GATE Register (Offset = 320h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1807. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8320h

Figure 2-899. RTI3_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_RTI3_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1808. RTI3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_RTI3_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for Corresponding RTI Reset Source: mod_g_rst_n

2.6.89 CFG0_WDT0_CLK_GATE Registers

2.6.89.1 CFG0_CLK_GATE Register (Offset = 328h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1809. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8328h

Figure 2-900. WDT0_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_WDT0_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1810. WDT0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_WDT0_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for WDT Reset Source: mod_g_rst_n

2.6.90 CFG0_WDT1_CLK_GATE Registers

2.6.90.1 CFG0_CLK_GATE Register (Offset = 32Ch) [reset = 0h]

Short Description:

Long Description:

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Table 2-1811. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 832Ch

Figure 2-901. WDT1_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_WDT1_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1812. WDT1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_WDT1_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for WDT Reset Source: mod_g_rst_n

2.6.91 CFG0_WDT2_CLK_GATE Registers

2.6.91.1 CFG0_CLK_GATE Register (Offset = 330h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1813. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8330h

Figure 2-902. WDT2_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_WDT2_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1814. WDT2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_WDT2_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for WDT Reset Source: mod_g_rst_n

2.6.92 CFG0_WDT3_CLK_GATE Registers

2.6.92.1 CFG0_CLK_GATE Register (Offset = 334h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1815. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8334h

Figure 2-903. WDT3_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_WDT3_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1816. WDT3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_WDT3_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for WDT Reset Source: mod_g_rst_n

2.6.93 CFG0_MCSPI0_CLK_GATE Registers

2.6.93.1 CFG0_CLK_GATE Register (Offset = 33Ch) [reset = 0h]

Short Description:

Long Description:

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Table 2-1817. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 833Ch

Figure 2-904. MCSPI0_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_SPI0_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1818. MCSPI0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_SPI0_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for Corresponding SPI Reset Source: mod_g_rst_n

2.6.94 CFG0_MCSPI1_CLK_GATE Registers

2.6.94.1 CFG0_CLK_GATE Register (Offset = 340h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1819. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8340h

Figure 2-905. MCSPI1_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_SPI1_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1820. MCSPI1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_SPI1_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for Corresponding SPI Reset Source: mod_g_rst_n

2.6.95 CFG0_MCSPI2_CLK_GATE Registers

2.6.95.1 CFG0_CLK_GATE Register (Offset = 344h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1821. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8344h

Figure 2-906. MCSPI2_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_SPI2_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1822. MCSPI2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_SPI2_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for Corresponding SPI Reset Source: mod_g_rst_n

2.6.96 CFG0_MCSPI3_CLK_GATE Registers

2.6.96.1 CFG0_CLK_GATE Register (Offset = 348h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1823. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8348h

Figure 2-907. MCSPI3_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_SPI3_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1824. MCSPI3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_SPI3_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for Corresponding SPI Reset Source: mod_g_rst_n

2.6.97 CFG0_MCSPI4_CLK_GATE Registers

2.6.97.1 CFG0_CLK_GATE Register (Offset = 34Ch) [reset = 0h]

Short Description:

Long Description:

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Table 2-1825. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 834Ch

Figure 2-908. MCSPI4_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_SPI4_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1826. MCSPI4_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_SPI4_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for Corresponding SPI Reset Source: mod_g_rst_n

2.6.98 CFG0_MMC0_CLK_GATE Registers

2.6.98.1 CFG0_CLK_GATE Register (Offset = 350h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1827. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8350h

Figure 2-909. MMC0_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_MMCSD_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1828. MMC0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_MMCSD_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for MMCSD Reset Source: mod_g_rst_n

2.6.99 CFG0_PRU-ICSS_UCLK_CLK_GATE Registers

2.6.99.1 CFG0_UCLK_CLK_GATE Register (Offset = 354h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1829. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8354h

Figure 2-910. PRU-ICSS_UCLK_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													PRU-ICSS_UCLK_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1830. PRU-ICSS_UCLK_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	PRU-ICSS_UCLK_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for ICSSM_UCLK Reset Source: mod_g_rst_n

2.6.100 CFG0_CPTS_CLK_GATE Registers

2.6.100.1 CFG0_CLK_GATE Register (Offset = 358h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1831. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8358h

Figure 2-911. CPTS_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_CPTS_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1832. CPTS_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_CPTS_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for CPTS Reset Source: mod_g_rst_n

2.6.101 CFG0_GPMC_CLK_GATE Registers

2.6.101.1 CFG0_CLK_GATE Register (Offset = 35Ch) [reset = 0h]

Short Description:

Long Description:

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Table 2-1833. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 835Ch

Figure 2-912. GPMC_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													GPMC_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1834. GPMC_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	GPMC_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for GPMC Reset Source: mod_g_rst_n

2.6.102 CFG0_CONTROLSS_PLL_CLK_GATE Registers

2.6.102.1 CFG0_PLL_CLK_GATE Register (Offset = 360h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1835. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8360h

Figure 2-913. CONTROLSS_PLL_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													CONTROLSS_PLL_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1836. CONTROLSS_PLL_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	CONTROLSS_PLL_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for CONTROLSS_PLL Reset Source: mod_g_rst_n

2.6.103 CFG0_I2C0_CLK_GATE Registers

2.6.103.1 CFG0_CLK_GATE Register (Offset = 364h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1837. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8364h

Figure 2-914. I2C0_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_I2C0_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1838. I2C0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_I2C0_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for I2C Reset Source: mod_g_rst_n

2.6.104 CFG0_I2C1_CLK_GATE Registers

2.6.104.1 CFG0_CLK_GATE Register (Offset = 368h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1839. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8368h

Figure 2-915. I2C1_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_I2C1_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1840. I2C1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_I2C1_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for I2C Reset Source: mod_g_rst_n

2.6.105 CFG0_I2C2_CLK_GATE Registers

2.6.105.1 CFG0_CLK_GATE Register (Offset = 36Ch) [reset = 0h]

Short Description:

Long Description:

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Table 2-1841. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 836Ch

Figure 2-916. I2C2_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_I2C2_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1842. I2C2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_I2C2_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for I2C Reset Source: mod_g_rst_n

2.6.106 CFG0_I2C3_CLK_GATE Registers

2.6.106.1 CFG0_CLK_GATE Register (Offset = 370h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1843. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8370h

Figure 2-917. I2C3_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_I2C3_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1844. I2C3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_I2C3_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for I2C Reset Source: mod_g_rst_n

2.6.107 CFG0_LIN0_CLK_GATE Registers

2.6.107.1 CFG0_CLK_GATE Register (Offset = 374h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1845. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8374h

Figure 2-918. LIN0_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_LIN0_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1846. LIN0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_LIN0_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for SPIB Reset Source: mod_g_rst_n

2.6.108 CFG0_LIN1_CLK_GATE Registers

2.6.108.1 CFG0_CLK_GATE Register (Offset = 378h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1847. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8378h

Figure 2-919. LIN1_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_LIN1_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1848. LIN1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_LIN1_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for SPIB Reset Source: mod_g_rst_n

2.6.109 CFG0_LIN2_CLK_GATE Registers

2.6.109.1 CFG0_CLK_GATE Register (Offset = 37Ch) [reset = 0h]

Short Description:

Long Description:

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Table 2-1849. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 837Ch

Figure 2-920. LIN2_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_LIN2_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1850. LIN2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_LIN2_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for SPIB Reset Source: mod_g_rst_n

2.6.110 CFG0_LIN3_CLK_GATE Registers

2.6.110.1 CFG0_CLK_GATE Register (Offset = 380h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1851. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8380h

Figure 2-921. LIN3_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_LIN3_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1852. LIN3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_LIN3_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for SPIB Reset Source: mod_g_rst_n

2.6.111 CFG0_LIN4_CLK_GATE Registers

2.6.111.1 CFG0_CLK_GATE Register (Offset = 384h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1853. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8384h

Figure 2-922. LIN4_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_LIN4_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1854. LIN4_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_LIN4_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for SPIB Reset Source: mod_g_rst_n

2.6.112 CFG0_UART0_CLK_GATE Registers

2.6.112.1 CFG0_CLK_GATE Register (Offset = 38Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1855. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 838Ch

Figure 2-923. UART0_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_UART0_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1856. UART0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_UART0_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for corresponding UART Reset Source: mod_g_rst_n

2.6.113 CFG0_UART1_CLK_GATE Registers

2.6.113.1 CFG0_CLK_GATE Register (Offset = 390h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1857. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8390h

Figure 2-924. UART1_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_UART1_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1858. UART1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_UART1_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for corresponding UART Reset Source: mod_g_rst_n

2.6.114 CFG0_UART2_CLK_GATE Registers

2.6.114.1 CFG0_CLK_GATE Register (Offset = 394h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1859. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8394h

Figure 2-925. UART2_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_UART2_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1860. UART2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_UART2_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for corresponding UART Reset Source: mod_g_rst_n

2.6.115 CFG0_UART3_CLK_GATE Registers

2.6.115.1 CFG0_CLK_GATE Register (Offset = 398h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1861. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8398h

Figure 2-926. UART3_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_UART3_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1862. UART3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_UART3_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for corresponding UART Reset Source: mod_g_rst_n

2.6.116 CFG0_UART4_CLK_GATE Registers

2.6.116.1 CFG0_CLK_GATE Register (Offset = 39Ch) [reset = 0h]

Short Description:

Long Description:

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Table 2-1863. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 839Ch

Figure 2-927. UART4_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_UART4_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1864. UART4_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_UART4_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for corresponding UART Reset Source: mod_g_rst_n

2.6.117 CFG0_UART5_CLK_GATE Registers

2.6.117.1 CFG0_CLK_GATE Register (Offset = 3A0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1865. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 83A0h

Figure 2-928. UART5_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_UART5_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1866. UART5_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_UART5_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for corresponding UART Reset Source: mod_g_rst_n

2.6.118 CFG0_RGMII_250_CLK_GATE Registers

2.6.118.1 CFG0_250_CLK_GATE Register (Offset = 3A4h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1867. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 83A4h

Figure 2-929. RGMII_250_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_RGMII_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1868. RGMII_250_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_RGMII_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for RGMII Reset Source: mod_g_rst_n

2.6.119 CFG0_RGMII_50_CLK_GATE Registers

2.6.119.1 CFG0_50_CLK_GATE Register (Offset = 3A8h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1869. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 83A8h

Figure 2-930. RGMII_50_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_MII100_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1870. RGMII_50_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_MII100_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for MII100 Reset Source: mod_g_rst_n

2.6.120 CFG0_RGMII_5_CLK_GATE Registers

2.6.120.1 CFG0_5_CLK_GATE Register (Offset = 3ACh) [reset = 0h]

Short Description:

Long Description:

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Table 2-1871. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 83ACh

Figure 2-931. RGMII_5_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_MII10_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1872. RGMII_5_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_MII10_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for MII10 Reset Source: mod_g_rst_n

2.6.121 CFG0_MMC0_32K_CLK_GATE Registers

2.6.121.1 CFG0_32K_CLK_GATE Register (Offset = 3B0h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1873. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 83B0h

Figure 2-932. MMC0_32K_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_MMCSD_32K_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1874. MMC0_32K_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_MMCSD_32K_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for MMCSD_32K Reset Source: mod_g_rst_n

2.6.122 CFG0_TEMPSENSE_32K_CLK_GATE Registers

2.6.122.1 CFG0_32K_CLK_GATE Register (Offset = 3B4h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1875. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 83B4h

Figure 2-933. TEMPSENSE_32K_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_TEMPSENSE_32K_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1876. TEMPSENSE_32K_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_TEMPSENSE_32K_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for TEMPSENSE_32K Reset Source: mod_g_rst_n

2.6.123 CFG0_CPSW_CLK_GATE Registers

2.6.123.1 CFG0_CLK_GATE Register (Offset = 3B8h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1877. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 83B8h

Figure 2-934. CPSW_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_CPSW_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1878. CPSW_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_CPSW_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for CPSW CPPI Reset Source: mod_g_rst_n

2.6.124 CFG0_MSS_PRU-ICSS_IEP_CLK_GATE Registers

2.6.124.1 CFG0_PRU-ICSS_IEP_CLK_GATE Register (Offset = 3BCh) [reset = 0h]

Short Description:

Long Description:

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Table 2-1879. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 83BCh

Figure 2-935. MSS_PRU-ICSS_IEP_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_PRU-ICSS_IEP_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1880. MSS_PRU-ICSS_IEP_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_PRU-ICSS_IEP_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for ICSSM_IEP Reset Source: mod_g_rst_n

2.6.125 CFG0_MSS_PRU-ICSS_CORE_CLK_GATE Registers

2.6.125.1 CFG0_PRU-ICSS_CORE_CLK_GATE Register (Offset = 3C0h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1881. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 83C0h

Figure 2-936. MSS_PRU-ICSS_CORE_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_PRU-ICSS_CORE_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1882. MSS_PRU-ICSS_CORE_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_PRU-ICSS_CORE_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for ICSSM_CORE Reset Source: mod_g_rst_n

2.6.126 CFG0_MSS_PRU-ICSS_SYS_CLK_GATE Registers

2.6.126.1 CFG0_PRU-ICSS_SYS_CLK_GATE Register (Offset = 3C4h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1883. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 83C4h

Figure 2-937. MSS_PRU-ICSS_SYS_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_PRU-ICSS_SYS_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1884. MSS_PRU-ICSS_SYS_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_PRU-ICSS_SYS_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for ICSSM_SYS Reset Source: mod_g_rst_n

2.6.127 CFG0_MSS_ELM_CLK_GATE Registers

2.6.127.1 CFG0_ELM_CLK_GATE Register (Offset = 3C8h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1885. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 83C8h

Figure 2-938. MSS_ELM_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_ELM_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1886. MSS_ELM_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_ELM_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for ELM Reset Source: mod_g_rst_n

2.6.128 CFG0_R5SS0_CORE0_GATE Registers

2.6.128.1 CFG0_CORE0_GATE Register (Offset = 3CCh) [reset = 0h]

Short Description:

Long Description:

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Table 2-1887. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 83CCh

Figure 2-939. R5SS0_CORE0_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													R5_COREA_GATE0_CLKGATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1888. R5SS0_CORE0_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	R5_COREA_GATE0_CLKGATE	R/W	0h	writing 111 will gate clock to CORE0 related peripherals inside Cortexr5ss Reset Source: mod_g_rst_n

2.6.129 CFG0_R5SS1_CORE0_GATE Registers

2.6.129.1 CFG0_CORE0_GATE Register (Offset = 3D0h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1889. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 83D0h

Figure 2-940. R5SS1_CORE0_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													R5_COREA_GATE1_CLKGATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1890. R5SS1_CORE0_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	R5_COREA_GATE1_CLKGATE	R/W	0h	writing 111 will gate clock to CORE0 related peripherals inside Cortexr5ss Reset Source: mod_g_rst_n

2.6.130 CFG0_R5SS0_CORE1_GATE Registers

2.6.130.1 CFG0_CORE1_GATE Register (Offset = 3D4h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1891. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 83D4h

Figure 2-941. R5SS0_CORE1_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													R5_COREB_GATE0_CLKGATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1892. R5SS0_CORE1_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	R5_COREB_GATE0_CLKGATE	R/W	0h	writing 111 will gate clock to CORE1 related peripherals inside Cortexr5ss Reset Source: mod_g_rst_n

2.6.131 CFG0_R5SS1_CORE1_GATE Registers

2.6.131.1 CFG0_CORE1_GATE Register (Offset = 3D8h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1893. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 83D8h

Figure 2-942. R5SS1_CORE1_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													R5_COREB_GATE1_CLKGATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1894. R5SS1_CORE1_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	R5_COREB_GATE1_CLKGATE	R/W	0h	writing 111 will gate clock to CORE1 related peripherals inside Cortexr5ss Reset Source: mod_g_rst_n

2.6.132 CFG0_MCAN0_CLK_STATUS Registers

2.6.132.1 CFG0_CLK_STATUS Register (Offset = 400h) [reset = 1h]

Short Description:

Long Description:

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Table 2-1895. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8400h

Figure 2-943. MCAN0_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_MCAN0_CLK_STATUS_CURRDIVIDER								MSS_MCAN0_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-1896. MCAN0_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_MCAN0_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for corresponding MCAN Reset Source: mod_g_rst_n
7:0	MSS_MCAN0_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for corresponding MCAN Reset Source: mod_g_rst_n

2.6.133 CFG0_MCAN1_CLK_STATUS Registers

2.6.133.1 CFG0_CLK_STATUS Register (Offset = 404h) [reset = 1h]

Short Description:

Long Description:

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Table 2-1897. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8404h

Figure 2-944. MCAN1_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_MCAN1_CLK_STATUS_CURRDIVIDER								MSS_MCAN1_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-1898. MCAN1_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_MCAN1_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for corresponding MCAN Reset Source: mod_g_rst_n
7:0	MSS_MCAN1_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for corresponding MCAN Reset Source: mod_g_rst_n

2.6.134 CFG0_MCAN2_CLK_STATUS Registers

2.6.134.1 CFG0_CLK_STATUS Register (Offset = 408h) [reset = 1h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1899. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8408h

Figure 2-945. MCAN2_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_MCAN2_CLK_STATUS_CURRDIVIDER								MSS_MCAN2_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-1900. MCAN2_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_MCAN2_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for corresponding MCAN Reset Source: mod_g_rst_n
7:0	MSS_MCAN2_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for corresponding MCAN Reset Source: mod_g_rst_n

2.6.135 CFG0_MCAN3_CLK_STATUS Registers

2.6.135.1 CFG0_CLK_STATUS Register (Offset = 40Ch) [reset = 1h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1901. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 840Ch

Figure 2-946. MCAN3_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_MCAN3_CLK_STATUS_CURRDIVIDER								MSS_MCAN3_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-1902. MCAN3_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_MCAN3_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for corresponding MCAN Reset Source: mod_g_rst_n
7:0	MSS_MCAN3_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for corresponding MCAN Reset Source: mod_g_rst_n

2.6.136 CFG0_QSPI0_CLK_STATUS Registers

2.6.136.1 CFG0_CLK_STATUS Register (Offset = 410h) [reset = 1h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1903. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8410h

Figure 2-947. QSPI0_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_QSPI_CLK_STATUS_CURRDIVIDER								MSS_QSPI_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-1904. QSPI0_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_QSPI_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for QSPI Reset Source: mod_g_rst_n
7:0	MSS_QSPI_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for QSPI Reset Source: mod_g_rst_n

2.6.137 CFG0_RTI0_CLK_STATUS Registers

2.6.137.1 CFG0_CLK_STATUS Register (Offset = 414h) [reset = 1h]

Short Description:

Long Description:

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Table 2-1905. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8414h

Figure 2-948. RTI0_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_RTI0_CLK_STATUS_CURRDIVIDER								MSS_RTI0_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-1906. RTI0_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_RTI0_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for Corresponding RTI Reset Source: mod_g_rst_n
7:0	MSS_RTI0_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for Corresponding RTI Reset Source: mod_g_rst_n

2.6.138 CFG0_RTI1_CLK_STATUS Registers

2.6.138.1 CFG0_CLK_STATUS Register (Offset = 418h) [reset = 1h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1907. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8418h

Figure 2-949. RTI1_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_RTI1_CLK_STATUS_CURRDIVIDER								MSS_RTI1_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-1908. RTI1_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_RTI1_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for Corresponding RTI Reset Source: mod_g_rst_n
7:0	MSS_RTI1_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for Corresponding RTI Reset Source: mod_g_rst_n

2.6.139 CFG0_RTI2_CLK_STATUS Registers

2.6.139.1 CFG0_CLK_STATUS Register (Offset = 41Ch) [reset = 1h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1909. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 841Ch

Figure 2-950. RTI2_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_RTI2_CLK_STATUS_CURRDIVIDER								MSS_RTI2_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-1910. RTI2_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_RTI2_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for Corresponding RTI Reset Source: mod_g_rst_n
7:0	MSS_RTI2_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for Corresponding RTI Reset Source: mod_g_rst_n

2.6.140 CFG0_RTI3_CLK_STATUS Registers

2.6.140.1 CFG0_CLK_STATUS Register (Offset = 420h) [reset = 1h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1911. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8420h

Figure 2-951. RTI3_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_RTI3_CLK_STATUS_CURRDIVIDER								MSS_RTI3_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-1912. RTI3_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_RTI3_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for Corresponding RTI Reset Source: mod_g_rst_n
7:0	MSS_RTI3_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for Corresponding RTI Reset Source: mod_g_rst_n

2.6.141 CFG0_WDT0_CLK_STATUS Registers

2.6.141.1 CFG0_CLK_STATUS Register (Offset = 428h) [reset = 1h]

Short Description:

Long Description:

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Table 2-1913. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8428h

Figure 2-952. WDT0_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_WDT0_CLK_STATUS_CURRDIVIDER								MSS_WDT0_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-1914. WDT0_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_WDT0_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for WDT Reset Source: mod_g_rst_n
7:0	MSS_WDT0_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for WDT Reset Source: mod_g_rst_n

2.6.142 CFG0_WDT1_CLK_STATUS Registers

2.6.142.1 CFG0_CLK_STATUS Register (Offset = 42Ch) [reset = 1h]

Short Description:

Long Description:

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Table 2-1915. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 842Ch

Figure 2-953. WDT1_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_WDT1_CLK_STATUS_CURRDIVIDER								MSS_WDT1_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-1916. WDT1_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_WDT1_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for WDT Reset Source: mod_g_rst_n
7:0	MSS_WDT1_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for WDT Reset Source: mod_g_rst_n

2.6.143 CFG0_WDT2_CLK_STATUS Registers

2.6.143.1 CFG0_CLK_STATUS Register (Offset = 430h) [reset = 1h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1917. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8430h

Figure 2-954. WDT2_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_WDT2_CLK_STATUS_CURRDIVIDER								MSS_WDT2_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-1918. WDT2_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_WDT2_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for WDT Reset Source: mod_g_rst_n
7:0	MSS_WDT2_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for WDT Reset Source: mod_g_rst_n

2.6.144 CFG0_WDT3_CLK_STATUS Registers

2.6.144.1 CFG0_CLK_STATUS Register (Offset = 434h) [reset = 1h]

Short Description:

Long Description:

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Table 2-1919. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8434h

Figure 2-955. WDT3_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_WDT3_CLK_STATUS_CURRDIVIDER								MSS_WDT3_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-1920. WDT3_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_WDT3_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for WDT Reset Source: mod_g_rst_n
7:0	MSS_WDT3_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for WDT Reset Source: mod_g_rst_n

2.6.145 CFG0_MCSPI0_CLK_STATUS Registers

2.6.145.1 CFG0_CLK_STATUS Register (Offset = 43Ch) [reset = 1h]

Short Description:

Long Description:

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Table 2-1921. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 843Ch

Figure 2-956. MCSPI0_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_SPI0_CLK_STATUS_CURRDIVIDER								MSS_SPI0_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-1922. MCSPI0_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_SPI0_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for Corresponding SPI Reset Source: mod_g_rst_n
7:0	MSS_SPI0_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for Corresponding SPI Reset Source: mod_g_rst_n

2.6.146 CFG0_MCSPI1_CLK_STATUS Registers

2.6.146.1 CFG0_CLK_STATUS Register (Offset = 440h) [reset = 1h]

Short Description:

Long Description:

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Table 2-1923. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8440h

Figure 2-957. MCSPI1_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_SPI1_CLK_STATUS_CURRDIVIDER								MSS_SPI1_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-1924. MCSPI1_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_SPI1_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for Corresponding SPI Reset Source: mod_g_rst_n
7:0	MSS_SPI1_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for Corresponding SPI Reset Source: mod_g_rst_n

2.6.147 CFG0_MCSPI2_CLK_STATUS Registers

2.6.147.1 CFG0_CLK_STATUS Register (Offset = 444h) [reset = 1h]

Short Description:

Long Description:

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Table 2-1925. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8444h

Figure 2-958. MCSPI2_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_SPI2_CLK_STATUS_CURRDIVIDER								MSS_SPI2_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-1926. MCSPI2_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_SPI2_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for Corresponding SPI Reset Source: mod_g_rst_n
7:0	MSS_SPI2_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for Corresponding SPI Reset Source: mod_g_rst_n

2.6.148 CFG0_MCSPI3_CLK_STATUS Registers

2.6.148.1 CFG0_CLK_STATUS Register (Offset = 448h) [reset = 1h]

Short Description:

Long Description:

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Table 2-1927. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8448h

Figure 2-959. MCSPI3_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_SPI3_CLK_STATUS_CURRDIVIDER								MSS_SPI3_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-1928. MCSPI3_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_SPI3_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for Corresponding SPI Reset Source: mod_g_rst_n
7:0	MSS_SPI3_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for Corresponding SPI Reset Source: mod_g_rst_n

2.6.149 CFG0_MCSPI4_CLK_STATUS Registers

2.6.149.1 CFG0_CLK_STATUS Register (Offset = 44Ch) [reset = 1h]

Short Description:

Long Description:

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Table 2-1929. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 844Ch

Figure 2-960. MCSPI4_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_SPI4_CLK_STATUS_CURRDIVIDER								MSS_SPI4_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-1930. MCSPI4_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_SPI4_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for Corresponding SPI Reset Source: mod_g_rst_n
7:0	MSS_SPI4_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for Corresponding SPI Reset Source: mod_g_rst_n

2.6.150 CFG0_MMC0_CLK_STATUS Registers

2.6.150.1 CFG0_CLK_STATUS Register (Offset = 450h) [reset = 1h]

Short Description:

Long Description:

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Table 2-1931. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8450h

Figure 2-961. MMC0_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_MMCSD_CLK_STATUS_CURRDIVIDER								MSS_MMCSD_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-1932. MMC0_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_MMCSD_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for MMCSD Reset Source: mod_g_rst_n
7:0	MSS_MMCSD_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for MMCSD Reset Source: mod_g_rst_n

2.6.151 CFG0_PRU-ICSS_UCLK_CLK_STATUS Registers

2.6.151.1 CFG0_UCLK_CLK_STATUS Register (Offset = 454h) [reset = 1h]

Short Description:

Long Description:

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Table 2-1933. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8454h

Figure 2-962. PRU-ICSS_UCLK_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRU-ICSS_UCLK_CLK_STATUS_CURRDIVIDER								PRU-ICSS_UCLK_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-1934. PRU-ICSS_UCLK_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	PRU-ICSS_UCLK_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for ICSSM_UCLK Reset Source: mod_g_rst_n
7:0	PRU-ICSS_UCLK_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for ICSSM_UCLK Reset Source: mod_g_rst_n

2.6.152 CFG0_CPTS_CLK_STATUS Registers

2.6.152.1 CFG0_CLK_STATUS Register (Offset = 458h) [reset = 1h]

Short Description:

Long Description:

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Table 2-1935. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8458h

Figure 2-963. CPTS_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_CPTS_CLK_STATUS_CURRDIVIDER								MSS_CPTS_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-1936. CPTS_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_CPTS_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for CPTS Reset Source: mod_g_rst_n
7:0	MSS_CPTS_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for CPTS Reset Source: mod_g_rst_n

2.6.153 CFG0_GPMC_CLK_STATUS Registers

2.6.153.1 CFG0_CLK_STATUS Register (Offset = 45Ch) [reset = 1h]

Short Description:

Long Description:

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Table 2-1937. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 845Ch

Figure 2-964. GPMC_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_CLK_STATUS_CURRDIVIDER								GPMC_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-1938. GPMC_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	GPMC_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for GPMC Reset Source: mod_g_rst_n
7:0	GPMC_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for GPMC Reset Source: mod_g_rst_n

2.6.154 CFG0_CONTROLSS_PLL_CLK_STATUS Registers

2.6.154.1 CFG0_PLL_CLK_STATUS Register (Offset = 460h) [reset = 1h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1939. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8460h

Figure 2-965. CONTROLSS_PLL_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONTROLSS_PLL_CLK_STATUS_CURRDIVIDER								CONTROLSS_PLL_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-1940. CONTROLSS_PLL_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	CONTROLSS_PLL_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for CONTROLSS_PLL Reset Source: mod_g_rst_n
7:0	CONTROLSS_PLL_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for CONTROLSS_PLL Reset Source: mod_g_rst_n

2.6.155 CFG0_I2C_CLK_STATUS Registers

2.6.155.1 CFG0_CLK_STATUS Register (Offset = 464h) [reset = 1h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1941. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8464h

Figure 2-966. I2C_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_I2C_CLK_STATUS_CURRDIVIDER								MSS_I2C_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-1942. I2C_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_I2C_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for I2C Reset Source: mod_g_rst_n
7:0	MSS_I2C_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for I2C Reset Source: mod_g_rst_n

2.6.156 CFG0_LIN0_UART0_CLK_STATUS Registers

2.6.156.1 CFG0_UART0_CLK_STATUS Register (Offset = 474h) [reset = 1h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1943. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8474h

Figure 2-967. LIN0_UART0_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_LIN0_UART0_CLK_STATUS_CURRDIVIDER								MSS_LIN0_UART0_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-1944. LIN0_UART0_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_LIN0_UART0_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for corresponding UART and LIN Reset Source: mod_g_rst_n
7:0	MSS_LIN0_UART0_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for corresponding UART and LIN Reset Source: mod_g_rst_n

2.6.157 CFG0_LIN1_UART1_CLK_STATUS Registers

2.6.157.1 CFG0_UART1_CLK_STATUS Register (Offset = 478h) [reset = 1h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1945. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8478h

Figure 2-968. LIN1_UART1_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_LIN1_UART1_CLK_STATUS_CURRDIVIDER								MSS_LIN1_UART1_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-1946. LIN1_UART1_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_LIN1_UART1_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for corresponding UART and LIN Reset Source: mod_g_rst_n
7:0	MSS_LIN1_UART1_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for corresponding UART and LIN Reset Source: mod_g_rst_n

2.6.158 CFG0_LIN2_UART2_CLK_STATUS Registers

2.6.158.1 CFG0_UART2_CLK_STATUS Register (Offset = 47Ch) [reset = 1h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1947. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 847Ch

Figure 2-969. LIN2_UART2_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_LIN2_UART2_CLK_STATUS_CURRDIVIDER								MSS_LIN2_UART2_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-1948. LIN2_UART2_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_LIN2_UART2_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for corresponding UART and LIN Reset Source: mod_g_rst_n
7:0	MSS_LIN2_UART2_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for corresponding UART and LIN Reset Source: mod_g_rst_n

2.6.159 CFG0_LIN3_UART3_CLK_STATUS Registers

2.6.159.1 CFG0_UART3_CLK_STATUS Register (Offset = 480h) [reset = 1h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1949. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8480h

Figure 2-970. LIN3_UART3_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_LIN3_UART3_CLK_STATUS_CURRDIVIDER								MSS_LIN3_UART3_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-1950. LIN3_UART3_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_LIN3_UART3_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for corresponding UART and LIN Reset Source: mod_g_rst_n
7:0	MSS_LIN3_UART3_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for corresponding UART and LIN Reset Source: mod_g_rst_n

2.6.160 CFG0_LIN4_UART4_CLK_STATUS Registers

2.6.160.1 CFG0_UART4_CLK_STATUS Register (Offset = 484h) [reset = 1h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1951. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8484h

Figure 2-971. LIN4_UART4_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_LIN4_UART4_CLK_STATUS_CURRDIVIDER								MSS_LIN4_UART4_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-1952. LIN4_UART4_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_LIN4_UART4_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for corresponding UART and LIN Reset Source: mod_g_rst_n
7:0	MSS_LIN4_UART4_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for corresponding UART and LIN Reset Source: mod_g_rst_n

2.6.161 CFG0_LIN5_UART5_CLK_STATUS Registers

2.6.161.1 CFG0_UART5_CLK_STATUS Register (Offset = 488h) [reset = 1h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1953. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8488h

Figure 2-972. LIN5_UART5_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_LIN5_UART5_CLK_STATUS_CURRDIVIDER								MSS_LIN5_UART5_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-1954. LIN5_UART5_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_LIN5_UART5_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for corresponding UART and LIN Reset Source: mod_g_rst_n
7:0	MSS_LIN5_UART5_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for corresponding UART and LIN Reset Source: mod_g_rst_n

2.6.162 CFG0_RGMII_250_CLK_STATUS Registers

2.6.162.1 CFG0_250_CLK_STATUS Register (Offset = 48Ch) [reset = 100h]

Short Description:

Long Description:

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Table 2-1955. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 848Ch

Figure 2-973. RGMII_250_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
989680															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_RGMII_CLK_STATUS_CURRDIVIDER								RESERVED							
R								NONE							
1h								0							

Access Types Legend

Table 2-1956. RGMII_250_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_RGMII_CLK_STATUS_CURRDIVIDER	R	1h	Status shows the current divider value choosen for RGMII Reset Source: mod_g_rst_n
7:0	RESERVED	NONE		Reserved

2.6.163 CFG0_RGMII_50_CLK_STATUS Registers

2.6.163.1 CFG0_50_CLK_STATUS Register (Offset = 490h) [reset = 900h]

Short Description:

Long Description:

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Table 2-1957. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8490h

Figure 2-974. RGMII_50_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
254a47a80															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_MII100_CLK_STATUS_CURRDIVIDER								RESERVED							
R								NONE							
9h								0							

Access Types Legend

Table 2-1958. RGMII_50_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_MII100_CLK_STATUS_CURRDIVIDER	R	9h	Status shows the current divider value choosen for MII100 Reset Source: mod_g_rst_n
7:0	RESERVED	NONE		Reserved

2.6.164 CFG0_RGMII_5_CLK_STATUS Registers

2.6.164.1 CFG0_5_CLK_STATUS Register (Offset = 494h) [reset = 6300h]

Short Description:

Long Description:

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Table 2-1959. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8494h

Figure 2-975. RGMII_5_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
a0129a62780															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_MII10_CLK_STATUS_CURRDIVIDER								RESERVED							
R								NONE							
63h								0							

Access Types Legend

Table 2-1960. RGMII_5_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_MII10_CLK_STATUS_CURRDIVIDER	R	63h	Status shows the current divider value choosen for MII10 Reset Source: mod_g_rst_n
7:0	RESERVED	NONE		Reserved

2.6.165 CFG0_MMC0_32K_CLK_STATUS Registers

2.6.165.1 CFG0_32K_CLK_STATUS Register (Offset = 49Ch) [reset = 30c00h]

Short Description:

Long Description:

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Table 2-1961. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 849Ch

Figure 2-976. MMC0_32K_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														MMC0_32K_CLK_STATUS_CURRDIVIDER	
NONE														R	
28fa6ae00														30ch	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MMC0_32K_CLK_STATUS_CURRDIVIDER								RESERVED							
R								NONE							
30ch								0							

Access Types Legend

Table 2-1962. MMC0_32K_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE		Reserved
17:8	MMC0_32K_CLK_STATUS_CURRDIVIDER	R	30Ch	Status shows the current divider value choosen for XTAL_32K Reset Source: mod_g_rst_n
7:0	RESERVED	NONE		Reserved

2.6.166 CFG0_TEMPSENSE_32K_CLK_STATUS Registers

2.6.166.1 CFG0_32K_CLK_STATUS Register (Offset = 4A0h) [reset = 30c00h]

Short Description:

Long Description:

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Table 2-1963. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 84A0h

Figure 2-977. TEMPSENSE_32K_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														TEMPSENSE_32K_CLK_STATUS_CURRDIVIDER	
NONE														R	
28fa6ae00														30ch	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEMPSENSE_32K_CLK_STATUS_CURRDIVIDER								RESERVED							
R								NONE							
30ch								0							

Access Types Legend

Table 2-1964. TEMPSENSE_32K_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE		Reserved
17:8	TEMPSENSE_32K_CLK_STATUS_CURRDIVIDER	R	30Ch	Status shows the current divider value choosen for XTAL_32K Reset Source: mod_g_rst_n
7:0	RESERVED	NONE		Reserved

2.6.167 CFG0_MSS_ELM_CLK_STATUS Registers

2.6.167.1 CFG0_ELM_CLK_STATUS Register (Offset = 4A4h) [reset = 300h]

Short Description:

Long Description:

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Table 2-1965. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 84A4h

Figure 2-978. MSS_ELM_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
68e7780															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSS_ELM_CLK_STATUS_CURRDIVIDER								RESERVED							
R								NONE							
3h								0							

Access Types Legend

Table 2-1966. MSS_ELM_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MSS_ELM_CLK_STATUS_CURRDIVIDER	R	3h	Status shows the current divider value choosen for ELM Reset Source: mod_g_rst_n
7:0	RESERVED	NONE		Reserved

2.6.168 CFG0_R5SS0_POR_RST_CTRL Registers

2.6.168.1 CFG0_POR_RST_CTRL Register (Offset = 500h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1967. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8500h

Figure 2-979. R5SS0_POR_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_CR5SS_POR_RST_CTRL0_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1968. R5SS0_POR_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_CR5SS_POR_RST_CTRL0_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. write pulse bit field: writing 111 will assert por reset to R5SS Read is always 000 Reset Source: mod_g_rst_n

2.6.169 CFG0_R5SS1_POR_RST_CTRL Registers

2.6.169.1 CFG0_POR_RST_CTRL Register (Offset = 504h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1969. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8504h

Figure 2-980. R5SS1_POR_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_CR5SS_POR_RST_CTRL1_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1970. R5SS1_POR_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_CR5SS_POR_RST_CTRL1_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. write pulse bit field: writing 111 will assert por reset to R5SS Read is always 000 Reset Source: mod_g_rst_n

2.6.170 CFG0_R5SS0_CORE0_GRST_CTRL Registers

2.6.170.1 CFG0_CORE0_GRST_CTRL Register (Offset = 508h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1971. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8508h

Figure 2-981. R5SS0_CORE0_GRST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_CR5SSA_RST_CTRL0_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1972. R5SS0_CORE0_GRST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_CR5SSA_RST_CTRL0_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. write pulse bit field: writing 111 will reset CORE0 and MSS_CORE0_VIM Reset Source: mod_g_rst_n

2.6.171 CFG0_R5SS1_CORE0_GRST_CTRL Registers

2.6.171.1 CFG0_CORE0_GRST_CTRL Register (Offset = 50Ch) [reset = 0h]

Short Description:

Long Description:

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Table 2-1973. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 850Ch

Figure 2-982. R5SS1_CORE0_GRST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_CR5SSA_RST_CTRL1_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1974. R5SS1_CORE0_GRST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_CR5SSA_RST_CTRL1_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. write pulse bit field: writing 111 will reset CORE0 and MSS_CORE0_VIM Reset Source: mod_g_rst_n

2.6.172 CFG0_R5SS0_CORE1_GRST_CTRL Registers

2.6.172.1 CFG0_CORE1_GRST_CTRL Register (Offset = 510h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1975. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8510h

Figure 2-983. R5SS0_CORE1_GRST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_CR5SSB_RST_CTRL0_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1976. R5SS0_CORE1_GRST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_CR5SSB_RST_CTRL0_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. write pulse bit field: writing 111 will reset CORE1 and MSS_CORE1_VIM Reset Source: mod_g_rst_n

2.6.173 CFG0_R5SS1_CORE1_GRST_CTRL Registers

2.6.173.1 CFG0_CORE1_GRST_CTRL Register (Offset = 514h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1977. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8514h

Figure 2-984. R5SS1_CORE1_GRST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_CR5SSB_RST_CTRL1_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1978. R5SS1_CORE1_GRST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_CR5SSB_RST_CTRL1_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. write pulse bit field: writing 111 will reset CORE1 and MSS_CORE1_VIM Reset Source: mod_g_rst_n

2.6.174 CFG0_R5SS0_CORE0_LRST_CTRL Registers

2.6.174.1 CFG0_CORE0_LRST_CTRL Register (Offset = 518h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1979. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8518h

Figure 2-985. R5SS0_CORE0_LRST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_R5FSS0_RST_CTRL0_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1980. R5SS0_CORE0_LRST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_R5FSS0_RST_CTRL0_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. write pulse bit field: writing 111 will reset CORE0 only Reset Source: mod_g_rst_n

2.6.175 CFG0_R5SS1_CORE0_LRST_CTRL Registers

2.6.175.1 CFG0_CORE0_LRST_CTRL Register (Offset = 51Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1981. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 851Ch

Figure 2-986. R5SS1_CORE0_LRST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_R5FSS0_RST_CTRL1_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1982. R5SS1_CORE0_LRST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_R5FSS0_RST_CTRL1_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. write pulse bit field: writing 111 will reset CORE0 only Reset Source: mod_g_rst_n

2.6.176 CFG0_R5SS0_CORE1_LRST_CTRL Registers

2.6.176.1 CFG0_CORE1_LRST_CTRL Register (Offset = 520h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1983. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8520h

Figure 2-987. R5SS0_CORE1_LRST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_R5FSS1_RST_CTRL0_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1984. R5SS0_CORE1_LRST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_R5FSS1_RST_CTRL0_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. write pulse bit field: writing 111 will reset CORE1 only Reset Source: mod_g_rst_n

2.6.177 CFG0_R5SS1_CORE1_LRST_CTRL Registers

2.6.177.1 CFG0_CORE1_LRST_CTRL Register (Offset = 524h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1985. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8524h

Figure 2-988. R5SS1_CORE1_LRST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_R5FSS1_RST_CTRL1_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1986. R5SS1_CORE1_LRST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_R5FSS1_RST_CTRL1_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. write pulse bit field: writing 111 will reset CORE1 only Reset Source: mod_g_rst_n

2.6.178 CFG0_R5SS0_VIM0_RST_CTRL Registers

2.6.178.1 CFG0_VIM0_RST_CTRL Register (Offset = 528h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1987. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8528h

Figure 2-989. R5SS0_VIM0_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_VIMA_RST_CTRL 0_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1988. R5SS0_VIM0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_VIMA_RST_CTRL0 _ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset MSS_CORE0_VIM Writing 000 will deassert the reset Reset Source: mod_g_rst_n

2.6.179 CFG0_R5SS1_VIM0_RST_CTRL Registers

2.6.179.1 CFG0_VIM0_RST_CTRL Register (Offset = 52Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1989. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 852Ch

Figure 2-990. R5SS1_VIM0_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_VIMA_RST_CTRL 1_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1990. R5SS1_VIM0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_VIMA_RST_CTRL1 _ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset MSS_CORE0_VIM Writing 000 will deassert the reset Reset Source: mod_g_rst_n

2.6.180 CFG0_R5SS0_VIM1_RST_CTRL Registers

2.6.180.1 CFG0_VIM1_RST_CTRL Register (Offset = 530h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1991. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8530h

Figure 2-991. R5SS0_VIM1_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_VIMB_RST_CTRL0_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1992. R5SS0_VIM1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_VIMB_RST_CTRL0_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset MSS_CORE1_VIM Reset Source: mod_g_rst_n

2.6.181 CFG0_R5SS1_VIM1_RST_CTRL Registers

2.6.181.1 CFG0_VIM1_RST_CTRL Register (Offset = 534h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1993. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8534h

Figure 2-992. R5SS1_VIM1_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_VIMB_RST_CTRL 1_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1994. R5SS1_VIM1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_VIMB_RST_CTRL1 _ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset MSS_CORE1_VIM Reset Source: mod_g_rst_n

2.6.182 CFG0_MCRC0_RST_CTRL Registers

2.6.182.1 CFG0_RST_CTRL Register (Offset = 538h) [reset = 0h]

Short Description:

Long Description:

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Table 2-1995. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8538h

Figure 2-993. MCRC0_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_CRC_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1996. MCRC0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_CRC_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset MCRC Reset Source: mod_g_rst_n

2.6.183 CFG0_RTI0_RST_CTRL Registers

2.6.183.1 CFG0_RST_CTRL Register (Offset = 53Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1997. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 853Ch

Figure 2-994. RTI0_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_RTI0_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-1998. RTI0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_RTI0_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset corresponding RTI Reset Source: mod_g_rst_n

2.6.184 CFG0_RTI1_RST_CTRL Registers

2.6.184.1 CFG0_RST_CTRL Register (Offset = 540h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-1999. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8540h

Figure 2-995. RTI1_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_RTI1_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2000. RTI1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_RTI1_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset corresponding RTI Reset Source: mod_g_rst_n

2.6.185 CFG0_RTI2_RST_CTRL Registers

2.6.185.1 CFG0_RST_CTRL Register (Offset = 544h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2001. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8544h

Figure 2-996. RTI2_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_RTI2_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2002. RTI2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_RTI2_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset corresponding RTI Reset Source: mod_g_rst_n

2.6.186 CFG0_RTI3_RST_CTRL Registers

2.6.186.1 CFG0_RST_CTRL Register (Offset = 548h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2003. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8548h

Figure 2-997. RTI3_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_RTI3_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2004. RTI3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_RTI3_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset corresponding RTI Reset Source: mod_g_rst_n

2.6.187 CFG0_WDT0_RST_CTRL Registers

2.6.187.1 CFG0_RST_CTRL Register (Offset = 54Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2005. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 854Ch

Figure 2-998. WDT0_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_WDT0_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2006. WDT0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_WDT0_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset WDT Reset Source: mod_g_rst_n

2.6.188 CFG0_WDT1_RST_CTRL Registers

2.6.188.1 CFG0_RST_CTRL Register (Offset = 550h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2007. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8550h

Figure 2-999. WDT1_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_WDT1_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2008. WDT1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_WDT1_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset WDT Reset Source: mod_g_rst_n

2.6.189 CFG0_WDT2_RST_CTRL Registers

2.6.189.1 CFG0_RST_CTRL Register (Offset = 554h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2009. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8554h

Figure 2-1000. WDT2_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_WDT2_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2010. WDT2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_WDT2_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset WDT Reset Source: mod_g_rst_n

2.6.190 CFG0_WDT3_RST_CTRL Registers

2.6.190.1 CFG0_RST_CTRL Register (Offset = 558h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2011. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8558h

Figure 2-1001. WDT3_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_WDT3_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2012. WDT3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_WDT3_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset WDT Reset Source: mod_g_rst_n

2.6.191 CFG0_TOP_ESM_RST_CTRL Registers

2.6.191.1 CFG0_ESM_RST_CTRL Register (Offset = 55Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2013. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 855Ch

Figure 2-1002. TOP_ESM_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_ESM_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2014. TOP_ESM_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_ESM_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset ESM Reset Source: mod_g_rst_n

2.6.192 CFG0_DCC0_RST_CTRL Registers

2.6.192.1 CFG0_RST_CTRL Register (Offset = 560h) [reset = 0h]

Short Description:

Long Description:

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Table 2-2015. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8560h

Figure 2-1003. DCC0_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_DCCA_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2016. DCC0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_DCCA_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset DCCA Reset Source: mod_g_rst_n

2.6.193 CFG0_DCC1_RST_CTRL Registers

2.6.193.1 CFG0_RST_CTRL Register (Offset = 564h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2017. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8564h

Figure 2-1004. DCC1_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_DCCB_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2018. DCC1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_DCCB_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset DCCB Reset Source: mod_g_rst_n

2.6.194 CFG0_DCC2_RST_CTRL Registers

2.6.194.1 CFG0_RST_CTRL Register (Offset = 568h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2019. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8568h

Figure 2-1005. DCC2_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_DCCC_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2020. DCC2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_DCCC_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset DCCC Reset Source: mod_g_rst_n

2.6.195 CFG0_DCC3_RST_CTRL Registers

2.6.195.1 CFG0_RST_CTRL Register (Offset = 56Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2021. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 856Ch

Figure 2-1006. DCC3_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_DCCD_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2022. DCC3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_DCCD_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset DCCD Reset Source: mod_g_rst_n

2.6.196 CFG0_MCSPI0_RST_CTRL Registers

2.6.196.1 CFG0_RST_CTRL Register (Offset = 570h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2023. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8570h

Figure 2-1007. MCSPI0_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_SPI0_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2024. MCSPI0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_SPI0_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset Corresponding SPI Reset Source: mod_g_rst_n

2.6.197 CFG0_MCSPI1_RST_CTRL Registers

2.6.197.1 CFG0_RST_CTRL Register (Offset = 574h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2025. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8574h

Figure 2-1008. MCSPI1_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_SPI1_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2026. MCSPI1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_SPI1_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset Corresponding SPI Reset Source: mod_g_rst_n

2.6.198 CFG0_MCSPI2_RST_CTRL Registers

2.6.198.1 CFG0_RST_CTRL Register (Offset = 578h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2027. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8578h

Figure 2-1009. MCSPI2_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_SPI2_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2028. MCSPI2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_SPI2_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset Corresponding SPI Reset Source: mod_g_rst_n

2.6.199 CFG0_MCSPI3_RST_CTRL Registers

2.6.199.1 CFG0_RST_CTRL Register (Offset = 57Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2029. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 857Ch

Figure 2-1010. MCSPI3_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_SPI3_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2030. MCSPI3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_SPI3_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset Corresponding SPI Reset Source: mod_g_rst_n

2.6.200 CFG0_MCSPI4_RST_CTRL Registers

2.6.200.1 CFG0_RST_CTRL Register (Offset = 580h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2031. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8580h

Figure 2-1011. MCSPI4_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_SPI4_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2032. MCSPI4_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_SPI4_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset Corresponding SPI Reset Source: mod_g_rst_n

2.6.201 CFG0_QSPI0_RST_CTRL Registers

2.6.201.1 CFG0_RST_CTRL Register (Offset = 584h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2033. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8584h

Figure 2-1012. QSPI0_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_QSPI_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2034. QSPI0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_QSPI_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset QSPI Reset Source: mod_g_rst_n

2.6.202 CFG0_MCAN0_RST_CTRL Registers

2.6.202.1 CFG0_RST_CTRL Register (Offset = 588h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2035. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8588h

Figure 2-1013. MCAN0_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_MCAN0_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2036. MCAN0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_MCAN0_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset corresponding MCAN Reset Source: mod_g_rst_n

2.6.203 CFG0_MCAN1_RST_CTRL Registers

2.6.203.1 CFG0_RST_CTRL Register (Offset = 58Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2037. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 858Ch

Figure 2-1014. MCAN1_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_MCAN1_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2038. MCAN1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_MCAN1_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset corresponding MCAN Reset Source: mod_g_rst_n

2.6.204 CFG0_MCAN2_RST_CTRL Registers

2.6.204.1 CFG0_RST_CTRL Register (Offset = 590h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2039. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8590h

Figure 2-1015. MCAN2_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_MCAN2_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2040. MCAN2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_MCAN2_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset corresponding MCAN Reset Source: mod_g_rst_n

2.6.205 CFG0_MCAN3_RST_CTRL Registers

2.6.205.1 CFG0_RST_CTRL Register (Offset = 594h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2041. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8594h

Figure 2-1016. MCAN3_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_MCAN3_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2042. MCAN3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_MCAN3_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset corresponding MCAN Reset Source: mod_g_rst_n

2.6.206 CFG0_I2C0_RST_CTRL Registers

2.6.206.1 CFG0_RST_CTRL Register (Offset = 598h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2043. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8598h

Figure 2-1017. I2C0_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_I2C0_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2044. I2C0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_I2C0_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset corresponding I2C Reset Source: mod_g_rst_n

2.6.207 CFG0_I2C1_RST_CTRL Registers

2.6.207.1 CFG0_RST_CTRL Register (Offset = 59Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2045. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 859Ch

Figure 2-1018. I2C1_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_I2C1_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2046. I2C1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_I2C1_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset corresponding I2C Reset Source: mod_g_rst_n

2.6.208 CFG0_I2C2_RST_CTRL Registers

2.6.208.1 CFG0_RST_CTRL Register (Offset = 5A0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2047. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 85A0h

Figure 2-1019. I2C2_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_I2C2_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2048. I2C2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_I2C2_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset corresponding I2C Reset Source: mod_g_rst_n

2.6.209 CFG0_I2C3_RST_CTRL Registers

2.6.209.1 CFG0_RST_CTRL Register (Offset = 5A4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2049. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 85A4h

Figure 2-1020. I2C3_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_I2C3_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2050. I2C3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_I2C3_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset corresponding I2C Reset Source: mod_g_rst_n

2.6.210 CFG0_UART0_RST_CTRL Registers

2.6.210.1 CFG0_RST_CTRL Register (Offset = 5A8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2051. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 85A8h

Figure 2-1021. UART0_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_UART0_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2052. UART0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_UART0_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset corresponding UART instance Reset Source: mod_g_rst_n

2.6.211 CFG0_UART1_RST_CTRL Registers

2.6.211.1 CFG0_RST_CTRL Register (Offset = 5ACh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2053. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 85ACh

Figure 2-1022. UART1_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_UART1_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2054. UART1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_UART1_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset corresponding UART instance Reset Source: mod_g_rst_n

2.6.212 CFG0_UART2_RST_CTRL Registers

2.6.212.1 CFG0_RST_CTRL Register (Offset = 5B0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2055. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 85B0h

Figure 2-1023. UART2_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_UART2_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2056. UART2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_UART2_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset corresponding UART instance Reset Source: mod_g_rst_n

2.6.213 CFG0_UART3_RST_CTRL Registers

2.6.213.1 CFG0_RST_CTRL Register (Offset = 5B4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2057. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 85B4h

Figure 2-1024. UART3_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_UART3_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2058. UART3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_UART3_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset corresponding UART instance Reset Source: mod_g_rst_n

2.6.214 CFG0_UART4_RST_CTRL Registers

2.6.214.1 CFG0_RST_CTRL Register (Offset = 5B8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2059. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 85B8h

Figure 2-1025. UART4_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_UART4_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2060. UART4_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_UART4_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset corresponding UART instance Reset Source: mod_g_rst_n

2.6.215 CFG0_UART5_RST_CTRL Registers

2.6.215.1 CFG0_RST_CTRL Register (Offset = 5BCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2061. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 85BCh

Figure 2-1026. UART5_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_UART5_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2062. UART5_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_UART5_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset corresponding UART instance Reset Source: mod_g_rst_n

2.6.216 CFG0_LIN0_RST_CTRL Registers

2.6.216.1 CFG0_RST_CTRL Register (Offset = 5C0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2063. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 85C0h

Figure 2-1027. LIN0_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_LIN0_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2064. LIN0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_LIN0_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset LIN Reset Source: mod_g_rst_n

2.6.217 CFG0_LIN1_RST_CTRL Registers

2.6.217.1 CFG0_RST_CTRL Register (Offset = 5C4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2065. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 85C4h

Figure 2-1028. LIN1_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_LIN1_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2066. LIN1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_LIN1_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset LIN Reset Source: mod_g_rst_n

2.6.218 CFG0_LIN2_RST_CTRL Registers

2.6.218.1 CFG0_RST_CTRL Register (Offset = 5C8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2067. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 85C8h

Figure 2-1029. LIN2_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_LIN2_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2068. LIN2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_LIN2_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset LIN Reset Source: mod_g_rst_n

2.6.219 CFG0_LIN3_RST_CTRL Registers

2.6.219.1 CFG0_RST_CTRL Register (Offset = 5CCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2069. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 85CCh

Figure 2-1030. LIN3_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_LIN3_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2070. LIN3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_LIN3_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset LIN Reset Source: mod_g_rst_n

2.6.220 CFG0_LIN4_RST_CTRL Registers

2.6.220.1 CFG0_RST_CTRL Register (Offset = 5D0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2071. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 85D0h

Figure 2-1031. LIN4_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_LIN4_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2072. LIN4_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_LIN4_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset LIN Reset Source: mod_g_rst_n

2.6.221 CFG0_EDMA_RST_CTRL Registers

2.6.221.1 CFG0_RST_CTRL Register (Offset = 5D8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2073. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 85D8h

Figure 2-1032. EDMA_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	MSS_EDMA_RST_CTRL_TPTCA1_ASSERT			RESERVED	MSS_EDMA_RST_CTRL_TPTCA0_ASSERT			RESERVED	MSS_EDMA_RST_CTRL_TPCCA_ASSERT			RESERVED	MSS_EDMA_RST_CTRL_ASSERT		
NONE	R/W			NONE	R/W			NONE	R/W			NONE	R/W		
0	0h			0	0h			0	0h			0	0h		

Access Types Legend

Table 2-2074. EDMA_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE		Reserved
14:12	MSS_EDMA_RST_CTRL_TPTCA1_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset MSS_TPTCA1 Reset Source: mod_g_rst_n
11	RESERVED	NONE		Reserved
10:8	MSS_EDMA_RST_CTRL_TPTCA0_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset MSS_TPTCA0 Reset Source: mod_g_rst_n
7	RESERVED	NONE		Reserved
6:4	MSS_EDMA_RST_CTRL_TPCCA_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset MSS_TPCCA Reset Source: mod_g_rst_n
3	RESERVED	NONE		Reserved
2:0	MSS_EDMA_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset EDMA Reset Source: mod_g_rst_n

2.6.222 CFG0_INFRA_RST_CTRL Registers

2.6.222.1 CFG0_RST_CTRL Register (Offset = 5DCh) [reset = 0h]

Short Description:

Long Description:

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Table 2-2075. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 85DCh

Figure 2-1033. INFRA_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_INFRA_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2076. INFRA_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_INFRA_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset MSS INFRA Reset Source: mod_g_rst_n

2.6.223 CFG0_CPSW_RST_CTRL Registers

2.6.223.1 CFG0_RST_CTRL Register (Offset = 5E0h) [reset = 0h]

Short Description:

Long Description:

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Table 2-2077. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 85E0h

Figure 2-1034. CPSW_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_CPSW_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2078. CPSW_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_CPSW_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset MSS CPSW Reset Source: mod_g_rst_n

2.6.224 CFG0_MSS_PRU-ICSS_RST_CTRL Registers

2.6.224.1 CFG0_PRU-ICSS_RST_CTRL Register (Offset = 5E4h) [reset = 0h]

Short Description:

Long Description:

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Table 2-2079. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 85E4h

Figure 2-1035. MSS_PRU-ICSS_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															MSS_PRU-ICSS_RST_CTRL_ASSERT
NONE															R/W
0															0h

Access Types Legend

Table 2-2080. MSS_PRU-ICSS_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_PRU-ICSS_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset MSS ICSSM Reset Source: mod_g_rst_n

2.6.225 CFG0_MMC0_RST_CTRL Registers

2.6.225.1 CFG0_RST_CTRL Register (Offset = 5E8h) [reset = 0h]

Short Description:

Long Description:

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Table 2-2081. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 85E8h

Figure 2-1036. MMC0_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_MMCSD_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2082. MMC0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_MMCSD_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset MMCSD Reset Source: mod_g_rst_n

2.6.226 CFG0_GPIO0_RST_CTRL Registers

2.6.226.1 CFG0_RST_CTRL Register (Offset = 5ECh) [reset = 0h]

Short Description:

Long Description:

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Table 2-2083. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 85ECh

Figure 2-1037. GPIO0_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_GPIO0_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2084. GPIO0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_GPIO0_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset corresponding GPIO Reset Source: mod_g_rst_n

2.6.227 CFG0_GPIO1_RST_CTRL Registers

2.6.227.1 CFG0_RST_CTRL Register (Offset = 5F0h) [reset = 0h]

Short Description:

Long Description:

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Table 2-2085. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 85F0h

Figure 2-1038. GPIO1_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_GPIO1_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2086. GPIO1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_GPIO1_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset corresponding GPIO Reset Source: mod_g_rst_n

2.6.228 CFG0_GPIO2_RST_CTRL Registers

2.6.228.1 CFG0_RST_CTRL Register (Offset = 5F4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2087. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 85F4h

Figure 2-1039. GPIO2_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_GPIO2_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2088. GPIO2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_GPIO2_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset corresponding GPIO Reset Source: mod_g_rst_n

2.6.229 CFG0_GPIO3_RST_CTRL Registers

2.6.229.1 CFG0_RST_CTRL Register (Offset = 5F8h) [reset = 0h]

Short Description:

Long Description:

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Table 2-2089. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 85F8h

Figure 2-1040. GPIO3_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_GPIO3_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2090. GPIO3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_GPIO3_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset corresponding GPIO Reset Source: mod_g_rst_n

2.6.230 CFG0_SPINLOCK0_RST_CTRL Registers

2.6.230.1 CFG0_RST_CTRL Register (Offset = 5FCh) [reset = 0h]

Short Description:

Long Description:

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Table 2-2091. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 85FCh

Figure 2-1041. SPINLOCK0_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_SPINLOCK_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2092. SPINLOCK0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_SPINLOCK_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset SPINLOCK Reset Source: mod_g_rst_n

2.6.231 CFG0_GPMC_RST_CTRL Registers

2.6.231.1 CFG0_RST_CTRL Register (Offset = 600h) [reset = 0h]

Short Description:

Long Description:

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Table 2-2093. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8600h

Figure 2-1042. GPMC_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													GPMC_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2094. GPMC_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	GPMC_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset GPMC Reset Source: mod_g_rst_n

2.6.232 CFG0_TEMPSENSE_32K_RST_CTRL Registers

2.6.232.1 CFG0_32K_RST_CTRL Register (Offset = 604h) [reset = 0h]

Short Description:

Long Description:

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Table 2-2095. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8604h

Figure 2-1043. TEMPSENSE_32K_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													TEMPSENSE_32K_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2096. TEMPSENSE_32K_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	TEMPSENSE_32K_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset TEMPSENSE **Note: This bit will only be reset by PORz. Reset Source: mod_por_rst_n

2.6.233 CFG0_MSS_ELM_RST_CTRL Registers

2.6.233.1 CFG0_ELM_RST_CTRL Register (Offset = 608h) [reset = 0h]

Short Description:

Long Description:

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Table 2-2097. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8608h

Figure 2-1044. MSS_ELM_RST_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MSS_ELM_RST_CTRL_ASSERT		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2098. MSS_ELM_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	MSS_ELM_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 111 will reset ELM Reset Source: mod_g_rst_n

2.6.234 CFG0_L2OCRAM_BANK0_PD_CTRL Registers

2.6.234.1 CFG0_BANK0_PD_CTRL Register (Offset = 700h) [reset = 770h]

Short Description:

Long Description:

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Table 2-2099. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8700h

Figure 2-1045. L2OCRAM_BANK0_PD_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
422af318															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					MSS_L2_BANKA_PD_CTRL_AGOODIN			RESERVED	MSS_L2_BANKA_PD_CTRL_AONIN			RESERVED	MSS_L2_BANKA_PD_CTRL_ISO		
NONE					R/W			NONE	R/W			NONE	R/W		
422af318					7h			0	7h			0	0h		

Access Types Legend

Table 2-2100. L2OCRAM_BANK0_PD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE		Reserved
10:8	MSS_L2_BANKA_PD_CTRL_AGOODIN	R/W	7h	SW control for power signal AGOODIN for MSS_L2_BANKA Reset Source: mod_g_rst_n
7	RESERVED	NONE		Reserved
6:4	MSS_L2_BANKA_PD_CTRL_AONIN	R/W	7h	SW control for power signal AONIN for MSS_L2_BANKA Reset Source: mod_g_rst_n
3	RESERVED	NONE		Reserved
2:0	MSS_L2_BANKA_PD_CTRL_ISO	R/W	0h	SW control for power signal ISO for MSS_L2_BANKA Reset Source: mod_g_rst_n

2.6.235 CFG0_L2OCRAM_BANK1_PD_CTRL Registers

2.6.235.1 CFG0_BANK1_PD_CTRL Register (Offset = 704h) [reset = 770h]

Short Description:

Long Description:

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Table 2-2101. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8704h

Figure 2-1046. L2OCRAM_BANK1_PD_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
422af318															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					MSS_L2_BANKB_PD_CTRL_AGOODIN			RESERVED	MSS_L2_BANKB_PD_CTRL_AONIN			RESERVED	MSS_L2_BANKB_PD_CTRL_ISO		
NONE					R/W			NONE	R/W			NONE	R/W		
422af318					7h			0	7h			0	0h		

Access Types Legend

Table 2-2102. L2OCRAM_BANK1_PD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE		Reserved
10:8	MSS_L2_BANKB_PD_CTRL_AGOODIN	R/W	7h	SW control for power signal AGOODIN for MSS_L2_BANKB Reset Source: mod_g_rst_n
7	RESERVED	NONE		Reserved
6:4	MSS_L2_BANKB_PD_CTRL_AONIN	R/W	7h	SW control for power signal AONIN for MSS_L2_BANKB Reset Source: mod_g_rst_n
3	RESERVED	NONE		Reserved
2:0	MSS_L2_BANKB_PD_CTRL_ISO	R/W	0h	SW control for power signal ISO for MSS_L2_BANKB Reset Source: mod_g_rst_n

2.6.236 CFG0_L2OCRAM_BANK2_PD_CTRL Registers

2.6.236.1 CFG0_BANK2_PD_CTRL Register (Offset = 708h) [reset = 770h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2103. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8708h

Figure 2-1047. L2OCRAM_BANK2_PD_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
422af318															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					MSS_L2_BANKC_PD_CTRL_AGOODIN			RESERVED	MSS_L2_BANKC_PD_CTRL_AONIN			RESERVED	MSS_L2_BANKC_PD_CTRL_ISO		
NONE					R/W			NONE	R/W			NONE	R/W		
422af318					7h			0	7h			0	0h		

Access Types Legend

Table 2-2104. L2OCRAM_BANK2_PD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE		Reserved
10:8	MSS_L2_BANKC_PD_CTRL_AGOODIN	R/W	7h	SW control for power signal AGOODIN for MSS_L2_BANKC Reset Source: mod_g_rst_n
7	RESERVED	NONE		Reserved
6:4	MSS_L2_BANKC_PD_CTRL_AONIN	R/W	7h	SW control for power signal AONIN for MSS_L2_BANKC Reset Source: mod_g_rst_n
3	RESERVED	NONE		Reserved
2:0	MSS_L2_BANKC_PD_CTRL_ISO	R/W	0h	SW control for power signal ISO for MSS_L2_BANKC Reset Source: mod_g_rst_n

2.6.237 CFG0_L2OCRAM_BANK3_PD_CTRL Registers

2.6.237.1 CFG0_BANK3_PD_CTRL Register (Offset = 70Ch) [reset = 770h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2105. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 870Ch

Figure 2-1048. L2OCRAM_BANK3_PD_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
422af318															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					MSS_L2_BANKD_PD_CTRL_AGOODIN			RESERVED	MSS_L2_BANKD_PD_CTRL_AONIN			RESERVED	MSS_L2_BANKD_PD_CTRL_ISO		
NONE					R/W			NONE	R/W			NONE	R/W		
422af318					7h			0	7h			0	0h		

Access Types Legend

Table 2-2106. L2OCRAM_BANK3_PD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE		Reserved
10:8	MSS_L2_BANKD_PD_CTRL_AGOODIN	R/W	7h	SW control for power signal AGOODIN for MSS_L2_BANKD Reset Source: mod_g_rst_n
7	RESERVED	NONE		Reserved
6:4	MSS_L2_BANKD_PD_CTRL_AONIN	R/W	7h	SW control for power signal AONIN for MSS_L2_BANKD Reset Source: mod_g_rst_n
3	RESERVED	NONE		Reserved
2:0	MSS_L2_BANKD_PD_CTRL_ISO	R/W	0h	SW control for power signal ISO for MSS_L2_BANKD Reset Source: mod_g_rst_n

2.6.238 CFG0_L2OCRAM_BANK0_PD_STATUS Registers

2.6.238.1 CFG0_BANK0_PD_STATUS Register (Offset = 710h) [reset = 3h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2107. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8710h

Figure 2-1049. L2OCRAM_BANK0_PD_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
1															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														MSS_L2_BANKA_PD_STATUS_AGOODOUT	MSS_L2_BANKA_PD_STATUS_AONOUT
NONE														R	R
1														1h	1h

Access Types Legend

Table 2-2108. L2OCRAM_BANK0_PD_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1	MSS_L2_BANKA_PD_STATUS_AGOODOUT	R	1h	SW status indicating the pgoodin of MSS_L2_BANKA Reset Source: mod_g_rst_n
0	MSS_L2_BANKA_PD_STATUS_AONOUT	R	1h	SW status indicating the ponin of MSS_L2_BANKA Reset Source: mod_g_rst_n

2.6.239 CFG0_L2OCRAM_BANK1_PD_STATUS Registers

2.6.239.1 CFG0_BANK1_PD_STATUS Register (Offset = 714h) [reset = 3h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2109. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8714h

Figure 2-1050. L2OCRAM_BANK1_PD_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
1															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														MSS_L2_BANKB_PD_STATUS_AGOODOUT	MSS_L2_BANKB_PD_STATUS_AONOUT
NONE														R	R
1														1h	1h

Access Types Legend

Table 2-2110. L2OCRAM_BANK1_PD_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1	MSS_L2_BANKB_PD_STATUS_AGOODOUT	R	1h	SW status indicating the pgoodin of MSS_L2_BANKB Reset Source: mod_g_rst_n
0	MSS_L2_BANKB_PD_STATUS_AONOUT	R	1h	SW status indicating the ponin of MSS_L2_BANKB Reset Source: mod_g_rst_n

2.6.240 CFG0_L2OCRAM_BANK2_PD_STATUS Registers

2.6.240.1 CFG0_BANK2_PD_STATUS Register (Offset = 718h) [reset = 3h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2111. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8718h

Figure 2-1051. L2OCRAM_BANK2_PD_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
1															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														MSS_L2_BANKC_PD_STATUS_AGOODOUT	MSS_L2_BANKC_PD_STATUS_AONOUT
NONE														R	R
1														1h	1h

Access Types Legend

Table 2-2112. L2OCRAM_BANK2_PD_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1	MSS_L2_BANKC_PD_STATUS_AGOODOUT	R	1h	SW status indicating the pgoodin of MSS_L2_BANKC Reset Source: mod_g_rst_n
0	MSS_L2_BANKC_PD_STATUS_AONOUT	R	1h	SW status indicating the ponin of MSS_L2_BANKC Reset Source: mod_g_rst_n

2.6.241 CFG0_L2OCRAM_BANK3_PD_STATUS Registers

2.6.241.1 CFG0_BANK3_PD_STATUS Register (Offset = 71Ch) [reset = 3h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2113. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 871Ch

Figure 2-1052. L2OCRAM_BANK3_PD_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
1															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														MSS_L2_BANKD_PD_STATUS_AGOODOUT	MSS_L2_BANKD_PD_STATUS_AONOUT
NONE														R	R
1														1h	1h

Access Types Legend

Table 2-2114. L2OCRAM_BANK3_PD_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1	MSS_L2_BANKD_PD_STATUS_AGOODOUT	R	1h	SW status indicating the pgoodin of MSS_L2_BANKD Reset Source: mod_g_rst_n
0	MSS_L2_BANKD_PD_STATUS_AONOUT	R	1h	SW status indicating the ponin of MSS_L2_BANKD Reset Source: mod_g_rst_n

2.6.242 CFG0_HW_REG0 Registers

2.6.242.1 CFG0_REG0 Register (Offset = 720h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2115. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8720h

Figure 2-1053. HW_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_REG0_HWREG															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_REG0_HWREG															
R/W															
0h															

Access Types Legend

Table 2-2116. HW_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HW_REG0_HWREG	R/W	0h	HW Reserved regiser Reset Source: mod_g_rst_n

2.6.243 CFG0_HW_REG1 Registers

2.6.243.1 CFG0_REG1 Register (Offset = 724h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2117. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8724h

Figure 2-1054. HW_REG1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_REG1_HWREG															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_REG1_HWREG															
R/W															
0h															

Access Types Legend

Table 2-2118. HW_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HW_REG1_HWREG	R/W	0h	HW Reserved regiser Reset Source: mod_g_rst_n

2.6.244 CFG0_HW_REG2 Registers

2.6.244.1 CFG0_REG2 Register (Offset = 728h) [reset = 0h]

Short Description:

Long Description:

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Table 2-2119. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8728h

Figure 2-1055. HW_REG2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_REG2_HWREG															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_REG2_HWREG															
R/W															
0h															

Access Types Legend

Table 2-2120. HW_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HW_REG2_HWREG	R/W	0h	HW Reserved regiser Reset Source: mod_g_rst_n

2.6.245 CFG0_HW_REG3 Registers

2.6.245.1 CFG0_REG3 Register (Offset = 72Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2121. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 872Ch

Figure 2-1056. HW_REG3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_REG3_HWREG															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_REG3_HWREG															
R/W															
0h															

Access Types Legend

Table 2-2122. HW_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HW_REG3_HWREG	R/W	0h	HW Reserved regiser Reset Source: mod_g_rst_n

2.6.246 CFG0_HSM_RTIA_CLK_SRC_SEL Registers

2.6.246.1 CFG0_RTIA_CLK_SRC_SEL Register (Offset = 800h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2123. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8800h

Figure 2-1057. HSM_RTIA_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				HSM_RTIA_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-2124. HSM_RTIA_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	HSM_RTIA_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for HSM_Corresponding RTI.Data should be loaded as multibit. For example: if 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.6.247 CFG0_HSM_WDT_CLK_SRC_SEL Registers

2.6.247.1 CFG0_WDT_CLK_SRC_SEL Register (Offset = 804h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2125. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8804h

Figure 2-1058. HSM_WDT_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				HSM_WDT_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-2126. HSM_WDT_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	HSM_WDT_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for HSM_WDT.Data should be loaded as multibit. For example: if 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.6.248 CFG0_HSM_RTC_CLK_SRC_SEL Registers

2.6.248.1 CFG0_RTC_CLK_SRC_SEL Register (Offset = 808h) [reset = 777h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2127. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8808h

Figure 2-1059. HSM_RTC_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
422af323															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				HSM_RTC_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
422af323				777h											

Access Types Legend

Table 2-2128. HSM_RTC_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	HSM_RTC_CLK_SRC_SEL_CLKSRCSEL	R/W	777h	Select line for selecting source clock for HSM_RTC.Data should be loaded as multibit. For example: if 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.6.249 CFG0_HSM_DMTA_CLK_SRC_SEL Registers

2.6.249.1 CFG0_DMTA_CLK_SRC_SEL Register (Offset = 80Ch) [reset = 0h]

Short Description:

Long Description:

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Table 2-2129. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 880Ch

Figure 2-1060. HSM_DMTA_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				HSM_DMTA_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-2130. HSM_DMTA_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	HSM_DMTA_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for HSM_DMTA.Data should be loaded as multibit. For example: if 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.6.250 CFG0_HSM_DMTB_CLK_SRC_SEL Registers

2.6.250.1 CFG0_DMTB_CLK_SRC_SEL Register (Offset = 810h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2131. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8810h

Figure 2-1061. HSM_DMTB_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				HSM_DMTB_CLK_SRC_SEL_CLKSRCSEL											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-2132. HSM_DMTB_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	HSM_DMTB_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for HSM_DMTB.Data should be loaded as multibit. For example: if 0x5 should be selected then 0x555 should be configured to the register. Reset Source: mod_g_rst_n

2.6.251 CFG0_HSM_RTI_CLK_DIV_VAL Registers

2.6.251.1 CFG0_RTI_CLK_DIV_VAL Register (Offset = 814h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2133. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8814h

Figure 2-1062. HSM_RTI_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				HSM_RTI_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-2134. HSM_RTI_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	HSM_RTI_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value HSM RTI selected clock.Data should be loaded as multibit. For example: if divider value of 0x8 should be selected then 0x888 should be configured to the register. Reset Source: mod_g_rst_n

2.6.252 CFG0_HSM_WDT_CLK_DIV_VAL Registers

2.6.252.1 CFG0_WDT_CLK_DIV_VAL Register (Offset = 818h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2135. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8818h

Figure 2-1063. HSM_WDT_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				HSM_WDT_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-2136. HSM_WDT_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	HSM_WDT_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value HSM WDT selected clock.Data should be loaded as multibit. For example: if divider value of 0x8 should be selected then 0x888 should be configured to the register. Reset Source: mod_g_rst_n

2.6.253 CFG0_HSM_RTC_CLK_DIV_VAL Registers

2.6.253.1 CFG0_RTC_CLK_DIV_VAL Register (Offset = 81Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2137. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 881Ch

Figure 2-1064. HSM_RTC_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				HSM_RTC_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-2138. HSM_RTC_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	HSM_RTC_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value HSM RTC selected clock.Data should be loaded as multibit. For example: if divider value of 0x8 should be selected then 0x888 should be configured to the register. Reset Source: mod_g_rst_n

2.6.254 CFG0_HSM_DMTA_CLK_DIV_VAL Registers

2.6.254.1 CFG0_DMTA_CLK_DIV_VAL Register (Offset = 820h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2139. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8820h

Figure 2-1065. HSM_DMTA_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				HSM_DMTA_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-2140. HSM_DMTA_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	HSM_DMTA_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value HSM DMTA selected clock.Data should be loaded as multibit. For example: if divider value of 0x8 should be selected then 0x888 should be configured to the register. Reset Source: mod_g_rst_n

2.6.255 CFG0_HSM_DMTB_CLK_DIV_VAL Registers

2.6.255.1 CFG0_DMTB_CLK_DIV_VAL Register (Offset = 824h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2141. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8824h

Figure 2-1066. HSM_DMTB_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				HSM_DMTB_CLK_DIV_VAL_CLKDIVR											
NONE				R/W											
0				0h											

Access Types Legend

Table 2-2142. HSM_DMTB_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	HSM_DMTB_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value HSM DMTB selected clock.Data should be loaded as multibit. For example: if divider value of 0x8 should be selected then 0x888 should be configured to the register. Reset Source: mod_g_rst_n

2.6.256 CFG0_HSM_RTI_CLK_GATE Registers

2.6.256.1 CFG0_RTI_CLK_GATE Register (Offset = 828h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2143. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8828h

Figure 2-1067. HSM_RTI_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													HSM_RTI_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2144. HSM_RTI_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	HSM_RTI_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for HSM RTI Reset Source: mod_g_rst_n

2.6.257 CFG0_HSM_WDT_CLK_GATE Registers

2.6.257.1 CFG0_WDT_CLK_GATE Register (Offset = 82Ch) [reset = 0h]

Short Description:

Long Description:

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Table 2-2145. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 882Ch

Figure 2-1068. HSM_WDT_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													HSM_WDT_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2146. HSM_WDT_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	HSM_WDT_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for HSM WDT Reset Source: mod_g_rst_n

2.6.258 CFG0_HSM_RTC_CLK_GATE Registers

2.6.258.1 CFG0_RTC_CLK_GATE Register (Offset = 830h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2147. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8830h

Figure 2-1069. HSM_RTC_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													HSM_RTC_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2148. HSM_RTC_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	HSM_RTC_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for HSM RTC Reset Source: mod_g_rst_n

2.6.259 CFG0_HSM_DMTA_CLK_GATE Registers

2.6.259.1 CFG0_DMTA_CLK_GATE Register (Offset = 834h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2149. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8834h

Figure 2-1070. HSM_DMTA_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													HSM_DMTA_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2150. HSM_DMTA_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	HSM_DMTA_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for HSM DMTA Reset Source: mod_g_rst_n

2.6.260 CFG0_HSM_DMTB_CLK_GATE Registers

2.6.260.1 CFG0_DMTB_CLK_GATE Register (Offset = 838h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2151. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8838h

Figure 2-1071. HSM_DMTB_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													HSM_DMTB_CLK_GATE_GATED		
NONE													R/W		
0													0h		

Access Types Legend

Table 2-2152. HSM_DMTB_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	HSM_DMTB_CLK_GATE_GATED	R/W	0h	writing 111 will gate clock for HSM DMTB Reset Source: mod_g_rst_n

2.6.261 CFG0_HSM_RTI_CLK_STATUS Registers

2.6.261.1 CFG0_RTI_CLK_STATUS Register (Offset = 83Ch) [reset = 1h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2153. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 883Ch

Figure 2-1072. HSM_RTI_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSM_RTI_CLK_STATUS_CURRDIVIDER								HSM_RTI_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-2154. HSM_RTI_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	HSM_RTI_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for HSM_RTI Reset Source: mod_g_rst_n
7:0	HSM_RTI_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for HSM_RTI Reset Source: mod_g_rst_n

2.6.262 CFG0_HSM_WDT_CLK_STATUS Registers

2.6.262.1 CFG0_WDT_CLK_STATUS Register (Offset = 840h) [reset = 1h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2155. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8840h

Figure 2-1073. HSM_WDT_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSM_WDT_CLK_STATUS_CURRDIVIDER								HSM_WDT_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-2156. HSM_WDT_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	HSM_WDT_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for HSM_WDT Reset Source: mod_g_rst_n
7:0	HSM_WDT_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for HSM_WDT Reset Source: mod_g_rst_n

2.6.263 CFG0_HSM_RTC_CLK_STATUS Registers

2.6.263.1 CFG0_RTC_CLK_STATUS Register (Offset = 844h) [reset = 80h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2157. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8844h

Figure 2-1074. HSM_RTC_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
f4240															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSM_RTC_CLK_STATUS_CURRDIVIDER								HSM_RTC_CLK_STATUS_CLKINUSE							
R								R							
0h								80h							

Access Types Legend

Table 2-2158. HSM_RTC_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	HSM_RTC_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for HSM_RTC Reset Source: mod_g_rst_n
7:0	HSM_RTC_CLK_STATUS_CLKINUSE	R	80h	Status shows the source clock slected for HSM_RTC Reset Source: mod_g_rst_n

2.6.264 CFG0_HSM_DMTA_CLK_STATUS Registers

2.6.264.1 CFG0_DMTA_CLK_STATUS Register (Offset = 848h) [reset = 1h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2159. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8848h

Figure 2-1075. HSM_DMTA_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSM_DMTA_CLK_STATUS_CURRDIVIDER								HSM_DMTA_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-2160. HSM_DMTA_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	HSM_DMTA_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for HSM_DMTA Reset Source: mod_g_rst_n
7:0	HSM_DMTA_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for HSM_DMTA Reset Source: mod_g_rst_n

2.6.265 CFG0_HSM_DMTB_CLK_STATUS Registers

2.6.265.1 CFG0_DMTB_CLK_STATUS Register (Offset = 84Ch) [reset = 1h]

Short Description:

Long Description:

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Table 2-2161. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 884Ch

Figure 2-1076. HSM_DMTB_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSM_DMTB_CLK_STATUS_CURRDIVIDER								HSM_DMTB_CLK_STATUS_CLKINUSE							
R								R							
0h								1h							

Access Types Legend

Table 2-2162. HSM_DMTB_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	HSM_DMTB_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for HSM_DMTB Reset Source: mod_g_rst_n
7:0	HSM_DMTB_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for HSM_DMTB Reset Source: mod_g_rst_n

2.6.266 CFG0_HW_SPARE_RW0 Registers

2.6.266.1 CFG0_SPARE_RW0 Register (Offset = FD0h) [reset = 0h]

Short Description:

Long Description:

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Table 2-2163. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8FD0h

Figure 2-1077. HW_SPARE_RW0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RW0_HW_SPARE_RW0															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RW0_HW_SPARE_RW0															
R/W															
0h															

Access Types Legend

Table 2-2164. HW_SPARE_RW0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HW_SPARE_RW0_HW_SPARE_RW0	R/W	0h	Reserved for HW RandD Reset Source: mod_g_rst_n

2.6.267 CFG0_HW_SPARE_RW1 Registers

2.6.267.1 CFG0_SPARE_RW1 Register (Offset = FD4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2165. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8FD4h

Figure 2-1078. HW_SPARE_RW1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RW1_HW_SPARE_RW1															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RW1_HW_SPARE_RW1															
R/W															
0h															

Access Types Legend

Table 2-2166. HW_SPARE_RW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HW_SPARE_RW1_HW_SPARE_RW1	R/W	0h	Reserved for HW RandD Reset Source: mod_g_rst_n

2.6.268 CFG0_HW_SPARE_RW2 Registers

2.6.268.1 CFG0_SPARE_RW2 Register (Offset = FD8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2167. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8FD8h

Figure 2-1079. HW_SPARE_RW2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RW2_HW_SPARE_RW2															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RW2_HW_SPARE_RW2															
R/W															
0h															

Access Types Legend

Table 2-2168. HW_SPARE_RW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HW_SPARE_RW2_HW_SPARE_RW2	R/W	0h	Reserved for HW RandD Reset Source: mod_g_rst_n

2.6.269 CFG0_HW_SPARE_RW3 Registers

2.6.269.1 CFG0_SPARE_RW3 Register (Offset = FDCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2169. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8FDCh

Figure 2-1080. HW_SPARE_RW3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RW3_HW_SPARE_RW3															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RW3_HW_SPARE_RW3															
R/W															
0h															

Access Types Legend

Table 2-2170. HW_SPARE_RW3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HW_SPARE_RW3_HW_SPARE_RW3	R/W	0h	Reserved for HW RandD Reset Source: mod_g_rst_n

2.6.270 CFG0_HW_SPARE_RO0 Registers

2.6.270.1 CFG0_SPARE_RO0 Register (Offset = FE0h) [reset = 0h]

Short Description:

Long Description:

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Table 2-2171. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8FE0h

Figure 2-1081. HW_SPARE_RO0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RO0_HW_SPARE_RO0															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RO0_HW_SPARE_RO0															
R															
0h															

Access Types Legend

Table 2-2172. HW_SPARE_RO0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HW_SPARE_RO0_HW_SPARE_RO0	R	0h	Reserved for HW RandD Reset Source: mod_g_rst_n

2.6.271 CFG0_HW_SPARE_RO1 Registers

2.6.271.1 CFG0_SPARE_RO1 Register (Offset = FE4h) [reset = 0h]

Short Description:

Long Description:

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Table 2-2173. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8FE4h

Figure 2-1082. HW_SPARE_RO1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RO1_HW_SPARE_RO1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RO1_HW_SPARE_RO1															
R															
0h															

Access Types Legend

Table 2-2174. HW_SPARE_RO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HW_SPARE_RO1_HW_SPARE_RO1	R	0h	Reserved for HW RandD Reset Source: mod_g_rst_n

2.6.272 CFG0_HW_SPARE_RO2 Registers

2.6.272.1 CFG0_SPARE_RO2 Register (Offset = FE8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2175. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8FE8h

Figure 2-1083. HW_SPARE_RO2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RO2_HW_SPARE_RO2															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RO2_HW_SPARE_RO2															
R															
0h															

Access Types Legend

Table 2-2176. HW_SPARE_RO2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HW_SPARE_RO2_HW_SPARE_RO2	R	0h	Reserved for HW RandD Reset Source: mod_g_rst_n

2.6.273 CFG0_HW_SPARE_RO3 Registers

2.6.273.1 CFG0_SPARE_RO3 Register (Offset = FECh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 2-2177. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8FECh

Figure 2-1084. HW_SPARE_RO3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RO3_HW_SPARE_RO3															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RO3_HW_SPARE_RO3															
R															
0h															

Access Types Legend

Table 2-2178. HW_SPARE_RO3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HW_SPARE_RO3_HW_SPARE_RO3	R	0h	Reserved for HW RandD Reset Source: mod_g_rst_n

2.6.274 CFG0_HW_SPARE_WPH Registers

2.6.274.1 CFG0_SPARE_WPH Register (Offset = FF0h) [reset = 0h]

Short Description:

Long Description:

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Table 2-2179. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8FF0h

Figure 2-1085. HW_SPARE_WPH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_WPH_HW_SPARE_WPH															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_WPH_HW_SPARE_WPH															
R/W															
0h															

Access Types Legend

Table 2-2180. HW_SPARE_WPH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HW_SPARE_WPH_HW_SPARE_WPH	R/W	0h	Reserved for HW RandD Reset Source: mod_g_rst_n

2.6.275 CFG0_HW_SPARE_REC Registers

2.6.275.1 CFG0_SPARE_REC Register (Offset = FF4h) [reset = 0h]

Short Description:

Long Description:

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Table 2-2181. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 8FF4h

Figure 2-1086. HW_SPARE_REC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_REC_HW_SPARE_REC31	HW_SPARE_REC_HW_SPARE_REC30	HW_SPARE_REC_HW_SPARE_REC29	HW_SPARE_REC_HW_SPARE_REC28	HW_SPARE_REC_HW_SPARE_REC27	HW_SPARE_REC_HW_SPARE_REC26	HW_SPARE_REC_HW_SPARE_REC25	HW_SPARE_REC_HW_SPARE_REC24	HW_SPARE_REC_HW_SPARE_REC23	HW_SPARE_REC_HW_SPARE_REC22	HW_SPARE_REC_HW_SPARE_REC21	HW_SPARE_REC_HW_SPARE_REC20	HW_SPARE_REC_HW_SPARE_REC19	HW_SPARE_REC_HW_SPARE_REC18	HW_SPARE_REC_HW_SPARE_REC17	HW_SPARE_REC_HW_SPARE_REC16
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_REC_HW_SPARE_REC15	HW_SPARE_REC_HW_SPARE_REC14	HW_SPARE_REC_HW_SPARE_REC13	HW_SPARE_REC_HW_SPARE_REC12	HW_SPARE_REC_HW_SPARE_REC11	HW_SPARE_REC_HW_SPARE_REC10	HW_SPARE_REC_HW_SPARE_REC9	HW_SPARE_REC_HW_SPARE_REC8	HW_SPARE_REC_HW_SPARE_REC7	HW_SPARE_REC_HW_SPARE_REC6	HW_SPARE_REC_HW_SPARE_REC5	HW_SPARE_REC_HW_SPARE_REC4	HW_SPARE_REC_HW_SPARE_REC3	HW_SPARE_REC_HW_SPARE_REC2	HW_SPARE_REC_HW_SPARE_REC1	HW_SPARE_REC_HW_SPARE_REC0
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 2-2182. HW_SPARE_REC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HW_SPARE_REC_HW_SPARE_REC31	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
30	HW_SPARE_REC_HW_SPARE_REC30	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
29	HW_SPARE_REC_HW_SPARE_REC29	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
28	HW_SPARE_REC_HW_SPARE_REC28	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
27	HW_SPARE_REC_HW_SPARE_REC27	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
26	HW_SPARE_REC_HW_SPARE_REC26	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
25	HW_SPARE_REC_HW_SPARE_REC25	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
24	HW_SPARE_REC_HW_SPARE_REC24	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
23	HW_SPARE_REC_HW_SPARE_REC23	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n

Table 2-2182. HW_SPARE_REC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	HW_SPARE_REC_HW_SPARE_REC22	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
21	HW_SPARE_REC_HW_SPARE_REC21	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
20	HW_SPARE_REC_HW_SPARE_REC20	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
19	HW_SPARE_REC_HW_SPARE_REC19	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
18	HW_SPARE_REC_HW_SPARE_REC18	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
17	HW_SPARE_REC_HW_SPARE_REC17	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
16	HW_SPARE_REC_HW_SPARE_REC16	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
15	HW_SPARE_REC_HW_SPARE_REC15	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
14	HW_SPARE_REC_HW_SPARE_REC14	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
13	HW_SPARE_REC_HW_SPARE_REC13	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
12	HW_SPARE_REC_HW_SPARE_REC12	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
11	HW_SPARE_REC_HW_SPARE_REC11	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
10	HW_SPARE_REC_HW_SPARE_REC10	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
9	HW_SPARE_REC_HW_SPARE_REC9	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
8	HW_SPARE_REC_HW_SPARE_REC8	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
7	HW_SPARE_REC_HW_SPARE_REC7	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
6	HW_SPARE_REC_HW_SPARE_REC6	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
5	HW_SPARE_REC_HW_SPARE_REC5	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
4	HW_SPARE_REC_HW_SPARE_REC4	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
3	HW_SPARE_REC_HW_SPARE_REC3	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
2	HW_SPARE_REC_HW_SPARE_REC2	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
1	HW_SPARE_REC_HW_SPARE_REC1	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n
0	HW_SPARE_REC_HW_SPARE_REC0	R/W1TC	0h	Reserved for HW RandD Reset Source: mod_g_rst_n

2.6.276 CFG0_LOCK0_KICK0 Registers

2.6.276.1 CFG0_KICK0 Register (Offset = 1008h) [reset = 0h]

Short Description: - KICK0 component

Long Description: - KICK0 component

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Table 2-2183. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 9008h

Figure 2-1087. LOCK0_KICK0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LOCK0_KICK0															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCK0_KICK0															
R/W															
0h															

Access Types Legend

Table 2-2184. LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0	R/W	0h	- KICK0 component Reset Source: mod_g_rst_n

2.6.277 CFG0_LOCK0_KICK1 Registers

2.6.277.1 CFG0_KICK1 Register (Offset = 100Ch) [reset = 0h]

Short Description: - KICK1 component

Long Description: - KICK1 component

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Table 2-2185. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 900Ch

Figure 2-1088. LOCK0_KICK1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LOCK0_KICK1															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCK0_KICK1															
R/W															
0h															

Access Types Legend

Table 2-2186. LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1	R/W	0h	- KICK1 component Reset Source: mod_g_rst_n

2.6.278 CFG0_INTR_RAW_STATUS Registers

2.6.278.1 CFG0_RAW_STATUS Register (Offset = 1010h) [reset = 0h]

Short Description: Interrupt Raw Status/Set Register

Long Description: Interrupt Raw Status/Set Register

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Table 2-2187. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 9010h

Figure 2-1089. INTR_RAW_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												PROXY_ERR	KICK_ERR	ADDR_ERR	PROT_ERR
NONE												R/W1TS	R/W1TS	R/W1TS	R/W1TS
0												0h	0h	0h	0h

Access Types Legend

Table 2-2188. INTR_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	PROXY_ERR	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

2.6.279 CFG0_INTR_ENABLED_STATUS_CLEAR Registers

2.6.279.1 CFG0_ENABLED_STATUS_CLEAR Register (Offset = 1014h) [reset = 0h]

Short Description: Interrupt Enabled Status/Clear register

Long Description: Interrupt Enabled Status/Clear register

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Table 2-2189. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 9014h

Figure 2-1090. INTR_ENABLED_STATUS_CLEAR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												ENABLED_PROXY_ERR	ENABLED_KICK_ERR	ENABLED_ADDR_ERR	ENABLED_PROT_ERR
NONE												R/W1TC	R/W1TC	R/W1TC	R/W1TC
0												0h	0h	0h	0h

Access Types Legend

Table 2-2190. INTR_ENABLED_STATUS_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	ENABLED_PROXY_ERR	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	ENABLED_KICK_ERR	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ENABLED_ADDR_ERR	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	ENABLED_PROT_ERR	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: mod_g_rst_n

2.6.280 CFG0_INTR_ENABLE Registers

2.6.280.1 CFG0_ENABLE Register (Offset = 1018h) [reset = 0h]

Short Description: Interrupt Enable register

Long Description: Interrupt Enable register

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Table 2-2191. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 9018h

Figure 2-1091. INTR_ENABLE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												PROXY_ERR_EN	KICK_ERR_EN	ADDR_ERR_EN	PROT_ERR_EN
NONE												R/W1TS	R/W1TS	R/W1TS	R/W1TS
0												0h	0h	0h	0h

Access Types Legend

Table 2-2192. INTR_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	PROXY_ERR_EN	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

2.6.281 CFG0_INTR_ENABLE_CLEAR Registers

2.6.281.1 CFG0_ENABLE_CLEAR Register (Offset = 101Ch) [reset = 0h]

Short Description: Interrupt Enable Clear register

Long Description: Interrupt Enable Clear register

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Table 2-2193. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 901Ch

Figure 2-1092. INTR_ENABLE_CLEAR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												PROXY_ERR_EN_CLR	KICK_ERR_EN_CLR	ADDR_ERR_EN_CLR	PROT_ERR_EN_CLR
NONE												R/W1TC	R/W1TC	R/W1TC	R/W1TC
0												0h	0h	0h	0h

Access Types Legend

Table 2-2194. INTR_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	PROXY_ERR_EN_CLR	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
2	KICK_ERR_EN_CLR	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
1	ADDR_ERR_EN_CLR	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n
0	PROT_ERR_EN_CLR	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: mod_g_rst_n

2.6.282 CFG0_EOI Registers

2.6.282.1 CFG0_EOI Register (Offset = 1020h) [reset = 0h]

Short Description: EOI register

Long Description: EOI register

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Table 2-2195. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 9020h

Figure 2-1093. EOI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								EOI_VECTOR							
NONE								R/W							
0								0h							

Access Types Legend

Table 2-2196. EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	EOI_VECTOR	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip. Reset Source: mod_g_rst_n

2.6.283 CFG0_FAULT_ADDRESS Registers

2.6.283.1 CFG0_ADDRESS Register (Offset = 1024h) [reset = 0h]

Short Description: Fault Address register

Long Description: Fault Address register

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Table 2-2197. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 9024h

Figure 2-1094. FAULT_ADDRESS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FAULT_ADDR															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FAULT_ADDR															
R															
0h															

Access Types Legend

Table 2-2198. FAULT_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR	R	0h	Fault Address. Reset Source: mod_g_rst_n

2.6.284 CFG0_FAULT_TYPE_STATUS Registers

2.6.284.1 CFG0_TYPE_STATUS Register (Offset = 1028h) [reset = 0h]

Short Description: Fault Type Status register

Long Description: Fault Type Status register

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Table 2-2199. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 9028h

Figure 2-1095. FAULT_TYPE_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									FAULT_NS	FAULT_TYPE					
NONE									R	R					
0									0h	0h					

Access Types Legend

Table 2-2200. FAULT_TYPE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE		Reserved
6	FAULT_NS	R	0h	Non-secure access. Reset Source: mod_g_rst_n
5:0	FAULT_TYPE	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype ! = 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault Reset Source: mod_g_rst_n

2.6.285 CFG0_FAULT_ATTR_STATUS Registers

2.6.285.1 CFG0_ATTR_STATUS Register (Offset = 102Ch) [reset = 0h]

Short Description: Fault Attribute Status register

Long Description: Fault Attribute Status register

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Table 2-2201. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 902Ch

Figure 2-1096. FAULT_ATTR_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FAULT_XID												FAULT_ROUTEID			
R												R			
0h												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FAULT_ROUTEID								FAULT_PRIVID							
R								R							
0h								0h							

Access Types Legend

Table 2-2202. FAULT_ATTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID	R	0h	XID. Reset Source: mod_g_rst_n
19:8	FAULT_ROUTEID	R	0h	Route ID. Reset Source: mod_g_rst_n
7:0	FAULT_PRIVID	R	0h	Privilege ID. Reset Source: mod_g_rst_n

2.6.286 CFG0_FAULT_CLEAR Registers

2.6.286.1 CFG0_CLEAR Register (Offset = 1030h) [reset = 0h]

Short Description: Fault Clear register

Long Description: Fault Clear register

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Table 2-2203. Instance Table

Instance Name	Physical Address
MSS_RCM_MMR0	5320 9030h

Figure 2-1097. FAULT_CLEAR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															FAULT_CLR
NONE															W
0															0h

Access Types Legend

Table 2-2204. FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	FAULT_CLR	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. Reset Source: mod_g_rst_n

2.6.287 Access Table

Table 2-2205. Access Type Codes

Access Type	Code	Description
R	R	Read
R/W	R/W	Read / Write
R/W1TC	R/W1TC	Read/Write 1 To Clear
R/W1TS	R/W1TS	Read/Write 1 To Set
W	W	Write

3 Real-time Control Subsystem (CONTROLSS) Registers

The Real-time Control Subsystem (CONTROLSS) registers are described in the following sections.

Note

All images except ADC images uses hexadecimal. ADC uses binary due to legacy documentation.

3.1 CONTROLSS 16-bit Register Access Note

Note

8-bit wide register access is **not allowed** for ADC, EPWM, DAC, CMPSS, EQEP, SDFM, and FSI MMR regions. 16-bit access must be used instead.

3.2 ADC_CFG Registers

Table 3-1. CONTROLSS_ADC[0:2]_CFG Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_ADC0_CFG Physical Address	CONTROLSS_ADC1_CFG Physical Address	CONTROLSS_ADC2_CFG Physical Address
0h	16	ADC_CFG_ADCCTL1	502C 0000h	502C 1000h	502C 2000h
2h	16	ADC_CFG_ADCCTL2	502C 0002h	502C 1002h	502C 2002h
4h	16	ADC_CFG_ADCBURSTCTL	502C 0004h	502C 1004h	502C 2004h
6h	16	ADC_CFG_ADCINTFLG	502C 0006h	502C 1006h	502C 2006h
8h	16	ADC_CFG_ADCINTFLGCLR	502C 0008h	502C 1008h	502C 2008h
Ah	16	ADC_CFG_ADCINTOVF	502C 000Ah	502C 100Ah	502C 200Ah
Ch	16	ADC_CFG_ADCINTOVFCLR	502C 000Ch	502C 100Ch	502C 200Ch
Eh	16	ADC_CFG_ADCINTSEL1N2	502C 000Eh	502C 100Eh	502C 200Eh
10h	16	ADC_CFG_ADCINTSEL3N4	502C 0010h	502C 1010h	502C 2010h
12h	16	ADC_CFG_ADCSOCPRICTL	502C 0012h	502C 1012h	502C 2012h
14h	16	ADC_CFG_ADCINTSOCSEL1	502C 0014h	502C 1014h	502C 2014h
16h	16	ADC_CFG_ADCINTSOCSEL2	502C 0016h	502C 1016h	502C 2016h
18h	16	ADC_CFG_ADCSOCFLG1	502C 0018h	502C 1018h	502C 2018h
1Ah	16	ADC_CFG_ADCSOCFRC1	502C 001Ah	502C 101Ah	502C 201Ah
1Ch	16	ADC_CFG_ADCSOCOVF1	502C 001Ch	502C 101Ch	502C 201Ch
1Eh	16	ADC_CFG_ADCSOCOVFCLR1	502C 001Eh	502C 101Eh	502C 201Eh
20h	32	ADC_CFG_ADCSOC0CTL	502C 0020h	502C 1020h	502C 2020h
24h	32	ADC_CFG_ADCSOC1CTL	502C 0024h	502C 1024h	502C 2024h
28h	32	ADC_CFG_ADCSOC2CTL	502C 0028h	502C 1028h	502C 2028h
2Ch	32	ADC_CFG_ADCSOC3CTL	502C 002Ch	502C 102Ch	502C 202Ch
30h	32	ADC_CFG_ADCSOC4CTL	502C 0030h	502C 1030h	502C 2030h
34h	32	ADC_CFG_ADCSOC5CTL	502C 0034h	502C 1034h	502C 2034h
38h	32	ADC_CFG_ADCSOC6CTL	502C 0038h	502C 1038h	502C 2038h
3Ch	32	ADC_CFG_ADCSOC7CTL	502C 003Ch	502C 103Ch	502C 203Ch
40h	32	ADC_CFG_ADCSOC8CTL	502C 0040h	502C 1040h	502C 2040h
44h	32	ADC_CFG_ADCSOC9CTL	502C 0044h	502C 1044h	502C 2044h
48h	32	ADC_CFG_ADCSOC10CTL	502C 0048h	502C 1048h	502C 2048h
4Ch	32	ADC_CFG_ADCSOC11CTL	502C 004Ch	502C 104Ch	502C 204Ch
50h	32	ADC_CFG_ADCSOC12CTL	502C 0050h	502C 1050h	502C 2050h
54h	32	ADC_CFG_ADCSOC13CTL	502C 0054h	502C 1054h	502C 2054h
58h	32	ADC_CFG_ADCSOC14CTL	502C 0058h	502C 1058h	502C 2058h
5Ch	32	ADC_CFG_ADCSOC15CTL	502C 005Ch	502C 105Ch	502C 205Ch
60h	16	ADC_CFG_ADCEVTSTAT	502C 0060h	502C 1060h	502C 2060h
64h	16	ADC_CFG_ADCEVTCLR	502C 0064h	502C 1064h	502C 2064h
68h	16	ADC_CFG_ADCEVTSEL	502C 0068h	502C 1068h	502C 2068h
6Ch	16	ADC_CFG_ADCEVTINTSEL	502C 006Ch	502C 106Ch	502C 206Ch
70h	16	ADC_CFG_ADCOSDETECT	502C 0070h	502C 1070h	502C 2070h
72h	16	ADC_CFG_ADCCOUNTER	502C 0072h	502C 1072h	502C 2072h
74h	16	ADC_CFG_ADCREV	502C 0074h	502C 1074h	502C 2074h
76h	16	ADC_CFG_ADCOFFTRIM	502C 0076h	502C 1076h	502C 2076h
7Ch	32	ADC_CFG_ADCCONFIG	502C 007Ch	502C 107Ch	502C 207Ch
80h	16	ADC_CFG_ADCPPB1CONFIG	502C 0080h	502C 1080h	502C 2080h
82h	16	ADC_CFG_ADCPPB1STAMP	502C 0082h	502C 1082h	502C 2082h
84h	16	ADC_CFG_ADCPPB1OFFCAL	502C 0084h	502C 1084h	502C 2084h

Table 3-1. CONTROLSS_ADC[0:2]_CFG Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_ADC0_CFG Physical Address	CONTROLSS_ADC1_CFG Physical Address	CONTROLSS_ADC2_CFG Physical Address
86h	16	ADC_CFG_ADCPPB1OFFREF	502C 0086h	502C 1086h	502C 2086h
88h	32	ADC_CFG_ADCPPB1TRIPHI	502C 0088h	502C 1088h	502C 2088h
8Ch	32	ADC_CFG_ADCPPB1TRIPLO	502C 008Ch	502C 108Ch	502C 208Ch
90h	16	ADC_CFG_ADCPPB2CONFIG	502C 0090h	502C 1090h	502C 2090h
92h	16	ADC_CFG_ADCPPB2STAMP	502C 0092h	502C 1092h	502C 2092h
94h	16	ADC_CFG_ADCPPB2OFFCAL	502C 0094h	502C 1094h	502C 2094h
96h	16	ADC_CFG_ADCPPB2OFFREF	502C 0096h	502C 1096h	502C 2096h
98h	32	ADC_CFG_ADCPPB2TRIPHI	502C 0098h	502C 1098h	502C 2098h
9Ch	32	ADC_CFG_ADCPPB2TRIPLO	502C 009Ch	502C 109Ch	502C 209Ch
A0h	16	ADC_CFG_ADCPPB3CONFIG	502C 00A0h	502C 10A0h	502C 20A0h
A2h	16	ADC_CFG_ADCPPB3STAMP	502C 00A2h	502C 10A2h	502C 20A2h
A4h	16	ADC_CFG_ADCPPB3OFFCAL	502C 00A4h	502C 10A4h	502C 20A4h
A6h	16	ADC_CFG_ADCPPB3OFFREF	502C 00A6h	502C 10A6h	502C 20A6h
A8h	32	ADC_CFG_ADCPPB3TRIPHI	502C 00A8h	502C 10A8h	502C 20A8h
ACh	32	ADC_CFG_ADCPPB3TRIPLO	502C 00ACh	502C 10ACh	502C 20ACh
B0h	16	ADC_CFG_ADCPPB4CONFIG	502C 00B0h	502C 10B0h	502C 20B0h
B2h	16	ADC_CFG_ADCPPB4STAMP	502C 00B2h	502C 10B2h	502C 20B2h
B4h	16	ADC_CFG_ADCPPB4OFFCAL	502C 00B4h	502C 10B4h	502C 20B4h
B6h	16	ADC_CFG_ADCPPB4OFFREF	502C 00B6h	502C 10B6h	502C 20B6h
B8h	32	ADC_CFG_ADCPPB4TRIPHI	502C 00B8h	502C 10B8h	502C 20B8h
BCh	32	ADC_CFG_ADCPPB4TRIPLO	502C 00BCh	502C 10BCh	502C 20BCh
DEh	16	ADC_CFG_ADCINTCYCLE	502C 00DEh	502C 10DEh	502C 20DEh
E0h	32	ADC_CFG_ADCINLTRIM1	502C 00E0h	502C 10E0h	502C 20E0h
E4h	32	ADC_CFG_ADCINLTRIM2	502C 00E4h	502C 10E4h	502C 20E4h
E8h	32	ADC_CFG_ADCINLTRIM3	502C 00E8h	502C 10E8h	502C 20E8h
ECh	32	ADC_CFG_ADCINLTRIM4	502C 00ECh	502C 10ECh	502C 20ECh
F0h	32	ADC_CFG_ADCINLTRIM5	502C 00F0h	502C 10F0h	502C 20F0h
F4h	32	ADC_CFG_ADCINLTRIM6	502C 00F4h	502C 10F4h	502C 20F4h
FCh	32	ADC_CFG_ADCINLTRIMCTL	502C 00FCh	502C 10FCh	502C 20FCh

Table 3-2. CONTROLSS_ADC[3:4]_CFG Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_ADC3_CFG Physical Address	CONTROLSS_ADC4_CFG Physical Address
0h	16	ADC_CFG_ADCCTL1	502C 3000h	502C 4000h
2h	16	ADC_CFG_ADCCTL2	502C 3002h	502C 4002h
4h	16	ADC_CFG_ADCBURSTCTL	502C 3004h	502C 4004h
6h	16	ADC_CFG_ADCINTFLG	502C 3006h	502C 4006h
8h	16	ADC_CFG_ADCINTFLGCLR	502C 3008h	502C 4008h
Ah	16	ADC_CFG_ADCINTOVF	502C 300Ah	502C 400Ah
Ch	16	ADC_CFG_ADCINTOVFCLR	502C 300Ch	502C 400Ch
Eh	16	ADC_CFG_ADCINTSEL1N2	502C 300Eh	502C 400Eh
10h	16	ADC_CFG_ADCINTSEL3N4	502C 3010h	502C 4010h
12h	16	ADC_CFG_ADCSOCPRICTL	502C 3012h	502C 4012h
14h	16	ADC_CFG_ADCINTSOCSEL1	502C 3014h	502C 4014h
16h	16	ADC_CFG_ADCINTSOCSEL2	502C 3016h	502C 4016h
18h	16	ADC_CFG_ADCSOCFLG1	502C 3018h	502C 4018h

Table 3-2. CONTROLSS_ADC[3:4]_CFG Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_ADC3_CFG Physical Address	CONTROLSS_ADC4_CFG Physical Address
1Ah	16	ADC_CFG_ADCSOCFRC1	502C 301Ah	502C 401Ah
1Ch	16	ADC_CFG_ADCSOCOVF1	502C 301Ch	502C 401Ch
1Eh	16	ADC_CFG_ADCSOCOVFCLR1	502C 301Eh	502C 401Eh
20h	32	ADC_CFG_ADCSOC0CTL	502C 3020h	502C 4020h
24h	32	ADC_CFG_ADCSOC1CTL	502C 3024h	502C 4024h
28h	32	ADC_CFG_ADCSOC2CTL	502C 3028h	502C 4028h
2Ch	32	ADC_CFG_ADCSOC3CTL	502C 302Ch	502C 402Ch
30h	32	ADC_CFG_ADCSOC4CTL	502C 3030h	502C 4030h
34h	32	ADC_CFG_ADCSOC5CTL	502C 3034h	502C 4034h
38h	32	ADC_CFG_ADCSOC6CTL	502C 3038h	502C 4038h
3Ch	32	ADC_CFG_ADCSOC7CTL	502C 303Ch	502C 403Ch
40h	32	ADC_CFG_ADCSOC8CTL	502C 3040h	502C 4040h
44h	32	ADC_CFG_ADCSOC9CTL	502C 3044h	502C 4044h
48h	32	ADC_CFG_ADCSOC10CTL	502C 3048h	502C 4048h
4Ch	32	ADC_CFG_ADCSOC11CTL	502C 304Ch	502C 404Ch
50h	32	ADC_CFG_ADCSOC12CTL	502C 3050h	502C 4050h
54h	32	ADC_CFG_ADCSOC13CTL	502C 3054h	502C 4054h
58h	32	ADC_CFG_ADCSOC14CTL	502C 3058h	502C 4058h
5Ch	32	ADC_CFG_ADCSOC15CTL	502C 305Ch	502C 405Ch
60h	16	ADC_CFG_ADCEVTSTAT	502C 3060h	502C 4060h
64h	16	ADC_CFG_ADCEVTCLR	502C 3064h	502C 4064h
68h	16	ADC_CFG_ADCEVTSEL	502C 3068h	502C 4068h
6Ch	16	ADC_CFG_ADCEVTINTSEL	502C 306Ch	502C 406Ch
70h	16	ADC_CFG_ADCOSDETECT	502C 3070h	502C 4070h
72h	16	ADC_CFG_ADCCOUNTER	502C 3072h	502C 4072h
74h	16	ADC_CFG_ADCREV	502C 3074h	502C 4074h
76h	16	ADC_CFG_ADCOFFTRIM	502C 3076h	502C 4076h
7Ch	32	ADC_CFG_ADCCONFIG	502C 307Ch	502C 407Ch
80h	16	ADC_CFG_ADCPPB1CONFIG	502C 3080h	502C 4080h
82h	16	ADC_CFG_ADCPPB1STAMP	502C 3082h	502C 4082h
84h	16	ADC_CFG_ADCPPB1OFFCAL	502C 3084h	502C 4084h
86h	16	ADC_CFG_ADCPPB1OFFREF	502C 3086h	502C 4086h
88h	32	ADC_CFG_ADCPPB1TRIPHI	502C 3088h	502C 4088h
8Ch	32	ADC_CFG_ADCPPB1TRIPLO	502C 308Ch	502C 408Ch
90h	16	ADC_CFG_ADCPPB2CONFIG	502C 3090h	502C 4090h
92h	16	ADC_CFG_ADCPPB2STAMP	502C 3092h	502C 4092h
94h	16	ADC_CFG_ADCPPB2OFFCAL	502C 3094h	502C 4094h
96h	16	ADC_CFG_ADCPPB2OFFREF	502C 3096h	502C 4096h
98h	32	ADC_CFG_ADCPPB2TRIPHI	502C 3098h	502C 4098h
9Ch	32	ADC_CFG_ADCPPB2TRIPLO	502C 309Ch	502C 409Ch
A0h	16	ADC_CFG_ADCPPB3CONFIG	502C 30A0h	502C 40A0h
A2h	16	ADC_CFG_ADCPPB3STAMP	502C 30A2h	502C 40A2h
A4h	16	ADC_CFG_ADCPPB3OFFCAL	502C 30A4h	502C 40A4h
A6h	16	ADC_CFG_ADCPPB3OFFREF	502C 30A6h	502C 40A6h
A8h	32	ADC_CFG_ADCPPB3TRIPHI	502C 30A8h	502C 40A8h
ACh	32	ADC_CFG_ADCPPB3TRIPLO	502C 30ACh	502C 40ACh

Table 3-2. CONTROLSS_ADC[3:4]_CFG Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_ADC3_CFG Physical Address	CONTROLSS_ADC4_CFG Physical Address
B0h	16	ADC_CFG_ADCPPB4CONFIG	502C 30B0h	502C 40B0h
B2h	16	ADC_CFG_ADCPPB4STAMP	502C 30B2h	502C 40B2h
B4h	16	ADC_CFG_ADCPPB4OFFCAL	502C 30B4h	502C 40B4h
B6h	16	ADC_CFG_ADCPPB4OFFREF	502C 30B6h	502C 40B6h
B8h	32	ADC_CFG_ADCPPB4TRIPHI	502C 30B8h	502C 40B8h
BCh	32	ADC_CFG_ADCPPB4TRIPLO	502C 30BCh	502C 40BCh
DEh	16	ADC_CFG_ADCINTCYCLE	502C 30DEh	502C 40DEh
E0h	32	ADC_CFG_ADCINLTRIM1	502C 30E0h	502C 40E0h
E4h	32	ADC_CFG_ADCINLTRIM2	502C 30E4h	502C 40E4h
E8h	32	ADC_CFG_ADCINLTRIM3	502C 30E8h	502C 40E8h
ECh	32	ADC_CFG_ADCINLTRIM4	502C 30ECh	502C 40ECh
F0h	32	ADC_CFG_ADCINLTRIM5	502C 30F0h	502C 40F0h
F4h	32	ADC_CFG_ADCINLTRIM6	502C 30F4h	502C 40F4h
FCh	32	ADC_CFG_ADCINLTRIMCTL	502C 30FCh	502C 40FCh

3.2.1 ADC_CFG Instance Count Note

Note

n = 0 to 4 for the ADC_CFG registers defined below.

3.2.2 CONTROLSS_ADCn_CFG_ADCCTL1 Registers

3.2.2.1 ADCn_CFG_ADCCTL1 Register (Offset = 0h) [reset = h]

Short Description: ADC Control 1 Register

Long Description:

Return to Summary Table

Table 3-3. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0000h
CONTROLSS_ADC1_CFG	502C 1000h
CONTROLSS_ADC2_CFG	502C 2000h
CONTROLSS_ADC3_CFG	502C 3000h
CONTROLSS_ADC4_CFG	502C 4000h

Figure 3-1. ADCCTL1 Name Register

15	14	13	12	11	10	9	8
RESERVED		ADCBSY	RESERVED	ADCBSYCHN			
R		R	R	R			
0		0	0	0			
7	6	5	4	3	2	1	0
ADCPWDNZ	RESERVED				INTPULSEPOS	RESERVED	
R/W	R				R/W	R	
0	0				0	0	

Access Types Legend

Table 3-4. ADCCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	RESERVED	R		Reserved
13	ADCBSY	R	0h	ADC Busy. Set when ADC SOC is generated, cleared by hardware four ADC clocks after negative edge of S/H pulse. Used by the ADC state machine to determine if ADC is available to sample. 0 ADC is available to sample next channel 1 ADC is busy and cannot sample another channel
12	RESERVED	R		Reserved
11 - 8	ADCBSYCHN	R	0h	ADC Busy Channel. Set when an ADC Start of Conversion (SOC) is generated. When ADCBSY=0: holds the value of the last converted SOC When ADCBSY=1: reflects the SOC currently being processed 0h SOC0 is currently processing or was last SOC converted 1h SOC1 is currently processing or was last SOC converted 2h SOC2 is currently processing or was last SOC converted 3h SOC3 is currently processing or was last SOC converted 4h SOC4 is currently processing or was last SOC converted 5h SOC5 is currently processing or was last SOC converted 6h SOC6 is currently processing or was last SOC converted 7h SOC7 is currently processing or was last SOC converted 8h SOC8 is currently processing or was last SOC converted 9h SOC9 is currently processing or was last SOC converted Ah SOC10 is currently processing or was last SOC converted Bh SOC11 is currently processing or was last SOC converted Ch SOC12 is currently processing or was last SOC converted Dh SOC13 is currently processing or was last SOC converted Eh SOC14 is currently processing or was last SOC converted Fh SOC15 is currently processing or was last SOC converted

Table 3-4. ADCCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	ADCPWDNZ	R/W	0h	ADC Power Down (active low). This bit controls the power up and power down of all the analog circuitry inside the analog core. 0 All analog circuitry inside the core is powered down 1 All analog circuitry inside the core is powered up
6 - 3	RESERVED	R		Reserved
2	INTPULSEPOS	R/W	0h	ADC Interrupt Pulse Position. 0 Interrupt pulse generation occurs when ADC begins conversion (at the end of the acquisition window) plus a number of SYSCLK cycles as specified in the ADCINTCYCLE.OFFSET register. 1 Interrupt pulse generation occurs at the end of the conversion, 1 cycle prior to the ADC result latching into its result register
1 - 0	RESERVED	R		Reserved

3.2.3 CONTROLSS_ADCn_CFG_ADCCTL2 Registers

3.2.3.1 ADCn_CFG_ADCCTL2 Register (Offset = 2h) [reset = h]

Short Description: ADC Control 2 Register

Long Description:

Return to Summary Table

Table 3-5. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0002h
CONTROLSS_ADC1_CFG	502C 1002h
CONTROLSS_ADC2_CFG	502C 2002h
CONTROLSS_ADC3_CFG	502C 3002h
CONTROLSS_ADC4_CFG	502C 4002h

Figure 3-2. ADCCTL2 Name Register

15	14	13	12	11	10	9	8
RESERVED				RESERVED			
R				R			
0				0			
7	6	5	4	3	2	1	0
SIGNALMODE	RESOLUTION	RESERVED		PRESCALE			
R/W	R/W	R		R/W			
0	0	0		0			

Access Types Legend

Table 3-6. ADCCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	R		Reserved
12 - 8	RESERVED	R		Reserved
7	SIGNALMODE	R/W	0h	SOC Signaling Mode. Selects the input mode of the converter. Use the AdcSetMode function to change the signal mode. 0 Single-ended 1 Differential
6	RESOLUTION	R/W	0h	SOC Conversion Resolution. Selects the resolution of the converter. Use the AdcSetMode function to change the resolution. 0 12-bit resolution 1 16-bit resolution
5 - 4	RESERVED	R		Reserved
3 - 0	PRESCALE	R/W	0h	ADC Clock Prescaler. 0000 ADCCLK = Input Clock / 1.0 0001 Invalid 0010 ADCCLK = Input Clock / 2.0 0011 ADCCLK = Input Clock / 2.5 0100 ADCCLK = Input Clock / 3.0 0101 ADCCLK = Input Clock / 3.5 0110 ADCCLK = Input Clock / 4.0 0111 ADCCLK = Input Clock / 4.5 1000 ADCCLK = Input Clock / 5.0 1001 ADCCLK = Input Clock / 5.5 1010 ADCCLK = Input Clock / 6.0 1011 ADCCLK = Input Clock / 6.5 1100 ADCCLK = Input Clock / 7.0 1101 ADCCLK = Input Clock / 7.5 1110 ADCCLK = Input Clock / 8.0 1111 ADCCLK = Input Clock / 8.5

3.2.4 CONTROLSS_ADCn_CFG_ADCINTFLG Registers

3.2.4.1 ADCn_CFG_ADCINTFLG Register (Offset = 6h) [reset = h]

Short Description: ADC Interrupt Flag Register

Long Description:

Return to Summary Table

Table 3-7. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0006h
CONTROLSS_ADC1_CFG	502C 1006h
CONTROLSS_ADC2_CFG	502C 2006h
CONTROLSS_ADC3_CFG	502C 3006h
CONTROLSS_ADC4_CFG	502C 4006h

Figure 3-3. ADCINTFLG Name Register

15	14	13	12	11	10	9	8
RESERVED							
R							
0							
7	6	5	4	3	2	1	0
RESERVED				ADCINT4	ADCINT3	ADCINT2	ADCINT1
R				R	R	R	R
0				0	0	0	0

Access Types Legend

Table 3-8. ADCINTFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	RESERVED	R		Reserved
3	ADCINT4	R	0h	ADC Interrupt 4 Flag. Reading these flags indicates if the associated ADCINT pulse was generated since the last clear. 0 No ADC interrupt pulse generated 1 ADC interrupt pulse generated If the ADC interrupt is placed in continue to interrupt mode (INTSELxNy register) then further interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set. If the continuous mode is not enabled, then no further interrupt pulses are generated until the user clears this flag bit using the ADCINTFLGCLR register. Rather, an ADC interrupt overflow event occurs in the ADCINTOVF register.
2	ADCINT3	R	0h	ADC Interrupt 3 Flag. Reading these flags indicates if the associated ADCINT pulse was generated since the last clear. 0 No ADC interrupt pulse generated 1 ADC interrupt pulse generated If the ADC interrupt is placed in continue to interrupt mode (INTSELxNy register) then further interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set. If the continuous mode is not enabled, then no further interrupt pulses are generated until the user clears this flag bit using the ADCINTFLGCLR register. Rather, an ADC interrupt overflow event occurs in the ADCINTOVF register.

Table 3-8. ADCINTFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ADCINT2	R	0h	ADC Interrupt 2 Flag. Reading these flags indicates if the associated ADCINT pulse was generated since the last clear. 0 No ADC interrupt pulse generated 1 ADC interrupt pulse generated If the ADC interrupt is placed in continue to interrupt mode (INTSELxNy register) then further interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set. If the continuous mode is not enabled, then no further interrupt pulses are generated until the user clears this flag bit using the ADCINTFLGCLR register. Rather, an ADC interrupt overflow event occurs in the ADCINTOVF register.
0	ADCINT1	R	0h	ADC Interrupt 1 Flag. Reading these flags indicates if the associated ADCINT pulse was generated since the last clear. 0 No ADC interrupt pulse generated 1 ADC interrupt pulse generated If the ADC interrupt is placed in continue to interrupt mode (INTSELxNy register) then further interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set. If the continuous mode is not enabled, then no further interrupt pulses are generated until the user clears this flag bit using the ADCINTFLGCLR register. Rather, an ADC interrupt overflow event occurs in the ADCINTOVF register.

3.2.5 CONTROLSS_ADCn_CFG_ADCBURSTCTL Registers

3.2.5.1 ADCn_CFG_ADCBURSTCTL Register (Offset = 4h) [reset = h]

Short Description: ADC Burst Control Register

Long Description:

Return to Summary Table

Table 3-9. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0004h
CONTROLSS_ADC1_CFG	502C 1004h
CONTROLSS_ADC2_CFG	502C 2004h
CONTROLSS_ADC3_CFG	502C 3004h
CONTROLSS_ADC4_CFG	502C 4004h

Figure 3-4. ADCBURSTCTL Name Register

15	14	13	12	11	10	9	8
BURSTEN	RESERVED			BURSTSIZE			
R/W	R			R/W			
0	0			0			
7	6	5	4	3	2	1	0
RESERVED	BURSTTRIGSEL						
R	R/W						
0	0						

Access Types Legend

Table 3-10. ADCBURSTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	BURSTEN	R/W	0h	SOC Burst Mode Enable. This bit enables the SOC Burst Mode of operation. 0 Burst mode is disabled. 1 Burst mode is enabled.
14 - 12	RESERVED	R		Reserved
11 - 8	BURSTSIZE	R/W	0h	SOC Burst Size Select. This bit field determines how many SOCs are converted when a burst conversion sequence is started. The first SOC converted is defined by the round robin pointer, which is advanced as each SOC is converted. 0h 1 SOC converted 1h 2 SOCs converted 2h 3 SOCs converted 3h 4 SOCs converted 4h 5 SOCs converted 5h 6 SOCs converted 6h 7 SOCs converted 7h 8 SOCs converted 8h 9 SOCs converted 9h 10 SOCs converted Ah 11 SOCs converted Bh 12 SOCs converted Ch 13 SOCs converted Dh 14 SOCs converted Eh 15 SOCs converted Fh 16 SOCs converted
7	RESERVED	R		Reserved
6 - 0	BURSTTRIGSEL	R/W	0h	SOC Burst Trigger Source Select. Configures which trigger will start a burst conversion sequence. 00h - 7Fh: See AM602 spec. for trigger defintion

3.2.6 CONTROLSS_ADCn_CFG_ADCINTFLGCLR Registers

3.2.6.1 ADCn_CFG_ADCINTFLGCLR Register (Offset = 8h) [reset = h]

Short Description: ADC Interrupt Flag Clear Register

Long Description:

Return to Summary Table

Table 3-11. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0008h
CONTROLSS_ADC1_CFG	502C 1008h
CONTROLSS_ADC2_CFG	502C 2008h
CONTROLSS_ADC3_CFG	502C 3008h
CONTROLSS_ADC4_CFG	502C 4008h

Figure 3-5. ADCINTFLGCLR Name Register

15	14	13	12	11	10	9	8
RESERVED							
R							
0							
7	6	5	4	3	2	1	0
RESERVED				ADCINT4	ADCINT3	ADCINT2	ADCINT1
R				R-0/W	R-0/W	R-0/W	R-0/W
0				0	0	0	0

Access Types Legend

Table 3-12. ADCINTFLGCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	RESERVED	R		Reserved
3	ADCINT4	R-0/W	0h	ADC Interrupt 4 Flag Clear. Reads return 0. 0 No action 1 Clears ADCINT4 and ADCINT4RESULT flags in the ADCINTFLG register. If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set
2	ADCINT3	R-0/W	0h	ADC Interrupt 3 Flag Clear. Reads return 0. 0 No action 1 Clears ADCINT3 and ADCINT3RESULT flags in the ADCINTFLG register. If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set
1	ADCINT2	R-0/W	0h	ADC Interrupt 2 Flag Clear. Reads return 0. 0 No action 1 Clears ADCINT2 and ADCINT2RESULT flags in the ADCINTFLG register. . If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set
0	ADCINT1	R-0/W	0h	ADC Interrupt 1 Flag Clear. Reads return 0. 0 No action 1 Clears ADCINT1 and ADCINT1RESULT flags in the ADCINTFLG register. If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set

3.2.7 CONTROLSS_ADCn_CFG_ADCINTOVF Registers

3.2.7.1 ADCn_CFG_ADCINTOVF Register (Offset = Ah) [reset = h]

Short Description: ADC Interrupt Overflow Register

Long Description:

Return to Summary Table

Table 3-13. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 000Ah
CONTROLSS_ADC1_CFG	502C 100Ah
CONTROLSS_ADC2_CFG	502C 200Ah
CONTROLSS_ADC3_CFG	502C 300Ah
CONTROLSS_ADC4_CFG	502C 400Ah

Figure 3-6. ADCINTOVF Name Register

15	14	13	12	11	10	9	8
RESERVED							
R							
0							
7	6	5	4	3	2	1	0
RESERVED				ADCINT4	ADCINT3	ADCINT2	ADCINT1
R				R	R	R	R
0				0	0	0	0

Access Types Legend

Table 3-14. ADCINTOVF Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	RESERVED	R		Reserved
3	ADCINT4	R	0h	ADC Interrupt 4 Overflow Flags Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs. 0 No ADC interrupt overflow event detected. 1 ADC Interrupt overflow event detected. The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection.
2	ADCINT3	R	0h	ADC Interrupt 3 Overflow Flags Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs. 0 No ADC interrupt overflow event detected. 1 ADC Interrupt overflow event detected. The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection.
1	ADCINT2	R	0h	ADC Interrupt 2 Overflow Flags Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs. 0 No ADC interrupt overflow event detected. 1 ADC Interrupt overflow event detected. The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection.

Table 3-14. ADCINTOVF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ADCINT1	R	0h	ADC Interrupt 1 Overflow Flags Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs. 0 No ADC interrupt overflow event detected. 1 ADC Interrupt overflow event detected. The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection.

3.2.8 CONTROLSS_ADCn_CFG_ADCINTOVFCLR Registers

3.2.8.1 ADCn_CFG_ADCINTOVFCLR Register (Offset = Ch) [reset = h]

Short Description: ADC Interrupt Overflow Clear Register

Long Description:

Return to Summary Table

Table 3-15. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 000Ch
CONTROLSS_ADC1_CFG	502C 100Ch
CONTROLSS_ADC2_CFG	502C 200Ch
CONTROLSS_ADC3_CFG	502C 300Ch
CONTROLSS_ADC4_CFG	502C 400Ch

Figure 3-7. ADCINTOVFCLR Name Register

15	14	13	12	11	10	9	8
RESERVED							
R							
0							
7	6	5	4	3	2	1	0
RESERVED				ADCINT4	ADCINT3	ADCINT2	ADCINT1
R				R-0/W	R-0/W	R-0/W	R-0/W
0				0	0	0	0

Access Types Legend

Table 3-16. ADCINTOVFCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	RESERVED	R		Reserved
3	ADCINT4	R-0/W	0h	ADC Interrupt 4 Overflow Clear Bits 0 No action. 1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set.
2	ADCINT3	R-0/W	0h	ADC Interrupt 3 Overflow Clear Bits 0 No action. 1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set.
1	ADCINT2	R-0/W	0h	ADC Interrupt 2 Overflow Clear Bits 0 No action. 1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set.
0	ADCINT1	R-0/W	0h	ADC Interrupt 1 Overflow Clear Bits 0 No action. 1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set.

3.2.9 CONTROLSS_ADCn_CFG_ADCINTSEL1N2 Registers

3.2.9.1 ADCn_CFG_ADCINTSEL1N2 Register (Offset = Eh) [reset = h]

Short Description: ADC Interrupt 1 and 2 Selection Register

Long Description:

Return to Summary Table

Table 3-17. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 000Eh
CONTROLSS_ADC1_CFG	502C 100Eh
CONTROLSS_ADC2_CFG	502C 200Eh
CONTROLSS_ADC3_CFG	502C 300Eh
CONTROLSS_ADC4_CFG	502C 400Eh

Figure 3-8. ADCINTSEL1N2 Name Register

15	14	13	12	11	10	9	8
RESERVED	INT2CONT	INT2E	RESERVED	INT2SEL			
R	R/W	R/W	R	R/W			
0	0	0	0	0			
7	6	5	4	3	2	1	0
RESERVED	INT1CONT	INT1E	RESERVED	INT1SEL			
R	R/W	R/W	R	R/W			
0	0	0	0	0			

Access Types Legend

Table 3-18. ADCINTSEL1N2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R		Reserved
14	INT2CONT	R/W	0h	ADCINT2 Continue to Interrupt Mode 0 No further ADCINT2 pulses are generated until ADCINT2 flag (in ADCINTFLG register) is cleared by user. 1 ADCINT2 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not.
13	INT2E	R/W	0h	ADCINT2 Interrupt Enable 0 ADCINT2 is disabled 1 ADCINT2 is enabled
12	RESERVED	R		Reserved
11 - 8	INT2SEL	R/W	0h	ADCINT2 EOC Source Select 0h EOC0 is trigger for ADCINT2 1h EOC1 is trigger for ADCINT2 2h EOC2 is trigger for ADCINT2 3h EOC3 is trigger for ADCINT2 4h EOC4 is trigger for ADCINT2 5h EOC5 is trigger for ADCINT2 6h EOC6 is trigger for ADCINT2 7h EOC7 is trigger for ADCINT2 8h EOC8 is trigger for ADCINT2 9h EOC9 is trigger for ADCINT2 Ah EOC10 is trigger for ADCINT2 Bh EOC11 is trigger for ADCINT2 Ch EOC12 is trigger for ADCINT2 Dh EOC13 is trigger for ADCINT2 Eh EOC14 is trigger for ADCINT2 Fh EOC15 is trigger for ADCINT2
7	RESERVED	R		Reserved
6	INT1CONT	R/W	0h	ADCINT1 Continue to Interrupt Mode 0 No further ADCINT1 pulses are generated until ADCINT1 flag (in ADCINTFLG register) is cleared by user. 1 ADCINT1 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not.
5	INT1E	R/W	0h	ADCINT1 Interrupt Enable 0 ADCINT1 is disabled 1 ADCINT1 is enabled
4	RESERVED	R		Reserved

Table 3-18. ADCINTSEL1N2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	INT1SEL	R/W	0h	ADCINT1 EOC Source Select 0h EOC0 is trigger for ADCINT1 1h EOC1 is trigger for ADCINT1 2h EOC2 is trigger for ADCINT1 3h EOC3 is trigger for ADCINT1 4h EOC4 is trigger for ADCINT1 5h EOC5 is trigger for ADCINT1 6h EOC6 is trigger for ADCINT1 7h EOC7 is trigger for ADCINT1 8h EOC8 is trigger for ADCINT1 9h EOC9 is trigger for ADCINT1 Ah EOC10 is trigger for ADCINT1 Bh EOC11 is trigger for ADCINT1 Ch EOC12 is trigger for ADCINT1 Dh EOC13 is trigger for ADCINT1 Eh EOC14 is trigger for ADCINT1 Fh EOC15 is trigger for ADCINT1

3.2.10 CONTROLSS_ADCn_CFG_ADCINTSEL3N4 Registers

3.2.10.1 ADCn_CFG_ADCINTSEL3N4 Register (Offset = 10h) [reset = h]

Short Description: ADC Interrupt 3 and 4 Selection Register

Long Description:

Return to Summary Table

Table 3-19. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0010h
CONTROLSS_ADC1_CFG	502C 1010h
CONTROLSS_ADC2_CFG	502C 2010h
CONTROLSS_ADC3_CFG	502C 3010h
CONTROLSS_ADC4_CFG	502C 4010h

Figure 3-9. ADCINTSEL3N4 Name Register

15	14	13	12	11	10	9	8
RESERVED	INT4CONT	INT4E	RESERVED	INT4SEL			
R	R/W	R/W	R	R/W			
0	0	0	0	0			
7	6	5	4	3	2	1	0
RESERVED	INT3CONT	INT3E	RESERVED	INT3SEL			
R	R/W	R/W	R	R/W			
0	0	0	0	0			

Access Types Legend

Table 3-20. ADCINTSEL3N4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R		Reserved
14	INT4CONT	R/W	0h	ADCINT4 Continue to Interrupt Mode 0 No further ADCINT4 pulses are generated until ADCINT4 flag (in ADCINTFLG register) is cleared by user. 1 ADCINT4 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not.
13	INT4E	R/W	0h	ADCINT4 Interrupt Enable 0 ADCINT4 is disabled 1 ADCINT4 is enabled
12	RESERVED	R		Reserved
11 - 8	INT4SEL	R/W	0h	ADCINT4 EOC Source Select 0h EOC0 is trigger for ADCINT4 1h EOC1 is trigger for ADCINT4 2h EOC2 is trigger for ADCINT4 3h EOC3 is trigger for ADCINT4 4h EOC4 is trigger for ADCINT4 5h EOC5 is trigger for ADCINT4 6h EOC6 is trigger for ADCINT4 7h EOC7 is trigger for ADCINT4 8h EOC8 is trigger for ADCINT4 9h EOC9 is trigger for ADCINT4 Ah EOC10 is trigger for ADCINT4 Bh EOC11 is trigger for ADCINT4 Ch EOC12 is trigger for ADCINT4 Dh EOC13 is trigger for ADCINT4 Eh EOC14 is trigger for ADCINT4 Fh EOC15 is trigger for ADCINT4
7	RESERVED	R		Reserved
6	INT3CONT	R/W	0h	ADCINT3 Continue to Interrupt Mode 0 No further ADCINT3 pulses are generated until ADCINT3 flag (in ADCINTFLG register) is cleared by user. 1 ADCINT3 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not.
5	INT3E	R/W	0h	ADCINT3 Interrupt Enable 0 ADCINT3 is disabled 1 ADCINT3 is enabled
4	RESERVED	R		Reserved

Table 3-20. ADCINTSEL3N4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	INT3SEL	R/W	0h	ADCINT3 EOC Source Select 0h EOC0 is trigger for ADCINT3 1h EOC1 is trigger for ADCINT3 2h EOC2 is trigger for ADCINT3 3h EOC3 is trigger for ADCINT3 4h EOC4 is trigger for ADCINT3 5h EOC5 is trigger for ADCINT3 6h EOC6 is trigger for ADCINT3 7h EOC7 is trigger for ADCINT3 8h EOC8 is trigger for ADCINT3 9h EOC9 is trigger for ADCINT3 Ah EOC10 is trigger for ADCINT3 Bh EOC11 is trigger for ADCINT3 Ch EOC12 is trigger for ADCINT3 Dh EOC13 is trigger for ADCINT3 Eh EOC14 is trigger for ADCINT3 Fh EOC15 is trigger for ADCINT3

3.2.11 CONTROLSS_ADCn_CFG_ADCSOCPRICTL Registers

3.2.11.1 ADCn_CFG_ADCSOCPRICTL Register (Offset = 12h) [reset = h]

Short Description: ADC SOC Priority Control Register

Long Description:

Return to Summary Table

Table 3-21. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0012h
CONTROLSS_ADC1_CFG	502C 1012h
CONTROLSS_ADC2_CFG	502C 2012h
CONTROLSS_ADC3_CFG	502C 3012h
CONTROLSS_ADC4_CFG	502C 4012h

Figure 3-10. ADCSOCPRICTL Name Register

15	14	13	12	11	10	9	8
RESERVED						RRPOINTER	
R						R	
0						10000	
7	6	5	4	3	2	1	0
RRPOINTER			SOCPRIORITY				
R			R/W				
10000			0				

Access Types Legend

Table 3-22. ADCSOCPRICTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	R		Reserved

Table 3-22. ADCSOCPRICTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9 - 5	RRPOINTER	R	10h	Round Robin Pointer. Holds the value of the last converted round robin SOCx to be used by the round robin scheme to determine order of conversions. 00h SOC0 was last round robin SOC to convert, SOC1 is highest round robin priority. 01h SOC1 was last round robin SOC to convert, SOC2 is highest round robin priority. 02h SOC2 was last round robin SOC to convert, SOC3 is highest round robin priority. 03h SOC3 was last round robin SOC to convert, SOC4 is highest round robin priority. 04h SOC4 was last round robin SOC to convert, SOC5 is highest round robin priority. 05h SOC5 was last round robin SOC to convert, SOC6 is highest round robin priority. 06h SOC6 was last round robin SOC to convert, SOC7 is highest round robin priority. 07h SOC7 was last round robin SOC to convert, SOC8 is highest round robin priority. 08h SOC8 was last round robin SOC to convert, SOC9 is highest round robin priority. 09h SOC9 was last round robin SOC to convert, SOC10 is highest round robin priority. 0Ah SOC10 was last round robin SOC to convert, SOC11 is highest round robin priority. 0Bh SOC11 was last round robin SOC to convert, SOC12 is highest round robin priority. 0Ch SOC12 was last round robin SOC to convert, SOC13 is highest round robin priority. 0Dh SOC13 was last round robin SOC to convert, SOC14 is highest round robin priority. 0Eh SOC14 was last round robin SOC to convert, SOC15 is highest round robin priority. 0Fh SOC15 was last round robin SOC to convert, SOC0 is highest round robin priority. 10h Reset value to indicate no SOC has been converted. SOC0 is highest round robin priority. Set to this value when the device is reset, when the ADCCTL1.RESET bit is set, or when the ADCSOCPRICTL register is written. In the latter case, if a conversion is currently in progress, it will complete and then the new priority will take effect. Others Invalid value.
4 - 0	SOCPRIORITY	R/W	0h	SOC Priority Determines the cutoff point for priority mode and round robin arbitration for SOCx 00h SOC priority is handled in round robin mode for all channels. 01h SOC0 is high priority, rest of channels are in round robin mode. 02h SOC0-SOC1 are high priority, SOC2-SOC15 are in round robin mode. 03h SOC0-SOC2 are high priority, SOC3-SOC15 are in round robin mode. 04h SOC0-SOC3 are high priority, SOC4-SOC15 are in round robin mode. 05h SOC0-SOC4 are high priority, SOC5-SOC15 are in round robin mode. 06h SOC0-SOC5 are high priority, SOC6-SOC15 are in round robin mode. 07h SOC0-SOC6 are high priority, SOC7-SOC15 are in round robin mode. 08h SOC0-SOC7 are high priority, SOC8-SOC15 are in round robin mode. 09h SOC0-SOC8 are high priority, SOC9-SOC15 are in round robin mode. 0Ah SOC0-SOC9 are high priority, SOC10-SOC15 are in round robin mode. 0Bh SOC0-SOC10 are high priority, SOC11-SOC15 are in round robin mode. 0Ch SOC0-SOC11 are high priority, SOC12-SOC15 are in round robin mode. 0Dh SOC0-SOC12 are high priority, SOC13-SOC15 are in round robin mode. 0Eh SOC0-SOC13 are high priority, SOC14-SOC15 are in round robin mode. 0Fh SOC0-SOC14 are high priority, SOC15 is in round robin mode. 10h All SOCs are in high priority mode, arbitrated by SOC number. Others Invalid selection.

3.2.12 CONTROLSS_ADCn_CFG_ADCINTSOCSEL1 Registers

3.2.12.1 ADCn_CFG_ADCINTSOCSEL1 Register (Offset = 14h) [reset = h]

Short Description: ADC Interrupt SOC Selection 1 Register

Long Description:

Return to Summary Table

Table 3-23. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0014h
CONTROLSS_ADC1_CFG	502C 1014h
CONTROLSS_ADC2_CFG	502C 2014h
CONTROLSS_ADC3_CFG	502C 3014h
CONTROLSS_ADC4_CFG	502C 4014h

Figure 3-11. ADCINTSOCSEL1 Name Register

15	14	13	12	11	10	9	8
SOC7		SOC6		SOC5		SOC4	
R/W		R/W		R/W		R/W	
0		0		0		0	
7	6	5	4	3	2	1	0
SOC3		SOC2		SOC1		SOC0	
R/W		R/W		R/W		R/W	
0		0		0		0	

Access Types Legend

Table 3-24. ADCINTSOCSEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	SOC7	R/W	0h	SOC7 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC7. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC7. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC7. 10 ADCINT2 will trigger SOC7. 11 Invalid selection.
13 - 12	SOC6	R/W	0h	SOC6 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC6. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC6. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC6. 10 ADCINT2 will trigger SOC6. 11 Invalid selection.
11 - 10	SOC5	R/W	0h	SOC5 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC5. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC5. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC5. 10 ADCINT2 will trigger SOC5. 11 Invalid selection.
9 - 8	SOC4	R/W	0h	SOC4 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC4. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC4. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC4. 10 ADCINT2 will trigger SOC4. 11 Invalid selection.

Table 3-24. ADCINTSOCSEL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7 - 6	SOC3	R/W	0h	SOC3 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC3. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC3. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC3. 10 ADCINT2 will trigger SOC3. 11 Invalid selection.
5 - 4	SOC2	R/W	0h	SOC2 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC2. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC2. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC2. 10 ADCINT2 will trigger SOC2. 11 Invalid selection.
3 - 2	SOC1	R/W	0h	SOC1 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC1. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC1. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC1. 10 ADCINT2 will trigger SOC1. 11 Invalid selection.
1 - 0	SOC0	R/W	0h	SOC0 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC0. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC0. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC0. 10 ADCINT2 will trigger SOC0. 11 Invalid selection.

3.2.13 CONTROLSS_ADCn_CFG_ADCINTSOCSEL2 Registers

3.2.13.1 ADCn_CFG_ADCINTSOCSEL2 Register (Offset = 16h) [reset = h]

Short Description: ADC Interrupt SOC Selection 2 Register

Long Description:

Return to Summary Table

Table 3-25. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0016h
CONTROLSS_ADC1_CFG	502C 1016h
CONTROLSS_ADC2_CFG	502C 2016h
CONTROLSS_ADC3_CFG	502C 3016h
CONTROLSS_ADC4_CFG	502C 4016h

Figure 3-12. ADCINTSOCSEL2 Name Register

15	14	13	12	11	10	9	8
SOC15		SOC14		SOC13		SOC12	
R/W		R/W		R/W		R/W	
0		0		0		0	
7	6	5	4	3	2	1	0
SOC11		SOC10		SOC9		SOC8	
R/W		R/W		R/W		R/W	
0		0		0		0	

Access Types Legend

Table 3-26. ADCINTSOCSEL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	SOC15	R/W	0h	SOC15 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC15. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC15. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC15. 10 ADCINT2 will trigger SOC15. 11 Invalid selection.
13 - 12	SOC14	R/W	0h	SOC14 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC14. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC14. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC14. 10 ADCINT2 will trigger SOC14. 11 Invalid selection.
11 - 10	SOC13	R/W	0h	SOC13 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC13. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC13. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC13. 10 ADCINT2 will trigger SOC13. 11 Invalid selection.
9 - 8	SOC12	R/W	0h	SOC12 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC12. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC12. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC12. 10 ADCINT2 will trigger SOC12. 11 Invalid selection.

Table 3-26. ADCINTSOCSEL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7 - 6	SOC11	R/W	0h	SOC11 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC11. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC11. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC11. 10 ADCINT2 will trigger SOC11. 11 Invalid selection.
5 - 4	SOC10	R/W	0h	SOC10 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC10. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC10. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC10. 10 ADCINT2 will trigger SOC10. 11 Invalid selection.
3 - 2	SOC9	R/W	0h	SOC9 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC9. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC9. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC9. 10 ADCINT2 will trigger SOC9. 11 Invalid selection.
1 - 0	SOC8	R/W	0h	SOC8 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC8. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC8. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC8. 10 ADCINT2 will trigger SOC8. 11 Invalid selection.

3.2.14 CONTROLSS_ADCn_CFG_ADCSOCFLG1 Registers

3.2.14.1 ADCn_CFG_ADCSOCFLG1 Register (Offset = 18h) [reset = h]

Short Description: ADC SOC Flag 1 Register

Long Description:

Return to Summary Table

Table 3-27. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0018h
CONTROLSS_ADC1_CFG	502C 1018h
CONTROLSS_ADC2_CFG	502C 2018h
CONTROLSS_ADC3_CFG	502C 3018h
CONTROLSS_ADC4_CFG	502C 4018h

Figure 3-13. ADCSOCFLG1 Name Register

15	14	13	12	11	10	9	8
SOC15	SOC14	SOC13	SOC12	SOC11	SOC10	SOC9	SOC8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
SOC7	SOC6	SOC5	SOC4	SOC3	SOC2	SOC1	SOC0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-28. ADCSOCFLG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SOC15	R	0h	SOC15 Start of Conversion Flag. Indicates the state of SOC15 conversions. 0 No sample pending for SOC15. 1 Trigger has been received and sample is pending for SOC15. This bit will be automatically cleared when the SOC15 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
14	SOC14	R	0h	SOC14 Start of Conversion Flag. Indicates the state of SOC14 conversions. 0 No sample pending for SOC14. 1 Trigger has been received and sample is pending for SOC14. This bit will be automatically cleared when the SOC14 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
13	SOC13	R	0h	SOC13 Start of Conversion Flag. Indicates the state of SOC13 conversions. 0 No sample pending for SOC13. 1 Trigger has been received and sample is pending for SOC13. This bit will be automatically cleared when the SOC13 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.

Table 3-28. ADCSOCFLG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	SOC12	R	0h	SOC12 Start of Conversion Flag. Indicates the state of SOC12 conversions. 0 No sample pending for SOC12. 1 Trigger has been received and sample is pending for SOC12. This bit will be automatically cleared when the SOC12 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
11	SOC11	R	0h	SOC11 Start of Conversion Flag. Indicates the state of SOC11 conversions. 0 No sample pending for SOC11. 1 Trigger has been received and sample is pending for SOC11. This bit will be automatically cleared when the SOC11 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
10	SOC10	R	0h	SOC10 Start of Conversion Flag. Indicates the state of SOC10 conversions. 0 No sample pending for SOC10. 1 Trigger has been received and sample is pending for SOC10. This bit will be automatically cleared when the SOC10 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
9	SOC9	R	0h	SOC9 Start of Conversion Flag. Indicates the state of SOC9 conversions. 0 No sample pending for SOC9. 1 Trigger has been received and sample is pending for SOC9. This bit will be automatically cleared when the SOC9 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
8	SOC8	R	0h	SOC8 Start of Conversion Flag. Indicates the state of SOC8 conversions. 0 No sample pending for SOC8. 1 Trigger has been received and sample is pending for SOC8. This bit will be automatically cleared when the SOC8 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
7	SOC7	R	0h	SOC7 Start of Conversion Flag. Indicates the state of SOC7 conversions. 0 No sample pending for SOC7. 1 Trigger has been received and sample is pending for SOC7. This bit will be automatically cleared when the SOC7 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
6	SOC6	R	0h	SOC6 Start of Conversion Flag. Indicates the state of SOC6 conversions. 0 No sample pending for SOC6. 1 Trigger has been received and sample is pending for SOC6. This bit will be automatically cleared when the SOC6 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.

Table 3-28. ADCSOCFLG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	SOC5	R	0h	SOC5 Start of Conversion Flag. Indicates the state of SOC5 conversions. 0 No sample pending for SOC5. 1 Trigger has been received and sample is pending for SOC5. This bit will be automatically cleared when the SOC5 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
4	SOC4	R	0h	SOC4 Start of Conversion Flag. Indicates the state of SOC4 conversions. 0 No sample pending for SOC4. 1 Trigger has been received and sample is pending for SOC4. This bit will be automatically cleared when the SOC4 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
3	SOC3	R	0h	SOC3 Start of Conversion Flag. Indicates the state of SOC3 conversions. 0 No sample pending for SOC3. 1 Trigger has been received and sample is pending for SOC3. This bit will be automatically cleared when the SOC3 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
2	SOC2	R	0h	SOC2 Start of Conversion Flag. Indicates the state of SOC2 conversions. 0 No sample pending for SOC2. 1 Trigger has been received and sample is pending for SOC2. This bit will be automatically cleared when the SOC2 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
1	SOC1	R	0h	SOC1 Start of Conversion Flag. Indicates the state of SOC1 conversions. 0 No sample pending for SOC1. 1 Trigger has been received and sample is pending for SOC1. This bit will be automatically cleared when the SOC1 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
0	SOC0	R	0h	SOC0 Start of Conversion Flag. Indicates the state of SOC0 conversions. 0 No sample pending for SOC0. 1 Trigger has been received and sample is pending for SOC0. This bit will be automatically cleared when the SOC0 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.

3.2.15 CONTROLSS_ADCn_CFG_ADCSOCFRC1 Registers

3.2.15.1 ADCn_CFG_ADCSOCFRC1 Register (Offset = 1Ah) [reset = h]

Short Description: ADC SOC Force 1 Register

Long Description:

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Table 3-29. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 001Ah
CONTROLSS_ADC1_CFG	502C 101Ah
CONTROLSS_ADC2_CFG	502C 201Ah
CONTROLSS_ADC3_CFG	502C 301Ah
CONTROLSS_ADC4_CFG	502C 401Ah

Figure 3-14. ADCSOCFRC1 Name Register

15	14	13	12	11	10	9	8
SOC15	SOC14	SOC13	SOC12	SOC11	SOC10	SOC9	SOC8
R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0/W
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
SOC7	SOC6	SOC5	SOC4	SOC3	SOC2	SOC1	SOC0
R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0/W
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-30. ADCSOCFRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SOC15	R-0/W	0h	SOC15 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC15 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC15 flag bit to 1. This will cause a conversion to start once priority is given to SOC15. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC15 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
14	SOC14	R-0/W	0h	SOC14 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC14 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC14 flag bit to 1. This will cause a conversion to start once priority is given to SOC14. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC14 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.

Table 3-30. ADCSOCFRC1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	SOC13	R-0/W	0h	SOC13 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC13 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC13 flag bit to 1. This will cause a conversion to start once priority is given to SOC13. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC13 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
12	SOC12	R-0/W	0h	SOC12 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC12 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC12 flag bit to 1. This will cause a conversion to start once priority is given to SOC12. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC12 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
11	SOC11	R-0/W	0h	SOC11 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC11 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC11 flag bit to 1. This will cause a conversion to start once priority is given to SOC11. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC11 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
10	SOC10	R-0/W	0h	SOC10 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC10 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC10 flag bit to 1. This will cause a conversion to start once priority is given to SOC10. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC10 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
9	SOC9	R-0/W	0h	SOC9 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC9 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC9 flag bit to 1. This will cause a conversion to start once priority is given to SOC9. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC9 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.

Table 3-30. ADCSOCFRC1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	SOC8	R-0/W	0h	SOC8 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC8 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC8 flag bit to 1. This will cause a conversion to start once priority is given to SOC8. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC8 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
7	SOC7	R-0/W	0h	SOC7 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC7 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC7 flag bit to 1. This will cause a conversion to start once priority is given to SOC7. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC7 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
6	SOC6	R-0/W	0h	SOC6 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC6 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC6 flag bit to 1. This will cause a conversion to start once priority is given to SOC6. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC6 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
5	SOC5	R-0/W	0h	SOC5 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC5 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC5 flag bit to 1. This will cause a conversion to start once priority is given to SOC5. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC5 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
4	SOC4	R-0/W	0h	SOC4 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC4 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC4 flag bit to 1. This will cause a conversion to start once priority is given to SOC4. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC4 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.

Table 3-30. ADCSOCFRC1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	SOC3	R-0/W	0h	SOC3 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC3 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC3 flag bit to 1. This will cause a conversion to start once priority is given to SOC3. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC3 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
2	SOC2	R-0/W	0h	SOC2 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC2 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC2 flag bit to 1. This will cause a conversion to start once priority is given to SOC2. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC2 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
1	SOC1	R-0/W	0h	SOC1 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC1 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC1 flag bit to 1. This will cause a conversion to start once priority is given to SOC1. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC1 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
0	SOC0	R-0/W	0h	SOC0 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC0 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC0 flag bit to 1. This will cause a conversion to start once priority is given to SOC0. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC0 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.

3.2.16 CONTROLSS_ADCn_CFG_ADCSOCOVF1 Registers

3.2.16.1 ADCn_CFG_ADCSOCOVF1 Register (Offset = 1Ch) [reset = h]

Short Description: ADC SOC Overflow 1 Register

Long Description:

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Table 3-31. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 001Ch
CONTROLSS_ADC1_CFG	502C 101Ch
CONTROLSS_ADC2_CFG	502C 201Ch
CONTROLSS_ADC3_CFG	502C 301Ch
CONTROLSS_ADC4_CFG	502C 401Ch

Figure 3-15. ADCSOCOVF1 Name Register

15	14	13	12	11	10	9	8
SOC15	SOC14	SOC13	SOC12	SOC11	SOC10	SOC9	SOC8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
SOC7	SOC6	SOC5	SOC4	SOC3	SOC2	SOC1	SOC0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-32. ADCSOCOVF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SOC15	R	0h	SOC15 Start of Conversion Overflow Flag. Indicates an SOC15 event was generated in hardware while an existing SOC15 event was already pending. 0 No SOC15 event overflow. 1 SOC15 event overflow. An overflow condition does not stop SOC15 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
14	SOC14	R	0h	SOC14 Start of Conversion Overflow Flag. Indicates an SOC14 event was generated in hardware while an existing SOC14 event was already pending. 0 No SOC14 event overflow. 1 SOC14 event overflow. An overflow condition does not stop SOC14 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
13	SOC13	R	0h	SOC13 Start of Conversion Overflow Flag. Indicates an SOC13 event was generated in hardware while an existing SOC13 event was already pending. 0 No SOC13 event overflow. 1 SOC13 event overflow. An overflow condition does not stop SOC13 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
12	SOC12	R	0h	SOC12 Start of Conversion Overflow Flag. Indicates an SOC12 event was generated in hardware while an existing SOC12 event was already pending. 0 No SOC12 event overflow. 1 SOC12 event overflow. An overflow condition does not stop SOC12 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.

Table 3-32. ADCSOCOVF1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	SOC11	R	0h	SOC11 Start of Conversion Overflow Flag. Indicates an SOC11 event was generated in hardware while an existing SOC11 event was already pending. 0 No SOC11 event overflow. 1 SOC11 event overflow. An overflow condition does not stop SOC11 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
10	SOC10	R	0h	SOC10 Start of Conversion Overflow Flag. Indicates an SOC10 event was generated in hardware while an existing SOC10 event was already pending. 0 No SOC10 event overflow. 1 SOC10 event overflow. An overflow condition does not stop SOC10 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
9	SOC9	R	0h	SOC9 Start of Conversion Overflow Flag. Indicates an SOC9 event was generated in hardware while an existing SOC9 event was already pending. 0 No SOC9 event overflow. 1 SOC9 event overflow. An overflow condition does not stop SOC9 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
8	SOC8	R	0h	SOC8 Start of Conversion Overflow Flag. Indicates an SOC8 event was generated in hardware while an existing SOC8 event was already pending. 0 No SOC8 event overflow. 1 SOC8 event overflow. An overflow condition does not stop SOC8 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
7	SOC7	R	0h	SOC7 Start of Conversion Overflow Flag. Indicates an SOC7 event was generated in hardware while an existing SOC7 event was already pending. 0 No SOC7 event overflow. 1 SOC7 event overflow. An overflow condition does not stop SOC7 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
6	SOC6	R	0h	SOC6 Start of Conversion Overflow Flag. Indicates an SOC6 event was generated in hardware while an existing SOC6 event was already pending. 0 No SOC6 event overflow. 1 SOC6 event overflow. An overflow condition does not stop SOC6 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
5	SOC5	R	0h	SOC5 Start of Conversion Overflow Flag. Indicates an SOC5 event was generated in hardware while an existing SOC5 event was already pending. 0 No SOC5 event overflow. 1 SOC5 event overflow. An overflow condition does not stop SOC5 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
4	SOC4	R	0h	SOC4 Start of Conversion Overflow Flag. Indicates an SOC4 event was generated in hardware while an existing SOC4 event was already pending. 0 No SOC4 event overflow. 1 SOC4 event overflow. An overflow condition does not stop SOC4 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
3	SOC3	R	0h	SOC3 Start of Conversion Overflow Flag. Indicates an SOC3 event was generated in hardware while an existing SOC3 event was already pending. 0 No SOC3 event overflow. 1 SOC3 event overflow. An overflow condition does not stop SOC3 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
2	SOC2	R	0h	SOC2 Start of Conversion Overflow Flag. Indicates an SOC2 event was generated in hardware while an existing SOC2 event was already pending. 0 No SOC2 event overflow. 1 SOC2 event overflow. An overflow condition does not stop SOC2 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.

Table 3-32. ADCSOCOVF1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SOC1	R	0h	SOC1 Start of Conversion Overflow Flag. Indicates an SOC1 event was generated in hardware while an existing SOC1 event was already pending. 0 No SOC1 event overflow. 1 SOC1 event overflow. An overflow condition does not stop SOC1 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
0	SOC0	R	0h	SOC0 Start of Conversion Overflow Flag. Indicates an SOC0 event was generated in hardware while an existing SOC0 event was already pending. 0 No SOC0 event overflow. 1 SOC0 event overflow. An overflow condition does not stop SOC0 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.

3.2.17 CONTROLSS_ADCn_CFG_ADCSOCOVFCLR1 Registers

3.2.17.1 ADCn_CFG_ADCSOCOVFCLR1 Register (Offset = 1Eh) [reset = h]

Short Description: ADC SOC Overflow Clear 1 Register

Long Description:

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Table 3-33. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 001Eh
CONTROLSS_ADC1_CFG	502C 101Eh
CONTROLSS_ADC2_CFG	502C 201Eh
CONTROLSS_ADC3_CFG	502C 301Eh
CONTROLSS_ADC4_CFG	502C 401Eh

Figure 3-16. ADCSOCOVFCLR1 Name Register

15	14	13	12	11	10	9	8
SOC15	SOC14	SOC13	SOC12	SOC11	SOC10	SOC9	SOC8
R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0/W
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
SOC7	SOC6	SOC5	SOC4	SOC3	SOC2	SOC1	SOC0
R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0/W
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-34. ADCSOCOVFCLR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SOC15	R-0/W	0h	SOC15 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC15 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC15 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
14	SOC14	R-0/W	0h	SOC14 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC14 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC14 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
13	SOC13	R-0/W	0h	SOC13 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC13 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC13 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
12	SOC12	R-0/W	0h	SOC12 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC12 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC12 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..

Table 3-34. ADCSOCOVFCLR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	SOC11	R-0/W	0h	SOC11 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC11 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC11 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
10	SOC10	R-0/W	0h	SOC10 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC10 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC10 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
9	SOC9	R-0/W	0h	SOC9 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC9 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC9 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
8	SOC8	R-0/W	0h	SOC8 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC8 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC8 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
7	SOC7	R-0/W	0h	SOC7 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC7 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC7 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
6	SOC6	R-0/W	0h	SOC6 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC6 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC6 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
5	SOC5	R-0/W	0h	SOC5 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC5 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC5 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
4	SOC4	R-0/W	0h	SOC4 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC4 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC4 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
3	SOC3	R-0/W	0h	SOC3 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC3 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC3 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..

Table 3-34. ADCSOCOVFCLR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SOC2	R-0/W	0h	SOC2 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC2 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC2 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
1	SOC1	R-0/W	0h	SOC1 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC1 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC1 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
0	SOC0	R-0/W	0h	SOC0 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC0 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC0 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..

3.2.18 CONTROLSS_ADCn_CFG_ADCSOC0CTL Registers

3.2.18.1 ADCn_CFG_ADCSOC0CTL Register (Offset = 20h) [reset = h]

Short Description: ADC SOC0 Control Register

Long Description:

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Table 3-35. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0020h
CONTROLSS_ADC1_CFG	502C 1020h
CONTROLSS_ADC2_CFG	502C 2020h
CONTROLSS_ADC3_CFG	502C 3020h
CONTROLSS_ADC4_CFG	502C 4020h

Figure 3-17. ADCSOC0CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
R					R/W							R/W			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
R/W	R							R/W							
0	0							0							

Access Types Legend

Table 3-36. ADCSOC0CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	R		Reserved
26 - 20	TRIGSEL	R/W	0h	SOC0 Trigger Source Select. Along with the SOC0 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC0 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	R/W	0h	SOC0 Channel Select. Selects the channel to be converted when SOC0 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	R		Reserved
8 - 0	ACQPS	R/W	0h	SOC0 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

3.2.19 CONTROLSS_ADCn_CFG_ADCSOC1CTL Registers

3.2.19.1 ADCn_CFG_ADCSOC1CTL Register (Offset = 24h) [reset = h]

Short Description: ADC SOC1 Control Register

Long Description:

Return to Summary Table

Table 3-37. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0024h
CONTROLSS_ADC1_CFG	502C 1024h
CONTROLSS_ADC2_CFG	502C 2024h
CONTROLSS_ADC3_CFG	502C 3024h
CONTROLSS_ADC4_CFG	502C 4024h

Figure 3-18. ADCSOC1CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
R					R/W							R/W			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
R/W	R							R/W							
0	0							0							

Access Types Legend

Table 3-38. ADCSOC1CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	R		Reserved
26 - 20	TRIGSEL	R/W	0h	SOC1 Trigger Source Select. Along with the SOC1 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC1 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	R/W	0h	SOC1 Channel Select. Selects the channel to be converted when SOC1 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	R		Reserved
8 - 0	ACQPS	R/W	0h	SOC1 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

3.2.20 CONTROLSS_ADCn_CFG_ADCSOC2CTL Registers

3.2.20.1 ADCn_CFG_ADCSOC2CTL Register (Offset = 28h) [reset = h]

Short Description: ADC SOC2 Control Register

Long Description:

Return to Summary Table

Table 3-39. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0028h
CONTROLSS_ADC1_CFG	502C 1028h
CONTROLSS_ADC2_CFG	502C 2028h
CONTROLSS_ADC3_CFG	502C 3028h
CONTROLSS_ADC4_CFG	502C 4028h

Figure 3-19. ADCSOC2CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
R					R/W							R/W			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
R/W	R							R/W							
0	0							0							

Access Types Legend

Table 3-40. ADCSOC2CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	R		Reserved
26 - 20	TRIGSEL	R/W	0h	SOC2 Trigger Source Select. Along with the SOC2 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC2 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	R/W	0h	SOC2 Channel Select. Selects the channel to be converted when SOC2 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	R		Reserved
8 - 0	ACQPS	R/W	0h	SOC2 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

3.2.21 CONTROLSS_ADCn_CFG_ADCSOC3CTL Registers

3.2.21.1 ADCn_CFG_ADCSOC3CTL Register (Offset = 2Ch) [reset = h]

Short Description: ADC SOC3 Control Register

Long Description:

Return to Summary Table

Table 3-41. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 002Ch
CONTROLSS_ADC1_CFG	502C 102Ch
CONTROLSS_ADC2_CFG	502C 202Ch
CONTROLSS_ADC3_CFG	502C 302Ch
CONTROLSS_ADC4_CFG	502C 402Ch

Figure 3-20. ADCSOC3CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
R					R/W							R/W			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
R/W	R							R/W							
0	0							0							

Access Types Legend

Table 3-42. ADCSOC3CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	R		Reserved
26 - 20	TRIGSEL	R/W	0h	SOC3 Trigger Source Select. Along with the SOC3 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC3 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	R/W	0h	SOC3 Channel Select. Selects the channel to be converted when SOC3 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	R		Reserved
8 - 0	ACQPS	R/W	0h	SOC3 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

3.2.22 CONTROLSS_ADCn_CFG_ADCSOC4CTL Registers

3.2.22.1 ADCn_CFG_ADCSOC4CTL Register (Offset = 30h) [reset = h]

Short Description: ADC SOC4 Control Register

Long Description:

Return to Summary Table

Table 3-43. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0030h
CONTROLSS_ADC1_CFG	502C 1030h
CONTROLSS_ADC2_CFG	502C 2030h
CONTROLSS_ADC3_CFG	502C 3030h
CONTROLSS_ADC4_CFG	502C 4030h

Figure 3-21. ADCSOC4CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
R					R/W							R/W			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
R/W	R							R/W							
0	0							0							

Access Types Legend

Table 3-44. ADCSOC4CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	R		Reserved
26 - 20	TRIGSEL	R/W	0h	SOC4 Trigger Source Select. Along with the SOC4 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC4 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	R/W	0h	SOC4 Channel Select. Selects the channel to be converted when SOC4 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	R		Reserved
8 - 0	ACQPS	R/W	0h	SOC4 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

3.2.23 CONTROLSS_ADCn_CFG_ADCSOC5CTL Registers

3.2.23.1 ADCn_CFG_ADCSOC5CTL Register (Offset = 34h) [reset = h]

Short Description: ADC SOC5 Control Register

Long Description:

Return to Summary Table

Table 3-45. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0034h
CONTROLSS_ADC1_CFG	502C 1034h
CONTROLSS_ADC2_CFG	502C 2034h
CONTROLSS_ADC3_CFG	502C 3034h
CONTROLSS_ADC4_CFG	502C 4034h

Figure 3-22. ADCSOC5CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
R					R/W							R/W			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
R/W	R							R/W							
0	0							0							

Access Types Legend

Table 3-46. ADCSOC5CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	R		Reserved
26 - 20	TRIGSEL	R/W	0h	SOC5 Trigger Source Select. Along with the SOC5 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC5 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	R/W	0h	SOC5 Channel Select. Selects the channel to be converted when SOC5 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	R		Reserved
8 - 0	ACQPS	R/W	0h	SOC5 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

3.2.24 CONTROLSS_ADCn_CFG_ADCSOC6CTL Registers

3.2.24.1 ADCn_CFG_ADCSOC6CTL Register (Offset = 38h) [reset = h]

Short Description: ADC SOC6 Control Register

Long Description:

Return to Summary Table

Table 3-47. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0038h
CONTROLSS_ADC1_CFG	502C 1038h
CONTROLSS_ADC2_CFG	502C 2038h
CONTROLSS_ADC3_CFG	502C 3038h
CONTROLSS_ADC4_CFG	502C 4038h

Figure 3-23. ADCSOC6CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
R					R/W							R/W			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
R/W	R							R/W							
0	0							0							

Access Types Legend

Table 3-48. ADCSOC6CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	R		Reserved
26 - 20	TRIGSEL	R/W	0h	SOC6 Trigger Source Select. Along with the SOC6 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC6 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	R/W	0h	SOC6 Channel Select. Selects the channel to be converted when SOC6 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	R		Reserved
8 - 0	ACQPS	R/W	0h	SOC6 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

3.2.25 CONTROLSS_ADCn_CFG_ADCSOC7CTL Registers

3.2.25.1 ADCn_CFG_ADCSOC7CTL Register (Offset = 3Ch) [reset = h]

Short Description: ADC SOC7 Control Register

Long Description:

Return to Summary Table

Table 3-49. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 003Ch
CONTROLSS_ADC1_CFG	502C 103Ch
CONTROLSS_ADC2_CFG	502C 203Ch
CONTROLSS_ADC3_CFG	502C 303Ch
CONTROLSS_ADC4_CFG	502C 403Ch

Figure 3-24. ADCSOC7CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
R					R/W							R/W			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
R/W	R							R/W							
0	0							0							

Access Types Legend

Table 3-50. ADCSOC7CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	R		Reserved
26 - 20	TRIGSEL	R/W	0h	SOC7 Trigger Source Select. Along with the SOC7 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC7 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	R/W	0h	SOC7 Channel Select. Selects the channel to be converted when SOC7 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	R		Reserved
8 - 0	ACQPS	R/W	0h	SOC7 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

3.2.26 CONTROLSS_ADCn_CFG_ADCSOC8CTL Registers

3.2.26.1 ADCn_CFG_ADCSOC8CTL Register (Offset = 40h) [reset = h]

Short Description: ADC SOC8 Control Register

Long Description:

Return to Summary Table

Table 3-51. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0040h
CONTROLSS_ADC1_CFG	502C 1040h
CONTROLSS_ADC2_CFG	502C 2040h
CONTROLSS_ADC3_CFG	502C 3040h
CONTROLSS_ADC4_CFG	502C 4040h

Figure 3-25. ADCSOC8CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
R					R/W							R/W			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
R/W	R							R/W							
0	0							0							

Access Types Legend

Table 3-52. ADCSOC8CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	R		Reserved
26 - 20	TRIGSEL	R/W	0h	SOC8 Trigger Source Select. Along with the SOC8 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC8 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	R/W	0h	SOC8 Channel Select. Selects the channel to be converted when SOC8 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	R		Reserved
8 - 0	ACQPS	R/W	0h	SOC8 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device data sheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

3.2.27 CONTROLSS_ADCn_CFG_ADCSOC9CTL Registers

3.2.27.1 ADCn_CFG_ADCSOC9CTL Register (Offset = 44h) [reset = h]

Short Description: ADC SOC9 Control Register

Long Description:

Return to Summary Table

Table 3-53. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0044h
CONTROLSS_ADC1_CFG	502C 1044h
CONTROLSS_ADC2_CFG	502C 2044h
CONTROLSS_ADC3_CFG	502C 3044h
CONTROLSS_ADC4_CFG	502C 4044h

Figure 3-26. ADCSOC9CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
R					R/W							R/W			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
R/W	R							R/W							
0	0							0							

Access Types Legend

Table 3-54. ADCSOC9CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	R		Reserved
26 - 20	TRIGSEL	R/W	0h	SOC9 Trigger Source Select. Along with the SOC9 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC9 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	R/W	0h	SOC9 Channel Select. Selects the channel to be converted when SOC9 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	R		Reserved
8 - 0	ACQPS	R/W	0h	SOC9 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

3.2.28 CONTROLSS_ADCn_CFG_ADCSOC10CTL Registers

3.2.28.1 ADCn_CFG_ADCSOC10CTL Register (Offset = 48h) [reset = h]

Short Description: ADC SOC10 Control Register

Long Description:

Return to Summary Table

Table 3-55. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0048h
CONTROLSS_ADC1_CFG	502C 1048h
CONTROLSS_ADC2_CFG	502C 2048h
CONTROLSS_ADC3_CFG	502C 3048h
CONTROLSS_ADC4_CFG	502C 4048h

Figure 3-27. ADCSOC10CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
R					R/W							R/W			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
R/W	R							R/W							
0	0							0							

Access Types Legend

Table 3-56. ADCSOC10CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	R		Reserved
26 - 20	TRIGSEL	R/W	0h	SOC10 Trigger Source Select. Along with the SOC10 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC10 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	R/W	0h	SOC10 Channel Select. Selects the channel to be converted when SOC10 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	R		Reserved
8 - 0	ACQPS	R/W	0h	SOC10 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

3.2.29 CONTROLSS_ADCn_CFG_ADCSOC11CTL Registers

3.2.29.1 ADCn_CFG_ADCSOC11CTL Register (Offset = 4Ch) [reset = h]

Short Description: ADC SOC11 Control Register

Long Description:

Return to Summary Table

Table 3-57. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 004Ch
CONTROLSS_ADC1_CFG	502C 104Ch
CONTROLSS_ADC2_CFG	502C 204Ch
CONTROLSS_ADC3_CFG	502C 304Ch
CONTROLSS_ADC4_CFG	502C 404Ch

Figure 3-28. ADCSOC11CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
R					R/W							R/W			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
R/W	R							R/W							
0	0							0							

Access Types Legend

Table 3-58. ADCSOC11CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	R		Reserved
26 - 20	TRIGSEL	R/W	0h	SOC11 Trigger Source Select. Along with the SOC11 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC11 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	R/W	0h	SOC11 Channel Select. Selects the channel to be converted when SOC11 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	R		Reserved
8 - 0	ACQPS	R/W	0h	SOC11 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

3.2.30 CONTROLSS_ADCn_CFG_ADCSOC12CTL Registers

3.2.30.1 ADCn_CFG_ADCSOC12CTL Register (Offset = 50h) [reset = h]

Short Description: ADC SOC12 Control Register

Long Description:

Return to Summary Table

Table 3-59. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0050h
CONTROLSS_ADC1_CFG	502C 1050h
CONTROLSS_ADC2_CFG	502C 2050h
CONTROLSS_ADC3_CFG	502C 3050h
CONTROLSS_ADC4_CFG	502C 4050h

Figure 3-29. ADCSOC12CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
R					R/W							R/W			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
R/W	R							R/W							
0	0							0							

Access Types Legend

Table 3-60. ADCSOC12CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	R		Reserved
26 - 20	TRIGSEL	R/W	0h	SOC12 Trigger Source Select. Along with the SOC12 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC12 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	R/W	0h	SOC12 Channel Select. Selects the channel to be converted when SOC12 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	R		Reserved
8 - 0	ACQPS	R/W	0h	SOC12 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

3.2.31 CONTROLSS_ADCn_CFG_ADCSOC13CTL Registers

3.2.31.1 ADCn_CFG_ADCSOC13CTL Register (Offset = 54h) [reset = h]

Short Description: ADC SOC13 Control Register

Long Description:

Return to Summary Table

Table 3-61. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0054h
CONTROLSS_ADC1_CFG	502C 1054h
CONTROLSS_ADC2_CFG	502C 2054h
CONTROLSS_ADC3_CFG	502C 3054h
CONTROLSS_ADC4_CFG	502C 4054h

Figure 3-30. ADCSOC13CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
R					R/W							R/W			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
R/W	R							R/W							
0	0							0							

Access Types Legend

Table 3-62. ADCSOC13CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	R		Reserved
26 - 20	TRIGSEL	R/W	0h	SOC13 Trigger Source Select. Along with the SOC13 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC13 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	R/W	0h	SOC13 Channel Select. Selects the channel to be converted when SOC13 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	R		Reserved
8 - 0	ACQPS	R/W	0h	SOC13 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

3.2.32 CONTROLSS_ADCn_CFG_ADCSOC14CTL Registers

3.2.32.1 ADCn_CFG_ADCSOC14CTL Register (Offset = 58h) [reset = h]

Short Description: ADC SOC14 Control Register

Long Description:

Return to Summary Table

Table 3-63. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0058h
CONTROLSS_ADC1_CFG	502C 1058h
CONTROLSS_ADC2_CFG	502C 2058h
CONTROLSS_ADC3_CFG	502C 3058h
CONTROLSS_ADC4_CFG	502C 4058h

Figure 3-31. ADCSOC14CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
R					R/W							R/W			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
R/W	R							R/W							
0	0							0							

Access Types Legend

Table 3-64. ADCSOC14CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	R		Reserved
26 - 20	TRIGSEL	R/W	0h	SOC14 Trigger Source Select. Along with the SOC14 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC14 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	R/W	0h	SOC14 Channel Select. Selects the channel to be converted when SOC14 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	R		Reserved
8 - 0	ACQPS	R/W	0h	SOC14 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

3.2.33 CONTROLSS_ADCn_CFG_ADCSOC15CTL Registers

3.2.33.1 ADCn_CFG_ADCSOC15CTL Register (Offset = 5Ch) [reset = h]

Short Description: ADC SOC15 Control Register

Long Description:

Return to Summary Table

Table 3-65. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 005Ch
CONTROLSS_ADC1_CFG	502C 105Ch
CONTROLSS_ADC2_CFG	502C 205Ch
CONTROLSS_ADC3_CFG	502C 305Ch
CONTROLSS_ADC4_CFG	502C 405Ch

Figure 3-32. ADCSOC15CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
R					R/W							R/W			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
R/W	R							R/W							
0	0							0							

Access Types Legend

Table 3-66. ADCSOC15CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	R		Reserved
26 - 20	TRIGSEL	R/W	0h	SOC15 Trigger Source Select. Along with the SOC15 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC15 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	R/W	0h	SOC15 Channel Select. Selects the channel to be converted when SOC15 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	R		Reserved
8 - 0	ACQPS	R/W	0h	SOC15 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device data sheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

3.2.34 CONTROLSS_ADCn_CFG_ADCEVTSTAT Registers

3.2.34.1 ADCn_CFG_ADCEVTSTAT Register (Offset = 60h) [reset = h]

Short Description: ADC Event Status Register

Long Description:

Return to Summary Table

Table 3-67. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0060h
CONTROLSS_ADC1_CFG	502C 1060h
CONTROLSS_ADC2_CFG	502C 2060h
CONTROLSS_ADC3_CFG	502C 3060h
CONTROLSS_ADC4_CFG	502C 4060h

Figure 3-33. ADCEVTSTAT Name Register

15	14	13	12	11	10	9	8
RESERVED	PPB4ZER	PPB4TRIPLO	PPB4TRIPHI	RESERVED	PPB3ZER	PPB3TRIPLO	PPB3TRIPHI
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
RESERVED	PPB2ZER	PPB2TRIPLO	PPB2TRIPHI	RESERVED	PPB1ZER	PPB1TRIPLO	PPB1TRIPHI
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-68. ADCEVTSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R		Reserved
14	PPB4ZER	R	0h	Post Processing Block 4 Zero Crossing Flag. When set indicates the ADCPPB4RESULT register has changed sign. This bit is gated by EOC signal.
13	PPB4TRIPLO	R	0h	Post Processing Block 4 Trip Low Flag. When set indicates a digital compare trip low event has occurred.
12	PPB4TRIPHI	R	0h	Post Processing Block 4 Trip High Flag. When set indicates a digital compare trip high event has occurred.
11	RESERVED	R		Reserved
10	PPB3ZER	R	0h	Post Processing Block 3 Zero Crossing Flag. When set indicates the ADCPPB3RESULT register has changed sign. This bit is gated by EOC signal.
9	PPB3TRIPLO	R	0h	Post Processing Block 3 Trip Low Flag. When set indicates a digital compare trip low event has occurred.
8	PPB3TRIPHI	R	0h	Post Processing Block 3 Trip High Flag. When set indicates a digital compare trip high event has occurred.
7	RESERVED	R		Reserved
6	PPB2ZER	R	0h	Post Processing Block 2 Zero Crossing Flag. When set indicates the ADCPPB2RESULT register has changed sign. This bit is gated by EOC signal.
5	PPB2TRIPLO	R	0h	Post Processing Block 2 Trip Low Flag. When set indicates a digital compare trip low event has occurred.
4	PPB2TRIPHI	R	0h	Post Processing Block 2 Trip High Flag. When set indicates a digital compare trip high event has occurred.

Table 3-68. ADCEVTSTAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	R		Reserved
2	PPB1ZER	R	0h	Post Processing Block 1 Zero Crossing Flag. When set indicates the ADCPPB1RESULT register has changed sign. This bit is gated by EOC signal.
1	PPB1TRIPLO	R	0h	Post Processing Block 1 Trip Low Flag. When set indicates a digital compare trip low event has occurred.
0	PPB1TRIPHI	R	0h	Post Processing Block 1 Trip High Flag. When set indicates a digital compare trip high event has occurred.

3.2.35 CONTROLSS_ADCn_CFG_ADCEVTCLR Registers

3.2.35.1 ADCn_CFG_ADCEVTCLR Register (Offset = 64h) [reset = h]

Short Description: ADC Event Clear Register

Long Description:

Return to Summary Table

Table 3-69. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0064h
CONTROLSS_ADC1_CFG	502C 1064h
CONTROLSS_ADC2_CFG	502C 2064h
CONTROLSS_ADC3_CFG	502C 3064h
CONTROLSS_ADC4_CFG	502C 4064h

Figure 3-34. ADCEVTCLR Name Register

15	14	13	12	11	10	9	8
RESERVED	PPB4ZER	PPB4TRIPLO	PPB4TRIPHI	RESERVED	PPB3ZER	PPB3TRIPLO	PPB3TRIPHI
R	R-0/W	R-0/W	R-0/W	R	R-0/W	R-0/W	R-0/W
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
RESERVED	PPB2ZER	PPB2TRIPLO	PPB2TRIPHI	RESERVED	PPB1ZER	PPB1TRIPLO	PPB1TRIPHI
R	R-0/W	R-0/W	R-0/W	R	R-0/W	R-0/W	R-0/W
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-70. ADCEVTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R		Reserved
14	PPB4ZER	R-0/W	0h	Post Processing Block 4 Zero Crossing Clear. Clears the corresponding zero crossing flag in the ADCEVTSTAT register.
13	PPB4TRIPLO	R-0/W	0h	Post Processing Block 4 Trip Low Clear. Clears the corresponding trip low flag in the ADCEVTSTAT register.
12	PPB4TRIPHI	R-0/W	0h	Post Processing Block 4 Trip High Clear. Clears the corresponding trip high flag in the ADCEVTSTAT register.
11	RESERVED	R		Reserved
10	PPB3ZER	R-0/W	0h	Post Processing Block 3 Zero Crossing Clear. Clears the corresponding zero crossing flag in the ADCEVTSTAT register.
9	PPB3TRIPLO	R-0/W	0h	Post Processing Block 3 Trip Low Clear. Clears the corresponding trip low flag in the ADCEVTSTAT register.
8	PPB3TRIPHI	R-0/W	0h	Post Processing Block 3 Trip High Clear. Clears the corresponding trip high flag in the ADCEVTSTAT register.
7	RESERVED	R		Reserved
6	PPB2ZER	R-0/W	0h	Post Processing Block 2 Zero Crossing Clear. Clears the corresponding zero crossing flag in the ADCEVTSTAT register.
5	PPB2TRIPLO	R-0/W	0h	Post Processing Block 2 Trip Low Clear. Clears the corresponding trip low flag in the ADCEVTSTAT register.
4	PPB2TRIPHI	R-0/W	0h	Post Processing Block 2 Trip High Clear. Clears the corresponding trip high flag in the ADCEVTSTAT register.
3	RESERVED	R		Reserved
2	PPB1ZER	R-0/W	0h	Post Processing Block 1 Zero Crossing Clear. Clears the corresponding zero crossing flag in the ADCEVTSTAT register.

Table 3-70. ADCEVTCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	PPB1TRIPLO	R-0/W	0h	Post Processing Block 1 Trip Low Clear. Clears the corresponding trip low flag in the ADCEVTSTAT register.
0	PPB1TRIPHI	R-0/W	0h	Post Processing Block 1 Trip High Clear. Clears the corresponding trip high flag in the ADCEVTSTAT register.

3.2.36 CONTROLSS_ADCn_CFG_ADCEVTSEL Registers

3.2.36.1 ADCn_CFG_ADCEVTSEL Register (Offset = 68h) [reset = h]

Short Description: ADC Event Selection Register

Long Description:

Return to Summary Table

Table 3-71. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0068h
CONTROLSS_ADC1_CFG	502C 1068h
CONTROLSS_ADC2_CFG	502C 2068h
CONTROLSS_ADC3_CFG	502C 3068h
CONTROLSS_ADC4_CFG	502C 4068h

Figure 3-35. ADCEVTSEL Name Register

15	14	13	12	11	10	9	8
RESERVED	PPB4ZER	PPB4TRIPLO	PPB4TRIPHI	RESERVED	PPB3ZER	PPB3TRIPLO	PPB3TRIPHI
R	R/W	R/W	R/W	R	R/W	R/W	R/W
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
RESERVED	PPB2ZER	PPB2TRIPLO	PPB2TRIPHI	RESERVED	PPB1ZER	PPB1TRIPLO	PPB1TRIPHI
R	R/W	R/W	R/W	R	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-72. ADCEVTSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R		Reserved
14	PPB4ZER	R/W	0h	Post Processing Block 4 Zero Crossing Event Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
13	PPB4TRIPLO	R/W	0h	Post Processing Block 4 Trip Low Event Enable. Setting this bit allows the corresponding rising trip low flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
12	PPB4TRIPHI	R/W	0h	Post Processing Block 4 Trip High Event Enable. Setting this bit allows the corresponding rising trip high flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
11	RESERVED	R		Reserved
10	PPB3ZER	R/W	0h	Post Processing Block 3 Zero Crossing Event Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
9	PPB3TRIPLO	R/W	0h	Post Processing Block 3 Trip Low Event Enable. Setting this bit allows the corresponding rising trip low flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
8	PPB3TRIPHI	R/W	0h	Post Processing Block 3 Trip High Event Enable. Setting this bit allows the corresponding rising trip high flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.

Table 3-72. ADCEVTSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	RESERVED	R		Reserved
6	PPB2ZER	R/W	0h	Post Processing Block 2 Zero Crossing Event Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
5	PPB2TRIPLO	R/W	0h	Post Processing Block 2 Trip Low Event Enable. Setting this bit allows the corresponding rising trip low flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
4	PPB2TRIPHI	R/W	0h	Post Processing Block 2 Trip High Event Enable. Setting this bit allows the corresponding rising trip high flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
3	RESERVED	R		Reserved
2	PPB1ZER	R/W	0h	Post Processing Block 1 Zero Crossing Event Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
1	PPB1TRIPLO	R/W	0h	Post Processing Block 1 Trip Low Event Enable. Setting this bit allows the corresponding rising trip low flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
0	PPB1TRIPHI	R/W	0h	Post Processing Block 1 Trip High Event Enable. Setting this bit allows the corresponding rising trip high flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.

3.2.37 CONTROLSS_ADCn_CFG_ADCEVTINTSEL Registers

3.2.37.1 ADCn_CFG_ADCEVTINTSEL Register (Offset = 6Ch) [reset = h]

Short Description: ADC Event Interrupt Selection Register

Long Description:

Return to Summary Table

Table 3-73. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 006Ch
CONTROLSS_ADC1_CFG	502C 106Ch
CONTROLSS_ADC2_CFG	502C 206Ch
CONTROLSS_ADC3_CFG	502C 306Ch
CONTROLSS_ADC4_CFG	502C 406Ch

Figure 3-36. ADCEVTINTSEL Name Register

15	14	13	12	11	10	9	8
RESERVED	PPB4ZER	PPB4TRIPLO	PPB4TRIPHI	RESERVED	PPB3ZER	PPB3TRIPLO	PPB3TRIPHI
R	R/W	R/W	R/W	R	R/W	R/W	R/W
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
RESERVED	PPB2ZER	PPB2TRIPLO	PPB2TRIPHI	RESERVED	PPB1ZER	PPB1TRIPLO	PPB1TRIPHI
R	R/W	R/W	R/W	R	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-74. ADCEVTINTSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R		Reserved
14	PPB4ZER	R/W	0h	Post Processing Block 4 Zero Crossing Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
13	PPB4TRIPLO	R/W	0h	Post Processing Block 4 Trip Low Interrupt Enable. Setting this bit allows the corresponding rising trip low flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
12	PPB4TRIPHI	R/W	0h	Post Processing Block 4 Trip High Interrupt Enable. Setting this bit allows the corresponding rising trip high flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
11	RESERVED	R		Reserved
10	PPB3ZER	R/W	0h	Post Processing Block 3 Zero Crossing Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
9	PPB3TRIPLO	R/W	0h	Post Processing Block 3 Trip Low Interrupt Enable. Setting this bit allows the corresponding rising trip low flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
8	PPB3TRIPHI	R/W	0h	Post Processing Block 3 Trip High Interrupt Enable. Setting this bit allows the corresponding rising trip high flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.

Table 3-74. ADCEVTINTSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	RESERVED	R		Reserved
6	PPB2ZER	R/W	0h	Post Processing Block 2 Zero Crossing Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
5	PPB2TRIPLO	R/W	0h	Post Processing Block 2 Trip Low Interrupt Enable. Setting this bit allows the corresponding rising trip low flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
4	PPB2TRIPHI	R/W	0h	Post Processing Block 2 Trip High Interrupt Enable. Setting this bit allows the corresponding rising trip high flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
3	RESERVED	R		Reserved
2	PPB1ZER	R/W	0h	Post Processing Block 1 Zero Crossing Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
1	PPB1TRIPLO	R/W	0h	Post Processing Block 1 Trip Low Interrupt Enable. Setting this bit allows the corresponding rising trip low flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
0	PPB1TRIPHI	R/W	0h	Post Processing Block 1 Trip High Interrupt Enable. Setting this bit allows the corresponding rising trip high flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.

3.2.38 CONTROLSS_ADCn_CFG_ADCOSDETECT Registers

3.2.38.1 ADCn_CFG_ADCOSDETECT Register (Offset = 70h) [reset = h]

Short Description: ADC Open and Shorts Detect Register

Long Description:

Return to Summary Table

Table 3-75. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0070h
CONTROLSS_ADC1_CFG	502C 1070h
CONTROLSS_ADC2_CFG	502C 2070h
CONTROLSS_ADC3_CFG	502C 3070h
CONTROLSS_ADC4_CFG	502C 4070h

Figure 3-37. ADCOSDETECT Name Register

15	14	13	12	11	10	9	8
RESERVED							
R							
0							
7	6	5	4	3	2	1	0
RESERVED						DETECTCFG	
R						R/W	
0						0	

Access Types Legend

Table 3-76. ADCOSDETECT Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 3	RESERVED	R		Reserved
2 - 0	DETECTCFG	R/W	0h	ADC Opens and Shorts Detect Configuration. This bit field defines the open/shorts detection circuit state. 0h Open/Shorts detection circuit is disabled. 1h Open/Shorts detection circuit is enabled at zero scale. 2h Open/Shorts detection circuit is enabled at full scale. 3h Open/Shorts detection circuit is enabled at (nominal) 5/12 scale. 4h Open/Shorts detection circuit is enabled at (nominal) 7/12 scale. 5h Open/Shorts detection circuit is enabled with a (nominal) 5K pulldown to VSSA. 6h Open/Shorts detection circuit is enabled with a (nominal) 5K pullup to VDDA. 7h Open/Shorts detection circuit is enabled with a (nominal) 7K pulldown to VSSA.

3.2.39 CONTROLSS_ADCn_CFG_ADCCOUNTER Registers

3.2.39.1 ADCn_CFG_ADCCOUNTER Register (Offset = 72h) [reset = h]

Short Description: ADC Counter Register

Long Description:

Return to Summary Table

Table 3-77. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0072h
CONTROLSS_ADC1_CFG	502C 1072h
CONTROLSS_ADC2_CFG	502C 2072h
CONTROLSS_ADC3_CFG	502C 3072h
CONTROLSS_ADC4_CFG	502C 4072h

Figure 3-38. ADCCOUNTER Name Register

15	14	13	12	11	10	9	8
RESERVED				FREECOUNT			
R				R			
0				0			
7	6	5	4	3	2	1	0
FREECOUNT							
R							
0							

Access Types Legend

Table 3-78. ADCCOUNTER Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	R		Reserved
11 - 0	FREECOUNT	R	0h	ADC Free Running Counter Value. This bit field reflects the status of the free running ADC counter.

3.2.40 CONTROLSS_ADCn_CFG_ADCREV Registers

3.2.40.1 ADCn_CFG_ADCREV Register (Offset = 74h) [reset = h]

Short Description: ADC Revision Register

Long Description:

Return to Summary Table

Table 3-79. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0074h
CONTROLSS_ADC1_CFG	502C 1074h
CONTROLSS_ADC2_CFG	502C 2074h
CONTROLSS_ADC3_CFG	502C 3074h
CONTROLSS_ADC4_CFG	502C 4074h

Figure 3-39. ADCREV Name Register

15	14	13	12	11	10	9	8
REV							
R							
1							
7	6	5	4	3	2	1	0
TYPE							
R							
101							

Access Types Legend

Table 3-80. ADCREV Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	REV	R	1h	ADC Revision. To allow documentation of differences between revisions. First version is labeled as 00h.
7 - 0	TYPE	R	5h	ADC Type. Always set to 5 for this ADC.

3.2.41 CONTROLSS_ADCn_CFG_ADCOFFTRIM Registers

3.2.41.1 ADCn_CFG_ADCOFFTRIM Register (Offset = 76h) [reset = h]

Short Description: ADC Offset Trim Register

Long Description:

Return to Summary Table

Table 3-81. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0076h
CONTROLSS_ADC1_CFG	502C 1076h
CONTROLSS_ADC2_CFG	502C 2076h
CONTROLSS_ADC3_CFG	502C 3076h
CONTROLSS_ADC4_CFG	502C 4076h

Figure 3-40. ADCOFFTRIM Name Register

15	14	13	12	11	10	9	8
RESERVED							
R							
0							
7	6	5	4	3	2	1	0
OFFTRIM							
R/W							
0							

Access Types Legend

Table 3-82. ADCOFFTRIM Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	R		Reserved
7 - 0	OFFTRIM	R/W	0h	ADC Offset Trim Adjusts the conversion results of the converter up or down to account for offset error in the ADC. A factory trim setting will be loaded during device boot. Offset can be corrected in the range of +7 to -8 LSBs. Value is 16*Offset in 8-bit 2's complement: 7 LSB (16*7) = 112 6 LSB (16*6) = 96 5 LSB (16*5) = 80 4 LSB (16*4) = 64 3 LSB (16*3) = 48 2 LSB (16*2) = 32 1 LSB (16*1) = 16 0 LSB (16*0) = 0 -1 LSB (16*(-1)) = 240 : : -7LSB(16*(-7)) = 144

3.2.42 CONTROLSS_ADCn_CFG_ADCCONFIG Registers

3.2.42.1 ADCn_CFG_ADCCONFIG Register (Offset = 7Ch) [reset = h]

Short Description: ADC Config Register

Long Description:

Return to Summary Table

Table 3-83. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 007Ch
CONTROLSS_ADC1_CFG	502C 107Ch
CONTROLSS_ADC2_CFG	502C 207Ch
CONTROLSS_ADC3_CFG	502C 307Ch
CONTROLSS_ADC4_CFG	502C 407Ch

Figure 3-41. ADCCONFIG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CONFIG															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONFIG															
R/W															
0															

Access Types Legend

Table 3-84. ADCCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CONFIG	R/W	0h	ADC Configuration. This bit field is used for TI internal testing/ debugging.

3.2.43 CONTROLSS_ADCn_CFG_ADCPPB1CONFIG Registers

3.2.43.1 ADCn_CFG_ADCPPB1CONFIG Register (Offset = 80h) [reset = h]

Short Description: ADC PPB1 Config Register

Long Description:

Return to Summary Table

Table 3-85. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0080h
CONTROLSS_ADC1_CFG	502C 1080h
CONTROLSS_ADC2_CFG	502C 2080h
CONTROLSS_ADC3_CFG	502C 3080h
CONTROLSS_ADC4_CFG	502C 4080h

Figure 3-42. ADCPPB1CONFIG Name Register

15	14	13	12	11	10	9	8
RESERVED							
R							
0							
7	6	5	4	3	2	1	0
RESERVED		CBCEN	TWOSCOMPEN	CONFIG			
R		R/W	R/W	R/W			
0		0	0	0			

Access Types Legend

Table 3-86. ADCPPB1CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 6	RESERVED	R		Reserved
5	CBCEN	R/W	0h	ADC Post Processing Block Cycle By Cycle Enable. When set, this bit enables the post conversion hardware processing circuit to automatically clear the ADCEVTSTAT on a conversion if the event condition is no longer present.
4	TWOSCOMPEN	R/W	0h	ADC Post Processing Block 1 Two's Complement Enable. When set this bit enables the post conversion hardware processing circuit that performs a two's complement on the output of the offset/reference subtraction unit before storing the result in the ADCPPB1RESULT register. 0 ADCPPB1RESULT = ADCRESULTx - ADCPPB1OFFREF 1 ADCPPB1RESULT = ADCPPB1OFFREF - ADCRESULTx

Table 3-86. ADCPPB1CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	CONFIG	R/W	0h	ADC Post Processing Block 1 Configuration. This bit field defines which SOC/EOC/RESULT is assocatied with this post processing block. 0000 SOC0/EOC0/RESULT0 is associated with post processing block 1 0001 SOC1/EOC1/RESULT1 is associated with post processing block 1 0010 SOC2/EOC2/RESULT2 is associated with post processing block 1 0011 SOC3/EOC3/RESULT3 is associated with post processing block 1 0100 SOC4/EOC4/RESULT4 is associated with post processing block 1 0101 SOC5/EOC5/RESULT5 is associated with post processing block 1 0110 SOC6/EOC6/RESULT6 is associated with post processing block 1 0111 SOC7/EOC7/RESULT7 is associated with post processing block 1 1000 SOC8/EOC8/RESULT8 is associated with post processing block 1 1001 SOC9/EOC9/RESULT9 is associated with post processing block 1 1010 SOC10/EOC10/RESULT10 is associated with post processing block 1 1011 SOC11/EOC11/RESULT11 is associated with post processing block 1 1100 SOC12/EOC12/RESULT12 is associated with post processing block 1 1101 SOC13/EOC13/RESULT13 is associated with post processing block 1 1110 SOC14/EOC14/RESULT14 is associated with post processing block 1 1111 SOC15/EOC15/RESULT15 is associated with post processing block 1

3.2.44 CONTROLSS_ADCn_CFG_ADCPPB1STAMP Registers

3.2.44.1 ADCn_CFG_ADCPPB1STAMP Register (Offset = 82h) [reset = h]

Short Description: ADC PPB1 Sample Delay Time Stamp Register

Long Description:

Return to Summary Table

Table 3-87. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0082h
CONTROLSS_ADC1_CFG	502C 1082h
CONTROLSS_ADC2_CFG	502C 2082h
CONTROLSS_ADC3_CFG	502C 3082h
CONTROLSS_ADC4_CFG	502C 4082h

Figure 3-43. ADCPPB1STAMP Name Register

15	14	13	12	11	10	9	8
RESERVED				DLYSTAMP			
R				R			
0				0			
7	6	5	4	3	2	1	0
DLYSTAMP							
R							
0							

Access Types Legend

Table 3-88. ADCPPB1STAMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	R		Reserved
11 - 0	DLYSTAMP	R	0h	ADC Post Processing Block 1 Delay Time Stamp. When an SOC starts sampling the value contained in REQSTAMP is subtracted from the value in ADCCOUNTER.FREECOUNT and loaded into this bit field, thereby giving the number of system clock cycles delay between the SOC trigger and the actual start of the sample.

3.2.45 CONTROLSS_ADCn_CFG_ADCPPB1OFFCAL Registers

3.2.45.1 ADCn_CFG_ADCPPB1OFFCAL Register (Offset = 84h) [reset = h]

Short Description: ADC PPB1 Offset Calibration Register

Long Description:

Return to Summary Table

Table 3-89. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0084h
CONTROLSS_ADC1_CFG	502C 1084h
CONTROLSS_ADC2_CFG	502C 2084h
CONTROLSS_ADC3_CFG	502C 3084h
CONTROLSS_ADC4_CFG	502C 4084h

Figure 3-44. ADCPPB1OFFCAL Name Register

15	14	13	12	11	10	9	8
RESERVED						OFFCAL	
R						R/W	
0						0	
7	6	5	4	3	2	1	0
OFFCAL							
R/W							
0							

Access Types Legend

Table 3-90. ADCPPB1OFFCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	R		Reserved
9 - 0	OFFCAL	R/W	0h	ADC Post Processing Block 1 Offset Correction. This bit field can be used to digitally remove any system level offset inherent in the ADCIN circuit. This 10-bit signed value is subtracted from the ADC output before being stored in the ADCRESULT register. 000h No change. The ADC output is stored directly into ADCRESULT. 001h ADC output - 1 is stored into ADCRESULT. 002h ADC output - 2 is stored into ADCRESULT. ... 200h ADC output + 512 is stored into ADCRESULT. ... 3FFh ADC output + 1 is stored into ADCRESULT. NOTE: In 16-bit mode, the subtraction will saturate at 0000h and FFFFh before being stored into the ADCRESULT register. In 12-bit mode, the subtraction will saturate at 0000h and 0FFFh before being stored into the ADCRESULT register.

3.2.46 CONTROLSS_ADCn_CFG_ADCPPB1OFFREF Registers

3.2.46.1 ADCn_CFG_ADCPPB1OFFREF Register (Offset = 86h) [reset = h]

Short Description: ADC PPB1 Offset Reference Register

Long Description:

Return to Summary Table

Table 3-91. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0086h
CONTROLSS_ADC1_CFG	502C 1086h
CONTROLSS_ADC2_CFG	502C 2086h
CONTROLSS_ADC3_CFG	502C 3086h
CONTROLSS_ADC4_CFG	502C 4086h

Figure 3-45. ADCPPB1OFFREF Name Register

15	14	13	12	11	10	9	8
OFFREF							
R/W							
0							
7	6	5	4	3	2	1	0
OFFREF							
R/W							
0							

Access Types Legend

Table 3-92. ADCPPB1OFFREF Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	OFFREF	R/W	0h	ADC Post Processing Block 1 Offset Correction. This bit field can be used to either calculate the feedback error or convert a unipolar signal to bipolar by subtracting a reference value. This 16-bit unsigned value is subtracted from the ADCRESULT register before being passed through an optional two's complement function and stored in the ADCPPB1RESULT register. This subtraction is not saturated. 0000h No change. The ADCRESULT value is passed on. 0001h ADCRESULT - 1 is passed on. 0002h ADCRESULT - 2 is passed on. ... 8000h ADCRESULT - 32,768 is passed on. ... FFFFh ADCRESULT - 65,535 is passed on. NOTE: In 12-bit mode the size of this register does not change from 16-bits. It is the user's responsibility to ensure that only a 12-bit value is written to this register when in 12-bit mode.

3.2.47 CONTROLSS_ADCn_CFG_ADCPPB1TRIPHI Registers

3.2.47.1 ADCn_CFG_ADCPPB1TRIPHI Register (Offset = 88h) [reset = h]

Short Description: ADC PPB1 Trip High Register

Long Description:

Return to Summary Table

Table 3-93. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0088h
CONTROLSS_ADC1_CFG	502C 1088h
CONTROLSS_ADC2_CFG	502C 2088h
CONTROLSS_ADC3_CFG	502C 3088h
CONTROLSS_ADC4_CFG	502C 4088h

Figure 3-46. ADCPPB1TRIPHI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															HSIGN
R															R/W
0															0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIMITHI															
R/W															
0															

Access Types Legend

Table 3-94. ADCPPB1TRIPHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 17	RESERVED	R		Reserved
16	HSIGN	R/W	0h	High Limit Sign Bit. This is the sign bit (17th bit) to the LIMITHI bit field when in 16-bit ADC mode.
15 - 0	LIMITHI	R/W	0h	ADC Post Processing Block 1 Trip High Limit. This value sets the digital comparator trip high limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB1RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRESULT bit field of the ADCPPB1RESULT register.

3.2.48 CONTROLSS_ADCn_CFG_ADCPPB1TRIPLO Registers

3.2.48.1 ADCn_CFG_ADCPPB1TRIPLO Register (Offset = 8Ch) [reset = h]

Short Description: ADC PPB1 Trip Low/Trigger Time Stamp Register

Long Description:

Return to Summary Table

Table 3-95. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 008Ch
CONTROLSS_ADC1_CFG	502C 108Ch
CONTROLSS_ADC2_CFG	502C 208Ch
CONTROLSS_ADC3_CFG	502C 308Ch
CONTROLSS_ADC4_CFG	502C 408Ch

Figure 3-47. ADCPPB1TRIPLO Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
REQSTAMP												RESERVED			LSIGN
R												R			R/W
0												0			0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIMITLO															
R/W															
0															

Access Types Legend

Table 3-96. ADCPPB1TRIPLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	REQSTAMP	R	0h	ADC Post Processing Block 1 Request Time Stamp. When a trigger sets the associated SOC flag in the ADCSOCFLG1 register the value of ADCCOUNTER.FREECOUNT is loaded into this bit field.
19 - 17	RESERVED	R		Reserved
16	LSIGN	R/W	0h	Low Limit Sign Bit. This is the sign bit (17th bit) to the LIMITLO bit field when in 16-bit ADC mode.
15 - 0	LIMITLO	R/W	0h	ADC Post Processing Block 1 Trip Low Limit. This value sets the digital comparator trip low limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB1RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRSULT bit field of the ADCPPB1RESULT register.

3.2.49 CONTROLSS_ADCn_CFG_ADCPPB2CONFIG Registers

3.2.49.1 ADCn_CFG_ADCPPB2CONFIG Register (Offset = 90h) [reset = h]

Short Description: ADC PPB2 Config Register

Long Description:

Return to Summary Table

Table 3-97. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0090h
CONTROLSS_ADC1_CFG	502C 1090h
CONTROLSS_ADC2_CFG	502C 2090h
CONTROLSS_ADC3_CFG	502C 3090h
CONTROLSS_ADC4_CFG	502C 4090h

Figure 3-48. ADCPPB2CONFIG Name Register

15	14	13	12	11	10	9	8
RESERVED							
R							
0							
7	6	5	4	3	2	1	0
RESERVED		CBCEN	TWOSCOMPEN	CONFIG			
R		R/W	R/W	R/W			
0		0	0	0			

Access Types Legend

Table 3-98. ADCPPB2CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 6	RESERVED	R		Reserved
5	CBCEN	R/W	0h	ADC Post Processing Block Cycle By Cycle Enable. When set, this bit enables the post conversion hardware processing circuit to automatically clear the ADCEVTSTAT on a conversion if the event condition is no longer present.
4	TWOSCOMPEN	R/W	0h	ADC Post Processing Block 2 Two's Complement Enable. When set this bit enables the post conversion hardware processing circuit that performs a two's complement on the output of the offset/reference subtraction unit before storing the result in the ADCPPB2RESULT register. 0 ADCPPB2RESULT = ADCRESULTx - ADCPPB2OFFREF 1 ADCPPB2RESULT = ADCPPB2OFFREF - ADCRESULTx

Table 3-98. ADCPPB2CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	CONFIG	R/W	0h	ADC Post Processing Block 2 Configuration. This bit field defines which SOC/EOC/RESULT is assocatied with this post processing block. 0000 SOC0/EOC0/RESULT0 is associated with post processing block 2 0001 SOC1/EOC1/RESULT1 is associated with post processing block 2 0010 SOC2/EOC2/RESULT2 is associated with post processing block 2 0011 SOC3/EOC3/RESULT3 is associated with post processing block 2 0100 SOC4/EOC4/RESULT4 is associated with post processing block 2 0101 SOC5/EOC5/RESULT5 is associated with post processing block 2 0110 SOC6/EOC6/RESULT6 is associated with post processing block 2 0111 SOC7/EOC7/RESULT7 is associated with post processing block 2 1000 SOC8/EOC8/RESULT8 is associated with post processing block 2 1001 SOC9/EOC9/RESULT9 is associated with post processing block 2 1010 SOC10/EOC10/RESULT10 is associated with post processing block 2 1011 SOC11/EOC11/RESULT11 is associated with post processing block 2 1100 SOC12/EOC12/RESULT12 is associated with post processing block 2 1101 SOC13/EOC13/RESULT13 is associated with post processing block 2 1110 SOC14/EOC14/RESULT14 is associated with post processing block 2 1111 SOC15/EOC15/RESULT15 is associated with post processing block 2

3.2.50 CONTROLSS_ADCn_CFG_ADCPPB2STAMP Registers

3.2.50.1 ADCn_CFG_ADCPPB2STAMP Register (Offset = 92h) [reset = h]

Short Description: ADC PPB2 Sample Delay Time Stamp Register

Long Description:

Return to Summary Table

Table 3-99. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0092h
CONTROLSS_ADC1_CFG	502C 1092h
CONTROLSS_ADC2_CFG	502C 2092h
CONTROLSS_ADC3_CFG	502C 3092h
CONTROLSS_ADC4_CFG	502C 4092h

Figure 3-49. ADCPPB2STAMP Name Register

15	14	13	12	11	10	9	8
RESERVED				DLYSTAMP			
R				R			
0				0			
7	6	5	4	3	2	1	0
DLYSTAMP							
R							
0							

Access Types Legend

Table 3-100. ADCPPB2STAMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	R		Reserved
11 - 0	DLYSTAMP	R	0h	ADC Post Processing Block 2 Delay Time Stamp. When an SOC starts sampling the value contained in REQSTAMP is subtracted from the value in ADCCOUNTER.FREECOUNT and loaded into this bit field, thereby giving the number of system clock cycles delay between the SOC trigger and the actual start of the sample.

3.2.51 CONTROLSS_ADCn_CFG_ADCPPB2OFFCAL Registers

3.2.51.1 ADCn_CFG_ADCPPB2OFFCAL Register (Offset = 94h) [reset = h]

Short Description: ADC PPB2 Offset Calibration Register

Long Description:

Return to Summary Table

Table 3-101. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0094h
CONTROLSS_ADC1_CFG	502C 1094h
CONTROLSS_ADC2_CFG	502C 2094h
CONTROLSS_ADC3_CFG	502C 3094h
CONTROLSS_ADC4_CFG	502C 4094h

Figure 3-50. ADCPPB2OFFCAL Name Register

15	14	13	12	11	10	9	8
RESERVED						OFFCAL	
R						R/W	
0						0	
7	6	5	4	3	2	1	0
OFFCAL							
R/W							
0							

Access Types Legend

Table 3-102. ADCPPB2OFFCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	R		Reserved
9 - 0	OFFCAL	R/W	0h	ADC Post Processing Block 2 Offset Correction. This bit field can be used to digitally remove any system level offset inherent in the ADCIN circuit. This 10-bit signed value is subtracted from the ADC output before being stored in the ADCRESULT register. 000h No change. The ADC output is stored directly into ADCRESULT. 001h ADC output - 1 is stored into ADCRESULT. 002h ADC output - 2 is stored into ADCRESULT. ... 200h ADC output + 512 is stored into ADCRESULT. ... 3FFh ADC output + 1 is stored into ADCRESULT. NOTE: In 16-bit mode, the subtraction will saturate at 0000h and FFFFh before being stored into the ADCRESULT register. In 12-bit mode, the subtraction will saturate at 0000h and 0FFFh before being stored into the ADCRESULT register.

3.2.52 CONTROLSS_ADCn_CFG_ADCPPB2OFFREF Registers

3.2.52.1 ADCn_CFG_ADCPPB2OFFREF Register (Offset = 96h) [reset = h]

Short Description: ADC PPB2 Offset Reference Register

Long Description:

Return to Summary Table

Table 3-103. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0096h
CONTROLSS_ADC1_CFG	502C 1096h
CONTROLSS_ADC2_CFG	502C 2096h
CONTROLSS_ADC3_CFG	502C 3096h
CONTROLSS_ADC4_CFG	502C 4096h

Figure 3-51. ADCPPB2OFFREF Name Register

15	14	13	12	11	10	9	8
OFFREF							
R/W							
0							
7	6	5	4	3	2	1	0
OFFREF							
R/W							
0							

Access Types Legend

Table 3-104. ADCPPB2OFFREF Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	OFFREF	R/W	0h	ADC Post Processing Block 2 Offset Correction. This bit field can be used to either calculate the feedback error or convert a unipolar signal to bipolar by subtracting a reference value. This 16-bit unsigned value is subtracted from the ADCRESULT register before being passed through an optional two's complement function and stored in the ADCPPB2RESULT register. This subtraction is not saturated. 0000h No change. The ADCRESULT value is passed on. 0001h ADCRESULT - 1 is passed on. 0002h ADCRESULT - 2 is passed on. ... 8000h ADCRESULT - 32,768 is passed on. ... FFFFh ADCRESULT - 65,535 is passed on. NOTE: In 12-bit mode the size of this register does not change from 16-bits. It is the user's responsibility to ensure that only a 12-bit value is written to this register when in 12-bit mode.

3.2.53 CONTROLSS_ADCn_CFG_ADCPPB2TRIPHI Registers

3.2.53.1 ADCn_CFG_ADCPPB2TRIPHI Register (Offset = 98h) [reset = h]

Short Description: ADC PPB2 Trip High Register

Long Description:

Return to Summary Table

Table 3-105. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0098h
CONTROLSS_ADC1_CFG	502C 1098h
CONTROLSS_ADC2_CFG	502C 2098h
CONTROLSS_ADC3_CFG	502C 3098h
CONTROLSS_ADC4_CFG	502C 4098h

Figure 3-52. ADCPPB2TRIPHI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															HSIGN
R															R/W
0															0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIMITHI															
R/W															
0															

Access Types Legend

Table 3-106. ADCPPB2TRIPHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 17	RESERVED	R		Reserved
16	HSIGN	R/W	0h	High Limit Sign Bit. This is the sign bit (17th bit) to the LIMITHI bit field when in 16-bit ADC mode.
15 - 0	LIMITHI	R/W	0h	ADC Post Processing Block 2 Trip High Limit. This value sets the digital comparator trip high limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB2RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRESULT bit field of the ADCPPB2RESULT register.

3.2.54 CONTROLSS_ADCn_CFG_ADCPPB2TRIPLO Registers

3.2.54.1 ADCn_CFG_ADCPPB2TRIPLO Register (Offset = 9Ch) [reset = h]

Short Description: ADC PPB2 Trip Low/Trigger Time Stamp Register

Long Description:

Return to Summary Table

Table 3-107. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 009Ch
CONTROLSS_ADC1_CFG	502C 109Ch
CONTROLSS_ADC2_CFG	502C 209Ch
CONTROLSS_ADC3_CFG	502C 309Ch
CONTROLSS_ADC4_CFG	502C 409Ch

Figure 3-53. ADCPPB2TRIPLO Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
REQSTAMP												RESERVED			LSIGN
R												R			R/W
0												0			0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIMITLO															
R/W															
0															

Access Types Legend

Table 3-108. ADCPPB2TRIPLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	REQSTAMP	R	0h	ADC Post Processing Block 2 Request Time Stamp. When a trigger sets the associated SOC flag in the ADCSOCFLG1 register the value of ADCCOUNTER.FREECOUNT is loaded into this bit field.
19 - 17	RESERVED	R		Reserved
16	LSIGN	R/W	0h	Low Limit Sign Bit. This is the sign bit (17th bit) to the LIMITLO bit field when in 16-bit ADC mode.
15 - 0	LIMITLO	R/W	0h	ADC Post Processing Block 2 Trip Low Limit. This value sets the digital comparator trip low limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB2RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRSULT bit field of the ADCPPB2RESULT register.

3.2.55 CONTROLSS_ADCn_CFG_ADCPPB3CONFIG Registers

3.2.55.1 ADCn_CFG_ADCPPB3CONFIG Register (Offset = A0h) [reset = h]

Short Description: ADC PPB3 Config Register

Long Description:

Return to Summary Table

Table 3-109. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00A0h
CONTROLSS_ADC1_CFG	502C 10A0h
CONTROLSS_ADC2_CFG	502C 20A0h
CONTROLSS_ADC3_CFG	502C 30A0h
CONTROLSS_ADC4_CFG	502C 40A0h

Figure 3-54. ADCPPB3CONFIG Name Register

15	14	13	12	11	10	9	8
RESERVED							
R							
0							
7	6	5	4	3	2	1	0
RESERVED		CBCEN	TWOSCOMPEN	CONFIG			
R		R/W	R/W	R/W			
0		0	0	0			

Access Types Legend

Table 3-110. ADCPPB3CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 6	RESERVED	R		Reserved
5	CBCEN	R/W	0h	ADC Post Processing Block Cycle By Cycle Enable. When set, this bit enables the post conversion hardware processing circuit to automatically clear the ADCEVTSTAT on a conversion if the event condition is no longer present.
4	TWOSCOMPEN	R/W	0h	ADC Post Processing Block 3 Two's Complement Enable. When set this bit enables the post conversion hardware processing circuit that performs a two's complement on the output of the offset/reference subtraction unit before storing the result in the ADCPPB3RESULT register. 0 ADCPPB3RESULT = ADCRESULTx - ADCPPB3OFFREF 1 ADCPPB3RESULT = ADCPPB3OFFREF - ADCRESULTx

Table 3-110. ADCPPB3CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	CONFIG	R/W	0h	ADC Post Processing Block 3 Configuration. This bit field defines which SOC/EOC/RESULT is assocatied with this post processing block. 0000 SOC0/EOC0/RESULT0 is associated with post processing block 3 0001 SOC1/EOC1/RESULT1 is associated with post processing block 3 0010 SOC2/EOC2/RESULT2 is associated with post processing block 3 0011 SOC3/EOC3/RESULT3 is associated with post processing block 3 0100 SOC4/EOC4/RESULT4 is associated with post processing block 3 0101 SOC5/EOC5/RESULT5 is associated with post processing block 3 0110 SOC6/EOC6/RESULT6 is associated with post processing block 3 0111 SOC7/EOC7/RESULT7 is associated with post processing block 3 1000 SOC8/EOC8/RESULT8 is associated with post processing block 3 1001 SOC9/EOC9/RESULT9 is associated with post processing block 3 1010 SOC10/EOC10/RESULT10 is associated with post processing block 3 1011 SOC11/EOC11/RESULT11 is associated with post processing block 3 1100 SOC12/EOC12/RESULT12 is associated with post processing block 3 1101 SOC13/EOC13/RESULT13 is associated with post processing block 3 1110 SOC14/EOC14/RESULT14 is associated with post processing block 3 1111 SOC15/EOC15/RESULT15 is associated with post processing block 3

3.2.56 CONTROLSS_ADCn_CFG_ADCPPB3STAMP Registers

3.2.56.1 ADCn_CFG_ADCPPB3STAMP Register (Offset = A2h) [reset = h]

Short Description: ADC PPB3 Sample Delay Time Stamp Register

Long Description:

Return to Summary Table

Table 3-111. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00A2h
CONTROLSS_ADC1_CFG	502C 10A2h
CONTROLSS_ADC2_CFG	502C 20A2h
CONTROLSS_ADC3_CFG	502C 30A2h
CONTROLSS_ADC4_CFG	502C 40A2h

Figure 3-55. ADCPPB3STAMP Name Register

15	14	13	12	11	10	9	8
RESERVED				DLYSTAMP			
R				R			
0				0			
7	6	5	4	3	2	1	0
DLYSTAMP							
R							
0							

Access Types Legend

Table 3-112. ADCPPB3STAMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	R		Reserved
11 - 0	DLYSTAMP	R	0h	ADC Post Processing Block 3 Delay Time Stamp. When an SOC starts sampling the value contained in REQSTAMP is subtracted from the value in ADCCOUNTER.FREECOUNT and loaded into this bit field, thereby giving the number of system clock cycles delay between the SOC trigger and the actual start of the sample.

3.2.57 CONTROLSS_ADCn_CFG_ADCPPB3OFFCAL Registers

3.2.57.1 ADCn_CFG_ADCPPB3OFFCAL Register (Offset = A4h) [reset = h]

Short Description: ADC PPB3 Offset Calibration Register

Long Description:

Return to Summary Table

Table 3-113. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00A4h
CONTROLSS_ADC1_CFG	502C 10A4h
CONTROLSS_ADC2_CFG	502C 20A4h
CONTROLSS_ADC3_CFG	502C 30A4h
CONTROLSS_ADC4_CFG	502C 40A4h

Figure 3-56. ADCPPB3OFFCAL Name Register

15	14	13	12	11	10	9	8
RESERVED						OFFCAL	
R						R/W	
0						0	
7	6	5	4	3	2	1	0
OFFCAL							
R/W							
0							

Access Types Legend

Table 3-114. ADCPPB3OFFCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	R		Reserved
9 - 0	OFFCAL	R/W	0h	ADC Post Processing Block 3 Offset Correction. This bit field can be used to digitally remove any system level offset inherent in the ADCIN circuit. This 10-bit signed value is subtracted from the ADC output before being stored in the ADCRESULT register. 000h No change. The ADC output is stored directly into ADCRESULT. 001h ADC output - 1 is stored into ADCRESULT. 002h ADC output - 2 is stored into ADCRESULT. ... 200h ADC output + 512 is stored into ADCRESULT. ... 3FFh ADC output + 1 is stored into ADCRESULT. NOTE: In 16-bit mode, the subtraction will saturate at 0000h and FFFFh before being stored into the ADCRESULT register. In 12-bit mode, the subtraction will saturate at 0000h and 0FFFh before being stored into the ADCRESULT register.

3.2.58 CONTROLSS_ADCn_CFG_ADCPPB3OFFREF Registers

3.2.58.1 ADCn_CFG_ADCPPB3OFFREF Register (Offset = A6h) [reset = h]

Short Description: ADC PPB3 Offset Reference Register

Long Description:

Return to Summary Table

Table 3-115. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00A6h
CONTROLSS_ADC1_CFG	502C 10A6h
CONTROLSS_ADC2_CFG	502C 20A6h
CONTROLSS_ADC3_CFG	502C 30A6h
CONTROLSS_ADC4_CFG	502C 40A6h

Figure 3-57. ADCPPB3OFFREF Name Register

15	14	13	12	11	10	9	8
OFFREF							
R/W							
0							
7	6	5	4	3	2	1	0
OFFREF							
R/W							
0							

Access Types Legend

Table 3-116. ADCPPB3OFFREF Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	OFFREF	R/W	0h	ADC Post Processing Block 3 Offset Correction. This bit field can be used to either calculate the feedback error or convert a unipolar signal to bipolar by subtracting a reference value. This 16-bit unsigned value is subtracted from the ADCRESULT register before being passed through an optional two's complement function and stored in the ADCPPB3RESULT register. This subtraction is not saturated. 0000h No change. The ADCRESULT value is passed on. 0001h ADCRESULT - 1 is passed on. 0002h ADCRESULT - 2 is passed on. ... 8000h ADCRESULT - 32,768 is passed on. ... FFFFh ADCRESULT - 65,535 is passed on. NOTE: In 12-bit mode the size of this register does not change from 16-bits. It is the user's responsibility to ensure that only a 12-bit value is written to this register when in 12-bit mode.

3.2.59 CONTROLSS_ADCn_CFG_ADCPPB3TRIPHI Registers

3.2.59.1 ADCn_CFG_ADCPPB3TRIPHI Register (Offset = A8h) [reset = h]

Short Description: ADC PPB3 Trip High Register

Long Description:

Return to Summary Table

Table 3-117. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00A8h
CONTROLSS_ADC1_CFG	502C 10A8h
CONTROLSS_ADC2_CFG	502C 20A8h
CONTROLSS_ADC3_CFG	502C 30A8h
CONTROLSS_ADC4_CFG	502C 40A8h

Figure 3-58. ADCPPB3TRIPHI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															HSIGN
R															R/W
0															0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIMITHI															
R/W															
0															

Access Types Legend

Table 3-118. ADCPPB3TRIPHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 17	RESERVED	R		Reserved
16	HSIGN	R/W	0h	High Limit Sign Bit. This is the sign bit (17th bit) to the LIMITHI bit field when in 16-bit ADC mode.
15 - 0	LIMITHI	R/W	0h	ADC Post Processing Block 3 Trip High Limit. This value sets the digital comparator trip high limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB3RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRESULT bit field of the ADCPPB3RESULT register.

3.2.60 CONTROLSS_ADCn_CFG_ADCPPB3TRIPLO Registers

3.2.60.1 ADCn_CFG_ADCPPB3TRIPLO Register (Offset = ACh) [reset = h]

Short Description: ADC PPB3 Trip Low/Trigger Time Stamp Register

Long Description:

Return to Summary Table

Table 3-119. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00ACh
CONTROLSS_ADC1_CFG	502C 10ACh
CONTROLSS_ADC2_CFG	502C 20ACh
CONTROLSS_ADC3_CFG	502C 30ACh
CONTROLSS_ADC4_CFG	502C 40ACh

Figure 3-59. ADCPPB3TRIPLO Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
REQSTAMP												RESERVED			LSIGN
R												R			R/W
0												0			0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIMITLO															
R/W															
0															

Access Types Legend

Table 3-120. ADCPPB3TRIPLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	REQSTAMP	R	0h	ADC Post Processing Block 3 Request Time Stamp. When a trigger sets the associated SOC flag in the ADCSOCFLG1 register the value of ADCCOUNTER.FREECOUNT is loaded into this bit field.
19 - 17	RESERVED	R		Reserved
16	LSIGN	R/W	0h	Low Limit Sign Bit. This is the sign bit (17th bit) to the LIMITLO bit field when in 16-bit ADC mode.
15 - 0	LIMITLO	R/W	0h	ADC Post Processing Block 3 Trip Low Limit. This value sets the digital comparator trip low limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB3RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRSULT bit field of the ADCPPB3RESULT register.

3.2.61 CONTROLSS_ADCn_CFG_ADCPPB4CONFIG Registers

3.2.61.1 ADCn_CFG_ADCPPB4CONFIG Register (Offset = B0h) [reset = h]

Short Description: ADC PPB4 Config Register

Long Description:

Return to Summary Table

Table 3-121. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00B0h
CONTROLSS_ADC1_CFG	502C 10B0h
CONTROLSS_ADC2_CFG	502C 20B0h
CONTROLSS_ADC3_CFG	502C 30B0h
CONTROLSS_ADC4_CFG	502C 40B0h

Figure 3-60. ADCPPB4CONFIG Name Register

15	14	13	12	11	10	9	8
RESERVED							
R							
0							
7	6	5	4	3	2	1	0
RESERVED		CBCEN	TWOSCOMPEN	CONFIG			
R		R/W	R/W	R/W			
0		0	0	0			

Access Types Legend

Table 3-122. ADCPPB4CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 6	RESERVED	R		Reserved
5	CBCEN	R/W	0h	ADC Post Processing Block Cycle By Cycle Enable. When set, this bit enables the post conversion hardware processing circuit to automatically clear the ADCEVTSTAT on a conversion if the event condition is no longer present.
4	TWOSCOMPEN	R/W	0h	ADC Post Processing Block 4 Two's Complement Enable. When set this bit enables the post conversion hardware processing circuit that performs a two's complement on the output of the offset/reference subtraction unit before storing the result in the ADCPPB4RESULT register. 0 ADCPPB4RESULT = ADCRESULTx - ADCPPB4OFFREF 1 ADCPPB4RESULT = ADCPPB4OFFREF - ADCRESULTx

Table 3-122. ADCPPB4CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	CONFIG	R/W	0h	ADC Post Processing Block 4 Configuration. This bit field defines which SOC/EOC/RESULT is assocatied with this post processing block. 0000 SOC0/EOC0/RESULT0 is associated with post processing block 4 0001 SOC1/EOC1/RESULT1 is associated with post processing block 4 0010 SOC2/EOC2/RESULT2 is associated with post processing block 4 0011 SOC3/EOC3/RESULT3 is associated with post processing block 4 0100 SOC4/EOC4/RESULT4 is associated with post processing block 4 0101 SOC5/EOC5/RESULT5 is associated with post processing block 4 0110 SOC6/EOC6/RESULT6 is associated with post processing block 4 0111 SOC7/EOC7/RESULT7 is associated with post processing block 4 1000 SOC8/EOC8/RESULT8 is associated with post processing block 4 1001 SOC9/EOC9/RESULT9 is associated with post processing block 4 1010 SOC10/EOC10/RESULT10 is associated with post processing block 4 1011 SOC11/EOC11/RESULT11 is associated with post processing block 4 1100 SOC12/EOC12/RESULT12 is associated with post processing block 4 1101 SOC13/EOC13/RESULT13 is associated with post processing block 4 1110 SOC14/EOC14/RESULT14 is associated with post processing block 4 1111 SOC15/EOC15/RESULT15 is associated with post processing block 4

3.2.62 CONTROLSS_ADCn_CFG_ADCPPB4STAMP Registers

3.2.62.1 ADCn_CFG_ADCPPB4STAMP Register (Offset = B2h) [reset = h]

Short Description: ADC PPB4 Sample Delay Time Stamp Register

Long Description:

Return to Summary Table

Table 3-123. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00B2h
CONTROLSS_ADC1_CFG	502C 10B2h
CONTROLSS_ADC2_CFG	502C 20B2h
CONTROLSS_ADC3_CFG	502C 30B2h
CONTROLSS_ADC4_CFG	502C 40B2h

Figure 3-61. ADCPPB4STAMP Name Register

15	14	13	12	11	10	9	8
RESERVED				DLYSTAMP			
R				R			
0				0			
7	6	5	4	3	2	1	0
DLYSTAMP							
R							
0							

Access Types Legend

Table 3-124. ADCPPB4STAMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	R		Reserved
11 - 0	DLYSTAMP	R	0h	ADC Post Processing Block 4 Delay Time Stamp. When an SOC starts sampling the value contained in REQSTAMP is subtracted from the value in ADCCOUNTER.FREECOUNT and loaded into this bit field, thereby giving the number of system clock cycles delay between the SOC trigger and the actual start of the sample.

3.2.63 CONTROLSS_ADCn_CFG_ADCPPB4OFFCAL Registers

3.2.63.1 ADCn_CFG_ADCPPB4OFFCAL Register (Offset = B4h) [reset = h]

Short Description: ADC PPB4 Offset Calibration Register

Long Description:

Return to Summary Table

Table 3-125. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00B4h
CONTROLSS_ADC1_CFG	502C 10B4h
CONTROLSS_ADC2_CFG	502C 20B4h
CONTROLSS_ADC3_CFG	502C 30B4h
CONTROLSS_ADC4_CFG	502C 40B4h

Figure 3-62. ADCPPB4OFFCAL Name Register

15	14	13	12	11	10	9	8
RESERVED						OFFCAL	
R						R/W	
0						0	
7	6	5	4	3	2	1	0
OFFCAL							
R/W							
0							

Access Types Legend

Table 3-126. ADCPPB4OFFCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	R		Reserved
9 - 0	OFFCAL	R/W	0h	ADC Post Processing Block 4 Offset Correction. This bit field can be used to digitally remove any system level offset inherent in the ADCIN circuit. This 10-bit signed value is subtracted from the ADC output before being stored in the ADCRESULT register. 000h No change. The ADC output is stored directly into ADCRESULT. 001h ADC output - 1 is stored into ADCRESULT. 002h ADC output - 2 is stored into ADCRESULT. ... 200h ADC output + 512 is stored into ADCRESULT. ... 3FFh ADC output + 1 is stored into ADCRESULT. NOTE: In 16-bit mode, the subtraction will saturate at 0000h and FFFFh before being stored into the ADCRESULT register. In 12-bit mode, the subtraction will saturate at 0000h and 0FFFh before being stored into the ADCRESULT register.

3.2.64 CONTROLSS_ADCn_CFG_ADCPPB4OFFREF Registers

3.2.64.1 ADCn_CFG_ADCPPB4OFFREF Register (Offset = B6h) [reset = h]

Short Description: ADC PPB4 Offset Reference Register

Long Description:

Return to Summary Table

Table 3-127. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00B6h
CONTROLSS_ADC1_CFG	502C 10B6h
CONTROLSS_ADC2_CFG	502C 20B6h
CONTROLSS_ADC3_CFG	502C 30B6h
CONTROLSS_ADC4_CFG	502C 40B6h

Figure 3-63. ADCPPB4OFFREF Name Register

15	14	13	12	11	10	9	8
OFFREF							
R/W							
0							
7	6	5	4	3	2	1	0
OFFREF							
R/W							
0							

Access Types Legend

Table 3-128. ADCPPB4OFFREF Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	OFFREF	R/W	0h	ADC Post Processing Block 4 Offset Correction. This bit field can be used to either calculate the feedback error or convert a unipolar signal to bipolar by subtracting a reference value. This 16-bit unsigned value is subtracted from the ADCRESULT register before being passed through an optional two's complement function and stored in the ADCPPB4RESULT register. This subtraction is not saturated. 0000h No change. The ADCRESULT value is passed on. 0001h ADCRESULT - 1 is passed on. 0002h ADCRESULT - 2 is passed on. ... 8000h ADCRESULT - 32,768 is passed on. ... FFFFh ADCRESULT - 65,535 is passed on. NOTE: In 12-bit mode the size of this register does not change from 16-bits. It is the user's responsibility to ensure that only a 12-bit value is written to this register when in 12-bit mode.

3.2.65 CONTROLSS_ADCn_CFG_ADCPPB4TRIPHI Registers

3.2.65.1 ADCn_CFG_ADCPPB4TRIPHI Register (Offset = B8h) [reset = h]

Short Description: ADC PPB4 Trip High Register

Long Description:

Return to Summary Table

Table 3-129. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00B8h
CONTROLSS_ADC1_CFG	502C 10B8h
CONTROLSS_ADC2_CFG	502C 20B8h
CONTROLSS_ADC3_CFG	502C 30B8h
CONTROLSS_ADC4_CFG	502C 40B8h

Figure 3-64. ADCPPB4TRIPHI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															HSIGN
R															R/W
0															0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIMITHI															
R/W															
0															

Access Types Legend

Table 3-130. ADCPPB4TRIPHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 17	RESERVED	R		Reserved
16	HSIGN	R/W	0h	High Limit Sign Bit. This is the sign bit (17th bit) to the LIMITHI bit field when in 16-bit ADC mode.
15 - 0	LIMITHI	R/W	0h	ADC Post Processing Block 4 Trip High Limit. This value sets the digital comparator trip high limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB4RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRESULT bit field of the ADCPPB4RESULT register.

3.2.66 CONTROLSS_ADCn_CFG_ADCPPB4TRIPLO Registers

3.2.66.1 ADCn_CFG_ADCPPB4TRIPLO Register (Offset = BCh) [reset = h]

Short Description: ADC PPB4 Trip Low/Trigger Time Stamp Register

Long Description:

Return to Summary Table

Table 3-131. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00BCh
CONTROLSS_ADC1_CFG	502C 10BCh
CONTROLSS_ADC2_CFG	502C 20BCh
CONTROLSS_ADC3_CFG	502C 30BCh
CONTROLSS_ADC4_CFG	502C 40BCh

Figure 3-65. ADCPPB4TRIPLO Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
REQSTAMP												RESERVED			LSIGN
R												R			R/W
0												0			0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIMITLO															
R/W															
0															

Access Types Legend

Table 3-132. ADCPPB4TRIPLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	REQSTAMP	R	0h	ADC Post Processing Block 4 Request Time Stamp. When a trigger sets the associated SOC flag in the ADCSOCFLG1 register the value of ADCCOUNTER.FREECOUNT is loaded into this bit field.
19 - 17	RESERVED	R		Reserved
16	LSIGN	R/W	0h	Low Limit Sign Bit. This is the sign bit (17th bit) to the LIMITLO bit field when in 16-bit ADC mode.
15 - 0	LIMITLO	R/W	0h	ADC Post Processing Block 4 Trip Low Limit. This value sets the digital comparator trip low limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB4RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRSULT bit field of the ADCPPB4RESULT register.

3.2.67 CONTROLSS_ADCn_CFG_ADCINTCYCLE Registers

3.2.67.1 ADCn_CFG_ADCINTCYCLE Register (Offset = DEh) [reset = h]

Short Description: ADC Early Interrupt Generation Cycle

Long Description:

Return to Summary Table

Table 3-133. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00DEh
CONTROLSS_ADC1_CFG	502C 10DEh
CONTROLSS_ADC2_CFG	502C 20DEh
CONTROLSS_ADC3_CFG	502C 30DEh
CONTROLSS_ADC4_CFG	502C 40DEh

Figure 3-66. ADCINTCYCLE Name Register

15	14	13	12	11	10	9	8
DELAY							
R/W							
0							
7	6	5	4	3	2	1	0
DELAY							
R/W							
0							

Access Types Legend

Table 3-134. ADCINTCYCLE Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	DELAY	R/W	0h	ADC Early Interrupt Generation Cycle Delay: Defines the delay from the fall edge of ADCSOC in terms of system clock cycles, for the interrupt to be generated.

3.2.68 CONTROLSS_ADCn_CFG_ADCINLTRIM1 Registers

3.2.68.1 ADCn_CFG_ADCINLTRIM1 Register (Offset = E0h) [reset = h]

Short Description: ADC Linearity Trim 1 Register

Long Description:

Return to Summary Table

Table 3-135. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00E0h
CONTROLSS_ADC1_CFG	502C 10E0h
CONTROLSS_ADC2_CFG	502C 20E0h
CONTROLSS_ADC3_CFG	502C 30E0h
CONTROLSS_ADC4_CFG	502C 40E0h

Figure 3-67. ADCINLTRIM1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INLTRIM31TO0															
R/W															
11000000111111111101110															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INLTRIM31TO0															
R/W															
11000000111111111101110															

Access Types Legend

Table 3-136. ADCINLTRIM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	INLTRIM31TO0	R/W	C0FFEEh	ADC Linearity Trim Bits 31-0. This register should not be modified unless specifically indicated by TI Errata or other documentation. Modifying the contents of this register could cause this module to operate outside of data sheet specifications.

3.2.69 CONTROLSS_ADCn_CFG_ADCINLTRIM2 Registers

3.2.69.1 ADCn_CFG_ADCINLTRIM2 Register (Offset = E4h) [reset = h]

Short Description: ADC Linearity Trim 2 Register

Long Description:

Return to Summary Table

Table 3-137. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00E4h
CONTROLSS_ADC1_CFG	502C 10E4h
CONTROLSS_ADC2_CFG	502C 20E4h
CONTROLSS_ADC3_CFG	502C 30E4h
CONTROLSS_ADC4_CFG	502C 40E4h

Figure 3-68. ADCINLTRIM2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INLTRIM63TO32															
R/W															
11000000111111111101110															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INLTRIM63TO32															
R/W															
11000000111111111101110															

Access Types Legend

Table 3-138. ADCINLTRIM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	INLTRIM63TO32	R/W	C0FFEEh	ADC Linearity Trim Bits 63-32. This register should not be modified unless specifically indicated by TI Errata or other documentation. Modifying the contents of this register could cause this module to operate outside of datasheet specifications.

3.2.70 CONTROLSS_ADCn_CFG_ADCINLTRIM3 Registers

3.2.70.1 ADCn_CFG_ADCINLTRIM3 Register (Offset = E8h) [reset = h]

Short Description: ADC Linearity Trim 3 Register

Long Description:

Return to Summary Table

Table 3-139. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00E8h
CONTROLSS_ADC1_CFG	502C 10E8h
CONTROLSS_ADC2_CFG	502C 20E8h
CONTROLSS_ADC3_CFG	502C 30E8h
CONTROLSS_ADC4_CFG	502C 40E8h

Figure 3-69. ADCINLTRIM3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INLTRIM95TO64															
R/W															
11000000111111111101110															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INLTRIM95TO64															
R/W															
11000000111111111101110															

Access Types Legend

Table 3-140. ADCINLTRIM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	INLTRIM95TO64	R/W	C0FFEEh	ADC Linearity Trim Bits 95-64. This register should not be modified unless specifically indicated by TI Errata or other documentation. Modifying the contents of this register could cause this module to operate outside of data sheet specifications.

3.2.71 CONTROLSS_ADCn_CFG_ADCINLTRIM4 Registers

3.2.71.1 ADCn_CFG_ADCINLTRIM4 Register (Offset = ECh) [reset = h]

Short Description: ADC Linearity Trim 4 Register

Long Description:

Return to Summary Table

Table 3-141. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00ECh
CONTROLSS_ADC1_CFG	502C 10ECh
CONTROLSS_ADC2_CFG	502C 20ECh
CONTROLSS_ADC3_CFG	502C 30ECh
CONTROLSS_ADC4_CFG	502C 40ECh

Figure 3-70. ADCINLTRIM4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INLTRIM127TO96															
R/W															
11000000111111111101110															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INLTRIM127TO96															
R/W															
11000000111111111101110															

Access Types Legend

Table 3-142. ADCINLTRIM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	INLTRIM127TO96	R/W	C0FFEEh	ADC Linearity Trim Bits 127-96. This register should not be modified unless specifically indicated by TI Errata or other documentation. Modifying the contents of this register could cause this module to operate outside of data sheet specifications.

3.2.72 CONTROLSS_ADCn_CFG_ADCINLTRIM5 Registers

3.2.72.1 ADCn_CFG_ADCINLTRIM5 Register (Offset = F0h) [reset = h]

Short Description: ADC Linearity Trim 5 Register

Long Description:

Return to Summary Table

Table 3-143. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00F0h
CONTROLSS_ADC1_CFG	502C 10F0h
CONTROLSS_ADC2_CFG	502C 20F0h
CONTROLSS_ADC3_CFG	502C 30F0h
CONTROLSS_ADC4_CFG	502C 40F0h

Figure 3-71. ADCINLTRIM5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INLTRIM159TO128															
R/W															
11000000111111111101110															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INLTRIM159TO128															
R/W															
11000000111111111101110															

Access Types Legend

Table 3-144. ADCINLTRIM5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	INLTRIM159TO128	R/W	C0FFEEh	ADC Linearity Trim Bits 159-128. This register should not be modified unless specifically indicated by TI Errata or other documentation. Modifying the contents of this register could cause this module to operate outside of data sheet specifications.

3.2.73 CONTROLSS_ADCn_CFG_ADCINLTRIM6 Registers

3.2.73.1 ADCn_CFG_ADCINLTRIM6 Register (Offset = F4h) [reset = h]

Short Description: ADC Linearity Trim 6 Register

Long Description:

Return to Summary Table

Table 3-145. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00F4h
CONTROLSS_ADC1_CFG	502C 10F4h
CONTROLSS_ADC2_CFG	502C 20F4h
CONTROLSS_ADC3_CFG	502C 30F4h
CONTROLSS_ADC4_CFG	502C 40F4h

Figure 3-72. ADCINLTRIM6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INLTRIM191TO160															
R/W															
11000000111111111101110															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INLTRIM191TO160															
R/W															
11000000111111111101110															

Access Types Legend

Table 3-146. ADCINLTRIM6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	INLTRIM191TO160	R/W	C0FFEEh	ADC Linearity Trim Bits 191-160. This register should not be modified unless specifically indicated by TI Errata or other documentation. Modifying the contents of this register could cause this module to operate outside of data sheet specifications.

3.2.74 CONTROLSS_ADCn_CFG_ADCINLTRIMCTL Registers

3.2.74.1 ADCn_CFG_ADCINLTRIMCTL Register (Offset = FCh) [reset = h]

Short Description: ADC Linearity Trim Control Register

Long Description:

Return to Summary Table

Table 3-147. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00FCh
CONTROLSS_ADC1_CFG	502C 10FCh
CONTROLSS_ADC2_CFG	502C 20FCh
CONTROLSS_ADC3_CFG	502C 30FCh
CONTROLSS_ADC4_CFG	502C 40FCh

Figure 3-73. ADCINLTRIMCTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
KEY															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										CALIBSTEP					CALIB MODE
R										R/W					R/W
0										0					0

Access Types Legend

Table 3-148. ADCINLTRIMCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	KEY	R/W	0h	ADC Linearity Trim Control Write Key. Any write to this register must contain the value 0xA5A5 in these bit locations. If a write request attempts to load any other value into these bits, the write for the entire register is ignored. These bits always read back a zero.
15 - 6	RESERVED	R		Reserved
5 - 1	CALIBSTEP	R/W	0h	ADC Linearity Calibration Step. Defines which of the 24 steps of calibration is to be executed. Never set this bit field while the ADC SELFTRIM is in progress. The R-M-W operation could unintentionally set the CALIBMODE bit again.
0	CALIBMODE	R/W	0h	ADC Linearity Calibration Mode.

3.2.75 Access Table

Table 3-149. Access Type Codes

Access Type	Code	Description
R	R	Read
R/W	R/W	Read / Write
R-0/W	R-0/W	Read returns 0s/Write

3.3 ADC_RESULT_REGS Registers

Table 3-150. CONTROLSS_ADC[0:2]_RESULT Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_ADC0_RESULT Physical Address	CONTROLSS_ADC1_RESULT Physical Address	CONTROLSS_ADC2_RESULT Physical Address
0h	16	ADC_RESULT_REGS_ADCRESULT0	5010 0000h	5010 1000h	5010 2000h
2h	16	ADC_RESULT_REGS_ADCRESULT1	5010 0002h	5010 1002h	5010 2002h
4h	16	ADC_RESULT_REGS_ADCRESULT2	5010 0004h	5010 1004h	5010 2004h
6h	16	ADC_RESULT_REGS_ADCRESULT3	5010 0006h	5010 1006h	5010 2006h
8h	16	ADC_RESULT_REGS_ADCRESULT4	5010 0008h	5010 1008h	5010 2008h
Ah	16	ADC_RESULT_REGS_ADCRESULT5	5010 000Ah	5010 100Ah	5010 200Ah
Ch	16	ADC_RESULT_REGS_ADCRESULT6	5010 000Ch	5010 100Ch	5010 200Ch
Eh	16	ADC_RESULT_REGS_ADCRESULT7	5010 000Eh	5010 100Eh	5010 200Eh
10h	16	ADC_RESULT_REGS_ADCRESULT8	5010 0010h	5010 1010h	5010 2010h
12h	16	ADC_RESULT_REGS_ADCRESULT9	5010 0012h	5010 1012h	5010 2012h
14h	16	ADC_RESULT_REGS_ADCRESULT10	5010 0014h	5010 1014h	5010 2014h
16h	16	ADC_RESULT_REGS_ADCRESULT11	5010 0016h	5010 1016h	5010 2016h
18h	16	ADC_RESULT_REGS_ADCRESULT12	5010 0018h	5010 1018h	5010 2018h
1Ah	16	ADC_RESULT_REGS_ADCRESULT13	5010 001Ah	5010 101Ah	5010 201Ah
1Ch	16	ADC_RESULT_REGS_ADCRESULT14	5010 001Ch	5010 101Ch	5010 201Ch
1Eh	16	ADC_RESULT_REGS_ADCRESULT15	5010 001Eh	5010 101Eh	5010 201Eh
20h	32	ADC_RESULT_REGS_ADCPPB1RESULT	5010 0020h	5010 1020h	5010 2020h
24h	32	ADC_RESULT_REGS_ADCPPB2RESULT	5010 0024h	5010 1024h	5010 2024h
28h	32	ADC_RESULT_REGS_ADCPPB3RESULT	5010 0028h	5010 1028h	5010 2028h
2Ch	32	ADC_RESULT_REGS_ADCPPB4RESULT	5010 002Ch	5010 102Ch	5010 202Ch

Table 3-151. CONTROLSS_ADC[3:4]_RESULT Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_ADC3_RESULT Physical Address	CONTROLSS_ADC4_RESULT Physical Address
0h	16	ADC_RESULT_REGS_ADCRESULT0	5010 3000h	5010 4000h
2h	16	ADC_RESULT_REGS_ADCRESULT1	5010 3002h	5010 4002h
4h	16	ADC_RESULT_REGS_ADCRESULT2	5010 3004h	5010 4004h
6h	16	ADC_RESULT_REGS_ADCRESULT3	5010 3006h	5010 4006h
8h	16	ADC_RESULT_REGS_ADCRESULT4	5010 3008h	5010 4008h
Ah	16	ADC_RESULT_REGS_ADCRESULT5	5010 300Ah	5010 400Ah
Ch	16	ADC_RESULT_REGS_ADCRESULT6	5010 300Ch	5010 400Ch
Eh	16	ADC_RESULT_REGS_ADCRESULT7	5010 300Eh	5010 400Eh

Table 3-151. CONTROLSS_ADC[3:4]_RESULT Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_ADC3_RESULT Physical Address	CONTROLSS_ADC4_RESULT Physical Address
10h	16	ADC_RESULT_REGS_ADCRESULT8	5010 3010h	5010 4010h
12h	16	ADC_RESULT_REGS_ADCRESULT9	5010 3012h	5010 4012h
14h	16	ADC_RESULT_REGS_ADCRESULT10	5010 3014h	5010 4014h
16h	16	ADC_RESULT_REGS_ADCRESULT11	5010 3016h	5010 4016h
18h	16	ADC_RESULT_REGS_ADCRESULT12	5010 3018h	5010 4018h
1Ah	16	ADC_RESULT_REGS_ADCRESULT13	5010 301Ah	5010 401Ah
1Ch	16	ADC_RESULT_REGS_ADCRESULT14	5010 301Ch	5010 401Ch
1Eh	16	ADC_RESULT_REGS_ADCRESULT15	5010 301Eh	5010 401Eh
20h	32	ADC_RESULT_REGS_ADCPPB1RESULT	5010 3020h	5010 4020h
24h	32	ADC_RESULT_REGS_ADCPPB2RESULT	5010 3024h	5010 4024h
28h	32	ADC_RESULT_REGS_ADCPPB3RESULT	5010 3028h	5010 4028h
2Ch	32	ADC_RESULT_REGS_ADCPPB4RESULT	5010 302Ch	5010 402Ch

3.3.1 ADC_RESULT_REGS Instance Count Note

Note

n = 0 to 4 for the ADC_RESULT_REGS registers defined below.

3.3.2 CONTROLSS_ADCn_RESULT_REGS_ADCRESULT0 Registers

3.3.2.1 ADCn_RESULT_REGS_ADCRESULT0 Register (Offset = 0h)

Short Description: ADC Result 0 Register

Long Description:

Return to Summary Table

Table 3-152. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0000h
CONTROLSS_ADC1_RESULT	5010 1000h
CONTROLSS_ADC2_RESULT	5010 2000h
CONTROLSS_ADC3_RESULT	5010 3000h
CONTROLSS_ADC4_RESULT	5010 4000h

Access Types Legend

Table 3-153. ADCRESULT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	R	0h	ADC Result 0 - 16-bit ADC result. After the ADC completes a conversion of SOC0, the digital result is placed in this bit field.

3.3.3 CONTROLSS_ADCn_RESULT_REGS_ADCRESULT1 Registers

3.3.3.1 ADCn_RESULT_REGS_ADCRESULT1 Register (Offset = 2h)

Short Description: ADC Result 1 Register

Long Description:

Return to Summary Table

Table 3-154. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0002h
CONTROLSS_ADC1_RESULT	5010 1002h
CONTROLSS_ADC2_RESULT	5010 2002h
CONTROLSS_ADC3_RESULT	5010 3002h
CONTROLSS_ADC4_RESULT	5010 4002h

Access Types Legend

Table 3-155. ADCRESULT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	R	0h	ADC Result 1 - 16-bit ADC result. After the ADC completes a conversion of SOC1, the digital result is placed in this bit field.

3.3.4 CONTROLSS_ADCn_RESULT_REGS_ADCRESULT2 Registers

3.3.4.1 ADCn_RESULT_REGS_ADCRESULT2 Register (Offset = 4h)

Short Description: ADC Result 2 Register

Long Description:

Return to Summary Table

Table 3-156. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0004h
CONTROLSS_ADC1_RESULT	5010 1004h
CONTROLSS_ADC2_RESULT	5010 2004h
CONTROLSS_ADC3_RESULT	5010 3004h
CONTROLSS_ADC4_RESULT	5010 4004h

Access Types Legend

Table 3-157. ADCRESULT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	R	0h	ADC Result 2 - 16-bit ADC result. After the ADC completes a conversion of SOC2, the digital result is placed in this bit field.

3.3.5 CONTROLSS_ADCn_RESULT_REGS_ADCRESULT3 Registers

3.3.5.1 ADCn_RESULT_REGS_ADCRESULT3 Register (Offset = 6h)

Short Description: ADC Result 3 Register

Long Description:

Return to Summary Table

Table 3-158. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0006h
CONTROLSS_ADC1_RESULT	5010 1006h
CONTROLSS_ADC2_RESULT	5010 2006h
CONTROLSS_ADC3_RESULT	5010 3006h
CONTROLSS_ADC4_RESULT	5010 4006h

Access Types Legend

Table 3-159. ADCRESULT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	R	0h	ADC Result 3 - 16-bit ADC result. After the ADC completes a conversion of SOC3, the digital result is placed in this bit field.

3.3.6 CONTROLSS_ADCn_RESULT_REGS_ADCRESULT4 Registers

3.3.6.1 ADCn_RESULT_REGS_ADCRESULT4 Register (Offset = 8h)

Short Description: ADC Result 4 Register

Long Description:

Return to Summary Table

Table 3-160. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0008h
CONTROLSS_ADC1_RESULT	5010 1008h
CONTROLSS_ADC2_RESULT	5010 2008h
CONTROLSS_ADC3_RESULT	5010 3008h
CONTROLSS_ADC4_RESULT	5010 4008h

Access Types Legend

Table 3-161. ADCRESULT4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	R	0h	ADC Result 4 - 16-bit ADC result. After the ADC completes a conversion of SOC4, the digital result is placed in this bit field.

3.3.7 CONTROLSS_ADCn_RESULT_REGS_ADCRESULT5 Registers

3.3.7.1 ADCn_RESULT_REGS_ADCRESULT5 Register (Offset = Ah)

Short Description: ADC Result 5 Register

Long Description:

Return to Summary Table

Table 3-162. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 000Ah
CONTROLSS_ADC1_RESULT	5010 100Ah
CONTROLSS_ADC2_RESULT	5010 200Ah
CONTROLSS_ADC3_RESULT	5010 300Ah
CONTROLSS_ADC4_RESULT	5010 400Ah

Access Types Legend

Table 3-163. ADCRESULT5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	R	0h	ADC Result 5 - 16-bit ADC result. After the ADC completes a conversion of SOC5, the digital result is placed in this bit field.

3.3.8 CONTROLSS_ADCn_RESULT_REGS_ADCRESULT6 Registers

3.3.8.1 ADCn_RESULT_REGS_ADCRESULT6 Register (Offset = Ch)

Short Description: ADC Result 6 Register

Long Description:

Return to Summary Table

Table 3-164. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 000Ch
CONTROLSS_ADC1_RESULT	5010 100Ch
CONTROLSS_ADC2_RESULT	5010 200Ch
CONTROLSS_ADC3_RESULT	5010 300Ch
CONTROLSS_ADC4_RESULT	5010 400Ch

Access Types Legend

Table 3-165. ADCRESULT6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	R	0h	ADC Result 6 - 16-bit ADC result. After the ADC completes a conversion of SOC6, the digital result is placed in this bit field.

3.3.9 CONTROLSS_ADCn_RESULT_REGS_ADCRESULT7 Registers

3.3.9.1 ADCn_RESULT_REGS_ADCRESULT7 Register (Offset = Eh)

Short Description: ADC Result 7 Register

Long Description:

Return to Summary Table

Table 3-166. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 000Eh
CONTROLSS_ADC1_RESULT	5010 100Eh
CONTROLSS_ADC2_RESULT	5010 200Eh
CONTROLSS_ADC3_RESULT	5010 300Eh
CONTROLSS_ADC4_RESULT	5010 400Eh

Access Types Legend

Table 3-167. ADCRESULT7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	R	0h	ADC Result 7 - 16-bit ADC result. After the ADC completes a conversion of SOC7, the digital result is placed in this bit field.

3.3.10 CONTROLSS_ADCn_RESULT_REGS_ADCRESULT8 Registers

3.3.10.1 ADCn_RESULT_REGS_ADCRESULT8 Register (Offset = 10h)

Short Description: ADC Result 8 Register

Long Description:

Return to Summary Table

Table 3-168. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0010h
CONTROLSS_ADC1_RESULT	5010 1010h
CONTROLSS_ADC2_RESULT	5010 2010h
CONTROLSS_ADC3_RESULT	5010 3010h
CONTROLSS_ADC4_RESULT	5010 4010h

Access Types Legend

Table 3-169. ADCRESULT8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	R	0h	ADC Result 8 - 16-bit ADC result. After the ADC completes a conversion of SOC8, the digital result is placed in this bit field.

3.3.11 CONTROLSS_ADCn_RESULT_REGS_ADCRESULT9 Registers

3.3.11.1 ADCn_RESULT_REGS_ADCRESULT9 Register (Offset = 12h)

Short Description: ADC Result 9 Register

Long Description:

Return to Summary Table

Table 3-170. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0012h
CONTROLSS_ADC1_RESULT	5010 1012h
CONTROLSS_ADC2_RESULT	5010 2012h
CONTROLSS_ADC3_RESULT	5010 3012h
CONTROLSS_ADC4_RESULT	5010 4012h

Access Types Legend

Table 3-171. ADCRESULT9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	R	0h	ADC Result 9 - 16-bit ADC result. After the ADC completes a conversion of SOC9, the digital result is placed in this bit field.

3.3.12 CONTROLSS_ADCn_RESULT_REGS_ADCRESULT10 Registers

3.3.12.1 ADCn_RESULT_REGS_ADCRESULT10 Register (Offset = 14h)

Short Description: ADC Result 10 Register

Long Description:

Return to Summary Table

Table 3-172. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0014h
CONTROLSS_ADC1_RESULT	5010 1014h
CONTROLSS_ADC2_RESULT	5010 2014h
CONTROLSS_ADC3_RESULT	5010 3014h
CONTROLSS_ADC4_RESULT	5010 4014h

Access Types Legend

Table 3-173. ADCRESULT10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	R	0h	ADC Result 10 - 16-bit ADC result. After the ADC completes a conversion of SOC10, the digital result is placed in this bit field.

3.3.13 CONTROLSS_ADCn_RESULT_REGS_ADCRESULT11 Registers

3.3.13.1 ADCn_RESULT_REGS_ADCRESULT11 Register (Offset = 16h)

Short Description: ADC Result 11 Register

Long Description:

Return to Summary Table

Table 3-174. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0016h
CONTROLSS_ADC1_RESULT	5010 1016h
CONTROLSS_ADC2_RESULT	5010 2016h
CONTROLSS_ADC3_RESULT	5010 3016h
CONTROLSS_ADC4_RESULT	5010 4016h

Access Types Legend

Table 3-175. ADCRESULT11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	R	0h	ADC Result 11 - 16-bit ADC result. After the ADC completes a conversion of SOC11, the digital result is placed in this bit field.

3.3.14 CONTROLSS_ADCn_RESULT_REGS_ADCRESULT12 Registers

3.3.14.1 ADCn_RESULT_REGS_ADCRESULT12 Register (Offset = 18h)

Short Description: ADC Result 12 Register

Long Description:

Return to Summary Table

Table 3-176. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0018h
CONTROLSS_ADC1_RESULT	5010 1018h
CONTROLSS_ADC2_RESULT	5010 2018h
CONTROLSS_ADC3_RESULT	5010 3018h
CONTROLSS_ADC4_RESULT	5010 4018h

Access Types Legend

Table 3-177. ADCRESULT12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	R	0h	ADC Result 12 - 16-bit ADC result. After the ADC completes a conversion of SOC12, the digital result is placed in this bit field.

3.3.15 CONTROLSS_ADCn_RESULT_REGS_ADCRESULT13 Registers

3.3.15.1 ADCn_RESULT_REGS_ADCRESULT13 Register (Offset = 1Ah)

Short Description: ADC Result 13 Register

Long Description:

Return to Summary Table

Table 3-178. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 001Ah
CONTROLSS_ADC1_RESULT	5010 101Ah
CONTROLSS_ADC2_RESULT	5010 201Ah
CONTROLSS_ADC3_RESULT	5010 301Ah
CONTROLSS_ADC4_RESULT	5010 401Ah

Access Types Legend

Table 3-179. ADCRESULT13 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	R	0h	ADC Result 13 - 16-bit ADC result. After the ADC completes a conversion of SOC13, the digital result is placed in this bit field.

3.3.16 CONTROLSS_ADCn_RESULT_REGS_ADCRESULT14 Registers

3.3.16.1 ADCn_RESULT_REGS_ADCRESULT14 Register (Offset = 1Ch)

Short Description: ADC Result 14 Register

Long Description:

Return to Summary Table

Table 3-180. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 001Ch
CONTROLSS_ADC1_RESULT	5010 101Ch
CONTROLSS_ADC2_RESULT	5010 201Ch
CONTROLSS_ADC3_RESULT	5010 301Ch
CONTROLSS_ADC4_RESULT	5010 401Ch

Access Types Legend

Table 3-181. ADCRESULT14 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	R	0h	ADC Result 14 - 16-bit ADC result. After the ADC completes a conversion of SOC14, the digital result is placed in this bit field.

3.3.17 CONTROLSS_ADCn_RESULT_REGS_ADCRESULT15 Registers

3.3.17.1 ADCn_RESULT_REGS_ADCRESULT15 Register (Offset = 1Eh)

Short Description: ADC Result 15 Register

Long Description:

Return to Summary Table

Table 3-182. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 001Eh
CONTROLSS_ADC1_RESULT	5010 101Eh
CONTROLSS_ADC2_RESULT	5010 201Eh
CONTROLSS_ADC3_RESULT	5010 301Eh
CONTROLSS_ADC4_RESULT	5010 401Eh

Access Types Legend

Table 3-183. ADCRESULT15 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	R	0h	ADC Result 15 - 16-bit ADC result. After the ADC completes a conversion of SOC15, the digital result is placed in this bit field.

3.3.18 CONTROLSS_ADCn_RESULT_REGS_ADCPPB1RESULT Registers

3.3.18.1 ADCn_RESULT_REGS_ADCPPB1RESULT Register (Offset = 20h)

Short Description: ADC Post Processing Block 1 Result Register

Long Description:

Return to Summary Table

Table 3-184. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0020h
CONTROLSS_ADC1_RESULT	5010 1020h
CONTROLSS_ADC2_RESULT	5010 2020h
CONTROLSS_ADC3_RESULT	5010 3020h
CONTROLSS_ADC4_RESULT	5010 4020h

Access Types Legend

Table 3-185. ADCPPB1RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16. - NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15 - 0	PPBRESULT	R	0h	ADC Post Processing Block Result 1 - The result of the offset/ reference subtraction post conversion processing is stored in this register. If ADCINTFLG is polled in reading PPBRESULT, user needs to add a NOP instruction to verify that post conversion processing is populated in this register. - NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

3.3.19 CONTROLSS_ADCn_RESULT_REGS_ADCPPB2RESULT Registers

3.3.19.1 ADCn_RESULT_REGS_ADCPPB2RESULT Register (Offset = 24h)

Short Description: ADC Post Processing Block 2 Result Register

Long Description:

Return to Summary Table

Table 3-186. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0024h
CONTROLSS_ADC1_RESULT	5010 1024h
CONTROLSS_ADC2_RESULT	5010 2024h
CONTROLSS_ADC3_RESULT	5010 3024h
CONTROLSS_ADC4_RESULT	5010 4024h

Access Types Legend

Table 3-187. ADCPPB2RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16. - NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15 - 0	PPBRESULT	R	0h	ADC Post Processing Block Result 2 - The result of the offset/ reference subtraction post conversion processing is stored in this register. If ADCINTFLG is polled in reading PPBRESULT, user needs to add a NOP instruction to verify that post conversion processing is populated in this register. - NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

3.3.20 CONTROLSS_ADCn_RESULT_REGS_ADCPPB3RESULT Registers

3.3.20.1 ADCn_RESULT_REGS_ADCPPB3RESULT Register (Offset = 28h)

Short Description: ADC Post Processing Block 3 Result Register

Long Description:

Return to Summary Table

Table 3-188. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0028h
CONTROLSS_ADC1_RESULT	5010 1028h
CONTROLSS_ADC2_RESULT	5010 2028h
CONTROLSS_ADC3_RESULT	5010 3028h
CONTROLSS_ADC4_RESULT	5010 4028h

Access Types Legend

Table 3-189. ADCPPB3RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16. - NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15 - 0	PPBRESULT	R	0h	ADC Post Processing Block Result 3 - The result of the offset/ reference subtraction post conversion processing is stored in this register. If ADCINTFLG is polled in reading PPBRESULT, user needs to add a NOP instruction to verify that post conversion processing is populated in this register. - NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

3.3.21 CONTROLSS_ADCn_RESULT_REGS_ADCPPB4RESULT Registers

3.3.21.1 ADCn_RESULT_REGS_ADCPPB4RESULT Register (Offset = 2Ch)

Short Description: ADC Post Processing Block 4 Result Register

Long Description:

Return to Summary Table

Table 3-190. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 002Ch
CONTROLSS_ADC1_RESULT	5010 102Ch
CONTROLSS_ADC2_RESULT	5010 202Ch
CONTROLSS_ADC3_RESULT	5010 302Ch
CONTROLSS_ADC4_RESULT	5010 402Ch

Access Types Legend

Table 3-191. ADCPPB4RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16. - NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15 - 0	PPBRESULT	R	0h	ADC Post Processing Block Result 4 - The result of the offset/ reference subtraction post conversion processing is stored in this register. If ADCINTFLG is polled in reading PPBRESULT, user needs to add a NOP instruction to verify that post conversion processing is populated in this register. - NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

3.3.22 Access Table

Table 3-192. Access Type Codes

Access Type	Code	Description
R	R	Read

3.4 CONTROLSS_CMPSSA Registers

Table 3-193. MEM, MEM Registers, Base Address=0X0000000050200000, Length=4096

Offset	Length	Register Name	CONTROLSS_CMPSSA0 Physical Address	CONTROLSS_CMPSSA1 Physical Address	CONTROLSS_CMPSSA2 Physical Address
0h	16	COMPCTL	5020 0000h	5020 1000h	5020 2000h
4h	16	COMPSTS	5020 0004h	5020 1004h	5020 2004h
6h	16	COMPSTSCLR	5020 0006h	5020 1006h	5020 2006h
8h	16	COMPDACCTL	5020 0008h	5020 1008h	5020 2008h
Ah	16	COMPDACCTL2	5020 000Ah	5020 100Ah	5020 200Ah
Ch	16	DACHVALS	5020 000Ch	5020 100Ch	5020 200Ch
Eh	16	DACHVALA	5020 000Eh	5020 100Eh	5020 200Eh
10h	16	RAMPMAXREFA	5020 0010h	5020 1010h	5020 2010h
14h	16	RAMPMAXREFS	5020 0014h	5020 1014h	5020 2014h
18h	16	RAMPDECVALA	5020 0018h	5020 1018h	5020 2018h
1Ch	16	RAMPDECVALS	5020 001Ch	5020 101Ch	5020 201Ch
20h	16	RAMPSTS	5020 0020h	5020 1020h	5020 2020h
24h	16	DACLVALS	5020 0024h	5020 1024h	5020 2024h
26h	16	DACLVALA	5020 0026h	5020 1026h	5020 2026h
28h	16	RAMPDLYA	5020 0028h	5020 1028h	5020 2028h
2Ah	16	RAMPDLYS	5020 002Ah	5020 102Ah	5020 202Ah
2Ch	16	CTRIPLFILCTL	5020 002Ch	5020 102Ch	5020 202Ch
2Eh	16	CTRIPLFILCLKCTL	5020 002Eh	5020 102Eh	5020 202Eh
30h	16	CTRIPHFILCTL	5020 0030h	5020 1030h	5020 2030h
32h	16	CTRIPHFILCLKCTL	5020 0032h	5020 1032h	5020 2032h
34h	16	COMPLOCK	5020 0034h	5020 1034h	5020 2034h
38h	16	DACHVALS2	5020 0038h	5020 1038h	5020 2038h
3Ah	16	DACLVALS2	5020 003Ah	5020 103Ah	5020 203Ah
3Ch	16	CONFIG1	5020 003Ch	5020 103Ch	5020 203Ch

Table 3-194. MEM, MEM Registers, Base Address=0X0000000050200000, Length=4096

Offset	Length	Register Name	CONTROLSS_CMPSSA3 Physical Address	CONTROLSS_CMPSSA4 Physical Address	CONTROLSS_CMPSSA5 Physical Address
0h	16	COMPCTL	5020 3000h	5020 4000h	5020 5000h
4h	16	COMPSTS	5020 3004h	5020 4004h	5020 5004h
6h	16	COMPSTSCLR	5020 3006h	5020 4006h	5020 5006h
8h	16	COMPDACCTL	5020 3008h	5020 4008h	5020 5008h
Ah	16	COMPDACCTL2	5020 300Ah	5020 400Ah	5020 500Ah
Ch	16	DACHVALS	5020 300Ch	5020 400Ch	5020 500Ch
Eh	16	DACHVALA	5020 300Eh	5020 400Eh	5020 500Eh
10h	16	RAMPMAXREFA	5020 3010h	5020 4010h	5020 5010h
14h	16	RAMPMAXREFS	5020 3014h	5020 4014h	5020 5014h
18h	16	RAMPDECVALA	5020 3018h	5020 4018h	5020 5018h
1Ch	16	RAMPDECVALS	5020 301Ch	5020 401Ch	5020 501Ch
20h	16	RAMPSTS	5020 3020h	5020 4020h	5020 5020h
24h	16	DACLVALS	5020 3024h	5020 4024h	5020 5024h
26h	16	DACLVALA	5020 3026h	5020 4026h	5020 5026h
28h	16	RAMPDLYA	5020 3028h	5020 4028h	5020 5028h
2Ah	16	RAMPDLYS	5020 302Ah	5020 402Ah	5020 502Ah

Table 3-194. MEM, MEM Registers, Base Address=0X0000000050200000, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_CMPSSA3 Physical Address	CONTROLSS_CMPSSA4 Physical Address	CONTROLSS_CMPSSA5 Physical Address
2Ch	16	CTRIPLFILCTL	5020 302Ch	5020 402Ch	5020 502Ch
2Eh	16	CTRIPLFILCLKCTL	5020 302Eh	5020 402Eh	5020 502Eh
30h	16	CTRIPHFILCTL	5020 3030h	5020 4030h	5020 5030h
32h	16	CTRIPHFILCLKCTL	5020 3032h	5020 4032h	5020 5032h
34h	16	COMPLOCK	5020 3034h	5020 4034h	5020 5034h
38h	16	DACHVALS2	5020 3038h	5020 4038h	5020 5038h
3Ah	16	DACLVALS2	5020 303Ah	5020 403Ah	5020 503Ah
3Ch	16	CONFIG1	5020 303Ch	5020 403Ch	5020 503Ch

Table 3-195. MEM, MEM Registers, Base Address=0X0000000050200000, Length=4096

Offset	Length	Register Name	CONTROLSS_CMPSSA6 Physical Address	CONTROLSS_CMPSSA7 Physical Address	CONTROLSS_CMPSSA8 Physical Address
0h	16	COMPCTL	5020 6000h	5020 7000h	5020 8000h
4h	16	COMPSTS	5020 6004h	5020 7004h	5020 8004h
6h	16	COMPSTSCLR	5020 6006h	5020 7006h	5020 8006h
8h	16	COMPDACCTL	5020 6008h	5020 7008h	5020 8008h
Ah	16	COMPDACCTL2	5020 600Ah	5020 700Ah	5020 800Ah
Ch	16	DACHVALS	5020 600Ch	5020 700Ch	5020 800Ch
Eh	16	DACHVALA	5020 600Eh	5020 700Eh	5020 800Eh
10h	16	RAMPMAXREFA	5020 6010h	5020 7010h	5020 8010h
14h	16	RAMPMAXREFS	5020 6014h	5020 7014h	5020 8014h
18h	16	RAMPDECVALA	5020 6018h	5020 7018h	5020 8018h
1Ch	16	RAMPDECVALS	5020 601Ch	5020 701Ch	5020 801Ch
20h	16	RAMPSTS	5020 6020h	5020 7020h	5020 8020h
24h	16	DACLVALS	5020 6024h	5020 7024h	5020 8024h
26h	16	DACLVALA	5020 6026h	5020 7026h	5020 8026h
28h	16	RAMPDLYA	5020 6028h	5020 7028h	5020 8028h
2Ah	16	RAMPDLYS	5020 602Ah	5020 702Ah	5020 802Ah
2Ch	16	CTRIPLFILCTL	5020 602Ch	5020 702Ch	5020 802Ch
2Eh	16	CTRIPLFILCLKCTL	5020 602Eh	5020 702Eh	5020 802Eh
30h	16	CTRIPHFILCTL	5020 6030h	5020 7030h	5020 8030h
32h	16	CTRIPHFILCLKCTL	5020 6032h	5020 7032h	5020 8032h
34h	16	COMPLOCK	5020 6034h	5020 7034h	5020 8034h
38h	16	DACHVALS2	5020 6038h	5020 7038h	5020 8038h
3Ah	16	DACLVALS2	5020 603Ah	5020 703Ah	5020 803Ah
3Ch	16	CONFIG1	5020 603Ch	5020 703Ch	5020 803Ch

Table 3-196. MEM, MEM Registers, Base Address=0X0000000050200000, Length=4096

Offset	Length	Register Name	CONTROLSS_CMPSSA9 Physical Address
0h	16	COMPCTL	5020 9000h
4h	16	COMPSTS	5020 9004h
6h	16	COMPSTSCLR	5020 9006h
8h	16	COMPDACCTL	5020 9008h
Ah	16	COMPDACCTL2	5020 900Ah
Ch	16	DACHVALS	5020 900Ch

Table 3-196. MEM, MEM Registers, Base Address=0X0000000050200000, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_CMPSSA9 Physical Address
Eh	16	DACHVALA	5020 900Eh
10h	16	RAMPMAXREFA	5020 9010h
14h	16	RAMPMAXREFS	5020 9014h
18h	16	RAMPDECVALA	5020 9018h
1Ch	16	RAMPDECVALS	5020 901Ch
20h	16	RAMPSTS	5020 9020h
24h	16	DACLVALS	5020 9024h
26h	16	DACLVALA	5020 9026h
28h	16	RAMPDLYA	5020 9028h
2Ah	16	RAMPDLYS	5020 902Ah
2Ch	16	CTRIPLFILCTL	5020 902Ch
2Eh	16	CTRIPLFILCLKCTL	5020 902Eh
30h	16	CTRIPHFILCTL	5020 9030h
32h	16	CTRIPHFILCLKCTL	5020 9032h
34h	16	COMPLOCK	5020 9034h
38h	16	DACHVALS2	5020 9038h
3Ah	16	DACLVALS2	5020 903Ah
3Ch	16	CONFIG1	5020 903Ch

3.4.1 MEM_COMPCTL Registers

3.4.1.1 MEM_COMPCTL Register (Offset = 0h) [reset = 0h]

Short Description: CMPSS Comparator Control

Long Description: CMPSS Comparator Control Register

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Table 3-197. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0000h
CONTROLSS_CMPSSA1	5020 1000h
CONTROLSS_CMPSSA2	5020 2000h
CONTROLSS_CMPSSA3	5020 3000h
CONTROLSS_CMPSSA4	5020 4000h
CONTROLSS_CMPSSA5	5020 5000h
CONTROLSS_CMPSSA6	5020 6000h
CONTROLSS_CMPSSA7	5020 7000h
CONTROLSS_CMPSSA8	5020 8000h
CONTROLSS_CMPSSA9	5020 9000h

Figure 3-74. COMPCTL Name Register

15	14	13	12	11	10	9	8
COMPDACE	ASYNCLEN	CTRIPOUTLSEL		CTRIPLSEL		COMPLINV	COMPLSOURCE
R/W	R/W	R/W		R/W		R/W	R/W
0h	0h	0h		0h		0h	0h
7	6	5	4	3	2	1	0
RESERVED_1	ASYNCHEN	CTRIPOUTHSEL		CTRIPHSEL		COMPHINV	COMPHSOURCE
R	R/W	R/W		R/W		R/W	R/W
0h	0h	0h		0h		0h	0h

Access Types Legend

Table 3-198. COMPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	COMPDACE	R/W	0h	Comparator/DAC enable. 0 Comparator/DAC disabled 1 Comparator/DAC enabled Reset Source: cmpss12a_rst_mod_g_rst_n
14	ASYNCLEN	R/W	0h	Low comparator asynchronous path enable. Allows asynchronous comparator output to feed into OR gate with latched digital filter signal when CTRIPLSEL=3 or CTRIPOUTLSEL=3. 0 Asynchronous comparator output does not feed into OR gate with latched digital filter output 1 Asynchronous comparator output feeds into OR gate with latched digital filter output Reset Source: cmpss12a_rst_mod_g_rst_n
13:12	CTRIPOUTLSEL	R/W	0h	Low comparator CTRIPOUTL source select. 0 Asynchronous comparator output drives CTRIPOUTL 1 Synchronous comparator output drives CTRIPOUTL 2 Output of digital filter drives CTRIPOUTL 3 Latched output of digital filter drives CTRIPOUTL Reset Source: cmpss12a_rst_mod_g_rst_n

Table 3-198. COMPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:10	CTRIPLSEL	R/W	0h	Low comparator CTRIPL source select. 0 Asynchronous comparator output drives CTRIPL 1 Synchronous comparator output drives CTRIPL 2 Output of digital filter drives CTRIPL 3 Latched output of digital filter drives CTRIPL Reset Source: cmpss12a_rst_mod_g_rst_n
9	COMPLINV	R/W	0h	Low comparator output invert. 0 Output of comparator is not inverted 1 Output of comparator is inverted Reset Source: cmpss12a_rst_mod_g_rst_n
8	COMPLSOURCE	R/W	0h	CompL Pos Mux Select 0 positive mux selects INL_3p3v voltage [default] 1 postive mux selects INH_3p3v Reset Source: cmpss12a_rst_mod_g_rst_n
7	RESERVED_1	R	0h	Reserved Reset Source: cmpss12a_rst_mod_g_rst_n
6	ASYNCHEN	R/W	0h	High comparator asynchronous path enable. Allows asynchronous comparator output to feed into OR gate with latched digital filter signal when CTRIPHSEL=3 or CTRIPOUTHSEL=3. 0 Asynchronous comparator output does not feed into OR gate with latched digital filter output 1 Asynchronous comparator output feeds into OR gate with latched digital filter output Reset Source: cmpss12a_rst_mod_g_rst_n
5:4	CTRIPOUTHSEL	R/W	0h	High comparator CTRIPOUTH source select. 0 Asynchronous comparator output drives CTRIPOUTH 1 Synchronous comparator output drives CTRIPOUTH 2 Output of digital filter drives CTRIPOUTH 3 Latched output of digital filter drives CTRIPOUTH Reset Source: cmpss12a_rst_mod_g_rst_n
3:2	CTRIPHSEL	R/W	0h	High comparator CTRIPH source select. 0 Asynchronous comparator output drives CTRIPH 1 Synchronous comparator output drives CTRIPH 2 Output of digital filter drives CTRIPH 3 Latched output of digital filter drives CTRIPH Reset Source: cmpss12a_rst_mod_g_rst_n
1	COMPHINV	R/W	0h	High comparator output invert. 0 Output of comparator is not inverted 1 Output of comparator is inverted Reset Source: cmpss12a_rst_mod_g_rst_n
0	COMPHSOURCE	R/W	0h	CompH neg Mux slect 0 negative mux selects DAC voltage [default] 1 negative mux selects INL_3p3v Reset Source: cmpss12a_rst_mod_g_rst_n

3.4.2 MEM_COMPSTS Registers

3.4.2.1 MEM_COMPSTS Register (Offset = 4h) [reset = 0h]

Short Description: CMPSS Comparator Status R

Long Description: CMPSS Comparator Status Register

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Table 3-199. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0004h
CONTROLSS_CMPSSA1	5020 1004h
CONTROLSS_CMPSSA2	5020 2004h
CONTROLSS_CMPSSA3	5020 3004h
CONTROLSS_CMPSSA4	5020 4004h
CONTROLSS_CMPSSA5	5020 5004h
CONTROLSS_CMPSSA6	5020 6004h
CONTROLSS_CMPSSA7	5020 7004h
CONTROLSS_CMPSSA8	5020 8004h
CONTROLSS_CMPSSA9	5020 9004h

Figure 3-75. COMPSTS Name Register

15	14	13	12	11	10	9	8
RESERVED_2						COMPLLATCH	COMPLSTS
R						R	R
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED_1						COMPHLATCH	COMPHSTS
R						R	R
0h						0h	0h

Access Types Legend

Table 3-200. COMPSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_2	R	0h	Reserved Reset Source: cmpss12a_rst_mod_g_rst_n
9	COMPLLATCH	R	0h	Latched value of low comparator digital filter output Reset Source: cmpss12a_rst_mod_g_rst_n
8	COMPLSTS	R	0h	Low comparator digital filter output Reset Source: cmpss12a_rst_mod_g_rst_n
7:2	RESERVED_1	R	0h	Reserved Reset Source: cmpss12a_rst_mod_g_rst_n
1	COMPHLATCH	R	0h	Latched value of high comparator digital filter output Reset Source: cmpss12a_rst_mod_g_rst_n
0	COMPHSTS	R	0h	High comparator digital filter output Reset Source: cmpss12a_rst_mod_g_rst_n

3.4.3 MEM_COMPSTSCLR Registers

3.4.3.1 MEM_COMPSTSCLR Register (Offset = 6h) [reset = 0h]

Short Description: CMPSS Comparator Status C

Long Description: CMPSS Comparator Status Clear Register

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Table 3-201. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0006h
CONTROLSS_CMPSSA1	5020 1006h
CONTROLSS_CMPSSA2	5020 2006h
CONTROLSS_CMPSSA3	5020 3006h
CONTROLSS_CMPSSA4	5020 4006h
CONTROLSS_CMPSSA5	5020 5006h
CONTROLSS_CMPSSA6	5020 6006h
CONTROLSS_CMPSSA7	5020 7006h
CONTROLSS_CMPSSA8	5020 8006h
CONTROLSS_CMPSSA9	5020 9006h

Figure 3-76. COMPSTSCLR Name Register

15	14	13	12	11	10	9	8
RESERVED_3					LSYNCCLREN	LLATCHCLR	RESERVED_2
R					R/W	R/W1TS	R
0h					0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED_2					HSYNCCLREN	HLATCHCLR	RESERVED_1
R					R/W	R/W1TS	R
0h					0h	0h	0h

Access Types Legend

Table 3-202. COMPSTSCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED_3	R	0h	Reserved Reset Source: cmpss12a_rst_mod_g_rst_n
10	LSYNCCLREN	R/W	0h	Low comparator latch EPWMSYNCPER clear. Enable EPWMSYNCPER reset of low comparator digital filter output latch COMPSTS[COMPLLATCH]. 0 EPWMSYNCPER will not reset latch 1 EPWMSYNCPER will reset latch Reset Source: cmpss12a_rst_mod_g_rst_n
9	LLATCHCLR	R/W1TS	0h	Low comparator latch software clear. Perform software reset of low comparator digital filter output latch COMPSTS[COMPLLATCH]. Reads always return 0. 0 No effect 1 Generate a single pulse of latch reset signal for COMPSTS[COMPLLATCH] Reset Source: cmpss12a_rst_mod_g_rst_n
8:3	RESERVED_2	R	0h	Reserved Reset Source: cmpss12a_rst_mod_g_rst_n
2	HSYNCCLREN	R/W	0h	High comparator latch EPWMSYNCPER clear. Enable EPWMSYNCPER reset of high comparator digital filter output latch COMPSTS[COMPHLATCH]. 0 EPWMSYNCPER will not reset latch 1 EPWMSYNCPER will reset latch Reset Source: cmpss12a_rst_mod_g_rst_n

Table 3-202. COMPSTSCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	HLATCHCLR	R/W1TS	0h	High comparator latch software clear. Perform software reset of high comparator digital filter output latch COMPSTS[COMPHLATCH]. Reads always return 0. 0 No effect 1 Generate a single pulse of latch reset signal for COMPSTS[COMPHLATCH] Reset Source: cmpss12a_rst_mod_g_rst_n
0	RESERVED_1	R	0h	Reserved Reset Source: cmpss12a_rst_mod_g_rst_n

3.4.4 MEM_COMPDACCTL Registers

3.4.4.1 MEM_COMPDACCTL Register (Offset = 8h) [reset = 0h]

Short Description: CMPSS DAC Control Registe

Long Description: CMPSS DAC Control Register

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Table 3-203. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0008h
CONTROLSS_CMPSSA1	5020 1008h
CONTROLSS_CMPSSA2	5020 2008h
CONTROLSS_CMPSSA3	5020 3008h
CONTROLSS_CMPSSA4	5020 4008h
CONTROLSS_CMPSSA5	5020 5008h
CONTROLSS_CMPSSA6	5020 6008h
CONTROLSS_CMPSSA7	5020 7008h
CONTROLSS_CMPSSA8	5020 8008h
CONTROLSS_CMPSSA9	5020 9008h

Figure 3-77. COMPDACCTL Name Register

15	14	13	12	11	10	9	8
FREESOFT		RESERVED_1	BLANKEN	BLANKSOURCE			
R/W		R	R/W	R/W			
0h		0h	0h	0h			
7	6	5	4	3	2	1	0
SWLOADSEL	RAMPLOADSEL	SELREF	RAMPSOURCE				DACSOURCE
R/W	R/W	R/W	R/W				R/W
0h	0h	0h	0h				0h

Access Types Legend

Table 3-204. COMPDACCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	FREESOFT	R/W	0h	Free-run or software-run emulation behavior. Behavior of the ramp generator during emulation suspend. 00b Ramp generator stops immediately during emulation suspend 01b Ramp generator completes current ramp and stops at next EPWMSYNCPER during emulation suspend 1Xb Ramp generator runs freely Reset Source: cmpss12a_rst_mod_g_rst_n
13	RESERVED_1	R	0h	Reserved Reset Source: cmpss12a_rst_mod_g_rst_n
12	BLANKEN	R/W	0h	EPWMBLANK enable. This bit enables the EPWMBLANK signal. 0 EPWMBLANK signal is disabled. 1 EPWMBLANK signal is enabled. Reset Source: cmpss12a_rst_mod_g_rst_n
11:8	BLANKSOURCE	R/W	0h	EPWMBLANK source select. This bit field determines which EPWMnBLANK is passed on as the EPWMBLANK signal. Where n represents the maximum number of EPWMBLANK signals available on the device: 0 EPWM1BLANK 1 EPWM2BLANK 2 EPWM3BLANK ... n-1 EPWMnBLANK Reset Source: cmpss12a_rst_mod_g_rst_n

Table 3-204. COMPDACCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	SWLOADSEL	R/W	0h	Software load select. Determines whether DACxVALA is updated from DACxVALS on SYSCLK or EPWMSYNCPER. 0 DACxVALA is updated from DACxVALS on SYSCLK 1 DACxVALA is updated from DACxVALS on EPWMSYNCPER Reset Source: cmpss12a_rst_mod_g_rst_n
6	RAMPLOADSEL	R/W	0h	Ramp load select. Determines whether RAMPSTS is updated from RAMPMAXREFA or RAMPMAXREFS when COMPSTS[COMPHSTS] is triggered. 0 RAMPSTS is loaded from RAMPMAXREFA 1 RAMPSTS is loaded from RAMPMAXREFS Reset Source: cmpss12a_rst_mod_g_rst_n
5	SELREF	R/W	0h	CMPSS reference select 0 vref_1p8v as reference voltage [default] 1 vdd_1p8v as reference voltage Reset Source: cmpss12a_rst_mod_g_rst_n
4:1	RAMPSOURCE	R/W	0h	EPWMSYNCPER source select. Determines which EPWMnSYNCPER signal is used within the CMPSS module. Where n represents the maximum number of EPWMSYNCPER signals available on the device: 0 EPWM1SYNCPER 1 EPWM2SYNCPER 2 EPWM3SYNCPER ... n-1 EPWMnSYNCPER Reset Source: cmpss12a_rst_mod_g_rst_n
0	DACSOURCE	R/W	0h	DAC source select. Determines whether DACHVALA is updated from DACHVALS or from the ramp generator. 0 DACHVALA is updated from DACHVALS 1 DACHVALA is updated from the ramp generator Reset Source: cmpss12a_rst_mod_g_rst_n

3.4.5 MEM_COMPDACCTL2 Registers

3.4.5.1 MEM_COMPDACCTL2 Register (Offset = Ah) [reset = 0h]

Short Description: CMPSS DAC Control Registe

Long Description: CMPSS DAC Control Register 2

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Table 3-205. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 000Ah
CONTROLSS_CMPSSA1	5020 100Ah
CONTROLSS_CMPSSA2	5020 200Ah
CONTROLSS_CMPSSA3	5020 300Ah
CONTROLSS_CMPSSA4	5020 400Ah
CONTROLSS_CMPSSA5	5020 500Ah
CONTROLSS_CMPSSA6	5020 600Ah
CONTROLSS_CMPSSA7	5020 700Ah
CONTROLSS_CMPSSA8	5020 800Ah
CONTROLSS_CMPSSA9	5020 900Ah

Figure 3-78. COMPDACCTL2 Name Register

15	14	13	12	11	10	9	8
RESERVED_3					RAMPSOURCEUSEL	RESERVED_2	BLANKSOURCEUSEL
R					R/W	R	R/W
0h					0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED_1		DEACTIVESEL					DEENABLE
R		R/W					R/W
0h		0h					0h

Access Types Legend

Table 3-206. COMPDACCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED_3	R	0h	Reserved Reset Source: cmpss12a_rst_mod_g_rst_n
10	RAMPSOURCEUSEL	R/W	0h	0: Selects EPWM0 to 15 as RAMP source 1: Selects EPWM16 to 31 as RAMP source Reset Source: cmpss12a_rst_mod_g_rst_n
9	RESERVED_2	R	0h	Reserved Reset Source: cmpss12a_rst_mod_g_rst_n
8	BLANKSOURCEUSEL	R/W	0h	0: Selects EPWM0 to 15 as blank source 1: Selects EPWM16 to 31 as blank source Reset Source: cmpss12a_rst_mod_g_rst_n
7:6	RESERVED_1	R	0h	Reserved Reset Source: cmpss12a_rst_mod_g_rst_n
5:1	DEACTIVESEL	R/W	0h	DEACTIVE source select: 0x0 : EPWM1.DEACTIVE 0x1 : EPWM2.DEACTIVE 0x2 : EPWM3.DEACTIVE 0x3 : EPWM4.DEACTIVE . . 0x31 : EPWM32.DEACTIVE Reset Source: cmpss12a_rst_mod_g_rst_n
0	DEENABLE	R/W	0h	DE mode enable. 0 DE mode features disabled. 1 DE mode features enabled. Reset Source: cmpss12a_rst_mod_g_rst_n

3.4.6 MEM_DACHVALS Registers

3.4.6.1 MEM_DACHVALS Register (Offset = Ch) [reset = 0h]

Short Description: CMPSS High DAC Value Shad

Long Description: CMPSS High DAC Value Shadow Register

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Table 3-207. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 000Ch
CONTROLSS_CMPSSA1	5020 100Ch
CONTROLSS_CMPSSA2	5020 200Ch
CONTROLSS_CMPSSA3	5020 300Ch
CONTROLSS_CMPSSA4	5020 400Ch
CONTROLSS_CMPSSA5	5020 500Ch
CONTROLSS_CMPSSA6	5020 600Ch
CONTROLSS_CMPSSA7	5020 700Ch
CONTROLSS_CMPSSA8	5020 800Ch
CONTROLSS_CMPSSA9	5020 900Ch

Figure 3-79. DACHVALS Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DACVAL			
R				R/W			
0h				0h			
7	6	5	4	3	2	1	0
DACVAL							
R/W							
0h							

Access Types Legend

Table 3-208. DACHVALS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved Reset Source: cmpss12a_rst_mod_g_rst_n
11:0	DACVAL	R/W	0h	High DAC shadow value. When COMPDACCTL[DACSOURCE]=0, the value of DACHVALS is loaded into DACHVALA on the trigger signal selected by COMPDACCTL[SWLOADSEL]. Reset Source: cmpss12a_rst_mod_g_rst_n

3.4.7 MEM_DACHVALA Registers

3.4.7.1 MEM_DACHVALA Register (Offset = Eh) [reset = 0h]

Short Description: CMPSS High DAC Value Acti

Long Description: CMPSS High DAC Value Active Register

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Table 3-209. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 000Eh
CONTROLSS_CMPSSA1	5020 100Eh
CONTROLSS_CMPSSA2	5020 200Eh
CONTROLSS_CMPSSA3	5020 300Eh
CONTROLSS_CMPSSA4	5020 400Eh
CONTROLSS_CMPSSA5	5020 500Eh
CONTROLSS_CMPSSA6	5020 600Eh
CONTROLSS_CMPSSA7	5020 700Eh
CONTROLSS_CMPSSA8	5020 800Eh
CONTROLSS_CMPSSA9	5020 900Eh

Figure 3-80. DACHVALA Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DACVAL			
R				R			
0h				0h			
7	6	5	4	3	2	1	0
DACVAL							
R							
0h							

Access Types Legend

Table 3-210. DACHVALA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved Reset Source: cmpss12a_rst_mod_g_rst_n
11:0	DACVAL	R	0h	High DAC active value. Value that is actively driven by the high DAC. Reset Source: cmpss12a_rst_mod_g_rst_n

3.4.8 MEM_RAMPMAXREFA Registers

3.4.8.1 MEM_RAMPMAXREFA Register (Offset = 10h) [reset = 0h]

Short Description: CMPSS Ramp Max Reference

Long Description: CMPSS Ramp Max Reference Active Register

Return to Summary Table

Table 3-211. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0010h
CONTROLSS_CMPSSA1	5020 1010h
CONTROLSS_CMPSSA2	5020 2010h
CONTROLSS_CMPSSA3	5020 3010h
CONTROLSS_CMPSSA4	5020 4010h
CONTROLSS_CMPSSA5	5020 5010h
CONTROLSS_CMPSSA6	5020 6010h
CONTROLSS_CMPSSA7	5020 7010h
CONTROLSS_CMPSSA8	5020 8010h
CONTROLSS_CMPSSA9	5020 9010h

Figure 3-81. RAMPMAXREFA Name Register

15	14	13	12	11	10	9	8
RAMPMAXREF							
R							
0h							
7	6	5	4	3	2	1	0
RAMPMAXREF							
R							
0h							

Access Types Legend

Table 3-212. RAMPMAXREFA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RAMPMAXREF	R	0h	Ramp maximum reference active value. Latched value to be loaded into ramp generator RAMPSTS. Reset Source: cmpss12a_rst_mod_g_rst_n

3.4.9 MEM_RAMPMAXREFS Registers

3.4.9.1 MEM_RAMPMAXREFS Register (Offset = 14h) [reset = 0h]

Short Description: CMPSS Ramp Max Reference

Long Description: CMPSS Ramp Max Reference Shadow Register

Return to Summary Table

Table 3-213. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0014h
CONTROLSS_CMPSSA1	5020 1014h
CONTROLSS_CMPSSA2	5020 2014h
CONTROLSS_CMPSSA3	5020 3014h
CONTROLSS_CMPSSA4	5020 4014h
CONTROLSS_CMPSSA5	5020 5014h
CONTROLSS_CMPSSA6	5020 6014h
CONTROLSS_CMPSSA7	5020 7014h
CONTROLSS_CMPSSA8	5020 8014h
CONTROLSS_CMPSSA9	5020 9014h

Figure 3-82. RAMPMAXREFS Name Register

15	14	13	12	11	10	9	8
RAMPMAXREF							
R/W							
0h							
7	6	5	4	3	2	1	0
RAMPMAXREF							
R/W							
0h							

Access Types Legend

Table 3-214. RAMPMAXREFS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RAMPMAXREF	R/W	0h	Ramp maximum reference shadow. Unlatched value to be loaded into ramp generator RAMPSTS. Reset Source: cmpss12a_rst_mod_g_rst_n

3.4.10 MEM_RAMPDECVALA Registers

3.4.10.1 MEM_RAMPDECVALA Register (Offset = 18h) [reset = 0h]

Short Description: CMPSS Ramp Decrement Valu

Long Description: CMPSS Ramp Decrement Value Active Register

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Table 3-215. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0018h
CONTROLSS_CMPSSA1	5020 1018h
CONTROLSS_CMPSSA2	5020 2018h
CONTROLSS_CMPSSA3	5020 3018h
CONTROLSS_CMPSSA4	5020 4018h
CONTROLSS_CMPSSA5	5020 5018h
CONTROLSS_CMPSSA6	5020 6018h
CONTROLSS_CMPSSA7	5020 7018h
CONTROLSS_CMPSSA8	5020 8018h
CONTROLSS_CMPSSA9	5020 9018h

Figure 3-83. RAMPDECVALA Name Register

15	14	13	12	11	10	9	8
RAMPDECVAL							
R							
0h							
7	6	5	4	3	2	1	0
RAMPDECVAL							
R							
0h							

Access Types Legend

Table 3-216. RAMPDECVALA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RAMPDECVAL	R	0h	Ramp decrement value active. Latched value that will be subtracted from RAMPSTS. Reset Source: cmpss12a_rst_mod_g_rst_n

3.4.11 MEM_RAMPDECVALS Registers

3.4.11.1 MEM_RAMPDECVALS Register (Offset = 1Ch) [reset = 0h]

Short Description: CMPSS Ramp Decrement Valu

Long Description: CMPSS Ramp Decrement Value Shadow Register

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Table 3-217. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 001Ch
CONTROLSS_CMPSSA1	5020 101Ch
CONTROLSS_CMPSSA2	5020 201Ch
CONTROLSS_CMPSSA3	5020 301Ch
CONTROLSS_CMPSSA4	5020 401Ch
CONTROLSS_CMPSSA5	5020 501Ch
CONTROLSS_CMPSSA6	5020 601Ch
CONTROLSS_CMPSSA7	5020 701Ch
CONTROLSS_CMPSSA8	5020 801Ch
CONTROLSS_CMPSSA9	5020 901Ch

Figure 3-84. RAMPDECVALS Name Register

15	14	13	12	11	10	9	8
RAMPDECVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
RAMPDECVAL							
R/W							
0h							

Access Types Legend

Table 3-218. RAMPDECVALS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RAMPDECVAL	R/W	0h	Ramp decrement value shadow. Unlatched value to be loaded into RAMPDECVALA. Reset Source: cmpss12a_rst_mod_g_rst_n

3.4.12 MEM_RAMPSTS Registers

3.4.12.1 MEM_RAMPSTS Register (Offset = 20h) [reset = 0h]

Short Description: CMPSS Ramp Status Registe

Long Description: CMPSS Ramp Status Register

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Table 3-219. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0020h
CONTROLSS_CMPSSA1	5020 1020h
CONTROLSS_CMPSSA2	5020 2020h
CONTROLSS_CMPSSA3	5020 3020h
CONTROLSS_CMPSSA4	5020 4020h
CONTROLSS_CMPSSA5	5020 5020h
CONTROLSS_CMPSSA6	5020 6020h
CONTROLSS_CMPSSA7	5020 7020h
CONTROLSS_CMPSSA8	5020 8020h
CONTROLSS_CMPSSA9	5020 9020h

Figure 3-85. RAMPSTS Name Register

15	14	13	12	11	10	9	8
RAMPVALUE							
R							
0h							
7	6	5	4	3	2	1	0
RAMPVALUE							
R							
0h							

Access Types Legend

Table 3-220. RAMPSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RAMPVALUE	R	0h	Ramp value. Present value of ramp generator. Reset Source: cmpss12a_rst_mod_g_rst_n

3.4.13 MEM_DACLVALS Registers

3.4.13.1 MEM_DACLVALS Register (Offset = 24h) [reset = 0h]

Short Description: CMPSS Low DAC Value Shado

Long Description: CMPSS Low DAC Value Shadow Register

Return to Summary Table

Table 3-221. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0024h
CONTROLSS_CMPSSA1	5020 1024h
CONTROLSS_CMPSSA2	5020 2024h
CONTROLSS_CMPSSA3	5020 3024h
CONTROLSS_CMPSSA4	5020 4024h
CONTROLSS_CMPSSA5	5020 5024h
CONTROLSS_CMPSSA6	5020 6024h
CONTROLSS_CMPSSA7	5020 7024h
CONTROLSS_CMPSSA8	5020 8024h
CONTROLSS_CMPSSA9	5020 9024h

Figure 3-86. DACLVALS Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DACVAL			
R				R/W			
0h				0h			
7	6	5	4	3	2	1	0
DACVAL							
R/W							
0h							

Access Types Legend

Table 3-222. DACLVALS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved Reset Source: cmpss12a_rst_mod_g_rst_n
11:0	DACVAL	R/W	0h	Low DAC shadow value. value to be loaded into DACLVALA on the trigger signal selected by COMPDACCTL[SWLOADSEL]. Reset Source: cmpss12a_rst_mod_g_rst_n

3.4.14 MEM_DACLVALA Registers

3.4.14.1 MEM_DACLVALA Register (Offset = 26h) [reset = 0h]

Short Description: CMPSS Low DAC Value Activ

Long Description: CMPSS Low DAC Value Active Register

Return to Summary Table

Table 3-223. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0026h
CONTROLSS_CMPSSA1	5020 1026h
CONTROLSS_CMPSSA2	5020 2026h
CONTROLSS_CMPSSA3	5020 3026h
CONTROLSS_CMPSSA4	5020 4026h
CONTROLSS_CMPSSA5	5020 5026h
CONTROLSS_CMPSSA6	5020 6026h
CONTROLSS_CMPSSA7	5020 7026h
CONTROLSS_CMPSSA8	5020 8026h
CONTROLSS_CMPSSA9	5020 9026h

Figure 3-87. DACLVALA Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DACVAL			
R				R			
0h				0h			
7	6	5	4	3	2	1	0
DACVAL							
R							
0h							

Access Types Legend

Table 3-224. DACLVALA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved Reset Source: cmpss12a_rst_mod_g_rst_n
11:0	DACVAL	R	0h	Low DAC active value. Value that is actively driven by the low DAC. Reset Source: cmpss12a_rst_mod_g_rst_n

3.4.15 MEM_RAMPDLYA Registers

3.4.15.1 MEM_RAMPDLYA Register (Offset = 28h) [reset = 0h]

Short Description: CMPSS Ramp Delay Active R

Long Description: CMPSS Ramp Delay Active Register

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Table 3-225. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0028h
CONTROLSS_CMPSSA1	5020 1028h
CONTROLSS_CMPSSA2	5020 2028h
CONTROLSS_CMPSSA3	5020 3028h
CONTROLSS_CMPSSA4	5020 4028h
CONTROLSS_CMPSSA5	5020 5028h
CONTROLSS_CMPSSA6	5020 6028h
CONTROLSS_CMPSSA7	5020 7028h
CONTROLSS_CMPSSA8	5020 8028h
CONTROLSS_CMPSSA9	5020 9028h

Figure 3-88. RAMPDLYA Name Register

15	14	13	12	11	10	9	8
RESERVED_1			DELAY				
R			R				
0h			0h				
7	6	5	4	3	2	1	0
DELAY							
R							
0h							

Access Types Legend

Table 3-226. RAMPDLYA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_1	R	0h	Reserved Reset Source: cmpss12a_rst_mod_g_rst_n
12:0	DELAY	R	0h	Ramp delay active value. Latched value of the number of cycles to delay the start of the ramp generator decrementer after a EPWMSYNCPER is received. Reset Source: cmpss12a_rst_mod_g_rst_n

3.4.16 MEM_RAMPDLYS Registers

3.4.16.1 MEM_RAMPDLYS Register (Offset = 2Ah) [reset = 0h]

Short Description: CMPSS Ramp Delay Shadow R

Long Description: CMPSS Ramp Delay Shadow Register

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Table 3-227. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 002Ah
CONTROLSS_CMPSSA1	5020 102Ah
CONTROLSS_CMPSSA2	5020 202Ah
CONTROLSS_CMPSSA3	5020 302Ah
CONTROLSS_CMPSSA4	5020 402Ah
CONTROLSS_CMPSSA5	5020 502Ah
CONTROLSS_CMPSSA6	5020 602Ah
CONTROLSS_CMPSSA7	5020 702Ah
CONTROLSS_CMPSSA8	5020 802Ah
CONTROLSS_CMPSSA9	5020 902Ah

Figure 3-89. RAMPDLYS Name Register

15	14	13	12	11	10	9	8
RESERVED_1			DELAY				
R			R/W				
0h			0h				
7	6	5	4	3	2	1	0
DELAY							
R/W							
0h							

Access Types Legend

Table 3-228. RAMPDLYS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_1	R	0h	Reserved Reset Source: cmpss12a_rst_mod_g_rst_n
12:0	DELAY	R/W	0h	Ramp delay shadow value. Unlatched value to be loaded into RAMPDLYA. Reset Source: cmpss12a_rst_mod_g_rst_n

3.4.17 MEM_CTRIPLFILCTL Registers

3.4.17.1 MEM_CTRIPLFILCTL Register (Offset = 2Ch) [reset = 0h]

Short Description: CTRIPL Filter Control Reg

Long Description: CTRIPL Filter Control Register

Return to Summary Table

Table 3-229. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 002Ch
CONTROLSS_CMPSSA1	5020 102Ch
CONTROLSS_CMPSSA2	5020 202Ch
CONTROLSS_CMPSSA3	5020 302Ch
CONTROLSS_CMPSSA4	5020 402Ch
CONTROLSS_CMPSSA5	5020 502Ch
CONTROLSS_CMPSSA6	5020 602Ch
CONTROLSS_CMPSSA7	5020 702Ch
CONTROLSS_CMPSSA8	5020 802Ch
CONTROLSS_CMPSSA9	5020 902Ch

Figure 3-90. CTRIPLFILCTL Name Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED_2	THRESH					SAMPWIN
R/W1TS	R	R/W					R/W
0h	0h	0h					0h
7	6	5	4	3	2	1	0
SAMPWIN				RESERVED_1			
R/W				R			
0h				0h			

Access Types Legend

Table 3-230. CTRIPLFILCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R/W1TS	0h	Low filter initialization. 0 No effect 1 Initialize all samples to the filter input value Reset Source: cmpss12a_rst_mod_g_rst_n
14	RESERVED_2	R	0h	Reserved Reset Source: cmpss12a_rst_mod_g_rst_n
13:9	THRESH	R/W	0h	Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Threshold used is THRESH+1. Reset Source: cmpss12a_rst_mod_g_rst_n
8:4	SAMPWIN	R/W	0h	Low filter sample window size. Number of samples to monitor is SAMPWIN+1. Reset Source: cmpss12a_rst_mod_g_rst_n
3:0	RESERVED_1	R	0h	Reserved Reset Source: cmpss12a_rst_mod_g_rst_n

3.4.18 MEM_CTRIPLFILCLKCTL Registers

3.4.18.1 MEM_CTRIPLFILCLKCTL Register (Offset = 2Eh) [reset = 0h]

Short Description: CTRIPL Filter Clock Contr

Long Description: CTRIPL Filter Clock Control Register

Return to Summary Table

Table 3-231. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 002Eh
CONTROLSS_CMPSSA1	5020 102Eh
CONTROLSS_CMPSSA2	5020 202Eh
CONTROLSS_CMPSSA3	5020 302Eh
CONTROLSS_CMPSSA4	5020 402Eh
CONTROLSS_CMPSSA5	5020 502Eh
CONTROLSS_CMPSSA6	5020 602Eh
CONTROLSS_CMPSSA7	5020 702Eh
CONTROLSS_CMPSSA8	5020 802Eh
CONTROLSS_CMPSSA9	5020 902Eh

Figure 3-91. CTRIPLFILCLKCTL Name Register

15	14	13	12	11	10	9	8
CLKPRESCALE							
R/W							
0h							
7	6	5	4	3	2	1	0
CLKPRESCALE							
R/W							
0h							

Access Types Legend

Table 3-232. CTRIPLFILCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CLKPRESCALE	R/W	0h	Low filter sample clock prescale. Number of system clocks between samples is CLKPRESCALE+1. Reset Source: cmpss12a_rst_mod_g_rst_n

3.4.19 MEM_CTRIPHFILCTL Registers

3.4.19.1 MEM_CTRIPHFILCTL Register (Offset = 30h) [reset = 0h]

Short Description: CTRIPH Filter Control Reg

Long Description: CTRIPH Filter Control Register

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Table 3-233. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0030h
CONTROLSS_CMPSSA1	5020 1030h
CONTROLSS_CMPSSA2	5020 2030h
CONTROLSS_CMPSSA3	5020 3030h
CONTROLSS_CMPSSA4	5020 4030h
CONTROLSS_CMPSSA5	5020 5030h
CONTROLSS_CMPSSA6	5020 6030h
CONTROLSS_CMPSSA7	5020 7030h
CONTROLSS_CMPSSA8	5020 8030h
CONTROLSS_CMPSSA9	5020 9030h

Figure 3-92. CTRIPHFILCTL Name Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED_2	THRESH					SAMPWIN
R/W1TS	R	R/W					R/W
0h	0h	0h					0h
7	6	5	4	3	2	1	0
SAMPWIN				RESERVED_1			
R/W				R			
0h				0h			

Access Types Legend

Table 3-234. CTRIPHFILCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R/W1TS	0h	High filter initialization. 0 No effect 1 Initialize all samples to the filter input value Reset Source: cmpss12a_rst_mod_g_rst_n
14	RESERVED_2	R	0h	Reserved Reset Source: cmpss12a_rst_mod_g_rst_n
13:9	THRESH	R/W	0h	High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Threshold used is THRESH+1. Reset Source: cmpss12a_rst_mod_g_rst_n
8:4	SAMPWIN	R/W	0h	High filter sample window size. Number of samples to monitor is SAMPWIN+1. Reset Source: cmpss12a_rst_mod_g_rst_n
3:0	RESERVED_1	R	0h	Reserved Reset Source: cmpss12a_rst_mod_g_rst_n

3.4.20 MEM_CTRIPHFILCLKCTL Registers

3.4.20.1 MEM_CTRIPHFILCLKCTL Register (Offset = 32h) [reset = 0h]

Short Description: CTRIPH Filter Clock Contr

Long Description: CTRIPH Filter Clock Control Register

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Table 3-235. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0032h
CONTROLSS_CMPSSA1	5020 1032h
CONTROLSS_CMPSSA2	5020 2032h
CONTROLSS_CMPSSA3	5020 3032h
CONTROLSS_CMPSSA4	5020 4032h
CONTROLSS_CMPSSA5	5020 5032h
CONTROLSS_CMPSSA6	5020 6032h
CONTROLSS_CMPSSA7	5020 7032h
CONTROLSS_CMPSSA8	5020 8032h
CONTROLSS_CMPSSA9	5020 9032h

Figure 3-93. CTRIPHFILCLKCTL Name Register

15	14	13	12	11	10	9	8
CLKPRESCALE							
R/W							
0h							
7	6	5	4	3	2	1	0
CLKPRESCALE							
R/W							
0h							

Access Types Legend

Table 3-236. CTRIPHFILCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CLKPRESCALE	R/W	0h	High filter sample clock prescale. Number of system clocks between samples is CLKPRESCALE+1. Reset Source: cmpss12a_rst_mod_g_rst_n

3.4.21 MEM_COMPLOCK Registers

3.4.21.1 MEM_COMPLOCK Register (Offset = 34h) [reset = 0h]

Short Description: CMPSS Lock Register

Long Description: CMPSS Lock Register

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Table 3-237. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0034h
CONTROLSS_CMPSSA1	5020 1034h
CONTROLSS_CMPSSA2	5020 2034h
CONTROLSS_CMPSSA3	5020 3034h
CONTROLSS_CMPSSA4	5020 4034h
CONTROLSS_CMPSSA5	5020 5034h
CONTROLSS_CMPSSA6	5020 6034h
CONTROLSS_CMPSSA7	5020 7034h
CONTROLSS_CMPSSA8	5020 8034h
CONTROLSS_CMPSSA9	5020 9034h

Figure 3-94. COMPLOCK Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1			TEST	CTRIP	DACCTL	COMPHYSCTL	COMPCTL
R			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h

Access Types Legend

Table 3-238. COMPLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15:5	RESERVED_1	R	0h	Reserved Reset Source: cmpss12a_rst_mod_g_rst_n
4	TEST	R/W1TS	0h	TEST Lock. This bit, when set, will prevent any further writes to the any undocumented registers that may affect the performance/ behavior of this block. Once set this bit can only be cleared by a reset. Reset Source: cmpss12a_rst_mod_g_rst_n
3	CTRIP	R/W1TS	0h	Lock write-access to the CTRIPxFILTCTL and CTRIPxFILCLKCTL registers. 0 CTRIPxFILCTL and CTRIPxFILCLKCTL registers are not locked. Write 0 to this bit has no effect. 1 CTRIPxFILCTL and CTRIPxFILCLKCTL registers are locked. Only a system reset can clear this bit. Reset Source: cmpss12a_rst_mod_g_rst_n
2	DACCTL	R/W1TS	0h	Lock write-access to the DACCTL register. 0 DACCTL register is not locked. Write 0 to this bit has no effect. 1 DACCTL register is locked. Only a system reset can clear this bit. Reset Source: cmpss12a_rst_mod_g_rst_n
1	COMPHYSCTL	R/W1TS	0h	Lock write-access to the COMPHYSCTL register. 0 COMPHYSCTL register is not locked. Write 0 to this bit has no effect. 1 COMPHYSCTL register is locked. Only a system reset can clear this bit. Reset Source: cmpss12a_rst_mod_g_rst_n

Table 3-238. COMPLOCK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	COMPCTL	R/W1TS	0h	Lock write-access to the COMPCTL register. 0 COMPCTL register is not locked. Write 0 to this bit has no effect. 1 COMPCTL register is locked. Only a system reset can clear this bit. Reset Source: cmpss12a_rst_mod_g_rst_n

3.4.22 MEM_DACHVALS2 Registers

3.4.22.1 MEM_DACHVALS2 Register (Offset = 38h) [reset = 0h]

Short Description: CMPSS High DAC Value Shad

Long Description: CMPSS High DAC Value Shadow Register 2

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Table 3-239. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0038h
CONTROLSS_CMPSSA1	5020 1038h
CONTROLSS_CMPSSA2	5020 2038h
CONTROLSS_CMPSSA3	5020 3038h
CONTROLSS_CMPSSA4	5020 4038h
CONTROLSS_CMPSSA5	5020 5038h
CONTROLSS_CMPSSA6	5020 6038h
CONTROLSS_CMPSSA7	5020 7038h
CONTROLSS_CMPSSA8	5020 8038h
CONTROLSS_CMPSSA9	5020 9038h

Figure 3-95. DACHVALS2 Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DACVAL			
R				R/W			
0h				0h			
7	6	5	4	3	2	1	0
DACVAL							
R/W							
0h							

Access Types Legend

Table 3-240. DACHVALS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved Reset Source: cmpss12a_rst_mod_g_rst_n
11:0	DACVAL	R/W	0h	High DAC shadow register2 value. When COMPDACCTL[DACSOURCE]=0, the value of DACHVALS2 is loaded into DACHVALA when DE mode is enabled and selected DEACTIVE input is asserted. Reset Source: cmpss12a_rst_mod_g_rst_n

3.4.23 MEM_DACLVALS2 Registers

3.4.23.1 MEM_DACLVALS2 Register (Offset = 3Ah) [reset = 0h]

Short Description: CMPSS Low DAC Value Shado

Long Description: CMPSS Low DAC Value Shadow Register 2

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Table 3-241. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 003Ah
CONTROLSS_CMPSSA1	5020 103Ah
CONTROLSS_CMPSSA2	5020 203Ah
CONTROLSS_CMPSSA3	5020 303Ah
CONTROLSS_CMPSSA4	5020 403Ah
CONTROLSS_CMPSSA5	5020 503Ah
CONTROLSS_CMPSSA6	5020 603Ah
CONTROLSS_CMPSSA7	5020 703Ah
CONTROLSS_CMPSSA8	5020 803Ah
CONTROLSS_CMPSSA9	5020 903Ah

Figure 3-96. DACLVALS2 Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DACVAL			
R				R/W			
0h				0h			
7	6	5	4	3	2	1	0
DACVAL							
R/W							
0h							

Access Types Legend

Table 3-242. DACLVALS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved Reset Source: cmpss12a_rst_mod_g_rst_n
11:0	DACVAL	R/W	0h	Low DAC shadow register2 value. Value of DACHVALS2 is loaded into DACHVALA when DE mode is enabled and selected DEACTIVE input is asserted. Reset Source: cmpss12a_rst_mod_g_rst_n

3.4.24 MEM_CONFIG1 Registers

3.4.24.1 MEM_CONFIG1 Register (Offset = 3Ch) [reset = 0h]

Short Description: CMPSS Config1 Register

Long Description: CMPSS Config1 Register

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Table 3-243. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 003Ch
CONTROLSS_CMPSSA1	5020 103Ch
CONTROLSS_CMPSSA2	5020 203Ch
CONTROLSS_CMPSSA3	5020 303Ch
CONTROLSS_CMPSSA4	5020 403Ch
CONTROLSS_CMPSSA5	5020 503Ch
CONTROLSS_CMPSSA6	5020 603Ch
CONTROLSS_CMPSSA7	5020 703Ch
CONTROLSS_CMPSSA8	5020 803Ch
CONTROLSS_CMPSSA9	5020 903Ch

Figure 3-97. CONFIG1 Name Register

15	14	13	12	11	10	9	8
SPARE							
R/W							
0h							
7	6	5	4	3	2	1	0
COMPLHYS				COMPHHYS			
R/W				R/W			
0h				0h			

Access Types Legend

Table 3-244. CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	SPARE	R/W	0h	SPARE Reset Source: cmpss12a_rst_mod_g_rst_n
7:4	COMPLHYS	R/W	0h	compL Hysterisis hystl_1p1v[3] = reserved hystl_1p1v[2] = control which comparator output value the hysteresis is applied to hystl_1p1v[1:0] = hysteresis value 00 0 LSB 01 17.5 LSB 10 35 LSB 11 52.5 LSB Reset Source: cmpss12a_rst_mod_g_rst_n
3:0	COMPHHYS	R/W	0h	CompH Hysteresis hysth_1p1v[3] = reserved hysth_1p1v[2] 0 comparator hysteresis is applied when the comparator output is 1'b1 1 comparator hysteresis is applied when the comparator output is 1'b0 hysth_1p1v[1:0] = hysteresis value 00 0 LSB 01 17.5 LSB 10 35 LSB 11 52.5 LSB Reset Source: cmpss12a_rst_mod_g_rst_n

3.4.25 Access Table

Table 3-245. Access Type Codes

Access Type	Code	Description
R/W	R/W	Read / Write
R	R	Read
R/W1TS	R/W1TS	Read/Write 1 To Set

3.5 CONTROLSS_CMPSSB Registers

Table 3-246. MEM, MEM Registers, Base Address=0X0000000050220000, Length=4096

Offset	Length	Register Name	cmpss12b0 Physical Address	cmpss12b1 Physical Address	cmpss12b2 Physical Address
0h	16	COMPCTL	5022 0000h	5022 1000h	5022 2000h
4h	16	COMPSTS	5022 0004h	5022 1004h	5022 2004h
6h	16	COMPSTSCLR	5022 0006h	5022 1006h	5022 2006h
8h	16	COMPDACCTL	5022 0008h	5022 1008h	5022 2008h
Ah	16	COMPDACCTL2	5022 000Ah	5022 100Ah	5022 200Ah
Ch	16	DACHVALS	5022 000Ch	5022 100Ch	5022 200Ch
Eh	16	DACHVALA	5022 000Eh	5022 100Eh	5022 200Eh
10h	16	RAMPMAXREFA	5022 0010h	5022 1010h	5022 2010h
14h	16	RAMPMAXREFS	5022 0014h	5022 1014h	5022 2014h
18h	16	RAMPDECVALA	5022 0018h	5022 1018h	5022 2018h
1Ch	16	RAMPDECVALS	5022 001Ch	5022 101Ch	5022 201Ch
20h	16	RAMPSTS	5022 0020h	5022 1020h	5022 2020h
24h	16	DACLVALS	5022 0024h	5022 1024h	5022 2024h
26h	16	DACLVALA	5022 0026h	5022 1026h	5022 2026h
28h	16	RAMPDLYA	5022 0028h	5022 1028h	5022 2028h
2Ah	16	RAMPDLYS	5022 002Ah	5022 102Ah	5022 202Ah
2Ch	16	CTRIPLFILCTL	5022 002Ch	5022 102Ch	5022 202Ch
2Eh	16	CTRIPLFILCLKCTL	5022 002Eh	5022 102Eh	5022 202Eh
30h	16	CTRIPHFILCTL	5022 0030h	5022 1030h	5022 2030h
32h	16	CTRIPHFILCLKCTL	5022 0032h	5022 1032h	5022 2032h
34h	16	COMPLOCK	5022 0034h	5022 1034h	5022 2034h
38h	16	DACHVALS2	5022 0038h	5022 1038h	5022 2038h
3Ah	16	DACLVALS2	5022 003Ah	5022 103Ah	5022 203Ah
3Ch	16	CONFIG1	5022 003Ch	5022 103Ch	5022 203Ch

Table 3-247. MEM, MEM Registers, Base Address=0X0000000050220000, Length=4096

Offset	Length	Register Name	cmpss12b3 Physical Address	cmpss12b4 Physical Address	cmpss12b5 Physical Address
0h	16	COMPCTL	5022 3000h	5022 4000h	5022 5000h
4h	16	COMPSTS	5022 3004h	5022 4004h	5022 5004h
6h	16	COMPSTSCLR	5022 3006h	5022 4006h	5022 5006h
8h	16	COMPDACCTL	5022 3008h	5022 4008h	5022 5008h
Ah	16	COMPDACCTL2	5022 300Ah	5022 400Ah	5022 500Ah
Ch	16	DACHVALS	5022 300Ch	5022 400Ch	5022 500Ch
Eh	16	DACHVALA	5022 300Eh	5022 400Eh	5022 500Eh
10h	16	RAMPMAXREFA	5022 3010h	5022 4010h	5022 5010h
14h	16	RAMPMAXREFS	5022 3014h	5022 4014h	5022 5014h
18h	16	RAMPDECVALA	5022 3018h	5022 4018h	5022 5018h
1Ch	16	RAMPDECVALS	5022 301Ch	5022 401Ch	5022 501Ch
20h	16	RAMPSTS	5022 3020h	5022 4020h	5022 5020h
24h	16	DACLVALS	5022 3024h	5022 4024h	5022 5024h
26h	16	DACLVALA	5022 3026h	5022 4026h	5022 5026h
28h	16	RAMPDLYA	5022 3028h	5022 4028h	5022 5028h
2Ah	16	RAMPDLYS	5022 302Ah	5022 402Ah	5022 502Ah

Table 3-247. MEM, MEM Registers, Base Address=0X0000000050220000, Length=4096 (continued)

Offset	Length	Register Name	cmpss12b3 Physical Address	cmpss12b4 Physical Address	cmpss12b5 Physical Address
2Ch	16	CTRIPLFILCTL	5022 302Ch	5022 402Ch	5022 502Ch
2Eh	16	CTRIPLFILCLKCTL	5022 302Eh	5022 402Eh	5022 502Eh
30h	16	CTRIPHFILCTL	5022 3030h	5022 4030h	5022 5030h
32h	16	CTRIPHFILCLKCTL	5022 3032h	5022 4032h	5022 5032h
34h	16	COMPLOCK	5022 3034h	5022 4034h	5022 5034h
38h	16	DACHVALS2	5022 3038h	5022 4038h	5022 5038h
3Ah	16	DACLVALS2	5022 303Ah	5022 403Ah	5022 503Ah
3Ch	16	CONFIG1	5022 303Ch	5022 403Ch	5022 503Ch

Table 3-248. MEM, MEM Registers, Base Address=0X0000000050220000, Length=4096

Offset	Length	Register Name	cmpss12b6 Physical Address	cmpss12b7 Physical Address	cmpss12b8 Physical Address
0h	16	COMPCTL	5022 6000h	5022 7000h	5022 8000h
4h	16	COMPSTS	5022 6004h	5022 7004h	5022 8004h
6h	16	COMPSTSCLR	5022 6006h	5022 7006h	5022 8006h
8h	16	COMPDACCTL	5022 6008h	5022 7008h	5022 8008h
Ah	16	COMPDACCTL2	5022 600Ah	5022 700Ah	5022 800Ah
Ch	16	DACHVALS	5022 600Ch	5022 700Ch	5022 800Ch
Eh	16	DACHVALA	5022 600Eh	5022 700Eh	5022 800Eh
10h	16	RAMPMAXREFA	5022 6010h	5022 7010h	5022 8010h
14h	16	RAMPMAXREFS	5022 6014h	5022 7014h	5022 8014h
18h	16	RAMPDECVALA	5022 6018h	5022 7018h	5022 8018h
1Ch	16	RAMPDECVALS	5022 601Ch	5022 701Ch	5022 801Ch
20h	16	RAMPSTS	5022 6020h	5022 7020h	5022 8020h
24h	16	DACLVALS	5022 6024h	5022 7024h	5022 8024h
26h	16	DACLVALA	5022 6026h	5022 7026h	5022 8026h
28h	16	RAMPDLYA	5022 6028h	5022 7028h	5022 8028h
2Ah	16	RAMPDLYS	5022 602Ah	5022 702Ah	5022 802Ah
2Ch	16	CTRIPLFILCTL	5022 602Ch	5022 702Ch	5022 802Ch
2Eh	16	CTRIPLFILCLKCTL	5022 602Eh	5022 702Eh	5022 802Eh
30h	16	CTRIPHFILCTL	5022 6030h	5022 7030h	5022 8030h
32h	16	CTRIPHFILCLKCTL	5022 6032h	5022 7032h	5022 8032h
34h	16	COMPLOCK	5022 6034h	5022 7034h	5022 8034h
38h	16	DACHVALS2	5022 6038h	5022 7038h	5022 8038h
3Ah	16	DACLVALS2	5022 603Ah	5022 703Ah	5022 803Ah
3Ch	16	CONFIG1	5022 603Ch	5022 703Ch	5022 803Ch

Table 3-249. MEM, MEM Registers, Base Address=0X0000000050220000, Length=4096

Offset	Length	Register Name	cmpss12b9 Physical Address
0h	16	COMPCTL	5022 9000h
4h	16	COMPSTS	5022 9004h
6h	16	COMPSTSCLR	5022 9006h
8h	16	COMPDACCTL	5022 9008h
Ah	16	COMPDACCTL2	5022 900Ah
Ch	16	DACHVALS	5022 900Ch
Eh	16	DACHVALA	5022 900Eh

Table 3-249. MEM, MEM Registers, Base Address=0X0000000050220000, Length=4096 (continued)

Offset	Length	Register Name	cmpss12b9 Physical Address
10h	16	RAMPMAXREFA	5022 9010h
14h	16	RAMPMAXREFS	5022 9014h
18h	16	RAMPDECVALA	5022 9018h
1Ch	16	RAMPDECVALS	5022 901Ch
20h	16	RAMPSTS	5022 9020h
24h	16	DACLVALS	5022 9024h
26h	16	DACLVALA	5022 9026h
28h	16	RAMPDLYA	5022 9028h
2Ah	16	RAMPDLYS	5022 902Ah
2Ch	16	CTRIPLFILCTL	5022 902Ch
2Eh	16	CTRIPLFILCLKCTL	5022 902Eh
30h	16	CTRIPHFILCTL	5022 9030h
32h	16	CTRIPHFILCLKCTL	5022 9032h
34h	16	COMPLOCK	5022 9034h
38h	16	DACHVALS2	5022 9038h
3Ah	16	DACLVALS2	5022 903Ah
3Ch	16	CONFIG1	5022 903Ch

3.5.1 MEM_COMPCTL Registers

3.5.1.1 MEM_COMPCTL Register (Offset = 0h) [reset = 0h]

Short Description: CMPSS Comparator Control

Long Description: CMPSS Comparator Control Register

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Table 3-250. Instance Table

Instance Name	Physical Address
CMPSS12B0	5022 0000h
CMPSS12B1	5022 1000h
CMPSS12B2	5022 2000h
CMPSS12B3	5022 3000h
CMPSS12B4	5022 4000h
CMPSS12B5	5022 5000h
CMPSS12B6	5022 6000h
CMPSS12B7	5022 7000h
CMPSS12B8	5022 8000h
CMPSS12B9	5022 9000h

Figure 3-98. COMPCTL Name Register

15	14	13	12	11	10	9	8
COMPDACE	ASYNCLEN	CTRIPOUTLSEL		CTRIPLSEL		COMPLINV	RESERVED_3
R/W	R/W	R/W		R/W		R/W	R/W
0h	0h	0h		0h		0h	0h
7	6	5	4	3	2	1	0
RESERVED_2	ASYNCHEN	CTRIPOUTHSEL		CTRIPHSEL		COMPHINV	RESERVED_1
R	R/W	R/W		R/W		R/W	R/W
0h	0h	0h		0h		0h	0h

Access Types Legend

Table 3-251. COMPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	COMPDACE	R/W	0h	Comparator/DAC enable. 0 Comparator/DAC disabled 1 Comparator/DAC enabled Reset Source: cmpss12b_rst_mod_g_rst_n
14	ASYNCLEN	R/W	0h	Low comparator asynchronous path enable. Allows asynchronous comparator output to feed into OR gate with latched digital filter signal when CTRIPLSEL=3 or CTRIPOUTLSEL=3. 0 Asynchronous comparator output does not feed into OR gate with latched digital filter output 1 Asynchronous comparator output feeds into OR gate with latched digital filter output Reset Source: cmpss12b_rst_mod_g_rst_n
13:12	CTRIPOUTLSEL	R/W	0h	Low comparator CTRIPOUTL source select. 0 Asynchronous comparator output drives CTRIPOUTL 1 Synchronous comparator output drives CTRIPOUTL 2 Output of digital filter drives CTRIPOUTL 3 Latched output of digital filter drives CTRIPOUTL Reset Source: cmpss12b_rst_mod_g_rst_n
11:10	CTRIPLSEL	R/W	0h	Low comparator CTRIPL source select. 0 Asynchronous comparator output drives CTRIPL 1 Synchronous comparator output drives CTRIPL 2 Output of digital filter drives CTRIPL 3 Latched output of digital filter drives CTRIPL Reset Source: cmpss12b_rst_mod_g_rst_n

Table 3-251. COMPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	COMPLINV	R/W	0h	Low comparator output invert. 0 Output of comparator is not inverted 1 Output of comparator is inverted Reset Source: cmpss12b_rst_mod_g_rst_n
8	RESERVED_3	R/W	0h	Reserved for CMPSSB Reset Source: cmpss12b_rst_mod_g_rst_n
7	RESERVED_2	R	0h	Reserved Reset Source: cmpss12b_rst_mod_g_rst_n
6	ASYNCHEN	R/W	0h	High comparator asynchronous path enable. Allows asynchronous comparator output to feed into OR gate with latched digital filter signal when CTRIPHSEL=3 or CTRIPOUTHSEL=3. 0 Asynchronous comparator output does not feed into OR gate with latched digital filter output 1 Asynchronous comparator output feeds into OR gate with latched digital filter output Reset Source: cmpss12b_rst_mod_g_rst_n
5:4	CTRIPOUTHSEL	R/W	0h	High comparator CTRIPOUTH source select. 0 Asynchronous comparator output drives CTRIPOUTH 1 Synchronous comparator output drives CTRIPOUTH 2 Output of digital filter drives CTRIPOUTH 3 Latched output of digital filter drives CTRIPOUTH Reset Source: cmpss12b_rst_mod_g_rst_n
3:2	CTRIPHSEL	R/W	0h	High comparator CTRIPH source select. 0 Asynchronous comparator output drives CTRIPH 1 Synchronous comparator output drives CTRIPH 2 Output of digital filter drives CTRIPH 3 Latched output of digital filter drives CTRIPH Reset Source: cmpss12b_rst_mod_g_rst_n
1	COMPHINV	R/W	0h	High comparator output invert. 0 Output of comparator is not inverted 1 Output of comparator is inverted Reset Source: cmpss12b_rst_mod_g_rst_n
0	RESERVED_1	R/W	0h	Reserved for CMPSSB Reset Source: cmpss12b_rst_mod_g_rst_n

3.5.2 MEM_COMPSTS Registers

3.5.2.1 MEM_COMPSTS Register (Offset = 4h) [reset = 0h]

Short Description: CMPSS Comparator Status R

Long Description: CMPSS Comparator Status Register

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Table 3-252. Instance Table

Instance Name	Physical Address
CMPSS12B0	5022 0004h
CMPSS12B1	5022 1004h
CMPSS12B2	5022 2004h
CMPSS12B3	5022 3004h
CMPSS12B4	5022 4004h
CMPSS12B5	5022 5004h
CMPSS12B6	5022 6004h
CMPSS12B7	5022 7004h
CMPSS12B8	5022 8004h
CMPSS12B9	5022 9004h

Figure 3-99. COMPSTS Name Register

15	14	13	12	11	10	9	8
RESERVED_2						COMPLLATCH	COMPLSTS
R						R	R
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED_1						COMPHLATCH	COMPHSTS
R						R	R
0h						0h	0h

Access Types Legend

Table 3-253. COMPSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_2	R	0h	Reserved Reset Source: cmpss12b_rst_mod_g_rst_n
9	COMPLLATCH	R	0h	Latched value of low comparator digital filter output Reset Source: cmpss12b_rst_mod_g_rst_n
8	COMPLSTS	R	0h	Low comparator digital filter output Reset Source: cmpss12b_rst_mod_g_rst_n
7:2	RESERVED_1	R	0h	Reserved Reset Source: cmpss12b_rst_mod_g_rst_n
1	COMPHLATCH	R	0h	Latched value of high comparator digital filter output Reset Source: cmpss12b_rst_mod_g_rst_n
0	COMPHSTS	R	0h	High comparator digital filter output Reset Source: cmpss12b_rst_mod_g_rst_n

3.5.3 MEM_COMPSTSCLR Registers

3.5.3.1 MEM_COMPSTSCLR Register (Offset = 6h) [reset = 0h]

Short Description: CMPSS Comparator Status C

Long Description: CMPSS Comparator Status Clear Register

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Table 3-254. Instance Table

Instance Name	Physical Address
CMPSS12B0	5022 0006h
CMPSS12B1	5022 1006h
CMPSS12B2	5022 2006h
CMPSS12B3	5022 3006h
CMPSS12B4	5022 4006h
CMPSS12B5	5022 5006h
CMPSS12B6	5022 6006h
CMPSS12B7	5022 7006h
CMPSS12B8	5022 8006h
CMPSS12B9	5022 9006h

Figure 3-100. COMPSTSCLR Name Register

15	14	13	12	11	10	9	8
RESERVED_3					LSYNCCLREN	LLATCHCLR	RESERVED_2
R					R/W	R/W1TS	R
0h					0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED_2					HSYNCCLREN	HLATCHCLR	RESERVED_1
R					R/W	R/W1TS	R
0h					0h	0h	0h

Access Types Legend

Table 3-255. COMPSTSCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED_3	R	0h	Reserved Reset Source: cmpss12b_rst_mod_g_rst_n
10	LSYNCCLREN	R/W	0h	Low comparator latch EPWMSYNCPER clear. Enable EPWMSYNCPER reset of low comparator digital filter output latch COMPSTS[COMPLLATCH]. 0 EPWMSYNCPER will not reset latch 1 EPWMSYNCPER will reset latch Reset Source: cmpss12b_rst_mod_g_rst_n
9	LLATCHCLR	R/W1TS	0h	Low comparator latch software clear. Perform software reset of low comparator digital filter output latch COMPSTS[COMPLLATCH]. Reads always return 0. 0 No effect 1 Generate a single pulse of latch reset signal for COMPSTS[COMPLLATCH] Reset Source: cmpss12b_rst_mod_g_rst_n
8:3	RESERVED_2	R	0h	Reserved Reset Source: cmpss12b_rst_mod_g_rst_n
2	HSYNCCLREN	R/W	0h	High comparator latch EPWMSYNCPER clear. Enable EPWMSYNCPER reset of high comparator digital filter output latch COMPSTS[COMPHLATCH]. 0 EPWMSYNCPER will not reset latch 1 EPWMSYNCPER will reset latch Reset Source: cmpss12b_rst_mod_g_rst_n

Table 3-255. COMPSTSCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	HLATCHCLR	R/W1TS	0h	High comparator latch software clear. Perform software reset of high comparator digital filter output latch COMPSTS[COMPHLATCH]. Reads always return 0. 0 No effect 1 Generate a single pulse of latch reset signal for COMPSTS[COMPHLATCH] Reset Source: cmpss12b_rst_mod_g_rst_n
0	RESERVED_1	R	0h	Reserved Reset Source: cmpss12b_rst_mod_g_rst_n

3.5.4 MEM_COMPDACCTL Registers

3.5.4.1 MEM_COMPDACCTL Register (Offset = 8h) [reset = 0h]

Short Description: CMPSS DAC Control Registe

Long Description: CMPSS DAC Control Register

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Table 3-256. Instance Table

Instance Name	Physical Address
CMPSS12B0	5022 0008h
CMPSS12B1	5022 1008h
CMPSS12B2	5022 2008h
CMPSS12B3	5022 3008h
CMPSS12B4	5022 4008h
CMPSS12B5	5022 5008h
CMPSS12B6	5022 6008h
CMPSS12B7	5022 7008h
CMPSS12B8	5022 8008h
CMPSS12B9	5022 9008h

Figure 3-101. COMPDACCTL Name Register

15	14	13	12	11	10	9	8
FREESOFT		RESERVED_1	BLANKEN	BLANKSOURCE			
R/W		R	R/W	R/W			
0h		0h	0h	0h			
7	6	5	4	3	2	1	0
SWLOADSEL	RAMPLOADSEL	SELREF	RAMPSOURCE				DACSOURCE
R/W	R/W	R/W	R/W				R/W
0h	0h	0h	0h				0h

Access Types Legend

Table 3-257. COMPDACCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	FREESOFT	R/W	0h	Free-run or software-run emulation behavior. Behavior of the ramp generator during emulation suspend. 00b Ramp generator stops immediately during emulation suspend 01b Ramp generator completes current ramp and stops at next EPWMSYNCPER during emulation suspend 1Xb Ramp generator runs freely Reset Source: cmpss12b_rst_mod_g_rst_n
13	RESERVED_1	R	0h	Reserved Reset Source: cmpss12b_rst_mod_g_rst_n
12	BLANKEN	R/W	0h	EPWMBLANK enable. This bit enables the EPWMBLANK signal. 0 EPWMBLANK signal is disabled. 1 EPWMBLANK signal is enabled. Reset Source: cmpss12b_rst_mod_g_rst_n
11:8	BLANKSOURCE	R/W	0h	EPWMBLANK source select. This bit field determines which EPWMnBLANK is passed on as the EPWMBLANK signal. Where n represents the maximum number of EPWMBLANK signals available on the device: 0 EPWM1BLANK 1 EPWM2BLANK 2 EPWM3BLANK ... n-1 EPWMnBLANK Reset Source: cmpss12b_rst_mod_g_rst_n

Table 3-257. COMPDACCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	SWLOADSEL	R/W	0h	Software load select. Determines whether DACxVALA is updated from DACxVALS on SYSCLK or EPWMSYNCPER. 0 DACxVALA is updated from DACxVALS on SYSCLK 1 DACxVALA is updated from DACxVALS on EPWMSYNCPER Reset Source: cmpss12b_rst_mod_g_rst_n
6	RAMPLOADSEL	R/W	0h	Ramp load select. Determines whether RAMPSTS is updated from RAMPMAXREFA or RAMPMAXREFS when COMPSTS[COMPHSTS] is triggered. 0 RAMPSTS is loaded from RAMPMAXREFA 1 RAMPSTS is loaded from RAMPMAXREFS Reset Source: cmpss12b_rst_mod_g_rst_n
5	SELREF	R/W	0h	CMPSS reference select 0 vref_1p8v as reference voltage [default] 1 vdd_1p8v as reference voltage Reset Source: cmpss12b_rst_mod_g_rst_n
4:1	RAMPSOURCE	R/W	0h	EPWMSYNCPER source select. Determines which EPWMnSYNCPER signal is used within the CMPSS module. Where n represents the maximum number of EPWMSYNCPER signals available on the device: 0 EPWM1SYNCPER 1 EPWM2SYNCPER 2 EPWM3SYNCPER ... n-1 EPWMnSYNCPER Reset Source: cmpss12b_rst_mod_g_rst_n
0	DACSOURCE	R/W	0h	DAC source select. Determines whether DACHVALA is updated from DACHVALS or from the ramp generator. 0 DACHVALA is updated from DACHVALS 1 DACHVALA is updated from the ramp generator Reset Source: cmpss12b_rst_mod_g_rst_n

3.5.5 MEM_COMPDACCTL2 Registers

3.5.5.1 MEM_COMPDACCTL2 Register (Offset = Ah) [reset = 0h]

Short Description: CMPSS DAC Control Registe

Long Description: CMPSS DAC Control Register 2

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Table 3-258. Instance Table

Instance Name	Physical Address
CMPSS12B0	5022 000Ah
CMPSS12B1	5022 100Ah
CMPSS12B2	5022 200Ah
CMPSS12B3	5022 300Ah
CMPSS12B4	5022 400Ah
CMPSS12B5	5022 500Ah
CMPSS12B6	5022 600Ah
CMPSS12B7	5022 700Ah
CMPSS12B8	5022 800Ah
CMPSS12B9	5022 900Ah

Figure 3-102. COMPDACCTL2 Name Register

15	14	13	12	11	10	9	8
RESERVED_3					RAMPSOURCEUSEL	RESERVED_2	BLANKSOURCEUSEL
R					R/W	R	R/W
0h					0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED_1		DEACTIVESEL					DEENABLE
R		R/W					R/W
0h		0h					0h

Access Types Legend

Table 3-259. COMPDACCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED_3	R	0h	Reserved Reset Source: cmpss12b_rst_mod_g_rst_n
10	RAMPSOURCEUSEL	R/W	0h	0: Selects EPWM0 to 15 as RAMP source 1: Selects EPWM16 to 31 as RAMP source Reset Source: cmpss12b_rst_mod_g_rst_n
9	RESERVED_2	R	0h	Reserved Reset Source: cmpss12b_rst_mod_g_rst_n
8	BLANKSOURCEUSEL	R/W	0h	0: Selects EPWM0 to 15 as blank source 1: Selects EPWM16 to 31 as blank source Reset Source: cmpss12b_rst_mod_g_rst_n
7:6	RESERVED_1	R	0h	Reserved Reset Source: cmpss12b_rst_mod_g_rst_n
5:1	DEACTIVESEL	R/W	0h	DEACTIVE source select: 0x0 : EPWM1.DEACTIVE 0x1 : EPWM2.DEACTIVE 0x2 : EPWM3.DEACTIVE 0x3 : EPWM4.DEACTIVE . . 0x31 : EPWM32.DEACTIVE Reset Source: cmpss12b_rst_mod_g_rst_n
0	DEENABLE	R/W	0h	DE mode enable. 0 DE mode features disabled. 1 DE mode features enabled. Reset Source: cmpss12b_rst_mod_g_rst_n

3.5.6 MEM_DACHVALS Registers

3.5.6.1 MEM_DACHVALS Register (Offset = Ch) [reset = 0h]

Short Description: CMPSS High DAC Value Shad

Long Description: CMPSS High DAC Value Shadow Register

Return to Summary Table

Table 3-260. Instance Table

Instance Name	Physical Address
CMPSS12B0	5022 000Ch
CMPSS12B1	5022 100Ch
CMPSS12B2	5022 200Ch
CMPSS12B3	5022 300Ch
CMPSS12B4	5022 400Ch
CMPSS12B5	5022 500Ch
CMPSS12B6	5022 600Ch
CMPSS12B7	5022 700Ch
CMPSS12B8	5022 800Ch
CMPSS12B9	5022 900Ch

Figure 3-103. DACHVALS Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DACVAL			
R				R/W			
0h				0h			
7	6	5	4	3	2	1	0
DACVAL							
R/W							
0h							

Access Types Legend

Table 3-261. DACHVALS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved Reset Source: cmpss12b_rst_mod_g_rst_n
11:0	DACVAL	R/W	0h	High DAC shadow value. When COMPDACCTL[DACSOURCE]=0, the value of DACHVALS is loaded into DACHVALA on the trigger signal selected by COMPDACCTL[SWLOADSEL]. Reset Source: cmpss12b_rst_mod_g_rst_n

3.5.7 MEM_DACHVALA Registers

3.5.7.1 MEM_DACHVALA Register (Offset = Eh) [reset = 0h]

Short Description: CMPSS High DAC Value Acti

Long Description: CMPSS High DAC Value Active Register

Return to Summary Table

Table 3-262. Instance Table

Instance Name	Physical Address
CMPSS12B0	5022 000Eh
CMPSS12B1	5022 100Eh
CMPSS12B2	5022 200Eh
CMPSS12B3	5022 300Eh
CMPSS12B4	5022 400Eh
CMPSS12B5	5022 500Eh
CMPSS12B6	5022 600Eh
CMPSS12B7	5022 700Eh
CMPSS12B8	5022 800Eh
CMPSS12B9	5022 900Eh

Figure 3-104. DACHVALA Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DACVAL			
R				R			
0h				0h			
7	6	5	4	3	2	1	0
DACVAL							
R							
0h							

Access Types Legend

Table 3-263. DACHVALA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved Reset Source: cmpss12b_rst_mod_g_rst_n
11:0	DACVAL	R	0h	High DAC active value. Value that is actively driven by the high DAC. Reset Source: cmpss12b_rst_mod_g_rst_n

3.5.8 MEM_RAMPMAXREFA Registers

3.5.8.1 MEM_RAMPMAXREFA Register (Offset = 10h) [reset = 0h]

Short Description: CMPSS Ramp Max Reference

Long Description: CMPSS Ramp Max Reference Active Register

Return to Summary Table

Table 3-264. Instance Table

Instance Name	Physical Address
CMPSS12B0	5022 0010h
CMPSS12B1	5022 1010h
CMPSS12B2	5022 2010h
CMPSS12B3	5022 3010h
CMPSS12B4	5022 4010h
CMPSS12B5	5022 5010h
CMPSS12B6	5022 6010h
CMPSS12B7	5022 7010h
CMPSS12B8	5022 8010h
CMPSS12B9	5022 9010h

Figure 3-105. RAMPMAXREFA Name Register

15	14	13	12	11	10	9	8
RAMPMAXREF							
R							
0h							
7	6	5	4	3	2	1	0
RAMPMAXREF							
R							
0h							

Access Types Legend

Table 3-265. RAMPMAXREFA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RAMPMAXREF	R	0h	Ramp maximum reference active value. Latched value to be loaded into ramp generator RAMPSTS. Reset Source: cmpss12b_rst_mod_g_rst_n

3.5.9 MEM_RAMPMAXREFS Registers

3.5.9.1 MEM_RAMPMAXREFS Register (Offset = 14h) [reset = 0h]

Short Description: CMPSS Ramp Max Reference

Long Description: CMPSS Ramp Max Reference Shadow Register

Return to Summary Table

Table 3-266. Instance Table

Instance Name	Physical Address
CMPSS12B0	5022 0014h
CMPSS12B1	5022 1014h
CMPSS12B2	5022 2014h
CMPSS12B3	5022 3014h
CMPSS12B4	5022 4014h
CMPSS12B5	5022 5014h
CMPSS12B6	5022 6014h
CMPSS12B7	5022 7014h
CMPSS12B8	5022 8014h
CMPSS12B9	5022 9014h

Figure 3-106. RAMPMAXREFS Name Register

15	14	13	12	11	10	9	8
RAMPMAXREF							
R/W							
0h							
7	6	5	4	3	2	1	0
RAMPMAXREF							
R/W							
0h							

Access Types Legend

Table 3-267. RAMPMAXREFS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RAMPMAXREF	R/W	0h	Ramp maximum reference shadow. Unlatched value to be loaded into ramp generator RAMPSTS. Reset Source: cmpss12b_rst_mod_g_rst_n

3.5.10 MEM_RAMPDECVALA Registers

3.5.10.1 MEM_RAMPDECVALA Register (Offset = 18h) [reset = 0h]

Short Description: CMPSS Ramp Decrement Valu

Long Description: CMPSS Ramp Decrement Value Active Register

Return to Summary Table

Table 3-268. Instance Table

Instance Name	Physical Address
CMPSS12B0	5022 0018h
CMPSS12B1	5022 1018h
CMPSS12B2	5022 2018h
CMPSS12B3	5022 3018h
CMPSS12B4	5022 4018h
CMPSS12B5	5022 5018h
CMPSS12B6	5022 6018h
CMPSS12B7	5022 7018h
CMPSS12B8	5022 8018h
CMPSS12B9	5022 9018h

Figure 3-107. RAMPDECVALA Name Register

15	14	13	12	11	10	9	8
RAMPDECVAL							
R							
0h							
7	6	5	4	3	2	1	0
RAMPDECVAL							
R							
0h							

Access Types Legend

Table 3-269. RAMPDECVALA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RAMPDECVAL	R	0h	Ramp decrement value active. Latched value that will be subtracted from RAMPSTS. Reset Source: cmpss12b_rst_mod_g_rst_n

3.5.11 MEM_RAMPDECVALS Registers

3.5.11.1 MEM_RAMPDECVALS Register (Offset = 1Ch) [reset = 0h]

Short Description: CMPSS Ramp Decrement Valu

Long Description: CMPSS Ramp Decrement Value Shadow Register

Return to Summary Table

Table 3-270. Instance Table

Instance Name	Physical Address
CMPSS12B0	5022 001Ch
CMPSS12B1	5022 101Ch
CMPSS12B2	5022 201Ch
CMPSS12B3	5022 301Ch
CMPSS12B4	5022 401Ch
CMPSS12B5	5022 501Ch
CMPSS12B6	5022 601Ch
CMPSS12B7	5022 701Ch
CMPSS12B8	5022 801Ch
CMPSS12B9	5022 901Ch

Figure 3-108. RAMPDECVALS Name Register

15	14	13	12	11	10	9	8
RAMPDECVAL							
R/W							
0h							
7	6	5	4	3	2	1	0
RAMPDECVAL							
R/W							
0h							

Access Types Legend

Table 3-271. RAMPDECVALS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RAMPDECVAL	R/W	0h	Ramp decrement value shadow. Unlatched value to be loaded into RAMPDECVALA. Reset Source: cmpss12b_rst_mod_g_rst_n

3.5.12 MEM_RAMPSTS Registers

3.5.12.1 MEM_RAMPSTS Register (Offset = 20h) [reset = 0h]

Short Description: CMPSS Ramp Status Registe

Long Description: CMPSS Ramp Status Register

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Table 3-272. Instance Table

Instance Name	Physical Address
CMPSS12B0	5022 0020h
CMPSS12B1	5022 1020h
CMPSS12B2	5022 2020h
CMPSS12B3	5022 3020h
CMPSS12B4	5022 4020h
CMPSS12B5	5022 5020h
CMPSS12B6	5022 6020h
CMPSS12B7	5022 7020h
CMPSS12B8	5022 8020h
CMPSS12B9	5022 9020h

Figure 3-109. RAMPSTS Name Register

15	14	13	12	11	10	9	8
RAMPVALUE							
R							
0h							
7	6	5	4	3	2	1	0
RAMPVALUE							
R							
0h							

Access Types Legend

Table 3-273. RAMPSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RAMPVALUE	R	0h	Ramp value. Present value of ramp generator. Reset Source: cmpss12b_rst_mod_g_rst_n

3.5.13 MEM_DACLVALS Registers

3.5.13.1 MEM_DACLVALS Register (Offset = 24h) [reset = 0h]

Short Description: CMPSS Low DAC Value Shado

Long Description: CMPSS Low DAC Value Shadow Register

Return to Summary Table

Table 3-274. Instance Table

Instance Name	Physical Address
CMPSS12B0	5022 0024h
CMPSS12B1	5022 1024h
CMPSS12B2	5022 2024h
CMPSS12B3	5022 3024h
CMPSS12B4	5022 4024h
CMPSS12B5	5022 5024h
CMPSS12B6	5022 6024h
CMPSS12B7	5022 7024h
CMPSS12B8	5022 8024h
CMPSS12B9	5022 9024h

Figure 3-110. DACLVALS Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DACVAL			
R				R/W			
0h				0h			
7	6	5	4	3	2	1	0
DACVAL							
R/W							
0h							

Access Types Legend

Table 3-275. DACLVALS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved Reset Source: cmpss12b_rst_mod_g_rst_n
11:0	DACVAL	R/W	0h	Low DAC shadow value. value to be loaded into DACLVALA on the trigger signal selected by COMPDACCTL[SWLOADSEL]. Reset Source: cmpss12b_rst_mod_g_rst_n

3.5.14 MEM_DACLVALA Registers

3.5.14.1 MEM_DACLVALA Register (Offset = 26h) [reset = 0h]

Short Description: CMPSS Low DAC Value Activ

Long Description: CMPSS Low DAC Value Active Register

Return to Summary Table

Table 3-276. Instance Table

Instance Name	Physical Address
CMPSS12B0	5022 0026h
CMPSS12B1	5022 1026h
CMPSS12B2	5022 2026h
CMPSS12B3	5022 3026h
CMPSS12B4	5022 4026h
CMPSS12B5	5022 5026h
CMPSS12B6	5022 6026h
CMPSS12B7	5022 7026h
CMPSS12B8	5022 8026h
CMPSS12B9	5022 9026h

Figure 3-111. DACLVALA Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DACVAL			
R				R			
0h				0h			
7	6	5	4	3	2	1	0
DACVAL							
R							
0h							

Access Types Legend

Table 3-277. DACLVALA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved Reset Source: cmpss12b_rst_mod_g_rst_n
11:0	DACVAL	R	0h	Low DAC active value. Value that is actively driven by the low DAC. Reset Source: cmpss12b_rst_mod_g_rst_n

3.5.15 MEM_RAMPDLYA Registers

3.5.15.1 MEM_RAMPDLYA Register (Offset = 28h) [reset = 0h]

Short Description: CMPSS Ramp Delay Active R

Long Description: CMPSS Ramp Delay Active Register

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Table 3-278. Instance Table

Instance Name	Physical Address
CMPSS12B0	5022 0028h
CMPSS12B1	5022 1028h
CMPSS12B2	5022 2028h
CMPSS12B3	5022 3028h
CMPSS12B4	5022 4028h
CMPSS12B5	5022 5028h
CMPSS12B6	5022 6028h
CMPSS12B7	5022 7028h
CMPSS12B8	5022 8028h
CMPSS12B9	5022 9028h

Figure 3-112. RAMPDLYA Name Register

15	14	13	12	11	10	9	8
RESERVED_1			DELAY				
R			R				
0h			0h				
7	6	5	4	3	2	1	0
DELAY							
R							
0h							

Access Types Legend

Table 3-279. RAMPDLYA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_1	R	0h	Reserved Reset Source: cmpss12b_rst_mod_g_rst_n
12:0	DELAY	R	0h	Ramp delay active value. Latched value of the number of cycles to delay the start of the ramp generator decrementer after a EPWMSYNCPER is received. Reset Source: cmpss12b_rst_mod_g_rst_n

3.5.16 MEM_RAMPDLYS Registers

3.5.16.1 MEM_RAMPDLYS Register (Offset = 2Ah) [reset = 0h]

Short Description: CMPSS Ramp Delay Shadow R

Long Description: CMPSS Ramp Delay Shadow Register

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Table 3-280. Instance Table

Instance Name	Physical Address
CMPSS12B0	5022 002Ah
CMPSS12B1	5022 102Ah
CMPSS12B2	5022 202Ah
CMPSS12B3	5022 302Ah
CMPSS12B4	5022 402Ah
CMPSS12B5	5022 502Ah
CMPSS12B6	5022 602Ah
CMPSS12B7	5022 702Ah
CMPSS12B8	5022 802Ah
CMPSS12B9	5022 902Ah

Figure 3-113. RAMPDLYS Name Register

15	14	13	12	11	10	9	8
RESERVED_1			DELAY				
R			R/W				
0h			0h				
7	6	5	4	3	2	1	0
DELAY							
R/W							
0h							

Access Types Legend

Table 3-281. RAMPDLYS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_1	R	0h	Reserved Reset Source: cmpss12b_rst_mod_g_rst_n
12:0	DELAY	R/W	0h	Ramp delay shadow value. Unlatched value to be loaded into RAMPDLYA. Reset Source: cmpss12b_rst_mod_g_rst_n

3.5.17 MEM_CTRIPLFILCTL Registers

3.5.17.1 MEM_CTRIPLFILCTL Register (Offset = 2Ch) [reset = 0h]

Short Description: CTRIPL Filter Control Reg

Long Description: CTRIPL Filter Control Register

Return to Summary Table

Table 3-282. Instance Table

Instance Name	Physical Address
CMPSS12B0	5022 002Ch
CMPSS12B1	5022 102Ch
CMPSS12B2	5022 202Ch
CMPSS12B3	5022 302Ch
CMPSS12B4	5022 402Ch
CMPSS12B5	5022 502Ch
CMPSS12B6	5022 602Ch
CMPSS12B7	5022 702Ch
CMPSS12B8	5022 802Ch
CMPSS12B9	5022 902Ch

Figure 3-114. CTRIPLFILCTL Name Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED_2	THRESH					SAMPWIN
R/W1TS	R	R/W					R/W
0h	0h	0h					0h
7	6	5	4	3	2	1	0
SAMPWIN				RESERVED_1			
R/W				R			
0h				0h			

Access Types Legend

Table 3-283. CTRIPLFILCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R/W1TS	0h	Low filter initialization. 0 No effect 1 Initialize all samples to the filter input value Reset Source: cmpss12b_rst_mod_g_rst_n
14	RESERVED_2	R	0h	Reserved Reset Source: cmpss12b_rst_mod_g_rst_n
13:9	THRESH	R/W	0h	Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Threshold used is THRESH+1. Reset Source: cmpss12b_rst_mod_g_rst_n
8:4	SAMPWIN	R/W	0h	Low filter sample window size. Number of samples to monitor is SAMPWIN+1. Reset Source: cmpss12b_rst_mod_g_rst_n
3:0	RESERVED_1	R	0h	Reserved Reset Source: cmpss12b_rst_mod_g_rst_n

3.5.18 MEM_CTRIPLFILCLKCTL Registers

3.5.18.1 MEM_CTRIPLFILCLKCTL Register (Offset = 2Eh) [reset = 0h]

Short Description: CTRIPL Filter Clock Contr

Long Description: CTRIPL Filter Clock Control Register

Return to Summary Table

Table 3-284. Instance Table

Instance Name	Physical Address
CMPSS12B0	5022 002Eh
CMPSS12B1	5022 102Eh
CMPSS12B2	5022 202Eh
CMPSS12B3	5022 302Eh
CMPSS12B4	5022 402Eh
CMPSS12B5	5022 502Eh
CMPSS12B6	5022 602Eh
CMPSS12B7	5022 702Eh
CMPSS12B8	5022 802Eh
CMPSS12B9	5022 902Eh

Figure 3-115. CTRIPLFILCLKCTL Name Register

15	14	13	12	11	10	9	8
CLKPRESCALE							
R/W							
0h							
7	6	5	4	3	2	1	0
CLKPRESCALE							
R/W							
0h							

Access Types Legend

Table 3-285. CTRIPLFILCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CLKPRESCALE	R/W	0h	Low filter sample clock prescale. Number of system clocks between samples is CLKPRESCALE+1. Reset Source: cmpss12b_rst_mod_g_rst_n

3.5.19 MEM_CTRIPHFILCTL Registers

3.5.19.1 MEM_CTRIPHFILCTL Register (Offset = 30h) [reset = 0h]

Short Description: CTRIPH Filter Control Reg

Long Description: CTRIPH Filter Control Register

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Table 3-286. Instance Table

Instance Name	Physical Address
CMPSS12B0	5022 0030h
CMPSS12B1	5022 1030h
CMPSS12B2	5022 2030h
CMPSS12B3	5022 3030h
CMPSS12B4	5022 4030h
CMPSS12B5	5022 5030h
CMPSS12B6	5022 6030h
CMPSS12B7	5022 7030h
CMPSS12B8	5022 8030h
CMPSS12B9	5022 9030h

Figure 3-116. CTRIPHFILCTL Name Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED_2	THRESH					SAMPWIN
R/W1TS	R	R/W					R/W
0h	0h	0h					0h
7	6	5	4	3	2	1	0
SAMPWIN				RESERVED_1			
R/W				R			
0h				0h			

Access Types Legend

Table 3-287. CTRIPHFILCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R/W1TS	0h	High filter initialization. 0 No effect 1 Initialize all samples to the filter input value Reset Source: cmpss12b_rst_mod_g_rst_n
14	RESERVED_2	R	0h	Reserved Reset Source: cmpss12b_rst_mod_g_rst_n
13:9	THRESH	R/W	0h	High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Threshold used is THRESH+1. Reset Source: cmpss12b_rst_mod_g_rst_n
8:4	SAMPWIN	R/W	0h	High filter sample window size. Number of samples to monitor is SAMPWIN+1. Reset Source: cmpss12b_rst_mod_g_rst_n
3:0	RESERVED_1	R	0h	Reserved Reset Source: cmpss12b_rst_mod_g_rst_n

3.5.20 MEM_CTRIPHFILCLKCTL Registers

3.5.20.1 MEM_CTRIPHFILCLKCTL Register (Offset = 32h) [reset = 0h]

Short Description: CTRIPH Filter Clock Contr

Long Description: CTRIPH Filter Clock Control Register

Return to Summary Table

Table 3-288. Instance Table

Instance Name	Physical Address
CMPSS12B0	5022 0032h
CMPSS12B1	5022 1032h
CMPSS12B2	5022 2032h
CMPSS12B3	5022 3032h
CMPSS12B4	5022 4032h
CMPSS12B5	5022 5032h
CMPSS12B6	5022 6032h
CMPSS12B7	5022 7032h
CMPSS12B8	5022 8032h
CMPSS12B9	5022 9032h

Figure 3-117. CTRIPHFILCLKCTL Name Register

15	14	13	12	11	10	9	8
CLKPRESCALE							
R/W							
0h							
7	6	5	4	3	2	1	0
CLKPRESCALE							
R/W							
0h							

Access Types Legend

Table 3-289. CTRIPHFILCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CLKPRESCALE	R/W	0h	High filter sample clock prescale. Number of system clocks between samples is CLKPRESCALE+1. Reset Source: cmpss12b_rst_mod_g_rst_n

3.5.21 MEM_COMPLOCK Registers

3.5.21.1 MEM_COMPLOCK Register (Offset = 34h) [reset = 0h]

Short Description: CMPSS Lock Register

Long Description: CMPSS Lock Register

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Table 3-290. Instance Table

Instance Name	Physical Address
CMPSS12B0	5022 0034h
CMPSS12B1	5022 1034h
CMPSS12B2	5022 2034h
CMPSS12B3	5022 3034h
CMPSS12B4	5022 4034h
CMPSS12B5	5022 5034h
CMPSS12B6	5022 6034h
CMPSS12B7	5022 7034h
CMPSS12B8	5022 8034h
CMPSS12B9	5022 9034h

Figure 3-118. COMPLOCK Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1			TEST	CTRIP	DACCTL	COMPHYSCTL	COMPCTL
R			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h

Access Types Legend

Table 3-291. COMPLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15:5	RESERVED_1	R	0h	Reserved Reset Source: cmpss12b_rst_mod_g_rst_n
4	TEST	R/W1TS	0h	TEST Lock. This bit, when set, will prevent any further writes to the any undocumented registers that may affect the performance/ behavior of this block. Once set this bit can only be cleared by a reset. Reset Source: cmpss12b_rst_mod_g_rst_n
3	CTRIP	R/W1TS	0h	Lock write-access to the CTRIPxFILTCTL and CTRIPxFILCLKCTL registers. 0 CTRIPxFILCTL and CTRIPxFILCLKCTL registers are not locked. Write 0 to this bit has no effect. 1 CTRIPxFILCTL and CTRIPxFILCLKCTL registers are locked. Only a system reset can clear this bit. Reset Source: cmpss12b_rst_mod_g_rst_n
2	DACCTL	R/W1TS	0h	Lock write-access to the DACCTL register. 0 DACCTL register is not locked. Write 0 to this bit has no effect. 1 DACCTL register is locked. Only a system reset can clear this bit. Reset Source: cmpss12b_rst_mod_g_rst_n
1	COMPHYSCTL	R/W1TS	0h	Lock write-access to the COMPHYSCTL register. 0 COMPHYSCTL register is not locked. Write 0 to this bit has no effect. 1 COMPHYSCTL register is locked. Only a system reset can clear this bit. Reset Source: cmpss12b_rst_mod_g_rst_n

Table 3-291. COMPLOCK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	COMPCTL	R/W1TS	0h	Lock write-access to the COMPCTL register. 0 COMPCTL register is not locked. Write 0 to this bit has no effect. 1 COMPCTL register is locked. Only a system reset can clear this bit. Reset Source: cmpss12b_rst_mod_g_rst_n

3.5.22 MEM_DACHVALS2 Registers

3.5.22.1 MEM_DACHVALS2 Register (Offset = 38h) [reset = 0h]

Short Description: CMPSS High DAC Value Shad

Long Description: CMPSS High DAC Value Shadow Register 2

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Table 3-292. Instance Table

Instance Name	Physical Address
CMPSS12B0	5022 0038h
CMPSS12B1	5022 1038h
CMPSS12B2	5022 2038h
CMPSS12B3	5022 3038h
CMPSS12B4	5022 4038h
CMPSS12B5	5022 5038h
CMPSS12B6	5022 6038h
CMPSS12B7	5022 7038h
CMPSS12B8	5022 8038h
CMPSS12B9	5022 9038h

Figure 3-119. DACHVALS2 Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DACVAL			
R				R/W			
0h				0h			
7	6	5	4	3	2	1	0
DACVAL							
R/W							
0h							

Access Types Legend

Table 3-293. DACHVALS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved Reset Source: cmpss12b_rst_mod_g_rst_n
11:0	DACVAL	R/W	0h	High DAC shadow register2 value. When COMPDACCTL[DACSOURCE]=0, the value of DACHVALS2 is loaded into DACHVALA when DE mode is enabled and selected DEACTIVE input is asserted. Reset Source: cmpss12b_rst_mod_g_rst_n

3.5.23 MEM_DACLVALS2 Registers

3.5.23.1 MEM_DACLVALS2 Register (Offset = 3Ah) [reset = 0h]

Short Description: CMPSS Low DAC Value Shado

Long Description: CMPSS Low DAC Value Shadow Register 2

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Table 3-294. Instance Table

Instance Name	Physical Address
CMPSS12B0	5022 003Ah
CMPSS12B1	5022 103Ah
CMPSS12B2	5022 203Ah
CMPSS12B3	5022 303Ah
CMPSS12B4	5022 403Ah
CMPSS12B5	5022 503Ah
CMPSS12B6	5022 603Ah
CMPSS12B7	5022 703Ah
CMPSS12B8	5022 803Ah
CMPSS12B9	5022 903Ah

Figure 3-120. DACLVALS2 Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DACVAL			
R				R/W			
0h				0h			
7	6	5	4	3	2	1	0
DACVAL							
R/W							
0h							

Access Types Legend

Table 3-295. DACLVALS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved Reset Source: cmpss12b_rst_mod_g_rst_n
11:0	DACVAL	R/W	0h	Low DAC shadow register2 value. Value of DACHVALS2 is loaded into DACHVALA when DE mode is enabled and selected DEACTIVE input is asserted. Reset Source: cmpss12b_rst_mod_g_rst_n

3.5.24 MEM_CONFIG1 Registers

3.5.24.1 MEM_CONFIG1 Register (Offset = 3Ch) [reset = 0h]

Short Description: CMPSS Config1 Register

Long Description: CMPSS Config1 Register

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Table 3-296. Instance Table

Instance Name	Physical Address
CMPSS12B0	5022 003Ch
CMPSS12B1	5022 103Ch
CMPSS12B2	5022 203Ch
CMPSS12B3	5022 303Ch
CMPSS12B4	5022 403Ch
CMPSS12B5	5022 503Ch
CMPSS12B6	5022 603Ch
CMPSS12B7	5022 703Ch
CMPSS12B8	5022 803Ch
CMPSS12B9	5022 903Ch

Figure 3-121. CONFIG1 Name Register

15	14	13	12	11	10	9	8
SPARE							
R/W							
0h							
7	6	5	4	3	2	1	0
COMPLHYS				COMPHHYS			
R/W				R/W			
0h				0h			

Access Types Legend

Table 3-297. CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	SPARE	R/W	0h	SPARE Reset Source: cmpss12b_rst_mod_g_rst_n
7:4	COMPLHYS	R/W	0h	compL Hysterisis hystl_1p1v[3] = reserved hystl_1p1v[2] = control which comparator output value the hysteresis is applied to hystl_1p1v[1:0] = hysteresis value 00 0 LSB 01 17.5 LSB 10 35 LSB 11 52.5 LSB Reset Source: cmpss12b_rst_mod_g_rst_n
3:0	COMPHHYS	R/W	0h	CompH Hysteresis hysth_1p1v[3] = reserved hysth_1p1v[2] 0 comparator hysteresis is applied when the comparator output is 1'b1 1 comparator hysteresis is applied when the comparator output is 1'b0 hysth_1p1v[1:0] = hysteresis value 00 0 LSB 01 17.5 LSB 10 35 LSB 11 52.5 LSB Reset Source: cmpss12b_rst_mod_g_rst_n

3.5.25 Access Table

Table 3-298. Access Type Codes

Access Type	Code	Description
R/W	R/W	Read / Write
R	R	Read
R/W1TS	R/W1TS	Read/Write 1 To Set

3.6 DAC Registers

Table 3-299. MEM, MEM Registers, Base Address=0X0000000050260000, Length=4096

Offset	Length	Register Name	dac0 Physical Address
0h	16	DACREV	5026 0000h
2h	16	DACCTL_ALT2_	5026 0002h
4h	16	DACVALA	5026 0004h
6h	16	DACVALS	5026 0006h
8h	16	DACOUTEN	5026 0008h
Ah	16	DACLOCK	5026 000Ah
Ch	16	DACTRIM	5026 000Ch
Eh	16	DACCONFIG	5026 000Eh

3.6.1 MEM_DACREV Registers

3.6.1.1 MEM_DACREV Register (Offset = 0h) [reset = 0h]

Short Description: DAC Revision Register

Long Description: DAC Revision Register

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Table 3-300. Instance Table

Instance Name	Physical Address
DAC0	5026 0000h

Figure 3-122. DACREV Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
REV							
R							
0h							

Access Types Legend

Table 3-301. DACREV Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED_1	R	0h	Reserved Reset Source: dac_rst_mod_g_rst_n
7:0	REV	R	0h	DAC Revision Reset Source: dac_rst_mod_g_rst_n

3.6.2 MEM_DACCTL_ALT2_ Registers

3.6.2.1 MEM_ALT2_ Register (Offset = 2h) [reset = 0h]

Short Description: DAC Control Register

Long Description: DAC Control Register

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Table 3-302. Instance Table

Instance Name	Physical Address
DAC0	5026 0002h

Figure 3-123. DACCTL_ALT2_ Name Register

15	14	13	12	11	10	9	8
RESERVED_2							SYNCSEL
R							R/W
0h							0h
7	6	5	4	3	2	1	0
SYNCSEL				RESERVED_1	LOADMODE	MODE	DACREFSEL
R/W				R	R/W	R/W	R/W
0h				0h	0h	0h	0h

Access Types Legend

Table 3-303. DACCTL_ALT2_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	RESERVED_2	R	0h	Reserved Reset Source: dac_rst_mod_g_rst_n
8:4	SYNCSEL	R/W	0h	DAC EPWMSYNCPER select. Determines which EPWMSYNCPER signal will update the DACVALA register. Where n represents the maximum number of EPWMSYNCPER signals available on the device: 0 EPWM1SYNCPER 1 EPWM2SYNCPER 2 EPWM3SYNCPER ... n-1 EPWMnSYNCPER Reset Source: dac_rst_mod_g_rst_n
3	RESERVED_1	R	0h	Reserved Reset Source: dac_rst_mod_g_rst_n
2	LOADMODE	R/W	0h	DACVALA load mode. Determines when the DACVALA register is updated with the value from DACVALS. 0 Load on next SYSCLK 1 Load on next EPWMSYNCPER specified by SYNCSEL Reset Source: dac_rst_mod_g_rst_n
1	MODE	R/W	0h	DAC gain mode select. Selects the gain mode for the buffered output. The MODE value is only used when DACREFSEL=1 and internal ADC reference mode is selected. 0 Gain is 1 1 Gain is 2 Reset Source: dac_rst_mod_g_rst_n
0	DACREFSEL	R/W	0h	DAC reference select. Selects which voltage references are used by the DAC. 0 VDAC/VSSA are the reference voltages 1 ADC VREFHI/VSSA are the reference voltages Reset Source: dac_rst_mod_g_rst_n

3.6.3 MEM_DACVALA Registers

3.6.3.1 MEM_DACVALA Register (Offset = 4h) [reset = 0h]

Short Description: DAC Value Register - Acti

Long Description: DAC Value Register - Active

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Table 3-304. Instance Table

Instance Name	Physical Address
DAC0	5026 0004h

Figure 3-124. DACVALA Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DACVALA			
R				R			
0h				0h			
7	6	5	4	3	2	1	0
DACVALA							
R							
0h							

Access Types Legend

Table 3-305. DACVALA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved Reset Source: dac_rst_mod_g_rst_n
11:0	DACVALA	R	0h	Active output code currently driven by the DAC Reset Source: dac_rst_mod_g_rst_n

3.6.4 MEM_DACVALS Registers

3.6.4.1 MEM_DACVALS Register (Offset = 6h) [reset = 0h]

Short Description: DAC Value Register - Shad

Long Description: DAC Value Register - Shadow

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Table 3-306. Instance Table

Instance Name	Physical Address
DAC0	5026 0006h

Figure 3-125. DACVALS Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DACVALS			
R				R/W			
0h				0h			
7	6	5	4	3	2	1	0
DACVALS							
R/W							
0h							

Access Types Legend

Table 3-307. DACVALS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved Reset Source: dac_rst_mod_g_rst_n
11:0	DACVALS	R/W	0h	Shadow output code to be loaded into DACVALA Reset Source: dac_rst_mod_g_rst_n

3.6.5 MEM_DACOUTEN Registers

3.6.5.1 MEM_DACOUTEN Register (Offset = 8h) [reset = 0h]

Short Description: DAC Output Enable Registe

Long Description: DAC Output Enable Register

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Table 3-308. Instance Table

Instance Name	Physical Address
DAC0	5026 0008h

Figure 3-126. DACOUTEN Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1							DACOUTEN
R							R/W
0h							0h

Access Types Legend

Table 3-309. DACOUTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	RESERVED_1	R	0h	Reserved Reset Source: dac_rst_mod_g_rst_n
0	DACOUTEN	R/W	0h	DAC output enable 0 DAC output is disabled 1 DAC output is enabled Reset Source: dac_rst_mod_g_rst_n

3.6.6 MEM_DACLOCK Registers

3.6.6.1 MEM_DACLOCK Register (Offset = Ah) [reset = 0h]

Short Description: DAC Lock Register

Long Description: DAC Lock Register

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Table 3-310. Instance Table

Instance Name	Physical Address
DAC0	5026 000Ah

Figure 3-127. DACLOCK Name Register

15	14	13	12	11	10	9	8
KEY				RESERVED_1			
R/W				R			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED_1					DACOUTEN	DACVAL	DACCTL
R					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

Access Types Legend

Table 3-311. DACLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	KEY	R/W	0h	Writes to this register succeed only if this field is written with a value of 0xA. Only 16-bit writes will succeed [provided the KEY matches]. Read-modify-writes to individual bits in this register will be ignored. Reset Source: dac_rst_mod_g_rst_n
11:3	RESERVED_1	R	0h	Reserved Reset Source: dac_rst_mod_g_rst_n
2	DACOUTEN	R/W1TS	0h	Lock write-access to the DACOUTEN register. 0 DACOUTEN register is not locked. Write 0 to this bit has no effect. 1 DACOUTEN register is locked. Only a system reset can clear this bit. Reset Source: dac_rst_mod_g_rst_n
1	DACVAL	R/W1TS	0h	Lock write-access to the DACVALS register. 0 DACVALS register is not locked. Write 0 to this bit has no effect. 1 DACVALS register is locked. Only a system reset can clear this bit. Reset Source: dac_rst_mod_g_rst_n
0	DACCTL	R/W1TS	0h	Lock write-access to the DACCTL register. 0 DACCTL register is not locked. Write 0 to this bit has no effect. 1 DACCTL register is locked. Only a system reset can clear this bit. Reset Source: dac_rst_mod_g_rst_n

3.6.7 MEM_DACTRIM Registers

3.6.7.1 MEM_DACTRIM Register (Offset = Ch) [reset = 0h]

Short Description: DAC Trim Register

Long Description: DAC Trim Register

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Table 3-312. Instance Table

Instance Name	Physical Address
DAC0	5026 000Ch

Figure 3-128. DACTRIM Name Register

15	14	13	12	11	10	9	8
RESERVED_1				GAIN_TRIM			
R				R/W			
0h				0h			
7	6	5	4	3	2	1	0
OFFSET_TRIM							
R/W							
0h							

Access Types Legend

Table 3-313. DACTRIM Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved Reset Source: dac_rst_mod_g_rst_n
11:8	GAIN_TRIM	R/W	0h	DAC Gain Trim. This signed [two's complement] bit field is used to adjust the gain of the DAC. This register will be written with a factory set value during the device boot procedure. 1000 Gain is increased by the equivalent of 0.8% ... 1110 Gain is increased by the equivalent of 0.2% LSB 1111 Gain is increased by the equivalent of 0.1% LSB 0000 Gain is not adjusted 0001 Gain is decreased by the equivalent of 0.1% LSB 0010 Gain is decreased by the equivalent of 0.2% LSB ... 0111 Gain is decreased by the equivalent of 0.7% LSB Reset Source: dac_rst_mod_g_rst_n
7:0	OFFSET_TRIM	R/W	0h	DAC Offset Trim. This register should not be modified unless specifically indicated by TI Errata or other documentation. Modifying the contents of this register could cause this module to operate outside of datasheet specifications. Reset Source: dac_rst_mod_g_rst_n

3.6.8 MEM_DACCONFIG Registers

3.6.8.1 MEM_DACCONFIG Register (Offset = Eh) [reset = 0h]

Short Description: DAC Configuration Registe

Long Description: DAC Configuration Register

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Table 3-314. Instance Table

Instance Name	Physical Address
DAC0	5026 000Eh

Figure 3-129. DACCONFIG Name Register

15	14	13	12	11	10	9	8
CONFIG							
R/W							
0h							
7	6	5	4	3	2	1	0
CONFIG							
R/W							
0h							

Access Types Legend

Table 3-315. DACCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CONFIG	R/W	0h	DAC Configuration. This bit field is used for TI internal testing/ debugging. Reset Source: dac_rst_mod_g_rst_n

3.6.9 Access Table

Table 3-316. Access Type Codes

Access Type	Code	Description
R	R	Read
R/W	R/W	Read / Write
R/W1TS	R/W1TS	Read/Write 1 To Set

3.7 DMAXBAR Registers

Table 3-317. CFG0, CFG0 Registers, Base Address=0X00000000502D6000, Length=2048

Offset	Length	Register Name	dmaxbar_mmr Physical Address
0h	32	PID	502D 6000h
100h	32	DMAXBar0_GSEL	502D 6100h
104h	32	DMAXBar0_G0	502D 6104h
108h	32	DMAXBar0_G1	502D 6108h
10Ch	32	DMAXBar0_G2	502D 610Ch
110h	32	DMAXBar0_G3	502D 6110h
114h	32	DMAXBar0_G4	502D 6114h
118h	32	DMAXBar0_G5	502D 6118h
140h	32	DMAXBar1_GSEL	502D 6140h
144h	32	DMAXBar1_G0	502D 6144h
148h	32	DMAXBar1_G1	502D 6148h
14Ch	32	DMAXBar1_G2	502D 614Ch
150h	32	DMAXBar1_G3	502D 6150h
154h	32	DMAXBar1_G4	502D 6154h
158h	32	DMAXBar1_G5	502D 6158h
180h	32	DMAXBar2_GSEL	502D 6180h
184h	32	DMAXBar2_G0	502D 6184h
188h	32	DMAXBar2_G1	502D 6188h
18Ch	32	DMAXBar2_G2	502D 618Ch
190h	32	DMAXBar2_G3	502D 6190h
194h	32	DMAXBar2_G4	502D 6194h
198h	32	DMAXBar2_G5	502D 6198h
1C0h	32	DMAXBar3_GSEL	502D 61C0h
1C4h	32	DMAXBar3_G0	502D 61C4h
1C8h	32	DMAXBar3_G1	502D 61C8h
1CCh	32	DMAXBar3_G2	502D 61CCh
1D0h	32	DMAXBar3_G3	502D 61D0h
1D4h	32	DMAXBar3_G4	502D 61D4h
1D8h	32	DMAXBar3_G5	502D 61D8h
200h	32	DMAXBar4_GSEL	502D 6200h
204h	32	DMAXBar4_G0	502D 6204h
208h	32	DMAXBar4_G1	502D 6208h
20Ch	32	DMAXBar4_G2	502D 620Ch
210h	32	DMAXBar4_G3	502D 6210h
214h	32	DMAXBar4_G4	502D 6214h
218h	32	DMAXBar4_G5	502D 6218h
240h	32	DMAXBar5_GSEL	502D 6240h
244h	32	DMAXBar5_G0	502D 6244h
248h	32	DMAXBar5_G1	502D 6248h
24Ch	32	DMAXBar5_G2	502D 624Ch
250h	32	DMAXBar5_G3	502D 6250h
254h	32	DMAXBar5_G4	502D 6254h
258h	32	DMAXBar5_G5	502D 6258h
280h	32	DMAXBar6_GSEL	502D 6280h
284h	32	DMAXBar6_G0	502D 6284h

Table 3-317. CFG0, CFG0 Registers, Base Address=0X00000000502D6000, Length=2048 (continued)

Offset	Length	Register Name	dmaxbar_mmr Physical Address
288h	32	DMAXBar6_G1	502D 6288h
28Ch	32	DMAXBar6_G2	502D 628Ch
290h	32	DMAXBar6_G3	502D 6290h
294h	32	DMAXBar6_G4	502D 6294h
298h	32	DMAXBar6_G5	502D 6298h
2C0h	32	DMAXBar7_GSEL	502D 62C0h
2C4h	32	DMAXBar7_G0	502D 62C4h
2C8h	32	DMAXBar7_G1	502D 62C8h
2CCh	32	DMAXBar7_G2	502D 62CCh
2D0h	32	DMAXBar7_G3	502D 62D0h
2D4h	32	DMAXBar7_G4	502D 62D4h
2D8h	32	DMAXBar7_G5	502D 62D8h
300h	32	DMAXBar8_GSEL	502D 6300h
304h	32	DMAXBar8_G0	502D 6304h
308h	32	DMAXBar8_G1	502D 6308h
30Ch	32	DMAXBar8_G2	502D 630Ch
310h	32	DMAXBar8_G3	502D 6310h
314h	32	DMAXBar8_G4	502D 6314h
318h	32	DMAXBar8_G5	502D 6318h
340h	32	DMAXBar9_GSEL	502D 6340h
344h	32	DMAXBar9_G0	502D 6344h
348h	32	DMAXBar9_G1	502D 6348h
34Ch	32	DMAXBar9_G2	502D 634Ch
350h	32	DMAXBar9_G3	502D 6350h
354h	32	DMAXBar9_G4	502D 6354h
358h	32	DMAXBar9_G5	502D 6358h
380h	32	DMAXBar10_GSEL	502D 6380h
384h	32	DMAXBar10_G0	502D 6384h
388h	32	DMAXBar10_G1	502D 6388h
38Ch	32	DMAXBar10_G2	502D 638Ch
390h	32	DMAXBar10_G3	502D 6390h
394h	32	DMAXBar10_G4	502D 6394h
398h	32	DMAXBar10_G5	502D 6398h
3C0h	32	DMAXBar11_GSEL	502D 63C0h
3C4h	32	DMAXBar11_G0	502D 63C4h
3C8h	32	DMAXBar11_G1	502D 63C8h
3CCh	32	DMAXBar11_G2	502D 63CCh
3D0h	32	DMAXBar11_G3	502D 63D0h
3D4h	32	DMAXBar11_G4	502D 63D4h
3D8h	32	DMAXBar11_G5	502D 63D8h
400h	32	DMAXBar12_GSEL	502D 6400h
404h	32	DMAXBar12_G0	502D 6404h
408h	32	DMAXBar12_G1	502D 6408h
40Ch	32	DMAXBar12_G2	502D 640Ch
410h	32	DMAXBar12_G3	502D 6410h
414h	32	DMAXBar12_G4	502D 6414h
418h	32	DMAXBar12_G5	502D 6418h

Table 3-317. CFG0, CFG0 Registers, Base Address=0X00000000502D6000, Length=2048 (continued)

Offset	Length	Register Name	dmaxbar_mmr Physical Address
440h	32	DMAXBar13_GSEL	502D 6440h
444h	32	DMAXBar13_G0	502D 6444h
448h	32	DMAXBar13_G1	502D 6448h
44Ch	32	DMAXBar13_G2	502D 644Ch
450h	32	DMAXBar13_G3	502D 6450h
454h	32	DMAXBar13_G4	502D 6454h
458h	32	DMAXBar13_G5	502D 6458h
480h	32	DMAXBar14_GSEL	502D 6480h
484h	32	DMAXBar14_G0	502D 6484h
488h	32	DMAXBar14_G1	502D 6488h
48Ch	32	DMAXBar14_G2	502D 648Ch
490h	32	DMAXBar14_G3	502D 6490h
494h	32	DMAXBar14_G4	502D 6494h
498h	32	DMAXBar14_G5	502D 6498h
4C0h	32	DMAXBar15_GSEL	502D 64C0h
4C4h	32	DMAXBar15_G0	502D 64C4h
4C8h	32	DMAXBar15_G1	502D 64C8h
4CCh	32	DMAXBar15_G2	502D 64CCh
4D0h	32	DMAXBar15_G3	502D 64D0h
4D4h	32	DMAXBar15_G4	502D 64D4h
4D8h	32	DMAXBar15_G5	502D 64D8h

3.7.1 CFG0_PID Registers

3.7.1.1 CFG0_PID Register (Offset = 0h) [reset = 61800215h]

Short Description: PID register

Long Description: PID register

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Table 3-318. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6000h

Figure 3-130. PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PID_MSB16															
R															
6180h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_MISC					PID_MAJOR			PID_CUSTOM		PID_MINOR					
R					R			R		R					
0h					2h			0h		15h					

Access Types Legend

Table 3-319. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR	R	15h	Reset Source: mod_g_rst_n

3.7.2 CFG0_DMAXBAR0_GSEL Registers

3.7.2.1 CFG0_GSEL Register (Offset = 100h) [reset = 0h]

Short Description:

Long Description:

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Table 3-320. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6100h

Figure 3-131. DMAXBAR0_GSEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													DMAXBAR0_GSEL_GSEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-321. DMAXBAR0_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	DMAXBAR0_GSEL_GSEL	R/W	0h	Select input source: 0: G0 selected .. 5: G5 selected Reset Source: mod_g_rst_n

3.7.3 CFG0_DMAXBAR0_G0 Registers

3.7.3.1 CFG0_G0 Register (Offset = 104h) [reset = 0h]

Short Description:

Long Description:

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Table 3-322. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6104h

Figure 3-132. DMAXBAR0_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR0_G0_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-323. DMAXBAR0_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR0_G0_SEL	R/W	0h	ETPWM SOCA to corresponding xbar 1: PWMx.SOCA is selected 0: PWMx.SOCA is de-selected Reset Source: mod_g_rst_n

3.7.4 CFG0_DMAXBAR0_G1 Registers

3.7.4.1 CFG0_G1 Register (Offset = 108h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-324. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6108h

Figure 3-133. DMAXBAR0_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR0_G1_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-325. DMAXBAR0_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR0_G1_SEL	R/W	0h	ETPWM SOCB to corresponding xbar 1: PWMx.SOCB is selected 0: PWMx.SOCB is de-selected Reset Source: mod_g_rst_n

3.7.5 CFG0_DMAXBAR0_G2 Registers

3.7.5.1 CFG0_G2 Register (Offset = 10Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-326. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 610Ch

Figure 3-134. DMAXBAR0_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR0_G2_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-327. DMAXBAR0_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR0_G2_SEL	R/W	0h	ADC DMA requests to corresponding xbar 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.7.6 CFG0_DMAXBAR0_G3 Registers

3.7.6.1 CFG0_G3 Register (Offset = 110h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-328. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6110h

Figure 3-135. DMAXBAR0_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DMAXBAR0_G3_SEL			
NONE												R/W			
0												0h			

Access Types Legend

Table 3-329. DMAXBAR0_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:0	DMAXBAR0_G3_SEL	R/W	0h	FSI DMA requests to corresponding xbar 0: FSIRX0.RX_DMA_EVT 1 FSIRX0_DMATRIG1 2: FSIRX0_DMATRIG2 3: FSIRX1.RX_DMA_EVT 4 FSIRX1_DMATRIG1 5: FSIRX1_DMATRIG2 6: FSIRX2.RX_DMA_EVT 7 FSIRX2_DMATRIG1 8: FSIRX2_DMATRIG2 9: FSIRX3.RX_DMA_EVT 10 FSIRX3_DMATRIG1 11: FSIRX3_DMATRIG2 12: FSITX0.TX_DMA_EVT 13: FSITX1.TX_DMA_EVT 14: FSITX2.TX_DMA_EVT 15: FSITX3.TX_DMA_EVT Reset Source: mod_g_rst_n

3.7.7 CFG0_DMAXBAR0_G4 Registers

3.7.7.1 CFG0_G4 Register (Offset = 114h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-330. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6114h

Figure 3-136. DMAXBAR0_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													DMAXBAR0_G4_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-331. DMAXBAR0_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	DMAXBAR0_G4_SEL	R/W	0h	SDFM DMA requests to corresponding xbar 0: SD0.FILT1.DRINT 1: SD0.FILT2.DRINT 2: SD0.FILT3.DRINT 3: SD0.FILT4.DRINT 4: SD1.FILT1.DRINT 5: SD1.FILT2.DRINT 6: SD1.FILT3.DRINT 7: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.7.8 CFG0_DMAXBAR0_G5 Registers

3.7.8.1 CFG0_G5 Register (Offset = 118h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-332. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6118h

Figure 3-137. DMAXBAR0_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DMAXBAR0_G5_SEL			
NONE												R/W			
0												0h			

Access Types Legend

Table 3-333. DMAXBAR0_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:0	DMAXBAR0_G5_SEL	R/W	0h	ECAP DMA requests to corresponding xbar 0: ECAP0.DMA_INT 1: ECAP1.DMA_INT 2: ECAP2.DMA_INT 3: ECAP3.DMA_INT 4: ECAP4.DMA_INT 5: ECAP5.DMA_INT 6: ECAP6.DMA_INT 7: ECAP7.DMA_INT 8: ECAP8.DMA_INT 9: ECAP9.DMA_INT Reset Source: mod_g_rst_n

3.7.9 CFG0_DMAXBAR1_GSEL Registers

3.7.9.1 CFG0_GSEL Register (Offset = 140h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-334. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6140h

Figure 3-138. DMAXBAR1_GSEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													DMAXBAR1_GSEL_GSEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-335. DMAXBAR1_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	DMAXBAR1_GSEL_GSEL	R/W	0h	Select input source: 0: G0 selected .. 5: G5 selected Reset Source: mod_g_rst_n

3.7.10 CFG0_DMAXBAR1_G0 Registers

3.7.10.1 CFG0_G0 Register (Offset = 144h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-336. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6144h

Figure 3-139. DMAXBAR1_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR1_G0_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-337. DMAXBAR1_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR1_G0_SEL	R/W	0h	ETPWM SOCA to corresponding xbar 1: PWMx.SOCA is selected 0: PWMx.SOCA is de-selected Reset Source: mod_g_rst_n

3.7.11 CFG0_DMAXBAR1_G1 Registers

3.7.11.1 CFG0_G1 Register (Offset = 148h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-338. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6148h

Figure 3-140. DMAXBAR1_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR1_G1_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-339. DMAXBAR1_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR1_G1_SEL	R/W	0h	ETPWM SOCB to corresponding xbar 1: PWMx.SOCB is selected 0: PWMx.SOCB is de-selected Reset Source: mod_g_rst_n

3.7.12 CFG0_DMAXBAR1_G2 Registers

3.7.12.1 CFG0_G2 Register (Offset = 14Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-340. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 614Ch

Figure 3-141. DMAXBAR1_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR1_G2_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-341. DMAXBAR1_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR1_G2_SEL	R/W	0h	ADC DMA requests to corresponding xbar 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.7.13 CFG0_DMAXBAR1_G3 Registers

3.7.13.1 CFG0_G3 Register (Offset = 150h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-342. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6150h

Figure 3-142. DMAXBAR1_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DMAXBAR1_G3_SEL			
NONE												R/W			
0												0h			

Access Types Legend

Table 3-343. DMAXBAR1_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:0	DMAXBAR1_G3_SEL	R/W	0h	FSI DMA requests to corresponding xbar 0: FSIRX0.RX_DMA_EVT 1 FSIRX0_DMATRIG1 2: FSIRX0_DMATRIG2 3: FSIRX1.RX_DMA_EVT 4 FSIRX1_DMATRIG1 5: FSIRX1_DMATRIG2 6: FSIRX2.RX_DMA_EVT 7 FSIRX2_DMATRIG1 8: FSIRX2_DMATRIG2 9: FSIRX3.RX_DMA_EVT 10 FSIRX3_DMATRIG1 11: FSIRX3_DMATRIG2 12: FSITX0.TX_DMA_EVT 13: FSITX1.TX_DMA_EVT 14: FSITX2.TX_DMA_EVT 15: FSITX3.TX_DMA_EVT Reset Source: mod_g_rst_n

3.7.14 CFG0_DMAXBAR1_G4 Registers

3.7.14.1 CFG0_G4 Register (Offset = 154h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-344. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6154h

Figure 3-143. DMAXBAR1_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													DMAXBAR1_G4_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-345. DMAXBAR1_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	DMAXBAR1_G4_SEL	R/W	0h	SDFM DMA requests to corresponding xbar 0: SD0.FILT1.DRINT 1: SD0.FILT2.DRINT 2: SD0.FILT3.DRINT 3: SD0.FILT4.DRINT 4: SD1.FILT1.DRINT 5: SD1.FILT2.DRINT 6: SD1.FILT3.DRINT 7: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.7.15 CFG0_DMAXBAR1_G5 Registers

3.7.15.1 CFG0_G5 Register (Offset = 158h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-346. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6158h

Figure 3-144. DMAXBAR1_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DMAXBAR1_G5_SEL			
NONE												R/W			
0												0h			

Access Types Legend

Table 3-347. DMAXBAR1_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:0	DMAXBAR1_G5_SEL	R/W	0h	ECAP DMA requests to corresponding xbar 0: ECAP0.DMA_INT 1: ECAP1.DMA_INT 2: ECAP2.DMA_INT 3: ECAP3.DMA_INT 4: ECAP4.DMA_INT 5: ECAP5.DMA_INT 6: ECAP6.DMA_INT 7: ECAP7.DMA_INT 8: ECAP8.DMA_INT 9: ECAP9.DMA_INT Reset Source: mod_g_rst_n

3.7.16 CFG0_DMAXBAR2_GSEL Registers

3.7.16.1 CFG0_GSEL Register (Offset = 180h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-348. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6180h

Figure 3-145. DMAXBAR2_GSEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													DMAXBAR2_GSEL_GSEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-349. DMAXBAR2_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	DMAXBAR2_GSEL_GSEL	R/W	0h	Select input source: 0: G0 selected .. 5: G5 selected Reset Source: mod_g_rst_n

3.7.17 CFG0_DMAXBAR2_G0 Registers

3.7.17.1 CFG0_G0 Register (Offset = 184h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-350. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6184h

Figure 3-146. DMAXBAR2_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR2_G0_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-351. DMAXBAR2_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR2_G0_SEL	R/W	0h	ETPWM SOCA to corresponding xbar 1: PWMx.SOCA is selected 0: PWMx.SOCA is de-selected Reset Source: mod_g_rst_n

3.7.18 CFG0_DMAXBAR2_G1 Registers

3.7.18.1 CFG0_G1 Register (Offset = 188h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-352. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6188h

Figure 3-147. DMAXBAR2_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR2_G1_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-353. DMAXBAR2_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR2_G1_SEL	R/W	0h	ETPWM SOCB to corresponding xbar 1: PWMx.SOCB is selected 0: PWMx.SOCB is de-selected Reset Source: mod_g_rst_n

3.7.19 CFG0_DMAXBAR2_G2 Registers

3.7.19.1 CFG0_G2 Register (Offset = 18Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-354. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 618Ch

Figure 3-148. DMAXBAR2_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR2_G2_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-355. DMAXBAR2_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR2_G2_SEL	R/W	0h	ADC DMA requests to corresponding xbar 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.7.20 CFG0_DMAXBAR2_G3 Registers

3.7.20.1 CFG0_G3 Register (Offset = 190h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-356. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6190h

Figure 3-149. DMAXBAR2_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DMAXBAR2_G3_SEL			
NONE												R/W			
0												0h			

Access Types Legend

Table 3-357. DMAXBAR2_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:0	DMAXBAR2_G3_SEL	R/W	0h	FSI DMA requests to corresponding xbar 0: FSIRX0.RX_DMA_EVT 1 FSIRX0_DMATRIG1 2: FSIRX0_DMATRIG2 3: FSIRX1.RX_DMA_EVT 4 FSIRX1_DMATRIG1 5: FSIRX1_DMATRIG2 6: FSIRX2.RX_DMA_EVT 7 FSIRX2_DMATRIG1 8: FSIRX2_DMATRIG2 9: FSIRX3.RX_DMA_EVT 10 FSIRX3_DMATRIG1 11: FSIRX3_DMATRIG2 12: FSITX0.TX_DMA_EVT 13: FSITX1.TX_DMA_EVT 14: FSITX2.TX_DMA_EVT 15: FSITX3.TX_DMA_EVT Reset Source: mod_g_rst_n

3.7.21 CFG0_DMAXBAR2_G4 Registers

3.7.21.1 CFG0_G4 Register (Offset = 194h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-358. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6194h

Figure 3-150. DMAXBAR2_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													DMAXBAR2_G4_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-359. DMAXBAR2_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	DMAXBAR2_G4_SEL	R/W	0h	SDFM DMA requests to corresponding xbar 0: SD0.FILT1.DRINT 1: SD0.FILT2.DRINT 2: SD0.FILT3.DRINT 3: SD0.FILT4.DRINT 4: SD1.FILT1.DRINT 5: SD1.FILT2.DRINT 6: SD1.FILT3.DRINT 7: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.7.22 CFG0_DMAXBAR2_G5 Registers

3.7.22.1 CFG0_G5 Register (Offset = 198h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-360. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6198h

Figure 3-151. DMAXBAR2_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DMAXBAR2_G5_SEL			
NONE												R/W			
0												0h			

Access Types Legend

Table 3-361. DMAXBAR2_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:0	DMAXBAR2_G5_SEL	R/W	0h	ECAP DMA requests to corresponding xbar 0: ECAP0.DMA_INT 1: ECAP1.DMA_INT 2: ECAP2.DMA_INT 3: ECAP3.DMA_INT 4: ECAP4.DMA_INT 5: ECAP5.DMA_INT 6: ECAP6.DMA_INT 7: ECAP7.DMA_INT 8: ECAP8.DMA_INT 9: ECAP9.DMA_INT Reset Source: mod_g_rst_n

3.7.23 CFG0_DMAXBAR3_GSEL Registers

3.7.23.1 CFG0_GSEL Register (Offset = 1C0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-362. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 61C0h

Figure 3-152. DMAXBAR3_GSEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													DMAXBAR3_GSEL_GSEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-363. DMAXBAR3_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	DMAXBAR3_GSEL_GSEL	R/W	0h	Select input source: 0: G0 selected .. 5: G5 selected Reset Source: mod_g_rst_n

3.7.24 CFG0_DMAXBAR3_G0 Registers

3.7.24.1 CFG0_G0 Register (Offset = 1C4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-364. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 61C4h

Figure 3-153. DMAXBAR3_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR3_G0_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-365. DMAXBAR3_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR3_G0_SEL	R/W	0h	ETPWM SOCA to corresponding xbar 1: PWMx.SOCA is selected 0: PWMx.SOCA is de-selected Reset Source: mod_g_rst_n

3.7.25 CFG0_DMAXBAR3_G1 Registers

3.7.25.1 CFG0_G1 Register (Offset = 1C8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-366. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 61C8h

Figure 3-154. DMAXBAR3_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR3_G1_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-367. DMAXBAR3_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR3_G1_SEL	R/W	0h	ETPWM SOCB to corresponding xbar 1: PWMx.SOCB is selected 0: PWMx.SOCB is de-selected Reset Source: mod_g_rst_n

3.7.26 CFG0_DMAXBAR3_G2 Registers

3.7.26.1 CFG0_G2 Register (Offset = 1CCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-368. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 61CCh

Figure 3-155. DMAXBAR3_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR3_G2_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-369. DMAXBAR3_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR3_G2_SEL	R/W	0h	ADC DMA requests to corresponding xbar 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.7.27 CFG0_DMAXBAR3_G3 Registers

3.7.27.1 CFG0_G3 Register (Offset = 1D0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-370. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 61D0h

Figure 3-156. DMAXBAR3_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DMAXBAR3_G3_SEL			
NONE												R/W			
0												0h			

Access Types Legend

Table 3-371. DMAXBAR3_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:0	DMAXBAR3_G3_SEL	R/W	0h	FSI DMA requests to corresponding xbar 0: FSIRX0.RX_DMA_EVT 1 FSIRX0_DMATRIG1 2: FSIRX0_DMATRIG2 3: FSIRX1.RX_DMA_EVT 4 FSIRX1_DMATRIG1 5: FSIRX1_DMATRIG2 6: FSIRX2.RX_DMA_EVT 7 FSIRX2_DMATRIG1 8: FSIRX2_DMATRIG2 9: FSIRX3.RX_DMA_EVT 10 FSIRX3_DMATRIG1 11: FSIRX3_DMATRIG2 12: FSITX0.TX_DMA_EVT 13: FSITX1.TX_DMA_EVT 14: FSITX2.TX_DMA_EVT 15: FSITX3.TX_DMA_EVT Reset Source: mod_g_rst_n

3.7.28 CFG0_DMAXBAR3_G4 Registers

3.7.28.1 CFG0_G4 Register (Offset = 1D4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-372. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 61D4h

Figure 3-157. DMAXBAR3_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													DMAXBAR3_G4_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-373. DMAXBAR3_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	DMAXBAR3_G4_SEL	R/W	0h	SDFM DMA requests to corresponding xbar 0: SD0.FILT1.DRINT 1: SD0.FILT2.DRINT 2: SD0.FILT3.DRINT 3: SD0.FILT4.DRINT 4: SD1.FILT1.DRINT 5: SD1.FILT2.DRINT 6: SD1.FILT3.DRINT 7: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.7.29 CFG0_DMAXBAR3_G5 Registers

3.7.29.1 CFG0_G5 Register (Offset = 1D8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-374. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 61D8h

Figure 3-158. DMAXBAR3_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DMAXBAR3_G5_SEL			
NONE												R/W			
0												0h			

Access Types Legend

Table 3-375. DMAXBAR3_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:0	DMAXBAR3_G5_SEL	R/W	0h	ECAP DMA requests to corresponding xbar 0: ECAP0.DMA_INT 1: ECAP1.DMA_INT 2: ECAP2.DMA_INT 3: ECAP3.DMA_INT 4: ECAP4.DMA_INT 5: ECAP5.DMA_INT 6: ECAP6.DMA_INT 7: ECAP7.DMA_INT 8: ECAP8.DMA_INT 9: ECAP9.DMA_INT Reset Source: mod_g_rst_n

3.7.30 CFG0_DMAXBAR4_GSEL Registers

3.7.30.1 CFG0_GSEL Register (Offset = 200h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-376. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6200h

Figure 3-159. DMAXBAR4_GSEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													DMAXBAR4_GSEL_GSEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-377. DMAXBAR4_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	DMAXBAR4_GSEL_GSEL	R/W	0h	Select input source: 0: G0 selected .. 5: G5 selected Reset Source: mod_g_rst_n

3.7.31 CFG0_DMAXBAR4_G0 Registers

3.7.31.1 CFG0_G0 Register (Offset = 204h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-378. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6204h

Figure 3-160. DMAXBAR4_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR4_G0_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-379. DMAXBAR4_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR4_G0_SEL	R/W	0h	ETPWM SOCA to corresponding xbar 1: PWMx.SOCA is selected 0: PWMx.SOCA is de-selected Reset Source: mod_g_rst_n

3.7.32 CFG0_DMAXBAR4_G1 Registers

3.7.32.1 CFG0_G1 Register (Offset = 208h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-380. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6208h

Figure 3-161. DMAXBAR4_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR4_G1_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-381. DMAXBAR4_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR4_G1_SEL	R/W	0h	ETPWM SOCB to corresponding xbar 1: PWMx.SOCB is selected 0: PWMx.SOCB is de-selected Reset Source: mod_g_rst_n

3.7.33 CFG0_DMAXBAR4_G2 Registers

3.7.33.1 CFG0_G2 Register (Offset = 20Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-382. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 620Ch

Figure 3-162. DMAXBAR4_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR4_G2_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-383. DMAXBAR4_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR4_G2_SEL	R/W	0h	ADC DMA requests to corresponding xbar 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.7.34 CFG0_DMAXBAR4_G3 Registers

3.7.34.1 CFG0_G3 Register (Offset = 210h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-384. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6210h

Figure 3-163. DMAXBAR4_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DMAXBAR4_G3_SEL			
NONE												R/W			
0												0h			

Access Types Legend

Table 3-385. DMAXBAR4_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:0	DMAXBAR4_G3_SEL	R/W	0h	FSI DMA requests to corresponding xbar 0: FSIRX0.RX_DMA_EVT 1 FSIRX0_DMATRIG1 2: FSIRX0_DMATRIG2 3: FSIRX1.RX_DMA_EVT 4 FSIRX1_DMATRIG1 5: FSIRX1_DMATRIG2 6: FSIRX2.RX_DMA_EVT 7 FSIRX2_DMATRIG1 8: FSIRX2_DMATRIG2 9: FSIRX3.RX_DMA_EVT 10 FSIRX3_DMATRIG1 11: FSIRX3_DMATRIG2 12: FSITX0.TX_DMA_EVT 13: FSITX1.TX_DMA_EVT 14: FSITX2.TX_DMA_EVT 15: FSITX3.TX_DMA_EVT Reset Source: mod_g_rst_n

3.7.35 CFG0_DMAXBAR4_G4 Registers

3.7.35.1 CFG0_G4 Register (Offset = 214h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-386. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6214h

Figure 3-164. DMAXBAR4_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													DMAXBAR4_G4_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-387. DMAXBAR4_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	DMAXBAR4_G4_SEL	R/W	0h	SDFM DMA requests to corresponding xbar 0: SD0.FILT1.DRINT 1: SD0.FILT2.DRINT 2: SD0.FILT3.DRINT 3: SD0.FILT4.DRINT 4: SD1.FILT1.DRINT 5: SD1.FILT2.DRINT 6: SD1.FILT3.DRINT 7: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.7.36 CFG0_DMAXBAR4_G5 Registers

3.7.36.1 CFG0_G5 Register (Offset = 218h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-388. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6218h

Figure 3-165. DMAXBAR4_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DMAXBAR4_G5_SEL			
NONE												R/W			
0												0h			

Access Types Legend

Table 3-389. DMAXBAR4_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:0	DMAXBAR4_G5_SEL	R/W	0h	ECAP DMA requests to corresponding xbar 0: ECAP0.DMA_INT 1: ECAP1.DMA_INT 2: ECAP2.DMA_INT 3: ECAP3.DMA_INT 4: ECAP4.DMA_INT 5: ECAP5.DMA_INT 6: ECAP6.DMA_INT 7: ECAP7.DMA_INT 8: ECAP8.DMA_INT 9: ECAP9.DMA_INT Reset Source: mod_g_rst_n

3.7.37 CFG0_DMAXBAR5_GSEL Registers

3.7.37.1 CFG0_GSEL Register (Offset = 240h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-390. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6240h

Figure 3-166. DMAXBAR5_GSEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													DMAXBAR5_GSEL_GSEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-391. DMAXBAR5_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	DMAXBAR5_GSEL_GSEL	R/W	0h	Select input source: 0: G0 selected .. 5: G5 selected Reset Source: mod_g_rst_n

3.7.38 CFG0_DMAXBAR5_G0 Registers

3.7.38.1 CFG0_G0 Register (Offset = 244h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-392. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6244h

Figure 3-167. DMAXBAR5_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR5_G0_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-393. DMAXBAR5_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR5_G0_SEL	R/W	0h	ETPWM SOCA to corresponding xbar 1: PWMx.SOCA is selected 0: PWMx.SOCA is de-selected Reset Source: mod_g_rst_n

3.7.39 CFG0_DMAXBAR5_G1 Registers

3.7.39.1 CFG0_G1 Register (Offset = 248h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-394. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6248h

Figure 3-168. DMAXBAR5_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR5_G1_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-395. DMAXBAR5_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR5_G1_SEL	R/W	0h	ETPWM SOCB to corresponding xbar 1: PWMx.SOCB is selected 0: PWMx.SOCB is de-selected Reset Source: mod_g_rst_n

3.7.40 CFG0_DMAXBAR5_G2 Registers

3.7.40.1 CFG0_G2 Register (Offset = 24Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-396. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 624Ch

Figure 3-169. DMAXBAR5_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR5_G2_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-397. DMAXBAR5_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR5_G2_SEL	R/W	0h	ADC DMA requests to corresponding xbar 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.7.41 CFG0_DMAXBAR5_G3 Registers

3.7.41.1 CFG0_G3 Register (Offset = 250h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-398. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6250h

Figure 3-170. DMAXBAR5_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DMAXBAR5_G3_SEL			
NONE												R/W			
0												0h			

Access Types Legend

Table 3-399. DMAXBAR5_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:0	DMAXBAR5_G3_SEL	R/W	0h	FSI DMA requests to corresponding xbar 0: FSIRX0.RX_DMA_EVT 1 FSIRX0_DMATRIG1 2: FSIRX0_DMATRIG2 3: FSIRX1.RX_DMA_EVT 4 FSIRX1_DMATRIG1 5: FSIRX1_DMATRIG2 6: FSIRX2.RX_DMA_EVT 7 FSIRX2_DMATRIG1 8: FSIRX2_DMATRIG2 9: FSIRX3.RX_DMA_EVT 10 FSIRX3_DMATRIG1 11: FSIRX3_DMATRIG2 12: FSITX0.TX_DMA_EVT 13: FSITX1.TX_DMA_EVT 14: FSITX2.TX_DMA_EVT 15: FSITX3.TX_DMA_EVT Reset Source: mod_g_rst_n

3.7.42 CFG0_DMAXBAR5_G4 Registers

3.7.42.1 CFG0_G4 Register (Offset = 254h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-400. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6254h

Figure 3-171. DMAXBAR5_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													DMAXBAR5_G4_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-401. DMAXBAR5_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	DMAXBAR5_G4_SEL	R/W	0h	SDFM DMA requests to corresponding xbar 0: SD0.FILT1.DRINT 1: SD0.FILT2.DRINT 2: SD0.FILT3.DRINT 3: SD0.FILT4.DRINT 4: SD1.FILT1.DRINT 5: SD1.FILT2.DRINT 6: SD1.FILT3.DRINT 7: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.7.43 CFG0_DMAXBAR5_G5 Registers

3.7.43.1 CFG0_G5 Register (Offset = 258h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-402. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6258h

Figure 3-172. DMAXBAR5_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DMAXBAR5_G5_SEL			
NONE												R/W			
0												0h			

Access Types Legend

Table 3-403. DMAXBAR5_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:0	DMAXBAR5_G5_SEL	R/W	0h	ECAP DMA requests to corresponding xbar 0: ECAP0.DMA_INT 1: ECAP1.DMA_INT 2: ECAP2.DMA_INT 3: ECAP3.DMA_INT 4: ECAP4.DMA_INT 5: ECAP5.DMA_INT 6: ECAP6.DMA_INT 7: ECAP7.DMA_INT 8: ECAP8.DMA_INT 9: ECAP9.DMA_INT Reset Source: mod_g_rst_n

3.7.44 CFG0_DMAXBAR6_GSEL Registers

3.7.44.1 CFG0_GSEL Register (Offset = 280h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-404. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6280h

Figure 3-173. DMAXBAR6_GSEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													DMAXBAR6_GSEL_GSEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-405. DMAXBAR6_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	DMAXBAR6_GSEL_GSEL	R/W	0h	Select input source: 0: G0 selected .. 5: G5 selected Reset Source: mod_g_rst_n

3.7.45 CFG0_DMAXBAR6_G0 Registers

3.7.45.1 CFG0_G0 Register (Offset = 284h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-406. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6284h

Figure 3-174. DMAXBAR6_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR6_G0_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-407. DMAXBAR6_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR6_G0_SEL	R/W	0h	ETPWM SOCA to corresponding xbar 1: PWMx.SOCA is selected 0: PWMx.SOCA is de-selected Reset Source: mod_g_rst_n

3.7.46 CFG0_DMAXBAR6_G1 Registers

3.7.46.1 CFG0_G1 Register (Offset = 288h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-408. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6288h

Figure 3-175. DMAXBAR6_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR6_G1_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-409. DMAXBAR6_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR6_G1_SEL	R/W	0h	ETPWM SOCB to corresponding xbar 1: PWMx.SOCB is selected 0: PWMx.SOCB is de-selected Reset Source: mod_g_rst_n

3.7.47 CFG0_DMAXBAR6_G2 Registers

3.7.47.1 CFG0_G2 Register (Offset = 28Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-410. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 628Ch

Figure 3-176. DMAXBAR6_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR6_G2_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-411. DMAXBAR6_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR6_G2_SEL	R/W	0h	ADC DMA requests to corresponding xbar 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.7.48 CFG0_DMAXBAR6_G3 Registers

3.7.48.1 CFG0_G3 Register (Offset = 290h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-412. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6290h

Figure 3-177. DMAXBAR6_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DMAXBAR6_G3_SEL			
NONE												R/W			
0												0h			

Access Types Legend

Table 3-413. DMAXBAR6_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:0	DMAXBAR6_G3_SEL	R/W	0h	FSI DMA requests to corresponding xbar 0: FSIRX0.RX_DMA_EVT 1 FSIRX0_DMATRIG1 2: FSIRX0_DMATRIG2 3: FSIRX1.RX_DMA_EVT 4 FSIRX1_DMATRIG1 5: FSIRX1_DMATRIG2 6: FSIRX2.RX_DMA_EVT 7 FSIRX2_DMATRIG1 8: FSIRX2_DMATRIG2 9: FSIRX3.RX_DMA_EVT 10 FSIRX3_DMATRIG1 11: FSIRX3_DMATRIG2 12: FSITX0.TX_DMA_EVT 13: FSITX1.TX_DMA_EVT 14: FSITX2.TX_DMA_EVT 15: FSITX3.TX_DMA_EVT Reset Source: mod_g_rst_n

3.7.49 CFG0_DMAXBAR6_G4 Registers

3.7.49.1 CFG0_G4 Register (Offset = 294h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-414. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6294h

Figure 3-178. DMAXBAR6_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															DMAXBAR6_G4_SEL
NONE															R/W
0															0h

Access Types Legend

Table 3-415. DMAXBAR6_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	DMAXBAR6_G4_SEL	R/W	0h	SDFM DMA requests to corresponding xbar 0: SD0.FILT1.DRINT 1: SD0.FILT2.DRINT 2: SD0.FILT3.DRINT 3: SD0.FILT4.DRINT 4: SD1.FILT1.DRINT 5: SD1.FILT2.DRINT 6: SD1.FILT3.DRINT 7: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.7.50 CFG0_DMAXBAR6_G5 Registers

3.7.50.1 CFG0_G5 Register (Offset = 298h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-416. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6298h

Figure 3-179. DMAXBAR6_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DMAXBAR6_G5_SEL			
NONE												R/W			
0												0h			

Access Types Legend

Table 3-417. DMAXBAR6_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:0	DMAXBAR6_G5_SEL	R/W	0h	ECAP DMA requests to corresponding xbar 0: ECAP0.DMA_INT 1: ECAP1.DMA_INT 2: ECAP2.DMA_INT 3: ECAP3.DMA_INT 4: ECAP4.DMA_INT 5: ECAP5.DMA_INT 6: ECAP6.DMA_INT 7: ECAP7.DMA_INT 8: ECAP8.DMA_INT 9: ECAP9.DMA_INT Reset Source: mod_g_rst_n

3.7.51 CFG0_DMAXBAR7_GSEL Registers

3.7.51.1 CFG0_GSEL Register (Offset = 2C0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-418. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 62C0h

Figure 3-180. DMAXBAR7_GSEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													DMAXBAR7_GSEL_GSEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-419. DMAXBAR7_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	DMAXBAR7_GSEL_GSEL	R/W	0h	Select input source: 0: G0 selected .. 5: G5 selected Reset Source: mod_g_rst_n

3.7.52 CFG0_DMAXBAR7_G0 Registers

3.7.52.1 CFG0_G0 Register (Offset = 2C4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-420. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 62C4h

Figure 3-181. DMAXBAR7_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR7_G0_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-421. DMAXBAR7_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR7_G0_SEL	R/W	0h	ETPWM SOCA to corresponding xbar 1: PWMx.SOCA is selected 0: PWMx.SOCA is de-selected Reset Source: mod_g_rst_n

3.7.53 CFG0_DMAXBAR7_G1 Registers

3.7.53.1 CFG0_G1 Register (Offset = 2C8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-422. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 62C8h

Figure 3-182. DMAXBAR7_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR7_G1_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-423. DMAXBAR7_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR7_G1_SEL	R/W	0h	ETPWM SOCB to corresponding xbar 1: PWMx.SOCB is selected 0: PWMx.SOCB is de-selected Reset Source: mod_g_rst_n

3.7.54 CFG0_DMAXBAR7_G2 Registers

3.7.54.1 CFG0_G2 Register (Offset = 2CCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-424. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 62CCh

Figure 3-183. DMAXBAR7_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR7_G2_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-425. DMAXBAR7_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR7_G2_SEL	R/W	0h	ADC DMA requests to corresponding xbar 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.7.55 CFG0_DMAXBAR7_G3 Registers

3.7.55.1 CFG0_G3 Register (Offset = 2D0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-426. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 62D0h

Figure 3-184. DMAXBAR7_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DMAXBAR7_G3_SEL			
NONE												R/W			
0												0h			

Access Types Legend

Table 3-427. DMAXBAR7_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:0	DMAXBAR7_G3_SEL	R/W	0h	FSI DMA requests to corresponding xbar 0: FSIRX0.RX_DMA_EVT 1 FSIRX0_DMATRIG1 2: FSIRX0_DMATRIG2 3: FSIRX1.RX_DMA_EVT 4 FSIRX1_DMATRIG1 5: FSIRX1_DMATRIG2 6: FSIRX2.RX_DMA_EVT 7 FSIRX2_DMATRIG1 8: FSIRX2_DMATRIG2 9: FSIRX3.RX_DMA_EVT 10 FSIRX3_DMATRIG1 11: FSIRX3_DMATRIG2 12: FSITX0.TX_DMA_EVT 13: FSITX1.TX_DMA_EVT 14: FSITX2.TX_DMA_EVT 15: FSITX3.TX_DMA_EVT Reset Source: mod_g_rst_n

3.7.56 CFG0_DMAXBAR7_G4 Registers

3.7.56.1 CFG0_G4 Register (Offset = 2D4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-428. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 62D4h

Figure 3-185. DMAXBAR7_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													DMAXBAR7_G4_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-429. DMAXBAR7_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	DMAXBAR7_G4_SEL	R/W	0h	SDFM DMA requests to corresponding xbar 0: SD0.FILT1.DRINT 1: SD0.FILT2.DRINT 2: SD0.FILT3.DRINT 3: SD0.FILT4.DRINT 4: SD1.FILT1.DRINT 5: SD1.FILT2.DRINT 6: SD1.FILT3.DRINT 7: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.7.57 CFG0_DMAXBAR7_G5 Registers

3.7.57.1 CFG0_G5 Register (Offset = 2D8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-430. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 62D8h

Figure 3-186. DMAXBAR7_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DMAXBAR7_G5_SEL			
NONE												R/W			
0												0h			

Access Types Legend

Table 3-431. DMAXBAR7_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:0	DMAXBAR7_G5_SEL	R/W	0h	ECAP DMA requests to corresponding xbar 0: ECAP0.DMA_INT 1: ECAP1.DMA_INT 2: ECAP2.DMA_INT 3: ECAP3.DMA_INT 4: ECAP4.DMA_INT 5: ECAP5.DMA_INT 6: ECAP6.DMA_INT 7: ECAP7.DMA_INT 8: ECAP8.DMA_INT 9: ECAP9.DMA_INT Reset Source: mod_g_rst_n

3.7.58 CFG0_DMAXBAR8_GSEL Registers

3.7.58.1 CFG0_GSEL Register (Offset = 300h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-432. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6300h

Figure 3-187. DMAXBAR8_GSEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													DMAXBAR8_GSEL_GSEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-433. DMAXBAR8_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	DMAXBAR8_GSEL_GSEL	R/W	0h	Select input source: 0: G0 selected .. 5: G5 selected Reset Source: mod_g_rst_n

3.7.59 CFG0_DMAXBAR8_G0 Registers

3.7.59.1 CFG0_G0 Register (Offset = 304h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-434. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6304h

Figure 3-188. DMAXBAR8_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR8_G0_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-435. DMAXBAR8_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR8_G0_SEL	R/W	0h	ETPWM SOCA to corresponding xbar 1: PWMx.SOCA is selected 0: PWMx.SOCA is de-selected Reset Source: mod_g_rst_n

3.7.60 CFG0_DMAXBAR8_G1 Registers

3.7.60.1 CFG0_G1 Register (Offset = 308h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-436. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6308h

Figure 3-189. DMAXBAR8_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR8_G1_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-437. DMAXBAR8_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR8_G1_SEL	R/W	0h	ETPWM SOCB to corresponding xbar 1: PWMx.SOCB is selected 0: PWMx.SOCB is de-selected Reset Source: mod_g_rst_n

3.7.61 CFG0_DMAXBAR8_G2 Registers

3.7.61.1 CFG0_G2 Register (Offset = 30Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-438. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 630Ch

Figure 3-190. DMAXBAR8_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR8_G2_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-439. DMAXBAR8_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR8_G2_SEL	R/W	0h	ADC DMA requests to corresponding xbar 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.7.62 CFG0_DMAXBAR8_G3 Registers

3.7.62.1 CFG0_G3 Register (Offset = 310h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-440. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6310h

Figure 3-191. DMAXBAR8_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DMAXBAR8_G3_SEL			
NONE												R/W			
0												0h			

Access Types Legend

Table 3-441. DMAXBAR8_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:0	DMAXBAR8_G3_SEL	R/W	0h	FSI DMA requests to corresponding xbar 0: FSIRX0.RX_DMA_EVT 1 FSIRX0_DMATRIG1 2: FSIRX0_DMATRIG2 3: FSIRX1.RX_DMA_EVT 4 FSIRX1_DMATRIG1 5: FSIRX1_DMATRIG2 6: FSIRX2.RX_DMA_EVT 7 FSIRX2_DMATRIG1 8: FSIRX2_DMATRIG2 9: FSIRX3.RX_DMA_EVT 10 FSIRX3_DMATRIG1 11: FSIRX3_DMATRIG2 12: FSITX0.TX_DMA_EVT 13: FSITX1.TX_DMA_EVT 14: FSITX2.TX_DMA_EVT 15: FSITX3.TX_DMA_EVT Reset Source: mod_g_rst_n

3.7.63 CFG0_DMAXBAR8_G4 Registers

3.7.63.1 CFG0_G4 Register (Offset = 314h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-442. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6314h

Figure 3-192. DMAXBAR8_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															DMAXBAR8_G4_SEL
NONE															R/W
0															0h

Access Types Legend

Table 3-443. DMAXBAR8_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	DMAXBAR8_G4_SEL	R/W	0h	SDFM DMA requests to corresponding xbar 0: SD0.FILT1.DRINT 1: SD0.FILT2.DRINT 2: SD0.FILT3.DRINT 3: SD0.FILT4.DRINT 4: SD1.FILT1.DRINT 5: SD1.FILT2.DRINT 6: SD1.FILT3.DRINT 7: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.7.64 CFG0_DMAXBAR8_G5 Registers

3.7.64.1 CFG0_G5 Register (Offset = 318h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-444. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6318h

Figure 3-193. DMAXBAR8_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DMAXBAR8_G5_SEL			
NONE												R/W			
0												0h			

Access Types Legend

Table 3-445. DMAXBAR8_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:0	DMAXBAR8_G5_SEL	R/W	0h	ECAP DMA requests to corresponding xbar 0: ECAP0.DMA_INT 1: ECAP1.DMA_INT 2: ECAP2.DMA_INT 3: ECAP3.DMA_INT 4: ECAP4.DMA_INT 5: ECAP5.DMA_INT 6: ECAP6.DMA_INT 7: ECAP7.DMA_INT 8: ECAP8.DMA_INT 9: ECAP9.DMA_INT Reset Source: mod_g_rst_n

3.7.65 CFG0_DMAXBAR9_GSEL Registers

3.7.65.1 CFG0_GSEL Register (Offset = 340h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-446. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6340h

Figure 3-194. DMAXBAR9_GSEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													DMAXBAR9_GSEL_GSEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-447. DMAXBAR9_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	DMAXBAR9_GSEL_GSEL	R/W	0h	Select input source: 0: G0 selected .. 5: G5 selected Reset Source: mod_g_rst_n

3.7.66 CFG0_DMAXBAR9_G0 Registers

3.7.66.1 CFG0_G0 Register (Offset = 344h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-448. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6344h

Figure 3-195. DMAXBAR9_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR9_G0_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-449. DMAXBAR9_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR9_G0_SEL	R/W	0h	ETPWM SOCA to corresponding xbar 1: PWMx.SOCA is selected 0: PWMx.SOCA is de-selected Reset Source: mod_g_rst_n

3.7.67 CFG0_DMAXBAR9_G1 Registers

3.7.67.1 CFG0_G1 Register (Offset = 348h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-450. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6348h

Figure 3-196. DMAXBAR9_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR9_G1_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-451. DMAXBAR9_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR9_G1_SEL	R/W	0h	ETPWM SOCB to corresponding xbar 1: PWMx.SOCB is selected 0: PWMx.SOCB is de-selected Reset Source: mod_g_rst_n

3.7.68 CFG0_DMAXBAR9_G2 Registers

3.7.68.1 CFG0_G2 Register (Offset = 34Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-452. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 634Ch

Figure 3-197. DMAXBAR9_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR9_G2_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-453. DMAXBAR9_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR9_G2_SEL	R/W	0h	ADC DMA requests to corresponding xbar 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.7.69 CFG0_DMAXBAR9_G3 Registers

3.7.69.1 CFG0_G3 Register (Offset = 350h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-454. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6350h

Figure 3-198. DMAXBAR9_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DMAXBAR9_G3_SEL			
NONE												R/W			
0												0h			

Access Types Legend

Table 3-455. DMAXBAR9_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:0	DMAXBAR9_G3_SEL	R/W	0h	FSI DMA requests to corresponding xbar 0: FSIRX0.RX_DMA_EVT 1 FSIRX0_DMATRIG1 2: FSIRX0_DMATRIG2 3: FSIRX1.RX_DMA_EVT 4 FSIRX1_DMATRIG1 5: FSIRX1_DMATRIG2 6: FSIRX2.RX_DMA_EVT 7 FSIRX2_DMATRIG1 8: FSIRX2_DMATRIG2 9: FSIRX3.RX_DMA_EVT 10 FSIRX3_DMATRIG1 11: FSIRX3_DMATRIG2 12: FSITX0.TX_DMA_EVT 13: FSITX1.TX_DMA_EVT 14: FSITX2.TX_DMA_EVT 15: FSITX3.TX_DMA_EVT Reset Source: mod_g_rst_n

3.7.70 CFG0_DMAXBAR9_G4 Registers

3.7.70.1 CFG0_G4 Register (Offset = 354h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-456. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6354h

Figure 3-199. DMAXBAR9_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													DMAXBAR9_G4_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-457. DMAXBAR9_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	DMAXBAR9_G4_SEL	R/W	0h	SDFM DMA requests to corresponding xbar 0: SD0.FILT1.DRINT 1: SD0.FILT2.DRINT 2: SD0.FILT3.DRINT 3: SD0.FILT4.DRINT 4: SD1.FILT1.DRINT 5: SD1.FILT2.DRINT 6: SD1.FILT3.DRINT 7: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.7.71 CFG0_DMAXBAR9_G5 Registers

3.7.71.1 CFG0_G5 Register (Offset = 358h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-458. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6358h

Figure 3-200. DMAXBAR9_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DMAXBAR9_G5_SEL			
NONE												R/W			
0												0h			

Access Types Legend

Table 3-459. DMAXBAR9_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:0	DMAXBAR9_G5_SEL	R/W	0h	ECAP DMA requests to corresponding xbar 0: ECAP0.DMA_INT 1: ECAP1.DMA_INT 2: ECAP2.DMA_INT 3: ECAP3.DMA_INT 4: ECAP4.DMA_INT 5: ECAP5.DMA_INT 6: ECAP6.DMA_INT 7: ECAP7.DMA_INT 8: ECAP8.DMA_INT 9: ECAP9.DMA_INT Reset Source: mod_g_rst_n

3.7.72 CFG0_DMAXBAR10_GSEL Registers

3.7.72.1 CFG0_GSEL Register (Offset = 380h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-460. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6380h

Figure 3-201. DMAXBAR10_GSEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													DMAXBAR10_GSEL_GSEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-461. DMAXBAR10_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	DMAXBAR10_GSEL_GSEL	R/W	0h	Select input source: 0: G0 selected .. 5: G5 selected Reset Source: mod_g_rst_n

3.7.73 CFG0_DMAXBAR10_G0 Registers

3.7.73.1 CFG0_G0 Register (Offset = 384h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-462. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6384h

Figure 3-202. DMAXBAR10_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR10_G0_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-463. DMAXBAR10_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR10_G0_SEL	R/W	0h	ETPWM SOCA to corresponding xbar 1: PWMx.SOCA is selected 0: PWMx.SOCA is de-selected Reset Source: mod_g_rst_n

3.7.74 CFG0_DMAXBAR10_G1 Registers

3.7.74.1 CFG0_G1 Register (Offset = 388h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-464. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6388h

Figure 3-203. DMAXBAR10_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR10_G1_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-465. DMAXBAR10_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR10_G1_SEL	R/W	0h	ETPWM SOCB to corresponding xbar 1: PWMx.SOCB is selected 0: PWMx.SOCB is de-selected Reset Source: mod_g_rst_n

3.7.75 CFG0_DMAXBAR10_G2 Registers

3.7.75.1 CFG0_G2 Register (Offset = 38Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-466. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 638Ch

Figure 3-204. DMAXBAR10_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR10_G2_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-467. DMAXBAR10_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR10_G2_SEL	R/W	0h	ADC DMA requests to corresponding xbar 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.7.76 CFG0_DMAXBAR10_G3 Registers

3.7.76.1 CFG0_G3 Register (Offset = 390h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-468. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6390h

Figure 3-205. DMAXBAR10_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DMAXBAR10_G3_SEL			
NONE												R/W			
0												0h			

Access Types Legend

Table 3-469. DMAXBAR10_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:0	DMAXBAR10_G3_SEL	R/W	0h	FSI DMA requests to corresponding xbar 0: FSIRX0.RX_DMA_EVT 1 FSIRX0_DMATRIG1 2: FSIRX0_DMATRIG2 3: FSIRX1.RX_DMA_EVT 4 FSIRX1_DMATRIG1 5: FSIRX1_DMATRIG2 6: FSIRX2.RX_DMA_EVT 7 FSIRX2_DMATRIG1 8: FSIRX2_DMATRIG2 9: FSIRX3.RX_DMA_EVT 10 FSIRX3_DMATRIG1 11: FSIRX3_DMATRIG2 12: FSITX0.TX_DMA_EVT 13: FSITX1.TX_DMA_EVT 14: FSITX2.TX_DMA_EVT 15: FSITX3.TX_DMA_EVT Reset Source: mod_g_rst_n

3.7.77 CFG0_DMAXBAR10_G4 Registers

3.7.77.1 CFG0_G4 Register (Offset = 394h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-470. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6394h

Figure 3-206. DMAXBAR10_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													DMAXBAR10_G4_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-471. DMAXBAR10_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	DMAXBAR10_G4_SEL	R/W	0h	SDFM DMA requests to corresponding xbar 0: SD0.FILT1.DRINT 1: SD0.FILT2.DRINT 2: SD0.FILT3.DRINT 3: SD0.FILT4.DRINT 4: SD1.FILT1.DRINT 5: SD1.FILT2.DRINT 6: SD1.FILT3.DRINT 7: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.7.78 CFG0_DMAXBAR10_G5 Registers

3.7.78.1 CFG0_G5 Register (Offset = 398h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-472. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6398h

Figure 3-207. DMAXBAR10_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DMAXBAR10_G5_SEL			
NONE												R/W			
0												0h			

Access Types Legend

Table 3-473. DMAXBAR10_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:0	DMAXBAR10_G5_SEL	R/W	0h	ECAP DMA requests to corresponding xbar 0: ECAP0.DMA_INT 1: ECAP1.DMA_INT 2: ECAP2.DMA_INT 3: ECAP3.DMA_INT 4: ECAP4.DMA_INT 5: ECAP5.DMA_INT 6: ECAP6.DMA_INT 7: ECAP7.DMA_INT 8: ECAP8.DMA_INT 9: ECAP9.DMA_INT Reset Source: mod_g_rst_n

3.7.79 CFG0_DMAXBAR11_GSEL Registers

3.7.79.1 CFG0_GSEL Register (Offset = 3C0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-474. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 63C0h

Figure 3-208. DMAXBAR11_GSEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													DMAXBAR11_GSEL_GSEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-475. DMAXBAR11_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	DMAXBAR11_GSEL_GSEL	R/W	0h	Select input source: 0: G0 selected .. 5: G5 selected Reset Source: mod_g_rst_n

3.7.80 CFG0_DMAXBAR11_G0 Registers

3.7.80.1 CFG0_G0 Register (Offset = 3C4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-476. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 63C4h

Figure 3-209. DMAXBAR11_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR11_G0_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-477. DMAXBAR11_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR11_G0_SEL	R/W	0h	ETPWM SOCA to corresponding xbar 1: PWMx.SOCA is selected 0: PWMx.SOCA is de-selected Reset Source: mod_g_rst_n

3.7.81 CFG0_DMAXBAR11_G1 Registers

3.7.81.1 CFG0_G1 Register (Offset = 3C8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-478. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 63C8h

Figure 3-210. DMAXBAR11_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR11_G1_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-479. DMAXBAR11_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR11_G1_SEL	R/W	0h	ETPWM SOCB to corresponding xbar 1: PWMx.SOCB is selected 0: PWMx.SOCB is de-selected Reset Source: mod_g_rst_n

3.7.82 CFG0_DMAXBAR11_G2 Registers

3.7.82.1 CFG0_G2 Register (Offset = 3CCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-480. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 63CCh

Figure 3-211. DMAXBAR11_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR11_G2_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-481. DMAXBAR11_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR11_G2_SEL	R/W	0h	ADC DMA requests to corresponding xbar 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.7.83 CFG0_DMAXBAR11_G3 Registers

3.7.83.1 CFG0_G3 Register (Offset = 3D0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-482. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 63D0h

Figure 3-212. DMAXBAR11_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DMAXBAR11_G3_SEL			
NONE												R/W			
0												0h			

Access Types Legend

Table 3-483. DMAXBAR11_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:0	DMAXBAR11_G3_SEL	R/W	0h	FSI DMA requests to corresponding xbar 0: FSIRX0.RX_DMA_EVT 1 FSIRX0_DMATRIG1 2: FSIRX0_DMATRIG2 3: FSIRX1.RX_DMA_EVT 4 FSIRX1_DMATRIG1 5: FSIRX1_DMATRIG2 6: FSIRX2.RX_DMA_EVT 7 FSIRX2_DMATRIG1 8: FSIRX2_DMATRIG2 9: FSIRX3.RX_DMA_EVT 10 FSIRX3_DMATRIG1 11: FSIRX3_DMATRIG2 12: FSITX0.TX_DMA_EVT 13: FSITX1.TX_DMA_EVT 14: FSITX2.TX_DMA_EVT 15: FSITX3.TX_DMA_EVT Reset Source: mod_g_rst_n

3.7.84 CFG0_DMAXBAR11_G4 Registers

3.7.84.1 CFG0_G4 Register (Offset = 3D4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-484. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 63D4h

Figure 3-213. DMAXBAR11_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													DMAXBAR11_G4_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-485. DMAXBAR11_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	DMAXBAR11_G4_SEL	R/W	0h	SDFM DMA requests to corresponding xbar 0: SD0.FILT1.DRINT 1: SD0.FILT2.DRINT 2: SD0.FILT3.DRINT 3: SD0.FILT4.DRINT 4: SD1.FILT1.DRINT 5: SD1.FILT2.DRINT 6: SD1.FILT3.DRINT 7: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.7.85 CFG0_DMAXBAR11_G5 Registers

3.7.85.1 CFG0_G5 Register (Offset = 3D8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-486. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 63D8h

Figure 3-214. DMAXBAR11_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DMAXBAR11_G5_SEL			
NONE												R/W			
0												0h			

Access Types Legend

Table 3-487. DMAXBAR11_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:0	DMAXBAR11_G5_SEL	R/W	0h	ECAP DMA requests to corresponding xbar 0: ECAP0.DMA_INT 1: ECAP1.DMA_INT 2: ECAP2.DMA_INT 3: ECAP3.DMA_INT 4: ECAP4.DMA_INT 5: ECAP5.DMA_INT 6: ECAP6.DMA_INT 7: ECAP7.DMA_INT 8: ECAP8.DMA_INT 9: ECAP9.DMA_INT Reset Source: mod_g_rst_n

3.7.86 CFG0_DMAXBAR12_GSEL Registers

3.7.86.1 CFG0_GSEL Register (Offset = 400h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-488. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6400h

Figure 3-215. DMAXBAR12_GSEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													DMAXBAR12_GSEL_GSEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-489. DMAXBAR12_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	DMAXBAR12_GSEL_GSEL	R/W	0h	Select input source: 0: G0 selected .. 5: G5 selected Reset Source: mod_g_rst_n

3.7.87 CFG0_DMAXBAR12_G0 Registers

3.7.87.1 CFG0_G0 Register (Offset = 404h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-490. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6404h

Figure 3-216. DMAXBAR12_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR12_G0_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-491. DMAXBAR12_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR12_G0_SEL	R/W	0h	ETPWM SOCA to corresponding xbar 1: PWMx.SOCA is selected 0: PWMx.SOCA is de-selected Reset Source: mod_g_rst_n

3.7.88 CFG0_DMAXBAR12_G1 Registers

3.7.88.1 CFG0_G1 Register (Offset = 408h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-492. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6408h

Figure 3-217. DMAXBAR12_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR12_G1_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-493. DMAXBAR12_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR12_G1_SEL	R/W	0h	ETPWM SOCB to corresponding xbar 1: PWMx.SOCB is selected 0: PWMx.SOCB is de-selected Reset Source: mod_g_rst_n

3.7.89 CFG0_DMAXBAR12_G2 Registers

3.7.89.1 CFG0_G2 Register (Offset = 40Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-494. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 640Ch

Figure 3-218. DMAXBAR12_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR12_G2_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-495. DMAXBAR12_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR12_G2_SEL	R/W	0h	ADC DMA requests to corresponding xbar 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.7.90 CFG0_DMAXBAR12_G3 Registers

3.7.90.1 CFG0_G3 Register (Offset = 410h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-496. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6410h

Figure 3-219. DMAXBAR12_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DMAXBAR12_G3_SEL			
NONE												R/W			
0												0h			

Access Types Legend

Table 3-497. DMAXBAR12_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:0	DMAXBAR12_G3_SEL	R/W	0h	FSI DMA requests to corresponding xbar 0: FSIRX0.RX_DMA_EVT 1 FSIRX0_DMATRIG1 2: FSIRX0_DMATRIG2 3: FSIRX1.RX_DMA_EVT 4 FSIRX1_DMATRIG1 5: FSIRX1_DMATRIG2 6: FSIRX2.RX_DMA_EVT 7 FSIRX2_DMATRIG1 8: FSIRX2_DMATRIG2 9: FSIRX3.RX_DMA_EVT 10 FSIRX3_DMATRIG1 11: FSIRX3_DMATRIG2 12: FSITX0.TX_DMA_EVT 13: FSITX1.TX_DMA_EVT 14: FSITX2.TX_DMA_EVT 15: FSITX3.TX_DMA_EVT Reset Source: mod_g_rst_n

3.7.91 CFG0_DMAXBAR12_G4 Registers

3.7.91.1 CFG0_G4 Register (Offset = 414h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-498. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6414h

Figure 3-220. DMAXBAR12_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													DMAXBAR12_G4_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-499. DMAXBAR12_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	DMAXBAR12_G4_SEL	R/W	0h	SDFM DMA requests to corresponding xbar 0: SD0.FILT1.DRINT 1: SD0.FILT2.DRINT 2: SD0.FILT3.DRINT 3: SD0.FILT4.DRINT 4: SD1.FILT1.DRINT 5: SD1.FILT2.DRINT 6: SD1.FILT3.DRINT 7: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.7.92 CFG0_DMAXBAR12_G5 Registers

3.7.92.1 CFG0_G5 Register (Offset = 418h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-500. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6418h

Figure 3-221. DMAXBAR12_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DMAXBAR12_G5_SEL			
NONE												R/W			
0												0h			

Access Types Legend

Table 3-501. DMAXBAR12_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:0	DMAXBAR12_G5_SEL	R/W	0h	ECAP DMA requests to corresponding xbar 0: ECAP0.DMA_INT 1: ECAP1.DMA_INT 2: ECAP2.DMA_INT 3: ECAP3.DMA_INT 4: ECAP4.DMA_INT 5: ECAP5.DMA_INT 6: ECAP6.DMA_INT 7: ECAP7.DMA_INT 8: ECAP8.DMA_INT 9: ECAP9.DMA_INT Reset Source: mod_g_rst_n

3.7.93 CFG0_DMAXBAR13_GSEL Registers

3.7.93.1 CFG0_GSEL Register (Offset = 440h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-502. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6440h

Figure 3-222. DMAXBAR13_GSEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													DMAXBAR13_GSEL_GSEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-503. DMAXBAR13_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	DMAXBAR13_GSEL_GSEL	R/W	0h	Select input source: 0: G0 selected .. 5: G5 selected Reset Source: mod_g_rst_n

3.7.94 CFG0_DMAXBAR13_G0 Registers

3.7.94.1 CFG0_G0 Register (Offset = 444h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-504. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6444h

Figure 3-223. DMAXBAR13_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR13_G0_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-505. DMAXBAR13_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR13_G0_SEL	R/W	0h	ETPWM SOCA to corresponding xbar 1: PWMx.SOCA is selected 0: PWMx.SOCA is de-selected Reset Source: mod_g_rst_n

3.7.95 CFG0_DMAXBAR13_G1 Registers

3.7.95.1 CFG0_G1 Register (Offset = 448h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-506. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6448h

Figure 3-224. DMAXBAR13_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR13_G1_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-507. DMAXBAR13_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR13_G1_SEL	R/W	0h	ETPWM SOCB to corresponding xbar 1: PWMx.SOCB is selected 0: PWMx.SOCB is de-selected Reset Source: mod_g_rst_n

3.7.96 CFG0_DMAXBAR13_G2 Registers

3.7.96.1 CFG0_G2 Register (Offset = 44Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-508. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 644Ch

Figure 3-225. DMAXBAR13_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR13_G2_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-509. DMAXBAR13_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR13_G2_SEL	R/W	0h	ADC DMA requests to corresponding xbar 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.7.97 CFG0_DMAXBAR13_G3 Registers

3.7.97.1 CFG0_G3 Register (Offset = 450h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-510. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6450h

Figure 3-226. DMAXBAR13_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DMAXBAR13_G3_SEL			
NONE												R/W			
0												0h			

Access Types Legend

Table 3-511. DMAXBAR13_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:0	DMAXBAR13_G3_SEL	R/W	0h	FSI DMA requests to corresponding xbar 0: FSIRX0.RX_DMA_EVT 1 FSIRX0_DMATRIG1 2: FSIRX0_DMATRIG2 3: FSIRX1.RX_DMA_EVT 4 FSIRX1_DMATRIG1 5: FSIRX1_DMATRIG2 6: FSIRX2.RX_DMA_EVT 7 FSIRX2_DMATRIG1 8: FSIRX2_DMATRIG2 9: FSIRX3.RX_DMA_EVT 10 FSIRX3_DMATRIG1 11: FSIRX3_DMATRIG2 12: FSITX0.TX_DMA_EVT 13: FSITX1.TX_DMA_EVT 14: FSITX2.TX_DMA_EVT 15: FSITX3.TX_DMA_EVT Reset Source: mod_g_rst_n

3.7.98 CFG0_DMAXBAR13_G4 Registers

3.7.98.1 CFG0_G4 Register (Offset = 454h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-512. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6454h

Figure 3-227. DMAXBAR13_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													DMAXBAR13_G4_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-513. DMAXBAR13_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	DMAXBAR13_G4_SEL	R/W	0h	SDFM DMA requests to corresponding xbar 0: SD0.FILT1.DRINT 1: SD0.FILT2.DRINT 2: SD0.FILT3.DRINT 3: SD0.FILT4.DRINT 4: SD1.FILT1.DRINT 5: SD1.FILT2.DRINT 6: SD1.FILT3.DRINT 7: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.7.99 CFG0_DMAXBAR13_G5 Registers

3.7.99.1 CFG0_G5 Register (Offset = 458h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-514. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6458h

Figure 3-228. DMAXBAR13_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DMAXBAR13_G5_SEL			
NONE												R/W			
0												0h			

Access Types Legend

Table 3-515. DMAXBAR13_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:0	DMAXBAR13_G5_SEL	R/W	0h	ECAP DMA requests to corresponding xbar 0: ECAP0.DMA_INT 1: ECAP1.DMA_INT 2: ECAP2.DMA_INT 3: ECAP3.DMA_INT 4: ECAP4.DMA_INT 5: ECAP5.DMA_INT 6: ECAP6.DMA_INT 7: ECAP7.DMA_INT 8: ECAP8.DMA_INT 9: ECAP9.DMA_INT Reset Source: mod_g_rst_n

3.7.100 CFG0_DMAXBAR14_GSEL Registers

3.7.100.1 CFG0_GSEL Register (Offset = 480h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-516. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6480h

Figure 3-229. DMAXBAR14_GSEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													DMAXBAR14_GSEL_GSEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-517. DMAXBAR14_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	DMAXBAR14_GSEL_GSEL	R/W	0h	Select input source: 0: G0 selected .. 5: G5 selected Reset Source: mod_g_rst_n

3.7.101 CFG0_DMAXBAR14_G0 Registers

3.7.101.1 CFG0_G0 Register (Offset = 484h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-518. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6484h

Figure 3-230. DMAXBAR14_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR14_G0_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-519. DMAXBAR14_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR14_G0_SEL	R/W	0h	ETPWM SOCA to corresponding xbar 1: PWMx.SOCA is selected 0: PWMx.SOCA is de-selected Reset Source: mod_g_rst_n

3.7.102 CFG0_DMAXBAR14_G1 Registers

3.7.102.1 CFG0_G1 Register (Offset = 488h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-520. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6488h

Figure 3-231. DMAXBAR14_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR14_G1_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-521. DMAXBAR14_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR14_G1_SEL	R/W	0h	ETPWM SOCB to corresponding xbar 1: PWMx.SOCB is selected 0: PWMx.SOCB is de-selected Reset Source: mod_g_rst_n

3.7.103 CFG0_DMAXBAR14_G2 Registers

3.7.103.1 CFG0_G2 Register (Offset = 48Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-522. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 648Ch

Figure 3-232. DMAXBAR14_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR14_G2_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-523. DMAXBAR14_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR14_G2_SEL	R/W	0h	ADC DMA requests to corresponding xbar 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.7.104 CFG0_DMAXBAR14_G3 Registers

3.7.104.1 CFG0_G3 Register (Offset = 490h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-524. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6490h

Figure 3-233. DMAXBAR14_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DMAXBAR14_G3_SEL			
NONE												R/W			
0												0h			

Access Types Legend

Table 3-525. DMAXBAR14_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:0	DMAXBAR14_G3_SEL	R/W	0h	FSI DMA requests to corresponding xbar 0: FSIRX0.RX_DMA_EVT 1 FSIRX0_DMATRIG1 2: FSIRX0_DMATRIG2 3: FSIRX1.RX_DMA_EVT 4 FSIRX1_DMATRIG1 5: FSIRX1_DMATRIG2 6: FSIRX2.RX_DMA_EVT 7 FSIRX2_DMATRIG1 8: FSIRX2_DMATRIG2 9: FSIRX3.RX_DMA_EVT 10 FSIRX3_DMATRIG1 11: FSIRX3_DMATRIG2 12: FSITX0.TX_DMA_EVT 13: FSITX1.TX_DMA_EVT 14: FSITX2.TX_DMA_EVT 15: FSITX3.TX_DMA_EVT Reset Source: mod_g_rst_n

3.7.105 CFG0_DMAXBAR14_G4 Registers

3.7.105.1 CFG0_G4 Register (Offset = 494h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-526. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6494h

Figure 3-234. DMAXBAR14_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													DMAXBAR14_G4_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-527. DMAXBAR14_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	DMAXBAR14_G4_SEL	R/W	0h	SDFM DMA requests to corresponding xbar 0: SD0.FILT1.DRINT 1: SD0.FILT2.DRINT 2: SD0.FILT3.DRINT 3: SD0.FILT4.DRINT 4: SD1.FILT1.DRINT 5: SD1.FILT2.DRINT 6: SD1.FILT3.DRINT 7: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.7.106 CFG0_DMAXBAR14_G5 Registers

3.7.106.1 CFG0_G5 Register (Offset = 498h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-528. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 6498h

Figure 3-235. DMAXBAR14_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DMAXBAR14_G5_SEL			
NONE												R/W			
0												0h			

Access Types Legend

Table 3-529. DMAXBAR14_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:0	DMAXBAR14_G5_SEL	R/W	0h	ECAP DMA requests to corresponding xbar 0: ECAP0.DMA_INT 1: ECAP1.DMA_INT 2: ECAP2.DMA_INT 3: ECAP3.DMA_INT 4: ECAP4.DMA_INT 5: ECAP5.DMA_INT 6: ECAP6.DMA_INT 7: ECAP7.DMA_INT 8: ECAP8.DMA_INT 9: ECAP9.DMA_INT Reset Source: mod_g_rst_n

3.7.107 CFG0_DMAXBAR15_GSEL Registers

3.7.107.1 CFG0_GSEL Register (Offset = 4C0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-530. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 64C0h

Figure 3-236. DMAXBAR15_GSEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													DMAXBAR15_GSEL_GSEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-531. DMAXBAR15_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	DMAXBAR15_GSEL_GSEL	R/W	0h	Select input source: 0: G0 selected .. 5: G5 selected Reset Source: mod_g_rst_n

3.7.108 CFG0_DMAXBAR15_G0 Registers

3.7.108.1 CFG0_G0 Register (Offset = 4C4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-532. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 64C4h

Figure 3-237. DMAXBAR15_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR15_G0_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-533. DMAXBAR15_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR15_G0_SEL	R/W	0h	ETPWM SOCA to corresponding xbar 1: PWMx.SOCA is selected 0: PWMx.SOCA is de-selected Reset Source: mod_g_rst_n

3.7.109 CFG0_DMAXBAR15_G1 Registers

3.7.109.1 CFG0_G1 Register (Offset = 4C8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-534. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 64C8h

Figure 3-238. DMAXBAR15_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR15_G1_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-535. DMAXBAR15_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR15_G1_SEL	R/W	0h	ETPWM SOCB to corresponding xbar 1: PWMx.SOCB is selected 0: PWMx.SOCB is de-selected Reset Source: mod_g_rst_n

3.7.110 CFG0_DMAXBAR15_G2 Registers

3.7.110.1 CFG0_G2 Register (Offset = 4CCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-536. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 64CCh

Figure 3-239. DMAXBAR15_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMAXBAR15_G2_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-537. DMAXBAR15_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMAXBAR15_G2_SEL	R/W	0h	ADC DMA requests to corresponding xbar 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.7.111 CFG0_DMAXBAR15_G3 Registers

3.7.111.1 CFG0_G3 Register (Offset = 4D0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-538. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 64D0h

Figure 3-240. DMAXBAR15_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DMAXBAR15_G3_SEL			
NONE												R/W			
0												0h			

Access Types Legend

Table 3-539. DMAXBAR15_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:0	DMAXBAR15_G3_SEL	R/W	0h	FSI DMA requests to corresponding xbar 0: FSIRX0.RX_DMA_EVT 1 FSIRX0_DMATRIG1 2: FSIRX0_DMATRIG2 3: FSIRX1.RX_DMA_EVT 4 FSIRX1_DMATRIG1 5: FSIRX1_DMATRIG2 6: FSIRX2.RX_DMA_EVT 7 FSIRX2_DMATRIG1 8: FSIRX2_DMATRIG2 9: FSIRX3.RX_DMA_EVT 10 FSIRX3_DMATRIG1 11: FSIRX3_DMATRIG2 12: FSITX0.TX_DMA_EVT 13: FSITX1.TX_DMA_EVT 14: FSITX2.TX_DMA_EVT 15: FSITX3.TX_DMA_EVT Reset Source: mod_g_rst_n

3.7.112 CFG0_DMAXBAR15_G4 Registers

3.7.112.1 CFG0_G4 Register (Offset = 4D4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-540. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 64D4h

Figure 3-241. DMAXBAR15_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													DMAXBAR15_G4_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-541. DMAXBAR15_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	DMAXBAR15_G4_SEL	R/W	0h	SDFM DMA requests to corresponding xbar 0: SD0.FILT1.DRINT 1: SD0.FILT2.DRINT 2: SD0.FILT3.DRINT 3: SD0.FILT4.DRINT 4: SD1.FILT1.DRINT 5: SD1.FILT2.DRINT 6: SD1.FILT3.DRINT 7: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.7.113 CFG0_DMAXBAR15_G5 Registers

3.7.113.1 CFG0_G5 Register (Offset = 4D8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-542. Instance Table

Instance Name	Physical Address
DMAXBAR_MMR	502D 64D8h

Figure 3-242. DMAXBAR15_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DMAXBAR15_G5_SEL			
NONE												R/W			
0												0h			

Access Types Legend

Table 3-543. DMAXBAR15_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:0	DMAXBAR15_G5_SEL	R/W	0h	ECAP DMA requests to corresponding xbar 0: ECAP0.DMA_INT 1: ECAP1.DMA_INT 2: ECAP2.DMA_INT 3: ECAP3.DMA_INT 4: ECAP4.DMA_INT 5: ECAP5.DMA_INT 6: ECAP6.DMA_INT 7: ECAP7.DMA_INT 8: ECAP8.DMA_INT 9: ECAP9.DMA_INT Reset Source: mod_g_rst_n

3.7.114 Access Table

Table 3-544. Access Type Codes

Access Type	Code	Description
R	R	Read
R/W	R/W	Read / Write

3.8 ECAP Registers

Table 3-545. MEM, MEM Registers, Base Address=0X0000000050240000, Length=4096

Offset	Length	Register Name	ecap0 Physical Address	ecap1 Physical Address	ecap2 Physical Address
0h	32	TSCTR	5024 0000h	5024 1000h	5024 2000h
4h	32	CTRPHS	5024 0004h	5024 1004h	5024 2004h
8h	32	CAP1	5024 0008h	5024 1008h	5024 2008h
Ch	32	CAP2	5024 000Ch	5024 100Ch	5024 200Ch
10h	32	CAP3	5024 0010h	5024 1010h	5024 2010h
14h	32	CAP4	5024 0014h	5024 1014h	5024 2014h
24h	32	ECCTL0	5024 0024h	5024 1024h	5024 2024h
28h	16	ECCTL1	5024 0028h	5024 1028h	5024 2028h
2Ah	16	ECCTL2	5024 002Ah	5024 102Ah	5024 202Ah
2Ch	16	ECEINT	5024 002Ch	5024 102Ch	5024 202Ch
2Eh	16	ECFLG	5024 002Eh	5024 102Eh	5024 202Eh
30h	16	ECCLR	5024 0030h	5024 1030h	5024 2030h
32h	16	ECFRC	5024 0032h	5024 1032h	5024 2032h
3Ch	32	ECAPSYNCINSEL	5024 003Ch	5024 103Ch	5024 203Ch
40h	32	HRCTL	5024 0040h	5024 1040h	5024 2040h
48h	32	HRINTEN	5024 0048h	5024 1048h	5024 2048h
4Ch	32	HRFLG	5024 004Ch	5024 104Ch	5024 204Ch
50h	32	HRCLR	5024 0050h	5024 1050h	5024 2050h
54h	32	HRFRC	5024 0054h	5024 1054h	5024 2054h
58h	32	HRCALPRD	5024 0058h	5024 1058h	5024 2058h
5Ch	32	HRSYSCLKCTR	5024 005Ch	5024 105Ch	5024 205Ch
60h	32	HRSYSCLKCAP	5024 0060h	5024 1060h	5024 2060h
64h	32	HRCLKCTR	5024 0064h	5024 1064h	5024 2064h
68h	32	HRCLKCAP	5024 0068h	5024 1068h	5024 2068h
74h	32	HRDEBUGCTL	5024 0074h	5024 1074h	5024 2074h
78h	32	HRDEBUGOBSERVE1	5024 0078h	5024 1078h	5024 2078h
7Ch	32	HRDEBUGOBSERVE2	5024 007Ch	5024 107Ch	5024 207Ch
80h	32	MUNIT_COMMON_CTL	5024 0080h	5024 1080h	5024 2080h
C0h	32	MUNIT_1_CTL	5024 00C0h	5024 10C0h	5024 20C0h
C4h	32	MUNIT_1_SHADOW_CTL	5024 00C4h	5024 10C4h	5024 20C4h
D0h	32	MUNIT_1_MIN	5024 00D0h	5024 10D0h	5024 20D0h
D4h	32	MUNIT_1_MAX	5024 00D4h	5024 10D4h	5024 20D4h
D8h	32	MUNIT_1_MIN_SHADOW	5024 00D8h	5024 10D8h	5024 20D8h
DCh	32	MUNIT_1_MAX_SHADOW	5024 00DCh	5024 10DCh	5024 20DCh
E0h	32	MUNIT_1_DEBUG_RANGE_MIN	5024 00E0h	5024 10E0h	5024 20E0h
E4h	32	MUNIT_1_DEBUG_RANGE_MAX	5024 00E4h	5024 10E4h	5024 20E4h
100h	32	MUNIT_2_CTL	5024 0100h	5024 1100h	5024 2100h
104h	32	MUNIT_2_SHADOW_CTL	5024 0104h	5024 1104h	5024 2104h
110h	32	MUNIT_2_MIN	5024 0110h	5024 1110h	5024 2110h
114h	32	MUNIT_2_MAX	5024 0114h	5024 1114h	5024 2114h
118h	32	MUNIT_2_MIN_SHADOW	5024 0118h	5024 1118h	5024 2118h
11Ch	32	MUNIT_2_MAX_SHADOW	5024 011Ch	5024 111Ch	5024 211Ch
120h	32	MUNIT_2_DEBUG_RANGE_MIN	5024 0120h	5024 1120h	5024 2120h
124h	32	MUNIT_2_DEBUG_RANGE_MAX	5024 0124h	5024 1124h	5024 2124h

Table 3-546. MEM, MEM Registers, Base Address=0X0000000050240000, Length=4096

Offset	Length	Register Name	ecap3 Physical Address	ecap4 Physical Address	ecap5 Physical Address
0h	32	TSCTR	5024 3000h	5024 4000h	5024 5000h
4h	32	CTRPHS	5024 3004h	5024 4004h	5024 5004h
8h	32	CAP1	5024 3008h	5024 4008h	5024 5008h
Ch	32	CAP2	5024 300Ch	5024 400Ch	5024 500Ch
10h	32	CAP3	5024 3010h	5024 4010h	5024 5010h
14h	32	CAP4	5024 3014h	5024 4014h	5024 5014h
24h	32	ECCTL0	5024 3024h	5024 4024h	5024 5024h
28h	16	ECCTL1	5024 3028h	5024 4028h	5024 5028h
2Ah	16	ECCTL2	5024 302Ah	5024 402Ah	5024 502Ah
2Ch	16	ECEINT	5024 302Ch	5024 402Ch	5024 502Ch
2Eh	16	ECFLG	5024 302Eh	5024 402Eh	5024 502Eh
30h	16	ECCLR	5024 3030h	5024 4030h	5024 5030h
32h	16	ECFRC	5024 3032h	5024 4032h	5024 5032h
3Ch	32	ECAPSYNCINSEL	5024 303Ch	5024 403Ch	5024 503Ch
40h	32	HRCTL	5024 3040h	5024 4040h	5024 5040h
48h	32	HRINTEN	5024 3048h	5024 4048h	5024 5048h
4Ch	32	HRFLG	5024 304Ch	5024 404Ch	5024 504Ch
50h	32	HRCLR	5024 3050h	5024 4050h	5024 5050h
54h	32	HRFRC	5024 3054h	5024 4054h	5024 5054h
58h	32	HRCALPRD	5024 3058h	5024 4058h	5024 5058h
5Ch	32	HRSYSCLKCTR	5024 305Ch	5024 405Ch	5024 505Ch
60h	32	HRSYSCLKCAP	5024 3060h	5024 4060h	5024 5060h
64h	32	HRCLKCTR	5024 3064h	5024 4064h	5024 5064h
68h	32	HRCLKCAP	5024 3068h	5024 4068h	5024 5068h
74h	32	HRDEBUGCTL	5024 3074h	5024 4074h	5024 5074h
78h	32	HRDEBUGOBSERVE1	5024 3078h	5024 4078h	5024 5078h
7Ch	32	HRDEBUGOBSERVE2	5024 307Ch	5024 407Ch	5024 507Ch
80h	32	MUNIT_COMMON_CTL	5024 3080h	5024 4080h	5024 5080h
C0h	32	MUNIT_1_CTL	5024 30C0h	5024 40C0h	5024 50C0h
C4h	32	MUNIT_1_SHADOW_CTL	5024 30C4h	5024 40C4h	5024 50C4h
D0h	32	MUNIT_1_MIN	5024 30D0h	5024 40D0h	5024 50D0h
D4h	32	MUNIT_1_MAX	5024 30D4h	5024 40D4h	5024 50D4h
D8h	32	MUNIT_1_MIN_SHADOW	5024 30D8h	5024 40D8h	5024 50D8h
DCh	32	MUNIT_1_MAX_SHADOW	5024 30DCh	5024 40DCh	5024 50DCh
E0h	32	MUNIT_1_DEBUG_RANGE_MIN	5024 30E0h	5024 40E0h	5024 50E0h
E4h	32	MUNIT_1_DEBUG_RANGE_MAX	5024 30E4h	5024 40E4h	5024 50E4h
100h	32	MUNIT_2_CTL	5024 3100h	5024 4100h	5024 5100h
104h	32	MUNIT_2_SHADOW_CTL	5024 3104h	5024 4104h	5024 5104h
110h	32	MUNIT_2_MIN	5024 3110h	5024 4110h	5024 5110h
114h	32	MUNIT_2_MAX	5024 3114h	5024 4114h	5024 5114h
118h	32	MUNIT_2_MIN_SHADOW	5024 3118h	5024 4118h	5024 5118h
11Ch	32	MUNIT_2_MAX_SHADOW	5024 311Ch	5024 411Ch	5024 511Ch
120h	32	MUNIT_2_DEBUG_RANGE_MIN	5024 3120h	5024 4120h	5024 5120h
124h	32	MUNIT_2_DEBUG_RANGE_MAX	5024 3124h	5024 4124h	5024 5124h

Table 3-547. MEM, MEM Registers, Base Address=0X0000000050240000, Length=4096

Offset	Length	Register Name	ecap6 Physical Address	ecap7 Physical Address	ecap8 Physical Address
0h	32	TSCTR	5024 6000h	5024 7000h	5024 8000h
4h	32	CTRPHS	5024 6004h	5024 7004h	5024 8004h
8h	32	CAP1	5024 6008h	5024 7008h	5024 8008h
Ch	32	CAP2	5024 600Ch	5024 700Ch	5024 800Ch
10h	32	CAP3	5024 6010h	5024 7010h	5024 8010h
14h	32	CAP4	5024 6014h	5024 7014h	5024 8014h
24h	32	ECCTL0	5024 6024h	5024 7024h	5024 8024h
28h	16	ECCTL1	5024 6028h	5024 7028h	5024 8028h
2Ah	16	ECCTL2	5024 602Ah	5024 702Ah	5024 802Ah
2Ch	16	ECEINT	5024 602Ch	5024 702Ch	5024 802Ch
2Eh	16	ECFLG	5024 602Eh	5024 702Eh	5024 802Eh
30h	16	ECCLR	5024 6030h	5024 7030h	5024 8030h
32h	16	ECFRC	5024 6032h	5024 7032h	5024 8032h
3Ch	32	ECAPSYNCINSEL	5024 603Ch	5024 703Ch	5024 803Ch
40h	32	HRCTL	5024 6040h	5024 7040h	5024 8040h
48h	32	HRINTEN	5024 6048h	5024 7048h	5024 8048h
4Ch	32	HRFLG	5024 604Ch	5024 704Ch	5024 804Ch
50h	32	HRCLR	5024 6050h	5024 7050h	5024 8050h
54h	32	HRFRC	5024 6054h	5024 7054h	5024 8054h
58h	32	HRCALPRD	5024 6058h	5024 7058h	5024 8058h
5Ch	32	HRSYSCLKCTR	5024 605Ch	5024 705Ch	5024 805Ch
60h	32	HRSYSCLKCAP	5024 6060h	5024 7060h	5024 8060h
64h	32	HRCLKCTR	5024 6064h	5024 7064h	5024 8064h
68h	32	HRCLKCAP	5024 6068h	5024 7068h	5024 8068h
74h	32	HRDEBUGCTL	5024 6074h	5024 7074h	5024 8074h
78h	32	HRDEBUGOBSERVE1	5024 6078h	5024 7078h	5024 8078h
7Ch	32	HRDEBUGOBSERVE2	5024 607Ch	5024 707Ch	5024 807Ch
80h	32	MUNIT_COMMON_CTL	5024 6080h	5024 7080h	5024 8080h
C0h	32	MUNIT_1_CTL	5024 60C0h	5024 70C0h	5024 80C0h
C4h	32	MUNIT_1_SHADOW_CTL	5024 60C4h	5024 70C4h	5024 80C4h
D0h	32	MUNIT_1_MIN	5024 60D0h	5024 70D0h	5024 80D0h
D4h	32	MUNIT_1_MAX	5024 60D4h	5024 70D4h	5024 80D4h
D8h	32	MUNIT_1_MIN_SHADOW	5024 60D8h	5024 70D8h	5024 80D8h
DCh	32	MUNIT_1_MAX_SHADOW	5024 60DCh	5024 70DCh	5024 80DCh
E0h	32	MUNIT_1_DEBUG_RANGE_MIN	5024 60E0h	5024 70E0h	5024 80E0h
E4h	32	MUNIT_1_DEBUG_RANGE_MAX	5024 60E4h	5024 70E4h	5024 80E4h
100h	32	MUNIT_2_CTL	5024 6100h	5024 7100h	5024 8100h
104h	32	MUNIT_2_SHADOW_CTL	5024 6104h	5024 7104h	5024 8104h
110h	32	MUNIT_2_MIN	5024 6110h	5024 7110h	5024 8110h
114h	32	MUNIT_2_MAX	5024 6114h	5024 7114h	5024 8114h
118h	32	MUNIT_2_MIN_SHADOW	5024 6118h	5024 7118h	5024 8118h
11Ch	32	MUNIT_2_MAX_SHADOW	5024 611Ch	5024 711Ch	5024 811Ch
120h	32	MUNIT_2_DEBUG_RANGE_MIN	5024 6120h	5024 7120h	5024 8120h
124h	32	MUNIT_2_DEBUG_RANGE_MAX	5024 6124h	5024 7124h	5024 8124h

Table 3-548. MEM, MEM Registers, Base Address=0X0000000050240000, Length=4096

Offset	Length	Register Name	ecap9 Physical Address
0h	32	TSCTR	5024 9000h
4h	32	CTRPHS	5024 9004h
8h	32	CAP1	5024 9008h
Ch	32	CAP2	5024 900Ch
10h	32	CAP3	5024 9010h
14h	32	CAP4	5024 9014h
24h	32	ECCTL0	5024 9024h
28h	16	ECCTL1	5024 9028h
2Ah	16	ECCTL2	5024 902Ah
2Ch	16	ECEINT	5024 902Ch
2Eh	16	ECFLG	5024 902Eh
30h	16	ECCLR	5024 9030h
32h	16	ECFRC	5024 9032h
3Ch	32	ECAPSYNCINSEL	5024 903Ch
40h	32	HRCTL	5024 9040h
48h	32	HRINTEN	5024 9048h
4Ch	32	HRFLG	5024 904Ch
50h	32	HRCLR	5024 9050h
54h	32	HRFRC	5024 9054h
58h	32	HRCALPRD	5024 9058h
5Ch	32	HRSYSCLKCTR	5024 905Ch
60h	32	HRSYSCLKCAP	5024 9060h
64h	32	HRCLKCTR	5024 9064h
68h	32	HRCLKCAP	5024 9068h
74h	32	HRDEBUGCTL	5024 9074h
78h	32	HRDEBUGOBSERVE1	5024 9078h
7Ch	32	HRDEBUGOBSERVE2	5024 907Ch
80h	32	MUNIT_COMMON_CTL	5024 9080h
C0h	32	MUNIT_1_CTL	5024 90C0h
C4h	32	MUNIT_1_SHADOW_CTL	5024 90C4h
D0h	32	MUNIT_1_MIN	5024 90D0h
D4h	32	MUNIT_1_MAX	5024 90D4h
D8h	32	MUNIT_1_MIN_SHADOW	5024 90D8h
DCh	32	MUNIT_1_MAX_SHADOW	5024 90DCh
E0h	32	MUNIT_1_DEBUG_RANGE_MIN	5024 90E0h
E4h	32	MUNIT_1_DEBUG_RANGE_MAX	5024 90E4h
100h	32	MUNIT_2_CTL	5024 9100h
104h	32	MUNIT_2_SHADOW_CTL	5024 9104h
110h	32	MUNIT_2_MIN	5024 9110h
114h	32	MUNIT_2_MAX	5024 9114h
118h	32	MUNIT_2_MIN_SHADOW	5024 9118h
11Ch	32	MUNIT_2_MAX_SHADOW	5024 911Ch
120h	32	MUNIT_2_DEBUG_RANGE_MIN	5024 9120h
124h	32	MUNIT_2_DEBUG_RANGE_MAX	5024 9124h

3.8.1 MEM_TSCTR Registers

3.8.1.1 MEM_TSCTR Register (Offset = 0h) [reset = 0h]

Short Description: Time-Stamp Counter

Long Description: Time-Stamp Counter

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Table 3-549. Instance Table

Instance Name	Physical Address
ECAP0	5024 0000h
ECAP1	5024 1000h
ECAP2	5024 2000h
ECAP3	5024 3000h
ECAP4	5024 4000h
ECAP5	5024 5000h
ECAP6	5024 6000h
ECAP7	5024 7000h
ECAP8	5024 8000h
ECAP9	5024 9000h

Figure 3-243. TSCTR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TSCTR															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSCTR															
R/W															
0h															

Access Types Legend

Table 3-550. TSCTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TSCTR	R/W	0h	Active 32-bit counter register that is used as the capture time-base HR mode : 1] This register reads HRCOUNTER value and is not writable 2] can be reset using CTRFILTRESET 3] Its not synchronized to SYSCLK domain so reads may not be accurate Reset Source: ecap_rst_mod_g_rst_n

3.8.2 MEM_CTRPHS Registers

3.8.2.1 MEM_CTRPHS Register (Offset = 4h) [reset = 0h]

Short Description: Counter Phase Offset Valu

Long Description: Counter Phase Offset Value Register

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Table 3-551. Instance Table

Instance Name	Physical Address
ECAP0	5024 0004h
ECAP1	5024 1004h
ECAP2	5024 2004h
ECAP3	5024 3004h
ECAP4	5024 4004h
ECAP5	5024 5004h
ECAP6	5024 6004h
ECAP7	5024 7004h
ECAP8	5024 8004h
ECAP9	5024 9004h

Figure 3-244. CTRPHS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CTRPHS															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTRPHS															
R/W															
0h															

Access Types Legend

Table 3-552. CTRPHS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CTRPHS	R/W	0h	Counter phase value register that can be programmed for phase lag/lead. This register CTRPHS is loaded into TSCTR upon either a SYNCI event or S/W force via a control bit. Used to achieve phase control synchronization with respect to other eCAP and EPWM time-bases. This register is not applicable in HR mode. Reset Source: ecap_rst_mod_g_rst_n

3.8.3 MEM_CAP1 Registers

3.8.3.1 MEM_CAP1 Register (Offset = 8h) [reset = 0h]

Short Description: Capture 1 Register

Long Description: Capture 1 Register

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Table 3-553. Instance Table

Instance Name	Physical Address
ECAP0	5024 0008h
ECAP1	5024 1008h
ECAP2	5024 2008h
ECAP3	5024 3008h
ECAP4	5024 4008h
ECAP5	5024 5008h
ECAP6	5024 6008h
ECAP7	5024 7008h
ECAP8	5024 8008h
ECAP9	5024 9008h

Figure 3-245. CAP1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CAP1															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAP1															
R/W															
0h															

Access Types Legend

Table 3-554. CAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAP1	R/W	0h	This register can be loaded [written] by: - Time-Stamp counter value [TSCTR] during a capture event - Software - may be useful for test purposes or initialization - ARPD shadow register [CAP3] when used in APWM mode Reset Source: ecap_rst_mod_g_rst_n

3.8.4 MEM_CAP2 Registers

3.8.4.1 MEM_CAP2 Register (Offset = Ch) [reset = 0h]

Short Description: Capture 2 Register

Long Description: Capture 2 Register

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Table 3-555. Instance Table

Instance Name	Physical Address
ECAP0	5024 000Ch
ECAP1	5024 100Ch
ECAP2	5024 200Ch
ECAP3	5024 300Ch
ECAP4	5024 400Ch
ECAP5	5024 500Ch
ECAP6	5024 600Ch
ECAP7	5024 700Ch
ECAP8	5024 800Ch
ECAP9	5024 900Ch

Figure 3-246. CAP2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CAP2															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAP2															
R/W															
0h															

Access Types Legend

Table 3-556. CAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAP2	R/W	0h	This register can be loaded [written] by: - Time-Stamp [counter value] during a capture event - Software - may be useful for test purposes - ACMP shadow register [CAP4] when used in APWM mode Reset Source: ecap_rst_mod_g_rst_n

3.8.5 MEM_CAP3 Registers

3.8.5.1 MEM_CAP3 Register (Offset = 10h) [reset = 0h]

Short Description: Capture 3 Register

Long Description: Capture 3 Register

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Table 3-557. Instance Table

Instance Name	Physical Address
ECAP0	5024 0010h
ECAP1	5024 1010h
ECAP2	5024 2010h
ECAP3	5024 3010h
ECAP4	5024 4010h
ECAP5	5024 5010h
ECAP6	5024 6010h
ECAP7	5024 7010h
ECAP8	5024 8010h
ECAP9	5024 9010h

Figure 3-247. CAP3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CAP3															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAP3															
R/W															
0h															

Access Types Legend

Table 3-558. CAP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAP3	R/W	0h	In CMP mode, this is a time-stamp capture register. In APWM mode, this is the period shadow [APRD] register. You can update the PWM period value through this register. CAP3 [APRD] shadows CAP1 in this mode. Reset Source: ecap_rst_mod_g_rst_n

3.8.6 MEM_CAP4 Registers

3.8.6.1 MEM_CAP4 Register (Offset = 14h) [reset = 0h]

Short Description: Capture 4 Register

Long Description: Capture 4 Register

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Table 3-559. Instance Table

Instance Name	Physical Address
ECAP0	5024 0014h
ECAP1	5024 1014h
ECAP2	5024 2014h
ECAP3	5024 3014h
ECAP4	5024 4014h
ECAP5	5024 5014h
ECAP6	5024 6014h
ECAP7	5024 7014h
ECAP8	5024 8014h
ECAP9	5024 9014h

Figure 3-248. CAP4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CAP4															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAP4															
R/W															
0h															

Access Types Legend

Table 3-560. CAP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAP4	R/W	0h	In CMP mode, this is a time-stamp capture register. In APWM mode, this is the compare shadow [ACMP] register. You can update the PWM compare value via this register. CAP4 [ACMP] shadows CAP2 in this mode. Reset Source: ecap_rst_mod_g_rst_n

3.8.7 MEM_ECCTL0 Registers

3.8.7.1 MEM_ECCTL0 Register (Offset = 24h) [reset = ffh]

Short Description: Capture Control Register

Long Description: Capture Control Register 0

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Table 3-561. Instance Table

Instance Name	Physical Address
ECAP0	5024 0024h
ECAP1	5024 1024h
ECAP2	5024 2024h
ECAP3	5024 3024h
ECAP4	5024 4024h
ECAP5	5024 5024h
ECAP6	5024 6024h
ECAP7	5024 7024h
ECAP8	5024 8024h
ECAP9	5024 9024h

Figure 3-249. ECCTL0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_2														SOCEVTSEL	
R														R/W	
0h														0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QUALPRD				RESERVED_1				INPUTSEL							
R/W				R				R/W							
0h				0h				ffh							

Access Types Legend

Table 3-562. ECCTL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED_2	R	0h	Reserved Reset Source: ecap_rst_mod_g_rst_n
17:16	SOCEVTSEL	R/W	0h	ADC SOC event select Capture Mode: 00b [R/W] = SOC trigger source is CEVT1 01b [R/W] = SOC trigger source is CEVT2 10b [R/W] = SOC trigger source is CEVT3 11b [R/W] = SOC trigger source is CEVT4 APWM Mode: 00b [R/W] = SOC trigger interrupt source is period match 01b [R/W] = SOC trigger interrupt source is compare match 10b [R/W] = SOC trigger interrupt source is period match or compare match 11b [R/W] = Disabled Reset Source: ecap_rst_mod_g_rst_n
15:12	QUALPRD	R/W	0h	Qual period to filter out noise on input signals being monitored, Not applicable for HR mode. 0x0 : Bypass 0x1 : pulses of with 1 cycle or less will be filtered out 0x2 : pulses of with 2 cycles or less will be filtered out .... 0xF : pulses of with 15 cycles or less will be filtered out Reset Source: ecap_rst_mod_g_rst_n
11:8	RESERVED_1	R	0h	Reserved Reset Source: ecap_rst_mod_g_rst_n
7:0	INPUTSEL	R/W	FFh	Capture input source select bits 0x0 capture input is ECAPxINPUT[0] 0x1 capture input is ECAPxINPUT[1] 0x2 capture input is ECAPxINPUT[2] ... 0xFF capture input is ECAPxINPUT[256] Reset Source: ecap_rst_mod_g_rst_n

3.8.8 MEM_ECCTL1 Registers

3.8.8.1 MEM_ECCTL1 Register (Offset = 28h) [reset = 0h]

Short Description: Capture Control Register

Long Description: Capture Control Register 1

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Table 3-563. Instance Table

Instance Name	Physical Address
ECAP0	5024 0028h
ECAP1	5024 1028h
ECAP2	5024 2028h
ECAP3	5024 3028h
ECAP4	5024 4028h
ECAP5	5024 5028h
ECAP6	5024 6028h
ECAP7	5024 7028h
ECAP8	5024 8028h
ECAP9	5024 9028h

Figure 3-250. ECCTL1 Name Register

15	14	13	12	11	10	9	8
FREE_SOFT		PRESCALE					CAPLDEN
R/W		R/W					R/W
0h		0h					0h
7	6	5	4	3	2	1	0
CTRRST4	CAP4POL	CTRRST3	CAP3POL	CTRRST2	CAP2POL	CTRRST1	CAP1POL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 3-564. ECCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	FREE_SOFT	R/W	0h	Emulation Control Reset Source: ecap_rst_mod_g_rst_n 3 ECap_unaf_emu_sus2 TSCTR counter is unaffected by emulation suspend (Run Free) 2 ECap_unaf_emu_sus TSCTR counter is unaffected by emulation suspend (Run Free) 1 ECap_runs_until TSCTR counter runs until = 0
13:9	PRESCALE	R/W	0h	Event Filter prescale select Reset Source: ecap_rst_mod_g_rst_n 31 Ecap_div62 Divide by 62 30 Ecap_div60 Divide by 60 5 Ecap_div10 Divide by 10 4 Ecap_div8 Divide by 8 3 Ecap_div6 Divide by 6 2 Ecap_div4 Divide by 4 1 Ecap_div2 Divide by 2
8	CAPLDEN	R/W	0h	Enable Loading of CAP1-4 registers on a capture event. Note that this bit does not disable CEVTn events from being generated. Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_Enable Enable CAP1-4 register loads at capture event time.
7	CTRRST4	R/W	0h	Counter Reset on Capture Event 4 Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_reset_event4 Reset counter after Capture Event 4 time-stamp has been captured (used in difference mode operation)
6	CAP4POL	R/W	0h	Capture Event 4 Polarity select Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_cap_event4_fall Capture Event 4 triggered on a falling edge (FE)

Table 3-564. ECCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CTRRST3	R/W	0h	Counter Reset on Capture Event 3 Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_reset_event3 Reset counter after Event 3 time-stamp has been captured (used in difference mode operation)
4	CAP3POL	R/W	0h	Capture Event 3 Polarity select Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_cap_event3_fall Capture Event 3 triggered on a falling edge (FE)
3	CTRRST2	R/W	0h	Counter Reset on Capture Event 2 Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_reset_event2 Reset counter after Event 2 time-stamp has been captured (used in difference mode operation)
2	CAP2POL	R/W	0h	Capture Event 2 Polarity select Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_cap_event2_fall Capture Event 2 triggered on a falling edge (FE)
1	CTRRST1	R/W	0h	Counter Reset on Capture Event 1 Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_reset_event1 Reset counter after Event 1 time-stamp has been captured (used in difference mode operation)
0	CAP1POL	R/W	0h	Capture Event 1 Polarity select Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_cap_event1_fall Capture Event 1 triggered on a falling edge (FE)

3.8.9 MEM_ECCTL2 Registers

3.8.9.1 MEM_ECCTL2 Register (Offset = 2Ah) [reset = 6h]

Short Description: Capture Control Register

Long Description: Capture Control Register 2

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Table 3-565. Instance Table

Instance Name	Physical Address
ECAP0	5024 002Ah
ECAP1	5024 102Ah
ECAP2	5024 202Ah
ECAP3	5024 302Ah
ECAP4	5024 402Ah
ECAP5	5024 502Ah
ECAP6	5024 602Ah
ECAP7	5024 702Ah
ECAP8	5024 802Ah
ECAP9	5024 902Ah

Figure 3-251. ECCTL2 Name Register

15	14	13	12	11	10	9	8
MODCNTRSTS		DMAEVTSEL		CTRFILTRESET	APWMPOL	CAP_APWM	SWSYNC
R/W		R/W		R/W1TC	R/W	R/W	R/W1TS
0h		0h		0h	0h	0h	0h
7	6	5	4	3	2	1	0
SYNCO_SEL		SYNCI_EN	TSCTRSTOP	REARM	STOP_WRAP		CONT_ONESHT
R/W		R/W	R/W	R/W1TS	R/W		R/W
0h		0h	0h	0h	3h		0h

Access Types Legend

Table 3-566. ECCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	MODCNTRSTS	R/W	0h	This bit field reads current status on modulo counter 00b [R] = CAP1 register gets loaded on next capture event. 01b [R] = CAP2 register gets loaded on next capture event. 10b [R] = CAP3 register gets loaded on next capture event. 11b [R] = CAP4 register gets loaded on next capture event. Reset Source: ecap_rst_mod_g_rst_n
13:12	DMAEVTSEL	R/W	0h	DMA event select Capture Mode: 00b [R/W] = DMA interrupt source is CEVT1 01b [R/W] = DMA interrupt source is CEVT2 10b [R/W] = DMA interrupt source is CEVT3 11b [R/W] = DMA interrupt source is CEVT4 APWM Mode: 00b [R/W] = DMA interrupt source is period match 01b [R/W] = DMA interrupt source is compare match 10b [R/W] = DMA interrupt source is period match or compare match 11b [R/W] = Disabled Reset Source: ecap_rst_mod_g_rst_n
11	CTRFILTRESET	R/W1TC	0h	Reset Bit 0h [R] = No effect 1h [W] = Resets event filter, counter, modulo counter and CEVT[1,2,3,4] and CNTOVF , HRERROR flags Note: This provides an ability start capture module from known state in case spurious inputs are captured while ECAP is configured. Reset Source: ecap_rst_mod_g_rst_n

Table 3-566. ECCTL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	APWMPOL	R/W	0h	APWM output polarity select. This is applicable only in APWM operating mode. Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_output_active_l Output is active low (Compare ow value defines low time)
9	CAP_APWM	R/W	0h	CAP/APWM operating mode select Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_module_APWM ECAP module operates in APWM mode. This mode forces the following configuration: - Resets TSCTR on CTR = PRD event (period boundary) - Permits shadow loading on CAP1 and 2 registers - Disables loading of time-stamps into CAP1-4 registers - CAPx/APWMx pin operates as a APWM output
8	SWSYNC	R/W1TS	0h	Software-forced Counter [TSCTR] Synchronizer. This provides the user a method to generate a synchronization pulse through software. In APWM mode, the synchronization pulse can also be sourced from the CTR = PRD event. Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_write_TSCTR Writing a one forces a TSCTR shadow load of current ECAP module and any ECAP modules down-stream providing the SYNCO_SEL bits are 0,0. After writing a 1, this bit returns to a zero. Note: Selection CTR = PRD is meaningful only in APWM mode; however, you can choose it in CAP mode if you find doing so useful.
7:6	SYNCO_SEL	R/W	0h	Sync-Out Select Reset Source: ecap_rst_mod_g_rst_n 3 Ecap_disable_sync_ou Disable sync out signal t 1 Ecap_CTR_PRD_to_sync Select CTR = PRD event to be out the sync-out signal
5	SYNCI_EN	R/W	0h	Counter [TSCTR] Sync-In select mode Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_enable_counter_ Enable counter (TSCTR) to be register loaded from CTRPHS register upon either a SYNCI signal or a S/W force event.
4	TSCTRSTOP	R/W	0h	Time Stamp [TSCTR] Counter Stop [freeze] Control Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_TSCTR_free_runn TSCTR free-running ing
3	REARM	R/W1TS	0h	Re-Arming Control. Note: The re-arm function is valid in one shot or continuous mode Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_arms_oneshot Arms the one-shot sequence as follows: (1) Resets the Mod4 counter to zero (2) Unfreezes the Mod4 counter (3) Enables capture register loads
2:1	STOP_WRAP	R/W	3h	Stop value for one-shot mode. This is the number [between 1-4] of captures allowed to occur before the CAP[1-4] registers are frozen, that is, capture sequence is stopped. Wrap value for continuous mode. This is the number [between 1-4] of the capture register in which the circular buffer wraps around and starts again. Notes: STOP_WRAP is compared to Mod4 counter and, when equal, 2 actions occur: - Mod4 counter is stopped [frozen] - Capture register loads are inhibited In one-shot mode, further interrupt events are blocked until re-armed. Reset Source: ecap_rst_mod_g_rst_n 3 Ecap_StopEvent4_Wrap Stop after Capture Event 4 in Event2 one-shot mode Wrap after Capture Event 4 in continuous mode. 2 Ecap_StopEvent3_Wrap Stop after Capture Event 3 in Event2 one-shot mode Wrap after Capture Event 3 in continuous mode. 1 Ecap_StopEvent2_Wrap Stop after Capture Event 2 in Event2 one-shot mode Wrap after Capture Event 2 in continuous mode.
0	CONT_ONESHT	R/W	0h	Continuous or one-shot mode control [applicable only in capture mode] Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_opp_one Operate in one-Shot mode

3.8.10 MEM_ECEINT Registers

3.8.10.1 MEM_ECEINT Register (Offset = 2Ch) [reset = 0h]

Short Description: The interrupt enable bits

Long Description: The interrupt enable bits (CEVT1, ...) block any of the selected events from generating an interrupt. Events will still be latched into the flag bit (ECFLG register) and can be forced/cleared via the ECFRC/ ECCLR registers. The proper procedure for configuring peripheral modes and interrupts is as follows: - Disable global interrupts - Stop eCAP counter - Disable eCAP interrupts - Configure peripheral registers - Clear spurious eCAP interrupt flags - Enable eCAP interrupts - Start eCAP counter - Enable global interrupts

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Table 3-567. Instance Table

Instance Name	Physical Address
ECAP0	5024 002Ch
ECAP1	5024 102Ch
ECAP2	5024 202Ch
ECAP3	5024 302Ch
ECAP4	5024 402Ch
ECAP5	5024 502Ch
ECAP6	5024 602Ch
ECAP7	5024 702Ch
ECAP8	5024 802Ch
ECAP9	5024 902Ch

Figure 3-252. ECEINT Name Register

15	14	13	12	11	10	9	8
RESERVED_2			MUNIT_2_ERROR_EVT2	MUNIT_2_ERROR_EVT1	MUNIT_1_ERROR_EVT2	MUNIT_1_ERROR_EVT1	HRERROR
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CTR_EQ_CMP	CTR_EQ_PRD	CTROVF	CEVT4	CEVT3	CEVT2	CEVT1	RESERVED_1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 3-568. ECEINT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_2	R	0h	Reserved Reset Source: ecap_rst_mod_g_rst_n
12	MUNIT_2_ERROR_EVT2	R/W	0h	Monitoring unit 2 error event 2 interrupt enable 0 : Disable Monitoring unit 2 error event 2 interrupt 1 : Enable Monitoring unit 2 error event 2 interrupt Reset Source: ecap_rst_mod_g_rst_n
11	MUNIT_2_ERROR_EVT1	R/W	0h	Monitoring unit 2 error event 2 interrupt enable 0 : Disable Monitoring unit 2 error event 1 interrupt 1 : Enable Monitoring unit 2 error event 1 interrupt Reset Source: ecap_rst_mod_g_rst_n
10	MUNIT_1_ERROR_EVT2	R/W	0h	Monitoring unit 1 error event 1 interrupt enable 0 : Disable Monitoring unit 1 error event 2 interrupt 1 : Enable Monitoring unit 1 error event 2 interrupt Reset Source: ecap_rst_mod_g_rst_n
9	MUNIT_1_ERROR_EVT1	R/W	0h	Monitoring unit 1 error event 1 interrupt enable 0 : Disable Monitoring unit 1 error event 1 interrupt 1 : Enable Monitoring unit 1 error event 1 interrupt Reset Source: ecap_rst_mod_g_rst_n

Table 3-568. ECEINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	HRERROR	R/W	0h	High resolution error interrupt enable Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_enab_HRERROR_in Enable High Resolution Error terrupt as an Interrupt source
7	CTR_EQ_CMP	R/W	0h	Counter Equal Compare Interrupt Enable Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_enab_CE_interru Enable Compare Equal as an pt Interrupt source
6	CTR_EQ_PRD	R/W	0h	Counter Equal Period Interrupt Enable Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_enab_PE_interru Enable Period Equal as an pt Interrupt source
5	CTROVF	R/W	0h	Counter Overflow Interrupt Enable Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_enab_CO_interru Enable counter Overflow as an pt Interrupt source
4	CEVT4	R/W	0h	Capture Event 4 Interrupt Enable Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_enab_Cap4_inter Capture Event 4 Interrupt rupt Enable
3	CEVT3	R/W	0h	Capture Event 3 Interrupt Enable Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_enab_Cap3_inter Enable Capture Event 3 as an rupt Interrupt source
2	CEVT2	R/W	0h	Capture Event 2 Interrupt Enable Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_enab_Cap2_inter Enable Capture Event 2 as an rupt Interrupt source
1	CEVT1	R/W	0h	Capture Event 1 Interrupt Enable Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_enab_Cap1_inter Enable Capture Event 1 as an rupt Interrupt source
0	RESERVED_1	R	0h	Reserved Reset Source: ecap_rst_mod_g_rst_n

3.8.11 MEM_ECFLG Registers

3.8.11.1 MEM_ECFLG Register (Offset = 2Eh) [reset = 0h]

Short Description: Capture Interrupt Flag Re

Long Description: Capture Interrupt Flag Register

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Table 3-569. Instance Table

Instance Name	Physical Address
ECAP0	5024 002Eh
ECAP1	5024 102Eh
ECAP2	5024 202Eh
ECAP3	5024 302Eh
ECAP4	5024 402Eh
ECAP5	5024 502Eh
ECAP6	5024 602Eh
ECAP7	5024 702Eh
ECAP8	5024 802Eh
ECAP9	5024 902Eh

Figure 3-253. ECFLG Name Register

15	14	13	12	11	10	9	8
RESERVED_1			MUNIT_2_ERROR_EVT2	MUNIT_2_ERROR_EVT1	MUNIT_1_ERROR_EVT2	MUNIT_1_ERROR_EVT1	HRERROR
R			R	R	R	R	R
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CTR_CMP	CTR_PRD	CTROVF	CEVT4	CEVT3	CEVT2	CEVT1	INT
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 3-570. ECFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_1	R	0h	Reserved Reset Source: ecap_rst_mod_g_rst_n
12	MUNIT_2_ERROR_EVT2	R	0h	Error event 2 Interrupt Flag from monitoring unit 2 Reset Source: ecap_rst_mod_g_rst_n
11	MUNIT_2_ERROR_EVT1	R	0h	Error event 2 Interrupt Flag from monitoring unit 2 Reset Source: ecap_rst_mod_g_rst_n
10	MUNIT_1_ERROR_EVT2	R	0h	Error event 2 Interrupt Flag from monitoring unit 1 Reset Source: ecap_rst_mod_g_rst_n
9	MUNIT_1_ERROR_EVT1	R	0h	Error event 2 Interrupt Flag from monitoring unit 1 Reset Source: ecap_rst_mod_g_rst_n
8	HRERROR	R	0h	High resolution error status flag Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_indicate_high_r Indicates the High resolution esolution_error Error occurred
7	CTR_CMP	R	0h	Compare Equal Compare Status Flag. This flag is active only in APWM mode. Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_indicate_counte Indicates the counter (TSCTR) r_compare_reg reached the compare register value (ACMP)

Table 3-570. ECFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CTR_PRD	R	0h	Counter Equal Period Status Flag. This flag is only active in APWM mode. Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_indicate_period Indicates the counter (TSCTR) _value_reset reached the period register value (APRD) and was reset.
5	CTROVF	R	0h	Counter Overflow Status Flag. This flag is active in CAP and APWM mode. Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_indicate_counte Indicates the counter (TSCTR) r_trans has made the transition from FFFFFFFF to 00000000
4	CEVT4	R	0h	Capture Event 4 Status Flag This flag is only active in CAP mode. Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_indicate_4th_ev Indicates the fourth event ent_ECAPx occurred at ECAPx pin
3	CEVT3	R	0h	Capture Event 3 Status Flag. This flag is active only in CAP mode. Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_indicate_3rd_ev Indicates the third event ent_ECAPx occurred at ECAPx pin.
2	CEVT2	R	0h	Capture Event 2 Status Flag. This flag is only active in CAP mode. Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_indicate_2nd_ev Indicates the second event ent_ECAPx occurred at ECAPx pin.
1	CEVT1	R	0h	Capture Event 1 Status Flag. This flag is only active in CAP mode. Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_indicate_1st_ev Indicates the first event ent_ECAPx occurred at ECAPx pin.
0	INT	R	0h	Global Interrupt Status Flag Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_indicate_interr Indicates that an interrupt upt was generated.

3.8.12 MEM_ECCLR Registers

3.8.12.1 MEM_ECCLR Register (Offset = 30h) [reset = 0h]

Short Description: Capture Interrupt Clear R

Long Description: Capture Interrupt Clear Register

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Table 3-571. Instance Table

Instance Name	Physical Address
ECAP0	5024 0030h
ECAP1	5024 1030h
ECAP2	5024 2030h
ECAP3	5024 3030h
ECAP4	5024 4030h
ECAP5	5024 5030h
ECAP6	5024 6030h
ECAP7	5024 7030h
ECAP8	5024 8030h
ECAP9	5024 9030h

Figure 3-254. ECCLR Name Register

15	14	13	12	11	10	9	8
RESERVED_1			MUNIT_2_ERROR_EVT2	MUNIT_2_ERROR_EVT1	MUNIT_1_ERROR_EVT2	MUNIT_1_ERROR_EVT1	HRERROR
R			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CTR_CMP	CTR_PRD	CTROVF	CEVT4	CEVT3	CEVT2	CEVT1	INT
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 3-572. ECCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_1	R	0h	Reserved Reset Source: ecap_rst_mod_g_rst_n
12	MUNIT_2_ERROR_EVT2	R/W1TC	0h	Writing '1' clears MUNIT_2_ERROR_EVT2 interrupt flag Reset Source: ecap_rst_mod_g_rst_n
11	MUNIT_2_ERROR_EVT1	R/W1TC	0h	Writing '1' clears MUNIT_2_ERROR_EVT1 interrupt flag Reset Source: ecap_rst_mod_g_rst_n
10	MUNIT_1_ERROR_EVT2	R/W1TC	0h	Writing '1' clears MUNIT_1_ERROR_EVT2 interrupt flag Reset Source: ecap_rst_mod_g_rst_n
9	MUNIT_1_ERROR_EVT1	R/W1TC	0h	Writing '1' clears MUNIT_1_ERROR_EVT1 interrupt flag Reset Source: ecap_rst_mod_g_rst_n
8	HRERROR	R/W1TC	0h	High resolution error status Clear Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_1_clears_HRERRO Writing a 1 clears the HRERROR R flag.
7	CTR_CMP	R/W1TC	0h	Counter Equal Compare Status Clear Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_1_clears_CTR_CM Writing a 1 clears the CTR=CMP P flag.
6	CTR_PRD	R/W1TC	0h	Counter Equal Period Status Clear Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_1_clears_CTR_PR Writing a 1 clears the CTR=PRD D flag.

Table 3-572. ECCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CTROVF	R/W1TC	0h	Counter Overflow Status Clear Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_1_clears_CTROVF Writing a 1 clears the CTROVF flag.
4	CEVT4	R/W1TC	0h	Capture Event 4 Status Clear Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_1_clears_CEVT4 Writing a 1 clears the CEVT4 flag.
3	CEVT3	R/W1TC	0h	Capture Event 3 Status Clear Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_1_clears_CEVT3 Writing a 1 clears the CEVT3 flag.
2	CEVT2	R/W1TC	0h	Capture Event 2 Status Clear Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_1_clears_CEVT2 Writing a 1 clears the CEVT2 flag.
1	CEVT1	R/W1TC	0h	Capture Event 1 Status Clear Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_1_clears_CEVT1 Writing a 1 clears the CEVT1 flag.
0	INT	R/W1TC	0h	ECAP Global Interrupt Status Clear Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_1_clears_INT Writing a 1 clears the INT flag and enable further interrupts to be generated if any of the event flags are set to 1

3.8.13 MEM_ECFRC Registers

3.8.13.1 MEM_ECFRC Register (Offset = 32h) [reset = 0h]

Short Description: Capture Interrupt Force R

Long Description: Capture Interrupt Force Register

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Table 3-573. Instance Table

Instance Name	Physical Address
ECAP0	5024 0032h
ECAP1	5024 1032h
ECAP2	5024 2032h
ECAP3	5024 3032h
ECAP4	5024 4032h
ECAP5	5024 5032h
ECAP6	5024 6032h
ECAP7	5024 7032h
ECAP8	5024 8032h
ECAP9	5024 9032h

Figure 3-255. ECFRC Name Register

15	14	13	12	11	10	9	8
RESERVED_2			MUNIT_2_ERROR_EVT2	MUNIT_2_ERROR_EVT1	MUNIT_1_ERROR_EVT2	MUNIT_1_ERROR_EVT1	HRERROR
R			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CTR_CMP	CTR_PRD	CTROVF	CEVT4	CEVT3	CEVT2	CEVT1	RESERVED_1
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R
0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 3-574. ECFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_2	R	0h	Reserved Reset Source: ecap_rst_mod_g_rst_n
12	MUNIT_2_ERROR_EVT2	R/W1TS	0h	Writing '1' sets MUNIT_2_ERROR_EVT2 interrupt flag Reset Source: ecap_rst_mod_g_rst_n
11	MUNIT_2_ERROR_EVT1	R/W1TS	0h	Writing '1' sets MUNIT_2_ERROR_EVT1 interrupt flag Reset Source: ecap_rst_mod_g_rst_n
10	MUNIT_1_ERROR_EVT2	R/W1TS	0h	Writing '1' sets MUNIT_1_ERROR_EVT2 interrupt flag Reset Source: ecap_rst_mod_g_rst_n
9	MUNIT_1_ERROR_EVT1	R/W1TS	0h	Writing '1' sets MUNIT_1_ERROR_EVT1 interrupt flag Reset Source: ecap_rst_mod_g_rst_n
8	HRERROR	R/W1TS	0h	High resolution error Force interrupt Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_1_sets_CTR_CMP Writing a 1 sets the CTR_CMP flag.
7	CTR_CMP	R/W1TS	0h	Force Counter Equal Compare Interrupt. This event is only active in APWM mode. Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_1_sets_CTR_CMP Writing a 1 sets the CTR_CMP flag.
6	CTR_PRD	R/W1TS	0h	Force Counter Equal Period Interrupt. This event is only active in APWM mode. Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_1_clears_CTR_PR Writing a 1 sets the CTR_PRD D flag.

Table 3-574. ECFRC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CTROVF	R/W1TS	0h	Force Counter Overflow Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_1_sets_CTROVF Writing a 1 to this bit sets the CTROVF flag.
4	CEVT4	R/W1TS	0h	Force Capture Event 4. This event is only active in CAP mode. Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_1_sets_CEVT4 Writing a 1 sets the CEVT4 flag.
3	CEVT3	R/W1TS	0h	Force Capture Event 3. This event is only active in CAP mode. Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_1_sets_CEVT3 Writing a 1 sets the CEVT3 flag.
2	CEVT2	R/W1TS	0h	Force Capture Event 2. This event is only active in CAP mode. Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_1_sets_CEVT2 Writing a 1 sets the CEVT2 flag.
1	CEVT1	R/W1TS	0h	Force Capture Event 1. This event is only active in CAP mode. Reset Source: ecap_rst_mod_g_rst_n 1 Ecap_1_sets_CEVT1 Sets the CEVT1 flag.
0	RESERVED_1	R	0h	Reserved Reset Source: ecap_rst_mod_g_rst_n

3.8.14 MEM_ECAPSYNCINSEL Registers

3.8.14.1 MEM_ECAPSYNCINSEL Register (Offset = 3Ch) [reset = 1h]

Short Description: SYNC source select regist

Long Description: SYNC source select register

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Table 3-575. Instance Table

Instance Name	Physical Address
ECAP0	5024 003Ch
ECAP1	5024 103Ch
ECAP2	5024 203Ch
ECAP3	5024 303Ch
ECAP4	5024 403Ch
ECAP5	5024 503Ch
ECAP6	5024 603Ch
ECAP7	5024 703Ch
ECAP8	5024 803Ch
ECAP9	5024 903Ch

Figure 3-256. ECAPSYNCINSEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1									SEL						
R									R/W						
0h									1h						

Access Types Legend

Table 3-576. ECAPSYNCINSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED_1	R	0h	Reserved Reset Source: ecap_rst_mod_g_rst_n
6:0	SEL	R/W	1h	These bits determines the source of SYNCIN signal. 0x0 : Disabled using SOC tieoff. 0x7F : Reset Source: ecap_rst_mod_g_rst_n

3.8.15 MEM_HRCTL Registers

3.8.15.1 MEM_HRCTL Register (Offset = 40h) [reset = 0h]

Short Description: High-Res Control Register

Long Description: High-Res Control Register

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Table 3-577. Instance Table

Instance Name	Physical Address
ECAP0	5024 0040h
ECAP1	5024 1040h
ECAP2	5024 2040h
ECAP3	5024 3040h
ECAP4	5024 4040h
ECAP5	5024 5040h
ECAP6	5024 6040h
ECAP7	5024 7040h
ECAP8	5024 8040h
ECAP9	5024 9040h

Figure 3-257. HRCTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1										CALIBCONT	CALIBSTS	CALIBSTART	PRDSEL	HRCLKE	HRE
R/W										R/W	R	R/W1TS	R/W	R/W	R/W
0h										0h	0h	0h	0h	0h	0h

Access Types Legend

Table 3-578. HRCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED_1	R/W	0h	Reserved Reset Source: ecap_rst_mod_g_rst_n
5	CALIBCONT	R/W	0h	Continuous mode Calibration Select Bit: 0 Continuous mode disabled. 1 Continuous mode enabled. Calibration automatically restarts at end of current calibration cycle. Reset Source: ecap_rst_mod_g_rst_n
4	CALIBSTS	R	0h	Calibration status Bit: 0 No active calibration cycle 1 Calibration cycle in progress Reset Source: ecap_rst_mod_g_rst_n
3	CALIBSTART	R/W1TS	0h	Calibration start Bit: 0 No effect 1 Starts the calibration cycle Reset Source: ecap_rst_mod_g_rst_n
2	PRDSEL	R/W	0h	Calibration Period Match Select Bit: 0 Use SYSCLK Counter For Period Match [default at reset] 1 Reserved Reset Source: ecap_rst_mod_g_rst_n
1	HRCLKE	R/W	0h	High Resolution Clock Enable Bit: 0 High resolution clock disabled [default at reset] 1 High resolution clock enabled. The clock should be enabled before enabling the high res function via the HRE bit. Reset Source: ecap_rst_mod_g_rst_n

Table 3-578. HRCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HRE	R/W	0h	High Resolution Enable Bit: 0 High resolution mode disabled [default at reset] 1 High resolution mode enabled. Enabling this mode will connect the capture registers and edge event modes of the ECAP to be accessed by the High Res function. Note: The High Res clock needs to be enabled [using the HRCLKE bit] first before enabling the module. Allow a certain start up stabilization period before enabling the module. Reset Source: ecap_rst_mod_g_rst_n

3.8.16 MEM_HRINTEN Registers

3.8.16.1 MEM_HRINTEN Register (Offset = 48h) [reset = 0h]

Short Description: High-Res Calibration Inte

Long Description: High-Res Calibration Interrupt Enable Register

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Table 3-579. Instance Table

Instance Name	Physical Address
ECAP0	5024 0048h
ECAP1	5024 1048h
ECAP2	5024 2048h
ECAP3	5024 3048h
ECAP4	5024 4048h
ECAP5	5024 5048h
ECAP6	5024 6048h
ECAP7	5024 7048h
ECAP8	5024 8048h
ECAP9	5024 9048h

Figure 3-258. HRINTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_2															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2													CALPRDCHKSTS	CALIBDONE	RESERVED_1
R													R/W	R/W	R
0h													0h	0h	0h

Access Types Legend

Table 3-580. HRINTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED_2	R	0h	Reserved Reset Source: ecap_rst_mod_g_rst_n
2	CALPRDCHKSTS	R/W	0h	Calibration Period Check status Interrupt Enable: 0 Disable Calibration Period Check interrupt status 1 Enable Calibration Period Check interrupt status Reset Source: ecap_rst_mod_g_rst_n
1	CALIBDONE	R/W	0h	Calibration done Interrupt Enable: 0 Disable Calibration done Interrupt 1 Enable Calibration done Interrupt Reset Source: ecap_rst_mod_g_rst_n
0	RESERVED_1	R	0h	Reserved Reset Source: ecap_rst_mod_g_rst_n

3.8.17 MEM_HRFLG Registers

3.8.17.1 MEM_HRFLG Register (Offset = 4Ch) [reset = 0h]

Short Description: High-Res Calibration Inte

Long Description: High-Res Calibration Interrupt Flag Register

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Table 3-581. Instance Table

Instance Name	Physical Address
ECAP0	5024 004Ch
ECAP1	5024 104Ch
ECAP2	5024 204Ch
ECAP3	5024 304Ch
ECAP4	5024 404Ch
ECAP5	5024 504Ch
ECAP6	5024 604Ch
ECAP7	5024 704Ch
ECAP8	5024 804Ch
ECAP9	5024 904Ch

Figure 3-259. HRFLG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1													CALPRDCHKSTS	CALIBDONE	CALIBINT
R													R	R	R
0h													0h	0h	0h

Access Types Legend

Table 3-582. HRFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED_1	R	0h	Reserved Reset Source: ecap_rst_mod_g_rst_n
2	CALPRDCHKSTS	R	0h	Calibration period check status Flag Bit: 1 Indicates that calibration ended before PRDCHK due to overflow on one of the counters. 0 Indicates no event occurred. Note: This bit remains latched until cleared by the user using the HRCLR [CALPRDCHKSTS] bit. Reset Source: ecap_rst_mod_g_rst_n
1	CALIBDONE	R	0h	Calibration Done Interrupt Flag Bit: 1 Indicates calibration cycle is completed 0 Indicates calibration cycle has not completed. Note: This bit remains latched until cleared by the user using the HRCLR [CALIBDONE] bit. Reset Source: ecap_rst_mod_g_rst_n
0	CALIBINT	R	0h	Global calibration Interrupt Status Flag: 1 Indicates that an interrupt was generated from CALIBDONE or CALPRDCHKSTS. 0 Indicates no interrupt generated. Reset Source: ecap_rst_mod_g_rst_n

3.8.18 MEM_HRCLR Registers

3.8.18.1 MEM_HRCLR Register (Offset = 50h) [reset = 0h]

Short Description: High-Res Calibration Inte

Long Description: High-Res Calibration Interrupt Clear Register

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Table 3-583. Instance Table

Instance Name	Physical Address
ECAP0	5024 0050h
ECAP1	5024 1050h
ECAP2	5024 2050h
ECAP3	5024 3050h
ECAP4	5024 4050h
ECAP5	5024 5050h
ECAP6	5024 6050h
ECAP7	5024 7050h
ECAP8	5024 8050h
ECAP9	5024 9050h

Figure 3-260. HRCLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1													CALPRDCHKSTS	CALIBDONE	CALIBINT
R													R/W1TC	R/W1TC	R/W1TC
0h													0h	0h	0h

Access Types Legend

Table 3-584. HRCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED_1	R	0h	Reserved Reset Source: ecap_rst_mod_g_rst_n
2	CALPRDCHKSTS	R/W1TC	0h	Clear Calibration period check status Flag Bit: 1 Clears the CALPRDCHKSTS flag register bit. 0 No effect. Note: H/W has priority over CPU writes if the user tries to clear a flag bit and an event occurs on the same cycle that tries to set the flag for the selected bit. Reset Source: ecap_rst_mod_g_rst_n
1	CALIBDONE	R/W1TC	0h	Clear Calibration Done Interrupt Flag Bit: 1 Clears the CALIBDONE interrupt flag register bit. 0 No effect. Note: H/W has priority over CPU writes if the user tries to clear a flag bit and an event occurs on the same cycle that tries to set the flag for the selected bit. Reset Source: ecap_rst_mod_g_rst_n
0	CALIBINT	R/W1TC	0h	Clear Global calibration Interrupt Flag 1 Clears the Global interrupt flag and enables further interrupts to be generated if any of the event flags are set. 0 No effect. Reset Source: ecap_rst_mod_g_rst_n

3.8.19 MEM_HRFRC Registers

3.8.19.1 MEM_HRFRC Register (Offset = 54h) [reset = 0h]

Short Description: High-Res Calibration Inte

Long Description: High-Res Calibration Interrupt Force Register

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Table 3-585. Instance Table

Instance Name	Physical Address
ECAP0	5024 0054h
ECAP1	5024 1054h
ECAP2	5024 2054h
ECAP3	5024 3054h
ECAP4	5024 4054h
ECAP5	5024 5054h
ECAP6	5024 6054h
ECAP7	5024 7054h
ECAP8	5024 8054h
ECAP9	5024 9054h

Figure 3-261. HRFRC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_2															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2													CALPRDCHKSTS	CALIBDONE	RESERVED_1
R													R/W1TS	R/W1TS	R
0h													0h	0h	0h

Access Types Legend

Table 3-586. HRFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED_2	R	0h	Reserved Reset Source: ecap_rst_mod_g_rst_n
2	CALPRDCHKSTS	R/W1TS	0h	Force CALPRDCHKSTS flag: 0 No effect 1 Sets the CALPRDCHKSTS flag. Reset Source: ecap_rst_mod_g_rst_n
1	CALIBDONE	R/W1TS	0h	Force CALIBDONE flag: 0 No effect 1 Sets the CALIBDONE flag. Reset Source: ecap_rst_mod_g_rst_n
0	RESERVED_1	R	0h	Reserved Reset Source: ecap_rst_mod_g_rst_n

3.8.20 MEM_HRCALPRD Registers

3.8.20.1 MEM_HRCALPRD Register (Offset = 58h) [reset = 3fffffh]

Short Description: High-Res Calibration Peri

Long Description: High-Res Calibration Period Register

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Table 3-587. Instance Table

Instance Name	Physical Address
ECAP0	5024 0058h
ECAP1	5024 1058h
ECAP2	5024 2058h
ECAP3	5024 3058h
ECAP4	5024 4058h
ECAP5	5024 5058h
ECAP6	5024 6058h
ECAP7	5024 7058h
ECAP8	5024 8058h
ECAP9	5024 9058h

Figure 3-262. HRCALPRD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRD															
R/W															
3fffffh															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRD															
R/W															
3fffffh															

Access Types Legend

Table 3-588. HRCALPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PRD	R/W	3FFFFFh	Register to program calibration period. The period value is matched against HRSYSCLKCTR. On a match an interrupt is generated and the counter registers values are captured. Reset Source: ecap_rst_mod_g_rst_n

3.8.21 MEM_HRSYSCLKCTR Registers

3.8.21.1 MEM_HRSYSCLKCTR Register (Offset = 5Ch) [reset = 0h]

Short Description: High-Res Calibration SYSC

Long Description: High-Res Calibration SYSCLK Counter Register

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Table 3-589. Instance Table

Instance Name	Physical Address
ECAP0	5024 005Ch
ECAP1	5024 105Ch
ECAP2	5024 205Ch
ECAP3	5024 305Ch
ECAP4	5024 405Ch
ECAP5	5024 505Ch
ECAP6	5024 605Ch
ECAP7	5024 705Ch
ECAP8	5024 805Ch
ECAP9	5024 905Ch

Figure 3-263. HRSYSCLKCTR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HRSYSCLKCTR															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HRSYSCLKCTR															
R															
0h															

Access Types Legend

Table 3-590. HRSYSCLKCTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HRSYSCLKCTR	R	0h	Current SYSCLK counter value Reset Source: ecap_rst_mod_g_rst_n

3.8.22 MEM_HRSYSCLKCAP Registers

3.8.22.1 MEM_HRSYSCLKCAP Register (Offset = 60h) [reset = 0h]

Short Description: High-Res Calibration SYSC

Long Description: High-Res Calibration SYSCLK Capture Register

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Table 3-591. Instance Table

Instance Name	Physical Address
ECAP0	5024 0060h
ECAP1	5024 1060h
ECAP2	5024 2060h
ECAP3	5024 3060h
ECAP4	5024 4060h
ECAP5	5024 5060h
ECAP6	5024 6060h
ECAP7	5024 7060h
ECAP8	5024 8060h
ECAP9	5024 9060h

Figure 3-264. HRSYSCLKCAP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HRSYSCLKCAP															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HRSYSCLKCAP															
R															
0h															

Access Types Legend

Table 3-592. HRSYSCLKCAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HRSYSCLKCAP	R	0h	HRSYSCLKCTR is captures into this register at end of calibration cycle. Reset Source: ecap_rst_mod_g_rst_n

3.8.23 MEM_HRCLKCTR Registers

3.8.23.1 MEM_HRCLKCTR Register (Offset = 64h) [reset = 0h]

Short Description: High-Res Calibration HRCL

Long Description: High-Res Calibration HRCLK Counter Register

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Table 3-593. Instance Table

Instance Name	Physical Address
ECAP0	5024 0064h
ECAP1	5024 1064h
ECAP2	5024 2064h
ECAP3	5024 3064h
ECAP4	5024 4064h
ECAP5	5024 5064h
ECAP6	5024 6064h
ECAP7	5024 7064h
ECAP8	5024 8064h
ECAP9	5024 9064h

Figure 3-265. HRCLKCTR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HRCLKCTR															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HRCLKCTR															
R															
0h															

Access Types Legend

Table 3-594. HRCLKCTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HRCLKCTR	R	0h	Current HRCLK counter value Note: HRCLK is not synchronized to SYSCLK domain so reads may not be accurate Reset Source: ecap_rst_mod_g_rst_n

3.8.24 MEM_HRCLKCAP Registers

3.8.24.1 MEM_HRCLKCAP Register (Offset = 68h) [reset = 0h]

Short Description: High-Res Calibration HRCL

Long Description: High-Res Calibration HRCLK Capture Register

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Table 3-595. Instance Table

Instance Name	Physical Address
ECAP0	5024 0068h
ECAP1	5024 1068h
ECAP2	5024 2068h
ECAP3	5024 3068h
ECAP4	5024 4068h
ECAP5	5024 5068h
ECAP6	5024 6068h
ECAP7	5024 7068h
ECAP8	5024 8068h
ECAP9	5024 9068h

Figure 3-266. HRCLKCAP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HRCLKCAP															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HRCLKCAP															
R															
0h															

Access Types Legend

Table 3-596. HRCLKCAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HRCLKCAP	R	0h	HRCLKCTR is captures into this register at end of calibration cycle. Note: HRCLK is not synchronized to SYSCLK domain so reads may not be accurate Reset Source: ecap_rst_mod_g_rst_n

3.8.25 MEM_HRDEBUGCTL Registers

3.8.25.1 MEM_HRDEBUGCTL Register (Offset = 74h) [reset = 0h]

Short Description: High-Res Debug control re

Long Description: High-Res Debug control register

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Table 3-597. Instance Table

Instance Name	Physical Address
ECAP0	5024 0074h
ECAP1	5024 1074h
ECAP2	5024 2074h
ECAP3	5024 3074h
ECAP4	5024 4074h
ECAP5	5024 5074h
ECAP6	5024 6074h
ECAP7	5024 7074h
ECAP8	5024 8074h
ECAP9	5024 9074h

Figure 3-267. HRDEBUGCTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_3				OBSERVE_SRC_SEL				RESERVED_2		CALIB_INPUT_SEL		RESERVED_1	CAPIN_MMAP_SOURCE	DELAYRESETDLINE	DISABLEINVSEL
R				R/W				R		R/W		R	R/W	R/W	R/W
0h				0h				0h		0h		0h	0h	0h	0h

Access Types Legend

Table 3-598. HRDEBUGCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_3	R	0h	Reserved Reset Source: ecap_rst_mod_g_rst_n
11:8	OBSERVE_SRC_SEL	R/W	0h	Select bits for selecting source for OBSERVE1 and OBSERVE2 registers 1000 HROUTH and HROUTL will read HR1OUT 1001 HROUTH and HROUTL will read HR2OUT 1010 HROUTH and HROUTL will read Capture Delayline 1 OBS1 1011 HROUTH and HROUTL will read Capture Delayline 2 OBS1 1100 HROUTH and HROUTL will read Capture Delayline 1 OBS2 1101 HROUTH and HROUTL will read Capture Delayline 2 OBS2 Reset Source: ecap_rst_mod_g_rst_n
7:6	RESERVED_2	R	0h	Reserved Reset Source: ecap_rst_mod_g_rst_n

Table 3-598. HRDEBUGCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	CALIB_INPUT_SEL	R/W	0h	Select bit for calibration input, can be used to get fault coverage using these inputs 00 CAPIN is one of 128 inputs selected by INPUTSEL 01 CAPIN is connected to CAPIN_MEMMAP_SOURCE 10 CAPIN is internally generated signal waveform with 8*HRCLK cycle high and 8*HRCLK cycle low, used for linearity check of capture delay line 1 11 CAPIN is internally generated signal waveform with 8*HRCLK cycle high and 8*HRCLK cycle low, delayed by half HRCLK, used for linearity check of capture delay line 2 Reset Source: ecap_rst_mod_g_rst_n
3	RESERVED_1	R	0h	Reserved Reset Source: ecap_rst_mod_g_rst_n
2	CAPIN_MMAP_SOURCE	R/W	0h	Memory mapped CAPIN source Note : select CALIN source first, it may happen that you may see interrupt if MMAP source is different from current value of CAPIN. This is debug feature hence no additional HW is necessary to prevent this. Reset Source: ecap_rst_mod_g_rst_n
1	DELAYRESETDLINE	R/W	0h	Controls the reset delayline timing 0 reset is forced on next falling edge of HRCLK [1/2 cycle after capture] 1 reset is applied a cycle later [1 1/2 cycles after capture] Reset Source: ecap_rst_mod_g_rst_n
0	DISABLEINVSEL	R/W	0h	Disable INVSEL Logic: 0 State machine controls inversion on input signal 1 CAPIN signal propagated into delay line without inversion, this means only rising edges can be measured Reset Source: ecap_rst_mod_g_rst_n

3.8.26 MEM_HRDEBUGOBSERVE1 Registers

3.8.26.1 MEM_HRDEBUGOBSERVE1 Register (Offset = 78h) [reset = 0h]

Short Description: High-Res Raw output &

Long Description: High-Res Raw output & internal nodes of HRCLK capture delay line

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Table 3-599. Instance Table

Instance Name	Physical Address
ECAP0	5024 0078h
ECAP1	5024 1078h
ECAP2	5024 2078h
ECAP3	5024 3078h
ECAP4	5024 4078h
ECAP5	5024 5078h
ECAP6	5024 6078h
ECAP7	5024 7078h
ECAP8	5024 8078h
ECAP9	5024 9078h

Figure 3-268. HRDEBUGOBSERVE1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HROUTH															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HROUTH															
R															
0h															

Access Types Legend

Table 3-600. HRDEBUGOBSERVE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HROUTH	R	0h	Reads raw output of HROUT capture delay line 1 Reset Source: ecap_rst_mod_g_rst_n

3.8.27 MEM_HRDEBUGOBSERVE2 Registers

3.8.27.1 MEM_HRDEBUGOBSERVE2 Register (Offset = 7Ch) [reset = 0h]

Short Description: High-Res Raw output &

Long Description: High-Res Raw output & internal nodes of HRCLK capture delay line

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Table 3-601. Instance Table

Instance Name	Physical Address
ECAP0	5024 007Ch
ECAP1	5024 107Ch
ECAP2	5024 207Ch
ECAP3	5024 307Ch
ECAP4	5024 407Ch
ECAP5	5024 507Ch
ECAP6	5024 607Ch
ECAP7	5024 707Ch
ECAP8	5024 807Ch
ECAP9	5024 907Ch

Figure 3-269. HRDEBUGOBSERVE2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HROUTL															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HROUTL															
R															
0h															

Access Types Legend

Table 3-602. HRDEBUGOBSERVE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HROUTL	R	0h	Reads raw output of HROUT capture delay line 2 Reset Source: ecap_rst_mod_g_rst_n

3.8.28 MEM_MUNIT_COMMON_CTL Registers

3.8.28.1 MEM_COMMON_CTL Register (Offset = 80h) [reset = 0h]

Short Description: Control registers for mon

Long Description: Control registers for monitoring unit {#}

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Table 3-603. Instance Table

Instance Name	Physical Address
ECAP0	5024 0080h
ECAP1	5024 1080h
ECAP2	5024 2080h
ECAP3	5024 3080h
ECAP4	5024 4080h
ECAP5	5024 5080h
ECAP6	5024 6080h
ECAP7	5024 7080h
ECAP8	5024 8080h
ECAP9	5024 9080h

Figure 3-270. MUNIT_COMMON_CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2	GLDSTRBSEL							RESERVED_1	TRIPSEL						
R	R/W							R	R/W						
0h	0h							0h	0h						

Access Types Legend

Table 3-604. MUNIT_COMMON_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_3	R	0h	Reserved Reset Source: ecap_rst_mod_g_rst_n
15	RESERVED_2	R	0h	Reserved Reset Source: ecap_rst_mod_g_rst_n
14:8	GLDSTRBSEL	R/W	0h	Global load strobe select to enable shadow to active loading 0x0 : Disabled with SOC level tieoff. 0x1 to 0x7F : Global load strobe from SOC level including ETPWM global load strobes. Reset Source: ecap_rst_mod_g_rst_n
7	RESERVED_1	R	0h	Reserved Reset Source: ecap_rst_mod_g_rst_n
6:0	TRIPSEL	R/W	0h	Trip signal select to disable and enable signal monitoring automatically 0x0 : Disabled, Trip signals does not affect signal monitoring, achieved with SOC level tieoff. 0x1 to 0x7F : Signal monioring is disabled when selected signal is high and enabled when it is low Reset Source: ecap_rst_mod_g_rst_n

3.8.29 MEM_MUNIT_1_CTL Registers

3.8.29.1 MEM_1_CTL Register (Offset = C0h) [reset = 0h]

Short Description: Control registers for mon

Long Description: Control registers for monitoring unit 1

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Table 3-605. Instance Table

Instance Name	Physical Address
ECAP0	5024 00C0h
ECAP1	5024 10C0h
ECAP2	5024 20C0h
ECAP3	5024 30C0h
ECAP4	5024 40C0h
ECAP5	5024 50C0h
ECAP6	5024 60C0h
ECAP7	5024 70C0h
ECAP8	5024 80C0h
ECAP9	5024 90C0h

Figure 3-271. MUNIT_1_CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2				MON_SEL				RESERVED_1						DEBUG_RANGE_EN	EN
R				R/W				R						R/W	R/W
0h				0h				0h						0h	0h

Access Types Legend

Table 3-606. MUNIT_1_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_3	R	0h	Reserved Reset Source: ecap_rst_mod_g_rst_n
15:12	RESERVED_2	R	0h	Reserved Reset Source: ecap_rst_mod_g_rst_n
11:8	MON_SEL	R/W	0h	Type of monitoring 0 : High Pulse width 1 : Low Pulse width 2 : Period width from Rise to Rise 3 : Period width from fall to fall 4 : Monitor rise edge 5 : Monitor fall edge 6-15 : Reserved [High Pulse width] Reset Source: ecap_rst_mod_g_rst_n
7:2	RESERVED_1	R	0h	Reserved Reset Source: ecap_rst_mod_g_rst_n
1	DEBUG_RANGE_EN	R/W	0h	Debug mode enable. 0 : Debug mode is disabled. 1 : Debug mode of monitoring unit 1 is enabled to obtain the variation seen in the system for debug purpose. Range is captured in MUNIT_1_DEBUG_RANGE_MIN and MUNIT_1_DEBUG_RANGE_MAX registers Toggle DEBUG_RANGE_EN to restart this process, this will initialize MUNIT_1_DEBUG_RANGE_MIN and MUNIT_1_DEBUG_RANGE_MAX registers. Reset Source: ecap_rst_mod_g_rst_n

Table 3-606. MUNIT_1_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	EN	R/W	0h	0 : Monitoring unit 1 is disabled 1 : Monitoring unit 1 is enabled Reset Source: ecap_rst_mod_g_rst_n

3.8.30 MEM_MUNIT_1_SHADOW_CTL Registers

3.8.30.1 MEM_1_SHADOW_CTL Register (Offset = C4h) [reset = 0h]

Short Description: Shadow control registers

Long Description: Shadow control registers for monitoring unit 1

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Table 3-607. Instance Table

Instance Name	Physical Address
ECAP0	5024 00C4h
ECAP1	5024 10C4h
ECAP2	5024 20C4h
ECAP3	5024 30C4h
ECAP4	5024 40C4h
ECAP5	5024 50C4h
ECAP6	5024 60C4h
ECAP7	5024 70C4h
ECAP8	5024 80C4h
ECAP9	5024 90C4h

Figure 3-272. MUNIT_1_SHADOW_CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1													LOADMODE	SWSYNC	SYNCI_EN
R													R/W	R/W1TS	R/W
0h													0h	0h	0h

Access Types Legend

Table 3-608. MUNIT_1_SHADOW_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED_1	R	0h	Reserved Reset Source: ecap_rst_mod_g_rst_n
2	LOADMODE	R/W	0h	Load mode 0 : Active registers are loaded with shadow on next sync event 1 : Active registers are loaded with shadow on EPWMx.GLDLCSTRB event Reset Source: ecap_rst_mod_g_rst_n
1	SWSYNC	R/W1TS	0h	Copies Min and Max values from shadow to active registers immediately if MUNIT_1_SHADOW_CTL.SYNCI_EN is set. Reset Source: ecap_rst_mod_g_rst_n
0	SYNCI_EN	R/W	0h	Shadow Enable 0 : Disabled 1 : Enabled Reset Source: ecap_rst_mod_g_rst_n

3.8.31 MEM_MUNIT_1_MIN Registers

3.8.31.1 MEM_1_MIN Register (Offset = D0h) [reset = 0h]

Short Description: Min value for monitoring

Long Description: Min value for monitoring unit 1

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Table 3-609. Instance Table

Instance Name	Physical Address
ECAP0	5024 00D0h
ECAP1	5024 10D0h
ECAP2	5024 20D0h
ECAP3	5024 30D0h
ECAP4	5024 40D0h
ECAP5	5024 50D0h
ECAP6	5024 60D0h
ECAP7	5024 70D0h
ECAP8	5024 80D0h
ECAP9	5024 90D0h

Figure 3-273. MUNIT_1_MIN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MIN_VALUE															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIN_VALUE															
R/W															
0h															

Access Types Legend

Table 3-610. MUNIT_1_MIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MIN_VALUE	R/W	0h	Minimum value for monitoring Reset Source: ecap_rst_mod_g_rst_n

3.8.32 MEM_MUNIT_1_MAX Registers

3.8.32.1 MEM_1_MAX Register (Offset = D4h) [reset = 0h]

Short Description: Max value for monitoring

Long Description: Max value for monitoring unit 1

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Table 3-611. Instance Table

Instance Name	Physical Address
ECAP0	5024 00D4h
ECAP1	5024 10D4h
ECAP2	5024 20D4h
ECAP3	5024 30D4h
ECAP4	5024 40D4h
ECAP5	5024 50D4h
ECAP6	5024 60D4h
ECAP7	5024 70D4h
ECAP8	5024 80D4h
ECAP9	5024 90D4h

Figure 3-274. MUNIT_1_MAX Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MAX_VALUE															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAX_VALUE															
R/W															
0h															

Access Types Legend

Table 3-612. MUNIT_1_MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MAX_VALUE	R/W	0h	Maximum value for monitoring Reset Source: ecap_rst_mod_g_rst_n

3.8.33 MEM_MUNIT_1_MIN_SHADOW Registers

3.8.33.1 MEM_1_MIN_SHADOW Register (Offset = D8h) [reset = 0h]

Short Description: Shadow register for Min v

Long Description: Shadow register for Min value of monitoring unit 1

Return to Summary Table

Table 3-613. Instance Table

Instance Name	Physical Address
ECAP0	5024 00D8h
ECAP1	5024 10D8h
ECAP2	5024 20D8h
ECAP3	5024 30D8h
ECAP4	5024 40D8h
ECAP5	5024 50D8h
ECAP6	5024 60D8h
ECAP7	5024 70D8h
ECAP8	5024 80D8h
ECAP9	5024 90D8h

Figure 3-275. MUNIT_1_MIN_SHADOW Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MIN_VALUE_SHADOW															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIN_VALUE_SHADOW															
R/W															
0h															

Access Types Legend

Table 3-614. MUNIT_1_MIN_SHADOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MIN_VALUE_SHADOW	R/W	0h	Shadow minimum value for monitoring. Shadow value is loaded to active register on Sync event or global load strobe. Reset Source: ecap_rst_mod_g_rst_n

3.8.34 MEM_MUNIT_1_MAX_SHADOW Registers

3.8.34.1 MEM_1_MAX_SHADOW Register (Offset = DCh) [reset = 0h]

Short Description: Shadow register for Max v

Long Description: Shadow register for Max value of monitoring unit 1

Return to Summary Table

Table 3-615. Instance Table

Instance Name	Physical Address
ECAP0	5024 00DCh
ECAP1	5024 10DCh
ECAP2	5024 20DCh
ECAP3	5024 30DCh
ECAP4	5024 40DCh
ECAP5	5024 50DCh
ECAP6	5024 60DCh
ECAP7	5024 70DCh
ECAP8	5024 80DCh
ECAP9	5024 90DCh

Figure 3-276. MUNIT_1_MAX_SHADOW Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MAX_VALUE_SHADOW															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAX_VALUE_SHADOW															
R/W															
0h															

Access Types Legend

Table 3-616. MUNIT_1_MAX_SHADOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MAX_VALUE_SHADOW	R/W	0h	Shadow maximum value for monitoring. Shadow value is loaded to active register on Sync event or global load strobe. Reset Source: ecap_rst_mod_g_rst_n

3.8.35 MEM_MUNIT_1_DEBUG_RANGE_MIN Registers

3.8.35.1 MEM_1_DEBUG_RANGE_MIN Register (Offset = E0h) [reset = ffffffffh]

Short Description: Observed Min value of che

Long Description: Observed Min value of check being enabled on minotoring unit 1

Return to Summary Table

Table 3-617. Instance Table

Instance Name	Physical Address
ECAP0	5024 00E0h
ECAP1	5024 10E0h
ECAP2	5024 20E0h
ECAP3	5024 30E0h
ECAP4	5024 40E0h
ECAP5	5024 50E0h
ECAP6	5024 60E0h
ECAP7	5024 70E0h
ECAP8	5024 80E0h
ECAP9	5024 90E0h

Figure 3-277. MUNIT_1_DEBUG_RANGE_MIN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MIN_VALUE															
R															
ffffffffh															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIN_VALUE															
R															
ffffffffh															

Access Types Legend

Table 3-618. MUNIT_1_DEBUG_RANGE_MIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MIN_VALUE	R	FFFFFFFFh	Observed Min value of check being enabled on minotoring unit 1. Is updated when MUNIT_1_CTL.DEBUG_RANGE_EN is set to '1' Reset Source: ecap_rst_mod_g_rst_n

3.8.36 MEM_MUNIT_1_DEBUG_RANGE_MAX Registers

3.8.36.1 MEM_1_DEBUG_RANGE_MAX Register (Offset = E4h) [reset = 0h]

Short Description: Observed Max value of che

Long Description: Observed Max value of check being enabled on minotoring unit 1

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Table 3-619. Instance Table

Instance Name	Physical Address
ECAP0	5024 00E4h
ECAP1	5024 10E4h
ECAP2	5024 20E4h
ECAP3	5024 30E4h
ECAP4	5024 40E4h
ECAP5	5024 50E4h
ECAP6	5024 60E4h
ECAP7	5024 70E4h
ECAP8	5024 80E4h
ECAP9	5024 90E4h

Figure 3-278. MUNIT_1_DEBUG_RANGE_MAX Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MAX_VALUE															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAX_VALUE															
R															
0h															

Access Types Legend

Table 3-620. MUNIT_1_DEBUG_RANGE_MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MAX_VALUE	R	0h	Observed Min value of check being enabled on minotoring unit 1. Is updated when MUNIT_1_CTL.DEBUG_RANGE_EN is set to '1' Reset Source: ecap_rst_mod_g_rst_n

3.8.37 MEM_MUNIT_2_CTL Registers

3.8.37.1 MEM_2_CTL Register (Offset = 100h) [reset = 0h]

Short Description: Control registers for mon

Long Description: Control registers for monitoring unit 2

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Table 3-621. Instance Table

Instance Name	Physical Address
ECAP0	5024 0100h
ECAP1	5024 1100h
ECAP2	5024 2100h
ECAP3	5024 3100h
ECAP4	5024 4100h
ECAP5	5024 5100h
ECAP6	5024 6100h
ECAP7	5024 7100h
ECAP8	5024 8100h
ECAP9	5024 9100h

Figure 3-279. MUNIT_2_CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2				MON_SEL				RESERVED_1						DEBUG_RANGE_EN	EN
R				R/W				R						R/W	R/W
0h				0h				0h						0h	0h

Access Types Legend

Table 3-622. MUNIT_2_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_3	R	0h	Reserved Reset Source: ecap_rst_mod_g_rst_n
15:12	RESERVED_2	R	0h	Reserved Reset Source: ecap_rst_mod_g_rst_n
11:8	MON_SEL	R/W	0h	Type of monitoring 0 : High Pulse width 1 : Low Pulse width 2 : Period width from Rise to Rise 3 : Period width from fall to fall 4 : Monitor rise edge 5 : Monitor fall edge 6-15 : Reserved [High Pulse width] Reset Source: ecap_rst_mod_g_rst_n
7:2	RESERVED_1	R	0h	Reserved Reset Source: ecap_rst_mod_g_rst_n
1	DEBUG_RANGE_EN	R/W	0h	Debug mode enable. 0 : Debug mode is disabled. 1 : Debug mode of monitoring unit 2 is enabled to obtain the variation seen in the system for debug purpose. Range is captured in MUNIT_2_DEBUG_RANGE_MIN and MUNIT_2_DEBUG_RANGE_MAX registers Toggle DEBUG_RANGE_EN to restart this process, this will initialize MUNIT_2_DEBUG_RANGE_MIN and MUNIT_2_DEBUG_RANGE_MAX registers. Reset Source: ecap_rst_mod_g_rst_n

Table 3-622. MUNIT_2_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	EN	R/W	0h	0 : Monitoring unit 2 is disabled 1 : Monitoring unit 2 is enabled Reset Source: ecap_rst_mod_g_rst_n

3.8.38 MEM_MUNIT_2_SHADOW_CTL Registers

3.8.38.1 MEM_2_SHADOW_CTL Register (Offset = 104h) [reset = 0h]

Short Description: Shadow control registers

Long Description: Shadow control registers for monitoring unit 2

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Table 3-623. Instance Table

Instance Name	Physical Address
ECAP0	5024 0104h
ECAP1	5024 1104h
ECAP2	5024 2104h
ECAP3	5024 3104h
ECAP4	5024 4104h
ECAP5	5024 5104h
ECAP6	5024 6104h
ECAP7	5024 7104h
ECAP8	5024 8104h
ECAP9	5024 9104h

Figure 3-280. MUNIT_2_SHADOW_CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1													LOADMODE	SWSYNC	SYNCI_EN
R													R/W	R/W1TS	R/W
0h													0h	0h	0h

Access Types Legend

Table 3-624. MUNIT_2_SHADOW_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED_1	R	0h	Reserved Reset Source: ecap_rst_mod_g_rst_n
2	LOADMODE	R/W	0h	Load mode 0 : Active registers are loaded with shadow on next sync event 1 : Active registers are loaded with shadow on EPWMx.GLDLCSTRB event Reset Source: ecap_rst_mod_g_rst_n
1	SWSYNC	R/W1TS	0h	Copies Min and Max values from shadow to active registers immediately if MUNIT_2_SHADOW_CTL.SYNCI_EN is set. Reset Source: ecap_rst_mod_g_rst_n
0	SYNCI_EN	R/W	0h	Shadow Enable 0 : Disabled 1 : Enabled Reset Source: ecap_rst_mod_g_rst_n

3.8.39 MEM_MUNIT_2_MIN Registers

3.8.39.1 MEM_2_MIN Register (Offset = 110h) [reset = 0h]

Short Description: Min value for monitoring

Long Description: Min value for monitoring unit 2

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Table 3-625. Instance Table

Instance Name	Physical Address
ECAP0	5024 0110h
ECAP1	5024 1110h
ECAP2	5024 2110h
ECAP3	5024 3110h
ECAP4	5024 4110h
ECAP5	5024 5110h
ECAP6	5024 6110h
ECAP7	5024 7110h
ECAP8	5024 8110h
ECAP9	5024 9110h

Figure 3-281. MUNIT_2_MIN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MIN_VALUE															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIN_VALUE															
R/W															
0h															

Access Types Legend

Table 3-626. MUNIT_2_MIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MIN_VALUE	R/W	0h	Minimum value for monitoring Reset Source: ecap_rst_mod_g_rst_n

3.8.40 MEM_MUNIT_2_MAX Registers

3.8.40.1 MEM_2_MAX Register (Offset = 114h) [reset = 0h]

Short Description: Max value for monitoring

Long Description: Max value for monitoring unit 2

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Table 3-627. Instance Table

Instance Name	Physical Address
ECAP0	5024 0114h
ECAP1	5024 1114h
ECAP2	5024 2114h
ECAP3	5024 3114h
ECAP4	5024 4114h
ECAP5	5024 5114h
ECAP6	5024 6114h
ECAP7	5024 7114h
ECAP8	5024 8114h
ECAP9	5024 9114h

Figure 3-282. MUNIT_2_MAX Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MAX_VALUE															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAX_VALUE															
R/W															
0h															

Access Types Legend

Table 3-628. MUNIT_2_MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MAX_VALUE	R/W	0h	Maximum value for monitoring Reset Source: ecap_rst_mod_g_rst_n

3.8.41 MEM_MUNIT_2_MIN_SHADOW Registers

3.8.41.1 MEM_2_MIN_SHADOW Register (Offset = 118h) [reset = 0h]

Short Description: Shadow register for Min v

Long Description: Shadow register for Min value of monitoring unit 2

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Table 3-629. Instance Table

Instance Name	Physical Address
ECAP0	5024 0118h
ECAP1	5024 1118h
ECAP2	5024 2118h
ECAP3	5024 3118h
ECAP4	5024 4118h
ECAP5	5024 5118h
ECAP6	5024 6118h
ECAP7	5024 7118h
ECAP8	5024 8118h
ECAP9	5024 9118h

Figure 3-283. MUNIT_2_MIN_SHADOW Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MIN_VALUE_SHADOW															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIN_VALUE_SHADOW															
R/W															
0h															

Access Types Legend

Table 3-630. MUNIT_2_MIN_SHADOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MIN_VALUE_SHADOW	R/W	0h	Shadow minimum value for monitoring. Shadow value is loaded to active register on Sync event or global load strobe. Reset Source: ecap_rst_mod_g_rst_n

3.8.42 MEM_MUNIT_2_MAX_SHADOW Registers

3.8.42.1 MEM_2_MAX_SHADOW Register (Offset = 11Ch) [reset = 0h]

Short Description: Shadow register for Max v

Long Description: Shadow register for Max value of monitoring unit 2

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Table 3-631. Instance Table

Instance Name	Physical Address
ECAP0	5024 011Ch
ECAP1	5024 111Ch
ECAP2	5024 211Ch
ECAP3	5024 311Ch
ECAP4	5024 411Ch
ECAP5	5024 511Ch
ECAP6	5024 611Ch
ECAP7	5024 711Ch
ECAP8	5024 811Ch
ECAP9	5024 911Ch

Figure 3-284. MUNIT_2_MAX_SHADOW Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MAX_VALUE_SHADOW															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAX_VALUE_SHADOW															
R/W															
0h															

Access Types Legend

Table 3-632. MUNIT_2_MAX_SHADOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MAX_VALUE_SHADOW	R/W	0h	Shadow maximum value for monitoring. Shadow value is loaded to active register on Sync event or global load strobe. Reset Source: ecap_rst_mod_g_rst_n

3.8.43 MEM_MUNIT_2_DEBUG_RANGE_MIN Registers

3.8.43.1 MEM_2_DEBUG_RANGE_MIN Register (Offset = 120h) [reset = ffffffffh]

Short Description: Observed Min value of che

Long Description: Observed Min value of check being enabled on minotoring unit 2

Return to Summary Table

Table 3-633. Instance Table

Instance Name	Physical Address
ECAP0	5024 0120h
ECAP1	5024 1120h
ECAP2	5024 2120h
ECAP3	5024 3120h
ECAP4	5024 4120h
ECAP5	5024 5120h
ECAP6	5024 6120h
ECAP7	5024 7120h
ECAP8	5024 8120h
ECAP9	5024 9120h

Figure 3-285. MUNIT_2_DEBUG_RANGE_MIN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MIN_VALUE															
R															
ffffffffh															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIN_VALUE															
R															
ffffffffh															

Access Types Legend

Table 3-634. MUNIT_2_DEBUG_RANGE_MIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MIN_VALUE	R	FFFFFFFFh	Observed Min value of check being enabled on minotoring unit 2. Is updated when MUNIT_2_CTL.DEBUG_RANGE_EN is set to '1' Reset Source: ecap_rst_mod_g_rst_n

3.8.44 MEM_MUNIT_2_DEBUG_RANGE_MAX Registers

3.8.44.1 MEM_2_DEBUG_RANGE_MAX Register (Offset = 124h) [reset = 0h]

Short Description: Observed Max value of che

Long Description: Observed Max value of check being enabled on minotoring unit 2

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Table 3-635. Instance Table

Instance Name	Physical Address
ECAP0	5024 0124h
ECAP1	5024 1124h
ECAP2	5024 2124h
ECAP3	5024 3124h
ECAP4	5024 4124h
ECAP5	5024 5124h
ECAP6	5024 6124h
ECAP7	5024 7124h
ECAP8	5024 8124h
ECAP9	5024 9124h

Figure 3-286. MUNIT_2_DEBUG_RANGE_MAX Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MAX_VALUE															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAX_VALUE															
R															
0h															

Access Types Legend

Table 3-636. MUNIT_2_DEBUG_RANGE_MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MAX_VALUE	R	0h	Observed Min value of check being enabled on minotoring unit 2. Is updated when MUNIT_2_CTL.DEBUG_RANGE_EN is set to '1' Reset Source: ecap_rst_mod_g_rst_n

3.8.45 Access Table

Table 3-637. Access Type Codes

Access Type	Code	Description
R/W	R/W	Read / Write
R	R	Read
R/W1TC	R/W1TC	Read/Write 1 To Clear
R/W1TS	R/W1TS	Read/Write 1 To Set

3.9 EPWM Registers

Table 3-638. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM0_ G0 Physical Address	CONTROLSS_EPWM1_ G0 Physical Address	CONTROLSS_EPWM10_ G0 Physical Address
0h	16	TBCTL	5000 0000h	5000 1000h	5000 A000h
2h	16	TBCTL2	5000 0002h	5000 1002h	5000 A002h
6h	16	EPWMSYNCINSEL	5000 0006h	5000 1006h	5000 A006h
8h	16	TBCTR	5000 0008h	5000 1008h	5000 A008h
Ah	16	TBSTS	5000 000Ah	5000 100Ah	5000 A00Ah
Ch	16	EPWMSYNCOUTEN	5000 000Ch	5000 100Ch	5000 A00Ch
Eh	16	TBCTL3	5000 000Eh	5000 100Eh	5000 A00Eh
10h	16	CMPCTL	5000 0010h	5000 1010h	5000 A010h
12h	16	CMPCTL2	5000 0012h	5000 1012h	5000 A012h
18h	16	DBCTL	5000 0018h	5000 1018h	5000 A018h
1Ah	16	DBCTL2	5000 001Ah	5000 101Ah	5000 A01Ah
20h	16	AQCTL	5000 0020h	5000 1020h	5000 A020h
22h	16	AQTSRCSEL	5000 0022h	5000 1022h	5000 A022h
28h	16	PCCTL	5000 0028h	5000 1028h	5000 A028h
30h	16	VCAPCTL	5000 0030h	5000 1030h	5000 A030h
32h	16	VCNTCFG	5000 0032h	5000 1032h	5000 A032h
40h	16	HRCNFG	5000 0040h	5000 1040h	5000 A040h
4Eh	16	HRCNFG2	5000 004Eh	5000 104Eh	5000 A04Eh
5Ah	16	HRPCTL	5000 005Ah	5000 105Ah	5000 A05Ah
5Ch	16	TRREM	5000 005Ch	5000 105Ch	5000 A05Ch
68h	16	GLDCTL	5000 0068h	5000 1068h	5000 A068h
6Ah	16	GLDCFG	5000 006Ah	5000 106Ah	5000 A06Ah
70h	32	EPWMXLINK	5000 0070h	5000 1070h	5000 A070h

Table 3-639. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM11_ G0 Physical Address	CONTROLSS_EPWM12_ G0 Physical Address	CONTROLSS_EPWM13_ G0 Physical Address
0h	16	TBCTL	5000 B000h	5000 C000h	5000 D000h
2h	16	TBCTL2	5000 B002h	5000 C002h	5000 D002h
6h	16	EPWMSYNCINSEL	5000 B006h	5000 C006h	5000 D006h
8h	16	TBCTR	5000 B008h	5000 C008h	5000 D008h
Ah	16	TBSTS	5000 B00Ah	5000 C00Ah	5000 D00Ah
Ch	16	EPWMSYNCOUTEN	5000 B00Ch	5000 C00Ch	5000 D00Ch
Eh	16	TBCTL3	5000 B00Eh	5000 C00Eh	5000 D00Eh
10h	16	CMPCTL	5000 B010h	5000 C010h	5000 D010h
12h	16	CMPCTL2	5000 B012h	5000 C012h	5000 D012h
18h	16	DBCTL	5000 B018h	5000 C018h	5000 D018h
1Ah	16	DBCTL2	5000 B01Ah	5000 C01Ah	5000 D01Ah
20h	16	AQCTL	5000 B020h	5000 C020h	5000 D020h
22h	16	AQTSRCSEL	5000 B022h	5000 C022h	5000 D022h
28h	16	PCCTL	5000 B028h	5000 C028h	5000 D028h
30h	16	VCAPCTL	5000 B030h	5000 C030h	5000 D030h
32h	16	VCNTCFG	5000 B032h	5000 C032h	5000 D032h
40h	16	HRCNFG	5000 B040h	5000 C040h	5000 D040h

Table 3-639. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_EPWM11_ G0 Physical Address	CONTROLSS_EPWM12_ G0 Physical Address	CONTROLSS_EPWM13_ G0 Physical Address
4Eh	16	HRCNFG2	5000 B04Eh	5000 C04Eh	5000 D04Eh
5Ah	16	HRPCTL	5000 B05Ah	5000 C05Ah	5000 D05Ah
5Ch	16	TRREM	5000 B05Ch	5000 C05Ch	5000 D05Ch
68h	16	GLDCTL	5000 B068h	5000 C068h	5000 D068h
6Ah	16	GLDCFG	5000 B06Ah	5000 C06Ah	5000 D06Ah
70h	32	EPWMXLINK	5000 B070h	5000 C070h	5000 D070h

Table 3-640. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM14_ G0 Physical Address	CONTROLSS_EPWM15_ G0 Physical Address	CONTROLSS_EPWM16_ G0 Physical Address
0h	16	TBCTL	5000 E000h	5000 F000h	5001 0000h
2h	16	TBCTL2	5000 E002h	5000 F002h	5001 0002h
6h	16	EPWMSYNCINSEL	5000 E006h	5000 F006h	5001 0006h
8h	16	TBCTR	5000 E008h	5000 F008h	5001 0008h
Ah	16	TBSTS	5000 E00Ah	5000 F00Ah	5001 000Ah
Ch	16	EPWMSYNCOUTEN	5000 E00Ch	5000 F00Ch	5001 000Ch
Eh	16	TBCTL3	5000 E00Eh	5000 F00Eh	5001 000Eh
10h	16	CMPCTL	5000 E010h	5000 F010h	5001 0010h
12h	16	CMPCTL2	5000 E012h	5000 F012h	5001 0012h
18h	16	DBCTL	5000 E018h	5000 F018h	5001 0018h
1Ah	16	DBCTL2	5000 E01Ah	5000 F01Ah	5001 001Ah
20h	16	AQCTL	5000 E020h	5000 F020h	5001 0020h
22h	16	AQTSRCSEL	5000 E022h	5000 F022h	5001 0022h
28h	16	PCCTL	5000 E028h	5000 F028h	5001 0028h
30h	16	VCAPCTL	5000 E030h	5000 F030h	5001 0030h
32h	16	VCNTCFG	5000 E032h	5000 F032h	5001 0032h
40h	16	HRCNFG	5000 E040h	5000 F040h	5001 0040h
4Eh	16	HRCNFG2	5000 E04Eh	5000 F04Eh	5001 004Eh
5Ah	16	HRPCTL	5000 E05Ah	5000 F05Ah	5001 005Ah
5Ch	16	TRREM	5000 E05Ch	5000 F05Ch	5001 005Ch
68h	16	GLDCTL	5000 E068h	5000 F068h	5001 0068h
6Ah	16	GLDCFG	5000 E06Ah	5000 F06Ah	5001 006Ah
70h	32	EPWMXLINK	5000 E070h	5000 F070h	5001 0070h

Table 3-641. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM17_ G0 Physical Address	CONTROLSS_EPWM18_ G0 Physical Address	CONTROLSS_EPWM19_ G0 Physical Address
0h	16	TBCTL	5001 1000h	5001 2000h	5001 3000h
2h	16	TBCTL2	5001 1002h	5001 2002h	5001 3002h
6h	16	EPWMSYNCINSEL	5001 1006h	5001 2006h	5001 3006h
8h	16	TBCTR	5001 1008h	5001 2008h	5001 3008h
Ah	16	TBSTS	5001 100Ah	5001 200Ah	5001 300Ah
Ch	16	EPWMSYNCOUTEN	5001 100Ch	5001 200Ch	5001 300Ch
Eh	16	TBCTL3	5001 100Eh	5001 200Eh	5001 300Eh
10h	16	CMPCTL	5001 1010h	5001 2010h	5001 3010h
12h	16	CMPCTL2	5001 1012h	5001 2012h	5001 3012h

Table 3-641. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_EPWM17_ G0 Physical Address	CONTROLSS_EPWM18_ G0 Physical Address	CONTROLSS_EPWM19_ G0 Physical Address
18h	16	DBCTL	5001 1018h	5001 2018h	5001 3018h
1Ah	16	DBCTL2	5001 101Ah	5001 201Ah	5001 301Ah
20h	16	AQCTL	5001 1020h	5001 2020h	5001 3020h
22h	16	AQTSRCSEL	5001 1022h	5001 2022h	5001 3022h
28h	16	PCCTL	5001 1028h	5001 2028h	5001 3028h
30h	16	VCAPCTL	5001 1030h	5001 2030h	5001 3030h
32h	16	VCNTCFG	5001 1032h	5001 2032h	5001 3032h
40h	16	HRCNFG	5001 1040h	5001 2040h	5001 3040h
4Eh	16	HRCNFG2	5001 104Eh	5001 204Eh	5001 304Eh
5Ah	16	HRPCTL	5001 105Ah	5001 205Ah	5001 305Ah
5Ch	16	TRREM	5001 105Ch	5001 205Ch	5001 305Ch
68h	16	GLDCTL	5001 1068h	5001 2068h	5001 3068h
6Ah	16	GLDCFG	5001 106Ah	5001 206Ah	5001 306Ah
70h	32	EPWMXLINK	5001 1070h	5001 2070h	5001 3070h

Table 3-642. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM2_ G0 Physical Address	CONTROLSS_EPWM20_ G0 Physical Address	CONTROLSS_EPWM21_ G0 Physical Address
0h	16	TBCTL	5000 2000h	5001 4000h	5001 5000h
2h	16	TBCTL2	5000 2002h	5001 4002h	5001 5002h
6h	16	EPWMSYNCINSEL	5000 2006h	5001 4006h	5001 5006h
8h	16	TBCTR	5000 2008h	5001 4008h	5001 5008h
Ah	16	TBSTS	5000 200Ah	5001 400Ah	5001 500Ah
Ch	16	EPWMSYNCOUTEN	5000 200Ch	5001 400Ch	5001 500Ch
Eh	16	TBCTL3	5000 200Eh	5001 400Eh	5001 500Eh
10h	16	CMPCTL	5000 2010h	5001 4010h	5001 5010h
12h	16	CMPCTL2	5000 2012h	5001 4012h	5001 5012h
18h	16	DBCTL	5000 2018h	5001 4018h	5001 5018h
1Ah	16	DBCTL2	5000 201Ah	5001 401Ah	5001 501Ah
20h	16	AQCTL	5000 2020h	5001 4020h	5001 5020h
22h	16	AQTSRCSEL	5000 2022h	5001 4022h	5001 5022h
28h	16	PCCTL	5000 2028h	5001 4028h	5001 5028h
30h	16	VCAPCTL	5000 2030h	5001 4030h	5001 5030h
32h	16	VCNTCFG	5000 2032h	5001 4032h	5001 5032h
40h	16	HRCNFG	5000 2040h	5001 4040h	5001 5040h
4Eh	16	HRCNFG2	5000 204Eh	5001 404Eh	5001 504Eh
5Ah	16	HRPCTL	5000 205Ah	5001 405Ah	5001 505Ah
5Ch	16	TRREM	5000 205Ch	5001 405Ch	5001 505Ch
68h	16	GLDCTL	5000 2068h	5001 4068h	5001 5068h
6Ah	16	GLDCFG	5000 206Ah	5001 406Ah	5001 506Ah
70h	32	EPWMXLINK	5000 2070h	5001 4070h	5001 5070h

Table 3-643. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM22_ G0 Physical Address	CONTROLSS_EPWM23_ G0 Physical Address	CONTROLSS_EPWM24_ G0 Physical Address
0h	16	TBCTL	5001 6000h	5001 7000h	5001 8000h

Table 3-643. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_EPWM22_ G0 Physical Address	CONTROLSS_EPWM23_ G0 Physical Address	CONTROLSS_EPWM24_ G0 Physical Address
2h	16	TBCTL2	5001 6002h	5001 7002h	5001 8002h
6h	16	EPWMSYNCINSEL	5001 6006h	5001 7006h	5001 8006h
8h	16	TBCTR	5001 6008h	5001 7008h	5001 8008h
Ah	16	TBSTS	5001 600Ah	5001 700Ah	5001 800Ah
Ch	16	EPWMSYNCOUTEN	5001 600Ch	5001 700Ch	5001 800Ch
Eh	16	TBCTL3	5001 600Eh	5001 700Eh	5001 800Eh
10h	16	CMPCTL	5001 6010h	5001 7010h	5001 8010h
12h	16	CMPCTL2	5001 6012h	5001 7012h	5001 8012h
18h	16	DBCTL	5001 6018h	5001 7018h	5001 8018h
1Ah	16	DBCTL2	5001 601Ah	5001 701Ah	5001 801Ah
20h	16	AQCTL	5001 6020h	5001 7020h	5001 8020h
22h	16	AQTSRCSEL	5001 6022h	5001 7022h	5001 8022h
28h	16	PCCTL	5001 6028h	5001 7028h	5001 8028h
30h	16	VCAPCTL	5001 6030h	5001 7030h	5001 8030h
32h	16	VCNTCFG	5001 6032h	5001 7032h	5001 8032h
40h	16	HRCNFG	5001 6040h	5001 7040h	5001 8040h
4Eh	16	HRCNFG2	5001 604Eh	5001 704Eh	5001 804Eh
5Ah	16	HRPCTL	5001 605Ah	5001 705Ah	5001 805Ah
5Ch	16	TRREM	5001 605Ch	5001 705Ch	5001 805Ch
68h	16	GLDCTL	5001 6068h	5001 7068h	5001 8068h
6Ah	16	GLDCFG	5001 606Ah	5001 706Ah	5001 806Ah
70h	32	EPWMXLINK	5001 6070h	5001 7070h	5001 8070h

Table 3-644. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM25_ G0 Physical Address	CONTROLSS_EPWM26_ G0 Physical Address	CONTROLSS_EPWM27_ G0 Physical Address
0h	16	TBCTL	5001 9000h	5001 A000h	5001 B000h
2h	16	TBCTL2	5001 9002h	5001 A002h	5001 B002h
6h	16	EPWMSYNCINSEL	5001 9006h	5001 A006h	5001 B006h
8h	16	TBCTR	5001 9008h	5001 A008h	5001 B008h
Ah	16	TBSTS	5001 900Ah	5001 A00Ah	5001 B00Ah
Ch	16	EPWMSYNCOUTEN	5001 900Ch	5001 A00Ch	5001 B00Ch
Eh	16	TBCTL3	5001 900Eh	5001 A00Eh	5001 B00Eh
10h	16	CMPCTL	5001 9010h	5001 A010h	5001 B010h
12h	16	CMPCTL2	5001 9012h	5001 A012h	5001 B012h
18h	16	DBCTL	5001 9018h	5001 A018h	5001 B018h
1Ah	16	DBCTL2	5001 901Ah	5001 A01Ah	5001 B01Ah
20h	16	AQCTL	5001 9020h	5001 A020h	5001 B020h
22h	16	AQTSRCSEL	5001 9022h	5001 A022h	5001 B022h
28h	16	PCCTL	5001 9028h	5001 A028h	5001 B028h
30h	16	VCAPCTL	5001 9030h	5001 A030h	5001 B030h
32h	16	VCNTCFG	5001 9032h	5001 A032h	5001 B032h
40h	16	HRCNFG	5001 9040h	5001 A040h	5001 B040h
4Eh	16	HRCNFG2	5001 904Eh	5001 A04Eh	5001 B04Eh
5Ah	16	HRPCTL	5001 905Ah	5001 A05Ah	5001 B05Ah
5Ch	16	TRREM	5001 905Ch	5001 A05Ch	5001 B05Ch

Table 3-644. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_EPWM25_ G0 Physical Address	CONTROLSS_EPWM26_ G0 Physical Address	CONTROLSS_EPWM27_ G0 Physical Address
68h	16	GLDCTL	5001 9068h	5001 A068h	5001 B068h
6Ah	16	GLDCFG	5001 906Ah	5001 A06Ah	5001 B06Ah
70h	32	EPWMXLINK	5001 9070h	5001 A070h	5001 B070h

Table 3-645. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM28_ G0 Physical Address	CONTROLSS_EPWM29_ G0 Physical Address	CONTROLSS_EPWM3_ G0 Physical Address
0h	16	TBCTL	5001 C000h	5001 D000h	5000 3000h
2h	16	TBCTL2	5001 C002h	5001 D002h	5000 3002h
6h	16	EPWMSYNCINSEL	5001 C006h	5001 D006h	5000 3006h
8h	16	TBCTR	5001 C008h	5001 D008h	5000 3008h
Ah	16	TBSTS	5001 C00Ah	5001 D00Ah	5000 300Ah
Ch	16	EPWMSYNCOUTEN	5001 C00Ch	5001 D00Ch	5000 300Ch
Eh	16	TBCTL3	5001 C00Eh	5001 D00Eh	5000 300Eh
10h	16	CMPCTL	5001 C010h	5001 D010h	5000 3010h
12h	16	CMPCTL2	5001 C012h	5001 D012h	5000 3012h
18h	16	DBCTL	5001 C018h	5001 D018h	5000 3018h
1Ah	16	DBCTL2	5001 C01Ah	5001 D01Ah	5000 301Ah
20h	16	AQCTL	5001 C020h	5001 D020h	5000 3020h
22h	16	AQTSRCSEL	5001 C022h	5001 D022h	5000 3022h
28h	16	PCCTL	5001 C028h	5001 D028h	5000 3028h
30h	16	VCAPCTL	5001 C030h	5001 D030h	5000 3030h
32h	16	VCNTCFG	5001 C032h	5001 D032h	5000 3032h
40h	16	HRCNFG	5001 C040h	5001 D040h	5000 3040h
4Eh	16	HRCNFG2	5001 C04Eh	5001 D04Eh	5000 304Eh
5Ah	16	HRPCTL	5001 C05Ah	5001 D05Ah	5000 305Ah
5Ch	16	TRREM	5001 C05Ch	5001 D05Ch	5000 305Ch
68h	16	GLDCTL	5001 C068h	5001 D068h	5000 3068h
6Ah	16	GLDCFG	5001 C06Ah	5001 D06Ah	5000 306Ah
70h	32	EPWMXLINK	5001 C070h	5001 D070h	5000 3070h

Table 3-646. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM30_ G0 Physical Address	CONTROLSS_EPWM31_ G0 Physical Address	CONTROLSS_EPWM4_ G0 Physical Address
0h	16	TBCTL	5001 E000h	5001 F000h	5000 4000h
2h	16	TBCTL2	5001 E002h	5001 F002h	5000 4002h
6h	16	EPWMSYNCINSEL	5001 E006h	5001 F006h	5000 4006h
8h	16	TBCTR	5001 E008h	5001 F008h	5000 4008h
Ah	16	TBSTS	5001 E00Ah	5001 F00Ah	5000 400Ah
Ch	16	EPWMSYNCOUTEN	5001 E00Ch	5001 F00Ch	5000 400Ch
Eh	16	TBCTL3	5001 E00Eh	5001 F00Eh	5000 400Eh
10h	16	CMPCTL	5001 E010h	5001 F010h	5000 4010h
12h	16	CMPCTL2	5001 E012h	5001 F012h	5000 4012h
18h	16	DBCTL	5001 E018h	5001 F018h	5000 4018h
1Ah	16	DBCTL2	5001 E01Ah	5001 F01Ah	5000 401Ah
20h	16	AQCTL	5001 E020h	5001 F020h	5000 4020h

Table 3-646. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_EPWM30_ G0 Physical Address	CONTROLSS_EPWM31_ G0 Physical Address	CONTROLSS_EPWM4_ G0 Physical Address
22h	16	AQTSRCSEL	5001 E022h	5001 F022h	5000 4022h
28h	16	PCCTL	5001 E028h	5001 F028h	5000 4028h
30h	16	VCAPCTL	5001 E030h	5001 F030h	5000 4030h
32h	16	VCNTCFG	5001 E032h	5001 F032h	5000 4032h
40h	16	HRCNFG	5001 E040h	5001 F040h	5000 4040h
4Eh	16	HRCNFG2	5001 E04Eh	5001 F04Eh	5000 404Eh
5Ah	16	HRPCTL	5001 E05Ah	5001 F05Ah	5000 405Ah
5Ch	16	TRREM	5001 E05Ch	5001 F05Ch	5000 405Ch
68h	16	GLDCTL	5001 E068h	5001 F068h	5000 4068h
6Ah	16	GLDCFG	5001 E06Ah	5001 F06Ah	5000 406Ah
70h	32	EPWMXLINK	5001 E070h	5001 F070h	5000 4070h

Table 3-647. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM5_ G0 Physical Address	CONTROLSS_EPWM6_ G0 Physical Address	CONTROLSS_EPWM7_ G0 Physical Address
0h	16	TBCTL	5000 5000h	5000 6000h	5000 7000h
2h	16	TBCTL2	5000 5002h	5000 6002h	5000 7002h
6h	16	EPWMSYNCINSEL	5000 5006h	5000 6006h	5000 7006h
8h	16	TBCTR	5000 5008h	5000 6008h	5000 7008h
Ah	16	TBSTS	5000 500Ah	5000 600Ah	5000 700Ah
Ch	16	EPWMSYNCOUTEN	5000 500Ch	5000 600Ch	5000 700Ch
Eh	16	TBCTL3	5000 500Eh	5000 600Eh	5000 700Eh
10h	16	CMPCTL	5000 5010h	5000 6010h	5000 7010h
12h	16	CMPCTL2	5000 5012h	5000 6012h	5000 7012h
18h	16	DBCTL	5000 5018h	5000 6018h	5000 7018h
1Ah	16	DBCTL2	5000 501Ah	5000 601Ah	5000 701Ah
20h	16	AQCTL	5000 5020h	5000 6020h	5000 7020h
22h	16	AQTSRCSEL	5000 5022h	5000 6022h	5000 7022h
28h	16	PCCTL	5000 5028h	5000 6028h	5000 7028h
30h	16	VCAPCTL	5000 5030h	5000 6030h	5000 7030h
32h	16	VCNTCFG	5000 5032h	5000 6032h	5000 7032h
40h	16	HRCNFG	5000 5040h	5000 6040h	5000 7040h
4Eh	16	HRCNFG2	5000 504Eh	5000 604Eh	5000 704Eh
5Ah	16	HRPCTL	5000 505Ah	5000 605Ah	5000 705Ah
5Ch	16	TRREM	5000 505Ch	5000 605Ch	5000 705Ch
68h	16	GLDCTL	5000 5068h	5000 6068h	5000 7068h
6Ah	16	GLDCFG	5000 506Ah	5000 606Ah	5000 706Ah
70h	32	EPWMXLINK	5000 5070h	5000 6070h	5000 7070h

Table 3-648. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM8_ G0 Physical Address	CONTROLSS_EPWM9_ G0 Physical Address	CONTROLSS_EPWM0_ G1 Physical Address
0h	16	TBCTL	5000 8000h	5000 9000h	5004 0000h
2h	16	TBCTL2	5000 8002h	5000 9002h	5004 0002h
6h	16	EPWMSYNCINSEL	5000 8006h	5000 9006h	5004 0006h
8h	16	TBCTR	5000 8008h	5000 9008h	5004 0008h

Table 3-648. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_EPWM8_ G0 Physical Address	CONTROLSS_EPWM9_ G0 Physical Address	CONTROLSS_EPWM0_ G1 Physical Address
Ah	16	TBSTS	5000 800Ah	5000 900Ah	5004 000Ah
Ch	16	EPWMSYNCOUTEN	5000 800Ch	5000 900Ch	5004 000Ch
Eh	16	TBCTL3	5000 800Eh	5000 900Eh	5004 000Eh
10h	16	CMPCTL	5000 8010h	5000 9010h	5004 0010h
12h	16	CMPCTL2	5000 8012h	5000 9012h	5004 0012h
18h	16	DBCTL	5000 8018h	5000 9018h	5004 0018h
1Ah	16	DBCTL2	5000 801Ah	5000 901Ah	5004 001Ah
20h	16	AQCTL	5000 8020h	5000 9020h	5004 0020h
22h	16	AQTSRCSEL	5000 8022h	5000 9022h	5004 0022h
28h	16	PCCTL	5000 8028h	5000 9028h	5004 0028h
30h	16	VCAPCTL	5000 8030h	5000 9030h	5004 0030h
32h	16	VCNTCFG	5000 8032h	5000 9032h	5004 0032h
40h	16	HRCNFG	5000 8040h	5000 9040h	5004 0040h
4Eh	16	HRCNFG2	5000 804Eh	5000 904Eh	5004 004Eh
5Ah	16	HRPCTL	5000 805Ah	5000 905Ah	5004 005Ah
5Ch	16	TRREM	5000 805Ch	5000 905Ch	5004 005Ch
68h	16	GLDCTL	5000 8068h	5000 9068h	5004 0068h
6Ah	16	GLDCFG	5000 806Ah	5000 906Ah	5004 006Ah
70h	32	EPWMXLINK	5000 8070h	5000 9070h	5004 0070h

Table 3-649. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM1_ G1 Physical Address	CONTROLSS_EPWM10_ G1 Physical Address	CONTROLSS_EPWM11_ G1 Physical Address
0h	16	TBCTL	5004 1000h	5004 A000h	5004 B000h
2h	16	TBCTL2	5004 1002h	5004 A002h	5004 B002h
6h	16	EPWMSYNCINSEL	5004 1006h	5004 A006h	5004 B006h
8h	16	TBCTR	5004 1008h	5004 A008h	5004 B008h
Ah	16	TBSTS	5004 100Ah	5004 A00Ah	5004 B00Ah
Ch	16	EPWMSYNCOUTEN	5004 100Ch	5004 A00Ch	5004 B00Ch
Eh	16	TBCTL3	5004 100Eh	5004 A00Eh	5004 B00Eh
10h	16	CMPCTL	5004 1010h	5004 A010h	5004 B010h
12h	16	CMPCTL2	5004 1012h	5004 A012h	5004 B012h
18h	16	DBCTL	5004 1018h	5004 A018h	5004 B018h
1Ah	16	DBCTL2	5004 101Ah	5004 A01Ah	5004 B01Ah
20h	16	AQCTL	5004 1020h	5004 A020h	5004 B020h
22h	16	AQTSRCSEL	5004 1022h	5004 A022h	5004 B022h
28h	16	PCCTL	5004 1028h	5004 A028h	5004 B028h
30h	16	VCAPCTL	5004 1030h	5004 A030h	5004 B030h
32h	16	VCNTCFG	5004 1032h	5004 A032h	5004 B032h
40h	16	HRCNFG	5004 1040h	5004 A040h	5004 B040h
4Eh	16	HRCNFG2	5004 104Eh	5004 A04Eh	5004 B04Eh
5Ah	16	HRPCTL	5004 105Ah	5004 A05Ah	5004 B05Ah
5Ch	16	TRREM	5004 105Ch	5004 A05Ch	5004 B05Ch
68h	16	GLDCTL	5004 1068h	5004 A068h	5004 B068h
6Ah	16	GLDCFG	5004 106Ah	5004 A06Ah	5004 B06Ah

Table 3-649. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_EPWM1_ G1 Physical Address	CONTROLSS_EPWM10_ G1 Physical Address	CONTROLSS_EPWM11_ G1 Physical Address
70h	32	EPWMXLINK	5004 1070h	5004 A070h	5004 B070h

Table 3-650. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM12_ G1 Physical Address	CONTROLSS_EPWM13_ G1 Physical Address	CONTROLSS_EPWM14_ G1 Physical Address
0h	16	TBCTL	5004 C000h	5004 D000h	5004 E000h
2h	16	TBCTL2	5004 C002h	5004 D002h	5004 E002h
6h	16	EPWMSYNCINSEL	5004 C006h	5004 D006h	5004 E006h
8h	16	TBCTR	5004 C008h	5004 D008h	5004 E008h
Ah	16	TBSTS	5004 C00Ah	5004 D00Ah	5004 E00Ah
Ch	16	EPWMSYNCOUTEN	5004 C00Ch	5004 D00Ch	5004 E00Ch
Eh	16	TBCTL3	5004 C00Eh	5004 D00Eh	5004 E00Eh
10h	16	CMPCTL	5004 C010h	5004 D010h	5004 E010h
12h	16	CMPCTL2	5004 C012h	5004 D012h	5004 E012h
18h	16	DBCTL	5004 C018h	5004 D018h	5004 E018h
1Ah	16	DBCTL2	5004 C01Ah	5004 D01Ah	5004 E01Ah
20h	16	AQCTL	5004 C020h	5004 D020h	5004 E020h
22h	16	AQTSRCSEL	5004 C022h	5004 D022h	5004 E022h
28h	16	PCCTL	5004 C028h	5004 D028h	5004 E028h
30h	16	VCAPCTL	5004 C030h	5004 D030h	5004 E030h
32h	16	VCNTCFG	5004 C032h	5004 D032h	5004 E032h
40h	16	HRCNFG	5004 C040h	5004 D040h	5004 E040h
4Eh	16	HRCNFG2	5004 C04Eh	5004 D04Eh	5004 E04Eh
5Ah	16	HRPCTL	5004 C05Ah	5004 D05Ah	5004 E05Ah
5Ch	16	TRREM	5004 C05Ch	5004 D05Ch	5004 E05Ch
68h	16	GLDCTL	5004 C068h	5004 D068h	5004 E068h
6Ah	16	GLDCFG	5004 C06Ah	5004 D06Ah	5004 E06Ah
70h	32	EPWMXLINK	5004 C070h	5004 D070h	5004 E070h

Table 3-651. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM15_ G1 Physical Address	CONTROLSS_EPWM16_ G1 Physical Address	CONTROLSS_EPWM17_ G1 Physical Address
0h	16	TBCTL	5004 F000h	5005 0000h	5005 1000h
2h	16	TBCTL2	5004 F002h	5005 0002h	5005 1002h
6h	16	EPWMSYNCINSEL	5004 F006h	5005 0006h	5005 1006h
8h	16	TBCTR	5004 F008h	5005 0008h	5005 1008h
Ah	16	TBSTS	5004 F00Ah	5005 000Ah	5005 100Ah
Ch	16	EPWMSYNCOUTEN	5004 F00Ch	5005 000Ch	5005 100Ch
Eh	16	TBCTL3	5004 F00Eh	5005 000Eh	5005 100Eh
10h	16	CMPCTL	5004 F010h	5005 0010h	5005 1010h
12h	16	CMPCTL2	5004 F012h	5005 0012h	5005 1012h
18h	16	DBCTL	5004 F018h	5005 0018h	5005 1018h
1Ah	16	DBCTL2	5004 F01Ah	5005 001Ah	5005 101Ah
20h	16	AQCTL	5004 F020h	5005 0020h	5005 1020h
22h	16	AQTSRCSEL	5004 F022h	5005 0022h	5005 1022h
28h	16	PCCTL	5004 F028h	5005 0028h	5005 1028h

Table 3-651. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_EPWM15_ G1 Physical Address	CONTROLSS_EPWM16_ G1 Physical Address	CONTROLSS_EPWM17_ G1 Physical Address
30h	16	VCAPCTL	5004 F030h	5005 0030h	5005 1030h
32h	16	VCNTCFG	5004 F032h	5005 0032h	5005 1032h
40h	16	HRCNFG	5004 F040h	5005 0040h	5005 1040h
4Eh	16	HRCNFG2	5004 F04Eh	5005 004Eh	5005 104Eh
5Ah	16	HRPCTL	5004 F05Ah	5005 005Ah	5005 105Ah
5Ch	16	TRREM	5004 F05Ch	5005 005Ch	5005 105Ch
68h	16	GLDCTL	5004 F068h	5005 0068h	5005 1068h
6Ah	16	GLDCFG	5004 F06Ah	5005 006Ah	5005 106Ah
70h	32	EPWMXLINK	5004 F070h	5005 0070h	5005 1070h

Table 3-652. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM18_ G1 Physical Address	CONTROLSS_EPWM19_ G1 Physical Address	CONTROLSS_EPWM2_ G1 Physical Address
0h	16	TBCTL	5005 2000h	5005 3000h	5004 2000h
2h	16	TBCTL2	5005 2002h	5005 3002h	5004 2002h
6h	16	EPWMSYNCINSEL	5005 2006h	5005 3006h	5004 2006h
8h	16	TBCTR	5005 2008h	5005 3008h	5004 2008h
Ah	16	TBSTS	5005 200Ah	5005 300Ah	5004 200Ah
Ch	16	EPWMSYNCOUTEN	5005 200Ch	5005 300Ch	5004 200Ch
Eh	16	TBCTL3	5005 200Eh	5005 300Eh	5004 200Eh
10h	16	CMPCTL	5005 2010h	5005 3010h	5004 2010h
12h	16	CMPCTL2	5005 2012h	5005 3012h	5004 2012h
18h	16	DBCTL	5005 2018h	5005 3018h	5004 2018h
1Ah	16	DBCTL2	5005 201Ah	5005 301Ah	5004 201Ah
20h	16	AQCTL	5005 2020h	5005 3020h	5004 2020h
22h	16	AQTSRCSEL	5005 2022h	5005 3022h	5004 2022h
28h	16	PCCTL	5005 2028h	5005 3028h	5004 2028h
30h	16	VCAPCTL	5005 2030h	5005 3030h	5004 2030h
32h	16	VCNTCFG	5005 2032h	5005 3032h	5004 2032h
40h	16	HRCNFG	5005 2040h	5005 3040h	5004 2040h
4Eh	16	HRCNFG2	5005 204Eh	5005 304Eh	5004 204Eh
5Ah	16	HRPCTL	5005 205Ah	5005 305Ah	5004 205Ah
5Ch	16	TRREM	5005 205Ch	5005 305Ch	5004 205Ch
68h	16	GLDCTL	5005 2068h	5005 3068h	5004 2068h
6Ah	16	GLDCFG	5005 206Ah	5005 306Ah	5004 206Ah
70h	32	EPWMXLINK	5005 2070h	5005 3070h	5004 2070h

Table 3-653. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM20_ G1 Physical Address	CONTROLSS_EPWM21_ G1 Physical Address	CONTROLSS_EPWM22_ G1 Physical Address
0h	16	TBCTL	5005 4000h	5005 5000h	5005 6000h
2h	16	TBCTL2	5005 4002h	5005 5002h	5005 6002h
6h	16	EPWMSYNCINSEL	5005 4006h	5005 5006h	5005 6006h
8h	16	TBCTR	5005 4008h	5005 5008h	5005 6008h
Ah	16	TBSTS	5005 400Ah	5005 500Ah	5005 600Ah
Ch	16	EPWMSYNCOUTEN	5005 400Ch	5005 500Ch	5005 600Ch

Table 3-653. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_EPWM20_ G1 Physical Address	CONTROLSS_EPWM21_ G1 Physical Address	CONTROLSS_EPWM22_ G1 Physical Address
Eh	16	TBCTL3	5005 400Eh	5005 500Eh	5005 600Eh
10h	16	CMPCTL	5005 4010h	5005 5010h	5005 6010h
12h	16	CMPCTL2	5005 4012h	5005 5012h	5005 6012h
18h	16	DBCTL	5005 4018h	5005 5018h	5005 6018h
1Ah	16	DBCTL2	5005 401Ah	5005 501Ah	5005 601Ah
20h	16	AQCTL	5005 4020h	5005 5020h	5005 6020h
22h	16	AQTSRCSEL	5005 4022h	5005 5022h	5005 6022h
28h	16	PCCTL	5005 4028h	5005 5028h	5005 6028h
30h	16	VCAPCTL	5005 4030h	5005 5030h	5005 6030h
32h	16	VCNTCFG	5005 4032h	5005 5032h	5005 6032h
40h	16	HRCNFG	5005 4040h	5005 5040h	5005 6040h
4Eh	16	HRCNFG2	5005 404Eh	5005 504Eh	5005 604Eh
5Ah	16	HRPCTL	5005 405Ah	5005 505Ah	5005 605Ah
5Ch	16	TRREM	5005 405Ch	5005 505Ch	5005 605Ch
68h	16	GLDCTL	5005 4068h	5005 5068h	5005 6068h
6Ah	16	GLDCFG	5005 406Ah	5005 506Ah	5005 606Ah
70h	32	EPWMXLINK	5005 4070h	5005 5070h	5005 6070h

Table 3-654. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM23_ G1 Physical Address	CONTROLSS_EPWM24_ G1 Physical Address	CONTROLSS_EPWM25_ G1 Physical Address
0h	16	TBCTL	5005 7000h	5005 8000h	5005 9000h
2h	16	TBCTL2	5005 7002h	5005 8002h	5005 9002h
6h	16	EPWMSYNCINSEL	5005 7006h	5005 8006h	5005 9006h
8h	16	TBCTR	5005 7008h	5005 8008h	5005 9008h
Ah	16	TBSTS	5005 700Ah	5005 800Ah	5005 900Ah
Ch	16	EPWMSYNCOUTEN	5005 700Ch	5005 800Ch	5005 900Ch
Eh	16	TBCTL3	5005 700Eh	5005 800Eh	5005 900Eh
10h	16	CMPCTL	5005 7010h	5005 8010h	5005 9010h
12h	16	CMPCTL2	5005 7012h	5005 8012h	5005 9012h
18h	16	DBCTL	5005 7018h	5005 8018h	5005 9018h
1Ah	16	DBCTL2	5005 701Ah	5005 801Ah	5005 901Ah
20h	16	AQCTL	5005 7020h	5005 8020h	5005 9020h
22h	16	AQTSRCSEL	5005 7022h	5005 8022h	5005 9022h
28h	16	PCCTL	5005 7028h	5005 8028h	5005 9028h
30h	16	VCAPCTL	5005 7030h	5005 8030h	5005 9030h
32h	16	VCNTCFG	5005 7032h	5005 8032h	5005 9032h
40h	16	HRCNFG	5005 7040h	5005 8040h	5005 9040h
4Eh	16	HRCNFG2	5005 704Eh	5005 804Eh	5005 904Eh
5Ah	16	HRPCTL	5005 705Ah	5005 805Ah	5005 905Ah
5Ch	16	TRREM	5005 705Ch	5005 805Ch	5005 905Ch
68h	16	GLDCTL	5005 7068h	5005 8068h	5005 9068h
6Ah	16	GLDCFG	5005 706Ah	5005 806Ah	5005 906Ah
70h	32	EPWMXLINK	5005 7070h	5005 8070h	5005 9070h

Table 3-655. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM26_ G1 Physical Address	CONTROLSS_EPWM27_ G1 Physical Address	CONTROLSS_EPWM28_ G1 Physical Address
0h	16	TBCTL	5005 A000h	5005 B000h	5005 C000h
2h	16	TBCTL2	5005 A002h	5005 B002h	5005 C002h
6h	16	EPWMSYNCINSEL	5005 A006h	5005 B006h	5005 C006h
8h	16	TBCTR	5005 A008h	5005 B008h	5005 C008h
Ah	16	TBSTS	5005 A00Ah	5005 B00Ah	5005 C00Ah
Ch	16	EPWMSYNCOUTEN	5005 A00Ch	5005 B00Ch	5005 C00Ch
Eh	16	TBCTL3	5005 A00Eh	5005 B00Eh	5005 C00Eh
10h	16	CMPCTL	5005 A010h	5005 B010h	5005 C010h
12h	16	CMPCTL2	5005 A012h	5005 B012h	5005 C012h
18h	16	DBCTL	5005 A018h	5005 B018h	5005 C018h
1Ah	16	DBCTL2	5005 A01Ah	5005 B01Ah	5005 C01Ah
20h	16	AQCTL	5005 A020h	5005 B020h	5005 C020h
22h	16	AQTSRCSEL	5005 A022h	5005 B022h	5005 C022h
28h	16	PCCTL	5005 A028h	5005 B028h	5005 C028h
30h	16	VCAPCTL	5005 A030h	5005 B030h	5005 C030h
32h	16	VCNTCFG	5005 A032h	5005 B032h	5005 C032h
40h	16	HRCNFG	5005 A040h	5005 B040h	5005 C040h
4Eh	16	HRCNFG2	5005 A04Eh	5005 B04Eh	5005 C04Eh
5Ah	16	HRPCTL	5005 A05Ah	5005 B05Ah	5005 C05Ah
5Ch	16	TRREM	5005 A05Ch	5005 B05Ch	5005 C05Ch
68h	16	GLDCTL	5005 A068h	5005 B068h	5005 C068h
6Ah	16	GLDCFG	5005 A06Ah	5005 B06Ah	5005 C06Ah
70h	32	EPWMXLINK	5005 A070h	5005 B070h	5005 C070h

Table 3-656. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM29_ G1 Physical Address	CONTROLSS_EPWM3_ G1 Physical Address	CONTROLSS_EPWM30_ G1 Physical Address
0h	16	TBCTL	5005 D000h	5004 3000h	5005 E000h
2h	16	TBCTL2	5005 D002h	5004 3002h	5005 E002h
6h	16	EPWMSYNCINSEL	5005 D006h	5004 3006h	5005 E006h
8h	16	TBCTR	5005 D008h	5004 3008h	5005 E008h
Ah	16	TBSTS	5005 D00Ah	5004 300Ah	5005 E00Ah
Ch	16	EPWMSYNCOUTEN	5005 D00Ch	5004 300Ch	5005 E00Ch
Eh	16	TBCTL3	5005 D00Eh	5004 300Eh	5005 E00Eh
10h	16	CMPCTL	5005 D010h	5004 3010h	5005 E010h
12h	16	CMPCTL2	5005 D012h	5004 3012h	5005 E012h
18h	16	DBCTL	5005 D018h	5004 3018h	5005 E018h
1Ah	16	DBCTL2	5005 D01Ah	5004 301Ah	5005 E01Ah
20h	16	AQCTL	5005 D020h	5004 3020h	5005 E020h
22h	16	AQTSRCSEL	5005 D022h	5004 3022h	5005 E022h
28h	16	PCCTL	5005 D028h	5004 3028h	5005 E028h
30h	16	VCAPCTL	5005 D030h	5004 3030h	5005 E030h
32h	16	VCNTCFG	5005 D032h	5004 3032h	5005 E032h
40h	16	HRCNFG	5005 D040h	5004 3040h	5005 E040h
4Eh	16	HRCNFG2	5005 D04Eh	5004 304Eh	5005 E04Eh
5Ah	16	HRPCTL	5005 D05Ah	5004 305Ah	5005 E05Ah

Table 3-656. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_EPWM29_ G1 Physical Address	CONTROLSS_EPWM3_ G1 Physical Address	CONTROLSS_EPWM30_ G1 Physical Address
5Ch	16	TRREM	5005 D05Ch	5004 305Ch	5005 E05Ch
68h	16	GLDCTL	5005 D068h	5004 3068h	5005 E068h
6Ah	16	GLDCFG	5005 D06Ah	5004 306Ah	5005 E06Ah
70h	32	EPWMXLINK	5005 D070h	5004 3070h	5005 E070h

Table 3-657. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM31_ G1 Physical Address	CONTROLSS_EPWM4_ G1 Physical Address	CONTROLSS_EPWM5_ G1 Physical Address
0h	16	TBCTL	5005 F000h	5004 4000h	5004 5000h
2h	16	TBCTL2	5005 F002h	5004 4002h	5004 5002h
6h	16	EPWMSYNCINSEL	5005 F006h	5004 4006h	5004 5006h
8h	16	TBCTR	5005 F008h	5004 4008h	5004 5008h
Ah	16	TBSTS	5005 F00Ah	5004 400Ah	5004 500Ah
Ch	16	EPWMSYNCOUTEN	5005 F00Ch	5004 400Ch	5004 500Ch
Eh	16	TBCTL3	5005 F00Eh	5004 400Eh	5004 500Eh
10h	16	CMPCTL	5005 F010h	5004 4010h	5004 5010h
12h	16	CMPCTL2	5005 F012h	5004 4012h	5004 5012h
18h	16	DBCTL	5005 F018h	5004 4018h	5004 5018h
1Ah	16	DBCTL2	5005 F01Ah	5004 401Ah	5004 501Ah
20h	16	AQCTL	5005 F020h	5004 4020h	5004 5020h
22h	16	AQTSRCSEL	5005 F022h	5004 4022h	5004 5022h
28h	16	PCCTL	5005 F028h	5004 4028h	5004 5028h
30h	16	VCAPCTL	5005 F030h	5004 4030h	5004 5030h
32h	16	VCNTCFG	5005 F032h	5004 4032h	5004 5032h
40h	16	HRCNFG	5005 F040h	5004 4040h	5004 5040h
4Eh	16	HRCNFG2	5005 F04Eh	5004 404Eh	5004 504Eh
5Ah	16	HRPCTL	5005 F05Ah	5004 405Ah	5004 505Ah
5Ch	16	TRREM	5005 F05Ch	5004 405Ch	5004 505Ch
68h	16	GLDCTL	5005 F068h	5004 4068h	5004 5068h
6Ah	16	GLDCFG	5005 F06Ah	5004 406Ah	5004 506Ah
70h	32	EPWMXLINK	5005 F070h	5004 4070h	5004 5070h

Table 3-658. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM6_ G1 Physical Address	CONTROLSS_EPWM7_ G1 Physical Address	CONTROLSS_EPWM8_ G1 Physical Address
0h	16	TBCTL	5004 6000h	5004 7000h	5004 8000h
2h	16	TBCTL2	5004 6002h	5004 7002h	5004 8002h
6h	16	EPWMSYNCINSEL	5004 6006h	5004 7006h	5004 8006h
8h	16	TBCTR	5004 6008h	5004 7008h	5004 8008h
Ah	16	TBSTS	5004 600Ah	5004 700Ah	5004 800Ah
Ch	16	EPWMSYNCOUTEN	5004 600Ch	5004 700Ch	5004 800Ch
Eh	16	TBCTL3	5004 600Eh	5004 700Eh	5004 800Eh
10h	16	CMPCTL	5004 6010h	5004 7010h	5004 8010h
12h	16	CMPCTL2	5004 6012h	5004 7012h	5004 8012h
18h	16	DBCTL	5004 6018h	5004 7018h	5004 8018h
1Ah	16	DBCTL2	5004 601Ah	5004 701Ah	5004 801Ah

Table 3-658. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_EPWM6_ G1 Physical Address	CONTROLSS_EPWM7_ G1 Physical Address	CONTROLSS_EPWM8_ G1 Physical Address
20h	16	AQCTL	5004 6020h	5004 7020h	5004 8020h
22h	16	AQTSRCSEL	5004 6022h	5004 7022h	5004 8022h
28h	16	PCCTL	5004 6028h	5004 7028h	5004 8028h
30h	16	VCAPCTL	5004 6030h	5004 7030h	5004 8030h
32h	16	VCNTCFG	5004 6032h	5004 7032h	5004 8032h
40h	16	HRCNFG	5004 6040h	5004 7040h	5004 8040h
4Eh	16	HRCNFG2	5004 604Eh	5004 704Eh	5004 804Eh
5Ah	16	HRPCTL	5004 605Ah	5004 705Ah	5004 805Ah
5Ch	16	TRREM	5004 605Ch	5004 705Ch	5004 805Ch
68h	16	GLDCTL	5004 6068h	5004 7068h	5004 8068h
6Ah	16	GLDCFG	5004 606Ah	5004 706Ah	5004 806Ah
70h	32	EPWMXLINK	5004 6070h	5004 7070h	5004 8070h

Table 3-659. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM9_ G1 Physical Address	CONTROLSS_EPWM0_ G2 Physical Address	CONTROLSS_EPWM1_ G2 Physical Address
0h	16	TBCTL	5004 9000h	5008 0000h	5008 1000h
2h	16	TBCTL2	5004 9002h	5008 0002h	5008 1002h
6h	16	EPWMSYNCINSEL	5004 9006h	5008 0006h	5008 1006h
8h	16	TBCTR	5004 9008h	5008 0008h	5008 1008h
Ah	16	TBSTS	5004 900Ah	5008 000Ah	5008 100Ah
Ch	16	EPWMSYNCOUTEN	5004 900Ch	5008 000Ch	5008 100Ch
Eh	16	TBCTL3	5004 900Eh	5008 000Eh	5008 100Eh
10h	16	CMPCTL	5004 9010h	5008 0010h	5008 1010h
12h	16	CMPCTL2	5004 9012h	5008 0012h	5008 1012h
18h	16	DBCTL	5004 9018h	5008 0018h	5008 1018h
1Ah	16	DBCTL2	5004 901Ah	5008 001Ah	5008 101Ah
20h	16	AQCTL	5004 9020h	5008 0020h	5008 1020h
22h	16	AQTSRCSEL	5004 9022h	5008 0022h	5008 1022h
28h	16	PCCTL	5004 9028h	5008 0028h	5008 1028h
30h	16	VCAPCTL	5004 9030h	5008 0030h	5008 1030h
32h	16	VCNTCFG	5004 9032h	5008 0032h	5008 1032h
40h	16	HRCNFG	5004 9040h	5008 0040h	5008 1040h
4Eh	16	HRCNFG2	5004 904Eh	5008 004Eh	5008 104Eh
5Ah	16	HRPCTL	5004 905Ah	5008 005Ah	5008 105Ah
5Ch	16	TRREM	5004 905Ch	5008 005Ch	5008 105Ch
68h	16	GLDCTL	5004 9068h	5008 0068h	5008 1068h
6Ah	16	GLDCFG	5004 906Ah	5008 006Ah	5008 106Ah
70h	32	EPWMXLINK	5004 9070h	5008 0070h	5008 1070h

Table 3-660. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM10_ G2 Physical Address	CONTROLSS_EPWM11_ G2 Physical Address	CONTROLSS_EPWM12_ G2 Physical Address
0h	16	TBCTL	5008 A000h	5008 B000h	5008 C000h
2h	16	TBCTL2	5008 A002h	5008 B002h	5008 C002h
6h	16	EPWMSYNCINSEL	5008 A006h	5008 B006h	5008 C006h

Table 3-660. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_EPWM10_ G2 Physical Address	CONTROLSS_EPWM11_ G2 Physical Address	CONTROLSS_EPWM12_ G2 Physical Address
8h	16	TBCTR	5008 A008h	5008 B008h	5008 C008h
Ah	16	TBSTS	5008 A00Ah	5008 B00Ah	5008 C00Ah
Ch	16	EPWMSYNCOUTEN	5008 A00Ch	5008 B00Ch	5008 C00Ch
Eh	16	TBCTL3	5008 A00Eh	5008 B00Eh	5008 C00Eh
10h	16	CMPCTL	5008 A010h	5008 B010h	5008 C010h
12h	16	CMPCTL2	5008 A012h	5008 B012h	5008 C012h
18h	16	DBCTL	5008 A018h	5008 B018h	5008 C018h
1Ah	16	DBCTL2	5008 A01Ah	5008 B01Ah	5008 C01Ah
20h	16	AQCTL	5008 A020h	5008 B020h	5008 C020h
22h	16	AQTSRCSEL	5008 A022h	5008 B022h	5008 C022h
28h	16	PCCTL	5008 A028h	5008 B028h	5008 C028h
30h	16	VCAPCTL	5008 A030h	5008 B030h	5008 C030h
32h	16	VCNTCFG	5008 A032h	5008 B032h	5008 C032h
40h	16	HRCNFG	5008 A040h	5008 B040h	5008 C040h
4Eh	16	HRCNFG2	5008 A04Eh	5008 B04Eh	5008 C04Eh
5Ah	16	HRPCTL	5008 A05Ah	5008 B05Ah	5008 C05Ah
5Ch	16	TRREM	5008 A05Ch	5008 B05Ch	5008 C05Ch
68h	16	GLDCTL	5008 A068h	5008 B068h	5008 C068h
6Ah	16	GLDCFG	5008 A06Ah	5008 B06Ah	5008 C06Ah
70h	32	EPWMXLINK	5008 A070h	5008 B070h	5008 C070h

Table 3-661. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM13_ G2 Physical Address	CONTROLSS_EPWM14_ G2 Physical Address	CONTROLSS_EPWM15_ G2 Physical Address
0h	16	TBCTL	5008 D000h	5008 E000h	5008 F000h
2h	16	TBCTL2	5008 D002h	5008 E002h	5008 F002h
6h	16	EPWMSYNCINSEL	5008 D006h	5008 E006h	5008 F006h
8h	16	TBCTR	5008 D008h	5008 E008h	5008 F008h
Ah	16	TBSTS	5008 D00Ah	5008 E00Ah	5008 F00Ah
Ch	16	EPWMSYNCOUTEN	5008 D00Ch	5008 E00Ch	5008 F00Ch
Eh	16	TBCTL3	5008 D00Eh	5008 E00Eh	5008 F00Eh
10h	16	CMPCTL	5008 D010h	5008 E010h	5008 F010h
12h	16	CMPCTL2	5008 D012h	5008 E012h	5008 F012h
18h	16	DBCTL	5008 D018h	5008 E018h	5008 F018h
1Ah	16	DBCTL2	5008 D01Ah	5008 E01Ah	5008 F01Ah
20h	16	AQCTL	5008 D020h	5008 E020h	5008 F020h
22h	16	AQTSRCSEL	5008 D022h	5008 E022h	5008 F022h
28h	16	PCCTL	5008 D028h	5008 E028h	5008 F028h
30h	16	VCAPCTL	5008 D030h	5008 E030h	5008 F030h
32h	16	VCNTCFG	5008 D032h	5008 E032h	5008 F032h
40h	16	HRCNFG	5008 D040h	5008 E040h	5008 F040h
4Eh	16	HRCNFG2	5008 D04Eh	5008 E04Eh	5008 F04Eh
5Ah	16	HRPCTL	5008 D05Ah	5008 E05Ah	5008 F05Ah
5Ch	16	TRREM	5008 D05Ch	5008 E05Ch	5008 F05Ch
68h	16	GLDCTL	5008 D068h	5008 E068h	5008 F068h
6Ah	16	GLDCFG	5008 D06Ah	5008 E06Ah	5008 F06Ah

Table 3-661. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_EPWM13_ G2 Physical Address	CONTROLSS_EPWM14_ G2 Physical Address	CONTROLSS_EPWM15_ G2 Physical Address
70h	32	EPWMXLINK	5008 D070h	5008 E070h	5008 F070h

Table 3-662. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM16_ G2 Physical Address	CONTROLSS_EPWM17_ G2 Physical Address	CONTROLSS_EPWM18_ G2 Physical Address
0h	16	TBCTL	5009 0000h	5009 1000h	5009 2000h
2h	16	TBCTL2	5009 0002h	5009 1002h	5009 2002h
6h	16	EPWMSYNCINSEL	5009 0006h	5009 1006h	5009 2006h
8h	16	TBCTR	5009 0008h	5009 1008h	5009 2008h
Ah	16	TBSTS	5009 000Ah	5009 100Ah	5009 200Ah
Ch	16	EPWMSYNCOUTEN	5009 000Ch	5009 100Ch	5009 200Ch
Eh	16	TBCTL3	5009 000Eh	5009 100Eh	5009 200Eh
10h	16	CMPCTL	5009 0010h	5009 1010h	5009 2010h
12h	16	CMPCTL2	5009 0012h	5009 1012h	5009 2012h
18h	16	DBCTL	5009 0018h	5009 1018h	5009 2018h
1Ah	16	DBCTL2	5009 001Ah	5009 101Ah	5009 201Ah
20h	16	AQCTL	5009 0020h	5009 1020h	5009 2020h
22h	16	AQTSRCSEL	5009 0022h	5009 1022h	5009 2022h
28h	16	PCCTL	5009 0028h	5009 1028h	5009 2028h
30h	16	VCAPCTL	5009 0030h	5009 1030h	5009 2030h
32h	16	VCNTCFG	5009 0032h	5009 1032h	5009 2032h
40h	16	HRCNFG	5009 0040h	5009 1040h	5009 2040h
4Eh	16	HRCNFG2	5009 004Eh	5009 104Eh	5009 204Eh
5Ah	16	HRPCTL	5009 005Ah	5009 105Ah	5009 205Ah
5Ch	16	TRREM	5009 005Ch	5009 105Ch	5009 205Ch
68h	16	GLDCTL	5009 0068h	5009 1068h	5009 2068h
6Ah	16	GLDCFG	5009 006Ah	5009 106Ah	5009 206Ah
70h	32	EPWMXLINK	5009 0070h	5009 1070h	5009 2070h

Table 3-663. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM19_ G2 Physical Address	CONTROLSS_EPWM2_ G2 Physical Address	CONTROLSS_EPWM20_ G2 Physical Address
0h	16	TBCTL	5009 3000h	5008 2000h	5009 4000h
2h	16	TBCTL2	5009 3002h	5008 2002h	5009 4002h
6h	16	EPWMSYNCINSEL	5009 3006h	5008 2006h	5009 4006h
8h	16	TBCTR	5009 3008h	5008 2008h	5009 4008h
Ah	16	TBSTS	5009 300Ah	5008 200Ah	5009 400Ah
Ch	16	EPWMSYNCOUTEN	5009 300Ch	5008 200Ch	5009 400Ch
Eh	16	TBCTL3	5009 300Eh	5008 200Eh	5009 400Eh
10h	16	CMPCTL	5009 3010h	5008 2010h	5009 4010h
12h	16	CMPCTL2	5009 3012h	5008 2012h	5009 4012h
18h	16	DBCTL	5009 3018h	5008 2018h	5009 4018h
1Ah	16	DBCTL2	5009 301Ah	5008 201Ah	5009 401Ah
20h	16	AQCTL	5009 3020h	5008 2020h	5009 4020h
22h	16	AQTSRCSEL	5009 3022h	5008 2022h	5009 4022h
28h	16	PCCTL	5009 3028h	5008 2028h	5009 4028h

Table 3-663. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_EPWM19_ G2 Physical Address	CONTROLSS_EPWM2_ G2 Physical Address	CONTROLSS_EPWM20_ G2 Physical Address
30h	16	VCAPCTL	5009 3030h	5008 2030h	5009 4030h
32h	16	VCNTCFG	5009 3032h	5008 2032h	5009 4032h
40h	16	HRCNFG	5009 3040h	5008 2040h	5009 4040h
4Eh	16	HRCNFG2	5009 304Eh	5008 204Eh	5009 404Eh
5Ah	16	HRPCTL	5009 305Ah	5008 205Ah	5009 405Ah
5Ch	16	TRREM	5009 305Ch	5008 205Ch	5009 405Ch
68h	16	GLDCTL	5009 3068h	5008 2068h	5009 4068h
6Ah	16	GLDCFG	5009 306Ah	5008 206Ah	5009 406Ah
70h	32	EPWMXLINK	5009 3070h	5008 2070h	5009 4070h

Table 3-664. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM21_ G2 Physical Address	CONTROLSS_EPWM22_ G2 Physical Address	CONTROLSS_EPWM23_ G2 Physical Address
0h	16	TBCTL	5009 5000h	5009 6000h	5009 7000h
2h	16	TBCTL2	5009 5002h	5009 6002h	5009 7002h
6h	16	EPWMSYNCINSEL	5009 5006h	5009 6006h	5009 7006h
8h	16	TBCTR	5009 5008h	5009 6008h	5009 7008h
Ah	16	TBSTS	5009 500Ah	5009 600Ah	5009 700Ah
Ch	16	EPWMSYNCOUTEN	5009 500Ch	5009 600Ch	5009 700Ch
Eh	16	TBCTL3	5009 500Eh	5009 600Eh	5009 700Eh
10h	16	CMPCTL	5009 5010h	5009 6010h	5009 7010h
12h	16	CMPCTL2	5009 5012h	5009 6012h	5009 7012h
18h	16	DBCTL	5009 5018h	5009 6018h	5009 7018h
1Ah	16	DBCTL2	5009 501Ah	5009 601Ah	5009 701Ah
20h	16	AQCTL	5009 5020h	5009 6020h	5009 7020h
22h	16	AQTSRCSEL	5009 5022h	5009 6022h	5009 7022h
28h	16	PCCTL	5009 5028h	5009 6028h	5009 7028h
30h	16	VCAPCTL	5009 5030h	5009 6030h	5009 7030h
32h	16	VCNTCFG	5009 5032h	5009 6032h	5009 7032h
40h	16	HRCNFG	5009 5040h	5009 6040h	5009 7040h
4Eh	16	HRCNFG2	5009 504Eh	5009 604Eh	5009 704Eh
5Ah	16	HRPCTL	5009 505Ah	5009 605Ah	5009 705Ah
5Ch	16	TRREM	5009 505Ch	5009 605Ch	5009 705Ch
68h	16	GLDCTL	5009 5068h	5009 6068h	5009 7068h
6Ah	16	GLDCFG	5009 506Ah	5009 606Ah	5009 706Ah
70h	32	EPWMXLINK	5009 5070h	5009 6070h	5009 7070h

Table 3-665. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM24_ G2 Physical Address	CONTROLSS_EPWM25_ G2 Physical Address	CONTROLSS_EPWM26_ G2 Physical Address
0h	16	TBCTL	5009 8000h	5009 9000h	5009 A000h
2h	16	TBCTL2	5009 8002h	5009 9002h	5009 A002h
6h	16	EPWMSYNCINSEL	5009 8006h	5009 9006h	5009 A006h
8h	16	TBCTR	5009 8008h	5009 9008h	5009 A008h
Ah	16	TBSTS	5009 800Ah	5009 900Ah	5009 A00Ah
Ch	16	EPWMSYNCOUTEN	5009 800Ch	5009 900Ch	5009 A00Ch

Table 3-665. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_EPWM24_ G2 Physical Address	CONTROLSS_EPWM25_ G2 Physical Address	CONTROLSS_EPWM26_ G2 Physical Address
Eh	16	TBCTL3	5009 800Eh	5009 900Eh	5009 A00Eh
10h	16	CMPCTL	5009 8010h	5009 9010h	5009 A010h
12h	16	CMPCTL2	5009 8012h	5009 9012h	5009 A012h
18h	16	DBCTL	5009 8018h	5009 9018h	5009 A018h
1Ah	16	DBCTL2	5009 801Ah	5009 901Ah	5009 A01Ah
20h	16	AQCTL	5009 8020h	5009 9020h	5009 A020h
22h	16	AQTSRCSEL	5009 8022h	5009 9022h	5009 A022h
28h	16	PCCTL	5009 8028h	5009 9028h	5009 A028h
30h	16	VCAPCTL	5009 8030h	5009 9030h	5009 A030h
32h	16	VCNTCFG	5009 8032h	5009 9032h	5009 A032h
40h	16	HRCNFG	5009 8040h	5009 9040h	5009 A040h
4Eh	16	HRCNFG2	5009 804Eh	5009 904Eh	5009 A04Eh
5Ah	16	HRPCTL	5009 805Ah	5009 905Ah	5009 A05Ah
5Ch	16	TRREM	5009 805Ch	5009 905Ch	5009 A05Ch
68h	16	GLDCTL	5009 8068h	5009 9068h	5009 A068h
6Ah	16	GLDCFG	5009 806Ah	5009 906Ah	5009 A06Ah
70h	32	EPWMXLINK	5009 8070h	5009 9070h	5009 A070h

Table 3-666. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM27_ G2 Physical Address	CONTROLSS_EPWM28_ G2 Physical Address	CONTROLSS_EPWM29_ G2 Physical Address
0h	16	TBCTL	5009 B000h	5009 C000h	5009 D000h
2h	16	TBCTL2	5009 B002h	5009 C002h	5009 D002h
6h	16	EPWMSYNCINSEL	5009 B006h	5009 C006h	5009 D006h
8h	16	TBCTR	5009 B008h	5009 C008h	5009 D008h
Ah	16	TBSTS	5009 B00Ah	5009 C00Ah	5009 D00Ah
Ch	16	EPWMSYNCOUTEN	5009 B00Ch	5009 C00Ch	5009 D00Ch
Eh	16	TBCTL3	5009 B00Eh	5009 C00Eh	5009 D00Eh
10h	16	CMPCTL	5009 B010h	5009 C010h	5009 D010h
12h	16	CMPCTL2	5009 B012h	5009 C012h	5009 D012h
18h	16	DBCTL	5009 B018h	5009 C018h	5009 D018h
1Ah	16	DBCTL2	5009 B01Ah	5009 C01Ah	5009 D01Ah
20h	16	AQCTL	5009 B020h	5009 C020h	5009 D020h
22h	16	AQTSRCSEL	5009 B022h	5009 C022h	5009 D022h
28h	16	PCCTL	5009 B028h	5009 C028h	5009 D028h
30h	16	VCAPCTL	5009 B030h	5009 C030h	5009 D030h
32h	16	VCNTCFG	5009 B032h	5009 C032h	5009 D032h
40h	16	HRCNFG	5009 B040h	5009 C040h	5009 D040h
4Eh	16	HRCNFG2	5009 B04Eh	5009 C04Eh	5009 D04Eh
5Ah	16	HRPCTL	5009 B05Ah	5009 C05Ah	5009 D05Ah
5Ch	16	TRREM	5009 B05Ch	5009 C05Ch	5009 D05Ch
68h	16	GLDCTL	5009 B068h	5009 C068h	5009 D068h
6Ah	16	GLDCFG	5009 B06Ah	5009 C06Ah	5009 D06Ah
70h	32	EPWMXLINK	5009 B070h	5009 C070h	5009 D070h

Table 3-667. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM3_ G2 Physical Address	CONTROLSS_EPWM30_ G2 Physical Address	CONTROLSS_EPWM31_ G2 Physical Address
0h	16	TBCTL	5008 3000h	5009 E000h	5009 F000h
2h	16	TBCTL2	5008 3002h	5009 E002h	5009 F002h
6h	16	EPWMSYNCINSEL	5008 3006h	5009 E006h	5009 F006h
8h	16	TBCTR	5008 3008h	5009 E008h	5009 F008h
Ah	16	TBSTS	5008 300Ah	5009 E00Ah	5009 F00Ah
Ch	16	EPWMSYNCOUTEN	5008 300Ch	5009 E00Ch	5009 F00Ch
Eh	16	TBCTL3	5008 300Eh	5009 E00Eh	5009 F00Eh
10h	16	CMPCTL	5008 3010h	5009 E010h	5009 F010h
12h	16	CMPCTL2	5008 3012h	5009 E012h	5009 F012h
18h	16	DBCTL	5008 3018h	5009 E018h	5009 F018h
1Ah	16	DBCTL2	5008 301Ah	5009 E01Ah	5009 F01Ah
20h	16	AQCTL	5008 3020h	5009 E020h	5009 F020h
22h	16	AQTSRCSEL	5008 3022h	5009 E022h	5009 F022h
28h	16	PCCTL	5008 3028h	5009 E028h	5009 F028h
30h	16	VCAPCTL	5008 3030h	5009 E030h	5009 F030h
32h	16	VCNTCFG	5008 3032h	5009 E032h	5009 F032h
40h	16	HRCNFG	5008 3040h	5009 E040h	5009 F040h
4Eh	16	HRCNFG2	5008 304Eh	5009 E04Eh	5009 F04Eh
5Ah	16	HRPCTL	5008 305Ah	5009 E05Ah	5009 F05Ah
5Ch	16	TRREM	5008 305Ch	5009 E05Ch	5009 F05Ch
68h	16	GLDCTL	5008 3068h	5009 E068h	5009 F068h
6Ah	16	GLDCFG	5008 306Ah	5009 E06Ah	5009 F06Ah
70h	32	EPWMXLINK	5008 3070h	5009 E070h	5009 F070h

Table 3-668. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM4_ G2 Physical Address	CONTROLSS_EPWM5_ G2 Physical Address	CONTROLSS_EPWM6_ G2 Physical Address
0h	16	TBCTL	5008 4000h	5008 5000h	5008 6000h
2h	16	TBCTL2	5008 4002h	5008 5002h	5008 6002h
6h	16	EPWMSYNCINSEL	5008 4006h	5008 5006h	5008 6006h
8h	16	TBCTR	5008 4008h	5008 5008h	5008 6008h
Ah	16	TBSTS	5008 400Ah	5008 500Ah	5008 600Ah
Ch	16	EPWMSYNCOUTEN	5008 400Ch	5008 500Ch	5008 600Ch
Eh	16	TBCTL3	5008 400Eh	5008 500Eh	5008 600Eh
10h	16	CMPCTL	5008 4010h	5008 5010h	5008 6010h
12h	16	CMPCTL2	5008 4012h	5008 5012h	5008 6012h
18h	16	DBCTL	5008 4018h	5008 5018h	5008 6018h
1Ah	16	DBCTL2	5008 401Ah	5008 501Ah	5008 601Ah
20h	16	AQCTL	5008 4020h	5008 5020h	5008 6020h
22h	16	AQTSRCSEL	5008 4022h	5008 5022h	5008 6022h
28h	16	PCCTL	5008 4028h	5008 5028h	5008 6028h
30h	16	VCAPCTL	5008 4030h	5008 5030h	5008 6030h
32h	16	VCNTCFG	5008 4032h	5008 5032h	5008 6032h
40h	16	HRCNFG	5008 4040h	5008 5040h	5008 6040h
4Eh	16	HRCNFG2	5008 404Eh	5008 504Eh	5008 604Eh
5Ah	16	HRPCTL	5008 405Ah	5008 505Ah	5008 605Ah

Table 3-668. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_EPWM4_ G2 Physical Address	CONTROLSS_EPWM5_ G2 Physical Address	CONTROLSS_EPWM6_ G2 Physical Address
5Ch	16	TRREM	5008 405Ch	5008 505Ch	5008 605Ch
68h	16	GLDCTL	5008 4068h	5008 5068h	5008 6068h
6Ah	16	GLDCFG	5008 406Ah	5008 506Ah	5008 606Ah
70h	32	EPWMXLINK	5008 4070h	5008 5070h	5008 6070h

Table 3-669. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM7_ G2 Physical Address	CONTROLSS_EPWM8_ G2 Physical Address	CONTROLSS_EPWM9_ G2 Physical Address
0h	16	TBCTL	5008 7000h	5008 8000h	5008 9000h
2h	16	TBCTL2	5008 7002h	5008 8002h	5008 9002h
6h	16	EPWMSYNCINSEL	5008 7006h	5008 8006h	5008 9006h
8h	16	TBCTR	5008 7008h	5008 8008h	5008 9008h
Ah	16	TBSTS	5008 700Ah	5008 800Ah	5008 900Ah
Ch	16	EPWMSYNCOUTEN	5008 700Ch	5008 800Ch	5008 900Ch
Eh	16	TBCTL3	5008 700Eh	5008 800Eh	5008 900Eh
10h	16	CMPCTL	5008 7010h	5008 8010h	5008 9010h
12h	16	CMPCTL2	5008 7012h	5008 8012h	5008 9012h
18h	16	DBCTL	5008 7018h	5008 8018h	5008 9018h
1Ah	16	DBCTL2	5008 701Ah	5008 801Ah	5008 901Ah
20h	16	AQCTL	5008 7020h	5008 8020h	5008 9020h
22h	16	AQTSRCSEL	5008 7022h	5008 8022h	5008 9022h
28h	16	PCCTL	5008 7028h	5008 8028h	5008 9028h
30h	16	VCAPCTL	5008 7030h	5008 8030h	5008 9030h
32h	16	VCNTCFG	5008 7032h	5008 8032h	5008 9032h
40h	16	HRCNFG	5008 7040h	5008 8040h	5008 9040h
4Eh	16	HRCNFG2	5008 704Eh	5008 804Eh	5008 904Eh
5Ah	16	HRPCTL	5008 705Ah	5008 805Ah	5008 905Ah
5Ch	16	TRREM	5008 705Ch	5008 805Ch	5008 905Ch
68h	16	GLDCTL	5008 7068h	5008 8068h	5008 9068h
6Ah	16	GLDCFG	5008 706Ah	5008 806Ah	5008 906Ah
70h	32	EPWMXLINK	5008 7070h	5008 8070h	5008 9070h

Table 3-670. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM0_ G3 Physical Address	CONTROLSS_EPWM1_ G3 Physical Address	CONTROLSS_EPWM10_ G3 Physical Address
0h	16	TBCTL	500C 0000h	500C 1000h	500C A000h
2h	16	TBCTL2	500C 0002h	500C 1002h	500C A002h
6h	16	EPWMSYNCINSEL	500C 0006h	500C 1006h	500C A006h
8h	16	TBCTR	500C 0008h	500C 1008h	500C A008h
Ah	16	TBSTS	500C 000Ah	500C 100Ah	500C A00Ah
Ch	16	EPWMSYNCOUTEN	500C 000Ch	500C 100Ch	500C A00Ch
Eh	16	TBCTL3	500C 000Eh	500C 100Eh	500C A00Eh
10h	16	CMPCTL	500C 0010h	500C 1010h	500C A010h
12h	16	CMPCTL2	500C 0012h	500C 1012h	500C A012h
18h	16	DBCTL	500C 0018h	500C 1018h	500C A018h
1Ah	16	DBCTL2	500C 001Ah	500C 101Ah	500C A01Ah

Table 3-670. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_EPWM0_ G3 Physical Address	CONTROLSS_EPWM1_ G3 Physical Address	CONTROLSS_EPWM10_ G3 Physical Address
20h	16	AQCTL	500C 0020h	500C 1020h	500C A020h
22h	16	AQTSRCSEL	500C 0022h	500C 1022h	500C A022h
28h	16	PCCTL	500C 0028h	500C 1028h	500C A028h
30h	16	VCAPCTL	500C 0030h	500C 1030h	500C A030h
32h	16	VCNTCFG	500C 0032h	500C 1032h	500C A032h
40h	16	HRCNFG	500C 0040h	500C 1040h	500C A040h
4Eh	16	HRCNFG2	500C 004Eh	500C 104Eh	500C A04Eh
5Ah	16	HRPCTL	500C 005Ah	500C 105Ah	500C A05Ah
5Ch	16	TRREM	500C 005Ch	500C 105Ch	500C A05Ch
68h	16	GLDCTL	500C 0068h	500C 1068h	500C A068h
6Ah	16	GLDCFG	500C 006Ah	500C 106Ah	500C A06Ah
70h	32	EPWMXLINK	500C 0070h	500C 1070h	500C A070h

Table 3-671. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM11_ G3 Physical Address	CONTROLSS_EPWM12_ G3 Physical Address	CONTROLSS_EPWM13_ G3 Physical Address
0h	16	TBCTL	500C B000h	500C C000h	500C D000h
2h	16	TBCTL2	500C B002h	500C C002h	500C D002h
6h	16	EPWMSYNCINSEL	500C B006h	500C C006h	500C D006h
8h	16	TBCTR	500C B008h	500C C008h	500C D008h
Ah	16	TBSTS	500C B00Ah	500C C00Ah	500C D00Ah
Ch	16	EPWMSYNCOUTEN	500C B00Ch	500C C00Ch	500C D00Ch
Eh	16	TBCTL3	500C B00Eh	500C C00Eh	500C D00Eh
10h	16	CMPCTL	500C B010h	500C C010h	500C D010h
12h	16	CMPCTL2	500C B012h	500C C012h	500C D012h
18h	16	DBCTL	500C B018h	500C C018h	500C D018h
1Ah	16	DBCTL2	500C B01Ah	500C C01Ah	500C D01Ah
20h	16	AQCTL	500C B020h	500C C020h	500C D020h
22h	16	AQTSRCSEL	500C B022h	500C C022h	500C D022h
28h	16	PCCTL	500C B028h	500C C028h	500C D028h
30h	16	VCAPCTL	500C B030h	500C C030h	500C D030h
32h	16	VCNTCFG	500C B032h	500C C032h	500C D032h
40h	16	HRCNFG	500C B040h	500C C040h	500C D040h
4Eh	16	HRCNFG2	500C B04Eh	500C C04Eh	500C D04Eh
5Ah	16	HRPCTL	500C B05Ah	500C C05Ah	500C D05Ah
5Ch	16	TRREM	500C B05Ch	500C C05Ch	500C D05Ch
68h	16	GLDCTL	500C B068h	500C C068h	500C D068h
6Ah	16	GLDCFG	500C B06Ah	500C C06Ah	500C D06Ah
70h	32	EPWMXLINK	500C B070h	500C C070h	500C D070h

Table 3-672. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM14_ G3 Physical Address	CONTROLSS_EPWM15_ G3 Physical Address	CONTROLSS_EPWM16_ G3 Physical Address
0h	16	TBCTL	500C E000h	500C F000h	500D 0000h
2h	16	TBCTL2	500C E002h	500C F002h	500D 0002h
6h	16	EPWMSYNCINSEL	500C E006h	500C F006h	500D 0006h

Table 3-672. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_EPWM14_ G3 Physical Address	CONTROLSS_EPWM15_ G3 Physical Address	CONTROLSS_EPWM16_ G3 Physical Address
8h	16	TBCTR	500C E008h	500C F008h	500D 0008h
Ah	16	TBSTS	500C E00Ah	500C F00Ah	500D 000Ah
Ch	16	EPWMSYNCOUTEN	500C E00Ch	500C F00Ch	500D 000Ch
Eh	16	TBCTL3	500C E00Eh	500C F00Eh	500D 000Eh
10h	16	CMPCTL	500C E010h	500C F010h	500D 0010h
12h	16	CMPCTL2	500C E012h	500C F012h	500D 0012h
18h	16	DBCTL	500C E018h	500C F018h	500D 0018h
1Ah	16	DBCTL2	500C E01Ah	500C F01Ah	500D 001Ah
20h	16	AQCTL	500C E020h	500C F020h	500D 0020h
22h	16	AQTSRCSEL	500C E022h	500C F022h	500D 0022h
28h	16	PCCTL	500C E028h	500C F028h	500D 0028h
30h	16	VCAPCTL	500C E030h	500C F030h	500D 0030h
32h	16	VCNTCFG	500C E032h	500C F032h	500D 0032h
40h	16	HRCNFG	500C E040h	500C F040h	500D 0040h
4Eh	16	HRCNFG2	500C E04Eh	500C F04Eh	500D 004Eh
5Ah	16	HRPCTL	500C E05Ah	500C F05Ah	500D 005Ah
5Ch	16	TRREM	500C E05Ch	500C F05Ch	500D 005Ch
68h	16	GLDCTL	500C E068h	500C F068h	500D 0068h
6Ah	16	GLDCFG	500C E06Ah	500C F06Ah	500D 006Ah
70h	32	EPWMXLINK	500C E070h	500C F070h	500D 0070h

Table 3-673. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM17_ G3 Physical Address	CONTROLSS_EPWM18_ G3 Physical Address	CONTROLSS_EPWM19_ G3 Physical Address
0h	16	TBCTL	500D 1000h	500D 2000h	500D 3000h
2h	16	TBCTL2	500D 1002h	500D 2002h	500D 3002h
6h	16	EPWMSYNCINSEL	500D 1006h	500D 2006h	500D 3006h
8h	16	TBCTR	500D 1008h	500D 2008h	500D 3008h
Ah	16	TBSTS	500D 100Ah	500D 200Ah	500D 300Ah
Ch	16	EPWMSYNCOUTEN	500D 100Ch	500D 200Ch	500D 300Ch
Eh	16	TBCTL3	500D 100Eh	500D 200Eh	500D 300Eh
10h	16	CMPCTL	500D 1010h	500D 2010h	500D 3010h
12h	16	CMPCTL2	500D 1012h	500D 2012h	500D 3012h
18h	16	DBCTL	500D 1018h	500D 2018h	500D 3018h
1Ah	16	DBCTL2	500D 101Ah	500D 201Ah	500D 301Ah
20h	16	AQCTL	500D 1020h	500D 2020h	500D 3020h
22h	16	AQTSRCSEL	500D 1022h	500D 2022h	500D 3022h
28h	16	PCCTL	500D 1028h	500D 2028h	500D 3028h
30h	16	VCAPCTL	500D 1030h	500D 2030h	500D 3030h
32h	16	VCNTCFG	500D 1032h	500D 2032h	500D 3032h
40h	16	HRCNFG	500D 1040h	500D 2040h	500D 3040h
4Eh	16	HRCNFG2	500D 104Eh	500D 204Eh	500D 304Eh
5Ah	16	HRPCTL	500D 105Ah	500D 205Ah	500D 305Ah
5Ch	16	TRREM	500D 105Ch	500D 205Ch	500D 305Ch
68h	16	GLDCTL	500D 1068h	500D 2068h	500D 3068h
6Ah	16	GLDCFG	500D 106Ah	500D 206Ah	500D 306Ah

Table 3-673. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_EPWM17_ G3 Physical Address	CONTROLSS_EPWM18_ G3 Physical Address	CONTROLSS_EPWM19_ G3 Physical Address
70h	32	EPWMXLINK	500D 1070h	500D 2070h	500D 3070h

Table 3-674. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM2_ G3 Physical Address	CONTROLSS_EPWM20_ G3 Physical Address	CONTROLSS_EPWM21_ G3 Physical Address
0h	16	TBCTL	500C 2000h	500D 4000h	500D 5000h
2h	16	TBCTL2	500C 2002h	500D 4002h	500D 5002h
6h	16	EPWMSYNCINSEL	500C 2006h	500D 4006h	500D 5006h
8h	16	TBCTR	500C 2008h	500D 4008h	500D 5008h
Ah	16	TBSTS	500C 200Ah	500D 400Ah	500D 500Ah
Ch	16	EPWMSYNCOUTEN	500C 200Ch	500D 400Ch	500D 500Ch
Eh	16	TBCTL3	500C 200Eh	500D 400Eh	500D 500Eh
10h	16	CMPCTL	500C 2010h	500D 4010h	500D 5010h
12h	16	CMPCTL2	500C 2012h	500D 4012h	500D 5012h
18h	16	DBCTL	500C 2018h	500D 4018h	500D 5018h
1Ah	16	DBCTL2	500C 201Ah	500D 401Ah	500D 501Ah
20h	16	AQCTL	500C 2020h	500D 4020h	500D 5020h
22h	16	AQTSRCSEL	500C 2022h	500D 4022h	500D 5022h
28h	16	PCCTL	500C 2028h	500D 4028h	500D 5028h
30h	16	VCAPCTL	500C 2030h	500D 4030h	500D 5030h
32h	16	VCNTCFG	500C 2032h	500D 4032h	500D 5032h
40h	16	HRCNFG	500C 2040h	500D 4040h	500D 5040h
4Eh	16	HRCNFG2	500C 204Eh	500D 404Eh	500D 504Eh
5Ah	16	HRPCTL	500C 205Ah	500D 405Ah	500D 505Ah
5Ch	16	TRREM	500C 205Ch	500D 405Ch	500D 505Ch
68h	16	GLDCTL	500C 2068h	500D 4068h	500D 5068h
6Ah	16	GLDCFG	500C 206Ah	500D 406Ah	500D 506Ah
70h	32	EPWMXLINK	500C 2070h	500D 4070h	500D 5070h

Table 3-675. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM22_ G3 Physical Address	CONTROLSS_EPWM23_ G3 Physical Address	CONTROLSS_EPWM24_ G3 Physical Address
0h	16	TBCTL	500D 6000h	500D 7000h	500D 8000h
2h	16	TBCTL2	500D 6002h	500D 7002h	500D 8002h
6h	16	EPWMSYNCINSEL	500D 6006h	500D 7006h	500D 8006h
8h	16	TBCTR	500D 6008h	500D 7008h	500D 8008h
Ah	16	TBSTS	500D 600Ah	500D 700Ah	500D 800Ah
Ch	16	EPWMSYNCOUTEN	500D 600Ch	500D 700Ch	500D 800Ch
Eh	16	TBCTL3	500D 600Eh	500D 700Eh	500D 800Eh
10h	16	CMPCTL	500D 6010h	500D 7010h	500D 8010h
12h	16	CMPCTL2	500D 6012h	500D 7012h	500D 8012h
18h	16	DBCTL	500D 6018h	500D 7018h	500D 8018h
1Ah	16	DBCTL2	500D 601Ah	500D 701Ah	500D 801Ah
20h	16	AQCTL	500D 6020h	500D 7020h	500D 8020h
22h	16	AQTSRCSEL	500D 6022h	500D 7022h	500D 8022h
28h	16	PCCTL	500D 6028h	500D 7028h	500D 8028h

Table 3-675. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_EPWM22_ G3 Physical Address	CONTROLSS_EPWM23_ G3 Physical Address	CONTROLSS_EPWM24_ G3 Physical Address
30h	16	VCAPCTL	500D 6030h	500D 7030h	500D 8030h
32h	16	VCNTCFG	500D 6032h	500D 7032h	500D 8032h
40h	16	HRCNFG	500D 6040h	500D 7040h	500D 8040h
4Eh	16	HRCNFG2	500D 604Eh	500D 704Eh	500D 804Eh
5Ah	16	HRPCTL	500D 605Ah	500D 705Ah	500D 805Ah
5Ch	16	TRREM	500D 605Ch	500D 705Ch	500D 805Ch
68h	16	GLDCTL	500D 6068h	500D 7068h	500D 8068h
6Ah	16	GLDCFG	500D 606Ah	500D 706Ah	500D 806Ah
70h	32	EPWMXLINK	500D 6070h	500D 7070h	500D 8070h

Table 3-676. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM25_ G3 Physical Address	CONTROLSS_EPWM26_ G3 Physical Address	CONTROLSS_EPWM27_ G3 Physical Address
0h	16	TBCTL	500D 9000h	500D A000h	500D B000h
2h	16	TBCTL2	500D 9002h	500D A002h	500D B002h
6h	16	EPWMSYNCINSEL	500D 9006h	500D A006h	500D B006h
8h	16	TBCTR	500D 9008h	500D A008h	500D B008h
Ah	16	TBSTS	500D 900Ah	500D A00Ah	500D B00Ah
Ch	16	EPWMSYNCOUTEN	500D 900Ch	500D A00Ch	500D B00Ch
Eh	16	TBCTL3	500D 900Eh	500D A00Eh	500D B00Eh
10h	16	CMPCTL	500D 9010h	500D A010h	500D B010h
12h	16	CMPCTL2	500D 9012h	500D A012h	500D B012h
18h	16	DBCTL	500D 9018h	500D A018h	500D B018h
1Ah	16	DBCTL2	500D 901Ah	500D A01Ah	500D B01Ah
20h	16	AQCTL	500D 9020h	500D A020h	500D B020h
22h	16	AQTSRCSEL	500D 9022h	500D A022h	500D B022h
28h	16	PCCTL	500D 9028h	500D A028h	500D B028h
30h	16	VCAPCTL	500D 9030h	500D A030h	500D B030h
32h	16	VCNTCFG	500D 9032h	500D A032h	500D B032h
40h	16	HRCNFG	500D 9040h	500D A040h	500D B040h
4Eh	16	HRCNFG2	500D 904Eh	500D A04Eh	500D B04Eh
5Ah	16	HRPCTL	500D 905Ah	500D A05Ah	500D B05Ah
5Ch	16	TRREM	500D 905Ch	500D A05Ch	500D B05Ch
68h	16	GLDCTL	500D 9068h	500D A068h	500D B068h
6Ah	16	GLDCFG	500D 906Ah	500D A06Ah	500D B06Ah
70h	32	EPWMXLINK	500D 9070h	500D A070h	500D B070h

Table 3-677. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM28_ G3 Physical Address	CONTROLSS_EPWM29_ G3 Physical Address	CONTROLSS_EPWM3_ G3 Physical Address
0h	16	TBCTL	500D C000h	500D D000h	500C 3000h
2h	16	TBCTL2	500D C002h	500D D002h	500C 3002h
6h	16	EPWMSYNCINSEL	500D C006h	500D D006h	500C 3006h
8h	16	TBCTR	500D C008h	500D D008h	500C 3008h
Ah	16	TBSTS	500D C00Ah	500D D00Ah	500C 300Ah
Ch	16	EPWMSYNCOUTEN	500D C00Ch	500D D00Ch	500C 300Ch

Table 3-677. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_EPWM28_ G3 Physical Address	CONTROLSS_EPWM29_ G3 Physical Address	CONTROLSS_EPWM3_ G3 Physical Address
Eh	16	TBCTL3	500D C00Eh	500D D00Eh	500C 300Eh
10h	16	CMPCTL	500D C010h	500D D010h	500C 3010h
12h	16	CMPCTL2	500D C012h	500D D012h	500C 3012h
18h	16	DBCTL	500D C018h	500D D018h	500C 3018h
1Ah	16	DBCTL2	500D C01Ah	500D D01Ah	500C 301Ah
20h	16	AQCTL	500D C020h	500D D020h	500C 3020h
22h	16	AQTSRCSEL	500D C022h	500D D022h	500C 3022h
28h	16	PCCTL	500D C028h	500D D028h	500C 3028h
30h	16	VCAPCTL	500D C030h	500D D030h	500C 3030h
32h	16	VCNTCFG	500D C032h	500D D032h	500C 3032h
40h	16	HRCNFG	500D C040h	500D D040h	500C 3040h
4Eh	16	HRCNFG2	500D C04Eh	500D D04Eh	500C 304Eh
5Ah	16	HRPCTL	500D C05Ah	500D D05Ah	500C 305Ah
5Ch	16	TRREM	500D C05Ch	500D D05Ch	500C 305Ch
68h	16	GLDCTL	500D C068h	500D D068h	500C 3068h
6Ah	16	GLDCFG	500D C06Ah	500D D06Ah	500C 306Ah
70h	32	EPWMXLINK	500D C070h	500D D070h	500C 3070h

Table 3-678. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM30_ G3 Physical Address	CONTROLSS_EPWM31_ G3 Physical Address	CONTROLSS_EPWM4_ G3 Physical Address
0h	16	TBCTL	500D E000h	500D F000h	500C 4000h
2h	16	TBCTL2	500D E002h	500D F002h	500C 4002h
6h	16	EPWMSYNCINSEL	500D E006h	500D F006h	500C 4006h
8h	16	TBCTR	500D E008h	500D F008h	500C 4008h
Ah	16	TBSTS	500D E00Ah	500D F00Ah	500C 400Ah
Ch	16	EPWMSYNCOUTEN	500D E00Ch	500D F00Ch	500C 400Ch
Eh	16	TBCTL3	500D E00Eh	500D F00Eh	500C 400Eh
10h	16	CMPCTL	500D E010h	500D F010h	500C 4010h
12h	16	CMPCTL2	500D E012h	500D F012h	500C 4012h
18h	16	DBCTL	500D E018h	500D F018h	500C 4018h
1Ah	16	DBCTL2	500D E01Ah	500D F01Ah	500C 401Ah
20h	16	AQCTL	500D E020h	500D F020h	500C 4020h
22h	16	AQTSRCSEL	500D E022h	500D F022h	500C 4022h
28h	16	PCCTL	500D E028h	500D F028h	500C 4028h
30h	16	VCAPCTL	500D E030h	500D F030h	500C 4030h
32h	16	VCNTCFG	500D E032h	500D F032h	500C 4032h
40h	16	HRCNFG	500D E040h	500D F040h	500C 4040h
4Eh	16	HRCNFG2	500D E04Eh	500D F04Eh	500C 404Eh
5Ah	16	HRPCTL	500D E05Ah	500D F05Ah	500C 405Ah
5Ch	16	TRREM	500D E05Ch	500D F05Ch	500C 405Ch
68h	16	GLDCTL	500D E068h	500D F068h	500C 4068h
6Ah	16	GLDCFG	500D E06Ah	500D F06Ah	500C 406Ah
70h	32	EPWMXLINK	500D E070h	500D F070h	500C 4070h

Table 3-679. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM5_ G3 Physical Address	CONTROLSS_EPWM6_ G3 Physical Address	CONTROLSS_EPWM7_ G3 Physical Address
0h	16	TBCTL	500C 5000h	500C 6000h	500C 7000h
2h	16	TBCTL2	500C 5002h	500C 6002h	500C 7002h
6h	16	EPWMSYNCINSEL	500C 5006h	500C 6006h	500C 7006h
8h	16	TBCTR	500C 5008h	500C 6008h	500C 7008h
Ah	16	TBSTS	500C 500Ah	500C 600Ah	500C 700Ah
Ch	16	EPWMSYNCOUTEN	500C 500Ch	500C 600Ch	500C 700Ch
Eh	16	TBCTL3	500C 500Eh	500C 600Eh	500C 700Eh
10h	16	CMPCTL	500C 5010h	500C 6010h	500C 7010h
12h	16	CMPCTL2	500C 5012h	500C 6012h	500C 7012h
18h	16	DBCTL	500C 5018h	500C 6018h	500C 7018h
1Ah	16	DBCTL2	500C 501Ah	500C 601Ah	500C 701Ah
20h	16	AQCTL	500C 5020h	500C 6020h	500C 7020h
22h	16	AQTSRCSEL	500C 5022h	500C 6022h	500C 7022h
28h	16	PCCTL	500C 5028h	500C 6028h	500C 7028h
30h	16	VCAPCTL	500C 5030h	500C 6030h	500C 7030h
32h	16	VCNTCFG	500C 5032h	500C 6032h	500C 7032h
40h	16	HRCNFG	500C 5040h	500C 6040h	500C 7040h
4Eh	16	HRCNFG2	500C 504Eh	500C 604Eh	500C 704Eh
5Ah	16	HRPCTL	500C 505Ah	500C 605Ah	500C 705Ah
5Ch	16	TRREM	500C 505Ch	500C 605Ch	500C 705Ch
68h	16	GLDCTL	500C 5068h	500C 6068h	500C 7068h
6Ah	16	GLDCFG	500C 506Ah	500C 606Ah	500C 706Ah
70h	32	EPWMXLINK	500C 5070h	500C 6070h	500C 7070h

Table 3-680. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096

Offset	Length	Register Name	CONTROLSS_EPWM8_G3 Physical Address	CONTROLSS_EPWM9_G3 Physical Address
0h	16	TBCTL	500C 8000h	500C 9000h
2h	16	TBCTL2	500C 8002h	500C 9002h
6h	16	EPWMSYNCINSEL	500C 8006h	500C 9006h
8h	16	TBCTR	500C 8008h	500C 9008h
Ah	16	TBSTS	500C 800Ah	500C 900Ah
Ch	16	EPWMSYNCOUTEN	500C 800Ch	500C 900Ch
Eh	16	TBCTL3	500C 800Eh	500C 900Eh
10h	16	CMPCTL	500C 8010h	500C 9010h
12h	16	CMPCTL2	500C 8012h	500C 9012h
18h	16	DBCTL	500C 8018h	500C 9018h
1Ah	16	DBCTL2	500C 801Ah	500C 901Ah
20h	16	AQCTL	500C 8020h	500C 9020h
22h	16	AQTSRCSEL	500C 8022h	500C 9022h
28h	16	PCCTL	500C 8028h	500C 9028h
30h	16	VCAPCTL	500C 8030h	500C 9030h
32h	16	VCNTCFG	500C 8032h	500C 9032h
40h	16	HRCNFG	500C 8040h	500C 9040h
4Eh	16	HRCNFG2	500C 804Eh	500C 904Eh
5Ah	16	HRPCTL	500C 805Ah	500C 905Ah

Table 3-680. MEM, MEM Registers, Base Address=0X0000000050000000, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_EPWM8_G3 Physical Address	CONTROLSS_EPWM9_G3 Physical Address
5Ch	16	TRREM	500C 805Ch	500C 905Ch
68h	16	GLDCTL	500C 8068h	500C 9068h
6Ah	16	GLDCFG	500C 806Ah	500C 906Ah
70h	32	EPWMXLINK	500C 8070h	500C 9070h

3.9.1 MEM_TBCTL Registers

3.9.1.1 MEM_TBCTL Register (Offset = 0h) [reset = 83h]

Short Description: Time Base Control Registe

Long Description: Time Base Control Register

Return to Summary Table

Table 3-681. Instance Table

Instance Name	Physical Address
CONTROLSS_EPWM0_G0	5000 0000h
CONTROLSS_EPWM1_G0	5000 1000h
CONTROLSS_EPWM10_G0	5000 A000h
CONTROLSS_EPWM11_G0	5000 B000h
CONTROLSS_EPWM12_G0	5000 C000h
CONTROLSS_EPWM13_G0	5000 D000h
CONTROLSS_EPWM14_G0	5000 E000h
CONTROLSS_EPWM15_G0	5000 F000h
CONTROLSS_EPWM16_G0	5001 0000h
CONTROLSS_EPWM17_G0	5001 1000h
CONTROLSS_EPWM18_G0	5001 2000h
CONTROLSS_EPWM19_G0	5001 3000h
CONTROLSS_EPWM2_G0	5000 2000h
CONTROLSS_EPWM20_G0	5001 4000h
CONTROLSS_EPWM21_G0	5001 5000h
CONTROLSS_EPWM22_G0	5001 6000h
CONTROLSS_EPWM23_G0	5001 7000h
CONTROLSS_EPWM24_G0	5001 8000h
CONTROLSS_EPWM25_G0	5001 9000h
CONTROLSS_EPWM26_G0	5001 A000h
CONTROLSS_EPWM27_G0	5001 B000h
CONTROLSS_EPWM28_G0	5001 C000h
CONTROLSS_EPWM29_G0	5001 D000h
CONTROLSS_EPWM3_G0	5000 3000h
CONTROLSS_EPWM30_G0	5001 E000h
CONTROLSS_EPWM31_G0	5001 F000h
CONTROLSS_EPWM4_G0	5000 4000h
CONTROLSS_EPWM5_G0	5000 5000h
CONTROLSS_EPWM6_G0	5000 6000h
CONTROLSS_EPWM7_G0	5000 7000h
CONTROLSS_EPWM8_G0	5000 8000h
CONTROLSS_EPWM9_G0	5000 9000h
CONTROLSS_EPWM0_G1	5004 0000h
CONTROLSS_EPWM1_G1	5004 1000h
CONTROLSS_EPWM10_G1	5004 A000h
CONTROLSS_EPWM11_G1	5004 B000h
CONTROLSS_EPWM12_G1	5004 C000h
CONTROLSS_EPWM13_G1	5004 D000h
CONTROLSS_EPWM14_G1	5004 E000h

Table 3-681. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM15_G1	5004 F000h
CONTROLSS_EPWM16_G1	5005 0000h
CONTROLSS_EPWM17_G1	5005 1000h
CONTROLSS_EPWM18_G1	5005 2000h
CONTROLSS_EPWM19_G1	5005 3000h
CONTROLSS_EPWM2_G1	5004 2000h
CONTROLSS_EPWM20_G1	5005 4000h
CONTROLSS_EPWM21_G1	5005 5000h
CONTROLSS_EPWM22_G1	5005 6000h
CONTROLSS_EPWM23_G1	5005 7000h
CONTROLSS_EPWM24_G1	5005 8000h
CONTROLSS_EPWM25_G1	5005 9000h
CONTROLSS_EPWM26_G1	5005 A000h
CONTROLSS_EPWM27_G1	5005 B000h
CONTROLSS_EPWM28_G1	5005 C000h
CONTROLSS_EPWM29_G1	5005 D000h
CONTROLSS_EPWM3_G1	5004 3000h
CONTROLSS_EPWM30_G1	5005 E000h
CONTROLSS_EPWM31_G1	5005 F000h
CONTROLSS_EPWM4_G1	5004 4000h
CONTROLSS_EPWM5_G1	5004 5000h
CONTROLSS_EPWM6_G1	5004 6000h
CONTROLSS_EPWM7_G1	5004 7000h
CONTROLSS_EPWM8_G1	5004 8000h
CONTROLSS_EPWM9_G1	5004 9000h
CONTROLSS_EPWM0_G2	5008 0000h
CONTROLSS_EPWM1_G2	5008 1000h
CONTROLSS_EPWM10_G2	5008 A000h
CONTROLSS_EPWM11_G2	5008 B000h
CONTROLSS_EPWM12_G2	5008 C000h
CONTROLSS_EPWM13_G2	5008 D000h
CONTROLSS_EPWM14_G2	5008 E000h
CONTROLSS_EPWM15_G2	5008 F000h
CONTROLSS_EPWM16_G2	5009 0000h
CONTROLSS_EPWM17_G2	5009 1000h
CONTROLSS_EPWM18_G2	5009 2000h
CONTROLSS_EPWM19_G2	5009 3000h
CONTROLSS_EPWM2_G2	5008 2000h
CONTROLSS_EPWM20_G2	5009 4000h
CONTROLSS_EPWM21_G2	5009 5000h
CONTROLSS_EPWM22_G2	5009 6000h
CONTROLSS_EPWM23_G2	5009 7000h
CONTROLSS_EPWM24_G2	5009 8000h
CONTROLSS_EPWM25_G2	5009 9000h
CONTROLSS_EPWM26_G2	5009 A000h
CONTROLSS_EPWM27_G2	5009 B000h
CONTROLSS_EPWM28_G2	5009 C000h

Table 3-681. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM29_G2	5009 D000h
CONTROLSS_EPWM3_G2	5008 3000h
CONTROLSS_EPWM30_G2	5009 E000h
CONTROLSS_EPWM31_G2	5009 F000h
CONTROLSS_EPWM4_G2	5008 4000h
CONTROLSS_EPWM5_G2	5008 5000h
CONTROLSS_EPWM6_G2	5008 6000h
CONTROLSS_EPWM7_G2	5008 7000h
CONTROLSS_EPWM8_G2	5008 8000h
CONTROLSS_EPWM9_G2	5008 9000h
CONTROLSS_EPWM0_G3	500C 0000h
CONTROLSS_EPWM1_G3	500C 1000h
CONTROLSS_EPWM10_G3	500C A000h
CONTROLSS_EPWM11_G3	500C B000h
CONTROLSS_EPWM12_G3	500C C000h
CONTROLSS_EPWM13_G3	500C D000h
CONTROLSS_EPWM14_G3	500C E000h
CONTROLSS_EPWM15_G3	500C F000h
CONTROLSS_EPWM16_G3	500D 0000h
CONTROLSS_EPWM17_G3	500D 1000h
CONTROLSS_EPWM18_G3	500D 2000h
CONTROLSS_EPWM19_G3	500D 3000h
CONTROLSS_EPWM2_G3	500C 2000h
CONTROLSS_EPWM20_G3	500D 4000h
CONTROLSS_EPWM21_G3	500D 5000h
CONTROLSS_EPWM22_G3	500D 6000h
CONTROLSS_EPWM23_G3	500D 7000h
CONTROLSS_EPWM24_G3	500D 8000h
CONTROLSS_EPWM25_G3	500D 9000h
CONTROLSS_EPWM26_G3	500D A000h
CONTROLSS_EPWM27_G3	500D B000h
CONTROLSS_EPWM28_G3	500D C000h
CONTROLSS_EPWM29_G3	500D D000h
CONTROLSS_EPWM3_G3	500C 3000h
CONTROLSS_EPWM30_G3	500D E000h
CONTROLSS_EPWM31_G3	500D F000h
CONTROLSS_EPWM4_G3	500C 4000h
CONTROLSS_EPWM5_G3	500C 5000h
CONTROLSS_EPWM6_G3	500C 6000h
CONTROLSS_EPWM7_G3	500C 7000h
CONTROLSS_EPWM8_G3	500C 8000h
CONTROLSS_EPWM9_G3	500C 9000h

Figure 3-287. TBCTL Name Register

15	14	13	12	11	10	9	8
FREE_SOFT		PHSDIR	CLKDIV			HSPCLKDIV	
R/W		R/W	R/W			R/W	

Figure 3-287. TBCTL Name Register (continued)

0h		0h	0h		1h		
7	6	5	4	3	2	1	0
HSPCLKDIV	SWFSYNC	RESERVED_1		PRDLD	PHSEN	CTRMODE	
R/W	R/W1TS	R		R/W	R/W	R/W	
1h	0h	0h		0h	0h	3h	

Access Types Legend

Table 3-682. TBCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	FREE_SOFT	R/W	0h	Emulation Mode Bits. These bits select the behavior of the ePWM time-base counter during emulation events 00: Stop after the next time-base counter increment or decrement 01: Stop when counter completes a whole cycle: - Up-count mode: stop when the time-base counter = period [TBCTR = TBPRD] - Down-count mode: stop when the time-base counter = 0x00 [TBCTR = 0x00] - Up-down-count mode: stop when the time-base counter = 0x00 [TBCTR = 0x00] 1x: Free run Reset Source: epwm_rst_mod_g_rst_n
13	PHSDIR	R/W	0h	Phase Direction Bit This bit is only used when the time-base counter is configured in the up-down-count mode. The PHSDIR bit indicates the direction the time-base counter [TBCTR] will count after a synchronization event occurs and a new phase value is loaded from the phase [TBPHS] register. This is irrespective of the direction of the counter before the synchronization event.. In the up-count and down-count modes this bit is ignored. 0: Count down after the synchronization event. 1: Count up after the synchronization event. Reset Source: epwm_rst_mod_g_rst_n
12:10	CLKDIV	R/W	0h	Time Base Clock Pre-Scale Bits These bits select the time base clock pre-scale value [TBCLK = EPWMCLK/[HSPCLKDIV * CLKDIV]: 000: /1 [default on reset] 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128 Reset Source: epwm_rst_mod_g_rst_n
9:7	HSPCLKDIV	R/W	1h	High Speed Time Base Clock Pre-Scale Bits These bits determine part of the time-base clock prescale value. TBCLK = EPWMCLK / [HSPCLKDIV x CLKDIV]. This divisor emulates the HSPCLK in the TMS320x281x system as used on the Event Manager [EV] peripheral. 000: /1 001: /2 [default on reset] 010: /4 011: /6 100: /8 101: /10 110: /12 111: /14 Reset Source: epwm_rst_mod_g_rst_n
6	SWFSYNC	R/W1TS	0h	Software Forced Sync Pulse 0: Writing a 0 has no effect and reads always return a 0. 1: Writing a 1 forces a one-time synchronization pulse to be generated. SWFSYNC can be enabled to affect EPWMxSYNCO by setting the EPWMSYNCOUTEN.SWEN bit. Reset Source: epwm_rst_mod_g_rst_n
5:4	RESERVED_1	R	0h	Reserved Reset Source: epwm_rst_mod_g_rst_n
3	PRDLD	R/W	0h	Active Period Reg Load from Shadow Select 0: The period register [TBPRD] is loaded from its shadow register when the time-base counter, TBCTR, is equal to zero and/or a sync event as determined by the TBCTL2[PRDLDSYNC] bit. A write/read to the TBPRD register accesses the shadow register. 1: Immediate Mode [Shadow register bypassed]: A write or read to the TBPRD register accesses the active register. Reset Source: epwm_rst_mod_g_rst_n
2	PHSEN	R/W	0h	Counter Reg Load from Phase Reg Enable 0: Do not load the time-base counter [TBCTR] from the time-base phase register [TBPHS]. 1: Allow Counter to be loaded from the Phase register [TBPHS] and shadow to active load events when an EPWMxSYNCI input signal occurs or a software-forced sync signal, see bit 6. Reset Source: epwm_rst_mod_g_rst_n

Table 3-682. TBCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	CTRMODE	R/W	3h	Counter Mode The time-base counter mode is normally configured once and not changed during normal operation. If you change the mode of the counter, the change will take effect at the next TBCLK edge and the current counter value shall increment or decrement from the value before the mode change. These bits set the time-base counter mode of operation as follows: 00: Up-count mode 01: Down-count mode 10: Up-down count mode 11: Freeze counter operation [default on reset] Reset Source: epwm_rst_mod_g_rst_n

3.9.2 MEM_TBCTL2 Registers

3.9.2.1 MEM_TBCTL2 Register (Offset = 2h) [reset = 0h]

Short Description: Time Base Control Registe

Long Description: Time Base Control Register 2

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Table 3-683. Instance Table

Instance Name	Physical Address
CONTROLSS_EPWM0_G0	5000 0002h
CONTROLSS_EPWM1_G0	5000 1002h
CONTROLSS_EPWM10_G0	5000 A002h
CONTROLSS_EPWM11_G0	5000 B002h
CONTROLSS_EPWM12_G0	5000 C002h
CONTROLSS_EPWM13_G0	5000 D002h
CONTROLSS_EPWM14_G0	5000 E002h
CONTROLSS_EPWM15_G0	5000 F002h
CONTROLSS_EPWM16_G0	5001 0002h
CONTROLSS_EPWM17_G0	5001 1002h
CONTROLSS_EPWM18_G0	5001 2002h
CONTROLSS_EPWM19_G0	5001 3002h
CONTROLSS_EPWM2_G0	5000 2002h
CONTROLSS_EPWM20_G0	5001 4002h
CONTROLSS_EPWM21_G0	5001 5002h
CONTROLSS_EPWM22_G0	5001 6002h
CONTROLSS_EPWM23_G0	5001 7002h
CONTROLSS_EPWM24_G0	5001 8002h
CONTROLSS_EPWM25_G0	5001 9002h
CONTROLSS_EPWM26_G0	5001 A002h
CONTROLSS_EPWM27_G0	5001 B002h
CONTROLSS_EPWM28_G0	5001 C002h
CONTROLSS_EPWM29_G0	5001 D002h
CONTROLSS_EPWM3_G0	5000 3002h
CONTROLSS_EPWM30_G0	5001 E002h
CONTROLSS_EPWM31_G0	5001 F002h
CONTROLSS_EPWM4_G0	5000 4002h
CONTROLSS_EPWM5_G0	5000 5002h
CONTROLSS_EPWM6_G0	5000 6002h
CONTROLSS_EPWM7_G0	5000 7002h
CONTROLSS_EPWM8_G0	5000 8002h
CONTROLSS_EPWM9_G0	5000 9002h
CONTROLSS_EPWM0_G1	5004 0002h
CONTROLSS_EPWM1_G1	5004 1002h
CONTROLSS_EPWM10_G1	5004 A002h
CONTROLSS_EPWM11_G1	5004 B002h
CONTROLSS_EPWM12_G1	5004 C002h
CONTROLSS_EPWM13_G1	5004 D002h
CONTROLSS_EPWM14_G1	5004 E002h

Table 3-683. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM15_G1	5004 F002h
CONTROLSS_EPWM16_G1	5005 0002h
CONTROLSS_EPWM17_G1	5005 1002h
CONTROLSS_EPWM18_G1	5005 2002h
CONTROLSS_EPWM19_G1	5005 3002h
CONTROLSS_EPWM2_G1	5004 2002h
CONTROLSS_EPWM20_G1	5005 4002h
CONTROLSS_EPWM21_G1	5005 5002h
CONTROLSS_EPWM22_G1	5005 6002h
CONTROLSS_EPWM23_G1	5005 7002h
CONTROLSS_EPWM24_G1	5005 8002h
CONTROLSS_EPWM25_G1	5005 9002h
CONTROLSS_EPWM26_G1	5005 A002h
CONTROLSS_EPWM27_G1	5005 B002h
CONTROLSS_EPWM28_G1	5005 C002h
CONTROLSS_EPWM29_G1	5005 D002h
CONTROLSS_EPWM3_G1	5004 3002h
CONTROLSS_EPWM30_G1	5005 E002h
CONTROLSS_EPWM31_G1	5005 F002h
CONTROLSS_EPWM4_G1	5004 4002h
CONTROLSS_EPWM5_G1	5004 5002h
CONTROLSS_EPWM6_G1	5004 6002h
CONTROLSS_EPWM7_G1	5004 7002h
CONTROLSS_EPWM8_G1	5004 8002h
CONTROLSS_EPWM9_G1	5004 9002h
CONTROLSS_EPWM0_G2	5008 0002h
CONTROLSS_EPWM1_G2	5008 1002h
CONTROLSS_EPWM10_G2	5008 A002h
CONTROLSS_EPWM11_G2	5008 B002h
CONTROLSS_EPWM12_G2	5008 C002h
CONTROLSS_EPWM13_G2	5008 D002h
CONTROLSS_EPWM14_G2	5008 E002h
CONTROLSS_EPWM15_G2	5008 F002h
CONTROLSS_EPWM16_G2	5009 0002h
CONTROLSS_EPWM17_G2	5009 1002h
CONTROLSS_EPWM18_G2	5009 2002h
CONTROLSS_EPWM19_G2	5009 3002h
CONTROLSS_EPWM2_G2	5008 2002h
CONTROLSS_EPWM20_G2	5009 4002h
CONTROLSS_EPWM21_G2	5009 5002h
CONTROLSS_EPWM22_G2	5009 6002h
CONTROLSS_EPWM23_G2	5009 7002h
CONTROLSS_EPWM24_G2	5009 8002h
CONTROLSS_EPWM25_G2	5009 9002h
CONTROLSS_EPWM26_G2	5009 A002h
CONTROLSS_EPWM27_G2	5009 B002h
CONTROLSS_EPWM28_G2	5009 C002h

Table 3-683. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM29_G2	5009 D002h
CONTROLSS_EPWM3_G2	5008 3002h
CONTROLSS_EPWM30_G2	5009 E002h
CONTROLSS_EPWM31_G2	5009 F002h
CONTROLSS_EPWM4_G2	5008 4002h
CONTROLSS_EPWM5_G2	5008 5002h
CONTROLSS_EPWM6_G2	5008 6002h
CONTROLSS_EPWM7_G2	5008 7002h
CONTROLSS_EPWM8_G2	5008 8002h
CONTROLSS_EPWM9_G2	5008 9002h
CONTROLSS_EPWM0_G3	500C 0002h
CONTROLSS_EPWM1_G3	500C 1002h
CONTROLSS_EPWM10_G3	500C A002h
CONTROLSS_EPWM11_G3	500C B002h
CONTROLSS_EPWM12_G3	500C C002h
CONTROLSS_EPWM13_G3	500C D002h
CONTROLSS_EPWM14_G3	500C E002h
CONTROLSS_EPWM15_G3	500C F002h
CONTROLSS_EPWM16_G3	500D 0002h
CONTROLSS_EPWM17_G3	500D 1002h
CONTROLSS_EPWM18_G3	500D 2002h
CONTROLSS_EPWM19_G3	500D 3002h
CONTROLSS_EPWM2_G3	500C 2002h
CONTROLSS_EPWM20_G3	500D 4002h
CONTROLSS_EPWM21_G3	500D 5002h
CONTROLSS_EPWM22_G3	500D 6002h
CONTROLSS_EPWM23_G3	500D 7002h
CONTROLSS_EPWM24_G3	500D 8002h
CONTROLSS_EPWM25_G3	500D 9002h
CONTROLSS_EPWM26_G3	500D A002h
CONTROLSS_EPWM27_G3	500D B002h
CONTROLSS_EPWM28_G3	500D C002h
CONTROLSS_EPWM29_G3	500D D002h
CONTROLSS_EPWM3_G3	500C 3002h
CONTROLSS_EPWM30_G3	500D E002h
CONTROLSS_EPWM31_G3	500D F002h
CONTROLSS_EPWM4_G3	500C 4002h
CONTROLSS_EPWM5_G3	500C 5002h
CONTROLSS_EPWM6_G3	500C 6002h
CONTROLSS_EPWM7_G3	500C 7002h
CONTROLSS_EPWM8_G3	500C 8002h
CONTROLSS_EPWM9_G3	500C 9002h

Figure 3-288. TBCTL2 Name Register

15	14	13	12	11	10	9	8
PRDLDSYNC		RESERVED_3		RESERVED_2			
R/W		R		R			

Figure 3-288. TBCTL2 Name Register (continued)

0h		0h		0h			
7	6	5	4	3	2	1	0
OSHTSYNC	OSHTSYNCMODE	SELFCLRTRREM	RESERVED_1				
R/W1TS	R/W	R/W	R				
0h	0h	0h	0h				

Access Types Legend

Table 3-684. TBCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	PRDLDSYNC	R/W	0h	Shadow to Active Period Register Load on SYNC event 00: Shadow to Active Load of TBPRD occurs only when TBCTR = 0 [same as legacy]. 01: Shadow to Active Load of TBPRD occurs both when TBCTR = 0 and when SYNC occurs. 10: Shadow to Active Load of TBPRD occurs only when a SYNC is received. 11: Reserved Note: This bit selection is valid only if TBCTL[PRDLD]=0. Reset Source: epwm_rst_mod_g_rst_n
13:12	RESERVED_3	R	0h	Reserved Reset Source: epwm_rst_mod_g_rst_n
11:8	RESERVED_2	R	0h	Reserved Reset Source: epwm_rst_mod_g_rst_n
7	OSHTSYNC	R/W1TS	0h	Oneshot sync bit 0: Writing a '0' has no effect. 1: Allow one sync pulse to propogate. Reset Source: epwm_rst_mod_g_rst_n
6	OSHTSYNCMODE	R/W	0h	Oneshot sync enable bit 0: Oneshot sync mode disabled 1: Oneshot sync mode enabled Reset Source: epwm_rst_mod_g_rst_n
5	SELFCLRTRREM	R/W	0h	Loop back sync pulse to enable self sync operation 0: Self clear function of TRREM disabled. 1: Self clear function of TRREM enabled Reset Source: epwm_rst_mod_g_rst_n
4:0	RESERVED_1	R	0h	Reserved Reset Source: epwm_rst_mod_g_rst_n

3.9.3 MEM_EPWMSYNCINSEL Registers

3.9.3.1 MEM_EPWMSYNCINSEL Register (Offset = 6h) [reset = 1h]

Short Description: EPWMxSYNCIN Source Select

Long Description: EPWMxSYNCIN Source Select Register

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Table 3-685. Instance Table

Instance Name	Physical Address
CONTROLSS_EPWM0_G0	5000 0006h
CONTROLSS_EPWM1_G0	5000 1006h
CONTROLSS_EPWM10_G0	5000 A006h
CONTROLSS_EPWM11_G0	5000 B006h
CONTROLSS_EPWM12_G0	5000 C006h
CONTROLSS_EPWM13_G0	5000 D006h
CONTROLSS_EPWM14_G0	5000 E006h
CONTROLSS_EPWM15_G0	5000 F006h
CONTROLSS_EPWM16_G0	5001 0006h
CONTROLSS_EPWM17_G0	5001 1006h
CONTROLSS_EPWM18_G0	5001 2006h
CONTROLSS_EPWM19_G0	5001 3006h
CONTROLSS_EPWM2_G0	5000 2006h
CONTROLSS_EPWM20_G0	5001 4006h
CONTROLSS_EPWM21_G0	5001 5006h
CONTROLSS_EPWM22_G0	5001 6006h
CONTROLSS_EPWM23_G0	5001 7006h
CONTROLSS_EPWM24_G0	5001 8006h
CONTROLSS_EPWM25_G0	5001 9006h
CONTROLSS_EPWM26_G0	5001 A006h
CONTROLSS_EPWM27_G0	5001 B006h
CONTROLSS_EPWM28_G0	5001 C006h
CONTROLSS_EPWM29_G0	5001 D006h
CONTROLSS_EPWM3_G0	5000 3006h
CONTROLSS_EPWM30_G0	5001 E006h
CONTROLSS_EPWM31_G0	5001 F006h
CONTROLSS_EPWM4_G0	5000 4006h
CONTROLSS_EPWM5_G0	5000 5006h
CONTROLSS_EPWM6_G0	5000 6006h
CONTROLSS_EPWM7_G0	5000 7006h
CONTROLSS_EPWM8_G0	5000 8006h
CONTROLSS_EPWM9_G0	5000 9006h
CONTROLSS_EPWM0_G1	5004 0006h
CONTROLSS_EPWM1_G1	5004 1006h
CONTROLSS_EPWM10_G1	5004 A006h
CONTROLSS_EPWM11_G1	5004 B006h
CONTROLSS_EPWM12_G1	5004 C006h
CONTROLSS_EPWM13_G1	5004 D006h
CONTROLSS_EPWM14_G1	5004 E006h

Table 3-685. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM15_G1	5004 F006h
CONTROLSS_EPWM16_G1	5005 0006h
CONTROLSS_EPWM17_G1	5005 1006h
CONTROLSS_EPWM18_G1	5005 2006h
CONTROLSS_EPWM19_G1	5005 3006h
CONTROLSS_EPWM2_G1	5004 2006h
CONTROLSS_EPWM20_G1	5005 4006h
CONTROLSS_EPWM21_G1	5005 5006h
CONTROLSS_EPWM22_G1	5005 6006h
CONTROLSS_EPWM23_G1	5005 7006h
CONTROLSS_EPWM24_G1	5005 8006h
CONTROLSS_EPWM25_G1	5005 9006h
CONTROLSS_EPWM26_G1	5005 A006h
CONTROLSS_EPWM27_G1	5005 B006h
CONTROLSS_EPWM28_G1	5005 C006h
CONTROLSS_EPWM29_G1	5005 D006h
CONTROLSS_EPWM3_G1	5004 3006h
CONTROLSS_EPWM30_G1	5005 E006h
CONTROLSS_EPWM31_G1	5005 F006h
CONTROLSS_EPWM4_G1	5004 4006h
CONTROLSS_EPWM5_G1	5004 5006h
CONTROLSS_EPWM6_G1	5004 6006h
CONTROLSS_EPWM7_G1	5004 7006h
CONTROLSS_EPWM8_G1	5004 8006h
CONTROLSS_EPWM9_G1	5004 9006h
CONTROLSS_EPWM0_G2	5008 0006h
CONTROLSS_EPWM1_G2	5008 1006h
CONTROLSS_EPWM10_G2	5008 A006h
CONTROLSS_EPWM11_G2	5008 B006h
CONTROLSS_EPWM12_G2	5008 C006h
CONTROLSS_EPWM13_G2	5008 D006h
CONTROLSS_EPWM14_G2	5008 E006h
CONTROLSS_EPWM15_G2	5008 F006h
CONTROLSS_EPWM16_G2	5009 0006h
CONTROLSS_EPWM17_G2	5009 1006h
CONTROLSS_EPWM18_G2	5009 2006h
CONTROLSS_EPWM19_G2	5009 3006h
CONTROLSS_EPWM2_G2	5008 2006h
CONTROLSS_EPWM20_G2	5009 4006h
CONTROLSS_EPWM21_G2	5009 5006h
CONTROLSS_EPWM22_G2	5009 6006h
CONTROLSS_EPWM23_G2	5009 7006h
CONTROLSS_EPWM24_G2	5009 8006h
CONTROLSS_EPWM25_G2	5009 9006h
CONTROLSS_EPWM26_G2	5009 A006h
CONTROLSS_EPWM27_G2	5009 B006h
CONTROLSS_EPWM28_G2	5009 C006h

Table 3-685. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM29_G2	5009 D006h
CONTROLSS_EPWM3_G2	5008 3006h
CONTROLSS_EPWM30_G2	5009 E006h
CONTROLSS_EPWM31_G2	5009 F006h
CONTROLSS_EPWM4_G2	5008 4006h
CONTROLSS_EPWM5_G2	5008 5006h
CONTROLSS_EPWM6_G2	5008 6006h
CONTROLSS_EPWM7_G2	5008 7006h
CONTROLSS_EPWM8_G2	5008 8006h
CONTROLSS_EPWM9_G2	5008 9006h
CONTROLSS_EPWM0_G3	500C 0006h
CONTROLSS_EPWM1_G3	500C 1006h
CONTROLSS_EPWM10_G3	500C A006h
CONTROLSS_EPWM11_G3	500C B006h
CONTROLSS_EPWM12_G3	500C C006h
CONTROLSS_EPWM13_G3	500C D006h
CONTROLSS_EPWM14_G3	500C E006h
CONTROLSS_EPWM15_G3	500C F006h
CONTROLSS_EPWM16_G3	500D 0006h
CONTROLSS_EPWM17_G3	500D 1006h
CONTROLSS_EPWM18_G3	500D 2006h
CONTROLSS_EPWM19_G3	500D 3006h
CONTROLSS_EPWM2_G3	500C 2006h
CONTROLSS_EPWM20_G3	500D 4006h
CONTROLSS_EPWM21_G3	500D 5006h
CONTROLSS_EPWM22_G3	500D 6006h
CONTROLSS_EPWM23_G3	500D 7006h
CONTROLSS_EPWM24_G3	500D 8006h
CONTROLSS_EPWM25_G3	500D 9006h
CONTROLSS_EPWM26_G3	500D A006h
CONTROLSS_EPWM27_G3	500D B006h
CONTROLSS_EPWM28_G3	500D C006h
CONTROLSS_EPWM29_G3	500D D006h
CONTROLSS_EPWM3_G3	500C 3006h
CONTROLSS_EPWM30_G3	500D E006h
CONTROLSS_EPWM31_G3	500D F006h
CONTROLSS_EPWM4_G3	500C 4006h
CONTROLSS_EPWM5_G3	500C 5006h
CONTROLSS_EPWM6_G3	500C 6006h
CONTROLSS_EPWM7_G3	500C 7006h
CONTROLSS_EPWM8_G3	500C 8006h
CONTROLSS_EPWM9_G3	500C 9006h

Figure 3-289. EPWMSYNCINSEL Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							

Figure 3-289. EPWMSYNCINSEL Name Register (continued)

0h							
7	6	5	4	3	2	1	0
RESERVED_1	SEL						
R	R/W						
0h	1h						

Access Types Legend

Table 3-686. EPWMSYNCINSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:7	RESERVED_1	R	0h	Reserved Reset Source: epwm_rst_mod_g_rst_n
6:0	SEL	R/W	1h	These bits determine the source of the EPWMxSYNCI signal. 0x00 Disabled Other Values defined in device interconnect spec Reset Source: epwm_rst_mod_g_rst_n

3.9.4 MEM_TBCTR Registers

3.9.4.1 MEM_TBCTR Register (Offset = 8h) [reset = 0h]

Short Description: Time Base Counter Registe

Long Description: Time Base Counter Register

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Table 3-687. Instance Table

Instance Name	Physical Address
CONTROLSS_EPWM0_G0	5000 0008h
CONTROLSS_EPWM1_G0	5000 1008h
CONTROLSS_EPWM10_G0	5000 A008h
CONTROLSS_EPWM11_G0	5000 B008h
CONTROLSS_EPWM12_G0	5000 C008h
CONTROLSS_EPWM13_G0	5000 D008h
CONTROLSS_EPWM14_G0	5000 E008h
CONTROLSS_EPWM15_G0	5000 F008h
CONTROLSS_EPWM16_G0	5001 0008h
CONTROLSS_EPWM17_G0	5001 1008h
CONTROLSS_EPWM18_G0	5001 2008h
CONTROLSS_EPWM19_G0	5001 3008h
CONTROLSS_EPWM2_G0	5000 2008h
CONTROLSS_EPWM20_G0	5001 4008h
CONTROLSS_EPWM21_G0	5001 5008h
CONTROLSS_EPWM22_G0	5001 6008h
CONTROLSS_EPWM23_G0	5001 7008h
CONTROLSS_EPWM24_G0	5001 8008h
CONTROLSS_EPWM25_G0	5001 9008h
CONTROLSS_EPWM26_G0	5001 A008h
CONTROLSS_EPWM27_G0	5001 B008h
CONTROLSS_EPWM28_G0	5001 C008h
CONTROLSS_EPWM29_G0	5001 D008h
CONTROLSS_EPWM3_G0	5000 3008h
CONTROLSS_EPWM30_G0	5001 E008h
CONTROLSS_EPWM31_G0	5001 F008h
CONTROLSS_EPWM4_G0	5000 4008h
CONTROLSS_EPWM5_G0	5000 5008h
CONTROLSS_EPWM6_G0	5000 6008h
CONTROLSS_EPWM7_G0	5000 7008h
CONTROLSS_EPWM8_G0	5000 8008h
CONTROLSS_EPWM9_G0	5000 9008h
CONTROLSS_EPWM0_G1	5004 0008h
CONTROLSS_EPWM1_G1	5004 1008h
CONTROLSS_EPWM10_G1	5004 A008h
CONTROLSS_EPWM11_G1	5004 B008h
CONTROLSS_EPWM12_G1	5004 C008h
CONTROLSS_EPWM13_G1	5004 D008h
CONTROLSS_EPWM14_G1	5004 E008h

Table 3-687. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM15_G1	5004 F008h
CONTROLSS_EPWM16_G1	5005 0008h
CONTROLSS_EPWM17_G1	5005 1008h
CONTROLSS_EPWM18_G1	5005 2008h
CONTROLSS_EPWM19_G1	5005 3008h
CONTROLSS_EPWM2_G1	5004 2008h
CONTROLSS_EPWM20_G1	5005 4008h
CONTROLSS_EPWM21_G1	5005 5008h
CONTROLSS_EPWM22_G1	5005 6008h
CONTROLSS_EPWM23_G1	5005 7008h
CONTROLSS_EPWM24_G1	5005 8008h
CONTROLSS_EPWM25_G1	5005 9008h
CONTROLSS_EPWM26_G1	5005 A008h
CONTROLSS_EPWM27_G1	5005 B008h
CONTROLSS_EPWM28_G1	5005 C008h
CONTROLSS_EPWM29_G1	5005 D008h
CONTROLSS_EPWM3_G1	5004 3008h
CONTROLSS_EPWM30_G1	5005 E008h
CONTROLSS_EPWM31_G1	5005 F008h
CONTROLSS_EPWM4_G1	5004 4008h
CONTROLSS_EPWM5_G1	5004 5008h
CONTROLSS_EPWM6_G1	5004 6008h
CONTROLSS_EPWM7_G1	5004 7008h
CONTROLSS_EPWM8_G1	5004 8008h
CONTROLSS_EPWM9_G1	5004 9008h
CONTROLSS_EPWM0_G2	5008 0008h
CONTROLSS_EPWM1_G2	5008 1008h
CONTROLSS_EPWM10_G2	5008 A008h
CONTROLSS_EPWM11_G2	5008 B008h
CONTROLSS_EPWM12_G2	5008 C008h
CONTROLSS_EPWM13_G2	5008 D008h
CONTROLSS_EPWM14_G2	5008 E008h
CONTROLSS_EPWM15_G2	5008 F008h
CONTROLSS_EPWM16_G2	5009 0008h
CONTROLSS_EPWM17_G2	5009 1008h
CONTROLSS_EPWM18_G2	5009 2008h
CONTROLSS_EPWM19_G2	5009 3008h
CONTROLSS_EPWM2_G2	5008 2008h
CONTROLSS_EPWM20_G2	5009 4008h
CONTROLSS_EPWM21_G2	5009 5008h
CONTROLSS_EPWM22_G2	5009 6008h
CONTROLSS_EPWM23_G2	5009 7008h
CONTROLSS_EPWM24_G2	5009 8008h
CONTROLSS_EPWM25_G2	5009 9008h
CONTROLSS_EPWM26_G2	5009 A008h
CONTROLSS_EPWM27_G2	5009 B008h
CONTROLSS_EPWM28_G2	5009 C008h

Table 3-687. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM29_G2	5009 D008h
CONTROLSS_EPWM3_G2	5008 3008h
CONTROLSS_EPWM30_G2	5009 E008h
CONTROLSS_EPWM31_G2	5009 F008h
CONTROLSS_EPWM4_G2	5008 4008h
CONTROLSS_EPWM5_G2	5008 5008h
CONTROLSS_EPWM6_G2	5008 6008h
CONTROLSS_EPWM7_G2	5008 7008h
CONTROLSS_EPWM8_G2	5008 8008h
CONTROLSS_EPWM9_G2	5008 9008h
CONTROLSS_EPWM0_G3	500C 0008h
CONTROLSS_EPWM1_G3	500C 1008h
CONTROLSS_EPWM10_G3	500C A008h
CONTROLSS_EPWM11_G3	500C B008h
CONTROLSS_EPWM12_G3	500C C008h
CONTROLSS_EPWM13_G3	500C D008h
CONTROLSS_EPWM14_G3	500C E008h
CONTROLSS_EPWM15_G3	500C F008h
CONTROLSS_EPWM16_G3	500D 0008h
CONTROLSS_EPWM17_G3	500D 1008h
CONTROLSS_EPWM18_G3	500D 2008h
CONTROLSS_EPWM19_G3	500D 3008h
CONTROLSS_EPWM2_G3	500C 2008h
CONTROLSS_EPWM20_G3	500D 4008h
CONTROLSS_EPWM21_G3	500D 5008h
CONTROLSS_EPWM22_G3	500D 6008h
CONTROLSS_EPWM23_G3	500D 7008h
CONTROLSS_EPWM24_G3	500D 8008h
CONTROLSS_EPWM25_G3	500D 9008h
CONTROLSS_EPWM26_G3	500D A008h
CONTROLSS_EPWM27_G3	500D B008h
CONTROLSS_EPWM28_G3	500D C008h
CONTROLSS_EPWM29_G3	500D D008h
CONTROLSS_EPWM3_G3	500C 3008h
CONTROLSS_EPWM30_G3	500D E008h
CONTROLSS_EPWM31_G3	500D F008h
CONTROLSS_EPWM4_G3	500C 4008h
CONTROLSS_EPWM5_G3	500C 5008h
CONTROLSS_EPWM6_G3	500C 6008h
CONTROLSS_EPWM7_G3	500C 7008h
CONTROLSS_EPWM8_G3	500C 8008h
CONTROLSS_EPWM9_G3	500C 9008h

Figure 3-290. TBCTR Name Register

15	14	13	12	11	10	9	8
TBCTR							
R/W							

Figure 3-290. TBCTR Name Register (continued)

0h							
7	6	5	4	3	2	1	0
TBCTR							
R/W							
0h							

Access Types Legend

Table 3-688. TBCTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TBCTR	R/W	0h	Time Base Counter Register Reset Source: epwm_rst_mod_g_rst_n

3.9.5 MEM_TBSTS Registers

3.9.5.1 MEM_TBSTS Register (Offset = Ah) [reset = 1h]

Short Description: Time Base Status Register

Long Description: Time Base Status Register

Return to Summary Table

Table 3-689. Instance Table

Instance Name	Physical Address
CONTROLSS_EPWM0_G0	5000 000Ah
CONTROLSS_EPWM1_G0	5000 100Ah
CONTROLSS_EPWM10_G0	5000 A00Ah
CONTROLSS_EPWM11_G0	5000 B00Ah
CONTROLSS_EPWM12_G0	5000 C00Ah
CONTROLSS_EPWM13_G0	5000 D00Ah
CONTROLSS_EPWM14_G0	5000 E00Ah
CONTROLSS_EPWM15_G0	5000 F00Ah
CONTROLSS_EPWM16_G0	5001 000Ah
CONTROLSS_EPWM17_G0	5001 100Ah
CONTROLSS_EPWM18_G0	5001 200Ah
CONTROLSS_EPWM19_G0	5001 300Ah
CONTROLSS_EPWM2_G0	5000 200Ah
CONTROLSS_EPWM20_G0	5001 400Ah
CONTROLSS_EPWM21_G0	5001 500Ah
CONTROLSS_EPWM22_G0	5001 600Ah
CONTROLSS_EPWM23_G0	5001 700Ah
CONTROLSS_EPWM24_G0	5001 800Ah
CONTROLSS_EPWM25_G0	5001 900Ah
CONTROLSS_EPWM26_G0	5001 A00Ah
CONTROLSS_EPWM27_G0	5001 B00Ah
CONTROLSS_EPWM28_G0	5001 C00Ah
CONTROLSS_EPWM29_G0	5001 D00Ah
CONTROLSS_EPWM3_G0	5000 300Ah
CONTROLSS_EPWM30_G0	5001 E00Ah
CONTROLSS_EPWM31_G0	5001 F00Ah
CONTROLSS_EPWM4_G0	5000 400Ah
CONTROLSS_EPWM5_G0	5000 500Ah
CONTROLSS_EPWM6_G0	5000 600Ah
CONTROLSS_EPWM7_G0	5000 700Ah
CONTROLSS_EPWM8_G0	5000 800Ah
CONTROLSS_EPWM9_G0	5000 900Ah
CONTROLSS_EPWM0_G1	5004 000Ah
CONTROLSS_EPWM1_G1	5004 100Ah
CONTROLSS_EPWM10_G1	5004 A00Ah
CONTROLSS_EPWM11_G1	5004 B00Ah
CONTROLSS_EPWM12_G1	5004 C00Ah
CONTROLSS_EPWM13_G1	5004 D00Ah
CONTROLSS_EPWM14_G1	5004 E00Ah

Table 3-689. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM15_G1	5004 F00Ah
CONTROLSS_EPWM16_G1	5005 000Ah
CONTROLSS_EPWM17_G1	5005 100Ah
CONTROLSS_EPWM18_G1	5005 200Ah
CONTROLSS_EPWM19_G1	5005 300Ah
CONTROLSS_EPWM2_G1	5004 200Ah
CONTROLSS_EPWM20_G1	5005 400Ah
CONTROLSS_EPWM21_G1	5005 500Ah
CONTROLSS_EPWM22_G1	5005 600Ah
CONTROLSS_EPWM23_G1	5005 700Ah
CONTROLSS_EPWM24_G1	5005 800Ah
CONTROLSS_EPWM25_G1	5005 900Ah
CONTROLSS_EPWM26_G1	5005 A00Ah
CONTROLSS_EPWM27_G1	5005 B00Ah
CONTROLSS_EPWM28_G1	5005 C00Ah
CONTROLSS_EPWM29_G1	5005 D00Ah
CONTROLSS_EPWM3_G1	5004 300Ah
CONTROLSS_EPWM30_G1	5005 E00Ah
CONTROLSS_EPWM31_G1	5005 F00Ah
CONTROLSS_EPWM4_G1	5004 400Ah
CONTROLSS_EPWM5_G1	5004 500Ah
CONTROLSS_EPWM6_G1	5004 600Ah
CONTROLSS_EPWM7_G1	5004 700Ah
CONTROLSS_EPWM8_G1	5004 800Ah
CONTROLSS_EPWM9_G1	5004 900Ah
CONTROLSS_EPWM0_G2	5008 000Ah
CONTROLSS_EPWM1_G2	5008 100Ah
CONTROLSS_EPWM10_G2	5008 A00Ah
CONTROLSS_EPWM11_G2	5008 B00Ah
CONTROLSS_EPWM12_G2	5008 C00Ah
CONTROLSS_EPWM13_G2	5008 D00Ah
CONTROLSS_EPWM14_G2	5008 E00Ah
CONTROLSS_EPWM15_G2	5008 F00Ah
CONTROLSS_EPWM16_G2	5009 000Ah
CONTROLSS_EPWM17_G2	5009 100Ah
CONTROLSS_EPWM18_G2	5009 200Ah
CONTROLSS_EPWM19_G2	5009 300Ah
CONTROLSS_EPWM2_G2	5008 200Ah
CONTROLSS_EPWM20_G2	5009 400Ah
CONTROLSS_EPWM21_G2	5009 500Ah
CONTROLSS_EPWM22_G2	5009 600Ah
CONTROLSS_EPWM23_G2	5009 700Ah
CONTROLSS_EPWM24_G2	5009 800Ah
CONTROLSS_EPWM25_G2	5009 900Ah
CONTROLSS_EPWM26_G2	5009 A00Ah
CONTROLSS_EPWM27_G2	5009 B00Ah
CONTROLSS_EPWM28_G2	5009 C00Ah

Table 3-689. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM29_G2	5009 D00Ah
CONTROLSS_EPWM3_G2	5008 300Ah
CONTROLSS_EPWM30_G2	5009 E00Ah
CONTROLSS_EPWM31_G2	5009 F00Ah
CONTROLSS_EPWM4_G2	5008 400Ah
CONTROLSS_EPWM5_G2	5008 500Ah
CONTROLSS_EPWM6_G2	5008 600Ah
CONTROLSS_EPWM7_G2	5008 700Ah
CONTROLSS_EPWM8_G2	5008 800Ah
CONTROLSS_EPWM9_G2	5008 900Ah
CONTROLSS_EPWM0_G3	500C 000Ah
CONTROLSS_EPWM1_G3	500C 100Ah
CONTROLSS_EPWM10_G3	500C A00Ah
CONTROLSS_EPWM11_G3	500C B00Ah
CONTROLSS_EPWM12_G3	500C C00Ah
CONTROLSS_EPWM13_G3	500C D00Ah
CONTROLSS_EPWM14_G3	500C E00Ah
CONTROLSS_EPWM15_G3	500C F00Ah
CONTROLSS_EPWM16_G3	500D 000Ah
CONTROLSS_EPWM17_G3	500D 100Ah
CONTROLSS_EPWM18_G3	500D 200Ah
CONTROLSS_EPWM19_G3	500D 300Ah
CONTROLSS_EPWM2_G3	500C 200Ah
CONTROLSS_EPWM20_G3	500D 400Ah
CONTROLSS_EPWM21_G3	500D 500Ah
CONTROLSS_EPWM22_G3	500D 600Ah
CONTROLSS_EPWM23_G3	500D 700Ah
CONTROLSS_EPWM24_G3	500D 800Ah
CONTROLSS_EPWM25_G3	500D 900Ah
CONTROLSS_EPWM26_G3	500D A00Ah
CONTROLSS_EPWM27_G3	500D B00Ah
CONTROLSS_EPWM28_G3	500D C00Ah
CONTROLSS_EPWM29_G3	500D D00Ah
CONTROLSS_EPWM3_G3	500C 300Ah
CONTROLSS_EPWM30_G3	500D E00Ah
CONTROLSS_EPWM31_G3	500D F00Ah
CONTROLSS_EPWM4_G3	500C 400Ah
CONTROLSS_EPWM5_G3	500C 500Ah
CONTROLSS_EPWM6_G3	500C 600Ah
CONTROLSS_EPWM7_G3	500C 700Ah
CONTROLSS_EPWM8_G3	500C 800Ah
CONTROLSS_EPWM9_G3	500C 900Ah

Figure 3-291. TBSTS Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							

Figure 3-291. TBSTS Name Register (continued)

0h							
7	6	5	4	3	2	1	0
RESERVED_1					CTRMAX	SYNCI	CTRDIR
R					R/W1TC	R/W1TC	R
0h					0h	0h	1h

Access Types Legend

Table 3-690. TBSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:3	RESERVED_1	R	0h	Reserved Reset Source: epwm_rst_mod_g_rst_n
2	CTRMAX	R/W1TC	0h	Time-Base Counter Max Latched Status Bit 0: Reading a 0 indicates the time-base counter never reached its maximum value. Writing a 0 will have no effect. 1: Reading a 1 on this bit indicates that the time-base counter reached the max value 0xFFFF. Writing a 1 to this bit will clear the latched event. Reset Source: epwm_rst_mod_g_rst_n
1	SYNCI	R/W1TC	0h	Input Synchronization Latched Status Bit 0: Writing a 0 will have no effect. Reading a 0 indicates no external synchronization event has occurred. 1: Reading a 1 on this bit indicates that an external synchronization event has occurred [EPWMxSYNCI]. Writing a 1 to this bit will clear the latched event. Reset Source: epwm_rst_mod_g_rst_n
0	CTRDIR	R	1h	Time Base Counter Direction Status Bit 0: Time-Base Counter is currently counting down. 1: Time-Base Counter is currently counting up. Note: This bit is only valid when the counter is not frozen. Reset Source: epwm_rst_mod_g_rst_n

3.9.6 MEM_EPWMSYNCOUTEN Registers

3.9.6.1 MEM_EPWMSYNCOUTEN Register (Offset = Ch) [reset = 1h]

Short Description: EPWMxSYNCOUT Source Enabl

Long Description: EPWMxSYNCOUT Source Enable Register

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Table 3-691. Instance Table

Instance Name	Physical Address
CONTROLSS_EPWM0_G0	5000 000Ch
CONTROLSS_EPWM1_G0	5000 100Ch
CONTROLSS_EPWM10_G0	5000 A00Ch
CONTROLSS_EPWM11_G0	5000 B00Ch
CONTROLSS_EPWM12_G0	5000 C00Ch
CONTROLSS_EPWM13_G0	5000 D00Ch
CONTROLSS_EPWM14_G0	5000 E00Ch
CONTROLSS_EPWM15_G0	5000 F00Ch
CONTROLSS_EPWM16_G0	5001 000Ch
CONTROLSS_EPWM17_G0	5001 100Ch
CONTROLSS_EPWM18_G0	5001 200Ch
CONTROLSS_EPWM19_G0	5001 300Ch
CONTROLSS_EPWM2_G0	5000 200Ch
CONTROLSS_EPWM20_G0	5001 400Ch
CONTROLSS_EPWM21_G0	5001 500Ch
CONTROLSS_EPWM22_G0	5001 600Ch
CONTROLSS_EPWM23_G0	5001 700Ch
CONTROLSS_EPWM24_G0	5001 800Ch
CONTROLSS_EPWM25_G0	5001 900Ch
CONTROLSS_EPWM26_G0	5001 A00Ch
CONTROLSS_EPWM27_G0	5001 B00Ch
CONTROLSS_EPWM28_G0	5001 C00Ch
CONTROLSS_EPWM29_G0	5001 D00Ch
CONTROLSS_EPWM3_G0	5000 300Ch
CONTROLSS_EPWM30_G0	5001 E00Ch
CONTROLSS_EPWM31_G0	5001 F00Ch
CONTROLSS_EPWM4_G0	5000 400Ch
CONTROLSS_EPWM5_G0	5000 500Ch
CONTROLSS_EPWM6_G0	5000 600Ch
CONTROLSS_EPWM7_G0	5000 700Ch
CONTROLSS_EPWM8_G0	5000 800Ch
CONTROLSS_EPWM9_G0	5000 900Ch
CONTROLSS_EPWM0_G1	5004 000Ch
CONTROLSS_EPWM1_G1	5004 100Ch
CONTROLSS_EPWM10_G1	5004 A00Ch
CONTROLSS_EPWM11_G1	5004 B00Ch
CONTROLSS_EPWM12_G1	5004 C00Ch
CONTROLSS_EPWM13_G1	5004 D00Ch
CONTROLSS_EPWM14_G1	5004 E00Ch

Table 3-691. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM15_G1	5004 F00Ch
CONTROLSS_EPWM16_G1	5005 000Ch
CONTROLSS_EPWM17_G1	5005 100Ch
CONTROLSS_EPWM18_G1	5005 200Ch
CONTROLSS_EPWM19_G1	5005 300Ch
CONTROLSS_EPWM2_G1	5004 200Ch
CONTROLSS_EPWM20_G1	5005 400Ch
CONTROLSS_EPWM21_G1	5005 500Ch
CONTROLSS_EPWM22_G1	5005 600Ch
CONTROLSS_EPWM23_G1	5005 700Ch
CONTROLSS_EPWM24_G1	5005 800Ch
CONTROLSS_EPWM25_G1	5005 900Ch
CONTROLSS_EPWM26_G1	5005 A00Ch
CONTROLSS_EPWM27_G1	5005 B00Ch
CONTROLSS_EPWM28_G1	5005 C00Ch
CONTROLSS_EPWM29_G1	5005 D00Ch
CONTROLSS_EPWM3_G1	5004 300Ch
CONTROLSS_EPWM30_G1	5005 E00Ch
CONTROLSS_EPWM31_G1	5005 F00Ch
CONTROLSS_EPWM4_G1	5004 400Ch
CONTROLSS_EPWM5_G1	5004 500Ch
CONTROLSS_EPWM6_G1	5004 600Ch
CONTROLSS_EPWM7_G1	5004 700Ch
CONTROLSS_EPWM8_G1	5004 800Ch
CONTROLSS_EPWM9_G1	5004 900Ch
CONTROLSS_EPWM0_G2	5008 000Ch
CONTROLSS_EPWM1_G2	5008 100Ch
CONTROLSS_EPWM10_G2	5008 A00Ch
CONTROLSS_EPWM11_G2	5008 B00Ch
CONTROLSS_EPWM12_G2	5008 C00Ch
CONTROLSS_EPWM13_G2	5008 D00Ch
CONTROLSS_EPWM14_G2	5008 E00Ch
CONTROLSS_EPWM15_G2	5008 F00Ch
CONTROLSS_EPWM16_G2	5009 000Ch
CONTROLSS_EPWM17_G2	5009 100Ch
CONTROLSS_EPWM18_G2	5009 200Ch
CONTROLSS_EPWM19_G2	5009 300Ch
CONTROLSS_EPWM2_G2	5008 200Ch
CONTROLSS_EPWM20_G2	5009 400Ch
CONTROLSS_EPWM21_G2	5009 500Ch
CONTROLSS_EPWM22_G2	5009 600Ch
CONTROLSS_EPWM23_G2	5009 700Ch
CONTROLSS_EPWM24_G2	5009 800Ch
CONTROLSS_EPWM25_G2	5009 900Ch
CONTROLSS_EPWM26_G2	5009 A00Ch
CONTROLSS_EPWM27_G2	5009 B00Ch
CONTROLSS_EPWM28_G2	5009 C00Ch

Table 3-691. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM29_G2	5009 D00Ch
CONTROLSS_EPWM3_G2	5008 300Ch
CONTROLSS_EPWM30_G2	5009 E00Ch
CONTROLSS_EPWM31_G2	5009 F00Ch
CONTROLSS_EPWM4_G2	5008 400Ch
CONTROLSS_EPWM5_G2	5008 500Ch
CONTROLSS_EPWM6_G2	5008 600Ch
CONTROLSS_EPWM7_G2	5008 700Ch
CONTROLSS_EPWM8_G2	5008 800Ch
CONTROLSS_EPWM9_G2	5008 900Ch
CONTROLSS_EPWM0_G3	500C 000Ch
CONTROLSS_EPWM1_G3	500C 100Ch
CONTROLSS_EPWM10_G3	500C A00Ch
CONTROLSS_EPWM11_G3	500C B00Ch
CONTROLSS_EPWM12_G3	500C C00Ch
CONTROLSS_EPWM13_G3	500C D00Ch
CONTROLSS_EPWM14_G3	500C E00Ch
CONTROLSS_EPWM15_G3	500C F00Ch
CONTROLSS_EPWM16_G3	500D 000Ch
CONTROLSS_EPWM17_G3	500D 100Ch
CONTROLSS_EPWM18_G3	500D 200Ch
CONTROLSS_EPWM19_G3	500D 300Ch
CONTROLSS_EPWM2_G3	500C 200Ch
CONTROLSS_EPWM20_G3	500D 400Ch
CONTROLSS_EPWM21_G3	500D 500Ch
CONTROLSS_EPWM22_G3	500D 600Ch
CONTROLSS_EPWM23_G3	500D 700Ch
CONTROLSS_EPWM24_G3	500D 800Ch
CONTROLSS_EPWM25_G3	500D 900Ch
CONTROLSS_EPWM26_G3	500D A00Ch
CONTROLSS_EPWM27_G3	500D B00Ch
CONTROLSS_EPWM28_G3	500D C00Ch
CONTROLSS_EPWM29_G3	500D D00Ch
CONTROLSS_EPWM3_G3	500C 300Ch
CONTROLSS_EPWM30_G3	500D E00Ch
CONTROLSS_EPWM31_G3	500D F00Ch
CONTROLSS_EPWM4_G3	500C 400Ch
CONTROLSS_EPWM5_G3	500C 500Ch
CONTROLSS_EPWM6_G3	500C 600Ch
CONTROLSS_EPWM7_G3	500C 700Ch
CONTROLSS_EPWM8_G3	500C 800Ch
CONTROLSS_EPWM9_G3	500C 900Ch

Figure 3-292. EPWMSYNCOUTEN Name Register

15	14	13	12	11	10	9	8
RESERVED_2							
R							

Figure 3-292. EPWMSYNCOUTEN Name Register (continued)

0h							
7	6	5	4	3	2	1	0
RESERVED_1	DCBEVT1EN	DCAEVT1EN	CMPDEN	CMPCEN	CMPBEN	ZEROEN	SWEN
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	1h

Access Types Legend

Table 3-692. EPWMSYNCOUTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED_2	R	0h	Reserved Reset Source: epwm_rst_mod_g_rst_n
7	RESERVED_1	R	0h	Reserved Reset Source: epwm_rst_mod_g_rst_n
6	DCBEVT1EN	R/W	0h	This bit enables the DCBEVT1.sync event to set the EPWMxSYNCO signal. 0 Disabled 1 The EPWMxSYNCO signal is pulsed for one PWM clock period upon a DCBEVT1.sync event Reset Source: epwm_rst_mod_g_rst_n
5	DCAEVT1EN	R/W	0h	This bit enables the DCAEVT1.sync event to set the EPWMxSYNCOUT signal. 0 Disabled 1 The EPWMxSYNCOUT signal is pulsed for one PWM clock period upon a DCAEVT1.sync event Reset Source: epwm_rst_mod_g_rst_n
4	CMPDEN	R/W	0h	This bit enables the TBCTR = CMPD event to set the EPWMxSYNCO signal. 0 Disabled 1 The EPWMxSYNCO signal is pulsed for one PWM clock period upon a time-base counter equal to counter compare D event [TBCTR = CMPD] Reset Source: epwm_rst_mod_g_rst_n
3	CMPCEN	R/W	0h	This bit enables the TBCTR = CMPC event to set the EPWMxSYNCO signal. 0 Disabled 1 The EPWMxSYNCO signal is pulsed for one PWM clock period upon a time-base counter equal to counter compare C event [TBCTR = CMPC] Reset Source: epwm_rst_mod_g_rst_n
2	CMPBEN	R/W	0h	This bit enables the TBCTR = CMPB event to set the EPWMxSYNCO signal. 0 Disabled 1 The EPWMxSYNCO signal is pulsed for one PWM clock period upon a time-base counter equal to counter compare B event [TBCTR = CMPB] Reset Source: epwm_rst_mod_g_rst_n
1	ZEROEN	R/W	0h	This bit enables the TBCTR = 0x0000 event to set the EPWMxSYNCOUT signal. 0 Disabled 1 The EPWMxSYNCOUT signal is pulsed for one PWM clock period upon the value of TBCTR changing to 0x0000 Reset Source: epwm_rst_mod_g_rst_n
0	SWEN	R/W	1h	This bit enables the TBCTL.SWFSYNC bit to set the EPWMxSYNCO signal. 0 Disabled 1 The EPWMxSYNCO signal is pulsed for one PWM clock period when the TBCTL.SWFSYNC bit is set Reset Source: epwm_rst_mod_g_rst_n

3.9.7 MEM_TBCTL3 Registers

3.9.7.1 MEM_TBCTL3 Register (Offset = Eh) [reset = 0h]

Short Description: Time Base Control Registe

Long Description: Time Base Control Register 3

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Table 3-693. Instance Table

Instance Name	Physical Address
CONTROLSS_EPWM0_G0	5000 000Eh
CONTROLSS_EPWM1_G0	5000 100Eh
CONTROLSS_EPWM10_G0	5000 A00Eh
CONTROLSS_EPWM11_G0	5000 B00Eh
CONTROLSS_EPWM12_G0	5000 C00Eh
CONTROLSS_EPWM13_G0	5000 D00Eh
CONTROLSS_EPWM14_G0	5000 E00Eh
CONTROLSS_EPWM15_G0	5000 F00Eh
CONTROLSS_EPWM16_G0	5001 000Eh
CONTROLSS_EPWM17_G0	5001 100Eh
CONTROLSS_EPWM18_G0	5001 200Eh
CONTROLSS_EPWM19_G0	5001 300Eh
CONTROLSS_EPWM2_G0	5000 200Eh
CONTROLSS_EPWM20_G0	5001 400Eh
CONTROLSS_EPWM21_G0	5001 500Eh
CONTROLSS_EPWM22_G0	5001 600Eh
CONTROLSS_EPWM23_G0	5001 700Eh
CONTROLSS_EPWM24_G0	5001 800Eh
CONTROLSS_EPWM25_G0	5001 900Eh
CONTROLSS_EPWM26_G0	5001 A00Eh
CONTROLSS_EPWM27_G0	5001 B00Eh
CONTROLSS_EPWM28_G0	5001 C00Eh
CONTROLSS_EPWM29_G0	5001 D00Eh
CONTROLSS_EPWM3_G0	5000 300Eh
CONTROLSS_EPWM30_G0	5001 E00Eh
CONTROLSS_EPWM31_G0	5001 F00Eh
CONTROLSS_EPWM4_G0	5000 400Eh
CONTROLSS_EPWM5_G0	5000 500Eh
CONTROLSS_EPWM6_G0	5000 600Eh
CONTROLSS_EPWM7_G0	5000 700Eh
CONTROLSS_EPWM8_G0	5000 800Eh
CONTROLSS_EPWM9_G0	5000 900Eh
CONTROLSS_EPWM0_G1	5004 000Eh
CONTROLSS_EPWM1_G1	5004 100Eh
CONTROLSS_EPWM10_G1	5004 A00Eh
CONTROLSS_EPWM11_G1	5004 B00Eh
CONTROLSS_EPWM12_G1	5004 C00Eh
CONTROLSS_EPWM13_G1	5004 D00Eh
CONTROLSS_EPWM14_G1	5004 E00Eh

Table 3-693. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM15_G1	5004 F00Eh
CONTROLSS_EPWM16_G1	5005 000Eh
CONTROLSS_EPWM17_G1	5005 100Eh
CONTROLSS_EPWM18_G1	5005 200Eh
CONTROLSS_EPWM19_G1	5005 300Eh
CONTROLSS_EPWM2_G1	5004 200Eh
CONTROLSS_EPWM20_G1	5005 400Eh
CONTROLSS_EPWM21_G1	5005 500Eh
CONTROLSS_EPWM22_G1	5005 600Eh
CONTROLSS_EPWM23_G1	5005 700Eh
CONTROLSS_EPWM24_G1	5005 800Eh
CONTROLSS_EPWM25_G1	5005 900Eh
CONTROLSS_EPWM26_G1	5005 A00Eh
CONTROLSS_EPWM27_G1	5005 B00Eh
CONTROLSS_EPWM28_G1	5005 C00Eh
CONTROLSS_EPWM29_G1	5005 D00Eh
CONTROLSS_EPWM3_G1	5004 300Eh
CONTROLSS_EPWM30_G1	5005 E00Eh
CONTROLSS_EPWM31_G1	5005 F00Eh
CONTROLSS_EPWM4_G1	5004 400Eh
CONTROLSS_EPWM5_G1	5004 500Eh
CONTROLSS_EPWM6_G1	5004 600Eh
CONTROLSS_EPWM7_G1	5004 700Eh
CONTROLSS_EPWM8_G1	5004 800Eh
CONTROLSS_EPWM9_G1	5004 900Eh
CONTROLSS_EPWM0_G2	5008 000Eh
CONTROLSS_EPWM1_G2	5008 100Eh
CONTROLSS_EPWM10_G2	5008 A00Eh
CONTROLSS_EPWM11_G2	5008 B00Eh
CONTROLSS_EPWM12_G2	5008 C00Eh
CONTROLSS_EPWM13_G2	5008 D00Eh
CONTROLSS_EPWM14_G2	5008 E00Eh
CONTROLSS_EPWM15_G2	5008 F00Eh
CONTROLSS_EPWM16_G2	5009 000Eh
CONTROLSS_EPWM17_G2	5009 100Eh
CONTROLSS_EPWM18_G2	5009 200Eh
CONTROLSS_EPWM19_G2	5009 300Eh
CONTROLSS_EPWM2_G2	5008 200Eh
CONTROLSS_EPWM20_G2	5009 400Eh
CONTROLSS_EPWM21_G2	5009 500Eh
CONTROLSS_EPWM22_G2	5009 600Eh
CONTROLSS_EPWM23_G2	5009 700Eh
CONTROLSS_EPWM24_G2	5009 800Eh
CONTROLSS_EPWM25_G2	5009 900Eh
CONTROLSS_EPWM26_G2	5009 A00Eh
CONTROLSS_EPWM27_G2	5009 B00Eh
CONTROLSS_EPWM28_G2	5009 C00Eh

Table 3-693. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM29_G2	5009 D00Eh
CONTROLSS_EPWM3_G2	5008 300Eh
CONTROLSS_EPWM30_G2	5009 E00Eh
CONTROLSS_EPWM31_G2	5009 F00Eh
CONTROLSS_EPWM4_G2	5008 400Eh
CONTROLSS_EPWM5_G2	5008 500Eh
CONTROLSS_EPWM6_G2	5008 600Eh
CONTROLSS_EPWM7_G2	5008 700Eh
CONTROLSS_EPWM8_G2	5008 800Eh
CONTROLSS_EPWM9_G2	5008 900Eh
CONTROLSS_EPWM0_G3	500C 000Eh
CONTROLSS_EPWM1_G3	500C 100Eh
CONTROLSS_EPWM10_G3	500C A00Eh
CONTROLSS_EPWM11_G3	500C B00Eh
CONTROLSS_EPWM12_G3	500C C00Eh
CONTROLSS_EPWM13_G3	500C D00Eh
CONTROLSS_EPWM14_G3	500C E00Eh
CONTROLSS_EPWM15_G3	500C F00Eh
CONTROLSS_EPWM16_G3	500D 000Eh
CONTROLSS_EPWM17_G3	500D 100Eh
CONTROLSS_EPWM18_G3	500D 200Eh
CONTROLSS_EPWM19_G3	500D 300Eh
CONTROLSS_EPWM2_G3	500C 200Eh
CONTROLSS_EPWM20_G3	500D 400Eh
CONTROLSS_EPWM21_G3	500D 500Eh
CONTROLSS_EPWM22_G3	500D 600Eh
CONTROLSS_EPWM23_G3	500D 700Eh
CONTROLSS_EPWM24_G3	500D 800Eh
CONTROLSS_EPWM25_G3	500D 900Eh
CONTROLSS_EPWM26_G3	500D A00Eh
CONTROLSS_EPWM27_G3	500D B00Eh
CONTROLSS_EPWM28_G3	500D C00Eh
CONTROLSS_EPWM29_G3	500D D00Eh
CONTROLSS_EPWM3_G3	500C 300Eh
CONTROLSS_EPWM30_G3	500D E00Eh
CONTROLSS_EPWM31_G3	500D F00Eh
CONTROLSS_EPWM4_G3	500C 400Eh
CONTROLSS_EPWM5_G3	500C 500Eh
CONTROLSS_EPWM6_G3	500C 600Eh
CONTROLSS_EPWM7_G3	500C 700Eh
CONTROLSS_EPWM8_G3	500C 800Eh
CONTROLSS_EPWM9_G3	500C 900Eh

Figure 3-293. TBCTL3 Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							

Figure 3-293. TBCTL3 Name Register (continued)

0h							
7	6	5	4	3	2	1	0
RESERVED_1							OSSFRCEN
R							R/W
0h							0h

Access Types Legend

Table 3-694. TBCTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	RESERVED_1	R	0h	Reserved Reset Source: epwm_rst_mod_g_rst_n
0	OSSFRCEN	R/W	0h	This bit determines which bit sets the EPWMxSYNCOUT One Shot Latch. 0 TBCTL2[OSHTSYNC] sets the One Shot Latch 1 GLDCTL2[OSHTLD] sets the One Shot Latch Reset Source: epwm_rst_mod_g_rst_n

3.9.8 MEM_CMPCTL Registers

3.9.8.1 MEM_CMPCTL Register (Offset = 10h) [reset = 0h]

Short Description: Counter Compare Control R

Long Description: Counter Compare Control Register

Return to Summary Table

Table 3-695. Instance Table

Instance Name	Physical Address
CONTROLSS_EPWM0_G0	5000 0010h
CONTROLSS_EPWM1_G0	5000 1010h
CONTROLSS_EPWM10_G0	5000 A010h
CONTROLSS_EPWM11_G0	5000 B010h
CONTROLSS_EPWM12_G0	5000 C010h
CONTROLSS_EPWM13_G0	5000 D010h
CONTROLSS_EPWM14_G0	5000 E010h
CONTROLSS_EPWM15_G0	5000 F010h
CONTROLSS_EPWM16_G0	5001 0010h
CONTROLSS_EPWM17_G0	5001 1010h
CONTROLSS_EPWM18_G0	5001 2010h
CONTROLSS_EPWM19_G0	5001 3010h
CONTROLSS_EPWM2_G0	5000 2010h
CONTROLSS_EPWM20_G0	5001 4010h
CONTROLSS_EPWM21_G0	5001 5010h
CONTROLSS_EPWM22_G0	5001 6010h
CONTROLSS_EPWM23_G0	5001 7010h
CONTROLSS_EPWM24_G0	5001 8010h
CONTROLSS_EPWM25_G0	5001 9010h
CONTROLSS_EPWM26_G0	5001 A010h
CONTROLSS_EPWM27_G0	5001 B010h
CONTROLSS_EPWM28_G0	5001 C010h
CONTROLSS_EPWM29_G0	5001 D010h
CONTROLSS_EPWM3_G0	5000 3010h
CONTROLSS_EPWM30_G0	5001 E010h
CONTROLSS_EPWM31_G0	5001 F010h
CONTROLSS_EPWM4_G0	5000 4010h
CONTROLSS_EPWM5_G0	5000 5010h
CONTROLSS_EPWM6_G0	5000 6010h
CONTROLSS_EPWM7_G0	5000 7010h
CONTROLSS_EPWM8_G0	5000 8010h
CONTROLSS_EPWM9_G0	5000 9010h
CONTROLSS_EPWM0_G1	5004 0010h
CONTROLSS_EPWM1_G1	5004 1010h
CONTROLSS_EPWM10_G1	5004 A010h
CONTROLSS_EPWM11_G1	5004 B010h
CONTROLSS_EPWM12_G1	5004 C010h
CONTROLSS_EPWM13_G1	5004 D010h
CONTROLSS_EPWM14_G1	5004 E010h

Table 3-695. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM15_G1	5004 F010h
CONTROLSS_EPWM16_G1	5005 0010h
CONTROLSS_EPWM17_G1	5005 1010h
CONTROLSS_EPWM18_G1	5005 2010h
CONTROLSS_EPWM19_G1	5005 3010h
CONTROLSS_EPWM2_G1	5004 2010h
CONTROLSS_EPWM20_G1	5005 4010h
CONTROLSS_EPWM21_G1	5005 5010h
CONTROLSS_EPWM22_G1	5005 6010h
CONTROLSS_EPWM23_G1	5005 7010h
CONTROLSS_EPWM24_G1	5005 8010h
CONTROLSS_EPWM25_G1	5005 9010h
CONTROLSS_EPWM26_G1	5005 A010h
CONTROLSS_EPWM27_G1	5005 B010h
CONTROLSS_EPWM28_G1	5005 C010h
CONTROLSS_EPWM29_G1	5005 D010h
CONTROLSS_EPWM3_G1	5004 3010h
CONTROLSS_EPWM30_G1	5005 E010h
CONTROLSS_EPWM31_G1	5005 F010h
CONTROLSS_EPWM4_G1	5004 4010h
CONTROLSS_EPWM5_G1	5004 5010h
CONTROLSS_EPWM6_G1	5004 6010h
CONTROLSS_EPWM7_G1	5004 7010h
CONTROLSS_EPWM8_G1	5004 8010h
CONTROLSS_EPWM9_G1	5004 9010h
CONTROLSS_EPWM0_G2	5008 0010h
CONTROLSS_EPWM1_G2	5008 1010h
CONTROLSS_EPWM10_G2	5008 A010h
CONTROLSS_EPWM11_G2	5008 B010h
CONTROLSS_EPWM12_G2	5008 C010h
CONTROLSS_EPWM13_G2	5008 D010h
CONTROLSS_EPWM14_G2	5008 E010h
CONTROLSS_EPWM15_G2	5008 F010h
CONTROLSS_EPWM16_G2	5009 0010h
CONTROLSS_EPWM17_G2	5009 1010h
CONTROLSS_EPWM18_G2	5009 2010h
CONTROLSS_EPWM19_G2	5009 3010h
CONTROLSS_EPWM2_G2	5008 2010h
CONTROLSS_EPWM20_G2	5009 4010h
CONTROLSS_EPWM21_G2	5009 5010h
CONTROLSS_EPWM22_G2	5009 6010h
CONTROLSS_EPWM23_G2	5009 7010h
CONTROLSS_EPWM24_G2	5009 8010h
CONTROLSS_EPWM25_G2	5009 9010h
CONTROLSS_EPWM26_G2	5009 A010h
CONTROLSS_EPWM27_G2	5009 B010h
CONTROLSS_EPWM28_G2	5009 C010h

Table 3-695. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM29_G2	5009 D010h
CONTROLSS_EPWM3_G2	5008 3010h
CONTROLSS_EPWM30_G2	5009 E010h
CONTROLSS_EPWM31_G2	5009 F010h
CONTROLSS_EPWM4_G2	5008 4010h
CONTROLSS_EPWM5_G2	5008 5010h
CONTROLSS_EPWM6_G2	5008 6010h
CONTROLSS_EPWM7_G2	5008 7010h
CONTROLSS_EPWM8_G2	5008 8010h
CONTROLSS_EPWM9_G2	5008 9010h
CONTROLSS_EPWM0_G3	500C 0010h
CONTROLSS_EPWM1_G3	500C 1010h
CONTROLSS_EPWM10_G3	500C A010h
CONTROLSS_EPWM11_G3	500C B010h
CONTROLSS_EPWM12_G3	500C C010h
CONTROLSS_EPWM13_G3	500C D010h
CONTROLSS_EPWM14_G3	500C E010h
CONTROLSS_EPWM15_G3	500C F010h
CONTROLSS_EPWM16_G3	500D 0010h
CONTROLSS_EPWM17_G3	500D 1010h
CONTROLSS_EPWM18_G3	500D 2010h
CONTROLSS_EPWM19_G3	500D 3010h
CONTROLSS_EPWM2_G3	500C 2010h
CONTROLSS_EPWM20_G3	500D 4010h
CONTROLSS_EPWM21_G3	500D 5010h
CONTROLSS_EPWM22_G3	500D 6010h
CONTROLSS_EPWM23_G3	500D 7010h
CONTROLSS_EPWM24_G3	500D 8010h
CONTROLSS_EPWM25_G3	500D 9010h
CONTROLSS_EPWM26_G3	500D A010h
CONTROLSS_EPWM27_G3	500D B010h
CONTROLSS_EPWM28_G3	500D C010h
CONTROLSS_EPWM29_G3	500D D010h
CONTROLSS_EPWM3_G3	500C 3010h
CONTROLSS_EPWM30_G3	500D E010h
CONTROLSS_EPWM31_G3	500D F010h
CONTROLSS_EPWM4_G3	500C 4010h
CONTROLSS_EPWM5_G3	500C 5010h
CONTROLSS_EPWM6_G3	500C 6010h
CONTROLSS_EPWM7_G3	500C 7010h
CONTROLSS_EPWM8_G3	500C 8010h
CONTROLSS_EPWM9_G3	500C 9010h

Figure 3-294. CMPCTL Name Register

15	14	13	12	11	10	9	8
LINKDUTYHR	RESERVED_3	LOADBSYNC		LOADASYNC		SHDWBFULL	SHDWAFULL
R/W	R	R/W		R/W		R	R

Figure 3-294. CMPCTL Name Register (continued)

0h	0h	0h		0h		0h	0h
7	6	5	4	3	2	1	0
RESERVED_2	SHDWBMODE	RESERVED_1	SHDWAMODE	LOADBMODE		LOADAMODE	
R	R/W	R	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	

Access Types Legend

Table 3-696. CMPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	LINKDUTYHR	R/W	0h	CMPAHR, CMPBHR Register Linking: 0 PWMA and PWMB outputs generated independently and CMPAHR, CMPBHR are independent values as on Type-4 1 When this bit is set CMPBHR assumes the same value as CMPAHR. This is typically used in complimentary PWM output generation [Section 7 details of the operation] Reset Source: epwm_rst_mod_g_rst_n
14	RESERVED_3	R	0h	Reserved Reset Source: epwm_rst_mod_g_rst_n
13:12	LOADBSYNC	R/W	0h	Shadow to Active CMPB Register Load on SYNC event 00: Shadow to Active Load of CMPB:CMPBHR occurs according to LOADBMODE [bits 1,0] [same as legacy] 01: Shadow to Active Load of CMPB:CMPBHR occurs both according to LOADBMODE bits and when SYNC occurs 10: Shadow to Active Load of CMPB:CMPBHR occurs only when a SYNC is received 11: Reserved Note: This bit is valid only if CMPCTL[SHDWBMODE] = 0. Reset Source: epwm_rst_mod_g_rst_n
11:10	LOADASYNC	R/W	0h	Shadow to Active CMPA Register Load on SYNC event 00: Shadow to Active Load of CMPA:CMPAHR occurs according to LOADAMODE [bits 1,0] [same as legacy] 01: Shadow to Active Load of CMPA:CMPAHR occurs both according to LOADAMODE bits and when SYNC occurs 10: Shadow to Active Load of CMPA:CMPAHR occurs only when a SYNC is received 11: Reserved Note: This bit is valid only if CMPCTL[SHDWAMODE] = 0. Reset Source: epwm_rst_mod_g_rst_n
9	SHDWBFULL	R	0h	Counter-compare B [CMPB] Shadow Register Full Status Flag This bit self clears once a loadstrobe occurs. 0: CMPB shadow FIFO not full yet 1: Indicates the CMPB shadow FIFO is full a CPU write will overwrite current shadow value Reset Source: epwm_rst_mod_g_rst_n
8	SHDWAFULL	R	0h	Counter-compare A [CMPA] Shadow Register Full Status Flag The flag bit is set when a 32-bit write to CMPA:CMPAHR register or a 16-bit write to CMPA register is made. A 16-bit write to CMPAHR register will not affect the flag. This bit self clears once a load-strobe occurs. 0: CMPA shadow FIFO not full yet 1: Indicates the CMPA shadow FIFO is full, a CPU write will overwrite the current shadow value Reset Source: epwm_rst_mod_g_rst_n
7	RESERVED_2	R	0h	Reserved Reset Source: epwm_rst_mod_g_rst_n
6	SHDWBMODE	R/W	0h	Counter-compare B [CMPB] Register Operating Mode 0: Shadow mode. Operates as a double buffer. All writes via the CPU access the shadow register 1: Immediate mode. Only the active compare B register is used. All writes and reads directly access the active register for immediate compare action Reset Source: epwm_rst_mod_g_rst_n
5	RESERVED_1	R	0h	Reserved Reset Source: epwm_rst_mod_g_rst_n
4	SHDWAMODE	R/W	0h	Counter-compare A [CMPA] Register Operating Mode 0: Shadow mode. Operates as a double buffer. All writes via the CPU access the shadow register 1: Immediate mode. Only the active compare register is used. All writes and reads directly access the active register for immediate compare action Reset Source: epwm_rst_mod_g_rst_n

Table 3-696. CMPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	LOADBMODE	R/W	0h	Active Counter-Compare B [CMPB] Load From Shadow Select Mode This bit has no effect in immediate mode [CMPCTL[SHDWBMODE] = 1]. 00: Load on CTR = Zero: Time-base counter equal to zero [TBCTR = 0x0000] 01: Load on CTR = PRD: Time-base counter equal to period [TBCTR = TBPRD] 10: Load on either CTR = Zero or CTR = PRD 11: Freeze [no loads possible] Reset Source: epwm_rst_mod_g_rst_n
1:0	LOADAMODE	R/W	0h	Active Counter-Compare A [CMPA] Load From Shadow Select Mode This bit has no effect in immediate mode [CMPCTL[SHDWAMODE] = 1]. 00: Load on CTR = Zero: Time-base counter equal to zero [TBCTR = 0x0000] 01: Load on CTR = PRD: Time-base counter equal to period [TBCTR = TBPRD] 10: Load on either CTR = Zero or CTR = PRD 11: Freeze [no loads possible] Reset Source: epwm_rst_mod_g_rst_n

3.9.9 MEM_CMPCTL2 Registers

3.9.9.1 MEM_CMPCTL2 Register (Offset = 12h) [reset = 0h]

Short Description: Counter Compare Control R

Long Description: Counter Compare Control Register 2

Return to Summary Table

Table 3-697. Instance Table

Instance Name	Physical Address
CONTROLSS_EPWM0_G0	5000 0012h
CONTROLSS_EPWM1_G0	5000 1012h
CONTROLSS_EPWM10_G0	5000 A012h
CONTROLSS_EPWM11_G0	5000 B012h
CONTROLSS_EPWM12_G0	5000 C012h
CONTROLSS_EPWM13_G0	5000 D012h
CONTROLSS_EPWM14_G0	5000 E012h
CONTROLSS_EPWM15_G0	5000 F012h
CONTROLSS_EPWM16_G0	5001 0012h
CONTROLSS_EPWM17_G0	5001 1012h
CONTROLSS_EPWM18_G0	5001 2012h
CONTROLSS_EPWM19_G0	5001 3012h
CONTROLSS_EPWM2_G0	5000 2012h
CONTROLSS_EPWM20_G0	5001 4012h
CONTROLSS_EPWM21_G0	5001 5012h
CONTROLSS_EPWM22_G0	5001 6012h
CONTROLSS_EPWM23_G0	5001 7012h
CONTROLSS_EPWM24_G0	5001 8012h
CONTROLSS_EPWM25_G0	5001 9012h
CONTROLSS_EPWM26_G0	5001 A012h
CONTROLSS_EPWM27_G0	5001 B012h
CONTROLSS_EPWM28_G0	5001 C012h
CONTROLSS_EPWM29_G0	5001 D012h
CONTROLSS_EPWM3_G0	5000 3012h
CONTROLSS_EPWM30_G0	5001 E012h
CONTROLSS_EPWM31_G0	5001 F012h
CONTROLSS_EPWM4_G0	5000 4012h
CONTROLSS_EPWM5_G0	5000 5012h
CONTROLSS_EPWM6_G0	5000 6012h
CONTROLSS_EPWM7_G0	5000 7012h
CONTROLSS_EPWM8_G0	5000 8012h
CONTROLSS_EPWM9_G0	5000 9012h
CONTROLSS_EPWM0_G1	5004 0012h
CONTROLSS_EPWM1_G1	5004 1012h
CONTROLSS_EPWM10_G1	5004 A012h
CONTROLSS_EPWM11_G1	5004 B012h
CONTROLSS_EPWM12_G1	5004 C012h
CONTROLSS_EPWM13_G1	5004 D012h
CONTROLSS_EPWM14_G1	5004 E012h

Table 3-697. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM15_G1	5004 F012h
CONTROLSS_EPWM16_G1	5005 0012h
CONTROLSS_EPWM17_G1	5005 1012h
CONTROLSS_EPWM18_G1	5005 2012h
CONTROLSS_EPWM19_G1	5005 3012h
CONTROLSS_EPWM2_G1	5004 2012h
CONTROLSS_EPWM20_G1	5005 4012h
CONTROLSS_EPWM21_G1	5005 5012h
CONTROLSS_EPWM22_G1	5005 6012h
CONTROLSS_EPWM23_G1	5005 7012h
CONTROLSS_EPWM24_G1	5005 8012h
CONTROLSS_EPWM25_G1	5005 9012h
CONTROLSS_EPWM26_G1	5005 A012h
CONTROLSS_EPWM27_G1	5005 B012h
CONTROLSS_EPWM28_G1	5005 C012h
CONTROLSS_EPWM29_G1	5005 D012h
CONTROLSS_EPWM3_G1	5004 3012h
CONTROLSS_EPWM30_G1	5005 E012h
CONTROLSS_EPWM31_G1	5005 F012h
CONTROLSS_EPWM4_G1	5004 4012h
CONTROLSS_EPWM5_G1	5004 5012h
CONTROLSS_EPWM6_G1	5004 6012h
CONTROLSS_EPWM7_G1	5004 7012h
CONTROLSS_EPWM8_G1	5004 8012h
CONTROLSS_EPWM9_G1	5004 9012h
CONTROLSS_EPWM0_G2	5008 0012h
CONTROLSS_EPWM1_G2	5008 1012h
CONTROLSS_EPWM10_G2	5008 A012h
CONTROLSS_EPWM11_G2	5008 B012h
CONTROLSS_EPWM12_G2	5008 C012h
CONTROLSS_EPWM13_G2	5008 D012h
CONTROLSS_EPWM14_G2	5008 E012h
CONTROLSS_EPWM15_G2	5008 F012h
CONTROLSS_EPWM16_G2	5009 0012h
CONTROLSS_EPWM17_G2	5009 1012h
CONTROLSS_EPWM18_G2	5009 2012h
CONTROLSS_EPWM19_G2	5009 3012h
CONTROLSS_EPWM2_G2	5008 2012h
CONTROLSS_EPWM20_G2	5009 4012h
CONTROLSS_EPWM21_G2	5009 5012h
CONTROLSS_EPWM22_G2	5009 6012h
CONTROLSS_EPWM23_G2	5009 7012h
CONTROLSS_EPWM24_G2	5009 8012h
CONTROLSS_EPWM25_G2	5009 9012h
CONTROLSS_EPWM26_G2	5009 A012h
CONTROLSS_EPWM27_G2	5009 B012h
CONTROLSS_EPWM28_G2	5009 C012h

Table 3-697. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM29_G2	5009 D012h
CONTROLSS_EPWM3_G2	5008 3012h
CONTROLSS_EPWM30_G2	5009 E012h
CONTROLSS_EPWM31_G2	5009 F012h
CONTROLSS_EPWM4_G2	5008 4012h
CONTROLSS_EPWM5_G2	5008 5012h
CONTROLSS_EPWM6_G2	5008 6012h
CONTROLSS_EPWM7_G2	5008 7012h
CONTROLSS_EPWM8_G2	5008 8012h
CONTROLSS_EPWM9_G2	5008 9012h
CONTROLSS_EPWM0_G3	500C 0012h
CONTROLSS_EPWM1_G3	500C 1012h
CONTROLSS_EPWM10_G3	500C A012h
CONTROLSS_EPWM11_G3	500C B012h
CONTROLSS_EPWM12_G3	500C C012h
CONTROLSS_EPWM13_G3	500C D012h
CONTROLSS_EPWM14_G3	500C E012h
CONTROLSS_EPWM15_G3	500C F012h
CONTROLSS_EPWM16_G3	500D 0012h
CONTROLSS_EPWM17_G3	500D 1012h
CONTROLSS_EPWM18_G3	500D 2012h
CONTROLSS_EPWM19_G3	500D 3012h
CONTROLSS_EPWM2_G3	500C 2012h
CONTROLSS_EPWM20_G3	500D 4012h
CONTROLSS_EPWM21_G3	500D 5012h
CONTROLSS_EPWM22_G3	500D 6012h
CONTROLSS_EPWM23_G3	500D 7012h
CONTROLSS_EPWM24_G3	500D 8012h
CONTROLSS_EPWM25_G3	500D 9012h
CONTROLSS_EPWM26_G3	500D A012h
CONTROLSS_EPWM27_G3	500D B012h
CONTROLSS_EPWM28_G3	500D C012h
CONTROLSS_EPWM29_G3	500D D012h
CONTROLSS_EPWM3_G3	500C 3012h
CONTROLSS_EPWM30_G3	500D E012h
CONTROLSS_EPWM31_G3	500D F012h
CONTROLSS_EPWM4_G3	500C 4012h
CONTROLSS_EPWM5_G3	500C 5012h
CONTROLSS_EPWM6_G3	500C 6012h
CONTROLSS_EPWM7_G3	500C 7012h
CONTROLSS_EPWM8_G3	500C 8012h
CONTROLSS_EPWM9_G3	500C 9012h

Figure 3-295. CMPCTL2 Name Register

15	14	13	12	11	10	9	8
RESERVED_3		LOADDSYNC		LOADCSYNC		RESERVED_2	
R		R/W		R/W		R	

Figure 3-295. CMPCTL2 Name Register (continued)

0h		0h		0h		0h	
7	6	5	4	3	2	1	0
RESERVED_2	SHDWDMODE	RESERVED_1	SHDWCMODE	LOADDMODE		LOADCMODE	
R	R/W	R	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	

Access Types Legend

Table 3-698. CMPCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED_3	R	0h	Reserved Reset Source: epwm_rst_mod_g_rst_n
13:12	LOADDSYNC	R/W	0h	Shadow to Active CMPD Register Load on SYNC event 00: Shadow to Active Load of CMPD occurs according to LOADDMODE 01: Shadow to Active Load of CMPD occurs both according to LOADDMODE bits and when SYNC occurs 10: Shadow to Active Load of CMPD occurs only when a SYNC is received 11: Reserved Note: This bit is valid only if CMPCTL2[SHDWDMODE] = 0. Reset Source: epwm_rst_mod_g_rst_n
11:10	LOADCSYNC	R/W	0h	Shadow to Active CMPC Register Load on SYNC event 00: Shadow to Active Load of CMPC occurs according to LOADCMODE 01: Shadow to Active Load of CMPC occurs both according to LOADCMODE bits and when SYNC occurs 10: Shadow to Active Load of CMPC occurs only when a SYNC is received 11: Reserved Note: This bit is valid only if CMPCTL2[SHDWCMODE] = 0. Reset Source: epwm_rst_mod_g_rst_n
9:7	RESERVED_2	R	0h	Reserved Reset Source: epwm_rst_mod_g_rst_n
6	SHDWDMODE	R/W	0h	Counter-Compare D Register Operating Mode 0: Shadow mode - operates as a double buffer. All writes via the CPU access Shadow register. 1: Immediate mode - only the Active compare register is used. All writes/reads via the CPU directly access the Active register for immediate Compare action. Reset Source: epwm_rst_mod_g_rst_n
5	RESERVED_1	R	0h	Reserved Reset Source: epwm_rst_mod_g_rst_n
4	SHDWCMODE	R/W	0h	Counter-Compare C Register Operating Mode 0: Shadow mode - operates as a double buffer. All writes via the CPU access Shadow register. 1: Immediate mode - only the Active compare register is used. All writes/reads via the CPU directly access the Active register for immediate Compare action. Reset Source: epwm_rst_mod_g_rst_n
3:2	LOADDMODE	R/W	0h	Active Counter-Compare D [CMPD] Load from Shadow Select Mode 00: Load on CTR = Zero: Time-base counter equal to zero [TBCTR = 0x0000] 01: Load on CTR = PRD: Time-base counter equal to period [TBCTR = TBPRD] 10: Load on either CTR = Zero or CTR = PRD 11: Freeze [no loads possible] Note: Has no effect in Immediate mode. Reset Source: epwm_rst_mod_g_rst_n
1:0	LOADCMODE	R/W	0h	Active Counter-Compare C [CMPC] Load from Shadow Select Mode 00: Load on CTR = Zero: Time-base counter equal to zero [TBCTR = 0x0000] 01: Load on CTR = PRD: Time-base counter equal to period [TBCTR = TBPRD] 10: Load on either CTR = Zero or CTR = PRD 11: Freeze [no loads possible] Note: Has no effect in Immediate mode. Reset Source: epwm_rst_mod_g_rst_n

3.9.10 MEM_DBCTL Registers

3.9.10.1 MEM_DBCTL Register (Offset = 18h) [reset = 0h]

Short Description: Dead-Band Generator Contr

Long Description: Dead-Band Generator Control Register

Return to Summary Table

Table 3-699. Instance Table

Instance Name	Physical Address
CONTROLSS_EPWM0_G0	5000 0018h
CONTROLSS_EPWM1_G0	5000 1018h
CONTROLSS_EPWM10_G0	5000 A018h
CONTROLSS_EPWM11_G0	5000 B018h
CONTROLSS_EPWM12_G0	5000 C018h
CONTROLSS_EPWM13_G0	5000 D018h
CONTROLSS_EPWM14_G0	5000 E018h
CONTROLSS_EPWM15_G0	5000 F018h
CONTROLSS_EPWM16_G0	5001 0018h
CONTROLSS_EPWM17_G0	5001 1018h
CONTROLSS_EPWM18_G0	5001 2018h
CONTROLSS_EPWM19_G0	5001 3018h
CONTROLSS_EPWM2_G0	5000 2018h
CONTROLSS_EPWM20_G0	5001 4018h
CONTROLSS_EPWM21_G0	5001 5018h
CONTROLSS_EPWM22_G0	5001 6018h
CONTROLSS_EPWM23_G0	5001 7018h
CONTROLSS_EPWM24_G0	5001 8018h
CONTROLSS_EPWM25_G0	5001 9018h
CONTROLSS_EPWM26_G0	5001 A018h
CONTROLSS_EPWM27_G0	5001 B018h
CONTROLSS_EPWM28_G0	5001 C018h
CONTROLSS_EPWM29_G0	5001 D018h
CONTROLSS_EPWM3_G0	5000 3018h
CONTROLSS_EPWM30_G0	5001 E018h
CONTROLSS_EPWM31_G0	5001 F018h
CONTROLSS_EPWM4_G0	5000 4018h
CONTROLSS_EPWM5_G0	5000 5018h
CONTROLSS_EPWM6_G0	5000 6018h
CONTROLSS_EPWM7_G0	5000 7018h
CONTROLSS_EPWM8_G0	5000 8018h
CONTROLSS_EPWM9_G0	5000 9018h
CONTROLSS_EPWM0_G1	5004 0018h
CONTROLSS_EPWM1_G1	5004 1018h
CONTROLSS_EPWM10_G1	5004 A018h
CONTROLSS_EPWM11_G1	5004 B018h
CONTROLSS_EPWM12_G1	5004 C018h
CONTROLSS_EPWM13_G1	5004 D018h
CONTROLSS_EPWM14_G1	5004 E018h

Table 3-699. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM15_G1	5004 F018h
CONTROLSS_EPWM16_G1	5005 0018h
CONTROLSS_EPWM17_G1	5005 1018h
CONTROLSS_EPWM18_G1	5005 2018h
CONTROLSS_EPWM19_G1	5005 3018h
CONTROLSS_EPWM2_G1	5004 2018h
CONTROLSS_EPWM20_G1	5005 4018h
CONTROLSS_EPWM21_G1	5005 5018h
CONTROLSS_EPWM22_G1	5005 6018h
CONTROLSS_EPWM23_G1	5005 7018h
CONTROLSS_EPWM24_G1	5005 8018h
CONTROLSS_EPWM25_G1	5005 9018h
CONTROLSS_EPWM26_G1	5005 A018h
CONTROLSS_EPWM27_G1	5005 B018h
CONTROLSS_EPWM28_G1	5005 C018h
CONTROLSS_EPWM29_G1	5005 D018h
CONTROLSS_EPWM3_G1	5004 3018h
CONTROLSS_EPWM30_G1	5005 E018h
CONTROLSS_EPWM31_G1	5005 F018h
CONTROLSS_EPWM4_G1	5004 4018h
CONTROLSS_EPWM5_G1	5004 5018h
CONTROLSS_EPWM6_G1	5004 6018h
CONTROLSS_EPWM7_G1	5004 7018h
CONTROLSS_EPWM8_G1	5004 8018h
CONTROLSS_EPWM9_G1	5004 9018h
CONTROLSS_EPWM0_G2	5008 0018h
CONTROLSS_EPWM1_G2	5008 1018h
CONTROLSS_EPWM10_G2	5008 A018h
CONTROLSS_EPWM11_G2	5008 B018h
CONTROLSS_EPWM12_G2	5008 C018h
CONTROLSS_EPWM13_G2	5008 D018h
CONTROLSS_EPWM14_G2	5008 E018h
CONTROLSS_EPWM15_G2	5008 F018h
CONTROLSS_EPWM16_G2	5009 0018h
CONTROLSS_EPWM17_G2	5009 1018h
CONTROLSS_EPWM18_G2	5009 2018h
CONTROLSS_EPWM19_G2	5009 3018h
CONTROLSS_EPWM2_G2	5008 2018h
CONTROLSS_EPWM20_G2	5009 4018h
CONTROLSS_EPWM21_G2	5009 5018h
CONTROLSS_EPWM22_G2	5009 6018h
CONTROLSS_EPWM23_G2	5009 7018h
CONTROLSS_EPWM24_G2	5009 8018h
CONTROLSS_EPWM25_G2	5009 9018h
CONTROLSS_EPWM26_G2	5009 A018h
CONTROLSS_EPWM27_G2	5009 B018h
CONTROLSS_EPWM28_G2	5009 C018h

Table 3-699. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM29_G2	5009 D018h
CONTROLSS_EPWM3_G2	5008 3018h
CONTROLSS_EPWM30_G2	5009 E018h
CONTROLSS_EPWM31_G2	5009 F018h
CONTROLSS_EPWM4_G2	5008 4018h
CONTROLSS_EPWM5_G2	5008 5018h
CONTROLSS_EPWM6_G2	5008 6018h
CONTROLSS_EPWM7_G2	5008 7018h
CONTROLSS_EPWM8_G2	5008 8018h
CONTROLSS_EPWM9_G2	5008 9018h
CONTROLSS_EPWM0_G3	500C 0018h
CONTROLSS_EPWM1_G3	500C 1018h
CONTROLSS_EPWM10_G3	500C A018h
CONTROLSS_EPWM11_G3	500C B018h
CONTROLSS_EPWM12_G3	500C C018h
CONTROLSS_EPWM13_G3	500C D018h
CONTROLSS_EPWM14_G3	500C E018h
CONTROLSS_EPWM15_G3	500C F018h
CONTROLSS_EPWM16_G3	500D 0018h
CONTROLSS_EPWM17_G3	500D 1018h
CONTROLSS_EPWM18_G3	500D 2018h
CONTROLSS_EPWM19_G3	500D 3018h
CONTROLSS_EPWM2_G3	500C 2018h
CONTROLSS_EPWM20_G3	500D 4018h
CONTROLSS_EPWM21_G3	500D 5018h
CONTROLSS_EPWM22_G3	500D 6018h
CONTROLSS_EPWM23_G3	500D 7018h
CONTROLSS_EPWM24_G3	500D 8018h
CONTROLSS_EPWM25_G3	500D 9018h
CONTROLSS_EPWM26_G3	500D A018h
CONTROLSS_EPWM27_G3	500D B018h
CONTROLSS_EPWM28_G3	500D C018h
CONTROLSS_EPWM29_G3	500D D018h
CONTROLSS_EPWM3_G3	500C 3018h
CONTROLSS_EPWM30_G3	500D E018h
CONTROLSS_EPWM31_G3	500D F018h
CONTROLSS_EPWM4_G3	500C 4018h
CONTROLSS_EPWM5_G3	500C 5018h
CONTROLSS_EPWM6_G3	500C 6018h
CONTROLSS_EPWM7_G3	500C 7018h
CONTROLSS_EPWM8_G3	500C 8018h
CONTROLSS_EPWM9_G3	500C 9018h

Figure 3-296. DBCTL Name Register

15	14	13	12	11	10	9	8
HALFCYCLE	DEDB_MODE	OUTSWAP		SHDWDBFED MODE	SHDWDBRED MODE	LOADFEDMODE	

Figure 3-296. DBCTL Name Register (continued)

R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
LOADREDMODE		IN_MODE		POLSEL		OUT_MODE	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	

Access Types Legend

Table 3-700. DBCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	HALFCYCLE	R/W	0h	Half Cycle Clocking Enable Bit 0: Full cycle clocking enabled. The dead-band counters are clocked at the TBCLK rate. 1: Half cycle clocking enabled. The dead-band counters are clocked at TBCLK*2. Reset Source: epwm_rst_mod_g_rst_n
14	DEDB_MODE	R/W	0h	Dead Band Dual-Edge B Mode Control [S8 switch] 0: Rising edge delay applied to InA/InB as selected by S4 switch [IN-MODE bits] on A signal path only. Falling edge delay applied to InA/InB as selected by S5 switch [INMODE bits] on B signal path only. 1: Rising edge delay and falling edge delay applied to source selected by S4 switch [INMODE bits] and output to B signal path only. Note: When this bit is set to 1, user should always either set OUT_MODE bits such that Apath = InA OR OUTSWAP bits such that OutA=Bpath otherwise, OutA will be invalid. Reset Source: epwm_rst_mod_g_rst_n
13:12	OUTSWAP	R/W	0h	Dead Band Output Swap Control Bit 13 controls the S6 switch and bit 12 controls the S7 switch. 00: OutA and OutB signals are as defined by OUT-MODE bits. 01: OutA = A-path as defined by OUT-MODE bits. OutB = A-path as defined by OUT-MODE bits [rising edge delay or delay-bypassed A signal path]. 10: OutA = B-path as defined by OUT-MODE bits [falling edge delay or delay-bypassed B signal path]. OutB = B-path as defined by OUT-MODE bits. 11: OutA = B-path as defined by OUT-MODE bits [falling edge delay or delay-bypassed B signal path]. OutB = A-path as defined by OUT-MODE bits [rising edge delay or delay-bypassed A signal path]. Reset Source: epwm_rst_mod_g_rst_n
11	SHDWDBFEDMODE	R/W	0h	FED Dead-Band Load Mode 0: Immediate mode. Only the active DBFED register is used. All writes/reads via the CPU directly access the active register for immediate "FED dead-band action." 1: Shadow mode. Operates as a double buffer. All writes via the CPU access Shadow register. Default at Reset is Immediate mode [for compatibility with legacy]. Reset Source: epwm_rst_mod_g_rst_n
10	SHDWDBREDMODE	R/W	0h	RED Dead-Band Load Mode 0: Immediate mode. Only the active DBRED register is used. All writes/reads via the CPU directly access the active register for immediate "RED dead-band action." 1: Shadow mode. Operates as a double buffer. All writes via the CPU access Shadow register. Default at Reset is Immediate mode [for compatibility with legacy]. Reset Source: epwm_rst_mod_g_rst_n
9:8	LOADFEDMODE	R/W	0h	Active DBFED Load from Shadow Select Mode 00: Load on Counter = 0 [CNT_eq] 01: Load on Counter = Period [PRD_eq] 10: Load on either Counter = 0, or Counter = Period 11: Freeze [no loads possible] Note: has no effect in Immediate mode. Reset Source: epwm_rst_mod_g_rst_n
7:6	LOADREDMODE	R/W	0h	Active DBRED Load from Shadow Select Mode 00: Load on Counter = 0 [CNT_eq] 01: Load on Counter = Period [PRD_eq] 10: Load on either Counter = 0, or Counter = Period 11: Freeze [no loads possible] Note: has no effect in Immediate mode. Reset Source: epwm_rst_mod_g_rst_n

Table 3-700. DBCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	IN_MODE	R/W	0h	Dead-Band Input Mode Control Bit 5 controls the S5 switch and bit 4 controls the S4 switch shown. This allows you to select the input source to the falling-edge and rising-edge delay. To produce classical dead-band waveforms the default is EPWMxA In is the source for both falling and rising-edge delays. 00: EPWMxA In [from the action-qualifier] is the source for both falling-edge and rising-edge delay. 01: EPWMxB In [from the action-qualifier] is the source for rising-edge delayed signal. EPWMxA In [from the action-qualifier] is the source for falling-edge delayed signal. 10: EPWMxA In [from the action-qualifier] is the source for rising-edge delayed signal. EPWMxB In [from the action-qualifier] is the source for falling-edge delayed signal. 11: EPWMxB In [from the action-qualifier] is the source for both rising-edge delay and falling-edge delayed signal. Reset Source: epwm_rst_mod_g_rst_n
3:2	POLSEL	R/W	0h	Polarity Select Control Bit 3 controls the S3 switch and bit 2 controls the S2 switch. This allows you to selectively invert one of the delayed signals before it is sent out of the dead-band submodule. The following descriptions correspond to classical upper/lower switch control as found in one leg of a digital motor control inverter. These assume that DBCTL[OUT_MODE] = 1,1 and DBCTL[IN_MODE] = 0x0. Other enhanced modes are also possible, but not regarded as typical usage modes. 00: Active high [AH] mode. Neither EPWMxA nor EPWMxB is inverted [default]. 01: Active low complementary [ALC] mode. EPWMxA is inverted. 10: Active high complementary [AHC]. EPWMxB is inverted. 11: Active low [AL] mode. Both EPWMxA and EPWMxB are inverted. Reset Source: epwm_rst_mod_g_rst_n
1:0	OUT_MODE	R/W	0h	Dead-Band Output Mode Control Bit 1 controls the S1 switch and bit 0 controls the S0 switch. 00: DBM is fully disabled or by-passed. In this mode the POLSEL and IN-MODE bits have no effect. 01: Apath = InA [delay is by-passed for A signal path] Bpath = FED [Falling Edge Delay in B signal path] 10: Apath = RED [Rising Edge Delay in A signal path] Bpath = InB [delay is by-passed for B signal path] 11: DBM is fully enabled [i.e. both RED and FED active] Reset Source: epwm_rst_mod_g_rst_n

3.9.11 MEM_DBCTL2 Registers

3.9.11.1 MEM_DBCTL2 Register (Offset = 1Ah) [reset = 0h]

Short Description: Dead-Band Generator Contr

Long Description: Dead-Band Generator Control Register 2

Return to Summary Table

Table 3-701. Instance Table

Instance Name	Physical Address
CONTROLSS_EPWM0_G0	5000 001Ah
CONTROLSS_EPWM1_G0	5000 101Ah
CONTROLSS_EPWM10_G0	5000 A01Ah
CONTROLSS_EPWM11_G0	5000 B01Ah
CONTROLSS_EPWM12_G0	5000 C01Ah
CONTROLSS_EPWM13_G0	5000 D01Ah
CONTROLSS_EPWM14_G0	5000 E01Ah
CONTROLSS_EPWM15_G0	5000 F01Ah
CONTROLSS_EPWM16_G0	5001 001Ah
CONTROLSS_EPWM17_G0	5001 101Ah
CONTROLSS_EPWM18_G0	5001 201Ah
CONTROLSS_EPWM19_G0	5001 301Ah
CONTROLSS_EPWM2_G0	5000 201Ah
CONTROLSS_EPWM20_G0	5001 401Ah
CONTROLSS_EPWM21_G0	5001 501Ah
CONTROLSS_EPWM22_G0	5001 601Ah
CONTROLSS_EPWM23_G0	5001 701Ah
CONTROLSS_EPWM24_G0	5001 801Ah
CONTROLSS_EPWM25_G0	5001 901Ah
CONTROLSS_EPWM26_G0	5001 A01Ah
CONTROLSS_EPWM27_G0	5001 B01Ah
CONTROLSS_EPWM28_G0	5001 C01Ah
CONTROLSS_EPWM29_G0	5001 D01Ah
CONTROLSS_EPWM3_G0	5000 301Ah
CONTROLSS_EPWM30_G0	5001 E01Ah
CONTROLSS_EPWM31_G0	5001 F01Ah
CONTROLSS_EPWM4_G0	5000 401Ah
CONTROLSS_EPWM5_G0	5000 501Ah
CONTROLSS_EPWM6_G0	5000 601Ah
CONTROLSS_EPWM7_G0	5000 701Ah
CONTROLSS_EPWM8_G0	5000 801Ah
CONTROLSS_EPWM9_G0	5000 901Ah
CONTROLSS_EPWM0_G1	5004 001Ah
CONTROLSS_EPWM1_G1	5004 101Ah
CONTROLSS_EPWM10_G1	5004 A01Ah
CONTROLSS_EPWM11_G1	5004 B01Ah
CONTROLSS_EPWM12_G1	5004 C01Ah
CONTROLSS_EPWM13_G1	5004 D01Ah
CONTROLSS_EPWM14_G1	5004 E01Ah

Table 3-701. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM15_G1	5004 F01Ah
CONTROLSS_EPWM16_G1	5005 001Ah
CONTROLSS_EPWM17_G1	5005 101Ah
CONTROLSS_EPWM18_G1	5005 201Ah
CONTROLSS_EPWM19_G1	5005 301Ah
CONTROLSS_EPWM2_G1	5004 201Ah
CONTROLSS_EPWM20_G1	5005 401Ah
CONTROLSS_EPWM21_G1	5005 501Ah
CONTROLSS_EPWM22_G1	5005 601Ah
CONTROLSS_EPWM23_G1	5005 701Ah
CONTROLSS_EPWM24_G1	5005 801Ah
CONTROLSS_EPWM25_G1	5005 901Ah
CONTROLSS_EPWM26_G1	5005 A01Ah
CONTROLSS_EPWM27_G1	5005 B01Ah
CONTROLSS_EPWM28_G1	5005 C01Ah
CONTROLSS_EPWM29_G1	5005 D01Ah
CONTROLSS_EPWM3_G1	5004 301Ah
CONTROLSS_EPWM30_G1	5005 E01Ah
CONTROLSS_EPWM31_G1	5005 F01Ah
CONTROLSS_EPWM4_G1	5004 401Ah
CONTROLSS_EPWM5_G1	5004 501Ah
CONTROLSS_EPWM6_G1	5004 601Ah
CONTROLSS_EPWM7_G1	5004 701Ah
CONTROLSS_EPWM8_G1	5004 801Ah
CONTROLSS_EPWM9_G1	5004 901Ah
CONTROLSS_EPWM0_G2	5008 001Ah
CONTROLSS_EPWM1_G2	5008 101Ah
CONTROLSS_EPWM10_G2	5008 A01Ah
CONTROLSS_EPWM11_G2	5008 B01Ah
CONTROLSS_EPWM12_G2	5008 C01Ah
CONTROLSS_EPWM13_G2	5008 D01Ah
CONTROLSS_EPWM14_G2	5008 E01Ah
CONTROLSS_EPWM15_G2	5008 F01Ah
CONTROLSS_EPWM16_G2	5009 001Ah
CONTROLSS_EPWM17_G2	5009 101Ah
CONTROLSS_EPWM18_G2	5009 201Ah
CONTROLSS_EPWM19_G2	5009 301Ah
CONTROLSS_EPWM2_G2	5008 201Ah
CONTROLSS_EPWM20_G2	5009 401Ah
CONTROLSS_EPWM21_G2	5009 501Ah
CONTROLSS_EPWM22_G2	5009 601Ah
CONTROLSS_EPWM23_G2	5009 701Ah
CONTROLSS_EPWM24_G2	5009 801Ah
CONTROLSS_EPWM25_G2	5009 901Ah
CONTROLSS_EPWM26_G2	5009 A01Ah
CONTROLSS_EPWM27_G2	5009 B01Ah
CONTROLSS_EPWM28_G2	5009 C01Ah

Table 3-701. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM29_G2	5009 D01Ah
CONTROLSS_EPWM3_G2	5008 301Ah
CONTROLSS_EPWM30_G2	5009 E01Ah
CONTROLSS_EPWM31_G2	5009 F01Ah
CONTROLSS_EPWM4_G2	5008 401Ah
CONTROLSS_EPWM5_G2	5008 501Ah
CONTROLSS_EPWM6_G2	5008 601Ah
CONTROLSS_EPWM7_G2	5008 701Ah
CONTROLSS_EPWM8_G2	5008 801Ah
CONTROLSS_EPWM9_G2	5008 901Ah
CONTROLSS_EPWM0_G3	500C 001Ah
CONTROLSS_EPWM1_G3	500C 101Ah
CONTROLSS_EPWM10_G3	500C A01Ah
CONTROLSS_EPWM11_G3	500C B01Ah
CONTROLSS_EPWM12_G3	500C C01Ah
CONTROLSS_EPWM13_G3	500C D01Ah
CONTROLSS_EPWM14_G3	500C E01Ah
CONTROLSS_EPWM15_G3	500C F01Ah
CONTROLSS_EPWM16_G3	500D 001Ah
CONTROLSS_EPWM17_G3	500D 101Ah
CONTROLSS_EPWM18_G3	500D 201Ah
CONTROLSS_EPWM19_G3	500D 301Ah
CONTROLSS_EPWM2_G3	500C 201Ah
CONTROLSS_EPWM20_G3	500D 401Ah
CONTROLSS_EPWM21_G3	500D 501Ah
CONTROLSS_EPWM22_G3	500D 601Ah
CONTROLSS_EPWM23_G3	500D 701Ah
CONTROLSS_EPWM24_G3	500D 801Ah
CONTROLSS_EPWM25_G3	500D 901Ah
CONTROLSS_EPWM26_G3	500D A01Ah
CONTROLSS_EPWM27_G3	500D B01Ah
CONTROLSS_EPWM28_G3	500D C01Ah
CONTROLSS_EPWM29_G3	500D D01Ah
CONTROLSS_EPWM3_G3	500C 301Ah
CONTROLSS_EPWM30_G3	500D E01Ah
CONTROLSS_EPWM31_G3	500D F01Ah
CONTROLSS_EPWM4_G3	500C 401Ah
CONTROLSS_EPWM5_G3	500C 501Ah
CONTROLSS_EPWM6_G3	500C 601Ah
CONTROLSS_EPWM7_G3	500C 701Ah
CONTROLSS_EPWM8_G3	500C 801Ah
CONTROLSS_EPWM9_G3	500C 901Ah

Figure 3-297. DBCTL2 Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							

Figure 3-297. DBCTL2 Name Register (continued)

0h							
7	6	5	4	3	2	1	0
RESERVED_1					SHDWDBCTLMODE	LOADDBCTLMODE	
R					R/W	R/W	
0h					0h	0h	

Access Types Legend

Table 3-702. DBCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:3	RESERVED_1	R	0h	Reserved Reset Source: epwm_rst_mod_g_rst_n
2	SHDWDBCTLMODE	R/W	0h	DBCTL Load Mode 0: Immediate mode - only the Active DBCTL register is used. All writes/reads via the CPU directly access the Active register. 1: Shadow mode - All writes and reads to bits [5:0] of the DBCTL register are shadowed. All other bits still access the active register. Reset Source: epwm_rst_mod_g_rst_n
1:0	LOADDBCTLMODE	R/W	0h	Active DBCTL Load from Shadow Select Mode 00: Load on Counter = 0 [CNT_eq] 01: Load on Counter = Period [PRD_eq] 10: Load on either Counter = 0, or Counter = Period 11: Freeze [no loads possible] Note: has no effect in Immediate mode Reset Source: epwm_rst_mod_g_rst_n

3.9.12 MEM_AQCTL Registers

3.9.12.1 MEM_AQCTL Register (Offset = 20h) [reset = 0h]

Short Description: Action Qualifier Control

Long Description: Action Qualifier Control Register

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Table 3-703. Instance Table

Instance Name	Physical Address
CONTROLSS_EPWM0_G0	5000 0020h
CONTROLSS_EPWM1_G0	5000 1020h
CONTROLSS_EPWM10_G0	5000 A020h
CONTROLSS_EPWM11_G0	5000 B020h
CONTROLSS_EPWM12_G0	5000 C020h
CONTROLSS_EPWM13_G0	5000 D020h
CONTROLSS_EPWM14_G0	5000 E020h
CONTROLSS_EPWM15_G0	5000 F020h
CONTROLSS_EPWM16_G0	5001 0020h
CONTROLSS_EPWM17_G0	5001 1020h
CONTROLSS_EPWM18_G0	5001 2020h
CONTROLSS_EPWM19_G0	5001 3020h
CONTROLSS_EPWM2_G0	5000 2020h
CONTROLSS_EPWM20_G0	5001 4020h
CONTROLSS_EPWM21_G0	5001 5020h
CONTROLSS_EPWM22_G0	5001 6020h
CONTROLSS_EPWM23_G0	5001 7020h
CONTROLSS_EPWM24_G0	5001 8020h
CONTROLSS_EPWM25_G0	5001 9020h
CONTROLSS_EPWM26_G0	5001 A020h
CONTROLSS_EPWM27_G0	5001 B020h
CONTROLSS_EPWM28_G0	5001 C020h
CONTROLSS_EPWM29_G0	5001 D020h
CONTROLSS_EPWM3_G0	5000 3020h
CONTROLSS_EPWM30_G0	5001 E020h
CONTROLSS_EPWM31_G0	5001 F020h
CONTROLSS_EPWM4_G0	5000 4020h
CONTROLSS_EPWM5_G0	5000 5020h
CONTROLSS_EPWM6_G0	5000 6020h
CONTROLSS_EPWM7_G0	5000 7020h
CONTROLSS_EPWM8_G0	5000 8020h
CONTROLSS_EPWM9_G0	5000 9020h
CONTROLSS_EPWM0_G1	5004 0020h
CONTROLSS_EPWM1_G1	5004 1020h
CONTROLSS_EPWM10_G1	5004 A020h
CONTROLSS_EPWM11_G1	5004 B020h
CONTROLSS_EPWM12_G1	5004 C020h
CONTROLSS_EPWM13_G1	5004 D020h
CONTROLSS_EPWM14_G1	5004 E020h

Table 3-703. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM15_G1	5004 F020h
CONTROLSS_EPWM16_G1	5005 0020h
CONTROLSS_EPWM17_G1	5005 1020h
CONTROLSS_EPWM18_G1	5005 2020h
CONTROLSS_EPWM19_G1	5005 3020h
CONTROLSS_EPWM2_G1	5004 2020h
CONTROLSS_EPWM20_G1	5005 4020h
CONTROLSS_EPWM21_G1	5005 5020h
CONTROLSS_EPWM22_G1	5005 6020h
CONTROLSS_EPWM23_G1	5005 7020h
CONTROLSS_EPWM24_G1	5005 8020h
CONTROLSS_EPWM25_G1	5005 9020h
CONTROLSS_EPWM26_G1	5005 A020h
CONTROLSS_EPWM27_G1	5005 B020h
CONTROLSS_EPWM28_G1	5005 C020h
CONTROLSS_EPWM29_G1	5005 D020h
CONTROLSS_EPWM3_G1	5004 3020h
CONTROLSS_EPWM30_G1	5005 E020h
CONTROLSS_EPWM31_G1	5005 F020h
CONTROLSS_EPWM4_G1	5004 4020h
CONTROLSS_EPWM5_G1	5004 5020h
CONTROLSS_EPWM6_G1	5004 6020h
CONTROLSS_EPWM7_G1	5004 7020h
CONTROLSS_EPWM8_G1	5004 8020h
CONTROLSS_EPWM9_G1	5004 9020h
CONTROLSS_EPWM0_G2	5008 0020h
CONTROLSS_EPWM1_G2	5008 1020h
CONTROLSS_EPWM10_G2	5008 A020h
CONTROLSS_EPWM11_G2	5008 B020h
CONTROLSS_EPWM12_G2	5008 C020h
CONTROLSS_EPWM13_G2	5008 D020h
CONTROLSS_EPWM14_G2	5008 E020h
CONTROLSS_EPWM15_G2	5008 F020h
CONTROLSS_EPWM16_G2	5009 0020h
CONTROLSS_EPWM17_G2	5009 1020h
CONTROLSS_EPWM18_G2	5009 2020h
CONTROLSS_EPWM19_G2	5009 3020h
CONTROLSS_EPWM2_G2	5008 2020h
CONTROLSS_EPWM20_G2	5009 4020h
CONTROLSS_EPWM21_G2	5009 5020h
CONTROLSS_EPWM22_G2	5009 6020h
CONTROLSS_EPWM23_G2	5009 7020h
CONTROLSS_EPWM24_G2	5009 8020h
CONTROLSS_EPWM25_G2	5009 9020h
CONTROLSS_EPWM26_G2	5009 A020h
CONTROLSS_EPWM27_G2	5009 B020h
CONTROLSS_EPWM28_G2	5009 C020h

Table 3-703. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM29_G2	5009 D020h
CONTROLSS_EPWM3_G2	5008 3020h
CONTROLSS_EPWM30_G2	5009 E020h
CONTROLSS_EPWM31_G2	5009 F020h
CONTROLSS_EPWM4_G2	5008 4020h
CONTROLSS_EPWM5_G2	5008 5020h
CONTROLSS_EPWM6_G2	5008 6020h
CONTROLSS_EPWM7_G2	5008 7020h
CONTROLSS_EPWM8_G2	5008 8020h
CONTROLSS_EPWM9_G2	5008 9020h
CONTROLSS_EPWM0_G3	500C 0020h
CONTROLSS_EPWM1_G3	500C 1020h
CONTROLSS_EPWM10_G3	500C A020h
CONTROLSS_EPWM11_G3	500C B020h
CONTROLSS_EPWM12_G3	500C C020h
CONTROLSS_EPWM13_G3	500C D020h
CONTROLSS_EPWM14_G3	500C E020h
CONTROLSS_EPWM15_G3	500C F020h
CONTROLSS_EPWM16_G3	500D 0020h
CONTROLSS_EPWM17_G3	500D 1020h
CONTROLSS_EPWM18_G3	500D 2020h
CONTROLSS_EPWM19_G3	500D 3020h
CONTROLSS_EPWM2_G3	500C 2020h
CONTROLSS_EPWM20_G3	500D 4020h
CONTROLSS_EPWM21_G3	500D 5020h
CONTROLSS_EPWM22_G3	500D 6020h
CONTROLSS_EPWM23_G3	500D 7020h
CONTROLSS_EPWM24_G3	500D 8020h
CONTROLSS_EPWM25_G3	500D 9020h
CONTROLSS_EPWM26_G3	500D A020h
CONTROLSS_EPWM27_G3	500D B020h
CONTROLSS_EPWM28_G3	500D C020h
CONTROLSS_EPWM29_G3	500D D020h
CONTROLSS_EPWM3_G3	500C 3020h
CONTROLSS_EPWM30_G3	500D E020h
CONTROLSS_EPWM31_G3	500D F020h
CONTROLSS_EPWM4_G3	500C 4020h
CONTROLSS_EPWM5_G3	500C 5020h
CONTROLSS_EPWM6_G3	500C 6020h
CONTROLSS_EPWM7_G3	500C 7020h
CONTROLSS_EPWM8_G3	500C 8020h
CONTROLSS_EPWM9_G3	500C 9020h

Figure 3-298. AQCTL Name Register

15	14	13	12	11	10	9	8
RESERVED_3				LDAQBSYNC		LDAQASYNC	
R				R/W		R/W	

Figure 3-298. AQCTL Name Register (continued)

0h				0h		0h	
7	6	5	4	3	2	1	0
RESERVED_2	SHDWAQBMODE	RESERVED_1	SHDWAQAMODE	LDAQBMODE		LDAQAMODE	
R	R/W	R	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	

Access Types Legend

Table 3-704. AQCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_3	R	0h	Reserved Reset Source: epwm_rst_mod_g_rst_n
11:10	LDAQBSYNC	R/W	0h	Shadow to Active AQCTLB Register Load on SYNC event 00: Shadow to Active Load of AQCTLB occurs according to LDAQBMODE 01: Shadow to Active Load of AQCTLB occurs both according to LDAQBMODE bits and when SYNC occurs. 10: Shadow to Active Load of AQCTLB occurs only when a SYNC is received. 11: Reserved Note: This bit is valid only if AQCTL[SHDWAQBMODE] = 1. Reset Source: epwm_rst_mod_g_rst_n
9:8	LDAQASYNC	R/W	0h	Shadow to Active AQCTLA Register Load on SYNC event 00: Shadow to Active Load of AQCTLA occurs according to LDAQAMODE 01: Shadow to Active Load of AQCTLA occurs both according to LDAQAMODE bits and when SYNC occurs. 10: Shadow to Active Load of AQCTLA occurs only when a SYNC is received. 11: Reserved Note: This bit is valid only if AQCTL[SHDWAQAMODE] = 1. Reset Source: epwm_rst_mod_g_rst_n
7	RESERVED_2	R	0h	Reserved Reset Source: epwm_rst_mod_g_rst_n
6	SHDWAQBMODE	R/W	0h	Action Qualifier B Register operating mode 1: Shadow mode - operates as a double buffer. All writes via the CPU access Shadow register. 0: Immediate mode - only the Active action qualifier register is used. All writes/reads via the CPU directly access the Active register. Reset Source: epwm_rst_mod_g_rst_n
5	RESERVED_1	R	0h	Reserved Reset Source: epwm_rst_mod_g_rst_n
4	SHDWAQAMODE	R/W	0h	Action Qualifier A Register operating mode 1: Shadow mode - operates as a double buffer. All writes via the CPU access Shadow register. 0: Immediate mode - only the Active action qualifier register is used. All writes/reads via the CPU directly access the Active register. Reset Source: epwm_rst_mod_g_rst_n
3:2	LDAQBMODE	R/W	0h	Active Action Qualifier B Load from Shadow Select Mode 00: Load on CTR = Zero: Time-base counter equal to zero [TBCTR = 0x0000] 01: Load on CTR = PRD: Time-base counter equal to period [TBCTR = TBPRD] 10: Load on either CTR = Zero or CTR = PRD 11: Freeze [no loads possible] Note: has no effect in Immediate mode. Reset Source: epwm_rst_mod_g_rst_n
1:0	LDAQAMODE	R/W	0h	Active Action Qualifier A Load from Shadow Select Mode 00: Load on CTR = Zero: Time-base counter equal to zero [TBCTR = 0x0000] 01: Load on CTR = PRD: Time-base counter equal to period [TBCTR = TBPRD] 10: Load on either CTR = Zero or CTR = PRD 11: Freeze [no loads possible] Note: has no effect in Immediate mode. Reset Source: epwm_rst_mod_g_rst_n

3.9.13 MEM_AQTSRCSEL Registers

3.9.13.1 MEM_AQTSRCSEL Register (Offset = 22h) [reset = 0h]

Short Description: Action Qualifier Trigger

Long Description: Action Qualifier Trigger Event Source Select Register

Return to Summary Table

Table 3-705. Instance Table

Instance Name	Physical Address
CONTROLSS_EPWM0_G0	5000 0022h
CONTROLSS_EPWM1_G0	5000 1022h
CONTROLSS_EPWM10_G0	5000 A022h
CONTROLSS_EPWM11_G0	5000 B022h
CONTROLSS_EPWM12_G0	5000 C022h
CONTROLSS_EPWM13_G0	5000 D022h
CONTROLSS_EPWM14_G0	5000 E022h
CONTROLSS_EPWM15_G0	5000 F022h
CONTROLSS_EPWM16_G0	5001 0022h
CONTROLSS_EPWM17_G0	5001 1022h
CONTROLSS_EPWM18_G0	5001 2022h
CONTROLSS_EPWM19_G0	5001 3022h
CONTROLSS_EPWM2_G0	5000 2022h
CONTROLSS_EPWM20_G0	5001 4022h
CONTROLSS_EPWM21_G0	5001 5022h
CONTROLSS_EPWM22_G0	5001 6022h
CONTROLSS_EPWM23_G0	5001 7022h
CONTROLSS_EPWM24_G0	5001 8022h
CONTROLSS_EPWM25_G0	5001 9022h
CONTROLSS_EPWM26_G0	5001 A022h
CONTROLSS_EPWM27_G0	5001 B022h
CONTROLSS_EPWM28_G0	5001 C022h
CONTROLSS_EPWM29_G0	5001 D022h
CONTROLSS_EPWM3_G0	5000 3022h
CONTROLSS_EPWM30_G0	5001 E022h
CONTROLSS_EPWM31_G0	5001 F022h
CONTROLSS_EPWM4_G0	5000 4022h
CONTROLSS_EPWM5_G0	5000 5022h
CONTROLSS_EPWM6_G0	5000 6022h
CONTROLSS_EPWM7_G0	5000 7022h
CONTROLSS_EPWM8_G0	5000 8022h
CONTROLSS_EPWM9_G0	5000 9022h
CONTROLSS_EPWM0_G1	5004 0022h
CONTROLSS_EPWM1_G1	5004 1022h
CONTROLSS_EPWM10_G1	5004 A022h
CONTROLSS_EPWM11_G1	5004 B022h
CONTROLSS_EPWM12_G1	5004 C022h
CONTROLSS_EPWM13_G1	5004 D022h
CONTROLSS_EPWM14_G1	5004 E022h

Table 3-705. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM15_G1	5004 F022h
CONTROLSS_EPWM16_G1	5005 0022h
CONTROLSS_EPWM17_G1	5005 1022h
CONTROLSS_EPWM18_G1	5005 2022h
CONTROLSS_EPWM19_G1	5005 3022h
CONTROLSS_EPWM2_G1	5004 2022h
CONTROLSS_EPWM20_G1	5005 4022h
CONTROLSS_EPWM21_G1	5005 5022h
CONTROLSS_EPWM22_G1	5005 6022h
CONTROLSS_EPWM23_G1	5005 7022h
CONTROLSS_EPWM24_G1	5005 8022h
CONTROLSS_EPWM25_G1	5005 9022h
CONTROLSS_EPWM26_G1	5005 A022h
CONTROLSS_EPWM27_G1	5005 B022h
CONTROLSS_EPWM28_G1	5005 C022h
CONTROLSS_EPWM29_G1	5005 D022h
CONTROLSS_EPWM3_G1	5004 3022h
CONTROLSS_EPWM30_G1	5005 E022h
CONTROLSS_EPWM31_G1	5005 F022h
CONTROLSS_EPWM4_G1	5004 4022h
CONTROLSS_EPWM5_G1	5004 5022h
CONTROLSS_EPWM6_G1	5004 6022h
CONTROLSS_EPWM7_G1	5004 7022h
CONTROLSS_EPWM8_G1	5004 8022h
CONTROLSS_EPWM9_G1	5004 9022h
CONTROLSS_EPWM0_G2	5008 0022h
CONTROLSS_EPWM1_G2	5008 1022h
CONTROLSS_EPWM10_G2	5008 A022h
CONTROLSS_EPWM11_G2	5008 B022h
CONTROLSS_EPWM12_G2	5008 C022h
CONTROLSS_EPWM13_G2	5008 D022h
CONTROLSS_EPWM14_G2	5008 E022h
CONTROLSS_EPWM15_G2	5008 F022h
CONTROLSS_EPWM16_G2	5009 0022h
CONTROLSS_EPWM17_G2	5009 1022h
CONTROLSS_EPWM18_G2	5009 2022h
CONTROLSS_EPWM19_G2	5009 3022h
CONTROLSS_EPWM2_G2	5008 2022h
CONTROLSS_EPWM20_G2	5009 4022h
CONTROLSS_EPWM21_G2	5009 5022h
CONTROLSS_EPWM22_G2	5009 6022h
CONTROLSS_EPWM23_G2	5009 7022h
CONTROLSS_EPWM24_G2	5009 8022h
CONTROLSS_EPWM25_G2	5009 9022h
CONTROLSS_EPWM26_G2	5009 A022h
CONTROLSS_EPWM27_G2	5009 B022h
CONTROLSS_EPWM28_G2	5009 C022h

Table 3-705. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM29_G2	5009 D022h
CONTROLSS_EPWM3_G2	5008 3022h
CONTROLSS_EPWM30_G2	5009 E022h
CONTROLSS_EPWM31_G2	5009 F022h
CONTROLSS_EPWM4_G2	5008 4022h
CONTROLSS_EPWM5_G2	5008 5022h
CONTROLSS_EPWM6_G2	5008 6022h
CONTROLSS_EPWM7_G2	5008 7022h
CONTROLSS_EPWM8_G2	5008 8022h
CONTROLSS_EPWM9_G2	5008 9022h
CONTROLSS_EPWM0_G3	500C 0022h
CONTROLSS_EPWM1_G3	500C 1022h
CONTROLSS_EPWM10_G3	500C A022h
CONTROLSS_EPWM11_G3	500C B022h
CONTROLSS_EPWM12_G3	500C C022h
CONTROLSS_EPWM13_G3	500C D022h
CONTROLSS_EPWM14_G3	500C E022h
CONTROLSS_EPWM15_G3	500C F022h
CONTROLSS_EPWM16_G3	500D 0022h
CONTROLSS_EPWM17_G3	500D 1022h
CONTROLSS_EPWM18_G3	500D 2022h
CONTROLSS_EPWM19_G3	500D 3022h
CONTROLSS_EPWM2_G3	500C 2022h
CONTROLSS_EPWM20_G3	500D 4022h
CONTROLSS_EPWM21_G3	500D 5022h
CONTROLSS_EPWM22_G3	500D 6022h
CONTROLSS_EPWM23_G3	500D 7022h
CONTROLSS_EPWM24_G3	500D 8022h
CONTROLSS_EPWM25_G3	500D 9022h
CONTROLSS_EPWM26_G3	500D A022h
CONTROLSS_EPWM27_G3	500D B022h
CONTROLSS_EPWM28_G3	500D C022h
CONTROLSS_EPWM29_G3	500D D022h
CONTROLSS_EPWM3_G3	500C 3022h
CONTROLSS_EPWM30_G3	500D E022h
CONTROLSS_EPWM31_G3	500D F022h
CONTROLSS_EPWM4_G3	500C 4022h
CONTROLSS_EPWM5_G3	500C 5022h
CONTROLSS_EPWM6_G3	500C 6022h
CONTROLSS_EPWM7_G3	500C 7022h
CONTROLSS_EPWM8_G3	500C 8022h
CONTROLSS_EPWM9_G3	500C 9022h

Figure 3-299. AQTSRCSEL Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							

Figure 3-299. AQTSRCSEL Name Register (continued)

0h							
7	6	5	4	3	2	1	0
T2SEL				T1SEL			
R/W				R/W			
0h				0h			

Access Types Legend

Table 3-706. AQTSRCSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED_1	R	0h	Reserved Reset Source: epwm_rst_mod_g_rst_n
7:4	T2SEL	R/W	0h	T2 Event Source Select Bits 0000: DCAEVT1 0001: DCAEVT2 0010: DCBEVT1 0011: DCBEVT2 0100: TZ1 0101: TZ2 0110: TZ3 0111: EPWMxSYNCI 1000: DCEVTFILT Others: Reserved Reset Source: epwm_rst_mod_g_rst_n
3:0	T1SEL	R/W	0h	T1 Event Source Select Bits 0000: DCAEVT1 0001: DCAEVT2 0010: DCBEVT1 0011: DCBEVT2 0100: TZ1 0101: TZ2 0110: TZ3 0111: EPWMxSYNCI 1000: DCEVTFILT Others: Reserved Reset Source: epwm_rst_mod_g_rst_n

3.9.14 MEM_PCCTL Registers

3.9.14.1 MEM_PCCTL Register (Offset = 28h) [reset = 0h]

Short Description: PWM Chopper Control Regis

Long Description: PWM Chopper Control Register

Return to Summary Table

Table 3-707. Instance Table

Instance Name	Physical Address
CONTROLSS_EPWM0_G0	5000 0028h
CONTROLSS_EPWM1_G0	5000 1028h
CONTROLSS_EPWM10_G0	5000 A028h
CONTROLSS_EPWM11_G0	5000 B028h
CONTROLSS_EPWM12_G0	5000 C028h
CONTROLSS_EPWM13_G0	5000 D028h
CONTROLSS_EPWM14_G0	5000 E028h
CONTROLSS_EPWM15_G0	5000 F028h
CONTROLSS_EPWM16_G0	5001 0028h
CONTROLSS_EPWM17_G0	5001 1028h
CONTROLSS_EPWM18_G0	5001 2028h
CONTROLSS_EPWM19_G0	5001 3028h
CONTROLSS_EPWM2_G0	5000 2028h
CONTROLSS_EPWM20_G0	5001 4028h
CONTROLSS_EPWM21_G0	5001 5028h
CONTROLSS_EPWM22_G0	5001 6028h
CONTROLSS_EPWM23_G0	5001 7028h
CONTROLSS_EPWM24_G0	5001 8028h
CONTROLSS_EPWM25_G0	5001 9028h
CONTROLSS_EPWM26_G0	5001 A028h
CONTROLSS_EPWM27_G0	5001 B028h
CONTROLSS_EPWM28_G0	5001 C028h
CONTROLSS_EPWM29_G0	5001 D028h
CONTROLSS_EPWM3_G0	5000 3028h
CONTROLSS_EPWM30_G0	5001 E028h
CONTROLSS_EPWM31_G0	5001 F028h
CONTROLSS_EPWM4_G0	5000 4028h
CONTROLSS_EPWM5_G0	5000 5028h
CONTROLSS_EPWM6_G0	5000 6028h
CONTROLSS_EPWM7_G0	5000 7028h
CONTROLSS_EPWM8_G0	5000 8028h
CONTROLSS_EPWM9_G0	5000 9028h
CONTROLSS_EPWM0_G1	5004 0028h
CONTROLSS_EPWM1_G1	5004 1028h
CONTROLSS_EPWM10_G1	5004 A028h
CONTROLSS_EPWM11_G1	5004 B028h
CONTROLSS_EPWM12_G1	5004 C028h
CONTROLSS_EPWM13_G1	5004 D028h
CONTROLSS_EPWM14_G1	5004 E028h

Table 3-707. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM15_G1	5004 F028h
CONTROLSS_EPWM16_G1	5005 0028h
CONTROLSS_EPWM17_G1	5005 1028h
CONTROLSS_EPWM18_G1	5005 2028h
CONTROLSS_EPWM19_G1	5005 3028h
CONTROLSS_EPWM2_G1	5004 2028h
CONTROLSS_EPWM20_G1	5005 4028h
CONTROLSS_EPWM21_G1	5005 5028h
CONTROLSS_EPWM22_G1	5005 6028h
CONTROLSS_EPWM23_G1	5005 7028h
CONTROLSS_EPWM24_G1	5005 8028h
CONTROLSS_EPWM25_G1	5005 9028h
CONTROLSS_EPWM26_G1	5005 A028h
CONTROLSS_EPWM27_G1	5005 B028h
CONTROLSS_EPWM28_G1	5005 C028h
CONTROLSS_EPWM29_G1	5005 D028h
CONTROLSS_EPWM3_G1	5004 3028h
CONTROLSS_EPWM30_G1	5005 E028h
CONTROLSS_EPWM31_G1	5005 F028h
CONTROLSS_EPWM4_G1	5004 4028h
CONTROLSS_EPWM5_G1	5004 5028h
CONTROLSS_EPWM6_G1	5004 6028h
CONTROLSS_EPWM7_G1	5004 7028h
CONTROLSS_EPWM8_G1	5004 8028h
CONTROLSS_EPWM9_G1	5004 9028h
CONTROLSS_EPWM0_G2	5008 0028h
CONTROLSS_EPWM1_G2	5008 1028h
CONTROLSS_EPWM10_G2	5008 A028h
CONTROLSS_EPWM11_G2	5008 B028h
CONTROLSS_EPWM12_G2	5008 C028h
CONTROLSS_EPWM13_G2	5008 D028h
CONTROLSS_EPWM14_G2	5008 E028h
CONTROLSS_EPWM15_G2	5008 F028h
CONTROLSS_EPWM16_G2	5009 0028h
CONTROLSS_EPWM17_G2	5009 1028h
CONTROLSS_EPWM18_G2	5009 2028h
CONTROLSS_EPWM19_G2	5009 3028h
CONTROLSS_EPWM2_G2	5008 2028h
CONTROLSS_EPWM20_G2	5009 4028h
CONTROLSS_EPWM21_G2	5009 5028h
CONTROLSS_EPWM22_G2	5009 6028h
CONTROLSS_EPWM23_G2	5009 7028h
CONTROLSS_EPWM24_G2	5009 8028h
CONTROLSS_EPWM25_G2	5009 9028h
CONTROLSS_EPWM26_G2	5009 A028h
CONTROLSS_EPWM27_G2	5009 B028h
CONTROLSS_EPWM28_G2	5009 C028h

Table 3-707. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM29_G2	5009 D028h
CONTROLSS_EPWM3_G2	5008 3028h
CONTROLSS_EPWM30_G2	5009 E028h
CONTROLSS_EPWM31_G2	5009 F028h
CONTROLSS_EPWM4_G2	5008 4028h
CONTROLSS_EPWM5_G2	5008 5028h
CONTROLSS_EPWM6_G2	5008 6028h
CONTROLSS_EPWM7_G2	5008 7028h
CONTROLSS_EPWM8_G2	5008 8028h
CONTROLSS_EPWM9_G2	5008 9028h
CONTROLSS_EPWM0_G3	500C 0028h
CONTROLSS_EPWM1_G3	500C 1028h
CONTROLSS_EPWM10_G3	500C A028h
CONTROLSS_EPWM11_G3	500C B028h
CONTROLSS_EPWM12_G3	500C C028h
CONTROLSS_EPWM13_G3	500C D028h
CONTROLSS_EPWM14_G3	500C E028h
CONTROLSS_EPWM15_G3	500C F028h
CONTROLSS_EPWM16_G3	500D 0028h
CONTROLSS_EPWM17_G3	500D 1028h
CONTROLSS_EPWM18_G3	500D 2028h
CONTROLSS_EPWM19_G3	500D 3028h
CONTROLSS_EPWM2_G3	500C 2028h
CONTROLSS_EPWM20_G3	500D 4028h
CONTROLSS_EPWM21_G3	500D 5028h
CONTROLSS_EPWM22_G3	500D 6028h
CONTROLSS_EPWM23_G3	500D 7028h
CONTROLSS_EPWM24_G3	500D 8028h
CONTROLSS_EPWM25_G3	500D 9028h
CONTROLSS_EPWM26_G3	500D A028h
CONTROLSS_EPWM27_G3	500D B028h
CONTROLSS_EPWM28_G3	500D C028h
CONTROLSS_EPWM29_G3	500D D028h
CONTROLSS_EPWM3_G3	500C 3028h
CONTROLSS_EPWM30_G3	500D E028h
CONTROLSS_EPWM31_G3	500D F028h
CONTROLSS_EPWM4_G3	500C 4028h
CONTROLSS_EPWM5_G3	500C 5028h
CONTROLSS_EPWM6_G3	500C 6028h
CONTROLSS_EPWM7_G3	500C 7028h
CONTROLSS_EPWM8_G3	500C 8028h
CONTROLSS_EPWM9_G3	500C 9028h

Figure 3-300. PCCTL Name Register

15	14	13	12	11	10	9	8
RESERVED_1					CHPDUTY		
R					R/W		

Figure 3-300. PCCTL Name Register (continued)

0h						0h	
7	6	5	4	3	2	1	0
CHPFREQ			OSHTWTH				CHPEN
R/W			R/W				R/W
0h			0h				0h

Access Types Legend

Table 3-708. PCCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED_1	R	0h	Reserved Reset Source: epwm_rst_mod_g_rst_n
10:8	CHPDUTY	R/W	0h	Chopping Clock Duty Cycle 000: Duty = 1/8 [12.5%] 001: Duty = 2/8 [25.0%] 010: Duty = 3/8 [37.5%] 011: Duty = 4/8 [50.0%] 100: Duty = 5/8 [62.5%] 101: Duty = 6/8 [75.0%] 110: Duty = 7/8 [87.5%] 111: Reserved Reset Source: epwm_rst_mod_g_rst_n
7:5	CHPFREQ	R/W	0h	Chopping Clock Frequency 000: Divide by 1 [no prescale, = 12.5 MHz at 100 MHz TBCLK] 001: Divide by 2 [6.25 MHz at 100 MHz TBCLK] 010: Divide by 3 [4.16 MHz at 100 MHz TBCLK] 011: Divide by 4 [3.12 MHz at 100 MHz TBCLK] 100: Divide by 5 [2.50 MHz at 100 MHz TBCLK] 101: Divide by 6 [2.08 MHz at 100 MHz TBCLK] 110: Divide by 7 [1.78 MHz at 100 MHz TBCLK] 111: Divide by 8 [1.56 MHz at 100 MHz TBCLK] Reset Source: epwm_rst_mod_g_rst_n
4:1	OSHTWTH	R/W	0h	One-Shot Pulse Width 0000: 1 x EPWMCLK / 8 wide [= 80 ns at 100 MHz EPWMCLK] 0001: 2 x EPWMCLK / 8 wide [= 160 ns at 100 MHz EPWMCLK] 0010: 3 x EPWMCLK / 8 wide [= 240 ns at 100 MHz EPWMCLK] 0011: 4 x EPWMCLK / 8 wide [= 320 ns at 100 MHz EPWMCLK] 0100: 5 x EPWMCLK / 8 wide [= 400 ns at 100 MHz EPWMCLK] 0101: 6 x EPWMCLK / 8 wide [= 480 ns at 100 MHz EPWMCLK] 0110: 7 x EPWMCLK / 8 wide [= 560 ns at 100 MHz EPWMCLK] 0111: 8 x EPWMCLK / 8 wide [= 640 ns at 100 MHz EPWMCLK] 1000: 9 x EPWMCLK / 8 wide [= 720 ns at 100 MHz EPWMCLK] 1001: 10 x EPWMCLK / 8 wide [= 800 ns at 100 MHz EPWMCLK] 1010: 11 x EPWMCLK / 8 wide [= 880 ns at 100 MHz EPWMCLK] 1011: 12 x EPWMCLK / 8 wide [= 960 ns at 100 MHz EPWMCLK] 1100: 13 x EPWMCLK / 8 wide [= 1040 ns at 100 MHz EPWMCLK] 1101: 14 x EPWMCLK / 8 wide [= 1120 ns at 100 MHz EPWMCLK] 1110: 15 x EPWMCLK / 8 wide [= 1200 ns at 100 MHz EPWMCLK] 1111: 16 x EPWMCLK / 8 wide [= 1280 ns at 100 MHz EPWMCLK] Reset Source: epwm_rst_mod_g_rst_n
0	CHPEN	R/W	0h	PWM-Chopping Enable 0: Disable [bypass] PWM chopping function 1: Enable chopping function Reset Source: epwm_rst_mod_g_rst_n

3.9.15 MEM_VCAPCTL Registers

3.9.15.1 MEM_VCAPCTL Register (Offset = 30h) [reset = 0h]

Short Description: Valley Capture Control Re

Long Description: Valley Capture Control Register

Return to Summary Table

Table 3-709. Instance Table

Instance Name	Physical Address
CONTROLSS_EPWM0_G0	5000 0030h
CONTROLSS_EPWM1_G0	5000 1030h
CONTROLSS_EPWM10_G0	5000 A030h
CONTROLSS_EPWM11_G0	5000 B030h
CONTROLSS_EPWM12_G0	5000 C030h
CONTROLSS_EPWM13_G0	5000 D030h
CONTROLSS_EPWM14_G0	5000 E030h
CONTROLSS_EPWM15_G0	5000 F030h
CONTROLSS_EPWM16_G0	5001 0030h
CONTROLSS_EPWM17_G0	5001 1030h
CONTROLSS_EPWM18_G0	5001 2030h
CONTROLSS_EPWM19_G0	5001 3030h
CONTROLSS_EPWM2_G0	5000 2030h
CONTROLSS_EPWM20_G0	5001 4030h
CONTROLSS_EPWM21_G0	5001 5030h
CONTROLSS_EPWM22_G0	5001 6030h
CONTROLSS_EPWM23_G0	5001 7030h
CONTROLSS_EPWM24_G0	5001 8030h
CONTROLSS_EPWM25_G0	5001 9030h
CONTROLSS_EPWM26_G0	5001 A030h
CONTROLSS_EPWM27_G0	5001 B030h
CONTROLSS_EPWM28_G0	5001 C030h
CONTROLSS_EPWM29_G0	5001 D030h
CONTROLSS_EPWM3_G0	5000 3030h
CONTROLSS_EPWM30_G0	5001 E030h
CONTROLSS_EPWM31_G0	5001 F030h
CONTROLSS_EPWM4_G0	5000 4030h
CONTROLSS_EPWM5_G0	5000 5030h
CONTROLSS_EPWM6_G0	5000 6030h
CONTROLSS_EPWM7_G0	5000 7030h
CONTROLSS_EPWM8_G0	5000 8030h
CONTROLSS_EPWM9_G0	5000 9030h
CONTROLSS_EPWM0_G1	5004 0030h
CONTROLSS_EPWM1_G1	5004 1030h
CONTROLSS_EPWM10_G1	5004 A030h
CONTROLSS_EPWM11_G1	5004 B030h
CONTROLSS_EPWM12_G1	5004 C030h
CONTROLSS_EPWM13_G1	5004 D030h
CONTROLSS_EPWM14_G1	5004 E030h

Table 3-709. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM15_G1	5004 F030h
CONTROLSS_EPWM16_G1	5005 0030h
CONTROLSS_EPWM17_G1	5005 1030h
CONTROLSS_EPWM18_G1	5005 2030h
CONTROLSS_EPWM19_G1	5005 3030h
CONTROLSS_EPWM2_G1	5004 2030h
CONTROLSS_EPWM20_G1	5005 4030h
CONTROLSS_EPWM21_G1	5005 5030h
CONTROLSS_EPWM22_G1	5005 6030h
CONTROLSS_EPWM23_G1	5005 7030h
CONTROLSS_EPWM24_G1	5005 8030h
CONTROLSS_EPWM25_G1	5005 9030h
CONTROLSS_EPWM26_G1	5005 A030h
CONTROLSS_EPWM27_G1	5005 B030h
CONTROLSS_EPWM28_G1	5005 C030h
CONTROLSS_EPWM29_G1	5005 D030h
CONTROLSS_EPWM3_G1	5004 3030h
CONTROLSS_EPWM30_G1	5005 E030h
CONTROLSS_EPWM31_G1	5005 F030h
CONTROLSS_EPWM4_G1	5004 4030h
CONTROLSS_EPWM5_G1	5004 5030h
CONTROLSS_EPWM6_G1	5004 6030h
CONTROLSS_EPWM7_G1	5004 7030h
CONTROLSS_EPWM8_G1	5004 8030h
CONTROLSS_EPWM9_G1	5004 9030h
CONTROLSS_EPWM0_G2	5008 0030h
CONTROLSS_EPWM1_G2	5008 1030h
CONTROLSS_EPWM10_G2	5008 A030h
CONTROLSS_EPWM11_G2	5008 B030h
CONTROLSS_EPWM12_G2	5008 C030h
CONTROLSS_EPWM13_G2	5008 D030h
CONTROLSS_EPWM14_G2	5008 E030h
CONTROLSS_EPWM15_G2	5008 F030h
CONTROLSS_EPWM16_G2	5009 0030h
CONTROLSS_EPWM17_G2	5009 1030h
CONTROLSS_EPWM18_G2	5009 2030h
CONTROLSS_EPWM19_G2	5009 3030h
CONTROLSS_EPWM2_G2	5008 2030h
CONTROLSS_EPWM20_G2	5009 4030h
CONTROLSS_EPWM21_G2	5009 5030h
CONTROLSS_EPWM22_G2	5009 6030h
CONTROLSS_EPWM23_G2	5009 7030h
CONTROLSS_EPWM24_G2	5009 8030h
CONTROLSS_EPWM25_G2	5009 9030h
CONTROLSS_EPWM26_G2	5009 A030h
CONTROLSS_EPWM27_G2	5009 B030h
CONTROLSS_EPWM28_G2	5009 C030h

Table 3-709. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM29_G2	5009 D030h
CONTROLSS_EPWM3_G2	5008 3030h
CONTROLSS_EPWM30_G2	5009 E030h
CONTROLSS_EPWM31_G2	5009 F030h
CONTROLSS_EPWM4_G2	5008 4030h
CONTROLSS_EPWM5_G2	5008 5030h
CONTROLSS_EPWM6_G2	5008 6030h
CONTROLSS_EPWM7_G2	5008 7030h
CONTROLSS_EPWM8_G2	5008 8030h
CONTROLSS_EPWM9_G2	5008 9030h
CONTROLSS_EPWM0_G3	500C 0030h
CONTROLSS_EPWM1_G3	500C 1030h
CONTROLSS_EPWM10_G3	500C A030h
CONTROLSS_EPWM11_G3	500C B030h
CONTROLSS_EPWM12_G3	500C C030h
CONTROLSS_EPWM13_G3	500C D030h
CONTROLSS_EPWM14_G3	500C E030h
CONTROLSS_EPWM15_G3	500C F030h
CONTROLSS_EPWM16_G3	500D 0030h
CONTROLSS_EPWM17_G3	500D 1030h
CONTROLSS_EPWM18_G3	500D 2030h
CONTROLSS_EPWM19_G3	500D 3030h
CONTROLSS_EPWM2_G3	500C 2030h
CONTROLSS_EPWM20_G3	500D 4030h
CONTROLSS_EPWM21_G3	500D 5030h
CONTROLSS_EPWM22_G3	500D 6030h
CONTROLSS_EPWM23_G3	500D 7030h
CONTROLSS_EPWM24_G3	500D 8030h
CONTROLSS_EPWM25_G3	500D 9030h
CONTROLSS_EPWM26_G3	500D A030h
CONTROLSS_EPWM27_G3	500D B030h
CONTROLSS_EPWM28_G3	500D C030h
CONTROLSS_EPWM29_G3	500D D030h
CONTROLSS_EPWM3_G3	500C 3030h
CONTROLSS_EPWM30_G3	500D E030h
CONTROLSS_EPWM31_G3	500D F030h
CONTROLSS_EPWM4_G3	500C 4030h
CONTROLSS_EPWM5_G3	500C 5030h
CONTROLSS_EPWM6_G3	500C 6030h
CONTROLSS_EPWM7_G3	500C 7030h
CONTROLSS_EPWM8_G3	500C 8030h
CONTROLSS_EPWM9_G3	500C 9030h

Figure 3-301. VCAPCTL Name Register

15	14	13	12	11	10	9	8
RESERVED_2					EDGEFILTDLY SEL	VDELAYDIV	

Figure 3-301. VCAPCTL Name Register (continued)

R					R/W	R/W	
0h					0h	0h	
7	6	5	4	3	2	1	0
VDELAYDIV	RESERVED_1		TRIGSEL			VCAPSTART	VCAPE
R/W	R		R/W			R/W1TS	R/W
0h	0h		0h			0h	0h

Access Types Legend

Table 3-710. VCAPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED_2	R	0h	Reserved Reset Source: epwm_rst_mod_g_rst_n
10	EDGEFILTDLYSEL	R/W	0h	Valley Switching Mode Delay Selection 0: No delay applied to the edge filter output 1: HWDELAYVAL delay applied to the edge filter output Reset Source: epwm_rst_mod_g_rst_n
9:7	VDELAYDIV	R/W	0h	Valley Delay Mode Divide Enable 000: HWVDELVAL = SWVDELVAL 001: HWVDELVAL = VCNTVAL+SWVDELVAL 010: HWVDELVAL = VCNTVAL"1+SWVDELVAL 011: HWVDELVAL = VCNTVAL"2+SWVDELVAL 100: HWVDELVAL = VCNTVAL"4+SWVDELVAL Note: Delay value between the consecutive edge captures can optionally be divided by using these bits. Reset Source: epwm_rst_mod_g_rst_n
6:5	RESERVED_1	R	0h	Reserved Reset Source: epwm_rst_mod_g_rst_n
4:2	TRIGSEL	R/W	0h	Status of Numbered of Captured Events 000: Capture sequence is triggered by software via writes to VCAPCTL[VCAPSTART]. 001: Capture sequence is triggered by CNT_zero event. 010: Capture sequence is triggered by PRD_eq event. 011: Capture sequence is triggered by CNT_zero or PRD_eq event. 100: Capture sequence is triggered by DCAEVT1 event. 101: Capture sequence is triggered by DCAEVT2 event. 110: Capture sequence is triggered by DCBEVT1 event. 111: Capture sequence is triggered by DCBEVT2 event. Note: Valley capture sequence triggered by the selected event in this register field. Once the chosen event occurs the capture sequence is armed. Event captures occur based of the event chosen in DCFCTL[SRCSEL] register. Note: Same event may not be chosen in both DCFCTL[SRCSEL] and VCAPCTL[TRIGSEL] registers. Note: Once the chosen event in VCAPCTL[TRIGSEL] occurs, irrespective of the current capture status, capture sequence is retriggered. Reset Source: epwm_rst_mod_g_rst_n
1	VCAPSTART	R/W1TS	0h	Valley Capture Start 0: Writing a 0 has no effect 1: Trigger the capture sequence once if VCAPCTL[TRIGSEL]=0x0 Note: This bit is used to start valley capture sequence through software. VCAPCTL[TRIGSEL] has to be chosen for software trigger for this bit to have any effect. Writing of 1 will result in one capture sequence trigger. Reset Source: epwm_rst_mod_g_rst_n
0	VCAPE	R/W	0h	Valley Capture Enable/Disable 0: Disabled 1: Enabled Reset Source: epwm_rst_mod_g_rst_n

3.9.16 MEM_VCNTCFG Registers

3.9.16.1 MEM_VCNTCFG Register (Offset = 32h) [reset = 0h]

Short Description: Valley Counter Config Reg

Long Description: Valley Counter Config Register

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Table 3-711. Instance Table

Instance Name	Physical Address
CONTROLSS_EPWM0_G0	5000 0032h
CONTROLSS_EPWM1_G0	5000 1032h
CONTROLSS_EPWM10_G0	5000 A032h
CONTROLSS_EPWM11_G0	5000 B032h
CONTROLSS_EPWM12_G0	5000 C032h
CONTROLSS_EPWM13_G0	5000 D032h
CONTROLSS_EPWM14_G0	5000 E032h
CONTROLSS_EPWM15_G0	5000 F032h
CONTROLSS_EPWM16_G0	5001 0032h
CONTROLSS_EPWM17_G0	5001 1032h
CONTROLSS_EPWM18_G0	5001 2032h
CONTROLSS_EPWM19_G0	5001 3032h
CONTROLSS_EPWM2_G0	5000 2032h
CONTROLSS_EPWM20_G0	5001 4032h
CONTROLSS_EPWM21_G0	5001 5032h
CONTROLSS_EPWM22_G0	5001 6032h
CONTROLSS_EPWM23_G0	5001 7032h
CONTROLSS_EPWM24_G0	5001 8032h
CONTROLSS_EPWM25_G0	5001 9032h
CONTROLSS_EPWM26_G0	5001 A032h
CONTROLSS_EPWM27_G0	5001 B032h
CONTROLSS_EPWM28_G0	5001 C032h
CONTROLSS_EPWM29_G0	5001 D032h
CONTROLSS_EPWM3_G0	5000 3032h
CONTROLSS_EPWM30_G0	5001 E032h
CONTROLSS_EPWM31_G0	5001 F032h
CONTROLSS_EPWM4_G0	5000 4032h
CONTROLSS_EPWM5_G0	5000 5032h
CONTROLSS_EPWM6_G0	5000 6032h
CONTROLSS_EPWM7_G0	5000 7032h
CONTROLSS_EPWM8_G0	5000 8032h
CONTROLSS_EPWM9_G0	5000 9032h
CONTROLSS_EPWM0_G1	5004 0032h
CONTROLSS_EPWM1_G1	5004 1032h
CONTROLSS_EPWM10_G1	5004 A032h
CONTROLSS_EPWM11_G1	5004 B032h
CONTROLSS_EPWM12_G1	5004 C032h
CONTROLSS_EPWM13_G1	5004 D032h
CONTROLSS_EPWM14_G1	5004 E032h

Table 3-711. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM15_G1	5004 F032h
CONTROLSS_EPWM16_G1	5005 0032h
CONTROLSS_EPWM17_G1	5005 1032h
CONTROLSS_EPWM18_G1	5005 2032h
CONTROLSS_EPWM19_G1	5005 3032h
CONTROLSS_EPWM2_G1	5004 2032h
CONTROLSS_EPWM20_G1	5005 4032h
CONTROLSS_EPWM21_G1	5005 5032h
CONTROLSS_EPWM22_G1	5005 6032h
CONTROLSS_EPWM23_G1	5005 7032h
CONTROLSS_EPWM24_G1	5005 8032h
CONTROLSS_EPWM25_G1	5005 9032h
CONTROLSS_EPWM26_G1	5005 A032h
CONTROLSS_EPWM27_G1	5005 B032h
CONTROLSS_EPWM28_G1	5005 C032h
CONTROLSS_EPWM29_G1	5005 D032h
CONTROLSS_EPWM3_G1	5004 3032h
CONTROLSS_EPWM30_G1	5005 E032h
CONTROLSS_EPWM31_G1	5005 F032h
CONTROLSS_EPWM4_G1	5004 4032h
CONTROLSS_EPWM5_G1	5004 5032h
CONTROLSS_EPWM6_G1	5004 6032h
CONTROLSS_EPWM7_G1	5004 7032h
CONTROLSS_EPWM8_G1	5004 8032h
CONTROLSS_EPWM9_G1	5004 9032h
CONTROLSS_EPWM0_G2	5008 0032h
CONTROLSS_EPWM1_G2	5008 1032h
CONTROLSS_EPWM10_G2	5008 A032h
CONTROLSS_EPWM11_G2	5008 B032h
CONTROLSS_EPWM12_G2	5008 C032h
CONTROLSS_EPWM13_G2	5008 D032h
CONTROLSS_EPWM14_G2	5008 E032h
CONTROLSS_EPWM15_G2	5008 F032h
CONTROLSS_EPWM16_G2	5009 0032h
CONTROLSS_EPWM17_G2	5009 1032h
CONTROLSS_EPWM18_G2	5009 2032h
CONTROLSS_EPWM19_G2	5009 3032h
CONTROLSS_EPWM2_G2	5008 2032h
CONTROLSS_EPWM20_G2	5009 4032h
CONTROLSS_EPWM21_G2	5009 5032h
CONTROLSS_EPWM22_G2	5009 6032h
CONTROLSS_EPWM23_G2	5009 7032h
CONTROLSS_EPWM24_G2	5009 8032h
CONTROLSS_EPWM25_G2	5009 9032h
CONTROLSS_EPWM26_G2	5009 A032h
CONTROLSS_EPWM27_G2	5009 B032h
CONTROLSS_EPWM28_G2	5009 C032h

Table 3-711. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM29_G2	5009 D032h
CONTROLSS_EPWM3_G2	5008 3032h
CONTROLSS_EPWM30_G2	5009 E032h
CONTROLSS_EPWM31_G2	5009 F032h
CONTROLSS_EPWM4_G2	5008 4032h
CONTROLSS_EPWM5_G2	5008 5032h
CONTROLSS_EPWM6_G2	5008 6032h
CONTROLSS_EPWM7_G2	5008 7032h
CONTROLSS_EPWM8_G2	5008 8032h
CONTROLSS_EPWM9_G2	5008 9032h
CONTROLSS_EPWM0_G3	500C 0032h
CONTROLSS_EPWM1_G3	500C 1032h
CONTROLSS_EPWM10_G3	500C A032h
CONTROLSS_EPWM11_G3	500C B032h
CONTROLSS_EPWM12_G3	500C C032h
CONTROLSS_EPWM13_G3	500C D032h
CONTROLSS_EPWM14_G3	500C E032h
CONTROLSS_EPWM15_G3	500C F032h
CONTROLSS_EPWM16_G3	500D 0032h
CONTROLSS_EPWM17_G3	500D 1032h
CONTROLSS_EPWM18_G3	500D 2032h
CONTROLSS_EPWM19_G3	500D 3032h
CONTROLSS_EPWM2_G3	500C 2032h
CONTROLSS_EPWM20_G3	500D 4032h
CONTROLSS_EPWM21_G3	500D 5032h
CONTROLSS_EPWM22_G3	500D 6032h
CONTROLSS_EPWM23_G3	500D 7032h
CONTROLSS_EPWM24_G3	500D 8032h
CONTROLSS_EPWM25_G3	500D 9032h
CONTROLSS_EPWM26_G3	500D A032h
CONTROLSS_EPWM27_G3	500D B032h
CONTROLSS_EPWM28_G3	500D C032h
CONTROLSS_EPWM29_G3	500D D032h
CONTROLSS_EPWM3_G3	500C 3032h
CONTROLSS_EPWM30_G3	500D E032h
CONTROLSS_EPWM31_G3	500D F032h
CONTROLSS_EPWM4_G3	500C 4032h
CONTROLSS_EPWM5_G3	500C 5032h
CONTROLSS_EPWM6_G3	500C 6032h
CONTROLSS_EPWM7_G3	500C 7032h
CONTROLSS_EPWM8_G3	500C 8032h
CONTROLSS_EPWM9_G3	500C 9032h

Figure 3-302. VCNTCFG Name Register

15	14	13	12	11	10	9	8
STOPEDGESTS	RESERVED_2			STOPEDGE			

Figure 3-302. VCNTCFG Name Register (continued)

R	R	R/W
0h	0h	0h

7	6	5	4	3	2	1	0
STARTEDGESTS	RESERVED_1			STARTEDGE			
R	R			R/W			
0h	0h			0h			

Access Types Legend

Table 3-712. VCNTCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	STOPEDGESTS	R	0h	Stop Edge Status Bit 0: Stop edge has not occurred 1: Stop edge occurred Note: This bit is set only after the trigger sequence is armed [upon occurrence of trigger pulse selected through VCAPCTL[TRIGSEL]] and STOPEDGE occurs. Note:This bit is reset by the occurrence of the trigger pulse selected through VCAPCTL[TRIGSEL] Reset Source: epwm_rst_mod_g_rst_n
14:12	RESERVED_2	R	0h	Reserved Reset Source: epwm_rst_mod_g_rst_n
11:8	STOPEDGE	R/W	0h	Counter Stop Edge Selection Once the counter operation is armed, upon occurrence of trigger pulse selected through VCAPCTL[TRIGSEL] pulse - valley counter would stop counting upon the occurrence of chosen number of events thorough this bit field. Stop counting on occurrence of: 0000: Do not stop 0001 1st edge 0010: 2nd edge 0011: 3rd edge ... 1,1,1,1: 15th edge Reset Source: epwm_rst_mod_g_rst_n
7	STARTEDGESTS	R	0h	Start Edge Status Bit 0: Start edge has not occurred 1: Start edge occurred Note: This bit is set only after the trigger sequence is armed [upon occurrence of trigger pulse selected through VCAPCTL[TRIGSEL]] and STARTEDGE occurs. Note:This bit is reset by the occurrence of the trigger pulse selected through VCAPCTL[TRIGSEL] Reset Source: epwm_rst_mod_g_rst_n
6:4	RESERVED_1	R	0h	Reserved Reset Source: epwm_rst_mod_g_rst_n
3:0	STARTEDGE	R/W	0h	Counter Start Edge Selection Once the counter operation is armed, upon occurrence of trigger pulse selected through VCAPCTL[TRIGSEL] pulse - valley counter would start counting upon the occurrence of chosen number of events thorough this bit field. Start counting on occurrence of 0000: Do not start 0001: 1st edge 0010: 2nd edge 0011: 3rd edge ... 1111: 15th edge Reset Source: epwm_rst_mod_g_rst_n

3.9.17 MEM_HRCNFG Registers

3.9.17.1 MEM_HRCNFG Register (Offset = 40h) [reset = 0h]

Short Description: HRPWM Configuration Regis

Long Description: HRPWM Configuration Register This register is only accessible on EPWM modules with HRPWM capabilities.

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Table 3-713. Instance Table

Instance Name	Physical Address
CONTROLSS_EPWM0_G0	5000 0040h
CONTROLSS_EPWM1_G0	5000 1040h
CONTROLSS_EPWM10_G0	5000 A040h
CONTROLSS_EPWM11_G0	5000 B040h
CONTROLSS_EPWM12_G0	5000 C040h
CONTROLSS_EPWM13_G0	5000 D040h
CONTROLSS_EPWM14_G0	5000 E040h
CONTROLSS_EPWM15_G0	5000 F040h
CONTROLSS_EPWM16_G0	5001 0040h
CONTROLSS_EPWM17_G0	5001 1040h
CONTROLSS_EPWM18_G0	5001 2040h
CONTROLSS_EPWM19_G0	5001 3040h
CONTROLSS_EPWM2_G0	5000 2040h
CONTROLSS_EPWM20_G0	5001 4040h
CONTROLSS_EPWM21_G0	5001 5040h
CONTROLSS_EPWM22_G0	5001 6040h
CONTROLSS_EPWM23_G0	5001 7040h
CONTROLSS_EPWM24_G0	5001 8040h
CONTROLSS_EPWM25_G0	5001 9040h
CONTROLSS_EPWM26_G0	5001 A040h
CONTROLSS_EPWM27_G0	5001 B040h
CONTROLSS_EPWM28_G0	5001 C040h
CONTROLSS_EPWM29_G0	5001 D040h
CONTROLSS_EPWM3_G0	5000 3040h
CONTROLSS_EPWM30_G0	5001 E040h
CONTROLSS_EPWM31_G0	5001 F040h
CONTROLSS_EPWM4_G0	5000 4040h
CONTROLSS_EPWM5_G0	5000 5040h
CONTROLSS_EPWM6_G0	5000 6040h
CONTROLSS_EPWM7_G0	5000 7040h
CONTROLSS_EPWM8_G0	5000 8040h
CONTROLSS_EPWM9_G0	5000 9040h
CONTROLSS_EPWM0_G1	5004 0040h
CONTROLSS_EPWM1_G1	5004 1040h
CONTROLSS_EPWM10_G1	5004 A040h
CONTROLSS_EPWM11_G1	5004 B040h
CONTROLSS_EPWM12_G1	5004 C040h
CONTROLSS_EPWM13_G1	5004 D040h

Table 3-713. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM14_G1	5004 E040h
CONTROLSS_EPWM15_G1	5004 F040h
CONTROLSS_EPWM16_G1	5005 0040h
CONTROLSS_EPWM17_G1	5005 1040h
CONTROLSS_EPWM18_G1	5005 2040h
CONTROLSS_EPWM19_G1	5005 3040h
CONTROLSS_EPWM2_G1	5004 2040h
CONTROLSS_EPWM20_G1	5005 4040h
CONTROLSS_EPWM21_G1	5005 5040h
CONTROLSS_EPWM22_G1	5005 6040h
CONTROLSS_EPWM23_G1	5005 7040h
CONTROLSS_EPWM24_G1	5005 8040h
CONTROLSS_EPWM25_G1	5005 9040h
CONTROLSS_EPWM26_G1	5005 A040h
CONTROLSS_EPWM27_G1	5005 B040h
CONTROLSS_EPWM28_G1	5005 C040h
CONTROLSS_EPWM29_G1	5005 D040h
CONTROLSS_EPWM3_G1	5004 3040h
CONTROLSS_EPWM30_G1	5005 E040h
CONTROLSS_EPWM31_G1	5005 F040h
CONTROLSS_EPWM4_G1	5004 4040h
CONTROLSS_EPWM5_G1	5004 5040h
CONTROLSS_EPWM6_G1	5004 6040h
CONTROLSS_EPWM7_G1	5004 7040h
CONTROLSS_EPWM8_G1	5004 8040h
CONTROLSS_EPWM9_G1	5004 9040h
CONTROLSS_EPWM0_G2	5008 0040h
CONTROLSS_EPWM1_G2	5008 1040h
CONTROLSS_EPWM10_G2	5008 A040h
CONTROLSS_EPWM11_G2	5008 B040h
CONTROLSS_EPWM12_G2	5008 C040h
CONTROLSS_EPWM13_G2	5008 D040h
CONTROLSS_EPWM14_G2	5008 E040h
CONTROLSS_EPWM15_G2	5008 F040h
CONTROLSS_EPWM16_G2	5009 0040h
CONTROLSS_EPWM17_G2	5009 1040h
CONTROLSS_EPWM18_G2	5009 2040h
CONTROLSS_EPWM19_G2	5009 3040h
CONTROLSS_EPWM2_G2	5008 2040h
CONTROLSS_EPWM20_G2	5009 4040h
CONTROLSS_EPWM21_G2	5009 5040h
CONTROLSS_EPWM22_G2	5009 6040h
CONTROLSS_EPWM23_G2	5009 7040h
CONTROLSS_EPWM24_G2	5009 8040h
CONTROLSS_EPWM25_G2	5009 9040h
CONTROLSS_EPWM26_G2	5009 A040h
CONTROLSS_EPWM27_G2	5009 B040h

Table 3-713. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM28_G2	5009 C040h
CONTROLSS_EPWM29_G2	5009 D040h
CONTROLSS_EPWM3_G2	5008 3040h
CONTROLSS_EPWM30_G2	5009 E040h
CONTROLSS_EPWM31_G2	5009 F040h
CONTROLSS_EPWM4_G2	5008 4040h
CONTROLSS_EPWM5_G2	5008 5040h
CONTROLSS_EPWM6_G2	5008 6040h
CONTROLSS_EPWM7_G2	5008 7040h
CONTROLSS_EPWM8_G2	5008 8040h
CONTROLSS_EPWM9_G2	5008 9040h
CONTROLSS_EPWM0_G3	500C 0040h
CONTROLSS_EPWM1_G3	500C 1040h
CONTROLSS_EPWM10_G3	500C A040h
CONTROLSS_EPWM11_G3	500C B040h
CONTROLSS_EPWM12_G3	500C C040h
CONTROLSS_EPWM13_G3	500C D040h
CONTROLSS_EPWM14_G3	500C E040h
CONTROLSS_EPWM15_G3	500C F040h
CONTROLSS_EPWM16_G3	500D 0040h
CONTROLSS_EPWM17_G3	500D 1040h
CONTROLSS_EPWM18_G3	500D 2040h
CONTROLSS_EPWM19_G3	500D 3040h
CONTROLSS_EPWM2_G3	500C 2040h
CONTROLSS_EPWM20_G3	500D 4040h
CONTROLSS_EPWM21_G3	500D 5040h
CONTROLSS_EPWM22_G3	500D 6040h
CONTROLSS_EPWM23_G3	500D 7040h
CONTROLSS_EPWM24_G3	500D 8040h
CONTROLSS_EPWM25_G3	500D 9040h
CONTROLSS_EPWM26_G3	500D A040h
CONTROLSS_EPWM27_G3	500D B040h
CONTROLSS_EPWM28_G3	500D C040h
CONTROLSS_EPWM29_G3	500D D040h
CONTROLSS_EPWM3_G3	500C 3040h
CONTROLSS_EPWM30_G3	500D E040h
CONTROLSS_EPWM31_G3	500D F040h
CONTROLSS_EPWM4_G3	500C 4040h
CONTROLSS_EPWM5_G3	500C 5040h
CONTROLSS_EPWM6_G3	500C 6040h
CONTROLSS_EPWM7_G3	500C 7040h
CONTROLSS_EPWM8_G3	500C 8040h
CONTROLSS_EPWM9_G3	500C 9040h

Figure 3-303. HRCNFG Name Register

15	14	13	12	11	10	9	8
LINESEL		RESERVED_1	HRLOADB		CTLMODEB	EDGMODEB	

Figure 3-303. HRCNFG Name Register (continued)

R/W		R	R/W		R/W	R/W	R/W
0h		0h	0h			0h	0h
7	6	5	4	3		2	1 0
SWAPAB	AUTOCONV	SELOUTB	HRLOAD			CTLMODE	EDGMODE
R/W	R/W	R/W	R/W			R/W	R/W
0h	0h	0h	0h			0h	0h

Access Types Legend

Table 3-714. HRCNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	LINESEL	R/W	0h	Delay Line Selection Bits: Selects which of the 4 delay lines for a particular ePWM/EPWM module to send to CALIN for calibration. Reset Source: epwm_rst_mod_g_rst_n
13	RESERVED_1	R	0h	Reserved Reset Source: epwm_rst_mod_g_rst_n
12:11	HRLOADB	R/W	0h	Shadow Mode Bit Selects the time event that loads the CMPBHR shadow value into the active register. 00: Load on CTR = Zero: Time-base counter equal to zero [TBCTR = 0x0000] 01: Load on CTR = PRD: Time-base counter equal to period [TBCTR = TBPRD] 10: Load on either CTR = Zero or CTR = PRD 11: Load on CMPB_EQ [Translator Event CMPB-3] Reset Source: epwm_rst_mod_g_rst_n
10	CTLMODEB	R/W	0h	Control Mode Bits Selects the register [CMP/TBPRD or TBPHS] that controls the MEP: 0: CMPBHR[8] or TBPRDHR[8] Register controls the edge position [i.e., this is duty or period control mode]. [Default on Reset] 1: TBPHSHR[8] Register controls the edge position [i.e., this is phase control mode]. Reset Source: epwm_rst_mod_g_rst_n
9:8	EDGMODEB	R/W	0h	Edge Mode Bits Selects the edge of the PWM that is controlled by the micro-edge position [MEP] logic: 00: HRPWM capability is disabled [default on reset] 01: MEP control of rising edge [CMPBHR] 10: MEP control of falling edge [CMPBHR] 11: MEP control of both edges [TBPHSHR or TBPRDHR] Reset Source: epwm_rst_mod_g_rst_n
7	SWAPAB	R/W	0h	Swap ePWM A & B Output Signals This bit enables the swapping of the A & B signal outputs. The selection is as follows: 0: ePWMxA and ePWMxB outputs are unchanged. 1: ePWMxA signal appears on ePWMxB output and ePWMxB signal appears on ePWMxA output. Reset Source: epwm_rst_mod_g_rst_n
6	AUTOCONV	R/W	0h	Auto Convert Delay Line Value Selects whether the fractional duty cycle/period/phase in the CMPAHR/TBPRDHR/TBPHSHR register is automatically scaled by the MEP scale factor in the HRMSTEP register or manually scaled by calculations in application software. The SFO library function automatically updates the HRMSTEP register with the appropriate MEP scale factor. 0: Automatic HRMSTEP scaling is disabled. 1: Automatic HRMSTEP scaling is enabled. If application software is manually scaling the fractional duty cycle, or phase [i.e. software sets CMPAHR = [fraction[PWMduty * PWMperiod] * MEP Scale Factor]<<8 + 0x080 for duty cycle], then this mode must be disabled. Reset Source: epwm_rst_mod_g_rst_n
5	SELOUTB	R/W	0h	EPWMxB Output Select Bit This bit selects which signal is output on the ePWMxB channel output. The inversion will take the high resolution mode into account and the inverted signal will contain any high resolution modification. The inversion takes place as the last step in modifying the ePWMxB signal. 0: ePWMxB output is normal. 1: ePWMxB output is inverted version of ePWMxA signal. Reset Source: epwm_rst_mod_g_rst_n

Table 3-714. HRCNFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:3	HRLOAD	R/W	0h	Shadow Mode Bit Selects the time event that loads the CMPAHR shadow value into the active register. 00: Load on CTR = Zero: Time-base counter equal to zero [TBCTR = 0x0000] 01: Load on CTR = PRD: Time-base counter equal to period [TBCTR = TBPRD] 10: Load on either CTR = Zero or CTR = PRD 11: Load on CMPA_EQ [Translator Event CMPA-3] Reset Source: epwm_rst_mod_g_rst_n
2	CTLMODE	R/W	0h	Control Mode Bits Selects the register [CMP/TBPRD or TBPHS] that controls the MEP: 0: CMPAHR[8] or TBPRDHR[8] Register controls the edge position [i.e., this is duty or period control mode]. [Default on Reset] 1: TBPHSHR[8] Register controls the edge position [i.e., this is phase control mode]. Reset Source: epwm_rst_mod_g_rst_n
1:0	EDGMODE	R/W	0h	Edge Mode Bits Selects the edge of the PWM that is controlled by the micro-edge position [MEP] logic: 00: HRPWM capability is disabled [default on reset] 01: MEP control of rising edge [CMPAHR] 10: MEP control of falling edge [CMPAHR] 11: MEP control of both edges [TBPHSHR or TBPRDHR] Reset Source: epwm_rst_mod_g_rst_n

3.9.18 MEM_HRCNFG2 Registers

3.9.18.1 MEM_HRCNFG2 Register (Offset = 4Eh) [reset = 0h]

Short Description: HRPWM Configuration 2 Reg

Long Description: HRPWM Configuration 2 Register This register is only accessible on EPWM modules with HRPWM capabilities. Only 16 bit accesses are allowed for this register. Debugger access in 32 bit mode may display incorrect values.

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Table 3-715. Instance Table

Instance Name	Physical Address
CONTROLSS_EPWM0_G0	5000 004Eh
CONTROLSS_EPWM1_G0	5000 104Eh
CONTROLSS_EPWM10_G0	5000 A04Eh
CONTROLSS_EPWM11_G0	5000 B04Eh
CONTROLSS_EPWM12_G0	5000 C04Eh
CONTROLSS_EPWM13_G0	5000 D04Eh
CONTROLSS_EPWM14_G0	5000 E04Eh
CONTROLSS_EPWM15_G0	5000 F04Eh
CONTROLSS_EPWM16_G0	5001 004Eh
CONTROLSS_EPWM17_G0	5001 104Eh
CONTROLSS_EPWM18_G0	5001 204Eh
CONTROLSS_EPWM19_G0	5001 304Eh
CONTROLSS_EPWM2_G0	5000 204Eh
CONTROLSS_EPWM20_G0	5001 404Eh
CONTROLSS_EPWM21_G0	5001 504Eh
CONTROLSS_EPWM22_G0	5001 604Eh
CONTROLSS_EPWM23_G0	5001 704Eh
CONTROLSS_EPWM24_G0	5001 804Eh
CONTROLSS_EPWM25_G0	5001 904Eh
CONTROLSS_EPWM26_G0	5001 A04Eh
CONTROLSS_EPWM27_G0	5001 B04Eh
CONTROLSS_EPWM28_G0	5001 C04Eh
CONTROLSS_EPWM29_G0	5001 D04Eh
CONTROLSS_EPWM3_G0	5000 304Eh
CONTROLSS_EPWM30_G0	5001 E04Eh
CONTROLSS_EPWM31_G0	5001 F04Eh
CONTROLSS_EPWM4_G0	5000 404Eh
CONTROLSS_EPWM5_G0	5000 504Eh
CONTROLSS_EPWM6_G0	5000 604Eh
CONTROLSS_EPWM7_G0	5000 704Eh
CONTROLSS_EPWM8_G0	5000 804Eh
CONTROLSS_EPWM9_G0	5000 904Eh
CONTROLSS_EPWM0_G1	5004 004Eh
CONTROLSS_EPWM1_G1	5004 104Eh
CONTROLSS_EPWM10_G1	5004 A04Eh
CONTROLSS_EPWM11_G1	5004 B04Eh
CONTROLSS_EPWM12_G1	5004 C04Eh
CONTROLSS_EPWM13_G1	5004 D04Eh

Table 3-715. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM14_G1	5004 E04Eh
CONTROLSS_EPWM15_G1	5004 F04Eh
CONTROLSS_EPWM16_G1	5005 004Eh
CONTROLSS_EPWM17_G1	5005 104Eh
CONTROLSS_EPWM18_G1	5005 204Eh
CONTROLSS_EPWM19_G1	5005 304Eh
CONTROLSS_EPWM2_G1	5004 204Eh
CONTROLSS_EPWM20_G1	5005 404Eh
CONTROLSS_EPWM21_G1	5005 504Eh
CONTROLSS_EPWM22_G1	5005 604Eh
CONTROLSS_EPWM23_G1	5005 704Eh
CONTROLSS_EPWM24_G1	5005 804Eh
CONTROLSS_EPWM25_G1	5005 904Eh
CONTROLSS_EPWM26_G1	5005 A04Eh
CONTROLSS_EPWM27_G1	5005 B04Eh
CONTROLSS_EPWM28_G1	5005 C04Eh
CONTROLSS_EPWM29_G1	5005 D04Eh
CONTROLSS_EPWM3_G1	5004 304Eh
CONTROLSS_EPWM30_G1	5005 E04Eh
CONTROLSS_EPWM31_G1	5005 F04Eh
CONTROLSS_EPWM4_G1	5004 404Eh
CONTROLSS_EPWM5_G1	5004 504Eh
CONTROLSS_EPWM6_G1	5004 604Eh
CONTROLSS_EPWM7_G1	5004 704Eh
CONTROLSS_EPWM8_G1	5004 804Eh
CONTROLSS_EPWM9_G1	5004 904Eh
CONTROLSS_EPWM0_G2	5008 004Eh
CONTROLSS_EPWM1_G2	5008 104Eh
CONTROLSS_EPWM10_G2	5008 A04Eh
CONTROLSS_EPWM11_G2	5008 B04Eh
CONTROLSS_EPWM12_G2	5008 C04Eh
CONTROLSS_EPWM13_G2	5008 D04Eh
CONTROLSS_EPWM14_G2	5008 E04Eh
CONTROLSS_EPWM15_G2	5008 F04Eh
CONTROLSS_EPWM16_G2	5009 004Eh
CONTROLSS_EPWM17_G2	5009 104Eh
CONTROLSS_EPWM18_G2	5009 204Eh
CONTROLSS_EPWM19_G2	5009 304Eh
CONTROLSS_EPWM2_G2	5008 204Eh
CONTROLSS_EPWM20_G2	5009 404Eh
CONTROLSS_EPWM21_G2	5009 504Eh
CONTROLSS_EPWM22_G2	5009 604Eh
CONTROLSS_EPWM23_G2	5009 704Eh
CONTROLSS_EPWM24_G2	5009 804Eh
CONTROLSS_EPWM25_G2	5009 904Eh
CONTROLSS_EPWM26_G2	5009 A04Eh
CONTROLSS_EPWM27_G2	5009 B04Eh

Table 3-715. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM28_G2	5009 C04Eh
CONTROLSS_EPWM29_G2	5009 D04Eh
CONTROLSS_EPWM3_G2	5008 304Eh
CONTROLSS_EPWM30_G2	5009 E04Eh
CONTROLSS_EPWM31_G2	5009 F04Eh
CONTROLSS_EPWM4_G2	5008 404Eh
CONTROLSS_EPWM5_G2	5008 504Eh
CONTROLSS_EPWM6_G2	5008 604Eh
CONTROLSS_EPWM7_G2	5008 704Eh
CONTROLSS_EPWM8_G2	5008 804Eh
CONTROLSS_EPWM9_G2	5008 904Eh
CONTROLSS_EPWM0_G3	500C 004Eh
CONTROLSS_EPWM1_G3	500C 104Eh
CONTROLSS_EPWM10_G3	500C A04Eh
CONTROLSS_EPWM11_G3	500C B04Eh
CONTROLSS_EPWM12_G3	500C C04Eh
CONTROLSS_EPWM13_G3	500C D04Eh
CONTROLSS_EPWM14_G3	500C E04Eh
CONTROLSS_EPWM15_G3	500C F04Eh
CONTROLSS_EPWM16_G3	500D 004Eh
CONTROLSS_EPWM17_G3	500D 104Eh
CONTROLSS_EPWM18_G3	500D 204Eh
CONTROLSS_EPWM19_G3	500D 304Eh
CONTROLSS_EPWM2_G3	500C 204Eh
CONTROLSS_EPWM20_G3	500D 404Eh
CONTROLSS_EPWM21_G3	500D 504Eh
CONTROLSS_EPWM22_G3	500D 604Eh
CONTROLSS_EPWM23_G3	500D 704Eh
CONTROLSS_EPWM24_G3	500D 804Eh
CONTROLSS_EPWM25_G3	500D 904Eh
CONTROLSS_EPWM26_G3	500D A04Eh
CONTROLSS_EPWM27_G3	500D B04Eh
CONTROLSS_EPWM28_G3	500D C04Eh
CONTROLSS_EPWM29_G3	500D D04Eh
CONTROLSS_EPWM3_G3	500C 304Eh
CONTROLSS_EPWM30_G3	500D E04Eh
CONTROLSS_EPWM31_G3	500D F04Eh
CONTROLSS_EPWM4_G3	500C 404Eh
CONTROLSS_EPWM5_G3	500C 504Eh
CONTROLSS_EPWM6_G3	500C 604Eh
CONTROLSS_EPWM7_G3	500C 704Eh
CONTROLSS_EPWM8_G3	500C 804Eh
CONTROLSS_EPWM9_G3	500C 904Eh

Figure 3-304. HRCNFG2 Name Register

15	14	13	12	11	10	9	8
NOBYPASS	DELLOADFRC	RESERVED_1					

Figure 3-304. HRCNFG2 Name Register (continued)

R/W	R/W	R					
0h	0h	0h					
7	6	5	4	3	2	1	0
RESERVED_1		CTLMODEDBFED		CTLMODEDBRED		EDGMODEDB	
R		R/W		R/W		R/W	
0h		0h		0h		0h	

Access Types Legend

Table 3-716. HRCNFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	NOBYPASS	R/W	0h	No Bypass Delay Line Update Bit: For internal test purposes, this bit disables the 1 SYSCLK cycle bypass before delay line is updated. Reset Source: epwm_rst_mod_g_rst_n
14	DELLOADFRC	R/W	0h	Delay Line Load Software Force: For internal test purposes, software force generates a pulse which forces a delay line update [similar to PRD_eq/CNT_zero strobe]. Reset Source: epwm_rst_mod_g_rst_n
13:6	RESERVED_1	R	0h	Reserved Reset Source: epwm_rst_mod_g_rst_n
5:4	CTLMODEDBFED	R/W	0h	Shadow Mode Bit - selection should match DBCTL[LOADFEDMODE] Selects the time event that loads the DBFEDHR shadow value into the active register. 00 Load on CTR = Zero: Time-base counter equal to zero [TBCTR = 0x0000] 01 Load on CTR = PRD: Time-base counter equal to period [TBCTR = TBPRD] 10 Load on either CTR = Zero or CTR = PRD 11 Reserved Reset Source: epwm_rst_mod_g_rst_n
3:2	CTLMODEDBRED	R/W	0h	Shadow Mode Bit - selection should match DBCTL[LOADREDMODE] Selects the time event that loads the DBREDHR shadow value into the active register. 00 Load on CTR = Zero: Time-base counter equal to zero [TBCTR = 0x0000] 01 Load on CTR = PRD: Time-base counter equal to period [TBCTR = TBPRD] 10 Load on either CTR = Zero or CTR = PRD 11 Reserved Reset Source: epwm_rst_mod_g_rst_n
1:0	EDGMODEDB	R/W	0h	Edge Mode Bits Selects the edge of the PWM that is controlled by the micro-edge position [MEP] logic: 00 HRPWM capability is disabled [default on reset] 01 MEP control of rising edge [DBREDHR] 10 MEP control of falling edge [DBFEDHR] 11 MEP control of both edges [rising edge of DBREDHR or falling edge of DBFEDHR] Reset Source: epwm_rst_mod_g_rst_n

3.9.19 MEM_HRPCTL Registers

3.9.19.1 MEM_HRPCTL Register (Offset = 5Ah) [reset = 0h]

Short Description: High Resolution Period Co

Long Description: High Resolution Period Control Register This register is only accessible on EPWM modules with HRPWM capabilities.

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Table 3-717. Instance Table

Instance Name	Physical Address
CONTROLSS_EPWM0_G0	5000 005Ah
CONTROLSS_EPWM1_G0	5000 105Ah
CONTROLSS_EPWM10_G0	5000 A05Ah
CONTROLSS_EPWM11_G0	5000 B05Ah
CONTROLSS_EPWM12_G0	5000 C05Ah
CONTROLSS_EPWM13_G0	5000 D05Ah
CONTROLSS_EPWM14_G0	5000 E05Ah
CONTROLSS_EPWM15_G0	5000 F05Ah
CONTROLSS_EPWM16_G0	5001 005Ah
CONTROLSS_EPWM17_G0	5001 105Ah
CONTROLSS_EPWM18_G0	5001 205Ah
CONTROLSS_EPWM19_G0	5001 305Ah
CONTROLSS_EPWM2_G0	5000 205Ah
CONTROLSS_EPWM20_G0	5001 405Ah
CONTROLSS_EPWM21_G0	5001 505Ah
CONTROLSS_EPWM22_G0	5001 605Ah
CONTROLSS_EPWM23_G0	5001 705Ah
CONTROLSS_EPWM24_G0	5001 805Ah
CONTROLSS_EPWM25_G0	5001 905Ah
CONTROLSS_EPWM26_G0	5001 A05Ah
CONTROLSS_EPWM27_G0	5001 B05Ah
CONTROLSS_EPWM28_G0	5001 C05Ah
CONTROLSS_EPWM29_G0	5001 D05Ah
CONTROLSS_EPWM3_G0	5000 305Ah
CONTROLSS_EPWM30_G0	5001 E05Ah
CONTROLSS_EPWM31_G0	5001 F05Ah
CONTROLSS_EPWM4_G0	5000 405Ah
CONTROLSS_EPWM5_G0	5000 505Ah
CONTROLSS_EPWM6_G0	5000 605Ah
CONTROLSS_EPWM7_G0	5000 705Ah
CONTROLSS_EPWM8_G0	5000 805Ah
CONTROLSS_EPWM9_G0	5000 905Ah
CONTROLSS_EPWM0_G1	5004 005Ah
CONTROLSS_EPWM1_G1	5004 105Ah
CONTROLSS_EPWM10_G1	5004 A05Ah
CONTROLSS_EPWM11_G1	5004 B05Ah
CONTROLSS_EPWM12_G1	5004 C05Ah
CONTROLSS_EPWM13_G1	5004 D05Ah

Table 3-717. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM14_G1	5004 E05Ah
CONTROLSS_EPWM15_G1	5004 F05Ah
CONTROLSS_EPWM16_G1	5005 005Ah
CONTROLSS_EPWM17_G1	5005 105Ah
CONTROLSS_EPWM18_G1	5005 205Ah
CONTROLSS_EPWM19_G1	5005 305Ah
CONTROLSS_EPWM2_G1	5004 205Ah
CONTROLSS_EPWM20_G1	5005 405Ah
CONTROLSS_EPWM21_G1	5005 505Ah
CONTROLSS_EPWM22_G1	5005 605Ah
CONTROLSS_EPWM23_G1	5005 705Ah
CONTROLSS_EPWM24_G1	5005 805Ah
CONTROLSS_EPWM25_G1	5005 905Ah
CONTROLSS_EPWM26_G1	5005 A05Ah
CONTROLSS_EPWM27_G1	5005 B05Ah
CONTROLSS_EPWM28_G1	5005 C05Ah
CONTROLSS_EPWM29_G1	5005 D05Ah
CONTROLSS_EPWM3_G1	5004 305Ah
CONTROLSS_EPWM30_G1	5005 E05Ah
CONTROLSS_EPWM31_G1	5005 F05Ah
CONTROLSS_EPWM4_G1	5004 405Ah
CONTROLSS_EPWM5_G1	5004 505Ah
CONTROLSS_EPWM6_G1	5004 605Ah
CONTROLSS_EPWM7_G1	5004 705Ah
CONTROLSS_EPWM8_G1	5004 805Ah
CONTROLSS_EPWM9_G1	5004 905Ah
CONTROLSS_EPWM0_G2	5008 005Ah
CONTROLSS_EPWM1_G2	5008 105Ah
CONTROLSS_EPWM10_G2	5008 A05Ah
CONTROLSS_EPWM11_G2	5008 B05Ah
CONTROLSS_EPWM12_G2	5008 C05Ah
CONTROLSS_EPWM13_G2	5008 D05Ah
CONTROLSS_EPWM14_G2	5008 E05Ah
CONTROLSS_EPWM15_G2	5008 F05Ah
CONTROLSS_EPWM16_G2	5009 005Ah
CONTROLSS_EPWM17_G2	5009 105Ah
CONTROLSS_EPWM18_G2	5009 205Ah
CONTROLSS_EPWM19_G2	5009 305Ah
CONTROLSS_EPWM2_G2	5008 205Ah
CONTROLSS_EPWM20_G2	5009 405Ah
CONTROLSS_EPWM21_G2	5009 505Ah
CONTROLSS_EPWM22_G2	5009 605Ah
CONTROLSS_EPWM23_G2	5009 705Ah
CONTROLSS_EPWM24_G2	5009 805Ah
CONTROLSS_EPWM25_G2	5009 905Ah
CONTROLSS_EPWM26_G2	5009 A05Ah
CONTROLSS_EPWM27_G2	5009 B05Ah

Table 3-717. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM28_G2	5009 C05Ah
CONTROLSS_EPWM29_G2	5009 D05Ah
CONTROLSS_EPWM3_G2	5008 305Ah
CONTROLSS_EPWM30_G2	5009 E05Ah
CONTROLSS_EPWM31_G2	5009 F05Ah
CONTROLSS_EPWM4_G2	5008 405Ah
CONTROLSS_EPWM5_G2	5008 505Ah
CONTROLSS_EPWM6_G2	5008 605Ah
CONTROLSS_EPWM7_G2	5008 705Ah
CONTROLSS_EPWM8_G2	5008 805Ah
CONTROLSS_EPWM9_G2	5008 905Ah
CONTROLSS_EPWM0_G3	500C 005Ah
CONTROLSS_EPWM1_G3	500C 105Ah
CONTROLSS_EPWM10_G3	500C A05Ah
CONTROLSS_EPWM11_G3	500C B05Ah
CONTROLSS_EPWM12_G3	500C C05Ah
CONTROLSS_EPWM13_G3	500C D05Ah
CONTROLSS_EPWM14_G3	500C E05Ah
CONTROLSS_EPWM15_G3	500C F05Ah
CONTROLSS_EPWM16_G3	500D 005Ah
CONTROLSS_EPWM17_G3	500D 105Ah
CONTROLSS_EPWM18_G3	500D 205Ah
CONTROLSS_EPWM19_G3	500D 305Ah
CONTROLSS_EPWM2_G3	500C 205Ah
CONTROLSS_EPWM20_G3	500D 405Ah
CONTROLSS_EPWM21_G3	500D 505Ah
CONTROLSS_EPWM22_G3	500D 605Ah
CONTROLSS_EPWM23_G3	500D 705Ah
CONTROLSS_EPWM24_G3	500D 805Ah
CONTROLSS_EPWM25_G3	500D 905Ah
CONTROLSS_EPWM26_G3	500D A05Ah
CONTROLSS_EPWM27_G3	500D B05Ah
CONTROLSS_EPWM28_G3	500D C05Ah
CONTROLSS_EPWM29_G3	500D D05Ah
CONTROLSS_EPWM3_G3	500C 305Ah
CONTROLSS_EPWM30_G3	500D E05Ah
CONTROLSS_EPWM31_G3	500D F05Ah
CONTROLSS_EPWM4_G3	500C 405Ah
CONTROLSS_EPWM5_G3	500C 505Ah
CONTROLSS_EPWM6_G3	500C 605Ah
CONTROLSS_EPWM7_G3	500C 705Ah
CONTROLSS_EPWM8_G3	500C 805Ah
CONTROLSS_EPWM9_G3	500C 905Ah

Figure 3-305. HRPCTL Name Register

15	14	13	12	11	10	9	8
RESERVED_1							

Figure 3-305. HRPCTL Name Register (continued)

R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1	PWMSYNCSELX			HRPSYNCE	TBPHSHRLOADE	PWMSYNCSEL	HRPE
R	R/W			R/W	R/W	R/W	R/W
0h	0h			0h	0h	0h	0h

Access Types Legend

Table 3-718. HRPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:7	RESERVED_1	R	0h	Reserved Reset Source: epwm_rst_mod_g_rst_n
6:4	PWMSYNCSELX	R/W	0h	Extended selection bits for EPWMSYNCPER 000: EPWMSYNCPER is defined by PWMSYNCSEL - ' default condition [compatible with previous EPWM versions] 001: Reserved 010: Reserved 011: Reserved 100: CTR = CMPC, Count direction Up 101: CTR = CMPC, Count direction Down 110: CTR = CMPD, Count direction Up 111: CTR = CMPD, Count direction Down Reset Source: epwm_rst_mod_g_rst_n
3	HRPSYNCE	R/W	0h	SYNC Enable Bit [TRSYNCE]/High Resolution Period SYNC Enable Bit [HRPSYNCE] Reset Source: epwm_rst_mod_g_rst_n
2	TBPHSHRLOADE	R/W	0h	TBPHSHR Load Enable This bit allows you to synchronize ePWM modules with a high-resolution phase on a SYNCIN, TBCTL[SWFSYNC] or digital compare event. This allows for multiple ePWM modules operating at the same frequency to be phase aligned with high-resolution. 0: Disables synchronization of high-resolution phase on a SYNCIN, TBCTL[SWFSYNC] or digital compare event: 1: Synchronize the high-resolution phase on a SYNCIN, TBCTL[SWFSYNC] or digital comparator synchronization event. The phase is synchronized using the contents of the high-resolution phase TBPHSHR register. The TBCTL[PHSEN] bit which enables the loading of the TBCTR register with TBPHS register value on a SYNCIN or TBCTL[SWFSYNC] event works independently. However, users need to enable this bit also if they want to control phase in conjunction with the high-resolution period feature. This bit and the TBCTL[PHSEN] bit must be set to 1 when high-resolution period is enabled for up-down count mode even if TBPHSHR = 0x0000. This bit does not need to be set when only high-resolution duty is enabled. Reset Source: epwm_rst_mod_g_rst_n
1	PWMSYNCSEL	R/W	0h	PWMSYNC Source Select Bit: This bit selects the source for the EPWMSYNCPER signal that goes to the CMPSS and GPDAC: 0 CTR = PRD: Time-base counter equal to period [TBCTR = TBPRD] 1 CTR = zero: Time-base counter equal to zero [TBCTR = 0x00] Reset Source: epwm_rst_mod_g_rst_n
0	HRPE	R/W	0h	High Resolution Period Enable Bit 0: High resolution period feature disabled. In this mode the ePWM behaves as a Type 0 ePWM. 1: High resolution period enabled. In this mode the HRPWM module can control high-resolution of both the duty and frequency. When high-resolution period is enabled, TBCTL[CTRMODE] = 0,1 [down-count mode] is not supported. Reset Source: epwm_rst_mod_g_rst_n

3.9.20 MEM_TRREM Registers

3.9.20.1 MEM_TRREM Register (Offset = 5Ch) [reset = 0h]

Short Description: HRPWM High Resolution Rem

Long Description: HRPWM High Resolution Remainder Register This register is only accessible on EPWM modules with HRPWM capabilities.

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Table 3-719. Instance Table

Instance Name	Physical Address
CONTROLSS_EPWM0_G0	5000 005Ch
CONTROLSS_EPWM1_G0	5000 105Ch
CONTROLSS_EPWM10_G0	5000 A05Ch
CONTROLSS_EPWM11_G0	5000 B05Ch
CONTROLSS_EPWM12_G0	5000 C05Ch
CONTROLSS_EPWM13_G0	5000 D05Ch
CONTROLSS_EPWM14_G0	5000 E05Ch
CONTROLSS_EPWM15_G0	5000 F05Ch
CONTROLSS_EPWM16_G0	5001 005Ch
CONTROLSS_EPWM17_G0	5001 105Ch
CONTROLSS_EPWM18_G0	5001 205Ch
CONTROLSS_EPWM19_G0	5001 305Ch
CONTROLSS_EPWM2_G0	5000 205Ch
CONTROLSS_EPWM20_G0	5001 405Ch
CONTROLSS_EPWM21_G0	5001 505Ch
CONTROLSS_EPWM22_G0	5001 605Ch
CONTROLSS_EPWM23_G0	5001 705Ch
CONTROLSS_EPWM24_G0	5001 805Ch
CONTROLSS_EPWM25_G0	5001 905Ch
CONTROLSS_EPWM26_G0	5001 A05Ch
CONTROLSS_EPWM27_G0	5001 B05Ch
CONTROLSS_EPWM28_G0	5001 C05Ch
CONTROLSS_EPWM29_G0	5001 D05Ch
CONTROLSS_EPWM3_G0	5000 305Ch
CONTROLSS_EPWM30_G0	5001 E05Ch
CONTROLSS_EPWM31_G0	5001 F05Ch
CONTROLSS_EPWM4_G0	5000 405Ch
CONTROLSS_EPWM5_G0	5000 505Ch
CONTROLSS_EPWM6_G0	5000 605Ch
CONTROLSS_EPWM7_G0	5000 705Ch
CONTROLSS_EPWM8_G0	5000 805Ch
CONTROLSS_EPWM9_G0	5000 905Ch
CONTROLSS_EPWM0_G1	5004 005Ch
CONTROLSS_EPWM1_G1	5004 105Ch
CONTROLSS_EPWM10_G1	5004 A05Ch
CONTROLSS_EPWM11_G1	5004 B05Ch
CONTROLSS_EPWM12_G1	5004 C05Ch
CONTROLSS_EPWM13_G1	5004 D05Ch

Table 3-719. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM14_G1	5004 E05Ch
CONTROLSS_EPWM15_G1	5004 F05Ch
CONTROLSS_EPWM16_G1	5005 005Ch
CONTROLSS_EPWM17_G1	5005 105Ch
CONTROLSS_EPWM18_G1	5005 205Ch
CONTROLSS_EPWM19_G1	5005 305Ch
CONTROLSS_EPWM2_G1	5004 205Ch
CONTROLSS_EPWM20_G1	5005 405Ch
CONTROLSS_EPWM21_G1	5005 505Ch
CONTROLSS_EPWM22_G1	5005 605Ch
CONTROLSS_EPWM23_G1	5005 705Ch
CONTROLSS_EPWM24_G1	5005 805Ch
CONTROLSS_EPWM25_G1	5005 905Ch
CONTROLSS_EPWM26_G1	5005 A05Ch
CONTROLSS_EPWM27_G1	5005 B05Ch
CONTROLSS_EPWM28_G1	5005 C05Ch
CONTROLSS_EPWM29_G1	5005 D05Ch
CONTROLSS_EPWM3_G1	5004 305Ch
CONTROLSS_EPWM30_G1	5005 E05Ch
CONTROLSS_EPWM31_G1	5005 F05Ch
CONTROLSS_EPWM4_G1	5004 405Ch
CONTROLSS_EPWM5_G1	5004 505Ch
CONTROLSS_EPWM6_G1	5004 605Ch
CONTROLSS_EPWM7_G1	5004 705Ch
CONTROLSS_EPWM8_G1	5004 805Ch
CONTROLSS_EPWM9_G1	5004 905Ch
CONTROLSS_EPWM0_G2	5008 005Ch
CONTROLSS_EPWM1_G2	5008 105Ch
CONTROLSS_EPWM10_G2	5008 A05Ch
CONTROLSS_EPWM11_G2	5008 B05Ch
CONTROLSS_EPWM12_G2	5008 C05Ch
CONTROLSS_EPWM13_G2	5008 D05Ch
CONTROLSS_EPWM14_G2	5008 E05Ch
CONTROLSS_EPWM15_G2	5008 F05Ch
CONTROLSS_EPWM16_G2	5009 005Ch
CONTROLSS_EPWM17_G2	5009 105Ch
CONTROLSS_EPWM18_G2	5009 205Ch
CONTROLSS_EPWM19_G2	5009 305Ch
CONTROLSS_EPWM2_G2	5008 205Ch
CONTROLSS_EPWM20_G2	5009 405Ch
CONTROLSS_EPWM21_G2	5009 505Ch
CONTROLSS_EPWM22_G2	5009 605Ch
CONTROLSS_EPWM23_G2	5009 705Ch
CONTROLSS_EPWM24_G2	5009 805Ch
CONTROLSS_EPWM25_G2	5009 905Ch
CONTROLSS_EPWM26_G2	5009 A05Ch
CONTROLSS_EPWM27_G2	5009 B05Ch

Table 3-719. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM28_G2	5009 C05Ch
CONTROLSS_EPWM29_G2	5009 D05Ch
CONTROLSS_EPWM3_G2	5008 305Ch
CONTROLSS_EPWM30_G2	5009 E05Ch
CONTROLSS_EPWM31_G2	5009 F05Ch
CONTROLSS_EPWM4_G2	5008 405Ch
CONTROLSS_EPWM5_G2	5008 505Ch
CONTROLSS_EPWM6_G2	5008 605Ch
CONTROLSS_EPWM7_G2	5008 705Ch
CONTROLSS_EPWM8_G2	5008 805Ch
CONTROLSS_EPWM9_G2	5008 905Ch
CONTROLSS_EPWM0_G3	500C 005Ch
CONTROLSS_EPWM1_G3	500C 105Ch
CONTROLSS_EPWM10_G3	500C A05Ch
CONTROLSS_EPWM11_G3	500C B05Ch
CONTROLSS_EPWM12_G3	500C C05Ch
CONTROLSS_EPWM13_G3	500C D05Ch
CONTROLSS_EPWM14_G3	500C E05Ch
CONTROLSS_EPWM15_G3	500C F05Ch
CONTROLSS_EPWM16_G3	500D 005Ch
CONTROLSS_EPWM17_G3	500D 105Ch
CONTROLSS_EPWM18_G3	500D 205Ch
CONTROLSS_EPWM19_G3	500D 305Ch
CONTROLSS_EPWM2_G3	500C 205Ch
CONTROLSS_EPWM20_G3	500D 405Ch
CONTROLSS_EPWM21_G3	500D 505Ch
CONTROLSS_EPWM22_G3	500D 605Ch
CONTROLSS_EPWM23_G3	500D 705Ch
CONTROLSS_EPWM24_G3	500D 805Ch
CONTROLSS_EPWM25_G3	500D 905Ch
CONTROLSS_EPWM26_G3	500D A05Ch
CONTROLSS_EPWM27_G3	500D B05Ch
CONTROLSS_EPWM28_G3	500D C05Ch
CONTROLSS_EPWM29_G3	500D D05Ch
CONTROLSS_EPWM3_G3	500C 305Ch
CONTROLSS_EPWM30_G3	500D E05Ch
CONTROLSS_EPWM31_G3	500D F05Ch
CONTROLSS_EPWM4_G3	500C 405Ch
CONTROLSS_EPWM5_G3	500C 505Ch
CONTROLSS_EPWM6_G3	500C 605Ch
CONTROLSS_EPWM7_G3	500C 705Ch
CONTROLSS_EPWM8_G3	500C 805Ch
CONTROLSS_EPWM9_G3	500C 905Ch

Figure 3-306. TRREM Name Register

15	14	13	12	11	10	9	8
RESERVED_1					TRREM		

Figure 3-306. TRREM Name Register (continued)

R						R/W	
0h						0h	
7	6	5	4	3	2	1	0
TRREM							
R/W							
0h							

Access Types Legend

Table 3-720. TRREM Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED_1	R	0h	Reserved Reset Source: epwm_rst_mod_g_rst_n
10:0	TRREM	R/W	0h	HRPWM Remainder Bits: This 11-bit value keeps track of the remainder portion of the HRPWM algorithm calculations. This value keeps track of the remainder portion of the HRPWM hardware calculations. Notes: 1. The lower 8-bits of the TRREM register can be automatically initialized with the TBPHSHR value on a SYNCIN or TBCTL[SWFSYNC] event or DC event [if enabled]. The user can also write a value with the CPU. 2. Priority of TRREM register updates: Sync [software or hardware] TBPHSHR copied to TRREM : Highest Priority HRPWM Hardware [updates TRREM register]: Next priority CPU Write To TRREM Register: Lowest Priority 3. Bit 10 of TRREM register is not used in asymmetrical mode. This bit can be forced to zero. TRREM will be initialized to 0x0 and 0x100 in Up and Up-down modes respectively. Asymmetrical Mode: TRREM[7:0] = TBPHSHR[15:8] TRREM[10,9,8] = 0,0,0 Symmetrical Mode: TRREM[7:0] = TBPHSHR[15:8] TRREM[10,9,8] = 0,0,1 Reset Source: epwm_rst_mod_g_rst_n

3.9.21 MEM_GLDCTL Registers

3.9.21.1 MEM_GLDCTL Register (Offset = 68h) [reset = 0h]

Short Description: Global PWM Load Control R

Long Description: Global PWM Load Control Register

Return to Summary Table

Table 3-721. Instance Table

Instance Name	Physical Address
CONTROLSS_EPWM0_G0	5000 0068h
CONTROLSS_EPWM1_G0	5000 1068h
CONTROLSS_EPWM10_G0	5000 A068h
CONTROLSS_EPWM11_G0	5000 B068h
CONTROLSS_EPWM12_G0	5000 C068h
CONTROLSS_EPWM13_G0	5000 D068h
CONTROLSS_EPWM14_G0	5000 E068h
CONTROLSS_EPWM15_G0	5000 F068h
CONTROLSS_EPWM16_G0	5001 0068h
CONTROLSS_EPWM17_G0	5001 1068h
CONTROLSS_EPWM18_G0	5001 2068h
CONTROLSS_EPWM19_G0	5001 3068h
CONTROLSS_EPWM2_G0	5000 2068h
CONTROLSS_EPWM20_G0	5001 4068h
CONTROLSS_EPWM21_G0	5001 5068h
CONTROLSS_EPWM22_G0	5001 6068h
CONTROLSS_EPWM23_G0	5001 7068h
CONTROLSS_EPWM24_G0	5001 8068h
CONTROLSS_EPWM25_G0	5001 9068h
CONTROLSS_EPWM26_G0	5001 A068h
CONTROLSS_EPWM27_G0	5001 B068h
CONTROLSS_EPWM28_G0	5001 C068h
CONTROLSS_EPWM29_G0	5001 D068h
CONTROLSS_EPWM3_G0	5000 3068h
CONTROLSS_EPWM30_G0	5001 E068h
CONTROLSS_EPWM31_G0	5001 F068h
CONTROLSS_EPWM4_G0	5000 4068h
CONTROLSS_EPWM5_G0	5000 5068h
CONTROLSS_EPWM6_G0	5000 6068h
CONTROLSS_EPWM7_G0	5000 7068h
CONTROLSS_EPWM8_G0	5000 8068h
CONTROLSS_EPWM9_G0	5000 9068h
CONTROLSS_EPWM0_G1	5004 0068h
CONTROLSS_EPWM1_G1	5004 1068h
CONTROLSS_EPWM10_G1	5004 A068h
CONTROLSS_EPWM11_G1	5004 B068h
CONTROLSS_EPWM12_G1	5004 C068h
CONTROLSS_EPWM13_G1	5004 D068h
CONTROLSS_EPWM14_G1	5004 E068h

Table 3-721. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM15_G1	5004 F068h
CONTROLSS_EPWM16_G1	5005 0068h
CONTROLSS_EPWM17_G1	5005 1068h
CONTROLSS_EPWM18_G1	5005 2068h
CONTROLSS_EPWM19_G1	5005 3068h
CONTROLSS_EPWM2_G1	5004 2068h
CONTROLSS_EPWM20_G1	5005 4068h
CONTROLSS_EPWM21_G1	5005 5068h
CONTROLSS_EPWM22_G1	5005 6068h
CONTROLSS_EPWM23_G1	5005 7068h
CONTROLSS_EPWM24_G1	5005 8068h
CONTROLSS_EPWM25_G1	5005 9068h
CONTROLSS_EPWM26_G1	5005 A068h
CONTROLSS_EPWM27_G1	5005 B068h
CONTROLSS_EPWM28_G1	5005 C068h
CONTROLSS_EPWM29_G1	5005 D068h
CONTROLSS_EPWM3_G1	5004 3068h
CONTROLSS_EPWM30_G1	5005 E068h
CONTROLSS_EPWM31_G1	5005 F068h
CONTROLSS_EPWM4_G1	5004 4068h
CONTROLSS_EPWM5_G1	5004 5068h
CONTROLSS_EPWM6_G1	5004 6068h
CONTROLSS_EPWM7_G1	5004 7068h
CONTROLSS_EPWM8_G1	5004 8068h
CONTROLSS_EPWM9_G1	5004 9068h
CONTROLSS_EPWM0_G2	5008 0068h
CONTROLSS_EPWM1_G2	5008 1068h
CONTROLSS_EPWM10_G2	5008 A068h
CONTROLSS_EPWM11_G2	5008 B068h
CONTROLSS_EPWM12_G2	5008 C068h
CONTROLSS_EPWM13_G2	5008 D068h
CONTROLSS_EPWM14_G2	5008 E068h
CONTROLSS_EPWM15_G2	5008 F068h
CONTROLSS_EPWM16_G2	5009 0068h
CONTROLSS_EPWM17_G2	5009 1068h
CONTROLSS_EPWM18_G2	5009 2068h
CONTROLSS_EPWM19_G2	5009 3068h
CONTROLSS_EPWM2_G2	5008 2068h
CONTROLSS_EPWM20_G2	5009 4068h
CONTROLSS_EPWM21_G2	5009 5068h
CONTROLSS_EPWM22_G2	5009 6068h
CONTROLSS_EPWM23_G2	5009 7068h
CONTROLSS_EPWM24_G2	5009 8068h
CONTROLSS_EPWM25_G2	5009 9068h
CONTROLSS_EPWM26_G2	5009 A068h
CONTROLSS_EPWM27_G2	5009 B068h
CONTROLSS_EPWM28_G2	5009 C068h

Table 3-721. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM29_G2	5009 D068h
CONTROLSS_EPWM3_G2	5008 3068h
CONTROLSS_EPWM30_G2	5009 E068h
CONTROLSS_EPWM31_G2	5009 F068h
CONTROLSS_EPWM4_G2	5008 4068h
CONTROLSS_EPWM5_G2	5008 5068h
CONTROLSS_EPWM6_G2	5008 6068h
CONTROLSS_EPWM7_G2	5008 7068h
CONTROLSS_EPWM8_G2	5008 8068h
CONTROLSS_EPWM9_G2	5008 9068h
CONTROLSS_EPWM0_G3	500C 0068h
CONTROLSS_EPWM1_G3	500C 1068h
CONTROLSS_EPWM10_G3	500C A068h
CONTROLSS_EPWM11_G3	500C B068h
CONTROLSS_EPWM12_G3	500C C068h
CONTROLSS_EPWM13_G3	500C D068h
CONTROLSS_EPWM14_G3	500C E068h
CONTROLSS_EPWM15_G3	500C F068h
CONTROLSS_EPWM16_G3	500D 0068h
CONTROLSS_EPWM17_G3	500D 1068h
CONTROLSS_EPWM18_G3	500D 2068h
CONTROLSS_EPWM19_G3	500D 3068h
CONTROLSS_EPWM2_G3	500C 2068h
CONTROLSS_EPWM20_G3	500D 4068h
CONTROLSS_EPWM21_G3	500D 5068h
CONTROLSS_EPWM22_G3	500D 6068h
CONTROLSS_EPWM23_G3	500D 7068h
CONTROLSS_EPWM24_G3	500D 8068h
CONTROLSS_EPWM25_G3	500D 9068h
CONTROLSS_EPWM26_G3	500D A068h
CONTROLSS_EPWM27_G3	500D B068h
CONTROLSS_EPWM28_G3	500D C068h
CONTROLSS_EPWM29_G3	500D D068h
CONTROLSS_EPWM3_G3	500C 3068h
CONTROLSS_EPWM30_G3	500D E068h
CONTROLSS_EPWM31_G3	500D F068h
CONTROLSS_EPWM4_G3	500C 4068h
CONTROLSS_EPWM5_G3	500C 5068h
CONTROLSS_EPWM6_G3	500C 6068h
CONTROLSS_EPWM7_G3	500C 7068h
CONTROLSS_EPWM8_G3	500C 8068h
CONTROLSS_EPWM9_G3	500C 9068h

Figure 3-307. GLDCTL Name Register

15	14	13	12	11	10	9	8
RESERVED_2			GLDCNT			GLDPRD	
R			R			R/W	

Figure 3-307. GLDCTL Name Register (continued)

0h			0h				0h
7	6	5	4	3	2	1	0
GLDPRD	RESERVED_1	OSHTMODE	GLDMODE				GLD
R/W	R	R/W	R/W				R/W
0h	0h	0h	0h				0h

Access Types Legend

Table 3-722. GLDCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_2	R	0h	Reserved Reset Source: epwm_rst_mod_g_rst_n
12:10	GLDCNT	R	0h	Global Load Strobe Counter Register These bits indicate how many selected events have occurred: 000: No events 001: 1 event 010: 2 events 011: 3 events 100: 4 events 101: 5 events 110: 6 events 111: 7 events Reset Source: epwm_rst_mod_g_rst_n
9:7	GLDPRD	R/W	0h	Global Load Strobe Period Select Register These bits select how many selected events need to occur before a load strobe is generated 000: Disable counter 001: Generate strobe on GLDCNT = 001 [1st event] 010: Generate strobe on GLDCNT = 010 [2nd event] 011: Generate strobe on GLDCNT = 011 [3rd event] 100: Generate strobe on GLDCNT = 011 [4th event] 101: Generate strobe on GLDCNT = 001 [5th event] 110: Generate strobe on GLDCNT = 010 [6th event] 111: Generate strobe on GLDCNT = 011 [7th event] Reset Source: epwm_rst_mod_g_rst_n
6	RESERVED_1	R	0h	Reserved Reset Source: epwm_rst_mod_g_rst_n
5	OSHTMODE	R/W	0h	One Shot Load Mode Control Bit 0: One shot load mode is disabled and shadow to active loading happens continuously on all the chosen load strobes. 1: One shot mode is active. All load strobes are blocked until GLDCTL2[OSHTLD] is written with 1. Note: One Shot mode can only be used with global shadow to active load mode enabled [GLDCTL[GLD]=1] Reset Source: epwm_rst_mod_g_rst_n
4:1	GLDMODE	R/W	0h	Global Load Pulse selection for Shadow to Active Mode Reloads 0000: Load on Counter = 0 [CNT_ZRO] 0001: Load on Counter = Period [PRD_EQ] 0010: Load on either Counter = 0, or Counter = Period 0011: Load on SYNCEVT - this is logical OR of DCAEVT1.sync, DCBEVT1.sync, EPWMxSYNCI and TBCTL[SWFSYNC] 0100: Load on SYNCEVT or CNT_ZRO 0101: Load on SYNCEVT or PRD_EQ 0110: Load on SYNCEVT or CNT_ZRO or PRD_EQ 1000: Load on Counter = CMPCU [CMPC_EQ counter incrementing] 1001: Load on Counter = CMPCD [CMPC_EQ counter decrementing] 1010: Load on Counter = CMPDU [CMPD_EQ counter incrementing] 1011: Load on Counter = CMPDD [CMPD_EQ counter decrementing] 1100: Reserved ... 1110: Reserved 1111: Load on GLDCTL2[GFRCLD] write Reset Source: epwm_rst_mod_g_rst_n
0	GLD	R/W	0h	Global Shadow to Active Load Event Control 0: Shadow to active reload for all shadowed registers happens as per the individual reload control bits specified [Compatible with previous EPWM versions]. 1: When set, all the shadow to active reload events are defined by GLDMODE bits in GLDCTL register. All the shadow registers use same reload pulse from shadow to active reloading. Individual LOADMODE bits are ignored. Reset Source: epwm_rst_mod_g_rst_n

3.9.22 MEM_GLDCFG Registers

3.9.22.1 MEM_GLDCFG Register (Offset = 6Ah) [reset = 0h]

Short Description: Global PWM Load Config Re

Long Description: Global PWM Load Config Register

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Table 3-723. Instance Table

Instance Name	Physical Address
CONTROLSS_EPWM0_G0	5000 006Ah
CONTROLSS_EPWM1_G0	5000 106Ah
CONTROLSS_EPWM10_G0	5000 A06Ah
CONTROLSS_EPWM11_G0	5000 B06Ah
CONTROLSS_EPWM12_G0	5000 C06Ah
CONTROLSS_EPWM13_G0	5000 D06Ah
CONTROLSS_EPWM14_G0	5000 E06Ah
CONTROLSS_EPWM15_G0	5000 F06Ah
CONTROLSS_EPWM16_G0	5001 006Ah
CONTROLSS_EPWM17_G0	5001 106Ah
CONTROLSS_EPWM18_G0	5001 206Ah
CONTROLSS_EPWM19_G0	5001 306Ah
CONTROLSS_EPWM2_G0	5000 206Ah
CONTROLSS_EPWM20_G0	5001 406Ah
CONTROLSS_EPWM21_G0	5001 506Ah
CONTROLSS_EPWM22_G0	5001 606Ah
CONTROLSS_EPWM23_G0	5001 706Ah
CONTROLSS_EPWM24_G0	5001 806Ah
CONTROLSS_EPWM25_G0	5001 906Ah
CONTROLSS_EPWM26_G0	5001 A06Ah
CONTROLSS_EPWM27_G0	5001 B06Ah
CONTROLSS_EPWM28_G0	5001 C06Ah
CONTROLSS_EPWM29_G0	5001 D06Ah
CONTROLSS_EPWM3_G0	5000 306Ah
CONTROLSS_EPWM30_G0	5001 E06Ah
CONTROLSS_EPWM31_G0	5001 F06Ah
CONTROLSS_EPWM4_G0	5000 406Ah
CONTROLSS_EPWM5_G0	5000 506Ah
CONTROLSS_EPWM6_G0	5000 606Ah
CONTROLSS_EPWM7_G0	5000 706Ah
CONTROLSS_EPWM8_G0	5000 806Ah
CONTROLSS_EPWM9_G0	5000 906Ah
CONTROLSS_EPWM0_G1	5004 006Ah
CONTROLSS_EPWM1_G1	5004 106Ah
CONTROLSS_EPWM10_G1	5004 A06Ah
CONTROLSS_EPWM11_G1	5004 B06Ah
CONTROLSS_EPWM12_G1	5004 C06Ah
CONTROLSS_EPWM13_G1	5004 D06Ah
CONTROLSS_EPWM14_G1	5004 E06Ah

Table 3-723. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM15_G1	5004 F06Ah
CONTROLSS_EPWM16_G1	5005 006Ah
CONTROLSS_EPWM17_G1	5005 106Ah
CONTROLSS_EPWM18_G1	5005 206Ah
CONTROLSS_EPWM19_G1	5005 306Ah
CONTROLSS_EPWM2_G1	5004 206Ah
CONTROLSS_EPWM20_G1	5005 406Ah
CONTROLSS_EPWM21_G1	5005 506Ah
CONTROLSS_EPWM22_G1	5005 606Ah
CONTROLSS_EPWM23_G1	5005 706Ah
CONTROLSS_EPWM24_G1	5005 806Ah
CONTROLSS_EPWM25_G1	5005 906Ah
CONTROLSS_EPWM26_G1	5005 A06Ah
CONTROLSS_EPWM27_G1	5005 B06Ah
CONTROLSS_EPWM28_G1	5005 C06Ah
CONTROLSS_EPWM29_G1	5005 D06Ah
CONTROLSS_EPWM3_G1	5004 306Ah
CONTROLSS_EPWM30_G1	5005 E06Ah
CONTROLSS_EPWM31_G1	5005 F06Ah
CONTROLSS_EPWM4_G1	5004 406Ah
CONTROLSS_EPWM5_G1	5004 506Ah
CONTROLSS_EPWM6_G1	5004 606Ah
CONTROLSS_EPWM7_G1	5004 706Ah
CONTROLSS_EPWM8_G1	5004 806Ah
CONTROLSS_EPWM9_G1	5004 906Ah
CONTROLSS_EPWM0_G2	5008 006Ah
CONTROLSS_EPWM1_G2	5008 106Ah
CONTROLSS_EPWM10_G2	5008 A06Ah
CONTROLSS_EPWM11_G2	5008 B06Ah
CONTROLSS_EPWM12_G2	5008 C06Ah
CONTROLSS_EPWM13_G2	5008 D06Ah
CONTROLSS_EPWM14_G2	5008 E06Ah
CONTROLSS_EPWM15_G2	5008 F06Ah
CONTROLSS_EPWM16_G2	5009 006Ah
CONTROLSS_EPWM17_G2	5009 106Ah
CONTROLSS_EPWM18_G2	5009 206Ah
CONTROLSS_EPWM19_G2	5009 306Ah
CONTROLSS_EPWM2_G2	5008 206Ah
CONTROLSS_EPWM20_G2	5009 406Ah
CONTROLSS_EPWM21_G2	5009 506Ah
CONTROLSS_EPWM22_G2	5009 606Ah
CONTROLSS_EPWM23_G2	5009 706Ah
CONTROLSS_EPWM24_G2	5009 806Ah
CONTROLSS_EPWM25_G2	5009 906Ah
CONTROLSS_EPWM26_G2	5009 A06Ah
CONTROLSS_EPWM27_G2	5009 B06Ah
CONTROLSS_EPWM28_G2	5009 C06Ah

Table 3-723. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM29_G2	5009 D06Ah
CONTROLSS_EPWM3_G2	5008 306Ah
CONTROLSS_EPWM30_G2	5009 E06Ah
CONTROLSS_EPWM31_G2	5009 F06Ah
CONTROLSS_EPWM4_G2	5008 406Ah
CONTROLSS_EPWM5_G2	5008 506Ah
CONTROLSS_EPWM6_G2	5008 606Ah
CONTROLSS_EPWM7_G2	5008 706Ah
CONTROLSS_EPWM8_G2	5008 806Ah
CONTROLSS_EPWM9_G2	5008 906Ah
CONTROLSS_EPWM0_G3	500C 006Ah
CONTROLSS_EPWM1_G3	500C 106Ah
CONTROLSS_EPWM10_G3	500C A06Ah
CONTROLSS_EPWM11_G3	500C B06Ah
CONTROLSS_EPWM12_G3	500C C06Ah
CONTROLSS_EPWM13_G3	500C D06Ah
CONTROLSS_EPWM14_G3	500C E06Ah
CONTROLSS_EPWM15_G3	500C F06Ah
CONTROLSS_EPWM16_G3	500D 006Ah
CONTROLSS_EPWM17_G3	500D 106Ah
CONTROLSS_EPWM18_G3	500D 206Ah
CONTROLSS_EPWM19_G3	500D 306Ah
CONTROLSS_EPWM2_G3	500C 206Ah
CONTROLSS_EPWM20_G3	500D 406Ah
CONTROLSS_EPWM21_G3	500D 506Ah
CONTROLSS_EPWM22_G3	500D 606Ah
CONTROLSS_EPWM23_G3	500D 706Ah
CONTROLSS_EPWM24_G3	500D 806Ah
CONTROLSS_EPWM25_G3	500D 906Ah
CONTROLSS_EPWM26_G3	500D A06Ah
CONTROLSS_EPWM27_G3	500D B06Ah
CONTROLSS_EPWM28_G3	500D C06Ah
CONTROLSS_EPWM29_G3	500D D06Ah
CONTROLSS_EPWM3_G3	500C 306Ah
CONTROLSS_EPWM30_G3	500D E06Ah
CONTROLSS_EPWM31_G3	500D F06Ah
CONTROLSS_EPWM4_G3	500C 406Ah
CONTROLSS_EPWM5_G3	500C 506Ah
CONTROLSS_EPWM6_G3	500C 606Ah
CONTROLSS_EPWM7_G3	500C 706Ah
CONTROLSS_EPWM8_G3	500C 806Ah
CONTROLSS_EPWM9_G3	500C 906Ah

Figure 3-308. GLDCFG Name Register

15	14	13	12	11	10	9	8
RESERVED_1					AQCSFRC	AQCTLB_AQCTLB2	AQCTLA_AQCTLA2

Figure 3-308. GLDCFG Name Register (continued)

R					R/W	R/W	R/W
0h					0h	0h	0h
7	6	5	4	3	2	1	0
DBCTL	DBFED_DBFEDHR	DBRED_DBREDHR	CMPD	CMPC	CMPB_CMPBHR	CMPA_CMPAHR	TBPRD_TBPRDHR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 3-724. GLDCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED_1	R	0h	Reserved Reset Source: epwm_rst_mod_g_rst_n
10	AQCSFRC	R/W	0h	Global load event configuration for AQCSFRC 0: Registers use local reload configuration even if GLDCTL[GLD]=1 [reload is compatible with previous EPWMs] 1: Registers use global load configuration if this bit is set and GLDCTL[GLD]=1 Reset Source: epwm_rst_mod_g_rst_n
9	AQCTLB_AQCTLB2	R/W	0h	Global load event configuration for AQCTLB_AQCTLB2 0: Registers use local reload configuration even if GLDCTL[GLD]=1 [reload is compatible with previous EPWMs] 1: Registers use global load configuration if this bit is set and GLDCTL[GLD]=1 Reset Source: epwm_rst_mod_g_rst_n
8	AQCTLA_AQCTLA2	R/W	0h	Global load event configuration for AQCTLA_AQCTLA2 0: Registers use local reload configuration even if GLDCTL[GLD]=1 [reload is compatible with previous EPWMs] 1: Registers use global load configuration if this bit is set and GLDCTL[GLD]=1 Reset Source: epwm_rst_mod_g_rst_n
7	DBCTL	R/W	0h	Global load event configuration for DBCTL 0: Registers use local reload configuration even if GLDCTL[GLD]=1 [reload is compatible with previous EPWMs] 1: Registers use global load configuration if this bit is set and GLDCTL[GLD]=1 Reset Source: epwm_rst_mod_g_rst_n
6	DBFED_DBFEDHR	R/W	0h	Global load event configuration for DBFED_DBFEDHR 0: Registers use local reload configuration even if GLDCTL[GLD]=1 [reload is compatible with previous EPWMs] 1: Registers use global load configuration if this bit is set and GLDCTL[GLD]=1 Reset Source: epwm_rst_mod_g_rst_n
5	DBRED_DBREDHR	R/W	0h	Global load event configuration for DBRED_DBREDHR 0: Registers use local reload configuration even if GLDCTL[GLD]=1 [reload is compatible with previous EPWMs] 1: Registers use global load configuration if this bit is set and GLDCTL[GLD]=1 Reset Source: epwm_rst_mod_g_rst_n
4	CMPD	R/W	0h	Global load event configuration for CMPD 0: Registers use local reload configuration even if GLDCTL[GLD]=1 [reload is compatible with previous EPWMs] 1: Registers use global load configuration if this bit is set and GLDCTL[GLD]=1 Reset Source: epwm_rst_mod_g_rst_n
3	CMPC	R/W	0h	Global load event configuration for CMPC 0: Registers use local reload configuration even if GLDCTL[GLD]=1 [reload is compatible with previous EPWMs] 1: Registers use global load configuration if this bit is set and GLDCTL[GLD]=1 Reset Source: epwm_rst_mod_g_rst_n
2	CMPB_CMPBHR	R/W	0h	Global load event configuration for CMPB_CMPBHR 0: Registers use local reload configuration even if GLDCTL[GLD]=1 [reload is compatible with previous EPWMs] 1: Registers use global load configuration if this bit is set and GLDCTL[GLD]=1 Reset Source: epwm_rst_mod_g_rst_n

Table 3-724. GLDCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CMPA_CMPAHR	R/W	0h	Global load event configuration for CMPA_CMPAHR 0: Registers use local reload configuration even if GLDCTL[GLD]=1 [reload is compatible with previous EPWMs] 1: Registers use global load configuration if this bit is set and GLDCTL[GLD]=1 Reset Source: epwm_rst_mod_g_rst_n
0	TBPRD_TBPRDHR	R/W	0h	Global load event configuration for TBPRD_TBPRDHR 0: Registers use local reload configuration even if GLDCTL[GLD]=1 [reload is compatible with previous EPWMs] 1: Registers use global load configuration if this bit is set and GLDCTL[GLD]=1 Reset Source: epwm_rst_mod_g_rst_n

3.9.23 MEM_EPWMXLINK Registers

3.9.23.1 MEM_EPWMXLINK Register (Offset = 70h) [reset = 0h]

Short Description: EPWMx Link Register Th

Long Description: EPWMx Link Register This register controls which EPWMs are linked to other EPWM modules. The default reset value will vary for each module. The reset value will link each EPWM module to itself to prevent unintentional linking of modules.

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Table 3-725. Instance Table

Instance Name	Physical Address
CONTROLSS_EPWM0_G0	5000 0070h
CONTROLSS_EPWM1_G0	5000 1070h
CONTROLSS_EPWM10_G0	5000 A070h
CONTROLSS_EPWM11_G0	5000 B070h
CONTROLSS_EPWM12_G0	5000 C070h
CONTROLSS_EPWM13_G0	5000 D070h
CONTROLSS_EPWM14_G0	5000 E070h
CONTROLSS_EPWM15_G0	5000 F070h
CONTROLSS_EPWM16_G0	5001 0070h
CONTROLSS_EPWM17_G0	5001 1070h
CONTROLSS_EPWM18_G0	5001 2070h
CONTROLSS_EPWM19_G0	5001 3070h
CONTROLSS_EPWM2_G0	5000 2070h
CONTROLSS_EPWM20_G0	5001 4070h
CONTROLSS_EPWM21_G0	5001 5070h
CONTROLSS_EPWM22_G0	5001 6070h
CONTROLSS_EPWM23_G0	5001 7070h
CONTROLSS_EPWM24_G0	5001 8070h
CONTROLSS_EPWM25_G0	5001 9070h
CONTROLSS_EPWM26_G0	5001 A070h
CONTROLSS_EPWM27_G0	5001 B070h
CONTROLSS_EPWM28_G0	5001 C070h
CONTROLSS_EPWM29_G0	5001 D070h
CONTROLSS_EPWM3_G0	5000 3070h
CONTROLSS_EPWM30_G0	5001 E070h
CONTROLSS_EPWM31_G0	5001 F070h
CONTROLSS_EPWM4_G0	5000 4070h
CONTROLSS_EPWM5_G0	5000 5070h
CONTROLSS_EPWM6_G0	5000 6070h
CONTROLSS_EPWM7_G0	5000 7070h
CONTROLSS_EPWM8_G0	5000 8070h
CONTROLSS_EPWM9_G0	5000 9070h
CONTROLSS_EPWM0_G1	5004 0070h
CONTROLSS_EPWM1_G1	5004 1070h
CONTROLSS_EPWM10_G1	5004 A070h
CONTROLSS_EPWM11_G1	5004 B070h
CONTROLSS_EPWM12_G1	5004 C070h
CONTROLSS_EPWM13_G1	5004 D070h

Table 3-725. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM14_G1	5004 E070h
CONTROLSS_EPWM15_G1	5004 F070h
CONTROLSS_EPWM16_G1	5005 0070h
CONTROLSS_EPWM17_G1	5005 1070h
CONTROLSS_EPWM18_G1	5005 2070h
CONTROLSS_EPWM19_G1	5005 3070h
CONTROLSS_EPWM2_G1	5004 2070h
CONTROLSS_EPWM20_G1	5005 4070h
CONTROLSS_EPWM21_G1	5005 5070h
CONTROLSS_EPWM22_G1	5005 6070h
CONTROLSS_EPWM23_G1	5005 7070h
CONTROLSS_EPWM24_G1	5005 8070h
CONTROLSS_EPWM25_G1	5005 9070h
CONTROLSS_EPWM26_G1	5005 A070h
CONTROLSS_EPWM27_G1	5005 B070h
CONTROLSS_EPWM28_G1	5005 C070h
CONTROLSS_EPWM29_G1	5005 D070h
CONTROLSS_EPWM3_G1	5004 3070h
CONTROLSS_EPWM30_G1	5005 E070h
CONTROLSS_EPWM31_G1	5005 F070h
CONTROLSS_EPWM4_G1	5004 4070h
CONTROLSS_EPWM5_G1	5004 5070h
CONTROLSS_EPWM6_G1	5004 6070h
CONTROLSS_EPWM7_G1	5004 7070h
CONTROLSS_EPWM8_G1	5004 8070h
CONTROLSS_EPWM9_G1	5004 9070h
CONTROLSS_EPWM0_G2	5008 0070h
CONTROLSS_EPWM1_G2	5008 1070h
CONTROLSS_EPWM10_G2	5008 A070h
CONTROLSS_EPWM11_G2	5008 B070h
CONTROLSS_EPWM12_G2	5008 C070h
CONTROLSS_EPWM13_G2	5008 D070h
CONTROLSS_EPWM14_G2	5008 E070h
CONTROLSS_EPWM15_G2	5008 F070h
CONTROLSS_EPWM16_G2	5009 0070h
CONTROLSS_EPWM17_G2	5009 1070h
CONTROLSS_EPWM18_G2	5009 2070h
CONTROLSS_EPWM19_G2	5009 3070h
CONTROLSS_EPWM2_G2	5008 2070h
CONTROLSS_EPWM20_G2	5009 4070h
CONTROLSS_EPWM21_G2	5009 5070h
CONTROLSS_EPWM22_G2	5009 6070h
CONTROLSS_EPWM23_G2	5009 7070h
CONTROLSS_EPWM24_G2	5009 8070h
CONTROLSS_EPWM25_G2	5009 9070h
CONTROLSS_EPWM26_G2	5009 A070h
CONTROLSS_EPWM27_G2	5009 B070h

Table 3-725. Instance Table (continued)

Instance Name	Physical Address
CONTROLSS_EPWM28_G2	5009 C070h
CONTROLSS_EPWM29_G2	5009 D070h
CONTROLSS_EPWM3_G2	5008 3070h
CONTROLSS_EPWM30_G2	5009 E070h
CONTROLSS_EPWM31_G2	5009 F070h
CONTROLSS_EPWM4_G2	5008 4070h
CONTROLSS_EPWM5_G2	5008 5070h
CONTROLSS_EPWM6_G2	5008 6070h
CONTROLSS_EPWM7_G2	5008 7070h
CONTROLSS_EPWM8_G2	5008 8070h
CONTROLSS_EPWM9_G2	5008 9070h
CONTROLSS_EPWM0_G3	500C 0070h
CONTROLSS_EPWM1_G3	500C 1070h
CONTROLSS_EPWM10_G3	500C A070h
CONTROLSS_EPWM11_G3	500C B070h
CONTROLSS_EPWM12_G3	500C C070h
CONTROLSS_EPWM13_G3	500C D070h
CONTROLSS_EPWM14_G3	500C E070h
CONTROLSS_EPWM15_G3	500C F070h
CONTROLSS_EPWM16_G3	500D 0070h
CONTROLSS_EPWM17_G3	500D 1070h
CONTROLSS_EPWM18_G3	500D 2070h
CONTROLSS_EPWM19_G3	500D 3070h
CONTROLSS_EPWM2_G3	500C 2070h
CONTROLSS_EPWM20_G3	500D 4070h
CONTROLSS_EPWM21_G3	500D 5070h
CONTROLSS_EPWM22_G3	500D 6070h
CONTROLSS_EPWM23_G3	500D 7070h
CONTROLSS_EPWM24_G3	500D 8070h
CONTROLSS_EPWM25_G3	500D 9070h
CONTROLSS_EPWM26_G3	500D A070h
CONTROLSS_EPWM27_G3	500D B070h
CONTROLSS_EPWM28_G3	500D C070h
CONTROLSS_EPWM29_G3	500D D070h
CONTROLSS_EPWM3_G3	500C 3070h
CONTROLSS_EPWM30_G3	500D E070h
CONTROLSS_EPWM31_G3	500D F070h
CONTROLSS_EPWM4_G3	500C 4070h
CONTROLSS_EPWM5_G3	500C 5070h
CONTROLSS_EPWM6_G3	500C 6070h
CONTROLSS_EPWM7_G3	500C 7070h
CONTROLSS_EPWM8_G3	500C 8070h
CONTROLSS_EPWM9_G3	500C 9070h

Figure 3-309. EPWMXLINK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Figure 3-309. EPWMXLINK Name Register (continued)

RESERVED_2	GLDCTL2LINK	CMPDLINK	CMPCLINK
R	R/W	R/W	R/W
0h	0h	0h	0h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	CMPBLINK					CMPALINK					TBPRDLINK				
NONE	R/W					R/W					R/W				
0	0h					0h					0h				

Access Types Legend

Table 3-726. EPWMXLINK Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED_2	R	0h	Reserved Reserved Reset Source: epwm_rst_mod_g_rst_n
30:26	GLDCTL2LINK	R/W	0h	GLDCTL2 Link Bits Writes to the GLDCTL2 registers in the ePWM module selected by the following bit selections results in a simultaneous write to the current ePWM module's GLDCTL2 registers. 00000: ePWM1 00001: ePWM2 00010: ePWM3 00011: ePWM4 00100: ePWM5 00101: ePWM6 00110: ePWM7 00111: ePWM8 01000: ePWM9 01001: ePWM10 01010: ePWM11 01011: ePWM12 01100: ePWM13 ... 11111: ePWM32 Reset Source: epwm_rst_mod_g_rst_n
25:21	CMPDLINK	R/W	0h	CMPD Link Bits Writes to the CMPD registers in the ePWM module selected by the following bit selections results in a simultaneous write to the current ePWM module's CMPD registers. 00000: ePWM1 00001: ePWM2 00010: ePWM3 00011: ePWM4 00100: ePWM5 00101: ePWM6 00110: ePWM7 00111: ePWM8 01000: ePWM9 01001: ePWM10 01010: ePWM11 01011: ePWM12 01100: ePWM13 ... 11111: ePWM32 Reset Source: epwm_rst_mod_g_rst_n
20:16	CMPCLINK	R/W	0h	CMPC Link Bits Writes to the CMPC registers in the ePWM module selected by the following bit selections results in a simultaneous write to the current ePWM module's CMPC registers. 00000: ePWM1 00001: ePWM2 00010: ePWM3 00011: ePWM4 00100: ePWM5 00101: ePWM6 00110: ePWM7 00111: ePWM8 01000: ePWM9 01001: ePWM10 01010: ePWM11 01011: ePWM12 01100: ePWM13 ... 11111: ePWM32 Reset Source: epwm_rst_mod_g_rst_n
15	RESERVED	NONE		Reserved
14:10	CMPBLINK	R/W	0h	CMPB_CMPBHR Link Bits Writes to the CMPB_CMPBHR registers in the ePWM module selected by the following bit selections results in a simultaneous write to the current ePWM module's CMPB_CMPBHR registers. 00000: ePWM1 00001: ePWM2 00010: ePWM3 00011: ePWM4 00100: ePWM5 00101: ePWM6 00110: ePWM7 00111: ePWM8 01000: ePWM9 01001: ePWM10 01010: ePWM11 01011: ePWM12 01100: ePWM13 ... 11111: ePWM32 Reset Source: epwm_rst_mod_g_rst_n
9:5	CMPALINK	R/W	0h	CMPA_CMPAHR Link Bits Writes to the CMPA_CMPAHR registers in the ePWM module selected by the following bit selections results in a simultaneous write to the current ePWM module's CMPA_CMPAHR registers. 00000: ePWM1 00001: ePWM2 00010: ePWM3 00011: ePWM4 00100: ePWM5 00101: ePWM6 00110: ePWM7 00111: ePWM8 01000: ePWM9 01001: ePWM10 01010: ePWM11 01011: ePWM12 01100: ePWM13 ... 11111: ePWM32 Reset Source: epwm_rst_mod_g_rst_n

Table 3-726. EPWMXLINK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	TBPRDLINK	R/W	0h	TBPRD_TBPRDHR Link Bits Writes to the TBPRD:TBPRDHR registers in the ePWM module selected by the following bit selections results in a simultaneous write to the current ePWM module's TBPRD_TBPRDHR registers. 00000: ePWM1 00001: ePWM2 00010: ePWM3 00011: ePWM4 00100: ePWM5 00101: ePWM6 00110: ePWM7 00111: ePWM8 01000: ePWM9 01001: ePWM10 01010: ePWM11 01011: ePWM12 01100: ePWM13 ... 11111: ePWM32 Reset Source: epwm_rst_mod_g_rst_n

3.9.24 Access Table

Table 3-727. Access Type Codes

Access Type	Code	Description
R/W	R/W	Read / Write
R/W1TS	R/W1TS	Read/Write 1 To Set
R	R	Read
R/W1TC	R/W1TC	Read/Write 1 To Clear

3.10 EQEP Registers

Table 3-728. MEM, MEM Registers, Base Address=0X0000000050270000, Length=4096

Offset	Length	Register Name	eqep0 Physical Address	eqep1 Physical Address	eqep2 Physical Address
0h	32	QPOSCNT	5027 0000h	5027 1000h	5027 2000h
4h	32	QPOSINIT	5027 0004h	5027 1004h	5027 2004h
8h	32	QPOSMAX	5027 0008h	5027 1008h	5027 2008h
Ch	32	QPOSCMP	5027 000Ch	5027 100Ch	5027 200Ch
10h	32	QPOSILAT	5027 0010h	5027 1010h	5027 2010h
14h	32	QPOSSLAT	5027 0014h	5027 1014h	5027 2014h
18h	32	QPOSLAT	5027 0018h	5027 1018h	5027 2018h
1Ch	32	QUTMR	5027 001Ch	5027 101Ch	5027 201Ch
20h	32	QUPRD	5027 0020h	5027 1020h	5027 2020h
24h	16	QWDTMR	5027 0024h	5027 1024h	5027 2024h
26h	16	QWDPRD	5027 0026h	5027 1026h	5027 2026h
28h	16	QDECCTL	5027 0028h	5027 1028h	5027 2028h
2Ah	16	QEPCTL	5027 002Ah	5027 102Ah	5027 202Ah
2Ch	16	QCAPCTL	5027 002Ch	5027 102Ch	5027 202Ch
2Eh	16	QPOSCTL	5027 002Eh	5027 102Eh	5027 202Eh
30h	16	QEINT	5027 0030h	5027 1030h	5027 2030h
32h	16	QFLG	5027 0032h	5027 1032h	5027 2032h
34h	16	QCLR	5027 0034h	5027 1034h	5027 2034h
36h	16	QFRC	5027 0036h	5027 1036h	5027 2036h
38h	16	QEPSTS	5027 0038h	5027 1038h	5027 2038h
3Ah	16	QCTMR	5027 003Ah	5027 103Ah	5027 203Ah
3Ch	16	QCPRD	5027 003Ch	5027 103Ch	5027 203Ch
3Eh	16	QCTMRLAT	5027 003Eh	5027 103Eh	5027 203Eh
40h	16	QCPRDLAT	5027 0040h	5027 1040h	5027 2040h
60h	32	REV	5027 0060h	5027 1060h	5027 2060h
64h	32	QEPSTROBESEL	5027 0064h	5027 1064h	5027 2064h
68h	32	QMACTRL	5027 0068h	5027 1068h	5027 2068h
6Ch	32	QEPSRCSEL	5027 006Ch	5027 106Ch	5027 206Ch

3.10.1 MEM_QPOSCNT Registers

3.10.1.1 MEM_QPOSCNT Register (Offset = 0h) [reset = 0h]

Short Description: Position Counter

Long Description: Position Counter

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Table 3-729. Instance Table

Instance Name	Physical Address
EQEP0	5027 0000h
EQEP1	5027 1000h
EQEP2	5027 2000h

Figure 3-310. QPOSCNT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
QPOSCNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QPOSCNT															
R/W															
0h															

Access Types Legend

Table 3-730. QPOSCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QPOSCNT	R/W	0h	Position Counter This 32-bit position counter register counts up/ down on every eQEP pulse based on direction input. This counter acts as a position integrator whose count value is proportional to position from a give reference point. This Register acts as a Read ONLY register while counter is counting up/down. Note: It is recommended to only write to the position counter register [QPOSCNT] during initialization, i.e. when the eQEP position counter is disabled [QPEN bit of QEPCTL is zero]. Once the position counter is enabled [QPEN bit is one], writing to the eQEP position counter register [QPOSCNT] may cause unexpected results. Reset Source: eqep_rst_mod_g_rst_n

3.10.2 MEM_QPOSINIT Registers

3.10.2.1 MEM_QPOSINIT Register (Offset = 4h) [reset = 0h]

Short Description: Position Counter Init

Long Description: Position Counter Init

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Table 3-731. Instance Table

Instance Name	Physical Address
EQEP0	5027 0004h
EQEP1	5027 1004h
EQEP2	5027 2004h

Figure 3-311. QPOSINIT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
QPOSINIT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QPOSINIT															
R/W															
0h															

Access Types Legend

Table 3-732. QPOSINIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QPOSINIT	R/W	0h	Position Counter Init This register contains the position value that is used to initialize the position counter based on external strobe or index event. The position counter can be initialized through software. Writes to this register should always be full 32-bit writes. Reset Source: eqep_rst_mod_g_rst_n

3.10.3 MEM_QPOSMAX Registers

3.10.3.1 MEM_QPOSMAX Register (Offset = 8h) [reset = 0h]

Short Description: Maximum Position Count

Long Description: Maximum Position Count

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Table 3-733. Instance Table

Instance Name	Physical Address
EQEP0	5027 0008h
EQEP1	5027 1008h
EQEP2	5027 2008h

Figure 3-312. QPOSMAX Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
QPOSMAX															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QPOSMAX															
R/W															
0h															

Access Types Legend

Table 3-734. QPOSMAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QPOSMAX	R/W	0h	Maximum Position Count This register contains the maximum position counter value. Writes to this register should always be full 32-bit writes. Reset Source: eqep_rst_mod_g_rst_n

3.10.4 MEM_QPOSCMP Registers

3.10.4.1 MEM_QPOSCMP Register (Offset = Ch) [reset = 0h]

Short Description: Position Compare

Long Description: Position Compare

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Table 3-735. Instance Table

Instance Name	Physical Address
EQEP0	5027 000Ch
EQEP1	5027 100Ch
EQEP2	5027 200Ch

Figure 3-313. QPOSCMP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
QPOSCMP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QPOSCMP															
R/W															
0h															

Access Types Legend

Table 3-736. QPOSCMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QPOSCMP	R/W	0h	Position Compare The position-compare value in this register is compared with the position counter [QPOSCNT] to generate sync output and/or interrupt on compare match. Reset Source: eqep_rst_mod_g_rst_n

3.10.5 MEM_QPOSILAT Registers

3.10.5.1 MEM_QPOSILAT Register (Offset = 10h) [reset = 0h]

Short Description: Index Position Latch

Long Description: Index Position Latch

Return to Summary Table

Table 3-737. Instance Table

Instance Name	Physical Address
EQEP0	5027 0010h
EQEP1	5027 1010h
EQEP2	5027 2010h

Figure 3-314. QPOSILAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
QPOSILAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QPOSILAT															
R															
0h															

Access Types Legend

Table 3-738. QPOSILAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QPOSILAT	R	0h	Index Position Latch The position-counter value is latched into this register on an index event as defined by the QEPCTL[IEL] bits. Reset Source: eqep_rst_mod_g_rst_n

3.10.6 MEM_QPOSSLAT Registers

3.10.6.1 MEM_QPOSSLAT Register (Offset = 14h) [reset = 0h]

Short Description: Strobe Position Latch

Long Description: Strobe Position Latch

Return to Summary Table

Table 3-739. Instance Table

Instance Name	Physical Address
EQEP0	5027 0014h
EQEP1	5027 1014h
EQEP2	5027 2014h

Figure 3-315. QPOSSLAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
QPOSSLAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QPOSSLAT															
R															
0h															

Access Types Legend

Table 3-740. QPOSSLAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QPOSSLAT	R	0h	Strobe Position Latch The position-counter value is latched into this register on a strobe event as defined by the QEPCTL[SEL] bits. Reset Source: eqep_rst_mod_g_rst_n

3.10.7 MEM_QPOSLAT Registers

3.10.7.1 MEM_QPOSLAT Register (Offset = 18h) [reset = 0h]

Short Description: Position Latch

Long Description: Position Latch

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Table 3-741. Instance Table

Instance Name	Physical Address
EQEP0	5027 0018h
EQEP1	5027 1018h
EQEP2	5027 2018h

Figure 3-316. QPOSLAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
QPOSLAT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QPOSLAT															
R															
0h															

Access Types Legend

Table 3-742. QPOSLAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QPOSLAT	R	0h	Position Latch The position-counter value is latched into this register on a unit time out event. Reset Source: eqep_rst_mod_g_rst_n

3.10.8 MEM_QUTMR Registers

3.10.8.1 MEM_QUTMR Register (Offset = 1Ch) [reset = 0h]

Short Description: QEP Unit Timer

Long Description: QEP Unit Timer

Return to Summary Table

Table 3-743. Instance Table

Instance Name	Physical Address
EQEP0	5027 001Ch
EQEP1	5027 101Ch
EQEP2	5027 201Ch

Figure 3-317. QUTMR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
QUTMR															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QUTMR															
R/W															
0h															

Access Types Legend

Table 3-744. QUTMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUTMR	R/W	0h	QEP Unit Timer This register acts as time base for unit time event generation. When this timer value matches the unit time period value a unit time event is generated. Reset Source: eqep_rst_mod_g_rst_n

3.10.9 MEM_QUPRD Registers

3.10.9.1 MEM_QUPRD Register (Offset = 20h) [reset = 0h]

Short Description: QEP Unit Period

Long Description: QEP Unit Period

Return to Summary Table

Table 3-745. Instance Table

Instance Name	Physical Address
EQEP0	5027 0020h
EQEP1	5027 1020h
EQEP2	5027 2020h

Figure 3-318. QUPRD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
QUPRD															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QUPRD															
R/W															
0h															

Access Types Legend

Table 3-746. QUPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUPRD	R/W	0h	QEP Unit Period This register contains the period count for the unit timer to generate periodic unit time events. These events latch the eQEP position information at periodic intervals and optionally generate an interrupt. Writes to this register should always be full 32-bit writes. Reset Source: eqep_rst_mod_g_rst_n

3.10.10 MEM_QWDTMR Registers

3.10.10.1 MEM_QWDTMR Register (Offset = 24h) [reset = 0h]

Short Description: QEP Watchdog Timer

Long Description: QEP Watchdog Timer

Return to Summary Table

Table 3-747. Instance Table

Instance Name	Physical Address
EQEP0	5027 0024h
EQEP1	5027 1024h
EQEP2	5027 2024h

Figure 3-319. QWDTMR Name Register

15	14	13	12	11	10	9	8
QWDTMR							
R/W							
0h							
7	6	5	4	3	2	1	0
QWDTMR							
R/W							
0h							

Access Types Legend

Table 3-748. QWDTMR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	QWDTMR	R/W	0h	QEP Watchdog Timer This register acts as time base for the watchdog to detect motor stalls. When this timer value matches with the watchdog's period value a watchdog timeout interrupt is generated. This register is reset upon edge transition in quadrature-clock indicating the motion. Reset Source: eqep_rst_mod_g_rst_n

3.10.11 MEM_QWDPRD Registers

3.10.11.1 MEM_QWDPRD Register (Offset = 26h) [reset = 0h]

Short Description: QEP Watchdog Period

Long Description: QEP Watchdog Period

Return to Summary Table

Table 3-749. Instance Table

Instance Name	Physical Address
EQEP0	5027 0026h
EQEP1	5027 1026h
EQEP2	5027 2026h

Figure 3-320. QWDPRD Name Register

15	14	13	12	11	10	9	8
QWDPRD							
R/W							
0h							
7	6	5	4	3	2	1	0
QWDPRD							
R/W							
0h							

Access Types Legend

Table 3-750. QWDPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	QWDPRD	R/W	0h	QEP Watchdog Period This register contains the time-out count for the eQEP peripheral watch dog timer. When the watchdog timer value matches the watchdog period value, a watchdog timeout interrupt is generated. Reset Source: eqep_rst_mod_g_rst_n

3.10.12 MEM_QDECCTL Registers

3.10.12.1 MEM_QDECCTL Register (Offset = 28h) [reset = 0h]

Short Description: Quadrature Decoder Contro

Long Description: Quadrature Decoder Control

Return to Summary Table

Table 3-751. Instance Table

Instance Name	Physical Address
EQEP0	5027 0028h
EQEP1	5027 1028h
EQEP2	5027 2028h

Figure 3-321. QDECCTL Name Register

15	14	13	12	11	10	9	8
QSRC		SOEN	SPSEL	XCR	SWAP	IGATE	QAP
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
QBP	QIP	QSP	RESERVED_1				QIDIRE
R/W	R/W	R/W	R				R/W
0h	0h	0h	0h				0h

Access Types Legend

Table 3-752. QDECCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	QSRC	R/W	0h	Position-counter source selection Reset Source: eqep_rst_mod_g_rst_n
13	SOEN	R/W	0h	Sync output-enable Reset Source: eqep_rst_mod_g_rst_n 1 SYNC_ENABLE Enable position-compare sync output
12	SPSEL	R/W	0h	Sync output pin selection Reset Source: eqep_rst_mod_g_rst_n 1 STROBE_PIN Strobe pin is used for sync output
11	XCR	R/W	0h	External Clock Rate Reset Source: eqep_rst_mod_g_rst_n 1 XCR_1XRESOL 1x resolution: Count the rising edge only
10	SWAP	R/W	0h	CLK/DIR Signal Source for Position Counter Reset Source: eqep_rst_mod_g_rst_n 1 SWAP_ENABLE Quadrature-clock inputs are swapped
9	IGATE	R/W	0h	Index pulse gating option Reset Source: eqep_rst_mod_g_rst_n 1 IGATE_ENABLE Gate the index pin with strobe
8	QAP	R/W	0h	QEPA input polarity Reset Source: eqep_rst_mod_g_rst_n 1 QAP_POLAR Negates QEPA input
7	QBP	R/W	0h	QEPB input polarity Reset Source: eqep_rst_mod_g_rst_n 1 QBP_POLAR Negates QEPB input
6	QIP	R/W	0h	QEPI input polarity Reset Source: eqep_rst_mod_g_rst_n 1 QIP_POLAR Negates QEPI input
5	QSP	R/W	0h	QEPS input polarity Reset Source: eqep_rst_mod_g_rst_n 1 QSP_POLAR Negates QEPS input
4:1	RESERVED_1	R	0h	Reserved Reset Source: eqep_rst_mod_g_rst_n
0	QIDIRE	R/W	0h	0 - Compatible mode, Behavior same as existing devices 1 - Enhancement for Direction change during Index will be enabled Reset Source: eqep_rst_mod_g_rst_n

3.10.13 MEM_QEPCTL Registers

3.10.13.1 MEM_QEPCTL Register (Offset = 2Ah) [reset = 0h]

Short Description: QEP Control

Long Description: QEP Control

Return to Summary Table

Table 3-753. Instance Table

Instance Name	Physical Address
EQEP0	5027 002Ah
EQEP1	5027 102Ah
EQEP2	5027 202Ah

Figure 3-322. QEPCTL Name Register

15	14	13	12	11	10	9	8
FREE_SOFT		PCRM		SEI		IEI	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	
7	6	5	4	3	2	1	0
SWI	SEL	IEL		QPEN	QCLM	UTE	WDE
R/W	R/W	R/W		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Access Types Legend

Table 3-754. QEPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	FREE_SOFT	R/W	0h	Emulation mode Reset Source: eqep_rst_mod_g_rst_n 3 FREE_SOFT_3 Same as FREE_SOFT_2 2 FREE_SOFT_2 QPOSCNT behavior Position counter is unaffected by emulation suspend 2h (R/W) = QWDTMR behavior Watchdog counter is unaffected by emulation suspend 2h (R/W) = QUTMR behavior Unit timer is unaffected by emulation suspend 2h (R/W) = QCTMR behavior Capture Timer is unaffected by emulation suspend 1 FREE_SOFT_1 QPOSCNT behavior Position counter continues to count until the rollover 1h (R/W) = QWDTMR behavior Watchdog counter counts until WD period match roll over 1h (R/W) = QUTMR behavior Unit timer counts until period rollover 1h (R/W) = QCTMR behavior Capture Timer counts until next unit period event
13:12	PCRM	R/W	0h	Postion counter reset Reset Source: eqep_rst_mod_g_rst_n 3 PCRM_TIMEEVENT Position counter reset on a unit time event 2 PCRM_FIRSTINDEX Position counter reset on the first index event 1 PCRM_MAXPOS Position counter reset on the maximum position
11:10	SEI	R/W	0h	Strobe event initialization of position counter Reset Source: eqep_rst_mod_g_rst_n 3 SEI_INITQEPSCLOCK Clockwise Direction: Initializes the position counter on the rising edge of QEPS strobe Counter Clockwise Direction: Initializes the position counter on the falling edge of QEPS strobe 2 SEI_INITQEPSRISING Initializes the position counter on rising edge of the QEPS signal 1 SEI_NOTHING1 Does nothing (action disabled)
9:8	IEI	R/W	0h	Index event init of position count Reset Source: eqep_rst_mod_g_rst_n 3 IEI_INITFALLING Initializes the position counter on the falling edge of QEPI signal (QPOSCNT = QPOSINIT) 2 IEI_INITRISING Initializes the position counter on the rising edge of the QEPI signal (QPOSCNT = QPOSINIT) 1 IEI_NOTHING1 Do nothing (action disabled)

Table 3-754. QEPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	SWI	R/W	0h	Software init position counter Reset Source: eqep_rst_mod_g_rst_n 1 SWI_INITPOS Initialize position counter (QPOSCNT=QPOSINIT). This bit is not cleared automatically
6	SEL	R/W	0h	Strobe event latch of position counter Reset Source: eqep_rst_mod_g_rst_n 1 SEL_QEPSCLOCK Clockwise Direction: Position counter is latched on rising edge of QEPS strobe Counter Clockwise Direction: Position counter is latched on falling edge of QEPS strobe
5:4	IEL	R/W	0h	Index event latch of position counter [software index marker] Reset Source: eqep_rst_mod_g_rst_n 3 IEL_SIM Software index marker. Latches the position counter and quadrature direction flag on index event marker. The position counter is latched to the QPOSILAT register and the direction flag is latched in the QEPSTS[QDLF] bit. This mode is useful for software index marking. 2 IEL_POSFALLING Latches position counter on falling edge of the index signal 1 IEL_POSRISING Latches position counter on rising edge of the index signal
3	QPEN	R/W	0h	Quadrature position counter enable/software reset Reset Source: eqep_rst_mod_g_rst_n 1 QPEN_ENABLE eQEP position counter is enabled
2	QCLM	R/W	0h	QEP capture latch mode Reset Source: eqep_rst_mod_g_rst_n 1 QCLM_TIMEOUT Latch on unit time out. Position counter, capture timer and capture period values are latched into QPOSLAT, QCTMRLAT and QCPRDLAT registers on unit time out.
1	UTE	R/W	0h	QEP unit timer enable Reset Source: eqep_rst_mod_g_rst_n 1 UTE_ENABLE Enable unit timer
0	WDE	R/W	0h	QEP watchdog enable Reset Source: eqep_rst_mod_g_rst_n 1 WDE_ENABLE Enable the eQEP watchdog timer

3.10.14 MEM_QCAPCTL Registers

3.10.14.1 MEM_QCAPCTL Register (Offset = 2Ch) [reset = 0h]

Short Description: Qaudrature Capture Contro

Long Description: Qaudrature Capture Control

Return to Summary Table

Table 3-755. Instance Table

Instance Name	Physical Address
EQEP0	5027 002Ch
EQEP1	5027 102Ch
EQEP2	5027 202Ch

Figure 3-323. QCAPCTL Name Register

15	14	13	12	11	10	9	8
CEN	RESERVED_1						
R/W	R						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED_1	CCPS			UPPS			
R	R/W			R/W			
0h	0h			0h			

Access Types Legend

Table 3-756. QCAPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CEN	R/W	0h	Enable eQEP capture Reset Source: eqep_rst_mod_g_rst_n 1 CEN_ENABLE eQEP capture unit is enabled
14:7	RESERVED_1	R	0h	Reserved Reset Source: eqep_rst_mod_g_rst_n
6:4	CCPS	R/W	0h	eQEP capture timer clock prescaler Reset Source: eqep_rst_mod_g_rst_n 7 SYSCLKOUT128 CAPCLK = SYSCLKOUT/128 6 SYSCLKOUT64 CAPCLK = SYSCLKOUT/64 5 SYSCLKOUT32 CAPCLK = SYSCLKOUT/32 4 SYSCLKOUT16 CAPCLK = SYSCLKOUT/16 3 SYSCLKOUT8 CAPCLK = SYSCLKOUT/8 2 SYSCLKOUT4 CAPCLK = SYSCLKOUT/4 1 SYSCLKOUT2 CAPCLK = SYSCLKOUT/2
3:0	UPPS	R/W	0h	Unit position event prescaler Reset Source: eqep_rst_mod_g_rst_n 15 QCLK_RSVD3 Reserved 14 QCLK_RSVD2 Reserved 13 QCLK_RSVD1 Reserved 12 QCLK_RSVD0 Reserved 11 QCLK2048 UPEVNT = QCLK/2048 10 QCLK1024 UPEVNT = QCLK/1024 9 QCLK512 UPEVNT = QCLK/512 8 QCLK256 UPEVNT = QCLK/256 7 QCLK128 UPEVNT = QCLK/128 6 QCLK64 UPEVNT = QCLK/64 5 QCLK32 UPEVNT = QCLK/32 4 QCLK16 UPEVNT = QCLK/16 3 QCLK8 UPEVNT = QCLK/8 2 QCLK4 UPEVNT = QCLK/4 1 QCLK2 UPEVNT = QCLK/2

3.10.15 MEM_QPOSCTL Registers

3.10.15.1 MEM_QPOSCTL Register (Offset = 2Eh) [reset = 0h]

Short Description: Position Compare Control

Long Description: Position Compare Control

Return to Summary Table

Table 3-757. Instance Table

Instance Name	Physical Address
EQEP0	5027 002Eh
EQEP1	5027 102Eh
EQEP2	5027 202Eh

Figure 3-324. QPOSCTL Name Register

15	14	13	12	11	10	9	8
PCSHDW	PCLOAD	PCPOL	PCE	PCSPW			
R/W	R/W	R/W	R/W	R/W			
0h	0h	0h	0h	0h			
7	6	5	4	3	2	1	0
PCSPW							
R/W							
0h							

Access Types Legend

Table 3-758. QPOSCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PCSHDW	R/W	0h	Position compare of shadow enable Reset Source: eqep_rst_mod_g_rst_n 1 PCSHDW_ENABLE Shadow enabled
14	PCLOAD	R/W	0h	Position compare of shadow load Reset Source: eqep_rst_mod_g_rst_n 1 PCLOAD_QPOSCMP Load when QPOSCNT = QPOSCMP
13	PCPOL	R/W	0h	Polarity of sync output Reset Source: eqep_rst_mod_g_rst_n 1 PCPOL_LOW Active LOW pulse output
12	PCE	R/W	0h	Position compare enable/disable Reset Source: eqep_rst_mod_g_rst_n 1 PCE_ENABLE Enable position compare unit
11:0	PCSPW	R/W	0h	Select-position-compare sync output pulse width Reset Source: eqep_rst_mod_g_rst_n 4095 SYSCLKOUT16384 4096 * 4 * SYSCLKOUT cycles 1 SYSCLKOUT8 2 * 4 * SYSCLKOUT cycles

3.10.16 MEM_QEINT Registers

3.10.16.1 MEM_QEINT Register (Offset = 30h) [reset = 0h]

Short Description: QEP Interrupt Control

Long Description: QEP Interrupt Control

Return to Summary Table

Table 3-759. Instance Table

Instance Name	Physical Address
EQEP0	5027 0030h
EQEP1	5027 1030h
EQEP2	5027 2030h

Figure 3-325. QEINT Name Register

15	14	13	12	11	10	9	8
RESERVED_2			QMAE	UTO	IEL	SEL	PCM
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
PCR	PCO	PCU	WTO	QDC	QPE	PCE	RESERVED_1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 3-760. QEINT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_2	R	0h	Reserved Reset Source: eqep_rst_mod_g_rst_n
12	QMAE	R/W	0h	QMA Error Interrupt enable Reset Source: eqep_rst_mod_g_rst_n 1 QMAE_ENABLE Interrupt is enabled
11	UTO	R/W	0h	Unit time out interrupt enable Reset Source: eqep_rst_mod_g_rst_n 1 UTO_ENABLE Interrupt is enabled
10	IEL	R/W	0h	Index event latch interrupt enable Reset Source: eqep_rst_mod_g_rst_n 1 IEL_ENABLE Interrupt is enabled
9	SEL	R/W	0h	Strobe event latch interrupt enable Reset Source: eqep_rst_mod_g_rst_n 1 SEL_ENABLE Interrupt is enabled
8	PCM	R/W	0h	Position-compare match interrupt enable Reset Source: eqep_rst_mod_g_rst_n 1 PCM_ENABLE Interrupt is enabled
7	PCR	R/W	0h	Position-compare ready interrupt enable Reset Source: eqep_rst_mod_g_rst_n 1 PCR_ENABLE Interrupt is enabled
6	PCO	R/W	0h	Position counter overflow interrupt enable Reset Source: eqep_rst_mod_g_rst_n 1 PCO_ENABLE Interrupt is enabled
5	PCU	R/W	0h	Position counter underflow interrupt enable Reset Source: eqep_rst_mod_g_rst_n 1 PCU_ENABLE Interrupt is enabled
4	WTO	R/W	0h	Watchdog time out interrupt enable Reset Source: eqep_rst_mod_g_rst_n 1 WTO_ENABLE Interrupt is enabled
3	QDC	R/W	0h	Quadrature direction change interrupt enable Reset Source: eqep_rst_mod_g_rst_n 1 QDC_ENABLE Interrupt is enabled
2	QPE	R/W	0h	Quadrature phase error interrupt enable Reset Source: eqep_rst_mod_g_rst_n 1 QPE_ENABLE Interrupt is enabled
1	PCE	R/W	0h	Position counter error interrupt enable Reset Source: eqep_rst_mod_g_rst_n 1 PCE_ENABLE Interrupt is enabled
0	RESERVED_1	R	0h	Reserved Reset Source: eqep_rst_mod_g_rst_n

3.10.17 MEM_QFLG Registers

3.10.17.1 MEM_QFLG Register (Offset = 32h) [reset = 0h]

Short Description: QEP Interrupt Flag

Long Description: QEP Interrupt Flag

Return to Summary Table

Table 3-761. Instance Table

Instance Name	Physical Address
EQEP0	5027 0032h
EQEP1	5027 1032h
EQEP2	5027 2032h

Figure 3-326. QFLG Name Register

15	14	13	12	11	10	9	8
RESERVED_1			QMAE	UTO	IEL	SEL	PCM
R			R	R	R	R	R
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
PCR	PCO	PCU	WTO	QDC	PHE	PCE	INT
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 3-762. QFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_1	R	0h	Reserved Reset Source: eqep_rst_mod_g_rst_n
12	QMAE	R	0h	QMA Error interrupt flag Reset Source: eqep_rst_mod_g_rst_n 1 QMAE_FLAG Interrupt was generated
11	UTO	R	0h	Unit time out interrupt flag Reset Source: eqep_rst_mod_g_rst_n 1 UTO_FLAG Set by eQEP unit timer period match
10	IEL	R	0h	Index event latch interrupt flag Reset Source: eqep_rst_mod_g_rst_n 1 IEL_FLAG This bit is set after latching the QPOSCNT to QPOSILAT
9	SEL	R	0h	Strobe event latch interrupt flag Reset Source: eqep_rst_mod_g_rst_n 1 SEL_FLAG This bit is set after latching the QPOSCNT to QPOSSLAT
8	PCM	R	0h	eQEP compare match event interrupt flag Reset Source: eqep_rst_mod_g_rst_n 1 PCM_FLAG This bit is set on position-compare match
7	PCR	R	0h	Position-compare ready interrupt flag Reset Source: eqep_rst_mod_g_rst_n 1 PCR_FLAG This bit is set after transferring the shadow register value to the active position compare register
6	PCO	R	0h	Position counter overflow interrupt flag Reset Source: eqep_rst_mod_g_rst_n 1 PCO_FLAG This bit is set on position counter overflow.
5	PCU	R	0h	Position counter underflow interrupt flag Reset Source: eqep_rst_mod_g_rst_n 1 PCU_FLAG This bit is set on position counter underflow.
4	WTO	R	0h	Watchdog timeout interrupt flag Reset Source: eqep_rst_mod_g_rst_n 1 WTO_FLAG Set by watchdog timeout
3	QDC	R	0h	Quadrature direction change interrupt flag Reset Source: eqep_rst_mod_g_rst_n 1 QDC_FLAG Interrupt was generated

Table 3-762. QFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	PHE	R	0h	Quadrature phase error interrupt flag Reset Source: eqep_rst_mod_g_rst_n 1 PHE_FLAG Set on simultaneous transition of QEPA and QEPB
1	PCE	R	0h	Position counter error interrupt flag Reset Source: eqep_rst_mod_g_rst_n 1 PCE_FLAG Position counter error
0	INT	R	0h	Global interrupt status flag Reset Source: eqep_rst_mod_g_rst_n 1 INT_FLAG Interrupt was generated

3.10.18 MEM_QCLR Registers

3.10.18.1 MEM_QCLR Register (Offset = 34h) [reset = 0h]

Short Description: QEP Interrupt Clear

Long Description: QEP Interrupt Clear

Return to Summary Table

Table 3-763. Instance Table

Instance Name	Physical Address
EQEP0	5027 0034h
EQEP1	5027 1034h
EQEP2	5027 2034h

Figure 3-327. QCLR Name Register

15	14	13	12	11	10	9	8
RESERVED_1			QMAE	UTO	IEL	SEL	PCM
R			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
PCR	PCO	PCU	WTO	QDC	PHE	PCE	INT
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 3-764. QCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_1	R	0h	Reserved Reset Source: eqep_rst_mod_g_rst_n
12	QMAE	R/W1TS	0h	Clear QMA Error interrupt flag Reset Source: eqep_rst_mod_g_rst_n 1 QMAE_CLR Clears the interrupt flag
11	UTO	R/W1TS	0h	Clear unit time out interrupt flag Reset Source: eqep_rst_mod_g_rst_n 1 UTO_CLR Clears the interrupt flag
10	IEL	R/W1TS	0h	Clear index event latch interrupt flag Reset Source: eqep_rst_mod_g_rst_n 1 IEL_CLR Clears the interrupt flag
9	SEL	R/W1TS	0h	Clear strobe event latch interrupt flag Reset Source: eqep_rst_mod_g_rst_n 1 SEL_CLR Clears the interrupt flag
8	PCM	R/W1TS	0h	Clear eQEP compare match event interrupt flag Reset Source: eqep_rst_mod_g_rst_n 1 PCM_CLR Clears the interrupt flag
7	PCR	R/W1TS	0h	Clear position-compare ready interrupt flag Reset Source: eqep_rst_mod_g_rst_n 1 PCR_CLR Clears the interrupt flag
6	PCO	R/W1TS	0h	Clear position counter overflow interrupt flag Reset Source: eqep_rst_mod_g_rst_n 1 PCO_CLR Clears the interrupt flag
5	PCU	R/W1TS	0h	Clear position counter underflow interrupt flag Reset Source: eqep_rst_mod_g_rst_n 1 PCU_CLR Clears the interrupt flag
4	WTO	R/W1TS	0h	Clear watchdog timeout interrupt flag Reset Source: eqep_rst_mod_g_rst_n 1 WTO_CLR Clears the interrupt flag
3	QDC	R/W1TS	0h	Clear quadrature direction change interrupt flag Reset Source: eqep_rst_mod_g_rst_n 1 QDC_CLR Clears the interrupt flag
2	PHE	R/W1TS	0h	Clear quadrature phase error interrupt flag Reset Source: eqep_rst_mod_g_rst_n 1 PHE_CLR Clears the interrupt flag
1	PCE	R/W1TS	0h	Clear position counter error interrupt flag Reset Source: eqep_rst_mod_g_rst_n 1 PCE_CLR Clears the interrupt flag

Table 3-764. QCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	INT	R/W1TS	0h	Global interrupt clear flag Reset Source: eqep_rst_mod_g_rst_n 1 INT_CLR Clears the interrupt flag

3.10.19 MEM_QFRC Registers

3.10.19.1 MEM_QFRC Register (Offset = 36h) [reset = 0h]

Short Description: QEP Interrupt Force

Long Description: QEP Interrupt Force

Return to Summary Table

Table 3-765. Instance Table

Instance Name	Physical Address
EQEP0	5027 0036h
EQEP1	5027 1036h
EQEP2	5027 2036h

Figure 3-328. QFRC Name Register

15	14	13	12	11	10	9	8
RESERVED_2			QMAE	UTO	IEL	SEL	PCM
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
PCR	PCO	PCU	WTO	QDC	PHE	PCE	RESERVED_1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 3-766. QFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_2	R	0h	Reserved Reset Source: eqep_rst_mod_g_rst_n
12	QMAE	R/W	0h	Force QMA error interrupt Reset Source: eqep_rst_mod_g_rst_n 1 QMAE_FORCE Force the interrupt
11	UTO	R/W	0h	Force unit time out interrupt Reset Source: eqep_rst_mod_g_rst_n 1 UTO_FORCE Force the interrupt
10	IEL	R/W	0h	Force index event latch interrupt Reset Source: eqep_rst_mod_g_rst_n 1 IEL_FORCE Force the interrupt
9	SEL	R/W	0h	Force strobe event latch interrupt Reset Source: eqep_rst_mod_g_rst_n 1 SEL_FORCE Force the interrupt
8	PCM	R/W	0h	Force position-compare match interrupt Reset Source: eqep_rst_mod_g_rst_n 1 PCM_FORCE Force the interrupt
7	PCR	R/W	0h	Force position-compare ready interrupt Reset Source: eqep_rst_mod_g_rst_n 1 PCR_FORCE Force the interrupt
6	PCO	R/W	0h	Force position counter overflow interrupt Reset Source: eqep_rst_mod_g_rst_n 1 PCO_FORCE Force the interrupt
5	PCU	R/W	0h	Force position counter underflow interrupt Reset Source: eqep_rst_mod_g_rst_n 1 PCU_FORCE Force the interrupt
4	WTO	R/W	0h	Force watchdog time out interrupt Reset Source: eqep_rst_mod_g_rst_n 1 WTO_FORCE Force the interrupt
3	QDC	R/W	0h	Force quadrature direction change interrupt Reset Source: eqep_rst_mod_g_rst_n 1 QDC_FORCE Force the interrupt
2	PHE	R/W	0h	Force quadrature phase error interrupt Reset Source: eqep_rst_mod_g_rst_n 1 PHE_FORCE Force the interrupt
1	PCE	R/W	0h	Force position counter error interrupt Reset Source: eqep_rst_mod_g_rst_n 1 PCE_FORCE Force the interrupt
0	RESERVED_1	R	0h	Reserved Reset Source: eqep_rst_mod_g_rst_n

3.10.20 MEM_QEPSTS Registers

3.10.20.1 MEM_QEPSTS Register (Offset = 38h) [reset = 80h]

Short Description: QEP Status

Long Description: QEP Status

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Table 3-767. Instance Table

Instance Name	Physical Address
EQEP0	5027 0038h
EQEP1	5027 1038h
EQEP2	5027 2038h

Figure 3-329. QEPSTS Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
UPEVNT	FIDF	QDF	QDLF	COEF	CDEF	FIMF	PCEF
R/W1TS	R	R	R	R/W1TS	R/W1TS	R/W1TS	R
1h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 3-768. QEPSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED_1	R	0h	Reserved Reset Source: eqep_rst_mod_g_rst_n
7	UPEVNT	R/W1TS	1h	Unit position event flag Reset Source: eqep_rst_mod_g_rst_n 1 UPEVNT_DETCT Unit position event detected. Write 1 to clear
6	FIDF	R	0h	Direction on the first index marker Status of the direction is latched on the first index event marker. Reset Source: eqep_rst_mod_g_rst_n 1 FIDF_CLK Clockwise rotation (or forward movement) on the first index event
5	QDF	R	0h	Quadrature direction flag Reset Source: eqep_rst_mod_g_rst_n 1 QDF_CLK Clockwise rotation (or forward movement)
4	QDLF	R	0h	eQEP direction latch flag Reset Source: eqep_rst_mod_g_rst_n 1 QDLF_CLK Clockwise rotation (or forward movement) on index event marker
3	COEF	R/W1TS	0h	Capture overflow error flag Reset Source: eqep_rst_mod_g_rst_n 1 COEF_OVF Overflow occurred in eQEP Capture timer (QEPCTMR). This bit is cleared by writing a '1'.
2	CDEF	R/W1TS	0h	Capture direction error flag Reset Source: eqep_rst_mod_g_rst_n 1 CDEF_DIRECT Direction change occurred between the capture position event. This bit is cleared by writing a '1'.
1	FIMF	R/W1TS	0h	First index marker flag Reset Source: eqep_rst_mod_g_rst_n 1 FIMF_SETINDEX Set by first occurrence of index pulse. This bit is cleared by writing a '1'.
0	PCEF	R	0h	Position counter error flag. This bit is not sticky and it is updated for every index event. Reset Source: eqep_rst_mod_g_rst_n 1 PCEF_ERROR Position counter error

3.10.21 MEM_QCTMR Registers

3.10.21.1 MEM_QCTMR Register (Offset = 3Ah) [reset = 0h]

Short Description: QEP Capture Timer

Long Description: QEP Capture Timer

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Table 3-769. Instance Table

Instance Name	Physical Address
EQEP0	5027 003Ah
EQEP1	5027 103Ah
EQEP2	5027 203Ah

Figure 3-330. QCTMR Name Register

15	14	13	12	11	10	9	8
QCTMR							
R/W							
0h							
7	6	5	4	3	2	1	0
QCTMR							
R/W							
0h							

Access Types Legend

Table 3-770. QCTMR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	QCTMR	R/W	0h	This register provides time base for edge capture unit. Reset Source: eqep_rst_mod_g_rst_n

3.10.22 MEM_QCPRD Registers

3.10.22.1 MEM_QCPRD Register (Offset = 3Ch) [reset = 0h]

Short Description: QEP Capture Period

Long Description: QEP Capture Period

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Table 3-771. Instance Table

Instance Name	Physical Address
EQEP0	5027 003Ch
EQEP1	5027 103Ch
EQEP2	5027 203Ch

Figure 3-331. QCPRD Name Register

15	14	13	12	11	10	9	8
QCPRD							
R/W							
0h							
7	6	5	4	3	2	1	0
QCPRD							
R/W							
0h							

Access Types Legend

Table 3-772. QCPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	QCPRD	R/W	0h	This register holds the period count value between the last successive eQEP position events Reset Source: eqep_rst_mod_g_rst_n

3.10.23 MEM_QCTMRLAT Registers

3.10.23.1 MEM_QCTMRLAT Register (Offset = 3Eh) [reset = 0h]

Short Description: QEP Capture Latch

Long Description: QEP Capture Latch

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Table 3-773. Instance Table

Instance Name	Physical Address
EQEP0	5027 003Eh
EQEP1	5027 103Eh
EQEP2	5027 203Eh

Figure 3-332. QCTMRLAT Name Register

15	14	13	12	11	10	9	8
QCTMRLAT							
R							
0h							
7	6	5	4	3	2	1	0
QCTMRLAT							
R							
0h							

Access Types Legend

Table 3-774. QCTMRLAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	QCTMRLAT	R	0h	The eQEP capture timer value can be latched into this register on two events viz., unit timeout event, reading the eQEP position counter. Reset Source: eqep_rst_mod_g_rst_n

3.10.24 MEM_QCPRDLAT Registers

3.10.24.1 MEM_QCPRDLAT Register (Offset = 40h) [reset = 0h]

Short Description: QEP Capture Period Latch

Long Description: QEP Capture Period Latch

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Table 3-775. Instance Table

Instance Name	Physical Address
EQEP0	5027 0040h
EQEP1	5027 1040h
EQEP2	5027 2040h

Figure 3-333. QCPRDLAT Name Register

15	14	13	12	11	10	9	8
QCPRDLAT							
R							
0h							
7	6	5	4	3	2	1	0
QCPRDLAT							
R							
0h							

Access Types Legend

Table 3-776. QCPRDLAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	QCPRDLAT	R	0h	eQEP capture period value can be latched into this register on two events viz., unit timeout event, reading the eQEP position counter. Reset Source: eqep_rst_mod_g_rst_n

3.10.25 MEM_REV Registers

3.10.25.1 MEM_REV Register (Offset = 60h) [reset = 11h]

Short Description: QEP Revision Number

Long Description: QEP Revision Number

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Table 3-777. Instance Table

Instance Name	Physical Address
EQEP0	5027 0060h
EQEP1	5027 1060h
EQEP2	5027 2060h

Figure 3-334. REV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1										MINOR			MAJOR		
R										R			R		
0h										2h			1h		

Access Types Legend

Table 3-778. REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED_1	R	0h	Reserved Reset Source: eqep_rst_mod_g_rst_n
5:3	MINOR	R	2h	This field specifies the Minor Revision number for the eQEP IP. Reset Source: eqep_rst_mod_g_rst_n
2:0	MAJOR	R	1h	This field specifies the Major Revision number for the eQEP IP. Reset Source: eqep_rst_mod_g_rst_n

3.10.26 MEM_QEPSTROBESEL Registers

3.10.26.1 MEM_QEPSTROBESEL Register (Offset = 64h) [reset = 0h]

Short Description: QEP Strobe select registe

Long Description: QEP Strobe select register. This feature is not applicable to AM263x products

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Table 3-779. Instance Table

Instance Name	Physical Address
EQEP0	5027 0064h
EQEP1	5027 1064h
EQEP2	5027 2064h

Figure 3-335. QEPSTROBESEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1														STROBESEL	
R														R/W	
0h														0h	

Access Types Legend

Table 3-780. QEPSTROBESEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED_1	R	0h	Reserved Reset Source: eqep_rst_mod_g_rst_n
1:0	STROBESEL	R/W	0h	Strobe source select: this feature is not applicable to AM263x products Reset Source: eqep_rst_mod_g_rst_n 3 ADCSOCB_AS_QS QEP Strobe after polarity mux ORed with ADCSOCB.this feature is not applicable to AM263x products 2 ADCSOCA_AS_QS QEP Strobe after polarity mux ORed with ADCSOCA.this feature is not applicable to AM263x products 1 QS_AFTER_POL_MUX QEP Strobe after polarity mux.this feature is not applicable to AM263x products

3.10.27 MEM_QMACTRL Registers

3.10.27.1 MEM_QMACTRL Register (Offset = 68h) [reset = 0h]

Short Description: QMA Control register

Long Description: QMA Control register

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Table 3-781. Instance Table

Instance Name	Physical Address
EQEP0	5027 0068h
EQEP1	5027 1068h
EQEP2	5027 2068h

Figure 3-336. QMACTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1													MODE		
R													R/W		
0h													0h		

Access Types Legend

Table 3-782. QMACTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED_1	R	0h	Reserved Reset Source: eqep_rst_mod_g_rst_n
2:0	MODE	R/W	0h	Select Mode for QMA mode: 000 : QMA Module is bypassed. 001 : QMA Mode-1 operation selected 010 : QMA Mode-2 operation selected 011 : QMA Module is bypassed [reserved] 1xx : QMA Module is bypassed [reserved] Reset Source: eqep_rst_mod_g_rst_n

3.10.28 MEM_QEPSRCSEL Registers

3.10.28.1 MEM_QEPSRCSEL Register (Offset = 6Ch) [reset = 0h]

Short Description: QEP Source Select Registe

Long Description: QEP Source Select Register

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Table 3-783. Instance Table

Instance Name	Physical Address
EQEP0	5027 006Ch
EQEP1	5027 106Ch
EQEP2	5027 206Ch

Figure 3-337. QEPSRCSEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_4			QEPSSEL					RESERVED_3			QEPISEL				
R			R/W					R			R/W				
0h			0h					0h			0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2			QEPBSEL					RESERVED_1			QEPASEL				
R			R/W					R			R/W				
0h			0h					0h			0h				

Access Types Legend

Table 3-784. QEPSRCSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED_4	R	0h	Reserved Reset Source: eqep_rst_mod_g_rst_n
28:24	QEPSSEL	R/W	0h	QEP Strobe source select: 0x0: Device Pin [Default] 0x1 to 0x1F : To be defined in SOC context Note: eQEP needs to be disabled before configuring these bits as it can lead to unexpected behavior if eQEP is running. Reset Source: eqep_rst_mod_g_rst_n
23:21	RESERVED_3	R	0h	Reserved Reset Source: eqep_rst_mod_g_rst_n
20:16	QEPISEL	R/W	0h	QEP Index source select: 0x0: Device Pin [Default] 0x1 to 0x1F : To be defined in SOC context Note: eQEP needs to be disabled before configuring these bits as it can lead to unexpected behavior if eQEP is running. Reset Source: eqep_rst_mod_g_rst_n
15:13	RESERVED_2	R	0h	Reserved Reset Source: eqep_rst_mod_g_rst_n
12:8	QEPBSEL	R/W	0h	QEPB source select: 0x0: Device Pin [Default] 0x1 to 0x1F : To be defined in SOC context Note: eQEP needs to be disabled before configuring these bits as it can lead to unexpected behavior if eQEP is running. Reset Source: eqep_rst_mod_g_rst_n
7:5	RESERVED_1	R	0h	Reserved Reset Source: eqep_rst_mod_g_rst_n
4:0	QEPASEL	R/W	0h	QEPA source select: 0x0: Device Pin [Default] 0x1 to 0x1F : To be defined in SOC context Note: eQEP needs to be disabled before configuring these bits as it can lead to unexpected behavior if eQEP is running. Reset Source: eqep_rst_mod_g_rst_n

3.10.29 Access Table

Table 3-785. Access Type Codes

Access Type	Code	Description
R/W	R/W	Read / Write
R	R	Read

Table 3-785. Access Type Codes (continued)

Access Type	Code	Description
R/W1TS	R/W1TS	Read/Write 1 To Set

3.11 FSI_RX Registers

Table 3-786. MEM, MEM Registers, Base Address=0X0000000050290000, Length=4096

Offset	Length	Register Name	fsi_rx0 Physical Address	fsi_rx1 Physical Address	fsi_rx2 Physical Address
0h	16	RX_MASTER_CTRL_ALTC_	5029 0000h	5029 1000h	502B 0000h
8h	16	RX_OPER_CTRL	5029 0008h	5029 1008h	502B 0008h
Ch	16	RX_FRAME_INFO	5029 000Ch	5029 100Ch	502B 000Ch
Eh	16	RX_FRAME_TAG_UDATA	5029 000Eh	5029 100Eh	502B 000Eh
10h	16	RX_DMA_CTRL	5029 0010h	5029 1010h	502B 0010h
14h	16	RX_EVT_STS_ALT1_	5029 0014h	5029 1014h	502B 0014h
16h	16	RX_CRC_INFO	5029 0016h	5029 1016h	502B 0016h
18h	16	RX_EVT_CLR_ALT1_	5029 0018h	5029 1018h	502B 0018h
1Ah	16	RX_EVT_FRC_ALT1_	5029 001Ah	5029 101Ah	502B 001Ah
1Ch	16	RX_BUF_PTR_LOAD	5029 001Ch	5029 101Ch	502B 001Ch
1Eh	16	RX_BUF_PTR_STS	5029 001Eh	5029 101Eh	502B 001Eh
20h	16	RX_FRAME_WD_CTRL	5029 0020h	5029 1020h	502B 0020h
24h	32	RX_FRAME_WD_REF	5029 0024h	5029 1024h	502B 0024h
28h	32	RX_FRAME_WD_CNT	5029 0028h	5029 1028h	502B 0028h
2Ch	16	RX_PING_WD_CTRL	5029 002Ch	5029 102Ch	502B 002Ch
2Eh	16	RX_PING_TAG	5029 002Eh	5029 102Eh	502B 002Eh
30h	32	RX_PING_WD_REF	5029 0030h	5029 1030h	502B 0030h
34h	32	RX_PING_WD_CNT	5029 0034h	5029 1034h	502B 0034h
38h	16	RX_INT1_CTRL_ALT1_	5029 0038h	5029 1038h	502B 0038h
3Ah	16	RX_INT2_CTRL_ALT1_	5029 003Ah	5029 103Ah	502B 003Ah
3Ch	16	RX_LOCK_CTRL	5029 003Ch	5029 103Ch	502B 003Ch
40h	32	RX_ECC_DATA	5029 0040h	5029 1040h	502B 0040h
44h	16	RX_ECC_VAL	5029 0044h	5029 1044h	502B 0044h
48h	32	RX_ECC_SEC_DATA	5029 0048h	5029 1048h	502B 0048h
4Ch	16	RX_ECC_LOG	5029 004Ch	5029 104Ch	502B 004Ch
50h	16	RX_FRAME_TAG_CMP	5029 0050h	5029 1050h	502B 0050h
52h	16	RX_PING_TAG_CMP	5029 0052h	5029 1052h	502B 0052h
58h	32	RX_TRIG_CTRL_0	5029 0058h	5029 1058h	502B 0058h
5Ch	32	RX_TRIG_WIDTH_0	5029 005Ch	5029 105Ch	502B 005Ch
60h	16	RX_DLYLINE_CTRL	5029 0060h	5029 1060h	502B 0060h
64h	32	RX_TRIG_CTRL_1	5029 0064h	5029 1064h	502B 0064h
68h	32	RX_TRIG_CTRL_2	5029 0068h	5029 1068h	502B 0068h
6Ch	32	RX_TRIG_CTRL_3	5029 006Ch	5029 106Ch	502B 006Ch
70h	32	RX_VIS_1	5029 0070h	5029 1070h	502B 0070h
74h	16	RX_UDATA_FILTER	5029 0074h	5029 1074h	502B 0074h
80h + Formula	16	RX_BUF_BASE_N	5029 0080h + Formula	5029 1080h + Formula	502B 0080h + Formula

Table 3-787. MEM, MEM Registers, Base Address=0X0000000050290000, Length=4096

Offset	Length	Register Name	fsi_rx3 Physical Address
0h	16	RX_MASTER_CTRL_ALTC_	502B 1000h
8h	16	RX_OPER_CTRL	502B 1008h
Ch	16	RX_FRAME_INFO	502B 100Ch
Eh	16	RX_FRAME_TAG_UDATA	502B 100Eh

Table 3-787. MEM, MEM Registers, Base Address=0X0000000050290000, Length=4096 (continued)

Offset	Length	Register Name	fsi_rx3 Physical Address
10h	16	RX_DMA_CTRL	502B 1010h
14h	16	RX_EVT_STS_ALT1_	502B 1014h
16h	16	RX_CRC_INFO	502B 1016h
18h	16	RX_EVT_CLR_ALT1_	502B 1018h
1Ah	16	RX_EVT_FRC_ALT1_	502B 101Ah
1Ch	16	RX_BUF_PTR_LOAD	502B 101Ch
1Eh	16	RX_BUF_PTR_STS	502B 101Eh
20h	16	RX_FRAME_WD_CTRL	502B 1020h
24h	32	RX_FRAME_WD_REF	502B 1024h
28h	32	RX_FRAME_WD_CNT	502B 1028h
2Ch	16	RX_PING_WD_CTRL	502B 102Ch
2Eh	16	RX_PING_TAG	502B 102Eh
30h	32	RX_PING_WD_REF	502B 1030h
34h	32	RX_PING_WD_CNT	502B 1034h
38h	16	RX_INT1_CTRL_ALT1_	502B 1038h
3Ah	16	RX_INT2_CTRL_ALT1_	502B 103Ah
3Ch	16	RX_LOCK_CTRL	502B 103Ch
40h	32	RX_ECC_DATA	502B 1040h
44h	16	RX_ECC_VAL	502B 1044h
48h	32	RX_ECC_SEC_DATA	502B 1048h
4Ch	16	RX_ECC_LOG	502B 104Ch
50h	16	RX_FRAME_TAG_CMP	502B 1050h
52h	16	RX_PING_TAG_CMP	502B 1052h
58h	32	RX_TRIG_CTRL_0	502B 1058h
5Ch	32	RX_TRIG_WIDTH_0	502B 105Ch
60h	16	RX_DLYLINE_CTRL	502B 1060h
64h	32	RX_TRIG_CTRL_1	502B 1064h
68h	32	RX_TRIG_CTRL_2	502B 1068h
6Ch	32	RX_TRIG_CTRL_3	502B 106Ch
70h	32	RX_VIS_1	502B 1070h
74h	16	RX_UDATA_FILTER	502B 1074h
80h + Formula	16	RX_BUF_BASE_N	502B 1080h + Formula

3.11.1 MEM_RX_MASTER_CTRL_ALTC_ Registers

3.11.1.1 MEM_MASTER_CTRL_ALTC_ Register (Offset = 0h) [reset = 0h]

Short Description: Receive master control re

Long Description: Receive master control register

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Table 3-788. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0000h
FSI_RX1	5029 1000h
FSI_RX2	502B 0000h
FSI_RX3	502B 1000h

Figure 3-338. RX_MASTER_CTRL_ALTC_ Name Register

15	14	13	12	11	10	9	8
KEY							
W							
0h							
7	6	5	4	3	2	1	0
RESERVED_1			DATA_FILTER_EN	INPUT_ISOLATE	SPI_PAIRING	INT_LOOPBACK	CORE_RST
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Access Types Legend

Table 3-789. RX_MASTER_CTRL_ALTC_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	KEY	W	0h	Write Key. In order to write to this register, 0xA5 must be written to this field at the same time. Otherwise, writes are ignored. The key is cleared immediately after writing, so it must be written again for every change to this register. Reset Source: fsi_rx_rst_mod_g_rst_n
7:5	RESERVED_1	R	0h	Reserved Reset Source: fsi_rx_rst_mod_g_rst_n
4	DATA_FILTER_EN	R/W	0h	Data Filter Enable Bit. 0h [R/W] = Data filtering is disabled. 1h [R/W] = Data filtering is enabled. Reset Source: fsi_rx_rst_mod_g_rst_n
3	INPUT_ISOLATE	R/W	0h	When set to 1, the FSI RX inputs [RXCLK, RXD0 and RXD1] will be isolated from what is driven from the device pins and will be held at inactive level of '1'.This isolation facilitates the user to switch the RX inputs to a different set of device pins and hence any potential glitch that could occur during the process of switching will not affect the RX module itself. Reset Source: fsi_rx_rst_mod_g_rst_n
2	SPI_PAIRING	R/W	0h	Clock Pairing for SPI-like Behavior Enable bit This bit enables the internal clock pairing with the FSI TX module. This feature internally connects the TXCLK to RXCLK allowing the FSI TX module, acting as a SPI master, to clock data into the receiver and out of the transmitter like a standard SPI module. This configuration is valid when the Module is in SPI mode only [RX_OPER_CTRL.SPI_MODE = 1] 0h [R/W] = SPI clock pairing is not enabled. 1h [R/W] = SPI clock pairing is enabled. The RXCLK will be internally connected to the TXCLK of the corresponding FSI module. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect. Reset Source: fsi_rx_rst_mod_g_rst_n

Table 3-789. RX_MASTER_CTRL_ALTC_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	INT_LOOPBACK	R/W	0h	Internal Loopback Enable bit This bit enables the internal loopback functionality of the FSI receiver. By enabling this bit, a mux will select the signals coming directly from the corresponding FSI transmitter module rather than from the pins. 0h [R/W] = Internal loopback is disabled. The FSI RX module will receive signals coming from the pins. 1h [R/W] = Internal loopback is enabled. The FSI RX module will receive signals from the directly from FSI TX module rather than the pins. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect. Reset Source: fsi_rx_rst_mod_g_rst_n
0	CORE_RST	R/W	0h	Receiver Master Core Reset bit This bit controls the receiver master core reset. In order to receive any frame, this bit must be cleared. Note: For reset to take affect, the FSI RX module must be held in reset for at least 4 SYSCLK cycles. 0h [R/W] = Receiver core is not in reset and can receive frames. 1h [R/W] = Receiver core is held in reset. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect. Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.2 MEM_RX_OPER_CTRL Registers

3.11.2.1 MEM_OPER_CTRL Register (Offset = 8h) [reset = 0h]

Short Description: Receive operation control

Long Description: Receive operation control register

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Table 3-790. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0008h
FSI_RX1	5029 1008h
FSI_RX2	502B 0008h
FSI_RX3	502B 1008h

Figure 3-339. RX_OPER_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED_1							PING_WD_RST_MODE
R							R/W
0h							0h
7	6	5	4	3	2	1	0
ECC_SEL	N_WORDS				SPI_MODE	DATA_WIDTH	
R/W	R/W				R/W	R/W	
0h	0h				0h	0h	

Access Types Legend

Table 3-791. RX_OPER_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	RESERVED_1	R	0h	Reserved Reset Source: fsi_rx_rst_mod_g_rst_n
8	PING_WD_RST_MODE	R/W	0h	Ping Watchdog Timeout Mode Select bit This bit selects the mode by which the ping watchdog counter is reset. The watchdog counter can be reset and restarted only by ping frames or by any received frame. 0h [R/W] = The ping watchdog counter will reset and restart only by ping frames. 1h [R/W] = The ping watchdog counter will reset and restart by any received frame. Reset Source: fsi_rx_rst_mod_g_rst_n
7	ECC_SEL	R/W	0h	ECC Data Width Select bit This bit selects between whether the ECC computation is done on 16-bit or 32-bit words. 0h [R/W] = 32-bit ECC is used. 1h [R/W] = 16-bit ECC is used. Reset Source: fsi_rx_rst_mod_g_rst_n
6:3	N_WORDS	R/W	0h	Number of Words to Receive This field defines the number of words which will be received in a DATA_N_WORD frame. This is a user-defined field that must match the corresponding field in the transmitter. Set this bitfield to be one less than the number of words to be received. This value is only applicable when the frame type received is DATA_N_WORD. 0h [R/W] = 1 data word frame [16-bit data]. 1h [R/W] = 2 data word frame [32-bit data]. .. Fh [R/W] = 16 data word frame [256-bit data]. Reset Source: fsi_rx_rst_mod_g_rst_n
2	SPI_MODE	R/W	0h	SPI Mode Enable bit This bit enables and disables the SPI compatibility mode of the FSI RX. The received data must be formatted as an FSI frame in order for the data to properly be received. SPI compatibility mode will allow FSI RX to receive data that is sent using SPI signal format. Refer to the applicable section in the FSI TRM chapter for more information. 0h [R/W] = FSI is in normal mode of operation. 1h [R/W] = FSI is operating in SPI compatibility mode. Reset Source: fsi_rx_rst_mod_g_rst_n

Table 3-791. RX_OPER_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	DATA_WIDTH	R/W	0h	Receive Data Width Select bit These bits decide the number of data lines used for receiving data. 0h [R/W] = Data will be received on one data line, RXD0. 1h [R/W] = Data will be received on two data lines, RXD0 and RXD1. 2h, 3h [R/W] = Reserved Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.3 MEM_RX_FRAME_INFO Registers

3.11.3.1 MEM_FRAME_INFO Register (Offset = Ch) [reset = 0h]

Short Description: Receive frame control reg

Long Description: Receive frame control register

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Table 3-792. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 000Ch
FSI_RX1	5029 100Ch
FSI_RX2	502B 000Ch
FSI_RX3	502B 100Ch

Figure 3-340. RX_FRAME_INFO Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1				FRAME_TYPE			
R				R			
0h				0h			

Access Types Legend

Table 3-793. RX_FRAME_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED_1	R	0h	Reserved Reset Source: fsi_rx_rst_mod_g_rst_n
3:0	FRAME_TYPE	R	0h	Received Frame Type This field indicates the type of frame that was successfully received last. 0000b [R/W] = A ping frame was received 0100b [R/W] = A DATA_1_WORD frame was received [16-bit data]. 0101b [R/W] = A DATA_2_WORD frame was received [32-bit data]. 0110b [R/W] = A DATA_4_WORD frame was received [64-bit data]. 0111b [R/W] = A DATA_6_WORD frame was received [96-bit data]. 0011b [R/W] = A DATA_N_WORD frame was received. The N_WORD field will determine the number of words [1 to 16] to be sent. The number of words received must equal the value programmed in RX_OPER_CTRL.N_WORDS. 1111b [R/W] = An error frame was received. This frame can be used during error conditions or any condition where the transmitter wants to signal the receiver for attention. However, the user software is at liberty to use this for any purpose. 0001b, 0010b, and 1000b through 1110b are Reserved and should not be used. Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.4 MEM_RX_FRAME_TAG_UDATA Registers

3.11.4.1 MEM_FRAME_TAG_UDATA Register (Offset = Eh) [reset = 0h]

Short Description: Receive frame tag and use

Long Description: Receive frame tag and user data register

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Table 3-794. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 000Eh
FSI_RX1	5029 100Eh
FSI_RX2	502B 000Eh
FSI_RX3	502B 100Eh

Figure 3-341. RX_FRAME_TAG_UDATA Name Register

15	14	13	12	11	10	9	8
USER_DATA							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1			FRAME_TAG				ZERO
R			R				R
0h			0h				0h

Access Types Legend

Table 3-795. RX_FRAME_TAG_UDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	USER_DATA	R	0h	Received User Data This field contains the 8-bit user data field of the last successfully received frame. Reset Source: fsi_rx_rst_mod_g_rst_n
7:5	RESERVED_1	R	0h	Reserved Reset Source: fsi_rx_rst_mod_g_rst_n
4:1	FRAME_TAG	R	0h	Received Frame Tag This field contains the 4-bit frame tag from the last successfully received frame. This is intentionally shifted into bits 4:1 so that the register can be used as a 32-bit address index based on the received tag. Reset Source: fsi_rx_rst_mod_g_rst_n
0	ZERO	R	0h	Zero bit This bit will always read as 0. This is intentionally provided to create a 32-bit offset if required. Using the FRAME_TAG and ZERO bits of this register [bits 4:0], application software can directly index into an array of 32-bit data. Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.5 MEM_RX_DMA_CTRL Registers

3.11.5.1 MEM_DMA_CTRL Register (Offset = 10h) [reset = 0h]

Short Description: Receive DMA event control

Long Description: Receive DMA event control register

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Table 3-796. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0010h
FSI_RX1	5029 1010h
FSI_RX2	502B 0010h
FSI_RX3	502B 1010h

Figure 3-342. RX_DMA_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1							DMA_EVT_EN
R							R/W
0h							0h

Access Types Legend

Table 3-797. RX_DMA_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	RESERVED_1	R	0h	Reserved Reset Source: fsi_rx_rst_mod_g_rst_n
0	DMA_EVT_EN	R/W	0h	DMA Event Enable bit This bit will enable a DMA Event to be generated upon the completion of a frame reception. 0h [R/W] = A DMA event will not be generated. 1h [R/W] = A DMA event will be generated upon the reception of a frame. Note: The DMA event will only be generated for data frames. Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.6 MEM_RX_EVT_STS_ALT1_ Registers

3.11.6.1 MEM_EVT_STS_ALT1_ Register (Offset = 14h) [reset = 0h]

Short Description: Receive event and error s

Long Description: Receive event and error status flag register

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Table 3-798. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0014h
FSI_RX1	5029 1014h
FSI_RX2	502B 0014h
FSI_RX3	502B 1014h

Figure 3-343. RX_EVT_STS_ALT1_ Name Register

15	14	13	12	11	10	9	8
RESERVED_1	ERROR_TAG_MATCH	DATA_TAG_MATCH	PING_TAG_MATCH	DATA_FRAME	FRAME_OVERRUN	PING_FRAME	ERR_FRAME
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
BUF_UNDERRUN	FRAME_DONE	BUF_OVERRUN	EOF_ERR	TYPE_ERR	CRC_ERR	FRAME_WD_TO	PING_WD_TO
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 3-799. RX_EVT_STS_ALT1_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved Reset Source: fsi_rx_rst_mod_g_rst_n
14	ERROR_TAG_MATCH	R	0h	Error Tag Match Flag This bit indicates that an error frame was received with a tag comparison matching the masked tag reference. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h [R] = No tag-matched error frame received. 1h [R] = A tag-matched error frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset Source: fsi_rx_rst_mod_g_rst_n
13	DATA_TAG_MATCH	R	0h	Data Tag Match Flag This bit indicates that a dataframe was received with a tag comparison matching the masked tag reference. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h [R] = No tag-matched data frame received. 1h [R] = A tag-matched data frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset Source: fsi_rx_rst_mod_g_rst_n
12	PING_TAG_MATCH	R	0h	Ping Tag Match Flag This bit indicates that a ping frame was received with a tag comparison matching the masked tag reference. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h [R] = No tag-matched ping frame received. 1h [R] = A tag-matched ping frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset Source: fsi_rx_rst_mod_g_rst_n

Table 3-799. RX_EVT_STS_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	DATA_FRAME	R	0h	Data Frame Received Flag This bit indicates that an data frame has been received. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h [R] = No data frame has been received. 1h [R] = A data frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset Source: fsi_rx_rst_mod_g_rst_n
10	FRAME_OVERRUN	R	0h	Frame Overrun Flag This bit indicates that a frame overrun condition has occured. This bit gets set to 1 when a new DATA/ERROR frame is received and the corresponding DATA_FRAME_RCVD/ ERROR_FRAME_RCVD flag is still set to 1. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h [R] = Frame overrun has not ocurred. 1h [R] = Frame overrun has ocurred. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset Source: fsi_rx_rst_mod_g_rst_n
9	PING_FRAME	R	0h	Ping Frame Received Flag This bit indicates that an ping frame has been received. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h [R] = No ping frame has been received. 1h [R] = A ping frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset Source: fsi_rx_rst_mod_g_rst_n
8	ERR_FRAME	R	0h	Error Frame Received Flag This bit indicates that an error frame has been received. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h [R] = No error frame has been received. 1h [R] = An error frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset Source: fsi_rx_rst_mod_g_rst_n
7	BUF_UNDERRUN	R	0h	Receive Buffer Underrun Flag This bit indicates that a buffer underrun condition has occured in the receive buffer. This will happen when software reads the buffer which is empty and has no valid data. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h [R] = Receive Buffer Underrun has not ocurred. 1h [R] = Receive Buffer Underrun has ocurred. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset Source: fsi_rx_rst_mod_g_rst_n
6	FRAME_DONE	R	0h	Frame Done Flag This bit indicates that a frame has been successfully received without error. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h [R] = No frame has been successfully received. 1h [R] = A frame has been successfully received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset Source: fsi_rx_rst_mod_g_rst_n
5	BUF_OVERRUN	R	0h	Receive Buffer Overrun Flag This bit indicates that a buffer overrun condition has occured in the receive buffer. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h [R] = Receive buffer overrun has not ocurred. 1h [R] = Receive buffer overrun has ocurred. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset Source: fsi_rx_rst_mod_g_rst_n
4	EOF_ERR	R	0h	End-of-Frame Error Flag This bit indicates that an invalid end-of-frame bit pattern has been received. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h [R] = Invalid end-of-frame has not been received. 1h [R] = Invalid end-of-frame has been received To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset Source: fsi_rx_rst_mod_g_rst_n
3	TYPE_ERR	R	0h	Frame Type Error Flag This bit inditcates that an invalid frame type has been received. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h [R] = Invalid frame type has not been received. 1h [R] = Invalid frame type has been received To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset Source: fsi_rx_rst_mod_g_rst_n

Table 3-799. RX_EVT_STS_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CRC_ERR	R	0h	CRC Error Flag This bit indicates that a CRC error has occured. A CRC error will be generated on a data frame where the received CRC and the computed CRC do not match. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h [R] = CRC error has not occured. 1h [R] = CRC error has occured. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset Source: fsi_rx_rst_mod_g_rst_n
1	FRAME_WD_TO	R	0h	Frame Watchdog Timeout Flag This bit indicates that the frame watchdog timer has timed out. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h [R] = Frame watchdog timeout has not occured. 1h [R] = Frame watchdog timeout has occured. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset Source: fsi_rx_rst_mod_g_rst_n
0	PING_WD_TO	R	0h	Ping Watchdog Timeout Flag This bit indicates that the ping watchdog timer has timed out. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h [R] = Ping watchdog timeout has not occured. 1h [R] = Ping watchdog timeout has occured. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.7 MEM_RX_CRC_INFO Registers

3.11.7.1 MEM_CRC_INFO Register (Offset = 16h) [reset = 0h]

Short Description: Receive CRC info of recei

Long Description: Receive CRC info of received and computed CRC

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Table 3-800. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0016h
FSI_RX1	5029 1016h
FSI_RX2	502B 0016h
FSI_RX3	502B 1016h

Figure 3-344. RX_CRC_INFO Name Register

15	14	13	12	11	10	9	8
CALC_CRC							
R							
0h							
7	6	5	4	3	2	1	0
RX_CRC							
R							
0h							

Access Types Legend

Table 3-801. RX_CRC_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	CALC_CRC	R	0h	Harware Calculated CRC Value This bitfield contains the CRC value that was calculated on the last received data. The contents of this bitfield are valid only when data frames are received. Note: The contents of this bitfield are invalid for ping and error frames. Reset Source: fsi_rx_rst_mod_g_rst_n
7:0	RX_CRC	R	0h	Received CRC Value This bitfield contains the CRC value that was last received a frame. The contents of this bitfield are valid only when data frames are received. Note: The contents of this bitfield are invalid for ping and error frames. Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.8 MEM_RX_EVT_CLR_ALT1_ Registers

3.11.8.1 MEM_EVT_CLR_ALT1_ Register (Offset = 18h) [reset = 0h]

Short Description: Receive event and error c

Long Description: Receive event and error clear register

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Table 3-802. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0018h
FSI_RX1	5029 1018h
FSI_RX2	502B 0018h
FSI_RX3	502B 1018h

Figure 3-345. RX_EVT_CLR_ALT1_ Name Register

15	14	13	12	11	10	9	8
RESERVED_1	ERROR_TAG_MATCH	DATA_TAG_MATCH	PING_TAG_MATCH	DATA_FRAME	FRAME_OVERRUN	PING_FRAME	ERR_FRAME
R	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
BUF_UNDERRUN	FRAME_DONE	BUF_OVERRUN	EOF_ERR	TYPE_ERR	CRC_ERR	FRAME_WD_TO	PING_WD_TO
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 3-803. RX_EVT_CLR_ALT1_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved Reset Source: fsi_rx_rst_mod_g_rst_n
14	ERROR_TAG_MATCH	W	0h	Error Tag Match Glag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset Source: fsi_rx_rst_mod_g_rst_n
13	DATA_TAG_MATCH	W	0h	Data Tag Match Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset Source: fsi_rx_rst_mod_g_rst_n
12	PING_TAG_MATCH	W	0h	Ping Tag Match Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset Source: fsi_rx_rst_mod_g_rst_n
11	DATA_FRAME	W	0h	Data Frame Received Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset Source: fsi_rx_rst_mod_g_rst_n
10	FRAME_OVERRUN	W	0h	Frame Overrun Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset Source: fsi_rx_rst_mod_g_rst_n

Table 3-803. RX_EVT_CLR_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	PING_FRAME	W	0h	Ping Frame Received Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset Source: fsi_rx_rst_mod_g_rst_n
8	ERR_FRAME	W	0h	Error Frame Received Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset Source: fsi_rx_rst_mod_g_rst_n
7	BUF_UNDERRUN	W	0h	Receive Buffer Underrun Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h [R/W] = Writing a 0 to this bit will have no effect. 1h [R/W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset Source: fsi_rx_rst_mod_g_rst_n
6	FRAME_DONE	W	0h	Frame Done Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset Source: fsi_rx_rst_mod_g_rst_n
5	BUF_OVERRUN	W	0h	Receive Buffer Overrun Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset Source: fsi_rx_rst_mod_g_rst_n
4	EOF_ERR	W	0h	End-of-Frame Error Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset Source: fsi_rx_rst_mod_g_rst_n
3	TYPE_ERR	W	0h	Frame Type Error Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset Source: fsi_rx_rst_mod_g_rst_n
2	CRC_ERR	W	0h	CRC Error Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset Source: fsi_rx_rst_mod_g_rst_n
1	FRAME_WD_TO	W	0h	Frame Watchdog Timeout Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset Source: fsi_rx_rst_mod_g_rst_n
0	PING_WD_TO	W	0h	Ping Watchdog Timeout Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.9 MEM_RX_EVT_FRC_ALT1_ Registers

3.11.9.1 MEM_EVT_FRC_ALT1_ Register (Offset = 1Ah) [reset = 0h]

Short Description: Receive event and error f

Long Description: Receive event and error flag force register

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Table 3-804. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 001Ah
FSI_RX1	5029 101Ah
FSI_RX2	502B 001Ah
FSI_RX3	502B 101Ah

Figure 3-346. RX_EVT_FRC_ALT1_ Name Register

15	14	13	12	11	10	9	8
RESERVED_1	ERROR_TAG_MATCH	DATA_TAG_MATCH	PING_TAG_MATCH	DATA_FRAME	FRAME_OVERRUN	PING_FRAME	ERR_FRAME
R	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
BUF_UNDERRUN	FRAME_DONE	BUF_OVERRUN	EOF_ERR	TYPE_ERR	CRC_ERR	FRAME_WD_TO	PING_WD_TO
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 3-805. RX_EVT_FRC_ALT1_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved Reset Source: fsi_rx_rst_mod_g_rst_n
14	ERROR_TAG_MATCH	W	0h	Error Tag Match Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding bit in the RX_EVT_STS Register. Reset Source: fsi_rx_rst_mod_g_rst_n
13	DATA_TAG_MATCH	W	0h	Data Tag Match Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding bit in the RX_EVT_STS Register. Reset Source: fsi_rx_rst_mod_g_rst_n
12	PING_TAG_MATCH	W	0h	Ping Tag Match Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding bit in the RX_EVT_STS Register. Reset Source: fsi_rx_rst_mod_g_rst_n
11	DATA_FRAME	W	0h	Data Frame Received Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding bit in the RX_EVT_STS Register. Reset Source: fsi_rx_rst_mod_g_rst_n

Table 3-805. RX_EVT_FRC_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	FRAME_OVERRUN	W	0h	Frame Overrun Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding bit in the RX_EVT_STS Register. Reset Source: fsi_rx_rst_mod_g_rst_n
9	PING_FRAME	W	0h	Ping Frame Received Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding bit in the RX_EVT_STS Register. Reset Source: fsi_rx_rst_mod_g_rst_n
8	ERR_FRAME	W	0h	Error Frame Received Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding bit in the RX_EVT_STS Register. Reset Source: fsi_rx_rst_mod_g_rst_n
7	BUF_UNDERRUN	W	0h	Receive Buffer Underrun Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding bit in the RX_EVT_STS Register. Reset Source: fsi_rx_rst_mod_g_rst_n
6	FRAME_DONE	W	0h	Frame Done Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding bit in the RX_EVT_STS Register. Reset Source: fsi_rx_rst_mod_g_rst_n
5	BUF_OVERRUN	W	0h	Receive Buffer Overrun Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding bit in the RX_EVT_STS Register. Reset Source: fsi_rx_rst_mod_g_rst_n
4	EOF_ERR	W	0h	End-of-Frame Error Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding bit in the RX_EVT_STS Register. Reset Source: fsi_rx_rst_mod_g_rst_n
3	TYPE_ERR	W	0h	Frame Type Error Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding bit in the RX_EVT_STS Register. Reset Source: fsi_rx_rst_mod_g_rst_n
2	CRC_ERR	W	0h	CRC Error Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding bit in the RX_EVT_STS Register. Reset Source: fsi_rx_rst_mod_g_rst_n
1	FRAME_WD_TO	W	0h	Frame Watchdog Timeout Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding bit in the RX_EVT_STS Register. Reset Source: fsi_rx_rst_mod_g_rst_n

Table 3-805. RX_EVT_FRC_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PING_WD_TO	W	0h	Ping Watchdog Timeout Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding bit in the RX_EVT_STS Register. Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.10 MEM_RX_BUF_PTR_LOAD Registers

3.11.10.1 MEM_BUF_PTR_LOAD Register (Offset = 1Ch) [reset = 0h]

Short Description: Receive buffer pointer lo

Long Description: Receive buffer pointer load register

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Table 3-806. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 001Ch
FSI_RX1	5029 101Ch
FSI_RX2	502B 001Ch
FSI_RX3	502B 101Ch

Figure 3-347. RX_BUF_PTR_LOAD Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1				BUF_PTR_LOAD			
R				R/W			
0h				0h			

Access Types Legend

Table 3-807. RX_BUF_PTR_LOAD Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED_1	R	0h	Reserved Reset Source: fsi_rx_rst_mod_g_rst_n
3:0	BUF_PTR_LOAD	R/W	0h	Buffer Pointer Load. This is the value to be loaded into the receive word pointer when written. This is to allow software to force the receiver to start storing the received data starting at a specific location in the buffer. NOTE: The value of the CURR_BUF_PTR in the RX_BUF_PTR_STS will not get reflected immediately. This will take effect only when there is a valid receive operation with incoming clocks after [3 RXCLK + 3 SYCLK] cycles. Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.11 MEM_RX_BUF_PTR_STS Registers

3.11.11.1 MEM_BUF_PTR_STS Register (Offset = 1Eh) [reset = 0h]

Short Description: Receive buffer pointer st

Long Description: Receive buffer pointer status register

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Table 3-808. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 001Eh
FSI_RX1	5029 101Eh
FSI_RX2	502B 001Eh
FSI_RX3	502B 101Eh

Figure 3-348. RX_BUF_PTR_STS Name Register

15	14	13	12	11	10	9	8
RESERVED_2			CURR_WORD_CNT				
R			R				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED_1				CURR_BUF_PTR			
R				R			
0h				0h			

Access Types Legend

Table 3-809. RX_BUF_PTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_2	R	0h	Reserved Reset Source: fsi_rx_rst_mod_g_rst_n
12:8	CURR_WORD_CNT	R	0h	Words Available in the Receive Buffer This bitfield indicates the number of valid data words present in the receive buffer that have not been read by the application software. This bitfield is only valid when there is no active transfer. Note: This value will not be valid if there has been a buffer overrun or underrun condition. Reset Source: fsi_rx_rst_mod_g_rst_n
7:4	RESERVED_1	R	0h	Reserved Reset Source: fsi_rx_rst_mod_g_rst_n
3:0	CURR_BUF_PTR	R	0h	Current Buffer Pointer Index This bitfield will show the current index of the buffer pointer. This value is only valid when there is no active transmission. Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.12 MEM_RX_FRAME_WD_CTRL Registers

3.11.12.1 MEM_FRAME_WD_CTRL Register (Offset = 20h) [reset = 0h]

Short Description: Receive frame watchdog co

Long Description: Receive frame watchdog control register

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Table 3-810. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0020h
FSI_RX1	5029 1020h
FSI_RX2	502B 0020h
FSI_RX3	502B 1020h

Figure 3-349. RX_FRAME_WD_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1						FRAME_WD_EN	FRAME_WD_CNT_RST
R						R/W	R/W
0h						0h	0h

Access Types Legend

Table 3-811. RX_FRAME_WD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:2	RESERVED_1	R	0h	Reserved Reset Source: fsi_rx_rst_mod_g_rst_n
1	FRAME_WD_EN	R/W	0h	Frame Watchdog Counter Enable bit This bit will enable or disable the frame watchdog counter. The counter [RX_FRAME_WD_CNT] will begin counting from 0 when a valid start-of-frame pattern is received. When the reference value [RX_FRAME_WD_REF] is reached, it will generate a frame watchdog timeout event [RX_EVT_STS.FRAME_WD_TO] and the counter value will reset to 0 and continue counting on the next valid start-of-frame. 0h [R/W] = The frame watchdog counter is disabled and not running. 1h [R/W] = The frame watchdog counter logic is enabled and running. Reset Source: fsi_rx_rst_mod_g_rst_n
0	FRAME_WD_CNT_RST	R/W	0h	Frame Watchdog Counter Reset bit This bit will reset the frame watchdog counter to 0. Writing a 1 to this bit will reset the frame watchdog counter to 0. The counter will stay in reset as long as this bit is set to 1. This bit needs to be cleared to 0 to use the counter 0h [R/W] = Clear the FRAME_WD_CNT_RST. 1h [W] = The frame watchdog counter will be reset to 0. Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.13 MEM_RX_FRAME_WD_REF Registers

3.11.13.1 MEM_FRAME_WD_REF Register (Offset = 24h) [reset = 0h]

Short Description: Receive frame watchdog co

Long Description: Receive frame watchdog counter reference

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Table 3-812. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0024h
FSI_RX1	5029 1024h
FSI_RX2	502B 0024h
FSI_RX3	502B 1024h

Figure 3-350. RX_FRAME_WD_REF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FRAME_WD_REF															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRAME_WD_REF															
R/W															
0h															

Access Types Legend

Table 3-813. RX_FRAME_WD_REF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FRAME_WD_REF	R/W	0h	Frame Watchdog Counter Reference Value This is the 32-bit reference value for the frame watchdog timeout counter. The counter will count up starting from 0 at a valid start-of-frame pattern and continue counting until this value is reached. Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.14 MEM_RX_FRAME_WD_CNT Registers

3.11.14.1 MEM_FRAME_WD_CNT Register (Offset = 28h) [reset = 0h]

Short Description: Receive frame watchdog cu

Long Description: Receive frame watchdog current count

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Table 3-814. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0028h
FSI_RX1	5029 1028h
FSI_RX2	502B 0028h
FSI_RX3	502B 1028h

Figure 3-351. RX_FRAME_WD_CNT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FRAME_WD_CNT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRAME_WD_CNT															
R															
0h															

Access Types Legend

Table 3-815. RX_FRAME_WD_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FRAME_WD_CNT	R	0h	Frame Watchdog Counter Value This is the 32-bit read-only register which shows the current value of the frame watchdog counter. This counter is reset to 0 in a variety of ways: A write to FRME_WD_CNT_RST, a match with FRAME_WD_REF, or the reception of a successful data frame. Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.15 MEM_RX_PING_WD_CTRL Registers

3.11.15.1 MEM_PING_WD_CTRL Register (Offset = 2Ch) [reset = 0h]

Short Description: Receive ping watchdog con

Long Description: Receive ping watchdog control register

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Table 3-816. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 002Ch
FSI_RX1	5029 102Ch
FSI_RX2	502B 002Ch
FSI_RX3	502B 102Ch

Figure 3-352. RX_PING_WD_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1						PING_WD_EN	PING_WD_RST
R						R/W	R/W
0h						0h	0h

Access Types Legend

Table 3-817. RX_PING_WD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:2	RESERVED_1	R	0h	Reserved Reset Source: fsi_rx_rst_mod_g_rst_n
1	PING_WD_EN	R/W	0h	Ping Watchdog Counter Enable bit This bit will enable or disable the ping watchdog counter. The counter [RX_PING_WD_CNT] will begin counting from 0 when it is enabled. When the reference value [RX_PING_WD_REF] is reached, it will generate a ping watchdog timeout event [RX_EVT_STS.PING_WD_TO] and the counter value will reset to 0, and resume counting 0h [R/W] = The ping watchdog counter is disabled and not running. 1h [R/W] = The ping watchdog counter logic is enabled and running. Reset Source: fsi_rx_rst_mod_g_rst_n
0	PING_WD_RST	R/W	0h	Ping Watchdog Counter Reset bit This bit will reset the ping watchdog counter to 0. Writing a 1 to this bit will reset the ping watchdog counter to 0. The counter will stay in reset as long as this bit is set to 1. This bit needs to be cleared to 0 to use the counter 0h [R/W] = Clear the PING_WD_RST. 1h [W] = The ping watchdog counter will be reset to 0. Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.16 MEM_RX_PING_TAG Registers

3.11.16.1 MEM_PING_TAG Register (Offset = 2Eh) [reset = 0h]

Short Description: Receive ping tag register

Long Description: Receive ping tag register

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Table 3-818. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 002Eh
FSI_RX1	5029 102Eh
FSI_RX2	502B 002Eh
FSI_RX3	502B 102Eh

Figure 3-353. RX_PING_TAG Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1			PING_TAG				ZERO
R			R				R
0h			0h				0h

Access Types Legend

Table 3-819. RX_PING_TAG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:5	RESERVED_1	R	0h	Reserved Reset Source: fsi_rx_rst_mod_g_rst_n
4:1	PING_TAG	R	0h	Received Ping Frame Tag This field contains the 4-bit frame tag from the last successfully received ping frame. This is intentionally shifted into bits 4:1 so that the register can be used as a 32-bit address index based on the received tag. Reset Source: fsi_rx_rst_mod_g_rst_n
0	ZERO	R	0h	Zero bit This bit will always read as 0. This is intentionally provided to create a 32-bit offset if required. Using the PING_TAG and ZERO bits of this register [bits 4:0], application software can directly index into an array of 32-bit data. Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.17 MEM_RX_PING_WD_REF Registers

3.11.17.1 MEM_PING_WD_REF Register (Offset = 30h) [reset = 0h]

Short Description: Receive ping watchdog cou

Long Description: Receive ping watchdog counter reference

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Table 3-820. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0030h
FSI_RX1	5029 1030h
FSI_RX2	502B 0030h
FSI_RX3	502B 1030h

Figure 3-354. RX_PING_WD_REF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PING_WD_REF															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PING_WD_REF															
R/W															
0h															

Access Types Legend

Table 3-821. RX_PING_WD_REF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PING_WD_REF	R/W	0h	Ping Watchdog Counter Reference Value This is the 32-bit reference value for the ping watchdog timeout counter. The counter will count up starting from 0 and continue counting until this value is reached. Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.18 MEM_RX_PING_WD_CNT Registers

3.11.18.1 MEM_PING_WD_CNT Register (Offset = 34h) [reset = 0h]

Short Description: Receive pingwatchdog curr

Long Description: Receive pingwatchdog current count

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Table 3-822. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0034h
FSI_RX1	5029 1034h
FSI_RX2	502B 0034h
FSI_RX3	502B 1034h

Figure 3-355. RX_PING_WD_CNT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PING_WD_CNT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PING_WD_CNT															
R															
0h															

Access Types Legend

Table 3-823. RX_PING_WD_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PING_WD_CNT	R	0h	Ping Watchdog Counter Value This is the 32-bit read-only register which shows the current value of the ping watchdog counter. This counter is reset to 0 in a variety of ways: A write to PING_WD_RST, a match with PING_WD_REF, or the reception of a ping frame. Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.19 MEM_RX_INT1_CTRL_ALT1_ Registers

3.11.19.1 MEM_INT1_CTRL_ALT1_ Register (Offset = 38h) [reset = 0h]

Short Description: Receive interrupt control

Long Description: Receive interrupt control register for RX_INT1

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Table 3-824. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0038h
FSI_RX1	5029 1038h
FSI_RX2	502B 0038h
FSI_RX3	502B 1038h

Figure 3-356. RX_INT1_CTRL_ALT1_ Name Register

15	14	13	12	11	10	9	8
RESERVED_1	INT1_EN_ERROR_TAG_MATCH	INT1_EN_DATA_TAG_MATCH	INT1_EN_PING_TAG_MATCH	INT1_EN_DATA_FRAME	INT1_EN_FRAME_OVERRUN	INT1_EN_PING_FRAME	INT1_EN_ERR_FRAME
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
INT1_EN_UNDERRUN	INT1_EN_FRAME_DONE	INT1_EN_OVERRUN	INT1_EN_EOF_ERR	INT1_EN_TYPE_ERR	INT1_EN_CRC_ERR	INT1_EN_FRAME_WD_TO	INT1_EN_PING_WD_TO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 3-825. RX_INT1_CTRL_ALT1_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved Reset Source: fsi_rx_rst_mod_g_rst_n
14	INT1_EN_ERROR_TAG_MATCH	R/W	0h	Enable Error Frame Received with Tag Match Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT1. 1h [R/W] = An error frame received with matching tag will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: fsi_rx_rst_mod_g_rst_n
13	INT1_EN_DATA_TAG_MATCH	R/W	0h	Enable Data Frame Received with Tag Match Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT1. 1h [R/W] = A data frame received with matching tag will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: fsi_rx_rst_mod_g_rst_n
12	INT1_EN_PING_TAG_MATCH	R/W	0h	Enable Ping Frame Received with Tag Match Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT1. 1h [R/W] = A ping frame received with matching tag will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: fsi_rx_rst_mod_g_rst_n

Table 3-825. RX_INT1_CTRL_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	INT1_EN_DATA_FRAME	R/W	0h	Enable Data Frame Received Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT1. 1h [R/W] = A data frame received event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: fsi_rx_rst_mod_g_rst_n
10	INT1_EN_FRAME_OVERRUN	R/W	0h	Enable Frame Overrun Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT1. 1h [R/W] = A frame overrun event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: fsi_rx_rst_mod_g_rst_n
9	INT1_EN_PING_FRAME	R/W	0h	Enable Ping Frame Received Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT1. 1h [R/W] = A ping frame received event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: fsi_rx_rst_mod_g_rst_n
8	INT1_EN_ERR_FRAME	R/W	0h	Enable ERROR Frame Received Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT1. 1h [R/W] = A error frame received event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: fsi_rx_rst_mod_g_rst_n
7	INT1_EN_UNDERRUN	R/W	0h	Enable Buffer Underrun Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT1. 1h [R/W] = A buffer underrun event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: fsi_rx_rst_mod_g_rst_n
6	INT1_EN_FRAME_DONE	R/W	0h	Enable Frame Done Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT1. 1h [R/W] = A frame done event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: fsi_rx_rst_mod_g_rst_n
5	INT1_EN_OVERRUN	R/W	0h	Enable Receive Buffer Overrun Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT1. 1h [R/W] = A receive buffer overrun event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: fsi_rx_rst_mod_g_rst_n
4	INT1_EN_EOF_ERR	R/W	0h	Enable End-of-Frame Error Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT1. 1h [R/W] = An end-of-frame error event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: fsi_rx_rst_mod_g_rst_n
3	INT1_EN_TYPE_ERR	R/W	0h	Enable Frame Type Error Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT1. 1h [R/W] = A frame type error event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: fsi_rx_rst_mod_g_rst_n

Table 3-825. RX_INT1_CTRL_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	INT1_EN_CRC_ERR	R/W	0h	Enable CRC Error Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT1. 1h [R/W] = A CRC error will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: fsi_rx_rst_mod_g_rst_n
1	INT1_EN_FRAME_WD_TO	R/W	0h	Enable Frame Watchdog Timeout Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT1. 1h [R/W] = A frame watchdog timeout event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: fsi_rx_rst_mod_g_rst_n
0	INT1_EN_PING_WD_TO	R/W	0h	Enable Ping Watchdog Timeout Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT1. 1h [R/W] = A ping watchdog timeout event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.20 MEM_RX_INT2_CTRL_ALT1_ Registers

3.11.20.1 MEM_INT2_CTRL_ALT1_ Register (Offset = 3Ah) [reset = 0h]

Short Description: Receive interrupt control

Long Description: Receive interrupt control register for RX_INT2

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Table 3-826. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 003Ah
FSI_RX1	5029 103Ah
FSI_RX2	502B 003Ah
FSI_RX3	502B 103Ah

Figure 3-357. RX_INT2_CTRL_ALT1_ Name Register

15	14	13	12	11	10	9	8
RESERVED_1	INT2_EN_ERROR_TAG_MATCH	INT2_EN_DATA_TAG_MATCH	INT2_EN_PING_TAG_MATCH	INT2_EN_DATA_FRAME	INT2_EN_FRAME_OVERRUN	INT2_EN_PING_FRAME	INT2_EN_ERR_FRAME
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
INT2_EN_UNDERRUN	INT2_EN_FRAME_DONE	INT2_EN_OVERRUN	INT2_EN_EOF_ERR	INT2_EN_TYPE_ERR	INT2_EN_CRC_ERR	INT2_EN_FRAME_WD_TO	INT2_EN_PING_WD_TO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 3-827. RX_INT2_CTRL_ALT1_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved Reset Source: fsi_rx_rst_mod_g_rst_n
14	INT2_EN_ERROR_TAG_MATCH	R/W	0h	Enable Error Frame Received with Tag Match Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT2. 1h [R/W] = An error frame received with matching tag will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: fsi_rx_rst_mod_g_rst_n
13	INT2_EN_DATA_TAG_MATCH	R/W	0h	Enable Data Frame Received with Tag Match Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT2. 1h [R/W] = A data frame received with matching tag will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: fsi_rx_rst_mod_g_rst_n
12	INT2_EN_PING_TAG_MATCH	R/W	0h	Enable Ping Frame Received with Tag Match Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT2. 1h [R/W] = A ping frame received with matching tag will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: fsi_rx_rst_mod_g_rst_n

Table 3-827. RX_INT2_CTRL_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	INT2_EN_DATA_FRAME	R/W	0h	Enable Data Frame Received Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT2. 1h [R/W] = A data frame received event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: fsi_rx_rst_mod_g_rst_n
10	INT2_EN_FRAME_OVERRUN	R/W	0h	Enable Frame Overrun Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT2. 1h [R/W] = A frame overrun event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: fsi_rx_rst_mod_g_rst_n
9	INT2_EN_PING_FRAME	R/W	0h	Enable Ping Frame Received Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT2. 1h [R/W] = A ping frame received event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: fsi_rx_rst_mod_g_rst_n
8	INT2_EN_ERR_FRAME	R/W	0h	Enable Error Frame Received Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT2. 1h [R/W] = A error frame received event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: fsi_rx_rst_mod_g_rst_n
7	INT2_EN_UNDERRUN	R/W	0h	Enable Buffer Underrun Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT2. 1h [R/W] = A buffer underrun event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: fsi_rx_rst_mod_g_rst_n
6	INT2_EN_FRAME_DONE	R/W	0h	Enable Frame Done Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT2. 1h [R/W] = A frame done event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: fsi_rx_rst_mod_g_rst_n
5	INT2_EN_OVERRUN	R/W	0h	Enable Buffer Overrun Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT2. 1h [R/W] = A buffer overrun event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: fsi_rx_rst_mod_g_rst_n
4	INT2_EN_EOF_ERR	R/W	0h	Enable End-of-Frame Error Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT2. 1h [R/W] = An end-of-frame error event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: fsi_rx_rst_mod_g_rst_n
3	INT2_EN_TYPE_ERR	R/W	0h	Enable Frame Type Error Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT2. 1h [R/W] = A frame type error event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: fsi_rx_rst_mod_g_rst_n

Table 3-827. RX_INT2_CTRL_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	INT2_EN_CRC_ERR	R/W	0h	Enable CRC Error Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT2. 1h [R/W] = A CRC error will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: fsi_rx_rst_mod_g_rst_n
1	INT2_EN_FRAME_WD_TO	R/W	0h	Enable Frame Watchdog Timeout Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT2. 1h [R/W] = A frame watchdog timeout event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: fsi_rx_rst_mod_g_rst_n
0	INT2_EN_PING_WD_TO	R/W	0h	Enable Ping Watchdog Timeout Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h [R/W] = This event will not trigger an interrupt on RX_INT2. 1h [R/W] = A ping watchdog timeout event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.21 MEM_RX_LOCK_CTRL Registers

3.11.21.1 MEM_LOCK_CTRL Register (Offset = 3Ch) [reset = 0h]

Short Description: Receive lock control regi

Long Description: Receive lock control register

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Table 3-828. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 003Ch
FSI_RX1	5029 103Ch
FSI_RX2	502B 003Ch
FSI_RX3	502B 103Ch

Figure 3-358. RX_LOCK_CTRL Name Register

15	14	13	12	11	10	9	8
KEY							
W							
0h							
7	6	5	4	3	2	1	0
RESERVED_1							LOCK
R							R/W
0h							0h

Access Types Legend

Table 3-829. RX_LOCK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	KEY	W	0h	Write Key. In order to write to this register, 0xA5 must be written to this field at the same time. Otherwise, writes are ignored. The key is cleared immediately after writing, so it must be written again for every change to this register. Reset Source: fsi_rx_rst_mod_g_rst_n
7:1	RESERVED_1	R	0h	Reserved Reset Source: fsi_rx_rst_mod_g_rst_n
0	LOCK	R/W	0h	Control Register Lock Enable bit This bit locks the contents of all the receive control registers that support a lock protection. Once locked, further writes will not take effect until SYSRS unlocks the register. Once set, further writes even to this bit will be ignored. 0h [R/W] = Receive control registers can be modified and are not locked. 1h [R/W] = Receive control registers are locked and cannot be modified until this bit is cleared by SYSRS. Any further writes to this bit are ignored. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect. Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.22 MEM_RX_ECC_DATA Registers

3.11.22.1 MEM_ECC_DATA Register (Offset = 40h) [reset = 0h]

Short Description: Receive ECC data register

Long Description: Receive ECC data register

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Table 3-830. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0040h
FSI_RX1	5029 1040h
FSI_RX2	502B 0040h
FSI_RX3	502B 1040h

Figure 3-359. RX_ECC_DATA Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA_HIGH															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA_LOW															
R/W															
0h															

Access Types Legend

Table 3-831. RX_ECC_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DATA_HIGH	R/W	0h	Upper 16 bits of ECC Data Writing to this bitfield will cause the ECC logic to compute the ECC[SEC-DED] the entire 32-bit register and update TX_ECC_VAL register with the results. Software should write to these 16 bits of the register in a 32-bit write when needing to compute ECC for 32-bits for the full TX_ECC_DATA register. Reset Source: fsi_rx_rst_mod_g_rst_n
15:0	DATA_LOW	R/W	0h	Lower 16 bits of ECC Data Writing to this bitfield will cause the ECC logic to compute the ECC[SEC-DED] for these 16 bits and update the TX_ECC_VAL register with the results. Software should write to these register bits as a 16-bit write when needing to compute ECC for 16-bits. Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.23 MEM_RX_ECC_VAL Registers

3.11.23.1 MEM_ECC_VAL Register (Offset = 44h) [reset = 0h]

Short Description: Receive ECC value registe

Long Description: Receive ECC value register

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Table 3-832. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0044h
FSI_RX1	5029 1044h
FSI_RX2	502B 0044h
FSI_RX3	502B 1044h

Figure 3-360. RX_ECC_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1	ECC_VAL						
R	R/W						
0h	0h						

Access Types Legend

Table 3-833. RX_ECC_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:7	RESERVED_1	R	0h	Reserved Reset Source: fsi_rx_rst_mod_g_rst_n
6:0	ECC_VAL	R/W	0h	ECC Value for SEC-DED check This field contains the ECC value to be used for SEC-DED either for 16-bit or 32-bit data in the RX_ECC_DATA register. Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.24 MEM_RX_ECC_SEC_DATA Registers

3.11.24.1 MEM_ECC_SEC_DATA Register (Offset = 48h) [reset = 0h]

Short Description: Receive ECC corrected dat

Long Description: Receive ECC corrected data register

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Table 3-834. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0048h
FSI_RX1	5029 1048h
FSI_RX2	502B 0048h
FSI_RX3	502B 1048h

Figure 3-361. RX_ECC_SEC_DATA Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEC_DATA															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEC_DATA															
R															
0h															

Access Types Legend

Table 3-835. RX_ECC_SEC_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SEC_DATA	R	0h	ECC Single Error Corrected Data The ECC corrected data will be available in this register. This value is valid only when there are no bit errors, or a single bit error was detected. Otherwise, the contents of this register are invalid and should not be used. Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.25 MEM_RX_ECC_LOG Registers

3.11.25.1 MEM_ECC_LOG Register (Offset = 4Ch) [reset = 3h]

Short Description: Receive ECC log and statu

Long Description: Receive ECC log and status register

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Table 3-836. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 004Ch
FSI_RX1	5029 104Ch
FSI_RX2	502B 004Ch
FSI_RX3	502B 104Ch

Figure 3-362. RX_ECC_LOG Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1						MBE	SBE
R						R	R
0h						1h	1h

Access Types Legend

Table 3-837. RX_ECC_LOG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:2	RESERVED_1	R	0h	Reserved Reset Source: fsi_rx_rst_mod_g_rst_n
1	MBE	R	1h	Multiple Bit Errors Detected This bit indicates the occurrence of multiple bit errors.The data is corrupted and cannot be corrected. If this bit is set, the data present in RX_ECC_SEC_DATA is invalid and should not be used. 0h [R] Multiple Bit Errors were not detected. Check the SBE bit for single bit errors. 1h [R] Multiple Bit Errors were detected. The data is not able to be corrected. The value present in RX_ECC_SEC_DATA is invalid and should not be used. Reset Source: fsi_rx_rst_mod_g_rst_n
0	SBE	R	1h	Single Bit Error Detected This bit indicates the occurrence of a single bit error in the data. The data is autocorrected and placed into the RX_ECC_SEC_DATA register. This bit is valid only if MBE is 0. 0h [R] No bit errors were detected. The value in RX_ECC_SEC_DATA is correct. 1h [R] A single bit error was detected and corrected. The corrected data is present in RX_ECC_SEC_DATA. Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.26 MEM_RX_FRAME_TAG_CMP Registers

3.11.26.1 MEM_FRAME_TAG_CMP Register (Offset = 50h) [reset = 0h]

Short Description: Receive frame tag compare

Long Description: Receive frame tag compare register

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Table 3-838. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0050h
FSI_RX1	5029 1050h
FSI_RX2	502B 0050h
FSI_RX3	502B 1050h

Figure 3-363. RX_FRAME_TAG_CMP Name Register

15	14	13	12	11	10	9	8
RESERVED_1						BROADCAST_EN	CMP_EN
R						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
TAG_MASK				TAG_REF			
R/W				R/W			
0h				0h			

Access Types Legend

Table 3-839. RX_FRAME_TAG_CMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved Reset Source: fsi_rx_rst_mod_g_rst_n
9	BROADCAST_EN	R/W	0h	Broadcast Enable bit This will enable the reception of a ping frame broadcast. When this bit is set, bit 3 of the received tag will be treated as a broadcast notification. If bit 3 of the received tag is set to 1, a ping tag match event will be triggered regardless of the. A match caused by the comparison of TAG_MASK and TAG_REF will still be considered a match and the frame tag match event will be triggered as normal This bit only takes effect only if CMP_EN is set to 1. 0h [R/W] Broadcast frame match disabled. 1h [R/W] Broadcast frame match enabled. Reset Source: fsi_rx_rst_mod_g_rst_n
8	CMP_EN	R/W	0h	Frame Tag Compare Enable bit Set this bit to enable the comparison of an incoming frame tag and the value stored in the frame tag reference. A match caused by the comparison of TAG_MASK, TAG_REF, and the incoming frame tag will trigger the apprpriate frame tag match event. 0h [R/W] Frame tag comparison is disabled. 1h [R/W] Frame tag comparison is enabled. Reset Source: fsi_rx_rst_mod_g_rst_n
7:4	TAG_MASK	R/W	0h	Frame Tag Mask Any bit position in this register set to 0 will be used in the comparison of the incoming frame tag and the value stored in TAG_REF. A bit position set to 1 will be ignored in the tag comparison. This mask value is used only for non-ping frames. Reset Source: fsi_rx_rst_mod_g_rst_n
3:0	TAG_REF	R/W	0h	Frame Tag Reference The reference tag to check against when comparing the TAG_MASK and the incoming frame tag. This reference value is used only for non-ping frames. Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.27 MEM_RX_PING_TAG_CMP Registers

3.11.27.1 MEM_PING_TAG_CMP Register (Offset = 52h) [reset = 0h]

Short Description: Receive ping tag compare

Long Description: Receive ping tag compare register

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Table 3-840. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0052h
FSI_RX1	5029 1052h
FSI_RX2	502B 0052h
FSI_RX3	502B 1052h

Figure 3-364. RX_PING_TAG_CMP Name Register

15	14	13	12	11	10	9	8
RESERVED_1						BROADCAST_EN	CMP_EN
R						R/W	R/W
0h						0h	0h
7	6	5	4	3	2	1	0
TAG_MASK				TAG_REF			
R/W				R/W			
0h				0h			

Access Types Legend

Table 3-841. RX_PING_TAG_CMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved Reset Source: fsi_rx_rst_mod_g_rst_n
9	BROADCAST_EN	R/W	0h	Broadcast Enable bit This will enable the reception of a ping frame broadcast. When this bit is set, bit 3 of the received tag will be treated as a broadcast notification. If bit 3 of the received tag is set to 1, a ping tag match event will be triggered regardless of the. A match caused by the comparison of TAG_MASK and TAG_REF will still be considered a match and the ping tag match event will be triggered as normal This bit only takes effect only if CMP_EN is set to 1. 0h [R/W] Broadcast frame match disabled. 1h [R/W] Broadcast frame match enabled. Reset Source: fsi_rx_rst_mod_g_rst_n
8	CMP_EN	R/W	0h	Ping Tag Compare Enable bit Set this bit to enable the comparison of an incoming ping tag and the value stored in the ping tag reference. A match caused by the comparison of TAG_MASK, TAG_REF, and the incoming ping tag will trigger a ping frame tag match event. 0h [R/W] Ping tag comparison is disabled. 1h [R/W] Ping tag comparison is enabled. Reset Source: fsi_rx_rst_mod_g_rst_n
7:4	TAG_MASK	R/W	0h	Ping Tag Mask Any bit position in this register set to 0 will be used in the comparison of the incoming ping frame tag and the value stored in TAG_REF. A bit position set to 1 will be ignored in the tag comparison. This mask value is used only for ping frames. Reset Source: fsi_rx_rst_mod_g_rst_n
3:0	TAG_REF	R/W	0h	Ping Tag Reference The reference tag to check against when comparing the TAG_MASK and the incoming ping tag. This reference value is used only for ping frames. Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.28 MEM_RX_TRIG_CTRL_0 Registers

3.11.28.1 MEM_TRIG_CTRL_0 Register (Offset = 58h) [reset = 0h]

Short Description: Receive Trigger Control r

Long Description: Receive Trigger Control register 0

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Table 3-842. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0058h
FSI_RX1	5029 1058h
FSI_RX2	502B 0058h
FSI_RX3	502B 1058h

Figure 3-365. RX_TRIG_CTRL_0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RX_TRIG_DLY															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_TRIG_DLY								RESERVED_1			TRIG_SEL				TRIG_EN
R/W								R			R/W				R/W
0h								0h			0h				0h

Access Types Legend

Table 3-843. RX_TRIG_CTRL_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RX_TRIG_DLY	R/W	0h	This is the 24 bit count of the trigger delay in SYSCLK cycles. If enabled, the Trigger-1 output of the trigger module will generate a 3 SYSCLK wide trigger pulse after the selected input trigger source sees a rising edge with a delay defined by this 24-bt value. Reset Source: fsi_rx_rst_mod_g_rst_n
7:5	RESERVED_1	R	0h	Reserved Reset Source: fsi_rx_rst_mod_g_rst_n
4:1	TRIG_SEL	R/W	0h	This is the mux select value which selects which of the inputs will be used as the trigger source. Reset Source: fsi_rx_rst_mod_g_rst_n
0	TRIG_EN	R/W	0h	This is the enable for the RX output trigger generation. The output triggers will be generated only if this bit is set to 1. If this bit is 0, then no trigger will be generated by this module. Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.29 MEM_RX_TRIG_WIDTH_0 Registers

3.11.29.1 MEM_TRIG_WIDTH_0 Register (Offset = 5Ch) [reset = 0h]

Short Description: Receive Trigger Wdith reg

Long Description: Receive Trigger Wdith register 0

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Table 3-844. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 005Ch
FSI_RX1	5029 105Ch
FSI_RX2	502B 005Ch
FSI_RX3	502B 105Ch

Figure 3-366. RX_TRIG_WIDTH_0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_TRIG_WIDTH															
R/W															
0h															

Access Types Legend

Table 3-845. RX_TRIG_WIDTH_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_1	R	0h	Reserved Reset Source: fsi_rx_rst_mod_g_rst_n
15:0	RX_TRIG_WIDTH	R/W	0h	This register decides the width[in SYSCLK cycles] of wide pulse output of the RX trigger module. Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.30 MEM_RX_DLYLINE_CTRL Registers

3.11.30.1 MEM_DLYLINE_CTRL Register (Offset = 60h) [reset = 0h]

Short Description: Receive delay line contro

Long Description: Receive delay line control register

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Table 3-846. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0060h
FSI_RX1	5029 1060h
FSI_RX2	502B 0060h
FSI_RX3	502B 1060h

Figure 3-367. RX_DLYLINE_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED_1	RXD1_DLY					RXD0_DLY	
R	R/W					R/W	
0h	0h					0h	
7	6	5	4	3	2	1	0
RXD0_DLY				RXCLK_DLY			
R/W				R/W			
0h				0h			

Access Types Legend

Table 3-847. RX_DLYLINE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved Reset Source: fsi_rx_rst_mod_g_rst_n
14:10	RXD1_DLY	R/W	0h	Delay Line Tap Select for RXD1 This bitfield selects the number of delay elements inserted into the RXD1 path from the pin boundary to the receiver core. 0h [R/W] Zero delay elements are included in the RXD1 path. RXD1 is taken directly from the pin. 1h [R/W] One delay element is included in the RXD1 path. 2h [R/W] Two delay elements are included in the RXD1 path. ... 1Fh [R/W] 31 delay elements are included in the RXD1 path, the maximum. Reset Source: fsi_rx_rst_mod_g_rst_n
9:5	RXD0_DLY	R/W	0h	Delay Line Tap Select for RXD0 This bitfield selects the number of delay elements inserted into the RXD0 path from the pin boundary to the receiver core. 0h [R/W] Zero delay elements are included in the RXD0 path. RXD0 is taken directly from the pin. 1h [R/W] One delay element is included in the RXD0 path. 2h [R/W] Two delay elements are included in the RXD0 path. ... 1Fh [R/W] 31 delay elements are included in the RXD0 path, the maximum. Reset Source: fsi_rx_rst_mod_g_rst_n
4:0	RXCLK_DLY	R/W	0h	Delay Line Tap Select for RXCLK This bitfield selects the number of delay elements inserted into the RXCLK path from the pin boundary to the receiver core. 0h [R/W] Zero delay elements are included in the RXCLK path. RXCLK is taken directly from the pin. 1h [R/W] One delay element is included in the RXCLK path. 2h [R/W] Two delay elements are included in the RXCLK path. ... 1Fh [R/W] 31 delay elements are included in the RXCLK path, the maximum. Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.31 MEM_RX_TRIG_CTRL_1 Registers

3.11.31.1 MEM_TRIG_CTRL_1 Register (Offset = 64h) [reset = 0h]

Short Description: Receive Trigger Control r

Long Description: Receive Trigger Control register 1

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Table 3-848. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0064h
FSI_RX1	5029 1064h
FSI_RX2	502B 0064h
FSI_RX3	502B 1064h

Figure 3-368. RX_TRIG_CTRL_1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RX_TRIG_DLY															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_TRIG_DLY								RESERVED_1			TRIG_SEL				TRIG_EN
R/W								R			R/W				R/W
0h								0h			0h				0h

Access Types Legend

Table 3-849. RX_TRIG_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RX_TRIG_DLY	R/W	0h	This is the 24 bit count of the trigger delay in SYSCLK cycles. If enabled, the Trigger-1 output of the trigger module will generate a 3 SYSCLK wide trigger pulse after the selected input trigger source sees a rising edge with a delay defined by this 24-bt value. Reset Source: fsi_rx_rst_mod_g_rst_n
7:5	RESERVED_1	R	0h	Reserved Reset Source: fsi_rx_rst_mod_g_rst_n
4:1	TRIG_SEL	R/W	0h	This is the mux select value which selects which of the inputs will be used as the trigger source. Reset Source: fsi_rx_rst_mod_g_rst_n
0	TRIG_EN	R/W	0h	This is the enable for the RX output trigger generation. The output triggers will be generated only if this bit is set to 1. If this bit is 0, then no trigger will be generated by this module. Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.32 MEM_RX_TRIG_CTRL_2 Registers

3.11.32.1 MEM_TRIG_CTRL_2 Register (Offset = 68h) [reset = 0h]

Short Description: Receive Trigger Control r

Long Description: Receive Trigger Control register 2

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Table 3-850. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0068h
FSI_RX1	5029 1068h
FSI_RX2	502B 0068h
FSI_RX3	502B 1068h

Figure 3-369. RX_TRIG_CTRL_2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RX_TRIG_DLY															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_TRIG_DLY								RESERVED_1			TRIG_SEL				TRIG_EN
R/W								R			R/W				R/W
0h								0h			0h				0h

Access Types Legend

Table 3-851. RX_TRIG_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RX_TRIG_DLY	R/W	0h	This is the 24 bit count of the trigger delay in SYSCLK cycles. If enabled, the Trigger-1 output of the trigger module will generate a 3 SYSCLK wide trigger pulse after the selected input trigger source sees a rising edge with a delay defined by this 24-bt value. Reset Source: fsi_rx_rst_mod_g_rst_n
7:5	RESERVED_1	R	0h	Reserved Reset Source: fsi_rx_rst_mod_g_rst_n
4:1	TRIG_SEL	R/W	0h	This is the mux select value which selects which of the inputs will be used as the trigger source. Reset Source: fsi_rx_rst_mod_g_rst_n
0	TRIG_EN	R/W	0h	This is the enable for the RX output trigger generation. The output triggers will be generated only if this bit is set to 1. If this bit is 0, then no trigger will be generated by this module. Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.33 MEM_RX_TRIG_CTRL_3 Registers

3.11.33.1 MEM_TRIG_CTRL_3 Register (Offset = 6Ch) [reset = 0h]

Short Description: Receive Trigger Control r

Long Description: Receive Trigger Control register 3

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Table 3-852. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 006Ch
FSI_RX1	5029 106Ch
FSI_RX2	502B 006Ch
FSI_RX3	502B 106Ch

Figure 3-370. RX_TRIG_CTRL_3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RX_TRIG_DLY															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_TRIG_DLY								RESERVED_1			TRIG_SEL				TRIG_EN
R/W								R			R/W				R/W
0h								0h			0h				0h

Access Types Legend

Table 3-853. RX_TRIG_CTRL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RX_TRIG_DLY	R/W	0h	This is the 24 bit count of the trigger delay in SYSCLK cycles. If enabled, the Trigger-1 output of the trigger module will generate a 3 SYSCLK wide trigger pulse after the selected input trigger source sees a rising edge with a delay defined by this 24-bt value. Reset Source: fsi_rx_rst_mod_g_rst_n
7:5	RESERVED_1	R	0h	Reserved Reset Source: fsi_rx_rst_mod_g_rst_n
4:1	TRIG_SEL	R/W	0h	This is the mux select value which selects which of the inputs will be used as the trigger source. Reset Source: fsi_rx_rst_mod_g_rst_n
0	TRIG_EN	R/W	0h	This is the enable for the RX output trigger generation. The output triggers will be generated only if this bit is set to 1. If this bit is 0, then no trigger will be generated by this module. Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.34 MEM_RX_VIS_1 Registers

3.11.34.1 MEM_VIS_1 Register (Offset = 70h) [reset = 0h]

Short Description: Receive debug visibility

Long Description: Receive debug visibility register 1

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Table 3-854. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0070h
FSI_RX1	5029 1070h
FSI_RX2	502B 0070h
FSI_RX3	502B 1070h

Figure 3-371. RX_VIS_1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_2															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2												RX_CORE_STS	RESERVED_1		
R												R	R		
0h												0h	0h		

Access Types Legend

Table 3-855. RX_VIS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_2	R	0h	Reserved Reset Source: fsi_rx_rst_mod_g_rst_n
3	RX_CORE_STS	R	0h	Receiver Core Status bit This bit indicates the status of the receiver core. If this bit is set, the receiver should undergo a reset and subsequent resynchronization with the transmitter. This bit will be always be set when the receiver has detected and end of frame error or a frame type error. This bit can also be set if the receiver becomes corrupted due to noise on the signal lines. If the receiver has experienced a ping watchdog or frame watchdog timeout, this bit should be read to determine if the cause was due to a corrupt transaction, thus putting the receiver core into an unrecoverable state. Only a soft reset will reset the recevier core and thus reset this bit. 0h [R] The receiver core is operating normally. 1h [R] The receiver core has entered into an error state and should be reset. Reset Source: fsi_rx_rst_mod_g_rst_n
2:0	RESERVED_1	R	0h	Reserved Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.35 MEM_RX_UDATA_FILTER Registers

3.11.35.1 MEM_UDATA_FILTER Register (Offset = 74h) [reset = 0h]

Short Description: Receive User Data Filter

Long Description: Receive User Data Filter Control register

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Table 3-856. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0074h
FSI_RX1	5029 1074h
FSI_RX2	502B 0074h
FSI_RX3	502B 1074h

Figure 3-372. RX_UDATA_FILTER Name Register

15	14	13	12	11	10	9	8
UDATA_MASK							
R/W							
0h							
7	6	5	4	3	2	1	0
UDATA_REG							
R/W							
0h							

Access Types Legend

Table 3-857. RX_UDATA_FILTER Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	UDATA_MASK	R/W	0h	Bit Mask to be used for comparing the USERDATA field when filtering is enabled. Every bit that is '1' in this register will be masked for comparison. If a bit position is '1', then it will be considered a successful match for that bit position. Reset Source: fsi_rx_rst_mod_g_rst_n
7:0	UDATA_REG	R/W	0h	Reference to be used for comparing the USERDATA field when filtering is enabled. Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.36 MEM_RX_BUF_BASE_N Registers

3.11.36.1 MEM_BUF_BASE_N Register (Offset = 80h) [reset = 0h]

Short Description: Base address for receive

Long Description: Base address for receive data buffer

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Offset = 80h + (j * 2h); where j = 0h to Fh

Table 3-858. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0080h
FSI_RX1	5029 1080h
FSI_RX2	502B 0080h
FSI_RX3	502B 1080h

Figure 3-373. RX_BUF_BASE_N Name Register

15	14	13	12	11	10	9	8
BASE_ADDRESS							
R							
0h							
7	6	5	4	3	2	1	0
BASE_ADDRESS							
R							
0h							

Access Types Legend

Table 3-859. RX_BUF_BASE_N Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	BASE_ADDRESS	R	0h	Receive Data Buffer Base Address This is the base address of the 16-word data buffer used by the receiver. Reset Source: fsi_rx_rst_mod_g_rst_n

3.11.37 Access Table

Table 3-860. Access Type Codes

Access Type	Code	Description
W	W	Write
R	R	Read
R/W	R/W	Read / Write

3.12 FSI_TX Registers

Table 3-861. MEM, MEM Registers, Base Address=0X0000000050280000, Length=4096

Offset	Length	Register Name	fsi_tx0 Physical Address	fsi_tx1 Physical Address	fsi_tx2 Physical Address
0h	16	TX_MASTER_CTRL	5028 0000h	5028 1000h	502A 0000h
4h	16	TX_CLK_CTRL	5028 0004h	5028 1004h	502A 0004h
8h	16	TX_OPER_CTRL_LO_ALT2_	5028 0008h	5028 1008h	502A 0008h
Ah	16	TX_OPER_CTRL_HI_ALT1_	5028 000Ah	5028 100Ah	502A 000Ah
Ch	16	TX_FRAME_CTRL	5028 000Ch	5028 100Ch	502A 000Ch
Eh	16	TX_FRAME_TAG_UDATA	5028 000Eh	5028 100Eh	502A 000Eh
10h	16	TX_BUF_PTR_LOAD	5028 0010h	5028 1010h	502A 0010h
12h	16	TX_BUF_PTR_STS	5028 0012h	5028 1012h	502A 0012h
14h	16	TX_PING_CTRL_ALT1_	5028 0014h	5028 1014h	502A 0014h
16h	16	TX_PING_TAG	5028 0016h	5028 1016h	502A 0016h
18h	32	TX_PING_TO_REF	5028 0018h	5028 1018h	502A 0018h
1Ch	32	TX_PING_TO_CNT	5028 001Ch	5028 101Ch	502A 001Ch
20h	16	TX_INT_CTRL	5028 0020h	5028 1020h	502A 0020h
22h	16	TX_DMA_CTRL	5028 0022h	5028 1022h	502A 0022h
24h	16	TX_LOCK_CTRL	5028 0024h	5028 1024h	502A 0024h
28h	16	TX_EVT_STS	5028 0028h	5028 1028h	502A 0028h
2Ch	16	TX_EVT_CLR	5028 002Ch	5028 102Ch	502A 002Ch
2Eh	16	TX_EVT_FRC	5028 002Eh	5028 102Eh	502A 002Eh
30h	16	TX_USER_CRC	5028 0030h	5028 1030h	502A 0030h
40h	32	TX_ECC_DATA	5028 0040h	5028 1040h	502A 0040h
44h	16	TX_ECC_VAL	5028 0044h	5028 1044h	502A 0044h
48h	16	TX_DLYLINE_CTRL	5028 0048h	5028 1048h	502A 0048h
80h + Formula	16	TX_BUF_BASE_N	5028 0080h + Formula	5028 1080h + Formula	502A 0080h + Formula

Table 3-862. MEM, MEM Registers, Base Address=0X0000000050280000, Length=4096

Offset	Length	Register Name	fsi_tx3 Physical Address
0h	16	TX_MASTER_CTRL	502A 1000h
8h	16	TX_OPER_CTRL_LO_ALT2_	502A 1008h
Ah	16	TX_OPER_CTRL_HI_ALT1_	502A 100Ah
Ch	16	TX_FRAME_CTRL	502A 100Ch
Eh	16	TX_FRAME_TAG_UDATA	502A 100Eh
10h	16	TX_BUF_PTR_LOAD	502A 1010h
12h	16	TX_BUF_PTR_STS	502A 1012h
14h	16	TX_PING_CTRL_ALT1_	502A 1014h
16h	16	TX_PING_TAG	502A 1016h
18h	32	TX_PING_TO_REF	502A 1018h
1Ch	32	TX_PING_TO_CNT	502A 101Ch
20h	16	TX_INT_CTRL	502A 1020h
22h	16	TX_DMA_CTRL	502A 1022h
24h	16	TX_LOCK_CTRL	502A 1024h
28h	16	TX_EVT_STS	502A 1028h
2Ch	16	TX_EVT_CLR	502A 102Ch
2Eh	16	TX_EVT_FRC	502A 102Eh

Table 3-862. MEM, MEM Registers, Base Address=0X0000000050280000, Length=4096 (continued)

Offset	Length	Register Name	fsi_tx3 Physical Address
30h	16	TX_USER_CRC	502A 1030h
40h	32	TX_ECC_DATA	502A 1040h
44h	16	TX_ECC_VAL	502A 1044h
48h	16	TX_DLYLINE_CTRL	502A 1048h
80h + Formula	16	TX_BUF_BASE_N	502A 1080h + Formula

3.12.1 MEM_TX_MASTER_CTRL Registers

3.12.1.1 MEM_MASTER_CTRL Register (Offset = 0h) [reset = 0h]

Short Description: Transmit master control r

Long Description: Transmit master control register

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Table 3-863. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 0000h
FSI_TX1	5028 1000h
FSI_TX2	502A 0000h
FSI_TX3	502A 1000h

Figure 3-374. TX_MASTER_CTRL Name Register

15	14	13	12	11	10	9	8
KEY							
W							
0h							
7	6	5	4	3	2	1	0
RESERVED_1						FLUSH	CORE_RST
R						R/W	R/W
0h						0h	0h

Access Types Legend

Table 3-864. TX_MASTER_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	KEY	W	0h	Write Key In order to write to any bit in this register, 0xA5 must be written to this field at the same time. Otherwise, writes are ignored. The key is cleared immediately after writing, so it must be written again for every change to this register. Reset Source: fsi_tx_rst_mod_g_rst_n
7:2	RESERVED_1	R	0h	Reserved Reset Source: fsi_tx_rst_mod_g_rst_n
1	FLUSH	R/W	0h	Flush Operation Start bit This bit will cause the transmitter to initiate a flush pattern of a single toggle on the TXD0 and TXD1 followed by five full cycles of TXCLK. This bit should be written only when the CORE_RST bit is 0 and the clock to the Transmitter core is turned on. 0h [R/W] = Clear this bit. 1h [R/W] = Setting this bit will Initiate flush sequence. To properly execute a flush sequence, Set FLUSH to 1, wait for five TXCLK cycles then clear FLUSH to 0. Note: The KEY field must contain 0xA5 for any write to this bit to take effect. The software must keep this bit set to 1 for at least five TXCLK cycles before setting it back to 0. Reset Source: fsi_tx_rst_mod_g_rst_n
0	CORE_RST	R/W	0h	Transmitter Master Core Reset bit This bit controls the transmitter master core reset. In order to send any frame, this bit must be cleared. 0h [R/W] = Transmitter core is not in reset and can transmit frames. 1h [R/W] = Transmitter core is held in reset. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect. Reset Source: fsi_tx_rst_mod_g_rst_n

3.12.2 MEM_TX_CLK_CTRL Registers

3.12.2.1 MEM_CLK_CTRL Register (Offset = 4h) [reset = 0h]

Short Description: Transmit clock control re

Long Description: Transmit clock control register

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Table 3-865. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 0004h
FSI_TX1	5028 1004h
FSI_TX2	502A 0004h
FSI_TX3	502A 1004h

Figure 3-375. TX_CLK_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED_1						PRESCALE_VAL	
R						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PRESCALE_VAL						CLK_EN	CLK_RST
R/W						R/W	R/W
0h						0h	0h

Access Types Legend

Table 3-866. TX_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved Reset Source: fsi_tx_rst_mod_g_rst_n
9:2	PRESCALE_VAL	R/W	0h	Clock Divider Prescale Value The input clock is divided by this 8-bit value and fed into the transmitter core. This divided clock is the rate at which TXCLK will operate. 0h [R/W] = Reserved 1h [R/W] = Input clock /1 2h [R/W] = Input clock /2 3h [R/W] = Input clock /3 4h [R/W] = Input clock /4 ... FFh [R/W] = Input clock /255 TXCLKIN = Input clock / PRESCALE_VAL In FSI mode: TXCLK = TXCLKIN / 2 In SPI mode: TXCLK = TXCLKIN Reset Source: fsi_tx_rst_mod_g_rst_n
1	CLK_EN	R/W	0h	Clock Divider Enable bit This bit will enable and disable the input clock divider and start the clock to the transmitter core. 0h [R/W] = The input clock divider is not enabled and the clock is not connected to the transmitter core. 1h [R/W] = The input clock to the transmitter core is being divided by the PRESCALE_VAL and enabled. Reset Source: fsi_tx_rst_mod_g_rst_n
0	CLK_RST	R/W	0h	Clock Divider Reset bit This bit will reset the clock counter in the clock divider. 0h [R/W] = The clock divider is set based on the value in PRESCALE_VAL. The input clock will be divided by PRESCALE_VAL if CLK_EN is set. 1h [R/W] = The clock divider will be reset to 0 and will stay reset until software writes a 0 to this bit. Reset Source: fsi_tx_rst_mod_g_rst_n

3.12.3 MEM_TX_OPER_CTRL_LO_ALT2_ Registers

3.12.3.1 MEM_OPER_CTRL_LO_ALT2_ Register (Offset = 8h) [reset = 0h]

Short Description: Transmit operation contro

Long Description: Transmit operation control register low

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Table 3-867. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 0008h
FSI_TX1	5028 1008h
FSI_TX2	502A 0008h
FSI_TX3	502A 1008h

Figure 3-376. TX_OPER_CTRL_LO_ALT2_ Name Register

15	14	13	12	11	10	9	8
RESERVED_1					SEL_TDM_IN	TDM_ENABLE	SEL_PLLCLK
R					R/W	R/W	R/W
0h					0h	0h	0h
7	6	5	4	3	2	1	0
PING_TO_MODE	SW_CRC	START_MODE			SPI_MODE	DATA_WIDTH	
R/W	R/W	R/W			R/W	R/W	
0h	0h	0h			0h	0h	

Access Types Legend

Table 3-868. TX_OPER_CTRL_LO_ALT2_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED_1	R	0h	Reserved Reset Source: fsi_tx_rst_mod_g_rst_n
10	SEL_TDM_IN	R/W	0h	Input TDM port Select bit This bit selects the input port for the transmitter core between the TDM input pins or the RX module. When this bit is '0', the inputs selected for TDM are from the TDM input pins. When this bit is '1', then inputs selected for TDM are from the RX module. Reset Source: fsi_tx_rst_mod_g_rst_n
9	TDM_ENABLE	R/W	0h	Transmit TDM Mode Enable bit. This bit enables the TDM Mode for multi-slave TDM operation. 0h [R/W] Transmit TDM Mode is not enabled. 1h [R/W] Transmit TDM Mode is enabled. Reset Source: fsi_tx_rst_mod_g_rst_n
8	SEL_PLLCLK	R/W	0h	Input Clock Select bit This bit selects the input clock source for the transmitter core. 0h [R/W] = SYSCLK is the source of the transmitter clock into the clock prescaler. 1h [R/W] = PLLRAWCLK is the source of the transmitter core clock into the clock prescaler. Reset Source: fsi_tx_rst_mod_g_rst_n
7	PING_TO_MODE	R/W	0h	Ping Counter Reset Mode Select bit This bit selects when the ping counter will reset. 0h [R/W] = The ping counter will reset and restart only on hardware initiated ping frames, when ping counter has timed out. 1h [R/W] = The ping counter will reset and restart on any software initiated frame as well as a ping counter timeout Reset Source: fsi_tx_rst_mod_g_rst_n
6	SW_CRC	R/W	0h	CRC Source Select bit This bit selects the source of the CRC value that is transmitted. 0h [R/W] = The transmitted CRC value is computed by hardware. 1h [R/W] = The transmitted CRC value is sourced from the value programmed in the TX_USER_CRC register. Reset Source: fsi_tx_rst_mod_g_rst_n

Table 3-868. TX_OPER_CTRL_LO_ALT2_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:3	START_MODE	R/W	0h	Transmission Start Mode Select bit These bits select the method by which a new frame transmission is started. 0h [R/W] = Only a software write to TX_FRAME_CTRL.START initiate a new transmission. 1h [R/W] = The configured external trigger will initiate a new transmission. 2h [R/W] = Either writing to TX_FRAME_CTRL.START or the TX_FRAME_TAG_UDATA register will initiate a new transmission. All other combinations of bits are illegal and reserved for future use. Reset Source: fsi_tx_rst_mod_g_rst_n
2	SPI_MODE	R/W	0h	SPI Mode Select bit This bit enables and disables SPI compatibility mode. 0h [R/W] = FSI is in normal mode of operation. 1h [R/W] = FSI is operating in SPI compatibility mode. Reset Source: fsi_tx_rst_mod_g_rst_n
1:0	DATA_WIDTH	R/W	0h	Transmit Data Width Select bits These bits define the number of data lines used by the transmitter. 0h [R/W] = Data will be transmitted on one data line [TXD0] 1h [R/W] = Data will be transmitted on two data lines [TXD0 and TXD1]. The format of the data is described in the preceeding chapter. 2h, 3h [R/W] = Reserved Reset Source: fsi_tx_rst_mod_g_rst_n

3.12.4 MEM_TX_OPER_CTRL_HI_ALT1_ Registers

3.12.4.1 MEM_OPER_CTRL_HI_ALT1_ Register (Offset = Ah) [reset = 0h]

Short Description: Transmit operation contro

Long Description: Transmit operation control register high

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Table 3-869. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 000Ah
FSI_TX1	5028 100Ah
FSI_TX2	502A 000Ah
FSI_TX3	502A 100Ah

Figure 3-377. TX_OPER_CTRL_HI_ALT1_ Name Register

15	14	13	12	11	10	9	8
RESERVED_2			EXT_TRIG_SEL				
R			R/W				
0h			0h				
7	6	5	4	3	2	1	0
EXT_TRIG_SEL	ECC_SEL	FORCE_ERR	RESERVED_1				
R/W	R/W	R/W	R				
0h	0h	0h	0h				

Access Types Legend

Table 3-870. TX_OPER_CTRL_HI_ALT1_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_2	R	0h	Reserved Reset Source: fsi_tx_rst_mod_g_rst_n
12:7	EXT_TRIG_SEL	R/W	0h	External Trigger Select bit These bits define which of the 64 external inputs will be used as the source for the external input trigger. 00h [R/W] = Trigger 1 is the source. 01h [R/W] = Trigger 2 is the source. 02h [R/W] = Trigger 3 is the source. ... 3Fh [R/W] = Trigger 64 is the source. Reset Source: fsi_tx_rst_mod_g_rst_n
6	ECC_SEL	R/W	0h	ECC Data Width Select bit This bit selects between 16-bit and 32-bit ECC computation. 0h [R/W] = 32-bit ECC is used. 1h [R/W] = 16-bit ECC is used. Reset Source: fsi_tx_rst_mod_g_rst_n
5	FORCE_ERR	R/W	0h	Error Frame Force bit This bit will force the the CRC value of the transmitted data frame to 0 whenever there is a buffer overrun or underrun condition. This can be used to force a corrupted CRC as the data is not guaranteed to be reliable. The receiver will treat the data as invalid and can handle this as needed. Note: DO NOT use FORCE_ERR if using the SW CRC mode [FSI Transmit]. 0h [R/W] = The CRC will not be forced to 0. 1h [R/W] = The CRC will be forced to 0 in a buffer overrun or underrun condition. Reset Source: fsi_tx_rst_mod_g_rst_n
4:0	RESERVED_1	R	0h	Reserved Reset Source: fsi_tx_rst_mod_g_rst_n

3.12.5 MEM_TX_FRAME_CTRL Registers

3.12.5.1 MEM_FRAME_CTRL Register (Offset = Ch) [reset = 0h]

Short Description: Transmit frame control re

Long Description: Transmit frame control register

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Table 3-871. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 000Ch
FSI_TX1	5028 100Ch
FSI_TX2	502A 000Ch
FSI_TX3	502A 100Ch

Figure 3-378. TX_FRAME_CTRL Name Register

15	14	13	12	11	10	9	8
START	RESERVED_1						
R/W	R						
0h	0h						
7	6	5	4	3	2	1	0
N_WORDS				FRAME_TYPE			
R/W				R/W			
0h				0h			

Access Types Legend

Table 3-872. TX_FRAME_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	START	R/W	0h	Start Transmission bit This bit will cause the FSI to start transmitting the next frame. 0h [R/W] = Writing a 0 to this bit will have no effect. 1h [R/W] = Start the next transmission. This bit will be cleared by hardware. Reset Source: fsi_tx_rst_mod_g_rst_n
14:8	RESERVED_1	R	0h	Reserved Reset Source: fsi_tx_rst_mod_g_rst_n
7:4	N_WORDS	R/W	0h	Number of Words to be Transmitted This field defines the number of words which will be transmitted in a DATA_N_WORD frame. This is a user-defined field that must match the corresponding field in the receiver. Set this bitfield to be one less than the number of words to be transmitted. 0h [R/W] = 1 data word frame [16-bit data]. 1h [R/W] = 2 data word frame [32-bit data]. .. Fh [R/W] = 16 data word frame [256-bit data]. Reset Source: fsi_tx_rst_mod_g_rst_n
3:0	FRAME_TYPE	R/W	0h	Transmit Frame Type This field determines the type of frame that will be transmitted next. 0000b [R/W] = Ping Frame. This frame can be sent either by software or automatically by hardware. 0100b [R/W] = DATA_1_WORD Frame. One word data frame [16-bit data]. 0101b [R/W] = DATA_2_WORD Frame. Two word data frame [32-bit data]. 0110b [R/W] = DATA_4_WORD Frame. Four word data frame [64-bit data]. 0111b [R/W] = DATA_6_WORD Frame. Six word data frame [96-bit data]. 0011b [R/W] = DATA_N_WORD Frame. The N_WORDS field will determine the number of words [1 to 16] to be sent. Both the transmitter and receiver must have the same value programmed. 1111b [R/W] = Error Frame. This frame can be used during error conditions or any condition where the transmitter wants to notify the receiver of a high priorty status. However, the user software is at liberty to use this for any purpose. 0001b, 0010b, and 1000b through 1110b are Reserved and should not be used. Reset Source: fsi_tx_rst_mod_g_rst_n

3.12.6 MEM_TX_FRAME_TAG_UDATA Registers

3.12.6.1 MEM_FRAME_TAG_UDATA Register (Offset = Eh) [reset = 0h]

Short Description: Transmit frame tag and us

Long Description: Transmit frame tag and user data register

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Table 3-873. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 000Eh
FSI_TX1	5028 100Eh
FSI_TX2	502A 000Eh
FSI_TX3	502A 100Eh

Figure 3-379. TX_FRAME_TAG_UDATA Name Register

15	14	13	12	11	10	9	8
USER_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_1				FRAME_TAG			
R				R/W			
0h				0h			

Access Types Legend

Table 3-874. TX_FRAME_TAG_UDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	USER_DATA	R/W	0h	User Data bits This is a user-defined value that will be loaded into the the user data phase of the frame. This 8-bit value can be used by the receiver for any application need. This value will not impact any hardware behavior. Reset Source: fsi_tx_rst_mod_g_rst_n
7:4	RESERVED_1	R	0h	Reserved Reset Source: fsi_tx_rst_mod_g_rst_n
3:0	FRAME_TAG	R/W	0h	This will be used only for software initiated transmissions. Frame tag bits This is a user-defined value that will be loaded into the frame tag phase of the next transmission. The receiver may use the frame tag for any application need. This value will not impact any hardware behavior For external triggers do not use this register. Use the TX_PING_TAG register instead. Reset Source: fsi_tx_rst_mod_g_rst_n

3.12.7 MEM_TX_BUF_PTR_LOAD Registers

3.12.7.1 MEM_BUF_PTR_LOAD Register (Offset = 10h) [reset = 0h]

Short Description: Transmit buffer pointer c

Long Description: Transmit buffer pointer control load register

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Table 3-875. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 0010h
FSI_TX1	5028 1010h
FSI_TX2	502A 0010h
FSI_TX3	502A 1010h

Figure 3-380. TX_BUF_PTR_LOAD Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1				BUF_PTR_LOAD			
R				R/W			
0h				0h			

Access Types Legend

Table 3-876. TX_BUF_PTR_LOAD Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED_1	R	0h	Reserved Reset Source: fsi_tx_rst_mod_g_rst_n
3:0	BUF_PTR_LOAD	R/W	0h	Buffer Pointer Load bits These bits are used to force the transmit buffer pointer to a desired index within the transmit buffer. The next transmission will begin picking data from this index and increment appropriately. This value will be reflected in TX_BUF_PTR_STS only after a minimum 3 SYSCLK cycles + 3 TXCLK cycles. This value should not be written while there is an active transmission as it may corrupt the ongoing frame or other undefined behavior. Reset Source: fsi_tx_rst_mod_g_rst_n

3.12.8 MEM_TX_BUF_PTR_STS Registers

3.12.8.1 MEM_BUF_PTR_STS Register (Offset = 12h) [reset = 0h]

Short Description: Transmit buffer pointer c

Long Description: Transmit buffer pointer control status register

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Table 3-877. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 0012h
FSI_TX1	5028 1012h
FSI_TX2	502A 0012h
FSI_TX3	502A 1012h

Figure 3-381. TX_BUF_PTR_STS Name Register

15	14	13	12	11	10	9	8
RESERVED_2			CURR_WORD_CNT				
R			R				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED_1				CURR_BUF_PTR			
R				R			
0h				0h			

Access Types Legend

Table 3-878. TX_BUF_PTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_2	R	0h	Reserved Reset Source: fsi_tx_rst_mod_g_rst_n
12:8	CURR_WORD_CNT	R	0h	Words Remaining in the transmit buffer This value indicates the number of words present in the data buffer which have not yet been transmitted. This value is only valid when there is no active transmission. Note: This value will not be valid if there is a buffer overrun or underrun condition. Reset Source: fsi_tx_rst_mod_g_rst_n
7:4	RESERVED_1	R	0h	Reserved Reset Source: fsi_tx_rst_mod_g_rst_n
3:0	CURR_BUF_PTR	R	0h	Current Buffer Pointer Index This bitfield will show the current index of the buffer pointer. This value is only valid when there is no active transmission. Reset Source: fsi_tx_rst_mod_g_rst_n

3.12.9 MEM_TX_PING_CTRL_ALT1_ Registers

3.12.9.1 MEM_PING_CTRL_ALT1_ Register (Offset = 14h) [reset = 0h]

Short Description: Transmit ping control reg

Long Description: Transmit ping control register

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Table 3-879. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 0014h
FSI_TX1	5028 1014h
FSI_TX2	502A 0014h
FSI_TX3	502A 1014h

Figure 3-382. TX_PING_CTRL_ALT1_ Name Register

15	14	13	12	11	10	9	8
RESERVED_1							EXT_TRIG_SEL
R							R/W
0h							0h
7	6	5	4	3	2	1	0
EXT_TRIG_SEL					EXT_TRIG_EN	TIMER_EN	CNT_RST
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Access Types Legend

Table 3-880. TX_PING_CTRL_ALT1_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	RESERVED_1	R	0h	Reserved Reset Source: fsi_tx_rst_mod_g_rst_n
8:3	EXT_TRIG_SEL	R/W	0h	External Trigger Select bits This bitfield will select one of the 64 external trigger inputs to as the source to generate a ping frame. A ping frame will only be generated if the EXT_TRIG_EN bit is set. 0h [R/W] = Trigger 1 will be used to generate a ping frame. 1h [R/W] = Trigger 2 will be used to generate a ping frame. .. 3Fh [R/W] = Trigger 64 will be used to generate a ping frame. Reset Source: fsi_tx_rst_mod_g_rst_n
2	EXT_TRIG_EN	R/W	0h	External Trigger Enable bit This bit will allow the external trigger logic to generate a ping frame. 0h [R/W] = External triggers will not be used to generate ping frames. 1h [R/W] = The selected external trigger [selected by EXT_TRIG_SEL bits] will be able to generate a ping frame. The ping timer will be ignored if this bit is set. Reset Source: fsi_tx_rst_mod_g_rst_n
1	TIMER_EN	R/W	0h	Ping Timer Enable bit This bit will enable the ping timer for generating periodic ping frames. 0h [R/W] = The ping timer is disabled and will not generate ping frames. 1h [R/W] = The ping timer is enabled and can be used to generate ping frames.Once the timer count reaches the value set by the TX_PING_TO_REF register, it will initiate a ping frame transmission. Note: If the ping timer is used, EXT_TRIG_EN should not be set as it will override this function. Reset Source: fsi_tx_rst_mod_g_rst_n
0	CNT_RST	R/W	0h	Ping Counter Reset bit Writing a 1 to this bit will reset the ping counter to 0. The counter will stay in reset as long as this bit is set to 1. This bit needs to be cleared to 0 to use the counter. 0h [R/W] = Clear the CNT_RST. 1h [R/W] = The ping counter will be reset to 0. Reset Source: fsi_tx_rst_mod_g_rst_n

3.12.10 MEM_TX_PING_TAG Registers

3.12.10.1 MEM_PING_TAG Register (Offset = 16h) [reset = 0h]

Short Description: Transmit ping tag registe

Long Description: Transmit ping tag register

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Table 3-881. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 0016h
FSI_TX1	5028 1016h
FSI_TX2	502A 0016h
FSI_TX3	502A 1016h

Figure 3-383. TX_PING_TAG Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1				TAG			
R				R/W			
0h				0h			

Access Types Legend

Table 3-882. TX_PING_TAG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED_1	R	0h	Reserved Reset Source: fsi_tx_rst_mod_g_rst_n
3:0	TAG	R/W	0h	Ping Frame Tag This field contains a 4-bit tag which will be sent in any ping frame that is initiated by an external trigger or the ping timer. This field is user-defined and can be set based on the application requirement. If a ping frame is generated manually, the transmitted tag will be from TX_FRAME_TAG_UDATA.FRAME_TAG, not this value. Reset Source: fsi_tx_rst_mod_g_rst_n

3.12.11 MEM_TX_PING_TO_REF Registers

3.12.11.1 MEM_PING_TO_REF Register (Offset = 18h) [reset = 0h]

Short Description: Transmit ping timeout cou

Long Description: Transmit ping timeout counter reference

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Table 3-883. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 0018h
FSI_TX1	5028 1018h
FSI_TX2	502A 0018h
FSI_TX3	502A 1018h

Figure 3-384. TX_PING_TO_REF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TO_REF															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TO_REF															
R/W															
0h															

Access Types Legend

Table 3-884. TX_PING_TO_REF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TO_REF	R/W	0h	Ping Timer Reference Value. This is the 32-bit reference value for the ping timer. The timer will increment the counter starting from 0. When the reference value is reached, it will generate a timeout event, triggering a ping frame transmission. The counter will then reset to 0 and continue counting. Reset Source: fsi_tx_rst_mod_g_rst_n

3.12.12 MEM_TX_PING_TO_CNT Registers

3.12.12.1 MEM_PING_TO_CNT Register (Offset = 1Ch) [reset = 0h]

Short Description: Transmit ping timeout cur

Long Description: Transmit ping timeout current count

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Table 3-885. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 001Ch
FSI_TX1	5028 101Ch
FSI_TX2	502A 001Ch
FSI_TX3	502A 101Ch

Figure 3-385. TX_PING_TO_CNT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TO_CNT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TO_CNT															
R															
0h															

Access Types Legend

Table 3-886. TX_PING_TO_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TO_CNT	R	0h	Ping Timer Counter Value This register contains the current value of the ping timer counter. After reset, this counter will increment until it reaches the reference value [TX_PING_TO_REF], at which point it generates a ping frame transmission. After this point, the counter will reset to 0 and continue counting. This is a free-running counter Reset Source: fsi_tx_rst_mod_g_rst_n

3.12.13 MEM_TX_INT_CTRL Registers

3.12.13.1 MEM_INT_CTRL Register (Offset = 20h) [reset = 0h]

Short Description: Transmit interrupt event

Long Description: Transmit interrupt event control register

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Table 3-887. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 0020h
FSI_TX1	5028 1020h
FSI_TX2	502A 0020h
FSI_TX3	502A 1020h

Figure 3-386. TX_INT_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED_2				INT2_EN_PING_TO	INT2_EN_BUF_OVERRUN	INT2_EN_BUF_UNDERRUN	INT2_EN_FRAME_DONE
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED_1				INT1_EN_PING_TO	INT1_EN_BUF_OVERRUN	INT1_EN_BUF_UNDERRUN	INT1_EN_FRAME_DONE
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Access Types Legend

Table 3-888. TX_INT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_2	R	0h	Reserved Reset Source: fsi_tx_rst_mod_g_rst_n
11	INT2_EN_PING_TO	R/W	0h	Enable PING Timer Interrupt to INT2 This bit allows the event to generate an interrupt on the INT2 line. 0h [R/W] = This event will not trigger an interrupt on TX_INT2. 1h [R/W] = The ping timer event will trigger an interrupt on TX_INT2. Reset Source: fsi_tx_rst_mod_g_rst_n
10	INT2_EN_BUF_OVERRUN	R/W	0h	Enable Buffer Overrun Interrupt to INT2 This bit allows the event to generate an interrupt on the INT2 line. 0h [R/W] = This event will not trigger an interrupt on TX_INT2. 1h [R/W] = A Buffer Overrun condition will trigger an interrupt on TX_INT2. Reset Source: fsi_tx_rst_mod_g_rst_n
9	INT2_EN_BUF_UNDERRUN	R/W	0h	Enable Buffer Underrun Interrupt to INT2 This bit allows the event to generate an interrupt on the INT2 line. 0h [R/W] = This event will not trigger an interrupt on TX_INT2. 1h [R/W] = A Buffer Underrun condition will trigger an interrupt on TX_INT2. Reset Source: fsi_tx_rst_mod_g_rst_n
8	INT2_EN_FRAME_DONE	R/W	0h	Enable Frame Done interrupt to INT2 This bit allows the event to generate an interrupt on the INT2 line. 0h [R/W] = This event will not trigger an interrupt on TX_INT2. 1h [R/W] = A Frame Done event will trigger an interrupt on TX_INT2. Reset Source: fsi_tx_rst_mod_g_rst_n
7:4	RESERVED_1	R	0h	Reserved Reset Source: fsi_tx_rst_mod_g_rst_n

Table 3-888. TX_INT_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	INT1_EN_PING_TO	R/W	0h	Enable Ping Timer Interrupt to INT1 This bit allows the event to generate an interrupt on the INT1 line. 0h [R/W] = This event will not trigger an interrupt on TX_INT1. 1h [R/W] = The ping timer event will trigger an interrupt on TX_INT1. Reset Source: fsi_tx_rst_mod_g_rst_n
2	INT1_EN_BUF_OVERRUN	R/W	0h	Enable Buffer Overrun Interrupt to INT1 This bit allows the event to generate an interrupt on the INT1 line. 0h [R/W] = This event will not trigger an interrupt on TX_INT1. 1h [R/W] = A Buffer Overrun condition will trigger an interrupt on TX_INT1. Reset Source: fsi_tx_rst_mod_g_rst_n
1	INT1_EN_BUF_UNDERRUN	R/W	0h	Enable Buffer Underrun Interrupt to INT1 This bit allows the event to generate an interrupt on the INT1 line. 0h [R/W] = This event will not trigger an interrupt on TX_INT1. 1h [R/W] = A Buffer Underrun condition will trigger an interrupt on TX_INT1. Reset Source: fsi_tx_rst_mod_g_rst_n
0	INT1_EN_FRAME_DONE	R/W	0h	Enable Frame Done interrupt to INT1 This bit allows the event to generate an interrupt on the INT1 line. 0h [R/W] = This event will not trigger an interrupt on TX_INT1. 1h [R/W] = A Frame Done event will trigger an interrupt on TX_INT1. Reset Source: fsi_tx_rst_mod_g_rst_n

3.12.14 MEM_TX_DMA_CTRL Registers

3.12.14.1 MEM_DMA_CTRL Register (Offset = 22h) [reset = 0h]

Short Description: Transmit DMA event contro

Long Description: Transmit DMA event control register

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Table 3-889. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 0022h
FSI_TX1	5028 1022h
FSI_TX2	502A 0022h
FSI_TX3	502A 1022h

Figure 3-387. TX_DMA_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1							DMA_EVT_EN
R							R/W
0h							0h

Access Types Legend

Table 3-890. TX_DMA_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	RESERVED_1	R	0h	Reserved Reset Source: fsi_tx_rst_mod_g_rst_n
0	DMA_EVT_EN	R/W	0h	DMA Event Enable bit This bit will enable the DMA event to be generated upon the completion of a transmit frame. 0h [R/W] = A DMA event will not be generated. 1h [R/W] = A DMA event will be generated upon the completion of a transmitted frame. Note: The DMA event will only be generated for data frames. Reset Source: fsi_tx_rst_mod_g_rst_n

3.12.15 MEM_TX_LOCK_CTRL Registers

3.12.15.1 MEM_LOCK_CTRL Register (Offset = 24h) [reset = 0h]

Short Description: Transmit lock control reg

Long Description: Transmit lock control register

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Table 3-891. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 0024h
FSI_TX1	5028 1024h
FSI_TX2	502A 0024h
FSI_TX3	502A 1024h

Figure 3-388. TX_LOCK_CTRL Name Register

15	14	13	12	11	10	9	8
KEY							
W							
0h							
7	6	5	4	3	2	1	0
RESERVED_1							LOCK
R							R/W
0h							0h

Access Types Legend

Table 3-892. TX_LOCK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	KEY	W	0h	Write Key In order to write to this register, 0xA5 must be written to this field at the same time. Otherwise, writes are ignored. The key is cleared immediately after writing, so it must be written again for every change to this register. Reset Source: fsi_tx_rst_mod_g_rst_n
7:1	RESERVED_1	R	0h	Reserved Reset Source: fsi_tx_rst_mod_g_rst_n
0	LOCK	R/W	0h	Control Register Lock Enable bit This bit locks the contents of all the transmit control registers that support a lock protection. Once locked, further writes will not take effect until a SYSRS has reset this register. Once set, further writes to this bit will be ignored. 0h [R/W] = Transmit control registers can be modified and are not locked. 1h [R/W] = Transmit control registers are locked and cannot be modified until this bit is cleared by SYSRS. Any further writes to this bit are ignored. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect. Reset Source: fsi_tx_rst_mod_g_rst_n

3.12.16 MEM_TX_EVT_STS Registers

3.12.16.1 MEM_EVT_STS Register (Offset = 28h) [reset = 0h]

Short Description: Transmit event and error

Long Description: Transmit event and error status flag register

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Table 3-893. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 0028h
FSI_TX1	5028 1028h
FSI_TX2	502A 0028h
FSI_TX3	502A 1028h

Figure 3-389. TX_EVT_STS Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1				PING_TRIGGERED	BUF_OVERRUN	BUF_UNDERRUN	FRAME_DONE
R				R	R	R	R
0h				0h	0h	0h	0h

Access Types Legend

Table 3-894. TX_EVT_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED_1	R	0h	Reserved Reset Source: fsi_tx_rst_mod_g_rst_n
3	PING_TRIGGERED	R	0h	Ping Frame Triggered Flag Bit This bit indicates that a ping frame has been triggered. This bit is set by hardware when either the ping timer or an external trigger event have occured. Software can also force this bit to get set by writing to the TX_EVT_FRC register. 0h [R] = A ping frame has not been triggered. 1h [R] = A ping frame has been triggered by either the ping timer or external trigger. To clear this bit, write to the corresponding bit in the TX_EVT_CLR register. Reset Source: fsi_tx_rst_mod_g_rst_n
2	BUF_OVERRUN	R	0h	Buffer Overrun Flag Bit This bit inditcates that buffer overrun has occured.Software can also force this bit to get set by writing to the TX_EVT_FRC register. 0h [R] = Buffer Overrun has not occured. 1h [R] = Buffer Overrun has occured. To clear this bit, write to the corresponding bit in the TX_EVT_CLR register. Reset Source: fsi_tx_rst_mod_g_rst_n
1	BUF_UNDERRUN	R	0h	Buffer Underrun Flag Bit This bit inditcates that buffer underrun has occured.Software can also force this bit to get set by writing to the TX_EVT_FRC register. 0h [R] = Buffer Underrun has not occured. 1h [R] = Buffer Underrun has occured. To clear this bit, write to the corresponding bit in the TX_EVT_CLR register. Reset Source: fsi_tx_rst_mod_g_rst_n

Table 3-894. TX_EVT_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	FRAME_DONE	R	0h	Frame Done Flag Bit This bit inditcates a Frame Done condition. This bit is set by hardware when a frame transmission has been completed. Software can also force this bit to get set by writing to the TX_EVT_FRC register. 0h [R] = Frame Done condition has not occured. 1h [R] = Frame Done condition has occured. To clear this bit, write to the corresponding bit in the TX_EVT_CLR register. Reset Source: fsi_tx_rst_mod_g_rst_n

3.12.17 MEM_TX_EVT_CLR Registers

3.12.17.1 MEM_EVT_CLR Register (Offset = 2Ch) [reset = 0h]

Short Description: Transmit event and error

Long Description: Transmit event and error clear register

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Table 3-895. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 002Ch
FSI_TX1	5028 102Ch
FSI_TX2	502A 002Ch
FSI_TX3	502A 102Ch

Figure 3-390. TX_EVT_CLR Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1				PING_TRIGGERED	BUF_OVERRUN	BUF_UNDERRUN	FRAME_DONE
R				W	W	W	W
0h				0h	0h	0h	0h

Access Types Legend

Table 3-896. TX_EVT_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED_1	R	0h	Reserved Reset Source: fsi_tx_rst_mod_g_rst_n
3	PING_TRIGGERED	W	0h	Ping Frame Triggered Flag Clear bit This bit clears the corresponding bit in the TX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the TX_EVT_STS register to 0. Note: This bit may not always be cleared when writing to the corresponding TX_EVT_CLR bit. If PING_TIMEOUT MODE is configured to be 0, a hardware ping timeout may occur when another frame is actively being transmitted. In this case, if this bit still shows as 1 after the clear bit is written then the ping frame has been triggered but not serviced. This bit does not indicate that the ping frame has been completely sent, only that it has been triggered by the timeout event. Reset Source: fsi_tx_rst_mod_g_rst_n
2	BUF_OVERRUN	W	0h	Buffer Overrun Flag Clear bit This bit clears the corresponding bit in the TX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the TX_EVT_STS register to 0. Reset Source: fsi_tx_rst_mod_g_rst_n
1	BUF_UNDERRUN	W	0h	Buffer Underrun Flag Clear bit This bit clears the corresponding bit in the TX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the TX_EVT_STS register to 0. Reset Source: fsi_tx_rst_mod_g_rst_n

Table 3-896. TX_EVT_CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	FRAME_DONE	W	0h	Frame Done Flag Clear bit This bit clears the corresponding bit in the TX_EVT_STS register. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Writing a 1 to this bit will clear the corresponding bit in the TX_EVT_STS register to 0. Reset Source: fsi_tx_rst_mod_g_rst_n

3.12.18 MEM_TX_EVT_FRC Registers

3.12.18.1 MEM_EVT_FRC Register (Offset = 2Eh) [reset = 0h]

Short Description: Transmit event and error

Long Description: Transmit event and error flag force register

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Table 3-897. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 002Eh
FSI_TX1	5028 102Eh
FSI_TX2	502A 002Eh
FSI_TX3	502A 102Eh

Figure 3-391. TX_EVT_FRC Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1				PING_TRIGGERED	BUF_OVERRUN	BUF_UNDERRUN	FRAME_DONE
R				W	W	W	W
0h				0h	0h	0h	0h

Access Types Legend

Table 3-898. TX_EVT_FRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED_1	R	0h	Reserved Reset Source: fsi_tx_rst_mod_g_rst_n
3	PING_TRIGGERED	W	0h	Ping Frame Triggered Flag Force bit This bit will cause the corresponding bit in the TX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding flag bit in the TX_EVT_STS Register. Reset Source: fsi_tx_rst_mod_g_rst_n
2	BUF_OVERRUN	W	0h	Buffer Overrun Flag Force bit This bit will cause the corresponding bit in the TX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [R/W] = Writing a 0 to this bit will have no effect. 1h [R/W] = Force the corresponding flag bit in the TX_EVT_STS Register. Reset Source: fsi_tx_rst_mod_g_rst_n
1	BUF_UNDERRUN	W	0h	Buffer Underrun Flag Force bit This bit will cause the corresponding bit in the TX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding flag bit in the TX_EVT_STS Register. Reset Source: fsi_tx_rst_mod_g_rst_n
0	FRAME_DONE	W	0h	Frame Done Flag Force bit This bit will cause the corresponding bit in the TX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h [W] = Writing a 0 to this bit will have no effect. 1h [W] = Force the corresponding flag bit in the TX_EVT_STS Register. Reset Source: fsi_tx_rst_mod_g_rst_n

3.12.19 MEM_TX_USER_CRC Registers

3.12.19.1 MEM_USER_CRC Register (Offset = 30h) [reset = 0h]

Short Description: Transmit user-defined CRC

Long Description: Transmit user-defined CRC register

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Table 3-899. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 0030h
FSI_TX1	5028 1030h
FSI_TX2	502A 0030h
FSI_TX3	502A 1030h

Figure 3-392. TX_USER_CRC Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
USER_CRC							
R/W							
0h							

Access Types Legend

Table 3-900. TX_USER_CRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED_1	R	0h	Reserved Reset Source: fsi_tx_rst_mod_g_rst_n
7:0	USER_CRC	R/W	0h	User-defined CRC This register contains the 8-bit CRC value to be transmitted in the next frame if the transmission is set for user-defined CRC option [TX_OPER_CTRL_LO.SW_CRC = 1]. This register is ignored if the hardware CRC generation is enabled. Reset Source: fsi_tx_rst_mod_g_rst_n

3.12.20 MEM_TX_ECC_DATA Registers

3.12.20.1 MEM_ECC_DATA Register (Offset = 40h) [reset = 0h]

Short Description: Transmit ECC data registe

Long Description: Transmit ECC data register

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Table 3-901. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 0040h
FSI_TX1	5028 1040h
FSI_TX2	502A 0040h
FSI_TX3	502A 1040h

Figure 3-393. TX_ECC_DATA Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA_HIGH															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA_LOW															
R/W															
0h															

Access Types Legend

Table 3-902. TX_ECC_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DATA_HIGH	R/W	0h	Upper 16 bits of ECC Data Writing to this bitfield will cause the ECC logic to compute the ECC[SEC-DED] the entire 32-bit register and update TX_ECC_VAL register with the results. Software should write to these 16 bits of the register in a 32-bit write when needing to compute ECC for 32-bits for the full TX_ECC_DATA register. Reset Source: fsi_tx_rst_mod_g_rst_n
15:0	DATA_LOW	R/W	0h	Lower 16 bits of ECC Data Writing to this bitfield will cause the ECC logic to compute the ECC[SEC-DED] for these 16 bits and update the TX_ECC_VAL register with the results. Software should write to these register bits as a 16-bit write when needing to compute ECC for 16-bits. Reset Source: fsi_tx_rst_mod_g_rst_n

3.12.21 MEM_TX_ECC_VAL Registers

3.12.21.1 MEM_ECC_VAL Register (Offset = 44h) [reset = ch]

Short Description: Transmit ECC value regist

Long Description: Transmit ECC value register

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Table 3-903. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 0044h
FSI_TX1	5028 1044h
FSI_TX2	502A 0044h
FSI_TX3	502A 1044h

Figure 3-394. TX_ECC_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1	ECC_VAL						
R	R						
0h	ch						

Access Types Legend

Table 3-904. TX_ECC_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:7	RESERVED_1	R	0h	Reserved Reset Source: fsi_tx_rst_mod_g_rst_n
6:0	ECC_VAL	R	Ch	Computed ECC Value This field contains the ECC value computed using SEC-DED either for 16-bit or 32-bit data in the TX_ECC_DATA register. Reset Source: fsi_tx_rst_mod_g_rst_n

3.12.22 MEM_TX_DLYLINE_CTRL Registers

3.12.22.1 MEM_DLYLINE_CTRL Register (Offset = 48h) [reset = 0h]

Short Description: Transmit delay Line contr

Long Description: Transmit delay Line control register

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Table 3-905. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 0048h
FSI_TX1	5028 1048h
FSI_TX2	502A 0048h
FSI_TX3	502A 1048h

Figure 3-395. TX_DLYLINE_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED_1	TXD1_DLY					TXD0_DLY	
R	R/W					R/W	
0h	0h					0h	
7	6	5	4	3	2	1	0
TXD0_DLY				TXCLK_DLY			
R/W				R/W			
0h				0h			

Access Types Legend

Table 3-906. TX_DLYLINE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved Reset Source: fsi_tx_rst_mod_g_rst_n
14:10	TXD1_DLY	R/W	0h	Delay Line Tap Select for TXD1 This bitfield selects the number of delay elements inserted into the TXD1 path from the pin boundary to the receiver core. 0h [R/W] Zero delay elements are included in the TXD1 path. TXD1 is taken directly from the pin. 1h [R/W] One delay element is included in the TXD1 path. 2h [R/W] Two delay elements are included in the TXD1 path. ... 1Fh [R/W] 31 delay elements are included in the TXD1 path, the maximum. Reset Source: fsi_tx_rst_mod_g_rst_n
9:5	TXD0_DLY	R/W	0h	Delay Line Tap Select for TXD0 This bitfield selects the number of delay elements inserted into the TXD0 path from the pin boundary to the receiver core. 0h [R/W] Zero delay elements are included in the TXD0 path. TXD0 is taken directly from the pin. 1h [R/W] One delay element is included in the TXD0 path. 2h [R/W] Two delay elements are included in the TXD0 path. ... 1Fh [R/W] 31 delay elements are included in the TXD0 path, the maximum. Reset Source: fsi_tx_rst_mod_g_rst_n
4:0	TXCLK_DLY	R/W	0h	Delay Line Tap Select for TXCLK This bitfield selects the number of delay elements inserted into the RXCLK path from the pin boundary to the receiver core. 0h [R/W] Zero delay elements are included in the TXCLK path. TXCLK is taken directly from the pin. 1h [R/W] One delay element is included in the TXCLK path. 2h [R/W] Two delay elements are included in the TXCLK path. ... 1Fh [R/W] 31 delay elements are included in the TXCLK path, the maximum. Reset Source: fsi_tx_rst_mod_g_rst_n

3.12.23 MEM_TX_BUF_BASE_N Registers

3.12.23.1 MEM_BUF_BASE_N Register (Offset = 80h) [reset = 0h]

Short Description: Base address for transmit

Long Description: Base address for transmit buffer

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Offset = 80h + (j * 2h); where j = 0h to Fh

Table 3-907. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 0080h
FSI_TX1	5028 1080h
FSI_TX2	502A 0080h
FSI_TX3	502A 1080h

Figure 3-396. TX_BUF_BASE_N Name Register

15	14	13	12	11	10	9	8
BASE_ADDRESS							
R/W							
0h							
7	6	5	4	3	2	1	0
BASE_ADDRESS							
R/W							
0h							

Access Types Legend

Table 3-908. TX_BUF_BASE_N Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	BASE_ADDRESS	R/W	0h	Transmit Data Buffer Base Address This is the base address of the 16-word data buffer used by the transmitter. Reset Source: fsi_tx_rst_mod_g_rst_n

3.12.24 Access Table

Table 3-909. Access Type Codes

Access Type	Code	Description
W	W	Write
R	R	Read
R/W	R/W	Read / Write

3.13 GLOBAL_CTRL Registers

Table 3-910. MEM, MEM Registers, Base Address=0X00000000502F0000, Length=4096

Offset	Length	Register Name	CONTROLSS_CTRL Physical Address
0h	32	PID	502F 0000h
4h	32	epwm_staticxbar_sel0	502F 0004h
8h	32	epwm_staticxbar_sel1	502F 0008h
10h	32	epwm_clksync	502F 0010h
18h	32	sdfm1_clk0_sel	502F 0018h
20h	32	emustopn_mask	502F 0020h
28h	32	clb_aq_en0	502F 0028h
30h	32	clb_aq_en1	502F 0030h
38h	32	clb_db_en0	502F 0038h
40h	32	clb_db_en1	502F 0040h
44h	32	ADCSOCFRCGBSEL	502F 0044h
48h	32	ADCSOCFRCGB	502F 0048h
50h	32	XBAR_LOOPBACK_CTRL	502F 0050h
60h	32	EPWM_SOCA_SEL	502F 0060h
64h	32	EPWM_SOCB_SEL	502F 0064h
70h	32	ADCEXTCHXBar0_G0_SEL	502F 0070h
100h	32	etpwm0_clk_gate	502F 0100h
104h	32	etpwm1_clk_gate	502F 0104h
108h	32	etpwm2_clk_gate	502F 0108h
10Ch	32	etpwm3_clk_gate	502F 010Ch
110h	32	etpwm4_clk_gate	502F 0110h
114h	32	etpwm5_clk_gate	502F 0114h
118h	32	etpwm6_clk_gate	502F 0118h
11Ch	32	etpwm7_clk_gate	502F 011Ch
120h	32	etpwm8_clk_gate	502F 0120h
124h	32	etpwm9_clk_gate	502F 0124h
128h	32	etpwm10_clk_gate	502F 0128h
12Ch	32	etpwm11_clk_gate	502F 012Ch
130h	32	etpwm12_clk_gate	502F 0130h
134h	32	etpwm13_clk_gate	502F 0134h
138h	32	etpwm14_clk_gate	502F 0138h
13Ch	32	etpwm15_clk_gate	502F 013Ch
140h	32	etpwm16_clk_gate	502F 0140h
144h	32	etpwm17_clk_gate	502F 0144h
148h	32	etpwm18_clk_gate	502F 0148h
14Ch	32	etpwm19_clk_gate	502F 014Ch
150h	32	etpwm20_clk_gate	502F 0150h
154h	32	etpwm21_clk_gate	502F 0154h
158h	32	etpwm22_clk_gate	502F 0158h
15Ch	32	etpwm23_clk_gate	502F 015Ch
160h	32	etpwm24_clk_gate	502F 0160h
164h	32	etpwm25_clk_gate	502F 0164h
168h	32	etpwm26_clk_gate	502F 0168h
16Ch	32	etpwm27_clk_gate	502F 016Ch
170h	32	etpwm28_clk_gate	502F 0170h

Table 3-910. MEM, MEM Registers, Base Address=0X00000000502F0000, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_CTRL Physical Address
174h	32	etpwm29_clk_gate	502F 0174h
178h	32	etpwm30_clk_gate	502F 0178h
17Ch	32	etpwm31_clk_gate	502F 017Ch
180h	32	fsi_tx0_clk_gate	502F 0180h
184h	32	fsi_tx1_clk_gate	502F 0184h
188h	32	fsi_tx2_clk_gate	502F 0188h
18Ch	32	fsi_tx3_clk_gate	502F 018Ch
190h	32	fsi_rx0_clk_gate	502F 0190h
194h	32	fsi_rx1_clk_gate	502F 0194h
198h	32	fsi_rx2_clk_gate	502F 0198h
19Ch	32	fsi_rx3_clk_gate	502F 019Ch
1A0h	32	cmpss12b0_clk_gate	502F 01A0h
1D0h	32	cmpss8b0_clk_gate	502F 01D0h
200h	32	ecap0_clk_gate	502F 0200h
204h	32	ecap1_clk_gate	502F 0204h
208h	32	ecap2_clk_gate	502F 0208h
20Ch	32	ecap3_clk_gate	502F 020Ch
210h	32	ecap4_clk_gate	502F 0210h
214h	32	ecap5_clk_gate	502F 0214h
218h	32	ecap6_clk_gate	502F 0218h
21Ch	32	ecap7_clk_gate	502F 021Ch
220h	32	ecap8_clk_gate	502F 0220h
224h	32	ecap9_clk_gate	502F 0224h
240h	32	eqep0_clk_gate	502F 0240h
244h	32	eqep1_clk_gate	502F 0244h
248h	32	eqep2_clk_gate	502F 0248h
250h	32	sdfm0_clk_gate	502F 0250h
254h	32	sdfm1_clk_gate	502F 0254h
258h	32	dac_clk_gate	502F 0258h
25Ch	32	adc0_clk_gate	502F 025Ch
260h	32	adc1_clk_gate	502F 0260h
264h	32	adc2_clk_gate	502F 0264h
268h	32	adc3_clk_gate	502F 0268h
26Ch	32	adc4_clk_gate	502F 026Ch
270h	32	otto0_clk_gate	502F 0270h
274h	32	otto1_clk_gate	502F 0274h
278h	32	otto2_clk_gate	502F 0278h
27Ch	32	otto3_clk_gate	502F 027Ch
280h	32	sdfm0_pll_clk_gate	502F 0280h
284h	32	sdfm1_pll_clk_gate	502F 0284h
288h	32	fsi_tx0_pll_clk_gate	502F 0288h
28Ch	32	fsi_tx1_pll_clk_gate	502F 028Ch
290h	32	fsi_tx2_pll_clk_gate	502F 0290h
294h	32	fsi_tx3_pll_clk_gate	502F 0294h
29Ch	32	adc_sctile0_clk_gate	502F 029Ch
300h	32	etpwm0_rst	502F 0300h
304h	32	etpwm1_rst	502F 0304h

Table 3-910. MEM, MEM Registers, Base Address=0X00000000502F0000, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_CTRL Physical Address
308h	32	etpwm2_rst	502F 0308h
30Ch	32	etpwm3_rst	502F 030Ch
310h	32	etpwm4_rst	502F 0310h
314h	32	etpwm5_rst	502F 0314h
318h	32	etpwm6_rst	502F 0318h
31Ch	32	etpwm7_rst	502F 031Ch
320h	32	etpwm8_rst	502F 0320h
324h	32	etpwm9_rst	502F 0324h
328h	32	etpwm10_rst	502F 0328h
32Ch	32	etpwm11_rst	502F 032Ch
330h	32	etpwm12_rst	502F 0330h
334h	32	etpwm13_rst	502F 0334h
338h	32	etpwm14_rst	502F 0338h
33Ch	32	etpwm15_rst	502F 033Ch
340h	32	etpwm16_rst	502F 0340h
344h	32	etpwm17_rst	502F 0344h
348h	32	etpwm18_rst	502F 0348h
34Ch	32	etpwm19_rst	502F 034Ch
350h	32	etpwm20_rst	502F 0350h
354h	32	etpwm21_rst	502F 0354h
358h	32	etpwm22_rst	502F 0358h
35Ch	32	etpwm23_rst	502F 035Ch
360h	32	etpwm24_rst	502F 0360h
364h	32	etpwm25_rst	502F 0364h
368h	32	etpwm26_rst	502F 0368h
36Ch	32	etpwm27_rst	502F 036Ch
370h	32	etpwm28_rst	502F 0370h
374h	32	etpwm29_rst	502F 0374h
378h	32	etpwm30_rst	502F 0378h
37Ch	32	etpwm31_rst	502F 037Ch
380h	32	fsi_tx0_rst	502F 0380h
384h	32	fsi_tx1_rst	502F 0384h
388h	32	fsi_tx2_rst	502F 0388h
38Ch	32	fsi_tx3_rst	502F 038Ch
390h	32	fsi_rx0_rst	502F 0390h
394h	32	fsi_rx1_rst	502F 0394h
398h	32	fsi_rx2_rst	502F 0398h
39Ch	32	fsi_rx3_rst	502F 039Ch
3A0h	32	cmpss12b0_rst	502F 03A0h
3D0h	32	cmpss8b0_rst	502F 03D0h
400h	32	ecap0_rst	502F 0400h
404h	32	ecap1_rst	502F 0404h
408h	32	ecap2_rst	502F 0408h
40Ch	32	ecap3_rst	502F 040Ch
410h	32	ecap4_rst	502F 0410h
414h	32	ecap5_rst	502F 0414h
418h	32	ecap6_rst	502F 0418h

Table 3-910. MEM, MEM Registers, Base Address=0X00000000502F0000, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_CTRL Physical Address
41Ch	32	ecap7_rst	502F 041Ch
420h	32	ecap8_rst	502F 0420h
424h	32	ecap9_rst	502F 0424h
440h	32	eqep0_rst	502F 0440h
444h	32	eqep1_rst	502F 0444h
448h	32	eqep2_rst	502F 0448h
450h	32	sdfm0_rst	502F 0450h
454h	32	sdfm1_rst	502F 0454h
458h	32	dac_rst	502F 0458h
45Ch	32	adc0_rst	502F 045Ch
460h	32	adc1_rst	502F 0460h
464h	32	adc2_rst	502F 0464h
468h	32	adc3_rst	502F 0468h
46Ch	32	adc4_rst	502F 046Ch
470h	32	otto0_rst	502F 0470h
474h	32	otto1_rst	502F 0474h
478h	32	otto2_rst	502F 0478h
47Ch	32	otto3_rst	502F 047Ch
484h	32	adc_sctile0_rst	502F 0484h
500h	32	epwm0_halten	502F 0500h
504h	32	epwm1_halten	502F 0504h
508h	32	epwm2_halten	502F 0508h
50Ch	32	epwm3_halten	502F 050Ch
510h	32	epwm4_halten	502F 0510h
514h	32	epwm5_halten	502F 0514h
518h	32	epwm6_halten	502F 0518h
51Ch	32	epwm7_halten	502F 051Ch
520h	32	epwm8_halten	502F 0520h
524h	32	epwm9_halten	502F 0524h
528h	32	epwm10_halten	502F 0528h
52Ch	32	epwm11_halten	502F 052Ch
530h	32	epwm12_halten	502F 0530h
534h	32	epwm13_halten	502F 0534h
538h	32	epwm14_halten	502F 0538h
53Ch	32	epwm15_halten	502F 053Ch
540h	32	epwm16_halten	502F 0540h
544h	32	epwm17_halten	502F 0544h
548h	32	epwm18_halten	502F 0548h
54Ch	32	epwm19_halten	502F 054Ch
550h	32	epwm20_halten	502F 0550h
554h	32	epwm21_halten	502F 0554h
558h	32	epwm22_halten	502F 0558h
55Ch	32	epwm23_halten	502F 055Ch
560h	32	epwm24_halten	502F 0560h
564h	32	epwm25_halten	502F 0564h
568h	32	epwm26_halten	502F 0568h
56Ch	32	epwm27_halten	502F 056Ch

Table 3-910. MEM, MEM Registers, Base Address=0X00000000502F0000, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_CTRL Physical Address
570h	32	epwm28_halten	502F 0570h
574h	32	epwm29_halten	502F 0574h
578h	32	epwm30_halten	502F 0578h
57Ch	32	epwm31_halten	502F 057Ch
5D0h	32	ecap0_halten	502F 05D0h
5D4h	32	ecap1_halten	502F 05D4h
5D8h	32	ecap2_halten	502F 05D8h
5DCh	32	ecap3_halten	502F 05DCh
5E0h	32	ecap4_halten	502F 05E0h
5E4h	32	ecap5_halten	502F 05E4h
5E8h	32	ecap6_halten	502F 05E8h
5ECh	32	ecap7_halten	502F 05ECh
5F0h	32	ecap8_halten	502F 05F0h
5F4h	32	ecap9_halten	502F 05F4h
5F8h	32	eqep0_halten	502F 05F8h
5FCh	32	eqep1_halten	502F 05FCh
600h	32	eqep2_halten	502F 0600h
1008h	32	LOCK0_KICK0	502F 1008h
100Ch	32	LOCK0_KICK1	502F 100Ch
1010h	32	intr_raw_status	502F 1010h
1014h	32	intr_enabled_status_clear	502F 1014h
1018h	32	intr_enable	502F 1018h
101Ch	32	intr_enable_clear	502F 101Ch
1020h	32	eoi	502F 1020h
1024h	32	fault_address	502F 1024h
1028h	32	fault_type_status	502F 1028h
102Ch	32	fault_attr_status	502F 102Ch
1030h	32	fault_clear	502F 1030h

3.13.1 MEM_PID Registers

3.13.1.1 MEM_PID Register (Offset = 0h) [reset = 61800214h]

Short Description: PID register

Long Description: PID register

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Table 3-911. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0000h

Figure 3-397. PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PID_MSB16															
R															
6180h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_MISC					PID_MAJOR			PID_CUSTOM		PID_MINOR					
R					R			R		R					
0h					2h			0h		14h					

Access Types Legend

Table 3-912. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16	R	6180h	Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
15:11	PID_MISC	R	0h	Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
10:8	PID_MAJOR	R	2h	Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
7:6	PID_CUSTOM	R	0h	Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
5:0	PID_MINOR	R	14h	Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.2 MEM_EPWM_STATICXBAR_SEL0 Registers

3.13.2.1 MEM_STATICXBAR_SEL0 Register (Offset = 4h) [reset = 0h]

Short Description:

Long Description:

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Table 3-913. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0004h

Figure 3-398. EPWM_STATICXBAR_SEL0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EPWM_STATICXBAR_SEL0_ETPWM15		EPWM_STATICXBAR_SEL0_ETPWM14		EPWM_STATICXBAR_SEL0_ETPWM13		EPWM_STATICXBAR_SEL0_ETPWM12		EPWM_STATICXBAR_SEL0_ETPWM11		EPWM_STATICXBAR_SEL0_ETPWM10		EPWM_STATICXBAR_SEL0_ETPWM9		EPWM_STATICXBAR_SEL0_ETPWM8	
R/W		R/W		R/W		R/W		R/W		R/W		R/W		R/W	
0h		0h		0h		0h		0h		0h		0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EPWM_STATICXBAR_SEL0_ETPWM7		EPWM_STATICXBAR_SEL0_ETPWM6		EPWM_STATICXBAR_SEL0_ETPWM5		EPWM_STATICXBAR_SEL0_ETPWM4		EPWM_STATICXBAR_SEL0_ETPWM3		EPWM_STATICXBAR_SEL0_ETPWM2		EPWM_STATICXBAR_SEL0_ETPWM1		EPWM_STATICXBAR_SEL0_ETPWM0	
R/W		R/W		R/W		R/W		R/W		R/W		R/W		R/W	
0h		0h		0h		0h		0h		0h		0h		0h	

Access Types Legend

Table 3-914. EPWM_STATICXBAR_SEL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	EPWM_STATICXBAR_SEL0_ETPWM15	R/W	0h	ETPWM15 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
29:28	EPWM_STATICXBAR_SEL0_ETPWM14	R/W	0h	ETPWM14 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
27:26	EPWM_STATICXBAR_SEL0_ETPWM13	R/W	0h	ETPWM13 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
25:24	EPWM_STATICXBAR_SEL0_ETPWM12	R/W	0h	ETPWM12 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
23:22	EPWM_STATICXBAR_SEL0_ETPWM11	R/W	0h	ETPWM11 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
21:20	EPWM_STATICXBAR_SEL0_ETPWM10	R/W	0h	ETPWM10 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
19:18	EPWM_STATICXBAR_SEL0_ETPWM9	R/W	0h	ETPWM9 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
17:16	EPWM_STATICXBAR_SEL0_ETPWM8	R/W	0h	ETPWM8 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
15:14	EPWM_STATICXBAR_SEL0_ETPWM7	R/W	0h	ETPWM7 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

Table 3-914. EPWM_STATICXBAR_SEL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:12	EPWM_STATICXBAR_SEL0_ETPWM6	R/W	0h	ETPWM6 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
11:10	EPWM_STATICXBAR_SEL0_ETPWM5	R/W	0h	ETPWM5 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
9:8	EPWM_STATICXBAR_SEL0_ETPWM4	R/W	0h	ETPWM4 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
7:6	EPWM_STATICXBAR_SEL0_ETPWM3	R/W	0h	ETPWM3 access from PCR grouping. Write the following value to access groups - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
5:4	EPWM_STATICXBAR_SEL0_ETPWM2	R/W	0h	ETPWM2 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
3:2	EPWM_STATICXBAR_SEL0_ETPWM1	R/W	0h	ETPWM1 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1:0	EPWM_STATICXBAR_SEL0_ETPWM0	R/W	0h	ETPWM0 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.3 MEM_EPWM_STATICXBAR_SEL1 Registers

3.13.3.1 MEM_STATICXBAR_SEL1 Register (Offset = 8h) [reset = 0h]

Short Description:

Long Description:

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Table 3-915. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0008h

Figure 3-399. EPWM_STATICXBAR_SEL1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EPWM_STATICXBAR_SEL1_ETPWM31		EPWM_STATICXBAR_SEL1_ETPWM30		EPWM_STATICXBAR_SEL1_ETPWM29		EPWM_STATICXBAR_SEL1_ETPWM28		EPWM_STATICXBAR_SEL1_ETPWM27		EPWM_STATICXBAR_SEL1_ETPWM26		EPWM_STATICXBAR_SEL1_ETPWM25		EPWM_STATICXBAR_SEL1_ETPWM24	
R/W		R/W		R/W		R/W		R/W		R/W		R/W		R/W	
0h		0h		0h		0h		0h		0h		0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EPWM_STATICXBAR_SEL1_ETPWM23		EPWM_STATICXBAR_SEL1_ETPWM22		EPWM_STATICXBAR_SEL1_ETPWM21		EPWM_STATICXBAR_SEL1_ETPWM20		EPWM_STATICXBAR_SEL1_ETPWM19		EPWM_STATICXBAR_SEL1_ETPWM18		EPWM_STATICXBAR_SEL1_ETPWM17		EPWM_STATICXBAR_SEL1_ETPWM16	
R/W		R/W		R/W		R/W		R/W		R/W		R/W		R/W	
0h		0h		0h		0h		0h		0h		0h		0h	

Access Types Legend

Table 3-916. EPWM_STATICXBAR_SEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	EPWM_STATICXBAR_SEL1_ETPWM31	R/W	0h	ETPWM31 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
29:28	EPWM_STATICXBAR_SEL1_ETPWM30	R/W	0h	ETPWM30 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
27:26	EPWM_STATICXBAR_SEL1_ETPWM29	R/W	0h	ETPWM29 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
25:24	EPWM_STATICXBAR_SEL1_ETPWM28	R/W	0h	ETPWM28 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
23:22	EPWM_STATICXBAR_SEL1_ETPWM27	R/W	0h	ETPWM27 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
21:20	EPWM_STATICXBAR_SEL1_ETPWM26	R/W	0h	ETPWM26 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
19:18	EPWM_STATICXBAR_SEL1_ETPWM25	R/W	0h	ETPWM25 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
17:16	EPWM_STATICXBAR_SEL1_ETPWM24	R/W	0h	ETPWM24 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
15:14	EPWM_STATICXBAR_SEL1_ETPWM23	R/W	0h	ETPWM23 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

Table 3-916. EPWM_STATICXBAR_SEL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:12	EPWM_STATICXBAR_SEL1_ETPWM22	R/W	0h	ETPWM22 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
11:10	EPWM_STATICXBAR_SEL1_ETPWM21	R/W	0h	ETPWM21 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
9:8	EPWM_STATICXBAR_SEL1_ETPWM20	R/W	0h	ETPWM20 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
7:6	EPWM_STATICXBAR_SEL1_ETPWM19	R/W	0h	ETPWM19 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
5:4	EPWM_STATICXBAR_SEL1_ETPWM18	R/W	0h	ETPWM18 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
3:2	EPWM_STATICXBAR_SEL1_ETPWM17	R/W	0h	ETPWM17 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1:0	EPWM_STATICXBAR_SEL1_ETPWM16	R/W	0h	ETPWM16 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.4 MEM_EPWM_CLKSYNC Registers

3.13.4.1 MEM_CLKSYNC Register (Offset = 10h) [reset = 0h]

Short Description:

Long Description:

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Table 3-917. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0010h

Figure 3-400. EPWM_CLKSYNC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EPWM_CLKSYNC_BIT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EPWM_CLKSYNC_BIT															
R/W															
0h															

Access Types Legend

Table 3-918. EPWM_CLKSYNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EPWM_CLKSYNC_BIT	R/W	0h	ETPWM clock sync for each EPWM instance. Set the bit corresponding to the instance number to enable that EPWM instance. When set, all enabled EPWM module clocks are started with the first rising edge of TBCLK aligned.Refer to TRM for more details. Writing 1'b1 will allow to enable corresponding EPWM instance Writing 1'b0 will disable corresponding EPWM instance. Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.5 MEM_SDFM1_CLK0_SEL Registers

3.13.5.1 MEM_CLK0_SEL Register (Offset = 18h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-919. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0018h

Figure 3-401. SDFM1_CLK0_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															SDFM1_CLK0_SEL_SEL
NONE															R/W
0															0h

Access Types Legend

Table 3-920. SDFM1_CLK0_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	SDFM1_CLK0_SEL_SEL	R/W	0h	SDFM1 clock CK0 select Write 1'b0: source is SDFM1 CK0 from Pinmux Write 1'b1: source is SDFM0 CK0 from Pinmux Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.6 MEM_EMUSTOPN_MASK Registers

3.13.6.1 MEM_MASK Register (Offset = 20h) [reset = 0h]

Short Description:

Long Description:

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Table 3-921. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0020h

Figure 3-402. EMUSTOPN_MASK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EMUSTOPN_MASK_CR5B1	EMUSTOPN_MASK_CR5A1	EMUSTOPN_MASK_CR5B0	EMUSTOPN_MASK_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-922. EMUSTOPN_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EMUSTOPN_MASK_CR5B1	R/W	0h	Bit-mask for debug suspend cpu cores to EPWM 1'b0 : CR5B1 enabled to control EMUSTOPn 1'b1 : CR5B1 disabled to control EMUSTOPn Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EMUSTOPN_MASK_CR5A1	R/W	0h	Bit-mask for debug suspend cpu cores to EPWM 1'b0 : CR5A1 enabled to control EMUSTOPn 1'b1 : CR5A1 disabled to control EMUSTOPn Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EMUSTOPN_MASK_CR5B0	R/W	0h	Bit-mask for debug suspend cpu cores to EPWM 1'b0 : CR5B0 enabled to control EMUSTOPn 1'b1 : CR5B0 disabled to control EMUSTOPn Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EMUSTOPN_MASK_CR5A0	R/W	0h	Bit-mask for debug suspend cpu cores to EPWM 1'b0 : CR5A0 enabled to control EMUSTOPn 1'b1 : CR5A0 disabled to control EMUSTOPn Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.7 MEM_CLB_AQ_EN0 Registers

3.13.7.1 MEM_AQ_EN0 Register (Offset = 28h) [reset = 0h]

Short Description:

Long Description:

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Table 3-923. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0028h

Figure 3-403. CLB_AQ_EN0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLB_AQ_EN0_ENABLE															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLB_AQ_EN0_ENABLE															
R/W															
0h															

Access Types Legend

Table 3-924. CLB_AQ_EN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLB_AQ_EN0_ENABLE	R/W	0h	Enable ICCS control to CLB_AQ signal of PWM[15:0]. Set Bitx to 1'b1 to enable it for PWMx. Here x varies from 0-15. Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.8 MEM_CLB_AQ_EN1 Registers

3.13.8.1 MEM_AQ_EN1 Register (Offset = 30h) [reset = 0h]

Short Description:

Long Description:

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Table 3-925. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0030h

Figure 3-404. CLB_AQ_EN1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLB_AQ_EN1_ENABLE															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLB_AQ_EN1_ENABLE															
R/W															
0h															

Access Types Legend

Table 3-926. CLB_AQ_EN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLB_AQ_EN1_ENABLE	R/W	0h	Enable ICCS control to CLB_AQ signal of PWM[31:16].Set Bitx to 1'b1 to enable it for PWMx. Here x varies from 16-31. Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.9 MEM_CLB_DB_EN0 Registers

3.13.9.1 MEM_DB_EN0 Register (Offset = 38h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-927. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0038h

Figure 3-405. CLB_DB_EN0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLB_DB_EN0_ENABLE															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLB_DB_EN0_ENABLE															
R/W															
0h															

Access Types Legend

Table 3-928. CLB_DB_EN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLB_DB_EN0_ENABLE	R/W	0h	Enable ICCS control to CLB_DB signal of PWM[15:0]. Set Bitx to 1'b1 to enable it for PWMx. Here x varies from 0-15. Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.10 MEM_CLB_DB_EN1 Registers

3.13.10.1 MEM_DB_EN1 Register (Offset = 40h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-929. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0040h

Figure 3-406. CLB_DB_EN1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLB_DB_EN1_ENABLE															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLB_DB_EN1_ENABLE															
R/W															
0h															

Access Types Legend

Table 3-930. CLB_DB_EN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLB_DB_EN1_ENABLE	R/W	0h	Enable ICCS control to CLB_DB signal of PWM[31:16].Set Bitx to 1'b1 to enable it for PWMx. Here x varies from 16-31. Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.11 MEM_ADCSOCFRCGBSEL Registers

3.13.11.1 MEM_ADCSOCFRCGBSEL Register (Offset = 44h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-931. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0044h

Figure 3-407. ADCSOCFRCGBSEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									ADCSOCFRCGBSEL_ENABLE						
NONE									R/W						
0									0h						

Access Types Legend

Table 3-932. ADCSOCFRCGBSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE		Reserved
6:0	ADCSOCFRCGBSEL_ENABLE	R/W	0h	ADCSOCFRCGBSEL has one bit for each ADC BIT FIELD Description bitx ADCx Indicate if ADCx selected for global SW trigger 1b'0 : Not selected for Global SW Trigger 1b'1 : Selected for Global SW TriggerReset Reset type: SYSRSn Note: x represents 0-4 Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.12 MEM_ADCSOCFRCGB Registers

3.13.12.1 MEM_ADCSOCFRCGB Register (Offset = 48h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-933. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0048h

Figure 3-408. ADCSOCFRCGB Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADCSOCFRCGB_TRIG															
R/W															
0h															

Access Types Legend

Table 3-934. ADCSOCFRCGB Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	ADCSOCFRCGB_TRIG	R/W	0h	ADCSOCFRCGB has one bit for each SOC[Start of conversion] BIT FIELD Description bitxx SOCxx Indicate if SOCxx selected for global SW trigger 1b'0 : Not selected for Global SW Trigger 1b'1 : Selected for Global SW Trigger Reset type: SYSRSn Note: xx represents 0-15 Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.13 MEM_XBAR_LOOPBACK_CTRL Registers

3.13.13.1 MEM_LOOPBACK_CTRL Register (Offset = 50h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-935. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0050h

Figure 3-409. XBAR_LOOPBACK_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XBAR_LOOPBACK_CTRL_ENABLE															
R/W															
0h															

Access Types Legend

Table 3-936. XBAR_LOOPBACK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	XBAR_LOOPBACK_CTRL_ENABLE	R/W	0h	Mux select to enable Loopback for corresponding outputxbar signal to the inputxbar Write 1'b0: Loopback disabled [default] Write 1'b1: Loopback enable **Note: Each Mux select bit corresponds to the corresponding XBAR_LOOPBACK_CTRL_MUX Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.14 MEM_EPWM_SOCA_SEL Registers

3.13.14.1 MEM_SOCA_SEL Register (Offset = 60h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-937. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0060h

Figure 3-410. EPWM_SOCA_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EPWM_SOCA_SEL_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EPWM_SOCA_SEL_SEL															
R/W															
0h															

Access Types Legend

Table 3-938. EPWM_SOCA_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EPWM_SOCA_SEL_SEL	R/W	0h	MUX select to choose EPWM SOC A to EQEPx.SOCA and PWMBAR. Each bit in SOC_A_SEL corresponds to each input EPWM_SOCA_SELundefined:pwm_socaundefined Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.15 MEM_EPWM_SOCB_SEL Registers

3.13.15.1 MEM_SOCB_SEL Register (Offset = 64h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-939. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0064h

Figure 3-411. EPWM_SOCB_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EPWM_SOCB_SEL_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EPWM_SOCB_SEL_SEL															
R/W															
0h															

Access Types Legend

Table 3-940. EPWM_SOCB_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EPWM_SOCB_SEL_SEL	R/W	0h	MUX select to choose EPWM SOC B to EQEPx.SOCB and PWMBAR. Each bit in SOC_B_SEL corresponds to each input EPWM_SOCB_SELundefined:pwm_socbundefined Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.16 MEM_ADCEXTCHXBAR0_G0_SEL Registers

3.13.16.1 MEM_G0_SEL Register (Offset = 70h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-941. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0070h

Figure 3-412. ADCEXTCHXBAR0_G0_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												ADCEXTCHXBAR0_G0_SEL_SEL			
NONE												R/W			
0												0h			

Access Types Legend

Table 3-942. ADCEXTCHXBAR0_G0_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:0	ADCEXTCHXBAR0_G0_SEL_SEL	R/W	0h	ADC EXTCH XBar 0 Input Select 4'b0000: ADC0EXTCHSEL_BIT0 4'b0001: ADC0EXTCHSEL_BIT1 4'b0010: ADC1EXTCHSEL_BIT0 4'b0011: ADC1EXTCHSEL_BIT1 4'b0100: ADC2EXTCHSEL_BIT0 4'b0101: ADC2EXTCHSEL_BIT1 4'b0110: ADC3EXTCHSEL_BIT0 4'b0111: ADC3EXTCHSEL_BIT1 4'b1000: ADC4EXTCHSEL_BIT0 4'b1001: ADC4EXTCHSEL_BIT1 4'b1010: Example: ADC2EXTCHSEL_BIT0 needs to be connect to ADC_EXTCH_XBAROUT3, then ADCEXTCHXBar3.G0.SEL set to 4'b0100 Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.17 MEM_ETPWM0_CLK_GATE Registers

3.13.17.1 MEM_CLK_GATE Register (Offset = 100h) [reset = 0h]

Short Description:

Long Description:

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Table 3-943. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0100h

Figure 3-413. ETPWM0_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM0_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-944. ETPWM0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM0_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.18 MEM_ETPWM1_CLK_GATE Registers

3.13.18.1 MEM_CLK_GATE Register (Offset = 104h) [reset = 0h]

Short Description:

Long Description:

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Table 3-945. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0104h

Figure 3-414. ETPWM1_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM1_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-946. ETPWM1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM1_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.19 MEM_ETPWM2_CLK_GATE Registers

3.13.19.1 MEM_CLK_GATE Register (Offset = 108h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-947. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0108h

Figure 3-415. ETPWM2_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM2_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-948. ETPWM2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM2_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.20 MEM_ETPWM3_CLK_GATE Registers

3.13.20.1 MEM_CLK_GATE Register (Offset = 10Ch) [reset = 0h]

Short Description:

Long Description:

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Table 3-949. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 010Ch

Figure 3-416. ETPWM3_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM3_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-950. ETPWM3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM3_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.21 MEM_ETPWM4_CLK_GATE Registers

3.13.21.1 MEM_CLK_GATE Register (Offset = 110h) [reset = 0h]

Short Description:

Long Description:

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Table 3-951. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0110h

Figure 3-417. ETPWM4_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM4_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-952. ETPWM4_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM4_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.22 MEM_ETPWM5_CLK_GATE Registers

3.13.22.1 MEM_CLK_GATE Register (Offset = 114h) [reset = 0h]

Short Description:

Long Description:

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Table 3-953. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0114h

Figure 3-418. ETPWM5_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM5_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-954. ETPWM5_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM5_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.23 MEM_ETPWM6_CLK_GATE Registers

3.13.23.1 MEM_CLK_GATE Register (Offset = 118h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-955. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0118h

Figure 3-419. ETPWM6_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM6_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-956. ETPWM6_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM6_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.24 MEM_ETPWM7_CLK_GATE Registers

3.13.24.1 MEM_CLK_GATE Register (Offset = 11Ch) [reset = 0h]

Short Description:

Long Description:

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Table 3-957. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 011Ch

Figure 3-420. ETPWM7_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM7_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-958. ETPWM7_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM7_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.25 MEM_ETPWM8_CLK_GATE Registers

3.13.25.1 MEM_CLK_GATE Register (Offset = 120h) [reset = 0h]

Short Description:

Long Description:

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Table 3-959. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0120h

Figure 3-421. ETPWM8_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM8_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-960. ETPWM8_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM8_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.26 MEM_ETPWM9_CLK_GATE Registers

3.13.26.1 MEM_CLK_GATE Register (Offset = 124h) [reset = 0h]

Short Description:

Long Description:

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Table 3-961. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0124h

Figure 3-422. ETPWM9_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM9_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-962. ETPWM9_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM9_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.27 MEM_ETPWM10_CLK_GATE Registers

3.13.27.1 MEM_CLK_GATE Register (Offset = 128h) [reset = 0h]

Short Description:

Long Description:

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Table 3-963. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0128h

Figure 3-423. ETPWM10_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM10_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-964. ETPWM10_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM10_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.28 MEM_ETPWM11_CLK_GATE Registers

3.13.28.1 MEM_CLK_GATE Register (Offset = 12Ch) [reset = 0h]

Short Description:

Long Description:

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Table 3-965. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 012Ch

Figure 3-424. ETPWM11_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM11_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-966. ETPWM11_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM11_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.29 MEM_ETPWM12_CLK_GATE Registers

3.13.29.1 MEM_CLK_GATE Register (Offset = 130h) [reset = 0h]

Short Description:

Long Description:

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Table 3-967. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0130h

Figure 3-425. ETPWM12_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM12_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-968. ETPWM12_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM12_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.30 MEM_ETPWM13_CLK_GATE Registers

3.13.30.1 MEM_CLK_GATE Register (Offset = 134h) [reset = 0h]

Short Description:

Long Description:

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Table 3-969. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0134h

Figure 3-426. ETPWM13_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM13_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-970. ETPWM13_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM13_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.31 MEM_ETPWM14_CLK_GATE Registers

3.13.31.1 MEM_CLK_GATE Register (Offset = 138h) [reset = 0h]

Short Description:

Long Description:

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Table 3-971. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0138h

Figure 3-427. ETPWM14_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM14_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-972. ETPWM14_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM14_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.32 MEM_ETPWM15_CLK_GATE Registers

3.13.32.1 MEM_CLK_GATE Register (Offset = 13Ch) [reset = 0h]

Short Description:

Long Description:

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Table 3-973. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 013Ch

Figure 3-428. ETPWM15_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM15_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-974. ETPWM15_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM15_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.33 MEM_ETPWM16_CLK_GATE Registers

3.13.33.1 MEM_CLK_GATE Register (Offset = 140h) [reset = 0h]

Short Description:

Long Description:

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Table 3-975. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0140h

Figure 3-429. ETPWM16_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM16_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-976. ETPWM16_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM16_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.34 MEM_ETPWM17_CLK_GATE Registers

3.13.34.1 MEM_CLK_GATE Register (Offset = 144h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-977. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0144h

Figure 3-430. ETPWM17_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM17_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-978. ETPWM17_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM17_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.35 MEM_ETPWM18_CLK_GATE Registers

3.13.35.1 MEM_CLK_GATE Register (Offset = 148h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-979. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0148h

Figure 3-431. ETPWM18_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM18_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-980. ETPWM18_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM18_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.36 MEM_ETPWM19_CLK_GATE Registers

3.13.36.1 MEM_CLK_GATE Register (Offset = 14Ch) [reset = 0h]

Short Description:

Long Description:

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Table 3-981. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 014Ch

Figure 3-432. ETPWM19_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM19_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-982. ETPWM19_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM19_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.37 MEM_ETPWM20_CLK_GATE Registers

3.13.37.1 MEM_CLK_GATE Register (Offset = 150h) [reset = 0h]

Short Description:

Long Description:

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Table 3-983. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0150h

Figure 3-433. ETPWM20_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM20_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-984. ETPWM20_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM20_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.38 MEM_ETPWM21_CLK_GATE Registers

3.13.38.1 MEM_CLK_GATE Register (Offset = 154h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-985. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0154h

Figure 3-434. ETPWM21_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM21_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-986. ETPWM21_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM21_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.39 MEM_ETPWM22_CLK_GATE Registers

3.13.39.1 MEM_CLK_GATE Register (Offset = 158h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-987. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0158h

Figure 3-435. ETPWM22_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM22_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-988. ETPWM22_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM22_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.40 MEM_ETPWM23_CLK_GATE Registers

3.13.40.1 MEM_CLK_GATE Register (Offset = 15Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-989. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 015Ch

Figure 3-436. ETPWM23_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM23_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-990. ETPWM23_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM23_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.41 MEM_ETPWM24_CLK_GATE Registers

3.13.41.1 MEM_CLK_GATE Register (Offset = 160h) [reset = 0h]

Short Description:

Long Description:

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Table 3-991. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0160h

Figure 3-437. ETPWM24_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM24_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-992. ETPWM24_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM24_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.42 MEM_ETPWM25_CLK_GATE Registers

3.13.42.1 MEM_CLK_GATE Register (Offset = 164h) [reset = 0h]

Short Description:

Long Description:

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Table 3-993. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0164h

Figure 3-438. ETPWM25_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM25_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-994. ETPWM25_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM25_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.43 MEM_ETPWM26_CLK_GATE Registers

3.13.43.1 MEM_CLK_GATE Register (Offset = 168h) [reset = 0h]

Short Description:

Long Description:

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Table 3-995. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0168h

Figure 3-439. ETPWM26_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM26_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-996. ETPWM26_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM26_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.44 MEM_ETPWM27_CLK_GATE Registers

3.13.44.1 MEM_CLK_GATE Register (Offset = 16Ch) [reset = 0h]

Short Description:

Long Description:

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Table 3-997. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 016Ch

Figure 3-440. ETPWM27_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM27_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-998. ETPWM27_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM27_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.45 MEM_ETPWM28_CLK_GATE Registers

3.13.45.1 MEM_CLK_GATE Register (Offset = 170h) [reset = 0h]

Short Description:

Long Description:

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Table 3-999. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0170h

Figure 3-441. ETPWM28_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM28_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1000. ETPWM28_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM28_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.46 MEM_ETPWM29_CLK_GATE Registers

3.13.46.1 MEM_CLK_GATE Register (Offset = 174h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1001. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0174h

Figure 3-442. ETPWM29_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM29_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1002. ETPWM29_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM29_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.47 MEM_ETPWM30_CLK_GATE Registers

3.13.47.1 MEM_CLK_GATE Register (Offset = 178h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1003. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0178h

Figure 3-443. ETPWM30_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM30_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1004. ETPWM30_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM30_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.48 MEM_ETPWM31_CLK_GATE Registers

3.13.48.1 MEM_CLK_GATE Register (Offset = 17Ch) [reset = 0h]

Short Description:

Long Description:

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Table 3-1005. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 017Ch

Figure 3-444. ETPWM31_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM31_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1006. ETPWM31_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM31_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.49 MEM_FSI_TX0_CLK_GATE Registers

3.13.49.1 MEM_TX0_CLK_GATE Register (Offset = 180h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1007. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0180h

Figure 3-445. FSI_TX0_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													FSI_TX0_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1008. FSI_TX0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	FSI_TX0_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding fsi_tx Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.50 MEM_FSI_TX1_CLK_GATE Registers

3.13.50.1 MEM_TX1_CLK_GATE Register (Offset = 184h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1009. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0184h

Figure 3-446. FSI_TX1_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													FSI_TX1_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1010. FSI_TX1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	FSI_TX1_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding fsi_tx Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.51 MEM_FSI_TX2_CLK_GATE Registers

3.13.51.1 MEM_TX2_CLK_GATE Register (Offset = 188h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1011. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0188h

Figure 3-447. FSI_TX2_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													FSI_TX2_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1012. FSI_TX2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	FSI_TX2_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding fsi_tx Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.52 MEM_FSI_TX3_CLK_GATE Registers

3.13.52.1 MEM_TX3_CLK_GATE Register (Offset = 18Ch) [reset = 0h]

Short Description:

Long Description:

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Table 3-1013. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 018Ch

Figure 3-448. FSI_TX3_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													FSI_TX3_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1014. FSI_TX3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	FSI_TX3_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding fsi_tx Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.53 MEM_FSI_RX0_CLK_GATE Registers

3.13.53.1 MEM_RX0_CLK_GATE Register (Offset = 190h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1015. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0190h

Figure 3-449. FSI_RX0_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													FSI_RX0_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1016. FSI_RX0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	FSI_RX0_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding fsi_rx Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.54 MEM_FSI_RX1_CLK_GATE Registers

3.13.54.1 MEM_RX1_CLK_GATE Register (Offset = 194h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1017. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0194h

Figure 3-450. FSI_RX1_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													FSI_RX1_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1018. FSI_RX1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	FSI_RX1_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding fsi_rx Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.55 MEM_FSI_RX2_CLK_GATE Registers

3.13.55.1 MEM_RX2_CLK_GATE Register (Offset = 198h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1019. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0198h

Figure 3-451. FSI_RX2_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													FSI_RX2_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1020. FSI_RX2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	FSI_RX2_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding fsi_rx Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.56 MEM_FSI_RX3_CLK_GATE Registers

3.13.56.1 MEM_RX3_CLK_GATE Register (Offset = 19Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1021. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 019Ch

Figure 3-452. FSI_RX3_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													FSI_RX3_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1022. FSI_RX3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	FSI_RX3_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding fsi_rx Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.57 MEM_CMPSS12B0_CLK_GATE Registers

3.13.57.1 MEM_CLK_GATE Register (Offset = 1A0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1023. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01A0h

Figure 3-453. CMPSS12B0_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													CMPSS12B0_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1024. CMPSS12B0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	CMPSS12B0_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding cmpss12b Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.58 MEM_CMPSS8B0_CLK_GATE Registers

3.13.58.1 MEM_CLK_GATE Register (Offset = 1D0h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1025. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01D0h

Figure 3-454. CMPSS8B0_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													CMPSS8B0_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1026. CMPSS8B0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	CMPSS8B0_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding cmpss8b Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.59 MEM_ECAP0_CLK_GATE Registers

3.13.59.1 MEM_CLK_GATE Register (Offset = 200h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1027. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0200h

Figure 3-455. ECAP0_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ECAP0_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1028. ECAP0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ECAP0_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding ecap Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.60 MEM_ECAP1_CLK_GATE Registers

3.13.60.1 MEM_CLK_GATE Register (Offset = 204h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1029. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0204h

Figure 3-456. ECAP1_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ECAP1_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1030. ECAP1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ECAP1_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding ecap Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.61 MEM_ECAP2_CLK_GATE Registers

3.13.61.1 MEM_CLK_GATE Register (Offset = 208h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1031. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0208h

Figure 3-457. ECAP2_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ECAP2_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1032. ECAP2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ECAP2_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding ecap Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.62 MEM_ECAP3_CLK_GATE Registers

3.13.62.1 MEM_CLK_GATE Register (Offset = 20Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1033. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 020Ch

Figure 3-458. ECAP3_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ECAP3_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1034. ECAP3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ECAP3_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding ecap Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.63 MEM_ECAP4_CLK_GATE Registers

3.13.63.1 MEM_CLK_GATE Register (Offset = 210h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1035. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0210h

Figure 3-459. ECAP4_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ECAP4_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1036. ECAP4_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ECAP4_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding ecap Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.64 MEM_ECAP5_CLK_GATE Registers

3.13.64.1 MEM_CLK_GATE Register (Offset = 214h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1037. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0214h

Figure 3-460. ECAP5_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ECAP5_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1038. ECAP5_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ECAP5_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding ecap Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.65 MEM_ECAP6_CLK_GATE Registers

3.13.65.1 MEM_CLK_GATE Register (Offset = 218h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1039. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0218h

Figure 3-461. ECAP6_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ECAP6_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1040. ECAP6_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ECAP6_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding ecap Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.66 MEM_ECAP7_CLK_GATE Registers

3.13.66.1 MEM_CLK_GATE Register (Offset = 21Ch) [reset = 0h]

Short Description:

Long Description:

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Table 3-1041. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 021Ch

Figure 3-462. ECAP7_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ECAP7_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1042. ECAP7_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ECAP7_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding ecap Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.67 MEM_ECAP8_CLK_GATE Registers

3.13.67.1 MEM_CLK_GATE Register (Offset = 220h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1043. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0220h

Figure 3-463. ECAP8_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ECAP8_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1044. ECAP8_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ECAP8_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding ecap Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.68 MEM_ECAP9_CLK_GATE Registers

3.13.68.1 MEM_CLK_GATE Register (Offset = 224h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1045. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0224h

Figure 3-464. ECAP9_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ECAP9_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1046. ECAP9_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ECAP9_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding ecap Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.69 MEM_EQEP0_CLK_GATE Registers

3.13.69.1 MEM_CLK_GATE Register (Offset = 240h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1047. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0240h

Figure 3-465. EQEP0_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													EQEP0_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1048. EQEP0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	EQEP0_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding eqep Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.70 MEM_EQEP1_CLK_GATE Registers

3.13.70.1 MEM_CLK_GATE Register (Offset = 244h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1049. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0244h

Figure 3-466. EQEP1_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													EQEP1_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1050. EQEP1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	EQEP1_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding eqep Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.71 MEM_EQEP2_CLK_GATE Registers

3.13.71.1 MEM_CLK_GATE Register (Offset = 248h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1051. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0248h

Figure 3-467. EQEP2_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													EQEP2_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1052. EQEP2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	EQEP2_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding eqep Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.72 MEM_SDFM0_CLK_GATE Registers

3.13.72.1 MEM_CLK_GATE Register (Offset = 250h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1053. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0250h

Figure 3-468. SDFM0_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															SDFM0_CLK_GATE_CLK_GATE
NONE															R/W
0															0h

Access Types Legend

Table 3-1054. SDFM0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	SDFM0_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding sdfm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.73 MEM_SDFM1_CLK_GATE Registers

3.13.73.1 MEM_CLK_GATE Register (Offset = 254h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1055. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0254h

Figure 3-469. SDFM1_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													SDFM1_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1056. SDFM1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	SDFM1_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding sdfm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.74 MEM_DAC_CLK_GATE Registers

3.13.74.1 MEM_CLK_GATE Register (Offset = 258h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1057. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0258h

Figure 3-470. DAC_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													DAC_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1058. DAC_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	DAC_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for dac Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.75 MEM_ADC0_CLK_GATE Registers

3.13.75.1 MEM_CLK_GATE Register (Offset = 25Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1059. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 025Ch

Figure 3-471. ADC0_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ADC0_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1060. ADC0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ADC0_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding adc Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.76 MEM_ADC1_CLK_GATE Registers

3.13.76.1 MEM_CLK_GATE Register (Offset = 260h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1061. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0260h

Figure 3-472. ADC1_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ADC1_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1062. ADC1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ADC1_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding adc Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.77 MEM_ADC2_CLK_GATE Registers

3.13.77.1 MEM_CLK_GATE Register (Offset = 264h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1063. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0264h

Figure 3-473. ADC2_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ADC2_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1064. ADC2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ADC2_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding adc Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.78 MEM_ADC3_CLK_GATE Registers

3.13.78.1 MEM_CLK_GATE Register (Offset = 268h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1065. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0268h

Figure 3-474. ADC3_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ADC3_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1066. ADC3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ADC3_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding adc Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.79 MEM_ADC4_CLK_GATE Registers

3.13.79.1 MEM_CLK_GATE Register (Offset = 26Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1067. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 026Ch

Figure 3-475. ADC4_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ADC4_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1068. ADC4_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ADC4_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding adc Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.80 MEM_OTTO0_CLK_GATE Registers

3.13.80.1 MEM_CLK_GATE Register (Offset = 270h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1069. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0270h

Figure 3-476. OTTO0_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													OTTO0_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1070. OTTO0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	OTTO0_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding otto Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.81 MEM_OTTO1_CLK_GATE Registers

3.13.81.1 MEM_CLK_GATE Register (Offset = 274h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1071. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0274h

Figure 3-477. OTTO1_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													OTTO1_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1072. OTTO1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	OTTO1_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding otto Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.82 MEM_OTTO2_CLK_GATE Registers

3.13.82.1 MEM_CLK_GATE Register (Offset = 278h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1073. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0278h

Figure 3-478. OTTO2_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													OTTO2_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1074. OTTO2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	OTTO2_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding otto Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.83 MEM_OTTO3_CLK_GATE Registers

3.13.83.1 MEM_CLK_GATE Register (Offset = 27Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1075. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 027Ch

Figure 3-479. OTTO3_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													OTTO3_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1076. OTTO3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	OTTO3_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding otto Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.84 MEM_SDFM0_PLL_CLK_GATE Registers

3.13.84.1 MEM_PLL_CLK_GATE Register (Offset = 280h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1077. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0280h

Figure 3-480. SDFM0_PLL_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													SDFM0_PLL_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1078. SDFM0_PLL_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	SDFM0_PLL_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding sdfm pll clock Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.85 MEM_SDFM1_PLL_CLK_GATE Registers

3.13.85.1 MEM_PLL_CLK_GATE Register (Offset = 284h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1079. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0284h

Figure 3-481. SDFM1_PLL_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													SDFM1_PLL_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1080. SDFM1_PLL_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	SDFM1_PLL_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding sdfm pll clock Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.86 MEM_FSI_TX0_PLL_CLK_GATE Registers

3.13.86.1 MEM_TX0_PLL_CLK_GATE Register (Offset = 288h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1081. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0288h

Figure 3-482. FSI_TX0_PLL_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													FSI_TX0_PLL_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1082. FSI_TX0_PLL_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	FSI_TX0_PLL_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding fsi rx pll clock Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.87 MEM_FSI_TX1_PLL_CLK_GATE Registers

3.13.87.1 MEM_TX1_PLL_CLK_GATE Register (Offset = 28Ch) [reset = 0h]

Short Description:

Long Description:

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Table 3-1083. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 028Ch

Figure 3-483. FSI_TX1_PLL_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													FSI_TX1_PLL_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1084. FSI_TX1_PLL_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	FSI_TX1_PLL_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding fsi rx pll clock Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.88 MEM_FSI_TX2_PLL_CLK_GATE Registers

3.13.88.1 MEM_TX2_PLL_CLK_GATE Register (Offset = 290h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1085. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0290h

Figure 3-484. FSI_TX2_PLL_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													FSI_TX2_PLL_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1086. FSI_TX2_PLL_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	FSI_TX2_PLL_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding fsi rx pll clock Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.89 MEM_FSI_TX3_PLL_CLK_GATE Registers

3.13.89.1 MEM_TX3_PLL_CLK_GATE Register (Offset = 294h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1087. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0294h

Figure 3-485. FSI_TX3_PLL_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													FSI_TX3_PLL_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1088. FSI_TX3_PLL_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	FSI_TX3_PLL_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding fsi rx pll clock Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.90 MEM_ADC_SCTILE0_CLK_GATE Registers

3.13.90.1 MEM_SCTILE0_CLK_GATE Register (Offset = 29Ch) [reset = 0h]

Short Description:

Long Description:

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Table 3-1089. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 029Ch

Figure 3-486. ADC_SCTILE0_CLK_GATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ADC_SCTILE0_CLK_GATE_CLK_GATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1090. ADC_SCTILE0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ADC_SCTILE0_CLK_GATE_CLK_GATE	R/W	0h	writing 3b'111 will gate clock for corresponding adc safety tiles Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.91 MEM_ETPWM0_RST Registers

3.13.91.1 MEM_RST Register (Offset = 300h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1091. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0300h

Figure 3-487. ETPWM0_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM0_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1092. ETPWM0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM0_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.92 MEM_ETPWM1_RST Registers

3.13.92.1 MEM_RST Register (Offset = 304h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1093. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0304h

Figure 3-488. ETPWM1_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM1_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1094. ETPWM1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM1_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.93 MEM_ETPWM2_RST Registers

3.13.93.1 MEM_RST Register (Offset = 308h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1095. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0308h

Figure 3-489. ETPWM2_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM2_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1096. ETPWM2_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM2_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.94 MEM_ETPWM3_RST Registers

3.13.94.1 MEM_RST Register (Offset = 30Ch) [reset = 0h]

Short Description:

Long Description:

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Table 3-1097. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 030Ch

Figure 3-490. ETPWM3_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM3_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1098. ETPWM3_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM3_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.95 MEM_ETPWM4_RST Registers

3.13.95.1 MEM_RST Register (Offset = 310h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1099. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0310h

Figure 3-491. ETPWM4_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM4_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1100. ETPWM4_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM4_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.96 MEM_ETPWM5_RST Registers

3.13.96.1 MEM_RST Register (Offset = 314h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1101. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0314h

Figure 3-492. ETPWM5_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM5_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1102. ETPWM5_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM5_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.97 MEM_ETPWM6_RST Registers

3.13.97.1 MEM_RST Register (Offset = 318h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1103. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0318h

Figure 3-493. ETPWM6_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM6_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1104. ETPWM6_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM6_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.98 MEM_ETPWM7_RST Registers

3.13.98.1 MEM_RST Register (Offset = 31Ch) [reset = 0h]

Short Description:

Long Description:

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Table 3-1105. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 031Ch

Figure 3-494. ETPWM7_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM7_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1106. ETPWM7_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM7_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.99 MEM_ETPWM8_RST Registers

3.13.99.1 MEM_RST Register (Offset = 320h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1107. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0320h

Figure 3-495. ETPWM8_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM8_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1108. ETPWM8_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM8_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.100 MEM_ETPWM9_RST Registers

3.13.100.1 MEM_RST Register (Offset = 324h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1109. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0324h

Figure 3-496. ETPWM9_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM9_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1110. ETPWM9_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM9_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.101 MEM_ETPWM10_RST Registers

3.13.101.1 MEM_RST Register (Offset = 328h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1111. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0328h

Figure 3-497. ETPWM10_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM10_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1112. ETPWM10_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM10_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.102 MEM_ETPWM11_RST Registers

3.13.102.1 MEM_RST Register (Offset = 32Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1113. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 032Ch

Figure 3-498. ETPWM11_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM11_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1114. ETPWM11_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM11_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.103 MEM_ETPWM12_RST Registers

3.13.103.1 MEM_RST Register (Offset = 330h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1115. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0330h

Figure 3-499. ETPWM12_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM12_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1116. ETPWM12_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM12_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.104 MEM_ETPWM13_RST Registers

3.13.104.1 MEM_RST Register (Offset = 334h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1117. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0334h

Figure 3-500. ETPWM13_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM13_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1118. ETPWM13_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM13_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.105 MEM_ETPWM14_RST Registers

3.13.105.1 MEM_RST Register (Offset = 338h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1119. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0338h

Figure 3-501. ETPWM14_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM14_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1120. ETPWM14_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM14_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.106 MEM_ETPWM15_RST Registers

3.13.106.1 MEM_RST Register (Offset = 33Ch) [reset = 0h]

Short Description:

Long Description:

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Table 3-1121. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 033Ch

Figure 3-502. ETPWM15_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM15_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1122. ETPWM15_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM15_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.107 MEM_ETPWM16_RST Registers

3.13.107.1 MEM_RST Register (Offset = 340h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1123. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0340h

Figure 3-503. ETPWM16_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM16_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1124. ETPWM16_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM16_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.108 MEM_ETPWM17_RST Registers

3.13.108.1 MEM_RST Register (Offset = 344h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1125. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0344h

Figure 3-504. ETPWM17_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM17_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1126. ETPWM17_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM17_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.109 MEM_ETPWM18_RST Registers

3.13.109.1 MEM_RST Register (Offset = 348h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1127. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0348h

Figure 3-505. ETPWM18_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM18_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1128. ETPWM18_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM18_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.110 MEM_ETPWM19_RST Registers

3.13.110.1 MEM_RST Register (Offset = 34Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1129. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 034Ch

Figure 3-506. ETPWM19_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM19_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1130. ETPWM19_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM19_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.111 MEM_ETPWM20_RST Registers

3.13.111.1 MEM_RST Register (Offset = 350h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1131. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0350h

Figure 3-507. ETPWM20_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM20_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1132. ETPWM20_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM20_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.112 MEM_ETPWM21_RST Registers

3.13.112.1 MEM_RST Register (Offset = 354h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1133. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0354h

Figure 3-508. ETPWM21_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM21_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1134. ETPWM21_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM21_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.113 MEM_ETPWM22_RST Registers

3.13.113.1 MEM_RST Register (Offset = 358h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1135. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0358h

Figure 3-509. ETPWM22_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM22_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1136. ETPWM22_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM22_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.114 MEM_ETPWM23_RST Registers

3.13.114.1 MEM_RST Register (Offset = 35Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1137. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 035Ch

Figure 3-510. ETPWM23_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM23_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1138. ETPWM23_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM23_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.115 MEM_ETPWM24_RST Registers

3.13.115.1 MEM_RST Register (Offset = 360h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1139. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0360h

Figure 3-511. ETPWM24_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM24_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1140. ETPWM24_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM24_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.116 MEM_ETPWM25_RST Registers

3.13.116.1 MEM_RST Register (Offset = 364h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1141. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0364h

Figure 3-512. ETPWM25_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM25_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1142. ETPWM25_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM25_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.117 MEM_ETPWM26_RST Registers

3.13.117.1 MEM_RST Register (Offset = 368h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1143. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0368h

Figure 3-513. ETPWM26_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM26_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1144. ETPWM26_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM26_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.118 MEM_ETPWM27_RST Registers

3.13.118.1 MEM_RST Register (Offset = 36Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1145. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 036Ch

Figure 3-514. ETPWM27_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM27_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1146. ETPWM27_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM27_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.119 MEM_ETPWM28_RST Registers

3.13.119.1 MEM_RST Register (Offset = 370h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1147. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0370h

Figure 3-515. ETPWM28_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM28_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1148. ETPWM28_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM28_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.120 MEM_ETPWM29_RST Registers

3.13.120.1 MEM_RST Register (Offset = 374h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1149. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0374h

Figure 3-516. ETPWM29_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM29_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1150. ETPWM29_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM29_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.121 MEM_ETPWM30_RST Registers

3.13.121.1 MEM_RST Register (Offset = 378h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1151. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0378h

Figure 3-517. ETPWM30_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM30_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1152. ETPWM30_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM30_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.122 MEM_ETPWM31_RST Registers

3.13.122.1 MEM_RST Register (Offset = 37Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1153. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 037Ch

Figure 3-518. ETPWM31_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ETPWM31_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1154. ETPWM31_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ETPWM31_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding etpwm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.123 MEM_FSI_TX0_RST Registers

3.13.123.1 MEM_TX0_RST Register (Offset = 380h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1155. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0380h

Figure 3-519. FSI_TX0_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															FSI_TX0_RST_RST
NONE															R/W
0															0h

Access Types Legend

Table 3-1156. FSI_TX0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	FSI_TX0_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding fsi_tx Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.124 MEM_FSI_TX1_RST Registers

3.13.124.1 MEM_TX1_RST Register (Offset = 384h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1157. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0384h

Figure 3-520. FSI_TX1_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															FSI_TX1_RST_RST
NONE															R/W
0															0h

Access Types Legend

Table 3-1158. FSI_TX1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	FSI_TX1_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding fsi_tx Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.125 MEM_FSI_TX2_RST Registers

3.13.125.1 MEM_TX2_RST Register (Offset = 388h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1159. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0388h

Figure 3-521. FSI_TX2_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															FSI_TX2_RST_RST
NONE															R/W
0															0h

Access Types Legend

Table 3-1160. FSI_TX2_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	FSI_TX2_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding fsi_tx Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.126 MEM_FSI_TX3_RST Registers

3.13.126.1 MEM_TX3_RST Register (Offset = 38Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1161. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 038Ch

Figure 3-522. FSI_TX3_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															FSI_TX3_RST_RST
NONE															R/W
0															0h

Access Types Legend

Table 3-1162. FSI_TX3_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	FSI_TX3_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding fsi_tx Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.127 MEM_FSI_RX0_RST Registers

3.13.127.1 MEM_RX0_RST Register (Offset = 390h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1163. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0390h

Figure 3-523. FSI_RX0_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															FSI_RX0_RST_RST
NONE															R/W
0															0h

Access Types Legend

Table 3-1164. FSI_RX0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	FSI_RX0_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding fsi_rx Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.128 MEM_FSI_RX1_RST Registers

3.13.128.1 MEM_RX1_RST Register (Offset = 394h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1165. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0394h

Figure 3-524. FSI_RX1_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															FSI_RX1_RST_RST
NONE															R/W
0															0h

Access Types Legend

Table 3-1166. FSI_RX1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	FSI_RX1_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding fsi_rx Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.129 MEM_FSI_RX2_RST Registers

3.13.129.1 MEM_RX2_RST Register (Offset = 398h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1167. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0398h

Figure 3-525. FSI_RX2_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															FSI_RX2_RST_RST
NONE															R/W
0															0h

Access Types Legend

Table 3-1168. FSI_RX2_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	FSI_RX2_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding fsi_rx Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.130 MEM_FSI_RX3_RST Registers

3.13.130.1 MEM_RX3_RST Register (Offset = 39Ch) [reset = 0h]

Short Description:

Long Description:

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Table 3-1169. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 039Ch

Figure 3-526. FSI_RX3_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															FSI_RX3_RST_RST
NONE															R/W
0															0h

Access Types Legend

Table 3-1170. FSI_RX3_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	FSI_RX3_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding fsi_rx Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.131 MEM_CMPSS12B0_RST Registers

3.13.131.1 MEM_RST Register (Offset = 3A0h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1171. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03A0h

Figure 3-527. CMPSS12B0_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													CMPSS12B0_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1172. CMPSS12B0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	CMPSS12B0_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding cmpss12b Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.132 MEM_CMPSS8B0_RST Registers

3.13.132.1 MEM_RST Register (Offset = 3D0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1173. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03D0h

Figure 3-528. CMPSS8B0_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													CMPSS8B0_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1174. CMPSS8B0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	CMPSS8B0_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding cmpss8b Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.133 MEM_ECAP0_RST Registers

3.13.133.1 MEM_RST Register (Offset = 400h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1175. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0400h

Figure 3-529. ECAP0_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ECAP0_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1176. ECAP0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ECAP0_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding ecap Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.134 MEM_ECAP1_RST Registers

3.13.134.1 MEM_RST Register (Offset = 404h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1177. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0404h

Figure 3-530. ECAP1_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															ECAP1_RST_RST
NONE															R/W
0															0h

Access Types Legend

Table 3-1178. ECAP1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ECAP1_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding ecap Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.135 MEM_ECAP2_RST Registers

3.13.135.1 MEM_RST Register (Offset = 408h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1179. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0408h

Figure 3-531. ECAP2_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ECAP2_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1180. ECAP2_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ECAP2_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding ecap Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.136 MEM_ECAP3_RST Registers

3.13.136.1 MEM_RST Register (Offset = 40Ch) [reset = 0h]

Short Description:

Long Description:

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Table 3-1181. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 040Ch

Figure 3-532. ECAP3_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ECAP3_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1182. ECAP3_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ECAP3_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding ecap Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.137 MEM_ECAP4_RST Registers

3.13.137.1 MEM_RST Register (Offset = 410h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1183. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0410h

Figure 3-533. ECAP4_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ECAP4_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1184. ECAP4_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ECAP4_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding ecap Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.138 MEM_ECAP5_RST Registers

3.13.138.1 MEM_RST Register (Offset = 414h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1185. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0414h

Figure 3-534. ECAP5_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														ECAP5_RST_RST	
NONE														R/W	
0														0h	

Access Types Legend

Table 3-1186. ECAP5_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ECAP5_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding ecap Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.139 MEM_ECAP6_RST Registers

3.13.139.1 MEM_RST Register (Offset = 418h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1187. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0418h

Figure 3-535. ECAP6_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ECAP6_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1188. ECAP6_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ECAP6_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding ecap Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.140 MEM_ECAP7_RST Registers

3.13.140.1 MEM_RST Register (Offset = 41Ch) [reset = 0h]

Short Description:

Long Description:

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Table 3-1189. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 041Ch

Figure 3-536. ECAP7_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														ECAP7_RST_RST	
NONE														R/W	
0														0h	

Access Types Legend

Table 3-1190. ECAP7_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ECAP7_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding ecap Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.141 MEM_ECAP8_RST Registers

3.13.141.1 MEM_RST Register (Offset = 420h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1191. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0420h

Figure 3-537. ECAP8_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ECAP8_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1192. ECAP8_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ECAP8_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding ecap Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.142 MEM_ECAP9_RST Registers

3.13.142.1 MEM_RST Register (Offset = 424h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1193. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0424h

Figure 3-538. ECAP9_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ECAP9_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1194. ECAP9_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ECAP9_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding ecap Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.143 MEM_EQEP0_RST Registers

3.13.143.1 MEM_RST Register (Offset = 440h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1195. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0440h

Figure 3-539. EQEP0_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														EQEP0_RST_RST	
NONE														R/W	
0														0h	

Access Types Legend

Table 3-1196. EQEP0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	EQEP0_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding eqep Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.144 MEM_EQEP1_RST Registers

3.13.144.1 MEM_RST Register (Offset = 444h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1197. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0444h

Figure 3-540. EQEP1_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														EQEP1_RST_RST	
NONE														R/W	
0														0h	

Access Types Legend

Table 3-1198. EQEP1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	EQEP1_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding eqep Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.145 MEM_EQEP2_RST Registers

3.13.145.1 MEM_RST Register (Offset = 448h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1199. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0448h

Figure 3-541. EQEP2_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													EQEP2_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1200. EQEP2_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	EQEP2_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding eqep Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.146 MEM_SDFM0_RST Registers

3.13.146.1 MEM_RST Register (Offset = 450h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1201. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0450h

Figure 3-542. SDFM0_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															SDFM0_RST_RST
NONE															R/W
0															0h

Access Types Legend

Table 3-1202. SDFM0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	SDFM0_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding sdfm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.147 MEM_SDFM1_RST Registers

3.13.147.1 MEM_RST Register (Offset = 454h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1203. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0454h

Figure 3-543. SDFM1_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													SDFM1_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1204. SDFM1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	SDFM1_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding sdfm Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.148 MEM_DAC_RST Registers

3.13.148.1 MEM_RST Register (Offset = 458h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1205. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0458h

Figure 3-544. DAC_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														DAC_RST_RST	
NONE														R/W	
0														0h	

Access Types Legend

Table 3-1206. DAC_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	DAC_RST_RST	R/W	0h	writing 3b'111 will generate reset for dac Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.149 MEM_ADC0_RST Registers

3.13.149.1 MEM_RST Register (Offset = 45Ch) [reset = 0h]

Short Description:

Long Description:

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Table 3-1207. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 045Ch

Figure 3-545. ADC0_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ADC0_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1208. ADC0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ADC0_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding adc Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.150 MEM_ADC1_RST Registers

3.13.150.1 MEM_RST Register (Offset = 460h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1209. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0460h

Figure 3-546. ADC1_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															ADC1_RST_RST
NONE															R/W
0															0h

Access Types Legend

Table 3-1210. ADC1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ADC1_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding adc Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.151 MEM_ADC2_RST Registers

3.13.151.1 MEM_RST Register (Offset = 464h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1211. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0464h

Figure 3-547. ADC2_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ADC2_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1212. ADC2_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ADC2_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding adc Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.152 MEM_ADC3_RST Registers

3.13.152.1 MEM_RST Register (Offset = 468h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1213. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0468h

Figure 3-548. ADC3_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															ADC3_RST_RST
NONE															R/W
0															0h

Access Types Legend

Table 3-1214. ADC3_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ADC3_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding adc Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.153 MEM_ADC4_RST Registers

3.13.153.1 MEM_RST Register (Offset = 46Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1215. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 046Ch

Figure 3-549. ADC4_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ADC4_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1216. ADC4_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ADC4_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding adc Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.154 MEM_OTTO0_RST Registers

3.13.154.1 MEM_RST Register (Offset = 470h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1217. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0470h

Figure 3-550. OTTO0_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													OTTO0_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1218. OTTO0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	OTTO0_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding otto Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.155 MEM_OTTO1_RST Registers

3.13.155.1 MEM_RST Register (Offset = 474h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1219. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0474h

Figure 3-551. OTTO1_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													OTTO1_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1220. OTTO1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	OTTO1_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding otto Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.156 MEM_OTTO2_RST Registers

3.13.156.1 MEM_RST Register (Offset = 478h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1221. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0478h

Figure 3-552. OTTO2_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													OTTO2_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1222. OTTO2_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	OTTO2_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding otto Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.157 MEM_OTTO3_RST Registers

3.13.157.1 MEM_RST Register (Offset = 47Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1223. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 047Ch

Figure 3-553. OTTO3_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													OTTO3_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1224. OTTO3_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	OTTO3_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding otto Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.158 MEM_ADC_SCTILE0_RST Registers

3.13.158.1 MEM_SCTILE0_RST Register (Offset = 484h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1225. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0484h

Figure 3-554. ADC_SCTILE0_RST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ADC_SCTILE0_RST_RST		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1226. ADC_SCTILE0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ADC_SCTILE0_RST_RST	R/W	0h	writing 3b'111 will generate reset for corresponding adc safety tiles Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.159 MEM_EPWM0_HALTEN Registers

3.13.159.1 MEM_HALTEN Register (Offset = 500h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1227. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0500h

Figure 3-555. EPWM0_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EPWM0_HALTEN_CR5B1	EPWM0_HALTEN_CR5A1	EPWM0_HALTEN_CR5B0	EPWM0_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1228. EPWM0_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EPWM0_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EPWM0_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EPWM0_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EPWM0_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.160 MEM_EPWM1_HALTEN Registers

3.13.160.1 MEM_HALTEN Register (Offset = 504h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1229. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0504h

Figure 3-556. EPWM1_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EPWM1_HALTEN_CR5B1	EPWM1_HALTEN_CR5A1	EPWM1_HALTEN_CR5B0	EPWM1_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1230. EPWM1_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EPWM1_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EPWM1_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EPWM1_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EPWM1_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.161 MEM_EPWM2_HALTEN Registers

3.13.161.1 MEM_HALTEN Register (Offset = 508h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1231. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0508h

Figure 3-557. EPWM2_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EPWM2_HALTEN_CR5B1	EPWM2_HALTEN_CR5A1	EPWM2_HALTEN_CR5B0	EPWM2_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1232. EPWM2_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EPWM2_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EPWM2_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EPWM2_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EPWM2_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.162 MEM_EPWM3_HALTEN Registers

3.13.162.1 MEM_HALTEN Register (Offset = 50Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1233. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 050Ch

Figure 3-558. EPWM3_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EPWM3_HALTEN_CR5B1	EPWM3_HALTEN_CR5A1	EPWM3_HALTEN_CR5B0	EPWM3_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1234. EPWM3_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EPWM3_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EPWM3_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EPWM3_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EPWM3_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.163 MEM_EPWM4_HALTEN Registers

3.13.163.1 MEM_HALTEN Register (Offset = 510h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1235. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0510h

Figure 3-559. EPWM4_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EPWM4_HALTEN_CR5B1	EPWM4_HALTEN_CR5A1	EPWM4_HALTEN_CR5B0	EPWM4_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1236. EPWM4_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EPWM4_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EPWM4_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EPWM4_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EPWM4_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.164 MEM_EPWM5_HALTEN Registers

3.13.164.1 MEM_HALTEN Register (Offset = 514h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1237. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0514h

Figure 3-560. EPWM5_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EPWM5_HALTEN_CR5B1	EPWM5_HALTEN_CR5A1	EPWM5_HALTEN_CR5B0	EPWM5_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1238. EPWM5_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EPWM5_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EPWM5_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EPWM5_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EPWM5_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.165 MEM_EPWM6_HALTEN Registers

3.13.165.1 MEM_HALTEN Register (Offset = 518h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1239. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0518h

Figure 3-561. EPWM6_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EPWM6_HALTEN_CR5B1	EPWM6_HALTEN_CR5A1	EPWM6_HALTEN_CR5B0	EPWM6_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1240. EPWM6_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EPWM6_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EPWM6_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EPWM6_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EPWM6_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.166 MEM_EPWM7_HALTEN Registers

3.13.166.1 MEM_HALTEN Register (Offset = 51Ch) [reset = 0h]

Short Description:

Long Description:

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Table 3-1241. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 051Ch

Figure 3-562. EPWM7_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EPWM7_HALTEN_CR5B1	EPWM7_HALTEN_CR5A1	EPWM7_HALTEN_CR5B0	EPWM7_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1242. EPWM7_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EPWM7_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EPWM7_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EPWM7_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EPWM7_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.167 MEM_EPWM8_HALTEN Registers

3.13.167.1 MEM_HALTEN Register (Offset = 520h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1243. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0520h

Figure 3-563. EPWM8_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EPWM8_HALTEN_CR5B1	EPWM8_HALTEN_CR5A1	EPWM8_HALTEN_CR5B0	EPWM8_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1244. EPWM8_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EPWM8_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EPWM8_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EPWM8_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EPWM8_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.168 MEM_EPWM9_HALTEN Registers

3.13.168.1 MEM_HALTEN Register (Offset = 524h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1245. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0524h

Figure 3-564. EPWM9_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EPWM9_HALTEN_CR5B1	EPWM9_HALTEN_CR5A1	EPWM9_HALTEN_CR5B0	EPWM9_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1246. EPWM9_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EPWM9_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EPWM9_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EPWM9_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EPWM9_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.169 MEM_EPWM10_HALTEN Registers

3.13.169.1 MEM_HALTEN Register (Offset = 528h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1247. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0528h

Figure 3-565. EPWM10_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EPWM10_HALTEN_CR5B1	EPWM10_HALTEN_CR5A1	EPWM10_HALTEN_CR5B0	EPWM10_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1248. EPWM10_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EPWM10_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EPWM10_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EPWM10_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EPWM10_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.170 MEM_EPWM11_HALTEN Registers

3.13.170.1 MEM_HALTEN Register (Offset = 52Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1249. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 052Ch

Figure 3-566. EPWM11_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EPWM11_HALTEN_CR5B1	EPWM11_HALTEN_CR5A1	EPWM11_HALTEN_CR5B0	EPWM11_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1250. EPWM11_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EPWM11_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EPWM11_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EPWM11_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EPWM11_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.171 MEM_EPWM12_HALTEN Registers

3.13.171.1 MEM_HALTEN Register (Offset = 530h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1251. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0530h

Figure 3-567. EPWM12_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EPWM12_HALTEN_CR5B1	EPWM12_HALTEN_CR5A1	EPWM12_HALTEN_CR5B0	EPWM12_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1252. EPWM12_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EPWM12_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EPWM12_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EPWM12_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EPWM12_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.172 MEM_EPWM13_HALTEN Registers

3.13.172.1 MEM_HALTEN Register (Offset = 534h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1253. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0534h

Figure 3-568. EPWM13_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EPWM13_HALTEN_CR5B1	EPWM13_HALTEN_CR5A1	EPWM13_HALTEN_CR5B0	EPWM13_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1254. EPWM13_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EPWM13_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EPWM13_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EPWM13_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EPWM13_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.173 MEM_EPWM14_HALTEN Registers

3.13.173.1 MEM_HALTEN Register (Offset = 538h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1255. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0538h

Figure 3-569. EPWM14_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EPWM14_HALTEN_CR5B1	EPWM14_HALTEN_CR5A1	EPWM14_HALTEN_CR5B0	EPWM14_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1256. EPWM14_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EPWM14_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EPWM14_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EPWM14_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EPWM14_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.174 MEM_EPWM15_HALTEN Registers

3.13.174.1 MEM_HALTEN Register (Offset = 53Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1257. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 053Ch

Figure 3-570. EPWM15_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EPWM15_HALTEN_CR5B1	EPWM15_HALTEN_CR5A1	EPWM15_HALTEN_CR5B0	EPWM15_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1258. EPWM15_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EPWM15_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EPWM15_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EPWM15_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EPWM15_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.175 MEM_EPWM16_HALTEN Registers

3.13.175.1 MEM_HALTEN Register (Offset = 540h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1259. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0540h

Figure 3-571. EPWM16_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EPWM16_HALTEN_CR5B1	EPWM16_HALTEN_CR5A1	EPWM16_HALTEN_CR5B0	EPWM16_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1260. EPWM16_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EPWM16_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EPWM16_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EPWM16_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EPWM16_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.176 MEM_EPWM17_HALTEN Registers

3.13.176.1 MEM_HALTEN Register (Offset = 544h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1261. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0544h

Figure 3-572. EPWM17_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EPWM17_HALTEN_CR5B1	EPWM17_HALTEN_CR5A1	EPWM17_HALTEN_CR5B0	EPWM17_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1262. EPWM17_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EPWM17_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EPWM17_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EPWM17_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EPWM17_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.177 MEM_EPWM18_HALTEN Registers

3.13.177.1 MEM_HALTEN Register (Offset = 548h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1263. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0548h

Figure 3-573. EPWM18_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EPWM18_HALTEN_CR5B1	EPWM18_HALTEN_CR5A1	EPWM18_HALTEN_CR5B0	EPWM18_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1264. EPWM18_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EPWM18_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EPWM18_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EPWM18_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EPWM18_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.178 MEM_EPWM19_HALTEN Registers

3.13.178.1 MEM_HALTEN Register (Offset = 54Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1265. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 054Ch

Figure 3-574. EPWM19_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EPWM19_HALTEN_CR5B1	EPWM19_HALTEN_CR5A1	EPWM19_HALTEN_CR5B0	EPWM19_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1266. EPWM19_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EPWM19_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EPWM19_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EPWM19_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EPWM19_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.179 MEM_EPWM20_HALTEN Registers

3.13.179.1 MEM_HALTEN Register (Offset = 550h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1267. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0550h

Figure 3-575. EPWM20_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EPWM20_HALTEN_CR5B1	EPWM20_HALTEN_CR5A1	EPWM20_HALTEN_CR5B0	EPWM20_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1268. EPWM20_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EPWM20_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EPWM20_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EPWM20_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EPWM20_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.180 MEM_EPWM21_HALTEN Registers

3.13.180.1 MEM_HALTEN Register (Offset = 554h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1269. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0554h

Figure 3-576. EPWM21_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EPWM21_HALTEN_CR5B1	EPWM21_HALTEN_CR5A1	EPWM21_HALTEN_CR5B0	EPWM21_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1270. EPWM21_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EPWM21_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EPWM21_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EPWM21_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EPWM21_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.181 MEM_EPWM22_HALTEN Registers

3.13.181.1 MEM_HALTEN Register (Offset = 558h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1271. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0558h

Figure 3-577. EPWM22_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EPWM22_HALTEN_CR5B1	EPWM22_HALTEN_CR5A1	EPWM22_HALTEN_CR5B0	EPWM22_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1272. EPWM22_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EPWM22_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EPWM22_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EPWM22_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EPWM22_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.182 MEM_EPWM23_HALTEN Registers

3.13.182.1 MEM_HALTEN Register (Offset = 55Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1273. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 055Ch

Figure 3-578. EPWM23_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EPWM23_HALTEN_CR5B1	EPWM23_HALTEN_CR5A1	EPWM23_HALTEN_CR5B0	EPWM23_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1274. EPWM23_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EPWM23_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EPWM23_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EPWM23_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EPWM23_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.183 MEM_EPWM24_HALTEN Registers

3.13.183.1 MEM_HALTEN Register (Offset = 560h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1275. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0560h

Figure 3-579. EPWM24_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EPWM24_HALTEN_CR5B1	EPWM24_HALTEN_CR5A1	EPWM24_HALTEN_CR5B0	EPWM24_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1276. EPWM24_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EPWM24_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EPWM24_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EPWM24_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EPWM24_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.184 MEM_EPWM25_HALTEN Registers

3.13.184.1 MEM_HALTEN Register (Offset = 564h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1277. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0564h

Figure 3-580. EPWM25_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EPWM25_HALTEN_CR5B1	EPWM25_HALTEN_CR5A1	EPWM25_HALTEN_CR5B0	EPWM25_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1278. EPWM25_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EPWM25_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EPWM25_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EPWM25_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EPWM25_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.185 MEM_EPWM26_HALTEN Registers

3.13.185.1 MEM_HALTEN Register (Offset = 568h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1279. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0568h

Figure 3-581. EPWM26_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EPWM26_HALTEN_CR5B1	EPWM26_HALTEN_CR5A1	EPWM26_HALTEN_CR5B0	EPWM26_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1280. EPWM26_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EPWM26_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EPWM26_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EPWM26_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EPWM26_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.186 MEM_EPWM27_HALTEN Registers

3.13.186.1 MEM_HALTEN Register (Offset = 56Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1281. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 056Ch

Figure 3-582. EPWM27_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EPWM27_HALTEN_CR5B1	EPWM27_HALTEN_CR5A1	EPWM27_HALTEN_CR5B0	EPWM27_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1282. EPWM27_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EPWM27_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EPWM27_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EPWM27_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EPWM27_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.187 MEM_EPWM28_HALTEN Registers

3.13.187.1 MEM_HALTEN Register (Offset = 570h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1283. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0570h

Figure 3-583. EPWM28_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EPWM28_HALTEN_CR5B1	EPWM28_HALTEN_CR5A1	EPWM28_HALTEN_CR5B0	EPWM28_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1284. EPWM28_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EPWM28_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EPWM28_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EPWM28_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EPWM28_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.188 MEM_EPWM29_HALTEN Registers

3.13.188.1 MEM_HALTEN Register (Offset = 574h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1285. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0574h

Figure 3-584. EPWM29_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EPWM29_HALTEN_CR5B1	EPWM29_HALTEN_CR5A1	EPWM29_HALTEN_CR5B0	EPWM29_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1286. EPWM29_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EPWM29_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EPWM29_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EPWM29_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EPWM29_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.189 MEM_EPWM30_HALTEN Registers

3.13.189.1 MEM_HALTEN Register (Offset = 578h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1287. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0578h

Figure 3-585. EPWM30_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EPWM30_HALTEN_CR5B1	EPWM30_HALTEN_CR5A1	EPWM30_HALTEN_CR5B0	EPWM30_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1288. EPWM30_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EPWM30_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EPWM30_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EPWM30_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EPWM30_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.190 MEM_EPWM31_HALTEN Registers

3.13.190.1 MEM_HALTEN Register (Offset = 57Ch) [reset = 0h]

Short Description:

Long Description:

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Table 3-1289. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 057Ch

Figure 3-586. EPWM31_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EPWM31_HALTEN_CR5B1	EPWM31_HALTEN_CR5A1	EPWM31_HALTEN_CR5B0	EPWM31_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1290. EPWM31_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EPWM31_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EPWM31_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EPWM31_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EPWM31_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.191 MEM_ECAP0_HALTEN Registers

3.13.191.1 MEM_HALTEN Register (Offset = 5D0h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1291. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05D0h

Figure 3-587. ECAP0_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												ECAP0_HALTEN_CR5B1	ECAP0_HALTEN_CR5A1	ECAP0_HALTEN_CR5B0	ECAP0_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1292. ECAP0_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	ECAP0_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	ECAP0_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	ECAP0_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	ECAP0_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.192 MEM_ECAP1_HALTEN Registers

3.13.192.1 MEM_HALTEN Register (Offset = 5D4h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1293. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05D4h

Figure 3-588. ECAP1_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												ECAP1_HALTEN_CR5B1	ECAP1_HALTEN_CR5A1	ECAP1_HALTEN_CR5B0	ECAP1_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1294. ECAP1_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	ECAP1_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	ECAP1_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	ECAP1_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	ECAP1_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.193 MEM_ECAP2_HALTEN Registers

3.13.193.1 MEM_HALTEN Register (Offset = 5D8h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1295. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05D8h

Figure 3-589. ECAP2_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												ECAP2_HALTEN_CR5B1	ECAP2_HALTEN_CR5A1	ECAP2_HALTEN_CR5B0	ECAP2_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1296. ECAP2_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	ECAP2_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	ECAP2_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	ECAP2_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	ECAP2_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.194 MEM_ECAP3_HALTEN Registers

3.13.194.1 MEM_HALTEN Register (Offset = 5DCh) [reset = 0h]

Short Description:

Long Description:

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Table 3-1297. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05DCh

Figure 3-590. ECAP3_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												ECAP3_HALTEN_CR5B1	ECAP3_HALTEN_CR5A1	ECAP3_HALTEN_CR5B0	ECAP3_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1298. ECAP3_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	ECAP3_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	ECAP3_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	ECAP3_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	ECAP3_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.195 MEM_ECAP4_HALTEN Registers

3.13.195.1 MEM_HALTEN Register (Offset = 5E0h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1299. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05E0h

Figure 3-591. ECAP4_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												ECAP4_HALTEN_CR5B1	ECAP4_HALTEN_CR5A1	ECAP4_HALTEN_CR5B0	ECAP4_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1300. ECAP4_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	ECAP4_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	ECAP4_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	ECAP4_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	ECAP4_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.196 MEM_ECAP5_HALTEN Registers

3.13.196.1 MEM_HALTEN Register (Offset = 5E4h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1301. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05E4h

Figure 3-592. ECAP5_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												ECAP5_HALTEN_CR5B1	ECAP5_HALTEN_CR5A1	ECAP5_HALTEN_CR5B0	ECAP5_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1302. ECAP5_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	ECAP5_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	ECAP5_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	ECAP5_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	ECAP5_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.197 MEM_ECAP6_HALTEN Registers

3.13.197.1 MEM_HALTEN Register (Offset = 5E8h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1303. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05E8h

Figure 3-593. ECAP6_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												ECAP6_HALTEN_CR5B1	ECAP6_HALTEN_CR5A1	ECAP6_HALTEN_CR5B0	ECAP6_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1304. ECAP6_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	ECAP6_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	ECAP6_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	ECAP6_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	ECAP6_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.198 MEM_ECAP7_HALTEN Registers

3.13.198.1 MEM_HALTEN Register (Offset = 5ECh) [reset = 0h]

Short Description:

Long Description:

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Table 3-1305. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05ECh

Figure 3-594. ECAP7_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												ECAP7_HALTEN_CR5B1	ECAP7_HALTEN_CR5A1	ECAP7_HALTEN_CR5B0	ECAP7_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1306. ECAP7_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	ECAP7_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	ECAP7_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	ECAP7_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	ECAP7_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.199 MEM_ECAP8_HALTEN Registers

3.13.199.1 MEM_HALTEN Register (Offset = 5F0h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1307. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05F0h

Figure 3-595. ECAP8_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												ECAP8_HALTEN_CR5B1	ECAP8_HALTEN_CR5A1	ECAP8_HALTEN_CR5B0	ECAP8_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1308. ECAP8_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	ECAP8_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	ECAP8_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	ECAP8_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	ECAP8_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.200 MEM_ECAP9_HALTEN Registers

3.13.200.1 MEM_HALTEN Register (Offset = 5F4h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1309. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05F4h

Figure 3-596. ECAP9_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												ECAP9_HALTEN_CR5B1	ECAP9_HALTEN_CR5A1	ECAP9_HALTEN_CR5B0	ECAP9_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1310. ECAP9_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	ECAP9_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	ECAP9_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	ECAP9_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	ECAP9_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.201 MEM_EQEP0_HALTEN Registers

3.13.201.1 MEM_HALTEN Register (Offset = 5F8h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1311. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05F8h

Figure 3-597. EQEP0_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EQEP0_HALTEN_CR5B1	EQEP0_HALTEN_CR5A1	EQEP0_HALTEN_CR5B0	EQEP0_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1312. EQEP0_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EQEP0_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EQEP0_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EQEP0_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EQEP0_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.202 MEM_EQEP1_HALTEN Registers

3.13.202.1 MEM_HALTEN Register (Offset = 5FCh) [reset = 0h]

Short Description:

Long Description:

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Table 3-1313. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05FCh

Figure 3-598. EQEP1_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EQEP1_HALTEN_CR5B1	EQEP1_HALTEN_CR5A1	EQEP1_HALTEN_CR5B0	EQEP1_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1314. EQEP1_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EQEP1_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EQEP1_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EQEP1_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EQEP1_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.203 MEM_EQEP2_HALTEN Registers

3.13.203.1 MEM_HALTEN Register (Offset = 600h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1315. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0600h

Figure 3-599. EQEP2_HALTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												EQEP2_HALTEN_CR5B1	EQEP2_HALTEN_CR5A1	EQEP2_HALTEN_CR5B0	EQEP2_HALTEN_CR5A0
NONE												R/W	R/W	R/W	R/W
0												0h	0h	0h	0h

Access Types Legend

Table 3-1316. EQEP2_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	EQEP2_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	EQEP2_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	EQEP2_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	EQEP2_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.204 MEM_LOCK0_KICK0 Registers

3.13.204.1 MEM_KICK0 Register (Offset = 1008h) [reset = 0h]

Short Description: - KICK0 component

Long Description: - KICK0 component

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Table 3-1317. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 1008h

Figure 3-600. LOCK0_KICK0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LOCK0_KICK0															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCK0_KICK0															
R/W															
0h															

Access Types Legend

Table 3-1318. LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0	R/W	0h	- KICK0 component Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.205 MEM_LOCK0_KICK1 Registers

3.13.205.1 MEM_KICK1 Register (Offset = 100Ch) [reset = 0h]

Short Description: - KICK1 component

Long Description: - KICK1 component

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Table 3-1319. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 100Ch

Figure 3-601. LOCK0_KICK1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LOCK0_KICK1															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCK0_KICK1															
R/W															
0h															

Access Types Legend

Table 3-1320. LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1	R/W	0h	- KICK1 component Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.206 MEM_INTR_RAW_STATUS Registers

3.13.206.1 MEM_RAW_STATUS Register (Offset = 1010h) [reset = 0h]

Short Description: Interrupt Raw Status/Set

Long Description: Interrupt Raw Status/Set Register

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Table 3-1321. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 1010h

Figure 3-602. INTR_RAW_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												PROXY_ERR	KICK_ERR	ADDR_ERR	PROT_ERR
NONE												R/W1TS	R/W1TS	R/W1TS	R/W1TS
0												0h	0h	0h	0h

Access Types Legend

Table 3-1322. INTR_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	PROXY_ERR	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	KICK_ERR	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	ADDR_ERR	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	PROT_ERR	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.207 MEM_INTR_ENABLED_STATUS_CLEAR Registers

3.13.207.1 MEM_ENABLED_STATUS_CLEAR Register (Offset = 1014h) [reset = 0h]

Short Description: Interrupt Enabled Status

Long Description: Interrupt Enabled Status/Clear register

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Table 3-1323. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 1014h

Figure 3-603. INTR_ENABLED_STATUS_CLEAR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												ENABLED_PROXY_ERR	ENABLED_KICK_ERR	ENABLED_ADDR_ERR	ENABLED_PROT_ERR
NONE												R/W1TC	R/W1TC	R/W1TC	R/W1TC
0												0h	0h	0h	0h

Access Types Legend

Table 3-1324. INTR_ENABLED_STATUS_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	ENABLED_PROXY_ERR	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	ENABLED_KICK_ERR	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	ENABLED_ADDR_ERR	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	ENABLED_PROT_ERR	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.208 MEM_INTR_ENABLE Registers

3.13.208.1 MEM_ENABLE Register (Offset = 1018h) [reset = 0h]

Short Description: Interrupt Enable registe

Long Description: Interrupt Enable register

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Table 3-1325. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 1018h

Figure 3-604. INTR_ENABLE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												PROXY_ERR_EN	KICK_ERR_EN	ADDR_ERR_EN	PROT_ERR_EN
NONE												R/W1TS	R/W1TS	R/W1TS	R/W1TS
0												0h	0h	0h	0h

Access Types Legend

Table 3-1326. INTR_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	PROXY_ERR_EN	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	KICK_ERR_EN	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	ADDR_ERR_EN	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	PROT_ERR_EN	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.209 MEM_INTR_ENABLE_CLEAR Registers

3.13.209.1 MEM_ENABLE_CLEAR Register (Offset = 101Ch) [reset = 0h]

Short Description: Interrupt Enable Clear r

Long Description: Interrupt Enable Clear register

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Table 3-1327. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 101Ch

Figure 3-605. INTR_ENABLE_CLEAR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												PROXY_ERR_EN_CLR	KICK_ERR_EN_CLR	ADDR_ERR_EN_CLR	PROT_ERR_EN_CLR
NONE												R/W1TC	R/W1TC	R/W1TC	R/W1TC
0												0h	0h	0h	0h

Access Types Legend

Table 3-1328. INTR_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	PROXY_ERR_EN_CLR	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
2	KICK_ERR_EN_CLR	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
1	ADDR_ERR_EN_CLR	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
0	PROT_ERR_EN_CLR	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.210 MEM_EOI Registers

3.13.210.1 MEM_EOI Register (Offset = 1020h) [reset = 0h]

Short Description: EOI register

Long Description: EOI register

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Table 3-1329. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 1020h

Figure 3-606. EOI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								EOI_VECTOR							
NONE								R/W							
0								0h							

Access Types Legend

Table 3-1330. EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	EOI_VECTOR	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip. Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.211 MEM_FAULT_ADDRESS Registers

3.13.211.1 MEM_ADDRESS Register (Offset = 1024h) [reset = 0h]

Short Description: Fault Address register

Long Description: Fault Address register

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Table 3-1331. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 1024h

Figure 3-607. FAULT_ADDRESS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FAULT_ADDR															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FAULT_ADDR															
R															
0h															

Access Types Legend

Table 3-1332. FAULT_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR	R	0h	Fault Address. Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.212 MEM_FAULT_TYPE_STATUS Registers

3.13.212.1 MEM_TYPE_STATUS Register (Offset = 1028h) [reset = 0h]

Short Description: Fault Type Status regist

Long Description: Fault Type Status register

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Table 3-1333. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 1028h

Figure 3-608. FAULT_TYPE_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									FAULT_NS	FAULT_TYPE					
NONE									R	R					
0									0h	0h					

Access Types Legend

Table 3-1334. FAULT_TYPE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE		Reserved
6	FAULT_NS	R	0h	Non-secure access. Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
5:0	FAULT_TYPE	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype != 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.213 MEM_FAULT_ATTR_STATUS Registers

3.13.213.1 MEM_ATTR_STATUS Register (Offset = 102Ch) [reset = 0h]

Short Description: Fault Attribute Status r

Long Description: Fault Attribute Status register

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Table 3-1335. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 102Ch

Figure 3-609. FAULT_ATTR_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FAULT_XID												FAULT_ROUTEID			
R												R			
0h												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FAULT_ROUTEID								FAULT_PRIVID							
R								R							
0h								0h							

Access Types Legend

Table 3-1336. FAULT_ATTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID	R	0h	XID. Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
19:8	FAULT_ROUTEID	R	0h	Route ID. Reset Source: c2k_global_ctrl_rst_mod_g_rst_n
7:0	FAULT_PRIVID	R	0h	Privilege ID. Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.214 MEM_FAULT_CLEAR Registers

3.13.214.1 MEM_CLEAR Register (Offset = 1030h) [reset = 0h]

Short Description: Fault Clear register

Long Description: Fault Clear register

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Table 3-1337. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 1030h

Figure 3-610. FAULT_CLEAR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															FAULT_CLR
NONE															W
0															0h

Access Types Legend

Table 3-1338. FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	FAULT_CLR	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. Reset Source: c2k_global_ctrl_rst_mod_g_rst_n

3.13.215 Access Table

Table 3-1339. Access Type Codes

Access Type	Code	Description
R	R	Read
R/W	R/W	Read / Write
R/W1TS	R/W1TS	Read/Write 1 To Set
R/W1TC	R/W1TC	Read/Write 1 To Clear
W	W	Write

3.14 INPUTXBAR Registers

Table 3-1340. CONTROLSS_INPUTXBAR Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_INPUTXBAR Physical Address
0h	32	INPUTXBAR_PID	502D 0000h
100h	0	INPUTXBAR_INPUTXBAR0_GSEL	502D 0100h
104h	8	INPUTXBAR_INPUTXBAR0_G0	502D 0104h
108h	8	INPUTXBAR_INPUTXBAR0_G1	502D 0108h
140h	0	INPUTXBAR_INPUTXBAR1_GSEL	502D 0140h
144h	8	INPUTXBAR_INPUTXBAR1_G0	502D 0144h
148h	8	INPUTXBAR_INPUTXBAR1_G1	502D 0148h

Table 3-1340. CONTROLSS_INPUTXBAR Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_INPUTXBAR Physical Address
180h	0	INPUTXBAR_INPUTXBAR2_GSEL	502D 0180h
184h	8	INPUTXBAR_INPUTXBAR2_G0	502D 0184h
188h	8	INPUTXBAR_INPUTXBAR2_G1	502D 0188h
1C0h	0	INPUTXBAR_INPUTXBAR3_GSEL	502D 01C0h
1C4h	8	INPUTXBAR_INPUTXBAR3_G0	502D 01C4h
1C8h	8	INPUTXBAR_INPUTXBAR3_G1	502D 01C8h
200h	0	INPUTXBAR_INPUTXBAR4_GSEL	502D 0200h
204h	8	INPUTXBAR_INPUTXBAR4_G0	502D 0204h
208h	8	INPUTXBAR_INPUTXBAR4_G1	502D 0208h
240h	0	INPUTXBAR_INPUTXBAR5_GSEL	502D 0240h
244h	8	INPUTXBAR_INPUTXBAR5_G0	502D 0244h
248h	8	INPUTXBAR_INPUTXBAR5_G1	502D 0248h
280h	0	INPUTXBAR_INPUTXBAR6_GSEL	502D 0280h
284h	8	INPUTXBAR_INPUTXBAR6_G0	502D 0284h
288h	8	INPUTXBAR_INPUTXBAR6_G1	502D 0288h
2C0h	0	INPUTXBAR_INPUTXBAR7_GSEL	502D 02C0h
2C4h	8	INPUTXBAR_INPUTXBAR7_G0	502D 02C4h
2C8h	8	INPUTXBAR_INPUTXBAR7_G1	502D 02C8h
300h	0	INPUTXBAR_INPUTXBAR8_GSEL	502D 0300h
304h	8	INPUTXBAR_INPUTXBAR8_G0	502D 0304h
308h	8	INPUTXBAR_INPUTXBAR8_G1	502D 0308h
340h	0	INPUTXBAR_INPUTXBAR9_GSEL	502D 0340h
344h	8	INPUTXBAR_INPUTXBAR9_G0	502D 0344h
348h	8	INPUTXBAR_INPUTXBAR9_G1	502D 0348h
380h	0	INPUTXBAR_INPUTXBAR10_GSEL	502D 0380h
384h	8	INPUTXBAR_INPUTXBAR10_G0	502D 0384h
388h	8	INPUTXBAR_INPUTXBAR10_G1	502D 0388h
3C0h	0	INPUTXBAR_INPUTXBAR11_GSEL	502D 03C0h
3C4h	8	INPUTXBAR_INPUTXBAR11_G0	502D 03C4h
3C8h	8	INPUTXBAR_INPUTXBAR11_G1	502D 03C8h
400h	0	INPUTXBAR_INPUTXBAR12_GSEL	502D 0400h
404h	8	INPUTXBAR_INPUTXBAR12_G0	502D 0404h
408h	8	INPUTXBAR_INPUTXBAR12_G1	502D 0408h
440h	0	INPUTXBAR_INPUTXBAR13_GSEL	502D 0440h
444h	8	INPUTXBAR_INPUTXBAR13_G0	502D 0444h
448h	8	INPUTXBAR_INPUTXBAR13_G1	502D 0448h
480h	0	INPUTXBAR_INPUTXBAR14_GSEL	502D 0480h
484h	8	INPUTXBAR_INPUTXBAR14_G0	502D 0484h
488h	8	INPUTXBAR_INPUTXBAR14_G1	502D 0488h
4C0h	0	INPUTXBAR_INPUTXBAR15_GSEL	502D 04C0h
4C4h	8	INPUTXBAR_INPUTXBAR15_G0	502D 04C4h
4C8h	8	INPUTXBAR_INPUTXBAR15_G1	502D 04C8h
500h	0	INPUTXBAR_INPUTXBAR16_GSEL	502D 0500h
504h	8	INPUTXBAR_INPUTXBAR16_G0	502D 0504h
508h	8	INPUTXBAR_INPUTXBAR16_G1	502D 0508h
540h	0	INPUTXBAR_INPUTXBAR17_GSEL	502D 0540h

Table 3-1340. CONTROLSS_INPUTXBAR Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_INPUTXBAR Physical Address
544h	8	INPUTXBAR_INPUTXBAR17_G0	502D 0544h
548h	8	INPUTXBAR_INPUTXBAR17_G1	502D 0548h
580h	0	INPUTXBAR_INPUTXBAR18_GSEL	502D 0580h
584h	8	INPUTXBAR_INPUTXBAR18_G0	502D 0584h
588h	8	INPUTXBAR_INPUTXBAR18_G1	502D 0588h
5C0h	0	INPUTXBAR_INPUTXBAR19_GSEL	502D 05C0h
5C4h	8	INPUTXBAR_INPUTXBAR19_G0	502D 05C4h
5C8h	8	INPUTXBAR_INPUTXBAR19_G1	502D 05C8h
600h	0	INPUTXBAR_INPUTXBAR20_GSEL	502D 0600h
604h	8	INPUTXBAR_INPUTXBAR20_G0	502D 0604h
608h	8	INPUTXBAR_INPUTXBAR20_G1	502D 0608h
640h	0	INPUTXBAR_INPUTXBAR21_GSEL	502D 0640h
644h	8	INPUTXBAR_INPUTXBAR21_G0	502D 0644h
648h	8	INPUTXBAR_INPUTXBAR21_G1	502D 0648h
680h	0	INPUTXBAR_INPUTXBAR22_GSEL	502D 0680h
684h	8	INPUTXBAR_INPUTXBAR22_G0	502D 0684h
688h	8	INPUTXBAR_INPUTXBAR22_G1	502D 0688h
6C0h	0	INPUTXBAR_INPUTXBAR23_GSEL	502D 06C0h
6C4h	8	INPUTXBAR_INPUTXBAR23_G0	502D 06C4h
6C8h	8	INPUTXBAR_INPUTXBAR23_G1	502D 06C8h
700h	0	INPUTXBAR_INPUTXBAR24_GSEL	502D 0700h
704h	8	INPUTXBAR_INPUTXBAR24_G0	502D 0704h
708h	8	INPUTXBAR_INPUTXBAR24_G1	502D 0708h
740h	0	INPUTXBAR_INPUTXBAR25_GSEL	502D 0740h
744h	8	INPUTXBAR_INPUTXBAR25_G0	502D 0744h
748h	8	INPUTXBAR_INPUTXBAR25_G1	502D 0748h
780h	0	INPUTXBAR_INPUTXBAR26_GSEL	502D 0780h
784h	8	INPUTXBAR_INPUTXBAR26_G0	502D 0784h
788h	8	INPUTXBAR_INPUTXBAR26_G1	502D 0788h
7C0h	0	INPUTXBAR_INPUTXBAR27_GSEL	502D 07C0h
7C4h	8	INPUTXBAR_INPUTXBAR27_G0	502D 07C4h
7C8h	8	INPUTXBAR_INPUTXBAR27_G1	502D 07C8h
800h	0	INPUTXBAR_INPUTXBAR28_GSEL	502D 0800h
804h	8	INPUTXBAR_INPUTXBAR28_G0	502D 0804h
808h	8	INPUTXBAR_INPUTXBAR28_G1	502D 0808h
840h	0	INPUTXBAR_INPUTXBAR29_GSEL	502D 0840h
844h	8	INPUTXBAR_INPUTXBAR29_G0	502D 0844h
848h	8	INPUTXBAR_INPUTXBAR29_G1	502D 0848h
880h	0	INPUTXBAR_INPUTXBAR30_GSEL	502D 0880h
884h	8	INPUTXBAR_INPUTXBAR30_G0	502D 0884h
888h	8	INPUTXBAR_INPUTXBAR30_G1	502D 0888h
8C0h	0	INPUTXBAR_INPUTXBAR31_GSEL	502D 08C0h
8C4h	8	INPUTXBAR_INPUTXBAR31_G0	502D 08C4h
8C8h	8	INPUTXBAR_INPUTXBAR31_G1	502D 08C8h

3.14.1 CONTROLSS_INPUTXBAR_PID Registers

3.14.1.1 INPUTXBAR_PID Register (Offset = 0h) [reset = h]

Short Description: PID register

Long Description:

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Table 3-1341. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0000h

Access Types Legend

Table 3-1342. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	PID_MSB16	RO	6180h	Not Defined
15 - 11	PID_MISC	RO	0h	Not Defined
10 - 8	PID_MAJOR	RO	2h	Not Defined
7 - 6	PID_CUSTOM	RO	0h	Not Defined
5 - 0	PID_MINOR	RO	14h	Not Defined

3.14.2 CONTROLSS_INPUTXBARn_GSEL Registers

3.14.2.1 INPUTXBARn_GSEL Register (Offset = 100h) [reset = h]

Short Description: RW

Long Description:

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Equation Description:

N=0x100+0x40*n* where *n* goes from 0-31 (1)

Table 3-1343. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0**N**h

Access Types Legend

Table 3-1344. GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GSEL	RW	0h	Select input source Group:0 G0 selected1 G1 selected

3.14.3 CONTROLSS_INPUTXBARn_G0 Registers

3.14.3.1 INPUTXBARn_G0 Register (Offset = 104h) [reset = h]

Short Description: RW

Long Description:

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Equation Description

:

N=0x104+0x40*n* where *n* goes from 0-31 (2)

Table 3-1345. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0**N**h

Access Types Legend

Table 3-1346. G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	SEL	RW	0h	Select input source:0 G0.0 selected..x G0.x selected

3.14.4 CONTROLSS_INPUTXBARn_G1 Registers

3.14.4.1 INPUTXBARn_G1 Register (Offset = 108h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x108+0x40*n* where *n* goes from 0-31 (3)

Table 3-1347. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0**N**h

Access Types Legend

Table 3-1348. G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	Select input source:0 G1.0 selected..31 G1.31 selected

3.14.5 Access Table

Table 3-1349. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write

3.15 INTXBAR Registers

Table 3-1350. CFG0, CFG0 Registers, Base Address=0X00000000502D5000, Length=4096

Offset	Length	Register Name	intxbar_mmr Physical Address
0h	32	PID	502D 5000h
100h	32	INTXBar0_G0	502D 5100h
104h	32	INTXBar0_G1	502D 5104h
108h	32	INTXBar0_G2	502D 5108h
10Ch	32	INTXBar0_G3	502D 510Ch
110h	32	INTXBar0_G4	502D 5110h
114h	32	INTXBar0_G5	502D 5114h
118h	32	INTXBar0_G6	502D 5118h
140h	32	INTXBar1_G0	502D 5140h
144h	32	INTXBar1_G1	502D 5144h
148h	32	INTXBar1_G2	502D 5148h
14Ch	32	INTXBar1_G3	502D 514Ch
150h	32	INTXBar1_G4	502D 5150h
154h	32	INTXBar1_G5	502D 5154h
158h	32	INTXBar1_G6	502D 5158h
180h	32	INTXBar2_G0	502D 5180h
184h	32	INTXBar2_G1	502D 5184h
188h	32	INTXBar2_G2	502D 5188h
18Ch	32	INTXBar2_G3	502D 518Ch
190h	32	INTXBar2_G4	502D 5190h
194h	32	INTXBar2_G5	502D 5194h
198h	32	INTXBar2_G6	502D 5198h
1C0h	32	INTXBar3_G0	502D 51C0h
1C4h	32	INTXBar3_G1	502D 51C4h
1C8h	32	INTXBar3_G2	502D 51C8h
1CCh	32	INTXBar3_G3	502D 51CCh
1D0h	32	INTXBar3_G4	502D 51D0h
1D4h	32	INTXBar3_G5	502D 51D4h
1D8h	32	INTXBar3_G6	502D 51D8h
200h	32	INTXBar4_G0	502D 5200h
204h	32	INTXBar4_G1	502D 5204h
208h	32	INTXBar4_G2	502D 5208h
20Ch	32	INTXBar4_G3	502D 520Ch
210h	32	INTXBar4_G4	502D 5210h
214h	32	INTXBar4_G5	502D 5214h
218h	32	INTXBar4_G6	502D 5218h
240h	32	INTXBar5_G0	502D 5240h
244h	32	INTXBar5_G1	502D 5244h
248h	32	INTXBar5_G2	502D 5248h
24Ch	32	INTXBar5_G3	502D 524Ch
250h	32	INTXBar5_G4	502D 5250h
254h	32	INTXBar5_G5	502D 5254h
258h	32	INTXBar5_G6	502D 5258h
280h	32	INTXBar6_G0	502D 5280h
284h	32	INTXBar6_G1	502D 5284h

Table 3-1350. CFG0, CFG0 Registers, Base Address=0X00000000502D5000, Length=4096 (continued)

Offset	Length	Register Name	intxbar_mmr Physical Address
288h	32	INTXBar6_G2	502D 5288h
28Ch	32	INTXBar6_G3	502D 528Ch
290h	32	INTXBar6_G4	502D 5290h
294h	32	INTXBar6_G5	502D 5294h
298h	32	INTXBar6_G6	502D 5298h
2C0h	32	INTXBar7_G0	502D 52C0h
2C4h	32	INTXBar7_G1	502D 52C4h
2C8h	32	INTXBar7_G2	502D 52C8h
2CCh	32	INTXBar7_G3	502D 52CCh
2D0h	32	INTXBar7_G4	502D 52D0h
2D4h	32	INTXBar7_G5	502D 52D4h
2D8h	32	INTXBar7_G6	502D 52D8h
300h	32	INTXBar8_G0	502D 5300h
304h	32	INTXBar8_G1	502D 5304h
308h	32	INTXBar8_G2	502D 5308h
30Ch	32	INTXBar8_G3	502D 530Ch
310h	32	INTXBar8_G4	502D 5310h
314h	32	INTXBar8_G5	502D 5314h
318h	32	INTXBar8_G6	502D 5318h
340h	32	INTXBar9_G0	502D 5340h
344h	32	INTXBar9_G1	502D 5344h
348h	32	INTXBar9_G2	502D 5348h
34Ch	32	INTXBar9_G3	502D 534Ch
350h	32	INTXBar9_G4	502D 5350h
354h	32	INTXBar9_G5	502D 5354h
358h	32	INTXBar9_G6	502D 5358h
380h	32	INTXBar10_G0	502D 5380h
384h	32	INTXBar10_G1	502D 5384h
388h	32	INTXBar10_G2	502D 5388h
38Ch	32	INTXBar10_G3	502D 538Ch
390h	32	INTXBar10_G4	502D 5390h
394h	32	INTXBar10_G5	502D 5394h
398h	32	INTXBar10_G6	502D 5398h
3C0h	32	INTXBar11_G0	502D 53C0h
3C4h	32	INTXBar11_G1	502D 53C4h
3C8h	32	INTXBar11_G2	502D 53C8h
3CCh	32	INTXBar11_G3	502D 53CCh
3D0h	32	INTXBar11_G4	502D 53D0h
3D4h	32	INTXBar11_G5	502D 53D4h
3D8h	32	INTXBar11_G6	502D 53D8h
400h	32	INTXBar12_G0	502D 5400h
404h	32	INTXBar12_G1	502D 5404h
408h	32	INTXBar12_G2	502D 5408h
40Ch	32	INTXBar12_G3	502D 540Ch
410h	32	INTXBar12_G4	502D 5410h
414h	32	INTXBar12_G5	502D 5414h
418h	32	INTXBar12_G6	502D 5418h

Table 3-1350. CFG0, CFG0 Registers, Base Address=0X00000000502D5000, Length=4096 (continued)

Offset	Length	Register Name	intxbar_mmr Physical Address
440h	32	INTXBar13_G0	502D 5440h
444h	32	INTXBar13_G1	502D 5444h
448h	32	INTXBar13_G2	502D 5448h
44Ch	32	INTXBar13_G3	502D 544Ch
450h	32	INTXBar13_G4	502D 5450h
454h	32	INTXBar13_G5	502D 5454h
458h	32	INTXBar13_G6	502D 5458h
480h	32	INTXBar14_G0	502D 5480h
484h	32	INTXBar14_G1	502D 5484h
488h	32	INTXBar14_G2	502D 5488h
48Ch	32	INTXBar14_G3	502D 548Ch
490h	32	INTXBar14_G4	502D 5490h
494h	32	INTXBar14_G5	502D 5494h
498h	32	INTXBar14_G6	502D 5498h
4C0h	32	INTXBar15_G0	502D 54C0h
4C4h	32	INTXBar15_G1	502D 54C4h
4C8h	32	INTXBar15_G2	502D 54C8h
4CCh	32	INTXBar15_G3	502D 54CCh
4D0h	32	INTXBar15_G4	502D 54D0h
4D4h	32	INTXBar15_G5	502D 54D4h
4D8h	32	INTXBar15_G6	502D 54D8h
500h	32	INTXBar16_G0	502D 5500h
504h	32	INTXBar16_G1	502D 5504h
508h	32	INTXBar16_G2	502D 5508h
50Ch	32	INTXBar16_G3	502D 550Ch
510h	32	INTXBar16_G4	502D 5510h
514h	32	INTXBar16_G5	502D 5514h
518h	32	INTXBar16_G6	502D 5518h
540h	32	INTXBar17_G0	502D 5540h
544h	32	INTXBar17_G1	502D 5544h
548h	32	INTXBar17_G2	502D 5548h
54Ch	32	INTXBar17_G3	502D 554Ch
550h	32	INTXBar17_G4	502D 5550h
554h	32	INTXBar17_G5	502D 5554h
558h	32	INTXBar17_G6	502D 5558h
580h	32	INTXBar18_G0	502D 5580h
584h	32	INTXBar18_G1	502D 5584h
588h	32	INTXBar18_G2	502D 5588h
58Ch	32	INTXBar18_G3	502D 558Ch
590h	32	INTXBar18_G4	502D 5590h
594h	32	INTXBar18_G5	502D 5594h
598h	32	INTXBar18_G6	502D 5598h
5C0h	32	INTXBar19_G0	502D 55C0h
5C4h	32	INTXBar19_G1	502D 55C4h
5C8h	32	INTXBar19_G2	502D 55C8h
5CCh	32	INTXBar19_G3	502D 55CCh
5D0h	32	INTXBar19_G4	502D 55D0h

Table 3-1350. CFG0, CFG0 Registers, Base Address=0X00000000502D5000, Length=4096 (continued)

Offset	Length	Register Name	intxbar_mmr Physical Address
5D4h	32	INTXBar19_G5	502D 55D4h
5D8h	32	INTXBar19_G6	502D 55D8h
600h	32	INTXBar20_G0	502D 5600h
604h	32	INTXBar20_G1	502D 5604h
608h	32	INTXBar20_G2	502D 5608h
60Ch	32	INTXBar20_G3	502D 560Ch
610h	32	INTXBar20_G4	502D 5610h
614h	32	INTXBar20_G5	502D 5614h
618h	32	INTXBar20_G6	502D 5618h
640h	32	INTXBar21_G0	502D 5640h
644h	32	INTXBar21_G1	502D 5644h
648h	32	INTXBar21_G2	502D 5648h
64Ch	32	INTXBar21_G3	502D 564Ch
650h	32	INTXBar21_G4	502D 5650h
654h	32	INTXBar21_G5	502D 5654h
658h	32	INTXBar21_G6	502D 5658h
680h	32	INTXBar22_G0	502D 5680h
684h	32	INTXBar22_G1	502D 5684h
688h	32	INTXBar22_G2	502D 5688h
68Ch	32	INTXBar22_G3	502D 568Ch
690h	32	INTXBar22_G4	502D 5690h
694h	32	INTXBar22_G5	502D 5694h
698h	32	INTXBar22_G6	502D 5698h
6C0h	32	INTXBar23_G0	502D 56C0h
6C4h	32	INTXBar23_G1	502D 56C4h
6C8h	32	INTXBar23_G2	502D 56C8h
6CCh	32	INTXBar23_G3	502D 56CCh
6D0h	32	INTXBar23_G4	502D 56D0h
6D4h	32	INTXBar23_G5	502D 56D4h
6D8h	32	INTXBar23_G6	502D 56D8h
700h	32	INTXBar24_G0	502D 5700h
704h	32	INTXBar24_G1	502D 5704h
708h	32	INTXBar24_G2	502D 5708h
70Ch	32	INTXBar24_G3	502D 570Ch
710h	32	INTXBar24_G4	502D 5710h
714h	32	INTXBar24_G5	502D 5714h
718h	32	INTXBar24_G6	502D 5718h
740h	32	INTXBar25_G0	502D 5740h
744h	32	INTXBar25_G1	502D 5744h
748h	32	INTXBar25_G2	502D 5748h
74Ch	32	INTXBar25_G3	502D 574Ch
750h	32	INTXBar25_G4	502D 5750h
754h	32	INTXBar25_G5	502D 5754h
758h	32	INTXBar25_G6	502D 5758h
780h	32	INTXBar26_G0	502D 5780h
784h	32	INTXBar26_G1	502D 5784h
788h	32	INTXBar26_G2	502D 5788h

Table 3-1350. CFG0, CFG0 Registers, Base Address=0X00000000502D5000, Length=4096 (continued)

Offset	Length	Register Name	intxbar_mmr Physical Address
78Ch	32	INTXBar26_G3	502D 578Ch
790h	32	INTXBar26_G4	502D 5790h
794h	32	INTXBar26_G5	502D 5794h
798h	32	INTXBar26_G6	502D 5798h
7C0h	32	INTXBar27_G0	502D 57C0h
7C4h	32	INTXBar27_G1	502D 57C4h
7C8h	32	INTXBar27_G2	502D 57C8h
7CCh	32	INTXBar27_G3	502D 57CCh
7D0h	32	INTXBar27_G4	502D 57D0h
7D4h	32	INTXBar27_G5	502D 57D4h
7D8h	32	INTXBar27_G6	502D 57D8h
800h	32	INTXBar28_G0	502D 5800h
804h	32	INTXBar28_G1	502D 5804h
808h	32	INTXBar28_G2	502D 5808h
80Ch	32	INTXBar28_G3	502D 580Ch
810h	32	INTXBar28_G4	502D 5810h
814h	32	INTXBar28_G5	502D 5814h
818h	32	INTXBar28_G6	502D 5818h
840h	32	INTXBar29_G0	502D 5840h
844h	32	INTXBar29_G1	502D 5844h
848h	32	INTXBar29_G2	502D 5848h
84Ch	32	INTXBar29_G3	502D 584Ch
850h	32	INTXBar29_G4	502D 5850h
854h	32	INTXBar29_G5	502D 5854h
858h	32	INTXBar29_G6	502D 5858h
880h	32	INTXBar30_G0	502D 5880h
884h	32	INTXBar30_G1	502D 5884h
888h	32	INTXBar30_G2	502D 5888h
88Ch	32	INTXBar30_G3	502D 588Ch
890h	32	INTXBar30_G4	502D 5890h
894h	32	INTXBar30_G5	502D 5894h
898h	32	INTXBar30_G6	502D 5898h
8C0h	32	INTXBar31_G0	502D 58C0h
8C4h	32	INTXBar31_G1	502D 58C4h
8C8h	32	INTXBar31_G2	502D 58C8h
8CCh	32	INTXBar31_G3	502D 58CCh
8D0h	32	INTXBar31_G4	502D 58D0h
8D4h	32	INTXBar31_G5	502D 58D4h
8D8h	32	INTXBar31_G6	502D 58D8h

3.15.1 CFG0_PID Registers

3.15.1.1 CFG0_PID Register (Offset = 0h) [reset = 61800215h]

Short Description: PID register

Long Description: PID register

Return to Summary Table

Table 3-1351. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5000h

Figure 3-611. PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PID_MSB16															
R															
6180h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_MISC					PID_MAJOR			PID_CUSTOM		PID_MINOR					
R					R			R		R					
0h					2h			0h		15h					

Access Types Legend

Table 3-1352. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR	R	15h	Reset Source: mod_g_rst_n

3.15.2 CFG0_INTXBAR0_G0 Registers

3.15.2.1 CFG0_G0 Register (Offset = 100h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1353. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5100h

Figure 3-612. INTXBAR0_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR0_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR0_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1354. INTXBAR0_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR0_G0_SEL	R/W	0h	ETPWM INT interrupt to corresponding xbar 1: PWMx.INT is selected 0: PWMx.INT is de-selected Reset Source: mod_g_rst_n

3.15.3 CFG0_INTXBAR0_G1 Registers

3.15.3.1 CFG0_G1 Register (Offset = 104h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1355. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5104h

Figure 3-613. INTXBAR0_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR0_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR0_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1356. INTXBAR0_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR0_G1_SEL	R/W	0h	ETPWM TZINT interrupt to corresponding xbar 1: PWMx.TZINT is selected 0: PWMx.TZINT is de-selected Reset Source: mod_g_rst_n

3.15.4 CFG0_INTXBAR0_G2 Registers

3.15.4.1 CFG0_G2 Register (Offset = 108h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1357. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5108h

Figure 3-614. INTXBAR0_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							INTXBAR0_G2_SEL								
NONE							R/W								
0							0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR0_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1358. INTXBAR0_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24:0	INTXBAR0_G2_SEL	R/W	0h	Corresponding INT XBar G2 Input Select 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.15.5 CFG0_INTXBAR0_G3 Registers

3.15.5.1 CFG0_G3 Register (Offset = 10Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1359. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 510Ch

Figure 3-615. INTXBAR0_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR0_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-1360. INTXBAR0_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	INTXBAR0_G3_SEL	R/W	0h	Corresponding INT XBar G3 Input Select 0: FSIRX0.INT1N 1: FSIRX0.INT2N 2: FSIRX1.INT1N 3: FSIRX1.INT2N 4: FSIRX2.INT1N 5: FSIRX2.INT2N 6: FSIRX3.INT1N 7: FSIRX3.INT2N 8: FSITX0.INT1N 9: FSITX0.INT2N 10: FSITX1.INT1N 11: FSITX1.INT2N 12: FSITX2.INT1N 13: FSITX2.INT2N 14: FSITX3.INT1N 15: FSITX3.INT2N Reset Source: mod_g_rst_n

3.15.6 CFG0_INTXBAR0_G4 Registers

3.15.6.1 CFG0_G4 Register (Offset = 110h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1361. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5110h

Figure 3-616. INTXBAR0_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR0_G4_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1362. INTXBAR0_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR0_G4_SEL	R/W	0h	Corresponding INT XBar G4 Input Select 0: SD0.ERR 1: SD0.FILT1.DRINT 2: SD0.FILT2.DRINT 3: SD0.FILT3.DRINT 4: SD0.FILT4.DRINT 5: SD1.ERR 6: SD1.FILT1.DRINT 7: SD1.FILT2.DRINT 8: SD1.FILT3.DRINT 9: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.15.7 CFG0_INTXBAR0_G5 Registers

3.15.7.1 CFG0_G5 Register (Offset = 114h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1363. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5114h

Figure 3-617. INTXBAR0_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR0_G5_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1364. INTXBAR0_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR0_G5_SEL	R/W	0h	Corresponding INT XBar G5 Input Select 0: ECAP0.INT 1: ECAP1.INT 2: ECAP2.INT 3: ECAP3.INT 4: ECAP4.INT 5: ECAP5.INT 6: ECAP6.INT 7: ECAP7.INT 8: ECAP8.INT 9: ECAP9.INT Reset Source: mod_g_rst_n

3.15.8 CFG0_INTXBAR0_G6 Registers

3.15.8.1 CFG0_G6 Register (Offset = 118h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1365. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5118h

Figure 3-618. INTXBAR0_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													INTXBAR0_G6_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1366. INTXBAR0_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	INTXBAR0_G6_SEL	R/W	0h	Corresponding INT XBar G6 Input Select 0: EQEP0.INT 1: EQEP1.INT 2: EQEP2.INT Reset Source: mod_g_rst_n

3.15.9 CFG0_INTXBAR1_G0 Registers

3.15.9.1 CFG0_G0 Register (Offset = 140h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1367. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5140h

Figure 3-619. INTXBAR1_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR1_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR1_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1368. INTXBAR1_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR1_G0_SEL	R/W	0h	ETPWM INT interrupt to corresponding xbar 1: PWMx.INT is selected 0: PWMx.INT is de-selected Reset Source: mod_g_rst_n

3.15.10 CFG0_INTXBAR1_G1 Registers

3.15.10.1 CFG0_G1 Register (Offset = 144h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1369. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5144h

Figure 3-620. INTXBAR1_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR1_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR1_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1370. INTXBAR1_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR1_G1_SEL	R/W	0h	ETPWM TZINT interrupt to corresponding xbar 1: PWMx.TZINT is selected 0: PWMx.TZINT is de-selected Reset Source: mod_g_rst_n

3.15.11 CFG0_INTXBAR1_G2 Registers

3.15.11.1 CFG0_G2 Register (Offset = 148h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1371. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5148h

Figure 3-621. INTXBAR1_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							INTXBAR1_G2_SEL								
NONE							R/W								
0							0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR1_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1372. INTXBAR1_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24:0	INTXBAR1_G2_SEL	R/W	0h	Corresponding INT XBar G2 Input Select 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.15.12 CFG0_INTXBAR1_G3 Registers

3.15.12.1 CFG0_G3 Register (Offset = 14Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1373. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 514Ch

Figure 3-622. INTXBAR1_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR1_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-1374. INTXBAR1_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	INTXBAR1_G3_SEL	R/W	0h	Corresponding INT XBar G3 Input Select 0: FSIRX0.INT1N 1: FSIRX0.INT2N 2: FSIRX1.INT1N 3: FSIRX1.INT2N 4: FSIRX2.INT1N 5: FSIRX2.INT2N 6: FSIRX3.INT1N 7: FSIRX3.INT2N 8: FSITX0.INT1N 9: FSITX0.INT2N 10: FSITX1.INT1N 11: FSITX1.INT2N 12: FSITX2.INT1N 13: FSITX2.INT2N 14: FSITX3.INT1N 15: FSITX3.INT2N Reset Source: mod_g_rst_n

3.15.13 CFG0_INTXBAR1_G4 Registers

3.15.13.1 CFG0_G4 Register (Offset = 150h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1375. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5150h

Figure 3-623. INTXBAR1_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR1_G4_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1376. INTXBAR1_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR1_G4_SEL	R/W	0h	Corresponding INT XBar G4 Input Select 0: SD0.ERR 1: SD0.FILT1.DRINT 2: SD0.FILT2.DRINT 3: SD0.FILT3.DRINT 4: SD0.FILT4.DRINT 5: SD1.ERR 6: SD1.FILT1.DRINT 7: SD1.FILT2.DRINT 8: SD1.FILT3.DRINT 9: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.15.14 CFG0_INTXBAR1_G5 Registers

3.15.14.1 CFG0_G5 Register (Offset = 154h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1377. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5154h

Figure 3-624. INTXBAR1_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR1_G5_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1378. INTXBAR1_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR1_G5_SEL	R/W	0h	Corresponding INT XBar G5 Input Select 0: ECAP0.INT 1: ECAP1.INT 2: ECAP2.INT 3: ECAP3.INT 4: ECAP4.INT 5: ECAP5.INT 6: ECAP6.INT 7: ECAP7.INT 8: ECAP8.INT 9: ECAP9.INT Reset Source: mod_g_rst_n

3.15.15 CFG0_INTXBAR1_G6 Registers

3.15.15.1 CFG0_G6 Register (Offset = 158h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1379. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5158h

Figure 3-625. INTXBAR1_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															INTXBAR1_G6_SEL
NONE															R/W
0															0h

Access Types Legend

Table 3-1380. INTXBAR1_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	INTXBAR1_G6_SEL	R/W	0h	Corresponding INT XBar G6 Input Select 0: EQEP0.INT 1: EQEP1.INT 2: EQEP2.INT Reset Source: mod_g_rst_n

3.15.16 CFG0_INTXBAR2_G0 Registers

3.15.16.1 CFG0_G0 Register (Offset = 180h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1381. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5180h

Figure 3-626. INTXBAR2_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR2_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR2_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1382. INTXBAR2_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR2_G0_SEL	R/W	0h	ETPWM INT interrupt to corresponding xbar 1: PWMx.INT is selected 0: PWMx.INT is de-selected Reset Source: mod_g_rst_n

3.15.17 CFG0_INTXBAR2_G1 Registers

3.15.17.1 CFG0_G1 Register (Offset = 184h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1383. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5184h

Figure 3-627. INTXBAR2_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR2_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR2_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1384. INTXBAR2_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR2_G1_SEL	R/W	0h	ETPWM TZINT interrupt to corresponding xbar 1: PWMx.TZINT is selected 0: PWMx.TZINT is de-selected Reset Source: mod_g_rst_n

3.15.18 CFG0_INTXBAR2_G2 Registers

3.15.18.1 CFG0_G2 Register (Offset = 188h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1385. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5188h

Figure 3-628. INTXBAR2_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							INTXBAR2_G2_SEL								
NONE							R/W								
0							0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR2_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1386. INTXBAR2_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24:0	INTXBAR2_G2_SEL	R/W	0h	Corresponding INT XBar G2 Input Select 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.15.19 CFG0_INTXBAR2_G3 Registers

3.15.19.1 CFG0_G3 Register (Offset = 18Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1387. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 518Ch

Figure 3-629. INTXBAR2_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR2_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-1388. INTXBAR2_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	INTXBAR2_G3_SEL	R/W	0h	Corresponding INT XBar G3 Input Select 0: FSIRX0.INT1N 1: FSIRX0.INT2N 2: FSIRX1.INT1N 3: FSIRX1.INT2N 4: FSIRX2.INT1N 5: FSIRX2.INT2N 6: FSIRX3.INT1N 7: FSIRX3.INT2N 8: FSITX0.INT1N 9: FSITX0.INT2N 10: FSITX1.INT1N 11: FSITX1.INT2N 12: FSITX2.INT1N 13: FSITX2.INT2N 14: FSITX3.INT1N 15: FSITX3.INT2N Reset Source: mod_g_rst_n

3.15.20 CFG0_INTXBAR2_G4 Registers

3.15.20.1 CFG0_G4 Register (Offset = 190h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1389. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5190h

Figure 3-630. INTXBAR2_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR2_G4_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1390. INTXBAR2_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR2_G4_SEL	R/W	0h	Corresponding INT XBar G4 Input Select 0: SD0.ERR 1: SD0.FILT1.DRINT 2: SD0.FILT2.DRINT 3: SD0.FILT3.DRINT 4: SD0.FILT4.DRINT 5: SD1.ERR 6: SD1.FILT1.DRINT 7: SD1.FILT2.DRINT 8: SD1.FILT3.DRINT 9: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.15.21 CFG0_INTXBAR2_G5 Registers

3.15.21.1 CFG0_G5 Register (Offset = 194h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1391. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5194h

Figure 3-631. INTXBAR2_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR2_G5_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1392. INTXBAR2_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR2_G5_SEL	R/W	0h	Corresponding INT XBar G5 Input Select 0: ECAP0.INT 1: ECAP1.INT 2: ECAP2.INT 3: ECAP3.INT 4: ECAP4.INT 5: ECAP5.INT 6: ECAP6.INT 7: ECAP7.INT 8: ECAP8.INT 9: ECAP9.INT Reset Source: mod_g_rst_n

3.15.22 CFG0_INTXBAR2_G6 Registers

3.15.22.1 CFG0_G6 Register (Offset = 198h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1393. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5198h

Figure 3-632. INTXBAR2_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													INTXBAR2_G6_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1394. INTXBAR2_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	INTXBAR2_G6_SEL	R/W	0h	Corresponding INT XBar G6 Input Select 0: EQEP0.INT 1: EQEP1.INT 2: EQEP2.INT Reset Source: mod_g_rst_n

3.15.23 CFG0_INTXBAR3_G0 Registers

3.15.23.1 CFG0_G0 Register (Offset = 1C0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1395. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 51C0h

Figure 3-633. INTXBAR3_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR3_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR3_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1396. INTXBAR3_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR3_G0_SEL	R/W	0h	ETPWM INT interrupt to corresponding xbar 1: PWMx.INT is selected 0: PWMx.INT is de-selected Reset Source: mod_g_rst_n

3.15.24 CFG0_INTXBAR3_G1 Registers

3.15.24.1 CFG0_G1 Register (Offset = 1C4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1397. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 51C4h

Figure 3-634. INTXBAR3_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR3_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR3_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1398. INTXBAR3_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR3_G1_SEL	R/W	0h	ETPWM TZINT interrupt to corresponding xbar 1: PWMx.TZINT is selected 0: PWMx.TZINT is de-selected Reset Source: mod_g_rst_n

3.15.25 CFG0_INTXBAR3_G2 Registers

3.15.25.1 CFG0_G2 Register (Offset = 1C8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1399. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 51C8h

Figure 3-635. INTXBAR3_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							INTXBAR3_G2_SEL								
NONE							R/W								
0							0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR3_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1400. INTXBAR3_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24:0	INTXBAR3_G2_SEL	R/W	0h	Corresponding INT XBar G2 Input Select 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.15.26 CFG0_INTXBAR3_G3 Registers

3.15.26.1 CFG0_G3 Register (Offset = 1CCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1401. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 51CCh

Figure 3-636. INTXBAR3_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR3_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-1402. INTXBAR3_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	INTXBAR3_G3_SEL	R/W	0h	Corresponding INT XBar G3 Input Select 0: FSIRX0.INT1N 1: FSIRX0.INT2N 2: FSIRX1.INT1N 3: FSIRX1.INT2N 4: FSIRX2.INT1N 5: FSIRX2.INT2N 6: FSIRX3.INT1N 7: FSIRX3.INT2N 8: FSITX0.INT1N 9: FSITX0.INT2N 10: FSITX1.INT1N 11: FSITX1.INT2N 12: FSITX2.INT1N 13: FSITX2.INT2N 14: FSITX3.INT1N 15: FSITX3.INT2N Reset Source: mod_g_rst_n

3.15.27 CFG0_INTXBAR3_G4 Registers

3.15.27.1 CFG0_G4 Register (Offset = 1D0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1403. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 51D0h

Figure 3-637. INTXBAR3_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR3_G4_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1404. INTXBAR3_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR3_G4_SEL	R/W	0h	Corresponding INT XBar G4 Input Select 0: SD0.ERR 1: SD0.FILT1.DRINT 2: SD0.FILT2.DRINT 3: SD0.FILT3.DRINT 4: SD0.FILT4.DRINT 5: SD1.ERR 6: SD1.FILT1.DRINT 7: SD1.FILT2.DRINT 8: SD1.FILT3.DRINT 9: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.15.28 CFG0_INTXBAR3_G5 Registers

3.15.28.1 CFG0_G5 Register (Offset = 1D4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1405. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 51D4h

Figure 3-638. INTXBAR3_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR3_G5_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1406. INTXBAR3_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR3_G5_SEL	R/W	0h	Corresponding INT XBar G5 Input Select 0: ECAP0.INT 1: ECAP1.INT 2: ECAP2.INT 3: ECAP3.INT 4: ECAP4.INT 5: ECAP5.INT 6: ECAP6.INT 7: ECAP7.INT 8: ECAP8.INT 9: ECAP9.INT Reset Source: mod_g_rst_n

3.15.29 CFG0_INTXBAR3_G6 Registers

3.15.29.1 CFG0_G6 Register (Offset = 1D8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1407. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 51D8h

Figure 3-639. INTXBAR3_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														INTXBAR3_G6_SEL	
NONE														R/W	
0														0h	

Access Types Legend

Table 3-1408. INTXBAR3_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	INTXBAR3_G6_SEL	R/W	0h	Corresponding INT XBar G6 Input Select 0: EQEP0.INT 1: EQEP1.INT 2: EQEP2.INT Reset Source: mod_g_rst_n

3.15.30 CFG0_INTXBAR4_G0 Registers

3.15.30.1 CFG0_G0 Register (Offset = 200h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1409. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5200h

Figure 3-640. INTXBAR4_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR4_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR4_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1410. INTXBAR4_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR4_G0_SEL	R/W	0h	ETPWM INT interrupt to corresponding xbar 1: PWMx.INT is selected 0: PWMx.INT is de-selected Reset Source: mod_g_rst_n

3.15.31 CFG0_INTXBAR4_G1 Registers

3.15.31.1 CFG0_G1 Register (Offset = 204h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1411. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5204h

Figure 3-641. INTXBAR4_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR4_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR4_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1412. INTXBAR4_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR4_G1_SEL	R/W	0h	ETPWM TZINT interrupt to corresponding xbar 1: PWMx.TZINT is selected 0: PWMx.TZINT is de-selected Reset Source: mod_g_rst_n

3.15.32 CFG0_INTXBAR4_G2 Registers

3.15.32.1 CFG0_G2 Register (Offset = 208h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1413. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5208h

Figure 3-642. INTXBAR4_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							INTXBAR4_G2_SEL								
NONE							R/W								
0							0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR4_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1414. INTXBAR4_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24:0	INTXBAR4_G2_SEL	R/W	0h	Corresponding INT XBar G2 Input Select 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.15.33 CFG0_INTXBAR4_G3 Registers

3.15.33.1 CFG0_G3 Register (Offset = 20Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1415. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 520Ch

Figure 3-643. INTXBAR4_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR4_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-1416. INTXBAR4_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	INTXBAR4_G3_SEL	R/W	0h	Corresponding INT XBar G3 Input Select 0: FSIRX0.INT1N 1: FSIRX0.INT2N 2: FSIRX1.INT1N 3: FSIRX1.INT2N 4: FSIRX2.INT1N 5: FSIRX2.INT2N 6: FSIRX3.INT1N 7: FSIRX3.INT2N 8: FSITX0.INT1N 9: FSITX0.INT2N 10: FSITX1.INT1N 11: FSITX1.INT2N 12: FSITX2.INT1N 13: FSITX2.INT2N 14: FSITX3.INT1N 15: FSITX3.INT2N Reset Source: mod_g_rst_n

3.15.34 CFG0_INTXBAR4_G4 Registers

3.15.34.1 CFG0_G4 Register (Offset = 210h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1417. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5210h

Figure 3-644. INTXBAR4_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR4_G4_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1418. INTXBAR4_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR4_G4_SEL	R/W	0h	Corresponding INT XBar G4 Input Select 0: SD0.ERR 1: SD0.FILT1.DRINT 2: SD0.FILT2.DRINT 3: SD0.FILT3.DRINT 4: SD0.FILT4.DRINT 5: SD1.ERR 6: SD1.FILT1.DRINT 7: SD1.FILT2.DRINT 8: SD1.FILT3.DRINT 9: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.15.35 CFG0_INTXBAR4_G5 Registers

3.15.35.1 CFG0_G5 Register (Offset = 214h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1419. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5214h

Figure 3-645. INTXBAR4_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR4_G5_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1420. INTXBAR4_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR4_G5_SEL	R/W	0h	Corresponding INT XBar G5 Input Select 0: ECAP0.INT 1: ECAP1.INT 2: ECAP2.INT 3: ECAP3.INT 4: ECAP4.INT 5: ECAP5.INT 6: ECAP6.INT 7: ECAP7.INT 8: ECAP8.INT 9: ECAP9.INT Reset Source: mod_g_rst_n

3.15.36 CFG0_INTXBAR4_G6 Registers

3.15.36.1 CFG0_G6 Register (Offset = 218h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1421. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5218h

Figure 3-646. INTXBAR4_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													INTXBAR4_G6_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1422. INTXBAR4_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	INTXBAR4_G6_SEL	R/W	0h	Corresponding INT XBar G6 Input Select 0: EQEP0.INT 1: EQEP1.INT 2: EQEP2.INT Reset Source: mod_g_rst_n

3.15.37 CFG0_INTXBAR5_G0 Registers

3.15.37.1 CFG0_G0 Register (Offset = 240h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1423. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5240h

Figure 3-647. INTXBAR5_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR5_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR5_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1424. INTXBAR5_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR5_G0_SEL	R/W	0h	ETPWM INT interrupt to corresponding xbar 1: PWMx.INT is selected 0: PWMx.INT is de-selected Reset Source: mod_g_rst_n

3.15.38 CFG0_INTXBAR5_G1 Registers

3.15.38.1 CFG0_G1 Register (Offset = 244h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1425. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5244h

Figure 3-648. INTXBAR5_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR5_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR5_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1426. INTXBAR5_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR5_G1_SEL	R/W	0h	ETPWM TZINT interrupt to corresponding xbar 1: PWMx.TZINT is selected 0: PWMx.TZINT is de-selected Reset Source: mod_g_rst_n

3.15.39 CFG0_INTXBAR5_G2 Registers

3.15.39.1 CFG0_G2 Register (Offset = 248h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1427. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5248h

Figure 3-649. INTXBAR5_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							INTXBAR5_G2_SEL								
NONE							R/W								
0							0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR5_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1428. INTXBAR5_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24:0	INTXBAR5_G2_SEL	R/W	0h	Corresponding INT XBar G2 Input Select 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.15.40 CFG0_INTXBAR5_G3 Registers

3.15.40.1 CFG0_G3 Register (Offset = 24Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1429. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 524Ch

Figure 3-650. INTXBAR5_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR5_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-1430. INTXBAR5_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	INTXBAR5_G3_SEL	R/W	0h	Corresponding INT XBar G3 Input Select 0: FSIRX0.INT1N 1: FSIRX0.INT2N 2: FSIRX1.INT1N 3: FSIRX1.INT2N 4: FSIRX2.INT1N 5: FSIRX2.INT2N 6: FSIRX3.INT1N 7: FSIRX3.INT2N 8: FSITX0.INT1N 9: FSITX0.INT2N 10: FSITX1.INT1N 11: FSITX1.INT2N 12: FSITX2.INT1N 13: FSITX2.INT2N 14: FSITX3.INT1N 15: FSITX3.INT2N Reset Source: mod_g_rst_n

3.15.41 CFG0_INTXBAR5_G4 Registers

3.15.41.1 CFG0_G4 Register (Offset = 250h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1431. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5250h

Figure 3-651. INTXBAR5_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR5_G4_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1432. INTXBAR5_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR5_G4_SEL	R/W	0h	Corresponding INT XBar G4 Input Select 0: SD0.ERR 1: SD0.FILT1.DRINT 2: SD0.FILT2.DRINT 3: SD0.FILT3.DRINT 4: SD0.FILT4.DRINT 5: SD1.ERR 6: SD1.FILT1.DRINT 7: SD1.FILT2.DRINT 8: SD1.FILT3.DRINT 9: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.15.42 CFG0_INTXBAR5_G5 Registers

3.15.42.1 CFG0_G5 Register (Offset = 254h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1433. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5254h

Figure 3-652. INTXBAR5_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR5_G5_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1434. INTXBAR5_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR5_G5_SEL	R/W	0h	Corresponding INT XBar G5 Input Select 0: ECAP0.INT 1: ECAP1.INT 2: ECAP2.INT 3: ECAP3.INT 4: ECAP4.INT 5: ECAP5.INT 6: ECAP6.INT 7: ECAP7.INT 8: ECAP8.INT 9: ECAP9.INT Reset Source: mod_g_rst_n

3.15.43 CFG0_INTXBAR5_G6 Registers

3.15.43.1 CFG0_G6 Register (Offset = 258h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1435. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5258h

Figure 3-653. INTXBAR5_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														INTXBAR5_G6_SEL	
NONE														R/W	
0														0h	

Access Types Legend

Table 3-1436. INTXBAR5_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	INTXBAR5_G6_SEL	R/W	0h	Corresponding INT XBar G6 Input Select 0: EQEP0.INT 1: EQEP1.INT 2: EQEP2.INT Reset Source: mod_g_rst_n

3.15.44 CFG0_INTXBAR6_G0 Registers

3.15.44.1 CFG0_G0 Register (Offset = 280h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1437. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5280h

Figure 3-654. INTXBAR6_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR6_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR6_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1438. INTXBAR6_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR6_G0_SEL	R/W	0h	ETPWM INT interrupt to corresponding xbar 1: PWMx.INT is selected 0: PWMx.INT is de-selected Reset Source: mod_g_rst_n

3.15.45 CFG0_INTXBAR6_G1 Registers

3.15.45.1 CFG0_G1 Register (Offset = 284h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1439. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5284h

Figure 3-655. INTXBAR6_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR6_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR6_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1440. INTXBAR6_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR6_G1_SEL	R/W	0h	ETPWM TZINT interrupt to corresponding xbar 1: PWMx.TZINT is selected 0: PWMx.TZINT is de-selected Reset Source: mod_g_rst_n

3.15.46 CFG0_INTXBAR6_G2 Registers

3.15.46.1 CFG0_G2 Register (Offset = 288h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1441. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5288h

Figure 3-656. INTXBAR6_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							INTXBAR6_G2_SEL								
NONE							R/W								
0							0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR6_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1442. INTXBAR6_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24:0	INTXBAR6_G2_SEL	R/W	0h	Corresponding INT XBar G2 Input Select 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.15.47 CFG0_INTXBAR6_G3 Registers

3.15.47.1 CFG0_G3 Register (Offset = 28Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1443. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 528Ch

Figure 3-657. INTXBAR6_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR6_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-1444. INTXBAR6_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	INTXBAR6_G3_SEL	R/W	0h	Corresponding INT XBar G3 Input Select 0: FSIRX0.INT1N 1: FSIRX0.INT2N 2: FSIRX1.INT1N 3: FSIRX1.INT2N 4: FSIRX2.INT1N 5: FSIRX2.INT2N 6: FSIRX3.INT1N 7: FSIRX3.INT2N 8: FSITX0.INT1N 9: FSITX0.INT2N 10: FSITX1.INT1N 11: FSITX1.INT2N 12: FSITX2.INT1N 13: FSITX2.INT2N 14: FSITX3.INT1N 15: FSITX3.INT2N Reset Source: mod_g_rst_n

3.15.48 CFG0_INTXBAR6_G4 Registers

3.15.48.1 CFG0_G4 Register (Offset = 290h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1445. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5290h

Figure 3-658. INTXBAR6_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR6_G4_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1446. INTXBAR6_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR6_G4_SEL	R/W	0h	Corresponding INT XBar G4 Input Select 0: SD0.ERR 1: SD0.FILT1.DRINT 2: SD0.FILT2.DRINT 3: SD0.FILT3.DRINT 4: SD0.FILT4.DRINT 5: SD1.ERR 6: SD1.FILT1.DRINT 7: SD1.FILT2.DRINT 8: SD1.FILT3.DRINT 9: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.15.49 CFG0_INTXBAR6_G5 Registers

3.15.49.1 CFG0_G5 Register (Offset = 294h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1447. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5294h

Figure 3-659. INTXBAR6_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR6_G5_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1448. INTXBAR6_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR6_G5_SEL	R/W	0h	Corresponding INT XBar G5 Input Select 0: ECAP0.INT 1: ECAP1.INT 2: ECAP2.INT 3: ECAP3.INT 4: ECAP4.INT 5: ECAP5.INT 6: ECAP6.INT 7: ECAP7.INT 8: ECAP8.INT 9: ECAP9.INT Reset Source: mod_g_rst_n

3.15.50 CFG0_INTXBAR6_G6 Registers

3.15.50.1 CFG0_G6 Register (Offset = 298h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1449. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5298h

Figure 3-660. INTXBAR6_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													INTXBAR6_G6_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1450. INTXBAR6_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	INTXBAR6_G6_SEL	R/W	0h	Corresponding INT XBar G6 Input Select 0: EQEP0.INT 1: EQEP1.INT 2: EQEP2.INT Reset Source: mod_g_rst_n

3.15.51 CFG0_INTXBAR7_G0 Registers

3.15.51.1 CFG0_G0 Register (Offset = 2C0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1451. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 52C0h

Figure 3-661. INTXBAR7_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR7_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR7_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1452. INTXBAR7_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR7_G0_SEL	R/W	0h	ETPWM INT interrupt to corresponding xbar 1: PWMx.INT is selected 0: PWMx.INT is de-selected Reset Source: mod_g_rst_n

3.15.52 CFG0_INTXBAR7_G1 Registers

3.15.52.1 CFG0_G1 Register (Offset = 2C4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1453. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 52C4h

Figure 3-662. INTXBAR7_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR7_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR7_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1454. INTXBAR7_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR7_G1_SEL	R/W	0h	ETPWM TZINT interrupt to corresponding xbar 1: PWMx.TZINT is selected 0: PWMx.TZINT is de-selected Reset Source: mod_g_rst_n

3.15.53 CFG0_INTXBAR7_G2 Registers

3.15.53.1 CFG0_G2 Register (Offset = 2C8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1455. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 52C8h

Figure 3-663. INTXBAR7_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							INTXBAR7_G2_SEL								
NONE							R/W								
0							0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR7_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1456. INTXBAR7_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24:0	INTXBAR7_G2_SEL	R/W	0h	Corresponding INT XBar G2 Input Select 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.15.54 CFG0_INTXBAR7_G3 Registers

3.15.54.1 CFG0_G3 Register (Offset = 2CCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1457. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 52CCh

Figure 3-664. INTXBAR7_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR7_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-1458. INTXBAR7_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	INTXBAR7_G3_SEL	R/W	0h	Corresponding INT XBar G3 Input Select 0: FSIRX0.INT1N 1: FSIRX0.INT2N 2: FSIRX1.INT1N 3: FSIRX1.INT2N 4: FSIRX2.INT1N 5: FSIRX2.INT2N 6: FSIRX3.INT1N 7: FSIRX3.INT2N 8: FSITX0.INT1N 9: FSITX0.INT2N 10: FSITX1.INT1N 11: FSITX1.INT2N 12: FSITX2.INT1N 13: FSITX2.INT2N 14: FSITX3.INT1N 15: FSITX3.INT2N Reset Source: mod_g_rst_n

3.15.55 CFG0_INTXBAR7_G4 Registers

3.15.55.1 CFG0_G4 Register (Offset = 2D0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1459. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 52D0h

Figure 3-665. INTXBAR7_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR7_G4_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1460. INTXBAR7_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR7_G4_SEL	R/W	0h	Corresponding INT XBar G4 Input Select 0: SD0.ERR 1: SD0.FILT1.DRINT 2: SD0.FILT2.DRINT 3: SD0.FILT3.DRINT 4: SD0.FILT4.DRINT 5: SD1.ERR 6: SD1.FILT1.DRINT 7: SD1.FILT2.DRINT 8: SD1.FILT3.DRINT 9: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.15.56 CFG0_INTXBAR7_G5 Registers

3.15.56.1 CFG0_G5 Register (Offset = 2D4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1461. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 52D4h

Figure 3-666. INTXBAR7_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR7_G5_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1462. INTXBAR7_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR7_G5_SEL	R/W	0h	Corresponding INT XBar G5 Input Select 0: ECAP0.INT 1: ECAP1.INT 2: ECAP2.INT 3: ECAP3.INT 4: ECAP4.INT 5: ECAP5.INT 6: ECAP6.INT 7: ECAP7.INT 8: ECAP8.INT 9: ECAP9.INT Reset Source: mod_g_rst_n

3.15.57 CFG0_INTXBAR7_G6 Registers

3.15.57.1 CFG0_G6 Register (Offset = 2D8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1463. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 52D8h

Figure 3-667. INTXBAR7_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													INTXBAR7_G6_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1464. INTXBAR7_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	INTXBAR7_G6_SEL	R/W	0h	Corresponding INT XBar G6 Input Select 0: EQEP0.INT 1: EQEP1.INT 2: EQEP2.INT Reset Source: mod_g_rst_n

3.15.58 CFG0_INTXBAR8_G0 Registers

3.15.58.1 CFG0_G0 Register (Offset = 300h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1465. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5300h

Figure 3-668. INTXBAR8_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR8_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR8_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1466. INTXBAR8_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR8_G0_SEL	R/W	0h	ETPWM INT interrupt to corresponding xbar 1: PWMx.INT is selected 0: PWMx.INT is de-selected Reset Source: mod_g_rst_n

3.15.59 CFG0_INTXBAR8_G1 Registers

3.15.59.1 CFG0_G1 Register (Offset = 304h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1467. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5304h

Figure 3-669. INTXBAR8_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR8_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR8_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1468. INTXBAR8_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR8_G1_SEL	R/W	0h	ETPWM TZINT interrupt to corresponding xbar 1: PWMx.TZINT is selected 0: PWMx.TZINT is de-selected Reset Source: mod_g_rst_n

3.15.60 CFG0_INTXBAR8_G2 Registers

3.15.60.1 CFG0_G2 Register (Offset = 308h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1469. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5308h

Figure 3-670. INTXBAR8_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							INTXBAR8_G2_SEL								
NONE							R/W								
0							0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR8_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1470. INTXBAR8_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24:0	INTXBAR8_G2_SEL	R/W	0h	Corresponding INT XBar G2 Input Select 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.15.61 CFG0_INTXBAR8_G3 Registers

3.15.61.1 CFG0_G3 Register (Offset = 30Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1471. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 530Ch

Figure 3-671. INTXBAR8_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR8_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-1472. INTXBAR8_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	INTXBAR8_G3_SEL	R/W	0h	Corresponding INT XBar G3 Input Select 0: FSIRX0.INT1N 1: FSIRX0.INT2N 2: FSIRX1.INT1N 3: FSIRX1.INT2N 4: FSIRX2.INT1N 5: FSIRX2.INT2N 6: FSIRX3.INT1N 7: FSIRX3.INT2N 8: FSITX0.INT1N 9: FSITX0.INT2N 10: FSITX1.INT1N 11: FSITX1.INT2N 12: FSITX2.INT1N 13: FSITX2.INT2N 14: FSITX3.INT1N 15: FSITX3.INT2N Reset Source: mod_g_rst_n

3.15.62 CFG0_INTXBAR8_G4 Registers

3.15.62.1 CFG0_G4 Register (Offset = 310h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1473. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5310h

Figure 3-672. INTXBAR8_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR8_G4_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1474. INTXBAR8_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR8_G4_SEL	R/W	0h	Corresponding INT XBar G4 Input Select 0: SD0.ERR 1: SD0.FILT1.DRINT 2: SD0.FILT2.DRINT 3: SD0.FILT3.DRINT 4: SD0.FILT4.DRINT 5: SD1.ERR 6: SD1.FILT1.DRINT 7: SD1.FILT2.DRINT 8: SD1.FILT3.DRINT 9: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.15.63 CFG0_INTXBAR8_G5 Registers

3.15.63.1 CFG0_G5 Register (Offset = 314h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1475. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5314h

Figure 3-673. INTXBAR8_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR8_G5_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1476. INTXBAR8_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR8_G5_SEL	R/W	0h	Corresponding INT XBar G5 Input Select 0: ECAP0.INT 1: ECAP1.INT 2: ECAP2.INT 3: ECAP3.INT 4: ECAP4.INT 5: ECAP5.INT 6: ECAP6.INT 7: ECAP7.INT 8: ECAP8.INT 9: ECAP9.INT Reset Source: mod_g_rst_n

3.15.64 CFG0_INTXBAR8_G6 Registers

3.15.64.1 CFG0_G6 Register (Offset = 318h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1477. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5318h

Figure 3-674. INTXBAR8_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															INTXBAR8_G6_SEL
NONE															R/W
0															0h

Access Types Legend

Table 3-1478. INTXBAR8_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	INTXBAR8_G6_SEL	R/W	0h	Corresponding INT XBar G6 Input Select 0: EQEP0.INT 1: EQEP1.INT 2: EQEP2.INT Reset Source: mod_g_rst_n

3.15.65 CFG0_INTXBAR9_G0 Registers

3.15.65.1 CFG0_G0 Register (Offset = 340h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1479. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5340h

Figure 3-675. INTXBAR9_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR9_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR9_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1480. INTXBAR9_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR9_G0_SEL	R/W	0h	ETPWM INT interrupt to corresponding xbar 1: PWMx.INT is selected 0: PWMx.INT is de-selected Reset Source: mod_g_rst_n

3.15.66 CFG0_INTXBAR9_G1 Registers

3.15.66.1 CFG0_G1 Register (Offset = 344h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1481. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5344h

Figure 3-676. INTXBAR9_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR9_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR9_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1482. INTXBAR9_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR9_G1_SEL	R/W	0h	ETPWM TZINT interrupt to corresponding xbar 1: PWMx.TZINT is selected 0: PWMx.TZINT is de-selected Reset Source: mod_g_rst_n

3.15.67 CFG0_INTXBAR9_G2 Registers

3.15.67.1 CFG0_G2 Register (Offset = 348h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1483. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5348h

Figure 3-677. INTXBAR9_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							INTXBAR9_G2_SEL								
NONE							R/W								
0							0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR9_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1484. INTXBAR9_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24:0	INTXBAR9_G2_SEL	R/W	0h	Corresponding INT XBar G2 Input Select 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.15.68 CFG0_INTXBAR9_G3 Registers

3.15.68.1 CFG0_G3 Register (Offset = 34Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1485. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 534Ch

Figure 3-678. INTXBAR9_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR9_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-1486. INTXBAR9_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	INTXBAR9_G3_SEL	R/W	0h	Corresponding INT XBar G3 Input Select 0: FSIRX0.INT1N 1: FSIRX0.INT2N 2: FSIRX1.INT1N 3: FSIRX1.INT2N 4: FSIRX2.INT1N 5: FSIRX2.INT2N 6: FSIRX3.INT1N 7: FSIRX3.INT2N 8: FSITX0.INT1N 9: FSITX0.INT2N 10: FSITX1.INT1N 11: FSITX1.INT2N 12: FSITX2.INT1N 13: FSITX2.INT2N 14: FSITX3.INT1N 15: FSITX3.INT2N Reset Source: mod_g_rst_n

3.15.69 CFG0_INTXBAR9_G4 Registers

3.15.69.1 CFG0_G4 Register (Offset = 350h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1487. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5350h

Figure 3-679. INTXBAR9_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR9_G4_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1488. INTXBAR9_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR9_G4_SEL	R/W	0h	Corresponding INT XBar G4 Input Select 0: SD0.ERR 1: SD0.FILT1.DRINT 2: SD0.FILT2.DRINT 3: SD0.FILT3.DRINT 4: SD0.FILT4.DRINT 5: SD1.ERR 6: SD1.FILT1.DRINT 7: SD1.FILT2.DRINT 8: SD1.FILT3.DRINT 9: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.15.70 CFG0_INTXBAR9_G5 Registers

3.15.70.1 CFG0_G5 Register (Offset = 354h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1489. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5354h

Figure 3-680. INTXBAR9_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR9_G5_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1490. INTXBAR9_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR9_G5_SEL	R/W	0h	Corresponding INT XBar G5 Input Select 0: ECAP0.INT 1: ECAP1.INT 2: ECAP2.INT 3: ECAP3.INT 4: ECAP4.INT 5: ECAP5.INT 6: ECAP6.INT 7: ECAP7.INT 8: ECAP8.INT 9: ECAP9.INT Reset Source: mod_g_rst_n

3.15.71 CFG0_INTXBAR9_G6 Registers

3.15.71.1 CFG0_G6 Register (Offset = 358h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1491. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5358h

Figure 3-681. INTXBAR9_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															INTXBAR9_G6_SEL
NONE															R/W
0															0h

Access Types Legend

Table 3-1492. INTXBAR9_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	INTXBAR9_G6_SEL	R/W	0h	Corresponding INT XBar G6 Input Select 0: EQEP0.INT 1: EQEP1.INT 2: EQEP2.INT Reset Source: mod_g_rst_n

3.15.72 CFG0_INTXBAR10_G0 Registers

3.15.72.1 CFG0_G0 Register (Offset = 380h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1493. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5380h

Figure 3-682. INTXBAR10_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR10_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR10_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1494. INTXBAR10_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR10_G0_SEL	R/W	0h	ETPWM INT interrupt to corresponding xbar 1: PWMx.INT is selected 0: PWMx.INT is de-selected Reset Source: mod_g_rst_n

3.15.73 CFG0_INTXBAR10_G1 Registers

3.15.73.1 CFG0_G1 Register (Offset = 384h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1495. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5384h

Figure 3-683. INTXBAR10_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR10_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR10_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1496. INTXBAR10_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR10_G1_SEL	R/W	0h	ETPWM TZINT interrupt to corresponding xbar 1: PWMx.TZINT is selected 0: PWMx.TZINT is de-selected Reset Source: mod_g_rst_n

3.15.74 CFG0_INTXBAR10_G2 Registers

3.15.74.1 CFG0_G2 Register (Offset = 388h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1497. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5388h

Figure 3-684. INTXBAR10_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							INTXBAR10_G2_SEL								
NONE							R/W								
0							0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR10_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1498. INTXBAR10_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24:0	INTXBAR10_G2_SEL	R/W	0h	Corresponding INT XBar G2 Input Select 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.15.75 CFG0_INTXBAR10_G3 Registers

3.15.75.1 CFG0_G3 Register (Offset = 38Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1499. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 538Ch

Figure 3-685. INTXBAR10_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR10_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-1500. INTXBAR10_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	INTXBAR10_G3_SEL	R/W	0h	Corresponding INT XBar G3 Input Select 0: FSIRX0.INT1N 1: FSIRX0.INT2N 2: FSIRX1.INT1N 3: FSIRX1.INT2N 4: FSIRX2.INT1N 5: FSIRX2.INT2N 6: FSIRX3.INT1N 7: FSIRX3.INT2N 8: FSITX0.INT1N 9: FSITX0.INT2N 10: FSITX1.INT1N 11: FSITX1.INT2N 12: FSITX2.INT1N 13: FSITX2.INT2N 14: FSITX3.INT1N 15: FSITX3.INT2N Reset Source: mod_g_rst_n

3.15.76 CFG0_INTXBAR10_G4 Registers

3.15.76.1 CFG0_G4 Register (Offset = 390h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1501. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5390h

Figure 3-686. INTXBAR10_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR10_G4_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1502. INTXBAR10_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR10_G4_SEL	R/W	0h	Corresponding INT XBar G4 Input Select 0: SD0.ERR 1: SD0.FILT1.DRINT 2: SD0.FILT2.DRINT 3: SD0.FILT3.DRINT 4: SD0.FILT4.DRINT 5: SD1.ERR 6: SD1.FILT1.DRINT 7: SD1.FILT2.DRINT 8: SD1.FILT3.DRINT 9: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.15.77 CFG0_INTXBAR10_G5 Registers

3.15.77.1 CFG0_G5 Register (Offset = 394h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1503. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5394h

Figure 3-687. INTXBAR10_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR10_G5_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1504. INTXBAR10_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR10_G5_SEL	R/W	0h	Corresponding INT XBar G5 Input Select 0: ECAP0.INT 1: ECAP1.INT 2: ECAP2.INT 3: ECAP3.INT 4: ECAP4.INT 5: ECAP5.INT 6: ECAP6.INT 7: ECAP7.INT 8: ECAP8.INT 9: ECAP9.INT Reset Source: mod_g_rst_n

3.15.78 CFG0_INTXBAR10_G6 Registers

3.15.78.1 CFG0_G6 Register (Offset = 398h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1505. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5398h

Figure 3-688. INTXBAR10_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													INTXBAR10_G6_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1506. INTXBAR10_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	INTXBAR10_G6_SEL	R/W	0h	Corresponding INT XBar G6 Input Select 0: EQEP0.INT 1: EQEP1.INT 2: EQEP2.INT Reset Source: mod_g_rst_n

3.15.79 CFG0_INTXBAR11_G0 Registers

3.15.79.1 CFG0_G0 Register (Offset = 3C0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1507. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 53C0h

Figure 3-689. INTXBAR11_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR11_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR11_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1508. INTXBAR11_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR11_G0_SEL	R/W	0h	ETPWM INT interrupt to corresponding xbar 1: PWMx.INT is selected 0: PWMx.INT is de-selected Reset Source: mod_g_rst_n

3.15.80 CFG0_INTXBAR11_G1 Registers

3.15.80.1 CFG0_G1 Register (Offset = 3C4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1509. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 53C4h

Figure 3-690. INTXBAR11_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR11_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR11_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1510. INTXBAR11_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR11_G1_SEL	R/W	0h	ETPWM TZINT interrupt to corresponding xbar 1: PWMx.TZINT is selected 0: PWMx.TZINT is de-selected Reset Source: mod_g_rst_n

3.15.81 CFG0_INTXBAR11_G2 Registers

3.15.81.1 CFG0_G2 Register (Offset = 3C8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1511. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 53C8h

Figure 3-691. INTXBAR11_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							INTXBAR11_G2_SEL								
NONE							R/W								
0							0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR11_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1512. INTXBAR11_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24:0	INTXBAR11_G2_SEL	R/W	0h	Corresponding INT XBar G2 Input Select 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.15.82 CFG0_INTXBAR11_G3 Registers

3.15.82.1 CFG0_G3 Register (Offset = 3CCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1513. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 53CCh

Figure 3-692. INTXBAR11_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR11_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-1514. INTXBAR11_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	INTXBAR11_G3_SEL	R/W	0h	Corresponding INT XBar G3 Input Select 0: FSIRX0.INT1N 1: FSIRX0.INT2N 2: FSIRX1.INT1N 3: FSIRX1.INT2N 4: FSIRX2.INT1N 5: FSIRX2.INT2N 6: FSIRX3.INT1N 7: FSIRX3.INT2N 8: FSITX0.INT1N 9: FSITX0.INT2N 10: FSITX1.INT1N 11: FSITX1.INT2N 12: FSITX2.INT1N 13: FSITX2.INT2N 14: FSITX3.INT1N 15: FSITX3.INT2N Reset Source: mod_g_rst_n

3.15.83 CFG0_INTXBAR11_G4 Registers

3.15.83.1 CFG0_G4 Register (Offset = 3D0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1515. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 53D0h

Figure 3-693. INTXBAR11_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR11_G4_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1516. INTXBAR11_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR11_G4_SEL	R/W	0h	Corresponding INT XBar G4 Input Select 0: SD0.ERR 1: SD0.FILT1.DRINT 2: SD0.FILT2.DRINT 3: SD0.FILT3.DRINT 4: SD0.FILT4.DRINT 5: SD1.ERR 6: SD1.FILT1.DRINT 7: SD1.FILT2.DRINT 8: SD1.FILT3.DRINT 9: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.15.84 CFG0_INTXBAR11_G5 Registers

3.15.84.1 CFG0_G5 Register (Offset = 3D4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1517. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 53D4h

Figure 3-694. INTXBAR11_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR11_G5_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1518. INTXBAR11_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR11_G5_SEL	R/W	0h	Corresponding INT XBar G5 Input Select 0: ECAP0.INT 1: ECAP1.INT 2: ECAP2.INT 3: ECAP3.INT 4: ECAP4.INT 5: ECAP5.INT 6: ECAP6.INT 7: ECAP7.INT 8: ECAP8.INT 9: ECAP9.INT Reset Source: mod_g_rst_n

3.15.85 CFG0_INTXBAR11_G6 Registers

3.15.85.1 CFG0_G6 Register (Offset = 3D8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1519. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 53D8h

Figure 3-695. INTXBAR11_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													INTXBAR11_G6_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1520. INTXBAR11_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	INTXBAR11_G6_SEL	R/W	0h	Corresponding INT XBar G6 Input Select 0: EQEP0.INT 1: EQEP1.INT 2: EQEP2.INT Reset Source: mod_g_rst_n

3.15.86 CFG0_INTXBAR12_G0 Registers

3.15.86.1 CFG0_G0 Register (Offset = 400h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1521. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5400h

Figure 3-696. INTXBAR12_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR12_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR12_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1522. INTXBAR12_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR12_G0_SEL	R/W	0h	ETPWM INT interrupt to corresponding xbar 1: PWMx.INT is selected 0: PWMx.INT is de-selected Reset Source: mod_g_rst_n

3.15.87 CFG0_INTXBAR12_G1 Registers

3.15.87.1 CFG0_G1 Register (Offset = 404h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1523. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5404h

Figure 3-697. INTXBAR12_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR12_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR12_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1524. INTXBAR12_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR12_G1_SEL	R/W	0h	ETPWM TZINT interrupt to corresponding xbar 1: PWMx.TZINT is selected 0: PWMx.TZINT is de-selected Reset Source: mod_g_rst_n

3.15.88 CFG0_INTXBAR12_G2 Registers

3.15.88.1 CFG0_G2 Register (Offset = 408h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1525. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5408h

Figure 3-698. INTXBAR12_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							INTXBAR12_G2_SEL								
NONE							R/W								
0							0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR12_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1526. INTXBAR12_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24:0	INTXBAR12_G2_SEL	R/W	0h	Corresponding INT XBar G2 Input Select 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.15.89 CFG0_INTXBAR12_G3 Registers

3.15.89.1 CFG0_G3 Register (Offset = 40Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1527. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 540Ch

Figure 3-699. INTXBAR12_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR12_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-1528. INTXBAR12_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	INTXBAR12_G3_SEL	R/W	0h	Corresponding INT XBar G3 Input Select 0: FSIRX0.INT1N 1: FSIRX0.INT2N 2: FSIRX1.INT1N 3: FSIRX1.INT2N 4: FSIRX2.INT1N 5: FSIRX2.INT2N 6: FSIRX3.INT1N 7: FSIRX3.INT2N 8: FSITX0.INT1N 9: FSITX0.INT2N 10: FSITX1.INT1N 11: FSITX1.INT2N 12: FSITX2.INT1N 13: FSITX2.INT2N 14: FSITX3.INT1N 15: FSITX3.INT2N Reset Source: mod_g_rst_n

3.15.90 CFG0_INTXBAR12_G4 Registers

3.15.90.1 CFG0_G4 Register (Offset = 410h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1529. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5410h

Figure 3-700. INTXBAR12_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR12_G4_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1530. INTXBAR12_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR12_G4_SEL	R/W	0h	Corresponding INT XBar G4 Input Select 0: SD0.ERR 1: SD0.FILT1.DRINT 2: SD0.FILT2.DRINT 3: SD0.FILT3.DRINT 4: SD0.FILT4.DRINT 5: SD1.ERR 6: SD1.FILT1.DRINT 7: SD1.FILT2.DRINT 8: SD1.FILT3.DRINT 9: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.15.91 CFG0_INTXBAR12_G5 Registers

3.15.91.1 CFG0_G5 Register (Offset = 414h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1531. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5414h

Figure 3-701. INTXBAR12_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR12_G5_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1532. INTXBAR12_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR12_G5_SEL	R/W	0h	Corresponding INT XBar G5 Input Select 0: ECAP0.INT 1: ECAP1.INT 2: ECAP2.INT 3: ECAP3.INT 4: ECAP4.INT 5: ECAP5.INT 6: ECAP6.INT 7: ECAP7.INT 8: ECAP8.INT 9: ECAP9.INT Reset Source: mod_g_rst_n

3.15.92 CFG0_INTXBAR12_G6 Registers

3.15.92.1 CFG0_G6 Register (Offset = 418h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1533. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5418h

Figure 3-702. INTXBAR12_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													INTXBAR12_G6_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1534. INTXBAR12_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	INTXBAR12_G6_SEL	R/W	0h	Corresponding INT XBar G6 Input Select 0: EQEP0.INT 1: EQEP1.INT 2: EQEP2.INT Reset Source: mod_g_rst_n

3.15.93 CFG0_INTXBAR13_G0 Registers

3.15.93.1 CFG0_G0 Register (Offset = 440h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1535. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5440h

Figure 3-703. INTXBAR13_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR13_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR13_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1536. INTXBAR13_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR13_G0_SEL	R/W	0h	ETPWM INT interrupt to corresponding xbar 1: PWMx.INT is selected 0: PWMx.INT is de-selected Reset Source: mod_g_rst_n

3.15.94 CFG0_INTXBAR13_G1 Registers

3.15.94.1 CFG0_G1 Register (Offset = 444h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1537. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5444h

Figure 3-704. INTXBAR13_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR13_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR13_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1538. INTXBAR13_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR13_G1_SEL	R/W	0h	ETPWM TZINT interrupt to corresponding xbar 1: PWMx.TZINT is selected 0: PWMx.TZINT is de-selected Reset Source: mod_g_rst_n

3.15.95 CFG0_INTXBAR13_G2 Registers

3.15.95.1 CFG0_G2 Register (Offset = 448h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1539. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5448h

Figure 3-705. INTXBAR13_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							INTXBAR13_G2_SEL								
NONE							R/W								
0							0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR13_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1540. INTXBAR13_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24:0	INTXBAR13_G2_SEL	R/W	0h	Corresponding INT XBar G2 Input Select 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.15.96 CFG0_INTXBAR13_G3 Registers

3.15.96.1 CFG0_G3 Register (Offset = 44Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1541. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 544Ch

Figure 3-706. INTXBAR13_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR13_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-1542. INTXBAR13_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	INTXBAR13_G3_SEL	R/W	0h	Corresponding INT XBar G3 Input Select 0: FSIRX0.INT1N 1: FSIRX0.INT2N 2: FSIRX1.INT1N 3: FSIRX1.INT2N 4: FSIRX2.INT1N 5: FSIRX2.INT2N 6: FSIRX3.INT1N 7: FSIRX3.INT2N 8: FSITX0.INT1N 9: FSITX0.INT2N 10: FSITX1.INT1N 11: FSITX1.INT2N 12: FSITX2.INT1N 13: FSITX2.INT2N 14: FSITX3.INT1N 15: FSITX3.INT2N Reset Source: mod_g_rst_n

3.15.97 CFG0_INTXBAR13_G4 Registers

3.15.97.1 CFG0_G4 Register (Offset = 450h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1543. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5450h

Figure 3-707. INTXBAR13_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR13_G4_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1544. INTXBAR13_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR13_G4_SEL	R/W	0h	Corresponding INT XBar G4 Input Select 0: SD0.ERR 1: SD0.FILT1.DRINT 2: SD0.FILT2.DRINT 3: SD0.FILT3.DRINT 4: SD0.FILT4.DRINT 5: SD1.ERR 6: SD1.FILT1.DRINT 7: SD1.FILT2.DRINT 8: SD1.FILT3.DRINT 9: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.15.98 CFG0_INTXBAR13_G5 Registers

3.15.98.1 CFG0_G5 Register (Offset = 454h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1545. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5454h

Figure 3-708. INTXBAR13_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR13_G5_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1546. INTXBAR13_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR13_G5_SEL	R/W	0h	Corresponding INT XBar G5 Input Select 0: ECAP0.INT 1: ECAP1.INT 2: ECAP2.INT 3: ECAP3.INT 4: ECAP4.INT 5: ECAP5.INT 6: ECAP6.INT 7: ECAP7.INT 8: ECAP8.INT 9: ECAP9.INT Reset Source: mod_g_rst_n

3.15.99 CFG0_INTXBAR13_G6 Registers

3.15.99.1 CFG0_G6 Register (Offset = 458h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1547. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5458h

Figure 3-709. INTXBAR13_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															INTXBAR13_G6_SEL
NONE															R/W
0															0h

Access Types Legend

Table 3-1548. INTXBAR13_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	INTXBAR13_G6_SEL	R/W	0h	Corresponding INT XBar G6 Input Select 0: EQEP0.INT 1: EQEP1.INT 2: EQEP2.INT Reset Source: mod_g_rst_n

3.15.100 CFG0_INTXBAR14_G0 Registers

3.15.100.1 CFG0_G0 Register (Offset = 480h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1549. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5480h

Figure 3-710. INTXBAR14_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR14_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR14_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1550. INTXBAR14_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR14_G0_SEL	R/W	0h	ETPWM INT interrupt to corresponding xbar 1: PWMx.INT is selected 0: PWMx.INT is de-selected Reset Source: mod_g_rst_n

3.15.101 CFG0_INTXBAR14_G1 Registers

3.15.101.1 CFG0_G1 Register (Offset = 484h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1551. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5484h

Figure 3-711. INTXBAR14_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR14_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR14_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1552. INTXBAR14_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR14_G1_SEL	R/W	0h	ETPWM TZINT interrupt to corresponding xbar 1: PWMx.TZINT is selected 0: PWMx.TZINT is de-selected Reset Source: mod_g_rst_n

3.15.102 CFG0_INTXBAR14_G2 Registers

3.15.102.1 CFG0_G2 Register (Offset = 488h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1553. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5488h

Figure 3-712. INTXBAR14_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							INTXBAR14_G2_SEL								
NONE							R/W								
0							0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR14_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1554. INTXBAR14_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24:0	INTXBAR14_G2_SEL	R/W	0h	Corresponding INT XBar G2 Input Select 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.15.103 CFG0_INTXBAR14_G3 Registers

3.15.103.1 CFG0_G3 Register (Offset = 48Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1555. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 548Ch

Figure 3-713. INTXBAR14_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR14_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-1556. INTXBAR14_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	INTXBAR14_G3_SEL	R/W	0h	Corresponding INT XBar G3 Input Select 0: FSIRX0.INT1N 1: FSIRX0.INT2N 2: FSIRX1.INT1N 3: FSIRX1.INT2N 4: FSIRX2.INT1N 5: FSIRX2.INT2N 6: FSIRX3.INT1N 7: FSIRX3.INT2N 8: FSITX0.INT1N 9: FSITX0.INT2N 10: FSITX1.INT1N 11: FSITX1.INT2N 12: FSITX2.INT1N 13: FSITX2.INT2N 14: FSITX3.INT1N 15: FSITX3.INT2N Reset Source: mod_g_rst_n

3.15.104 CFG0_INTXBAR14_G4 Registers

3.15.104.1 CFG0_G4 Register (Offset = 490h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1557. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5490h

Figure 3-714. INTXBAR14_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR14_G4_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1558. INTXBAR14_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR14_G4_SEL	R/W	0h	Corresponding INT XBar G4 Input Select 0: SD0.ERR 1: SD0.FILT1.DRINT 2: SD0.FILT2.DRINT 3: SD0.FILT3.DRINT 4: SD0.FILT4.DRINT 5: SD1.ERR 6: SD1.FILT1.DRINT 7: SD1.FILT2.DRINT 8: SD1.FILT3.DRINT 9: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.15.105 CFG0_INTXBAR14_G5 Registers

3.15.105.1 CFG0_G5 Register (Offset = 494h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1559. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5494h

Figure 3-715. INTXBAR14_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR14_G5_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1560. INTXBAR14_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR14_G5_SEL	R/W	0h	Corresponding INT XBar G5 Input Select 0: ECAP0.INT 1: ECAP1.INT 2: ECAP2.INT 3: ECAP3.INT 4: ECAP4.INT 5: ECAP5.INT 6: ECAP6.INT 7: ECAP7.INT 8: ECAP8.INT 9: ECAP9.INT Reset Source: mod_g_rst_n

3.15.106 CFG0_INTXBAR14_G6 Registers

3.15.106.1 CFG0_G6 Register (Offset = 498h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1561. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5498h

Figure 3-716. INTXBAR14_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													INTXBAR14_G6_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1562. INTXBAR14_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	INTXBAR14_G6_SEL	R/W	0h	Corresponding INT XBar G6 Input Select 0: EQEP0.INT 1: EQEP1.INT 2: EQEP2.INT Reset Source: mod_g_rst_n

3.15.107 CFG0_INTXBAR15_G0 Registers

3.15.107.1 CFG0_G0 Register (Offset = 4C0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1563. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 54C0h

Figure 3-717. INTXBAR15_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR15_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR15_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1564. INTXBAR15_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR15_G0_SEL	R/W	0h	ETPWM INT interrupt to corresponding xbar 1: PWMx.INT is selected 0: PWMx.INT is de-selected Reset Source: mod_g_rst_n

3.15.108 CFG0_INTXBAR15_G1 Registers

3.15.108.1 CFG0_G1 Register (Offset = 4C4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1565. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 54C4h

Figure 3-718. INTXBAR15_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR15_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR15_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1566. INTXBAR15_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR15_G1_SEL	R/W	0h	ETPWM TZINT interrupt to corresponding xbar 1: PWMx.TZINT is selected 0: PWMx.TZINT is de-selected Reset Source: mod_g_rst_n

3.15.109 CFG0_INTXBAR15_G2 Registers

3.15.109.1 CFG0_G2 Register (Offset = 4C8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1567. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 54C8h

Figure 3-719. INTXBAR15_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							INTXBAR15_G2_SEL								
NONE							R/W								
0							0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR15_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1568. INTXBAR15_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24:0	INTXBAR15_G2_SEL	R/W	0h	Corresponding INT XBar G2 Input Select 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.15.110 CFG0_INTXBAR15_G3 Registers

3.15.110.1 CFG0_G3 Register (Offset = 4CCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1569. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 54CCh

Figure 3-720. INTXBAR15_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR15_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-1570. INTXBAR15_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	INTXBAR15_G3_SEL	R/W	0h	Corresponding INT XBar G3 Input Select 0: FSIRX0.INT1N 1: FSIRX0.INT2N 2: FSIRX1.INT1N 3: FSIRX1.INT2N 4: FSIRX2.INT1N 5: FSIRX2.INT2N 6: FSIRX3.INT1N 7: FSIRX3.INT2N 8: FSITX0.INT1N 9: FSITX0.INT2N 10: FSITX1.INT1N 11: FSITX1.INT2N 12: FSITX2.INT1N 13: FSITX2.INT2N 14: FSITX3.INT1N 15: FSITX3.INT2N Reset Source: mod_g_rst_n

3.15.111 CFG0_INTXBAR15_G4 Registers

3.15.111.1 CFG0_G4 Register (Offset = 4D0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1571. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 54D0h

Figure 3-721. INTXBAR15_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR15_G4_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1572. INTXBAR15_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR15_G4_SEL	R/W	0h	Corresponding INT XBar G4 Input Select 0: SD0.ERR 1: SD0.FILT1.DRINT 2: SD0.FILT2.DRINT 3: SD0.FILT3.DRINT 4: SD0.FILT4.DRINT 5: SD1.ERR 6: SD1.FILT1.DRINT 7: SD1.FILT2.DRINT 8: SD1.FILT3.DRINT 9: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.15.112 CFG0_INTXBAR15_G5 Registers

3.15.112.1 CFG0_G5 Register (Offset = 4D4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1573. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 54D4h

Figure 3-722. INTXBAR15_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR15_G5_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1574. INTXBAR15_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR15_G5_SEL	R/W	0h	Corresponding INT XBar G5 Input Select 0: ECAP0.INT 1: ECAP1.INT 2: ECAP2.INT 3: ECAP3.INT 4: ECAP4.INT 5: ECAP5.INT 6: ECAP6.INT 7: ECAP7.INT 8: ECAP8.INT 9: ECAP9.INT Reset Source: mod_g_rst_n

3.15.113 CFG0_INTXBAR15_G6 Registers

3.15.113.1 CFG0_G6 Register (Offset = 4D8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1575. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 54D8h

Figure 3-723. INTXBAR15_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													INTXBAR15_G6_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1576. INTXBAR15_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	INTXBAR15_G6_SEL	R/W	0h	Corresponding INT XBar G6 Input Select 0: EQEP0.INT 1: EQEP1.INT 2: EQEP2.INT Reset Source: mod_g_rst_n

3.15.114 CFG0_INTXBAR16_G0 Registers

3.15.114.1 CFG0_G0 Register (Offset = 500h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1577. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5500h

Figure 3-724. INTXBAR16_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR16_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR16_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1578. INTXBAR16_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR16_G0_SEL	R/W	0h	ETPWM INT interrupt to corresponding xbar 1: PWMx.INT is selected 0: PWMx.INT is de-selected Reset Source: mod_g_rst_n

3.15.115 CFG0_INTXBAR16_G1 Registers

3.15.115.1 CFG0_G1 Register (Offset = 504h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1579. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5504h

Figure 3-725. INTXBAR16_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR16_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR16_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1580. INTXBAR16_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR16_G1_SEL	R/W	0h	ETPWM TZINT interrupt to corresponding xbar 1: PWMx.TZINT is selected 0: PWMx.TZINT is de-selected Reset Source: mod_g_rst_n

3.15.116 CFG0_INTXBAR16_G2 Registers

3.15.116.1 CFG0_G2 Register (Offset = 508h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1581. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5508h

Figure 3-726. INTXBAR16_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							INTXBAR16_G2_SEL								
NONE							R/W								
0							0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR16_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1582. INTXBAR16_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24:0	INTXBAR16_G2_SEL	R/W	0h	Corresponding INT XBar G2 Input Select 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.15.117 CFG0_INTXBAR16_G3 Registers

3.15.117.1 CFG0_G3 Register (Offset = 50Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1583. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 550Ch

Figure 3-727. INTXBAR16_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR16_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-1584. INTXBAR16_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	INTXBAR16_G3_SEL	R/W	0h	Corresponding INT XBar G3 Input Select 0: FSIRX0.INT1N 1: FSIRX0.INT2N 2: FSIRX1.INT1N 3: FSIRX1.INT2N 4: FSIRX2.INT1N 5: FSIRX2.INT2N 6: FSIRX3.INT1N 7: FSIRX3.INT2N 8: FSITX0.INT1N 9: FSITX0.INT2N 10: FSITX1.INT1N 11: FSITX1.INT2N 12: FSITX2.INT1N 13: FSITX2.INT2N 14: FSITX3.INT1N 15: FSITX3.INT2N Reset Source: mod_g_rst_n

3.15.118 CFG0_INTXBAR16_G4 Registers

3.15.118.1 CFG0_G4 Register (Offset = 510h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1585. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5510h

Figure 3-728. INTXBAR16_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR16_G4_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1586. INTXBAR16_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR16_G4_SEL	R/W	0h	Corresponding INT XBar G4 Input Select 0: SD0.ERR 1: SD0.FILT1.DRINT 2: SD0.FILT2.DRINT 3: SD0.FILT3.DRINT 4: SD0.FILT4.DRINT 5: SD1.ERR 6: SD1.FILT1.DRINT 7: SD1.FILT2.DRINT 8: SD1.FILT3.DRINT 9: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.15.119 CFG0_INTXBAR16_G5 Registers

3.15.119.1 CFG0_G5 Register (Offset = 514h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1587. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5514h

Figure 3-729. INTXBAR16_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR16_G5_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1588. INTXBAR16_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR16_G5_SEL	R/W	0h	Corresponding INT XBar G5 Input Select 0: ECAP0.INT 1: ECAP1.INT 2: ECAP2.INT 3: ECAP3.INT 4: ECAP4.INT 5: ECAP5.INT 6: ECAP6.INT 7: ECAP7.INT 8: ECAP8.INT 9: ECAP9.INT Reset Source: mod_g_rst_n

3.15.120 CFG0_INTXBAR16_G6 Registers

3.15.120.1 CFG0_G6 Register (Offset = 518h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1589. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5518h

Figure 3-730. INTXBAR16_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													INTXBAR16_G6_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1590. INTXBAR16_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	INTXBAR16_G6_SEL	R/W	0h	Corresponding INT XBar G6 Input Select 0: EQEP0.INT 1: EQEP1.INT 2: EQEP2.INT Reset Source: mod_g_rst_n

3.15.121 CFG0_INTXBAR17_G0 Registers

3.15.121.1 CFG0_G0 Register (Offset = 540h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1591. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5540h

Figure 3-731. INTXBAR17_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR17_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR17_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1592. INTXBAR17_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR17_G0_SEL	R/W	0h	ETPWM INT interrupt to corresponding xbar 1: PWMx.INT is selected 0: PWMx.INT is de-selected Reset Source: mod_g_rst_n

3.15.122 CFG0_INTXBAR17_G1 Registers

3.15.122.1 CFG0_G1 Register (Offset = 544h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1593. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5544h

Figure 3-732. INTXBAR17_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR17_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR17_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1594. INTXBAR17_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR17_G1_SEL	R/W	0h	ETPWM TZINT interrupt to corresponding xbar 1: PWMx.TZINT is selected 0: PWMx.TZINT is de-selected Reset Source: mod_g_rst_n

3.15.123 CFG0_INTXBAR17_G2 Registers

3.15.123.1 CFG0_G2 Register (Offset = 548h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1595. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5548h

Figure 3-733. INTXBAR17_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							INTXBAR17_G2_SEL								
NONE							R/W								
0							0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR17_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1596. INTXBAR17_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24:0	INTXBAR17_G2_SEL	R/W	0h	Corresponding INT XBar G2 Input Select 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.15.124 CFG0_INTXBAR17_G3 Registers

3.15.124.1 CFG0_G3 Register (Offset = 54Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1597. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 554Ch

Figure 3-734. INTXBAR17_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR17_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-1598. INTXBAR17_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	INTXBAR17_G3_SEL	R/W	0h	Corresponding INT XBar G3 Input Select 0: FSIRX0.INT1N 1: FSIRX0.INT2N 2: FSIRX1.INT1N 3: FSIRX1.INT2N 4: FSIRX2.INT1N 5: FSIRX2.INT2N 6: FSIRX3.INT1N 7: FSIRX3.INT2N 8: FSITX0.INT1N 9: FSITX0.INT2N 10: FSITX1.INT1N 11: FSITX1.INT2N 12: FSITX2.INT1N 13: FSITX2.INT2N 14: FSITX3.INT1N 15: FSITX3.INT2N Reset Source: mod_g_rst_n

3.15.125 CFG0_INTXBAR17_G4 Registers

3.15.125.1 CFG0_G4 Register (Offset = 550h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1599. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5550h

Figure 3-735. INTXBAR17_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR17_G4_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1600. INTXBAR17_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR17_G4_SEL	R/W	0h	Corresponding INT XBar G4 Input Select 0: SD0.ERR 1: SD0.FILT1.DRINT 2: SD0.FILT2.DRINT 3: SD0.FILT3.DRINT 4: SD0.FILT4.DRINT 5: SD1.ERR 6: SD1.FILT1.DRINT 7: SD1.FILT2.DRINT 8: SD1.FILT3.DRINT 9: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.15.126 CFG0_INTXBAR17_G5 Registers

3.15.126.1 CFG0_G5 Register (Offset = 554h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1601. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5554h

Figure 3-736. INTXBAR17_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR17_G5_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1602. INTXBAR17_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR17_G5_SEL	R/W	0h	Corresponding INT XBar G5 Input Select 0: ECAP0.INT 1: ECAP1.INT 2: ECAP2.INT 3: ECAP3.INT 4: ECAP4.INT 5: ECAP5.INT 6: ECAP6.INT 7: ECAP7.INT 8: ECAP8.INT 9: ECAP9.INT Reset Source: mod_g_rst_n

3.15.127 CFG0_INTXBAR17_G6 Registers

3.15.127.1 CFG0_G6 Register (Offset = 558h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1603. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5558h

Figure 3-737. INTXBAR17_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													INTXBAR17_G6_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1604. INTXBAR17_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	INTXBAR17_G6_SEL	R/W	0h	Corresponding INT XBar G6 Input Select 0: EQEP0.INT 1: EQEP1.INT 2: EQEP2.INT Reset Source: mod_g_rst_n

3.15.128 CFG0_INTXBAR18_G0 Registers

3.15.128.1 CFG0_G0 Register (Offset = 580h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1605. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5580h

Figure 3-738. INTXBAR18_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR18_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR18_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1606. INTXBAR18_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR18_G0_SEL	R/W	0h	ETPWM INT interrupt to corresponding xbar 1: PWMx.INT is selected 0: PWMx.INT is de-selected Reset Source: mod_g_rst_n

3.15.129 CFG0_INTXBAR18_G1 Registers

3.15.129.1 CFG0_G1 Register (Offset = 584h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1607. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5584h

Figure 3-739. INTXBAR18_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR18_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR18_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1608. INTXBAR18_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR18_G1_SEL	R/W	0h	ETPWM TZINT interrupt to corresponding xbar 1: PWMx.TZINT is selected 0: PWMx.TZINT is de-selected Reset Source: mod_g_rst_n

3.15.130 CFG0_INTXBAR18_G2 Registers

3.15.130.1 CFG0_G2 Register (Offset = 588h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1609. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5588h

Figure 3-740. INTXBAR18_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							INTXBAR18_G2_SEL								
NONE							R/W								
0							0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR18_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1610. INTXBAR18_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24:0	INTXBAR18_G2_SEL	R/W	0h	Corresponding INT XBar G2 Input Select 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.15.131 CFG0_INTXBAR18_G3 Registers

3.15.131.1 CFG0_G3 Register (Offset = 58Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1611. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 558Ch

Figure 3-741. INTXBAR18_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR18_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-1612. INTXBAR18_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	INTXBAR18_G3_SEL	R/W	0h	Corresponding INT XBar G3 Input Select 0: FSIRX0.INT1N 1: FSIRX0.INT2N 2: FSIRX1.INT1N 3: FSIRX1.INT2N 4: FSIRX2.INT1N 5: FSIRX2.INT2N 6: FSIRX3.INT1N 7: FSIRX3.INT2N 8: FSITX0.INT1N 9: FSITX0.INT2N 10: FSITX1.INT1N 11: FSITX1.INT2N 12: FSITX2.INT1N 13: FSITX2.INT2N 14: FSITX3.INT1N 15: FSITX3.INT2N Reset Source: mod_g_rst_n

3.15.132 CFG0_INTXBAR18_G4 Registers

3.15.132.1 CFG0_G4 Register (Offset = 590h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1613. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5590h

Figure 3-742. INTXBAR18_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR18_G4_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1614. INTXBAR18_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR18_G4_SEL	R/W	0h	Corresponding INT XBar G4 Input Select 0: SD0.ERR 1: SD0.FILT1.DRINT 2: SD0.FILT2.DRINT 3: SD0.FILT3.DRINT 4: SD0.FILT4.DRINT 5: SD1.ERR 6: SD1.FILT1.DRINT 7: SD1.FILT2.DRINT 8: SD1.FILT3.DRINT 9: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.15.133 CFG0_INTXBAR18_G5 Registers

3.15.133.1 CFG0_G5 Register (Offset = 594h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1615. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5594h

Figure 3-743. INTXBAR18_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR18_G5_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1616. INTXBAR18_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR18_G5_SEL	R/W	0h	Corresponding INT XBar G5 Input Select 0: ECAP0.INT 1: ECAP1.INT 2: ECAP2.INT 3: ECAP3.INT 4: ECAP4.INT 5: ECAP5.INT 6: ECAP6.INT 7: ECAP7.INT 8: ECAP8.INT 9: ECAP9.INT Reset Source: mod_g_rst_n

3.15.134 CFG0_INTXBAR18_G6 Registers

3.15.134.1 CFG0_G6 Register (Offset = 598h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1617. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5598h

Figure 3-744. INTXBAR18_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													INTXBAR18_G6_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1618. INTXBAR18_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	INTXBAR18_G6_SEL	R/W	0h	Corresponding INT XBar G6 Input Select 0: EQEP0.INT 1: EQEP1.INT 2: EQEP2.INT Reset Source: mod_g_rst_n

3.15.135 CFG0_INTXBAR19_G0 Registers

3.15.135.1 CFG0_G0 Register (Offset = 5C0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1619. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 55C0h

Figure 3-745. INTXBAR19_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR19_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR19_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1620. INTXBAR19_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR19_G0_SEL	R/W	0h	ETPWM INT interrupt to corresponding xbar 1: PWMx.INT is selected 0: PWMx.INT is de-selected Reset Source: mod_g_rst_n

3.15.136 CFG0_INTXBAR19_G1 Registers

3.15.136.1 CFG0_G1 Register (Offset = 5C4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1621. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 55C4h

Figure 3-746. INTXBAR19_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR19_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR19_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1622. INTXBAR19_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR19_G1_SEL	R/W	0h	ETPWM TZINT interrupt to corresponding xbar 1: PWMx.TZINT is selected 0: PWMx.TZINT is de-selected Reset Source: mod_g_rst_n

3.15.137 CFG0_INTXBAR19_G2 Registers

3.15.137.1 CFG0_G2 Register (Offset = 5C8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1623. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 55C8h

Figure 3-747. INTXBAR19_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							INTXBAR19_G2_SEL								
NONE							R/W								
0							0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR19_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1624. INTXBAR19_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24:0	INTXBAR19_G2_SEL	R/W	0h	Corresponding INT XBar G2 Input Select 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.15.138 CFG0_INTXBAR19_G3 Registers

3.15.138.1 CFG0_G3 Register (Offset = 5CCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1625. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 55CCh

Figure 3-748. INTXBAR19_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR19_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-1626. INTXBAR19_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	INTXBAR19_G3_SEL	R/W	0h	Corresponding INT XBar G3 Input Select 0: FSIRX0.INT1N 1: FSIRX0.INT2N 2: FSIRX1.INT1N 3: FSIRX1.INT2N 4: FSIRX2.INT1N 5: FSIRX2.INT2N 6: FSIRX3.INT1N 7: FSIRX3.INT2N 8: FSITX0.INT1N 9: FSITX0.INT2N 10: FSITX1.INT1N 11: FSITX1.INT2N 12: FSITX2.INT1N 13: FSITX2.INT2N 14: FSITX3.INT1N 15: FSITX3.INT2N Reset Source: mod_g_rst_n

3.15.139 CFG0_INTXBAR19_G4 Registers

3.15.139.1 CFG0_G4 Register (Offset = 5D0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1627. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 55D0h

Figure 3-749. INTXBAR19_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR19_G4_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1628. INTXBAR19_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR19_G4_SEL	R/W	0h	Corresponding INT XBar G4 Input Select 0: SD0.ERR 1: SD0.FILT1.DRINT 2: SD0.FILT2.DRINT 3: SD0.FILT3.DRINT 4: SD0.FILT4.DRINT 5: SD1.ERR 6: SD1.FILT1.DRINT 7: SD1.FILT2.DRINT 8: SD1.FILT3.DRINT 9: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.15.140 CFG0_INTXBAR19_G5 Registers

3.15.140.1 CFG0_G5 Register (Offset = 5D4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1629. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 55D4h

Figure 3-750. INTXBAR19_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR19_G5_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1630. INTXBAR19_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR19_G5_SEL	R/W	0h	Corresponding INT XBar G5 Input Select 0: ECAP0.INT 1: ECAP1.INT 2: ECAP2.INT 3: ECAP3.INT 4: ECAP4.INT 5: ECAP5.INT 6: ECAP6.INT 7: ECAP7.INT 8: ECAP8.INT 9: ECAP9.INT Reset Source: mod_g_rst_n

3.15.141 CFG0_INTXBAR19_G6 Registers

3.15.141.1 CFG0_G6 Register (Offset = 5D8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1631. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 55D8h

Figure 3-751. INTXBAR19_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													INTXBAR19_G6_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1632. INTXBAR19_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	INTXBAR19_G6_SEL	R/W	0h	Corresponding INT XBar G6 Input Select 0: EQEP0.INT 1: EQEP1.INT 2: EQEP2.INT Reset Source: mod_g_rst_n

3.15.142 CFG0_INTXBAR20_G0 Registers

3.15.142.1 CFG0_G0 Register (Offset = 600h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1633. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5600h

Figure 3-752. INTXBAR20_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR20_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR20_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1634. INTXBAR20_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR20_G0_SEL	R/W	0h	ETPWM INT interrupt to corresponding xbar 1: PWMx.INT is selected 0: PWMx.INT is de-selected Reset Source: mod_g_rst_n

3.15.143 CFG0_INTXBAR20_G1 Registers

3.15.143.1 CFG0_G1 Register (Offset = 604h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1635. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5604h

Figure 3-753. INTXBAR20_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR20_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR20_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1636. INTXBAR20_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR20_G1_SEL	R/W	0h	ETPWM TZINT interrupt to corresponding xbar 1: PWMx.TZINT is selected 0: PWMx.TZINT is de-selected Reset Source: mod_g_rst_n

3.15.144 CFG0_INTXBAR20_G2 Registers

3.15.144.1 CFG0_G2 Register (Offset = 608h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1637. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5608h

Figure 3-754. INTXBAR20_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							INTXBAR20_G2_SEL								
NONE							R/W								
0							0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR20_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1638. INTXBAR20_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24:0	INTXBAR20_G2_SEL	R/W	0h	Corresponding INT XBar G2 Input Select 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.15.145 CFG0_INTXBAR20_G3 Registers

3.15.145.1 CFG0_G3 Register (Offset = 60Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1639. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 560Ch

Figure 3-755. INTXBAR20_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR20_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-1640. INTXBAR20_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	INTXBAR20_G3_SEL	R/W	0h	Corresponding INT XBar G3 Input Select 0: FSIRX0.INT1N 1: FSIRX0.INT2N 2: FSIRX1.INT1N 3: FSIRX1.INT2N 4: FSIRX2.INT1N 5: FSIRX2.INT2N 6: FSIRX3.INT1N 7: FSIRX3.INT2N 8: FSITX0.INT1N 9: FSITX0.INT2N 10: FSITX1.INT1N 11: FSITX1.INT2N 12: FSITX2.INT1N 13: FSITX2.INT2N 14: FSITX3.INT1N 15: FSITX3.INT2N Reset Source: mod_g_rst_n

3.15.146 CFG0_INTXBAR20_G4 Registers

3.15.146.1 CFG0_G4 Register (Offset = 610h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1641. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5610h

Figure 3-756. INTXBAR20_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR20_G4_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1642. INTXBAR20_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR20_G4_SEL	R/W	0h	Corresponding INT XBar G4 Input Select 0: SD0.ERR 1: SD0.FILT1.DRINT 2: SD0.FILT2.DRINT 3: SD0.FILT3.DRINT 4: SD0.FILT4.DRINT 5: SD1.ERR 6: SD1.FILT1.DRINT 7: SD1.FILT2.DRINT 8: SD1.FILT3.DRINT 9: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.15.147 CFG0_INTXBAR20_G5 Registers

3.15.147.1 CFG0_G5 Register (Offset = 614h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1643. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5614h

Figure 3-757. INTXBAR20_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR20_G5_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1644. INTXBAR20_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR20_G5_SEL	R/W	0h	Corresponding INT XBar G5 Input Select 0: ECAP0.INT 1: ECAP1.INT 2: ECAP2.INT 3: ECAP3.INT 4: ECAP4.INT 5: ECAP5.INT 6: ECAP6.INT 7: ECAP7.INT 8: ECAP8.INT 9: ECAP9.INT Reset Source: mod_g_rst_n

3.15.148 CFG0_INTXBAR20_G6 Registers

3.15.148.1 CFG0_G6 Register (Offset = 618h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1645. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5618h

Figure 3-758. INTXBAR20_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													INTXBAR20_G6_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1646. INTXBAR20_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	INTXBAR20_G6_SEL	R/W	0h	Corresponding INT XBar G6 Input Select 0: EQEP0.INT 1: EQEP1.INT 2: EQEP2.INT Reset Source: mod_g_rst_n

3.15.149 CFG0_INTXBAR21_G0 Registers

3.15.149.1 CFG0_G0 Register (Offset = 640h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1647. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5640h

Figure 3-759. INTXBAR21_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR21_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR21_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1648. INTXBAR21_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR21_G0_SEL	R/W	0h	ETPWM INT interrupt to corresponding xbar 1: PWMx.INT is selected 0: PWMx.INT is de-selected Reset Source: mod_g_rst_n

3.15.150 CFG0_INTXBAR21_G1 Registers

3.15.150.1 CFG0_G1 Register (Offset = 644h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1649. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5644h

Figure 3-760. INTXBAR21_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR21_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR21_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1650. INTXBAR21_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR21_G1_SEL	R/W	0h	ETPWM TZINT interrupt to corresponding xbar 1: PWMx.TZINT is selected 0: PWMx.TZINT is de-selected Reset Source: mod_g_rst_n

3.15.151 CFG0_INTXBAR21_G2 Registers

3.15.151.1 CFG0_G2 Register (Offset = 648h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1651. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5648h

Figure 3-761. INTXBAR21_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							INTXBAR21_G2_SEL								
NONE							R/W								
0							0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR21_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1652. INTXBAR21_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24:0	INTXBAR21_G2_SEL	R/W	0h	Corresponding INT XBar G2 Input Select 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.15.152 CFG0_INTXBAR21_G3 Registers

3.15.152.1 CFG0_G3 Register (Offset = 64Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1653. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 564Ch

Figure 3-762. INTXBAR21_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR21_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-1654. INTXBAR21_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	INTXBAR21_G3_SEL	R/W	0h	Corresponding INT XBar G3 Input Select 0: FSIRX0.INT1N 1: FSIRX0.INT2N 2: FSIRX1.INT1N 3: FSIRX1.INT2N 4: FSIRX2.INT1N 5: FSIRX2.INT2N 6: FSIRX3.INT1N 7: FSIRX3.INT2N 8: FSITX0.INT1N 9: FSITX0.INT2N 10: FSITX1.INT1N 11: FSITX1.INT2N 12: FSITX2.INT1N 13: FSITX2.INT2N 14: FSITX3.INT1N 15: FSITX3.INT2N Reset Source: mod_g_rst_n

3.15.153 CFG0_INTXBAR21_G4 Registers

3.15.153.1 CFG0_G4 Register (Offset = 650h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1655. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5650h

Figure 3-763. INTXBAR21_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR21_G4_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1656. INTXBAR21_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR21_G4_SEL	R/W	0h	Corresponding INT XBar G4 Input Select 0: SD0.ERR 1: SD0.FILT1.DRINT 2: SD0.FILT2.DRINT 3: SD0.FILT3.DRINT 4: SD0.FILT4.DRINT 5: SD1.ERR 6: SD1.FILT1.DRINT 7: SD1.FILT2.DRINT 8: SD1.FILT3.DRINT 9: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.15.154 CFG0_INTXBAR21_G5 Registers

3.15.154.1 CFG0_G5 Register (Offset = 654h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1657. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5654h

Figure 3-764. INTXBAR21_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR21_G5_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1658. INTXBAR21_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR21_G5_SEL	R/W	0h	Corresponding INT XBar G5 Input Select 0: ECAP0.INT 1: ECAP1.INT 2: ECAP2.INT 3: ECAP3.INT 4: ECAP4.INT 5: ECAP5.INT 6: ECAP6.INT 7: ECAP7.INT 8: ECAP8.INT 9: ECAP9.INT Reset Source: mod_g_rst_n

3.15.155 CFG0_INTXBAR21_G6 Registers

3.15.155.1 CFG0_G6 Register (Offset = 658h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1659. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5658h

Figure 3-765. INTXBAR21_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													INTXBAR21_G6_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1660. INTXBAR21_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	INTXBAR21_G6_SEL	R/W	0h	Corresponding INT XBar G6 Input Select 0: EQEP0.INT 1: EQEP1.INT 2: EQEP2.INT Reset Source: mod_g_rst_n

3.15.156 CFG0_INTXBAR22_G0 Registers

3.15.156.1 CFG0_G0 Register (Offset = 680h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1661. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5680h

Figure 3-766. INTXBAR22_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR22_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR22_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1662. INTXBAR22_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR22_G0_SEL	R/W	0h	ETPWM INT interrupt to corresponding xbar 1: PWMx.INT is selected 0: PWMx.INT is de-selected Reset Source: mod_g_rst_n

3.15.157 CFG0_INTXBAR22_G1 Registers

3.15.157.1 CFG0_G1 Register (Offset = 684h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1663. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5684h

Figure 3-767. INTXBAR22_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR22_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR22_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1664. INTXBAR22_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR22_G1_SEL	R/W	0h	ETPWM TZINT interrupt to corresponding xbar 1: PWMx.TZINT is selected 0: PWMx.TZINT is de-selected Reset Source: mod_g_rst_n

3.15.158 CFG0_INTXBAR22_G2 Registers

3.15.158.1 CFG0_G2 Register (Offset = 688h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1665. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5688h

Figure 3-768. INTXBAR22_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							INTXBAR22_G2_SEL								
NONE							R/W								
0							0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR22_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1666. INTXBAR22_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24:0	INTXBAR22_G2_SEL	R/W	0h	Corresponding INT XBar G2 Input Select 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.15.159 CFG0_INTXBAR22_G3 Registers

3.15.159.1 CFG0_G3 Register (Offset = 68Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1667. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 568Ch

Figure 3-769. INTXBAR22_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR22_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-1668. INTXBAR22_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	INTXBAR22_G3_SEL	R/W	0h	Corresponding INT XBar G3 Input Select 0: FSIRX0.INT1N 1: FSIRX0.INT2N 2: FSIRX1.INT1N 3: FSIRX1.INT2N 4: FSIRX2.INT1N 5: FSIRX2.INT2N 6: FSIRX3.INT1N 7: FSIRX3.INT2N 8: FSITX0.INT1N 9: FSITX0.INT2N 10: FSITX1.INT1N 11: FSITX1.INT2N 12: FSITX2.INT1N 13: FSITX2.INT2N 14: FSITX3.INT1N 15: FSITX3.INT2N Reset Source: mod_g_rst_n

3.15.160 CFG0_INTXBAR22_G4 Registers

3.15.160.1 CFG0_G4 Register (Offset = 690h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1669. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5690h

Figure 3-770. INTXBAR22_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR22_G4_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1670. INTXBAR22_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR22_G4_SEL	R/W	0h	Corresponding INT XBar G4 Input Select 0: SD0.ERR 1: SD0.FILT1.DRINT 2: SD0.FILT2.DRINT 3: SD0.FILT3.DRINT 4: SD0.FILT4.DRINT 5: SD1.ERR 6: SD1.FILT1.DRINT 7: SD1.FILT2.DRINT 8: SD1.FILT3.DRINT 9: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.15.161 CFG0_INTXBAR22_G5 Registers

3.15.161.1 CFG0_G5 Register (Offset = 694h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1671. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5694h

Figure 3-771. INTXBAR22_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR22_G5_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1672. INTXBAR22_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR22_G5_SEL	R/W	0h	Corresponding INT XBar G5 Input Select 0: ECAP0.INT 1: ECAP1.INT 2: ECAP2.INT 3: ECAP3.INT 4: ECAP4.INT 5: ECAP5.INT 6: ECAP6.INT 7: ECAP7.INT 8: ECAP8.INT 9: ECAP9.INT Reset Source: mod_g_rst_n

3.15.162 CFG0_INTXBAR22_G6 Registers

3.15.162.1 CFG0_G6 Register (Offset = 698h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1673. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5698h

Figure 3-772. INTXBAR22_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													INTXBAR22_G6_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1674. INTXBAR22_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	INTXBAR22_G6_SEL	R/W	0h	Corresponding INT XBar G6 Input Select 0: EQEP0.INT 1: EQEP1.INT 2: EQEP2.INT Reset Source: mod_g_rst_n

3.15.163 CFG0_INTXBAR23_G0 Registers

3.15.163.1 CFG0_G0 Register (Offset = 6C0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1675. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 56C0h

Figure 3-773. INTXBAR23_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR23_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR23_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1676. INTXBAR23_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR23_G0_SEL	R/W	0h	ETPWM INT interrupt to corresponding xbar 1: PWMx.INT is selected 0: PWMx.INT is de-selected Reset Source: mod_g_rst_n

3.15.164 CFG0_INTXBAR23_G1 Registers

3.15.164.1 CFG0_G1 Register (Offset = 6C4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1677. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 56C4h

Figure 3-774. INTXBAR23_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR23_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR23_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1678. INTXBAR23_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR23_G1_SEL	R/W	0h	ETPWM TZINT interrupt to corresponding xbar 1: PWMx.TZINT is selected 0: PWMx.TZINT is de-selected Reset Source: mod_g_rst_n

3.15.165 CFG0_INTXBAR23_G2 Registers

3.15.165.1 CFG0_G2 Register (Offset = 6C8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1679. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 56C8h

Figure 3-775. INTXBAR23_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							INTXBAR23_G2_SEL								
NONE							R/W								
0							0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR23_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1680. INTXBAR23_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24:0	INTXBAR23_G2_SEL	R/W	0h	Corresponding INT XBar G2 Input Select 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.15.166 CFG0_INTXBAR23_G3 Registers

3.15.166.1 CFG0_G3 Register (Offset = 6CCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1681. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 56CCh

Figure 3-776. INTXBAR23_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR23_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-1682. INTXBAR23_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	INTXBAR23_G3_SEL	R/W	0h	Corresponding INT XBar G3 Input Select 0: FSIRX0.INT1N 1: FSIRX0.INT2N 2: FSIRX1.INT1N 3: FSIRX1.INT2N 4: FSIRX2.INT1N 5: FSIRX2.INT2N 6: FSIRX3.INT1N 7: FSIRX3.INT2N 8: FSITX0.INT1N 9: FSITX0.INT2N 10: FSITX1.INT1N 11: FSITX1.INT2N 12: FSITX2.INT1N 13: FSITX2.INT2N 14: FSITX3.INT1N 15: FSITX3.INT2N Reset Source: mod_g_rst_n

3.15.167 CFG0_INTXBAR23_G4 Registers

3.15.167.1 CFG0_G4 Register (Offset = 6D0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1683. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 56D0h

Figure 3-777. INTXBAR23_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR23_G4_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1684. INTXBAR23_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR23_G4_SEL	R/W	0h	Corresponding INT XBar G4 Input Select 0: SD0.ERR 1: SD0.FILT1.DRINT 2: SD0.FILT2.DRINT 3: SD0.FILT3.DRINT 4: SD0.FILT4.DRINT 5: SD1.ERR 6: SD1.FILT1.DRINT 7: SD1.FILT2.DRINT 8: SD1.FILT3.DRINT 9: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.15.168 CFG0_INTXBAR23_G5 Registers

3.15.168.1 CFG0_G5 Register (Offset = 6D4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1685. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 56D4h

Figure 3-778. INTXBAR23_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR23_G5_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1686. INTXBAR23_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR23_G5_SEL	R/W	0h	Corresponding INT XBar G5 Input Select 0: ECAP0.INT 1: ECAP1.INT 2: ECAP2.INT 3: ECAP3.INT 4: ECAP4.INT 5: ECAP5.INT 6: ECAP6.INT 7: ECAP7.INT 8: ECAP8.INT 9: ECAP9.INT Reset Source: mod_g_rst_n

3.15.169 CFG0_INTXBAR23_G6 Registers

3.15.169.1 CFG0_G6 Register (Offset = 6D8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1687. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 56D8h

Figure 3-779. INTXBAR23_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													INTXBAR23_G6_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1688. INTXBAR23_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	INTXBAR23_G6_SEL	R/W	0h	Corresponding INT XBar G6 Input Select 0: EQEP0.INT 1: EQEP1.INT 2: EQEP2.INT Reset Source: mod_g_rst_n

3.15.170 CFG0_INTXBAR24_G0 Registers

3.15.170.1 CFG0_G0 Register (Offset = 700h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1689. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5700h

Figure 3-780. INTXBAR24_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR24_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR24_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1690. INTXBAR24_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR24_G0_SEL	R/W	0h	ETPWM INT interrupt to corresponding xbar 1: PWMx.INT is selected 0: PWMx.INT is de-selected Reset Source: mod_g_rst_n

3.15.171 CFG0_INTXBAR24_G1 Registers

3.15.171.1 CFG0_G1 Register (Offset = 704h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1691. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5704h

Figure 3-781. INTXBAR24_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR24_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR24_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1692. INTXBAR24_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR24_G1_SEL	R/W	0h	ETPWM TZINT interrupt to corresponding xbar 1: PWMx.TZINT is selected 0: PWMx.TZINT is de-selected Reset Source: mod_g_rst_n

3.15.172 CFG0_INTXBAR24_G2 Registers

3.15.172.1 CFG0_G2 Register (Offset = 708h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1693. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5708h

Figure 3-782. INTXBAR24_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							INTXBAR24_G2_SEL								
NONE							R/W								
0							0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR24_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1694. INTXBAR24_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24:0	INTXBAR24_G2_SEL	R/W	0h	Corresponding INT XBar G2 Input Select 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.15.173 CFG0_INTXBAR24_G3 Registers

3.15.173.1 CFG0_G3 Register (Offset = 70Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1695. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 570Ch

Figure 3-783. INTXBAR24_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR24_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-1696. INTXBAR24_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	INTXBAR24_G3_SEL	R/W	0h	Corresponding INT XBar G3 Input Select 0: FSIRX0.INT1N 1: FSIRX0.INT2N 2: FSIRX1.INT1N 3: FSIRX1.INT2N 4: FSIRX2.INT1N 5: FSIRX2.INT2N 6: FSIRX3.INT1N 7: FSIRX3.INT2N 8: FSITX0.INT1N 9: FSITX0.INT2N 10: FSITX1.INT1N 11: FSITX1.INT2N 12: FSITX2.INT1N 13: FSITX2.INT2N 14: FSITX3.INT1N 15: FSITX3.INT2N Reset Source: mod_g_rst_n

3.15.174 CFG0_INTXBAR24_G4 Registers

3.15.174.1 CFG0_G4 Register (Offset = 710h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1697. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5710h

Figure 3-784. INTXBAR24_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR24_G4_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1698. INTXBAR24_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR24_G4_SEL	R/W	0h	Corresponding INT XBar G4 Input Select 0: SD0.ERR 1: SD0.FILT1.DRINT 2: SD0.FILT2.DRINT 3: SD0.FILT3.DRINT 4: SD0.FILT4.DRINT 5: SD1.ERR 6: SD1.FILT1.DRINT 7: SD1.FILT2.DRINT 8: SD1.FILT3.DRINT 9: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.15.175 CFG0_INTXBAR24_G5 Registers

3.15.175.1 CFG0_G5 Register (Offset = 714h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1699. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5714h

Figure 3-785. INTXBAR24_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR24_G5_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1700. INTXBAR24_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR24_G5_SEL	R/W	0h	Corresponding INT XBar G5 Input Select 0: ECAP0.INT 1: ECAP1.INT 2: ECAP2.INT 3: ECAP3.INT 4: ECAP4.INT 5: ECAP5.INT 6: ECAP6.INT 7: ECAP7.INT 8: ECAP8.INT 9: ECAP9.INT Reset Source: mod_g_rst_n

3.15.176 CFG0_INTXBAR24_G6 Registers

3.15.176.1 CFG0_G6 Register (Offset = 718h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1701. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5718h

Figure 3-786. INTXBAR24_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													INTXBAR24_G6_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1702. INTXBAR24_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	INTXBAR24_G6_SEL	R/W	0h	Corresponding INT XBar G6 Input Select 0: EQEP0.INT 1: EQEP1.INT 2: EQEP2.INT Reset Source: mod_g_rst_n

3.15.177 CFG0_INTXBAR25_G0 Registers

3.15.177.1 CFG0_G0 Register (Offset = 740h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1703. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5740h

Figure 3-787. INTXBAR25_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR25_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR25_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1704. INTXBAR25_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR25_G0_SEL	R/W	0h	ETPWM INT interrupt to corresponding xbar 1: PWMx.INT is selected 0: PWMx.INT is de-selected Reset Source: mod_g_rst_n

3.15.178 CFG0_INTXBAR25_G1 Registers

3.15.178.1 CFG0_G1 Register (Offset = 744h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1705. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5744h

Figure 3-788. INTXBAR25_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR25_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR25_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1706. INTXBAR25_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR25_G1_SEL	R/W	0h	ETPWM TZINT interrupt to corresponding xbar 1: PWMx.TZINT is selected 0: PWMx.TZINT is de-selected Reset Source: mod_g_rst_n

3.15.179 CFG0_INTXBAR25_G2 Registers

3.15.179.1 CFG0_G2 Register (Offset = 748h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1707. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5748h

Figure 3-789. INTXBAR25_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							INTXBAR25_G2_SEL								
NONE							R/W								
0							0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR25_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1708. INTXBAR25_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24:0	INTXBAR25_G2_SEL	R/W	0h	Corresponding INT XBar G2 Input Select 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.15.180 CFG0_INTXBAR25_G3 Registers

3.15.180.1 CFG0_G3 Register (Offset = 74Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1709. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 574Ch

Figure 3-790. INTXBAR25_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR25_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-1710. INTXBAR25_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	INTXBAR25_G3_SEL	R/W	0h	Corresponding INT XBar G3 Input Select 0: FSIRX0.INT1N 1: FSIRX0.INT2N 2: FSIRX1.INT1N 3: FSIRX1.INT2N 4: FSIRX2.INT1N 5: FSIRX2.INT2N 6: FSIRX3.INT1N 7: FSIRX3.INT2N 8: FSITX0.INT1N 9: FSITX0.INT2N 10: FSITX1.INT1N 11: FSITX1.INT2N 12: FSITX2.INT1N 13: FSITX2.INT2N 14: FSITX3.INT1N 15: FSITX3.INT2N Reset Source: mod_g_rst_n

3.15.181 CFG0_INTXBAR25_G4 Registers

3.15.181.1 CFG0_G4 Register (Offset = 750h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1711. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5750h

Figure 3-791. INTXBAR25_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR25_G4_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1712. INTXBAR25_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR25_G4_SEL	R/W	0h	Corresponding INT XBar G4 Input Select 0: SD0.ERR 1: SD0.FILT1.DRINT 2: SD0.FILT2.DRINT 3: SD0.FILT3.DRINT 4: SD0.FILT4.DRINT 5: SD1.ERR 6: SD1.FILT1.DRINT 7: SD1.FILT2.DRINT 8: SD1.FILT3.DRINT 9: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.15.182 CFG0_INTXBAR25_G5 Registers

3.15.182.1 CFG0_G5 Register (Offset = 754h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1713. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5754h

Figure 3-792. INTXBAR25_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR25_G5_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1714. INTXBAR25_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR25_G5_SEL	R/W	0h	Corresponding INT XBar G5 Input Select 0: ECAP0.INT 1: ECAP1.INT 2: ECAP2.INT 3: ECAP3.INT 4: ECAP4.INT 5: ECAP5.INT 6: ECAP6.INT 7: ECAP7.INT 8: ECAP8.INT 9: ECAP9.INT Reset Source: mod_g_rst_n

3.15.183 CFG0_INTXBAR25_G6 Registers

3.15.183.1 CFG0_G6 Register (Offset = 758h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1715. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5758h

Figure 3-793. INTXBAR25_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													INTXBAR25_G6_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1716. INTXBAR25_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	INTXBAR25_G6_SEL	R/W	0h	Corresponding INT XBar G6 Input Select 0: EQEP0.INT 1: EQEP1.INT 2: EQEP2.INT Reset Source: mod_g_rst_n

3.15.184 CFG0_INTXBAR26_G0 Registers

3.15.184.1 CFG0_G0 Register (Offset = 780h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1717. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5780h

Figure 3-794. INTXBAR26_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR26_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR26_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1718. INTXBAR26_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR26_G0_SEL	R/W	0h	ETPWM INT interrupt to corresponding xbar 1: PWMx.INT is selected 0: PWMx.INT is de-selected Reset Source: mod_g_rst_n

3.15.185 CFG0_INTXBAR26_G1 Registers

3.15.185.1 CFG0_G1 Register (Offset = 784h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1719. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5784h

Figure 3-795. INTXBAR26_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR26_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR26_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1720. INTXBAR26_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR26_G1_SEL	R/W	0h	ETPWM TZINT interrupt to corresponding xbar 1: PWMx.TZINT is selected 0: PWMx.TZINT is de-selected Reset Source: mod_g_rst_n

3.15.186 CFG0_INTXBAR26_G2 Registers

3.15.186.1 CFG0_G2 Register (Offset = 788h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1721. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5788h

Figure 3-796. INTXBAR26_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							INTXBAR26_G2_SEL								
NONE							R/W								
0							0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR26_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1722. INTXBAR26_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24:0	INTXBAR26_G2_SEL	R/W	0h	Corresponding INT XBar G2 Input Select 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.15.187 CFG0_INTXBAR26_G3 Registers

3.15.187.1 CFG0_G3 Register (Offset = 78Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1723. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 578Ch

Figure 3-797. INTXBAR26_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR26_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-1724. INTXBAR26_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	INTXBAR26_G3_SEL	R/W	0h	Corresponding INT XBar G3 Input Select 0: FSIRX0.INT1N 1: FSIRX0.INT2N 2: FSIRX1.INT1N 3: FSIRX1.INT2N 4: FSIRX2.INT1N 5: FSIRX2.INT2N 6: FSIRX3.INT1N 7: FSIRX3.INT2N 8: FSITX0.INT1N 9: FSITX0.INT2N 10: FSITX1.INT1N 11: FSITX1.INT2N 12: FSITX2.INT1N 13: FSITX2.INT2N 14: FSITX3.INT1N 15: FSITX3.INT2N Reset Source: mod_g_rst_n

3.15.188 CFG0_INTXBAR26_G4 Registers

3.15.188.1 CFG0_G4 Register (Offset = 790h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1725. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5790h

Figure 3-798. INTXBAR26_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR26_G4_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1726. INTXBAR26_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR26_G4_SEL	R/W	0h	Corresponding INT XBar G4 Input Select 0: SD0.ERR 1: SD0.FILT1.DRINT 2: SD0.FILT2.DRINT 3: SD0.FILT3.DRINT 4: SD0.FILT4.DRINT 5: SD1.ERR 6: SD1.FILT1.DRINT 7: SD1.FILT2.DRINT 8: SD1.FILT3.DRINT 9: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.15.189 CFG0_INTXBAR26_G5 Registers

3.15.189.1 CFG0_G5 Register (Offset = 794h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1727. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5794h

Figure 3-799. INTXBAR26_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR26_G5_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1728. INTXBAR26_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR26_G5_SEL	R/W	0h	Corresponding INT XBar G5 Input Select 0: ECAP0.INT 1: ECAP1.INT 2: ECAP2.INT 3: ECAP3.INT 4: ECAP4.INT 5: ECAP5.INT 6: ECAP6.INT 7: ECAP7.INT 8: ECAP8.INT 9: ECAP9.INT Reset Source: mod_g_rst_n

3.15.190 CFG0_INTXBAR26_G6 Registers

3.15.190.1 CFG0_G6 Register (Offset = 798h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1729. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5798h

Figure 3-800. INTXBAR26_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													INTXBAR26_G6_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1730. INTXBAR26_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	INTXBAR26_G6_SEL	R/W	0h	Corresponding INT XBar G6 Input Select 0: EQEP0.INT 1: EQEP1.INT 2: EQEP2.INT Reset Source: mod_g_rst_n

3.15.191 CFG0_INTXBAR27_G0 Registers

3.15.191.1 CFG0_G0 Register (Offset = 7C0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1731. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 57C0h

Figure 3-801. INTXBAR27_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR27_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR27_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1732. INTXBAR27_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR27_G0_SEL	R/W	0h	ETPWM INT interrupt to corresponding xbar 1: PWMx.INT is selected 0: PWMx.INT is de-selected Reset Source: mod_g_rst_n

3.15.192 CFG0_INTXBAR27_G1 Registers

3.15.192.1 CFG0_G1 Register (Offset = 7C4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1733. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 57C4h

Figure 3-802. INTXBAR27_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR27_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR27_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1734. INTXBAR27_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR27_G1_SEL	R/W	0h	ETPWM TZINT interrupt to corresponding xbar 1: PWMx.TZINT is selected 0: PWMx.TZINT is de-selected Reset Source: mod_g_rst_n

3.15.193 CFG0_INTXBAR27_G2 Registers

3.15.193.1 CFG0_G2 Register (Offset = 7C8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1735. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 57C8h

Figure 3-803. INTXBAR27_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							INTXBAR27_G2_SEL								
NONE							R/W								
0							0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR27_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1736. INTXBAR27_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24:0	INTXBAR27_G2_SEL	R/W	0h	Corresponding INT XBar G2 Input Select 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.15.194 CFG0_INTXBAR27_G3 Registers

3.15.194.1 CFG0_G3 Register (Offset = 7CCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1737. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 57CCh

Figure 3-804. INTXBAR27_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR27_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-1738. INTXBAR27_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	INTXBAR27_G3_SEL	R/W	0h	Corresponding INT XBar G3 Input Select 0: FSIRX0.INT1N 1: FSIRX0.INT2N 2: FSIRX1.INT1N 3: FSIRX1.INT2N 4: FSIRX2.INT1N 5: FSIRX2.INT2N 6: FSIRX3.INT1N 7: FSIRX3.INT2N 8: FSITX0.INT1N 9: FSITX0.INT2N 10: FSITX1.INT1N 11: FSITX1.INT2N 12: FSITX2.INT1N 13: FSITX2.INT2N 14: FSITX3.INT1N 15: FSITX3.INT2N Reset Source: mod_g_rst_n

3.15.195 CFG0_INTXBAR27_G4 Registers

3.15.195.1 CFG0_G4 Register (Offset = 7D0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1739. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 57D0h

Figure 3-805. INTXBAR27_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR27_G4_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1740. INTXBAR27_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR27_G4_SEL	R/W	0h	Corresponding INT XBar G4 Input Select 0: SD0.ERR 1: SD0.FILT1.DRINT 2: SD0.FILT2.DRINT 3: SD0.FILT3.DRINT 4: SD0.FILT4.DRINT 5: SD1.ERR 6: SD1.FILT1.DRINT 7: SD1.FILT2.DRINT 8: SD1.FILT3.DRINT 9: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.15.196 CFG0_INTXBAR27_G5 Registers

3.15.196.1 CFG0_G5 Register (Offset = 7D4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1741. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 57D4h

Figure 3-806. INTXBAR27_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR27_G5_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1742. INTXBAR27_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR27_G5_SEL	R/W	0h	Corresponding INT XBar G5 Input Select 0: ECAP0.INT 1: ECAP1.INT 2: ECAP2.INT 3: ECAP3.INT 4: ECAP4.INT 5: ECAP5.INT 6: ECAP6.INT 7: ECAP7.INT 8: ECAP8.INT 9: ECAP9.INT Reset Source: mod_g_rst_n

3.15.197 CFG0_INTXBAR27_G6 Registers

3.15.197.1 CFG0_G6 Register (Offset = 7D8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1743. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 57D8h

Figure 3-807. INTXBAR27_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													INTXBAR27_G6_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1744. INTXBAR27_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	INTXBAR27_G6_SEL	R/W	0h	Corresponding INT XBar G6 Input Select 0: EQEP0.INT 1: EQEP1.INT 2: EQEP2.INT Reset Source: mod_g_rst_n

3.15.198 CFG0_INTXBAR28_G0 Registers

3.15.198.1 CFG0_G0 Register (Offset = 800h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1745. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5800h

Figure 3-808. INTXBAR28_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR28_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR28_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1746. INTXBAR28_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR28_G0_SEL	R/W	0h	ETPWM INT interrupt to corresponding xbar 1: PWMx.INT is selected 0: PWMx.INT is de-selected Reset Source: mod_g_rst_n

3.15.199 CFG0_INTXBAR28_G1 Registers

3.15.199.1 CFG0_G1 Register (Offset = 804h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1747. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5804h

Figure 3-809. INTXBAR28_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR28_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR28_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1748. INTXBAR28_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR28_G1_SEL	R/W	0h	ETPWM TZINT interrupt to corresponding xbar 1: PWMx.TZINT is selected 0: PWMx.TZINT is de-selected Reset Source: mod_g_rst_n

3.15.200 CFG0_INTXBAR28_G2 Registers

3.15.200.1 CFG0_G2 Register (Offset = 808h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1749. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5808h

Figure 3-810. INTXBAR28_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							INTXBAR28_G2_SEL								
NONE							R/W								
0							0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR28_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1750. INTXBAR28_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24:0	INTXBAR28_G2_SEL	R/W	0h	Corresponding INT XBar G2 Input Select 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.15.201 CFG0_INTXBAR28_G3 Registers

3.15.201.1 CFG0_G3 Register (Offset = 80Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1751. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 580Ch

Figure 3-811. INTXBAR28_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR28_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-1752. INTXBAR28_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	INTXBAR28_G3_SEL	R/W	0h	Corresponding INT XBar G3 Input Select 0: FSIRX0.INT1N 1: FSIRX0.INT2N 2: FSIRX1.INT1N 3: FSIRX1.INT2N 4: FSIRX2.INT1N 5: FSIRX2.INT2N 6: FSIRX3.INT1N 7: FSIRX3.INT2N 8: FSITX0.INT1N 9: FSITX0.INT2N 10: FSITX1.INT1N 11: FSITX1.INT2N 12: FSITX2.INT1N 13: FSITX2.INT2N 14: FSITX3.INT1N 15: FSITX3.INT2N Reset Source: mod_g_rst_n

3.15.202 CFG0_INTXBAR28_G4 Registers

3.15.202.1 CFG0_G4 Register (Offset = 810h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1753. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5810h

Figure 3-812. INTXBAR28_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR28_G4_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1754. INTXBAR28_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR28_G4_SEL	R/W	0h	Corresponding INT XBar G4 Input Select 0: SD0.ERR 1: SD0.FILT1.DRINT 2: SD0.FILT2.DRINT 3: SD0.FILT3.DRINT 4: SD0.FILT4.DRINT 5: SD1.ERR 6: SD1.FILT1.DRINT 7: SD1.FILT2.DRINT 8: SD1.FILT3.DRINT 9: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.15.203 CFG0_INTXBAR28_G5 Registers

3.15.203.1 CFG0_G5 Register (Offset = 814h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1755. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5814h

Figure 3-813. INTXBAR28_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR28_G5_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1756. INTXBAR28_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR28_G5_SEL	R/W	0h	Corresponding INT XBar G5 Input Select 0: ECAP0.INT 1: ECAP1.INT 2: ECAP2.INT 3: ECAP3.INT 4: ECAP4.INT 5: ECAP5.INT 6: ECAP6.INT 7: ECAP7.INT 8: ECAP8.INT 9: ECAP9.INT Reset Source: mod_g_rst_n

3.15.204 CFG0_INTXBAR28_G6 Registers

3.15.204.1 CFG0_G6 Register (Offset = 818h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1757. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5818h

Figure 3-814. INTXBAR28_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													INTXBAR28_G6_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1758. INTXBAR28_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	INTXBAR28_G6_SEL	R/W	0h	Corresponding INT XBar G6 Input Select 0: EQEP0.INT 1: EQEP1.INT 2: EQEP2.INT Reset Source: mod_g_rst_n

3.15.205 CFG0_INTXBAR29_G0 Registers

3.15.205.1 CFG0_G0 Register (Offset = 840h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1759. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5840h

Figure 3-815. INTXBAR29_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR29_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR29_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1760. INTXBAR29_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR29_G0_SEL	R/W	0h	ETPWM INT interrupt to corresponding xbar 1: PWMx.INT is selected 0: PWMx.INT is de-selected Reset Source: mod_g_rst_n

3.15.206 CFG0_INTXBAR29_G1 Registers

3.15.206.1 CFG0_G1 Register (Offset = 844h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1761. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5844h

Figure 3-816. INTXBAR29_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR29_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR29_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1762. INTXBAR29_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR29_G1_SEL	R/W	0h	ETPWM TZINT interrupt to corresponding xbar 1: PWMx.TZINT is selected 0: PWMx.TZINT is de-selected Reset Source: mod_g_rst_n

3.15.207 CFG0_INTXBAR29_G2 Registers

3.15.207.1 CFG0_G2 Register (Offset = 848h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1763. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5848h

Figure 3-817. INTXBAR29_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							INTXBAR29_G2_SEL								
NONE							R/W								
0							0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR29_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1764. INTXBAR29_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24:0	INTXBAR29_G2_SEL	R/W	0h	Corresponding INT XBar G2 Input Select 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.15.208 CFG0_INTXBAR29_G3 Registers

3.15.208.1 CFG0_G3 Register (Offset = 84Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1765. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 584Ch

Figure 3-818. INTXBAR29_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR29_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-1766. INTXBAR29_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	INTXBAR29_G3_SEL	R/W	0h	Corresponding INT XBar G3 Input Select 0: FSIRX0.INT1N 1: FSIRX0.INT2N 2: FSIRX1.INT1N 3: FSIRX1.INT2N 4: FSIRX2.INT1N 5: FSIRX2.INT2N 6: FSIRX3.INT1N 7: FSIRX3.INT2N 8: FSITX0.INT1N 9: FSITX0.INT2N 10: FSITX1.INT1N 11: FSITX1.INT2N 12: FSITX2.INT1N 13: FSITX2.INT2N 14: FSITX3.INT1N 15: FSITX3.INT2N Reset Source: mod_g_rst_n

3.15.209 CFG0_INTXBAR29_G4 Registers

3.15.209.1 CFG0_G4 Register (Offset = 850h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1767. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5850h

Figure 3-819. INTXBAR29_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR29_G4_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1768. INTXBAR29_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR29_G4_SEL	R/W	0h	Corresponding INT XBar G4 Input Select 0: SD0.ERR 1: SD0.FILT1.DRINT 2: SD0.FILT2.DRINT 3: SD0.FILT3.DRINT 4: SD0.FILT4.DRINT 5: SD1.ERR 6: SD1.FILT1.DRINT 7: SD1.FILT2.DRINT 8: SD1.FILT3.DRINT 9: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.15.210 CFG0_INTXBAR29_G5 Registers

3.15.210.1 CFG0_G5 Register (Offset = 854h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1769. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5854h

Figure 3-820. INTXBAR29_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR29_G5_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1770. INTXBAR29_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR29_G5_SEL	R/W	0h	Corresponding INT XBar G5 Input Select 0: ECAP0.INT 1: ECAP1.INT 2: ECAP2.INT 3: ECAP3.INT 4: ECAP4.INT 5: ECAP5.INT 6: ECAP6.INT 7: ECAP7.INT 8: ECAP8.INT 9: ECAP9.INT Reset Source: mod_g_rst_n

3.15.211 CFG0_INTXBAR29_G6 Registers

3.15.211.1 CFG0_G6 Register (Offset = 858h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1771. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5858h

Figure 3-821. INTXBAR29_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													INTXBAR29_G6_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1772. INTXBAR29_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	INTXBAR29_G6_SEL	R/W	0h	Corresponding INT XBar G6 Input Select 0: EQEP0.INT 1: EQEP1.INT 2: EQEP2.INT Reset Source: mod_g_rst_n

3.15.212 CFG0_INTXBAR30_G0 Registers

3.15.212.1 CFG0_G0 Register (Offset = 880h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1773. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5880h

Figure 3-822. INTXBAR30_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR30_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR30_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1774. INTXBAR30_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR30_G0_SEL	R/W	0h	ETPWM INT interrupt to corresponding xbar 1: PWMx.INT is selected 0: PWMx.INT is de-selected Reset Source: mod_g_rst_n

3.15.213 CFG0_INTXBAR30_G1 Registers

3.15.213.1 CFG0_G1 Register (Offset = 884h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1775. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5884h

Figure 3-823. INTXBAR30_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR30_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR30_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1776. INTXBAR30_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR30_G1_SEL	R/W	0h	ETPWM TZINT interrupt to corresponding xbar 1: PWMx.TZINT is selected 0: PWMx.TZINT is de-selected Reset Source: mod_g_rst_n

3.15.214 CFG0_INTXBAR30_G2 Registers

3.15.214.1 CFG0_G2 Register (Offset = 888h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1777. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5888h

Figure 3-824. INTXBAR30_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							INTXBAR30_G2_SEL								
NONE							R/W								
0							0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR30_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1778. INTXBAR30_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24:0	INTXBAR30_G2_SEL	R/W	0h	Corresponding INT XBar G2 Input Select 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.15.215 CFG0_INTXBAR30_G3 Registers

3.15.215.1 CFG0_G3 Register (Offset = 88Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1779. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 588Ch

Figure 3-825. INTXBAR30_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR30_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-1780. INTXBAR30_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	INTXBAR30_G3_SEL	R/W	0h	Corresponding INT XBar G3 Input Select 0: FSIRX0.INT1N 1: FSIRX0.INT2N 2: FSIRX1.INT1N 3: FSIRX1.INT2N 4: FSIRX2.INT1N 5: FSIRX2.INT2N 6: FSIRX3.INT1N 7: FSIRX3.INT2N 8: FSITX0.INT1N 9: FSITX0.INT2N 10: FSITX1.INT1N 11: FSITX1.INT2N 12: FSITX2.INT1N 13: FSITX2.INT2N 14: FSITX3.INT1N 15: FSITX3.INT2N Reset Source: mod_g_rst_n

3.15.216 CFG0_INTXBAR30_G4 Registers

3.15.216.1 CFG0_G4 Register (Offset = 890h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1781. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5890h

Figure 3-826. INTXBAR30_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR30_G4_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1782. INTXBAR30_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR30_G4_SEL	R/W	0h	Corresponding INT XBar G4 Input Select 0: SD0.ERR 1: SD0.FILT1.DRINT 2: SD0.FILT2.DRINT 3: SD0.FILT3.DRINT 4: SD0.FILT4.DRINT 5: SD1.ERR 6: SD1.FILT1.DRINT 7: SD1.FILT2.DRINT 8: SD1.FILT3.DRINT 9: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.15.217 CFG0_INTXBAR30_G5 Registers

3.15.217.1 CFG0_G5 Register (Offset = 894h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1783. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5894h

Figure 3-827. INTXBAR30_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR30_G5_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1784. INTXBAR30_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR30_G5_SEL	R/W	0h	Corresponding INT XBar G5 Input Select 0: ECAP0.INT 1: ECAP1.INT 2: ECAP2.INT 3: ECAP3.INT 4: ECAP4.INT 5: ECAP5.INT 6: ECAP6.INT 7: ECAP7.INT 8: ECAP8.INT 9: ECAP9.INT Reset Source: mod_g_rst_n

3.15.218 CFG0_INTXBAR30_G6 Registers

3.15.218.1 CFG0_G6 Register (Offset = 898h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1785. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 5898h

Figure 3-828. INTXBAR30_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													INTXBAR30_G6_SEL		
NONE													R/W		
0													0h		

Access Types Legend

Table 3-1786. INTXBAR30_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	INTXBAR30_G6_SEL	R/W	0h	Corresponding INT XBar G6 Input Select 0: EQEP0.INT 1: EQEP1.INT 2: EQEP2.INT Reset Source: mod_g_rst_n

3.15.219 CFG0_INTXBAR31_G0 Registers

3.15.219.1 CFG0_G0 Register (Offset = 8C0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1787. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 58C0h

Figure 3-829. INTXBAR31_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR31_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR31_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1788. INTXBAR31_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR31_G0_SEL	R/W	0h	ETPWM INT interrupt to corresponding xbar 1: PWMx.INT is selected 0: PWMx.INT is de-selected Reset Source: mod_g_rst_n

3.15.220 CFG0_INTXBAR31_G1 Registers

3.15.220.1 CFG0_G1 Register (Offset = 8C4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1789. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 58C4h

Figure 3-830. INTXBAR31_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTXBAR31_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR31_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1790. INTXBAR31_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR31_G1_SEL	R/W	0h	ETPWM TZINT interrupt to corresponding xbar 1: PWMx.TZINT is selected 0: PWMx.TZINT is de-selected Reset Source: mod_g_rst_n

3.15.221 CFG0_INTXBAR31_G2 Registers

3.15.221.1 CFG0_G2 Register (Offset = 8C8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1791. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 58C8h

Figure 3-831. INTXBAR31_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							INTXBAR31_G2_SEL								
NONE							R/W								
0							0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR31_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1792. INTXBAR31_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24:0	INTXBAR31_G2_SEL	R/W	0h	Corresponding INT XBar G2 Input Select 0: ADC0.INT1 1: ADC0.INT2 2: ADC0.INT3 3: ADC0.INT4 4: ADC0.EVTINT 5: ADC1.INT1 6: ADC1.INT2 7: ADC1.INT3 8: ADC1.INT4 9: ADC1.EVTINT 10: ADC2.INT1 11: ADC2.INT2 12: ADC2.INT3 13: ADC2.INT4 14: ADC2.EVTINT 15: ADC3.INT1 16: ADC3.INT2 17: ADC3.INT3 18: ADC3.INT4 19: ADC3.EVTINT 20: ADC4.INT1 21: ADC4.INT2 22: ADC4.INT3 23: ADC4.INT4 24: ADC4.EVTINT Reset Source: mod_g_rst_n

3.15.222 CFG0_INTXBAR31_G3 Registers

3.15.222.1 CFG0_G3 Register (Offset = 8CCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1793. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 58CCh

Figure 3-832. INTXBAR31_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTXBAR31_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-1794. INTXBAR31_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	INTXBAR31_G3_SEL	R/W	0h	Corresponding INT XBar G3 Input Select 0: FSIRX0.INT1N 1: FSIRX0.INT2N 2: FSIRX1.INT1N 3: FSIRX1.INT2N 4: FSIRX2.INT1N 5: FSIRX2.INT2N 6: FSIRX3.INT1N 7: FSIRX3.INT2N 8: FSITX0.INT1N 9: FSITX0.INT2N 10: FSITX1.INT1N 11: FSITX1.INT2N 12: FSITX2.INT1N 13: FSITX2.INT2N 14: FSITX3.INT1N 15: FSITX3.INT2N Reset Source: mod_g_rst_n

3.15.223 CFG0_INTXBAR31_G4 Registers

3.15.223.1 CFG0_G4 Register (Offset = 8D0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1795. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 58D0h

Figure 3-833. INTXBAR31_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR31_G4_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1796. INTXBAR31_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR31_G4_SEL	R/W	0h	Corresponding INT XBar G4 Input Select 0: SD0.ERR 1: SD0.FILT1.DRINT 2: SD0.FILT2.DRINT 3: SD0.FILT3.DRINT 4: SD0.FILT4.DRINT 5: SD1.ERR 6: SD1.FILT1.DRINT 7: SD1.FILT2.DRINT 8: SD1.FILT3.DRINT 9: SD1.FILT4.DRINT Reset Source: mod_g_rst_n

3.15.224 CFG0_INTXBAR31_G5 Registers

3.15.224.1 CFG0_G5 Register (Offset = 8D4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1797. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 58D4h

Figure 3-834. INTXBAR31_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTXBAR31_G5_SEL									
NONE						R/W									
0						0h									

Access Types Legend

Table 3-1798. INTXBAR31_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	INTXBAR31_G5_SEL	R/W	0h	Corresponding INT XBar G5 Input Select 0: ECAP0.INT 1: ECAP1.INT 2: ECAP2.INT 3: ECAP3.INT 4: ECAP4.INT 5: ECAP5.INT 6: ECAP6.INT 7: ECAP7.INT 8: ECAP8.INT 9: ECAP9.INT Reset Source: mod_g_rst_n

3.15.225 CFG0_INTXBAR31_G6 Registers

3.15.225.1 CFG0_G6 Register (Offset = 8D8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1799. Instance Table

Instance Name	Physical Address
INTXBAR_MMR	502D 58D8h

Figure 3-835. INTXBAR31_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															INTXBAR31_G6_SEL
NONE															R/W
0															0h

Access Types Legend

Table 3-1800. INTXBAR31_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	INTXBAR31_G6_SEL	R/W	0h	Corresponding INT XBar G6 Input Select 0: EQEP0.INT 1: EQEP1.INT 2: EQEP2.INT Reset Source: mod_g_rst_n

3.15.226 Access Table

Table 3-1801. Access Type Codes

Access Type	Code	Description
R	R	Read
R/W	R/W	Read / Write

3.16 MDLXBAR Registers

Table 3-1802. CFG0, CFG0 Registers, Base Address=0X00000000502D3000, Length=2048

Offset	Length	Register Name	mdlxbar_mmr Physical Address
0h	32	PID	502D 3000h
100h	32	MDLXBar0_G0	502D 3100h
104h	32	MDLXBar0_G1	502D 3104h
108h	32	MDLXBar0_G2	502D 3108h
140h	32	MDLXBar1_G0	502D 3140h
144h	32	MDLXBar1_G1	502D 3144h
148h	32	MDLXBar1_G2	502D 3148h
180h	32	MDLXBar2_G0	502D 3180h
184h	32	MDLXBar2_G1	502D 3184h
188h	32	MDLXBar2_G2	502D 3188h
1C0h	32	MDLXBar3_G0	502D 31C0h
1C4h	32	MDLXBar3_G1	502D 31C4h
1C8h	32	MDLXBar3_G2	502D 31C8h
200h	32	MDLXBar4_G0	502D 3200h
204h	32	MDLXBar4_G1	502D 3204h
208h	32	MDLXBar4_G2	502D 3208h
240h	32	MDLXBar5_G0	502D 3240h
244h	32	MDLXBar5_G1	502D 3244h
248h	32	MDLXBar5_G2	502D 3248h
280h	32	MDLXBar6_G0	502D 3280h
284h	32	MDLXBar6_G1	502D 3284h
288h	32	MDLXBar6_G2	502D 3288h
2C0h	32	MDLXBar7_G0	502D 32C0h
2C4h	32	MDLXBar7_G1	502D 32C4h
2C8h	32	MDLXBar7_G2	502D 32C8h
300h	32	MDLXBar8_G0	502D 3300h
304h	32	MDLXBar8_G1	502D 3304h
308h	32	MDLXBar8_G2	502D 3308h
340h	32	MDLXBar9_G0	502D 3340h
344h	32	MDLXBar9_G1	502D 3344h
348h	32	MDLXBar9_G2	502D 3348h
380h	32	MDLXBar10_G0	502D 3380h
384h	32	MDLXBar10_G1	502D 3384h
388h	32	MDLXBar10_G2	502D 3388h
3C0h	32	MDLXBar11_G0	502D 33C0h
3C4h	32	MDLXBar11_G1	502D 33C4h
3C8h	32	MDLXBar11_G2	502D 33C8h
400h	32	MDLXBar12_G0	502D 3400h
404h	32	MDLXBar12_G1	502D 3404h
408h	32	MDLXBar12_G2	502D 3408h
440h	32	MDLXBar13_G0	502D 3440h
444h	32	MDLXBar13_G1	502D 3444h
448h	32	MDLXBar13_G2	502D 3448h
480h	32	MDLXBar14_G0	502D 3480h
484h	32	MDLXBar14_G1	502D 3484h

Table 3-1802. CFG0, CFG0 Registers, Base Address=0X00000000502D3000, Length=2048 (continued)

Offset	Length	Register Name	mdlxbar_mmr Physical Address
488h	32	MDLXBar14_G2	502D 3488h
4C0h	32	MDLXBar15_G0	502D 34C0h
4C4h	32	MDLXBar15_G1	502D 34C4h
4C8h	32	MDLXBar15_G2	502D 34C8h

3.16.1 CFG0_PID Registers

3.16.1.1 CFG0_PID Register (Offset = 0h) [reset = 61800215h]

Short Description: PID register

Long Description: PID register

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Table 3-1803. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3000h

Figure 3-836. PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PID_MSB16															
R															
6180h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_MISC					PID_MAJOR			PID_CUSTOM		PID_MINOR					
R					R			R		R					
0h					2h			0h		15h					

Access Types Legend

Table 3-1804. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR	R	15h	Reset Source: mod_g_rst_n

3.16.2 CFG0_MDLXBAR0_G0 Registers

3.16.2.1 CFG0_G0 Register (Offset = 100h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1805. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3100h

Figure 3-837. MDLXBAR0_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR0_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR0_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1806. MDLXBAR0_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR0_G0_SEL	R/W	0h	MDL XBar0 G0 input bit select. Input source is PWMA sclk select 1: PWMA sclk bit[x] selected 0: PWMA sclk bit[x] is de-selected Reset Source: mod_g_rst_n

3.16.3 CFG0_MDLXBAR0_G1 Registers

3.16.3.1 CFG0_G1 Register (Offset = 104h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1807. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3104h

Figure 3-838. MDLXBAR0_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR0_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR0_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1808. MDLXBAR0_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR0_G1_SEL	R/W	0h	MDL XBar0 G1 input bit select. Input source is PWMB sclk select 1: PWMB sclk bit[x] selected 0: PWMB sclk bit[x] is de-selected Reset Source: mod_g_rst_n

3.16.4 CFG0_MDLXBAR0_G2 Registers

3.16.4.1 CFG0_G2 Register (Offset = 108h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1809. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3108h

Figure 3-839. MDLXBAR0_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR0_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR0_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1810. MDLXBAR0_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR0_G2_SEL	R/W	0h	MDL XBar0 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1: ICSS_PORT[y].GPO[x] selected. 0: ICSS_PORT[y].GPO[x] is de-selected Reset Source: mod_g_rst_n

3.16.5 CFG0_MDLXBAR1_G0 Registers

3.16.5.1 CFG0_G0 Register (Offset = 140h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1811. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3140h

Figure 3-840. MDLXBAR1_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR1_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR1_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1812. MDLXBAR1_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR1_G0_SEL	R/W	0h	MDL XBar1 G0 input bit select. Input source is PWMA sclk select 1: PWMA sclk bit[x] selected 0: PWMA sclk bit[x] is de-selected Reset Source: mod_g_rst_n

3.16.6 CFG0_MDLXBAR1_G1 Registers

3.16.6.1 CFG0_G1 Register (Offset = 144h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1813. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3144h

Figure 3-841. MDLXBAR1_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR1_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR1_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1814. MDLXBAR1_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR1_G1_SEL	R/W	0h	MDL XBar1 G1 input bit select. Input source is PWMB sclk select 1: PWMB sclk bit[x] selected 0: PWMB sclk bit[x] is de-selected Reset Source: mod_g_rst_n

3.16.7 CFG0_MDLXBAR1_G2 Registers

3.16.7.1 CFG0_G2 Register (Offset = 148h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1815. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3148h

Figure 3-842. MDLXBAR1_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR1_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR1_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1816. MDLXBAR1_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR1_G2_SEL	R/W	0h	MDL XBar1 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1: ICSS_PORT[y].GPO[x] selected. 0: ICSS_PORT[y].GPO[x] is de-selected Reset Source: mod_g_rst_n

3.16.8 CFG0_MDLXBAR2_G0 Registers

3.16.8.1 CFG0_G0 Register (Offset = 180h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1817. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3180h

Figure 3-843. MDLXBAR2_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR2_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR2_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1818. MDLXBAR2_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR2_G0_SEL	R/W	0h	MDL XBar2 G0 input bit select. Input source is PWMA sclk select 1: PWMA sclk bit[x] selected 0: PWMA sclk bit[x] is de-selected Reset Source: mod_g_rst_n

3.16.9 CFG0_MDLXBAR2_G1 Registers

3.16.9.1 CFG0_G1 Register (Offset = 184h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1819. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3184h

Figure 3-844. MDLXBAR2_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR2_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR2_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1820. MDLXBAR2_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR2_G1_SEL	R/W	0h	MDL XBar2 G1 input bit select. Input source is PWMB sclk select 1: PWMB sclk bit[x] selected 0: PWMB sclk bit[x] is de-selected Reset Source: mod_g_rst_n

3.16.10 CFG0_MDLXBAR2_G2 Registers

3.16.10.1 CFG0_G2 Register (Offset = 188h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1821. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3188h

Figure 3-845. MDLXBAR2_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR2_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR2_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1822. MDLXBAR2_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR2_G2_SEL	R/W	0h	MDL XBar2 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1: ICSS_PORT[y].GPO[x] selected. 0: ICSS_PORT[y].GPO[x] is de-selected Reset Source: mod_g_rst_n

3.16.11 CFG0_MDLXBAR3_G0 Registers

3.16.11.1 CFG0_G0 Register (Offset = 1C0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1823. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 31C0h

Figure 3-846. MDLXBAR3_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR3_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR3_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1824. MDLXBAR3_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR3_G0_SEL	R/W	0h	MDL XBar3 G0 input bit select. Input source is PWMA sclk select 1: PWMA sclk bit[x] selected 0: PWMA sclk bit[x] is de-selected Reset Source: mod_g_rst_n

3.16.12 CFG0_MDLXBAR3_G1 Registers

3.16.12.1 CFG0_G1 Register (Offset = 1C4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1825. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 31C4h

Figure 3-847. MDLXBAR3_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR3_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR3_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1826. MDLXBAR3_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR3_G1_SEL	R/W	0h	MDL XBar3 G1 input bit select. Input source is PWMB sclk select 1: PWMB sclk bit[x] selected 0: PWMB sclk bit[x] is de-selected Reset Source: mod_g_rst_n

3.16.13 CFG0_MDLXBAR3_G2 Registers

3.16.13.1 CFG0_G2 Register (Offset = 1C8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1827. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 31C8h

Figure 3-848. MDLXBAR3_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR3_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR3_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1828. MDLXBAR3_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR3_G2_SEL	R/W	0h	MDL XBar3 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1: ICSS_PORT[y].GPO[x] selected. 0: ICSS_PORT[y].GPO[x] is de-selected Reset Source: mod_g_rst_n

3.16.14 CFG0_MDLXBAR4_G0 Registers

3.16.14.1 CFG0_G0 Register (Offset = 200h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1829. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3200h

Figure 3-849. MDLXBAR4_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR4_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR4_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1830. MDLXBAR4_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR4_G0_SEL	R/W	0h	MDL XBar4 G0 input bit select. Input source is PWMA sclk select 1: PWMA sclk bit[x] selected 0: PWMA sclk bit[x] is de-selected Reset Source: mod_g_rst_n

3.16.15 CFG0_MDLXBAR4_G1 Registers

3.16.15.1 CFG0_G1 Register (Offset = 204h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1831. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3204h

Figure 3-850. MDLXBAR4_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR4_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR4_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1832. MDLXBAR4_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR4_G1_SEL	R/W	0h	MDL XBar4 G1 input bit select. Input source is PWMB sclk select 1: PWMB sclk bit[x] selected 0: PWMB sclk bit[x] is de-selected Reset Source: mod_g_rst_n

3.16.16 CFG0_MDLXBAR4_G2 Registers

3.16.16.1 CFG0_G2 Register (Offset = 208h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1833. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3208h

Figure 3-851. MDLXBAR4_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR4_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR4_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1834. MDLXBAR4_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR4_G2_SEL	R/W	0h	MDL XBar4 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1: ICSS_PORT[y].GPO[x] selected. 0: ICSS_PORT[y].GPO[x] is de-selected Reset Source: mod_g_rst_n

3.16.17 CFG0_MDLXBAR5_G0 Registers

3.16.17.1 CFG0_G0 Register (Offset = 240h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1835. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3240h

Figure 3-852. MDLXBAR5_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR5_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR5_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1836. MDLXBAR5_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR5_G0_SEL	R/W	0h	MDL XBar5 G0 input bit select. Input source is PWMA sclk select 1: PWMA sclk bit[x] selected 0: PWMA sclk bit[x] is de-selected Reset Source: mod_g_rst_n

3.16.18 CFG0_MDLXBAR5_G1 Registers

3.16.18.1 CFG0_G1 Register (Offset = 244h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1837. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3244h

Figure 3-853. MDLXBAR5_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR5_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR5_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1838. MDLXBAR5_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR5_G1_SEL	R/W	0h	MDL XBar5 G1 input bit select. Input source is PWMB sclk select 1: PWMB sclk bit[x] selected 0: PWMB sclk bit[x] is de-selected Reset Source: mod_g_rst_n

3.16.19 CFG0_MDLXBAR5_G2 Registers

3.16.19.1 CFG0_G2 Register (Offset = 248h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1839. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3248h

Figure 3-854. MDLXBAR5_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR5_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR5_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1840. MDLXBAR5_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR5_G2_SEL	R/W	0h	MDL XBar5 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1: ICSS_PORT[y].GPO[x] selected. 0: ICSS_PORT[y].GPO[x] is de-selected Reset Source: mod_g_rst_n

3.16.20 CFG0_MDLXBAR6_G0 Registers

3.16.20.1 CFG0_G0 Register (Offset = 280h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1841. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3280h

Figure 3-855. MDLXBAR6_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR6_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR6_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1842. MDLXBAR6_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR6_G0_SEL	R/W	0h	MDL XBar6 G0 input bit select. Input source is PWMA sclk select 1: PWMA sclk bit[x] selected 0: PWMA sclk bit[x] is de-selected Reset Source: mod_g_rst_n

3.16.21 CFG0_MDLXBAR6_G1 Registers

3.16.21.1 CFG0_G1 Register (Offset = 284h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1843. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3284h

Figure 3-856. MDLXBAR6_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR6_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR6_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1844. MDLXBAR6_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR6_G1_SEL	R/W	0h	MDL XBar6 G1 input bit select. Input source is PWMB sclk select 1: PWMB sclk bit[x] selected 0: PWMB sclk bit[x] is de-selected Reset Source: mod_g_rst_n

3.16.22 CFG0_MDLXBAR6_G2 Registers

3.16.22.1 CFG0_G2 Register (Offset = 288h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1845. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3288h

Figure 3-857. MDLXBAR6_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR6_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR6_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1846. MDLXBAR6_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR6_G2_SEL	R/W	0h	MDL XBar6 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1: ICSS_PORT[y].GPO[x] selected. 0: ICSS_PORT[y].GPO[x] is de-selected Reset Source: mod_g_rst_n

3.16.23 CFG0_MDLXBAR7_G0 Registers

3.16.23.1 CFG0_G0 Register (Offset = 2C0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1847. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 32C0h

Figure 3-858. MDLXBAR7_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR7_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR7_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1848. MDLXBAR7_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR7_G0_SEL	R/W	0h	MDL XBar7 G0 input bit select. Input source is PWMA sclk select 1: PWMA sclk bit[x] selected 0: PWMA sclk bit[x] is de-selected Reset Source: mod_g_rst_n

3.16.24 CFG0_MDLXBAR7_G1 Registers

3.16.24.1 CFG0_G1 Register (Offset = 2C4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1849. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 32C4h

Figure 3-859. MDLXBAR7_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR7_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR7_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1850. MDLXBAR7_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR7_G1_SEL	R/W	0h	MDL XBar7 G1 input bit select. Input source is PWMB sclk select 1: PWMB sclk bit[x] selected 0: PWMB sclk bit[x] is de-selected Reset Source: mod_g_rst_n

3.16.25 CFG0_MDLXBAR7_G2 Registers

3.16.25.1 CFG0_G2 Register (Offset = 2C8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1851. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 32C8h

Figure 3-860. MDLXBAR7_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR7_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR7_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1852. MDLXBAR7_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR7_G2_SEL	R/W	0h	MDL XBar7 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1: ICSS_PORT[y].GPO[x] selected. 0: ICSS_PORT[y].GPO[x] is de-selected Reset Source: mod_g_rst_n

3.16.26 CFG0_MDLXBAR8_G0 Registers

3.16.26.1 CFG0_G0 Register (Offset = 300h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1853. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3300h

Figure 3-861. MDLXBAR8_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR8_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR8_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1854. MDLXBAR8_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR8_G0_SEL	R/W	0h	MDL XBar8 G0 input bit select. Input source is PWMA sclk select 1: PWMA sclk bit[x] selected 0: PWMA sclk bit[x] is de-selected Reset Source: mod_g_rst_n

3.16.27 CFG0_MDLXBAR8_G1 Registers

3.16.27.1 CFG0_G1 Register (Offset = 304h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1855. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3304h

Figure 3-862. MDLXBAR8_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR8_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR8_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1856. MDLXBAR8_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR8_G1_SEL	R/W	0h	MDL XBar8 G1 input bit select. Input source is PWMB sclk select 1: PWMB sclk bit[x] selected 0: PWMB sclk bit[x] is de-selected Reset Source: mod_g_rst_n

3.16.28 CFG0_MDLXBAR8_G2 Registers

3.16.28.1 CFG0_G2 Register (Offset = 308h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1857. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3308h

Figure 3-863. MDLXBAR8_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR8_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR8_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1858. MDLXBAR8_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR8_G2_SEL	R/W	0h	MDL XBar8 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1: ICSS_PORT[y].GPO[x] selected. 0: ICSS_PORT[y].GPO[x] is de-selected Reset Source: mod_g_rst_n

3.16.29 CFG0_MDLXBAR9_G0 Registers

3.16.29.1 CFG0_G0 Register (Offset = 340h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1859. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3340h

Figure 3-864. MDLXBAR9_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR9_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR9_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1860. MDLXBAR9_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR9_G0_SEL	R/W	0h	MDL XBar9 G0 input bit select. Input source is PWMA sclk select 1: PWMA sclk bit[x] selected 0: PWMA sclk bit[x] is de-selected Reset Source: mod_g_rst_n

3.16.30 CFG0_MDLXBAR9_G1 Registers

3.16.30.1 CFG0_G1 Register (Offset = 344h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1861. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3344h

Figure 3-865. MDLXBAR9_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR9_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR9_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1862. MDLXBAR9_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR9_G1_SEL	R/W	0h	MDL XBar9 G1 input bit select. Input source is PWMB sclk select 1: PWMB sclk bit[x] selected 0: PWMB sclk bit[x] is de-selected Reset Source: mod_g_rst_n

3.16.31 CFG0_MDLXBAR9_G2 Registers

3.16.31.1 CFG0_G2 Register (Offset = 348h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1863. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3348h

Figure 3-866. MDLXBAR9_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR9_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR9_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1864. MDLXBAR9_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR9_G2_SEL	R/W	0h	MDL XBar9 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1: ICSS_PORT[y].GPO[x] selected. 0: ICSS_PORT[y].GPO[x] is de-selected Reset Source: mod_g_rst_n

3.16.32 CFG0_MDLXBAR10_G0 Registers

3.16.32.1 CFG0_G0 Register (Offset = 380h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1865. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3380h

Figure 3-867. MDLXBAR10_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR10_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR10_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1866. MDLXBAR10_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR10_G0_SEL	R/W	0h	MDL XBar10 G0 input bit select. Input source is PWMA sclk select 1: PWMA sclk bit[x] selected 0: PWMA sclk bit[x] is de-selected Reset Source: mod_g_rst_n

3.16.33 CFG0_MDLXBAR10_G1 Registers

3.16.33.1 CFG0_G1 Register (Offset = 384h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1867. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3384h

Figure 3-868. MDLXBAR10_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR10_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR10_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1868. MDLXBAR10_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR10_G1_SEL	R/W	0h	MDL XBar10 G1 input bit select. Input source is PWMB sclk select 1: PWMB sclk bit[x] selected 0: PWMB sclk bit[x] is de-selected Reset Source: mod_g_rst_n

3.16.34 CFG0_MDLXBAR10_G2 Registers

3.16.34.1 CFG0_G2 Register (Offset = 388h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1869. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3388h

Figure 3-869. MDLXBAR10_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR10_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR10_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1870. MDLXBAR10_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR10_G2_SEL	R/W	0h	MDL XBar10 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1: ICSS_PORT[y].GPO[x] selected. 0: ICSS_PORT[y].GPO[x] is de-selected Reset Source: mod_g_rst_n

3.16.35 CFG0_MDLXBAR11_G0 Registers

3.16.35.1 CFG0_G0 Register (Offset = 3C0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1871. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 33C0h

Figure 3-870. MDLXBAR11_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR11_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR11_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1872. MDLXBAR11_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR11_G0_SEL	R/W	0h	MDL XBar11 G0 input bit select. Input source is PWMA sclk select 1: PWMA sclk bit[x] selected 0: PWMA sclk bit[x] is de-selected Reset Source: mod_g_rst_n

3.16.36 CFG0_MDLXBAR11_G1 Registers

3.16.36.1 CFG0_G1 Register (Offset = 3C4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1873. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 33C4h

Figure 3-871. MDLXBAR11_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR11_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR11_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1874. MDLXBAR11_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR11_G1_SEL	R/W	0h	MDL XBar11 G1 input bit select. Input source is PWMB sclk select 1: PWMB sclk bit[x] selected 0: PWMB sclk bit[x] is de-selected Reset Source: mod_g_rst_n

3.16.37 CFG0_MDLXBAR11_G2 Registers

3.16.37.1 CFG0_G2 Register (Offset = 3C8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1875. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 33C8h

Figure 3-872. MDLXBAR11_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR11_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR11_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1876. MDLXBAR11_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR11_G2_SEL	R/W	0h	MDL XBar11 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1: ICSS_PORT[y].GPO[x] selected. 0: ICSS_PORT[y].GPO[x] is de-selected Reset Source: mod_g_rst_n

3.16.38 CFG0_MDLXBAR12_G0 Registers

3.16.38.1 CFG0_G0 Register (Offset = 400h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1877. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3400h

Figure 3-873. MDLXBAR12_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR12_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR12_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1878. MDLXBAR12_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR12_G0_SEL	R/W	0h	MDL XBar12 G0 input bit select. Input source is PWMA sclk select 1: PWMA sclk bit[x] selected 0: PWMA sclk bit[x] is de-selected Reset Source: mod_g_rst_n

3.16.39 CFG0_MDLXBAR12_G1 Registers

3.16.39.1 CFG0_G1 Register (Offset = 404h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1879. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3404h

Figure 3-874. MDLXBAR12_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR12_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR12_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1880. MDLXBAR12_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR12_G1_SEL	R/W	0h	MDL XBar12 G1 input bit select. Input source is PWMB sclk select 1: PWMB sclk bit[x] selected 0: PWMB sclk bit[x] is de-selected Reset Source: mod_g_rst_n

3.16.40 CFG0_MDLXBAR12_G2 Registers

3.16.40.1 CFG0_G2 Register (Offset = 408h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1881. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3408h

Figure 3-875. MDLXBAR12_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR12_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR12_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1882. MDLXBAR12_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR12_G2_SEL	R/W	0h	MDL XBar12 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1: ICSS_PORT[y].GPO[x] selected. 0: ICSS_PORT[y].GPO[x] is de-selected Reset Source: mod_g_rst_n

3.16.41 CFG0_MDLXBAR13_G0 Registers

3.16.41.1 CFG0_G0 Register (Offset = 440h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1883. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3440h

Figure 3-876. MDLXBAR13_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR13_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR13_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1884. MDLXBAR13_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR13_G0_SEL	R/W	0h	MDL XBar13 G0 input bit select. Input source is PWMA sclk select 1: PWMA sclk bit[x] selected 0: PWMA sclk bit[x] is de-selected Reset Source: mod_g_rst_n

3.16.42 CFG0_MDLXBAR13_G1 Registers

3.16.42.1 CFG0_G1 Register (Offset = 444h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1885. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3444h

Figure 3-877. MDLXBAR13_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR13_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR13_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1886. MDLXBAR13_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR13_G1_SEL	R/W	0h	MDL XBar13 G1 input bit select. Input source is PWMB sclk select 1: PWMB sclk bit[x] selected 0: PWMB sclk bit[x] is de-selected Reset Source: mod_g_rst_n

3.16.43 CFG0_MDLXBAR13_G2 Registers

3.16.43.1 CFG0_G2 Register (Offset = 448h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1887. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3448h

Figure 3-878. MDLXBAR13_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR13_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR13_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1888. MDLXBAR13_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR13_G2_SEL	R/W	0h	MDL XBar13 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1: ICSS_PORT[y].GPO[x] selected. 0: ICSS_PORT[y].GPO[x] is de-selected Reset Source: mod_g_rst_n

3.16.44 CFG0_MDLXBAR14_G0 Registers

3.16.44.1 CFG0_G0 Register (Offset = 480h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1889. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3480h

Figure 3-879. MDLXBAR14_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR14_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR14_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1890. MDLXBAR14_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR14_G0_SEL	R/W	0h	MDL XBar14 G0 input bit select. Input source is PWMA sclk select 1: PWMA sclk bit[x] selected 0: PWMA sclk bit[x] is de-selected Reset Source: mod_g_rst_n

3.16.45 CFG0_MDLXBAR14_G1 Registers

3.16.45.1 CFG0_G1 Register (Offset = 484h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1891. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3484h

Figure 3-880. MDLXBAR14_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR14_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR14_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1892. MDLXBAR14_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR14_G1_SEL	R/W	0h	MDL XBar14 G1 input bit select. Input source is PWMB sclk select 1: PWMB sclk bit[x] selected 0: PWMB sclk bit[x] is de-selected Reset Source: mod_g_rst_n

3.16.46 CFG0_MDLXBAR14_G2 Registers

3.16.46.1 CFG0_G2 Register (Offset = 488h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1893. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 3488h

Figure 3-881. MDLXBAR14_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR14_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR14_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1894. MDLXBAR14_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR14_G2_SEL	R/W	0h	MDL XBar14 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1: ICSS_PORT[y].GPO[x] selected. 0: ICSS_PORT[y].GPO[x] is de-selected Reset Source: mod_g_rst_n

3.16.47 CFG0_MDLXBAR15_G0 Registers

3.16.47.1 CFG0_G0 Register (Offset = 4C0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1895. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 34C0h

Figure 3-882. MDLXBAR15_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR15_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR15_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1896. MDLXBAR15_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR15_G0_SEL	R/W	0h	MDL XBar15 G0 input bit select. Input source is PWMA sclk select 1: PWMA sclk bit[x] selected 0: PWMA sclk bit[x] is de-selected Reset Source: mod_g_rst_n

3.16.48 CFG0_MDLXBAR15_G1 Registers

3.16.48.1 CFG0_G1 Register (Offset = 4C4h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1897. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 34C4h

Figure 3-883. MDLXBAR15_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR15_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR15_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1898. MDLXBAR15_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR15_G1_SEL	R/W	0h	MDL XBar15 G1 input bit select. Input source is PWMB sclk select 1: PWMB sclk bit[x] selected 0: PWMB sclk bit[x] is de-selected Reset Source: mod_g_rst_n

3.16.49 CFG0_MDLXBAR15_G2 Registers

3.16.49.1 CFG0_G2 Register (Offset = 4C8h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1899. Instance Table

Instance Name	Physical Address
MDLXBAR_MMR	502D 34C8h

Figure 3-884. MDLXBAR15_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MDLXBAR15_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDLXBAR15_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1900. MDLXBAR15_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR15_G2_SEL	R/W	0h	MDL XBar15 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1: ICSS_PORT[y].GPO[x] selected. 0: ICSS_PORT[y].GPO[x] is de-selected Reset Source: mod_g_rst_n

3.16.50 Access Table

Table 3-1901. Access Type Codes

Access Type	Code	Description
R	R	Read
R/W	R/W	Read / Write

3.17 OTTOCAL Registers

Table 3-1902. MEM, MEM Registers, Base Address=0X00000000502E0000, Length=4096

Offset	Length	Register Name	ottocal0 Physical Address	ottocal1 Physical Address	ottocal2 Physical Address
42h	16	HRPWR	502E 0042h	502E 1042h	502E 2042h
44h	16	HRCAL	502E 0044h	502E 1044h	502E 2044h
46h	16	HRPRD	502E 0046h	502E 1046h	502E 2046h
48h	16	HRCNT0	502E 0048h	502E 1048h	502E 2048h
4Ah	16	HRCNT1	502E 004Ah	502E 104Ah	502E 204Ah
4Ch	16	HRMSTEP	502E 004Ch	502E 104Ch	502E 204Ch

3.17.1 MEM_HRPWR Registers

3.17.1.1 MEM_HRPWR Register (Offset = 42h) [reset = 0h]

Short Description: HRPWM Power Register T

Long Description: HRPWM Power Register This register is only accessible on EPWM modules with HRPWM capabilities.

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Table 3-1903. Instance Table

Instance Name	Physical Address
OTTOCAL0	502E 0042h
OTTOCAL1	502E 1042h
OTTOCAL2	502E 2042h
OTTOCAL3	502E 3042h

Figure 3-885. HRPWR Name Register

15	14	13	12	11	10	9	8
CALPWRON	RESERVED_1					CALSEL	
R/W	R					R/W	
0h	0h					0h	
7	6	5	4	3	2	1	0
CALSEL		TESTSEL	CALSTS	CNTSEL	CALSTART	CALMODE	
R/W		R/W	R	R/W	R/W	R/W	
0h		0h	0h	0h	0h	0h	

Access Types Legend

Table 3-1904. HRPWR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CALPWRON	R/W	0h	MEP Calibration Power Bits [only available on ePWM1] 0: Disables MEP calibration logic in the HRPWM and reduces power consumption. 1: Enables MEP calibration logic Reset Source: ottocal_rst_mod_g_rst_n
14:10	RESERVED_1	R	0h	Reserved Reset Source: ottocal_rst_mod_g_rst_n
9:6	CALSEL	R/W	0h	EPWM Delay Line Selection for Calibration: Reset Source: ottocal_rst_mod_g_rst_n
5	TESTSEL	R/W	0h	Test Mode Select Bit: This bit selects if a dummy delay is added in Oscillator Calibration mode to help reducing frequency when small delays are used: Reset Source: ottocal_rst_mod_g_rst_n
4	CALSTS	R	0h	Calibration Status Bit: This bit, when set to 1, indicates that calibration is in progress. It is set to 0 when: Reset Source: ottocal_rst_mod_g_rst_n
3	CNTSEL	R/W	0h	Counter Select Bit: Functionality of this bit has changed. When HRCNT0 or HRCNT1 reaches 0xFFFF, both counters are frozen. This bit will have an effect on when calibration starts: Reset Source: ottocal_rst_mod_g_rst_n
2	CALSTART	R/W	0h	Calibration Start/Stop Bit: Reset Source: ottocal_rst_mod_g_rst_n
1:0	CALMODE	R/W	0h	Note: CALMODE bits in HRPWM Module. Not used here. Reset Source: ottocal_rst_mod_g_rst_n

3.17.2 MEM_HRCAL Registers

3.17.2.1 MEM_HRCAL Register (Offset = 44h) [reset = 0h]

Short Description: HRPWM Calibration Registe

Long Description: HRPWM Calibration Register

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Table 3-1905. Instance Table

Instance Name	Physical Address
OTTOCAL0	502E 0044h
OTTOCAL1	502E 1044h
OTTOCAL2	502E 2044h
OTTOCAL3	502E 3044h

Figure 3-886. HRCAL Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
HRCAL							
R/W							
0h							

Access Types Legend

Table 3-1906. HRCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED_1	R	0h	Reserved Reset Source: ottocal_rst_mod_g_rst_n
7:0	HRCAL	R/W	0h	These 8-bits are used to select the number of delay elements during oscillator calibration for the calibration delay line [DCAL] only. The user configures the desired delay and then initiates a calibration run. Based on the calibration run result, the delay is increased/decreased for the next calibration run. Reset Source: ottocal_rst_mod_g_rst_n

3.17.3 MEM_HRPRD Registers

3.17.3.1 MEM_HRPRD Register (Offset = 46h) [reset = 0h]

Short Description: HRPWM Period Register

Long Description: HRPWM Period Register

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Table 3-1907. Instance Table

Instance Name	Physical Address
OTTOCAL0	502E 0046h
OTTOCAL1	502E 1046h
OTTOCAL2	502E 2046h
OTTOCAL3	502E 3046h

Figure 3-887. HRPRD Name Register

15	14	13	12	11	10	9	8
HRPRD							
R/W							
0h							
7	6	5	4	3	2	1	0
HRPRD							
R/W							
0h							

Access Types Legend

Table 3-1908. HRPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	HRPRD	R/W	0h	These 8-bits are used to select the number of delay elements during oscillator calibration for the calibration delay line [DCAL] only. Reset Source: ottocal_rst_mod_g_rst_n

3.17.4 MEM_HRCNT0 Registers

3.17.4.1 MEM_HRCNT0 Register (Offset = 48h) [reset = 0h]

Short Description: HRPWM Counter 0 Register

Long Description: HRPWM Counter 0 Register

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Table 3-1909. Instance Table

Instance Name	Physical Address
OTTOCAL0	502E 0048h
OTTOCAL1	502E 1048h
OTTOCAL2	502E 2048h
OTTOCAL3	502E 3048h

Figure 3-888. HRCNT0 Name Register

15	14	13	12	11	10	9	8
HRCNT0							
R/W							
0h							
7	6	5	4	3	2	1	0
HRCNT0							
R/W							
0h							

Access Types Legend

Table 3-1910. HRCNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	HRCNT0	R/W	0h	The HRCNT0 counter increments on every ring oscillator clock pulse. Reset Source: ottocal_rst_mod_g_rst_n

3.17.5 MEM_HRCNT1 Registers

3.17.5.1 MEM_HRCNT1 Register (Offset = 4Ah) [reset = 0h]

Short Description: HRPWM Counter 1 Register

Long Description: HRPWM Counter 1 Register

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Table 3-1911. Instance Table

Instance Name	Physical Address
OTTOCAL0	502E 004Ah
OTTOCAL1	502E 104Ah
OTTOCAL2	502E 204Ah
OTTOCAL3	502E 304Ah

Figure 3-889. HRCNT1 Name Register

15	14	13	12	11	10	9	8
HRCNT1							
R/W							
0h							
7	6	5	4	3	2	1	0
HRCNT1							
R/W							
0h							

Access Types Legend

Table 3-1912. HRCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	HRCNT1	R/W	0h	The HRCNT1 counter increments on every system clock pulse. Reset Source: ottocal_rst_mod_g_rst_n

3.17.6 MEM_HRMSTEP Registers

3.17.6.1 MEM_HRMSTEP Register (Offset = 4Ch) [reset = 0h]

Short Description: HRPWM MEP Step Register

Long Description: HRPWM MEP Step Register This register is only accessible on EPWM modules with HRPWM capabilities. Only 16 bit accesses are allowed for this register. Debugger access in 32 bit mode may display incorrect values.

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Table 3-1913. Instance Table

Instance Name	Physical Address
OTTOCAL0	502E 004Ch
OTTOCAL1	502E 104Ch
OTTOCAL2	502E 204Ch
OTTOCAL3	502E 304Ch

Figure 3-890. HRMSTEP Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
HRMSTEP							
R/W							
0h							

Access Types Legend

Table 3-1914. HRMSTEP Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED_1	R	0h	Reserved Reset Source: ottocal_rst_mod_g_rst_n
7:0	HRMSTEP	R/W	0h	High Resolution MEP Step When auto-conversion is enabled [HRCNFG[AUTOCONV] = 1], This 8-bit field contains the MEP_ScaleFactor [number of MEP steps per coarse steps] used by the hardware to automatically convert the value in the CMPAHR, CMPBHR, DBFEDHR, DBREDHR , TBPHSHR, or TBPRDHR register to a scaled micro-edge delay on the high-resolution ePWM output. The value in this register is written by the SFO calibration software at the end of each calibration run. Reset Source: ottocal_rst_mod_g_rst_n

3.17.7 Access Table

Table 3-1915. Access Type Codes

Access Type	Code	Description
R/W	R/W	Read / Write
R	R	Read

3.18 OUTPUTXBAR Registers

Table 3-1916. CFG0, CFG0 Registers, Base Address=0X00000000502D8000, Length=2048

Offset	Length	Register Name	outputxbar_mmr0 Physical Address
0h	32	PID	502D 8000h
10h	32	OUTPUTXBar_Status	502D 8010h
14h	32	OUTPUTXBar_FlagInvert	502D 8014h
18h	32	OUTPUTXBar_Flag	502D 8018h
1Ch	32	OUTPUTXBar_Flag_CLR	502D 801Ch
20h	32	OUTPUTXBar_FlagForce	502D 8020h
24h	32	OUTPUTXBar_OutLatch	502D 8024h
28h	32	OUTPUTXBar_OutStretch	502D 8028h
2Ch	32	OUTPUTXBar_OutLength	502D 802Ch
30h	32	OUTPUTXBar_OutInvert	502D 8030h
100h	32	OUTPUTXBar0_G0	502D 8100h
104h	32	OUTPUTXBar0_G1	502D 8104h
108h	32	OUTPUTXBar0_G2	502D 8108h
10Ch	32	OUTPUTXBar0_G3	502D 810Ch
110h	32	OUTPUTXBar0_G4	502D 8110h
114h	32	OUTPUTXBar0_G5	502D 8114h
118h	32	OUTPUTXBar0_G6	502D 8118h
11Ch	32	OUTPUTXBar0_G7	502D 811Ch
120h	32	OUTPUTXBar0_G8	502D 8120h
124h	32	OUTPUTXBar0_G9	502D 8124h
128h	32	OUTPUTXBar0_G10	502D 8128h
140h	32	OUTPUTXBar1_G0	502D 8140h
144h	32	OUTPUTXBar1_G1	502D 8144h
148h	32	OUTPUTXBar1_G2	502D 8148h
14Ch	32	OUTPUTXBar1_G3	502D 814Ch
150h	32	OUTPUTXBar1_G4	502D 8150h
154h	32	OUTPUTXBar1_G5	502D 8154h
158h	32	OUTPUTXBar1_G6	502D 8158h
15Ch	32	OUTPUTXBar1_G7	502D 815Ch
160h	32	OUTPUTXBar1_G8	502D 8160h
164h	32	OUTPUTXBar1_G9	502D 8164h
168h	32	OUTPUTXBar1_G10	502D 8168h
180h	32	OUTPUTXBar2_G0	502D 8180h
184h	32	OUTPUTXBar2_G1	502D 8184h
188h	32	OUTPUTXBar2_G2	502D 8188h
18Ch	32	OUTPUTXBar2_G3	502D 818Ch
190h	32	OUTPUTXBar2_G4	502D 8190h
194h	32	OUTPUTXBar2_G5	502D 8194h
198h	32	OUTPUTXBar2_G6	502D 8198h
19Ch	32	OUTPUTXBar2_G7	502D 819Ch
1A0h	32	OUTPUTXBar2_G8	502D 81A0h
1A4h	32	OUTPUTXBar2_G9	502D 81A4h
1A8h	32	OUTPUTXBar2_G10	502D 81A8h
1C0h	32	OUTPUTXBar3_G0	502D 81C0h
1C4h	32	OUTPUTXBar3_G1	502D 81C4h

Table 3-1916. CFG0, CFG0 Registers, Base Address=0X00000000502D8000, Length=2048 (continued)

Offset	Length	Register Name	outputxbar_mmr0 Physical Address
1C8h	32	OUTPUTXBar3_G2	502D 81C8h
1CCh	32	OUTPUTXBar3_G3	502D 81CCh
1D0h	32	OUTPUTXBar3_G4	502D 81D0h
1D4h	32	OUTPUTXBar3_G5	502D 81D4h
1D8h	32	OUTPUTXBar3_G6	502D 81D8h
1DCh	32	OUTPUTXBar3_G7	502D 81DCh
1E0h	32	OUTPUTXBar3_G8	502D 81E0h
1E4h	32	OUTPUTXBar3_G9	502D 81E4h
1E8h	32	OUTPUTXBar3_G10	502D 81E8h
200h	32	OUTPUTXBar4_G0	502D 8200h
204h	32	OUTPUTXBar4_G1	502D 8204h
208h	32	OUTPUTXBar4_G2	502D 8208h
20Ch	32	OUTPUTXBar4_G3	502D 820Ch
210h	32	OUTPUTXBar4_G4	502D 8210h
214h	32	OUTPUTXBar4_G5	502D 8214h
218h	32	OUTPUTXBar4_G6	502D 8218h
21Ch	32	OUTPUTXBar4_G7	502D 821Ch
220h	32	OUTPUTXBar4_G8	502D 8220h
224h	32	OUTPUTXBar4_G9	502D 8224h
228h	32	OUTPUTXBar4_G10	502D 8228h
240h	32	OUTPUTXBar5_G0	502D 8240h
244h	32	OUTPUTXBar5_G1	502D 8244h
248h	32	OUTPUTXBar5_G2	502D 8248h
24Ch	32	OUTPUTXBar5_G3	502D 824Ch
250h	32	OUTPUTXBar5_G4	502D 8250h
254h	32	OUTPUTXBar5_G5	502D 8254h
258h	32	OUTPUTXBar5_G6	502D 8258h
25Ch	32	OUTPUTXBar5_G7	502D 825Ch
260h	32	OUTPUTXBar5_G8	502D 8260h
264h	32	OUTPUTXBar5_G9	502D 8264h
268h	32	OUTPUTXBar5_G10	502D 8268h
280h	32	OUTPUTXBar6_G0	502D 8280h
284h	32	OUTPUTXBar6_G1	502D 8284h
288h	32	OUTPUTXBar6_G2	502D 8288h
28Ch	32	OUTPUTXBar6_G3	502D 828Ch
290h	32	OUTPUTXBar6_G4	502D 8290h
294h	32	OUTPUTXBar6_G5	502D 8294h
298h	32	OUTPUTXBar6_G6	502D 8298h
29Ch	32	OUTPUTXBar6_G7	502D 829Ch
2A0h	32	OUTPUTXBar6_G8	502D 82A0h
2A4h	32	OUTPUTXBar6_G9	502D 82A4h
2A8h	32	OUTPUTXBar6_G10	502D 82A8h
2C0h	32	OUTPUTXBar7_G0	502D 82C0h
2C4h	32	OUTPUTXBar7_G1	502D 82C4h
2C8h	32	OUTPUTXBar7_G2	502D 82C8h
2CCh	32	OUTPUTXBar7_G3	502D 82CCh
2D0h	32	OUTPUTXBar7_G4	502D 82D0h

Table 3-1916. CFG0, CFG0 Registers, Base Address=0X00000000502D8000, Length=2048 (continued)

Offset	Length	Register Name	outputxbar_mmr0 Physical Address
2D4h	32	OUTPUTXBar7_G5	502D 82D4h
2D8h	32	OUTPUTXBar7_G6	502D 82D8h
2DCh	32	OUTPUTXBar7_G7	502D 82DCh
2E0h	32	OUTPUTXBar7_G8	502D 82E0h
2E4h	32	OUTPUTXBar7_G9	502D 82E4h
2E8h	32	OUTPUTXBar7_G10	502D 82E8h
300h	32	OUTPUTXBar8_G0	502D 8300h
304h	32	OUTPUTXBar8_G1	502D 8304h
308h	32	OUTPUTXBar8_G2	502D 8308h
30Ch	32	OUTPUTXBar8_G3	502D 830Ch
310h	32	OUTPUTXBar8_G4	502D 8310h
314h	32	OUTPUTXBar8_G5	502D 8314h
318h	32	OUTPUTXBar8_G6	502D 8318h
31Ch	32	OUTPUTXBar8_G7	502D 831Ch
320h	32	OUTPUTXBar8_G8	502D 8320h
324h	32	OUTPUTXBar8_G9	502D 8324h
328h	32	OUTPUTXBar8_G10	502D 8328h
340h	32	OUTPUTXBar9_G0	502D 8340h
344h	32	OUTPUTXBar9_G1	502D 8344h
348h	32	OUTPUTXBar9_G2	502D 8348h
34Ch	32	OUTPUTXBar9_G3	502D 834Ch
350h	32	OUTPUTXBar9_G4	502D 8350h
354h	32	OUTPUTXBar9_G5	502D 8354h
358h	32	OUTPUTXBar9_G6	502D 8358h
35Ch	32	OUTPUTXBar9_G7	502D 835Ch
360h	32	OUTPUTXBar9_G8	502D 8360h
364h	32	OUTPUTXBar9_G9	502D 8364h
368h	32	OUTPUTXBar9_G10	502D 8368h
380h	32	OUTPUTXBar10_G0	502D 8380h
384h	32	OUTPUTXBar10_G1	502D 8384h
388h	32	OUTPUTXBar10_G2	502D 8388h
38Ch	32	OUTPUTXBar10_G3	502D 838Ch
390h	32	OUTPUTXBar10_G4	502D 8390h
394h	32	OUTPUTXBar10_G5	502D 8394h
398h	32	OUTPUTXBar10_G6	502D 8398h
39Ch	32	OUTPUTXBar10_G7	502D 839Ch
3A0h	32	OUTPUTXBar10_G8	502D 83A0h
3A4h	32	OUTPUTXBar10_G9	502D 83A4h
3A8h	32	OUTPUTXBar10_G10	502D 83A8h
3C0h	32	OUTPUTXBar11_G0	502D 83C0h
3C4h	32	OUTPUTXBar11_G1	502D 83C4h
3C8h	32	OUTPUTXBar11_G2	502D 83C8h
3CCh	32	OUTPUTXBar11_G3	502D 83CCh
3D0h	32	OUTPUTXBar11_G4	502D 83D0h
3D4h	32	OUTPUTXBar11_G5	502D 83D4h
3D8h	32	OUTPUTXBar11_G6	502D 83D8h
3DCh	32	OUTPUTXBar11_G7	502D 83DCh

Table 3-1916. CFG0, CFG0 Registers, Base Address=0X00000000502D8000, Length=2048 (continued)

Offset	Length	Register Name	outputxbar_mmr0 Physical Address
3E0h	32	OUTPUTXBar11_G8	502D 83E0h
3E4h	32	OUTPUTXBar11_G9	502D 83E4h
3E8h	32	OUTPUTXBar11_G10	502D 83E8h
400h	32	OUTPUTXBar12_G0	502D 8400h
404h	32	OUTPUTXBar12_G1	502D 8404h
408h	32	OUTPUTXBar12_G2	502D 8408h
40Ch	32	OUTPUTXBar12_G3	502D 840Ch
410h	32	OUTPUTXBar12_G4	502D 8410h
414h	32	OUTPUTXBar12_G5	502D 8414h
418h	32	OUTPUTXBar12_G6	502D 8418h
41Ch	32	OUTPUTXBar12_G7	502D 841Ch
420h	32	OUTPUTXBar12_G8	502D 8420h
424h	32	OUTPUTXBar12_G9	502D 8424h
428h	32	OUTPUTXBar12_G10	502D 8428h
440h	32	OUTPUTXBar13_G0	502D 8440h
444h	32	OUTPUTXBar13_G1	502D 8444h
448h	32	OUTPUTXBar13_G2	502D 8448h
44Ch	32	OUTPUTXBar13_G3	502D 844Ch
450h	32	OUTPUTXBar13_G4	502D 8450h
454h	32	OUTPUTXBar13_G5	502D 8454h
458h	32	OUTPUTXBar13_G6	502D 8458h
45Ch	32	OUTPUTXBar13_G7	502D 845Ch
460h	32	OUTPUTXBar13_G8	502D 8460h
464h	32	OUTPUTXBar13_G9	502D 8464h
468h	32	OUTPUTXBar13_G10	502D 8468h
480h	32	OUTPUTXBar14_G0	502D 8480h
484h	32	OUTPUTXBar14_G1	502D 8484h
488h	32	OUTPUTXBar14_G2	502D 8488h
48Ch	32	OUTPUTXBar14_G3	502D 848Ch
490h	32	OUTPUTXBar14_G4	502D 8490h
494h	32	OUTPUTXBar14_G5	502D 8494h
498h	32	OUTPUTXBar14_G6	502D 8498h
49Ch	32	OUTPUTXBar14_G7	502D 849Ch
4A0h	32	OUTPUTXBar14_G8	502D 84A0h
4A4h	32	OUTPUTXBar14_G9	502D 84A4h
4A8h	32	OUTPUTXBar14_G10	502D 84A8h
4C0h	32	OUTPUTXBar15_G0	502D 84C0h
4C4h	32	OUTPUTXBar15_G1	502D 84C4h
4C8h	32	OUTPUTXBar15_G2	502D 84C8h
4CCh	32	OUTPUTXBar15_G3	502D 84CCh
4D0h	32	OUTPUTXBar15_G4	502D 84D0h
4D4h	32	OUTPUTXBar15_G5	502D 84D4h
4D8h	32	OUTPUTXBar15_G6	502D 84D8h
4DCh	32	OUTPUTXBar15_G7	502D 84DCh
4E0h	32	OUTPUTXBar15_G8	502D 84E0h
4E4h	32	OUTPUTXBar15_G9	502D 84E4h

Table 3-1916. CFG0, CFG0 Registers, Base Address=0X00000000502D8000, Length=2048 (continued)

Offset	Length	Register Name	outputxbar_mmr0 Physical Address
4E8h	32	OUTPUTXBar15_G10	502D 84E8h

3.18.1 CFG0_PID Registers

3.18.1.1 CFG0_PID Register (Offset = 0h) [reset = 61800215h]

Short Description: PID register

Long Description: PID register

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Table 3-1917. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8000h

Figure 3-891. PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PID_MSB16															
R															
6180h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_MISC					PID_MAJOR			PID_CUSTOM		PID_MINOR					
R					R			R		R					
0h					2h			0h		15h					

Access Types Legend

Table 3-1918. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR	R	15h	Reset Source: mod_g_rst_n

3.18.2 CFG0_OUTPUTXBAR_STATUS Registers

3.18.2.1 CFG0_STATUS Register (Offset = 10h) [reset = 0h]

Short Description:

Long Description:

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Table 3-1919. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8010h

Figure 3-892. OUTPUTXBAR_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR_STATUS_STS															
R															
0h															

Access Types Legend

Table 3-1920. OUTPUTXBAR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	OUTPUTXBAR_STATUS_STS	R	0h	Status Reset Source: mod_g_rst_n

3.18.3 CFG0_OUTPUTXBAR_FLAGINVERT Registers

3.18.3.1 CFG0_FLAGINVERT Register (Offset = 14h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1921. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8014h

Figure 3-893. OUTPUTXBAR_FLAGINVERT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR_FLAGINVERT_INVERT															
R/W															
0h															

Access Types Legend

Table 3-1922. OUTPUTXBAR_FLAGINVERT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	OUTPUTXBAR_FLAGINVERT_INVERT	R/W	0h	FlagInvert Reset Source: mod_g_rst_n

3.18.4 CFG0_OUTPUTXBAR_FLAG Registers

3.18.4.1 CFG0_FLAG Register (Offset = 18h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1923. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8018h

Figure 3-894. OUTPUTXBAR_FLAG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR_FLAG_BIT 15	OUTPUTXBAR_FLAG_BIT 14	OUTPUTXBAR_FLAG_BIT 13	OUTPUTXBAR_FLAG_BIT 12	OUTPUTXBAR_FLAG_BIT 11	OUTPUTXBAR_FLAG_BIT 10	OUTPUTXBAR_FLAG_BIT 9	OUTPUTXBAR_FLAG_BIT 8	OUTPUTXBAR_FLAG_BIT 7	OUTPUTXBAR_FLAG_BIT 6	OUTPUTXBAR_FLAG_BIT 5	OUTPUTXBAR_FLAG_BIT 4	OUTPUTXBAR_FLAG_BIT 3	OUTPUTXBAR_FLAG_BIT 2	OUTPUTXBAR_FLAG_BIT 1	OUTPUTXBAR_FLAG_BIT 0
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 3-1924. OUTPUTXBAR_FLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15	OUTPUTXBAR_FLAG_BIT15	R/W1TC	0h	output xbar flag Reset Source: outputxbar_flag_clr_n_15
14	OUTPUTXBAR_FLAG_BIT14	R/W1TC	0h	output xbar flag Reset Source: outputxbar_flag_clr_n_14
13	OUTPUTXBAR_FLAG_BIT13	R/W1TC	0h	output xbar flag Reset Source: outputxbar_flag_clr_n_13
12	OUTPUTXBAR_FLAG_BIT12	R/W1TC	0h	output xbar flag Reset Source: outputxbar_flag_clr_n_12
11	OUTPUTXBAR_FLAG_BIT11	R/W1TC	0h	output xbar flag Reset Source: outputxbar_flag_clr_n_11
10	OUTPUTXBAR_FLAG_BIT10	R/W1TC	0h	output xbar flag Reset Source: outputxbar_flag_clr_n_10
9	OUTPUTXBAR_FLAG_BIT9	R/W1TC	0h	output xbar flag Reset Source: outputxbar_flag_clr_n_9
8	OUTPUTXBAR_FLAG_BIT8	R/W1TC	0h	output xbar flag Reset Source: outputxbar_flag_clr_n_8
7	OUTPUTXBAR_FLAG_BIT7	R/W1TC	0h	output xbar flag Reset Source: outputxbar_flag_clr_n_7
6	OUTPUTXBAR_FLAG_BIT6	R/W1TC	0h	output xbar flag Reset Source: outputxbar_flag_clr_n_6
5	OUTPUTXBAR_FLAG_BIT5	R/W1TC	0h	output xbar flag Reset Source: outputxbar_flag_clr_n_5
4	OUTPUTXBAR_FLAG_BIT4	R/W1TC	0h	output xbar flag Reset Source: outputxbar_flag_clr_n_4

Table 3-1924. OUTPUTXBAR_FLAG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	OUTPUTXBAR_FLAG_BIT3	R/W1TC	0h	output xbar flag Reset Source: outputxbar_flag_clr_n_3
2	OUTPUTXBAR_FLAG_BIT2	R/W1TC	0h	output xbar flag Reset Source: outputxbar_flag_clr_n_2
1	OUTPUTXBAR_FLAG_BIT1	R/W1TC	0h	output xbar flag Reset Source: outputxbar_flag_clr_n_1
0	OUTPUTXBAR_FLAG_BIT0	R/W1TC	0h	output xbar flag Reset Source: outputxbar_flag_clr_n_0

3.18.5 CFG0_OUTPUTXBAR_FLAG_CLR Registers

3.18.5.1 CFG0_FLAG_CLR Register (Offset = 1Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1925. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 801Ch

Figure 3-895. OUTPUTXBAR_FLAG_CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR_FLAG_CLR_BIT15	OUTPUTXBAR_FLAG_CLR_BIT14	OUTPUTXBAR_FLAG_CLR_BIT13	OUTPUTXBAR_FLAG_CLR_BIT12	OUTPUTXBAR_FLAG_CLR_BIT11	OUTPUTXBAR_FLAG_CLR_BIT10	OUTPUTXBAR_FLAG_CLR_BIT9	OUTPUTXBAR_FLAG_CLR_BIT8	OUTPUTXBAR_FLAG_CLR_BIT7	OUTPUTXBAR_FLAG_CLR_BIT6	OUTPUTXBAR_FLAG_CLR_BIT5	OUTPUTXBAR_FLAG_CLR_BIT4	OUTPUTXBAR_FLAG_CLR_BIT3	OUTPUTXBAR_FLAG_CLR_BIT2	OUTPUTXBAR_FLAG_CLR_BIT1	OUTPUTXBAR_FLAG_CLR_BIT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 3-1926. OUTPUTXBAR_FLAG_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15	OUTPUTXBAR_FLAG_CLR_BIT15	R/W	0h	output xbar flag clear Reset Source: mod_g_rst_n
14	OUTPUTXBAR_FLAG_CLR_BIT14	R/W	0h	output xbar flag clear Reset Source: mod_g_rst_n
13	OUTPUTXBAR_FLAG_CLR_BIT13	R/W	0h	output xbar flag clear Reset Source: mod_g_rst_n
12	OUTPUTXBAR_FLAG_CLR_BIT12	R/W	0h	output xbar flag clear Reset Source: mod_g_rst_n
11	OUTPUTXBAR_FLAG_CLR_BIT11	R/W	0h	output xbar flag clear Reset Source: mod_g_rst_n
10	OUTPUTXBAR_FLAG_CLR_BIT10	R/W	0h	output xbar flag clear Reset Source: mod_g_rst_n
9	OUTPUTXBAR_FLAG_CLR_BIT9	R/W	0h	output xbar flag clear Reset Source: mod_g_rst_n
8	OUTPUTXBAR_FLAG_CLR_BIT8	R/W	0h	output xbar flag clear Reset Source: mod_g_rst_n
7	OUTPUTXBAR_FLAG_CLR_BIT7	R/W	0h	output xbar flag clear Reset Source: mod_g_rst_n
6	OUTPUTXBAR_FLAG_CLR_BIT6	R/W	0h	output xbar flag clear Reset Source: mod_g_rst_n
5	OUTPUTXBAR_FLAG_CLR_BIT5	R/W	0h	output xbar flag clear Reset Source: mod_g_rst_n
4	OUTPUTXBAR_FLAG_CLR_BIT4	R/W	0h	output xbar flag clear Reset Source: mod_g_rst_n

Table 3-1926. OUTPUTXBAR_FLAG_CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	OUTPUTXBAR_FLAG_CLR_BIT3	R/W	0h	output xbar flag clear Reset Source: mod_g_rst_n
2	OUTPUTXBAR_FLAG_CLR_BIT2	R/W	0h	output xbar flag clear Reset Source: mod_g_rst_n
1	OUTPUTXBAR_FLAG_CLR_BIT1	R/W	0h	output xbar flag clear Reset Source: mod_g_rst_n
0	OUTPUTXBAR_FLAG_CLR_BIT0	R/W	0h	output xbar flag clear Reset Source: mod_g_rst_n

3.18.6 CFG0_OUTPUTXBAR_FLAGFORCE Registers

3.18.6.1 CFG0_FLAGFORCE Register (Offset = 20h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1927. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8020h

Figure 3-896. OUTPUTXBAR_FLAGFORCE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR_FLAGFORCE_FRC															
R/W															
0h															

Access Types Legend

Table 3-1928. OUTPUTXBAR_FLAGFORCE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	OUTPUTXBAR_FLAGFORCE_FRC	R/W	0h	FlagForce Reset Source: mod_g_rst_n

3.18.7 CFG0_OUTPUTXBAR_OUTLATCH Registers

3.18.7.1 CFG0_OUTLATCH Register (Offset = 24h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1929. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8024h

Figure 3-897. OUTPUTXBAR_OUTLATCH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR_OUTLATCH_LATCHSEL															
R/W															
0h															

Access Types Legend

Table 3-1930. OUTPUTXBAR_OUTLATCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	OUTPUTXBAR_OUTLATCH_LATCHSEL	R/W	0h	OutLatch Reset Source: mod_g_rst_n

3.18.8 CFG0_OUTPUTXBAR_OUTSTRETCH Registers

3.18.8.1 CFG0_OUTSTRETCH Register (Offset = 28h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1931. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8028h

Figure 3-898. OUTPUTXBAR_OUTSTRETCH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR_OUTSTRETCH_STRETCHSEL															
R/W															
0h															

Access Types Legend

Table 3-1932. OUTPUTXBAR_OUTSTRETCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	OUTPUTXBAR_OUTSTRETCH_STRETCHSEL	R/W	0h	OutStretch Reset Source: mod_g_rst_n

3.18.9 CFG0_OUTPUTXBAR_OUTLENGTH Registers

3.18.9.1 CFG0_OUTLENGTH Register (Offset = 2Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1933. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 802Ch

Figure 3-899. OUTPUTXBAR_OUTLENGTH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR_OUTLENGTH_LENGTHSEL															
R/W															
0h															

Access Types Legend

Table 3-1934. OUTPUTXBAR_OUTLENGTH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	OUTPUTXBAR_OUTLENGTH_LENGTHSEL	R/W	0h	OutLength Reset Source: mod_g_rst_n

3.18.10 CFG0_OUTPUTXBAR_OUTINVERT Registers

3.18.10.1 CFG0_OUTINVERT Register (Offset = 30h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1935. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8030h

Figure 3-900. OUTPUTXBAR_OUTINVERT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR_OUTINVERT_OUTINVERT															
R/W															
0h															

Access Types Legend

Table 3-1936. OUTPUTXBAR_OUTINVERT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	OUTPUTXBAR_OUTINVERT_OUTINVERT	R/W	0h	OutInvert Reset Source: mod_g_rst_n

3.18.11 CFG0_OUTPUTXBAR0_G0 Registers

3.18.11.1 CFG0_G0 Register (Offset = 100h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1937. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8100h

Figure 3-901. OUTPUTXBAR0_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR0_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR0_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1938. OUTPUTXBAR0_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR0_G0_SEL	R/W	0h	G0: PWM XBar0 G0 input bit select. Input source is PWM[x].TRIPOUT 1: PWM[x] TRIPOUT selected 0: PWM[x] TRIPOUT is de-selected Reset Source: mod_g_rst_n

3.18.12 CFG0_OUTPUTXBAR0_G1 Registers

3.18.12.1 CFG0_G1 Register (Offset = 104h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1939. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8104h

Figure 3-902. OUTPUTXBAR0_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR0_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR0_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1940. OUTPUTXBAR0_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR0_G1_SEL	R/W	0h	G1: OUTPUT XBar0 G1 input bit select. Input source is PWM[x].SOCA 1: PWM[x] SOCA selected 0: PWM[x] SOCA is de-selected Reset Source: mod_g_rst_n

3.18.13 CFG0_OUTPUTXBAR0_G2 Registers

3.18.13.1 CFG0_G2 Register (Offset = 108h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1941. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8108h

Figure 3-903. OUTPUTXBAR0_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR0_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR0_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1942. OUTPUTXBAR0_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR0_G2_SEL	R/W	0h	G2: OUTPUT XBar0 G2 input bit select. Input source is PWM[x].SOCB 1: PWM[x] SOCB selected 0: PWM[x] SOCB is de-selected Reset Source: mod_g_rst_n

3.18.14 CFG0_OUTPUTXBAR0_G3 Registers

3.18.14.1 CFG0_G3 Register (Offset = 10Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1943. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 810Ch

Figure 3-904. OUTPUTXBAR0_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR0_G3_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR0_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-1944. OUTPUTXBAR0_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR0_G3_SEL	R/W	0h	G3: OUTPUT XBar0 G3 input bit select. Input source is DEL[x].ACTIVE 1: DEL[x] ACTIVE selected 0: DEL[x] ACTIVE is de-selected Reset Source: mod_g_rst_n

3.18.15 CFG0_OUTPUTXBAR0_G4 Registers

3.18.15.1 CFG0_G4 Register (Offset = 110h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1945. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8110h

Figure 3-905. OUTPUTXBAR0_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR0_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR0_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-1946. OUTPUTXBAR0_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR0_G4_SEL	R/W	0h	G4: OUTPUT XBar0 G4 input bit select. Input source is DEL[x].TRIP 1: DEL[x] TRIP selected 0: DEL[x] TRIP is de-selected Reset Source: mod_g_rst_n

3.18.16 CFG0_OUTPUTXBAR0_G5 Registers

3.18.16.1 CFG0_G5 Register (Offset = 114h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1947. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8114h

Figure 3-906. OUTPUTXBAR0_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								OUTPUTXBAR0_G5_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR0_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-1948. OUTPUTXBAR0_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	OUTPUTXBAR0_G5_SEL	R/W	0h	G5: OUTPUT XBar0 G5 input bit select. 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.18.17 CFG0_OUTPUTXBAR0_G6 Registers

3.18.17.1 CFG0_G6 Register (Offset = 118h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1949. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8118h

Figure 3-907. OUTPUTXBAR0_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR0_G6_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR0_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-1950. OUTPUTXBAR0_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR0_G6_SEL	R/W	0h	G6: OUTPUT XBar0 G6 Input Select 0: CMP12SS0.CTRIPOUTL 1: CMP12SS0.CTRIPOUTH 2: CMP12SS1.CTRIPOUTL 3: CMP12SS1.CTRIPOUTH 4: CMP12SS2.CTRIPOUTL 5: CMP12SS2.CTRIPOUTH 6: CMP12SS3.CTRIPOUTL 7: CMP12SS3.CTRIPOUTH 8: CMP12SS4.CTRIPOUTL 9: CMP12SS4.CTRIPOUTH 10: CMP12SS5.CTRIPOUTL 11: CMP12SS5.CTRIPOUTH 12: CMP12SS6.CTRIPOUTL 13: CMP12SS6.CTRIPOUTH 14: CMP12SS7.CTRIPOUTL 15: CMP12SS7.CTRIPOUTH 16: CMP12SS8.CTRIPOUTL 17: CMP12SS8.CTRIPOUTH 18: CMP12SS9.CTRIPOUTL 19: CMP12SS9.CTRIPOUTH Reset Source: mod_g_rst_n

3.18.18 CFG0_OUTPUTXBAR0_G7 Registers

3.18.18.1 CFG0_G7 Register (Offset = 11Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1951. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 811Ch

Figure 3-908. OUTPUTXBAR0_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR0_G7_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR0_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-1952. OUTPUTXBAR0_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR0_G7_SEL	R/W	0h	G7: OUTPUT XBar0 G7 Input Select 0: CMP8SS0.CTRIPOUTL 1: CMP8SS0.CTRIPOUTH 2: CMP8SS1.CTRIPOUTL 3: CMP8SS1.CTRIPOUTH 4: CMP8SS2.CTRIPOUTL 5: CMP8SS2.CTRIPOUTH 6: CMP8SS3.CTRIPOUTL 7: CMP8SS3.CTRIPOUTH 8: CMP8SS4.CTRIPOUTL 9: CMP8SS4.CTRIPOUTH 10: CMP8SS5.CTRIPOUTL 11: CMP8SS5.CTRIPOUTH 12: CMP8SS6.CTRIPOUTL 13: CMP8SS6.CTRIPOUTH 14: CMP8SS7.CTRIPOUTL 15: CMP8SS7.CTRIPOUTH 16: CMP8SS8.CTRIPOUTL 17: CMP8SS8.CTRIPOUTH 18: CMP8SS9.CTRIPOUTL 19: CMP8SS9.CTRIPOUTH Reset Source: mod_g_rst_n

3.18.19 CFG0_OUTPUTXBAR0_G8 Registers

3.18.19.1 CFG0_G8 Register (Offset = 120h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1953. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8120h

Figure 3-909. OUTPUTXBAR0_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR0_G8_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR0_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-1954. OUTPUTXBAR0_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR0_G8_SEL	R/W	0h	G8: OUTPUT XBar0 G8 Input Select 0: ADC0.EVT1 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1 EVT4 8: ADC2.EVT1 9: ADC2 EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.18.20 CFG0_OUTPUTXBAR0_G9 Registers

3.18.20.1 CFG0_G9 Register (Offset = 124h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1955. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8124h

Figure 3-910. OUTPUTXBAR0_G9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR0_G9_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR0_G9_SEL															
R/W															
0h															

Access Types Legend

Table 3-1956. OUTPUTXBAR0_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR0_G9_SEL	R/W	0h	G9: OUTPUT XBar0 G9 Input Select 0: PWMSyncOutXBar.SYNCOUT0 1: PWMSyncOutXBar.SYNCOUT1 2: PWMSyncOutXBar.SYNCOUT2 3: PWMSyncOutXBar.SYNCOUT3 4: EQEP0.I_OUT 5: EQEP0.S_OUT 6: EQEP1.I_OUT 7: EQEP1.S_OUT 8: EQEP2.I_OUT 9: EQEP2.S_OUT 10: ECAP0.OUT 11: ECAP1.OUT 12: ECAP2.OUT 13: ECAP3.OUT 14: ECAP4.OUT 15: ECAP5.OUT 16: ECAP6.OUT 17: ECAP7.OUT 18: ECAP8.OUT 19: ECAP9.OUT Reset Source: mod_g_rst_n

3.18.21 CFG0_OUTPUTXBAR0_G10 Registers

3.18.21.1 CFG0_G10 Register (Offset = 128h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1957. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8128h

Figure 3-911. OUTPUTXBAR0_G10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR0_G10_SEL															
R/W															
0h															

Access Types Legend

Table 3-1958. OUTPUTXBAR0_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	OUTPUTXBAR0_G10_SEL	R/W	0h	G10: OUTPUT XBar0 G10 Input Select 3:0: FSIRX0.RX_TRIG0 7:4: FSIRX1.RX_TRIG0 11:8: FSIRX2.RX_TRIG0 15:12: FSIRX3.RX_TRIG0 Reset Source: mod_g_rst_n

3.18.22 CFG0_OUTPUTXBAR1_G0 Registers

3.18.22.1 CFG0_G0 Register (Offset = 140h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1959. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8140h

Figure 3-912. OUTPUTXBAR1_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR1_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR1_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1960. OUTPUTXBAR1_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR1_G0_SEL	R/W	0h	G0: PWM XBar1 G0 input bit select. Input source is PWM[x].TRIPOUT 1: PWM[x] TRIPOUT selected 0: PWM[x] TRIPOUT is de-selected Reset Source: mod_g_rst_n

3.18.23 CFG0_OUTPUTXBAR1_G1 Registers

3.18.23.1 CFG0_G1 Register (Offset = 144h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1961. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8144h

Figure 3-913. OUTPUTXBAR1_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR1_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR1_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1962. OUTPUTXBAR1_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR1_G1_SEL	R/W	0h	G1: OUTPUT XBar1 G1 input bit select. Input source is PWM[x].SOCA 1: PWM[x] SOCA selected 0: PWM[x] SOCA is de-selected Reset Source: mod_g_rst_n

3.18.24 CFG0_OUTPUTXBAR1_G2 Registers

3.18.24.1 CFG0_G2 Register (Offset = 148h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1963. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8148h

Figure 3-914. OUTPUTXBAR1_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR1_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR1_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1964. OUTPUTXBAR1_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR1_G2_SEL	R/W	0h	G2: OUTPUT XBar1 G2 input bit select. Input source is PWM[x].SOCB 1: PWM[x] SOCB selected 0: PWM[x] SOCB is de-selected Reset Source: mod_g_rst_n

3.18.25 CFG0_OUTPUTXBAR1_G3 Registers

3.18.25.1 CFG0_G3 Register (Offset = 14Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1965. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 814Ch

Figure 3-915. OUTPUTXBAR1_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR1_G3_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR1_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-1966. OUTPUTXBAR1_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR1_G3_SEL	R/W	0h	G3: OUTPUT XBar1 G3 input bit select. Input source is DEL[x].ACTIVE 1: DEL[x] ACTIVE selected 0: DEL[x] ACTIVE is de-selected Reset Source: mod_g_rst_n

3.18.26 CFG0_OUTPUTXBAR1_G4 Registers

3.18.26.1 CFG0_G4 Register (Offset = 150h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1967. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8150h

Figure 3-916. OUTPUTXBAR1_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR1_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR1_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-1968. OUTPUTXBAR1_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR1_G4_SEL	R/W	0h	G4: OUTPUT XBar1 G4 input bit select. Input source is DEL[x].TRIP 1: DEL[x] TRIP selected 0: DEL[x] TRIP is de-selected Reset Source: mod_g_rst_n

3.18.27 CFG0_OUTPUTXBAR1_G5 Registers

3.18.27.1 CFG0_G5 Register (Offset = 154h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1969. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8154h

Figure 3-917. OUTPUTXBAR1_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								OUTPUTXBAR1_G5_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR1_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-1970. OUTPUTXBAR1_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	OUTPUTXBAR1_G5_SEL	R/W	0h	G5: OUTPUT XBar1 G5 input bit select. 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.18.28 CFG0_OUTPUTXBAR1_G6 Registers

3.18.28.1 CFG0_G6 Register (Offset = 158h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1971. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8158h

Figure 3-918. OUTPUTXBAR1_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR1_G6_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR1_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-1972. OUTPUTXBAR1_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR1_G6_SEL	R/W	0h	G6: OUTPUT XBar1 G6 Input Select 0: CMP12SS0.CTRIPOUTL 1: CMP12SS0.CTRIPOUTH 2: CMP12SS1.CTRIPOUTL 3: CMP12SS1.CTRIPOUTH 4: CMP12SS2.CTRIPOUTL 5: CMP12SS2.CTRIPOUTH 6: CMP12SS3.CTRIPOUTL 7: CMP12SS3.CTRIPOUTH 8: CMP12SS4.CTRIPOUTL 9: CMP12SS4.CTRIPOUTH 10: CMP12SS5.CTRIPOUTL 11: CMP12SS5.CTRIPOUTH 12: CMP12SS6.CTRIPOUTL 13: CMP12SS6.CTRIPOUTH 14: CMP12SS7.CTRIPOUTL 15: CMP12SS7.CTRIPOUTH 16: CMP12SS8.CTRIPOUTL 17: CMP12SS8.CTRIPOUTH 18: CMP12SS9.CTRIPOUTL 19: CMP12SS9.CTRIPOUTH Reset Source: mod_g_rst_n

3.18.29 CFG0_OUTPUTXBAR1_G7 Registers

3.18.29.1 CFG0_G7 Register (Offset = 15Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1973. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 815Ch

Figure 3-919. OUTPUTXBAR1_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR1_G7_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR1_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-1974. OUTPUTXBAR1_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR1_G7_SEL	R/W	0h	G7: OUTPUT XBar1 G7 Input Select 0: CMP8SS0.CTRIPOUTL 1: CMP8SS0.CTRIPOUTH 2: CMP8SS1.CTRIPOUTL 3: CMP8SS1.CTRIPOUTH 4: CMP8SS2.CTRIPOUTL 5: CMP8SS2.CTRIPOUTH 6: CMP8SS3.CTRIPOUTL 7: CMP8SS3.CTRIPOUTH 8: CMP8SS4.CTRIPOUTL 9: CMP8SS4.CTRIPOUTH 10: CMP8SS5.CTRIPOUTL 11: CMP8SS5.CTRIPOUTH 12: CMP8SS6.CTRIPOUTL 13: CMP8SS6.CTRIPOUTH 14: CMP8SS7.CTRIPOUTL 15: CMP8SS7.CTRIPOUTH 16: CMP8SS8.CTRIPOUTL 17: CMP8SS8.CTRIPOUTH 18: CMP8SS9.CTRIPOUTL 19: CMP8SS9.CTRIPOUTH Reset Source: mod_g_rst_n

3.18.30 CFG0_OUTPUTXBAR1_G8 Registers

3.18.30.1 CFG0_G8 Register (Offset = 160h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1975. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8160h

Figure 3-920. OUTPUTXBAR1_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR1_G8_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR1_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-1976. OUTPUTXBAR1_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR1_G8_SEL	R/W	0h	G8: OUTPUT XBar1 G8 Input Select 0: ADC0.EVT1 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1 EVT4 8: ADC2.EVT1 9: ADC2 EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.18.31 CFG0_OUTPUTXBAR1_G9 Registers

3.18.31.1 CFG0_G9 Register (Offset = 164h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1977. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8164h

Figure 3-921. OUTPUTXBAR1_G9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR1_G9_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR1_G9_SEL															
R/W															
0h															

Access Types Legend

Table 3-1978. OUTPUTXBAR1_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR1_G9_SEL	R/W	0h	G9: OUTPUT XBar1 G9 Input Select 0: PWMSyncOutXBar.SYNCOUT0 1: PWMSyncOutXBar.SYNCOUT1 2: PWMSyncOutXBar.SYNCOUT2 3: PWMSyncOutXBar.SYNCOUT3 4: EQEP0.I_OUT 5: EQEP0.S_OUT 6: EQEP1.I_OUT 7: EQEP1.S_OUT 8: EQEP2.I_OUT 9: EQEP2.S_OUT 10: ECAP0.OUT 11: ECAP1.OUT 12: ECAP2.OUT 13: ECAP3.OUT 14: ECAP4.OUT 15: ECAP5.OUT 16: ECAP6.OUT 17: ECAP7.OUT 18: ECAP8.OUT 19: ECAP9.OUT Reset Source: mod_g_rst_n

3.18.32 CFG0_OUTPUTXBAR1_G10 Registers

3.18.32.1 CFG0_G10 Register (Offset = 168h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1979. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8168h

Figure 3-922. OUTPUTXBAR1_G10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR1_G10_SEL															
R/W															
0h															

Access Types Legend

Table 3-1980. OUTPUTXBAR1_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	OUTPUTXBAR1_G10_SEL	R/W	0h	G10: OUTPUT XBar1 G10 Input Select 3:0: FSIRX0.RX_TRIG0 7:4: FSIRX1.RX_TRIG0 11:8: FSIRX2.RX_TRIG0 15:12: FSIRX3.RX_TRIG0 Reset Source: mod_g_rst_n

3.18.33 CFG0_OUTPUTXBAR2_G0 Registers

3.18.33.1 CFG0_G0 Register (Offset = 180h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1981. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8180h

Figure 3-923. OUTPUTXBAR2_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR2_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR2_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-1982. OUTPUTXBAR2_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR2_G0_SEL	R/W	0h	G0: PWM XBar2 G0 input bit select. Input source is PWM[x].TRIPOUT 1: PWM[x] TRIPOUT selected 0: PWM[x] TRIPOUT is de-selected Reset Source: mod_g_rst_n

3.18.34 CFG0_OUTPUTXBAR2_G1 Registers

3.18.34.1 CFG0_G1 Register (Offset = 184h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1983. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8184h

Figure 3-924. OUTPUTXBAR2_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR2_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR2_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-1984. OUTPUTXBAR2_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR2_G1_SEL	R/W	0h	G1: OUTPUT XBar2 G1 input bit select. Input source is PWM[x].SOCA 1: PWM[x] SOCA selected 0: PWM[x] SOCA is de-selected Reset Source: mod_g_rst_n

3.18.35 CFG0_OUTPUTXBAR2_G2 Registers

3.18.35.1 CFG0_G2 Register (Offset = 188h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1985. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8188h

Figure 3-925. OUTPUTXBAR2_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR2_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR2_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-1986. OUTPUTXBAR2_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR2_G2_SEL	R/W	0h	G2: OUTPUT XBar2 G2 input bit select. Input source is PWM[x].SOCB 1: PWM[x] SOCB selected 0: PWM[x] SOCB is de-selected Reset Source: mod_g_rst_n

3.18.36 CFG0_OUTPUTXBAR2_G3 Registers

3.18.36.1 CFG0_G3 Register (Offset = 18Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1987. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 818Ch

Figure 3-926. OUTPUTXBAR2_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR2_G3_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR2_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-1988. OUTPUTXBAR2_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR2_G3_SEL	R/W	0h	G3: OUTPUT XBar2 G3 input bit select. Input source is DEL[x].ACTIVE 1: DEL[x] ACTIVE selected 0: DEL[x] ACTIVE is de-selected Reset Source: mod_g_rst_n

3.18.37 CFG0_OUTPUTXBAR2_G4 Registers

3.18.37.1 CFG0_G4 Register (Offset = 190h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1989. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8190h

Figure 3-927. OUTPUTXBAR2_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR2_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR2_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-1990. OUTPUTXBAR2_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR2_G4_SEL	R/W	0h	G4: OUTPUT XBar2 G4 input bit select. Input source is DEL[x].TRIP 1: DEL[x] TRIP selected 0: DEL[x] TRIP is de-selected Reset Source: mod_g_rst_n

3.18.38 CFG0_OUTPUTXBAR2_G5 Registers

3.18.38.1 CFG0_G5 Register (Offset = 194h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1991. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8194h

Figure 3-928. OUTPUTXBAR2_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								OUTPUTXBAR2_G5_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR2_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-1992. OUTPUTXBAR2_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	OUTPUTXBAR2_G5_SEL	R/W	0h	G5: OUTPUT XBar2 G5 input bit select. 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.18.39 CFG0_OUTPUTXBAR2_G6 Registers

3.18.39.1 CFG0_G6 Register (Offset = 198h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1993. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8198h

Figure 3-929. OUTPUTXBAR2_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR2_G6_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR2_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-1994. OUTPUTXBAR2_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR2_G6_SEL	R/W	0h	G6: OUTPUT XBar2 G6 Input Select 0: CMP12SS0.CTRIPOUTL 1: CMP12SS0.CTRIPOUTH 2: CMP12SS1.CTRIPOUTL 3: CMP12SS1.CTRIPOUTH 4: CMP12SS2.CTRIPOUTL 5: CMP12SS2.CTRIPOUTH 6: CMP12SS3.CTRIPOUTL 7: CMP12SS3.CTRIPOUTH 8: CMP12SS4.CTRIPOUTL 9: CMP12SS4.CTRIPOUTH 10: CMP12SS5.CTRIPOUTL 11: CMP12SS5.CTRIPOUTH 12: CMP12SS6.CTRIPOUTL 13: CMP12SS6.CTRIPOUTH 14: CMP12SS7.CTRIPOUTL 15: CMP12SS7.CTRIPOUTH 16: CMP12SS8.CTRIPOUTL 17: CMP12SS8.CTRIPOUTH 18: CMP12SS9.CTRIPOUTL 19: CMP12SS9.CTRIPOUTH Reset Source: mod_g_rst_n

3.18.40 CFG0_OUTPUTXBAR2_G7 Registers

3.18.40.1 CFG0_G7 Register (Offset = 19Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1995. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 819Ch

Figure 3-930. OUTPUTXBAR2_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR2_G7_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR2_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-1996. OUTPUTXBAR2_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR2_G7_SEL	R/W	0h	G7: OUTPUT XBar2 G7 Input Select 0: CMP8SS0.CTRIPOUTL 1: CMP8SS0.CTRIPOUTH 2: CMP8SS1.CTRIPOUTL 3: CMP8SS1.CTRIPOUTH 4: CMP8SS2.CTRIPOUTL 5: CMP8SS2.CTRIPOUTH 6: CMP8SS3.CTRIPOUTL 7: CMP8SS3.CTRIPOUTH 8: CMP8SS4.CTRIPOUTL 9: CMP8SS4.CTRIPOUTH 10: CMP8SS5.CTRIPOUTL 11: CMP8SS5.CTRIPOUTH 12: CMP8SS6.CTRIPOUTL 13: CMP8SS6.CTRIPOUTH 14: CMP8SS7.CTRIPOUTL 15: CMP8SS7.CTRIPOUTH 16: CMP8SS8.CTRIPOUTL 17: CMP8SS8.CTRIPOUTH 18: CMP8SS9.CTRIPOUTL 19: CMP8SS9.CTRIPOUTH Reset Source: mod_g_rst_n

3.18.41 CFG0_OUTPUTXBAR2_G8 Registers

3.18.41.1 CFG0_G8 Register (Offset = 1A0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1997. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 81A0h

Figure 3-931. OUTPUTXBAR2_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR2_G8_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR2_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-1998. OUTPUTXBAR2_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR2_G8_SEL	R/W	0h	G8: OUTPUT XBar2 G8 Input Select 0: ADC0.EVT1 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1 EVT4 8: ADC2.EVT1 9: ADC2 EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.18.42 CFG0_OUTPUTXBAR2_G9 Registers

3.18.42.1 CFG0_G9 Register (Offset = 1A4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-1999. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 81A4h

Figure 3-932. OUTPUTXBAR2_G9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR2_G9_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR2_G9_SEL															
R/W															
0h															

Access Types Legend

Table 3-2000. OUTPUTXBAR2_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR2_G9_SEL	R/W	0h	G9: OUTPUT XBar2 G9 Input Select 0: PWMSyncOutXBar.SYNCOUT0 1: PWMSyncOutXBar.SYNCOUT1 2: PWMSyncOutXBar.SYNCOUT2 3: PWMSyncOutXBar.SYNCOUT3 4: EQEP0.I_OUT 5: EQEP0.S_OUT 6: EQEP1.I_OUT 7: EQEP1.S_OUT 8: EQEP2.I_OUT 9: EQEP2.S_OUT 10: ECAP0.OUT 11: ECAP1.OUT 12: ECAP2.OUT 13: ECAP3.OUT 14: ECAP4.OUT 15: ECAP5.OUT 16: ECAP6.OUT 17: ECAP7.OUT 18: ECAP8.OUT 19: ECAP9.OUT Reset Source: mod_g_rst_n

3.18.43 CFG0_OUTPUTXBAR2_G10 Registers

3.18.43.1 CFG0_G10 Register (Offset = 1A8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2001. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 81A8h

Figure 3-933. OUTPUTXBAR2_G10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR2_G10_SEL															
R/W															
0h															

Access Types Legend

Table 3-2002. OUTPUTXBAR2_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	OUTPUTXBAR2_G10_SEL	R/W	0h	G10: OUTPUT XBar2 G10 Input Select 3:0: FSIRX0.RX_TRIG0 7:4: FSIRX1.RX_TRIG0 11:8: FSIRX2.RX_TRIG0 15:12: FSIRX3.RX_TRIG0 Reset Source: mod_g_rst_n

3.18.44 CFG0_OUTPUTXBAR3_G0 Registers

3.18.44.1 CFG0_G0 Register (Offset = 1C0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2003. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 81C0h

Figure 3-934. OUTPUTXBAR3_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR3_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR3_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2004. OUTPUTXBAR3_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR3_G0_SEL	R/W	0h	G0: PWM XBar3 G0 input bit select. Input source is PWM[x].TRIPOUT 1: PWM[x] TRIPOUT selected 0: PWM[x] TRIPOUT is de-selected Reset Source: mod_g_rst_n

3.18.45 CFG0_OUTPUTXBAR3_G1 Registers

3.18.45.1 CFG0_G1 Register (Offset = 1C4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2005. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 81C4h

Figure 3-935. OUTPUTXBAR3_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR3_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR3_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2006. OUTPUTXBAR3_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR3_G1_SEL	R/W	0h	G1: OUTPUT XBar3 G1 input bit select. Input source is PWM[x].SOCA 1: PWM[x] SOCA selected 0: PWM[x] SOCA is de-selected Reset Source: mod_g_rst_n

3.18.46 CFG0_OUTPUTXBAR3_G2 Registers

3.18.46.1 CFG0_G2 Register (Offset = 1C8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2007. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 81C8h

Figure 3-936. OUTPUTXBAR3_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR3_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR3_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2008. OUTPUTXBAR3_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR3_G2_SEL	R/W	0h	G2: OUTPUT XBar3 G2 input bit select. Input source is PWM[x].SOCB 1: PWM[x] SOCB selected 0: PWM[x] SOCB is de-selected Reset Source: mod_g_rst_n

3.18.47 CFG0_OUTPUTXBAR3_G3 Registers

3.18.47.1 CFG0_G3 Register (Offset = 1CCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2009. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 81CCh

Figure 3-937. OUTPUTXBAR3_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR3_G3_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR3_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2010. OUTPUTXBAR3_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR3_G3_SEL	R/W	0h	G3: OUTPUT XBar3 G3 input bit select. Input source is DEL[x].ACTIVE 1: DEL[x] ACTIVE selected 0: DEL[x] ACTIVE is de-selected Reset Source: mod_g_rst_n

3.18.48 CFG0_OUTPUTXBAR3_G4 Registers

3.18.48.1 CFG0_G4 Register (Offset = 1D0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2011. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 81D0h

Figure 3-938. OUTPUTXBAR3_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR3_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR3_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2012. OUTPUTXBAR3_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR3_G4_SEL	R/W	0h	G4: OUTPUT XBar3 G4 input bit select. Input source is DEL[x].TRIP 1: DEL[x] TRIP selected 0: DEL[x] TRIP is de-selected Reset Source: mod_g_rst_n

3.18.49 CFG0_OUTPUTXBAR3_G5 Registers

3.18.49.1 CFG0_G5 Register (Offset = 1D4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2013. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 81D4h

Figure 3-939. OUTPUTXBAR3_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								OUTPUTXBAR3_G5_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR3_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2014. OUTPUTXBAR3_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	OUTPUTXBAR3_G5_SEL	R/W	0h	G5: OUTPUT XBar3 G5 input bit select. 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.18.50 CFG0_OUTPUTXBAR3_G6 Registers

3.18.50.1 CFG0_G6 Register (Offset = 1D8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2015. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 81D8h

Figure 3-940. OUTPUTXBAR3_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR3_G6_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR3_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2016. OUTPUTXBAR3_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR3_G6_SEL	R/W	0h	G6: OUTPUT XBar3 G6 Input Select 0: CMP12SS0.CTRIPOUTL 1: CMP12SS0.CTRIPOUTH 2: CMP12SS1.CTRIPOUTL 3: CMP12SS1.CTRIPOUTH 4: CMP12SS2.CTRIPOUTL 5: CMP12SS2.CTRIPOUTH 6: CMP12SS3.CTRIPOUTL 7: CMP12SS3.CTRIPOUTH 8: CMP12SS4.CTRIPOUTL 9: CMP12SS4.CTRIPOUTH 10: CMP12SS5.CTRIPOUTL 11: CMP12SS5.CTRIPOUTH 12: CMP12SS6.CTRIPOUTL 13: CMP12SS6.CTRIPOUTH 14: CMP12SS7.CTRIPOUTL 15: CMP12SS7.CTRIPOUTH 16: CMP12SS8.CTRIPOUTL 17: CMP12SS8.CTRIPOUTH 18: CMP12SS9.CTRIPOUTL 19: CMP12SS9.CTRIPOUTH Reset Source: mod_g_rst_n

3.18.51 CFG0_OUTPUTXBAR3_G7 Registers

3.18.51.1 CFG0_G7 Register (Offset = 1DCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2017. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 81DCh

Figure 3-941. OUTPUTXBAR3_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR3_G7_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR3_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2018. OUTPUTXBAR3_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR3_G7_SEL	R/W	0h	G7: OUTPUT XBar3 G7 Input Select 0: CMP8SS0.CTRIPOUTL 1: CMP8SS0.CTRIPOUTH 2: CMP8SS1.CTRIPOUTL 3: CMP8SS1.CTRIPOUTH 4: CMP8SS2.CTRIPOUTL 5: CMP8SS2.CTRIPOUTH 6: CMP8SS3.CTRIPOUTL 7: CMP8SS3.CTRIPOUTH 8: CMP8SS4.CTRIPOUTL 9: CMP8SS4.CTRIPOUTH 10: CMP8SS5.CTRIPOUTL 11: CMP8SS5.CTRIPOUTH 12: CMP8SS6.CTRIPOUTL 13: CMP8SS6.CTRIPOUTH 14: CMP8SS7.CTRIPOUTL 15: CMP8SS7.CTRIPOUTH 16: CMP8SS8.CTRIPOUTL 17: CMP8SS8.CTRIPOUTH 18: CMP8SS9.CTRIPOUTL 19: CMP8SS9.CTRIPOUTH Reset Source: mod_g_rst_n

3.18.52 CFG0_OUTPUTXBAR3_G8 Registers

3.18.52.1 CFG0_G8 Register (Offset = 1E0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2019. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 81E0h

Figure 3-942. OUTPUTXBAR3_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR3_G8_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR3_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2020. OUTPUTXBAR3_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR3_G8_SEL	R/W	0h	G8: OUTPUT XBar3 G8 Input Select 0: ADC0.EVT1 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1 EVT4 8: ADC2.EVT1 9: ADC2 EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.18.53 CFG0_OUTPUTXBAR3_G9 Registers

3.18.53.1 CFG0_G9 Register (Offset = 1E4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2021. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 81E4h

Figure 3-943. OUTPUTXBAR3_G9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR3_G9_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR3_G9_SEL															
R/W															
0h															

Access Types Legend

Table 3-2022. OUTPUTXBAR3_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR3_G9_SEL	R/W	0h	G9: OUTPUT XBar3 G9 Input Select 0: PWMSyncOutXBar.SYNCOUT0 1: PWMSyncOutXBar.SYNCOUT1 2: PWMSyncOutXBar.SYNCOUT2 3: PWMSyncOutXBar.SYNCOUT3 4: EQEP0.I_OUT 5: EQEP0.S_OUT 6: EQEP1.I_OUT 7: EQEP1.S_OUT 8: EQEP2.I_OUT 9: EQEP2.S_OUT 10: ECAP0.OUT 11: ECAP1.OUT 12: ECAP2.OUT 13: ECAP3.OUT 14: ECAP4.OUT 15: ECAP5.OUT 16: ECAP6.OUT 17: ECAP7.OUT 18: ECAP8.OUT 19: ECAP9.OUT Reset Source: mod_g_rst_n

3.18.54 CFG0_OUTPUTXBAR3_G10 Registers

3.18.54.1 CFG0_G10 Register (Offset = 1E8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2023. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 81E8h

Figure 3-944. OUTPUTXBAR3_G10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR3_G10_SEL															
R/W															
0h															

Access Types Legend

Table 3-2024. OUTPUTXBAR3_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	OUTPUTXBAR3_G10_SEL	R/W	0h	G10: OUTPUT XBar3 G10 Input Select 3:0: FSIRX0.RX_TRIG0 7:4: FSIRX1.RX_TRIG0 11:8: FSIRX2.RX_TRIG0 15:12: FSIRX3.RX_TRIG0 Reset Source: mod_g_rst_n

3.18.55 CFG0_OUTPUTXBAR4_G0 Registers

3.18.55.1 CFG0_G0 Register (Offset = 200h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2025. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8200h

Figure 3-945. OUTPUTXBAR4_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR4_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR4_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2026. OUTPUTXBAR4_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR4_G0_SEL	R/W	0h	G0: PWM XBar4 G0 input bit select. Input source is PWM[x].TRIPOUT 1: PWM[x] TRIPOUT selected 0: PWM[x] TRIPOUT is de-selected Reset Source: mod_g_rst_n

3.18.56 CFG0_OUTPUTXBAR4_G1 Registers

3.18.56.1 CFG0_G1 Register (Offset = 204h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2027. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8204h

Figure 3-946. OUTPUTXBAR4_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR4_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR4_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2028. OUTPUTXBAR4_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR4_G1_SEL	R/W	0h	G1: OUTPUT XBar4 G1 input bit select. Input source is PWM[x].SOCA 1: PWM[x] SOCA selected 0: PWM[x] SOCA is de-selected Reset Source: mod_g_rst_n

3.18.57 CFG0_OUTPUTXBAR4_G2 Registers

3.18.57.1 CFG0_G2 Register (Offset = 208h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2029. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8208h

Figure 3-947. OUTPUTXBAR4_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR4_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR4_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2030. OUTPUTXBAR4_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR4_G2_SEL	R/W	0h	G2: OUTPUT XBar4 G2 input bit select. Input source is PWM[x].SOCB 1: PWM[x] SOCB selected 0: PWM[x] SOCB is de-selected Reset Source: mod_g_rst_n

3.18.58 CFG0_OUTPUTXBAR4_G3 Registers

3.18.58.1 CFG0_G3 Register (Offset = 20Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2031. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 820Ch

Figure 3-948. OUTPUTXBAR4_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR4_G3_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR4_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2032. OUTPUTXBAR4_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR4_G3_SEL	R/W	0h	G3: OUTPUT XBar4 G3 input bit select. Input source is DEL[x].ACTIVE 1: DEL[x] ACTIVE selected 0: DEL[x] ACTIVE is de-selected Reset Source: mod_g_rst_n

3.18.59 CFG0_OUTPUTXBAR4_G4 Registers

3.18.59.1 CFG0_G4 Register (Offset = 210h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2033. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8210h

Figure 3-949. OUTPUTXBAR4_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR4_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR4_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2034. OUTPUTXBAR4_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR4_G4_SEL	R/W	0h	G4: OUTPUT XBar4 G4 input bit select. Input source is DEL[x].TRIP 1: DEL[x] TRIP selected 0: DEL[x] TRIP is de-selected Reset Source: mod_g_rst_n

3.18.60 CFG0_OUTPUTXBAR4_G5 Registers

3.18.60.1 CFG0_G5 Register (Offset = 214h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2035. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8214h

Figure 3-950. OUTPUTXBAR4_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								OUTPUTXBAR4_G5_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR4_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2036. OUTPUTXBAR4_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	OUTPUTXBAR4_G5_SEL	R/W	0h	G5: OUTPUT XBar4 G5 input bit select. 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.18.61 CFG0_OUTPUTXBAR4_G6 Registers

3.18.61.1 CFG0_G6 Register (Offset = 218h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2037. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8218h

Figure 3-951. OUTPUTXBAR4_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR4_G6_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR4_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2038. OUTPUTXBAR4_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR4_G6_SEL	R/W	0h	G6: OUTPUT XBar4 G6 Input Select 0: CMP12SS0.CTRIPOUTL 1: CMP12SS0.CTRIPOUTH 2: CMP12SS1.CTRIPOUTL 3: CMP12SS1.CTRIPOUTH 4: CMP12SS2.CTRIPOUTL 5: CMP12SS2.CTRIPOUTH 6: CMP12SS3.CTRIPOUTL 7: CMP12SS3.CTRIPOUTH 8: CMP12SS4.CTRIPOUTL 9: CMP12SS4.CTRIPOUTH 10: CMP12SS5.CTRIPOUTL 11: CMP12SS5.CTRIPOUTH 12: CMP12SS6.CTRIPOUTL 13: CMP12SS6.CTRIPOUTH 14: CMP12SS7.CTRIPOUTL 15: CMP12SS7.CTRIPOUTH 16: CMP12SS8.CTRIPOUTL 17: CMP12SS8.CTRIPOUTH 18: CMP12SS9.CTRIPOUTL 19: CMP12SS9.CTRIPOUTH Reset Source: mod_g_rst_n

3.18.62 CFG0_OUTPUTXBAR4_G7 Registers

3.18.62.1 CFG0_G7 Register (Offset = 21Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2039. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 821Ch

Figure 3-952. OUTPUTXBAR4_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR4_G7_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR4_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2040. OUTPUTXBAR4_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR4_G7_SEL	R/W	0h	G7: OUTPUT XBar4 G7 Input Select 0: CMP8SS0.CTRIPOUTL 1: CMP8SS0.CTRIPOUTH 2: CMP8SS1.CTRIPOUTL 3: CMP8SS1.CTRIPOUTH 4: CMP8SS2.CTRIPOUTL 5: CMP8SS2.CTRIPOUTH 6: CMP8SS3.CTRIPOUTL 7: CMP8SS3.CTRIPOUTH 8: CMP8SS4.CTRIPOUTL 9: CMP8SS4.CTRIPOUTH 10: CMP8SS5.CTRIPOUTL 11: CMP8SS5.CTRIPOUTH 12: CMP8SS6.CTRIPOUTL 13: CMP8SS6.CTRIPOUTH 14: CMP8SS7.CTRIPOUTL 15: CMP8SS7.CTRIPOUTH 16: CMP8SS8.CTRIPOUTL 17: CMP8SS8.CTRIPOUTH 18: CMP8SS9.CTRIPOUTL 19: CMP8SS9.CTRIPOUTH Reset Source: mod_g_rst_n

3.18.63 CFG0_OUTPUTXBAR4_G8 Registers

3.18.63.1 CFG0_G8 Register (Offset = 220h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2041. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8220h

Figure 3-953. OUTPUTXBAR4_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR4_G8_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR4_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2042. OUTPUTXBAR4_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR4_G8_SEL	R/W	0h	G8: OUTPUT XBar4 G8 Input Select 0: ADC0.EVT1 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1 EVT4 8: ADC2.EVT1 9: ADC2 EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.18.64 CFG0_OUTPUTXBAR4_G9 Registers

3.18.64.1 CFG0_G9 Register (Offset = 224h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2043. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8224h

Figure 3-954. OUTPUTXBAR4_G9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR4_G9_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR4_G9_SEL															
R/W															
0h															

Access Types Legend

Table 3-2044. OUTPUTXBAR4_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR4_G9_SEL	R/W	0h	G9: OUTPUT XBar4 G9 Input Select 0: PWMSyncOutXBar.SYNCOUT0 1: PWMSyncOutXBar.SYNCOUT1 2: PWMSyncOutXBar.SYNCOUT2 3: PWMSyncOutXBar.SYNCOUT3 4: EQEP0.I_OUT 5: EQEP0.S_OUT 6: EQEP1.I_OUT 7: EQEP1.S_OUT 8: EQEP2.I_OUT 9: EQEP2.S_OUT 10: ECAP0.OUT 11: ECAP1.OUT 12: ECAP2.OUT 13: ECAP3.OUT 14: ECAP4.OUT 15: ECAP5.OUT 16: ECAP6.OUT 17: ECAP7.OUT 18: ECAP8.OUT 19: ECAP9.OUT Reset Source: mod_g_rst_n

3.18.65 CFG0_OUTPUTXBAR4_G10 Registers

3.18.65.1 CFG0_G10 Register (Offset = 228h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2045. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8228h

Figure 3-955. OUTPUTXBAR4_G10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR4_G10_SEL															
R/W															
0h															

Access Types Legend

Table 3-2046. OUTPUTXBAR4_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	OUTPUTXBAR4_G10_SEL	R/W	0h	G10: OUTPUT XBar4 G10 Input Select 3:0: FSIRX0.RX_TRIG0 7:4: FSIRX1.RX_TRIG0 11:8: FSIRX2.RX_TRIG0 15:12: FSIRX3.RX_TRIG0 Reset Source: mod_g_rst_n

3.18.66 CFG0_OUTPUTXBAR5_G0 Registers

3.18.66.1 CFG0_G0 Register (Offset = 240h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2047. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8240h

Figure 3-956. OUTPUTXBAR5_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR5_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR5_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2048. OUTPUTXBAR5_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR5_G0_SEL	R/W	0h	G0: PWM XBar5 G0 input bit select. Input source is PWM[x].TRIPOUT 1: PWM[x] TRIPOUT selected 0: PWM[x] TRIPOUT is de-selected Reset Source: mod_g_rst_n

3.18.67 CFG0_OUTPUTXBAR5_G1 Registers

3.18.67.1 CFG0_G1 Register (Offset = 244h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2049. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8244h

Figure 3-957. OUTPUTXBAR5_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR5_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR5_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2050. OUTPUTXBAR5_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR5_G1_SEL	R/W	0h	G1: OUTPUT XBar5 G1 input bit select. Input source is PWM[x].SOCA 1: PWM[x] SOCA selected 0: PWM[x] SOCA is de-selected Reset Source: mod_g_rst_n

3.18.68 CFG0_OUTPUTXBAR5_G2 Registers

3.18.68.1 CFG0_G2 Register (Offset = 248h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2051. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8248h

Figure 3-958. OUTPUTXBAR5_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR5_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR5_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2052. OUTPUTXBAR5_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR5_G2_SEL	R/W	0h	G2: OUTPUT XBar5 G2 input bit select. Input source is PWM[x].SOCB 1: PWM[x] SOCB selected 0: PWM[x] SOCB is de-selected Reset Source: mod_g_rst_n

3.18.69 CFG0_OUTPUTXBAR5_G3 Registers

3.18.69.1 CFG0_G3 Register (Offset = 24Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2053. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 824Ch

Figure 3-959. OUTPUTXBAR5_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR5_G3_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR5_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2054. OUTPUTXBAR5_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR5_G3_SEL	R/W	0h	G3: OUTPUT XBar5 G3 input bit select. Input source is DEL[x].ACTIVE 1: DEL[x] ACTIVE selected 0: DEL[x] ACTIVE is de-selected Reset Source: mod_g_rst_n

3.18.70 CFG0_OUTPUTXBAR5_G4 Registers

3.18.70.1 CFG0_G4 Register (Offset = 250h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2055. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8250h

Figure 3-960. OUTPUTXBAR5_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR5_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR5_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2056. OUTPUTXBAR5_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR5_G4_SEL	R/W	0h	G4: OUTPUT XBar5 G4 input bit select. Input source is DEL[x].TRIP 1: DEL[x] TRIP selected 0: DEL[x] TRIP is de-selected Reset Source: mod_g_rst_n

3.18.71 CFG0_OUTPUTXBAR5_G5 Registers

3.18.71.1 CFG0_G5 Register (Offset = 254h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2057. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8254h

Figure 3-961. OUTPUTXBAR5_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								OUTPUTXBAR5_G5_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR5_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2058. OUTPUTXBAR5_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	OUTPUTXBAR5_G5_SEL	R/W	0h	G5: OUTPUT XBar5 G5 input bit select. 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.18.72 CFG0_OUTPUTXBAR5_G6 Registers

3.18.72.1 CFG0_G6 Register (Offset = 258h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2059. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8258h

Figure 3-962. OUTPUTXBAR5_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR5_G6_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR5_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2060. OUTPUTXBAR5_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR5_G6_SEL	R/W	0h	G6: OUTPUT XBar5 G6 Input Select 0: CMP12SS0.CTRIPOUTL 1: CMP12SS0.CTRIPOUTH 2: CMP12SS1.CTRIPOUTL 3: CMP12SS1.CTRIPOUTH 4: CMP12SS2.CTRIPOUTL 5: CMP12SS2.CTRIPOUTH 6: CMP12SS3.CTRIPOUTL 7: CMP12SS3.CTRIPOUTH 8: CMP12SS4.CTRIPOUTL 9: CMP12SS4.CTRIPOUTH 10: CMP12SS5.CTRIPOUTL 11: CMP12SS5.CTRIPOUTH 12: CMP12SS6.CTRIPOUTL 13: CMP12SS6.CTRIPOUTH 14: CMP12SS7.CTRIPOUTL 15: CMP12SS7.CTRIPOUTH 16: CMP12SS8.CTRIPOUTL 17: CMP12SS8.CTRIPOUTH 18: CMP12SS9.CTRIPOUTL 19: CMP12SS9.CTRIPOUTH Reset Source: mod_g_rst_n

3.18.73 CFG0_OUTPUTXBAR5_G7 Registers

3.18.73.1 CFG0_G7 Register (Offset = 25Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2061. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 825Ch

Figure 3-963. OUTPUTXBAR5_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR5_G7_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR5_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2062. OUTPUTXBAR5_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR5_G7_SEL	R/W	0h	G7: OUTPUT XBar5 G7 Input Select 0: CMP8SS0.CTRIPOUTL 1: CMP8SS0.CTRIPOUTH 2: CMP8SS1.CTRIPOUTL 3: CMP8SS1.CTRIPOUTH 4: CMP8SS2.CTRIPOUTL 5: CMP8SS2.CTRIPOUTH 6: CMP8SS3.CTRIPOUTL 7: CMP8SS3.CTRIPOUTH 8: CMP8SS4.CTRIPOUTL 9: CMP8SS4.CTRIPOUTH 10: CMP8SS5.CTRIPOUTL 11: CMP8SS5.CTRIPOUTH 12: CMP8SS6.CTRIPOUTL 13: CMP8SS6.CTRIPOUTH 14: CMP8SS7.CTRIPOUTL 15: CMP8SS7.CTRIPOUTH 16: CMP8SS8.CTRIPOUTL 17: CMP8SS8.CTRIPOUTH 18: CMP8SS9.CTRIPOUTL 19: CMP8SS9.CTRIPOUTH Reset Source: mod_g_rst_n

3.18.74 CFG0_OUTPUTXBAR5_G8 Registers

3.18.74.1 CFG0_G8 Register (Offset = 260h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2063. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8260h

Figure 3-964. OUTPUTXBAR5_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR5_G8_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR5_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2064. OUTPUTXBAR5_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR5_G8_SEL	R/W	0h	G8: OUTPUT XBar5 G8 Input Select 0: ADC0.EVT1 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1 EVT4 8: ADC2.EVT1 9: ADC2 EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.18.75 CFG0_OUTPUTXBAR5_G9 Registers

3.18.75.1 CFG0_G9 Register (Offset = 264h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2065. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8264h

Figure 3-965. OUTPUTXBAR5_G9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR5_G9_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR5_G9_SEL															
R/W															
0h															

Access Types Legend

Table 3-2066. OUTPUTXBAR5_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR5_G9_SEL	R/W	0h	G9: OUTPUT XBar5 G9 Input Select 0: PWMSyncOutXBar.SYNCOUT0 1: PWMSyncOutXBar.SYNCOUT1 2: PWMSyncOutXBar.SYNCOUT2 3: PWMSyncOutXBar.SYNCOUT3 4: EQEP0.I_OUT 5: EQEP0.S_OUT 6: EQEP1.I_OUT 7: EQEP1.S_OUT 8: EQEP2.I_OUT 9: EQEP2.S_OUT 10: ECAP0.OUT 11: ECAP1.OUT 12: ECAP2.OUT 13: ECAP3.OUT 14: ECAP4.OUT 15: ECAP5.OUT 16: ECAP6.OUT 17: ECAP7.OUT 18: ECAP8.OUT 19: ECAP9.OUT Reset Source: mod_g_rst_n

3.18.76 CFG0_OUTPUTXBAR5_G10 Registers

3.18.76.1 CFG0_G10 Register (Offset = 268h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2067. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8268h

Figure 3-966. OUTPUTXBAR5_G10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR5_G10_SEL															
R/W															
0h															

Access Types Legend

Table 3-2068. OUTPUTXBAR5_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	OUTPUTXBAR5_G10_SEL	R/W	0h	G10: OUTPUT XBar5 G10 Input Select 3:0: FSIRX0.RX_TRIG0 7:4: FSIRX1.RX_TRIG0 11:8: FSIRX2.RX_TRIG0 15:12: FSIRX3.RX_TRIG0 Reset Source: mod_g_rst_n

3.18.77 CFG0_OUTPUTXBAR6_G0 Registers

3.18.77.1 CFG0_G0 Register (Offset = 280h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2069. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8280h

Figure 3-967. OUTPUTXBAR6_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR6_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR6_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2070. OUTPUTXBAR6_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR6_G0_SEL	R/W	0h	G0: PWM XBar6 G0 input bit select. Input source is PWM[x].TRIPOUT 1: PWM[x] TRIPOUT selected 0: PWM[x] TRIPOUT is de-selected Reset Source: mod_g_rst_n

3.18.78 CFG0_OUTPUTXBAR6_G1 Registers

3.18.78.1 CFG0_G1 Register (Offset = 284h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2071. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8284h

Figure 3-968. OUTPUTXBAR6_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR6_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR6_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2072. OUTPUTXBAR6_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR6_G1_SEL	R/W	0h	G1: OUTPUT XBar6 G1 input bit select. Input source is PWM[x].SOCA 1: PWM[x] SOCA selected 0: PWM[x] SOCA is de-selected Reset Source: mod_g_rst_n

3.18.79 CFG0_OUTPUTXBAR6_G2 Registers

3.18.79.1 CFG0_G2 Register (Offset = 288h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2073. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8288h

Figure 3-969. OUTPUTXBAR6_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR6_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR6_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2074. OUTPUTXBAR6_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR6_G2_SEL	R/W	0h	G2: OUTPUT XBar6 G2 input bit select. Input source is PWM[x].SOCB 1: PWM[x] SOCB selected 0: PWM[x] SOCB is de-selected Reset Source: mod_g_rst_n

3.18.80 CFG0_OUTPUTXBAR6_G3 Registers

3.18.80.1 CFG0_G3 Register (Offset = 28Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2075. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 828Ch

Figure 3-970. OUTPUTXBAR6_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR6_G3_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR6_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2076. OUTPUTXBAR6_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR6_G3_SEL	R/W	0h	G3: OUTPUT XBar6 G3 input bit select. Input source is DEL[x].ACTIVE 1: DEL[x] ACTIVE selected 0: DEL[x] ACTIVE is de-selected Reset Source: mod_g_rst_n

3.18.81 CFG0_OUTPUTXBAR6_G4 Registers

3.18.81.1 CFG0_G4 Register (Offset = 290h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2077. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8290h

Figure 3-971. OUTPUTXBAR6_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR6_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR6_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2078. OUTPUTXBAR6_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR6_G4_SEL	R/W	0h	G4: OUTPUT XBar6 G4 input bit select. Input source is DEL[x].TRIP 1: DEL[x] TRIP selected 0: DEL[x] TRIP is de-selected Reset Source: mod_g_rst_n

3.18.82 CFG0_OUTPUTXBAR6_G5 Registers

3.18.82.1 CFG0_G5 Register (Offset = 294h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2079. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8294h

Figure 3-972. OUTPUTXBAR6_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								OUTPUTXBAR6_G5_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR6_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2080. OUTPUTXBAR6_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	OUTPUTXBAR6_G5_SEL	R/W	0h	G5: OUTPUT XBar6 G5 input bit select. 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.18.83 CFG0_OUTPUTXBAR6_G6 Registers

3.18.83.1 CFG0_G6 Register (Offset = 298h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2081. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8298h

Figure 3-973. OUTPUTXBAR6_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR6_G6_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR6_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2082. OUTPUTXBAR6_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR6_G6_SEL	R/W	0h	G6: OUTPUT XBar6 G6 Input Select 0: CMP12SS0.CTRIPOUTL 1: CMP12SS0.CTRIPOUTH 2: CMP12SS1.CTRIPOUTL 3: CMP12SS1.CTRIPOUTH 4: CMP12SS2.CTRIPOUTL 5: CMP12SS2.CTRIPOUTH 6: CMP12SS3.CTRIPOUTL 7: CMP12SS3.CTRIPOUTH 8: CMP12SS4.CTRIPOUTL 9: CMP12SS4.CTRIPOUTH 10: CMP12SS5.CTRIPOUTL 11: CMP12SS5.CTRIPOUTH 12: CMP12SS6.CTRIPOUTL 13: CMP12SS6.CTRIPOUTH 14: CMP12SS7.CTRIPOUTL 15: CMP12SS7.CTRIPOUTH 16: CMP12SS8.CTRIPOUTL 17: CMP12SS8.CTRIPOUTH 18: CMP12SS9.CTRIPOUTL 19: CMP12SS9.CTRIPOUTH Reset Source: mod_g_rst_n

3.18.84 CFG0_OUTPUTXBAR6_G7 Registers

3.18.84.1 CFG0_G7 Register (Offset = 29Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2083. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 829Ch

Figure 3-974. OUTPUTXBAR6_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR6_G7_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR6_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2084. OUTPUTXBAR6_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR6_G7_SEL	R/W	0h	G7: OUTPUT XBar6 G7 Input Select 0: CMP8SS0.CTRIPOUTL 1: CMP8SS0.CTRIPOUTH 2: CMP8SS1.CTRIPOUTL 3: CMP8SS1.CTRIPOUTH 4: CMP8SS2.CTRIPOUTL 5: CMP8SS2.CTRIPOUTH 6: CMP8SS3.CTRIPOUTL 7: CMP8SS3.CTRIPOUTH 8: CMP8SS4.CTRIPOUTL 9: CMP8SS4.CTRIPOUTH 10: CMP8SS5.CTRIPOUTL 11: CMP8SS5.CTRIPOUTH 12: CMP8SS6.CTRIPOUTL 13: CMP8SS6.CTRIPOUTH 14: CMP8SS7.CTRIPOUTL 15: CMP8SS7.CTRIPOUTH 16: CMP8SS8.CTRIPOUTL 17: CMP8SS8.CTRIPOUTH 18: CMP8SS9.CTRIPOUTL 19: CMP8SS9.CTRIPOUTH Reset Source: mod_g_rst_n

3.18.85 CFG0_OUTPUTXBAR6_G8 Registers

3.18.85.1 CFG0_G8 Register (Offset = 2A0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2085. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 82A0h

Figure 3-975. OUTPUTXBAR6_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR6_G8_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR6_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2086. OUTPUTXBAR6_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR6_G8_SEL	R/W	0h	G8: OUTPUT XBar6 G8 Input Select 0: ADC0.EVT1 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1 EVT4 8: ADC2.EVT1 9: ADC2 EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.18.86 CFG0_OUTPUTXBAR6_G9 Registers

3.18.86.1 CFG0_G9 Register (Offset = 2A4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2087. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 82A4h

Figure 3-976. OUTPUTXBAR6_G9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR6_G9_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR6_G9_SEL															
R/W															
0h															

Access Types Legend

Table 3-2088. OUTPUTXBAR6_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR6_G9_SEL	R/W	0h	G9: OUTPUT XBar6 G9 Input Select 0: PWMSyncOutXBar.SYNCOUT0 1: PWMSyncOutXBar.SYNCOUT1 2: PWMSyncOutXBar.SYNCOUT2 3: PWMSyncOutXBar.SYNCOUT3 4: EQEP0.I_OUT 5: EQEP0.S_OUT 6: EQEP1.I_OUT 7: EQEP1.S_OUT 8: EQEP2.I_OUT 9: EQEP2.S_OUT 10: ECAP0.OUT 11: ECAP1.OUT 12: ECAP2.OUT 13: ECAP3.OUT 14: ECAP4.OUT 15: ECAP5.OUT 16: ECAP6.OUT 17: ECAP7.OUT 18: ECAP8.OUT 19: ECAP9.OUT Reset Source: mod_g_rst_n

3.18.87 CFG0_OUTPUTXBAR6_G10 Registers

3.18.87.1 CFG0_G10 Register (Offset = 2A8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2089. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 82A8h

Figure 3-977. OUTPUTXBAR6_G10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR6_G10_SEL															
R/W															
0h															

Access Types Legend

Table 3-2090. OUTPUTXBAR6_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	OUTPUTXBAR6_G10_SEL	R/W	0h	G10: OUTPUT XBar6 G10 Input Select 3:0: FSIRX0.RX_TRIG0 7:4: FSIRX1.RX_TRIG0 11:8: FSIRX2.RX_TRIG0 15:12: FSIRX3.RX_TRIG0 Reset Source: mod_g_rst_n

3.18.88 CFG0_OUTPUTXBAR7_G0 Registers

3.18.88.1 CFG0_G0 Register (Offset = 2C0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2091. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 82C0h

Figure 3-978. OUTPUTXBAR7_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR7_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR7_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2092. OUTPUTXBAR7_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR7_G0_SEL	R/W	0h	G0: PWM XBar7 G0 input bit select. Input source is PWM[x].TRIPOUT 1: PWM[x] TRIPOUT selected 0: PWM[x] TRIPOUT is de-selected Reset Source: mod_g_rst_n

3.18.89 CFG0_OUTPUTXBAR7_G1 Registers

3.18.89.1 CFG0_G1 Register (Offset = 2C4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2093. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 82C4h

Figure 3-979. OUTPUTXBAR7_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR7_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR7_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2094. OUTPUTXBAR7_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR7_G1_SEL	R/W	0h	G1: OUTPUT XBar7 G1 input bit select. Input source is PWM[x].SOCA 1: PWM[x] SOCA selected 0: PWM[x] SOCA is de-selected Reset Source: mod_g_rst_n

3.18.90 CFG0_OUTPUTXBAR7_G2 Registers

3.18.90.1 CFG0_G2 Register (Offset = 2C8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2095. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 82C8h

Figure 3-980. OUTPUTXBAR7_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR7_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR7_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2096. OUTPUTXBAR7_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR7_G2_SEL	R/W	0h	G2: OUTPUT XBar7 G2 input bit select. Input source is PWM[x].SOCB 1: PWM[x] SOCB selected 0: PWM[x] SOCB is de-selected Reset Source: mod_g_rst_n

3.18.91 CFG0_OUTPUTXBAR7_G3 Registers

3.18.91.1 CFG0_G3 Register (Offset = 2CCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2097. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 82CCh

Figure 3-981. OUTPUTXBAR7_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR7_G3_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR7_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2098. OUTPUTXBAR7_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR7_G3_SEL	R/W	0h	G3: OUTPUT XBar7 G3 input bit select. Input source is DEL[x].ACTIVE 1: DEL[x] ACTIVE selected 0: DEL[x] ACTIVE is de-selected Reset Source: mod_g_rst_n

3.18.92 CFG0_OUTPUTXBAR7_G4 Registers

3.18.92.1 CFG0_G4 Register (Offset = 2D0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2099. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 82D0h

Figure 3-982. OUTPUTXBAR7_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR7_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR7_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2100. OUTPUTXBAR7_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR7_G4_SEL	R/W	0h	G4: OUTPUT XBar7 G4 input bit select. Input source is DEL[x].TRIP 1: DEL[x] TRIP selected 0: DEL[x] TRIP is de-selected Reset Source: mod_g_rst_n

3.18.93 CFG0_OUTPUTXBAR7_G5 Registers

3.18.93.1 CFG0_G5 Register (Offset = 2D4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2101. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 82D4h

Figure 3-983. OUTPUTXBAR7_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								OUTPUTXBAR7_G5_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR7_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2102. OUTPUTXBAR7_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	OUTPUTXBAR7_G5_SEL	R/W	0h	G5: OUTPUT XBar7 G5 input bit select. 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.18.94 CFG0_OUTPUTXBAR7_G6 Registers

3.18.94.1 CFG0_G6 Register (Offset = 2D8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2103. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 82D8h

Figure 3-984. OUTPUTXBAR7_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR7_G6_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR7_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2104. OUTPUTXBAR7_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR7_G6_SEL	R/W	0h	G6: OUTPUT XBar7 G6 Input Select 0: CMP12SS0.CTRIPOUTL 1: CMP12SS0.CTRIPOUTH 2: CMP12SS1.CTRIPOUTL 3: CMP12SS1.CTRIPOUTH 4: CMP12SS2.CTRIPOUTL 5: CMP12SS2.CTRIPOUTH 6: CMP12SS3.CTRIPOUTL 7: CMP12SS3.CTRIPOUTH 8: CMP12SS4.CTRIPOUTL 9: CMP12SS4.CTRIPOUTH 10: CMP12SS5.CTRIPOUTL 11: CMP12SS5.CTRIPOUTH 12: CMP12SS6.CTRIPOUTL 13: CMP12SS6.CTRIPOUTH 14: CMP12SS7.CTRIPOUTL 15: CMP12SS7.CTRIPOUTH 16: CMP12SS8.CTRIPOUTL 17: CMP12SS8.CTRIPOUTH 18: CMP12SS9.CTRIPOUTL 19: CMP12SS9.CTRIPOUTH Reset Source: mod_g_rst_n

3.18.95 CFG0_OUTPUTXBAR7_G7 Registers

3.18.95.1 CFG0_G7 Register (Offset = 2DCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2105. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 82DCh

Figure 3-985. OUTPUTXBAR7_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR7_G7_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR7_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2106. OUTPUTXBAR7_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR7_G7_SEL	R/W	0h	G7: OUTPUT XBar7 G7 Input Select 0: CMP8SS0.CTRIPOUTL 1: CMP8SS0.CTRIPOUTH 2: CMP8SS1.CTRIPOUTL 3: CMP8SS1.CTRIPOUTH 4: CMP8SS2.CTRIPOUTL 5: CMP8SS2.CTRIPOUTH 6: CMP8SS3.CTRIPOUTL 7: CMP8SS3.CTRIPOUTH 8: CMP8SS4.CTRIPOUTL 9: CMP8SS4.CTRIPOUTH 10: CMP8SS5.CTRIPOUTL 11: CMP8SS5.CTRIPOUTH 12: CMP8SS6.CTRIPOUTL 13: CMP8SS6.CTRIPOUTH 14: CMP8SS7.CTRIPOUTL 15: CMP8SS7.CTRIPOUTH 16: CMP8SS8.CTRIPOUTL 17: CMP8SS8.CTRIPOUTH 18: CMP8SS9.CTRIPOUTL 19: CMP8SS9.CTRIPOUTH Reset Source: mod_g_rst_n

3.18.96 CFG0_OUTPUTXBAR7_G8 Registers

3.18.96.1 CFG0_G8 Register (Offset = 2E0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2107. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 82E0h

Figure 3-986. OUTPUTXBAR7_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR7_G8_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR7_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2108. OUTPUTXBAR7_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR7_G8_SEL	R/W	0h	G8: OUTPUT XBar7 G8 Input Select 0: ADC0.EVT1 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1 EVT4 8: ADC2.EVT1 9: ADC2 EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.18.97 CFG0_OUTPUTXBAR7_G9 Registers

3.18.97.1 CFG0_G9 Register (Offset = 2E4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2109. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 82E4h

Figure 3-987. OUTPUTXBAR7_G9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR7_G9_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR7_G9_SEL															
R/W															
0h															

Access Types Legend

Table 3-2110. OUTPUTXBAR7_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR7_G9_SEL	R/W	0h	G9: OUTPUT XBar7 G9 Input Select 0: PWMSyncOutXBar.SYNCOUT0 1: PWMSyncOutXBar.SYNCOUT1 2: PWMSyncOutXBar.SYNCOUT2 3: PWMSyncOutXBar.SYNCOUT3 4: EQEP0.I_OUT 5: EQEP0.S_OUT 6: EQEP1.I_OUT 7: EQEP1.S_OUT 8: EQEP2.I_OUT 9: EQEP2.S_OUT 10: ECAP0.OUT 11: ECAP1.OUT 12: ECAP2.OUT 13: ECAP3.OUT 14: ECAP4.OUT 15: ECAP5.OUT 16: ECAP6.OUT 17: ECAP7.OUT 18: ECAP8.OUT 19: ECAP9.OUT Reset Source: mod_g_rst_n

3.18.98 CFG0_OUTPUTXBAR7_G10 Registers

3.18.98.1 CFG0_G10 Register (Offset = 2E8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2111. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 82E8h

Figure 3-988. OUTPUTXBAR7_G10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR7_G10_SEL															
R/W															
0h															

Access Types Legend

Table 3-2112. OUTPUTXBAR7_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	OUTPUTXBAR7_G10_SEL	R/W	0h	G10: OUTPUT XBar7 G10 Input Select 3:0: FSIRX0.RX_TRIG0 7:4: FSIRX1.RX_TRIG0 11:8: FSIRX2.RX_TRIG0 15:12: FSIRX3.RX_TRIG0 Reset Source: mod_g_rst_n

3.18.99 CFG0_OUTPUTXBAR8_G0 Registers

3.18.99.1 CFG0_G0 Register (Offset = 300h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2113. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8300h

Figure 3-989. OUTPUTXBAR8_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR8_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR8_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2114. OUTPUTXBAR8_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR8_G0_SEL	R/W	0h	G0: PWM XBar8 G0 input bit select. Input source is PWM[x].TRIPOUT 1: PWM[x] TRIPOUT selected 0: PWM[x] TRIPOUT is de-selected Reset Source: mod_g_rst_n

3.18.100 CFG0_OUTPUTXBAR8_G1 Registers

3.18.100.1 CFG0_G1 Register (Offset = 304h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2115. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8304h

Figure 3-990. OUTPUTXBAR8_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR8_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR8_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2116. OUTPUTXBAR8_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR8_G1_SEL	R/W	0h	G1: OUTPUT XBar8 G1 input bit select. Input source is PWM[x].SOCA 1: PWM[x] SOCA selected 0: PWM[x] SOCA is de-selected Reset Source: mod_g_rst_n

3.18.101 CFG0_OUTPUTXBAR8_G2 Registers

3.18.101.1 CFG0_G2 Register (Offset = 308h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2117. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8308h

Figure 3-991. OUTPUTXBAR8_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR8_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR8_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2118. OUTPUTXBAR8_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR8_G2_SEL	R/W	0h	G2: OUTPUT XBar8 G2 input bit select. Input source is PWM[x].SOCB 1: PWM[x] SOCB selected 0: PWM[x] SOCB is de-selected Reset Source: mod_g_rst_n

3.18.102 CFG0_OUTPUTXBAR8_G3 Registers

3.18.102.1 CFG0_G3 Register (Offset = 30Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2119. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 830Ch

Figure 3-992. OUTPUTXBAR8_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR8_G3_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR8_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2120. OUTPUTXBAR8_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR8_G3_SEL	R/W	0h	G3: OUTPUT XBar8 G3 input bit select. Input source is DEL[x].ACTIVE 1: DEL[x] ACTIVE selected 0: DEL[x] ACTIVE is de-selected Reset Source: mod_g_rst_n

3.18.103 CFG0_OUTPUTXBAR8_G4 Registers

3.18.103.1 CFG0_G4 Register (Offset = 310h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2121. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8310h

Figure 3-993. OUTPUTXBAR8_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR8_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR8_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2122. OUTPUTXBAR8_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR8_G4_SEL	R/W	0h	G4: OUTPUT XBar8 G4 input bit select. Input source is DEL[x].TRIP 1: DEL[x] TRIP selected 0: DEL[x] TRIP is de-selected Reset Source: mod_g_rst_n

3.18.104 CFG0_OUTPUTXBAR8_G5 Registers

3.18.104.1 CFG0_G5 Register (Offset = 314h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2123. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8314h

Figure 3-994. OUTPUTXBAR8_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								OUTPUTXBAR8_G5_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR8_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2124. OUTPUTXBAR8_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	OUTPUTXBAR8_G5_SEL	R/W	0h	G5: OUTPUT XBar8 G5 input bit select. 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.18.105 CFG0_OUTPUTXBAR8_G6 Registers

3.18.105.1 CFG0_G6 Register (Offset = 318h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2125. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8318h

Figure 3-995. OUTPUTXBAR8_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR8_G6_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR8_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2126. OUTPUTXBAR8_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR8_G6_SEL	R/W	0h	G6: OUTPUT XBar8 G6 Input Select 0: CMP12SS0.CTRIPOUTL 1: CMP12SS0.CTRIPOUTH 2: CMP12SS1.CTRIPOUTL 3: CMP12SS1.CTRIPOUTH 4: CMP12SS2.CTRIPOUTL 5: CMP12SS2.CTRIPOUTH 6: CMP12SS3.CTRIPOUTL 7: CMP12SS3.CTRIPOUTH 8: CMP12SS4.CTRIPOUTL 9: CMP12SS4.CTRIPOUTH 10: CMP12SS5.CTRIPOUTL 11: CMP12SS5.CTRIPOUTH 12: CMP12SS6.CTRIPOUTL 13: CMP12SS6.CTRIPOUTH 14: CMP12SS7.CTRIPOUTL 15: CMP12SS7.CTRIPOUTH 16: CMP12SS8.CTRIPOUTL 17: CMP12SS8.CTRIPOUTH 18: CMP12SS9.CTRIPOUTL 19: CMP12SS9.CTRIPOUTH Reset Source: mod_g_rst_n

3.18.106 CFG0_OUTPUTXBAR8_G7 Registers

3.18.106.1 CFG0_G7 Register (Offset = 31Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2127. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 831Ch

Figure 3-996. OUTPUTXBAR8_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR8_G7_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR8_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2128. OUTPUTXBAR8_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR8_G7_SEL	R/W	0h	G7: OUTPUT XBar8 G7 Input Select 0: CMP8SS0.CTRIPOUTL 1: CMP8SS0.CTRIPOUTH 2: CMP8SS1.CTRIPOUTL 3: CMP8SS1.CTRIPOUTH 4: CMP8SS2.CTRIPOUTL 5: CMP8SS2.CTRIPOUTH 6: CMP8SS3.CTRIPOUTL 7: CMP8SS3.CTRIPOUTH 8: CMP8SS4.CTRIPOUTL 9: CMP8SS4.CTRIPOUTH 10: CMP8SS5.CTRIPOUTL 11: CMP8SS5.CTRIPOUTH 12: CMP8SS6.CTRIPOUTL 13: CMP8SS6.CTRIPOUTH 14: CMP8SS7.CTRIPOUTL 15: CMP8SS7.CTRIPOUTH 16: CMP8SS8.CTRIPOUTL 17: CMP8SS8.CTRIPOUTH 18: CMP8SS9.CTRIPOUTL 19: CMP8SS9.CTRIPOUTH Reset Source: mod_g_rst_n

3.18.107 CFG0_OUTPUTXBAR8_G8 Registers

3.18.107.1 CFG0_G8 Register (Offset = 320h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2129. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8320h

Figure 3-997. OUTPUTXBAR8_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR8_G8_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR8_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2130. OUTPUTXBAR8_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR8_G8_SEL	R/W	0h	G8: OUTPUT XBar8 G8 Input Select 0: ADC0.EVT1 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1 EVT4 8: ADC2.EVT1 9: ADC2 EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.18.108 CFG0_OUTPUTXBAR8_G9 Registers

3.18.108.1 CFG0_G9 Register (Offset = 324h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2131. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8324h

Figure 3-998. OUTPUTXBAR8_G9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR8_G9_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR8_G9_SEL															
R/W															
0h															

Access Types Legend

Table 3-2132. OUTPUTXBAR8_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR8_G9_SEL	R/W	0h	G9: OUTPUT XBar8 G9 Input Select 0: PWMSyncOutXBar.SYNCOUT0 1: PWMSyncOutXBar.SYNCOUT1 2: PWMSyncOutXBar.SYNCOUT2 3: PWMSyncOutXBar.SYNCOUT3 4: EQEP0.I_OUT 5: EQEP0.S_OUT 6: EQEP1.I_OUT 7: EQEP1.S_OUT 8: EQEP2.I_OUT 9: EQEP2.S_OUT 10: ECAP0.OUT 11: ECAP1.OUT 12: ECAP2.OUT 13: ECAP3.OUT 14: ECAP4.OUT 15: ECAP5.OUT 16: ECAP6.OUT 17: ECAP7.OUT 18: ECAP8.OUT 19: ECAP9.OUT Reset Source: mod_g_rst_n

3.18.109 CFG0_OUTPUTXBAR8_G10 Registers

3.18.109.1 CFG0_G10 Register (Offset = 328h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2133. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8328h

Figure 3-999. OUTPUTXBAR8_G10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR8_G10_SEL															
R/W															
0h															

Access Types Legend

Table 3-2134. OUTPUTXBAR8_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	OUTPUTXBAR8_G10_SEL	R/W	0h	G10: OUTPUT XBar8 G10 Input Select 3:0: FSIRX0.RX_TRIG0 7:4: FSIRX1.RX_TRIG0 11:8: FSIRX2.RX_TRIG0 15:12: FSIRX3.RX_TRIG0 Reset Source: mod_g_rst_n

3.18.110 CFG0_OUTPUTXBAR9_G0 Registers

3.18.110.1 CFG0_G0 Register (Offset = 340h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2135. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8340h

Figure 3-1000. OUTPUTXBAR9_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR9_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR9_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2136. OUTPUTXBAR9_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR9_G0_SEL	R/W	0h	G0: PWM XBar9 G0 input bit select. Input source is PWM[x].TRIPOUT 1: PWM[x] TRIPOUT selected 0: PWM[x] TRIPOUT is de-selected Reset Source: mod_g_rst_n

3.18.111 CFG0_OUTPUTXBAR9_G1 Registers

3.18.111.1 CFG0_G1 Register (Offset = 344h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2137. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8344h

Figure 3-1001. OUTPUTXBAR9_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR9_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR9_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2138. OUTPUTXBAR9_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR9_G1_SEL	R/W	0h	G1: OUTPUT XBar9 G1 input bit select. Input source is PWM[x].SOCA 1: PWM[x] SOCA selected 0: PWM[x] SOCA is de-selected Reset Source: mod_g_rst_n

3.18.112 CFG0_OUTPUTXBAR9_G2 Registers

3.18.112.1 CFG0_G2 Register (Offset = 348h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2139. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8348h

Figure 3-1002. OUTPUTXBAR9_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR9_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR9_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2140. OUTPUTXBAR9_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR9_G2_SEL	R/W	0h	G2: OUTPUT XBar9 G2 input bit select. Input source is PWM[x].SOCB 1: PWM[x] SOCB selected 0: PWM[x] SOCB is de-selected Reset Source: mod_g_rst_n

3.18.113 CFG0_OUTPUTXBAR9_G3 Registers

3.18.113.1 CFG0_G3 Register (Offset = 34Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2141. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 834Ch

Figure 3-1003. OUTPUTXBAR9_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR9_G3_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR9_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2142. OUTPUTXBAR9_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR9_G3_SEL	R/W	0h	G3: OUTPUT XBar9 G3 input bit select. Input source is DEL[x].ACTIVE 1: DEL[x] ACTIVE selected 0: DEL[x] ACTIVE is de-selected Reset Source: mod_g_rst_n

3.18.114 CFG0_OUTPUTXBAR9_G4 Registers

3.18.114.1 CFG0_G4 Register (Offset = 350h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2143. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8350h

Figure 3-1004. OUTPUTXBAR9_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR9_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR9_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2144. OUTPUTXBAR9_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR9_G4_SEL	R/W	0h	G4: OUTPUT XBar9 G4 input bit select. Input source is DEL[x].TRIP 1: DEL[x] TRIP selected 0: DEL[x] TRIP is de-selected Reset Source: mod_g_rst_n

3.18.115 CFG0_OUTPUTXBAR9_G5 Registers

3.18.115.1 CFG0_G5 Register (Offset = 354h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2145. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8354h

Figure 3-1005. OUTPUTXBAR9_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								OUTPUTXBAR9_G5_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR9_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2146. OUTPUTXBAR9_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	OUTPUTXBAR9_G5_SEL	R/W	0h	G5: OUTPUT XBar9 G5 input bit select. 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.18.116 CFG0_OUTPUTXBAR9_G6 Registers

3.18.116.1 CFG0_G6 Register (Offset = 358h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2147. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8358h

Figure 3-1006. OUTPUTXBAR9_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR9_G6_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR9_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2148. OUTPUTXBAR9_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR9_G6_SEL	R/W	0h	G6: OUTPUT XBar9 G6 Input Select 0: CMP12SS0.CTRIPOUTL 1: CMP12SS0.CTRIPOUTH 2: CMP12SS1.CTRIPOUTL 3: CMP12SS1.CTRIPOUTH 4: CMP12SS2.CTRIPOUTL 5: CMP12SS2.CTRIPOUTH 6: CMP12SS3.CTRIPOUTL 7: CMP12SS3.CTRIPOUTH 8: CMP12SS4.CTRIPOUTL 9: CMP12SS4.CTRIPOUTH 10: CMP12SS5.CTRIPOUTL 11: CMP12SS5.CTRIPOUTH 12: CMP12SS6.CTRIPOUTL 13: CMP12SS6.CTRIPOUTH 14: CMP12SS7.CTRIPOUTL 15: CMP12SS7.CTRIPOUTH 16: CMP12SS8.CTRIPOUTL 17: CMP12SS8.CTRIPOUTH 18: CMP12SS9.CTRIPOUTL 19: CMP12SS9.CTRIPOUTH Reset Source: mod_g_rst_n

3.18.117 CFG0_OUTPUTXBAR9_G7 Registers

3.18.117.1 CFG0_G7 Register (Offset = 35Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2149. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 835Ch

Figure 3-1007. OUTPUTXBAR9_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR9_G7_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR9_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2150. OUTPUTXBAR9_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR9_G7_SEL	R/W	0h	G7: OUTPUT XBar9 G7 Input Select 0: CMP8SS0.CTRIPOUTL 1: CMP8SS0.CTRIPOUTH 2: CMP8SS1.CTRIPOUTL 3: CMP8SS1.CTRIPOUTH 4: CMP8SS2.CTRIPOUTL 5: CMP8SS2.CTRIPOUTH 6: CMP8SS3.CTRIPOUTL 7: CMP8SS3.CTRIPOUTH 8: CMP8SS4.CTRIPOUTL 9: CMP8SS4.CTRIPOUTH 10: CMP8SS5.CTRIPOUTL 11: CMP8SS5.CTRIPOUTH 12: CMP8SS6.CTRIPOUTL 13: CMP8SS6.CTRIPOUTH 14: CMP8SS7.CTRIPOUTL 15: CMP8SS7.CTRIPOUTH 16: CMP8SS8.CTRIPOUTL 17: CMP8SS8.CTRIPOUTH 18: CMP8SS9.CTRIPOUTL 19: CMP8SS9.CTRIPOUTH Reset Source: mod_g_rst_n

3.18.118 CFG0_OUTPUTXBAR9_G8 Registers

3.18.118.1 CFG0_G8 Register (Offset = 360h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2151. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8360h

Figure 3-1008. OUTPUTXBAR9_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR9_G8_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR9_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2152. OUTPUTXBAR9_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR9_G8_SEL	R/W	0h	G8: OUTPUT XBar9 G8 Input Select 0: ADC0.EVT1 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1 EVT4 8: ADC2.EVT1 9: ADC2 EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.18.119 CFG0_OUTPUTXBAR9_G9 Registers

3.18.119.1 CFG0_G9 Register (Offset = 364h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2153. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8364h

Figure 3-1009. OUTPUTXBAR9_G9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR9_G9_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR9_G9_SEL															
R/W															
0h															

Access Types Legend

Table 3-2154. OUTPUTXBAR9_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR9_G9_SEL	R/W	0h	G9: OUTPUT XBar9 G9 Input Select 0: PWMSyncOutXBar.SYNCOUT0 1: PWMSyncOutXBar.SYNCOUT1 2: PWMSyncOutXBar.SYNCOUT2 3: PWMSyncOutXBar.SYNCOUT3 4: EQEP0.I_OUT 5: EQEP0.S_OUT 6: EQEP1.I_OUT 7: EQEP1.S_OUT 8: EQEP2.I_OUT 9: EQEP2.S_OUT 10: ECAP0.OUT 11: ECAP1.OUT 12: ECAP2.OUT 13: ECAP3.OUT 14: ECAP4.OUT 15: ECAP5.OUT 16: ECAP6.OUT 17: ECAP7.OUT 18: ECAP8.OUT 19: ECAP9.OUT Reset Source: mod_g_rst_n

3.18.120 CFG0_OUTPUTXBAR9_G10 Registers

3.18.120.1 CFG0_G10 Register (Offset = 368h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2155. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8368h

Figure 3-1010. OUTPUTXBAR9_G10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR9_G10_SEL															
R/W															
0h															

Access Types Legend

Table 3-2156. OUTPUTXBAR9_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	OUTPUTXBAR9_G10_SEL	R/W	0h	G10: OUTPUT XBar9 G10 Input Select 3:0: FSIRX0.RX_TRIG0 7:4: FSIRX1.RX_TRIG0 11:8: FSIRX2.RX_TRIG0 15:12: FSIRX3.RX_TRIG0 Reset Source: mod_g_rst_n

3.18.121 CFG0_OUTPUTXBAR10_G0 Registers

3.18.121.1 CFG0_G0 Register (Offset = 380h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2157. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8380h

Figure 3-1011. OUTPUTXBAR10_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR10_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR10_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2158. OUTPUTXBAR10_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR10_G0_SEL	R/W	0h	G0: PWM XBar10 G0 input bit select. Input source is PWM[x].TRIPOUT 1: PWM[x] TRIPOUT selected 0: PWM[x] TRIPOUT is de-selected Reset Source: mod_g_rst_n

3.18.122 CFG0_OUTPUTXBAR10_G1 Registers

3.18.122.1 CFG0_G1 Register (Offset = 384h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2159. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8384h

Figure 3-1012. OUTPUTXBAR10_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR10_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR10_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2160. OUTPUTXBAR10_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR10_G1_SEL	R/W	0h	G1: OUTPUT XBar10 G1 input bit select. Input source is PWM[x].SOCA 1: PWM[x] SOCA selected 0: PWM[x] SOCA is de-selected Reset Source: mod_g_rst_n

3.18.123 CFG0_OUTPUTXBAR10_G2 Registers

3.18.123.1 CFG0_G2 Register (Offset = 388h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2161. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8388h

Figure 3-1013. OUTPUTXBAR10_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR10_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR10_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2162. OUTPUTXBAR10_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR10_G2_SEL	R/W	0h	G2: OUTPUT XBar10 G2 input bit select. Input source is PWM[x].SOCB 1: PWM[x] SOCB selected 0: PWM[x] SOCB is de-selected Reset Source: mod_g_rst_n

3.18.124 CFG0_OUTPUTXBAR10_G3 Registers

3.18.124.1 CFG0_G3 Register (Offset = 38Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2163. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 838Ch

Figure 3-1014. OUTPUTXBAR10_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR10_G3_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR10_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2164. OUTPUTXBAR10_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR10_G3_SEL	R/W	0h	G3: OUTPUT XBar10 G3 input bit select. Input source is DEL[x].ACTIVE 1: DEL[x] ACTIVE selected 0: DEL[x] ACTIVE is de-selected Reset Source: mod_g_rst_n

3.18.125 CFG0_OUTPUTXBAR10_G4 Registers

3.18.125.1 CFG0_G4 Register (Offset = 390h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2165. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8390h

Figure 3-1015. OUTPUTXBAR10_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR10_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR10_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2166. OUTPUTXBAR10_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR10_G4_SEL	R/W	0h	G4: OUTPUT XBar10 G4 input bit select. Input source is DEL[x].TRIP 1: DEL[x] TRIP selected 0: DEL[x] TRIP is de-selected Reset Source: mod_g_rst_n

3.18.126 CFG0_OUTPUTXBAR10_G5 Registers

3.18.126.1 CFG0_G5 Register (Offset = 394h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2167. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8394h

Figure 3-1016. OUTPUTXBAR10_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								OUTPUTXBAR10_G5_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR10_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2168. OUTPUTXBAR10_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	OUTPUTXBAR10_G5_SEL	R/W	0h	G5: OUTPUT XBar10 G5 input bit select. 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.18.127 CFG0_OUTPUTXBAR10_G6 Registers

3.18.127.1 CFG0_G6 Register (Offset = 398h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2169. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8398h

Figure 3-1017. OUTPUTXBAR10_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR10_G6_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR10_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2170. OUTPUTXBAR10_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR10_G6_SEL	R/W	0h	G6: OUTPUT XBar10 G6 Input Select 0: CMP12SS0.CTRIPOUTL 1: CMP12SS0.CTRIPOUTH 2: CMP12SS1.CTRIPOUTL 3: CMP12SS1.CTRIPOUTH 4: CMP12SS2.CTRIPOUTL 5: CMP12SS2.CTRIPOUTH 6: CMP12SS3.CTRIPOUTL 7: CMP12SS3.CTRIPOUTH 8: CMP12SS4.CTRIPOUTL 9: CMP12SS4.CTRIPOUTH 10: CMP12SS5.CTRIPOUTL 11: CMP12SS5.CTRIPOUTH 12: CMP12SS6.CTRIPOUTL 13: CMP12SS6.CTRIPOUTH 14: CMP12SS7.CTRIPOUTL 15: CMP12SS7.CTRIPOUTH 16: CMP12SS8.CTRIPOUTL 17: CMP12SS8.CTRIPOUTH 18: CMP12SS9.CTRIPOUTL 19: CMP12SS9.CTRIPOUTH Reset Source: mod_g_rst_n

3.18.128 CFG0_OUTPUTXBAR10_G7 Registers

3.18.128.1 CFG0_G7 Register (Offset = 39Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2171. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 839Ch

Figure 3-1018. OUTPUTXBAR10_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR10_G7_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR10_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2172. OUTPUTXBAR10_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR10_G7_SEL	R/W	0h	G7: OUTPUT XBar10 G7 Input Select 0: CMP8SS0.CTRIPOUTL 1: CMP8SS0.CTRIPOUTH 2: CMP8SS1.CTRIPOUTL 3: CMP8SS1.CTRIPOUTH 4: CMP8SS2.CTRIPOUTL 5: CMP8SS2.CTRIPOUTH 6: CMP8SS3.CTRIPOUTL 7: CMP8SS3.CTRIPOUTH 8: CMP8SS4.CTRIPOUTL 9: CMP8SS4.CTRIPOUTH 10: CMP8SS5.CTRIPOUTL 11: CMP8SS5.CTRIPOUTH 12: CMP8SS6.CTRIPOUTL 13: CMP8SS6.CTRIPOUTH 14: CMP8SS7.CTRIPOUTL 15: CMP8SS7.CTRIPOUTH 16: CMP8SS8.CTRIPOUTL 17: CMP8SS8.CTRIPOUTH 18: CMP8SS9.CTRIPOUTL 19: CMP8SS9.CTRIPOUTH Reset Source: mod_g_rst_n

3.18.129 CFG0_OUTPUTXBAR10_G8 Registers

3.18.129.1 CFG0_G8 Register (Offset = 3A0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2173. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 83A0h

Figure 3-1019. OUTPUTXBAR10_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR10_G8_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR10_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2174. OUTPUTXBAR10_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR10_G8_SEL	R/W	0h	G8: OUTPUT XBar10 G8 Input Select 0: ADC0.EVT1 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1 EVT4 8: ADC2.EVT1 9: ADC2 EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.18.130 CFG0_OUTPUTXBAR10_G9 Registers

3.18.130.1 CFG0_G9 Register (Offset = 3A4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2175. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 83A4h

Figure 3-1020. OUTPUTXBAR10_G9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR10_G9_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR10_G9_SEL															
R/W															
0h															

Access Types Legend

Table 3-2176. OUTPUTXBAR10_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR10_G9_SEL	R/W	0h	G9: OUTPUT XBar10 G9 Input Select 0: PWMSyncOutXBar.SYNCOUT0 1: PWMSyncOutXBar.SYNCOUT1 2: PWMSyncOutXBar.SYNCOUT2 3: PWMSyncOutXBar.SYNCOUT3 4: EQEP0.I_OUT 5: EQEP0.S_OUT 6: EQEP1.I_OUT 7: EQEP1.S_OUT 8: EQEP2.I_OUT 9: EQEP2.S_OUT 10: ECAP0.OUT 11: ECAP1.OUT 12: ECAP2.OUT 13: ECAP3.OUT 14: ECAP4.OUT 15: ECAP5.OUT 16: ECAP6.OUT 17: ECAP7.OUT 18: ECAP8.OUT 19: ECAP9.OUT Reset Source: mod_g_rst_n

3.18.131 CFG0_OUTPUTXBAR10_G10 Registers

3.18.131.1 CFG0_G10 Register (Offset = 3A8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2177. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 83A8h

Figure 3-1021. OUTPUTXBAR10_G10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR10_G10_SEL															
R/W															
0h															

Access Types Legend

Table 3-2178. OUTPUTXBAR10_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	OUTPUTXBAR10_G10_SEL	R/W	0h	G10: OUTPUT XBar10 G10 Input Select 3:0: FSIRX0.RX_TRIG0 7:4: FSIRX1.RX_TRIG0 11:8: FSIRX2.RX_TRIG0 15:12: FSIRX3.RX_TRIG0 Reset Source: mod_g_rst_n

3.18.132 CFG0_OUTPUTXBAR11_G0 Registers

3.18.132.1 CFG0_G0 Register (Offset = 3C0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2179. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 83C0h

Figure 3-1022. OUTPUTXBAR11_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR11_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR11_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2180. OUTPUTXBAR11_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR11_G0_SEL	R/W	0h	G0: PWM XBar11 G0 input bit select. Input source is PWM[x].TRIPOUT 1: PWM[x] TRIPOUT selected 0: PWM[x] TRIPOUT is de-selected Reset Source: mod_g_rst_n

3.18.133 CFG0_OUTPUTXBAR11_G1 Registers

3.18.133.1 CFG0_G1 Register (Offset = 3C4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2181. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 83C4h

Figure 3-1023. OUTPUTXBAR11_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR11_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR11_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2182. OUTPUTXBAR11_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR11_G1_SEL	R/W	0h	G1: OUTPUT XBar11 G1 input bit select. Input source is PWM[x].SOCA 1: PWM[x] SOCA selected 0: PWM[x] SOCA is de-selected Reset Source: mod_g_rst_n

3.18.134 CFG0_OUTPUTXBAR11_G2 Registers

3.18.134.1 CFG0_G2 Register (Offset = 3C8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2183. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 83C8h

Figure 3-1024. OUTPUTXBAR11_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR11_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR11_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2184. OUTPUTXBAR11_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR11_G2_SEL	R/W	0h	G2: OUTPUT XBar11 G2 input bit select. Input source is PWM[x].SOCB 1: PWM[x] SOCB selected 0: PWM[x] SOCB is de-selected Reset Source: mod_g_rst_n

3.18.135 CFG0_OUTPUTXBAR11_G3 Registers

3.18.135.1 CFG0_G3 Register (Offset = 3CCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2185. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 83CCh

Figure 3-1025. OUTPUTXBAR11_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR11_G3_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR11_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2186. OUTPUTXBAR11_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR11_G3_SEL	R/W	0h	G3: OUTPUT XBar11 G3 input bit select. Input source is DEL[x].ACTIVE 1: DEL[x] ACTIVE selected 0: DEL[x] ACTIVE is de-selected Reset Source: mod_g_rst_n

3.18.136 CFG0_OUTPUTXBAR11_G4 Registers

3.18.136.1 CFG0_G4 Register (Offset = 3D0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2187. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 83D0h

Figure 3-1026. OUTPUTXBAR11_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR11_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR11_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2188. OUTPUTXBAR11_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR11_G4_SEL	R/W	0h	G4: OUTPUT XBar11 G4 input bit select. Input source is DEL[x].TRIP 1: DEL[x] TRIP selected 0: DEL[x] TRIP is de-selected Reset Source: mod_g_rst_n

3.18.137 CFG0_OUTPUTXBAR11_G5 Registers

3.18.137.1 CFG0_G5 Register (Offset = 3D4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2189. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 83D4h

Figure 3-1027. OUTPUTXBAR11_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								OUTPUTXBAR11_G5_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR11_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2190. OUTPUTXBAR11_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	OUTPUTXBAR11_G5_SEL	R/W	0h	G5: OUTPUT XBar11 G5 input bit select. 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.18.138 CFG0_OUTPUTXBAR11_G6 Registers

3.18.138.1 CFG0_G6 Register (Offset = 3D8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2191. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 83D8h

Figure 3-1028. OUTPUTXBAR11_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR11_G6_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR11_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2192. OUTPUTXBAR11_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR11_G6_SEL	R/W	0h	G6: OUTPUT XBar11 G6 Input Select 0: CMP12SS0.CTRIPOUTL 1: CMP12SS0.CTRIPOUTH 2: CMP12SS1.CTRIPOUTL 3: CMP12SS1.CTRIPOUTH 4: CMP12SS2.CTRIPOUTL 5: CMP12SS2.CTRIPOUTH 6: CMP12SS3.CTRIPOUTL 7: CMP12SS3.CTRIPOUTH 8: CMP12SS4.CTRIPOUTL 9: CMP12SS4.CTRIPOUTH 10: CMP12SS5.CTRIPOUTL 11: CMP12SS5.CTRIPOUTH 12: CMP12SS6.CTRIPOUTL 13: CMP12SS6.CTRIPOUTH 14: CMP12SS7.CTRIPOUTL 15: CMP12SS7.CTRIPOUTH 16: CMP12SS8.CTRIPOUTL 17: CMP12SS8.CTRIPOUTH 18: CMP12SS9.CTRIPOUTL 19: CMP12SS9.CTRIPOUTH Reset Source: mod_g_rst_n

3.18.139 CFG0_OUTPUTXBAR11_G7 Registers

3.18.139.1 CFG0_G7 Register (Offset = 3DCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2193. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 83DCh

Figure 3-1029. OUTPUTXBAR11_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR11_G7_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR11_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2194. OUTPUTXBAR11_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR11_G7_SEL	R/W	0h	G7: OUTPUT XBar11 G7 Input Select 0: CMP8SS0.CTRIPOUTL 1: CMP8SS0.CTRIPOUTH 2: CMP8SS1.CTRIPOUTL 3: CMP8SS1.CTRIPOUTH 4: CMP8SS2.CTRIPOUTL 5: CMP8SS2.CTRIPOUTH 6: CMP8SS3.CTRIPOUTL 7: CMP8SS3.CTRIPOUTH 8: CMP8SS4.CTRIPOUTL 9: CMP8SS4.CTRIPOUTH 10: CMP8SS5.CTRIPOUTL 11: CMP8SS5.CTRIPOUTH 12: CMP8SS6.CTRIPOUTL 13: CMP8SS6.CTRIPOUTH 14: CMP8SS7.CTRIPOUTL 15: CMP8SS7.CTRIPOUTH 16: CMP8SS8.CTRIPOUTL 17: CMP8SS8.CTRIPOUTH 18: CMP8SS9.CTRIPOUTL 19: CMP8SS9.CTRIPOUTH Reset Source: mod_g_rst_n

3.18.140 CFG0_OUTPUTXBAR11_G8 Registers

3.18.140.1 CFG0_G8 Register (Offset = 3E0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2195. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 83E0h

Figure 3-1030. OUTPUTXBAR11_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR11_G8_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR11_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2196. OUTPUTXBAR11_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR11_G8_SEL	R/W	0h	G8: OUTPUT XBar11 G8 Input Select 0: ADC0.EVT1 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1 EVT4 8: ADC2.EVT1 9: ADC2 EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.18.141 CFG0_OUTPUTXBAR11_G9 Registers

3.18.141.1 CFG0_G9 Register (Offset = 3E4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2197. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 83E4h

Figure 3-1031. OUTPUTXBAR11_G9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR11_G9_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR11_G9_SEL															
R/W															
0h															

Access Types Legend

Table 3-2198. OUTPUTXBAR11_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR11_G9_SEL	R/W	0h	G9: OUTPUT XBar11 G9 Input Select 0: PWMSyncOutXBar.SYNCOUT0 1: PWMSyncOutXBar.SYNCOUT1 2: PWMSyncOutXBar.SYNCOUT2 3: PWMSyncOutXBar.SYNCOUT3 4: EQEP0.I_OUT 5: EQEP0.S_OUT 6: EQEP1.I_OUT 7: EQEP1.S_OUT 8: EQEP2.I_OUT 9: EQEP2.S_OUT 10: ECAP0.OUT 11: ECAP1.OUT 12: ECAP2.OUT 13: ECAP3.OUT 14: ECAP4.OUT 15: ECAP5.OUT 16: ECAP6.OUT 17: ECAP7.OUT 18: ECAP8.OUT 19: ECAP9.OUT Reset Source: mod_g_rst_n

3.18.142 CFG0_OUTPUTXBAR11_G10 Registers

3.18.142.1 CFG0_G10 Register (Offset = 3E8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2199. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 83E8h

Figure 3-1032. OUTPUTXBAR11_G10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR11_G10_SEL															
R/W															
0h															

Access Types Legend

Table 3-2200. OUTPUTXBAR11_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	OUTPUTXBAR11_G10_SEL	R/W	0h	G10: OUTPUT XBar11 G10 Input Select 3:0: FSIRX0.RX_TRIG0 7:4: FSIRX1.RX_TRIG0 11:8: FSIRX2.RX_TRIG0 15:12: FSIRX3.RX_TRIG0 Reset Source: mod_g_rst_n

3.18.143 CFG0_OUTPUTXBAR12_G0 Registers

3.18.143.1 CFG0_G0 Register (Offset = 400h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2201. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8400h

Figure 3-1033. OUTPUTXBAR12_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR12_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR12_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2202. OUTPUTXBAR12_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR12_G0_SEL	R/W	0h	G0: PWM XBar12 G0 input bit select. Input source is PWM[x].TRIPOUT 1: PWM[x] TRIPOUT selected 0: PWM[x] TRIPOUT is de-selected Reset Source: mod_g_rst_n

3.18.144 CFG0_OUTPUTXBAR12_G1 Registers

3.18.144.1 CFG0_G1 Register (Offset = 404h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2203. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8404h

Figure 3-1034. OUTPUTXBAR12_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR12_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR12_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2204. OUTPUTXBAR12_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR12_G1_SEL	R/W	0h	G1: OUTPUT XBar12 G1 input bit select. Input source is PWM[x].SOCA 1: PWM[x] SOCA selected 0: PWM[x] SOCA is de-selected Reset Source: mod_g_rst_n

3.18.145 CFG0_OUTPUTXBAR12_G2 Registers

3.18.145.1 CFG0_G2 Register (Offset = 408h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2205. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8408h

Figure 3-1035. OUTPUTXBAR12_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR12_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR12_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2206. OUTPUTXBAR12_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR12_G2_SEL	R/W	0h	G2: OUTPUT XBar12 G2 input bit select. Input source is PWM[x].SOCB 1: PWM[x] SOCB selected 0: PWM[x] SOCB is de-selected Reset Source: mod_g_rst_n

3.18.146 CFG0_OUTPUTXBAR12_G3 Registers

3.18.146.1 CFG0_G3 Register (Offset = 40Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2207. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 840Ch

Figure 3-1036. OUTPUTXBAR12_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR12_G3_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR12_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2208. OUTPUTXBAR12_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR12_G3_SEL	R/W	0h	G3: OUTPUT XBar12 G3 input bit select. Input source is DEL[x].ACTIVE 1: DEL[x] ACTIVE selected 0: DEL[x] ACTIVE is de-selected Reset Source: mod_g_rst_n

3.18.147 CFG0_OUTPUTXBAR12_G4 Registers

3.18.147.1 CFG0_G4 Register (Offset = 410h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2209. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8410h

Figure 3-1037. OUTPUTXBAR12_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR12_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR12_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2210. OUTPUTXBAR12_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR12_G4_SEL	R/W	0h	G4: OUTPUT XBar12 G4 input bit select. Input source is DEL[x].TRIP 1: DEL[x] TRIP selected 0: DEL[x] TRIP is de-selected Reset Source: mod_g_rst_n

3.18.148 CFG0_OUTPUTXBAR12_G5 Registers

3.18.148.1 CFG0_G5 Register (Offset = 414h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2211. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8414h

Figure 3-1038. OUTPUTXBAR12_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								OUTPUTXBAR12_G5_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR12_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2212. OUTPUTXBAR12_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	OUTPUTXBAR12_G5_SEL	R/W	0h	G5: OUTPUT XBar12 G5 input bit select. 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.18.149 CFG0_OUTPUTXBAR12_G6 Registers

3.18.149.1 CFG0_G6 Register (Offset = 418h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2213. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8418h

Figure 3-1039. OUTPUTXBAR12_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR12_G6_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR12_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2214. OUTPUTXBAR12_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR12_G6_SEL	R/W	0h	G6: OUTPUT XBar12 G6 Input Select 0: CMP12SS0.CTRIPOUTL 1: CMP12SS0.CTRIPOUTH 2: CMP12SS1.CTRIPOUTL 3: CMP12SS1.CTRIPOUTH 4: CMP12SS2.CTRIPOUTL 5: CMP12SS2.CTRIPOUTH 6: CMP12SS3.CTRIPOUTL 7: CMP12SS3.CTRIPOUTH 8: CMP12SS4.CTRIPOUTL 9: CMP12SS4.CTRIPOUTH 10: CMP12SS5.CTRIPOUTL 11: CMP12SS5.CTRIPOUTH 12: CMP12SS6.CTRIPOUTL 13: CMP12SS6.CTRIPOUTH 14: CMP12SS7.CTRIPOUTL 15: CMP12SS7.CTRIPOUTH 16: CMP12SS8.CTRIPOUTL 17: CMP12SS8.CTRIPOUTH 18: CMP12SS9.CTRIPOUTL 19: CMP12SS9.CTRIPOUTH Reset Source: mod_g_rst_n

3.18.150 CFG0_OUTPUTXBAR12_G7 Registers

3.18.150.1 CFG0_G7 Register (Offset = 41Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2215. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 841Ch

Figure 3-1040. OUTPUTXBAR12_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR12_G7_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR12_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2216. OUTPUTXBAR12_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR12_G7_SEL	R/W	0h	G7: OUTPUT XBar12 G7 Input Select 0: CMP8SS0.CTRIPOUTL 1: CMP8SS0.CTRIPOUTH 2: CMP8SS1.CTRIPOUTL 3: CMP8SS1.CTRIPOUTH 4: CMP8SS2.CTRIPOUTL 5: CMP8SS2.CTRIPOUTH 6: CMP8SS3.CTRIPOUTL 7: CMP8SS3.CTRIPOUTH 8: CMP8SS4.CTRIPOUTL 9: CMP8SS4.CTRIPOUTH 10: CMP8SS5.CTRIPOUTL 11: CMP8SS5.CTRIPOUTH 12: CMP8SS6.CTRIPOUTL 13: CMP8SS6.CTRIPOUTH 14: CMP8SS7.CTRIPOUTL 15: CMP8SS7.CTRIPOUTH 16: CMP8SS8.CTRIPOUTL 17: CMP8SS8.CTRIPOUTH 18: CMP8SS9.CTRIPOUTL 19: CMP8SS9.CTRIPOUTH Reset Source: mod_g_rst_n

3.18.151 CFG0_OUTPUTXBAR12_G8 Registers

3.18.151.1 CFG0_G8 Register (Offset = 420h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2217. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8420h

Figure 3-1041. OUTPUTXBAR12_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR12_G8_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR12_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2218. OUTPUTXBAR12_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR12_G8_SEL	R/W	0h	G8: OUTPUT XBar12 G8 Input Select 0: ADC0.EVT1 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1 EVT4 8: ADC2.EVT1 9: ADC2 EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.18.152 CFG0_OUTPUTXBAR12_G9 Registers

3.18.152.1 CFG0_G9 Register (Offset = 424h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2219. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8424h

Figure 3-1042. OUTPUTXBAR12_G9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR12_G9_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR12_G9_SEL															
R/W															
0h															

Access Types Legend

Table 3-2220. OUTPUTXBAR12_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR12_G9_SEL	R/W	0h	G9: OUTPUT XBar12 G9 Input Select 0: PWMSyncOutXBar.SYNCOUT0 1: PWMSyncOutXBar.SYNCOUT1 2: PWMSyncOutXBar.SYNCOUT2 3: PWMSyncOutXBar.SYNCOUT3 4: EQEP0.I_OUT 5: EQEP0.S_OUT 6: EQEP1.I_OUT 7: EQEP1.S_OUT 8: EQEP2.I_OUT 9: EQEP2.S_OUT 10: ECAP0.OUT 11: ECAP1.OUT 12: ECAP2.OUT 13: ECAP3.OUT 14: ECAP4.OUT 15: ECAP5.OUT 16: ECAP6.OUT 17: ECAP7.OUT 18: ECAP8.OUT 19: ECAP9.OUT Reset Source: mod_g_rst_n

3.18.153 CFG0_OUTPUTXBAR12_G10 Registers

3.18.153.1 CFG0_G10 Register (Offset = 428h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2221. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8428h

Figure 3-1043. OUTPUTXBAR12_G10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR12_G10_SEL															
R/W															
0h															

Access Types Legend

Table 3-2222. OUTPUTXBAR12_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	OUTPUTXBAR12_G10_SEL	R/W	0h	G10: OUTPUT XBar12 G10 Input Select 3:0: FSIRX0.RX_TRIG0 7:4: FSIRX1.RX_TRIG0 11:8: FSIRX2.RX_TRIG0 15:12: FSIRX3.RX_TRIG0 Reset Source: mod_g_rst_n

3.18.154 CFG0_OUTPUTXBAR13_G0 Registers

3.18.154.1 CFG0_G0 Register (Offset = 440h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2223. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8440h

Figure 3-1044. OUTPUTXBAR13_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR13_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR13_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2224. OUTPUTXBAR13_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR13_G0_SEL	R/W	0h	G0: PWM XBar13 G0 input bit select. Input source is PWM[x].TRIPOUT 1: PWM[x] TRIPOUT selected 0: PWM[x] TRIPOUT is de-selected Reset Source: mod_g_rst_n

3.18.155 CFG0_OUTPUTXBAR13_G1 Registers

3.18.155.1 CFG0_G1 Register (Offset = 444h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2225. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8444h

Figure 3-1045. OUTPUTXBAR13_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR13_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR13_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2226. OUTPUTXBAR13_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR13_G1_SEL	R/W	0h	G1: OUTPUT XBar13 G1 input bit select. Input source is PWM[x].SOCA 1: PWM[x] SOCA selected 0: PWM[x] SOCA is de-selected Reset Source: mod_g_rst_n

3.18.156 CFG0_OUTPUTXBAR13_G2 Registers

3.18.156.1 CFG0_G2 Register (Offset = 448h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2227. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8448h

Figure 3-1046. OUTPUTXBAR13_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR13_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR13_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2228. OUTPUTXBAR13_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR13_G2_SEL	R/W	0h	G2: OUTPUT XBar13 G2 input bit select. Input source is PWM[x].SOCB 1: PWM[x] SOCB selected 0: PWM[x] SOCB is de-selected Reset Source: mod_g_rst_n

3.18.157 CFG0_OUTPUTXBAR13_G3 Registers

3.18.157.1 CFG0_G3 Register (Offset = 44Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2229. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 844Ch

Figure 3-1047. OUTPUTXBAR13_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR13_G3_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR13_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2230. OUTPUTXBAR13_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR13_G3_SEL	R/W	0h	G3: OUTPUT XBar13 G3 input bit select. Input source is DEL[x].ACTIVE 1: DEL[x] ACTIVE selected 0: DEL[x] ACTIVE is de-selected Reset Source: mod_g_rst_n

3.18.158 CFG0_OUTPUTXBAR13_G4 Registers

3.18.158.1 CFG0_G4 Register (Offset = 450h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2231. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8450h

Figure 3-1048. OUTPUTXBAR13_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR13_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR13_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2232. OUTPUTXBAR13_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR13_G4_SEL	R/W	0h	G4: OUTPUT XBar13 G4 input bit select. Input source is DEL[x].TRIP 1: DEL[x] TRIP selected 0: DEL[x] TRIP is de-selected Reset Source: mod_g_rst_n

3.18.159 CFG0_OUTPUTXBAR13_G5 Registers

3.18.159.1 CFG0_G5 Register (Offset = 454h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2233. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8454h

Figure 3-1049. OUTPUTXBAR13_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								OUTPUTXBAR13_G5_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR13_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2234. OUTPUTXBAR13_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	OUTPUTXBAR13_G5_SEL	R/W	0h	G5: OUTPUT XBar13 G5 input bit select. 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.18.160 CFG0_OUTPUTXBAR13_G6 Registers

3.18.160.1 CFG0_G6 Register (Offset = 458h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2235. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8458h

Figure 3-1050. OUTPUTXBAR13_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR13_G6_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR13_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2236. OUTPUTXBAR13_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR13_G6_SEL	R/W	0h	G6: OUTPUT XBar13 G6 Input Select 0: CMP12SS0.CTRIPOUTL 1: CMP12SS0.CTRIPOUTH 2: CMP12SS1.CTRIPOUTL 3: CMP12SS1.CTRIPOUTH 4: CMP12SS2.CTRIPOUTL 5: CMP12SS2.CTRIPOUTH 6: CMP12SS3.CTRIPOUTL 7: CMP12SS3.CTRIPOUTH 8: CMP12SS4.CTRIPOUTL 9: CMP12SS4.CTRIPOUTH 10: CMP12SS5.CTRIPOUTL 11: CMP12SS5.CTRIPOUTH 12: CMP12SS6.CTRIPOUTL 13: CMP12SS6.CTRIPOUTH 14: CMP12SS7.CTRIPOUTL 15: CMP12SS7.CTRIPOUTH 16: CMP12SS8.CTRIPOUTL 17: CMP12SS8.CTRIPOUTH 18: CMP12SS9.CTRIPOUTL 19: CMP12SS9.CTRIPOUTH Reset Source: mod_g_rst_n

3.18.161 CFG0_OUTPUTXBAR13_G7 Registers

3.18.161.1 CFG0_G7 Register (Offset = 45Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2237. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 845Ch

Figure 3-1051. OUTPUTXBAR13_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR13_G7_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR13_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2238. OUTPUTXBAR13_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR13_G7_SEL	R/W	0h	G7: OUTPUT XBar13 G7 Input Select 0: CMP8SS0.CTRIPOUTL 1: CMP8SS0.CTRIPOUTH 2: CMP8SS1.CTRIPOUTL 3: CMP8SS1.CTRIPOUTH 4: CMP8SS2.CTRIPOUTL 5: CMP8SS2.CTRIPOUTH 6: CMP8SS3.CTRIPOUTL 7: CMP8SS3.CTRIPOUTH 8: CMP8SS4.CTRIPOUTL 9: CMP8SS4.CTRIPOUTH 10: CMP8SS5.CTRIPOUTL 11: CMP8SS5.CTRIPOUTH 12: CMP8SS6.CTRIPOUTL 13: CMP8SS6.CTRIPOUTH 14: CMP8SS7.CTRIPOUTL 15: CMP8SS7.CTRIPOUTH 16: CMP8SS8.CTRIPOUTL 17: CMP8SS8.CTRIPOUTH 18: CMP8SS9.CTRIPOUTL 19: CMP8SS9.CTRIPOUTH Reset Source: mod_g_rst_n

3.18.162 CFG0_OUTPUTXBAR13_G8 Registers

3.18.162.1 CFG0_G8 Register (Offset = 460h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2239. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8460h

Figure 3-1052. OUTPUTXBAR13_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR13_G8_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR13_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2240. OUTPUTXBAR13_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR13_G8_SEL	R/W	0h	G8: OUTPUT XBar13 G8 Input Select 0: ADC0.EVT1 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1 EVT4 8: ADC2.EVT1 9: ADC2 EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.18.163 CFG0_OUTPUTXBAR13_G9 Registers

3.18.163.1 CFG0_G9 Register (Offset = 464h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2241. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8464h

Figure 3-1053. OUTPUTXBAR13_G9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR13_G9_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR13_G9_SEL															
R/W															
0h															

Access Types Legend

Table 3-2242. OUTPUTXBAR13_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR13_G9_SEL	R/W	0h	G9: OUTPUT XBar13 G9 Input Select 0: PWMSyncOutXBar.SYNCOUT0 1: PWMSyncOutXBar.SYNCOUT1 2: PWMSyncOutXBar.SYNCOUT2 3: PWMSyncOutXBar.SYNCOUT3 4: EQEP0.I_OUT 5: EQEP0.S_OUT 6: EQEP1.I_OUT 7: EQEP1.S_OUT 8: EQEP2.I_OUT 9: EQEP2.S_OUT 10: ECAP0.OUT 11: ECAP1.OUT 12: ECAP2.OUT 13: ECAP3.OUT 14: ECAP4.OUT 15: ECAP5.OUT 16: ECAP6.OUT 17: ECAP7.OUT 18: ECAP8.OUT 19: ECAP9.OUT Reset Source: mod_g_rst_n

3.18.164 CFG0_OUTPUTXBAR13_G10 Registers

3.18.164.1 CFG0_G10 Register (Offset = 468h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2243. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8468h

Figure 3-1054. OUTPUTXBAR13_G10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR13_G10_SEL															
R/W															
0h															

Access Types Legend

Table 3-2244. OUTPUTXBAR13_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	OUTPUTXBAR13_G10_SEL	R/W	0h	G10: OUTPUT XBar13 G10 Input Select 3:0: FSIRX0.RX_TRIG0 7:4: FSIRX1.RX_TRIG0 11:8: FSIRX2.RX_TRIG0 15:12: FSIRX3.RX_TRIG0 Reset Source: mod_g_rst_n

3.18.165 CFG0_OUTPUTXBAR14_G0 Registers

3.18.165.1 CFG0_G0 Register (Offset = 480h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2245. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8480h

Figure 3-1055. OUTPUTXBAR14_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR14_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR14_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2246. OUTPUTXBAR14_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR14_G0_SEL	R/W	0h	G0: PWM XBar14 G0 input bit select. Input source is PWM[x].TRIPOUT 1: PWM[x] TRIPOUT selected 0: PWM[x] TRIPOUT is de-selected Reset Source: mod_g_rst_n

3.18.166 CFG0_OUTPUTXBAR14_G1 Registers

3.18.166.1 CFG0_G1 Register (Offset = 484h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2247. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8484h

Figure 3-1056. OUTPUTXBAR14_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR14_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR14_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2248. OUTPUTXBAR14_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR14_G1_SEL	R/W	0h	G1: OUTPUT XBar14 G1 input bit select. Input source is PWM[x].SOCA 1: PWM[x] SOCA selected 0: PWM[x] SOCA is de-selected Reset Source: mod_g_rst_n

3.18.167 CFG0_OUTPUTXBAR14_G2 Registers

3.18.167.1 CFG0_G2 Register (Offset = 488h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2249. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8488h

Figure 3-1057. OUTPUTXBAR14_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR14_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR14_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2250. OUTPUTXBAR14_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR14_G2_SEL	R/W	0h	G2: OUTPUT XBar14 G2 input bit select. Input source is PWM[x].SOCB 1: PWM[x] SOCB selected 0: PWM[x] SOCB is de-selected Reset Source: mod_g_rst_n

3.18.168 CFG0_OUTPUTXBAR14_G3 Registers

3.18.168.1 CFG0_G3 Register (Offset = 48Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2251. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 848Ch

Figure 3-1058. OUTPUTXBAR14_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR14_G3_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR14_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2252. OUTPUTXBAR14_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR14_G3_SEL	R/W	0h	G3: OUTPUT XBar14 G3 input bit select. Input source is DEL[x].ACTIVE 1: DEL[x] ACTIVE selected 0: DEL[x] ACTIVE is de-selected Reset Source: mod_g_rst_n

3.18.169 CFG0_OUTPUTXBAR14_G4 Registers

3.18.169.1 CFG0_G4 Register (Offset = 490h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2253. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8490h

Figure 3-1059. OUTPUTXBAR14_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR14_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR14_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2254. OUTPUTXBAR14_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR14_G4_SEL	R/W	0h	G4: OUTPUT XBar14 G4 input bit select. Input source is DEL[x].TRIP 1: DEL[x] TRIP selected 0: DEL[x] TRIP is de-selected Reset Source: mod_g_rst_n

3.18.170 CFG0_OUTPUTXBAR14_G5 Registers

3.18.170.1 CFG0_G5 Register (Offset = 494h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2255. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8494h

Figure 3-1060. OUTPUTXBAR14_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								OUTPUTXBAR14_G5_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR14_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2256. OUTPUTXBAR14_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	OUTPUTXBAR14_G5_SEL	R/W	0h	G5: OUTPUT XBar14 G5 input bit select. 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.18.171 CFG0_OUTPUTXBAR14_G6 Registers

3.18.171.1 CFG0_G6 Register (Offset = 498h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2257. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 8498h

Figure 3-1061. OUTPUTXBAR14_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR14_G6_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR14_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2258. OUTPUTXBAR14_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR14_G6_SEL	R/W	0h	G6: OUTPUT XBar14 G6 Input Select 0: CMP12SS0.CTRIPOUTL 1: CMP12SS0.CTRIPOUTH 2: CMP12SS1.CTRIPOUTL 3: CMP12SS1.CTRIPOUTH 4: CMP12SS2.CTRIPOUTL 5: CMP12SS2.CTRIPOUTH 6: CMP12SS3.CTRIPOUTL 7: CMP12SS3.CTRIPOUTH 8: CMP12SS4.CTRIPOUTL 9: CMP12SS4.CTRIPOUTH 10: CMP12SS5.CTRIPOUTL 11: CMP12SS5.CTRIPOUTH 12: CMP12SS6.CTRIPOUTL 13: CMP12SS6.CTRIPOUTH 14: CMP12SS7.CTRIPOUTL 15: CMP12SS7.CTRIPOUTH 16: CMP12SS8.CTRIPOUTL 17: CMP12SS8.CTRIPOUTH 18: CMP12SS9.CTRIPOUTL 19: CMP12SS9.CTRIPOUTH Reset Source: mod_g_rst_n

3.18.172 CFG0_OUTPUTXBAR14_G7 Registers

3.18.172.1 CFG0_G7 Register (Offset = 49Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2259. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 849Ch

Figure 3-1062. OUTPUTXBAR14_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR14_G7_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR14_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2260. OUTPUTXBAR14_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR14_G7_SEL	R/W	0h	G7: OUTPUT XBar14 G7 Input Select 0: CMP8SS0.CTRIPOUTL 1: CMP8SS0.CTRIPOUTH 2: CMP8SS1.CTRIPOUTL 3: CMP8SS1.CTRIPOUTH 4: CMP8SS2.CTRIPOUTL 5: CMP8SS2.CTRIPOUTH 6: CMP8SS3.CTRIPOUTL 7: CMP8SS3.CTRIPOUTH 8: CMP8SS4.CTRIPOUTL 9: CMP8SS4.CTRIPOUTH 10: CMP8SS5.CTRIPOUTL 11: CMP8SS5.CTRIPOUTH 12: CMP8SS6.CTRIPOUTL 13: CMP8SS6.CTRIPOUTH 14: CMP8SS7.CTRIPOUTL 15: CMP8SS7.CTRIPOUTH 16: CMP8SS8.CTRIPOUTL 17: CMP8SS8.CTRIPOUTH 18: CMP8SS9.CTRIPOUTL 19: CMP8SS9.CTRIPOUTH Reset Source: mod_g_rst_n

3.18.173 CFG0_OUTPUTXBAR14_G8 Registers

3.18.173.1 CFG0_G8 Register (Offset = 4A0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2261. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 84A0h

Figure 3-1063. OUTPUTXBAR14_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR14_G8_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR14_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2262. OUTPUTXBAR14_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR14_G8_SEL	R/W	0h	G8: OUTPUT XBar14 G8 Input Select 0: ADC0.EVT1 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1 EVT4 8: ADC2.EVT1 9: ADC2 EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.18.174 CFG0_OUTPUTXBAR14_G9 Registers

3.18.174.1 CFG0_G9 Register (Offset = 4A4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2263. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 84A4h

Figure 3-1064. OUTPUTXBAR14_G9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR14_G9_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR14_G9_SEL															
R/W															
0h															

Access Types Legend

Table 3-2264. OUTPUTXBAR14_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR14_G9_SEL	R/W	0h	G9: OUTPUT XBar14 G9 Input Select 0: PWMSyncOutXBar.SYNCOUT0 1: PWMSyncOutXBar.SYNCOUT1 2: PWMSyncOutXBar.SYNCOUT2 3: PWMSyncOutXBar.SYNCOUT3 4: EQEP0.I_OUT 5: EQEP0.S_OUT 6: EQEP1.I_OUT 7: EQEP1.S_OUT 8: EQEP2.I_OUT 9: EQEP2.S_OUT 10: ECAP0.OUT 11: ECAP1.OUT 12: ECAP2.OUT 13: ECAP3.OUT 14: ECAP4.OUT 15: ECAP5.OUT 16: ECAP6.OUT 17: ECAP7.OUT 18: ECAP8.OUT 19: ECAP9.OUT Reset Source: mod_g_rst_n

3.18.175 CFG0_OUTPUTXBAR14_G10 Registers

3.18.175.1 CFG0_G10 Register (Offset = 4A8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2265. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 84A8h

Figure 3-1065. OUTPUTXBAR14_G10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR14_G10_SEL															
R/W															
0h															

Access Types Legend

Table 3-2266. OUTPUTXBAR14_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	OUTPUTXBAR14_G10_SEL	R/W	0h	G10: OUTPUT XBar14 G10 Input Select 3:0: FSIRX0.RX_TRIG0 7:4: FSIRX1.RX_TRIG0 11:8: FSIRX2.RX_TRIG0 15:12: FSIRX3.RX_TRIG0 Reset Source: mod_g_rst_n

3.18.176 CFG0_OUTPUTXBAR15_G0 Registers

3.18.176.1 CFG0_G0 Register (Offset = 4C0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2267. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 84C0h

Figure 3-1066. OUTPUTXBAR15_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR15_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR15_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2268. OUTPUTXBAR15_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR15_G0_SEL	R/W	0h	G0: PWM XBar15 G0 input bit select. Input source is PWM[x].TRIPOUT 1: PWM[x] TRIPOUT selected 0: PWM[x] TRIPOUT is de-selected Reset Source: mod_g_rst_n

3.18.177 CFG0_OUTPUTXBAR15_G1 Registers

3.18.177.1 CFG0_G1 Register (Offset = 4C4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2269. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 84C4h

Figure 3-1067. OUTPUTXBAR15_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR15_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR15_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2270. OUTPUTXBAR15_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR15_G1_SEL	R/W	0h	G1: OUTPUT XBar15 G1 input bit select. Input source is PWM[x].SOCA 1: PWM[x] SOCA selected 0: PWM[x] SOCA is de-selected Reset Source: mod_g_rst_n

3.18.178 CFG0_OUTPUTXBAR15_G2 Registers

3.18.178.1 CFG0_G2 Register (Offset = 4C8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2271. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 84C8h

Figure 3-1068. OUTPUTXBAR15_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR15_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR15_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2272. OUTPUTXBAR15_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR15_G2_SEL	R/W	0h	G2: OUTPUT XBar15 G2 input bit select. Input source is PWM[x].SOCB 1: PWM[x] SOCB selected 0: PWM[x] SOCB is de-selected Reset Source: mod_g_rst_n

3.18.179 CFG0_OUTPUTXBAR15_G3 Registers

3.18.179.1 CFG0_G3 Register (Offset = 4CCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2273. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 84CCh

Figure 3-1069. OUTPUTXBAR15_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR15_G3_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR15_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2274. OUTPUTXBAR15_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR15_G3_SEL	R/W	0h	G3: OUTPUT XBar15 G3 input bit select. Input source is DEL[x].ACTIVE 1: DEL[x] ACTIVE selected 0: DEL[x] ACTIVE is de-selected Reset Source: mod_g_rst_n

3.18.180 CFG0_OUTPUTXBAR15_G4 Registers

3.18.180.1 CFG0_G4 Register (Offset = 4D0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2275. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 84D0h

Figure 3-1070. OUTPUTXBAR15_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUTXBAR15_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR15_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2276. OUTPUTXBAR15_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR15_G4_SEL	R/W	0h	G4: OUTPUT XBar15 G4 input bit select. Input source is DEL[x].TRIP 1: DEL[x] TRIP selected 0: DEL[x] TRIP is de-selected Reset Source: mod_g_rst_n

3.18.181 CFG0_OUTPUTXBAR15_G5 Registers

3.18.181.1 CFG0_G5 Register (Offset = 4D4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2277. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 84D4h

Figure 3-1071. OUTPUTXBAR15_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								OUTPUTXBAR15_G5_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR15_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2278. OUTPUTXBAR15_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	OUTPUTXBAR15_G5_SEL	R/W	0h	G5: OUTPUT XBar15 G5 input bit select. 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.18.182 CFG0_OUTPUTXBAR15_G6 Registers

3.18.182.1 CFG0_G6 Register (Offset = 4D8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2279. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 84D8h

Figure 3-1072. OUTPUTXBAR15_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR15_G6_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR15_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2280. OUTPUTXBAR15_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR15_G6_SEL	R/W	0h	G6: OUTPUT XBar15 G6 Input Select 0: CMP12SS0.CTRIPOUTL 1: CMP12SS0.CTRIPOUTH 2: CMP12SS1.CTRIPOUTL 3: CMP12SS1.CTRIPOUTH 4: CMP12SS2.CTRIPOUTL 5: CMP12SS2.CTRIPOUTH 6: CMP12SS3.CTRIPOUTL 7: CMP12SS3.CTRIPOUTH 8: CMP12SS4.CTRIPOUTL 9: CMP12SS4.CTRIPOUTH 10: CMP12SS5.CTRIPOUTL 11: CMP12SS5.CTRIPOUTH 12: CMP12SS6.CTRIPOUTL 13: CMP12SS6.CTRIPOUTH 14: CMP12SS7.CTRIPOUTL 15: CMP12SS7.CTRIPOUTH 16: CMP12SS8.CTRIPOUTL 17: CMP12SS8.CTRIPOUTH 18: CMP12SS9.CTRIPOUTL 19: CMP12SS9.CTRIPOUTH Reset Source: mod_g_rst_n

3.18.183 CFG0_OUTPUTXBAR15_G7 Registers

3.18.183.1 CFG0_G7 Register (Offset = 4DCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2281. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 84DCh

Figure 3-1073. OUTPUTXBAR15_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR15_G7_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR15_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2282. OUTPUTXBAR15_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR15_G7_SEL	R/W	0h	G7: OUTPUT XBar15 G7 Input Select 0: CMP8SS0.CTRIPOUTL 1: CMP8SS0.CTRIPOUTH 2: CMP8SS1.CTRIPOUTL 3: CMP8SS1.CTRIPOUTH 4: CMP8SS2.CTRIPOUTL 5: CMP8SS2.CTRIPOUTH 6: CMP8SS3.CTRIPOUTL 7: CMP8SS3.CTRIPOUTH 8: CMP8SS4.CTRIPOUTL 9: CMP8SS4.CTRIPOUTH 10: CMP8SS5.CTRIPOUTL 11: CMP8SS5.CTRIPOUTH 12: CMP8SS6.CTRIPOUTL 13: CMP8SS6.CTRIPOUTH 14: CMP8SS7.CTRIPOUTL 15: CMP8SS7.CTRIPOUTH 16: CMP8SS8.CTRIPOUTL 17: CMP8SS8.CTRIPOUTH 18: CMP8SS9.CTRIPOUTL 19: CMP8SS9.CTRIPOUTH Reset Source: mod_g_rst_n

3.18.184 CFG0_OUTPUTXBAR15_G8 Registers

3.18.184.1 CFG0_G8 Register (Offset = 4E0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2283. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 84E0h

Figure 3-1074. OUTPUTXBAR15_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR15_G8_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR15_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2284. OUTPUTXBAR15_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR15_G8_SEL	R/W	0h	G8: OUTPUT XBar15 G8 Input Select 0: ADC0.EVT1 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1 EVT4 8: ADC2.EVT1 9: ADC2 EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.18.185 CFG0_OUTPUTXBAR15_G9 Registers

3.18.185.1 CFG0_G9 Register (Offset = 4E4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2285. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 84E4h

Figure 3-1075. OUTPUTXBAR15_G9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												OUTPUTXBAR15_G9_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR15_G9_SEL															
R/W															
0h															

Access Types Legend

Table 3-2286. OUTPUTXBAR15_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	OUTPUTXBAR15_G9_SEL	R/W	0h	G9: OUTPUT XBar15 G9 Input Select 0: PWMSyncOutXBar.SYNCOUT0 1: PWMSyncOutXBar.SYNCOUT1 2: PWMSyncOutXBar.SYNCOUT2 3: PWMSyncOutXBar.SYNCOUT3 4: EQEP0.I_OUT 5: EQEP0.S_OUT 6: EQEP1.I_OUT 7: EQEP1.S_OUT 8: EQEP2.I_OUT 9: EQEP2.S_OUT 10: ECAP0.OUT 11: ECAP1.OUT 12: ECAP2.OUT 13: ECAP3.OUT 14: ECAP4.OUT 15: ECAP5.OUT 16: ECAP6.OUT 17: ECAP7.OUT 18: ECAP8.OUT 19: ECAP9.OUT Reset Source: mod_g_rst_n

3.18.186 CFG0_OUTPUTXBAR15_G10 Registers

3.18.186.1 CFG0_G10 Register (Offset = 4E8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2287. Instance Table

Instance Name	Physical Address
OUTPUTXBAR_MMR0	502D 84E8h

Figure 3-1076. OUTPUTXBAR15_G10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTXBAR15_G10_SEL															
R/W															
0h															

Access Types Legend

Table 3-2288. OUTPUTXBAR15_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	OUTPUTXBAR15_G10_SEL	R/W	0h	G10: OUTPUT XBar15 G10 Input Select 3:0: FSIRX0.RX_TRIG0 7:4: FSIRX1.RX_TRIG0 11:8: FSIRX2.RX_TRIG0 15:12: FSIRX3.RX_TRIG0 Reset Source: mod_g_rst_n

3.18.187 Access Table

Table 3-2289. Access Type Codes

Access Type	Code	Description
R	R	Read
R/W	R/W	Read / Write
R/W1TC	R/W1TC	Read/Write 1 To Clear

3.19 ICLXBAR Registers

Table 3-2290. CFG0, CFG0 Registers, Base Address=0X00000000502D4000, Length=2048

Offset	Length	Register Name	iclxbar_mmr Physical Address
0h	32	PID	502D 4000h
100h	32	ICLXBar0_G0	502D 4100h
104h	32	ICLXBar0_G1	502D 4104h
108h	32	ICLXBar0_G2	502D 4108h
140h	32	ICLXBar1_G0	502D 4140h
144h	32	ICLXBar1_G1	502D 4144h
148h	32	ICLXBar1_G2	502D 4148h
180h	32	ICLXBar2_G0	502D 4180h
184h	32	ICLXBar2_G1	502D 4184h
188h	32	ICLXBar2_G2	502D 4188h
1C0h	32	ICLXBar3_G0	502D 41C0h
1C4h	32	ICLXBar3_G1	502D 41C4h
1C8h	32	ICLXBar3_G2	502D 41C8h
200h	32	ICLXBar4_G0	502D 4200h
204h	32	ICLXBar4_G1	502D 4204h
208h	32	ICLXBar4_G2	502D 4208h
240h	32	ICLXBar5_G0	502D 4240h
244h	32	ICLXBar5_G1	502D 4244h
248h	32	ICLXBar5_G2	502D 4248h
280h	32	ICLXBar6_G0	502D 4280h
284h	32	ICLXBar6_G1	502D 4284h
288h	32	ICLXBar6_G2	502D 4288h
2C0h	32	ICLXBar7_G0	502D 42C0h
2C4h	32	ICLXBar7_G1	502D 42C4h
2C8h	32	ICLXBar7_G2	502D 42C8h
300h	32	ICLXBar8_G0	502D 4300h
304h	32	ICLXBar8_G1	502D 4304h
308h	32	ICLXBar8_G2	502D 4308h
340h	32	ICLXBar9_G0	502D 4340h
344h	32	ICLXBar9_G1	502D 4344h
348h	32	ICLXBar9_G2	502D 4348h
380h	32	ICLXBar10_G0	502D 4380h
384h	32	ICLXBar10_G1	502D 4384h
388h	32	ICLXBar10_G2	502D 4388h
3C0h	32	ICLXBar11_G0	502D 43C0h
3C4h	32	ICLXBar11_G1	502D 43C4h
3C8h	32	ICLXBar11_G2	502D 43C8h
400h	32	ICLXBar12_G0	502D 4400h
404h	32	ICLXBar12_G1	502D 4404h
408h	32	ICLXBar12_G2	502D 4408h
440h	32	ICLXBar13_G0	502D 4440h
444h	32	ICLXBar13_G1	502D 4444h
448h	32	ICLXBar13_G2	502D 4448h
480h	32	ICLXBar14_G0	502D 4480h
484h	32	ICLXBar14_G1	502D 4484h

Table 3-2290. CFG0, CFG0 Registers, Base Address=0X00000000502D4000, Length=2048 (continued)

Offset	Length	Register Name	iclxbar_mmr Physical Address
488h	32	ICLXBar14_G2	502D 4488h
4C0h	32	ICLXBar15_G0	502D 44C0h
4C4h	32	ICLXBar15_G1	502D 44C4h
4C8h	32	ICLXBar15_G2	502D 44C8h

3.19.1 CFG0_PID Registers

3.19.1.1 CFG0_PID Register (Offset = 0h) [reset = 61800215h]

Short Description: PID register

Long Description: PID register

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Table 3-2291. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4000h

Figure 3-1077. PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PID_MSB16															
R															
6180h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_MISC					PID_MAJOR			PID_CUSTOM		PID_MINOR					
R					R			R		R					
0h					2h			0h		15h					

Access Types Legend

Table 3-2292. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR	R	15h	Reset Source: mod_g_rst_n

3.19.2 CFG0_ICLXBAR0_G0 Registers

3.19.2.1 CFG0_G0 Register (Offset = 100h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2293. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4100h

Figure 3-1078. ICLXBAR0_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR0_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR0_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2294. ICLXBAR0_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR0_G0_SEL	R/W	0h	ICL XBar0 G0 input bit select. Input source is PWMA hr select 1: PWMA hr bit[x] selected 0: PWMA hr bit[x] is de-selected Reset Source: mod_g_rst_n

3.19.3 CFG0_ICLXBAR0_G1 Registers

3.19.3.1 CFG0_G1 Register (Offset = 104h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2295. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4104h

Figure 3-1079. ICLXBAR0_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR0_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR0_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2296. ICLXBAR0_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR0_G1_SEL	R/W	0h	ICL XBar0 G1 input bit select. Input source is PWMB hr select 1: PWMB hr bit[x] selected 0: PWMB hr bit[x] is de-selected Reset Source: mod_g_rst_n

3.19.4 CFG0_ICLXBAR0_G2 Registers

3.19.4.1 CFG0_G2 Register (Offset = 108h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2297. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4108h

Figure 3-1080. ICLXBAR0_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR0_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR0_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2298. ICLXBAR0_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR0_G2_SEL	R/W	0h	ICL XBar0 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1: ICSS_PORT[y].GPO[x] selected. 0: ICSS_PORT[y].GPO[x] is de-selected Reset Source: mod_g_rst_n

3.19.5 CFG0_ICLXBAR1_G0 Registers

3.19.5.1 CFG0_G0 Register (Offset = 140h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2299. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4140h

Figure 3-1081. ICLXBAR1_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR1_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR1_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2300. ICLXBAR1_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR1_G0_SEL	R/W	0h	ICL XBar1 G0 input bit select. Input source is PWMA hr select 1: PWMA hr bit[x] selected 0: PWMA hr bit[x] is de-selected Reset Source: mod_g_rst_n

3.19.6 CFG0_ICLXBAR1_G1 Registers

3.19.6.1 CFG0_G1 Register (Offset = 144h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2301. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4144h

Figure 3-1082. ICLXBAR1_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR1_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR1_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2302. ICLXBAR1_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR1_G1_SEL	R/W	0h	ICL XBar1 G1 input bit select. Input source is PWMB hr select 1: PWMB hr bit[x] selected 0: PWMB hr bit[x] is de-selected Reset Source: mod_g_rst_n

3.19.7 CFG0_ICLXBAR1_G2 Registers

3.19.7.1 CFG0_G2 Register (Offset = 148h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2303. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4148h

Figure 3-1083. ICLXBAR1_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR1_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR1_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2304. ICLXBAR1_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR1_G2_SEL	R/W	0h	ICL XBar1 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1: ICSS_PORT[y].GPO[x] selected. 0: ICSS_PORT[y].GPO[x] is de-selected Reset Source: mod_g_rst_n

3.19.8 CFG0_ICLXBAR2_G0 Registers

3.19.8.1 CFG0_G0 Register (Offset = 180h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2305. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4180h

Figure 3-1084. ICLXBAR2_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR2_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR2_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2306. ICLXBAR2_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR2_G0_SEL	R/W	0h	ICL XBar2 G0 input bit select. Input source is PWMA hr select 1: PWMA hr bit[x] selected 0: PWMA hr bit[x] is de-selected Reset Source: mod_g_rst_n

3.19.9 CFG0_ICLXBAR2_G1 Registers

3.19.9.1 CFG0_G1 Register (Offset = 184h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2307. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4184h

Figure 3-1085. ICLXBAR2_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR2_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR2_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2308. ICLXBAR2_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR2_G1_SEL	R/W	0h	ICL XBar2 G1 input bit select. Input source is PWMB hr select 1: PWMB hr bit[x] selected 0: PWMB hr bit[x] is de-selected Reset Source: mod_g_rst_n

3.19.10 CFG0_ICLXBAR2_G2 Registers

3.19.10.1 CFG0_G2 Register (Offset = 188h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2309. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4188h

Figure 3-1086. ICLXBAR2_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR2_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR2_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2310. ICLXBAR2_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR2_G2_SEL	R/W	0h	ICL XBar2 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1: ICSS_PORT[y].GPO[x] selected. 0: ICSS_PORT[y].GPO[x] is de-selected Reset Source: mod_g_rst_n

3.19.11 CFG0_ICLXBAR3_G0 Registers

3.19.11.1 CFG0_G0 Register (Offset = 1C0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2311. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 41C0h

Figure 3-1087. ICLXBAR3_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR3_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR3_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2312. ICLXBAR3_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR3_G0_SEL	R/W	0h	ICL XBar3 G0 input bit select. Input source is PWMA hr select 1: PWMA hr bit[x] selected 0: PWMA hr bit[x] is de-selected Reset Source: mod_g_rst_n

3.19.12 CFG0_ICLXBAR3_G1 Registers

3.19.12.1 CFG0_G1 Register (Offset = 1C4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2313. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 41C4h

Figure 3-1088. ICLXBAR3_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR3_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR3_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2314. ICLXBAR3_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR3_G1_SEL	R/W	0h	ICL XBar3 G1 input bit select. Input source is PWMB hr select 1: PWMB hr bit[x] selected 0: PWMB hr bit[x] is de-selected Reset Source: mod_g_rst_n

3.19.13 CFG0_ICLXBAR3_G2 Registers

3.19.13.1 CFG0_G2 Register (Offset = 1C8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2315. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 41C8h

Figure 3-1089. ICLXBAR3_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR3_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR3_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2316. ICLXBAR3_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR3_G2_SEL	R/W	0h	ICL XBar3 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1: ICSS_PORT[y].GPO[x] selected. 0: ICSS_PORT[y].GPO[x] is de-selected Reset Source: mod_g_rst_n

3.19.14 CFG0_ICLXBAR4_G0 Registers

3.19.14.1 CFG0_G0 Register (Offset = 200h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2317. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4200h

Figure 3-1090. ICLXBAR4_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR4_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR4_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2318. ICLXBAR4_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR4_G0_SEL	R/W	0h	ICL XBar4 G0 input bit select. Input source is PWMA hr select 1: PWMA hr bit[x] selected 0: PWMA hr bit[x] is de-selected Reset Source: mod_g_rst_n

3.19.15 CFG0_ICLXBAR4_G1 Registers

3.19.15.1 CFG0_G1 Register (Offset = 204h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2319. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4204h

Figure 3-1091. ICLXBAR4_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR4_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR4_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2320. ICLXBAR4_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR4_G1_SEL	R/W	0h	ICL XBar4 G1 input bit select. Input source is PWMB hr select 1: PWMB hr bit[x] selected 0: PWMB hr bit[x] is de-selected Reset Source: mod_g_rst_n

3.19.16 CFG0_ICLXBAR4_G2 Registers

3.19.16.1 CFG0_G2 Register (Offset = 208h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2321. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4208h

Figure 3-1092. ICLXBAR4_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR4_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR4_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2322. ICLXBAR4_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR4_G2_SEL	R/W	0h	ICL XBar4 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1: ICSS_PORT[y].GPO[x] selected. 0: ICSS_PORT[y].GPO[x] is de-selected Reset Source: mod_g_rst_n

3.19.17 CFG0_ICLXBAR5_G0 Registers

3.19.17.1 CFG0_G0 Register (Offset = 240h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2323. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4240h

Figure 3-1093. ICLXBAR5_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR5_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR5_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2324. ICLXBAR5_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR5_G0_SEL	R/W	0h	ICL XBar5 G0 input bit select. Input source is PWMA hr select 1: PWMA hr bit[x] selected 0: PWMA hr bit[x] is de-selected Reset Source: mod_g_rst_n

3.19.18 CFG0_ICLXBAR5_G1 Registers

3.19.18.1 CFG0_G1 Register (Offset = 244h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2325. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4244h

Figure 3-1094. ICLXBAR5_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR5_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR5_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2326. ICLXBAR5_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR5_G1_SEL	R/W	0h	ICL XBar5 G1 input bit select. Input source is PWMB hr select 1: PWMB hr bit[x] selected 0: PWMB hr bit[x] is de-selected Reset Source: mod_g_rst_n

3.19.19 CFG0_ICLXBAR5_G2 Registers

3.19.19.1 CFG0_G2 Register (Offset = 248h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2327. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4248h

Figure 3-1095. ICLXBAR5_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR5_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR5_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2328. ICLXBAR5_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR5_G2_SEL	R/W	0h	ICL XBar5 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1: ICSS_PORT[y].GPO[x] selected. 0: ICSS_PORT[y].GPO[x] is de-selected Reset Source: mod_g_rst_n

3.19.20 CFG0_ICLXBAR6_G0 Registers

3.19.20.1 CFG0_G0 Register (Offset = 280h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2329. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4280h

Figure 3-1096. ICLXBAR6_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR6_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR6_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2330. ICLXBAR6_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR6_G0_SEL	R/W	0h	ICL XBar6 G0 input bit select. Input source is PWMA hr select 1: PWMA hr bit[x] selected 0: PWMA hr bit[x] is de-selected Reset Source: mod_g_rst_n

3.19.21 CFG0_ICLXBAR6_G1 Registers

3.19.21.1 CFG0_G1 Register (Offset = 284h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2331. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4284h

Figure 3-1097. ICLXBAR6_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR6_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR6_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2332. ICLXBAR6_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR6_G1_SEL	R/W	0h	ICL XBar6 G1 input bit select. Input source is PWMB hr select 1: PWMB hr bit[x] selected 0: PWMB hr bit[x] is de-selected Reset Source: mod_g_rst_n

3.19.22 CFG0_ICLXBAR6_G2 Registers

3.19.22.1 CFG0_G2 Register (Offset = 288h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2333. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4288h

Figure 3-1098. ICLXBAR6_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR6_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR6_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2334. ICLXBAR6_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR6_G2_SEL	R/W	0h	ICL XBar6 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1: ICSS_PORT[y].GPO[x] selected. 0: ICSS_PORT[y].GPO[x] is de-selected Reset Source: mod_g_rst_n

3.19.23 CFG0_ICLXBAR7_G0 Registers

3.19.23.1 CFG0_G0 Register (Offset = 2C0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2335. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 42C0h

Figure 3-1099. ICLXBAR7_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR7_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR7_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2336. ICLXBAR7_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR7_G0_SEL	R/W	0h	ICL XBar7 G0 input bit select. Input source is PWMA hr select 1: PWMA hr bit[x] selected 0: PWMA hr bit[x] is de-selected Reset Source: mod_g_rst_n

3.19.24 CFG0_ICLXBAR7_G1 Registers

3.19.24.1 CFG0_G1 Register (Offset = 2C4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2337. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 42C4h

Figure 3-1100. ICLXBAR7_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR7_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR7_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2338. ICLXBAR7_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR7_G1_SEL	R/W	0h	ICL XBar7 G1 input bit select. Input source is PWMB hr select 1: PWMB hr bit[x] selected 0: PWMB hr bit[x] is de-selected Reset Source: mod_g_rst_n

3.19.25 CFG0_ICLXBAR7_G2 Registers

3.19.25.1 CFG0_G2 Register (Offset = 2C8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2339. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 42C8h

Figure 3-1101. ICLXBAR7_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR7_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR7_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2340. ICLXBAR7_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR7_G2_SEL	R/W	0h	ICL XBar7 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1: ICSS_PORT[y].GPO[x] selected. 0: ICSS_PORT[y].GPO[x] is de-selected Reset Source: mod_g_rst_n

3.19.26 CFG0_ICLXBAR8_G0 Registers

3.19.26.1 CFG0_G0 Register (Offset = 300h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2341. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4300h

Figure 3-1102. ICLXBAR8_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR8_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR8_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2342. ICLXBAR8_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR8_G0_SEL	R/W	0h	ICL XBar8 G0 input bit select. Input source is PWMA hr select 1: PWMA hr bit[x] selected 0: PWMA hr bit[x] is de-selected Reset Source: mod_g_rst_n

3.19.27 CFG0_ICLXBAR8_G1 Registers

3.19.27.1 CFG0_G1 Register (Offset = 304h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2343. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4304h

Figure 3-1103. ICLXBAR8_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR8_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR8_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2344. ICLXBAR8_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR8_G1_SEL	R/W	0h	ICL XBar8 G1 input bit select. Input source is PWMB hr select 1: PWMB hr bit[x] selected 0: PWMB hr bit[x] is de-selected Reset Source: mod_g_rst_n

3.19.28 CFG0_ICLXBAR8_G2 Registers

3.19.28.1 CFG0_G2 Register (Offset = 308h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2345. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4308h

Figure 3-1104. ICLXBAR8_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR8_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR8_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2346. ICLXBAR8_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR8_G2_SEL	R/W	0h	ICL XBar8 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1: ICSS_PORT[y].GPO[x] selected. 0: ICSS_PORT[y].GPO[x] is de-selected Reset Source: mod_g_rst_n

3.19.29 CFG0_ICLXBAR9_G0 Registers

3.19.29.1 CFG0_G0 Register (Offset = 340h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2347. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4340h

Figure 3-1105. ICLXBAR9_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR9_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR9_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2348. ICLXBAR9_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR9_G0_SEL	R/W	0h	ICL XBar9 G0 input bit select. Input source is PWMA hr select 1: PWMA hr bit[x] selected 0: PWMA hr bit[x] is de-selected Reset Source: mod_g_rst_n

3.19.30 CFG0_ICLXBAR9_G1 Registers

3.19.30.1 CFG0_G1 Register (Offset = 344h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2349. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4344h

Figure 3-1106. ICLXBAR9_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR9_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR9_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2350. ICLXBAR9_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR9_G1_SEL	R/W	0h	ICL XBar9 G1 input bit select. Input source is PWMB hr select 1: PWMB hr bit[x] selected 0: PWMB hr bit[x] is de-selected Reset Source: mod_g_rst_n

3.19.31 CFG0_ICLXBAR9_G2 Registers

3.19.31.1 CFG0_G2 Register (Offset = 348h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2351. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4348h

Figure 3-1107. ICLXBAR9_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR9_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR9_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2352. ICLXBAR9_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR9_G2_SEL	R/W	0h	ICL XBar9 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1: ICSS_PORT[y].GPO[x] selected. 0: ICSS_PORT[y].GPO[x] is de-selected Reset Source: mod_g_rst_n

3.19.32 CFG0_ICLXBAR10_G0 Registers

3.19.32.1 CFG0_G0 Register (Offset = 380h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2353. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4380h

Figure 3-1108. ICLXBAR10_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR10_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR10_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2354. ICLXBAR10_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR10_G0_SEL	R/W	0h	ICL XBar10 G0 input bit select. Input source is PWMA hr select 1: PWMA hr bit[x] selected 0: PWMA hr bit[x] is de-selected Reset Source: mod_g_rst_n

3.19.33 CFG0_ICLXBAR10_G1 Registers

3.19.33.1 CFG0_G1 Register (Offset = 384h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2355. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4384h

Figure 3-1109. ICLXBAR10_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR10_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR10_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2356. ICLXBAR10_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR10_G1_SEL	R/W	0h	ICL XBar10 G1 input bit select. Input source is PWMB hr select 1: PWMB hr bit[x] selected 0: PWMB hr bit[x] is de-selected Reset Source: mod_g_rst_n

3.19.34 CFG0_ICLXBAR10_G2 Registers

3.19.34.1 CFG0_G2 Register (Offset = 388h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2357. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4388h

Figure 3-1110. ICLXBAR10_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR10_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR10_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2358. ICLXBAR10_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR10_G2_SEL	R/W	0h	ICL XBar10 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1: ICSS_PORT[y].GPO[x] selected. 0: ICSS_PORT[y].GPO[x] is de-selected Reset Source: mod_g_rst_n

3.19.35 CFG0_ICLXBAR11_G0 Registers

3.19.35.1 CFG0_G0 Register (Offset = 3C0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2359. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 43C0h

Figure 3-1111. ICLXBAR11_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR11_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR11_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2360. ICLXBAR11_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR11_G0_SEL	R/W	0h	ICL XBar11 G0 input bit select. Input source is PWMA hr select 1: PWMA hr bit[x] selected 0: PWMA hr bit[x] is de-selected Reset Source: mod_g_rst_n

3.19.36 CFG0_ICLXBAR11_G1 Registers

3.19.36.1 CFG0_G1 Register (Offset = 3C4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2361. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 43C4h

Figure 3-1112. ICLXBAR11_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR11_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR11_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2362. ICLXBAR11_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR11_G1_SEL	R/W	0h	ICL XBar11 G1 input bit select. Input source is PWMB hr select 1: PWMB hr bit[x] selected 0: PWMB hr bit[x] is de-selected Reset Source: mod_g_rst_n

3.19.37 CFG0_ICLXBAR11_G2 Registers

3.19.37.1 CFG0_G2 Register (Offset = 3C8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2363. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 43C8h

Figure 3-1113. ICLXBAR11_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR11_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR11_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2364. ICLXBAR11_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR11_G2_SEL	R/W	0h	ICL XBar11 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1: ICSS_PORT[y].GPO[x] selected. 0: ICSS_PORT[y].GPO[x] is de-selected Reset Source: mod_g_rst_n

3.19.38 CFG0_ICLXBAR12_G0 Registers

3.19.38.1 CFG0_G0 Register (Offset = 400h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2365. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4400h

Figure 3-1114. ICLXBAR12_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR12_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR12_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2366. ICLXBAR12_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR12_G0_SEL	R/W	0h	ICL XBar12 G0 input bit select. Input source is PWMA hr select 1: PWMA hr bit[x] selected 0: PWMA hr bit[x] is de-selected Reset Source: mod_g_rst_n

3.19.39 CFG0_ICLXBAR12_G1 Registers

3.19.39.1 CFG0_G1 Register (Offset = 404h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2367. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4404h

Figure 3-1115. ICLXBAR12_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR12_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR12_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2368. ICLXBAR12_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR12_G1_SEL	R/W	0h	ICL XBar12 G1 input bit select. Input source is PWMB hr select 1: PWMB hr bit[x] selected 0: PWMB hr bit[x] is de-selected Reset Source: mod_g_rst_n

3.19.40 CFG0_ICLXBAR12_G2 Registers

3.19.40.1 CFG0_G2 Register (Offset = 408h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2369. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4408h

Figure 3-1116. ICLXBAR12_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR12_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR12_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2370. ICLXBAR12_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR12_G2_SEL	R/W	0h	ICL XBar12 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1: ICSS_PORT[y].GPO[x] selected. 0: ICSS_PORT[y].GPO[x] is de-selected Reset Source: mod_g_rst_n

3.19.41 CFG0_ICLXBAR13_G0 Registers

3.19.41.1 CFG0_G0 Register (Offset = 440h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2371. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4440h

Figure 3-1117. ICLXBAR13_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR13_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR13_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2372. ICLXBAR13_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR13_G0_SEL	R/W	0h	ICL XBar13 G0 input bit select. Input source is PWMA hr select 1: PWMA hr bit[x] selected 0: PWMA hr bit[x] is de-selected Reset Source: mod_g_rst_n

3.19.42 CFG0_ICLXBAR13_G1 Registers

3.19.42.1 CFG0_G1 Register (Offset = 444h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2373. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4444h

Figure 3-1118. ICLXBAR13_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR13_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR13_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2374. ICLXBAR13_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR13_G1_SEL	R/W	0h	ICL XBar13 G1 input bit select. Input source is PWMB hr select 1: PWMB hr bit[x] selected 0: PWMB hr bit[x] is de-selected Reset Source: mod_g_rst_n

3.19.43 CFG0_ICLXBAR13_G2 Registers

3.19.43.1 CFG0_G2 Register (Offset = 448h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2375. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4448h

Figure 3-1119. ICLXBAR13_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR13_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR13_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2376. ICLXBAR13_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR13_G2_SEL	R/W	0h	ICL XBar13 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1: ICSS_PORT[y].GPO[x] selected. 0: ICSS_PORT[y].GPO[x] is de-selected Reset Source: mod_g_rst_n

3.19.44 CFG0_ICLXBAR14_G0 Registers

3.19.44.1 CFG0_G0 Register (Offset = 480h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2377. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4480h

Figure 3-1120. ICLXBAR14_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR14_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR14_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2378. ICLXBAR14_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR14_G0_SEL	R/W	0h	ICL XBar14 G0 input bit select. Input source is PWMA hr select 1: PWMA hr bit[x] selected 0: PWMA hr bit[x] is de-selected Reset Source: mod_g_rst_n

3.19.45 CFG0_ICLXBAR14_G1 Registers

3.19.45.1 CFG0_G1 Register (Offset = 484h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2379. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4484h

Figure 3-1121. ICLXBAR14_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR14_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR14_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2380. ICLXBAR14_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR14_G1_SEL	R/W	0h	ICL XBar14 G1 input bit select. Input source is PWMB hr select 1: PWMB hr bit[x] selected 0: PWMB hr bit[x] is de-selected Reset Source: mod_g_rst_n

3.19.46 CFG0_ICLXBAR14_G2 Registers

3.19.46.1 CFG0_G2 Register (Offset = 488h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2381. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 4488h

Figure 3-1122. ICLXBAR14_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR14_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR14_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2382. ICLXBAR14_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR14_G2_SEL	R/W	0h	ICL XBar14 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1: ICSS_PORT[y].GPO[x] selected. 0: ICSS_PORT[y].GPO[x] is de-selected Reset Source: mod_g_rst_n

3.19.47 CFG0_ICLXBAR15_G0 Registers

3.19.47.1 CFG0_G0 Register (Offset = 4C0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2383. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 44C0h

Figure 3-1123. ICLXBAR15_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR15_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR15_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2384. ICLXBAR15_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR15_G0_SEL	R/W	0h	ICL XBar15 G0 input bit select. Input source is PWMA hr select 1: PWMA hr bit[x] selected 0: PWMA hr bit[x] is de-selected Reset Source: mod_g_rst_n

3.19.48 CFG0_ICLXBAR15_G1 Registers

3.19.48.1 CFG0_G1 Register (Offset = 4C4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2385. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 44C4h

Figure 3-1124. ICLXBAR15_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR15_G1_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR15_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2386. ICLXBAR15_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR15_G1_SEL	R/W	0h	ICL XBar15 G1 input bit select. Input source is PWMB hr select 1: PWMB hr bit[x] selected 0: PWMB hr bit[x] is de-selected Reset Source: mod_g_rst_n

3.19.49 CFG0_ICLXBAR15_G2 Registers

3.19.49.1 CFG0_G2 Register (Offset = 4C8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2387. Instance Table

Instance Name	Physical Address
ICLXBAR_MMR	502D 44C8h

Figure 3-1125. ICLXBAR15_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ICLXBAR15_G2_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICLXBAR15_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2388. ICLXBAR15_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR15_G2_SEL	R/W	0h	ICL XBar15 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1: ICSS_PORT[y].GPO[x] selected. 0: ICSS_PORT[y].GPO[x] is de-selected Reset Source: mod_g_rst_n

3.19.50 Access Table

Table 3-2389. Access Type Codes

Access Type	Code	Description
R	R	Read
R/W	R/W	Read / Write

3.20 PWMSYNCOUTXBAR Registers

Table 3-2390. CFG0, CFG0 Registers, Base Address=0X00000000502D2000, Length=1024

Offset	Length	Register Name	pwmsyncoutxbar_mmr0 Physical Address
0h	32	PID	502D 2000h
100h	32	pwmsyncoutxbar0_g0	502D 2100h
140h	32	pwmsyncoutxbar1_g0	502D 2140h
180h	32	pwmsyncoutxbar2_g0	502D 2180h
1C0h	32	pwmsyncoutxbar3_g0	502D 21C0h

3.20.1 CFG0_PID Registers

3.20.1.1 CFG0_PID Register (Offset = 0h) [reset = 61800215h]

Short Description: PID register

Long Description: PID register

Return to Summary Table

Table 3-2391. Instance Table

Instance Name	Physical Address
PWMSYNCOUTXBAR_MMR0	502D 2000h

Figure 3-1126. PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PID_MSB16															
R															
6180h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_MISC					PID_MAJOR			PID_CUSTOM		PID_MINOR					
R					R			R		R					
0h					2h			0h		15h					

Access Types Legend

Table 3-2392. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR	R	15h	Reset Source: mod_g_rst_n

3.20.2 CFG0_PWMSYNCOUTXBAR0_G0 Registers

3.20.2.1 CFG0_G0 Register (Offset = 100h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2393. Instance Table

Instance Name	Physical Address
PWMSYNCOUTXBAR_MMR0	502D 2100h

Figure 3-1127. PWMSYNCOUTXBAR0_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMSYNCOUTXBAR0_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMSYNCOUTXBAR0_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2394. PWMSYNCOUTXBAR0_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMSYNCOUTXBAR0_G0_SEL	R/W	0h	ETPWM pwmsyncout xbar0 select 1: PWM[x] SYNCOUT selected 0: PWM[x] SYNCOUT is de-selected Reset Source: mod_g_rst_n

3.20.3 CFG0_PWMSYNCOUTXBAR1_G0 Registers

3.20.3.1 CFG0_G0 Register (Offset = 140h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2395. Instance Table

Instance Name	Physical Address
PWMSYNCOUTXBAR_MMR0	502D 2140h

Figure 3-1128. PWMSYNCOUTXBAR1_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMSYNCOUTXBAR1_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMSYNCOUTXBAR1_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2396. PWMSYNCOUTXBAR1_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMSYNCOUTXBAR1_G0_SEL	R/W	0h	ETPWM pwmsyncout xbar1 select 1: PWM[x] SYNCOUT selected 0: PWM[x] SYNCOUT is de-selected Reset Source: mod_g_rst_n

3.20.4 CFG0_PWMSYNCOUTXBAR2_G0 Registers

3.20.4.1 CFG0_G0 Register (Offset = 180h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2397. Instance Table

Instance Name	Physical Address
PWMSYNCOUTXBAR_MMR0	502D 2180h

Figure 3-1129. PWMSYNCOUTXBAR2_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMSYNCOUTXBAR2_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMSYNCOUTXBAR2_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2398. PWMSYNCOUTXBAR2_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMSYNCOUTXBAR2_G0_SEL	R/W	0h	ETPWM pwmsyncout xbar2 select 1: PWM[x] SYNCOUT selected 0: PWM[x] SYNCOUT is de-selected Reset Source: mod_g_rst_n

3.20.5 CFG0_PWMSYNCOUTXBAR3_G0 Registers

3.20.5.1 CFG0_G0 Register (Offset = 1C0h) [reset = 0h]

Short Description:

Long Description:

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Table 3-2399. Instance Table

Instance Name	Physical Address
PWMSYNCOUTXBAR_MMR0	502D 21C0h

Figure 3-1130. PWMSYNCOUTXBAR3_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMSYNCOUTXBAR3_G0_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMSYNCOUTXBAR3_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2400. PWMSYNCOUTXBAR3_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMSYNCOUTXBAR3_G0_SEL	R/W	0h	ETPWM pwmsyncout xbar3 select 1: PWM[x] SYNCOUT selected 0: PWM[x] SYNCOUT is de-selected Reset Source: mod_g_rst_n

3.20.6 Access Table

Table 3-2401. Access Type Codes

Access Type	Code	Description
R	R	Read
R/W	R/W	Read / Write

3.21 PWMXBAR Registers

Table 3-2402. CFG0, CFG0 Registers, Base Address=0X00000000502D1000, Length=4096

Offset	Length	Register Name	pwmxbar_mmr0 Physical Address
0h	32	PID	502D 1000h
10h	32	PWMXBar_Status	502D 1010h
14h	32	PWMXBar_FlagInvert	502D 1014h
18h	32	PWMXBar_Flag	502D 1018h
1Ch	32	PWMXBar_Flag_CLR	502D 101Ch
100h	32	PWMXBar0_G0	502D 1100h
104h	32	PWMXBar0_G1	502D 1104h
108h	32	PWMXBar0_G2	502D 1108h
10Ch	32	PWMXBar0_G3	502D 110Ch
110h	32	PWMXBar0_G4	502D 1110h
114h	32	PWMXBar0_G5	502D 1114h
118h	32	PWMXBar0_G6	502D 1118h
11Ch	32	PWMXBar0_G7	502D 111Ch
120h	32	PWMXBar0_G8	502D 1120h
140h	32	PWMXBar1_G0	502D 1140h
144h	32	PWMXBar1_G1	502D 1144h
148h	32	PWMXBar1_G2	502D 1148h
14Ch	32	PWMXBar1_G3	502D 114Ch
150h	32	PWMXBar1_G4	502D 1150h
154h	32	PWMXBar1_G5	502D 1154h
158h	32	PWMXBar1_G6	502D 1158h
15Ch	32	PWMXBar1_G7	502D 115Ch
160h	32	PWMXBar1_G8	502D 1160h
180h	32	PWMXBar2_G0	502D 1180h
184h	32	PWMXBar2_G1	502D 1184h
188h	32	PWMXBar2_G2	502D 1188h
18Ch	32	PWMXBar2_G3	502D 118Ch
190h	32	PWMXBar2_G4	502D 1190h
194h	32	PWMXBar2_G5	502D 1194h
198h	32	PWMXBar2_G6	502D 1198h
19Ch	32	PWMXBar2_G7	502D 119Ch
1A0h	32	PWMXBar2_G8	502D 11A0h
1C0h	32	PWMXBar3_G0	502D 11C0h
1C4h	32	PWMXBar3_G1	502D 11C4h
1C8h	32	PWMXBar3_G2	502D 11C8h
1CCh	32	PWMXBar3_G3	502D 11CCh
1D0h	32	PWMXBar3_G4	502D 11D0h
1D4h	32	PWMXBar3_G5	502D 11D4h
1D8h	32	PWMXBar3_G6	502D 11D8h
1DCh	32	PWMXBar3_G7	502D 11DCh
1E0h	32	PWMXBar3_G8	502D 11E0h
200h	32	PWMXBar4_G0	502D 1200h
204h	32	PWMXBar4_G1	502D 1204h
208h	32	PWMXBar4_G2	502D 1208h
20Ch	32	PWMXBar4_G3	502D 120Ch

Table 3-2402. CFG0, CFG0 Registers, Base Address=0X00000000502D1000, Length=4096 (continued)

Offset	Length	Register Name	pwmxbar_mmr0 Physical Address
210h	32	PWMXBar4_G4	502D 1210h
214h	32	PWMXBar4_G5	502D 1214h
218h	32	PWMXBar4_G6	502D 1218h
21Ch	32	PWMXBar4_G7	502D 121Ch
220h	32	PWMXBar4_G8	502D 1220h
240h	32	PWMXBar5_G0	502D 1240h
244h	32	PWMXBar5_G1	502D 1244h
248h	32	PWMXBar5_G2	502D 1248h
24Ch	32	PWMXBar5_G3	502D 124Ch
250h	32	PWMXBar5_G4	502D 1250h
254h	32	PWMXBar5_G5	502D 1254h
258h	32	PWMXBar5_G6	502D 1258h
25Ch	32	PWMXBar5_G7	502D 125Ch
260h	32	PWMXBar5_G8	502D 1260h
280h	32	PWMXBar6_G0	502D 1280h
284h	32	PWMXBar6_G1	502D 1284h
288h	32	PWMXBar6_G2	502D 1288h
28Ch	32	PWMXBar6_G3	502D 128Ch
290h	32	PWMXBar6_G4	502D 1290h
294h	32	PWMXBar6_G5	502D 1294h
298h	32	PWMXBar6_G6	502D 1298h
29Ch	32	PWMXBar6_G7	502D 129Ch
2A0h	32	PWMXBar6_G8	502D 12A0h
2C0h	32	PWMXBar7_G0	502D 12C0h
2C4h	32	PWMXBar7_G1	502D 12C4h
2C8h	32	PWMXBar7_G2	502D 12C8h
2CCh	32	PWMXBar7_G3	502D 12CCh
2D0h	32	PWMXBar7_G4	502D 12D0h
2D4h	32	PWMXBar7_G5	502D 12D4h
2D8h	32	PWMXBar7_G6	502D 12D8h
2DCh	32	PWMXBar7_G7	502D 12DCh
2E0h	32	PWMXBar7_G8	502D 12E0h
300h	32	PWMXBar8_G0	502D 1300h
304h	32	PWMXBar8_G1	502D 1304h
308h	32	PWMXBar8_G2	502D 1308h
30Ch	32	PWMXBar8_G3	502D 130Ch
310h	32	PWMXBar8_G4	502D 1310h
314h	32	PWMXBar8_G5	502D 1314h
318h	32	PWMXBar8_G6	502D 1318h
31Ch	32	PWMXBar8_G7	502D 131Ch
320h	32	PWMXBar8_G8	502D 1320h
340h	32	PWMXBar9_G0	502D 1340h
344h	32	PWMXBar9_G1	502D 1344h
348h	32	PWMXBar9_G2	502D 1348h
34Ch	32	PWMXBar9_G3	502D 134Ch
350h	32	PWMXBar9_G4	502D 1350h
354h	32	PWMXBar9_G5	502D 1354h

Table 3-2402. CFG0, CFG0 Registers, Base Address=0X00000000502D1000, Length=4096 (continued)

Offset	Length	Register Name	pwmxbar_mmr0 Physical Address
358h	32	PWMXBar9_G6	502D 1358h
35Ch	32	PWMXBar9_G7	502D 135Ch
360h	32	PWMXBar9_G8	502D 1360h
380h	32	PWMXBar10_G0	502D 1380h
384h	32	PWMXBar10_G1	502D 1384h
388h	32	PWMXBar10_G2	502D 1388h
38Ch	32	PWMXBar10_G3	502D 138Ch
390h	32	PWMXBar10_G4	502D 1390h
394h	32	PWMXBar10_G5	502D 1394h
398h	32	PWMXBar10_G6	502D 1398h
39Ch	32	PWMXBar10_G7	502D 139Ch
3A0h	32	PWMXBar10_G8	502D 13A0h
3C0h	32	PWMXBar11_G0	502D 13C0h
3C4h	32	PWMXBar11_G1	502D 13C4h
3C8h	32	PWMXBar11_G2	502D 13C8h
3CCh	32	PWMXBar11_G3	502D 13CCh
3D0h	32	PWMXBar11_G4	502D 13D0h
3D4h	32	PWMXBar11_G5	502D 13D4h
3D8h	32	PWMXBar11_G6	502D 13D8h
3DCh	32	PWMXBar11_G7	502D 13DCh
3E0h	32	PWMXBar11_G8	502D 13E0h
400h	32	PWMXBar12_G0	502D 1400h
404h	32	PWMXBar12_G1	502D 1404h
408h	32	PWMXBar12_G2	502D 1408h
40Ch	32	PWMXBar12_G3	502D 140Ch
410h	32	PWMXBar12_G4	502D 1410h
414h	32	PWMXBar12_G5	502D 1414h
418h	32	PWMXBar12_G6	502D 1418h
41Ch	32	PWMXBar12_G7	502D 141Ch
420h	32	PWMXBar12_G8	502D 1420h
440h	32	PWMXBar13_G0	502D 1440h
444h	32	PWMXBar13_G1	502D 1444h
448h	32	PWMXBar13_G2	502D 1448h
44Ch	32	PWMXBar13_G3	502D 144Ch
450h	32	PWMXBar13_G4	502D 1450h
454h	32	PWMXBar13_G5	502D 1454h
458h	32	PWMXBar13_G6	502D 1458h
45Ch	32	PWMXBar13_G7	502D 145Ch
460h	32	PWMXBar13_G8	502D 1460h
480h	32	PWMXBar14_G0	502D 1480h
484h	32	PWMXBar14_G1	502D 1484h
488h	32	PWMXBar14_G2	502D 1488h
48Ch	32	PWMXBar14_G3	502D 148Ch
490h	32	PWMXBar14_G4	502D 1490h
494h	32	PWMXBar14_G5	502D 1494h
498h	32	PWMXBar14_G6	502D 1498h
49Ch	32	PWMXBar14_G7	502D 149Ch

Table 3-2402. CFG0, CFG0 Registers, Base Address=0X00000000502D1000, Length=4096 (continued)

Offset	Length	Register Name	pwmxbar_mmr0 Physical Address
4A0h	32	PWMXBar14_G8	502D 14A0h
4C0h	32	PWMXBar15_G0	502D 14C0h
4C4h	32	PWMXBar15_G1	502D 14C4h
4C8h	32	PWMXBar15_G2	502D 14C8h
4CCh	32	PWMXBar15_G3	502D 14CCh
4D0h	32	PWMXBar15_G4	502D 14D0h
4D4h	32	PWMXBar15_G5	502D 14D4h
4D8h	32	PWMXBar15_G6	502D 14D8h
4DCh	32	PWMXBar15_G7	502D 14DCh
4E0h	32	PWMXBar15_G8	502D 14E0h
500h	32	PWMXBar16_G0	502D 1500h
504h	32	PWMXBar16_G1	502D 1504h
508h	32	PWMXBar16_G2	502D 1508h
50Ch	32	PWMXBar16_G3	502D 150Ch
510h	32	PWMXBar16_G4	502D 1510h
514h	32	PWMXBar16_G5	502D 1514h
518h	32	PWMXBar16_G6	502D 1518h
51Ch	32	PWMXBar16_G7	502D 151Ch
520h	32	PWMXBar16_G8	502D 1520h
540h	32	PWMXBar17_G0	502D 1540h
544h	32	PWMXBar17_G1	502D 1544h
548h	32	PWMXBar17_G2	502D 1548h
54Ch	32	PWMXBar17_G3	502D 154Ch
550h	32	PWMXBar17_G4	502D 1550h
554h	32	PWMXBar17_G5	502D 1554h
558h	32	PWMXBar17_G6	502D 1558h
55Ch	32	PWMXBar17_G7	502D 155Ch
560h	32	PWMXBar17_G8	502D 1560h
580h	32	PWMXBar18_G0	502D 1580h
584h	32	PWMXBar18_G1	502D 1584h
588h	32	PWMXBar18_G2	502D 1588h
58Ch	32	PWMXBar18_G3	502D 158Ch
590h	32	PWMXBar18_G4	502D 1590h
594h	32	PWMXBar18_G5	502D 1594h
598h	32	PWMXBar18_G6	502D 1598h
59Ch	32	PWMXBar18_G7	502D 159Ch
5A0h	32	PWMXBar18_G8	502D 15A0h
5C0h	32	PWMXBar19_G0	502D 15C0h
5C4h	32	PWMXBar19_G1	502D 15C4h
5C8h	32	PWMXBar19_G2	502D 15C8h
5CCh	32	PWMXBar19_G3	502D 15CCh
5D0h	32	PWMXBar19_G4	502D 15D0h
5D4h	32	PWMXBar19_G5	502D 15D4h
5D8h	32	PWMXBar19_G6	502D 15D8h
5DCh	32	PWMXBar19_G7	502D 15DCh
5E0h	32	PWMXBar19_G8	502D 15E0h
600h	32	PWMXBar20_G0	502D 1600h

Table 3-2402. CFG0, CFG0 Registers, Base Address=0X00000000502D1000, Length=4096 (continued)

Offset	Length	Register Name	pwmxbar_mmr0 Physical Address
604h	32	PWMXBar20_G1	502D 1604h
608h	32	PWMXBar20_G2	502D 1608h
60Ch	32	PWMXBar20_G3	502D 160Ch
610h	32	PWMXBar20_G4	502D 1610h
614h	32	PWMXBar20_G5	502D 1614h
618h	32	PWMXBar20_G6	502D 1618h
61Ch	32	PWMXBar20_G7	502D 161Ch
620h	32	PWMXBar20_G8	502D 1620h
640h	32	PWMXBar21_G0	502D 1640h
644h	32	PWMXBar21_G1	502D 1644h
648h	32	PWMXBar21_G2	502D 1648h
64Ch	32	PWMXBar21_G3	502D 164Ch
650h	32	PWMXBar21_G4	502D 1650h
654h	32	PWMXBar21_G5	502D 1654h
658h	32	PWMXBar21_G6	502D 1658h
65Ch	32	PWMXBar21_G7	502D 165Ch
660h	32	PWMXBar21_G8	502D 1660h
680h	32	PWMXBar22_G0	502D 1680h
684h	32	PWMXBar22_G1	502D 1684h
688h	32	PWMXBar22_G2	502D 1688h
68Ch	32	PWMXBar22_G3	502D 168Ch
690h	32	PWMXBar22_G4	502D 1690h
694h	32	PWMXBar22_G5	502D 1694h
698h	32	PWMXBar22_G6	502D 1698h
69Ch	32	PWMXBar22_G7	502D 169Ch
6A0h	32	PWMXBar22_G8	502D 16A0h
6C0h	32	PWMXBar23_G0	502D 16C0h
6C4h	32	PWMXBar23_G1	502D 16C4h
6C8h	32	PWMXBar23_G2	502D 16C8h
6CCh	32	PWMXBar23_G3	502D 16CCh
6D0h	32	PWMXBar23_G4	502D 16D0h
6D4h	32	PWMXBar23_G5	502D 16D4h
6D8h	32	PWMXBar23_G6	502D 16D8h
6DCh	32	PWMXBar23_G7	502D 16DCh
6E0h	32	PWMXBar23_G8	502D 16E0h
700h	32	PWMXBar24_G0	502D 1700h
704h	32	PWMXBar24_G1	502D 1704h
708h	32	PWMXBar24_G2	502D 1708h
70Ch	32	PWMXBar24_G3	502D 170Ch
710h	32	PWMXBar24_G4	502D 1710h
714h	32	PWMXBar24_G5	502D 1714h
718h	32	PWMXBar24_G6	502D 1718h
71Ch	32	PWMXBar24_G7	502D 171Ch
720h	32	PWMXBar24_G8	502D 1720h
740h	32	PWMXBar25_G0	502D 1740h
744h	32	PWMXBar25_G1	502D 1744h
748h	32	PWMXBar25_G2	502D 1748h

Table 3-2402. CFG0, CFG0 Registers, Base Address=0X00000000502D1000, Length=4096 (continued)

Offset	Length	Register Name	pwmxbar_mmr0 Physical Address
74Ch	32	PWMXBar25_G3	502D 174Ch
750h	32	PWMXBar25_G4	502D 1750h
754h	32	PWMXBar25_G5	502D 1754h
758h	32	PWMXBar25_G6	502D 1758h
75Ch	32	PWMXBar25_G7	502D 175Ch
760h	32	PWMXBar25_G8	502D 1760h
780h	32	PWMXBar26_G0	502D 1780h
784h	32	PWMXBar26_G1	502D 1784h
788h	32	PWMXBar26_G2	502D 1788h
78Ch	32	PWMXBar26_G3	502D 178Ch
790h	32	PWMXBar26_G4	502D 1790h
794h	32	PWMXBar26_G5	502D 1794h
798h	32	PWMXBar26_G6	502D 1798h
79Ch	32	PWMXBar26_G7	502D 179Ch
7A0h	32	PWMXBar26_G8	502D 17A0h
7C0h	32	PWMXBar27_G0	502D 17C0h
7C4h	32	PWMXBar27_G1	502D 17C4h
7C8h	32	PWMXBar27_G2	502D 17C8h
7CCh	32	PWMXBar27_G3	502D 17CCh
7D0h	32	PWMXBar27_G4	502D 17D0h
7D4h	32	PWMXBar27_G5	502D 17D4h
7D8h	32	PWMXBar27_G6	502D 17D8h
7DCh	32	PWMXBar27_G7	502D 17DCh
7E0h	32	PWMXBar27_G8	502D 17E0h
800h	32	PWMXBar28_G0	502D 1800h
804h	32	PWMXBar28_G1	502D 1804h
808h	32	PWMXBar28_G2	502D 1808h
80Ch	32	PWMXBar28_G3	502D 180Ch
810h	32	PWMXBar28_G4	502D 1810h
814h	32	PWMXBar28_G5	502D 1814h
818h	32	PWMXBar28_G6	502D 1818h
81Ch	32	PWMXBar28_G7	502D 181Ch
820h	32	PWMXBar28_G8	502D 1820h
840h	32	PWMXBar29_G0	502D 1840h
844h	32	PWMXBar29_G1	502D 1844h
848h	32	PWMXBar29_G2	502D 1848h
84Ch	32	PWMXBar29_G3	502D 184Ch
850h	32	PWMXBar29_G4	502D 1850h
854h	32	PWMXBar29_G5	502D 1854h
858h	32	PWMXBar29_G6	502D 1858h
85Ch	32	PWMXBar29_G7	502D 185Ch
860h	32	PWMXBar29_G8	502D 1860h

3.21.1 CFG0_PID Registers

3.21.1.1 CFG0_PID Register (Offset = 0h) [reset = 61800215h]

Short Description: PID register

Long Description: PID register

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Table 3-2403. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1000h

Figure 3-1131. PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PID_MSB16															
R															
6180h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_MISC					PID_MAJOR			PID_CUSTOM		PID_MINOR					
R					R			R		R					
0h					2h			0h		15h					

Access Types Legend

Table 3-2404. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PID_MSB16	R	6180h	Reset Source: mod_g_rst_n
15:11	PID_MISC	R	0h	Reset Source: mod_g_rst_n
10:8	PID_MAJOR	R	2h	Reset Source: mod_g_rst_n
7:6	PID_CUSTOM	R	0h	Reset Source: mod_g_rst_n
5:0	PID_MINOR	R	15h	Reset Source: mod_g_rst_n

3.21.2 CFG0_PWMXBAR_STATUS Registers

3.21.2.1 CFG0_STATUS Register (Offset = 10h) [reset = 0h]

Short Description:

Long Description:

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Table 3-2405. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1010h

Figure 3-1132. PWMXBAR_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		PWMXBAR_STATUS_STS													
NONE		R													
0		0h													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR_STATUS_STS															
R															
0h															

Access Types Legend

Table 3-2406. PWMXBAR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE		Reserved
29:0	PWMXBAR_STATUS_STS	R	0h	Output Signal Status Reset Source: mod_g_rst_n

3.21.3 CFG0_PWMXBAR_FLAGINVERT Registers

3.21.3.1 CFG0_FLAGINVERT Register (Offset = 14h) [reset = 0h]

Short Description:

Long Description:

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Table 3-2407. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1014h

Figure 3-1133. PWMXBAR_FLAGINVERT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		PWMXBAR_FLAGINVERT_INVERT													
NONE		R/W													
0		0h													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR_FLAGINVERT_INVERT															
R/W															
0h															

Access Types Legend

Table 3-2408. PWMXBAR_FLAGINVERT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE		Reserved
29:0	PWMXBAR_FLAGINVERT_INVERT	R/W	0h	Output Signal Invert Before Latch Reset Source: mod_g_rst_n

3.21.4 CFG0_PWMXBAR_FLAG Registers

3.21.4.1 CFG0_FLAG Register (Offset = 18h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2409. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1018h

Figure 3-1134. PWMXBAR_FLAG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		PWMXBAR_FLAG_BIT29	PWMXBAR_FLAG_BIT28	PWMXBAR_FLAG_BIT27	PWMXBAR_FLAG_BIT26	PWMXBAR_FLAG_BIT25	PWMXBAR_FLAG_BIT24	PWMXBAR_FLAG_BIT23	PWMXBAR_FLAG_BIT22	PWMXBAR_FLAG_BIT21	PWMXBAR_FLAG_BIT20	PWMXBAR_FLAG_BIT19	PWMXBAR_FLAG_BIT18	PWMXBAR_FLAG_BIT17	PWMXBAR_FLAG_BIT16
NONE		R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0		0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR_FLAG_BIT15	PWMXBAR_FLAG_BIT14	PWMXBAR_FLAG_BIT13	PWMXBAR_FLAG_BIT12	PWMXBAR_FLAG_BIT11	PWMXBAR_FLAG_BIT10	PWMXBAR_FLAG_BIT9	PWMXBAR_FLAG_BIT8	PWMXBAR_FLAG_BIT7	PWMXBAR_FLAG_BIT6	PWMXBAR_FLAG_BIT5	PWMXBAR_FLAG_BIT4	PWMXBAR_FLAG_BIT3	PWMXBAR_FLAG_BIT2	PWMXBAR_FLAG_BIT1	PWMXBAR_FLAG_BIT0
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 3-2410. PWMXBAR_FLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE		Reserved
29	PWMXBAR_FLAG_BIT29	R/W1TC	0h	Output Signal Latched Flag Reset Source: pwmxbar_flag_clr_n_29
28	PWMXBAR_FLAG_BIT28	R/W1TC	0h	Output Signal Latched Flag Reset Source: pwmxbar_flag_clr_n_28
27	PWMXBAR_FLAG_BIT27	R/W1TC	0h	Output Signal Latched Flag Reset Source: pwmxbar_flag_clr_n_27
26	PWMXBAR_FLAG_BIT26	R/W1TC	0h	Output Signal Latched Flag Reset Source: pwmxbar_flag_clr_n_26
25	PWMXBAR_FLAG_BIT25	R/W1TC	0h	Output Signal Latched Flag Reset Source: pwmxbar_flag_clr_n_25
24	PWMXBAR_FLAG_BIT24	R/W1TC	0h	Output Signal Latched Flag Reset Source: pwmxbar_flag_clr_n_24
23	PWMXBAR_FLAG_BIT23	R/W1TC	0h	Output Signal Latched Flag Reset Source: pwmxbar_flag_clr_n_23
22	PWMXBAR_FLAG_BIT22	R/W1TC	0h	Output Signal Latched Flag Reset Source: pwmxbar_flag_clr_n_22
21	PWMXBAR_FLAG_BIT21	R/W1TC	0h	Output Signal Latched Flag Reset Source: pwmxbar_flag_clr_n_21
20	PWMXBAR_FLAG_BIT20	R/W1TC	0h	Output Signal Latched Flag Reset Source: pwmxbar_flag_clr_n_20
19	PWMXBAR_FLAG_BIT19	R/W1TC	0h	Output Signal Latched Flag Reset Source: pwmxbar_flag_clr_n_19
18	PWMXBAR_FLAG_BIT18	R/W1TC	0h	Output Signal Latched Flag Reset Source: pwmxbar_flag_clr_n_18
17	PWMXBAR_FLAG_BIT17	R/W1TC	0h	Output Signal Latched Flag Reset Source: pwmxbar_flag_clr_n_17
16	PWMXBAR_FLAG_BIT16	R/W1TC	0h	Output Signal Latched Flag Reset Source: pwmxbar_flag_clr_n_16
15	PWMXBAR_FLAG_BIT15	R/W1TC	0h	Output Signal Latched Flag Reset Source: pwmxbar_flag_clr_n_15
14	PWMXBAR_FLAG_BIT14	R/W1TC	0h	Output Signal Latched Flag Reset Source: pwmxbar_flag_clr_n_14
13	PWMXBAR_FLAG_BIT13	R/W1TC	0h	Output Signal Latched Flag Reset Source: pwmxbar_flag_clr_n_13
12	PWMXBAR_FLAG_BIT12	R/W1TC	0h	Output Signal Latched Flag Reset Source: pwmxbar_flag_clr_n_12

Table 3-2410. PWMXBAR_FLAG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	PWMXBAR_FLAG_BIT11	R/W1TC	0h	Output Signal Latched Flag Reset Source: pwmxbar_flag_clr_n_11
10	PWMXBAR_FLAG_BIT10	R/W1TC	0h	Output Signal Latched Flag Reset Source: pwmxbar_flag_clr_n_10
9	PWMXBAR_FLAG_BIT9	R/W1TC	0h	Output Signal Latched Flag Reset Source: pwmxbar_flag_clr_n_9
8	PWMXBAR_FLAG_BIT8	R/W1TC	0h	Output Signal Latched Flag Reset Source: pwmxbar_flag_clr_n_8
7	PWMXBAR_FLAG_BIT7	R/W1TC	0h	Output Signal Latched Flag Reset Source: pwmxbar_flag_clr_n_7
6	PWMXBAR_FLAG_BIT6	R/W1TC	0h	Output Signal Latched Flag Reset Source: pwmxbar_flag_clr_n_6
5	PWMXBAR_FLAG_BIT5	R/W1TC	0h	Output Signal Latched Flag Reset Source: pwmxbar_flag_clr_n_5
4	PWMXBAR_FLAG_BIT4	R/W1TC	0h	Output Signal Latched Flag Reset Source: pwmxbar_flag_clr_n_4
3	PWMXBAR_FLAG_BIT3	R/W1TC	0h	Output Signal Latched Flag Reset Source: pwmxbar_flag_clr_n_3
2	PWMXBAR_FLAG_BIT2	R/W1TC	0h	Output Signal Latched Flag Reset Source: pwmxbar_flag_clr_n_2
1	PWMXBAR_FLAG_BIT1	R/W1TC	0h	Output Signal Latched Flag Reset Source: pwmxbar_flag_clr_n_1
0	PWMXBAR_FLAG_BIT0	R/W1TC	0h	Output Signal Latched Flag Reset Source: pwmxbar_flag_clr_n_0

3.21.5 CFG0_PWMXBAR_FLAG_CLR Registers

3.21.5.1 CFG0_FLAG_CLR Register (Offset = 1Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2411. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 101Ch

Figure 3-1135. PWMXBAR_FLAG_CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		PWMXBAR_FLAG_CLR_BIT29	PWMXBAR_FLAG_CLR_BIT28	PWMXBAR_FLAG_CLR_BIT27	PWMXBAR_FLAG_CLR_BIT26	PWMXBAR_FLAG_CLR_BIT25	PWMXBAR_FLAG_CLR_BIT24	PWMXBAR_FLAG_CLR_BIT23	PWMXBAR_FLAG_CLR_BIT22	PWMXBAR_FLAG_CLR_BIT21	PWMXBAR_FLAG_CLR_BIT20	PWMXBAR_FLAG_CLR_BIT19	PWMXBAR_FLAG_CLR_BIT18	PWMXBAR_FLAG_CLR_BIT17	PWMXBAR_FLAG_CLR_BIT16
NONE		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0		0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR_FLAG_CLR_BIT15	PWMXBAR_FLAG_CLR_BIT14	PWMXBAR_FLAG_CLR_BIT13	PWMXBAR_FLAG_CLR_BIT12	PWMXBAR_FLAG_CLR_BIT11	PWMXBAR_FLAG_CLR_BIT10	PWMXBAR_FLAG_CLR_BIT9	PWMXBAR_FLAG_CLR_BIT8	PWMXBAR_FLAG_CLR_BIT7	PWMXBAR_FLAG_CLR_BIT6	PWMXBAR_FLAG_CLR_BIT5	PWMXBAR_FLAG_CLR_BIT4	PWMXBAR_FLAG_CLR_BIT3	PWMXBAR_FLAG_CLR_BIT2	PWMXBAR_FLAG_CLR_BIT1	PWMXBAR_FLAG_CLR_BIT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 3-2412. PWMXBAR_FLAG_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE		Reserved
29	PWMXBAR_FLAG_CLR_BIT29	R/W	0h	Output Signal Latched Flag Clear Reset Source: mod_g_rst_n
28	PWMXBAR_FLAG_CLR_BIT28	R/W	0h	Output Signal Latched Flag Clear Reset Source: mod_g_rst_n
27	PWMXBAR_FLAG_CLR_BIT27	R/W	0h	Output Signal Latched Flag Clear Reset Source: mod_g_rst_n
26	PWMXBAR_FLAG_CLR_BIT26	R/W	0h	Output Signal Latched Flag Clear Reset Source: mod_g_rst_n
25	PWMXBAR_FLAG_CLR_BIT25	R/W	0h	Output Signal Latched Flag Clear Reset Source: mod_g_rst_n
24	PWMXBAR_FLAG_CLR_BIT24	R/W	0h	Output Signal Latched Flag Clear Reset Source: mod_g_rst_n
23	PWMXBAR_FLAG_CLR_BIT23	R/W	0h	Output Signal Latched Flag Clear Reset Source: mod_g_rst_n
22	PWMXBAR_FLAG_CLR_BIT22	R/W	0h	Output Signal Latched Flag Clear Reset Source: mod_g_rst_n
21	PWMXBAR_FLAG_CLR_BIT21	R/W	0h	Output Signal Latched Flag Clear Reset Source: mod_g_rst_n
20	PWMXBAR_FLAG_CLR_BIT20	R/W	0h	Output Signal Latched Flag Clear Reset Source: mod_g_rst_n

Table 3-2412. PWMXBAR_FLAG_CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	PWMXBAR_FLAG_CLR_BIT19	R/W	0h	Output Signal Latched Flag Clear Reset Source: mod_g_rst_n
18	PWMXBAR_FLAG_CLR_BIT18	R/W	0h	Output Signal Latched Flag Clear Reset Source: mod_g_rst_n
17	PWMXBAR_FLAG_CLR_BIT17	R/W	0h	Output Signal Latched Flag Clear Reset Source: mod_g_rst_n
16	PWMXBAR_FLAG_CLR_BIT16	R/W	0h	Output Signal Latched Flag Clear Reset Source: mod_g_rst_n
15	PWMXBAR_FLAG_CLR_BIT15	R/W	0h	Output Signal Latched Flag Clear Reset Source: mod_g_rst_n
14	PWMXBAR_FLAG_CLR_BIT14	R/W	0h	Output Signal Latched Flag Clear Reset Source: mod_g_rst_n
13	PWMXBAR_FLAG_CLR_BIT13	R/W	0h	Output Signal Latched Flag Clear Reset Source: mod_g_rst_n
12	PWMXBAR_FLAG_CLR_BIT12	R/W	0h	Output Signal Latched Flag Clear Reset Source: mod_g_rst_n
11	PWMXBAR_FLAG_CLR_BIT11	R/W	0h	Output Signal Latched Flag Clear Reset Source: mod_g_rst_n
10	PWMXBAR_FLAG_CLR_BIT10	R/W	0h	Output Signal Latched Flag Clear Reset Source: mod_g_rst_n
9	PWMXBAR_FLAG_CLR_BIT9	R/W	0h	Output Signal Latched Flag Clear Reset Source: mod_g_rst_n
8	PWMXBAR_FLAG_CLR_BIT8	R/W	0h	Output Signal Latched Flag Clear Reset Source: mod_g_rst_n
7	PWMXBAR_FLAG_CLR_BIT7	R/W	0h	Output Signal Latched Flag Clear Reset Source: mod_g_rst_n
6	PWMXBAR_FLAG_CLR_BIT6	R/W	0h	Output Signal Latched Flag Clear Reset Source: mod_g_rst_n
5	PWMXBAR_FLAG_CLR_BIT5	R/W	0h	Output Signal Latched Flag Clear Reset Source: mod_g_rst_n
4	PWMXBAR_FLAG_CLR_BIT4	R/W	0h	Output Signal Latched Flag Clear Reset Source: mod_g_rst_n
3	PWMXBAR_FLAG_CLR_BIT3	R/W	0h	Output Signal Latched Flag Clear Reset Source: mod_g_rst_n
2	PWMXBAR_FLAG_CLR_BIT2	R/W	0h	Output Signal Latched Flag Clear Reset Source: mod_g_rst_n
1	PWMXBAR_FLAG_CLR_BIT1	R/W	0h	Output Signal Latched Flag Clear Reset Source: mod_g_rst_n
0	PWMXBAR_FLAG_CLR_BIT0	R/W	0h	Output Signal Latched Flag Clear Reset Source: mod_g_rst_n

3.21.6 CFG0_PWMXBAR0_G0 Registers

3.21.6.1 CFG0_G0 Register (Offset = 100h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2413. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1100h

Figure 3-1136. PWMXBAR0_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR0_G0_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR0_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2414. PWMXBAR0_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR0_G0_SEL	R/W	0h	PWM XBar0 G0 Input Select 0: CMP12SS0.CTRIPL 1: CMP12SS0.CTRIPH 2: CMP12SS1.CTRIPL 3: CMP12SS1.CTRIPH 4: CMP12SS2.CTRIPL 5: CMP12SS2.CTRIPH 6: CMP12SS3.CTRIPL 7: CMP12SS3.CTRIPH 8: CMP12SS4.CTRIPL 9: CMP12SS4.CTRIPH 10: CMP12SS5.CTRIPL 11: CMP12SS5.CTRIPH 12: CMP12SS6.CTRIPL 13: CMP12SS6.CTRIPH 14: CMP12SS7.CTRIPL 15: CMP12SS7.CTRIPH 16: CMP12SS8.CTRIPL 17: CMP12SS8.CTRIPH 18: CMP12SS9.CTRIPL 19: CMP12SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.7 CFG0_PWMXBAR0_G1 Registers

3.21.7.1 CFG0_G1 Register (Offset = 104h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2415. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1104h

Figure 3-1137. PWMXBAR0_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR0_G1_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR0_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2416. PWMXBAR0_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR0_G1_SEL	R/W	0h	PWM XBar0 G1 Input Select 0: CMP8SS0.CTRIPL 1: CMP8SS0.CTRIPH 2: CMP8SS1.CTRIPL 3: CMP8SS1.CTRIPH 4: CMP8SS2.CTRIPL 5: CMP8SS2.CTRIPH 6: CMP8SS3.CTRIPL 7: CMP8SS3.CTRIPH 8: CMP8SS4.CTRIPL 9: CMP8SS4.CTRIPH 10: CMP8SS5.CTRIPL 11: CMP8SS5.CTRIPH 12: CMP8SS6.CTRIPL 13: CMP8SS6.CTRIPH 14: CMP8SS7.CTRIPL 15: CMP8SS7.CTRIPH 16: CMP8SS8.CTRIPL 17: CMP8SS8.CTRIPH 18: CMP8SS9.CTRIPL 19: CMP8SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.8 CFG0_PWMXBAR0_G2 Registers

3.21.8.1 CFG0_G2 Register (Offset = 108h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2417. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1108h

Figure 3-1138. PWMXBAR0_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PWMXBAR0_G2_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR0_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2418. PWMXBAR0_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	PWMXBAR0_G2_SEL	R/W	0h	PWM XBar0 G2 Input Select 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.21.9 CFG0_PWMXBAR0_G3 Registers

3.21.9.1 CFG0_G3 Register (Offset = 10Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2419. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 110Ch

Figure 3-1139. PWMXBAR0_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR0_G3_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR0_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2420. PWMXBAR0_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR0_G3_SEL	R/W	0h	PWM XBar0 G3 Input Select 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1.EVT4 8: ADC2.EVT1 9: ADC2.EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.21.10 CFG0_PWMXBAR0_G4 Registers

3.21.10.1 CFG0_G4 Register (Offset = 110h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2421. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1110h

Figure 3-1140. PWMXBAR0_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR0_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR0_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2422. PWMXBAR0_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR0_G4_SEL	R/W	0h	PWM XBar0 G4 input bit select. Input source is INPUT XBAR. 1: INPUT XBAR output bit[x] selected 0: INPUT XBAR output bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.11 CFG0_PWMXBAR0_G5 Registers

3.21.11.1 CFG0_G5 Register (Offset = 114h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2423. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1114h

Figure 3-1141. PWMXBAR0_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR0_G5_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR0_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2424. PWMXBAR0_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR0_G5_SEL	R/W	0h	PWM XBar0 G5 input bit select. Input source is PWM TRIPOUT. 1: PWM TRIPOUT bit[x] selected 0: PWM TRIPOUT bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.12 CFG0_PWMXBAR0_G6 Registers

3.21.12.1 CFG0_G6 Register (Offset = 118h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2425. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1118h

Figure 3-1142. PWMXBAR0_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR0_G6_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR0_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2426. PWMXBAR0_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR0_G6_SEL	R/W	0h	PWM XBar0 G6 input bit select. Input source is PWM DEL TRIP 1: PWM DEL TRIP bit[x] selected 0: PWM DEL TRIP bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.13 CFG0_PWMXBAR0_G7 Registers

3.21.13.1 CFG0_G7 Register (Offset = 11Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2427. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 111Ch

Figure 3-1143. PWMXBAR0_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR0_G7_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR0_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2428. PWMXBAR0_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR0_G7_SEL	R/W	0h	PWM XBar0 G7 input bit select. Input source is PWM DEL ACTIVE 1: PWM DEL ACTIVE bit[x] selected 0: PWM DEL ACTIVE bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.14 CFG0_PWMXBAR0_G8 Registers

3.21.14.1 CFG0_G8 Register (Offset = 120h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2429. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1120h

Figure 3-1144. PWMXBAR0_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PWMXBAR0_G8_SEL												
NONE			R/W												
0			0h												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR0_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2430. PWMXBAR0_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:0	PWMXBAR0_G8_SEL	R/W	0h	PWM XBar0 G8 Input Select 0: EQEP0.ERR 1: EQEP1.ERR 2: EQEP2.ERR 6:3: FSIRX0.RX_TRIG4 10:7: FSIRX1.RX_TRIG4 14:11: FSIRX2.RX_TRIG4 18:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT Reset Source: mod_g_rst_n

3.21.15 CFG0_PWMXBAR1_G0 Registers

3.21.15.1 CFG0_G0 Register (Offset = 140h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2431. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1140h

Figure 3-1145. PWMXBAR1_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR1_G0_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR1_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2432. PWMXBAR1_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR1_G0_SEL	R/W	0h	PWM XBar1 G0 Input Select 0: CMP12SS0.CTRIPL 1: CMP12SS0.CTRIPH 2: CMP12SS1.CTRIPL 3: CMP12SS1.CTRIPH 4: CMP12SS2.CTRIPL 5: CMP12SS2.CTRIPH 6: CMP12SS3.CTRIPL 7: CMP12SS3.CTRIPH 8: CMP12SS4.CTRIPL 9: CMP12SS4.CTRIPH 10: CMP12SS5.CTRIPL 11: CMP12SS5.CTRIPH 12: CMP12SS6.CTRIPL 13: CMP12SS6.CTRIPH 14: CMP12SS7.CTRIPL 15: CMP12SS7.CTRIPH 16: CMP12SS8.CTRIPL 17: CMP12SS8.CTRIPH 18: CMP12SS9.CTRIPL 19: CMP12SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.16 CFG0_PWMXBAR1_G1 Registers

3.21.16.1 CFG0_G1 Register (Offset = 144h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2433. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1144h

Figure 3-1146. PWMXBAR1_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR1_G1_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR1_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2434. PWMXBAR1_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR1_G1_SEL	R/W	0h	PWM XBar1 G1 Input Select 0: CMP8SS0.CTRIPL 1: CMP8SS0.CTRIPH 2: CMP8SS1.CTRIPL 3: CMP8SS1.CTRIPH 4: CMP8SS2.CTRIPL 5: CMP8SS2.CTRIPH 6: CMP8SS3.CTRIPL 7: CMP8SS3.CTRIPH 8: CMP8SS4.CTRIPL 9: CMP8SS4.CTRIPH 10: CMP8SS5.CTRIPL 11: CMP8SS5.CTRIPH 12: CMP8SS6.CTRIPL 13: CMP8SS6.CTRIPH 14: CMP8SS7.CTRIPL 15: CMP8SS7.CTRIPH 16: CMP8SS8.CTRIPL 17: CMP8SS8.CTRIPH 18: CMP8SS9.CTRIPL 19: CMP8SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.17 CFG0_PWMXBAR1_G2 Registers

3.21.17.1 CFG0_G2 Register (Offset = 148h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2435. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1148h

Figure 3-1147. PWMXBAR1_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PWMXBAR1_G2_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR1_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2436. PWMXBAR1_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	PWMXBAR1_G2_SEL	R/W	0h	PWM XBar1 G2 Input Select 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.21.18 CFG0_PWMXBAR1_G3 Registers

3.21.18.1 CFG0_G3 Register (Offset = 14Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2437. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 114Ch

Figure 3-1148. PWMXBAR1_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR1_G3_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR1_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2438. PWMXBAR1_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR1_G3_SEL	R/W	0h	PWM XBar1 G3 Input Select 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1.EVT4 8: ADC2.EVT1 9: ADC2.EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.21.19 CFG0_PWMXBAR1_G4 Registers

3.21.19.1 CFG0_G4 Register (Offset = 150h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2439. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1150h

Figure 3-1149. PWMXBAR1_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR1_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR1_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2440. PWMXBAR1_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR1_G4_SEL	R/W	0h	PWM XBar1 G4 input bit select. Input source is INPUT XBAR. 1: INPUT XBAR output bit[x] selected 0: INPUT XBAR output bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.20 CFG0_PWMXBAR1_G5 Registers

3.21.20.1 CFG0_G5 Register (Offset = 154h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2441. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1154h

Figure 3-1150. PWMXBAR1_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR1_G5_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR1_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2442. PWMXBAR1_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR1_G5_SEL	R/W	0h	PWM XBar1 G5 input bit select. Input source is PWM TRIPOUT. 1: PWM TRIPOUT bit[x] selected 0: PWM TRIPOUT bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.21 CFG0_PWMXBAR1_G6 Registers

3.21.21.1 CFG0_G6 Register (Offset = 158h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2443. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1158h

Figure 3-1151. PWMXBAR1_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR1_G6_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR1_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2444. PWMXBAR1_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR1_G6_SEL	R/W	0h	PWM XBar1 G6 input bit select. Input source is PWM DEL TRIP 1: PWM DEL TRIP bit[x] selected 0: PWM DEL TRIP bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.22 CFG0_PWMXBAR1_G7 Registers

3.21.22.1 CFG0_G7 Register (Offset = 15Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2445. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 115Ch

Figure 3-1152. PWMXBAR1_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR1_G7_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR1_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2446. PWMXBAR1_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR1_G7_SEL	R/W	0h	PWM XBar1 G7 input bit select. Input source is PWM DEL ACTIVE 1: PWM DEL ACTIVE bit[x] selected 0: PWM DEL ACTIVE bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.23 CFG0_PWMXBAR1_G8 Registers

3.21.23.1 CFG0_G8 Register (Offset = 160h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2447. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1160h

Figure 3-1153. PWMXBAR1_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PWMXBAR1_G8_SEL												
NONE			R/W												
0			0h												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR1_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2448. PWMXBAR1_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:0	PWMXBAR1_G8_SEL	R/W	0h	PWM XBar1 G8 Input Select 0: EQEP0.ERR 1: EQEP1.ERR 2: EQEP2.ERR 6:3: FSIRX0.RX_TRIG4 10:7: FSIRX1.RX_TRIG4 14:11: FSIRX2.RX_TRIG4 18:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT Reset Source: mod_g_rst_n

3.21.24 CFG0_PWMXBAR2_G0 Registers

3.21.24.1 CFG0_G0 Register (Offset = 180h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2449. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1180h

Figure 3-1154. PWMXBAR2_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR2_G0_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR2_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2450. PWMXBAR2_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR2_G0_SEL	R/W	0h	PWM XBar2 G0 Input Select 0: CMP12SS0.CTRIPL 1: CMP12SS0.CTRIPH 2: CMP12SS1.CTRIPL 3: CMP12SS1.CTRIPH 4: CMP12SS2.CTRIPL 5: CMP12SS2.CTRIPH 6: CMP12SS3.CTRIPL 7: CMP12SS3.CTRIPH 8: CMP12SS4.CTRIPL 9: CMP12SS4.CTRIPH 10: CMP12SS5.CTRIPL 11: CMP12SS5.CTRIPH 12: CMP12SS6.CTRIPL 13: CMP12SS6.CTRIPH 14: CMP12SS7.CTRIPL 15: CMP12SS7.CTRIPH 16: CMP12SS8.CTRIPL 17: CMP12SS8.CTRIPH 18: CMP12SS9.CTRIPL 19: CMP12SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.25 CFG0_PWMXBAR2_G1 Registers

3.21.25.1 CFG0_G1 Register (Offset = 184h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2451. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1184h

Figure 3-1155. PWMXBAR2_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR2_G1_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR2_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2452. PWMXBAR2_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR2_G1_SEL	R/W	0h	PWM XBar2 G1 Input Select 0: CMP8SS0.CTRIPL 1: CMP8SS0.CTRIPH 2: CMP8SS1.CTRIPL 3: CMP8SS1.CTRIPH 4: CMP8SS2.CTRIPL 5: CMP8SS2.CTRIPH 6: CMP8SS3.CTRIPL 7: CMP8SS3.CTRIPH 8: CMP8SS4.CTRIPL 9: CMP8SS4.CTRIPH 10: CMP8SS5.CTRIPL 11: CMP8SS5.CTRIPH 12: CMP8SS6.CTRIPL 13: CMP8SS6.CTRIPH 14: CMP8SS7.CTRIPL 15: CMP8SS7.CTRIPH 16: CMP8SS8.CTRIPL 17: CMP8SS8.CTRIPH 18: CMP8SS9.CTRIPL 19: CMP8SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.26 CFG0_PWMXBAR2_G2 Registers

3.21.26.1 CFG0_G2 Register (Offset = 188h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2453. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1188h

Figure 3-1156. PWMXBAR2_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PWMXBAR2_G2_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR2_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2454. PWMXBAR2_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	PWMXBAR2_G2_SEL	R/W	0h	PWM XBar2 G2 Input Select 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.21.27 CFG0_PWMXBAR2_G3 Registers

3.21.27.1 CFG0_G3 Register (Offset = 18Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2455. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 118Ch

Figure 3-1157. PWMXBAR2_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR2_G3_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR2_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2456. PWMXBAR2_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR2_G3_SEL	R/W	0h	PWM XBar2 G3 Input Select 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1.EVT4 8: ADC2.EVT1 9: ADC2.EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.21.28 CFG0_PWMXBAR2_G4 Registers

3.21.28.1 CFG0_G4 Register (Offset = 190h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2457. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1190h

Figure 3-1158. PWMXBAR2_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR2_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR2_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2458. PWMXBAR2_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR2_G4_SEL	R/W	0h	PWM XBar2 G4 input bit select. Input source is INPUT XBAR. 1: INPUT XBAR output bit[x] selected 0: INPUT XBAR output bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.29 CFG0_PWMXBAR2_G5 Registers

3.21.29.1 CFG0_G5 Register (Offset = 194h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2459. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1194h

Figure 3-1159. PWMXBAR2_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR2_G5_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR2_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2460. PWMXBAR2_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR2_G5_SEL	R/W	0h	PWM XBar2 G5 input bit select. Input source is PWM TRIPOUT. 1: PWM TRIPOUT bit[x] selected 0: PWM TRIPOUT bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.30 CFG0_PWMXBAR2_G6 Registers

3.21.30.1 CFG0_G6 Register (Offset = 198h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2461. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1198h

Figure 3-1160. PWMXBAR2_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR2_G6_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR2_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2462. PWMXBAR2_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR2_G6_SEL	R/W	0h	PWM XBar2 G6 input bit select. Input source is PWM DEL TRIP 1: PWM DEL TRIP bit[x] selected 0: PWM DEL TRIP bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.31 CFG0_PWMXBAR2_G7 Registers

3.21.31.1 CFG0_G7 Register (Offset = 19Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2463. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 119Ch

Figure 3-1161. PWMXBAR2_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR2_G7_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR2_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2464. PWMXBAR2_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR2_G7_SEL	R/W	0h	PWM XBar2 G7 input bit select. Input source is PWM DEL ACTIVE 1: PWM DEL ACTIVE bit[x] selected 0: PWM DEL ACTIVE bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.32 CFG0_PWMXBAR2_G8 Registers

3.21.32.1 CFG0_G8 Register (Offset = 1A0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2465. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 11A0h

Figure 3-1162. PWMXBAR2_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PWMXBAR2_G8_SEL												
NONE			R/W												
0			0h												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR2_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2466. PWMXBAR2_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:0	PWMXBAR2_G8_SEL	R/W	0h	PWM XBar2 G8 Input Select 0: EQEP0.ERR 1: EQEP1.ERR 2: EQEP2.ERR 6:3: FSIRX0.RX_TRIG4 10:7: FSIRX1.RX_TRIG4 14:11: FSIRX2.RX_TRIG4 18:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT Reset Source: mod_g_rst_n

3.21.33 CFG0_PWMXBAR3_G0 Registers

3.21.33.1 CFG0_G0 Register (Offset = 1C0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2467. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 11C0h

Figure 3-1163. PWMXBAR3_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR3_G0_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR3_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2468. PWMXBAR3_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR3_G0_SEL	R/W	0h	PWM XBar3 G0 Input Select 0: CMP12SS0.CTRIPL 1: CMP12SS0.CTRIPH 2: CMP12SS1.CTRIPL 3: CMP12SS1.CTRIPH 4: CMP12SS2.CTRIPL 5: CMP12SS2.CTRIPH 6: CMP12SS3.CTRIPL 7: CMP12SS3.CTRIPH 8: CMP12SS4.CTRIPL 9: CMP12SS4.CTRIPH 10: CMP12SS5.CTRIPL 11: CMP12SS5.CTRIPH 12: CMP12SS6.CTRIPL 13: CMP12SS6.CTRIPH 14: CMP12SS7.CTRIPL 15: CMP12SS7.CTRIPH 16: CMP12SS8.CTRIPL 17: CMP12SS8.CTRIPH 18: CMP12SS9.CTRIPL 19: CMP12SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.34 CFG0_PWMXBAR3_G1 Registers

3.21.34.1 CFG0_G1 Register (Offset = 1C4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2469. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 11C4h

Figure 3-1164. PWMXBAR3_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR3_G1_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR3_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2470. PWMXBAR3_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR3_G1_SEL	R/W	0h	PWM XBar3 G1 Input Select 0: CMP8SS0.CTRIPL 1: CMP8SS0.CTRIPH 2: CMP8SS1.CTRIPL 3: CMP8SS1.CTRIPH 4: CMP8SS2.CTRIPL 5: CMP8SS2.CTRIPH 6: CMP8SS3.CTRIPL 7: CMP8SS3.CTRIPH 8: CMP8SS4.CTRIPL 9: CMP8SS4.CTRIPH 10: CMP8SS5.CTRIPL 11: CMP8SS5.CTRIPH 12: CMP8SS6.CTRIPL 13: CMP8SS6.CTRIPH 14: CMP8SS7.CTRIPL 15: CMP8SS7.CTRIPH 16: CMP8SS8.CTRIPL 17: CMP8SS8.CTRIPH 18: CMP8SS9.CTRIPL 19: CMP8SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.35 CFG0_PWMXBAR3_G2 Registers

3.21.35.1 CFG0_G2 Register (Offset = 1C8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2471. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 11C8h

Figure 3-1165. PWMXBAR3_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PWMXBAR3_G2_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR3_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2472. PWMXBAR3_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	PWMXBAR3_G2_SEL	R/W	0h	PWM XBar3 G2 Input Select 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.21.36 CFG0_PWMXBAR3_G3 Registers

3.21.36.1 CFG0_G3 Register (Offset = 1CCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2473. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 11CCh

Figure 3-1166. PWMXBAR3_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR3_G3_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR3_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2474. PWMXBAR3_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR3_G3_SEL	R/W	0h	PWM XBar3 G3 Input Select 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1.EVT4 8: ADC2.EVT1 9: ADC2.EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.21.37 CFG0_PWMXBAR3_G4 Registers

3.21.37.1 CFG0_G4 Register (Offset = 1D0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2475. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 11D0h

Figure 3-1167. PWMXBAR3_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR3_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR3_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2476. PWMXBAR3_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR3_G4_SEL	R/W	0h	PWM XBar3 G4 input bit select. Input source is INPUT XBAR. 1: INPUT XBAR output bit[x] selected 0: INPUT XBAR output bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.38 CFG0_PWMXBAR3_G5 Registers

3.21.38.1 CFG0_G5 Register (Offset = 1D4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2477. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 11D4h

Figure 3-1168. PWMXBAR3_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR3_G5_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR3_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2478. PWMXBAR3_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR3_G5_SEL	R/W	0h	PWM XBar3 G5 input bit select. Input source is PWM TRIPOUT. 1: PWM TRIPOUT bit[x] selected 0: PWM TRIPOUT bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.39 CFG0_PWMXBAR3_G6 Registers

3.21.39.1 CFG0_G6 Register (Offset = 1D8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2479. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 11D8h

Figure 3-1169. PWMXBAR3_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR3_G6_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR3_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2480. PWMXBAR3_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR3_G6_SEL	R/W	0h	PWM XBar3 G6 input bit select. Input source is PWM DEL TRIP 1: PWM DEL TRIP bit[x] selected 0: PWM DEL TRIP bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.40 CFG0_PWMXBAR3_G7 Registers

3.21.40.1 CFG0_G7 Register (Offset = 1DCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2481. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 11DCh

Figure 3-1170. PWMXBAR3_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR3_G7_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR3_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2482. PWMXBAR3_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR3_G7_SEL	R/W	0h	PWM XBar3 G7 input bit select. Input source is PWM DEL ACTIVE 1: PWM DEL ACTIVE bit[x] selected 0: PWM DEL ACTIVE bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.41 CFG0_PWMXBAR3_G8 Registers

3.21.41.1 CFG0_G8 Register (Offset = 1E0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2483. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 11E0h

Figure 3-1171. PWMXBAR3_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PWMXBAR3_G8_SEL												
NONE			R/W												
0			0h												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR3_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2484. PWMXBAR3_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:0	PWMXBAR3_G8_SEL	R/W	0h	PWM XBar3 G8 Input Select 0: EQEP0.ERR 1: EQEP1.ERR 2: EQEP2.ERR 6:3: FSIRX0.RX_TRIG4 10:7: FSIRX1.RX_TRIG4 14:11: FSIRX2.RX_TRIG4 18:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT Reset Source: mod_g_rst_n

3.21.42 CFG0_PWMXBAR4_G0 Registers

3.21.42.1 CFG0_G0 Register (Offset = 200h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2485. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1200h

Figure 3-1172. PWMXBAR4_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR4_G0_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR4_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2486. PWMXBAR4_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR4_G0_SEL	R/W	0h	PWM XBar4 G0 Input Select 0: CMP12SS0.CTRIPL 1: CMP12SS0.CTRIPH 2: CMP12SS1.CTRIPL 3: CMP12SS1.CTRIPH 4: CMP12SS2.CTRIPL 5: CMP12SS2.CTRIPH 6: CMP12SS3.CTRIPL 7: CMP12SS3.CTRIPH 8: CMP12SS4.CTRIPL 9: CMP12SS4.CTRIPH 10: CMP12SS5.CTRIPL 11: CMP12SS5.CTRIPH 12: CMP12SS6.CTRIPL 13: CMP12SS6.CTRIPH 14: CMP12SS7.CTRIPL 15: CMP12SS7.CTRIPH 16: CMP12SS8.CTRIPL 17: CMP12SS8.CTRIPH 18: CMP12SS9.CTRIPL 19: CMP12SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.43 CFG0_PWMXBAR4_G1 Registers

3.21.43.1 CFG0_G1 Register (Offset = 204h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2487. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1204h

Figure 3-1173. PWMXBAR4_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR4_G1_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR4_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2488. PWMXBAR4_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR4_G1_SEL	R/W	0h	PWM XBar4 G1 Input Select 0: CMP8SS0.CTRIPL 1: CMP8SS0.CTRIPH 2: CMP8SS1.CTRIPL 3: CMP8SS1.CTRIPH 4: CMP8SS2.CTRIPL 5: CMP8SS2.CTRIPH 6: CMP8SS3.CTRIPL 7: CMP8SS3.CTRIPH 8: CMP8SS4.CTRIPL 9: CMP8SS4.CTRIPH 10: CMP8SS5.CTRIPL 11: CMP8SS5.CTRIPH 12: CMP8SS6.CTRIPL 13: CMP8SS6.CTRIPH 14: CMP8SS7.CTRIPL 15: CMP8SS7.CTRIPH 16: CMP8SS8.CTRIPL 17: CMP8SS8.CTRIPH 18: CMP8SS9.CTRIPL 19: CMP8SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.44 CFG0_PWMXBAR4_G2 Registers

3.21.44.1 CFG0_G2 Register (Offset = 208h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2489. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1208h

Figure 3-1174. PWMXBAR4_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PWMXBAR4_G2_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR4_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2490. PWMXBAR4_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	PWMXBAR4_G2_SEL	R/W	0h	PWM XBar4 G2 Input Select 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.21.45 CFG0_PWMXBAR4_G3 Registers

3.21.45.1 CFG0_G3 Register (Offset = 20Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2491. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 120Ch

Figure 3-1175. PWMXBAR4_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR4_G3_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR4_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2492. PWMXBAR4_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR4_G3_SEL	R/W	0h	PWM XBar4 G3 Input Select 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1.EVT4 8: ADC2.EVT1 9: ADC2.EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.21.46 CFG0_PWMXBAR4_G4 Registers

3.21.46.1 CFG0_G4 Register (Offset = 210h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2493. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1210h

Figure 3-1176. PWMXBAR4_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR4_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR4_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2494. PWMXBAR4_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR4_G4_SEL	R/W	0h	PWM XBar4 G4 input bit select. Input source is INPUT XBAR. 1: INPUT XBAR output bit[x] selected 0: INPUT XBAR output bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.47 CFG0_PWMXBAR4_G5 Registers

3.21.47.1 CFG0_G5 Register (Offset = 214h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2495. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1214h

Figure 3-1177. PWMXBAR4_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR4_G5_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR4_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2496. PWMXBAR4_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR4_G5_SEL	R/W	0h	PWM XBar4 G5 input bit select. Input source is PWM TRIPOUT. 1: PWM TRIPOUT bit[x] selected 0: PWM TRIPOUT bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.48 CFG0_PWMXBAR4_G6 Registers

3.21.48.1 CFG0_G6 Register (Offset = 218h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2497. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1218h

Figure 3-1178. PWMXBAR4_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR4_G6_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR4_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2498. PWMXBAR4_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR4_G6_SEL	R/W	0h	PWM XBar4 G6 input bit select. Input source is PWM DEL TRIP 1: PWM DEL TRIP bit[x] selected 0: PWM DEL TRIP bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.49 CFG0_PWMXBAR4_G7 Registers

3.21.49.1 CFG0_G7 Register (Offset = 21Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2499. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 121Ch

Figure 3-1179. PWMXBAR4_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR4_G7_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR4_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2500. PWMXBAR4_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR4_G7_SEL	R/W	0h	PWM XBar4 G7 input bit select. Input source is PWM DEL ACTIVE 1: PWM DEL ACTIVE bit[x] selected 0: PWM DEL ACTIVE bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.50 CFG0_PWMXBAR4_G8 Registers

3.21.50.1 CFG0_G8 Register (Offset = 220h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2501. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1220h

Figure 3-1180. PWMXBAR4_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PWMXBAR4_G8_SEL												
NONE			R/W												
0			0h												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR4_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2502. PWMXBAR4_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:0	PWMXBAR4_G8_SEL	R/W	0h	PWM XBar4 G8 Input Select 0: EQEP0.ERR 1: EQEP1.ERR 2: EQEP2.ERR 6:3: FSIRX0.RX_TRIG4 10:7: FSIRX1.RX_TRIG4 14:11: FSIRX2.RX_TRIG4 18:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT Reset Source: mod_g_rst_n

3.21.51 CFG0_PWMXBAR5_G0 Registers

3.21.51.1 CFG0_G0 Register (Offset = 240h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2503. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1240h

Figure 3-1181. PWMXBAR5_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR5_G0_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR5_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2504. PWMXBAR5_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR5_G0_SEL	R/W	0h	PWM XBar5 G0 Input Select 0: CMP12SS0.CTRIPL 1: CMP12SS0.CTRIPH 2: CMP12SS1.CTRIPL 3: CMP12SS1.CTRIPH 4: CMP12SS2.CTRIPL 5: CMP12SS2.CTRIPH 6: CMP12SS3.CTRIPL 7: CMP12SS3.CTRIPH 8: CMP12SS4.CTRIPL 9: CMP12SS4.CTRIPH 10: CMP12SS5.CTRIPL 11: CMP12SS5.CTRIPH 12: CMP12SS6.CTRIPL 13: CMP12SS6.CTRIPH 14: CMP12SS7.CTRIPL 15: CMP12SS7.CTRIPH 16: CMP12SS8.CTRIPL 17: CMP12SS8.CTRIPH 18: CMP12SS9.CTRIPL 19: CMP12SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.52 CFG0_PWMXBAR5_G1 Registers

3.21.52.1 CFG0_G1 Register (Offset = 244h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2505. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1244h

Figure 3-1182. PWMXBAR5_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR5_G1_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR5_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2506. PWMXBAR5_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR5_G1_SEL	R/W	0h	PWM XBar5 G1 Input Select 0: CMP8SS0.CTRIPL 1: CMP8SS0.CTRIPH 2: CMP8SS1.CTRIPL 3: CMP8SS1.CTRIPH 4: CMP8SS2.CTRIPL 5: CMP8SS2.CTRIPH 6: CMP8SS3.CTRIPL 7: CMP8SS3.CTRIPH 8: CMP8SS4.CTRIPL 9: CMP8SS4.CTRIPH 10: CMP8SS5.CTRIPL 11: CMP8SS5.CTRIPH 12: CMP8SS6.CTRIPL 13: CMP8SS6.CTRIPH 14: CMP8SS7.CTRIPL 15: CMP8SS7.CTRIPH 16: CMP8SS8.CTRIPL 17: CMP8SS8.CTRIPH 18: CMP8SS9.CTRIPL 19: CMP8SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.53 CFG0_PWMXBAR5_G2 Registers

3.21.53.1 CFG0_G2 Register (Offset = 248h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2507. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1248h

Figure 3-1183. PWMXBAR5_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PWMXBAR5_G2_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR5_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2508. PWMXBAR5_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	PWMXBAR5_G2_SEL	R/W	0h	PWM XBar5 G2 Input Select 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.21.54 CFG0_PWMXBAR5_G3 Registers

3.21.54.1 CFG0_G3 Register (Offset = 24Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2509. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 124Ch

Figure 3-1184. PWMXBAR5_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR5_G3_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR5_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2510. PWMXBAR5_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR5_G3_SEL	R/W	0h	PWM XBar5 G3 Input Select 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1.EVT4 8: ADC2.EVT1 9: ADC2.EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.21.55 CFG0_PWMXBAR5_G4 Registers

3.21.55.1 CFG0_G4 Register (Offset = 250h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2511. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1250h

Figure 3-1185. PWMXBAR5_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR5_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR5_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2512. PWMXBAR5_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR5_G4_SEL	R/W	0h	PWM XBar5 G4 input bit select. Input source is INPUT XBAR. 1: INPUT XBAR output bit[x] selected 0: INPUT XBAR output bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.56 CFG0_PWMXBAR5_G5 Registers

3.21.56.1 CFG0_G5 Register (Offset = 254h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2513. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1254h

Figure 3-1186. PWMXBAR5_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR5_G5_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR5_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2514. PWMXBAR5_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR5_G5_SEL	R/W	0h	PWM XBar5 G5 input bit select. Input source is PWM TRIPOUT. 1: PWM TRIPOUT bit[x] selected 0: PWM TRIPOUT bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.57 CFG0_PWMXBAR5_G6 Registers

3.21.57.1 CFG0_G6 Register (Offset = 258h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2515. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1258h

Figure 3-1187. PWMXBAR5_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR5_G6_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR5_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2516. PWMXBAR5_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR5_G6_SEL	R/W	0h	PWM XBar5 G6 input bit select. Input source is PWM DEL TRIP 1: PWM DEL TRIP bit[x] selected 0: PWM DEL TRIP bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.58 CFG0_PWMXBAR5_G7 Registers

3.21.58.1 CFG0_G7 Register (Offset = 25Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2517. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 125Ch

Figure 3-1188. PWMXBAR5_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR5_G7_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR5_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2518. PWMXBAR5_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR5_G7_SEL	R/W	0h	PWM XBar5 G7 input bit select. Input source is PWM DEL ACTIVE 1: PWM DEL ACTIVE bit[x] selected 0: PWM DEL ACTIVE bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.59 CFG0_PWMXBAR5_G8 Registers

3.21.59.1 CFG0_G8 Register (Offset = 260h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2519. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1260h

Figure 3-1189. PWMXBAR5_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PWMXBAR5_G8_SEL												
NONE			R/W												
0			0h												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR5_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2520. PWMXBAR5_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:0	PWMXBAR5_G8_SEL	R/W	0h	PWM XBar5 G8 Input Select 0: EQEP0.ERR 1: EQEP1.ERR 2: EQEP2.ERR 6:3: FSIRX0.RX_TRIG4 10:7: FSIRX1.RX_TRIG4 14:11: FSIRX2.RX_TRIG4 18:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT Reset Source: mod_g_rst_n

3.21.60 CFG0_PWMXBAR6_G0 Registers

3.21.60.1 CFG0_G0 Register (Offset = 280h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2521. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1280h

Figure 3-1190. PWMXBAR6_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR6_G0_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR6_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2522. PWMXBAR6_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR6_G0_SEL	R/W	0h	PWM XBar6 G0 Input Select 0: CMP12SS0.CTRIPL 1: CMP12SS0.CTRIPH 2: CMP12SS1.CTRIPL 3: CMP12SS1.CTRIPH 4: CMP12SS2.CTRIPL 5: CMP12SS2.CTRIPH 6: CMP12SS3.CTRIPL 7: CMP12SS3.CTRIPH 8: CMP12SS4.CTRIPL 9: CMP12SS4.CTRIPH 10: CMP12SS5.CTRIPL 11: CMP12SS5.CTRIPH 12: CMP12SS6.CTRIPL 13: CMP12SS6.CTRIPH 14: CMP12SS7.CTRIPL 15: CMP12SS7.CTRIPH 16: CMP12SS8.CTRIPL 17: CMP12SS8.CTRIPH 18: CMP12SS9.CTRIPL 19: CMP12SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.61 CFG0_PWMXBAR6_G1 Registers

3.21.61.1 CFG0_G1 Register (Offset = 284h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2523. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1284h

Figure 3-1191. PWMXBAR6_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR6_G1_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR6_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2524. PWMXBAR6_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR6_G1_SEL	R/W	0h	PWM XBar6 G1 Input Select 0: CMP8SS0.CTRIPL 1: CMP8SS0.CTRIPH 2: CMP8SS1.CTRIPL 3: CMP8SS1.CTRIPH 4: CMP8SS2.CTRIPL 5: CMP8SS2.CTRIPH 6: CMP8SS3.CTRIPL 7: CMP8SS3.CTRIPH 8: CMP8SS4.CTRIPL 9: CMP8SS4.CTRIPH 10: CMP8SS5.CTRIPL 11: CMP8SS5.CTRIPH 12: CMP8SS6.CTRIPL 13: CMP8SS6.CTRIPH 14: CMP8SS7.CTRIPL 15: CMP8SS7.CTRIPH 16: CMP8SS8.CTRIPL 17: CMP8SS8.CTRIPH 18: CMP8SS9.CTRIPL 19: CMP8SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.62 CFG0_PWMXBAR6_G2 Registers

3.21.62.1 CFG0_G2 Register (Offset = 288h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2525. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1288h

Figure 3-1192. PWMXBAR6_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PWMXBAR6_G2_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR6_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2526. PWMXBAR6_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	PWMXBAR6_G2_SEL	R/W	0h	PWM XBar6 G2 Input Select 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.21.63 CFG0_PWMXBAR6_G3 Registers

3.21.63.1 CFG0_G3 Register (Offset = 28Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2527. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 128Ch

Figure 3-1193. PWMXBAR6_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR6_G3_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR6_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2528. PWMXBAR6_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR6_G3_SEL	R/W	0h	PWM XBar6 G3 Input Select 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1.EVT4 8: ADC2.EVT1 9: ADC2.EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.21.64 CFG0_PWMXBAR6_G4 Registers

3.21.64.1 CFG0_G4 Register (Offset = 290h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2529. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1290h

Figure 3-1194. PWMXBAR6_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR6_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR6_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2530. PWMXBAR6_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR6_G4_SEL	R/W	0h	PWM XBar6 G4 input bit select. Input source is INPUT XBAR. 1: INPUT XBAR output bit[x] selected 0: INPUT XBAR output bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.65 CFG0_PWMXBAR6_G5 Registers

3.21.65.1 CFG0_G5 Register (Offset = 294h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2531. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1294h

Figure 3-1195. PWMXBAR6_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR6_G5_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR6_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2532. PWMXBAR6_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR6_G5_SEL	R/W	0h	PWM XBar6 G5 input bit select. Input source is PWM TRIPOUT. 1: PWM TRIPOUT bit[x] selected 0: PWM TRIPOUT bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.66 CFG0_PWMXBAR6_G6 Registers

3.21.66.1 CFG0_G6 Register (Offset = 298h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2533. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1298h

Figure 3-1196. PWMXBAR6_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR6_G6_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR6_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2534. PWMXBAR6_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR6_G6_SEL	R/W	0h	PWM XBar6 G6 input bit select. Input source is PWM DEL TRIP 1: PWM DEL TRIP bit[x] selected 0: PWM DEL TRIP bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.67 CFG0_PWMXBAR6_G7 Registers

3.21.67.1 CFG0_G7 Register (Offset = 29Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2535. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 129Ch

Figure 3-1197. PWMXBAR6_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR6_G7_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR6_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2536. PWMXBAR6_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR6_G7_SEL	R/W	0h	PWM XBar6 G7 input bit select. Input source is PWM DEL ACTIVE 1: PWM DEL ACTIVE bit[x] selected 0: PWM DEL ACTIVE bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.68 CFG0_PWMXBAR6_G8 Registers

3.21.68.1 CFG0_G8 Register (Offset = 2A0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2537. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 12A0h

Figure 3-1198. PWMXBAR6_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PWMXBAR6_G8_SEL												
NONE			R/W												
0			0h												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR6_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2538. PWMXBAR6_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:0	PWMXBAR6_G8_SEL	R/W	0h	PWM XBar6 G8 Input Select 0: EQEP0.ERR 1: EQEP1.ERR 2: EQEP2.ERR 6:3: FSIRX0.RX_TRIG4 10:7: FSIRX1.RX_TRIG4 14:11: FSIRX2.RX_TRIG4 18:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT Reset Source: mod_g_rst_n

3.21.69 CFG0_PWMXBAR7_G0 Registers

3.21.69.1 CFG0_G0 Register (Offset = 2C0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2539. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 12C0h

Figure 3-1199. PWMXBAR7_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR7_G0_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR7_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2540. PWMXBAR7_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR7_G0_SEL	R/W	0h	PWM XBar7 G0 Input Select 0: CMP12SS0.CTRIPL 1: CMP12SS0.CTRIPH 2: CMP12SS1.CTRIPL 3: CMP12SS1.CTRIPH 4: CMP12SS2.CTRIPL 5: CMP12SS2.CTRIPH 6: CMP12SS3.CTRIPL 7: CMP12SS3.CTRIPH 8: CMP12SS4.CTRIPL 9: CMP12SS4.CTRIPH 10: CMP12SS5.CTRIPL 11: CMP12SS5.CTRIPH 12: CMP12SS6.CTRIPL 13: CMP12SS6.CTRIPH 14: CMP12SS7.CTRIPL 15: CMP12SS7.CTRIPH 16: CMP12SS8.CTRIPL 17: CMP12SS8.CTRIPH 18: CMP12SS9.CTRIPL 19: CMP12SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.70 CFG0_PWMXBAR7_G1 Registers

3.21.70.1 CFG0_G1 Register (Offset = 2C4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2541. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 12C4h

Figure 3-1200. PWMXBAR7_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR7_G1_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR7_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2542. PWMXBAR7_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR7_G1_SEL	R/W	0h	PWM XBar7 G1 Input Select 0: CMP8SS0.CTRIPL 1: CMP8SS0.CTRIPH 2: CMP8SS1.CTRIPL 3: CMP8SS1.CTRIPH 4: CMP8SS2.CTRIPL 5: CMP8SS2.CTRIPH 6: CMP8SS3.CTRIPL 7: CMP8SS3.CTRIPH 8: CMP8SS4.CTRIPL 9: CMP8SS4.CTRIPH 10: CMP8SS5.CTRIPL 11: CMP8SS5.CTRIPH 12: CMP8SS6.CTRIPL 13: CMP8SS6.CTRIPH 14: CMP8SS7.CTRIPL 15: CMP8SS7.CTRIPH 16: CMP8SS8.CTRIPL 17: CMP8SS8.CTRIPH 18: CMP8SS9.CTRIPL 19: CMP8SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.71 CFG0_PWMXBAR7_G2 Registers

3.21.71.1 CFG0_G2 Register (Offset = 2C8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2543. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 12C8h

Figure 3-1201. PWMXBAR7_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PWMXBAR7_G2_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR7_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2544. PWMXBAR7_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	PWMXBAR7_G2_SEL	R/W	0h	PWM XBar7 G2 Input Select 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.21.72 CFG0_PWMXBAR7_G3 Registers

3.21.72.1 CFG0_G3 Register (Offset = 2CCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2545. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 12CCh

Figure 3-1202. PWMXBAR7_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR7_G3_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR7_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2546. PWMXBAR7_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR7_G3_SEL	R/W	0h	PWM XBar7 G3 Input Select 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1.EVT4 8: ADC2.EVT1 9: ADC2.EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.21.73 CFG0_PWMXBAR7_G4 Registers

3.21.73.1 CFG0_G4 Register (Offset = 2D0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2547. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 12D0h

Figure 3-1203. PWMXBAR7_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR7_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR7_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2548. PWMXBAR7_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR7_G4_SEL	R/W	0h	PWM XBar7 G4 input bit select. Input source is INPUT XBAR. 1: INPUT XBAR output bit[x] selected 0: INPUT XBAR output bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.74 CFG0_PWMXBAR7_G5 Registers

3.21.74.1 CFG0_G5 Register (Offset = 2D4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2549. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 12D4h

Figure 3-1204. PWMXBAR7_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR7_G5_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR7_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2550. PWMXBAR7_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR7_G5_SEL	R/W	0h	PWM XBar7 G5 input bit select. Input source is PWM TRIPOUT. 1: PWM TRIPOUT bit[x] selected 0: PWM TRIPOUT bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.75 CFG0_PWMXBAR7_G6 Registers

3.21.75.1 CFG0_G6 Register (Offset = 2D8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2551. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 12D8h

Figure 3-1205. PWMXBAR7_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR7_G6_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR7_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2552. PWMXBAR7_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR7_G6_SEL	R/W	0h	PWM XBar7 G6 input bit select. Input source is PWM DEL TRIP 1: PWM DEL TRIP bit[x] selected 0: PWM DEL TRIP bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.76 CFG0_PWMXBAR7_G7 Registers

3.21.76.1 CFG0_G7 Register (Offset = 2DCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2553. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 12DCh

Figure 3-1206. PWMXBAR7_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR7_G7_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR7_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2554. PWMXBAR7_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR7_G7_SEL	R/W	0h	PWM XBar7 G7 input bit select. Input source is PWM DEL ACTIVE 1: PWM DEL ACTIVE bit[x] selected 0: PWM DEL ACTIVE bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.77 CFG0_PWMXBAR7_G8 Registers

3.21.77.1 CFG0_G8 Register (Offset = 2E0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2555. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 12E0h

Figure 3-1207. PWMXBAR7_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PWMXBAR7_G8_SEL												
NONE			R/W												
0			0h												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR7_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2556. PWMXBAR7_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:0	PWMXBAR7_G8_SEL	R/W	0h	PWM XBar7 G8 Input Select 0: EQEP0.ERR 1: EQEP1.ERR 2: EQEP2.ERR 6:3: FSIRX0.RX_TRIG4 10:7: FSIRX1.RX_TRIG4 14:11: FSIRX2.RX_TRIG4 18:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT Reset Source: mod_g_rst_n

3.21.78 CFG0_PWMXBAR8_G0 Registers

3.21.78.1 CFG0_G0 Register (Offset = 300h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2557. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1300h

Figure 3-1208. PWMXBAR8_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR8_G0_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR8_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2558. PWMXBAR8_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR8_G0_SEL	R/W	0h	PWM XBar8 G0 Input Select 0: CMP12SS0.CTRIPL 1: CMP12SS0.CTRIPH 2: CMP12SS1.CTRIPL 3: CMP12SS1.CTRIPH 4: CMP12SS2.CTRIPL 5: CMP12SS2.CTRIPH 6: CMP12SS3.CTRIPL 7: CMP12SS3.CTRIPH 8: CMP12SS4.CTRIPL 9: CMP12SS4.CTRIPH 10: CMP12SS5.CTRIPL 11: CMP12SS5.CTRIPH 12: CMP12SS6.CTRIPL 13: CMP12SS6.CTRIPH 14: CMP12SS7.CTRIPL 15: CMP12SS7.CTRIPH 16: CMP12SS8.CTRIPL 17: CMP12SS8.CTRIPH 18: CMP12SS9.CTRIPL 19: CMP12SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.79 CFG0_PWMXBAR8_G1 Registers

3.21.79.1 CFG0_G1 Register (Offset = 304h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2559. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1304h

Figure 3-1209. PWMXBAR8_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR8_G1_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR8_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2560. PWMXBAR8_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR8_G1_SEL	R/W	0h	PWM XBar8 G1 Input Select 0: CMP8SS0.CTRIPL 1: CMP8SS0.CTRIPH 2: CMP8SS1.CTRIPL 3: CMP8SS1.CTRIPH 4: CMP8SS2.CTRIPL 5: CMP8SS2.CTRIPH 6: CMP8SS3.CTRIPL 7: CMP8SS3.CTRIPH 8: CMP8SS4.CTRIPL 9: CMP8SS4.CTRIPH 10: CMP8SS5.CTRIPL 11: CMP8SS5.CTRIPH 12: CMP8SS6.CTRIPL 13: CMP8SS6.CTRIPH 14: CMP8SS7.CTRIPL 15: CMP8SS7.CTRIPH 16: CMP8SS8.CTRIPL 17: CMP8SS8.CTRIPH 18: CMP8SS9.CTRIPL 19: CMP8SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.80 CFG0_PWMXBAR8_G2 Registers

3.21.80.1 CFG0_G2 Register (Offset = 308h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2561. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1308h

Figure 3-1210. PWMXBAR8_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PWMXBAR8_G2_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR8_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2562. PWMXBAR8_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	PWMXBAR8_G2_SEL	R/W	0h	PWM XBar8 G2 Input Select 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.21.81 CFG0_PWMXBAR8_G3 Registers

3.21.81.1 CFG0_G3 Register (Offset = 30Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2563. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 130Ch

Figure 3-1211. PWMXBAR8_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR8_G3_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR8_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2564. PWMXBAR8_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR8_G3_SEL	R/W	0h	PWM XBar8 G3 Input Select 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1.EVT4 8: ADC2.EVT1 9: ADC2.EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.21.82 CFG0_PWMXBAR8_G4 Registers

3.21.82.1 CFG0_G4 Register (Offset = 310h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2565. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1310h

Figure 3-1212. PWMXBAR8_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR8_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR8_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2566. PWMXBAR8_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR8_G4_SEL	R/W	0h	PWM XBar8 G4 input bit select. Input source is INPUT XBAR. 1: INPUT XBAR output bit[x] selected 0: INPUT XBAR output bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.83 CFG0_PWMXBAR8_G5 Registers

3.21.83.1 CFG0_G5 Register (Offset = 314h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2567. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1314h

Figure 3-1213. PWMXBAR8_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR8_G5_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR8_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2568. PWMXBAR8_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR8_G5_SEL	R/W	0h	PWM XBar8 G5 input bit select. Input source is PWM TRIPOUT. 1: PWM TRIPOUT bit[x] selected 0: PWM TRIPOUT bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.84 CFG0_PWMXBAR8_G6 Registers

3.21.84.1 CFG0_G6 Register (Offset = 318h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2569. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1318h

Figure 3-1214. PWMXBAR8_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR8_G6_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR8_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2570. PWMXBAR8_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR8_G6_SEL	R/W	0h	PWM XBar8 G6 input bit select. Input source is PWM DEL TRIP 1: PWM DEL TRIP bit[x] selected 0: PWM DEL TRIP bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.85 CFG0_PWMXBAR8_G7 Registers

3.21.85.1 CFG0_G7 Register (Offset = 31Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2571. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 131Ch

Figure 3-1215. PWMXBAR8_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR8_G7_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR8_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2572. PWMXBAR8_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR8_G7_SEL	R/W	0h	PWM XBar8 G7 input bit select. Input source is PWM DEL ACTIVE 1: PWM DEL ACTIVE bit[x] selected 0: PWM DEL ACTIVE bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.86 CFG0_PWMXBAR8_G8 Registers

3.21.86.1 CFG0_G8 Register (Offset = 320h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2573. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1320h

Figure 3-1216. PWMXBAR8_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PWMXBAR8_G8_SEL												
NONE			R/W												
0			0h												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR8_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2574. PWMXBAR8_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:0	PWMXBAR8_G8_SEL	R/W	0h	PWM XBar8 G8 Input Select 0: EQEP0.ERR 1: EQEP1.ERR 2: EQEP2.ERR 6:3: FSIRX0.RX_TRIG4 10:7: FSIRX1.RX_TRIG4 14:11: FSIRX2.RX_TRIG4 18:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT Reset Source: mod_g_rst_n

3.21.87 CFG0_PWMXBAR9_G0 Registers

3.21.87.1 CFG0_G0 Register (Offset = 340h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2575. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1340h

Figure 3-1217. PWMXBAR9_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR9_G0_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR9_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2576. PWMXBAR9_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR9_G0_SEL	R/W	0h	PWM XBar9 G0 Input Select 0: CMP12SS0.CTRIPL 1: CMP12SS0.CTRIPH 2: CMP12SS1.CTRIPL 3: CMP12SS1.CTRIPH 4: CMP12SS2.CTRIPL 5: CMP12SS2.CTRIPH 6: CMP12SS3.CTRIPL 7: CMP12SS3.CTRIPH 8: CMP12SS4.CTRIPL 9: CMP12SS4.CTRIPH 10: CMP12SS5.CTRIPL 11: CMP12SS5.CTRIPH 12: CMP12SS6.CTRIPL 13: CMP12SS6.CTRIPH 14: CMP12SS7.CTRIPL 15: CMP12SS7.CTRIPH 16: CMP12SS8.CTRIPL 17: CMP12SS8.CTRIPH 18: CMP12SS9.CTRIPL 19: CMP12SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.88 CFG0_PWMXBAR9_G1 Registers

3.21.88.1 CFG0_G1 Register (Offset = 344h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2577. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1344h

Figure 3-1218. PWMXBAR9_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR9_G1_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR9_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2578. PWMXBAR9_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR9_G1_SEL	R/W	0h	PWM XBar9 G1 Input Select 0: CMP8SS0.CTRIPL 1: CMP8SS0.CTRIPH 2: CMP8SS1.CTRIPL 3: CMP8SS1.CTRIPH 4: CMP8SS2.CTRIPL 5: CMP8SS2.CTRIPH 6: CMP8SS3.CTRIPL 7: CMP8SS3.CTRIPH 8: CMP8SS4.CTRIPL 9: CMP8SS4.CTRIPH 10: CMP8SS5.CTRIPL 11: CMP8SS5.CTRIPH 12: CMP8SS6.CTRIPL 13: CMP8SS6.CTRIPH 14: CMP8SS7.CTRIPL 15: CMP8SS7.CTRIPH 16: CMP8SS8.CTRIPL 17: CMP8SS8.CTRIPH 18: CMP8SS9.CTRIPL 19: CMP8SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.89 CFG0_PWMXBAR9_G2 Registers

3.21.89.1 CFG0_G2 Register (Offset = 348h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2579. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1348h

Figure 3-1219. PWMXBAR9_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PWMXBAR9_G2_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR9_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2580. PWMXBAR9_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	PWMXBAR9_G2_SEL	R/W	0h	PWM XBar9 G2 Input Select 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.21.90 CFG0_PWMXBAR9_G3 Registers

3.21.90.1 CFG0_G3 Register (Offset = 34Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2581. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 134Ch

Figure 3-1220. PWMXBAR9_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR9_G3_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR9_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2582. PWMXBAR9_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR9_G3_SEL	R/W	0h	PWM XBar9 G3 Input Select 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1.EVT4 8: ADC2.EVT1 9: ADC2.EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.21.91 CFG0_PWMXBAR9_G4 Registers

3.21.91.1 CFG0_G4 Register (Offset = 350h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2583. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1350h

Figure 3-1221. PWMXBAR9_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR9_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR9_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2584. PWMXBAR9_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR9_G4_SEL	R/W	0h	PWM XBar9 G4 input bit select. Input source is INPUT XBAR. 1: INPUT XBAR output bit[x] selected 0: INPUT XBAR output bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.92 CFG0_PWMXBAR9_G5 Registers

3.21.92.1 CFG0_G5 Register (Offset = 354h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2585. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1354h

Figure 3-1222. PWMXBAR9_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR9_G5_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR9_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2586. PWMXBAR9_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR9_G5_SEL	R/W	0h	PWM XBar9 G5 input bit select. Input source is PWM TRIPOUT. 1: PWM TRIPOUT bit[x] selected 0: PWM TRIPOUT bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.93 CFG0_PWMXBAR9_G6 Registers

3.21.93.1 CFG0_G6 Register (Offset = 358h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2587. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1358h

Figure 3-1223. PWMXBAR9_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR9_G6_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR9_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2588. PWMXBAR9_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR9_G6_SEL	R/W	0h	PWM XBar9 G6 input bit select. Input source is PWM DEL TRIP 1: PWM DEL TRIP bit[x] selected 0: PWM DEL TRIP bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.94 CFG0_PWMXBAR9_G7 Registers

3.21.94.1 CFG0_G7 Register (Offset = 35Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2589. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 135Ch

Figure 3-1224. PWMXBAR9_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR9_G7_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR9_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2590. PWMXBAR9_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR9_G7_SEL	R/W	0h	PWM XBar9 G7 input bit select. Input source is PWM DEL ACTIVE 1: PWM DEL ACTIVE bit[x] selected 0: PWM DEL ACTIVE bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.95 CFG0_PWMXBAR9_G8 Registers

3.21.95.1 CFG0_G8 Register (Offset = 360h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2591. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1360h

Figure 3-1225. PWMXBAR9_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PWMXBAR9_G8_SEL												
NONE			R/W												
0			0h												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR9_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2592. PWMXBAR9_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:0	PWMXBAR9_G8_SEL	R/W	0h	PWM XBar9 G8 Input Select 0: EQEP0.ERR 1: EQEP1.ERR 2: EQEP2.ERR 6:3: FSIRX0.RX_TRIG4 10:7: FSIRX1.RX_TRIG4 14:11: FSIRX2.RX_TRIG4 18:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT Reset Source: mod_g_rst_n

3.21.96 CFG0_PWMXBAR10_G0 Registers

3.21.96.1 CFG0_G0 Register (Offset = 380h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2593. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1380h

Figure 3-1226. PWMXBAR10_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR10_G0_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR10_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2594. PWMXBAR10_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR10_G0_SEL	R/W	0h	PWM XBar10 G0 Input Select 0: CMP12SS0.CTRIPL 1: CMP12SS0.CTRIPH 2: CMP12SS1.CTRIPL 3: CMP12SS1.CTRIPH 4: CMP12SS2.CTRIPL 5: CMP12SS2.CTRIPH 6: CMP12SS3.CTRIPL 7: CMP12SS3.CTRIPH 8: CMP12SS4.CTRIPL 9: CMP12SS4.CTRIPH 10: CMP12SS5.CTRIPL 11: CMP12SS5.CTRIPH 12: CMP12SS6.CTRIPL 13: CMP12SS6.CTRIPH 14: CMP12SS7.CTRIPL 15: CMP12SS7.CTRIPH 16: CMP12SS8.CTRIPL 17: CMP12SS8.CTRIPH 18: CMP12SS9.CTRIPL 19: CMP12SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.97 CFG0_PWMXBAR10_G1 Registers

3.21.97.1 CFG0_G1 Register (Offset = 384h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2595. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1384h

Figure 3-1227. PWMXBAR10_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR10_G1_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR10_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2596. PWMXBAR10_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR10_G1_SEL	R/W	0h	PWM XBar10 G1 Input Select 0: CMP8SS0.CTRIPL 1: CMP8SS0.CTRIPH 2: CMP8SS1.CTRIPL 3: CMP8SS1.CTRIPH 4: CMP8SS2.CTRIPL 5: CMP8SS2.CTRIPH 6: CMP8SS3.CTRIPL 7: CMP8SS3.CTRIPH 8: CMP8SS4.CTRIPL 9: CMP8SS4.CTRIPH 10: CMP8SS5.CTRIPL 11: CMP8SS5.CTRIPH 12: CMP8SS6.CTRIPL 13: CMP8SS6.CTRIPH 14: CMP8SS7.CTRIPL 15: CMP8SS7.CTRIPH 16: CMP8SS8.CTRIPL 17: CMP8SS8.CTRIPH 18: CMP8SS9.CTRIPL 19: CMP8SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.98 CFG0_PWMXBAR10_G2 Registers

3.21.98.1 CFG0_G2 Register (Offset = 388h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2597. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1388h

Figure 3-1228. PWMXBAR10_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PWMXBAR10_G2_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR10_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2598. PWMXBAR10_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	PWMXBAR10_G2_SEL	R/W	0h	PWM XBar10 G2 Input Select 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.21.99 CFG0_PWMXBAR10_G3 Registers

3.21.99.1 CFG0_G3 Register (Offset = 38Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2599. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 138Ch

Figure 3-1229. PWMXBAR10_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR10_G3_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR10_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2600. PWMXBAR10_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR10_G3_SEL	R/W	0h	PWM XBar10 G3 Input Select 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1.EVT4 8: ADC2.EVT1 9: ADC2.EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.21.100 CFG0_PWMXBAR10_G4 Registers

3.21.100.1 CFG0_G4 Register (Offset = 390h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2601. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1390h

Figure 3-1230. PWMXBAR10_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR10_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR10_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2602. PWMXBAR10_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR10_G4_SEL	R/W	0h	PWM XBar10 G4 input bit select. Input source is INPUT XBAR. 1: INPUT XBAR output bit[x] selected 0: INPUT XBAR output bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.101 CFG0_PWMXBAR10_G5 Registers

3.21.101.1 CFG0_G5 Register (Offset = 394h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2603. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1394h

Figure 3-1231. PWMXBAR10_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR10_G5_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR10_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2604. PWMXBAR10_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR10_G5_SEL	R/W	0h	PWM XBar10 G5 input bit select. Input source is PWM TRIPOUT. 1: PWM TRIPOUT bit[x] selected 0: PWM TRIPOUT bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.102 CFG0_PWMXBAR10_G6 Registers

3.21.102.1 CFG0_G6 Register (Offset = 398h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2605. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1398h

Figure 3-1232. PWMXBAR10_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR10_G6_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR10_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2606. PWMXBAR10_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR10_G6_SEL	R/W	0h	PWM XBar10 G6 input bit select. Input source is PWM DEL TRIP 1: PWM DEL TRIP bit[x] selected 0: PWM DEL TRIP bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.103 CFG0_PWMXBAR10_G7 Registers

3.21.103.1 CFG0_G7 Register (Offset = 39Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2607. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 139Ch

Figure 3-1233. PWMXBAR10_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR10_G7_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR10_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2608. PWMXBAR10_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR10_G7_SEL	R/W	0h	PWM XBar10 G7 input bit select. Input source is PWM DEL ACTIVE 1: PWM DEL ACTIVE bit[x] selected 0: PWM DEL ACTIVE bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.104 CFG0_PWMXBAR10_G8 Registers

3.21.104.1 CFG0_G8 Register (Offset = 3A0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2609. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 13A0h

Figure 3-1234. PWMXBAR10_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PWMXBAR10_G8_SEL												
NONE			R/W												
0			0h												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR10_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2610. PWMXBAR10_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:0	PWMXBAR10_G8_SEL	R/W	0h	PWM XBar10 G8 Input Select 0: EQEP0.ERR 1: EQEP1.ERR 2: EQEP2.ERR 6:3: FSIRX0.RX_TRIG4 10:7: FSIRX1.RX_TRIG4 14:11: FSIRX2.RX_TRIG4 18:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT Reset Source: mod_g_rst_n

3.21.105 CFG0_PWMXBAR11_G0 Registers

3.21.105.1 CFG0_G0 Register (Offset = 3C0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2611. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 13C0h

Figure 3-1235. PWMXBAR11_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR11_G0_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR11_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2612. PWMXBAR11_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR11_G0_SEL	R/W	0h	PWM XBar11 G0 Input Select 0: CMP12SS0.CTRIPL 1: CMP12SS0.CTRIPH 2: CMP12SS1.CTRIPL 3: CMP12SS1.CTRIPH 4: CMP12SS2.CTRIPL 5: CMP12SS2.CTRIPH 6: CMP12SS3.CTRIPL 7: CMP12SS3.CTRIPH 8: CMP12SS4.CTRIPL 9: CMP12SS4.CTRIPH 10: CMP12SS5.CTRIPL 11: CMP12SS5.CTRIPH 12: CMP12SS6.CTRIPL 13: CMP12SS6.CTRIPH 14: CMP12SS7.CTRIPL 15: CMP12SS7.CTRIPH 16: CMP12SS8.CTRIPL 17: CMP12SS8.CTRIPH 18: CMP12SS9.CTRIPL 19: CMP12SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.106 CFG0_PWMXBAR11_G1 Registers

3.21.106.1 CFG0_G1 Register (Offset = 3C4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2613. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 13C4h

Figure 3-1236. PWMXBAR11_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR11_G1_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR11_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2614. PWMXBAR11_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR11_G1_SEL	R/W	0h	PWM XBar11 G1 Input Select 0: CMP8SS0.CTRIPL 1: CMP8SS0.CTRIPH 2: CMP8SS1.CTRIPL 3: CMP8SS1.CTRIPH 4: CMP8SS2.CTRIPL 5: CMP8SS2.CTRIPH 6: CMP8SS3.CTRIPL 7: CMP8SS3.CTRIPH 8: CMP8SS4.CTRIPL 9: CMP8SS4.CTRIPH 10: CMP8SS5.CTRIPL 11: CMP8SS5.CTRIPH 12: CMP8SS6.CTRIPL 13: CMP8SS6.CTRIPH 14: CMP8SS7.CTRIPL 15: CMP8SS7.CTRIPH 16: CMP8SS8.CTRIPL 17: CMP8SS8.CTRIPH 18: CMP8SS9.CTRIPL 19: CMP8SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.107 CFG0_PWMXBAR11_G2 Registers

3.21.107.1 CFG0_G2 Register (Offset = 3C8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2615. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 13C8h

Figure 3-1237. PWMXBAR11_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PWMXBAR11_G2_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR11_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2616. PWMXBAR11_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	PWMXBAR11_G2_SEL	R/W	0h	PWM XBar11 G2 Input Select 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.21.108 CFG0_PWMXBAR11_G3 Registers

3.21.108.1 CFG0_G3 Register (Offset = 3CCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2617. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 13CCh

Figure 3-1238. PWMXBAR11_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR11_G3_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR11_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2618. PWMXBAR11_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR11_G3_SEL	R/W	0h	PWM XBar11 G3 Input Select 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1.EVT4 8: ADC2.EVT1 9: ADC2.EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.21.109 CFG0_PWMXBAR11_G4 Registers

3.21.109.1 CFG0_G4 Register (Offset = 3D0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2619. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 13D0h

Figure 3-1239. PWMXBAR11_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR11_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR11_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2620. PWMXBAR11_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR11_G4_SEL	R/W	0h	PWM XBar11 G4 input bit select. Input source is INPUT XBAR. 1: INPUT XBAR output bit[x] selected 0: INPUT XBAR output bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.110 CFG0_PWMXBAR11_G5 Registers

3.21.110.1 CFG0_G5 Register (Offset = 3D4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2621. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 13D4h

Figure 3-1240. PWMXBAR11_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR11_G5_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR11_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2622. PWMXBAR11_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR11_G5_SEL	R/W	0h	PWM XBar11 G5 input bit select. Input source is PWM TRIPOUT. 1: PWM TRIPOUT bit[x] selected 0: PWM TRIPOUT bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.111 CFG0_PWMXBAR11_G6 Registers

3.21.111.1 CFG0_G6 Register (Offset = 3D8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2623. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 13D8h

Figure 3-1241. PWMXBAR11_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR11_G6_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR11_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2624. PWMXBAR11_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR11_G6_SEL	R/W	0h	PWM XBar11 G6 input bit select. Input source is PWM DEL TRIP 1: PWM DEL TRIP bit[x] selected 0: PWM DEL TRIP bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.112 CFG0_PWMXBAR11_G7 Registers

3.21.112.1 CFG0_G7 Register (Offset = 3DCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2625. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 13DCh

Figure 3-1242. PWMXBAR11_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR11_G7_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR11_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2626. PWMXBAR11_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR11_G7_SEL	R/W	0h	PWM XBar11 G7 input bit select. Input source is PWM DEL ACTIVE 1: PWM DEL ACTIVE bit[x] selected 0: PWM DEL ACTIVE bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.113 CFG0_PWMXBAR11_G8 Registers

3.21.113.1 CFG0_G8 Register (Offset = 3E0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2627. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 13E0h

Figure 3-1243. PWMXBAR11_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PWMXBAR11_G8_SEL												
NONE			R/W												
0			0h												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR11_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2628. PWMXBAR11_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:0	PWMXBAR11_G8_SEL	R/W	0h	PWM XBar11 G8 Input Select 0: EQEP0.ERR 1: EQEP1.ERR 2: EQEP2.ERR 6:3: FSIRX0.RX_TRIG4 10:7: FSIRX1.RX_TRIG4 14:11: FSIRX2.RX_TRIG4 18:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT Reset Source: mod_g_rst_n

3.21.114 CFG0_PWMXBAR12_G0 Registers

3.21.114.1 CFG0_G0 Register (Offset = 400h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2629. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1400h

Figure 3-1244. PWMXBAR12_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR12_G0_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR12_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2630. PWMXBAR12_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR12_G0_SEL	R/W	0h	PWM XBar12 G0 Input Select 0: CMP12SS0.CTRIPL 1: CMP12SS0.CTRIPH 2: CMP12SS1.CTRIPL 3: CMP12SS1.CTRIPH 4: CMP12SS2.CTRIPL 5: CMP12SS2.CTRIPH 6: CMP12SS3.CTRIPL 7: CMP12SS3.CTRIPH 8: CMP12SS4.CTRIPL 9: CMP12SS4.CTRIPH 10: CMP12SS5.CTRIPL 11: CMP12SS5.CTRIPH 12: CMP12SS6.CTRIPL 13: CMP12SS6.CTRIPH 14: CMP12SS7.CTRIPL 15: CMP12SS7.CTRIPH 16: CMP12SS8.CTRIPL 17: CMP12SS8.CTRIPH 18: CMP12SS9.CTRIPL 19: CMP12SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.115 CFG0_PWMXBAR12_G1 Registers

3.21.115.1 CFG0_G1 Register (Offset = 404h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2631. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1404h

Figure 3-1245. PWMXBAR12_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR12_G1_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR12_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2632. PWMXBAR12_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR12_G1_SEL	R/W	0h	PWM XBar12 G1 Input Select 0: CMP8SS0.CTRIPL 1: CMP8SS0.CTRIPH 2: CMP8SS1.CTRIPL 3: CMP8SS1.CTRIPH 4: CMP8SS2.CTRIPL 5: CMP8SS2.CTRIPH 6: CMP8SS3.CTRIPL 7: CMP8SS3.CTRIPH 8: CMP8SS4.CTRIPL 9: CMP8SS4.CTRIPH 10: CMP8SS5.CTRIPL 11: CMP8SS5.CTRIPH 12: CMP8SS6.CTRIPL 13: CMP8SS6.CTRIPH 14: CMP8SS7.CTRIPL 15: CMP8SS7.CTRIPH 16: CMP8SS8.CTRIPL 17: CMP8SS8.CTRIPH 18: CMP8SS9.CTRIPL 19: CMP8SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.116 CFG0_PWMXBAR12_G2 Registers

3.21.116.1 CFG0_G2 Register (Offset = 408h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2633. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1408h

Figure 3-1246. PWMXBAR12_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PWMXBAR12_G2_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR12_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2634. PWMXBAR12_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	PWMXBAR12_G2_SEL	R/W	0h	PWM XBar12 G2 Input Select 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.21.117 CFG0_PWMXBAR12_G3 Registers

3.21.117.1 CFG0_G3 Register (Offset = 40Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2635. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 140Ch

Figure 3-1247. PWMXBAR12_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR12_G3_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR12_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2636. PWMXBAR12_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR12_G3_SEL	R/W	0h	PWM XBar12 G3 Input Select 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1.EVT4 8: ADC2.EVT1 9: ADC2.EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.21.118 CFG0_PWMXBAR12_G4 Registers

3.21.118.1 CFG0_G4 Register (Offset = 410h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2637. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1410h

Figure 3-1248. PWMXBAR12_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR12_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR12_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2638. PWMXBAR12_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR12_G4_SEL	R/W	0h	PWM XBar12 G4 input bit select. Input source is INPUT XBAR. 1: INPUT XBAR output bit[x] selected 0: INPUT XBAR output bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.119 CFG0_PWMXBAR12_G5 Registers

3.21.119.1 CFG0_G5 Register (Offset = 414h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2639. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1414h

Figure 3-1249. PWMXBAR12_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR12_G5_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR12_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2640. PWMXBAR12_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR12_G5_SEL	R/W	0h	PWM XBar12 G5 input bit select. Input source is PWM TRIPOUT. 1: PWM TRIPOUT bit[x] selected 0: PWM TRIPOUT bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.120 CFG0_PWMXBAR12_G6 Registers

3.21.120.1 CFG0_G6 Register (Offset = 418h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2641. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1418h

Figure 3-1250. PWMXBAR12_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR12_G6_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR12_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2642. PWMXBAR12_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR12_G6_SEL	R/W	0h	PWM XBar12 G6 input bit select. Input source is PWM DEL TRIP 1: PWM DEL TRIP bit[x] selected 0: PWM DEL TRIP bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.121 CFG0_PWMXBAR12_G7 Registers

3.21.121.1 CFG0_G7 Register (Offset = 41Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2643. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 141Ch

Figure 3-1251. PWMXBAR12_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR12_G7_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR12_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2644. PWMXBAR12_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR12_G7_SEL	R/W	0h	PWM XBar12 G7 input bit select. Input source is PWM DEL ACTIVE 1: PWM DEL ACTIVE bit[x] selected 0: PWM DEL ACTIVE bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.122 CFG0_PWMXBAR12_G8 Registers

3.21.122.1 CFG0_G8 Register (Offset = 420h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2645. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1420h

Figure 3-1252. PWMXBAR12_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PWMXBAR12_G8_SEL												
NONE			R/W												
0			0h												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR12_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2646. PWMXBAR12_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:0	PWMXBAR12_G8_SEL	R/W	0h	PWM XBar12 G8 Input Select 0: EQEP0.ERR 1: EQEP1.ERR 2: EQEP2.ERR 6:3: FSIRX0.RX_TRIG4 10:7: FSIRX1.RX_TRIG4 14:11: FSIRX2.RX_TRIG4 18:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT Reset Source: mod_g_rst_n

3.21.123 CFG0_PWMXBAR13_G0 Registers

3.21.123.1 CFG0_G0 Register (Offset = 440h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2647. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1440h

Figure 3-1253. PWMXBAR13_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR13_G0_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR13_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2648. PWMXBAR13_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR13_G0_SEL	R/W	0h	PWM XBar13 G0 Input Select 0: CMP12SS0.CTRIPL 1: CMP12SS0.CTRIPH 2: CMP12SS1.CTRIPL 3: CMP12SS1.CTRIPH 4: CMP12SS2.CTRIPL 5: CMP12SS2.CTRIPH 6: CMP12SS3.CTRIPL 7: CMP12SS3.CTRIPH 8: CMP12SS4.CTRIPL 9: CMP12SS4.CTRIPH 10: CMP12SS5.CTRIPL 11: CMP12SS5.CTRIPH 12: CMP12SS6.CTRIPL 13: CMP12SS6.CTRIPH 14: CMP12SS7.CTRIPL 15: CMP12SS7.CTRIPH 16: CMP12SS8.CTRIPL 17: CMP12SS8.CTRIPH 18: CMP12SS9.CTRIPL 19: CMP12SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.124 CFG0_PWMXBAR13_G1 Registers

3.21.124.1 CFG0_G1 Register (Offset = 444h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2649. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1444h

Figure 3-1254. PWMXBAR13_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR13_G1_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR13_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2650. PWMXBAR13_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR13_G1_SEL	R/W	0h	PWM XBar13 G1 Input Select 0: CMP8SS0.CTRIPL 1: CMP8SS0.CTRIPH 2: CMP8SS1.CTRIPL 3: CMP8SS1.CTRIPH 4: CMP8SS2.CTRIPL 5: CMP8SS2.CTRIPH 6: CMP8SS3.CTRIPL 7: CMP8SS3.CTRIPH 8: CMP8SS4.CTRIPL 9: CMP8SS4.CTRIPH 10: CMP8SS5.CTRIPL 11: CMP8SS5.CTRIPH 12: CMP8SS6.CTRIPL 13: CMP8SS6.CTRIPH 14: CMP8SS7.CTRIPL 15: CMP8SS7.CTRIPH 16: CMP8SS8.CTRIPL 17: CMP8SS8.CTRIPH 18: CMP8SS9.CTRIPL 19: CMP8SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.125 CFG0_PWMXBAR13_G2 Registers

3.21.125.1 CFG0_G2 Register (Offset = 448h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2651. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1448h

Figure 3-1255. PWMXBAR13_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PWMXBAR13_G2_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR13_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2652. PWMXBAR13_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	PWMXBAR13_G2_SEL	R/W	0h	PWM XBar13 G2 Input Select 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.21.126 CFG0_PWMXBAR13_G3 Registers

3.21.126.1 CFG0_G3 Register (Offset = 44Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2653. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 144Ch

Figure 3-1256. PWMXBAR13_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR13_G3_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR13_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2654. PWMXBAR13_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR13_G3_SEL	R/W	0h	PWM XBar13 G3 Input Select 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1.EVT4 8: ADC2.EVT1 9: ADC2.EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.21.127 CFG0_PWMXBAR13_G4 Registers

3.21.127.1 CFG0_G4 Register (Offset = 450h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2655. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1450h

Figure 3-1257. PWMXBAR13_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR13_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR13_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2656. PWMXBAR13_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR13_G4_SEL	R/W	0h	PWM XBar13 G4 input bit select. Input source is INPUT XBAR. 1: INPUT XBAR output bit[x] selected 0: INPUT XBAR output bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.128 CFG0_PWMXBAR13_G5 Registers

3.21.128.1 CFG0_G5 Register (Offset = 454h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2657. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1454h

Figure 3-1258. PWMXBAR13_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR13_G5_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR13_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2658. PWMXBAR13_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR13_G5_SEL	R/W	0h	PWM XBar13 G5 input bit select. Input source is PWM TRIPOUT. 1: PWM TRIPOUT bit[x] selected 0: PWM TRIPOUT bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.129 CFG0_PWMXBAR13_G6 Registers

3.21.129.1 CFG0_G6 Register (Offset = 458h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2659. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1458h

Figure 3-1259. PWMXBAR13_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR13_G6_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR13_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2660. PWMXBAR13_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR13_G6_SEL	R/W	0h	PWM XBar13 G6 input bit select. Input source is PWM DEL TRIP 1: PWM DEL TRIP bit[x] selected 0: PWM DEL TRIP bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.130 CFG0_PWMXBAR13_G7 Registers

3.21.130.1 CFG0_G7 Register (Offset = 45Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2661. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 145Ch

Figure 3-1260. PWMXBAR13_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR13_G7_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR13_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2662. PWMXBAR13_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR13_G7_SEL	R/W	0h	PWM XBar13 G7 input bit select. Input source is PWM DEL ACTIVE 1: PWM DEL ACTIVE bit[x] selected 0: PWM DEL ACTIVE bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.131 CFG0_PWMXBAR13_G8 Registers

3.21.131.1 CFG0_G8 Register (Offset = 460h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2663. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1460h

Figure 3-1261. PWMXBAR13_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PWMXBAR13_G8_SEL												
NONE			R/W												
0			0h												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR13_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2664. PWMXBAR13_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:0	PWMXBAR13_G8_SEL	R/W	0h	PWM XBar13 G8 Input Select 0: EQEP0.ERR 1: EQEP1.ERR 2: EQEP2.ERR 6:3: FSIRX0.RX_TRIG4 10:7: FSIRX1.RX_TRIG4 14:11: FSIRX2.RX_TRIG4 18:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT Reset Source: mod_g_rst_n

3.21.132 CFG0_PWMXBAR14_G0 Registers

3.21.132.1 CFG0_G0 Register (Offset = 480h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2665. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1480h

Figure 3-1262. PWMXBAR14_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR14_G0_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR14_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2666. PWMXBAR14_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR14_G0_SEL	R/W	0h	PWM XBar14 G0 Input Select 0: CMP12SS0.CTRIPL 1: CMP12SS0.CTRIPH 2: CMP12SS1.CTRIPL 3: CMP12SS1.CTRIPH 4: CMP12SS2.CTRIPL 5: CMP12SS2.CTRIPH 6: CMP12SS3.CTRIPL 7: CMP12SS3.CTRIPH 8: CMP12SS4.CTRIPL 9: CMP12SS4.CTRIPH 10: CMP12SS5.CTRIPL 11: CMP12SS5.CTRIPH 12: CMP12SS6.CTRIPL 13: CMP12SS6.CTRIPH 14: CMP12SS7.CTRIPL 15: CMP12SS7.CTRIPH 16: CMP12SS8.CTRIPL 17: CMP12SS8.CTRIPH 18: CMP12SS9.CTRIPL 19: CMP12SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.133 CFG0_PWMXBAR14_G1 Registers

3.21.133.1 CFG0_G1 Register (Offset = 484h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2667. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1484h

Figure 3-1263. PWMXBAR14_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR14_G1_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR14_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2668. PWMXBAR14_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR14_G1_SEL	R/W	0h	PWM XBar14 G1 Input Select 0: CMP8SS0.CTRIPL 1: CMP8SS0.CTRIPH 2: CMP8SS1.CTRIPL 3: CMP8SS1.CTRIPH 4: CMP8SS2.CTRIPL 5: CMP8SS2.CTRIPH 6: CMP8SS3.CTRIPL 7: CMP8SS3.CTRIPH 8: CMP8SS4.CTRIPL 9: CMP8SS4.CTRIPH 10: CMP8SS5.CTRIPL 11: CMP8SS5.CTRIPH 12: CMP8SS6.CTRIPL 13: CMP8SS6.CTRIPH 14: CMP8SS7.CTRIPL 15: CMP8SS7.CTRIPH 16: CMP8SS8.CTRIPL 17: CMP8SS8.CTRIPH 18: CMP8SS9.CTRIPL 19: CMP8SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.134 CFG0_PWMXBAR14_G2 Registers

3.21.134.1 CFG0_G2 Register (Offset = 488h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2669. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1488h

Figure 3-1264. PWMXBAR14_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PWMXBAR14_G2_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR14_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2670. PWMXBAR14_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	PWMXBAR14_G2_SEL	R/W	0h	PWM XBar14 G2 Input Select 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.21.135 CFG0_PWMXBAR14_G3 Registers

3.21.135.1 CFG0_G3 Register (Offset = 48Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2671. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 148Ch

Figure 3-1265. PWMXBAR14_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR14_G3_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR14_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2672. PWMXBAR14_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR14_G3_SEL	R/W	0h	PWM XBar14 G3 Input Select 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1.EVT4 8: ADC2.EVT1 9: ADC2.EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.21.136 CFG0_PWMXBAR14_G4 Registers

3.21.136.1 CFG0_G4 Register (Offset = 490h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2673. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1490h

Figure 3-1266. PWMXBAR14_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR14_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR14_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2674. PWMXBAR14_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR14_G4_SEL	R/W	0h	PWM XBar14 G4 input bit select. Input source is INPUT XBAR. 1: INPUT XBAR output bit[x] selected 0: INPUT XBAR output bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.137 CFG0_PWMXBAR14_G5 Registers

3.21.137.1 CFG0_G5 Register (Offset = 494h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2675. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1494h

Figure 3-1267. PWMXBAR14_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR14_G5_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR14_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2676. PWMXBAR14_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR14_G5_SEL	R/W	0h	PWM XBar14 G5 input bit select. Input source is PWM TRIPOUT. 1: PWM TRIPOUT bit[x] selected 0: PWM TRIPOUT bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.138 CFG0_PWMXBAR14_G6 Registers

3.21.138.1 CFG0_G6 Register (Offset = 498h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2677. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1498h

Figure 3-1268. PWMXBAR14_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR14_G6_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR14_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2678. PWMXBAR14_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR14_G6_SEL	R/W	0h	PWM XBar14 G6 input bit select. Input source is PWM DEL TRIP 1: PWM DEL TRIP bit[x] selected 0: PWM DEL TRIP bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.139 CFG0_PWMXBAR14_G7 Registers

3.21.139.1 CFG0_G7 Register (Offset = 49Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2679. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 149Ch

Figure 3-1269. PWMXBAR14_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR14_G7_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR14_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2680. PWMXBAR14_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR14_G7_SEL	R/W	0h	PWM XBar14 G7 input bit select. Input source is PWM DEL ACTIVE 1: PWM DEL ACTIVE bit[x] selected 0: PWM DEL ACTIVE bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.140 CFG0_PWMXBAR14_G8 Registers

3.21.140.1 CFG0_G8 Register (Offset = 4A0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2681. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 14A0h

Figure 3-1270. PWMXBAR14_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PWMXBAR14_G8_SEL												
NONE			R/W												
0			0h												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR14_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2682. PWMXBAR14_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:0	PWMXBAR14_G8_SEL	R/W	0h	PWM XBar14 G8 Input Select 0: EQEP0.ERR 1: EQEP1.ERR 2: EQEP2.ERR 6:3: FSIRX0.RX_TRIG4 10:7: FSIRX1.RX_TRIG4 14:11: FSIRX2.RX_TRIG4 18:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT Reset Source: mod_g_rst_n

3.21.141 CFG0_PWMXBAR15_G0 Registers

3.21.141.1 CFG0_G0 Register (Offset = 4C0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2683. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 14C0h

Figure 3-1271. PWMXBAR15_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR15_G0_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR15_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2684. PWMXBAR15_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR15_G0_SEL	R/W	0h	PWM XBar15 G0 Input Select 0: CMP12SS0.CTRIPL 1: CMP12SS0.CTRIPH 2: CMP12SS1.CTRIPL 3: CMP12SS1.CTRIPH 4: CMP12SS2.CTRIPL 5: CMP12SS2.CTRIPH 6: CMP12SS3.CTRIPL 7: CMP12SS3.CTRIPH 8: CMP12SS4.CTRIPL 9: CMP12SS4.CTRIPH 10: CMP12SS5.CTRIPL 11: CMP12SS5.CTRIPH 12: CMP12SS6.CTRIPL 13: CMP12SS6.CTRIPH 14: CMP12SS7.CTRIPL 15: CMP12SS7.CTRIPH 16: CMP12SS8.CTRIPL 17: CMP12SS8.CTRIPH 18: CMP12SS9.CTRIPL 19: CMP12SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.142 CFG0_PWMXBAR15_G1 Registers

3.21.142.1 CFG0_G1 Register (Offset = 4C4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2685. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 14C4h

Figure 3-1272. PWMXBAR15_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR15_G1_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR15_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2686. PWMXBAR15_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR15_G1_SEL	R/W	0h	PWM XBar15 G1 Input Select 0: CMP8SS0.CTRIPL 1: CMP8SS0.CTRIPH 2: CMP8SS1.CTRIPL 3: CMP8SS1.CTRIPH 4: CMP8SS2.CTRIPL 5: CMP8SS2.CTRIPH 6: CMP8SS3.CTRIPL 7: CMP8SS3.CTRIPH 8: CMP8SS4.CTRIPL 9: CMP8SS4.CTRIPH 10: CMP8SS5.CTRIPL 11: CMP8SS5.CTRIPH 12: CMP8SS6.CTRIPL 13: CMP8SS6.CTRIPH 14: CMP8SS7.CTRIPL 15: CMP8SS7.CTRIPH 16: CMP8SS8.CTRIPL 17: CMP8SS8.CTRIPH 18: CMP8SS9.CTRIPL 19: CMP8SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.143 CFG0_PWMXBAR15_G2 Registers

3.21.143.1 CFG0_G2 Register (Offset = 4C8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2687. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 14C8h

Figure 3-1273. PWMXBAR15_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PWMXBAR15_G2_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR15_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2688. PWMXBAR15_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	PWMXBAR15_G2_SEL	R/W	0h	PWM XBar15 G2 Input Select 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.21.144 CFG0_PWMXBAR15_G3 Registers

3.21.144.1 CFG0_G3 Register (Offset = 4CCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2689. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 14CCh

Figure 3-1274. PWMXBAR15_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR15_G3_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR15_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2690. PWMXBAR15_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR15_G3_SEL	R/W	0h	PWM XBar15 G3 Input Select 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1.EVT4 8: ADC2.EVT1 9: ADC2.EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.21.145 CFG0_PWMXBAR15_G4 Registers

3.21.145.1 CFG0_G4 Register (Offset = 4D0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2691. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 14D0h

Figure 3-1275. PWMXBAR15_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR15_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR15_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2692. PWMXBAR15_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR15_G4_SEL	R/W	0h	PWM XBar15 G4 input bit select. Input source is INPUT XBAR. 1: INPUT XBAR output bit[x] selected 0: INPUT XBAR output bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.146 CFG0_PWMXBAR15_G5 Registers

3.21.146.1 CFG0_G5 Register (Offset = 4D4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2693. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 14D4h

Figure 3-1276. PWMXBAR15_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR15_G5_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR15_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2694. PWMXBAR15_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR15_G5_SEL	R/W	0h	PWM XBar15 G5 input bit select. Input source is PWM TRIPOUT. 1: PWM TRIPOUT bit[x] selected 0: PWM TRIPOUT bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.147 CFG0_PWMXBAR15_G6 Registers

3.21.147.1 CFG0_G6 Register (Offset = 4D8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2695. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 14D8h

Figure 3-1277. PWMXBAR15_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR15_G6_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR15_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2696. PWMXBAR15_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR15_G6_SEL	R/W	0h	PWM XBar15 G6 input bit select. Input source is PWM DEL TRIP 1: PWM DEL TRIP bit[x] selected 0: PWM DEL TRIP bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.148 CFG0_PWMXBAR15_G7 Registers

3.21.148.1 CFG0_G7 Register (Offset = 4DCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2697. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 14DCh

Figure 3-1278. PWMXBAR15_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR15_G7_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR15_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2698. PWMXBAR15_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR15_G7_SEL	R/W	0h	PWM XBar15 G7 input bit select. Input source is PWM DEL ACTIVE 1: PWM DEL ACTIVE bit[x] selected 0: PWM DEL ACTIVE bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.149 CFG0_PWMXBAR15_G8 Registers

3.21.149.1 CFG0_G8 Register (Offset = 4E0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2699. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 14E0h

Figure 3-1279. PWMXBAR15_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PWMXBAR15_G8_SEL												
NONE			R/W												
0			0h												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR15_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2700. PWMXBAR15_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:0	PWMXBAR15_G8_SEL	R/W	0h	PWM XBar15 G8 Input Select 0: EQEP0.ERR 1: EQEP1.ERR 2: EQEP2.ERR 6:3: FSIRX0.RX_TRIG4 10:7: FSIRX1.RX_TRIG4 14:11: FSIRX2.RX_TRIG4 18:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT Reset Source: mod_g_rst_n

3.21.150 CFG0_PWMXBAR16_G0 Registers

3.21.150.1 CFG0_G0 Register (Offset = 500h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2701. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1500h

Figure 3-1280. PWMXBAR16_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR16_G0_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR16_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2702. PWMXBAR16_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR16_G0_SEL	R/W	0h	PWM XBar16 G0 Input Select 0: CMP12SS0.CTRIPL 1: CMP12SS0.CTRIPH 2: CMP12SS1.CTRIPL 3: CMP12SS1.CTRIPH 4: CMP12SS2.CTRIPL 5: CMP12SS2.CTRIPH 6: CMP12SS3.CTRIPL 7: CMP12SS3.CTRIPH 8: CMP12SS4.CTRIPL 9: CMP12SS4.CTRIPH 10: CMP12SS5.CTRIPL 11: CMP12SS5.CTRIPH 12: CMP12SS6.CTRIPL 13: CMP12SS6.CTRIPH 14: CMP12SS7.CTRIPL 15: CMP12SS7.CTRIPH 16: CMP12SS8.CTRIPL 17: CMP12SS8.CTRIPH 18: CMP12SS9.CTRIPL 19: CMP12SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.151 CFG0_PWMXBAR16_G1 Registers

3.21.151.1 CFG0_G1 Register (Offset = 504h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2703. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1504h

Figure 3-1281. PWMXBAR16_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR16_G1_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR16_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2704. PWMXBAR16_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR16_G1_SEL	R/W	0h	PWM XBar16 G1 Input Select 0: CMP8SS0.CTRIPL 1: CMP8SS0.CTRIPH 2: CMP8SS1.CTRIPL 3: CMP8SS1.CTRIPH 4: CMP8SS2.CTRIPL 5: CMP8SS2.CTRIPH 6: CMP8SS3.CTRIPL 7: CMP8SS3.CTRIPH 8: CMP8SS4.CTRIPL 9: CMP8SS4.CTRIPH 10: CMP8SS5.CTRIPL 11: CMP8SS5.CTRIPH 12: CMP8SS6.CTRIPL 13: CMP8SS6.CTRIPH 14: CMP8SS7.CTRIPL 15: CMP8SS7.CTRIPH 16: CMP8SS8.CTRIPL 17: CMP8SS8.CTRIPH 18: CMP8SS9.CTRIPL 19: CMP8SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.152 CFG0_PWMXBAR16_G2 Registers

3.21.152.1 CFG0_G2 Register (Offset = 508h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2705. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1508h

Figure 3-1282. PWMXBAR16_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PWMXBAR16_G2_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR16_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2706. PWMXBAR16_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	PWMXBAR16_G2_SEL	R/W	0h	PWM XBar16 G2 Input Select 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.21.153 CFG0_PWMXBAR16_G3 Registers

3.21.153.1 CFG0_G3 Register (Offset = 50Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2707. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 150Ch

Figure 3-1283. PWMXBAR16_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR16_G3_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR16_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2708. PWMXBAR16_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR16_G3_SEL	R/W	0h	PWM XBar16 G3 Input Select 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1.EVT4 8: ADC2.EVT1 9: ADC2.EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.21.154 CFG0_PWMXBAR16_G4 Registers

3.21.154.1 CFG0_G4 Register (Offset = 510h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2709. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1510h

Figure 3-1284. PWMXBAR16_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR16_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR16_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2710. PWMXBAR16_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR16_G4_SEL	R/W	0h	PWM XBar16 G4 input bit select. Input source is INPUT XBAR. 1: INPUT XBAR output bit[x] selected 0: INPUT XBAR output bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.155 CFG0_PWMXBAR16_G5 Registers

3.21.155.1 CFG0_G5 Register (Offset = 514h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2711. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1514h

Figure 3-1285. PWMXBAR16_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR16_G5_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR16_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2712. PWMXBAR16_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR16_G5_SEL	R/W	0h	PWM XBar16 G5 input bit select. Input source is PWM TRIPOUT. 1: PWM TRIPOUT bit[x] selected 0: PWM TRIPOUT bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.156 CFG0_PWMXBAR16_G6 Registers

3.21.156.1 CFG0_G6 Register (Offset = 518h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2713. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1518h

Figure 3-1286. PWMXBAR16_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR16_G6_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR16_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2714. PWMXBAR16_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR16_G6_SEL	R/W	0h	PWM XBar16 G6 input bit select. Input source is PWM DEL TRIP 1: PWM DEL TRIP bit[x] selected 0: PWM DEL TRIP bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.157 CFG0_PWMXBAR16_G7 Registers

3.21.157.1 CFG0_G7 Register (Offset = 51Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2715. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 151Ch

Figure 3-1287. PWMXBAR16_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR16_G7_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR16_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2716. PWMXBAR16_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR16_G7_SEL	R/W	0h	PWM XBar16 G7 input bit select. Input source is PWM DEL ACTIVE 1: PWM DEL ACTIVE bit[x] selected 0: PWM DEL ACTIVE bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.158 CFG0_PWMXBAR16_G8 Registers

3.21.158.1 CFG0_G8 Register (Offset = 520h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2717. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1520h

Figure 3-1288. PWMXBAR16_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PWMXBAR16_G8_SEL												
NONE			R/W												
0			0h												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR16_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2718. PWMXBAR16_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:0	PWMXBAR16_G8_SEL	R/W	0h	PWM XBar16 G8 Input Select 0: EQEP0.ERR 1: EQEP1.ERR 2: EQEP2.ERR 6:3: FSIRX0.RX_TRIG4 10:7: FSIRX1.RX_TRIG4 14:11: FSIRX2.RX_TRIG4 18:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT Reset Source: mod_g_rst_n

3.21.159 CFG0_PWMXBAR17_G0 Registers

3.21.159.1 CFG0_G0 Register (Offset = 540h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2719. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1540h

Figure 3-1289. PWMXBAR17_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR17_G0_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR17_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2720. PWMXBAR17_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR17_G0_SEL	R/W	0h	PWM XBar17 G0 Input Select 0: CMP12SS0.CTRIPL 1: CMP12SS0.CTRIPH 2: CMP12SS1.CTRIPL 3: CMP12SS1.CTRIPH 4: CMP12SS2.CTRIPL 5: CMP12SS2.CTRIPH 6: CMP12SS3.CTRIPL 7: CMP12SS3.CTRIPH 8: CMP12SS4.CTRIPL 9: CMP12SS4.CTRIPH 10: CMP12SS5.CTRIPL 11: CMP12SS5.CTRIPH 12: CMP12SS6.CTRIPL 13: CMP12SS6.CTRIPH 14: CMP12SS7.CTRIPL 15: CMP12SS7.CTRIPH 16: CMP12SS8.CTRIPL 17: CMP12SS8.CTRIPH 18: CMP12SS9.CTRIPL 19: CMP12SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.160 CFG0_PWMXBAR17_G1 Registers

3.21.160.1 CFG0_G1 Register (Offset = 544h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2721. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1544h

Figure 3-1290. PWMXBAR17_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR17_G1_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR17_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2722. PWMXBAR17_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR17_G1_SEL	R/W	0h	PWM XBar17 G1 Input Select 0: CMP8SS0.CTRIPL 1: CMP8SS0.CTRIPH 2: CMP8SS1.CTRIPL 3: CMP8SS1.CTRIPH 4: CMP8SS2.CTRIPL 5: CMP8SS2.CTRIPH 6: CMP8SS3.CTRIPL 7: CMP8SS3.CTRIPH 8: CMP8SS4.CTRIPL 9: CMP8SS4.CTRIPH 10: CMP8SS5.CTRIPL 11: CMP8SS5.CTRIPH 12: CMP8SS6.CTRIPL 13: CMP8SS6.CTRIPH 14: CMP8SS7.CTRIPL 15: CMP8SS7.CTRIPH 16: CMP8SS8.CTRIPL 17: CMP8SS8.CTRIPH 18: CMP8SS9.CTRIPL 19: CMP8SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.161 CFG0_PWMXBAR17_G2 Registers

3.21.161.1 CFG0_G2 Register (Offset = 548h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2723. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1548h

Figure 3-1291. PWMXBAR17_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PWMXBAR17_G2_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR17_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2724. PWMXBAR17_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	PWMXBAR17_G2_SEL	R/W	0h	PWM XBar17 G2 Input Select 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.21.162 CFG0_PWMXBAR17_G3 Registers

3.21.162.1 CFG0_G3 Register (Offset = 54Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2725. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 154Ch

Figure 3-1292. PWMXBAR17_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR17_G3_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR17_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2726. PWMXBAR17_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR17_G3_SEL	R/W	0h	PWM XBar17 G3 Input Select 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1.EVT4 8: ADC2.EVT1 9: ADC2.EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.21.163 CFG0_PWMXBAR17_G4 Registers

3.21.163.1 CFG0_G4 Register (Offset = 550h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2727. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1550h

Figure 3-1293. PWMXBAR17_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR17_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR17_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2728. PWMXBAR17_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR17_G4_SEL	R/W	0h	PWM XBar17 G4 input bit select. Input source is INPUT XBAR. 1: INPUT XBAR output bit[x] selected 0: INPUT XBAR output bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.164 CFG0_PWMXBAR17_G5 Registers

3.21.164.1 CFG0_G5 Register (Offset = 554h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2729. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1554h

Figure 3-1294. PWMXBAR17_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR17_G5_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR17_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2730. PWMXBAR17_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR17_G5_SEL	R/W	0h	PWM XBar17 G5 input bit select. Input source is PWM TRIPOUT. 1: PWM TRIPOUT bit[x] selected 0: PWM TRIPOUT bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.165 CFG0_PWMXBAR17_G6 Registers

3.21.165.1 CFG0_G6 Register (Offset = 558h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2731. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1558h

Figure 3-1295. PWMXBAR17_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR17_G6_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR17_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2732. PWMXBAR17_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR17_G6_SEL	R/W	0h	PWM XBar17 G6 input bit select. Input source is PWM DEL TRIP 1: PWM DEL TRIP bit[x] selected 0: PWM DEL TRIP bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.166 CFG0_PWMXBAR17_G7 Registers

3.21.166.1 CFG0_G7 Register (Offset = 55Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2733. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 155Ch

Figure 3-1296. PWMXBAR17_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR17_G7_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR17_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2734. PWMXBAR17_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR17_G7_SEL	R/W	0h	PWM XBar17 G7 input bit select. Input source is PWM DEL ACTIVE 1: PWM DEL ACTIVE bit[x] selected 0: PWM DEL ACTIVE bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.167 CFG0_PWMXBAR17_G8 Registers

3.21.167.1 CFG0_G8 Register (Offset = 560h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2735. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1560h

Figure 3-1297. PWMXBAR17_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PWMXBAR17_G8_SEL												
NONE			R/W												
0			0h												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR17_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2736. PWMXBAR17_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:0	PWMXBAR17_G8_SEL	R/W	0h	PWM XBar17 G8 Input Select 0: EQEP0.ERR 1: EQEP1.ERR 2: EQEP2.ERR 6:3: FSIRX0.RX_TRIG4 10:7: FSIRX1.RX_TRIG4 14:11: FSIRX2.RX_TRIG4 18:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT Reset Source: mod_g_rst_n

3.21.168 CFG0_PWMXBAR18_G0 Registers

3.21.168.1 CFG0_G0 Register (Offset = 580h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2737. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1580h

Figure 3-1298. PWMXBAR18_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR18_G0_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR18_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2738. PWMXBAR18_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR18_G0_SEL	R/W	0h	PWM XBar18 G0 Input Select 0: CMP12SS0.CTRIPL 1: CMP12SS0.CTRIPH 2: CMP12SS1.CTRIPL 3: CMP12SS1.CTRIPH 4: CMP12SS2.CTRIPL 5: CMP12SS2.CTRIPH 6: CMP12SS3.CTRIPL 7: CMP12SS3.CTRIPH 8: CMP12SS4.CTRIPL 9: CMP12SS4.CTRIPH 10: CMP12SS5.CTRIPL 11: CMP12SS5.CTRIPH 12: CMP12SS6.CTRIPL 13: CMP12SS6.CTRIPH 14: CMP12SS7.CTRIPL 15: CMP12SS7.CTRIPH 16: CMP12SS8.CTRIPL 17: CMP12SS8.CTRIPH 18: CMP12SS9.CTRIPL 19: CMP12SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.169 CFG0_PWMXBAR18_G1 Registers

3.21.169.1 CFG0_G1 Register (Offset = 584h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2739. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1584h

Figure 3-1299. PWMXBAR18_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR18_G1_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR18_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2740. PWMXBAR18_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR18_G1_SEL	R/W	0h	PWM XBar18 G1 Input Select 0: CMP8SS0.CTRIPL 1: CMP8SS0.CTRIPH 2: CMP8SS1.CTRIPL 3: CMP8SS1.CTRIPH 4: CMP8SS2.CTRIPL 5: CMP8SS2.CTRIPH 6: CMP8SS3.CTRIPL 7: CMP8SS3.CTRIPH 8: CMP8SS4.CTRIPL 9: CMP8SS4.CTRIPH 10: CMP8SS5.CTRIPL 11: CMP8SS5.CTRIPH 12: CMP8SS6.CTRIPL 13: CMP8SS6.CTRIPH 14: CMP8SS7.CTRIPL 15: CMP8SS7.CTRIPH 16: CMP8SS8.CTRIPL 17: CMP8SS8.CTRIPH 18: CMP8SS9.CTRIPL 19: CMP8SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.170 CFG0_PWMXBAR18_G2 Registers

3.21.170.1 CFG0_G2 Register (Offset = 588h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2741. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1588h

Figure 3-1300. PWMXBAR18_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PWMXBAR18_G2_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR18_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2742. PWMXBAR18_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	PWMXBAR18_G2_SEL	R/W	0h	PWM XBar18 G2 Input Select 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.21.171 CFG0_PWMXBAR18_G3 Registers

3.21.171.1 CFG0_G3 Register (Offset = 58Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2743. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 158Ch

Figure 3-1301. PWMXBAR18_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR18_G3_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR18_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2744. PWMXBAR18_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR18_G3_SEL	R/W	0h	PWM XBar18 G3 Input Select 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1.EVT4 8: ADC2.EVT1 9: ADC2.EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.21.172 CFG0_PWMXBAR18_G4 Registers

3.21.172.1 CFG0_G4 Register (Offset = 590h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2745. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1590h

Figure 3-1302. PWMXBAR18_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR18_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR18_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2746. PWMXBAR18_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR18_G4_SEL	R/W	0h	PWM XBar18 G4 input bit select. Input source is INPUT XBAR. 1: INPUT XBAR output bit[x] selected 0: INPUT XBAR output bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.173 CFG0_PWMXBAR18_G5 Registers

3.21.173.1 CFG0_G5 Register (Offset = 594h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2747. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1594h

Figure 3-1303. PWMXBAR18_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR18_G5_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR18_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2748. PWMXBAR18_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR18_G5_SEL	R/W	0h	PWM XBar18 G5 input bit select. Input source is PWM TRIPOUT. 1: PWM TRIPOUT bit[x] selected 0: PWM TRIPOUT bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.174 CFG0_PWMXBAR18_G6 Registers

3.21.174.1 CFG0_G6 Register (Offset = 598h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2749. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1598h

Figure 3-1304. PWMXBAR18_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR18_G6_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR18_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2750. PWMXBAR18_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR18_G6_SEL	R/W	0h	PWM XBar18 G6 input bit select. Input source is PWM DEL TRIP 1: PWM DEL TRIP bit[x] selected 0: PWM DEL TRIP bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.175 CFG0_PWMXBAR18_G7 Registers

3.21.175.1 CFG0_G7 Register (Offset = 59Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2751. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 159Ch

Figure 3-1305. PWMXBAR18_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR18_G7_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR18_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2752. PWMXBAR18_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR18_G7_SEL	R/W	0h	PWM XBar18 G7 input bit select. Input source is PWM DEL ACTIVE 1: PWM DEL ACTIVE bit[x] selected 0: PWM DEL ACTIVE bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.176 CFG0_PWMXBAR18_G8 Registers

3.21.176.1 CFG0_G8 Register (Offset = 5A0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2753. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 15A0h

Figure 3-1306. PWMXBAR18_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PWMXBAR18_G8_SEL												
NONE			R/W												
0			0h												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR18_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2754. PWMXBAR18_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:0	PWMXBAR18_G8_SEL	R/W	0h	PWM XBar18 G8 Input Select 0: EQEP0.ERR 1: EQEP1.ERR 2: EQEP2.ERR 6:3: FSIRX0.RX_TRIG4 10:7: FSIRX1.RX_TRIG4 14:11: FSIRX2.RX_TRIG4 18:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT Reset Source: mod_g_rst_n

3.21.177 CFG0_PWMXBAR19_G0 Registers

3.21.177.1 CFG0_G0 Register (Offset = 5C0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2755. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 15C0h

Figure 3-1307. PWMXBAR19_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR19_G0_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR19_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2756. PWMXBAR19_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR19_G0_SEL	R/W	0h	PWM XBar19 G0 Input Select 0: CMP12SS0.CTRIPL 1: CMP12SS0.CTRIPH 2: CMP12SS1.CTRIPL 3: CMP12SS1.CTRIPH 4: CMP12SS2.CTRIPL 5: CMP12SS2.CTRIPH 6: CMP12SS3.CTRIPL 7: CMP12SS3.CTRIPH 8: CMP12SS4.CTRIPL 9: CMP12SS4.CTRIPH 10: CMP12SS5.CTRIPL 11: CMP12SS5.CTRIPH 12: CMP12SS6.CTRIPL 13: CMP12SS6.CTRIPH 14: CMP12SS7.CTRIPL 15: CMP12SS7.CTRIPH 16: CMP12SS8.CTRIPL 17: CMP12SS8.CTRIPH 18: CMP12SS9.CTRIPL 19: CMP12SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.178 CFG0_PWMXBAR19_G1 Registers

3.21.178.1 CFG0_G1 Register (Offset = 5C4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2757. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 15C4h

Figure 3-1308. PWMXBAR19_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR19_G1_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR19_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2758. PWMXBAR19_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR19_G1_SEL	R/W	0h	PWM XBar19 G1 Input Select 0: CMP8SS0.CTRIPL 1: CMP8SS0.CTRIPH 2: CMP8SS1.CTRIPL 3: CMP8SS1.CTRIPH 4: CMP8SS2.CTRIPL 5: CMP8SS2.CTRIPH 6: CMP8SS3.CTRIPL 7: CMP8SS3.CTRIPH 8: CMP8SS4.CTRIPL 9: CMP8SS4.CTRIPH 10: CMP8SS5.CTRIPL 11: CMP8SS5.CTRIPH 12: CMP8SS6.CTRIPL 13: CMP8SS6.CTRIPH 14: CMP8SS7.CTRIPL 15: CMP8SS7.CTRIPH 16: CMP8SS8.CTRIPL 17: CMP8SS8.CTRIPH 18: CMP8SS9.CTRIPL 19: CMP8SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.179 CFG0_PWMXBAR19_G2 Registers

3.21.179.1 CFG0_G2 Register (Offset = 5C8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2759. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 15C8h

Figure 3-1309. PWMXBAR19_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PWMXBAR19_G2_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR19_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2760. PWMXBAR19_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	PWMXBAR19_G2_SEL	R/W	0h	PWM XBar19 G2 Input Select 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.21.180 CFG0_PWMXBAR19_G3 Registers

3.21.180.1 CFG0_G3 Register (Offset = 5CCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2761. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 15CCh

Figure 3-1310. PWMXBAR19_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR19_G3_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR19_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2762. PWMXBAR19_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR19_G3_SEL	R/W	0h	PWM XBar19 G3 Input Select 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1.EVT4 8: ADC2.EVT1 9: ADC2.EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.21.181 CFG0_PWMXBAR19_G4 Registers

3.21.181.1 CFG0_G4 Register (Offset = 5D0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2763. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 15D0h

Figure 3-1311. PWMXBAR19_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR19_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR19_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2764. PWMXBAR19_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR19_G4_SEL	R/W	0h	PWM XBar19 G4 input bit select. Input source is INPUT XBAR. 1: INPUT XBAR output bit[x] selected 0: INPUT XBAR output bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.182 CFG0_PWMXBAR19_G5 Registers

3.21.182.1 CFG0_G5 Register (Offset = 5D4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2765. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 15D4h

Figure 3-1312. PWMXBAR19_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR19_G5_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR19_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2766. PWMXBAR19_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR19_G5_SEL	R/W	0h	PWM XBar19 G5 input bit select. Input source is PWM TRIPOUT. 1: PWM TRIPOUT bit[x] selected 0: PWM TRIPOUT bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.183 CFG0_PWMXBAR19_G6 Registers

3.21.183.1 CFG0_G6 Register (Offset = 5D8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2767. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 15D8h

Figure 3-1313. PWMXBAR19_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR19_G6_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR19_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2768. PWMXBAR19_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR19_G6_SEL	R/W	0h	PWM XBar19 G6 input bit select. Input source is PWM DEL TRIP 1: PWM DEL TRIP bit[x] selected 0: PWM DEL TRIP bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.184 CFG0_PWMXBAR19_G7 Registers

3.21.184.1 CFG0_G7 Register (Offset = 5DCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2769. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 15DCh

Figure 3-1314. PWMXBAR19_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR19_G7_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR19_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2770. PWMXBAR19_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR19_G7_SEL	R/W	0h	PWM XBar19 G7 input bit select. Input source is PWM DEL ACTIVE 1: PWM DEL ACTIVE bit[x] selected 0: PWM DEL ACTIVE bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.185 CFG0_PWMXBAR19_G8 Registers

3.21.185.1 CFG0_G8 Register (Offset = 5E0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2771. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 15E0h

Figure 3-1315. PWMXBAR19_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PWMXBAR19_G8_SEL												
NONE			R/W												
0			0h												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR19_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2772. PWMXBAR19_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:0	PWMXBAR19_G8_SEL	R/W	0h	PWM XBar19 G8 Input Select 0: EQEP0.ERR 1: EQEP1.ERR 2: EQEP2.ERR 6:3: FSIRX0.RX_TRIG4 10:7: FSIRX1.RX_TRIG4 14:11: FSIRX2.RX_TRIG4 18:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT Reset Source: mod_g_rst_n

3.21.186 CFG0_PWMXBAR20_G0 Registers

3.21.186.1 CFG0_G0 Register (Offset = 600h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2773. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1600h

Figure 3-1316. PWMXBAR20_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR20_G0_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR20_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2774. PWMXBAR20_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR20_G0_SEL	R/W	0h	PWM XBar20 G0 Input Select 0: CMP12SS0.CTRIPL 1: CMP12SS0.CTRIPH 2: CMP12SS1.CTRIPL 3: CMP12SS1.CTRIPH 4: CMP12SS2.CTRIPL 5: CMP12SS2.CTRIPH 6: CMP12SS3.CTRIPL 7: CMP12SS3.CTRIPH 8: CMP12SS4.CTRIPL 9: CMP12SS4.CTRIPH 10: CMP12SS5.CTRIPL 11: CMP12SS5.CTRIPH 12: CMP12SS6.CTRIPL 13: CMP12SS6.CTRIPH 14: CMP12SS7.CTRIPL 15: CMP12SS7.CTRIPH 16: CMP12SS8.CTRIPL 17: CMP12SS8.CTRIPH 18: CMP12SS9.CTRIPL 19: CMP12SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.187 CFG0_PWMXBAR20_G1 Registers

3.21.187.1 CFG0_G1 Register (Offset = 604h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2775. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1604h

Figure 3-1317. PWMXBAR20_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR20_G1_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR20_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2776. PWMXBAR20_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR20_G1_SEL	R/W	0h	PWM XBar20 G1 Input Select 0: CMP8SS0.CTRIPL 1: CMP8SS0.CTRIPH 2: CMP8SS1.CTRIPL 3: CMP8SS1.CTRIPH 4: CMP8SS2.CTRIPL 5: CMP8SS2.CTRIPH 6: CMP8SS3.CTRIPL 7: CMP8SS3.CTRIPH 8: CMP8SS4.CTRIPL 9: CMP8SS4.CTRIPH 10: CMP8SS5.CTRIPL 11: CMP8SS5.CTRIPH 12: CMP8SS6.CTRIPL 13: CMP8SS6.CTRIPH 14: CMP8SS7.CTRIPL 15: CMP8SS7.CTRIPH 16: CMP8SS8.CTRIPL 17: CMP8SS8.CTRIPH 18: CMP8SS9.CTRIPL 19: CMP8SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.188 CFG0_PWMXBAR20_G2 Registers

3.21.188.1 CFG0_G2 Register (Offset = 608h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2777. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1608h

Figure 3-1318. PWMXBAR20_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PWMXBAR20_G2_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR20_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2778. PWMXBAR20_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	PWMXBAR20_G2_SEL	R/W	0h	PWM XBar20 G2 Input Select 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.21.189 CFG0_PWMXBAR20_G3 Registers

3.21.189.1 CFG0_G3 Register (Offset = 60Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2779. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 160Ch

Figure 3-1319. PWMXBAR20_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR20_G3_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR20_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2780. PWMXBAR20_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR20_G3_SEL	R/W	0h	PWM XBar20 G3 Input Select 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1.EVT4 8: ADC2.EVT1 9: ADC2.EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.21.190 CFG0_PWMXBAR20_G4 Registers

3.21.190.1 CFG0_G4 Register (Offset = 610h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2781. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1610h

Figure 3-1320. PWMXBAR20_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR20_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR20_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2782. PWMXBAR20_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR20_G4_SEL	R/W	0h	PWM XBar20 G4 input bit select. Input source is INPUT XBAR. 1: INPUT XBAR output bit[x] selected 0: INPUT XBAR output bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.191 CFG0_PWMXBAR20_G5 Registers

3.21.191.1 CFG0_G5 Register (Offset = 614h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2783. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1614h

Figure 3-1321. PWMXBAR20_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR20_G5_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR20_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2784. PWMXBAR20_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR20_G5_SEL	R/W	0h	PWM XBar20 G5 input bit select. Input source is PWM TRIPOUT. 1: PWM TRIPOUT bit[x] selected 0: PWM TRIPOUT bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.192 CFG0_PWMXBAR20_G6 Registers

3.21.192.1 CFG0_G6 Register (Offset = 618h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2785. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1618h

Figure 3-1322. PWMXBAR20_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR20_G6_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR20_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2786. PWMXBAR20_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR20_G6_SEL	R/W	0h	PWM XBar20 G6 input bit select. Input source is PWM DEL TRIP 1: PWM DEL TRIP bit[x] selected 0: PWM DEL TRIP bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.193 CFG0_PWMXBAR20_G7 Registers

3.21.193.1 CFG0_G7 Register (Offset = 61Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2787. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 161Ch

Figure 3-1323. PWMXBAR20_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR20_G7_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR20_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2788. PWMXBAR20_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR20_G7_SEL	R/W	0h	PWM XBar20 G7 input bit select. Input source is PWM DEL ACTIVE 1: PWM DEL ACTIVE bit[x] selected 0: PWM DEL ACTIVE bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.194 CFG0_PWMXBAR20_G8 Registers

3.21.194.1 CFG0_G8 Register (Offset = 620h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2789. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1620h

Figure 3-1324. PWMXBAR20_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PWMXBAR20_G8_SEL												
NONE			R/W												
0			0h												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR20_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2790. PWMXBAR20_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:0	PWMXBAR20_G8_SEL	R/W	0h	PWM XBar20 G8 Input Select 0: EQEP0.ERR 1: EQEP1.ERR 2: EQEP2.ERR 6:3: FSIRX0.RX_TRIG4 10:7: FSIRX1.RX_TRIG4 14:11: FSIRX2.RX_TRIG4 18:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT Reset Source: mod_g_rst_n

3.21.195 CFG0_PWMXBAR21_G0 Registers

3.21.195.1 CFG0_G0 Register (Offset = 640h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2791. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1640h

Figure 3-1325. PWMXBAR21_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR21_G0_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR21_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2792. PWMXBAR21_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR21_G0_SEL	R/W	0h	PWM XBar21 G0 Input Select 0: CMP12SS0.CTRIPL 1: CMP12SS0.CTRIPH 2: CMP12SS1.CTRIPL 3: CMP12SS1.CTRIPH 4: CMP12SS2.CTRIPL 5: CMP12SS2.CTRIPH 6: CMP12SS3.CTRIPL 7: CMP12SS3.CTRIPH 8: CMP12SS4.CTRIPL 9: CMP12SS4.CTRIPH 10: CMP12SS5.CTRIPL 11: CMP12SS5.CTRIPH 12: CMP12SS6.CTRIPL 13: CMP12SS6.CTRIPH 14: CMP12SS7.CTRIPL 15: CMP12SS7.CTRIPH 16: CMP12SS8.CTRIPL 17: CMP12SS8.CTRIPH 18: CMP12SS9.CTRIPL 19: CMP12SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.196 CFG0_PWMXBAR21_G1 Registers

3.21.196.1 CFG0_G1 Register (Offset = 644h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2793. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1644h

Figure 3-1326. PWMXBAR21_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR21_G1_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR21_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2794. PWMXBAR21_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR21_G1_SEL	R/W	0h	PWM XBar21 G1 Input Select 0: CMP8SS0.CTRIPL 1: CMP8SS0.CTRIPH 2: CMP8SS1.CTRIPL 3: CMP8SS1.CTRIPH 4: CMP8SS2.CTRIPL 5: CMP8SS2.CTRIPH 6: CMP8SS3.CTRIPL 7: CMP8SS3.CTRIPH 8: CMP8SS4.CTRIPL 9: CMP8SS4.CTRIPH 10: CMP8SS5.CTRIPL 11: CMP8SS5.CTRIPH 12: CMP8SS6.CTRIPL 13: CMP8SS6.CTRIPH 14: CMP8SS7.CTRIPL 15: CMP8SS7.CTRIPH 16: CMP8SS8.CTRIPL 17: CMP8SS8.CTRIPH 18: CMP8SS9.CTRIPL 19: CMP8SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.197 CFG0_PWMXBAR21_G2 Registers

3.21.197.1 CFG0_G2 Register (Offset = 648h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2795. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1648h

Figure 3-1327. PWMXBAR21_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PWMXBAR21_G2_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR21_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2796. PWMXBAR21_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	PWMXBAR21_G2_SEL	R/W	0h	PWM XBar21 G2 Input Select 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.21.198 CFG0_PWMXBAR21_G3 Registers

3.21.198.1 CFG0_G3 Register (Offset = 64Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2797. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 164Ch

Figure 3-1328. PWMXBAR21_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR21_G3_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR21_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2798. PWMXBAR21_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR21_G3_SEL	R/W	0h	PWM XBar21 G3 Input Select 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1.EVT4 8: ADC2.EVT1 9: ADC2.EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.21.199 CFG0_PWMXBAR21_G4 Registers

3.21.199.1 CFG0_G4 Register (Offset = 650h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2799. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1650h

Figure 3-1329. PWMXBAR21_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR21_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR21_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2800. PWMXBAR21_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR21_G4_SEL	R/W	0h	PWM XBar21 G4 input bit select. Input source is INPUT XBAR. 1: INPUT XBAR output bit[x] selected 0: INPUT XBAR output bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.200 CFG0_PWMXBAR21_G5 Registers

3.21.200.1 CFG0_G5 Register (Offset = 654h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2801. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1654h

Figure 3-1330. PWMXBAR21_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR21_G5_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR21_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2802. PWMXBAR21_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR21_G5_SEL	R/W	0h	PWM XBar21 G5 input bit select. Input source is PWM TRIPOUT. 1: PWM TRIPOUT bit[x] selected 0: PWM TRIPOUT bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.201 CFG0_PWMXBAR21_G6 Registers

3.21.201.1 CFG0_G6 Register (Offset = 658h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2803. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1658h

Figure 3-1331. PWMXBAR21_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR21_G6_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR21_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2804. PWMXBAR21_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR21_G6_SEL	R/W	0h	PWM XBar21 G6 input bit select. Input source is PWM DEL TRIP 1: PWM DEL TRIP bit[x] selected 0: PWM DEL TRIP bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.202 CFG0_PWMXBAR21_G7 Registers

3.21.202.1 CFG0_G7 Register (Offset = 65Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2805. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 165Ch

Figure 3-1332. PWMXBAR21_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR21_G7_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR21_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2806. PWMXBAR21_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR21_G7_SEL	R/W	0h	PWM XBar21 G7 input bit select. Input source is PWM DEL ACTIVE 1: PWM DEL ACTIVE bit[x] selected 0: PWM DEL ACTIVE bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.203 CFG0_PWMXBAR21_G8 Registers

3.21.203.1 CFG0_G8 Register (Offset = 660h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2807. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1660h

Figure 3-1333. PWMXBAR21_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PWMXBAR21_G8_SEL												
NONE			R/W												
0			0h												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR21_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2808. PWMXBAR21_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:0	PWMXBAR21_G8_SEL	R/W	0h	PWM XBar21 G8 Input Select 0: EQEP0.ERR 1: EQEP1.ERR 2: EQEP2.ERR 6:3: FSIRX0.RX_TRIG4 10:7: FSIRX1.RX_TRIG4 14:11: FSIRX2.RX_TRIG4 18:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT Reset Source: mod_g_rst_n

3.21.204 CFG0_PWMXBAR22_G0 Registers

3.21.204.1 CFG0_G0 Register (Offset = 680h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2809. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1680h

Figure 3-1334. PWMXBAR22_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR22_G0_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR22_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2810. PWMXBAR22_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR22_G0_SEL	R/W	0h	PWM XBar22 G0 Input Select 0: CMP12SS0.CTRIPL 1: CMP12SS0.CTRIPH 2: CMP12SS1.CTRIPL 3: CMP12SS1.CTRIPH 4: CMP12SS2.CTRIPL 5: CMP12SS2.CTRIPH 6: CMP12SS3.CTRIPL 7: CMP12SS3.CTRIPH 8: CMP12SS4.CTRIPL 9: CMP12SS4.CTRIPH 10: CMP12SS5.CTRIPL 11: CMP12SS5.CTRIPH 12: CMP12SS6.CTRIPL 13: CMP12SS6.CTRIPH 14: CMP12SS7.CTRIPL 15: CMP12SS7.CTRIPH 16: CMP12SS8.CTRIPL 17: CMP12SS8.CTRIPH 18: CMP12SS9.CTRIPL 19: CMP12SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.205 CFG0_PWMXBAR22_G1 Registers

3.21.205.1 CFG0_G1 Register (Offset = 684h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2811. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1684h

Figure 3-1335. PWMXBAR22_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR22_G1_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR22_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2812. PWMXBAR22_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR22_G1_SEL	R/W	0h	PWM XBar22 G1 Input Select 0: CMP8SS0.CTRIPL 1: CMP8SS0.CTRIPH 2: CMP8SS1.CTRIPL 3: CMP8SS1.CTRIPH 4: CMP8SS2.CTRIPL 5: CMP8SS2.CTRIPH 6: CMP8SS3.CTRIPL 7: CMP8SS3.CTRIPH 8: CMP8SS4.CTRIPL 9: CMP8SS4.CTRIPH 10: CMP8SS5.CTRIPL 11: CMP8SS5.CTRIPH 12: CMP8SS6.CTRIPL 13: CMP8SS6.CTRIPH 14: CMP8SS7.CTRIPL 15: CMP8SS7.CTRIPH 16: CMP8SS8.CTRIPL 17: CMP8SS8.CTRIPH 18: CMP8SS9.CTRIPL 19: CMP8SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.206 CFG0_PWMXBAR22_G2 Registers

3.21.206.1 CFG0_G2 Register (Offset = 688h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2813. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1688h

Figure 3-1336. PWMXBAR22_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PWMXBAR22_G2_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR22_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2814. PWMXBAR22_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	PWMXBAR22_G2_SEL	R/W	0h	PWM XBar22 G2 Input Select 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.21.207 CFG0_PWMXBAR22_G3 Registers

3.21.207.1 CFG0_G3 Register (Offset = 68Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2815. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 168Ch

Figure 3-1337. PWMXBAR22_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR22_G3_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR22_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2816. PWMXBAR22_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR22_G3_SEL	R/W	0h	PWM XBar22 G3 Input Select 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1.EVT4 8: ADC2.EVT1 9: ADC2.EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.21.208 CFG0_PWMXBAR22_G4 Registers

3.21.208.1 CFG0_G4 Register (Offset = 690h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2817. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1690h

Figure 3-1338. PWMXBAR22_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR22_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR22_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2818. PWMXBAR22_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR22_G4_SEL	R/W	0h	PWM XBar22 G4 input bit select. Input source is INPUT XBAR. 1: INPUT XBAR output bit[x] selected 0: INPUT XBAR output bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.209 CFG0_PWMXBAR22_G5 Registers

3.21.209.1 CFG0_G5 Register (Offset = 694h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2819. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1694h

Figure 3-1339. PWMXBAR22_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR22_G5_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR22_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2820. PWMXBAR22_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR22_G5_SEL	R/W	0h	PWM XBar22 G5 input bit select. Input source is PWM TRIPOUT. 1: PWM TRIPOUT bit[x] selected 0: PWM TRIPOUT bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.210 CFG0_PWMXBAR22_G6 Registers

3.21.210.1 CFG0_G6 Register (Offset = 698h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2821. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1698h

Figure 3-1340. PWMXBAR22_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR22_G6_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR22_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2822. PWMXBAR22_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR22_G6_SEL	R/W	0h	PWM XBar22 G6 input bit select. Input source is PWM DEL TRIP 1: PWM DEL TRIP bit[x] selected 0: PWM DEL TRIP bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.211 CFG0_PWMXBAR22_G7 Registers

3.21.211.1 CFG0_G7 Register (Offset = 69Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2823. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 169Ch

Figure 3-1341. PWMXBAR22_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR22_G7_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR22_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2824. PWMXBAR22_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR22_G7_SEL	R/W	0h	PWM XBar22 G7 input bit select. Input source is PWM DEL ACTIVE 1: PWM DEL ACTIVE bit[x] selected 0: PWM DEL ACTIVE bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.212 CFG0_PWMXBAR22_G8 Registers

3.21.212.1 CFG0_G8 Register (Offset = 6A0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2825. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 16A0h

Figure 3-1342. PWMXBAR22_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PWMXBAR22_G8_SEL												
NONE			R/W												
0			0h												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR22_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2826. PWMXBAR22_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:0	PWMXBAR22_G8_SEL	R/W	0h	PWM XBar22 G8 Input Select 0: EQEP0.ERR 1: EQEP1.ERR 2: EQEP2.ERR 6:3: FSIRX0.RX_TRIG4 10:7: FSIRX1.RX_TRIG4 14:11: FSIRX2.RX_TRIG4 18:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT Reset Source: mod_g_rst_n

3.21.213 CFG0_PWMXBAR23_G0 Registers

3.21.213.1 CFG0_G0 Register (Offset = 6C0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2827. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 16C0h

Figure 3-1343. PWMXBAR23_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR23_G0_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR23_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2828. PWMXBAR23_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR23_G0_SEL	R/W	0h	PWM XBar23 G0 Input Select 0: CMP12SS0.CTRIPL 1: CMP12SS0.CTRIPH 2: CMP12SS1.CTRIPL 3: CMP12SS1.CTRIPH 4: CMP12SS2.CTRIPL 5: CMP12SS2.CTRIPH 6: CMP12SS3.CTRIPL 7: CMP12SS3.CTRIPH 8: CMP12SS4.CTRIPL 9: CMP12SS4.CTRIPH 10: CMP12SS5.CTRIPL 11: CMP12SS5.CTRIPH 12: CMP12SS6.CTRIPL 13: CMP12SS6.CTRIPH 14: CMP12SS7.CTRIPL 15: CMP12SS7.CTRIPH 16: CMP12SS8.CTRIPL 17: CMP12SS8.CTRIPH 18: CMP12SS9.CTRIPL 19: CMP12SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.214 CFG0_PWMXBAR23_G1 Registers

3.21.214.1 CFG0_G1 Register (Offset = 6C4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2829. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 16C4h

Figure 3-1344. PWMXBAR23_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR23_G1_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR23_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2830. PWMXBAR23_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR23_G1_SEL	R/W	0h	PWM XBar23 G1 Input Select 0: CMP8SS0.CTRIPL 1: CMP8SS0.CTRIPH 2: CMP8SS1.CTRIPL 3: CMP8SS1.CTRIPH 4: CMP8SS2.CTRIPL 5: CMP8SS2.CTRIPH 6: CMP8SS3.CTRIPL 7: CMP8SS3.CTRIPH 8: CMP8SS4.CTRIPL 9: CMP8SS4.CTRIPH 10: CMP8SS5.CTRIPL 11: CMP8SS5.CTRIPH 12: CMP8SS6.CTRIPL 13: CMP8SS6.CTRIPH 14: CMP8SS7.CTRIPL 15: CMP8SS7.CTRIPH 16: CMP8SS8.CTRIPL 17: CMP8SS8.CTRIPH 18: CMP8SS9.CTRIPL 19: CMP8SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.215 CFG0_PWMXBAR23_G2 Registers

3.21.215.1 CFG0_G2 Register (Offset = 6C8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2831. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 16C8h

Figure 3-1345. PWMXBAR23_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PWMXBAR23_G2_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR23_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2832. PWMXBAR23_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	PWMXBAR23_G2_SEL	R/W	0h	PWM XBar23 G2 Input Select 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.21.216 CFG0_PWMXBAR23_G3 Registers

3.21.216.1 CFG0_G3 Register (Offset = 6CCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2833. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 16CCh

Figure 3-1346. PWMXBAR23_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR23_G3_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR23_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2834. PWMXBAR23_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR23_G3_SEL	R/W	0h	PWM XBar23 G3 Input Select 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1.EVT4 8: ADC2.EVT1 9: ADC2.EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.21.217 CFG0_PWMXBAR23_G4 Registers

3.21.217.1 CFG0_G4 Register (Offset = 6D0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2835. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 16D0h

Figure 3-1347. PWMXBAR23_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR23_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR23_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2836. PWMXBAR23_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR23_G4_SEL	R/W	0h	PWM XBar23 G4 input bit select. Input source is INPUT XBAR. 1: INPUT XBAR output bit[x] selected 0: INPUT XBAR output bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.218 CFG0_PWMXBAR23_G5 Registers

3.21.218.1 CFG0_G5 Register (Offset = 6D4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2837. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 16D4h

Figure 3-1348. PWMXBAR23_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR23_G5_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR23_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2838. PWMXBAR23_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR23_G5_SEL	R/W	0h	PWM XBar23 G5 input bit select. Input source is PWM TRIPOUT. 1: PWM TRIPOUT bit[x] selected 0: PWM TRIPOUT bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.219 CFG0_PWMXBAR23_G6 Registers

3.21.219.1 CFG0_G6 Register (Offset = 6D8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2839. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 16D8h

Figure 3-1349. PWMXBAR23_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR23_G6_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR23_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2840. PWMXBAR23_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR23_G6_SEL	R/W	0h	PWM XBar23 G6 input bit select. Input source is PWM DEL TRIP 1: PWM DEL TRIP bit[x] selected 0: PWM DEL TRIP bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.220 CFG0_PWMXBAR23_G7 Registers

3.21.220.1 CFG0_G7 Register (Offset = 6DCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2841. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 16DCh

Figure 3-1350. PWMXBAR23_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR23_G7_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR23_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2842. PWMXBAR23_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR23_G7_SEL	R/W	0h	PWM XBar23 G7 input bit select. Input source is PWM DEL ACTIVE 1: PWM DEL ACTIVE bit[x] selected 0: PWM DEL ACTIVE bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.221 CFG0_PWMXBAR23_G8 Registers

3.21.221.1 CFG0_G8 Register (Offset = 6E0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2843. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 16E0h

Figure 3-1351. PWMXBAR23_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PWMXBAR23_G8_SEL												
NONE			R/W												
0			0h												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR23_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2844. PWMXBAR23_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:0	PWMXBAR23_G8_SEL	R/W	0h	PWM XBar23 G8 Input Select 0: EQEP0.ERR 1: EQEP1.ERR 2: EQEP2.ERR 6:3: FSIRX0.RX_TRIG4 10:7: FSIRX1.RX_TRIG4 14:11: FSIRX2.RX_TRIG4 18:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT Reset Source: mod_g_rst_n

3.21.222 CFG0_PWMXBAR24_G0 Registers

3.21.222.1 CFG0_G0 Register (Offset = 700h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2845. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1700h

Figure 3-1352. PWMXBAR24_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR24_G0_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR24_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2846. PWMXBAR24_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR24_G0_SEL	R/W	0h	PWM XBar24 G0 Input Select 0: CMP12SS0.CTRIPL 1: CMP12SS0.CTRIPH 2: CMP12SS1.CTRIPL 3: CMP12SS1.CTRIPH 4: CMP12SS2.CTRIPL 5: CMP12SS2.CTRIPH 6: CMP12SS3.CTRIPL 7: CMP12SS3.CTRIPH 8: CMP12SS4.CTRIPL 9: CMP12SS4.CTRIPH 10: CMP12SS5.CTRIPL 11: CMP12SS5.CTRIPH 12: CMP12SS6.CTRIPL 13: CMP12SS6.CTRIPH 14: CMP12SS7.CTRIPL 15: CMP12SS7.CTRIPH 16: CMP12SS8.CTRIPL 17: CMP12SS8.CTRIPH 18: CMP12SS9.CTRIPL 19: CMP12SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.223 CFG0_PWMXBAR24_G1 Registers

3.21.223.1 CFG0_G1 Register (Offset = 704h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2847. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1704h

Figure 3-1353. PWMXBAR24_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR24_G1_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR24_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2848. PWMXBAR24_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR24_G1_SEL	R/W	0h	PWM XBar24 G1 Input Select 0: CMP8SS0.CTRIPL 1: CMP8SS0.CTRIPH 2: CMP8SS1.CTRIPL 3: CMP8SS1.CTRIPH 4: CMP8SS2.CTRIPL 5: CMP8SS2.CTRIPH 6: CMP8SS3.CTRIPL 7: CMP8SS3.CTRIPH 8: CMP8SS4.CTRIPL 9: CMP8SS4.CTRIPH 10: CMP8SS5.CTRIPL 11: CMP8SS5.CTRIPH 12: CMP8SS6.CTRIPL 13: CMP8SS6.CTRIPH 14: CMP8SS7.CTRIPL 15: CMP8SS7.CTRIPH 16: CMP8SS8.CTRIPL 17: CMP8SS8.CTRIPH 18: CMP8SS9.CTRIPL 19: CMP8SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.224 CFG0_PWMXBAR24_G2 Registers

3.21.224.1 CFG0_G2 Register (Offset = 708h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2849. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1708h

Figure 3-1354. PWMXBAR24_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PWMXBAR24_G2_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR24_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2850. PWMXBAR24_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	PWMXBAR24_G2_SEL	R/W	0h	PWM XBar24 G2 Input Select 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.21.225 CFG0_PWMXBAR24_G3 Registers

3.21.225.1 CFG0_G3 Register (Offset = 70Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2851. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 170Ch

Figure 3-1355. PWMXBAR24_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR24_G3_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR24_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2852. PWMXBAR24_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR24_G3_SEL	R/W	0h	PWM XBar24 G3 Input Select 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1.EVT4 8: ADC2.EVT1 9: ADC2.EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.21.226 CFG0_PWMXBAR24_G4 Registers

3.21.226.1 CFG0_G4 Register (Offset = 710h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2853. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1710h

Figure 3-1356. PWMXBAR24_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR24_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR24_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2854. PWMXBAR24_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR24_G4_SEL	R/W	0h	PWM XBar24 G4 input bit select. Input source is INPUT XBAR. 1: INPUT XBAR output bit[x] selected 0: INPUT XBAR output bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.227 CFG0_PWMXBAR24_G5 Registers

3.21.227.1 CFG0_G5 Register (Offset = 714h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2855. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1714h

Figure 3-1357. PWMXBAR24_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR24_G5_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR24_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2856. PWMXBAR24_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR24_G5_SEL	R/W	0h	PWM XBar24 G5 input bit select. Input source is PWM TRIPOUT. 1: PWM TRIPOUT bit[x] selected 0: PWM TRIPOUT bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.228 CFG0_PWMXBAR24_G6 Registers

3.21.228.1 CFG0_G6 Register (Offset = 718h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2857. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1718h

Figure 3-1358. PWMXBAR24_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR24_G6_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR24_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2858. PWMXBAR24_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR24_G6_SEL	R/W	0h	PWM XBar24 G6 input bit select. Input source is PWM DEL TRIP 1: PWM DEL TRIP bit[x] selected 0: PWM DEL TRIP bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.229 CFG0_PWMXBAR24_G7 Registers

3.21.229.1 CFG0_G7 Register (Offset = 71Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2859. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 171Ch

Figure 3-1359. PWMXBAR24_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR24_G7_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR24_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2860. PWMXBAR24_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR24_G7_SEL	R/W	0h	PWM XBar24 G7 input bit select. Input source is PWM DEL ACTIVE 1: PWM DEL ACTIVE bit[x] selected 0: PWM DEL ACTIVE bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.230 CFG0_PWMXBAR24_G8 Registers

3.21.230.1 CFG0_G8 Register (Offset = 720h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2861. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1720h

Figure 3-1360. PWMXBAR24_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PWMXBAR24_G8_SEL												
NONE			R/W												
0			0h												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR24_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2862. PWMXBAR24_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:0	PWMXBAR24_G8_SEL	R/W	0h	PWM XBar24 G8 Input Select 0: EQEP0.ERR 1: EQEP1.ERR 2: EQEP2.ERR 6:3: FSIRX0.RX_TRIG4 10:7: FSIRX1.RX_TRIG4 14:11: FSIRX2.RX_TRIG4 18:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT Reset Source: mod_g_rst_n

3.21.231 CFG0_PWMXBAR25_G0 Registers

3.21.231.1 CFG0_G0 Register (Offset = 740h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2863. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1740h

Figure 3-1361. PWMXBAR25_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR25_G0_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR25_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2864. PWMXBAR25_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR25_G0_SEL	R/W	0h	PWM XBar25 G0 Input Select 0: CMP12SS0.CTRIPL 1: CMP12SS0.CTRIPH 2: CMP12SS1.CTRIPL 3: CMP12SS1.CTRIPH 4: CMP12SS2.CTRIPL 5: CMP12SS2.CTRIPH 6: CMP12SS3.CTRIPL 7: CMP12SS3.CTRIPH 8: CMP12SS4.CTRIPL 9: CMP12SS4.CTRIPH 10: CMP12SS5.CTRIPL 11: CMP12SS5.CTRIPH 12: CMP12SS6.CTRIPL 13: CMP12SS6.CTRIPH 14: CMP12SS7.CTRIPL 15: CMP12SS7.CTRIPH 16: CMP12SS8.CTRIPL 17: CMP12SS8.CTRIPH 18: CMP12SS9.CTRIPL 19: CMP12SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.232 CFG0_PWMXBAR25_G1 Registers

3.21.232.1 CFG0_G1 Register (Offset = 744h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2865. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1744h

Figure 3-1362. PWMXBAR25_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR25_G1_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR25_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2866. PWMXBAR25_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR25_G1_SEL	R/W	0h	PWM XBar25 G1 Input Select 0: CMP8SS0.CTRIPL 1: CMP8SS0.CTRIPH 2: CMP8SS1.CTRIPL 3: CMP8SS1.CTRIPH 4: CMP8SS2.CTRIPL 5: CMP8SS2.CTRIPH 6: CMP8SS3.CTRIPL 7: CMP8SS3.CTRIPH 8: CMP8SS4.CTRIPL 9: CMP8SS4.CTRIPH 10: CMP8SS5.CTRIPL 11: CMP8SS5.CTRIPH 12: CMP8SS6.CTRIPL 13: CMP8SS6.CTRIPH 14: CMP8SS7.CTRIPL 15: CMP8SS7.CTRIPH 16: CMP8SS8.CTRIPL 17: CMP8SS8.CTRIPH 18: CMP8SS9.CTRIPL 19: CMP8SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.233 CFG0_PWMXBAR25_G2 Registers

3.21.233.1 CFG0_G2 Register (Offset = 748h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2867. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1748h

Figure 3-1363. PWMXBAR25_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PWMXBAR25_G2_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR25_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2868. PWMXBAR25_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	PWMXBAR25_G2_SEL	R/W	0h	PWM XBar25 G2 Input Select 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.21.234 CFG0_PWMXBAR25_G3 Registers

3.21.234.1 CFG0_G3 Register (Offset = 74Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2869. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 174Ch

Figure 3-1364. PWMXBAR25_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR25_G3_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR25_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2870. PWMXBAR25_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR25_G3_SEL	R/W	0h	PWM XBar25 G3 Input Select 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1.EVT4 8: ADC2.EVT1 9: ADC2.EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.21.235 CFG0_PWMXBAR25_G4 Registers

3.21.235.1 CFG0_G4 Register (Offset = 750h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2871. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1750h

Figure 3-1365. PWMXBAR25_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR25_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR25_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2872. PWMXBAR25_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR25_G4_SEL	R/W	0h	PWM XBar25 G4 input bit select. Input source is INPUT XBAR. 1: INPUT XBAR output bit[x] selected 0: INPUT XBAR output bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.236 CFG0_PWMXBAR25_G5 Registers

3.21.236.1 CFG0_G5 Register (Offset = 754h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2873. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1754h

Figure 3-1366. PWMXBAR25_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR25_G5_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR25_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2874. PWMXBAR25_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR25_G5_SEL	R/W	0h	PWM XBar25 G5 input bit select. Input source is PWM TRIPOUT. 1: PWM TRIPOUT bit[x] selected 0: PWM TRIPOUT bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.237 CFG0_PWMXBAR25_G6 Registers

3.21.237.1 CFG0_G6 Register (Offset = 758h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2875. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1758h

Figure 3-1367. PWMXBAR25_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR25_G6_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR25_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2876. PWMXBAR25_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR25_G6_SEL	R/W	0h	PWM XBar25 G6 input bit select. Input source is PWM DEL TRIP 1: PWM DEL TRIP bit[x] selected 0: PWM DEL TRIP bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.238 CFG0_PWMXBAR25_G7 Registers

3.21.238.1 CFG0_G7 Register (Offset = 75Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2877. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 175Ch

Figure 3-1368. PWMXBAR25_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR25_G7_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR25_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2878. PWMXBAR25_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR25_G7_SEL	R/W	0h	PWM XBar25 G7 input bit select. Input source is PWM DEL ACTIVE 1: PWM DEL ACTIVE bit[x] selected 0: PWM DEL ACTIVE bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.239 CFG0_PWMXBAR25_G8 Registers

3.21.239.1 CFG0_G8 Register (Offset = 760h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2879. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1760h

Figure 3-1369. PWMXBAR25_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PWMXBAR25_G8_SEL												
NONE			R/W												
0			0h												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR25_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2880. PWMXBAR25_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:0	PWMXBAR25_G8_SEL	R/W	0h	PWM XBar25 G8 Input Select 0: EQEP0.ERR 1: EQEP1.ERR 2: EQEP2.ERR 6:3: FSIRX0.RX_TRIG4 10:7: FSIRX1.RX_TRIG4 14:11: FSIRX2.RX_TRIG4 18:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT Reset Source: mod_g_rst_n

3.21.240 CFG0_PWMXBAR26_G0 Registers

3.21.240.1 CFG0_G0 Register (Offset = 780h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2881. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1780h

Figure 3-1370. PWMXBAR26_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR26_G0_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR26_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2882. PWMXBAR26_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR26_G0_SEL	R/W	0h	PWM XBar26 G0 Input Select 0: CMP12SS0.CTRIPL 1: CMP12SS0.CTRIPH 2: CMP12SS1.CTRIPL 3: CMP12SS1.CTRIPH 4: CMP12SS2.CTRIPL 5: CMP12SS2.CTRIPH 6: CMP12SS3.CTRIPL 7: CMP12SS3.CTRIPH 8: CMP12SS4.CTRIPL 9: CMP12SS4.CTRIPH 10: CMP12SS5.CTRIPL 11: CMP12SS5.CTRIPH 12: CMP12SS6.CTRIPL 13: CMP12SS6.CTRIPH 14: CMP12SS7.CTRIPL 15: CMP12SS7.CTRIPH 16: CMP12SS8.CTRIPL 17: CMP12SS8.CTRIPH 18: CMP12SS9.CTRIPL 19: CMP12SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.241 CFG0_PWMXBAR26_G1 Registers

3.21.241.1 CFG0_G1 Register (Offset = 784h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2883. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1784h

Figure 3-1371. PWMXBAR26_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR26_G1_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR26_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2884. PWMXBAR26_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR26_G1_SEL	R/W	0h	PWM XBar26 G1 Input Select 0: CMP8SS0.CTRIPL 1: CMP8SS0.CTRIPH 2: CMP8SS1.CTRIPL 3: CMP8SS1.CTRIPH 4: CMP8SS2.CTRIPL 5: CMP8SS2.CTRIPH 6: CMP8SS3.CTRIPL 7: CMP8SS3.CTRIPH 8: CMP8SS4.CTRIPL 9: CMP8SS4.CTRIPH 10: CMP8SS5.CTRIPL 11: CMP8SS5.CTRIPH 12: CMP8SS6.CTRIPL 13: CMP8SS6.CTRIPH 14: CMP8SS7.CTRIPL 15: CMP8SS7.CTRIPH 16: CMP8SS8.CTRIPL 17: CMP8SS8.CTRIPH 18: CMP8SS9.CTRIPL 19: CMP8SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.242 CFG0_PWMXBAR26_G2 Registers

3.21.242.1 CFG0_G2 Register (Offset = 788h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2885. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1788h

Figure 3-1372. PWMXBAR26_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PWMXBAR26_G2_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR26_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2886. PWMXBAR26_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	PWMXBAR26_G2_SEL	R/W	0h	PWM XBar26 G2 Input Select 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.21.243 CFG0_PWMXBAR26_G3 Registers

3.21.243.1 CFG0_G3 Register (Offset = 78Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2887. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 178Ch

Figure 3-1373. PWMXBAR26_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR26_G3_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR26_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2888. PWMXBAR26_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR26_G3_SEL	R/W	0h	PWM XBar26 G3 Input Select 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1.EVT4 8: ADC2.EVT1 9: ADC2.EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.21.244 CFG0_PWMXBAR26_G4 Registers

3.21.244.1 CFG0_G4 Register (Offset = 790h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2889. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1790h

Figure 3-1374. PWMXBAR26_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR26_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR26_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2890. PWMXBAR26_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR26_G4_SEL	R/W	0h	PWM XBar26 G4 input bit select. Input source is INPUT XBAR. 1: INPUT XBAR output bit[x] selected 0: INPUT XBAR output bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.245 CFG0_PWMXBAR26_G5 Registers

3.21.245.1 CFG0_G5 Register (Offset = 794h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2891. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1794h

Figure 3-1375. PWMXBAR26_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR26_G5_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR26_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2892. PWMXBAR26_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR26_G5_SEL	R/W	0h	PWM XBar26 G5 input bit select. Input source is PWM TRIPOUT. 1: PWM TRIPOUT bit[x] selected 0: PWM TRIPOUT bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.246 CFG0_PWMXBAR26_G6 Registers

3.21.246.1 CFG0_G6 Register (Offset = 798h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2893. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1798h

Figure 3-1376. PWMXBAR26_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR26_G6_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR26_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2894. PWMXBAR26_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR26_G6_SEL	R/W	0h	PWM XBar26 G6 input bit select. Input source is PWM DEL TRIP 1: PWM DEL TRIP bit[x] selected 0: PWM DEL TRIP bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.247 CFG0_PWMXBAR26_G7 Registers

3.21.247.1 CFG0_G7 Register (Offset = 79Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2895. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 179Ch

Figure 3-1377. PWMXBAR26_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR26_G7_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR26_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2896. PWMXBAR26_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR26_G7_SEL	R/W	0h	PWM XBar26 G7 input bit select. Input source is PWM DEL ACTIVE 1: PWM DEL ACTIVE bit[x] selected 0: PWM DEL ACTIVE bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.248 CFG0_PWMXBAR26_G8 Registers

3.21.248.1 CFG0_G8 Register (Offset = 7A0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2897. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 17A0h

Figure 3-1378. PWMXBAR26_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PWMXBAR26_G8_SEL												
NONE			R/W												
0			0h												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR26_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2898. PWMXBAR26_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:0	PWMXBAR26_G8_SEL	R/W	0h	PWM XBar26 G8 Input Select 0: EQEP0.ERR 1: EQEP1.ERR 2: EQEP2.ERR 6:3: FSIRX0.RX_TRIG4 10:7: FSIRX1.RX_TRIG4 14:11: FSIRX2.RX_TRIG4 18:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT Reset Source: mod_g_rst_n

3.21.249 CFG0_PWMXBAR27_G0 Registers

3.21.249.1 CFG0_G0 Register (Offset = 7C0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2899. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 17C0h

Figure 3-1379. PWMXBAR27_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR27_G0_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR27_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2900. PWMXBAR27_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR27_G0_SEL	R/W	0h	PWM XBar27 G0 Input Select 0: CMP12SS0.CTRIPL 1: CMP12SS0.CTRIPH 2: CMP12SS1.CTRIPL 3: CMP12SS1.CTRIPH 4: CMP12SS2.CTRIPL 5: CMP12SS2.CTRIPH 6: CMP12SS3.CTRIPL 7: CMP12SS3.CTRIPH 8: CMP12SS4.CTRIPL 9: CMP12SS4.CTRIPH 10: CMP12SS5.CTRIPL 11: CMP12SS5.CTRIPH 12: CMP12SS6.CTRIPL 13: CMP12SS6.CTRIPH 14: CMP12SS7.CTRIPL 15: CMP12SS7.CTRIPH 16: CMP12SS8.CTRIPL 17: CMP12SS8.CTRIPH 18: CMP12SS9.CTRIPL 19: CMP12SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.250 CFG0_PWMXBAR27_G1 Registers

3.21.250.1 CFG0_G1 Register (Offset = 7C4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2901. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 17C4h

Figure 3-1380. PWMXBAR27_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR27_G1_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR27_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2902. PWMXBAR27_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR27_G1_SEL	R/W	0h	PWM XBar27 G1 Input Select 0: CMP8SS0.CTRIPL 1: CMP8SS0.CTRIPH 2: CMP8SS1.CTRIPL 3: CMP8SS1.CTRIPH 4: CMP8SS2.CTRIPL 5: CMP8SS2.CTRIPH 6: CMP8SS3.CTRIPL 7: CMP8SS3.CTRIPH 8: CMP8SS4.CTRIPL 9: CMP8SS4.CTRIPH 10: CMP8SS5.CTRIPL 11: CMP8SS5.CTRIPH 12: CMP8SS6.CTRIPL 13: CMP8SS6.CTRIPH 14: CMP8SS7.CTRIPL 15: CMP8SS7.CTRIPH 16: CMP8SS8.CTRIPL 17: CMP8SS8.CTRIPH 18: CMP8SS9.CTRIPL 19: CMP8SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.251 CFG0_PWMXBAR27_G2 Registers

3.21.251.1 CFG0_G2 Register (Offset = 7C8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2903. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 17C8h

Figure 3-1381. PWMXBAR27_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PWMXBAR27_G2_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR27_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2904. PWMXBAR27_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	PWMXBAR27_G2_SEL	R/W	0h	PWM XBar27 G2 Input Select 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.21.252 CFG0_PWMXBAR27_G3 Registers

3.21.252.1 CFG0_G3 Register (Offset = 7CCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2905. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 17CCh

Figure 3-1382. PWMXBAR27_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR27_G3_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR27_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2906. PWMXBAR27_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR27_G3_SEL	R/W	0h	PWM XBar27 G3 Input Select 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1.EVT4 8: ADC2.EVT1 9: ADC2.EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.21.253 CFG0_PWMXBAR27_G4 Registers

3.21.253.1 CFG0_G4 Register (Offset = 7D0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2907. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 17D0h

Figure 3-1383. PWMXBAR27_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR27_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR27_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2908. PWMXBAR27_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR27_G4_SEL	R/W	0h	PWM XBar27 G4 input bit select. Input source is INPUT XBAR. 1: INPUT XBAR output bit[x] selected 0: INPUT XBAR output bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.254 CFG0_PWMXBAR27_G5 Registers

3.21.254.1 CFG0_G5 Register (Offset = 7D4h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2909. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 17D4h

Figure 3-1384. PWMXBAR27_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR27_G5_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR27_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2910. PWMXBAR27_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR27_G5_SEL	R/W	0h	PWM XBar27 G5 input bit select. Input source is PWM TRIPOUT. 1: PWM TRIPOUT bit[x] selected 0: PWM TRIPOUT bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.255 CFG0_PWMXBAR27_G6 Registers

3.21.255.1 CFG0_G6 Register (Offset = 7D8h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2911. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 17D8h

Figure 3-1385. PWMXBAR27_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR27_G6_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR27_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2912. PWMXBAR27_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR27_G6_SEL	R/W	0h	PWM XBar27 G6 input bit select. Input source is PWM DEL TRIP 1: PWM DEL TRIP bit[x] selected 0: PWM DEL TRIP bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.256 CFG0_PWMXBAR27_G7 Registers

3.21.256.1 CFG0_G7 Register (Offset = 7DCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2913. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 17DCh

Figure 3-1386. PWMXBAR27_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR27_G7_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR27_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2914. PWMXBAR27_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR27_G7_SEL	R/W	0h	PWM XBar27 G7 input bit select. Input source is PWM DEL ACTIVE 1: PWM DEL ACTIVE bit[x] selected 0: PWM DEL ACTIVE bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.257 CFG0_PWMXBAR27_G8 Registers

3.21.257.1 CFG0_G8 Register (Offset = 7E0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2915. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 17E0h

Figure 3-1387. PWMXBAR27_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PWMXBAR27_G8_SEL												
NONE			R/W												
0			0h												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR27_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2916. PWMXBAR27_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:0	PWMXBAR27_G8_SEL	R/W	0h	PWM XBar27 G8 Input Select 0: EQEP0.ERR 1: EQEP1.ERR 2: EQEP2.ERR 6:3: FSIRX0.RX_TRIG4 10:7: FSIRX1.RX_TRIG4 14:11: FSIRX2.RX_TRIG4 18:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT Reset Source: mod_g_rst_n

3.21.258 CFG0_PWMXBAR28_G0 Registers

3.21.258.1 CFG0_G0 Register (Offset = 800h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2917. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1800h

Figure 3-1388. PWMXBAR28_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR28_G0_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR28_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2918. PWMXBAR28_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR28_G0_SEL	R/W	0h	PWM XBar28 G0 Input Select 0: CMP12SS0.CTRIPL 1: CMP12SS0.CTRIPH 2: CMP12SS1.CTRIPL 3: CMP12SS1.CTRIPH 4: CMP12SS2.CTRIPL 5: CMP12SS2.CTRIPH 6: CMP12SS3.CTRIPL 7: CMP12SS3.CTRIPH 8: CMP12SS4.CTRIPL 9: CMP12SS4.CTRIPH 10: CMP12SS5.CTRIPL 11: CMP12SS5.CTRIPH 12: CMP12SS6.CTRIPL 13: CMP12SS6.CTRIPH 14: CMP12SS7.CTRIPL 15: CMP12SS7.CTRIPH 16: CMP12SS8.CTRIPL 17: CMP12SS8.CTRIPH 18: CMP12SS9.CTRIPL 19: CMP12SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.259 CFG0_PWMXBAR28_G1 Registers

3.21.259.1 CFG0_G1 Register (Offset = 804h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2919. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1804h

Figure 3-1389. PWMXBAR28_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR28_G1_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR28_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2920. PWMXBAR28_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR28_G1_SEL	R/W	0h	PWM XBar28 G1 Input Select 0: CMP8SS0.CTRIPL 1: CMP8SS0.CTRIPH 2: CMP8SS1.CTRIPL 3: CMP8SS1.CTRIPH 4: CMP8SS2.CTRIPL 5: CMP8SS2.CTRIPH 6: CMP8SS3.CTRIPL 7: CMP8SS3.CTRIPH 8: CMP8SS4.CTRIPL 9: CMP8SS4.CTRIPH 10: CMP8SS5.CTRIPL 11: CMP8SS5.CTRIPH 12: CMP8SS6.CTRIPL 13: CMP8SS6.CTRIPH 14: CMP8SS7.CTRIPL 15: CMP8SS7.CTRIPH 16: CMP8SS8.CTRIPL 17: CMP8SS8.CTRIPH 18: CMP8SS9.CTRIPL 19: CMP8SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.260 CFG0_PWMXBAR28_G2 Registers

3.21.260.1 CFG0_G2 Register (Offset = 808h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2921. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1808h

Figure 3-1390. PWMXBAR28_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PWMXBAR28_G2_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR28_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2922. PWMXBAR28_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	PWMXBAR28_G2_SEL	R/W	0h	PWM XBar28 G2 Input Select 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.21.261 CFG0_PWMXBAR28_G3 Registers

3.21.261.1 CFG0_G3 Register (Offset = 80Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2923. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 180Ch

Figure 3-1391. PWMXBAR28_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR28_G3_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR28_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2924. PWMXBAR28_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR28_G3_SEL	R/W	0h	PWM XBar28 G3 Input Select 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1.EVT4 8: ADC2.EVT1 9: ADC2.EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.21.262 CFG0_PWMXBAR28_G4 Registers

3.21.262.1 CFG0_G4 Register (Offset = 810h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2925. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1810h

Figure 3-1392. PWMXBAR28_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR28_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR28_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2926. PWMXBAR28_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR28_G4_SEL	R/W	0h	PWM XBar28 G4 input bit select. Input source is INPUT XBAR. 1: INPUT XBAR output bit[x] selected 0: INPUT XBAR output bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.263 CFG0_PWMXBAR28_G5 Registers

3.21.263.1 CFG0_G5 Register (Offset = 814h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2927. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1814h

Figure 3-1393. PWMXBAR28_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR28_G5_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR28_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2928. PWMXBAR28_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR28_G5_SEL	R/W	0h	PWM XBar28 G5 input bit select. Input source is PWM TRIPOUT. 1: PWM TRIPOUT bit[x] selected 0: PWM TRIPOUT bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.264 CFG0_PWMXBAR28_G6 Registers

3.21.264.1 CFG0_G6 Register (Offset = 818h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2929. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1818h

Figure 3-1394. PWMXBAR28_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR28_G6_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR28_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2930. PWMXBAR28_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR28_G6_SEL	R/W	0h	PWM XBar28 G6 input bit select. Input source is PWM DEL TRIP 1: PWM DEL TRIP bit[x] selected 0: PWM DEL TRIP bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.265 CFG0_PWMXBAR28_G7 Registers

3.21.265.1 CFG0_G7 Register (Offset = 81Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2931. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 181Ch

Figure 3-1395. PWMXBAR28_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR28_G7_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR28_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2932. PWMXBAR28_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR28_G7_SEL	R/W	0h	PWM XBar28 G7 input bit select. Input source is PWM DEL ACTIVE 1: PWM DEL ACTIVE bit[x] selected 0: PWM DEL ACTIVE bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.266 CFG0_PWMXBAR28_G8 Registers

3.21.266.1 CFG0_G8 Register (Offset = 820h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2933. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1820h

Figure 3-1396. PWMXBAR28_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PWMXBAR28_G8_SEL												
NONE			R/W												
0			0h												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR28_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2934. PWMXBAR28_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:0	PWMXBAR28_G8_SEL	R/W	0h	PWM XBar28 G8 Input Select 0: EQEP0.ERR 1: EQEP1.ERR 2: EQEP2.ERR 6:3: FSIRX0.RX_TRIG4 10:7: FSIRX1.RX_TRIG4 14:11: FSIRX2.RX_TRIG4 18:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT Reset Source: mod_g_rst_n

3.21.267 CFG0_PWMXBAR29_G0 Registers

3.21.267.1 CFG0_G0 Register (Offset = 840h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2935. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1840h

Figure 3-1397. PWMXBAR29_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR29_G0_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR29_G0_SEL															
R/W															
0h															

Access Types Legend

Table 3-2936. PWMXBAR29_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR29_G0_SEL	R/W	0h	PWM XBar29 G0 Input Select 0: CMP12SS0.CTRIPL 1: CMP12SS0.CTRIPH 2: CMP12SS1.CTRIPL 3: CMP12SS1.CTRIPH 4: CMP12SS2.CTRIPL 5: CMP12SS2.CTRIPH 6: CMP12SS3.CTRIPL 7: CMP12SS3.CTRIPH 8: CMP12SS4.CTRIPL 9: CMP12SS4.CTRIPH 10: CMP12SS5.CTRIPL 11: CMP12SS5.CTRIPH 12: CMP12SS6.CTRIPL 13: CMP12SS6.CTRIPH 14: CMP12SS7.CTRIPL 15: CMP12SS7.CTRIPH 16: CMP12SS8.CTRIPL 17: CMP12SS8.CTRIPH 18: CMP12SS9.CTRIPL 19: CMP12SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.268 CFG0_PWMXBAR29_G1 Registers

3.21.268.1 CFG0_G1 Register (Offset = 844h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2937. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1844h

Figure 3-1398. PWMXBAR29_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR29_G1_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR29_G1_SEL															
R/W															
0h															

Access Types Legend

Table 3-2938. PWMXBAR29_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR29_G1_SEL	R/W	0h	PWM XBar29 G1 Input Select 0: CMP8SS0.CTRIPL 1: CMP8SS0.CTRIPH 2: CMP8SS1.CTRIPL 3: CMP8SS1.CTRIPH 4: CMP8SS2.CTRIPL 5: CMP8SS2.CTRIPH 6: CMP8SS3.CTRIPL 7: CMP8SS3.CTRIPH 8: CMP8SS4.CTRIPL 9: CMP8SS4.CTRIPH 10: CMP8SS5.CTRIPL 11: CMP8SS5.CTRIPH 12: CMP8SS6.CTRIPL 13: CMP8SS6.CTRIPH 14: CMP8SS7.CTRIPL 15: CMP8SS7.CTRIPH 16: CMP8SS8.CTRIPL 17: CMP8SS8.CTRIPH 18: CMP8SS9.CTRIPL 19: CMP8SS9.CTRIPH Reset Source: mod_g_rst_n

3.21.269 CFG0_PWMXBAR29_G2 Registers

3.21.269.1 CFG0_G2 Register (Offset = 848h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2939. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1848h

Figure 3-1399. PWMXBAR29_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PWMXBAR29_G2_SEL							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR29_G2_SEL															
R/W															
0h															

Access Types Legend

Table 3-2940. PWMXBAR29_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	PWMXBAR29_G2_SEL	R/W	0h	PWM XBar29 G2 Input Select 0: SDFM0.FILT1CEVT1 1: SDFM0.FILT1CEVT2 2: SDFM0.FILT1COMPHZ 3: SDFM0.FILT2CEVT1 4: SDFM0.FILT2CEVT2 5: SDFM0.FILT2COMPHZ 6: SDFM0.FILT3CEVT1 7: SDFM0.FILT3CEVT2 8: SDFM0.FILT3COMPHZ 9: SDFM0.FILT4CEVT1 10: SDFM0.FILT4CEVT2 11: SDFM0.FILT4COMPHZ 12: SDFM1.FILT1CEVT1 13: SDFM1.FILT1CEVT2 14: SDFM1.FILT1COMPHZ 15: SDFM1.FILT2CEVT1 16: SDFM1.FILT2CEVT2 17: SDFM1.FILT2COMPHZ 18: SDFM1.FILT3CEVT1 19: SDFM1.FILT3CEVT2 20: SDFM1.FILT3COMPHZ 21: SDFM1.FILT4CEVT1 22: SDFM1.FILT4CEVT2 23: SDFM1.FILT4COMPHZ Reset Source: mod_g_rst_n

3.21.270 CFG0_PWMXBAR29_G3 Registers

3.21.270.1 CFG0_G3 Register (Offset = 84Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2941. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 184Ch

Figure 3-1400. PWMXBAR29_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PWMXBAR29_G3_SEL			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR29_G3_SEL															
R/W															
0h															

Access Types Legend

Table 3-2942. PWMXBAR29_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	PWMXBAR29_G3_SEL	R/W	0h	PWM XBar29 G3 Input Select 1: ADC0.EVT2 2: ADC0.EVT3 3: ADC0.EVT4 4: ADC1.EVT1 5: ADC1.EVT2 6: ADC1.EVT3 7: ADC1.EVT4 8: ADC2.EVT1 9: ADC2.EVT2 10: ADC2.EVT3 11: ADC2.EVT4 12: ADC3.EVT1 13: ADC3.EVT2 14: ADC3.EVT3 15: ADC3.EVT4 16: ADC4.EVT1 17: ADC4.EVT2 18: ADC4.EVT3 19: ADC4.EVT4 Reset Source: mod_g_rst_n

3.21.271 CFG0_PWMXBAR29_G4 Registers

3.21.271.1 CFG0_G4 Register (Offset = 850h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2943. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1850h

Figure 3-1401. PWMXBAR29_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR29_G4_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR29_G4_SEL															
R/W															
0h															

Access Types Legend

Table 3-2944. PWMXBAR29_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR29_G4_SEL	R/W	0h	PWM XBar29 G4 input bit select. Input source is INPUT XBAR. 1: INPUT XBAR output bit[x] selected 0: INPUT XBAR output bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.272 CFG0_PWMXBAR29_G5 Registers

3.21.272.1 CFG0_G5 Register (Offset = 854h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2945. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1854h

Figure 3-1402. PWMXBAR29_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR29_G5_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR29_G5_SEL															
R/W															
0h															

Access Types Legend

Table 3-2946. PWMXBAR29_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR29_G5_SEL	R/W	0h	PWM XBar29 G5 input bit select. Input source is PWM TRIPOUT. 1: PWM TRIPOUT bit[x] selected 0: PWM TRIPOUT bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.273 CFG0_PWMXBAR29_G6 Registers

3.21.273.1 CFG0_G6 Register (Offset = 858h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2947. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1858h

Figure 3-1403. PWMXBAR29_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR29_G6_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR29_G6_SEL															
R/W															
0h															

Access Types Legend

Table 3-2948. PWMXBAR29_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR29_G6_SEL	R/W	0h	PWM XBar29 G6 input bit select. Input source is PWM DEL TRIP 1: PWM DEL TRIP bit[x] selected 0: PWM DEL TRIP bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.274 CFG0_PWMXBAR29_G7 Registers

3.21.274.1 CFG0_G7 Register (Offset = 85Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2949. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 185Ch

Figure 3-1404. PWMXBAR29_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWMXBAR29_G7_SEL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR29_G7_SEL															
R/W															
0h															

Access Types Legend

Table 3-2950. PWMXBAR29_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR29_G7_SEL	R/W	0h	PWM XBar29 G7 input bit select. Input source is PWM DEL ACTIVE 1: PWM DEL ACTIVE bit[x] selected 0: PWM DEL ACTIVE bit[x] is de-selected Reset Source: mod_g_rst_n

3.21.275 CFG0_PWMXBAR29_G8 Registers

3.21.275.1 CFG0_G8 Register (Offset = 860h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 3-2951. Instance Table

Instance Name	Physical Address
PWMXBAR_MMR0	502D 1860h

Figure 3-1405. PWMXBAR29_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PWMXBAR29_G8_SEL												
NONE			R/W												
0			0h												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMXBAR29_G8_SEL															
R/W															
0h															

Access Types Legend

Table 3-2952. PWMXBAR29_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:0	PWMXBAR29_G8_SEL	R/W	0h	PWM XBar29 G8 Input Select 0: EQEP0.ERR 1: EQEP1.ERR 2: EQEP2.ERR 6:3: FSIRX0.RX_TRIG4 10:7: FSIRX1.RX_TRIG4 14:11: FSIRX2.RX_TRIG4 18:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT Reset Source: mod_g_rst_n

3.21.276 Access Table

Table 3-2953. Access Type Codes

Access Type	Code	Description
R	R	Read
R/W	R/W	Read / Write
R/W1TC	R/W1TC	Read/Write 1 To Clear

3.22 SDFM Registers

Table 3-2954. MEM, MEM Registers, Base Address=0X0000000050268000, Length=4096

Offset	Length	Register Name	sdfm0 Physical Address	sdfm1 Physical Address
0h	32	SDIFLG	5026 8000h	5026 9000h
4h	32	SDIFLGCLR	5026 8004h	5026 9004h
8h	16	SDCTL	5026 8008h	5026 9008h
Ch	16	SDMFILEN	5026 800Ch	5026 900Ch
Eh	16	SDSTATUS	5026 800Eh	5026 900Eh
20h	16	SDCTLPARM1	5026 8020h	5026 9020h
22h	16	SDDFPARM1	5026 8022h	5026 9022h
24h	16	SDDPARM1	5026 8024h	5026 9024h
26h	16	SDFLT1CMPH1	5026 8026h	5026 9026h
28h	16	SDFLT1CMPL1	5026 8028h	5026 9028h
2Ah	16	SDCPARM1	5026 802Ah	5026 902Ah
2Ch	32	SDDATA1	5026 802Ch	5026 902Ch
30h	32	SDDATFIFO1	5026 8030h	5026 9030h
34h	16	SDCDATA1	5026 8034h	5026 9034h
36h	16	SDFLT1CMPH2	5026 8036h	5026 9036h
38h	16	SDFLT1CMPHZ	5026 8038h	5026 9038h
3Ah	16	SDFIFOCTL1	5026 803Ah	5026 903Ah
3Ch	16	SDSYNC1	5026 803Ch	5026 903Ch
3Eh	16	SDFLT1CMPL2	5026 803Eh	5026 903Eh
40h	16	SDCTLPARM2	5026 8040h	5026 9040h
42h	16	SDDFPARM2	5026 8042h	5026 9042h
44h	16	SDDPARM2	5026 8044h	5026 9044h
46h	16	SDFLT2CMPH1	5026 8046h	5026 9046h
48h	16	SDFLT2CMPL1	5026 8048h	5026 9048h
4Ah	16	SDCPARM2	5026 804Ah	5026 904Ah
4Ch	32	SDDATA2	5026 804Ch	5026 904Ch
50h	32	SDDATFIFO2	5026 8050h	5026 9050h
54h	16	SDCDATA2	5026 8054h	5026 9054h
56h	16	SDFLT2CMPH2	5026 8056h	5026 9056h
58h	16	SDFLT2CMPHZ	5026 8058h	5026 9058h
5Ah	16	SDFIFOCTL2	5026 805Ah	5026 905Ah
5Ch	16	SDSYNC2	5026 805Ch	5026 905Ch
5Eh	16	SDFLT2CMPL2	5026 805Eh	5026 905Eh
60h	16	SDCTLPARM3	5026 8060h	5026 9060h
62h	16	SDDFPARM3	5026 8062h	5026 9062h
64h	16	SDDPARM3	5026 8064h	5026 9064h
66h	16	SDFLT3CMPH1	5026 8066h	5026 9066h
68h	16	SDFLT3CMPL1	5026 8068h	5026 9068h
6Ah	16	SDCPARM3	5026 806Ah	5026 906Ah
6Ch	32	SDDATA3	5026 806Ch	5026 906Ch
70h	32	SDDATFIFO3	5026 8070h	5026 9070h
74h	16	SDCDATA3	5026 8074h	5026 9074h
76h	16	SDFLT3CMPH2	5026 8076h	5026 9076h
78h	16	SDFLT3CMPHZ	5026 8078h	5026 9078h
7Ah	16	SDFIFOCTL3	5026 807Ah	5026 907Ah

Table 3-2954. MEM, MEM Registers, Base Address=0X0000000050268000, Length=4096 (continued)

Offset	Length	Register Name	sdfm0 Physical Address	sdfm1 Physical Address
7Ch	16	SDSYNC3	5026 807Ch	5026 907Ch
7Eh	16	SDFLT3CMPL2	5026 807Eh	5026 907Eh
80h	16	SDCTLPARM4	5026 8080h	5026 9080h
82h	16	SDDFPARM4	5026 8082h	5026 9082h
84h	16	SDDPARM4	5026 8084h	5026 9084h
86h	16	SDFLT4CMPH1	5026 8086h	5026 9086h
88h	16	SDFLT4CMPL1	5026 8088h	5026 9088h
8Ah	16	SDCPARM4	5026 808Ah	5026 908Ah
8Ch	32	SDDATA4	5026 808Ch	5026 908Ch
90h	32	SDDATFIFO4	5026 8090h	5026 9090h
94h	16	SDCDATA4	5026 8094h	5026 9094h
96h	16	SDFLT4CMPH2	5026 8096h	5026 9096h
98h	16	SDFLT4CMPHZ	5026 8098h	5026 9098h
9Ah	16	SDFIFOCTL4	5026 809Ah	5026 909Ah
9Ch	16	SDSYNC4	5026 809Ch	5026 909Ch
9Eh	16	SDFLT4CMPL2	5026 809Eh	5026 909Eh
C0h	16	SDCOMP1CTL	5026 80C0h	5026 90C0h
C2h	16	SDCOMP1EVT2FLTCTL	5026 80C2h	5026 90C2h
C4h	16	SDCOMP1EVT2FLTCLKCTL	5026 80C4h	5026 90C4h
C6h	16	SDCOMP1EVT1FLTCTL	5026 80C6h	5026 90C6h
C8h	16	SDCOMP1EVT1FLTCLKCTL	5026 80C8h	5026 90C8h
CEh	16	SDCOMP1LOCK	5026 80CEh	5026 90CEh
D0h	16	SDCOMP2CTL	5026 80D0h	5026 90D0h
D2h	16	SDCOMP2EVT2FLTCTL	5026 80D2h	5026 90D2h
D4h	16	SDCOMP2EVT2FLTCLKCTL	5026 80D4h	5026 90D4h
D6h	16	SDCOMP2EVT1FLTCTL	5026 80D6h	5026 90D6h
D8h	16	SDCOMP2EVT1FLTCLKCTL	5026 80D8h	5026 90D8h
DEh	16	SDCOMP2LOCK	5026 80DEh	5026 90DEh
E0h	16	SDCOMP3CTL	5026 80E0h	5026 90E0h
E2h	16	SDCOMP3EVT2FLTCTL	5026 80E2h	5026 90E2h
E4h	16	SDCOMP3EVT2FLTCLKCTL	5026 80E4h	5026 90E4h
E6h	16	SDCOMP3EVT1FLTCTL	5026 80E6h	5026 90E6h
E8h	16	SDCOMP3EVT1FLTCLKCTL	5026 80E8h	5026 90E8h
EEh	16	SDCOMP3LOCK	5026 80EEh	5026 90EEh
F0h	16	SDCOMP4CTL	5026 80F0h	5026 90F0h
F2h	16	SDCOMP4EVT2FLTCTL	5026 80F2h	5026 90F2h
F4h	16	SDCOMP4EVT2FLTCLKCTL	5026 80F4h	5026 90F4h
F6h	16	SDCOMP4EVT1FLTCTL	5026 80F6h	5026 90F6h
F8h	16	SDCOMP4EVT1FLTCLKCTL	5026 80F8h	5026 90F8h
FEh	16	SDCOMP4LOCK	5026 80FEh	5026 90FEh

3.22.1 MEM_SDIFLG Registers

3.22.1.1 MEM_SDIFLG Register (Offset = 0h) [reset = 0h]

Short Description: SD Interrupt Flag Registe

Long Description: SD Interrupt Flag Register

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Table 3-2955. Instance Table

Instance Name	Physical Address
SDFM0	5026 8000h
SDFM1	5026 9000h

Figure 3-1406. SDIFLG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MIF	RESERVED_1							SDFFINT4	SDFFINT3	SDFFINT2	SDFFINT1	SDFFOVF4	SDFFOVF3	SDFFOVF2	SDFFOVF1
R	R							R	R	R	R	R	R	R	R
0h	0h							0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AF4	AF3	AF2	AF1	MF4	MF3	MF2	MF1	FLT4_FLG_CEVT2	FLT4_FLG_CEVT1	FLT3_FLG_CEVT2	FLT3_FLG_CEVT1	FLT2_FLG_CEVT2	FLT2_FLG_CEVT1	FLT1_FLG_CEVT2	FLT1_FLG_CEVT1
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 3-2956. SDIFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MIF	R	0h	Set whenever any "error" interrupt [MF1-4,IFL1-4,IFH1-4,SDFFOVF1-4] is active Reset Source: sdfm_rst_mod_g_rst_n
30:24	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
23	SDFFINT4	R	0h	SDFIFO data ready interrupt for Ch4 Reset Source: sdfm_rst_mod_g_rst_n
22	SDFFINT3	R	0h	SDFIFO data ready interrupt for Ch3 Reset Source: sdfm_rst_mod_g_rst_n
21	SDFFINT2	R	0h	SDFIFO data ready interrupt for Ch2 Reset Source: sdfm_rst_mod_g_rst_n
20	SDFFINT1	R	0h	SDFIFO data ready interrupt for Ch1 0: SDFIFO data ready interrupt has NOT occurred 1: SDFIFO data ready interrupt has occurred Reset Source: sdfm_rst_mod_g_rst_n
19	SDFFOVF4	R	0h	FIFO Overflow Flag for Ch4 Reset Source: sdfm_rst_mod_g_rst_n
18	SDFFOVF3	R	0h	FIFO Overflow Flag for Ch3 Reset Source: sdfm_rst_mod_g_rst_n
17	SDFFOVF2	R	0h	FIFO Overflow Flag for Ch2 Reset Source: sdfm_rst_mod_g_rst_n
16	SDFFOVF1	R	0h	FIFO Overflow Flag for Ch1 0 - FIFO has not overflowed 1 - FIFO overflowed. # words received in FIFO ' FIFO depth [16], NEW word is lost Reset Source: sdfm_rst_mod_g_rst_n
15	AF4	R	0h	Acknowledge flag for Filter 4 0: No new data available for Filter [in non-FIFO mode] 1: New data available for Filter [in non-FIFO mode] Reset Source: sdfm_rst_mod_g_rst_n
14	AF3	R	0h	Acknowledge flag for Filter 3 0: No new data available for Filter [in non-FIFO mode] 1: New data available for Filter [in non-FIFO mode] Reset Source: sdfm_rst_mod_g_rst_n

Table 3-2956. SDIFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	AF2	R	0h	Acknowledge flag for Filter 2 0: No new data available for Filter [in non-FIFO mode] 1: New data available for Filter [in non-FIFO mode] Reset Source: sdfm_rst_mod_g_rst_n
12	AF1	R	0h	Acknowledge flag for Filter 1 0: No new data available for Filter [in non-FIFO mode] 1: New data available for Filter [in non-FIFO mode] Reset Source: sdfm_rst_mod_g_rst_n
11	MF4	R	0h	Modulator Failure for Filter 4 0: Modulator is operating normally for Filter 1: Modulator failure for Filter Reset Source: sdfm_rst_mod_g_rst_n
10	MF3	R	0h	Modulator Failure for Filter 3 0: Modulator is operating normally for Filter 1: Modulator failure for Filter Reset Source: sdfm_rst_mod_g_rst_n
9	MF2	R	0h	Modulator Failure for Filter 2 0: Modulator is operating normally for Filter 1: Modulator failure for Filter Reset Source: sdfm_rst_mod_g_rst_n
8	MF1	R	0h	Modulator Failure for Filter 1 0: Modulator is operating normally for Filter 1: Modulator failure for Filter Reset Source: sdfm_rst_mod_g_rst_n
7	FLT4_FLG_CEVT2	R	0h	CEVT2 Interrupt flag for filter4 0: CEVT2 event has not occured 1: CEVT2 event has occurred Reset Source: sdfm_rst_mod_g_rst_n
6	FLT4_FLG_CEVT1	R	0h	CEVT1 Interrupt flag for filter4 0: CEVT1 event has not occured 1: CEVT1 event has occurred Reset Source: sdfm_rst_mod_g_rst_n
5	FLT3_FLG_CEVT2	R	0h	CEVT2 Interrupt flag for filter3 0: CEVT2 event has not occured 1: CEVT2 event has occurred Reset Source: sdfm_rst_mod_g_rst_n
4	FLT3_FLG_CEVT1	R	0h	CEVT1 Interrupt flag for filter3 0: CEVT1 event has not occured 1: CEVT1 event has occurred Reset Source: sdfm_rst_mod_g_rst_n
3	FLT2_FLG_CEVT2	R	0h	CEVT2 Interrupt flag for filter2 0: CEVT2 event has not occured 1: CEVT2 event has occurred Reset Source: sdfm_rst_mod_g_rst_n
2	FLT2_FLG_CEVT1	R	0h	CEVT1 Interrupt flag for filter2 0: CEVT1 event has not occured 1: CEVT1 event has occurred Reset Source: sdfm_rst_mod_g_rst_n
1	FLT1_FLG_CEVT2	R	0h	CEVT2 Interrupt flag for filter1 0: CEVT2 event has not occured 1: CEVT2 event has occurred Reset Source: sdfm_rst_mod_g_rst_n
0	FLT1_FLG_CEVT1	R	0h	CEVT1 Interrupt flag for filter1 0: CEVT1 event has not occured 1: CEVT1 event has occurred Reset Source: sdfm_rst_mod_g_rst_n

3.22.2 MEM_SDIFLGCLR Registers

3.22.2.1 MEM_SDIFLGCLR Register (Offset = 4h) [reset = 0h]

Short Description: SD Module Interrupt Flag

Long Description: SD Module Interrupt Flag Clear Bits: Writing a "1" will clear the respective flag bit in the SDIFLG register. Writes of "0" are ignored. Note: If user writes a "1" to clear a bit on the same cycle that the hardware is trying to set the bit to "1", then hardware has priority and the bit will not be cleared.

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Table 3-2957. Instance Table

Instance Name	Physical Address
SDFM0	5026 8004h
SDFM1	5026 9004h

Figure 3-1407. SDIFLGCLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MIF	RESERVED_1							SDFFINT4	SDFFINT3	SDFFINT2	SDFFINT1	SDFFOVF4	SDFFOVF3	SDFFOVF2	SDFFOVF1
R/W1TS	R							R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h							0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AF4	AF3	AF2	AF1	MF4	MF3	MF2	MF1	FLT4_FLG_CEVT2	FLT4_FLG_CEVT1	FLT3_FLG_CEVT2	FLT3_FLG_CEVT1	FLT2_FLG_CEVT2	FLT2_FLG_CEVT1	FLT1_FLG_CEVT2	FLT1_FLG_CEVT1
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 3-2958. SDIFLGCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MIF	R/W1TS	0h	Flag-clear bit for SDFM Master Interrupt flag. Writing a 1 to clear MIF flag in SDIFLG register Writes of "0" are ignored. Note: If the MIF flag is cleared and other Interrupts are still pending, MIF will again be set to 1 on the following SysClk cycle, and the INT output will be reasserted [pulsed low] Reset Source: sdfm_rst_mod_g_rst_n
30:24	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
23	SDFFINT4	R/W1TS	0h	SDFIFO data ready Interrupt flag-clear bit for Ch4 Reset Source: sdfm_rst_mod_g_rst_n
22	SDFFINT3	R/W1TS	0h	SDFIFO data ready Interrupt flag-clear bit for Ch3 Reset Source: sdfm_rst_mod_g_rst_n
21	SDFFINT2	R/W1TS	0h	SDFIFO data ready Interrupt flag-clear bit for Ch2 Reset Source: sdfm_rst_mod_g_rst_n
20	SDFFINT1	R/W1TS	0h	SDFIFO data ready Interrupt flag-clear bit for Ch1 Reset Source: sdfm_rst_mod_g_rst_n
19	SDFFOVF4	R/W1TS	0h	SDFIFO overflow clear Ch4 Reset Source: sdfm_rst_mod_g_rst_n
18	SDFFOVF3	R/W1TS	0h	SDFIFO overflow clear Ch3 Reset Source: sdfm_rst_mod_g_rst_n
17	SDFFOVF2	R/W1TS	0h	SDFIFO overflow clear Ch2 Reset Source: sdfm_rst_mod_g_rst_n
16	SDFFOVF1	R/W1TS	0h	SDFIFO overflow clear Ch1 Reset Source: sdfm_rst_mod_g_rst_n
15	AF4	R/W1TS	0h	Flag-clear bit for Acknowledge flag for Filter 4 Reset Source: sdfm_rst_mod_g_rst_n
14	AF3	R/W1TS	0h	Flag Clear bit for AF3 Reset Source: sdfm_rst_mod_g_rst_n

Table 3-2958. SDIFLGCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	AF2	R/W1TS	0h	Flag Clear bit for AF2 Reset Source: sdfm_rst_mod_g_rst_n
12	AF1	R/W1TS	0h	Flag Clear bit for AF1 Reset Source: sdfm_rst_mod_g_rst_n
11	MF4	R/W1TS	0h	Flag Clear bit for MF4 Reset Source: sdfm_rst_mod_g_rst_n
10	MF3	R/W1TS	0h	Flag Clear bit for MF3 Reset Source: sdfm_rst_mod_g_rst_n
9	MF2	R/W1TS	0h	Flag Clear bit for MF2 Reset Source: sdfm_rst_mod_g_rst_n
8	MF1	R/W1TS	0h	Flag Clear bit for MF1 Reset Source: sdfm_rst_mod_g_rst_n
7	FLT4_FLG_CEVT2	R/W1TS	0h	Flag Clear bit for FLT4_FLG_CEVT2 Reset Source: sdfm_rst_mod_g_rst_n
6	FLT4_FLG_CEVT1	R/W1TS	0h	Flag Clear bit for FLT4_FLG_CEVT1 Reset Source: sdfm_rst_mod_g_rst_n
5	FLT3_FLG_CEVT2	R/W1TS	0h	Flag Clear bit for FLT3_FLG_CEVT2 Reset Source: sdfm_rst_mod_g_rst_n
4	FLT3_FLG_CEVT1	R/W1TS	0h	Flag Clear bit for FLT3_FLG_CEVT1 Reset Source: sdfm_rst_mod_g_rst_n
3	FLT2_FLG_CEVT2	R/W1TS	0h	Flag Clear bit for FLT2_FLG_CEVT2 Reset Source: sdfm_rst_mod_g_rst_n
2	FLT2_FLG_CEVT1	R/W1TS	0h	Flag Clear bit for FLT2_FLG_CEVT1 Reset Source: sdfm_rst_mod_g_rst_n
1	FLT1_FLG_CEVT2	R/W1TS	0h	Flag Clear bit for FLT1_FLG_CEVT2 Reset Source: sdfm_rst_mod_g_rst_n
0	FLT1_FLG_CEVT1	R/W1TS	0h	Flag Clear bit for FLT1_FLG_CEVT1 Reset Source: sdfm_rst_mod_g_rst_n

3.22.3 MEM_SDCTL Registers

3.22.3.1 MEM_SDCTL Register (Offset = 8h) [reset = 0h]

Short Description: SD Control Register

Long Description: SD Control Register

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Table 3-2959. Instance Table

Instance Name	Physical Address
SDFM0	5026 8008h
SDFM1	5026 9008h

Figure 3-1408. SDCTL Name Register

15	14	13	12	11	10	9	8
RESERVED_3	RESERVED_2	MIE	RESERVED_1				
R	R	R/W	R				
0h	0h	0h	0h				
7	6	5	4	3	2	1	0
RESERVED_1				HZ4	HZ3	HZ2	HZ1
R				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Access Types Legend

Table 3-2960. SDCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_3	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
14	RESERVED_2	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
13	MIE	R/W	0h	Master SDy_ERR interrupt enable 0: SDy_ERR Interrupt and interrupt flags are disabled 1: SDy_ERR Interrupt and interrupt flags are enabled Reset Source: sdfm_rst_mod_g_rst_n
12:4	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
3	HZ4	R/W1TS	0h	Flag Clear bit for HZ4 Reset Source: sdfm_rst_mod_g_rst_n
2	HZ3	R/W1TS	0h	Flag Clear bit for HZ3 Reset Source: sdfm_rst_mod_g_rst_n
1	HZ2	R/W1TS	0h	Flag Clear bit for HZ2 Reset Source: sdfm_rst_mod_g_rst_n
0	HZ1	R/W1TS	0h	Flag Clear bit for HZ1 Reset Source: sdfm_rst_mod_g_rst_n

3.22.4 MEM_SDMFILEN Registers

3.22.4.1 MEM_SDMFILEN Register (Offset = Ch) [reset = 0h]

Short Description: SD Master Filter Enable

Long Description: SD Master Filter Enable

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Table 3-2961. Instance Table

Instance Name	Physical Address
SDFM0	5026 800Ch
SDFM1	5026 900Ch

Figure 3-1409. SDMFILEN Name Register

15	14	13	12	11	10	9	8
RESERVED_7			RESERVED_6	MFE	RESERVED_5	RESERVED_4	RESERVED_3
R			R	R/W	R	R	R
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED_3	RESERVED_2			RESERVED_1			
R	R			R			
0h	0h			0h			

Access Types Legend

Table 3-2962. SDMFILEN Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_7	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
12	RESERVED_6	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
11	MFE	R/W	0h	Master Filter Enable 0: All the four data filter units of SDFM module are disabled. All FIFOs are cleared 1: Data filter units can be enabled if bit FEN is '1'. Reset Source: sdfm_rst_mod_g_rst_n
10	RESERVED_5	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
9	RESERVED_4	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
8:7	RESERVED_3	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
6:4	RESERVED_2	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
3:0	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n

3.22.5 MEM_SDSTATUS Registers

3.22.5.1 MEM_SDSTATUS Register (Offset = Eh) [reset = 0h]

Short Description: SD Status Register

Long Description: SD Status Register

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Table 3-2963. Instance Table

Instance Name	Physical Address
SDFM0	5026 800Eh
SDFM1	5026 900Eh

Figure 3-1410. SDSTATUS Name Register

15	14	13	12	11	10	9	8
RESERVED_9	RESERVED_8	RESERVED_7	RESERVED_6	RESERVED_5	RESERVED_4	RESERVED_3	RESERVED_2
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED_1				HZ4	HZ3	HZ2	HZ1
R				R	R	R	R
0h				0h	0h	0h	0h

Access Types Legend

Table 3-2964. SDSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_9	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
14	RESERVED_8	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
13	RESERVED_7	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
12	RESERVED_6	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
11	RESERVED_5	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
10	RESERVED_4	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
9	RESERVED_3	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
8	RESERVED_2	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
7:4	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
3	HZ4	R	0h	High-level Threshold crossing [Z] flag Ch4 Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator IFHx flag, it does not have the ability to generate an interrupt. 0: Comparator filter output ' SDCMPHZ4.HLTZ 1: Comparator filter output '= SDCMPHZ4.HLTZ Reset Source: sdfm_rst_mod_g_rst_n
2	HZ3	R	0h	High-level Threshold crossing [Z] flag Ch3 Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator IFHx flag, it does not have the ability to generate an interrupt. 0: Comparator filter output ' SDCMPHZ3.HLTZ 1: Comparator filter output '= SDCMPHZ3.HLTZ Reset Source: sdfm_rst_mod_g_rst_n
1	HZ2	R	0h	High-level Threshold crossing [Z] flag Ch2 Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator IFHx flag, it does not have the ability to generate an interrupt. 0: Comparator filter output ' SDCMPHZ2.HLTZ 1: Comparator filter output '= SDCMPHZ2.HLTZ Reset Source: sdfm_rst_mod_g_rst_n

Table 3-2964. SDSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HZ1	R	0h	High-level Threshold crossing [Z] flag Ch1 Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator IFHx flag, it does not have the ability to generate an interrupt. 0: Comparator filter output ' SDCMPHZ1.HLTZ 1: Comparator filter output '= SDCMPHZ1.HLTZ Reset Source: sdfm_rst_mod_g_rst_n

3.22.6 MEM_SDCTLPARM1 Registers

3.22.6.1 MEM_SDCTLPARM1 Register (Offset = 20h) [reset = 0h]

Short Description: Control Parameter Registe

Long Description: Control Parameter Register for Ch1

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Table 3-2965. Instance Table

Instance Name	Physical Address
SDFM0	5026 8020h
SDFM1	5026 9020h

Figure 3-1411. SDCTLPARM1 Name Register

15	14	13	12	11	10	9	8
RESERVED_4							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_3	SDDATASYNC	RESERVED_2	SDCLKSYNC	SDCLKSEL	RESERVED_1	MOD	
R	R/W	R	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	

Access Types Legend

Table 3-2966. SDCTLPARM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED_4	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
7	RESERVED_3	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
6	SDDATASYNC	R/W	0h	0: SD Data is not passed through a synchronizer. 1: SD Data is passed through a synchronizer. Reset Source: sdfm_rst_mod_g_rst_n
5	RESERVED_2	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
4	SDCLKSYNC	R/W	0h	0: SD Clock is not passed through a synchronizer. 1: SD Clock is passed through a synchronizer. Reset Source: sdfm_rst_mod_g_rst_n
3	SDCLKSEL	R/W	0h	SD1 Clock source select. 0: Clock source to SDFM filter is its channel clock. 1: Clock source to SDFM filter is SD1 filter clock. Reset Source: sdfm_rst_mod_g_rst_n
2	RESERVED_1	R/W	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
1:0	MOD	R/W	0h	Modulator clock modes 0: Mode 0: Modulator clock running at 1x data rate 1: Reserved 2: Reserved 3: Reserved Reset Source: sdfm_rst_mod_g_rst_n

3.22.7 MEM_SDDFPARM1 Registers

3.22.7.1 MEM_SDDFPARM1 Register (Offset = 22h) [reset = 0h]

Short Description: Data Filter Parameter Reg

Long Description: Data Filter Parameter Register for Ch1

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Table 3-2967. Instance Table

Instance Name	Physical Address
SDFM0	5026 8022h
SDFM1	5026 9022h

Figure 3-1412. SDDFPARM1 Name Register

15	14	13	12	11	10	9	8
RESERVED_1			SDSYNCEN	SST		AE	FEN
R			R/W	R/W		R/W	R/W
0h			0h	0h		0h	0h
7	6	5	4	3	2	1	0
DOSR							
R/W							
0h							

Access Types Legend

Table 3-2968. SDDFPARM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
12	SDSYNCEN	R/W	0h	PWM synchronization [SDSYNC] of data filter 0: PWM synchronization of data filter is disabled 1: PWM synchronization of data filter is enabled Note: SDSYNCx.SYNCSEL bits define which PWM signal is used to synchronize PWMs Reset Source: sdfm_rst_mod_g_rst_n
11:10	SST	R/W	0h	Data filter structure 00: Data filter runs with a Sincfast structure 01: Data filter runs with a Sinc1 structure 10: Data filter runs with a Sinc2 structure 11: Data filter runs with a Sinc3 structure Reset Source: sdfm_rst_mod_g_rst_n
9	AE	R/W	0h	Data filter Acknowledge Enable 0: Acknowledge flag is disabled for the particular filter 1: Acknowledge flag is enabled for the particular filter Reset Source: sdfm_rst_mod_g_rst_n
8	FEN	R/W	0h	Filter Enable 0: The data filter is disabled and no data is produced 1: The data filter is enabled and data are produced in the data filter Note: When filter is disabled, DOSR counter held in reset, filter data erased. Also resets FIFO pointers and clears the FIFO Reset Source: sdfm_rst_mod_g_rst_n
7:0	DOSR	R/W	0h	Data filter Oversampling ratio The actual oversampling ratio of data filter is DOSR + 1 These bits set the oversampling ratio of the data filter. 0x0FF represents an oversampling ratio of 256. Reset Source: sdfm_rst_mod_g_rst_n

3.22.8 MEM_SDDPARM1 Registers

3.22.8.1 MEM_SDDPARM1 Register (Offset = 24h) [reset = 0h]

Short Description: Data Parameter Register f

Long Description: Data Parameter Register for Ch1

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Table 3-2969. Instance Table

Instance Name	Physical Address
SDFM0	5026 8024h
SDFM1	5026 9024h

Figure 3-1413. SDDPARM1 Name Register

15	14	13	12	11	10	9	8
SH					DR	RESERVED_1	
R/W					R/W	R	
0h					0h	0h	
7	6	5	4	3	2	1	0
RESERVED_1							
R							
0h							

Access Types Legend

Table 3-2970. SDDPARM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	SH	R/W	0h	Shift Control These bits indicate by how many bits the 16-bit window is shifted up when 16-bit data representation is chosen. Reset Source: sdfm_rst_mod_g_rst_n
10	DR	R/W	0h	Data filter Data representation 0: Data stored in 16b 2's complement 1: Data stored in 32b 2's complement Reset Source: sdfm_rst_mod_g_rst_n
9:0	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n

3.22.9 MEM_SDFLT1CMPH1 Registers

3.22.9.1 MEM_SDFLT1CMPH1 Register (Offset = 26h) [reset = 7fffh]

Short Description: High-level Threshold Regi

Long Description: High-level Threshold Register for Ch1

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Table 3-2971. Instance Table

Instance Name	Physical Address
SDFM0	5026 8026h
SDFM1	5026 9026h

Figure 3-1414. SDFLT1CMPH1 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	HLT						
R	R/W						
0h	7fffh						
7	6	5	4	3	2	1	0
HLT							
R/W							
7fffh							

Access Types Legend

Table 3-2972. SDFLT1CMPH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
14:0	HLT	R/W	7FFFh	Unsigned high-level threshold for the comparator filter output. Reset Source: sdfm_rst_mod_g_rst_n

3.22.10 MEM_SDFLT1CMPL1 Registers

3.22.10.1 MEM_SDFLT1CMPL1 Register (Offset = 28h) [reset = 0h]

Short Description: Low-level Threshold Regis

Long Description: Low-level Threshold Register for Ch1

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Table 3-2973. Instance Table

Instance Name	Physical Address
SDFM0	5026 8028h
SDFM1	5026 9028h

Figure 3-1415. SDFLT1CMPL1 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	LLT						
R	R/W						
0h	0h						
7	6	5	4	3	2	1	0
LLT							
R/W							
0h							

Access Types Legend

Table 3-2974. SDFLT1CMPL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
14:0	LLT	R/W	0h	Unsigned low-level threshold for the comparator filter output. Reset Source: sdfm_rst_mod_g_rst_n

3.22.11 MEM_SDCPARM1 Registers

3.22.11.1 MEM_SDCPARM1 Register (Offset = 2Ah) [reset = 0h]

Short Description: Comparator Filter Paramet

Long Description: Comparator Filter Parameter Register for Ch1

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Table 3-2975. Instance Table

Instance Name	Physical Address
SDFM0	5026 802Ah
SDFM1	5026 902Ah

Figure 3-1416. SDCPARM1 Name Register

15	14	13	12	11	10	9	8
CEVT2SEL		CEN	CEVT1SEL		HZEN	MFIE	CS1_CS0
R/W		R/W	R/W		R/W	R/W	R/W
0h		0h	0h		0h	0h	0h
7	6	5	4	3	2	1	0
CS1_CS0	EN_CEVT2	EN_CEVT1	COSR				
R/W	R/W	R/W	R/W				
0h	0h	0h	0h				

Access Types Legend

Table 3-2976. SDCPARM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	CEVT2SEL	R/W	0h	Comparator Event2 Select 00: COMPL1 01: COMPL1 OR COMPH1 10: COMPL2 11: COMPL2 OR COMPH2 Reset Source: sdfm_rst_mod_g_rst_n
13	CEN	R/W	0h	Comparator Filter enable 0: Disable comparator filter 1: Enable comparator filter Reset Source: sdfm_rst_mod_g_rst_n
12:11	CEVT1SEL	R/W	0h	Comparator Event1 Select 00: COMPH1 01: COMPL1 OR COMPH1 10: COMPH2 11: COMPL2 OR COMPH2 Reset Source: sdfm_rst_mod_g_rst_n
10	HZEN	R/W	0h	High level [Z] Threshold crossing output enable 0: Disable Higher level Threshold [Z] crossing 1: Enable Higher level Threhold [Z] crossing Reset Source: sdfm_rst_mod_g_rst_n
9	MFIE	R/W	0h	Modulator Failure Interrupt Enable 0: Disable modulator failure interrupt and its flag 1: Enable modulator failure interrupt and its flag Reset Source: sdfm_rst_mod_g_rst_n
8:7	CS1_CS0	R/W	0h	Comparator filter structure 00: Comparator filter runs with a sincfast structure 01: Comparator filter runs with a Sinc1 structure 10: Comparator filter runs with a Sinc2 structure 11: Comparator filter runs with a Sinc3 structure Reset Source: sdfm_rst_mod_g_rst_n
6	EN_CEVT2	R/W	0h	CEVT2 interrupt enable 0: Disable CEVT2 interrupt 1: Enable CEVT2 interrupt Reset Source: sdfm_rst_mod_g_rst_n
5	EN_CEVT1	R/W	0h	CEVT1 interrupt enable 0: Disable CEVT1 interrupt 1: Enable CEVT1 interrupt Reset Source: sdfm_rst_mod_g_rst_n
4:0	COSR	R/W	0h	Comparator Oversampling ratio. The actual rate is COSR + 1. These bits set the oversampling ratio of the filter. 0x1F represents an oversampling ratio of 32 Reset Source: sdfm_rst_mod_g_rst_n

3.22.12 MEM_SDDATA1 Registers

3.22.12.1 MEM_SDDATA1 Register (Offset = 2Ch) [reset = 0h]

Short Description: Data Filter Data Register

Long Description: Data Filter Data Register (16 or 32bit) for Ch1

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Table 3-2977. Instance Table

Instance Name	Physical Address
SDFM0	5026 802Ch
SDFM1	5026 902Ch

Figure 3-1417. SDDATA1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA32HI															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA16															
R															
0h															

Access Types Legend

Table 3-2978. SDDATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DATA32HI	R	0h	Hi-order 16b in 32b mode, 16-bit Data in 16b mode Reset Source: sdfm_rst_mod_g_rst_n
15:0	DATA16	R	0h	Lo-order 16b in 32b mode Reset Source: sdfm_rst_mod_g_rst_n

3.22.13 MEM_SDDATFIFO1 Registers

3.22.13.1 MEM_SDDATFIFO1 Register (Offset = 30h) [reset = 0h]

Short Description: Filter Data FIFO Output(3

Long Description: Filter Data FIFO Output(32b) for Ch1

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Table 3-2979. Instance Table

Instance Name	Physical Address
SDFM0	5026 8030h
SDFM1	5026 9030h

Figure 3-1418. SDDATFIFO1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA32HI															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA16															
R															
0h															

Access Types Legend

Table 3-2980. SDDATFIFO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DATA32HI	R	0h	Hi-order 16b in 32b mode, 16-bit Data in 16b mode Reset Source: sdfm_rst_mod_g_rst_n
15:0	DATA16	R	0h	Lo-order 16b in 32b mode Reset Source: sdfm_rst_mod_g_rst_n

3.22.14 MEM_SDCDATA1 Registers

3.22.14.1 MEM_SDCDATA1 Register (Offset = 34h) [reset = 0h]

Short Description: Comparator Filter Data Re

Long Description: Comparator Filter Data Register (16b) for Ch1

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Table 3-2981. Instance Table

Instance Name	Physical Address
SDFM0	5026 8034h
SDFM1	5026 9034h

Figure 3-1419. SDCDATA1 Name Register

15	14	13	12	11	10	9	8
DATA16							
R							
0h							
7	6	5	4	3	2	1	0
DATA16							
R							
0h							

Access Types Legend

Table 3-2982. SDCDATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	DATA16	R	0h	Comparator Data output - 16b only Reset Source: sdfm_rst_mod_g_rst_n

3.22.15 MEM_SDFLT1CMPH2 Registers

3.22.15.1 MEM_SDFLT1CMPH2 Register (Offset = 36h) [reset = 7fffh]

Short Description: Second high level threhol

Long Description: Second high level threhold for CH1

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Table 3-2983. Instance Table

Instance Name	Physical Address
SDFM0	5026 8036h
SDFM1	5026 9036h

Figure 3-1420. SDFLT1CMPH2 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	HLT2						
R	R/W						
0h	7fffh						
7	6	5	4	3	2	1	0
HLT2							
R/W							
7fffh							

Access Types Legend

Table 3-2984. SDFLT1CMPH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
14:0	HLT2	R/W	7FFFh	Second Unsigned high-level threshold for the comparator filter output. Reset Source: sdfm_rst_mod_g_rst_n

3.22.16 MEM_SDFLT1CMPHZ Registers

3.22.16.1 MEM_SDFLT1CMPHZ Register (Offset = 38h) [reset = 0h]

Short Description: High-level (Z) Threshold

Long Description: High-level (Z) Threshold Register for Ch1

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Table 3-2985. Instance Table

Instance Name	Physical Address
SDFM0	5026 8038h
SDFM1	5026 9038h

Figure 3-1421. SDFLT1CMPHZ Name Register

15	14	13	12	11	10	9	8
RESERVED_1	HLTZ						
R	R/W						
0h	0h						
7	6	5	4	3	2	1	0
HLTZ							
R/W							
0h							

Access Types Legend

Table 3-2986. SDFLT1CMPHZ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
14:0	HLTZ	R/W	0h	Unsigned High-level threshold [Z] for the comparator filter output Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator SDCMPHx, it does not have the ability to generate an interrupt. Reset Source: sdfm_rst_mod_g_rst_n

3.22.17 MEM_SDFIFOCTL1 Registers

3.22.17.1 MEM_SDFIFOCTL1 Register (Offset = 3Ah) [reset = 0h]

Short Description: FIFO Control Register for

Long Description: FIFO Control Register for Ch1

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Table 3-2987. Instance Table

Instance Name	Physical Address
SDFM0	5026 803Ah
SDFM1	5026 903Ah

Figure 3-1422. SDFIFOCTL1 Name Register

15	14	13	12	11	10	9	8
OVFIEN	DRINTSEL	FFEN	FFIEN	RESERVED_2	SDFFST		
R/W	R/W	R/W	R/W	R	R		
0h	0h	0h	0h	0h	0h		
7	6	5	4	3	2	1	0
SDFFST		RESERVED_1	SDFFIL				
R		R	R/W				
0h		0h	0h				

Access Types Legend

Table 3-2988. SDFIFOCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OVFIEN	R/W	0h	SDFIFO Overflow interrupt enable 0: SDFIFO Overflow condition will not generate an interrupt 1: SDFIFO overflow condition generates an interrupt on SDy_ERR Reset Source: sdfm_rst_mod_g_rst_n
14	DRINTSEL	R/W	0h	Data-Ready Interrupt [DRINT] source select 0 = AF1 [Select non-FIFO data-ready interrupt] 1 = SDFFINT1 [Select FIFO data-ready interrupt] Reset Source: sdfm_rst_mod_g_rst_n
13	FFEN	R/W	0h	SDFIFO Enable 0: Disable FIFO operation 1: Enable FIFO operation Note: When FIFO is disabled, FIFO contents are cleared Reset Source: sdfm_rst_mod_g_rst_n
12	FFIEN	R/W	0h	SDFIFO data ready Interrupt Enable Reset Source: sdfm_rst_mod_g_rst_n
11	RESERVED_2	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
10:6	SDFFST	R	0h	SDFIFO Status 00000 FIFO empty 00001 FIFO has 1 word . . . . 10000 FIFO has 16 words Reset Source: sdfm_rst_mod_g_rst_n
5	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
4:0	SDFFIL	R/W	0h	SDFIFO interrupt level bits The FIFO will generate an interrupt when the FIFO status [SDFFST] '= FIFO level [SDFFIL] Reset Source: sdfm_rst_mod_g_rst_n

3.22.18 MEM_SDSYNC1 Registers

3.22.18.1 MEM_SDSYNC1 Register (Offset = 3Ch) [reset = 400h]

Short Description: SD Filter Sync control fo

Long Description: SD Filter Sync control for Ch1

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Table 3-2989. Instance Table

Instance Name	Physical Address
SDFM0	5026 803Ch
SDFM1	5026 903Ch

Figure 3-1423. SDSYNC1 Name Register

15	14	13	12	11	10	9	8
RESERVED_1					WTSCLREN	FFSYNCCLREN	WTSYNCLR
R					R/W	R/W	R/W
0h					1h	0h	0h
7	6	5	4	3	2	1	0
WTSYNFLG	WTSYNCEN	SYNCSEL					
R	R/W	R/W					
0h	0h	0h					

Access Types Legend

Table 3-2990. SDSYNC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
10	WTSCLREN	R/W	1h	WTSYNFLG Clear-on-FIFOINT Enable 0: WTSYNFLG can only be cleared manually [using WTSYNCLR bit] 1: WTSYNFLG is cleared automatically on SDFFINT Reset Source: sdfm_rst_mod_g_rst_n
9	FFSYNCCLREN	R/W	0h	FIFO Clear-on-SDSYNC Enable 0: SDFIFO is not automaticaly cleared upon receiving SDSYNC 1: SDFIFO is automaticaly cleared upon receiving SDSYNC Reset Source: sdfm_rst_mod_g_rst_n
8	WTSYNCLR	R/W	0h	Wait-for-Sync Flag Clear [always reads 0] 0: Write of 0 has no affect 1: Write of 1 clears WTSYNFLG Reset Source: sdfm_rst_mod_g_rst_n
7	WTSYNFLG	R	0h	Wait-for-Sync Flag 0: SDSYNC event has not occurred 1: SDSYNC event occurred. Reset Source: sdfm_rst_mod_g_rst_n
6	WTSYNCEN	R/W	0h	Wait-for-Sync Enable 0: Incoming Data written to SDFIFO on every Data-Ready [DR] Event 1: Incoming Data written to SDFIFO on DR event only after SDSYNC event occurs Reset Source: sdfm_rst_mod_g_rst_n
5:0	SYNCSEL	R/W	0h	Defines source for the SDSYNC Input on this channel Refer SDSYNCx.SYNCSEL table Reset Source: sdfm_rst_mod_g_rst_n

3.22.19 MEM_SDFLT1CMPL2 Registers

3.22.19.1 MEM_SDFLT1CMPL2 Register (Offset = 3Eh) [reset = 0h]

Short Description: Second low level threhold

Long Description: Second low level threhold for CH1

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Table 3-2991. Instance Table

Instance Name	Physical Address
SDFM0	5026 803Eh
SDFM1	5026 903Eh

Figure 3-1424. SDFLT1CMPL2 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	LLT2						
R	R/W						
0h	0h						
7	6	5	4	3	2	1	0
LLT2							
R/W							
0h							

Access Types Legend

Table 3-2992. SDFLT1CMPL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
14:0	LLT2	R/W	0h	Second Unsigned low-level threshold for the comparator filter output. Reset Source: sdfm_rst_mod_g_rst_n

3.22.20 MEM_SDCTLPARM2 Registers

3.22.20.1 MEM_SDCTLPARM2 Register (Offset = 40h) [reset = 0h]

Short Description: Control Parameter Registe

Long Description: Control Parameter Register for Ch2

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Table 3-2993. Instance Table

Instance Name	Physical Address
SDFM0	5026 8040h
SDFM1	5026 9040h

Figure 3-1425. SDCTLPARM2 Name Register

15	14	13	12	11	10	9	8
RESERVED_4							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_3	SDDATASYNC	RESERVED_2	SDCLKSYNC	SDCLKSEL	RESERVED_1	MOD	
R	R/W	R	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	

Access Types Legend

Table 3-2994. SDCTLPARM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED_4	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
7	RESERVED_3	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
6	SDDATASYNC	R/W	0h	0: SD Data is not passed through a synchronizer. 1: SD Data is passed through a synchronizer. Reset Source: sdfm_rst_mod_g_rst_n
5	RESERVED_2	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
4	SDCLKSYNC	R/W	0h	0: SD Clock is not passed through a synchronizer. 1: SD Clock is passed through a synchronizer. Reset Source: sdfm_rst_mod_g_rst_n
3	SDCLKSEL	R/W	0h	SD2 Clock source select. 0: Clock source to SDFM filter is its channel clock. 1: Clock source to SDFM filter is SD1 filter clock. Reset Source: sdfm_rst_mod_g_rst_n
2	RESERVED_1	R/W	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
1:0	MOD	R/W	0h	Modulator clock modes 0: Mode 0: Modulator clock running at 1x data rate 1: Reserved 2: Reserved 3: Reserved Reset Source: sdfm_rst_mod_g_rst_n

3.22.21 MEM_SDDFPARM2 Registers

3.22.21.1 MEM_SDDFPARM2 Register (Offset = 42h) [reset = 0h]

Short Description: Data Filter Parameter Reg

Long Description: Data Filter Parameter Register for Ch2

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Table 3-2995. Instance Table

Instance Name	Physical Address
SDFM0	5026 8042h
SDFM1	5026 9042h

Figure 3-1426. SDDFPARM2 Name Register

15	14	13	12	11	10	9	8
RESERVED_1			SDSYNCEN	SST		AE	FEN
R			R/W	R/W		R/W	R/W
0h			0h	0h		0h	0h
7	6	5	4	3	2	1	0
DOSR							
R/W							
0h							

Access Types Legend

Table 3-2996. SDDFPARM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
12	SDSYNCEN	R/W	0h	PWM synchronization [SDSYNC] of data filter 0: PWM synchronization of data filter is disabled 1: PWM synchronization of data filter is enabled Note: SDSYNCx.SYNCSEL bits define which PWM signal is used to synchronize PWMs Reset Source: sdfm_rst_mod_g_rst_n
11:10	SST	R/W	0h	Data filter structure 00: Data filter runs with a Sincfast structure 01: Data filter runs with a Sinc1 structure 10: Data filter runs with a Sinc2 structure 11: Data filter runs with a Sinc3 structure Reset Source: sdfm_rst_mod_g_rst_n
9	AE	R/W	0h	Data filter Acknowledge Enable 0: Acknowledge flag is disabled for the particular filter 1: Acknowledge flag is enabled for the particular filter Reset Source: sdfm_rst_mod_g_rst_n
8	FEN	R/W	0h	Filter Enable 0: The data filter is disabled and no data is produced 1: The data filter is enabled and data are produced in the data filter Note: When filter is disabled, DOSR counter held in reset, filter data erased. Also resets FIFO pointers and clears the FIFO Reset Source: sdfm_rst_mod_g_rst_n
7:0	DOSR	R/W	0h	Data filter Oversampling ratio The actual oversampling ratio of data filter is DOSR + 1 These bits set the oversampling ratio of the data filter. 0x0FF represents an oversampling ratio of 256. Reset Source: sdfm_rst_mod_g_rst_n

3.22.22 MEM_SDDPARM2 Registers

3.22.22.1 MEM_SDDPARM2 Register (Offset = 44h) [reset = 0h]

Short Description: Data Parameter Register f

Long Description: Data Parameter Register for Ch2

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Table 3-2997. Instance Table

Instance Name	Physical Address
SDFM0	5026 8044h
SDFM1	5026 9044h

Figure 3-1427. SDDPARM2 Name Register

15	14	13	12	11	10	9	8
SH					DR	RESERVED_1	
R/W					R/W	R	
0h					0h	0h	
7	6	5	4	3	2	1	0
RESERVED_1							
R							
0h							

Access Types Legend

Table 3-2998. SDDPARM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	SH	R/W	0h	Shift Control These bits indicate by how many bits the 16-bit window is shifted up when 16-bit data representation is chosen. Reset Source: sdfm_rst_mod_g_rst_n
10	DR	R/W	0h	Data filter Data representation 0: Data stored in 16b 2's complement 1: Data stored in 32b 2's complement Reset Source: sdfm_rst_mod_g_rst_n
9:0	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n

3.22.23 MEM_SDFLT2CMPH1 Registers

3.22.23.1 MEM_SDFLT2CMPH1 Register (Offset = 46h) [reset = 7fffh]

Short Description: High-level Threshold Regi

Long Description: High-level Threshold Register for Ch2

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Table 3-2999. Instance Table

Instance Name	Physical Address
SDFM0	5026 8046h
SDFM1	5026 9046h

Figure 3-1428. SDFLT2CMPH1 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	HLT						
R	R/W						
0h	7fffh						
7	6	5	4	3	2	1	0
HLT							
R/W							
7fffh							

Access Types Legend

Table 3-3000. SDFLT2CMPH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
14:0	HLT	R/W	7FFFh	Unsigned high-level threshold for the comparator filter output. Reset Source: sdfm_rst_mod_g_rst_n

3.22.24 MEM_SDFLT2CMPL1 Registers

3.22.24.1 MEM_SDFLT2CMPL1 Register (Offset = 48h) [reset = 0h]

Short Description: Low-level Threshold Regis

Long Description: Low-level Threshold Register for Ch2

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Table 3-3001. Instance Table

Instance Name	Physical Address
SDFM0	5026 8048h
SDFM1	5026 9048h

Figure 3-1429. SDFLT2CMPL1 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	LLT						
R	R/W						
0h	0h						
7	6	5	4	3	2	1	0
LLT							
R/W							
0h							

Access Types Legend

Table 3-3002. SDFLT2CMPL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
14:0	LLT	R/W	0h	Unsigned low-level threshold for the comparator filter output. Reset Source: sdfm_rst_mod_g_rst_n

3.22.25 MEM_SDCPARM2 Registers

3.22.25.1 MEM_SDCPARM2 Register (Offset = 4Ah) [reset = 0h]

Short Description: Comparator Filter Paramet

Long Description: Comparator Filter Parameter Register for Ch2

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Table 3-3003. Instance Table

Instance Name	Physical Address
SDFM0	5026 804Ah
SDFM1	5026 904Ah

Figure 3-1430. SDCPARM2 Name Register

15	14	13	12	11	10	9	8
CEVT2SEL		CEN	CEVT1SEL		HZEN	MFIE	CS1_CS0
R/W		R/W	R/W		R/W	R/W	R/W
0h		0h	0h		0h	0h	0h
7	6	5	4	3	2	1	0
CS1_CS0	EN_CEVT2	EN_CEVT1	COSR				
R/W	R/W	R/W	R/W				
0h	0h	0h	0h				

Access Types Legend

Table 3-3004. SDCPARM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	CEVT2SEL	R/W	0h	Comparator Event2 Select 00: COMPL1 01: COMPL1 OR COMPH1 10: COMPL2 11: COMPL2 OR COMPH2 Reset Source: sdfm_rst_mod_g_rst_n
13	CEN	R/W	0h	Comparator Filter enable 0: Disable comparator filter 1: Enable comparator filter Reset Source: sdfm_rst_mod_g_rst_n
12:11	CEVT1SEL	R/W	0h	Comparator Event1 Select 00: COMPH1 01: COMPL1 OR COMPH1 10: COMPH2 11: COMPL2 OR COMPH2 Reset Source: sdfm_rst_mod_g_rst_n
10	HZEN	R/W	0h	High level [Z] Threshold crossing output enable 0: Disable Higher level Threshold [Z] crossing 1: Enable Higher level Threhold [Z] crossing Reset Source: sdfm_rst_mod_g_rst_n
9	MFIE	R/W	0h	Modulator Failure Interrupt Enable 0: Disable modulator failure interrupt and its flag 1: Enable modulator failure interrupt and its flag Reset Source: sdfm_rst_mod_g_rst_n
8:7	CS1_CS0	R/W	0h	Comparator filter structure 00: Comparator filter runs with a sincfast structure 01: Comparator filter runs with a Sinc1 structure 10: Comparator filter runs with a Sinc2 structure 11: Comparator filter runs with a Sinc3 structure Reset Source: sdfm_rst_mod_g_rst_n
6	EN_CEVT2	R/W	0h	CEVT2 interrupt enable 0: Disable CEVT2 interrupt 1: Enable CEVT2 interrupt Reset Source: sdfm_rst_mod_g_rst_n
5	EN_CEVT1	R/W	0h	CEVT1 interrupt enable 0: Disable CEVT1 interrupt 1: Enable CEVT1 interrupt Reset Source: sdfm_rst_mod_g_rst_n
4:0	COSR	R/W	0h	Comparator Oversampling ratio. The actual rate is COSR + 1. These bits set the oversampling ratio of the filter. 0x1F represents an oversampling ratio of 32 Reset Source: sdfm_rst_mod_g_rst_n

3.22.26 MEM_SDDATA2 Registers

3.22.26.1 MEM_SDDATA2 Register (Offset = 4Ch) [reset = 0h]

Short Description: Data Filter Data Register

Long Description: Data Filter Data Register (16 or 32bit) for Ch2

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Table 3-3005. Instance Table

Instance Name	Physical Address
SDFM0	5026 804Ch
SDFM1	5026 904Ch

Figure 3-1431. SDDATA2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA32HI															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA16															
R															
0h															

Access Types Legend

Table 3-3006. SDDATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DATA32HI	R	0h	Hi-order 16b in 32b mode, 16-bit Data in 16b mode Reset Source: sdfm_rst_mod_g_rst_n
15:0	DATA16	R	0h	Lo-order 16b in 32b mode Reset Source: sdfm_rst_mod_g_rst_n

3.22.27 MEM_SDDATFIFO2 Registers

3.22.27.1 MEM_SDDATFIFO2 Register (Offset = 50h) [reset = 0h]

Short Description: Filter Data FIFO Output(3

Long Description: Filter Data FIFO Output(32b) for Ch2

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Table 3-3007. Instance Table

Instance Name	Physical Address
SDFM0	5026 8050h
SDFM1	5026 9050h

Figure 3-1432. SDDATFIFO2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA32HI															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA16															
R															
0h															

Access Types Legend

Table 3-3008. SDDATFIFO2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DATA32HI	R	0h	Hi-order 16b in 32b mode, 16-bit Data in 16b mode Reset Source: sdfm_rst_mod_g_rst_n
15:0	DATA16	R	0h	Lo-order 16b in 32b mode Reset Source: sdfm_rst_mod_g_rst_n

3.22.28 MEM_SDCDATA2 Registers

3.22.28.1 MEM_SDCDATA2 Register (Offset = 54h) [reset = 0h]

Short Description: Comparator Filter Data Re

Long Description: Comparator Filter Data Register (16b) for Ch2

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Table 3-3009. Instance Table

Instance Name	Physical Address
SDFM0	5026 8054h
SDFM1	5026 9054h

Figure 3-1433. SDCDATA2 Name Register

15	14	13	12	11	10	9	8
DATA16							
R							
0h							
7	6	5	4	3	2	1	0
DATA16							
R							
0h							

Access Types Legend

Table 3-3010. SDCDATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	DATA16	R	0h	Comparator Data output - 16b only Reset Source: sdfm_rst_mod_g_rst_n

3.22.29 MEM_SDFLT2CMPH2 Registers

3.22.29.1 MEM_SDFLT2CMPH2 Register (Offset = 56h) [reset = 7fffh]

Short Description: Second high level threhol

Long Description: Second high level threhold for CH2

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Table 3-3011. Instance Table

Instance Name	Physical Address
SDFM0	5026 8056h
SDFM1	5026 9056h

Figure 3-1434. SDFLT2CMPH2 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	HLT2						
R	R/W						
0h	7fffh						
7	6	5	4	3	2	1	0
HLT2							
R/W							
7fffh							

Access Types Legend

Table 3-3012. SDFLT2CMPH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
14:0	HLT2	R/W	7FFFh	Second Unsigned high-level threshold for the comparator filter output. Reset Source: sdfm_rst_mod_g_rst_n

3.22.30 MEM_SDFLT2CMPHZ Registers

3.22.30.1 MEM_SDFLT2CMPHZ Register (Offset = 58h) [reset = 0h]

Short Description: High-level (Z) Threshold

Long Description: High-level (Z) Threshold Register for Ch2

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Table 3-3013. Instance Table

Instance Name	Physical Address
SDFM0	5026 8058h
SDFM1	5026 9058h

Figure 3-1435. SDFLT2CMPHZ Name Register

15	14	13	12	11	10	9	8
RESERVED_1	HLTZ						
R	R/W						
0h	0h						
7	6	5	4	3	2	1	0
HLTZ							
R/W							
0h							

Access Types Legend

Table 3-3014. SDFLT2CMPHZ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
14:0	HLTZ	R/W	0h	Unsigned High-level threshold [Z] for the comparator filter output Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator SDCMPHx, it does not have the ability to generate an interrupt. Reset Source: sdfm_rst_mod_g_rst_n

3.22.31 MEM_SDFIFOCTL2 Registers

3.22.31.1 MEM_SDFIFOCTL2 Register (Offset = 5Ah) [reset = 0h]

Short Description: FIFO Control Register for

Long Description: FIFO Control Register for Ch2

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Table 3-3015. Instance Table

Instance Name	Physical Address
SDFM0	5026 805Ah
SDFM1	5026 905Ah

Figure 3-1436. SDFIFOCTL2 Name Register

15	14	13	12	11	10	9	8
OVFIEN	DRINTSEL	FFEN	FFIEN	RESERVED_2	SDFFST		
R/W	R/W	R/W	R/W	R	R		
0h	0h	0h	0h	0h	0h		
7	6	5	4	3	2	1	0
SDFFST		RESERVED_1	SDFFIL				
R		R	R/W				
0h		0h	0h				

Access Types Legend

Table 3-3016. SDFIFOCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OVFIEN	R/W	0h	SDFIFO Overflow interrupt enable 0: SDFIFO Overflow condition will not generate an interrupt 1: SDFIFO overflow condition generates an interrupt on SDy_ERR Reset Source: sdfm_rst_mod_g_rst_n
14	DRINTSEL	R/W	0h	Data-Ready Interrupt [DRINT] source select 0 = AF1 [Select non-FIFO data-ready interrupt] 1 = SDFFINT1 [Select FIFO data-ready interrupt] Reset Source: sdfm_rst_mod_g_rst_n
13	FFEN	R/W	0h	SDFIFO Enable 0: Disable FIFO operation 1: Enable FIFO operation Note: When FIFO is disabled, FIFO contents are cleared Reset Source: sdfm_rst_mod_g_rst_n
12	FFIEN	R/W	0h	SDFIFO data ready Interrupt Enable Reset Source: sdfm_rst_mod_g_rst_n
11	RESERVED_2	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
10:6	SDFFST	R	0h	SDFIFO Status 00000 FIFO empty 00001 FIFO has 1 word . . . . 10000 FIFO has 16 words Reset Source: sdfm_rst_mod_g_rst_n
5	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
4:0	SDFFIL	R/W	0h	SDFIFO interrupt level bits The FIFO will generate an interrupt when the FIFO status [SDFFST] '= FIFO level [SDFFIL] Reset Source: sdfm_rst_mod_g_rst_n

3.22.32 MEM_SDSYNC2 Registers

3.22.32.1 MEM_SDSYNC2 Register (Offset = 5Ch) [reset = 400h]

Short Description: SD Filter Sync control fo

Long Description: SD Filter Sync control for Ch2

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Table 3-3017. Instance Table

Instance Name	Physical Address
SDFM0	5026 805Ch
SDFM1	5026 905Ch

Figure 3-1437. SDSYNC2 Name Register

15	14	13	12	11	10	9	8
RESERVED_1					WTSCLREN	FFSYNCCLREN	WTSYNCLR
R					R/W	R/W	R/W
0h					1h	0h	0h
7	6	5	4	3	2	1	0
WTSYNFLG	WTSYNCEN	SYNCSEL					
R	R/W	R/W					
0h	0h	0h					

Access Types Legend

Table 3-3018. SDSYNC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
10	WTSCLREN	R/W	1h	WTSYNFLG Clear-on-FIFOINT Enable 0: WTSYNFLG can only be cleared manually [using WTSYNCLR bit] 1: WTSYNFLG is cleared automatically on SDFFINT Reset Source: sdfm_rst_mod_g_rst_n
9	FFSYNCCLREN	R/W	0h	FIFO Clear-on-SDSYNC Enable 0: SDFIFO is not automaticaly cleared upon receiving SDSYNC 1: SDFIFO is automaticaly cleared upon receiving SDSYNC Reset Source: sdfm_rst_mod_g_rst_n
8	WTSYNCLR	R/W	0h	Wait-for-Sync Flag Clear [always reads 0] 0: Write of 0 has no affect 1: Write of 1 clears WTSYNFLG Reset Source: sdfm_rst_mod_g_rst_n
7	WTSYNFLG	R	0h	Wait-for-Sync Flag 0: SDSYNC event has not occurred 1: SDSYNC event occurred. Reset Source: sdfm_rst_mod_g_rst_n
6	WTSYNCEN	R/W	0h	Wait-for-Sync Enable 0: Incoming Data written to SDFIFO on every Data-Ready [DR] Event 1: Incoming Data written to SDFIFO on DR event only after SDSYNC event occurs Reset Source: sdfm_rst_mod_g_rst_n
5:0	SYNCSEL	R/W	0h	Defines source for the SDSYNC Input on this channel Refer SDSYNCx.SYNCSEL table Reset Source: sdfm_rst_mod_g_rst_n

3.22.33 MEM_SDFLT2CMPL2 Registers

3.22.33.1 MEM_SDFLT2CMPL2 Register (Offset = 5Eh) [reset = 0h]

Short Description: Second low level threhold

Long Description: Second low level threhold for CH2

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Table 3-3019. Instance Table

Instance Name	Physical Address
SDFM0	5026 805Eh
SDFM1	5026 905Eh

Figure 3-1438. SDFLT2CMPL2 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	LLT2						
R	R/W						
0h	0h						
7	6	5	4	3	2	1	0
LLT2							
R/W							
0h							

Access Types Legend

Table 3-3020. SDFLT2CMPL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
14:0	LLT2	R/W	0h	Second Unsigned low-level threshold for the comparator filter output. Reset Source: sdfm_rst_mod_g_rst_n

3.22.34 MEM_SDCTLPARM3 Registers

3.22.34.1 MEM_SDCTLPARM3 Register (Offset = 60h) [reset = 0h]

Short Description: Control Parameter Registe

Long Description: Control Parameter Register for Ch3

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Table 3-3021. Instance Table

Instance Name	Physical Address
SDFM0	5026 8060h
SDFM1	5026 9060h

Figure 3-1439. SDCTLPARM3 Name Register

15	14	13	12	11	10	9	8
RESERVED_4							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_3	SDDATASYNC	RESERVED_2	SDCLKSYNC	SDCLKSEL	RESERVED_1	MOD	
R	R/W	R	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	

Access Types Legend

Table 3-3022. SDCTLPARM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED_4	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
7	RESERVED_3	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
6	SDDATASYNC	R/W	0h	0: SD Data is not passed through a synchronizer. 1: SD Data is passed through a synchronizer. Reset Source: sdfm_rst_mod_g_rst_n
5	RESERVED_2	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
4	SDCLKSYNC	R/W	0h	0: SD Clock is not passed through a synchronizer. 1: SD Clock is passed through a synchronizer. Reset Source: sdfm_rst_mod_g_rst_n
3	SDCLKSEL	R/W	0h	SD3 Clock source select. 0: Clock source to SDFM filter is its channel clock. 1: Clock source to SDFM filter is SD1 filter clock. Reset Source: sdfm_rst_mod_g_rst_n
2	RESERVED_1	R/W	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
1:0	MOD	R/W	0h	Modulator clock modes 0: Mode 0: Modulator clock running at 1x data rate 1: Reserved 2: Reserved 3: Reserved Reset Source: sdfm_rst_mod_g_rst_n

3.22.35 MEM_SDDFPARM3 Registers

3.22.35.1 MEM_SDDFPARM3 Register (Offset = 62h) [reset = 0h]

Short Description: Data Filter Parameter Reg

Long Description: Data Filter Parameter Register for Ch3

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Table 3-3023. Instance Table

Instance Name	Physical Address
SDFM0	5026 8062h
SDFM1	5026 9062h

Figure 3-1440. SDDFPARM3 Name Register

15	14	13	12	11	10	9	8
RESERVED_1			SDSYNCEN	SST		AE	FEN
R			R/W	R/W		R/W	R/W
0h			0h	0h		0h	0h
7	6	5	4	3	2	1	0
DOSR							
R/W							
0h							

Access Types Legend

Table 3-3024. SDDFPARM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
12	SDSYNCEN	R/W	0h	PWM synchronization [SDSYNC] of data filter 0: PWM synchronization of data filter is disabled 1: PWM synchronization of data filter is enabled Note: SDSYNCx.SYNCSEL bits define which PWM signal is used to synchronize PWMs Reset Source: sdfm_rst_mod_g_rst_n
11:10	SST	R/W	0h	Data filter structure 00: Data filter runs with a Sincfast structure 01: Data filter runs with a Sinc1 structure 10: Data filter runs with a Sinc2 structure 11: Data filter runs with a Sinc3 structure Reset Source: sdfm_rst_mod_g_rst_n
9	AE	R/W	0h	Data filter Acknowledge Enable 0: Acknowledge flag is disabled for the particular filter 1: Acknowledge flag is enabled for the particular filter Reset Source: sdfm_rst_mod_g_rst_n
8	FEN	R/W	0h	Filter Enable 0: The data filter is disabled and no data is produced 1: The data filter is enabled and data are produced in the data filter Note: When filter is disabled, DOSR counter held in reset, filter data erased. Also resets FIFO pointers and clears the FIFO Reset Source: sdfm_rst_mod_g_rst_n
7:0	DOSR	R/W	0h	Data filter Oversampling ratio The actual oversampling ratio of data filter is DOSR + 1 These bits set the oversampling ratio of the data filter. 0x0FF represents an oversampling ratio of 256. Reset Source: sdfm_rst_mod_g_rst_n

3.22.36 MEM_SDDPARM3 Registers

3.22.36.1 MEM_SDDPARM3 Register (Offset = 64h) [reset = 0h]

Short Description: Data Parameter Register f

Long Description: Data Parameter Register for Ch3

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Table 3-3025. Instance Table

Instance Name	Physical Address
SDFM0	5026 8064h
SDFM1	5026 9064h

Figure 3-1441. SDDPARM3 Name Register

15	14	13	12	11	10	9	8
SH					DR	RESERVED_1	
R/W					R/W	R	
0h					0h	0h	
7	6	5	4	3	2	1	0
RESERVED_1							
R							
0h							

Access Types Legend

Table 3-3026. SDDPARM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	SH	R/W	0h	Shift Control These bits indicate by how many bits the 16-bit window is shifted up when 16-bit data representation is chosen. Reset Source: sdfm_rst_mod_g_rst_n
10	DR	R/W	0h	Data filter Data representation 0: Data stored in 16b 2's complement 1: Data stored in 32b 2's complement Reset Source: sdfm_rst_mod_g_rst_n
9:0	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n

3.22.37 MEM_SDFLT3CMPH1 Registers

3.22.37.1 MEM_SDFLT3CMPH1 Register (Offset = 66h) [reset = 7fffh]

Short Description: High-level Threshold Regi

Long Description: High-level Threshold Register for Ch3

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Table 3-3027. Instance Table

Instance Name	Physical Address
SDFM0	5026 8066h
SDFM1	5026 9066h

Figure 3-1442. SDFLT3CMPH1 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	HLT						
R	R/W						
0h	7fffh						
7	6	5	4	3	2	1	0
HLT							
R/W							
7fffh							

Access Types Legend

Table 3-3028. SDFLT3CMPH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
14:0	HLT	R/W	7FFFh	Unsigned high-level threshold for the comparator filter output. Reset Source: sdfm_rst_mod_g_rst_n

3.22.38 MEM_SDFLT3CMPL1 Registers

3.22.38.1 MEM_SDFLT3CMPL1 Register (Offset = 68h) [reset = 0h]

Short Description: Low-level Threshold Regis

Long Description: Low-level Threshold Register for Ch3

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Table 3-3029. Instance Table

Instance Name	Physical Address
SDFM0	5026 8068h
SDFM1	5026 9068h

Figure 3-1443. SDFLT3CMPL1 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	LLT						
R	R/W						
0h	0h						
7	6	5	4	3	2	1	0
LLT							
R/W							
0h							

Access Types Legend

Table 3-3030. SDFLT3CMPL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
14:0	LLT	R/W	0h	Unsigned low-level threshold for the comparator filter output. Reset Source: sdfm_rst_mod_g_rst_n

3.22.39 MEM_SDCPARM3 Registers

3.22.39.1 MEM_SDCPARM3 Register (Offset = 6Ah) [reset = 0h]

Short Description: Comparator Filter Paramet

Long Description: Comparator Filter Parameter Register for Ch3

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Table 3-3031. Instance Table

Instance Name	Physical Address
SDFM0	5026 806Ah
SDFM1	5026 906Ah

Figure 3-1444. SDCPARM3 Name Register

15	14	13	12	11	10	9	8
CEVT2SEL		CEN	CEVT1SEL		HZEN	MFIE	CS1_CS0
R/W		R/W	R/W		R/W	R/W	R/W
0h		0h	0h		0h	0h	0h
7	6	5	4	3	2	1	0
CS1_CS0	EN_CEVT2	EN_CEVT1	COSR				
R/W	R/W	R/W	R/W				
0h	0h	0h	0h				

Access Types Legend

Table 3-3032. SDCPARM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	CEVT2SEL	R/W	0h	Comparator Event2 Select 00: COMPL1 01: COMPL1 OR COMPH1 10: COMPL2 11: COMPL2 OR COMPH2 Reset Source: sdfm_rst_mod_g_rst_n
13	CEN	R/W	0h	Comparator Filter enable 0: Disable comparator filter 1: Enable comparator filter Reset Source: sdfm_rst_mod_g_rst_n
12:11	CEVT1SEL	R/W	0h	Comparator Event1 Select 00: COMPH1 01: COMPL1 OR COMPH1 10: COMPH2 11: COMPL2 OR COMPH2 Reset Source: sdfm_rst_mod_g_rst_n
10	HZEN	R/W	0h	High level [Z] Threshold crossing output enable 0: Disable Higher level Threshold [Z] crossing 1: Enable Higher level Threhold [Z] crossing Reset Source: sdfm_rst_mod_g_rst_n
9	MFIE	R/W	0h	Modulator Failure Interrupt Enable 0: Disable modulator failure interrupt and its flag 1: Enable modulator failure interrupt and its flag Reset Source: sdfm_rst_mod_g_rst_n
8:7	CS1_CS0	R/W	0h	Comparator filter structure 00: Comparator filter runs with a sincfast structure 01: Comparator filter runs with a Sinc1 structure 10: Comparator filter runs with a Sinc2 structure 11: Comparator filter runs with a Sinc3 structure Reset Source: sdfm_rst_mod_g_rst_n
6	EN_CEVT2	R/W	0h	CEVT2 interrupt enable 0: Disable CEVT2 interrupt 1: Enable CEVT2 interrupt Reset Source: sdfm_rst_mod_g_rst_n
5	EN_CEVT1	R/W	0h	CEVT1 interrupt enable 0: Disable CEVT1 interrupt 1: Enable CEVT1 interrupt Reset Source: sdfm_rst_mod_g_rst_n
4:0	COSR	R/W	0h	Comparator Oversampling ratio. The actual rate is COSR + 1. These bits set the oversampling ratio of the filter. 0x1F represents an oversampling ratio of 32 Reset Source: sdfm_rst_mod_g_rst_n

3.22.40 MEM_SDDATA3 Registers

3.22.40.1 MEM_SDDATA3 Register (Offset = 6Ch) [reset = 0h]

Short Description: Data Filter Data Register

Long Description: Data Filter Data Register (16 or 32bit) for Ch3

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Table 3-3033. Instance Table

Instance Name	Physical Address
SDFM0	5026 806Ch
SDFM1	5026 906Ch

Figure 3-1445. SDDATA3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA32HI															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA16															
R															
0h															

Access Types Legend

Table 3-3034. SDDATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DATA32HI	R	0h	Hi-order 16b in 32b mode, 16-bit Data in 16b mode Reset Source: sdfm_rst_mod_g_rst_n
15:0	DATA16	R	0h	Lo-order 16b in 32b mode Reset Source: sdfm_rst_mod_g_rst_n

3.22.41 MEM_SDDATFIFO3 Registers

3.22.41.1 MEM_SDDATFIFO3 Register (Offset = 70h) [reset = 0h]

Short Description: Filter Data FIFO Output(3

Long Description: Filter Data FIFO Output(32b) for Ch3

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Table 3-3035. Instance Table

Instance Name	Physical Address
SDFM0	5026 8070h
SDFM1	5026 9070h

Figure 3-1446. SDDATFIFO3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA32HI															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA16															
R															
0h															

Access Types Legend

Table 3-3036. SDDATFIFO3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DATA32HI	R	0h	Hi-order 16b in 32b mode, 16-bit Data in 16b mode Reset Source: sdfm_rst_mod_g_rst_n
15:0	DATA16	R	0h	Lo-order 16b in 32b mode Reset Source: sdfm_rst_mod_g_rst_n

3.22.42 MEM_SDCDATA3 Registers

3.22.42.1 MEM_SDCDATA3 Register (Offset = 74h) [reset = 0h]

Short Description: Comparator Filter Data Re

Long Description: Comparator Filter Data Register (16b) for Ch3

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Table 3-3037. Instance Table

Instance Name	Physical Address
SDFM0	5026 8074h
SDFM1	5026 9074h

Figure 3-1447. SDCDATA3 Name Register

15	14	13	12	11	10	9	8
DATA16							
R							
0h							
7	6	5	4	3	2	1	0
DATA16							
R							
0h							

Access Types Legend

Table 3-3038. SDCDATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	DATA16	R	0h	Comparator Data output - 16b only Reset Source: sdfm_rst_mod_g_rst_n

3.22.43 MEM_SDFLT3CMPH2 Registers

3.22.43.1 MEM_SDFLT3CMPH2 Register (Offset = 76h) [reset = 7fffh]

Short Description: Second high level threhol

Long Description: Second high level threhold for CH3

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Table 3-3039. Instance Table

Instance Name	Physical Address
SDFM0	5026 8076h
SDFM1	5026 9076h

Figure 3-1448. SDFLT3CMPH2 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	HLT2						
R	R/W						
0h	7fffh						
7	6	5	4	3	2	1	0
HLT2							
R/W							
7fffh							

Access Types Legend

Table 3-3040. SDFLT3CMPH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
14:0	HLT2	R/W	7FFFh	Second Unsigned high-level threshold for the comparator filter output. Reset Source: sdfm_rst_mod_g_rst_n

3.22.44 MEM_SDFLT3CMPHZ Registers

3.22.44.1 MEM_SDFLT3CMPHZ Register (Offset = 78h) [reset = 0h]

Short Description: High-level (Z) Threshold

Long Description: High-level (Z) Threshold Register for Ch3

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Table 3-3041. Instance Table

Instance Name	Physical Address
SDFM0	5026 8078h
SDFM1	5026 9078h

Figure 3-1449. SDFLT3CMPHZ Name Register

15	14	13	12	11	10	9	8
RESERVED_1	HLTZ						
R	R/W						
0h	0h						
7	6	5	4	3	2	1	0
HLTZ							
R/W							
0h							

Access Types Legend

Table 3-3042. SDFLT3CMPHZ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
14:0	HLTZ	R/W	0h	Unsigned High-level threshold [Z] for the comparator filter output Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator SDCMPHx, it does not have the ability to generate an interrupt. Reset Source: sdfm_rst_mod_g_rst_n

3.22.45 MEM_SDFIFOCTL3 Registers

3.22.45.1 MEM_SDFIFOCTL3 Register (Offset = 7Ah) [reset = 0h]

Short Description: FIFO Control Register for

Long Description: FIFO Control Register for Ch3

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Table 3-3043. Instance Table

Instance Name	Physical Address
SDFM0	5026 807Ah
SDFM1	5026 907Ah

Figure 3-1450. SDFIFOCTL3 Name Register

15	14	13	12	11	10	9	8
OVFIEN	DRINTSEL	FFEN	FFIEN	RESERVED_2	SDFFST		
R/W	R/W	R/W	R/W	R	R		
0h	0h	0h	0h	0h	0h		
7	6	5	4	3	2	1	0
SDFFST		RESERVED_1	SDFFIL				
R		R	R/W				
0h		0h	0h				

Access Types Legend

Table 3-3044. SDFIFOCTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OVFIEN	R/W	0h	SDFIFO Overflow interrupt enable 0: SDFIFO Overflow condition will not generate an interrupt 1: SDFIFO overflow condition generates an interrupt on SDy_ERR Reset Source: sdfm_rst_mod_g_rst_n
14	DRINTSEL	R/W	0h	Data-Ready Interrupt [DRINT] source select 0 = AF1 [Select non-FIFO data-ready interrupt] 1 = SDFFINT1 [Select FIFO data-ready interrupt] Reset Source: sdfm_rst_mod_g_rst_n
13	FFEN	R/W	0h	SDFIFO Enable 0: Disable FIFO operation 1: Enable FIFO operation Note: When FIFO is disabled, FIFO contents are cleared Reset Source: sdfm_rst_mod_g_rst_n
12	FFIEN	R/W	0h	SDFIFO data ready Interrupt Enable Reset Source: sdfm_rst_mod_g_rst_n
11	RESERVED_2	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
10:6	SDFFST	R	0h	SDFIFO Status 00000 FIFO empty 00001 FIFO has 1 word . . . . 10000 FIFO has 16 words Reset Source: sdfm_rst_mod_g_rst_n
5	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
4:0	SDFFIL	R/W	0h	SDFIFO interrupt level bits The FIFO will generate an interrupt when the FIFO status [SDFFST] '= FIFO level [SDFFIL] Reset Source: sdfm_rst_mod_g_rst_n

3.22.46 MEM_SDSYNC3 Registers

3.22.46.1 MEM_SDSYNC3 Register (Offset = 7Ch) [reset = 400h]

Short Description: SD Filter Sync control fo

Long Description: SD Filter Sync control for Ch3

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Table 3-3045. Instance Table

Instance Name	Physical Address
SDFM0	5026 807Ch
SDFM1	5026 907Ch

Figure 3-1451. SDSYNC3 Name Register

15	14	13	12	11	10	9	8
RESERVED_1					WTSCLREN	FFSYNCCLREN	WTSYNCLR
R					R/W	R/W	R/W
0h					1h	0h	0h
7	6	5	4	3	2	1	0
WTSYNFLG	WTSYNCEN	SYNCSEL					
R	R/W	R/W					
0h	0h	0h					

Access Types Legend

Table 3-3046. SDSYNC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
10	WTSCLREN	R/W	1h	WTSYNFLG Clear-on-FIFOINT Enable 0: WTSYNFLG can only be cleared manually [using WTSYNCLR bit] 1: WTSYNFLG is cleared automatically on SDFFINT Reset Source: sdfm_rst_mod_g_rst_n
9	FFSYNCCLREN	R/W	0h	FIFO Clear-on-SDSYNC Enable 0: SDFIFO is not automaticaly cleared upon receiving SDSYNC 1: SDFIFO is automaticaly cleared upon receiving SDSYNC Reset Source: sdfm_rst_mod_g_rst_n
8	WTSYNCLR	R/W	0h	Wait-for-Sync Flag Clear [always reads 0] 0: Write of 0 has no affect 1: Write of 1 clears WTSYNFLG Reset Source: sdfm_rst_mod_g_rst_n
7	WTSYNFLG	R	0h	Wait-for-Sync Flag 0: SDSYNC event has not occurred 1: SDSYNC event occurred. Reset Source: sdfm_rst_mod_g_rst_n
6	WTSYNCEN	R/W	0h	Wait-for-Sync Enable 0: Incoming Data written to SDFIFO on every Data-Ready [DR] Event 1: Incoming Data written to SDFIFO on DR event only after SDSYNC event occurs Reset Source: sdfm_rst_mod_g_rst_n
5:0	SYNCSEL	R/W	0h	Defines source for the SDSYNC Input on this channel Refer SDSYNCx.SYNCSEL table Reset Source: sdfm_rst_mod_g_rst_n

3.22.47 MEM_SDFLT3CMPL2 Registers

3.22.47.1 MEM_SDFLT3CMPL2 Register (Offset = 7Eh) [reset = 0h]

Short Description: Second low level threhold

Long Description: Second low level threhold for CH3

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Table 3-3047. Instance Table

Instance Name	Physical Address
SDFM0	5026 807Eh
SDFM1	5026 907Eh

Figure 3-1452. SDFLT3CMPL2 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	LLT2						
R	R/W						
0h	0h						
7	6	5	4	3	2	1	0
LLT2							
R/W							
0h							

Access Types Legend

Table 3-3048. SDFLT3CMPL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
14:0	LLT2	R/W	0h	Second Unsigned low-level threshold for the comparator filter output. Reset Source: sdfm_rst_mod_g_rst_n

3.22.48 MEM_SDCTLPARM4 Registers

3.22.48.1 MEM_SDCTLPARM4 Register (Offset = 80h) [reset = 0h]

Short Description: Control Parameter Registe

Long Description: Control Parameter Register for Ch4

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Table 3-3049. Instance Table

Instance Name	Physical Address
SDFM0	5026 8080h
SDFM1	5026 9080h

Figure 3-1453. SDCTLPARM4 Name Register

15	14	13	12	11	10	9	8
RESERVED_4							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_3	SDDATASYNC	RESERVED_2	SDCLKSYNC	SDCLKSEL	RESERVED_1	MOD	
R	R/W	R	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	

Access Types Legend

Table 3-3050. SDCTLPARM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED_4	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
7	RESERVED_3	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
6	SDDATASYNC	R/W	0h	0: SD Data is not passed through a synchronizer. 1: SD Data is passed through a synchronizer. Reset Source: sdfm_rst_mod_g_rst_n
5	RESERVED_2	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
4	SDCLKSYNC	R/W	0h	0: SD Clock is not passed through a synchronizer. 1: SD Clock is passed through a synchronizer. Reset Source: sdfm_rst_mod_g_rst_n
3	SDCLKSEL	R/W	0h	SD4 Clock source select. 0: Clock source to SDFM filter is its channel clock. 1: Clock source to SDFM filter is SD1 filter clock. Reset Source: sdfm_rst_mod_g_rst_n
2	RESERVED_1	R/W	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
1:0	MOD	R/W	0h	Modulator clock modes 0: Mode 0: Modulator clock running at 1x data rate 1: Reserved 2: Reserved 3: Reserved Reset Source: sdfm_rst_mod_g_rst_n

3.22.49 MEM_SDDFPARM4 Registers

3.22.49.1 MEM_SDDFPARM4 Register (Offset = 82h) [reset = 0h]

Short Description: Data Filter Parameter Reg

Long Description: Data Filter Parameter Register for Ch4

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Table 3-3051. Instance Table

Instance Name	Physical Address
SDFM0	5026 8082h
SDFM1	5026 9082h

Figure 3-1454. SDDFPARM4 Name Register

15	14	13	12	11	10	9	8
RESERVED_1			SDSYNCEN	SST		AE	FEN
R			R/W	R/W		R/W	R/W
0h			0h	0h		0h	0h
7	6	5	4	3	2	1	0
DOSR							
R/W							
0h							

Access Types Legend

Table 3-3052. SDDFPARM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
12	SDSYNCEN	R/W	0h	PWM synchronization [SDSYNC] of data filter 0: PWM synchronization of data filter is disabled 1: PWM synchronization of data filter is enabled Note: SDSYNCx.SYNCSEL bits define which PWM signal is used to synchronize PWMs Reset Source: sdfm_rst_mod_g_rst_n
11:10	SST	R/W	0h	Data filter structure 00: Data filter runs with a Sincfast structure 01: Data filter runs with a Sinc1 structure 10: Data filter runs with a Sinc2 structure 11: Data filter runs with a Sinc3 structure Reset Source: sdfm_rst_mod_g_rst_n
9	AE	R/W	0h	Data filter Acknowledge Enable 0: Acknowledge flag is disabled for the particular filter 1: Acknowledge flag is enabled for the particular filter Reset Source: sdfm_rst_mod_g_rst_n
8	FEN	R/W	0h	Filter Enable 0: The data filter is disabled and no data is produced 1: The data filter is enabled and data are produced in the data filter Note: When filter is disabled, DOSR counter held in reset, filter data erased. Also resets FIFO pointers and clears the FIFO Reset Source: sdfm_rst_mod_g_rst_n
7:0	DOSR	R/W	0h	Data filter Oversampling ratio The actual oversampling ratio of data filter is DOSR + 1 These bits set the oversampling ratio of the data filter. 0x0FF represents an oversampling ratio of 256. Reset Source: sdfm_rst_mod_g_rst_n

3.22.50 MEM_SDDPARM4 Registers

3.22.50.1 MEM_SDDPARM4 Register (Offset = 84h) [reset = 0h]

Short Description: Data Parameter Register f

Long Description: Data Parameter Register for Ch4

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Table 3-3053. Instance Table

Instance Name	Physical Address
SDFM0	5026 8084h
SDFM1	5026 9084h

Figure 3-1455. SDDPARM4 Name Register

15	14	13	12	11	10	9	8
SH					DR	RESERVED_1	
R/W					R/W	R	
0h					0h	0h	
7	6	5	4	3	2	1	0
RESERVED_1							
R							
0h							

Access Types Legend

Table 3-3054. SDDPARM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	SH	R/W	0h	Shift Control These bits indicate by how many bits the 16-bit window is shifted up when 16-bit data representation is chosen. Reset Source: sdfm_rst_mod_g_rst_n
10	DR	R/W	0h	Data filter Data representation 0: Data stored in 16b 2's complement 1: Data stored in 32b 2's complement Reset Source: sdfm_rst_mod_g_rst_n
9:0	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n

3.22.51 MEM_SDFLT4CMPH1 Registers

3.22.51.1 MEM_SDFLT4CMPH1 Register (Offset = 86h) [reset = 7fffh]

Short Description: High-level Threshold Regi

Long Description: High-level Threshold Register for Ch4

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Table 3-3055. Instance Table

Instance Name	Physical Address
SDFM0	5026 8086h
SDFM1	5026 9086h

Figure 3-1456. SDFLT4CMPH1 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	HLT						
R	R/W						
0h	7fffh						
7	6	5	4	3	2	1	0
HLT							
R/W							
7fffh							

Access Types Legend

Table 3-3056. SDFLT4CMPH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
14:0	HLT	R/W	7FFFh	Unsigned high-level threshold for the comparator filter output. Reset Source: sdfm_rst_mod_g_rst_n

3.22.52 MEM_SDFLT4CMPL1 Registers

3.22.52.1 MEM_SDFLT4CMPL1 Register (Offset = 88h) [reset = 0h]

Short Description: Low-level Threshold Regis

Long Description: Low-level Threshold Register for Ch4

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Table 3-3057. Instance Table

Instance Name	Physical Address
SDFM0	5026 8088h
SDFM1	5026 9088h

Figure 3-1457. SDFLT4CMPL1 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	LLT						
R	R/W						
0h	0h						
7	6	5	4	3	2	1	0
LLT							
R/W							
0h							

Access Types Legend

Table 3-3058. SDFLT4CMPL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
14:0	LLT	R/W	0h	Unsigned low-level threshold for the comparator filter output. Reset Source: sdfm_rst_mod_g_rst_n

3.22.53 MEM_SDCPARM4 Registers

3.22.53.1 MEM_SDCPARM4 Register (Offset = 8Ah) [reset = 0h]

Short Description: Comparator Filter Paramet

Long Description: Comparator Filter Parameter Register for Ch4

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Table 3-3059. Instance Table

Instance Name	Physical Address
SDFM0	5026 808Ah
SDFM1	5026 908Ah

Figure 3-1458. SDCPARM4 Name Register

15	14	13	12	11	10	9	8
CEVT2SEL		CEN	CEVT1SEL		HZEN	MFIE	CS1_CS0
R/W		R/W	R/W		R/W	R/W	R/W
0h		0h	0h		0h	0h	0h
7	6	5	4	3	2	1	0
CS1_CS0	EN_CEVT2	EN_CEVT1	COSR				
R/W	R/W	R/W	R/W				
0h	0h	0h	0h				

Access Types Legend

Table 3-3060. SDCPARM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	CEVT2SEL	R/W	0h	Comparator Event2 Select 00: COMPL1 01: COMPL1 OR COMPH1 10: COMPL2 11: COMPL2 OR COMPH2 Reset Source: sdfm_rst_mod_g_rst_n
13	CEN	R/W	0h	Comparator Filter enable 0: Disable comparator filter 1: Enable comparator filter Reset Source: sdfm_rst_mod_g_rst_n
12:11	CEVT1SEL	R/W	0h	Comparator Event1 Select 00: COMPH1 01: COMPL1 OR COMPH1 10: COMPH2 11: COMPL2 OR COMPH2 Reset Source: sdfm_rst_mod_g_rst_n
10	HZEN	R/W	0h	High level [Z] Threshold crossing output enable 0: Disable Higher level Threshold [Z] crossing 1: Enable Higher level Threhold [Z] crossing Reset Source: sdfm_rst_mod_g_rst_n
9	MFIE	R/W	0h	Modulator Failure Interrupt Enable 0: Disable modulator failure interrupt and its flag 1: Enable modulator failure interrupt and its flag Reset Source: sdfm_rst_mod_g_rst_n
8:7	CS1_CS0	R/W	0h	Comparator filter structure 00: Comparator filter runs with a sincfast structure 01: Comparator filter runs with a Sinc1 structure 10: Comparator filter runs with a Sinc2 structure 11: Comparator filter runs with a Sinc3 structure Reset Source: sdfm_rst_mod_g_rst_n
6	EN_CEVT2	R/W	0h	CEVT2 interrupt enable 0: Disable CEVT2 interrupt 1: Enable CEVT2 interrupt Reset Source: sdfm_rst_mod_g_rst_n
5	EN_CEVT1	R/W	0h	CEVT1 interrupt enable 0: Disable CEVT1 interrupt 1: Enable CEVT1 interrupt Reset Source: sdfm_rst_mod_g_rst_n
4:0	COSR	R/W	0h	Comparator Oversampling ratio. The actual rate is COSR + 1. These bits set the oversampling ratio of the filter. 0x1F represents an oversampling ratio of 32 Reset Source: sdfm_rst_mod_g_rst_n

3.22.54 MEM_SDDATA4 Registers

3.22.54.1 MEM_SDDATA4 Register (Offset = 8Ch) [reset = 0h]

Short Description: Data Filter Data Register

Long Description: Data Filter Data Register (16 or 32bit) for Ch4

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Table 3-3061. Instance Table

Instance Name	Physical Address
SDFM0	5026 808Ch
SDFM1	5026 908Ch

Figure 3-1459. SDDATA4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA32HI															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA16															
R															
0h															

Access Types Legend

Table 3-3062. SDDATA4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DATA32HI	R	0h	Hi-order 16b in 32b mode, 16-bit Data in 16b mode Reset Source: sdfm_rst_mod_g_rst_n
15:0	DATA16	R	0h	Lo-order 16b in 32b mode Reset Source: sdfm_rst_mod_g_rst_n

3.22.55 MEM_SDDATFIFO4 Registers

3.22.55.1 MEM_SDDATFIFO4 Register (Offset = 90h) [reset = 0h]

Short Description: Filter Data FIFO Output(3

Long Description: Filter Data FIFO Output(32b) for Ch4

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Table 3-3063. Instance Table

Instance Name	Physical Address
SDFM0	5026 8090h
SDFM1	5026 9090h

Figure 3-1460. SDDATFIFO4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA32HI															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA16															
R															
0h															

Access Types Legend

Table 3-3064. SDDATFIFO4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DATA32HI	R	0h	Hi-order 16b in 32b mode, 16-bit Data in 16b mode Reset Source: sdfm_rst_mod_g_rst_n
15:0	DATA16	R	0h	Lo-order 16b in 32b mode Reset Source: sdfm_rst_mod_g_rst_n

3.22.56 MEM_SDCDATA4 Registers

3.22.56.1 MEM_SDCDATA4 Register (Offset = 94h) [reset = 0h]

Short Description: Comparator Filter Data Re

Long Description: Comparator Filter Data Register (16b) for Ch4

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Table 3-3065. Instance Table

Instance Name	Physical Address
SDFM0	5026 8094h
SDFM1	5026 9094h

Figure 3-1461. SDCDATA4 Name Register

15	14	13	12	11	10	9	8
DATA16							
R							
0h							
7	6	5	4	3	2	1	0
DATA16							
R							
0h							

Access Types Legend

Table 3-3066. SDCDATA4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	DATA16	R	0h	Comparator Data output - 16b only Reset Source: sdfm_rst_mod_g_rst_n

3.22.57 MEM_SDFLT4CMPH2 Registers

3.22.57.1 MEM_SDFLT4CMPH2 Register (Offset = 96h) [reset = 7fffh]

Short Description: Second high level threhol

Long Description: Second high level threhold for CH4

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Table 3-3067. Instance Table

Instance Name	Physical Address
SDFM0	5026 8096h
SDFM1	5026 9096h

Figure 3-1462. SDFLT4CMPH2 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	HLT2						
R	R/W						
0h	7fffh						
7	6	5	4	3	2	1	0
HLT2							
R/W							
7fffh							

Access Types Legend

Table 3-3068. SDFLT4CMPH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
14:0	HLT2	R/W	7FFFh	Second Unsigned high-level threshold for the comparator filter output. Reset Source: sdfm_rst_mod_g_rst_n

3.22.58 MEM_SDFLT4CMPHZ Registers

3.22.58.1 MEM_SDFLT4CMPHZ Register (Offset = 98h) [reset = 0h]

Short Description: High-level (Z) Threshold

Long Description: High-level (Z) Threshold Register for Ch4

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Table 3-3069. Instance Table

Instance Name	Physical Address
SDFM0	5026 8098h
SDFM1	5026 9098h

Figure 3-1463. SDFLT4CMPHZ Name Register

15	14	13	12	11	10	9	8
RESERVED_1	HLTZ						
R	R/W						
0h	0h						
7	6	5	4	3	2	1	0
HLTZ							
R/W							
0h							

Access Types Legend

Table 3-3070. SDFLT4CMPHZ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
14:0	HLTZ	R/W	0h	Unsigned High-level threshold [Z] for the comparator filter output Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator SDCMPHx, it does not have the ability to generate an interrupt. Reset Source: sdfm_rst_mod_g_rst_n

3.22.59 MEM_SDFIFOCTL4 Registers

3.22.59.1 MEM_SDFIFOCTL4 Register (Offset = 9Ah) [reset = 0h]

Short Description: FIFO Control Register for

Long Description: FIFO Control Register for Ch4

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Table 3-3071. Instance Table

Instance Name	Physical Address
SDFM0	5026 809Ah
SDFM1	5026 909Ah

Figure 3-1464. SDFIFOCTL4 Name Register

15	14	13	12	11	10	9	8
OVFIEN	DRINTSEL	FFEN	FFIEN	RESERVED_2	SDFFST		
R/W	R/W	R/W	R/W	R	R		
0h	0h	0h	0h	0h	0h		
7	6	5	4	3	2	1	0
SDFFST		RESERVED_1	SDFFIL				
R		R	R/W				
0h		0h	0h				

Access Types Legend

Table 3-3072. SDFIFOCTL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OVFIEN	R/W	0h	SDFIFO Overflow interrupt enable 0: SDFIFO Overflow condition will not generate an interrupt 1: SDFIFO overflow condition generates an interrupt on SDy_ERR Reset Source: sdfm_rst_mod_g_rst_n
14	DRINTSEL	R/W	0h	Data-Ready Interrupt [DRINT] source select 0 = AF1 [Select non-FIFO data-ready interrupt] 1 = SDFFINT1 [Select FIFO data-ready interrupt] Reset Source: sdfm_rst_mod_g_rst_n
13	FFEN	R/W	0h	SDFIFO Enable 0: Disable FIFO operation 1: Enable FIFO operation Note: When FIFO is disabled, FIFO contents are cleared Reset Source: sdfm_rst_mod_g_rst_n
12	FFIEN	R/W	0h	SDFIFO data ready Interrupt Enable Reset Source: sdfm_rst_mod_g_rst_n
11	RESERVED_2	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
10:6	SDFFST	R	0h	SDFIFO Status 00000 FIFO empty 00001 FIFO has 1 word . . . . 10000 FIFO has 16 words Reset Source: sdfm_rst_mod_g_rst_n
5	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
4:0	SDFFIL	R/W	0h	SDFIFO interrupt level bits The FIFO will generate an interrupt when the FIFO status [SDFFST] '= FIFO level [SDFFIL] Reset Source: sdfm_rst_mod_g_rst_n

3.22.60 MEM_SDSYNC4 Registers

3.22.60.1 MEM_SDSYNC4 Register (Offset = 9Ch) [reset = 400h]

Short Description: SD Filter Sync control fo

Long Description: SD Filter Sync control for Ch4

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Table 3-3073. Instance Table

Instance Name	Physical Address
SDFM0	5026 809Ch
SDFM1	5026 909Ch

Figure 3-1465. SDSYNC4 Name Register

15	14	13	12	11	10	9	8
RESERVED_1					WTSCLREN	FFSYNCCLREN	WTSYNCLR
R					R/W	R/W	R/W
0h					1h	0h	0h
7	6	5	4	3	2	1	0
WTSYNFLG	WTSYNCEN	SYNCSEL					
R	R/W	R/W					
0h	0h	0h					

Access Types Legend

Table 3-3074. SDSYNC4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
10	WTSCLREN	R/W	1h	WTSYNFLG Clear-on-FIFOINT Enable 0: WTSYNFLG can only be cleared manually [using WTSYNCLR bit] 1: WTSYNFLG is cleared automatically on SDFFINT Reset Source: sdfm_rst_mod_g_rst_n
9	FFSYNCCLREN	R/W	0h	FIFO Clear-on-SDSYNC Enable 0: SDFIFO is not automaticaly cleared upon receiving SDSYNC 1: SDFIFO is automaticaly cleared upon receiving SDSYNC Reset Source: sdfm_rst_mod_g_rst_n
8	WTSYNCLR	R/W	0h	Wait-for-Sync Flag Clear [always reads 0] 0: Write of 0 has no affect 1: Write of 1 clears WTSYNFLG Reset Source: sdfm_rst_mod_g_rst_n
7	WTSYNFLG	R	0h	Wait-for-Sync Flag 0: SDSYNC event has not occurred 1: SDSYNC event occurred. Reset Source: sdfm_rst_mod_g_rst_n
6	WTSYNCEN	R/W	0h	Wait-for-Sync Enable 0: Incoming Data written to SDFIFO on every Data-Ready [DR] Event 1: Incoming Data written to SDFIFO on DR event only after SDSYNC event occurs Reset Source: sdfm_rst_mod_g_rst_n
5:0	SYNCSEL	R/W	0h	Defines source for the SDSYNC Input on this channel Refer SDSYNCx.SYNCSEL table Reset Source: sdfm_rst_mod_g_rst_n

3.22.61 MEM_SDFLT4CMPL2 Registers

3.22.61.1 MEM_SDFLT4CMPL2 Register (Offset = 9Eh) [reset = 0h]

Short Description: Second low level threhold

Long Description: Second low level threhold for CH4

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Table 3-3075. Instance Table

Instance Name	Physical Address
SDFM0	5026 809Eh
SDFM1	5026 909Eh

Figure 3-1466. SDFLT4CMPL2 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	LLT2						
R	R/W						
0h	0h						
7	6	5	4	3	2	1	0
LLT2							
R/W							
0h							

Access Types Legend

Table 3-3076. SDFLT4CMPL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
14:0	LLT2	R/W	0h	Second Unsigned low-level threshold for the comparator filter output. Reset Source: sdfm_rst_mod_g_rst_n

3.22.62 MEM_SDCOMP1CTL Registers

3.22.62.1 MEM_SDCOMP1CTL Register (Offset = C0h) [reset = 0h]

Short Description: SD Comparator event filte

Long Description: SD Comparator event filter1 Control Register

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Table 3-3077. Instance Table

Instance Name	Physical Address
SDFM0	5026 80C0h
SDFM1	5026 90C0h

Figure 3-1467. SDCOMP1CTL Name Register

15	14	13	12	11	10	9	8
RESERVED_10	RESERVED_9	RESERVED_8		CEVT2DIGFILTSEL		RESERVED_7	RESERVED_6
R	R	R		R/W		R	R
0h	0h	0h		0h		0h	0h
7	6	5	4	3	2	1	0
RESERVED_5	RESERVED_4	RESERVED_3		CEVT1DIGFILTSEL		RESERVED_2	RESERVED_1
R	R	R		R/W		R	R
0h	0h	0h		0h		0h	0h

Access Types Legend

Table 3-3078. SDCOMP1CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_10	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
14	RESERVED_9	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
13:12	RESERVED_8	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
11:10	CEVT2DIGFILTSEL	R/W	0h	High comparator COMPH source select. 0 CEVT2 output drives COMPLOUT 1 Reserved 2 Output of digital filter drives COMPLOUT 3 Reserved Reset Source: sdfm_rst_mod_g_rst_n
9	RESERVED_7	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
8	RESERVED_6	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
7	RESERVED_5	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
6	RESERVED_4	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
5:4	RESERVED_3	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
3:2	CEVT1DIGFILTSEL	R/W	0h	High comparator COMPH source select. 0 CEVT1 output drives COMPHOUT 1 Reserved 2 Output of digital filter drives COMPHOUT 3 Reserved Reset Source: sdfm_rst_mod_g_rst_n
1	RESERVED_2	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
0	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n

3.22.63 MEM_SDCOMP1EVT2FLTCTL Registers

3.22.63.1 MEM_SDCOMP1EVT2FLTCTL Register (Offset = C2h) [reset = 0h]

Short Description: COMPL/CEVT2 Digital filte

Long Description: COMPL/CEVT2 Digital filter1 Control Register

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Table 3-3079. Instance Table

Instance Name	Physical Address
SDFM0	5026 80C2h
SDFM1	5026 90C2h

Figure 3-1468. SDCOMP1EVT2FLTCTL Name Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED_2	THRESH					SAMPWIN
R/W1TS	R	R/W					R/W
0h	0h	0h					0h
7	6	5	4	3	2	1	0
SAMPWIN				RESERVED_1			
R/W				R			
0h				0h			

Access Types Legend

Table 3-3080. SDCOMP1EVT2FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R/W1TS	0h	Low filter initialization. 0 No effect 1 Initialize all samples to the filter input value Reset Source: sdfm_rst_mod_g_rst_n
14	RESERVED_2	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
13:9	THRESH	R/W	0h	Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Reset Source: sdfm_rst_mod_g_rst_n
8:4	SAMPWIN	R/W	0h	Low filter sample window size. Number of samples to monitor is SAMPWIN+1. Reset Source: sdfm_rst_mod_g_rst_n
3:0	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n

3.22.64 MEM_SDCOMP1EVT2FLTCLKCTL Registers

3.22.64.1 MEM_SDCOMP1EVT2FLTCLKCTL Register (Offset = C4h) [reset = 0h]

Short Description: COMPL/CEVT2 Digital filte

Long Description: COMPL/CEVT2 Digital filter1 Clock Control Register

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Table 3-3081. Instance Table

Instance Name	Physical Address
SDFM0	5026 80C4h
SDFM1	5026 90C4h

Figure 3-1469. SDCOMP1EVT2FLTCLKCTL Name Register

15	14	13	12	11	10	9	8
RESERVED_1						CLKPRESCALE	
R						R/W	
0h						0h	
7	6	5	4	3	2	1	0
CLKPRESCALE							
R/W							
0h							

Access Types Legend

Table 3-3082. SDCOMP1EVT2FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
9:0	CLKPRESCALE	R/W	0h	Low filter sample clock prescale. Number of system clocks between samples. Reset Source: sdfm_rst_mod_g_rst_n

3.22.65 MEM_SDCOMP1EVT1FLTCTL Registers

3.22.65.1 MEM_SDCOMP1EVT1FLTCTL Register (Offset = C6h) [reset = 0h]

Short Description: COMPH/CEVT1 Digital filte

Long Description: COMPH/CEVT1 Digital filter1 Control Register

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Table 3-3083. Instance Table

Instance Name	Physical Address
SDFM0	5026 80C6h
SDFM1	5026 90C6h

Figure 3-1470. SDCOMP1EVT1FLTCTL Name Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED_2	THRESH					SAMPWIN
R/W1TS	R	R/W					R/W
0h	0h	0h					0h
7	6	5	4	3	2	1	0
SAMPWIN				RESERVED_1			
R/W				R			
0h				0h			

Access Types Legend

Table 3-3084. SDCOMP1EVT1FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R/W1TS	0h	High filter initialization. 0 No effect 1 Initialize all samples to the filter input value Reset Source: sdfm_rst_mod_g_rst_n
14	RESERVED_2	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
13:9	THRESH	R/W	0h	High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Reset Source: sdfm_rst_mod_g_rst_n
8:4	SAMPWIN	R/W	0h	High filter sample window size. Number of samples to monitor is SAMPWIN+1. Reset Source: sdfm_rst_mod_g_rst_n
3:0	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n

3.22.66 MEM_SDCOMP1EVT1FLTCLKCTL Registers

3.22.66.1 MEM_SDCOMP1EVT1FLTCLKCTL Register (Offset = C8h) [reset = 0h]

Short Description: COMPH/CEVT1 Digital filte

Long Description: COMPH/CEVT1 Digital filter1 Clock Control Register

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Table 3-3085. Instance Table

Instance Name	Physical Address
SDFM0	5026 80C8h
SDFM1	5026 90C8h

Figure 3-1471. SDCOMP1EVT1FLTCLKCTL Name Register

15	14	13	12	11	10	9	8
RESERVED_1						CLKPRESCALE	
R						R/W	
0h						0h	
7	6	5	4	3	2	1	0
CLKPRESCALE							
R/W							
0h							

Access Types Legend

Table 3-3086. SDCOMP1EVT1FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
9:0	CLKPRESCALE	R/W	0h	High filter sample clock prescale. Number of system clocks between samples. Reset Source: sdfm_rst_mod_g_rst_n

3.22.67 MEM_SDCOMP1LOCK Registers

3.22.67.1 MEM_SDCOMP1LOCK Register (Offset = CEh) [reset = 0h]

Short Description: SD compartor event filte

Long Description: SD compartor event filter1 Lock Register

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Table 3-3087. Instance Table

Instance Name	Physical Address
SDFM0	5026 80CEh
SDFM1	5026 90CEh

Figure 3-1472. SDCOMP1LOCK Name Register

15	14	13	12	11	10	9	8
RESERVED_4							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_4			RESERVED_3	COMP	RESERVED_2	RESERVED_1	SDCOMP1CTL
R			R	R/W1TS	R	R	R/W1TS
0h			0h	0h	0h	0h	0h

Access Types Legend

Table 3-3088. SDCOMP1LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15:5	RESERVED_4	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
4	RESERVED_3	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
3	COMP	R/W1TS	0h	Lock write-access to the SDCOMP1EVT1/2FLTTCTL and COMP1FILCLKCTL registers. 0 SDCOMP1EVT1/2FLTCTL and SDCOMP1EVT1/2FLTCLKCTL registers are not locked. Write 0 to this bit has no effect. 1 SDCOMP1EVT1/2FLTCTL and SDCOMP1EVT1/2FLTCLKCTL registers are locked. Only a system reset can clear this bit. Reset Source: sdfm_rst_mod_g_rst_n
2	RESERVED_2	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
1	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
0	SDCOMP1CTL	R/W1TS	0h	Lock write-access to the SDCOMP1CTL register. 0 SDCOMP1CTL register is not locked. Write 0 to this bit has no effect. 1 SDCOMP1CTL register is locked. Only a system reset can clear this bit. Reset Source: sdfm_rst_mod_g_rst_n

3.22.68 MEM_SDCOMP2CTL Registers

3.22.68.1 MEM_SDCOMP2CTL Register (Offset = D0h) [reset = 0h]

Short Description: SD Comparator event filte

Long Description: SD Comparator event filter2 Control Register

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Table 3-3089. Instance Table

Instance Name	Physical Address
SDFM0	5026 80D0h
SDFM1	5026 90D0h

Figure 3-1473. SDCOMP2CTL Name Register

15	14	13	12	11	10	9	8
RESERVED_10	RESERVED_9	RESERVED_8		CEVT2DIGFILTSEL		RESERVED_7	RESERVED_6
R	R	R		R/W		R	R
0h	0h	0h		0h		0h	0h
7	6	5	4	3	2	1	0
RESERVED_5	RESERVED_4	RESERVED_3		CEVT1DIGFILTSEL		RESERVED_2	RESERVED_1
R	R	R		R/W		R	R
0h	0h	0h		0h		0h	0h

Access Types Legend

Table 3-3090. SDCOMP2CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_10	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
14	RESERVED_9	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
13:12	RESERVED_8	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
11:10	CEVT2DIGFILTSEL	R/W	0h	High comparator COMPH source select. 0 CEVT2 output drives COMPLOUT 1 Reserved 2 Output of digital filter drives COMPLOUT 3 Reserved Reset Source: sdfm_rst_mod_g_rst_n
9	RESERVED_7	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
8	RESERVED_6	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
7	RESERVED_5	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
6	RESERVED_4	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
5:4	RESERVED_3	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
3:2	CEVT1DIGFILTSEL	R/W	0h	High comparator COMPH source select. 0 CEVT1 output drives COMPHOUT 1 Reserved 2 Output of digital filter drives COMPHOUT 3 Reserved Reset Source: sdfm_rst_mod_g_rst_n
1	RESERVED_2	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
0	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n

3.22.69 MEM_SDCOMP2EVT2FLTCTL Registers

3.22.69.1 MEM_SDCOMP2EVT2FLTCTL Register (Offset = D2h) [reset = 0h]

Short Description: COMPL/CEVT2 Digital filte

Long Description: COMPL/CEVT2 Digital filter2 Control Register

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Table 3-3091. Instance Table

Instance Name	Physical Address
SDFM0	5026 80D2h
SDFM1	5026 90D2h

Figure 3-1474. SDCOMP2EVT2FLTCTL Name Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED_2	THRESH					SAMPWIN
R/W1TS	R	R/W					R/W
0h	0h	0h					0h
7	6	5	4	3	2	1	0
SAMPWIN				RESERVED_1			
R/W				R			
0h				0h			

Access Types Legend

Table 3-3092. SDCOMP2EVT2FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R/W1TS	0h	Low filter initialization. 0 No effect 1 Initialize all samples to the filter input value Reset Source: sdfm_rst_mod_g_rst_n
14	RESERVED_2	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
13:9	THRESH	R/W	0h	Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Reset Source: sdfm_rst_mod_g_rst_n
8:4	SAMPWIN	R/W	0h	Low filter sample window size. Number of samples to monitor is SAMPWIN+1. Reset Source: sdfm_rst_mod_g_rst_n
3:0	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n

3.22.70 MEM_SDCOMP2EVT2FLTCLKCTL Registers

3.22.70.1 MEM_SDCOMP2EVT2FLTCLKCTL Register (Offset = D4h) [reset = 0h]

Short Description: COMPL/CEVT2 Digital filte

Long Description: COMPL/CEVT2 Digital filter2 Clock Control Register

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Table 3-3093. Instance Table

Instance Name	Physical Address
SDFM0	5026 80D4h
SDFM1	5026 90D4h

Figure 3-1475. SDCOMP2EVT2FLTCLKCTL Name Register

15	14	13	12	11	10	9	8
RESERVED_1						CLKPRESCALE	
R						R/W	
0h						0h	
7	6	5	4	3	2	1	0
CLKPRESCALE							
R/W							
0h							

Access Types Legend

Table 3-3094. SDCOMP2EVT2FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
9:0	CLKPRESCALE	R/W	0h	Low filter sample clock prescale. Number of system clocks between samples. Reset Source: sdfm_rst_mod_g_rst_n

3.22.71 MEM_SDCOMP2EVT1FLTCTL Registers

3.22.71.1 MEM_SDCOMP2EVT1FLTCTL Register (Offset = D6h) [reset = 0h]

Short Description: COMPH/CEVT1 Digital filte

Long Description: COMPH/CEVT1 Digital filter2 Control Register

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Table 3-3095. Instance Table

Instance Name	Physical Address
SDFM0	5026 80D6h
SDFM1	5026 90D6h

Figure 3-1476. SDCOMP2EVT1FLTCTL Name Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED_2	THRESH					SAMPWIN
R/W1TS	R	R/W					R/W
0h	0h	0h					0h
7	6	5	4	3	2	1	0
SAMPWIN				RESERVED_1			
R/W				R			
0h				0h			

Access Types Legend

Table 3-3096. SDCOMP2EVT1FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R/W1TS	0h	High filter initialization. 0 No effect 1 Initialize all samples to the filter input value Reset Source: sdfm_rst_mod_g_rst_n
14	RESERVED_2	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
13:9	THRESH	R/W	0h	High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Reset Source: sdfm_rst_mod_g_rst_n
8:4	SAMPWIN	R/W	0h	High filter sample window size. Number of samples to monitor is SAMPWIN+1. Reset Source: sdfm_rst_mod_g_rst_n
3:0	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n

3.22.72 MEM_SDCOMP2EVT1FLTCLKCTL Registers

3.22.72.1 MEM_SDCOMP2EVT1FLTCLKCTL Register (Offset = D8h) [reset = 0h]

Short Description: COMPH/CEVT1 Digital filte

Long Description: COMPH/CEVT1 Digital filter2 Clock Control Register

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Table 3-3097. Instance Table

Instance Name	Physical Address
SDFM0	5026 80D8h
SDFM1	5026 90D8h

Figure 3-1477. SDCOMP2EVT1FLTCLKCTL Name Register

15	14	13	12	11	10	9	8
RESERVED_1						CLKPRESCALE	
R						R/W	
0h						0h	
7	6	5	4	3	2	1	0
CLKPRESCALE							
R/W							
0h							

Access Types Legend

Table 3-3098. SDCOMP2EVT1FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
9:0	CLKPRESCALE	R/W	0h	High filter sample clock prescale. Number of system clocks between samples. Reset Source: sdfm_rst_mod_g_rst_n

3.22.73 MEM_SDCOMP2LOCK Registers

3.22.73.1 MEM_SDCOMP2LOCK Register (Offset = DEh) [reset = 0h]

Short Description: SD compartor event filte

Long Description: SD compartor event filter2 Lock Register

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Table 3-3099. Instance Table

Instance Name	Physical Address
SDFM0	5026 80DEh
SDFM1	5026 90DEh

Figure 3-1478. SDCOMP2LOCK Name Register

15	14	13	12	11	10	9	8
RESERVED_4							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_4			RESERVED_3	COMP	RESERVED_2	RESERVED_1	SDCOMP2CTL
R			R	R/W1TS	R	R	R/W1TS
0h			0h	0h	0h	0h	0h

Access Types Legend

Table 3-3100. SDCOMP2LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15:5	RESERVED_4	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
4	RESERVED_3	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
3	COMP	R/W1TS	0h	Lock write-access to the SDCOMP2EVT1/2FLTTCTL and COMP2FILCLKCTL registers. 0 SDCOMP2EVT1/2FLTCTL and SDCOMP2EVT1/2FLTCLKCTL registers are not locked. Write 0 to this bit has no effect. 1 SDCOMP2EVT1/2FLTCTL and SDCOMP2EVT1/2FLTCLKCTL registers are locked. Only a system reset can clear this bit. Reset Source: sdfm_rst_mod_g_rst_n
2	RESERVED_2	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
1	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
0	SDCOMP2CTL	R/W1TS	0h	Lock write-access to the SDCOMP2CTL register. 0 SDCOMP2CTL register is not locked. Write 0 to this bit has no effect. 1 SDCOMP2CTL register is locked. Only a system reset can clear this bit. Reset Source: sdfm_rst_mod_g_rst_n

3.22.74 MEM_SDCOMP3CTL Registers

3.22.74.1 MEM_SDCOMP3CTL Register (Offset = E0h) [reset = 0h]

Short Description: SD Comparator event filte

Long Description: SD Comparator event filter3 Control Register

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Table 3-3101. Instance Table

Instance Name	Physical Address
SDFM0	5026 80E0h
SDFM1	5026 90E0h

Figure 3-1479. SDCOMP3CTL Name Register

15	14	13	12	11	10	9	8
RESERVED_10	RESERVED_9	RESERVED_8		CEVT2DIGFILTSEL		RESERVED_7	RESERVED_6
R	R	R		R/W		R	R
0h	0h	0h		0h		0h	0h
7	6	5	4	3	2	1	0
RESERVED_5	RESERVED_4	RESERVED_3		CEVT1DIGFILTSEL		RESERVED_2	RESERVED_1
R	R	R		R/W		R	R
0h	0h	0h		0h		0h	0h

Access Types Legend

Table 3-3102. SDCOMP3CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_10	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
14	RESERVED_9	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
13:12	RESERVED_8	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
11:10	CEVT2DIGFILTSEL	R/W	0h	High comparator COMPH source select. 0 CEVT2 output drives COMPLOUT 1 Reserved 2 Output of digital filter drives COMPLOUT 3 Reserved Reset Source: sdfm_rst_mod_g_rst_n
9	RESERVED_7	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
8	RESERVED_6	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
7	RESERVED_5	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
6	RESERVED_4	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
5:4	RESERVED_3	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
3:2	CEVT1DIGFILTSEL	R/W	0h	High comparator COMPH source select. 0 CEVT1 output drives COMPHOUT 1 Reserved 2 Output of digital filter drives COMPHOUT 3 Reserved Reset Source: sdfm_rst_mod_g_rst_n
1	RESERVED_2	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
0	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n

3.22.75 MEM_SDCOMP3EVT2FLTCTL Registers

3.22.75.1 MEM_SDCOMP3EVT2FLTCTL Register (Offset = E2h) [reset = 0h]

Short Description: COMPL/CEVT2 Digital filte

Long Description: COMPL/CEVT2 Digital filter3 Control Register

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Table 3-3103. Instance Table

Instance Name	Physical Address
SDFM0	5026 80E2h
SDFM1	5026 90E2h

Figure 3-1480. SDCOMP3EVT2FLTCTL Name Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED_2	THRESH					SAMPWIN
R/W1TS	R	R/W					R/W
0h	0h	0h					0h
7	6	5	4	3	2	1	0
SAMPWIN				RESERVED_1			
R/W				R			
0h				0h			

Access Types Legend

Table 3-3104. SDCOMP3EVT2FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R/W1TS	0h	Low filter initialization. 0 No effect 1 Initialize all samples to the filter input value Reset Source: sdfm_rst_mod_g_rst_n
14	RESERVED_2	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
13:9	THRESH	R/W	0h	Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Reset Source: sdfm_rst_mod_g_rst_n
8:4	SAMPWIN	R/W	0h	Low filter sample window size. Number of samples to monitor is SAMPWIN+1. Reset Source: sdfm_rst_mod_g_rst_n
3:0	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n

3.22.76 MEM_SDCOMP3EVT2FLTCLKCTL Registers

3.22.76.1 MEM_SDCOMP3EVT2FLTCLKCTL Register (Offset = E4h) [reset = 0h]

Short Description: COMPL/CEVT2 Digital filte

Long Description: COMPL/CEVT2 Digital filter3 Clock Control Register

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Table 3-3105. Instance Table

Instance Name	Physical Address
SDFM0	5026 80E4h
SDFM1	5026 90E4h

Figure 3-1481. SDCOMP3EVT2FLTCLKCTL Name Register

15	14	13	12	11	10	9	8
RESERVED_1						CLKPRESCALE	
R						R/W	
0h						0h	
7	6	5	4	3	2	1	0
CLKPRESCALE							
R/W							
0h							

Access Types Legend

Table 3-3106. SDCOMP3EVT2FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
9:0	CLKPRESCALE	R/W	0h	Low filter sample clock prescale. Number of system clocks between samples. Reset Source: sdfm_rst_mod_g_rst_n

3.22.77 MEM_SDCOMP3EVT1FLTCTL Registers

3.22.77.1 MEM_SDCOMP3EVT1FLTCTL Register (Offset = E6h) [reset = 0h]

Short Description: COMPH/CEVT1 Digital filte

Long Description: COMPH/CEVT1 Digital filter3 Control Register

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Table 3-3107. Instance Table

Instance Name	Physical Address
SDFM0	5026 80E6h
SDFM1	5026 90E6h

Figure 3-1482. SDCOMP3EVT1FLTCTL Name Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED_2	THRESH					SAMPWIN
R/W1TS	R	R/W					R/W
0h	0h	0h					0h
7	6	5	4	3	2	1	0
SAMPWIN				RESERVED_1			
R/W				R			
0h				0h			

Access Types Legend

Table 3-3108. SDCOMP3EVT1FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R/W1TS	0h	High filter initialization. 0 No effect 1 Initialize all samples to the filter input value Reset Source: sdfm_rst_mod_g_rst_n
14	RESERVED_2	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
13:9	THRESH	R/W	0h	High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Reset Source: sdfm_rst_mod_g_rst_n
8:4	SAMPWIN	R/W	0h	High filter sample window size. Number of samples to monitor is SAMPWIN+1. Reset Source: sdfm_rst_mod_g_rst_n
3:0	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n

3.22.78 MEM_SDCOMP3EVT1FLTCLKCTL Registers

3.22.78.1 MEM_SDCOMP3EVT1FLTCLKCTL Register (Offset = E8h) [reset = 0h]

Short Description: COMPH/CEVT1 Digital filte

Long Description: COMPH/CEVT1 Digital filter3 Clock Control Register

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Table 3-3109. Instance Table

Instance Name	Physical Address
SDFM0	5026 80E8h
SDFM1	5026 90E8h

Figure 3-1483. SDCOMP3EVT1FLTCLKCTL Name Register

15	14	13	12	11	10	9	8
RESERVED_1						CLKPRESCALE	
R						R/W	
0h						0h	
7	6	5	4	3	2	1	0
CLKPRESCALE							
R/W							
0h							

Access Types Legend

Table 3-3110. SDCOMP3EVT1FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
9:0	CLKPRESCALE	R/W	0h	High filter sample clock prescale. Number of system clocks between samples. Reset Source: sdfm_rst_mod_g_rst_n

3.22.79 MEM_SDCOMP3LOCK Registers

3.22.79.1 MEM_SDCOMP3LOCK Register (Offset = EEh) [reset = 0h]

Short Description: SD compartor event filte

Long Description: SD compartor event filter3 Lock Register

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Table 3-3111. Instance Table

Instance Name	Physical Address
SDFM0	5026 80EEh
SDFM1	5026 90EEh

Figure 3-1484. SDCOMP3LOCK Name Register

15	14	13	12	11	10	9	8
RESERVED_4							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_4			RESERVED_3	COMP	RESERVED_2	RESERVED_1	SDCOMP3CTL
R			R	R/W1TS	R	R	R/W1TS
0h			0h	0h	0h	0h	0h

Access Types Legend

Table 3-3112. SDCOMP3LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15:5	RESERVED_4	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
4	RESERVED_3	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
3	COMP	R/W1TS	0h	Lock write-access to the SDCOMP3EVT1/2FLTTCTL and COMP3FILCLKCTL registers. 0 SDCOMP3EVT1/2FLTCTL and SDCOMP3EVT1/2FLTCLKCTL registers are not locked. Write 0 to this bit has no effect. 1 SDCOMP3EVT1/2FLTCTL and SDCOMP3EVT1/2FLTCLKCTL registers are locked. Only a system reset can clear this bit. Reset Source: sdfm_rst_mod_g_rst_n
2	RESERVED_2	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
1	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
0	SDCOMP3CTL	R/W1TS	0h	Lock write-access to the SDCOMP3CTL register. 0 SDCOMP3CTL register is not locked. Write 0 to this bit has no effect. 1 SDCOMP3CTL register is locked. Only a system reset can clear this bit. Reset Source: sdfm_rst_mod_g_rst_n

3.22.80 MEM_SDCOMP4CTL Registers

3.22.80.1 MEM_SDCOMP4CTL Register (Offset = F0h) [reset = 0h]

Short Description: SD Comparator event filte

Long Description: SD Comparator event filter4 Control Register

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Table 3-3113. Instance Table

Instance Name	Physical Address
SDFM0	5026 80F0h
SDFM1	5026 90F0h

Figure 3-1485. SDCOMP4CTL Name Register

15	14	13	12	11	10	9	8
RESERVED_10	RESERVED_9	RESERVED_8		CEVT2DIGFILTSEL		RESERVED_7	RESERVED_6
R	R	R		R/W		R	R
0h	0h	0h		0h		0h	0h
7	6	5	4	3	2	1	0
RESERVED_5	RESERVED_4	RESERVED_3		CEVT1DIGFILTSEL		RESERVED_2	RESERVED_1
R	R	R		R/W		R	R
0h	0h	0h		0h		0h	0h

Access Types Legend

Table 3-3114. SDCOMP4CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_10	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
14	RESERVED_9	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
13:12	RESERVED_8	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
11:10	CEVT2DIGFILTSEL	R/W	0h	High comparator COMPH source select. 0 CEVT2 output drives COMPLOUT 1 Reserved 2 Output of digital filter drives COMPLOUT 3 Reserved Reset Source: sdfm_rst_mod_g_rst_n
9	RESERVED_7	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
8	RESERVED_6	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
7	RESERVED_5	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
6	RESERVED_4	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
5:4	RESERVED_3	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
3:2	CEVT1DIGFILTSEL	R/W	0h	High comparator COMPH source select. 0 CEVT1 output drives COMPHOUT 1 Reserved 2 Output of digital filter drives COMPHOUT 3 Reserved Reset Source: sdfm_rst_mod_g_rst_n
1	RESERVED_2	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
0	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n

3.22.81 MEM_SDCOMP4EVT2FLTCTL Registers

3.22.81.1 MEM_SDCOMP4EVT2FLTCTL Register (Offset = F2h) [reset = 0h]

Short Description: COMPL/CEVT2 Digital filte

Long Description: COMPL/CEVT2 Digital filter4 Control Register

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Table 3-3115. Instance Table

Instance Name	Physical Address
SDFM0	5026 80F2h
SDFM1	5026 90F2h

Figure 3-1486. SDCOMP4EVT2FLTCTL Name Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED_2	THRESH					SAMPWIN
R/W1TS	R	R/W					R/W
0h	0h	0h					0h
7	6	5	4	3	2	1	0
SAMPWIN				RESERVED_1			
R/W				R			
0h				0h			

Access Types Legend

Table 3-3116. SDCOMP4EVT2FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R/W1TS	0h	Low filter initialization. 0 No effect 1 Initialize all samples to the filter input value Reset Source: sdfm_rst_mod_g_rst_n
14	RESERVED_2	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
13:9	THRESH	R/W	0h	Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Reset Source: sdfm_rst_mod_g_rst_n
8:4	SAMPWIN	R/W	0h	Low filter sample window size. Number of samples to monitor is SAMPWIN+1. Reset Source: sdfm_rst_mod_g_rst_n
3:0	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n

3.22.82 MEM_SDCOMP4EVT2FLTCLKCTL Registers

3.22.82.1 MEM_SDCOMP4EVT2FLTCLKCTL Register (Offset = F4h) [reset = 0h]

Short Description: COMPL/CEVT2 Digital filte

Long Description: COMPL/CEVT2 Digital filter4 Clock Control Register

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Table 3-3117. Instance Table

Instance Name	Physical Address
SDFM0	5026 80F4h
SDFM1	5026 90F4h

Figure 3-1487. SDCOMP4EVT2FLTCLKCTL Name Register

15	14	13	12	11	10	9	8
RESERVED_1						CLKPRESCALE	
R						R/W	
0h						0h	
7	6	5	4	3	2	1	0
CLKPRESCALE							
R/W							
0h							

Access Types Legend

Table 3-3118. SDCOMP4EVT2FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
9:0	CLKPRESCALE	R/W	0h	Low filter sample clock prescale. Number of system clocks between samples. Reset Source: sdfm_rst_mod_g_rst_n

3.22.83 MEM_SDCOMP4EVT1FLTCTL Registers

3.22.83.1 MEM_SDCOMP4EVT1FLTCTL Register (Offset = F6h) [reset = 0h]

Short Description: COMPH/CEVT1 Digital filte

Long Description: COMPH/CEVT1 Digital filter4 Control Register

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Table 3-3119. Instance Table

Instance Name	Physical Address
SDFM0	5026 80F6h
SDFM1	5026 90F6h

Figure 3-1488. SDCOMP4EVT1FLTCTL Name Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED_2	THRESH					SAMPWIN
R/W1TS	R	R/W					R/W
0h	0h	0h					0h
7	6	5	4	3	2	1	0
SAMPWIN				RESERVED_1			
R/W				R			
0h				0h			

Access Types Legend

Table 3-3120. SDCOMP4EVT1FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R/W1TS	0h	High filter initialization. 0 No effect 1 Initialize all samples to the filter input value Reset Source: sdfm_rst_mod_g_rst_n
14	RESERVED_2	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
13:9	THRESH	R/W	0h	High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Reset Source: sdfm_rst_mod_g_rst_n
8:4	SAMPWIN	R/W	0h	High filter sample window size. Number of samples to monitor is SAMPWIN+1. Reset Source: sdfm_rst_mod_g_rst_n
3:0	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n

3.22.84 MEM_SDCOMP4EVT1FLTCLKCTL Registers

3.22.84.1 MEM_SDCOMP4EVT1FLTCLKCTL Register (Offset = F8h) [reset = 0h]

Short Description: COMPH/CEVT1 Digital filte

Long Description: COMPH/CEVT1 Digital filter4 Clock Control Register

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Table 3-3121. Instance Table

Instance Name	Physical Address
SDFM0	5026 80F8h
SDFM1	5026 90F8h

Figure 3-1489. SDCOMP4EVT1FLTCLKCTL Name Register

15	14	13	12	11	10	9	8
RESERVED_1						CLKPRESCALE	
R						R/W	
0h						0h	
7	6	5	4	3	2	1	0
CLKPRESCALE							
R/W							
0h							

Access Types Legend

Table 3-3122. SDCOMP4EVT1FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
9:0	CLKPRESCALE	R/W	0h	High filter sample clock prescale. Number of system clocks between samples. Reset Source: sdfm_rst_mod_g_rst_n

3.22.85 MEM_SDCOMP4LOCK Registers

3.22.85.1 MEM_SDCOMP4LOCK Register (Offset = FEh) [reset = 0h]

Short Description: SD compartor event filte

Long Description: SD compartor event filter4 Lock Register

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Table 3-3123. Instance Table

Instance Name	Physical Address
SDFM0	5026 80FEh
SDFM1	5026 90FEh

Figure 3-1490. SDCOMP4LOCK Name Register

15	14	13	12	11	10	9	8
RESERVED_4							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_4			RESERVED_3	COMP	RESERVED_2	RESERVED_1	SDCOMP4CTL
R			R	R/W1TS	R	R	R/W1TS
0h			0h	0h	0h	0h	0h

Access Types Legend

Table 3-3124. SDCOMP4LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15:5	RESERVED_4	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
4	RESERVED_3	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
3	COMP	R/W1TS	0h	Lock write-access to the SDCOMP4EVT1/2FLTTCTL and COMP4FILCLKCTL registers. 0 SDCOMP4EVT1/2FLTCTL and SDCOMP4EVT1/2FLTCLKCTL registers are not locked. Write 0 to this bit has no effect. 1 SDCOMP4EVT1/2FLTCTL and SDCOMP4EVT1/2FLTCLKCTL registers are locked. Only a system reset can clear this bit. Reset Source: sdfm_rst_mod_g_rst_n
2	RESERVED_2	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
1	RESERVED_1	R	0h	Reserved Reset Source: sdfm_rst_mod_g_rst_n
0	SDCOMP4CTL	R/W1TS	0h	Lock write-access to the SDCOMP4CTL register. 0 SDCOMP4CTL register is not locked. Write 0 to this bit has no effect. 1 SDCOMP4CTL register is locked. Only a system reset can clear this bit. Reset Source: sdfm_rst_mod_g_rst_n

3.22.86 Access Table

Table 3-3125. Access Type Codes

Access Type	Code	Description
R	R	Read
R/W1TS	R/W1TS	Read/Write 1 To Set
R/W	R/W	Read / Write

3.23 SoC_TIMESYNC_XBAR0 Registers

Table 3-3126. INTR_ROUTER_CFG, INTR_ROUTER_CFG Registers, Base Address=0X0000000052E00000, Length=1024

Offset	Length	Register Name	SoC_TIMESYNC_XBAR0_0 Physical Address
0h	32	PID	52E0 0000h
4h + Formula	32	muxcntl_N	52E0 0004h + Formula

3.23.1 INTR_ROUTER_CFG_PID Registers

3.23.1.1 INTR_CFG_PID Register (Offset = 0h) [reset = 66948100h]

Short Description: Identification register

Long Description: Identification register

Return to Summary Table

Table 3-3127. Instance Table

Instance Name	Physical Address
SOC_TIMESYNC_XBAR0_0	52E0 0000h

Figure 3-1491. PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		FUNCTION											
R		R		R											
1h		2h		694h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTLVER				MAJREV				CUSTOM		MINREV					
R				R				R		R					
10h				1h				0h		0h					

Access Types Legend

Table 3-3128. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	scheme Reset Source: intr_rst_n
29:28	BU	R	2h	bu Reset Source: intr_rst_n
27:16	FUNCTION	R	694h	function Reset Source: intr_rst_n
15:11	RTLVER	R	10h	rtl version Reset Source: intr_rst_n
10:8	MAJREV	R	1h	major version Reset Source: intr_rst_n
7:6	CUSTOM	R	0h	custom id Reset Source: intr_rst_n
5:0	MINREV	R	0h	minor version Reset Source: intr_rst_n

3.23.2 INTR_ROUTER_CFG_MUXCNTL_N Registers

3.23.2.1 INTR_CFG_MUXCNTL_N Register (Offset = 4h) [reset = 0h]

Short Description: Interrupt mux control reg

Long Description: Interrupt mux control register

Return to Summary Table

Offset = 4h + (j * 4h); where j = 0h to 13h

Table 3-3129. Instance Table

Instance Name	Physical Address
SOC_TIMESYNC_XBAR0_0	52E0 0004h

Figure 3-1492. MUXCNTL_N Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															INT_ENABLE
NONE															R/W
0															0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											MUX_CNTL				
NONE											R/W				
0											0h				

Access Types Legend

Table 3-3130. MUXCNTL_N Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE		Reserved
16	INT_ENABLE	R/W	0h	interrupt output enable for interrupt N Reset Source: intr_rst_n
15:5	RESERVED	NONE		Reserved
4:0	MUX_CNTL	R/W	0h	Mux control for interrupt N Reset Source: intr_rst_n

3.23.3 Access Table

Table 3-3131. Access Type Codes

Access Type	Code	Description
R	R	Read
R/W	R/W	Read / Write

3.24 SoC_TIMESYNC_XBAR1 Registers

Table 3-3132. INTR_ROUTER_CFG, INTR_ROUTER_CFG Registers, Base Address=0X0000000052E04000, Length=2048

Offset	Length	Register Name	SoC_TIMESYNC_XBAR1_1 Physical Address
0h	32	PID	52E0 4000h
4h + Formula	32	muxcntl_N	52E0 4004h + Formula

3.24.1 INTR_ROUTER_CFG_PID Registers

3.24.1.1 INTR_CFG_PID Register (Offset = 0h) [reset = 66948100h]

Short Description: Identification register

Long Description: Identification register

Return to Summary Table

Table 3-3133. Instance Table

Instance Name	Physical Address
SOC_TIMESYNC_XBAR1_1	52E0 4000h

Figure 3-1493. PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		FUNCTION											
R		R		R											
1h		2h		694h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTLVER				MAJREV				CUSTOM		MINREV					
R				R				R		R					
10h				1h				0h		0h					

Access Types Legend

Table 3-3134. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	scheme Reset Source: intr_rst_n
29:28	BU	R	2h	bu Reset Source: intr_rst_n
27:16	FUNCTION	R	694h	function Reset Source: intr_rst_n
15:11	RTLVER	R	10h	rtl version Reset Source: intr_rst_n
10:8	MAJREV	R	1h	major version Reset Source: intr_rst_n
7:6	CUSTOM	R	0h	custom id Reset Source: intr_rst_n
5:0	MINREV	R	0h	minor version Reset Source: intr_rst_n

3.24.2 INTR_ROUTER_CFG_MUXCNTL_N Registers

3.24.2.1 INTR_CFG_MUXCNTL_N Register (Offset = 4h) [reset = 0h]

Short Description: Interrupt mux control reg

Long Description: Interrupt mux control register

Return to Summary Table

Offset = 4h + (j * 4h); where j = 0h to 21h

Table 3-3135. Instance Table

Instance Name	Physical Address
SOC_TIMESYNC_XBAR1_1	52E0 4004h

Figure 3-1494. MUXCNTL_N Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															INT_ENABLE
NONE															R/W
0															0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												MUX_CNTL			
NONE												R/W			
0												0h			

Access Types Legend

Table 3-3136. MUXCNTL_N Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE		Reserved
16	INT_ENABLE	R/W	0h	interrupt output enable for interrupt N Reset Source: intr_rst_n
15:4	RESERVED	NONE		Reserved
3:0	MUX_CNTL	R/W	0h	Mux control for interrupt N Reset Source: intr_rst_n

3.24.3 Access Table

Table 3-3137. Access Type Codes

Access Type	Code	Description
R	R	Read
R/W	R/W	Read / Write

4 System-on-chip (SoC) Registers

The System-on-chip (SoC) module registers are described in the following sections.

Note

All images except for VIM images use hexadecimal. VIM uses decimal due to legacy documentation.

4.1 EXT_FLASH Registers

Table 4-1. MEM, MEM Registers, Base Address=0X0000000060000000, Length=33554432

Offset	Length	Register Name	ext_flash0 Physical Address	ext_flash1 Physical Address
0h	32	EXT_FLASH_START	6000 0000h	6200 0000h
1FFFFFCh	32	EXT_FLASH_END	61FF FFFCh	63FF FFFCh

4.1.1 MEM_EXT_FLASH_START Registers

4.1.1.1 MEM_FLASH_START Register (Offset = 0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 4-2. Instance Table

Instance Name	Physical Address
EXT_FLASH0	6000 0000h
EXT_FLASH1	6200 0000h

Figure 4-1. EXT_FLASH_START Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MEM_START															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MEM_START															
R/W															
0h															

Access Types Legend

Table 4-3. EXT_FLASH_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MEM_START	R/W	0h	External flash start Address Reset Source: ext_flash_rst_mod_g_rst_n

4.1.2 MEM_EXT_FLASH_END Registers

4.1.2.1 MEM_FLASH_END Register (Offset = 1FFFFFCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 4-4. Instance Table

Instance Name	Physical Address
EXT_FLASH0	61FF FFFCh
EXT_FLASH1	63FF FFFCh

Figure 4-2. EXT_FLASH_END Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MEM_END															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MEM_END															
R/W															
0h															

Access Types Legend

Table 4-5. EXT_FLASH_END Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MEM_END	R/W	0h	External flash end address Reset Source: ext_flash_rst_mod_g_rst_n

4.1.3 Access Table

Table 4-6. Access Type Codes

Access Type	Code	Description
R/W	R/W	Read / Write

4.2 EDMA_TRIGGER_XBAR_INTROUTER Registers

Table 4-7. INTR_ROUTER_CFG, INTR_ROUTER_CFG Registers, Base Address=0X0000000052E01000, Length=2048

Offset	Length	Register Name	EDMA_trigger_xbar_introuter Physical Address
0h	32	PID	52E0 1000h
4h + Formula	32	muxcntl_N	52E0 1004h + Formula

4.2.1 INTR_ROUTER_CFG_PID Registers

4.2.1.1 INTR_CFG_PID Register (Offset = 0h) [reset = 66948100h]

Short Description: Identification register

Long Description: Identification register

Return to Summary Table

Table 4-8. Instance Table

Instance Name	Physical Address
EDMA_TRIGGER_XBAR_INTROUTER	52E0 1000h

Figure 4-3. PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		FUNCTION											
R		R		R											
1h		2h		694h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTLVER					MAJREV			CUSTOM		MINREV					
R					R			R		R					
10h					1h			0h		0h					

Access Types Legend

Table 4-9. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	scheme
29:28	BU	R	2h	bu
27:16	FUNCTION	R	694h	function
15:11	RTLVER	R	10h	rtl version
10:8	MAJREV	R	1h	major version
7:6	CUSTOM	R	0h	custom id
5:0	MINREV	R	0h	minor version

4.2.2 INTR_ROUTER_CFG_MUXCNTL_N Registers

4.2.2.1 INTR_CFG_MUXCNTL_N Register (Offset = 4h) [reset = 0h]

Short Description: Interrupt mux control reg

Long Description: Interrupt mux control register

Return to Summary Table

Offset = 4h + (j * 4h); where j = 0h to 3Fh

Table 4-10. Instance Table

Instance Name	Physical Address
EDMA_TRIGGER_XBAR_INTROUTER	52E0 1004h

Figure 4-4. MUXCNTL_N Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															INT_ENABLE
NONE															R/W
0															0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MUX_CNTL							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-11. MUXCNTL_N Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE		Reserved
16	INT_ENABLE	R/W	0h	interrupt output enable for interrupt N
15:8	RESERVED	NONE		Reserved
7:0	MUX_CNTL	R/W	0h	Mux control for interrupt N

4.2.3 Access Table

Table 4-12. Access Type Codes

Access Type	Code	Description
R	R	Read
R/W	R/W	Read / Write

4.3 GPIO_XBAR_INTR Registers

Table 4-13. GPIO_XBAR_INTR Registers Base Address Table

Offset	Length	Acronym	GPIO_XBAR_INTR Physical Address
0h	32	GPIO_XBAR_INTR_PID	52E0 2000h
4h	16	GPIO_XBAR_INTR_MUXCNTL	52E0 2004h

4.3.1 GPIO_XBAR_INTR_PID Registers

4.3.1.1 GPIO_XBAR_INTR_PID Register (Offset = 0h) [reset = h]

Short Description: Identification register

Long Description:

Return to Summary Table

Table 4-14. Instance Table

Instance Name	Physical Address
GPIO_INTR_XBAR	52E0 2000h

Access Types Legend

Table 4-15. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	scheme
29 - 28	BU	RO	2h	bu
27 - 16	FUNCTION	RO	694h	function
15 - 11	RTLVER	RO	10h	rtl version
10 - 8	MAJREV	RO	1h	major version
7 - 6	CUSTOM	RO	0h	custom id
5 - 0	MINREV	RO	0h	minor version

4.3.2 GPIO_XBAR_INTR_MUXCNTL Registers

4.3.2.1 GPIO_XBAR_INTR_MUXCNTL Register (Offset = 4h) [reset = h]

Short Description: Interrupt mux control register

Long Description:

Return to Summary Table

Table 4-16. Instance Table

Instance Name	Physical Address
GPIO_INTR_XBAR	52E0 2004h

Access Types Legend

Table 4-17. MUXCNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
16	INT_ENABLE	RW	0h	interrupt output enable for interrupt N
	RESERVED	NONE		Reserved
7 - 0	ENABLE	RW	0h	Mux control for interrupt N

4.3.3 Access Table

Table 4-18. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write

4.4 PRU_ICSS_XBAR_INTR Registers

Table 4-19. PRU_ICSS_XBAR_INTR Registers Base Address Table

Offset	Length	Acronym	PRU_ICSS_XBAR_INTR Physical Address
0h	32	ICSSM_XBAR_INTR_PID	52E0 3000h
4h	16	ICSSM_XBAR_INTR_MUXCNTL	52E0 3004h

4.4.1 ICSSM_XBAR_INTR_PID Registers

4.4.1.1 ICSSM_XBAR_INTR_PID Register (Offset = 0h) [reset = h]

Short Description: Identification register

Long Description:

Return to Summary Table

Table 4-20. Instance Table

Instance Name	Physical Address
ICSSM_INTR_XBAR	52E0 3000h

Access Types Legend

Table 4-21. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	scheme
29 - 28	BU	RO	2h	bu
27 - 16	FUNCTION	RO	694h	function
15 - 11	RTLVER	RO	10h	rtl version
10 - 8	MAJREV	RO	1h	major version
7 - 6	CUSTOM	RO	0h	custom id
5 - 0	MINREV	RO	0h	minor version

4.4.2 ICSSM_XBAR_INTR_MUXCNTL Registers

4.4.2.1 ICSSM_XBAR_INTR_MUXCNTL Register (Offset = 4h) [reset = h]

Short Description: Interrupt mux control register

Long Description:

Return to Summary Table

Table 4-22. Instance Table

Instance Name	Physical Address
ICSSM_INTR_XBAR	52E0 3004h

Access Types Legend

Table 4-23. MUXCNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
16	INT_ENABLE	RW	0h	interrupt output enable for interrupt N
	RESERVED	NONE		Reserved
5 - 0	ENABLE	RW	0h	Mux control for interrupt N

4.4.3 Access Table

Table 4-24. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write

4.5 PRU-ICSS Registers

4.5.1 PRU_ICSS_CFG Registers

PRU_ICSS_CFG Registers lists the memory-mapped registers for the PRU-ICSS subsystem. All register offset addresses not listed in PRU_ICSS_CFG Registers should be considered as reserved locations and the register contents should not be modified.

Table 4-25. PRU_ICSS_CFG Instances

Instance	Base Address
PRU_ICSS_CFG	4802 6000h

Table 4-26. PRU_ICSS_CFG Registers

Offset	Acronym	Register Name	PRU_ICSS_CFG Physical Address
0h	PRU_ICSS_REVID	Revision Register	4802 6000h
4h	RESERVED		4802 6004h
8h	PRU_ICSS_GPCFG0	General Purpose Configuration 0 Register	4802 6008h
Ch	PRU_ICSS_GPCFG1	General Purpose Configuration 1 Register	4802 600Ch
10h	PRU_ICSS_CGR	Clock Gating Register	4802 6010h
14h	RESERVED		4802 6014h
28h	PRU_ICSS_PMAO	PRU Master Address Offset Register	4802 6028h
2Ch	PRU_ICSS_MII_RT	MII_RT Event Enable Register	4802 602Ch
30h	PRU_ICSS_IEPCLK	IEP Clock Source Register defines the source of the IEP clock.	4802 6030h
34h	PRU_ICSS_SPP	Scratch Pad Priority and Configuration Register	4802 6034h
40h	PRU_ICSS_PIN_MX	Pin Mux Select Register	4802 6040h

4.5.1.1 PRU_ICSS_REVID Register (Offset = 0h) [reset = 47000A02h]

PRU_ICSS_REVID is shown in Figure 4-5 and described in Table 4-28.

The Revision Register contains the ID and revision information.

Table 4-27. PRU_ICSS_REVID Instances

Instance	Physical Address
PRU_ICSS_CFG	4802 6000h

Figure 4-5. PRU_ICSS_REVID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															
R-6B080203 h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-28. PRU_ICSS_REVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REVISION	R	6B080203h	TI internal data. Identifies revision of peripheral.

4.5.1.2 PRU_ICSS_GPCFG0 Register (Offset = 8h) [reset = 0h]

PRU_ICSS_GPCFG0 is shown in Figure 4-6 and described in Table 4-30.

The General Purpose Configuration 0 Register defines the GPI/O configuration for PRU0.

Table 4-29. PRU_ICSS_GPCFG0 Instances

Instance	Physical Address
PRU_ICSS_CFG	4802 6008h

Figure 4-6. PRU_ICSS_GPCFG0 Register

31	30	29	28	27	26	25	24
RESERVED		PR0_PRU0_GP_MUX_SEL				PRU0_GPO_SH_SEL	PRU0_GPO_DIV1
R-0h		R/W-0h				R-0h	R/W-0h
23	22	21	20	19	18	17	16
PRU0_GPO_DIV1				PRU0_GPO_DIV0			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
PRU0_GPO_DIV0	PRU0_GPO_MODE	PRU0_GPI_SB	PRU0_GPI_DIV1				
R/W-0h	R/W-0h	R/W-0h	R/W-0h				
7	6	5	4	3	2	1	0
PRU0_GPI_DIV0					PRU0_GPI_CLK_MODE	PRU0_GPI_MODE	
R/W-0h					R/W-0h	R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-30. PRU_ICSS_GPCFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-26	PR0_PRU0_GP_MUX_SEL	R/W	0h	Controls the PRU-ICSS wrap mux selection. 0h: GP selected 1h: ENDAT (Peripheral Interface) 2h: MII mode 3h: SD mode 4h: Reserved
25	PRU0_GPO_SH_SEL	R	0h	Defines which shadow register is currently getting used for GPO shifting. 0h: gpo_sh0 is selected 1h: gpo_sh1 is selected
24-20	PRU0_GPO_DIV1	R/W	0h	Divisor value (divide by PRU0_GPO_DIV1 + 1). 0h: Div 1.0 1h: Div 1.5 2h: Div 2.0 .. 1Eh: Div 16.0 1Fh: Reserved

Table 4-30. PRU_ICSS_GPCFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-15	PRU0_GPO_DIV0	R/W	0h	Divisor value (divide by PRU0_GPO_DIV0 + 1). 0h: Div 1.0 1h: Div 1.5 2h: Div 2.0 .. 1Eh: Div 16.0 1Fh: Reserved
14	PRU0_GPO_MODE	R/W	0h	PRU GPO (R30) modes: 0h: Direct output mode 1h: Serial output mode
13	PRU0_GPI_SB	R/W	0h	Start Bit event for 28-bit shift mode. PRU0_GPI_SB (pru0_r31_status[29]) is set when first capture of a 1 on pru0_r31_status[0]. Read 0h: Start Bit event has not occurred. Read 1h: Start Bit event occurred. Write 0h: No Effect. Write 1h: Will clear PRU0_GPI_SB and clear the whole shift register.
12-8	PRU0_GPI_DIV1	R/W	0h	Divisor value (divide by PRU0_GPI_DIV1 + 1). 0h: Div 1.0 1h: Div 1.5 2h: Div 2.0 .. 1Eh: Div 16.0 1Fh: Reserved
7-3	PRU0_GPI_DIV0	R/W	0h	Divisor value (divide by PRU0_GPI_DIV0 + 1). 0h: Div 1.0 1h: Div 1.5 2h: Div 2.0 .. 1Eh: Div 16.0 1Fh: Reserved
2	PRU0_GPI_CLK_MODE	R/W	0h	Parallel 16-bit capture mode clock edge. 0h: Use the positive edge of pru0_r31_status[16] 1h: Use the negative edge of pru0_r31_status[16]
1-0	PRU0_GPI_MODE	R/W	0h	PRU GPI (R31) modes: 0h: Direct input mode 1h: 16-bit parallel capture mode 2h: 28-bit shift mode 3h: MII_RT mode

4.5.1.3 PRU_ICSS_GPCFG1 Register (Offset = Ch) [reset = 0h]

PRU_ICSS_GPCFG1 is shown in Figure 4-7 and described in Table 4-32.

The General Purpose Configuration 1 Register defines the GPI/O configuration for PRU1.

Table 4-31. PRU_ICSS_GPCFG1 Instances

Instance	Physical Address
PRU_ICSS_CFG	4802 600Ch

Figure 4-7. PRU_ICSS_GPCFG1 Register

31	30	29	28	27	26	25	24
RESERVED		PR0_PRU1_GP_MUX_SEL				PRU1_GPO_SH_SEL	PRU1_GPO_DIV1
R-0h		R/W-0h				R-0h	R/W-0h
23	22	21	20	19	18	17	16
PRU1_GPO_DIV1				PRU1_GPO_DIV0			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
PRU1_GPO_DIV0	PRU1_GPO_MODE	PRU1_GPI_SB	PRU1_GPI_DIV1				
R/W-0h	R/W-0h	R/W-0h	R/W-0h				
7	6	5	4	3	2	1	0
PRU1_GPI_DIV0					PRU1_GPI_CLK_MODE	PRU1_GPI_MODE	
R/W-0h					R/W-0h	R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-32. PRU_ICSS_GPCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-26	PR0_PRU1_GP_MUX_SEL	R/W	0h	Controls the PRU-ICSS wrap mux selection. 0h: GP selected 1h: ENDAT (Peripheral Interface) 2h: MII mode 3h: SD mode 4h: Reserved
25	PRU1_GPO_SH_SEL	R	0h	Defines which shadow register is currently getting used for GPO shifting. 0h = gpo_sh0 is selected 1h = gpo_sh1 is selected
24-20	PRU1_GPO_DIV1	R/W	0h	Divisor value (divide by PRU1_GPO_DIV1 + 1). 0h: Div 1.0 1h: Div 1.5 2h: Div 2.0 .. 1Eh: Div 16.0 1Fh: Reserved

Table 4-32. PRU_ICSS_GPCFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-15	PRU1_GPO_DIV0	R/W	0h	Divisor value (divide by PRU1_GPO_DIV0 + 1). 0h: Div 1.0 1h: Div 1.5 2h: Div 2.0 .. 1Eh: Div 16.0 1Fh: Reserved
14	PRU1_GPO_MODE	R/W	0h	PRU GPO (R30) modes: 0h: Direct output mode 1h: Serial output mode
13	PRU1_GPI_SB	R/W	0h	28-bit shift mode Start Bit event. PRU1_GPI_SB (pru1_r31_status[29]) is set when first capture of a 1 on pru1_r31_status[0]. Read 0: Start Bit event has not occurred. Read 1: Start Bit event occurred. Write 0: No Effect. Write 1: Will clear PRU1_GPI_SB and clear the whole shift register.
12-8	PRU1_GPI_DIV1	R/W	0h	Divisor value (divide by PRU1_GPI_DIV1 + 1). 0h: Div 1.0 1h: Div 1.5 2h: Div 2.0 .. 1Eh: Div 16.0 1Fh: Reserved
7-3	PRU1_GPI_DIV0	R/W	0h	Divisor value (divide by PRU1_GPI_DIV0 + 1). 0h: Div 1.0 1h: Div 1.5 2h: Div 2.0 .. 1Eh: Div 16.0 1Fh: Reserved
2	PRU1_GPI_CLK_MODE	R/W	0h	Parallel 16-bit capture mode clock edge. 0h: Use the positive edge of pru1_r31_status[16] 1h: Use the negative edge of pru1_r31_status[16]
1-0	PRU1_GPI_MODE	R/W	0h	PRU GPI (R31) modes: 0h: Direct input mode 1h: 16-bit parallel capture mode 2h: 28-bit shift mode 3h: MII_RT mode

4.5.1.4 PRU_ICSS_CGR Register (Offset = 10h) [reset = 00024924h]

PRU_ICSS_CGR is shown in Figure 4-8 and described in Table 4-34.

The Clock Gating Register controls the state of Clock Management of the different modules. Software should not clear PRU_ICSS_CLK_EN until PRU_ICSS_CLK_STOP_ACK is 1h.

Table 4-33. PRU_ICSS_CGR Instances

Instance	Physical Address
PRU_ICSS_CFG	4802 6010h

Figure 4-8. PRU_ICSS_CGR Register

31	30	29	28	27	26	25	24
ICSS_STOP_ACK	ICSS_STOP_REQ	RESERVED					
R/W-0h	R-0h	R-0h					
23	22	21	20	19	18	17	16
RESERVED						IEP_CLK_EN	IEP_CLK_STOP_ACK
R-0h						R/W-1h	R-0h
15	14	13	12	11	10	9	8
IEP_CLK_STOP_REQ	ECAP_CLK_EN	ECAP_CLK_STOP_ACK	ECAP_CLK_STOP_REQ	UART_CLK_EN	UART_CLK_STOP_ACK	UART_CLK_STOP_REQ	PRU_ICSS_INTC_CLK_EN
R/W-0h	R/W-1h	R-0h	R/W-0h	R/W-1h	R-0h	R/W-0h	R/W-1h
7	6	5	4	3	2	1	0
PRU_ICSS_INTC_CLK_STOP_ACK	PRU_ICSS_INTC_CLK_STOP_REQ	PRU1_CLK_EN	PRU1_CLK_STOP_ACK	PRU1_CLK_STOP_REQ	PRU0_CLK_EN	PRU0_CLK_STOP_ACK	PRU0_CLK_STOP_REQ
R-0h	R/W-0h	R/W-1h	R-0h	R/W-0h	R/W-1h	R-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-34. PRU_ICSS_CGR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ICSS_STOP_ACK	R/W	0h	Acknowledgement that ICSS clock can be stopped. 0h: Not Ready to Gate Clock 1h: Ready to Gate Clock
30	ICSS_STOP_REQ	R	0h	ICSS request to stop clock. 0h: No Gate Clock Request 1h: Gate Clock Request
29-18	RESERVED	R	0h	Reserved
17	IEP_CLK_EN	R/W	1h	IEP clock enable. 0h: Disable Clock 1h: Enable Clock
16	IEP_CLK_STOP_ACK	R	0h	Acknowledgement that IEP clock can be stopped. 0h: Not Ready to Gate Clock 1h: Ready to Gate Clock
15	IEP_CLK_STOP_REQ	R/W	0h	IEP request to stop clock. 0h: Do not request to stop Clock 1h: Request to stop Clock
14	ECAP_CLK_EN	R/W	1h	ECAP clock enable. 0h: Disable Clock 1h: Enable Clock

Table 4-34. PRU_ICSS_CGR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	ECAP_CLK_STOP_ACK	R	0h	Acknowledgement that ECAP clock can be stopped. 0h: Not Ready to Gate Clock 1h: Ready to Gate Clock
12	ECAP_CLK_STOP_REQ	R/W	0h	ECAP request to stop clock. 0h: Do not request to stop Clock 1h: Request to stop Clock
11	UART_CLK_EN	R/W	1h	UART clock enable. 0h: Disable Clock 1h: Enable Clock
10	UART_CLK_STOP_ACK	R	0h	Acknowledgement that UART clock can be stopped. 0h: Not Ready to Gate Clock 1h: Ready to Gate Clock
9	UART_CLK_STOP_REQ	R/W	0h	UART request to stop clock. 0h: Do not request to stop Clock 1h: Request to stop Clock
8	PRU_ICSS_INTC_CLK_EN	R/W	1h	PRU_ICSS_INTC clock enable. 0h: Disable Clock 1h: Enable Clock
7	PRU_ICSS_INTC_CLK_STOP_ACK	R	0h	Acknowledgement that PRU_ICSS_INTC clock can be stopped. 0h: Not Ready to Gate Clock 1h: Ready to Gate Clock
6	PRU_ICSS_INTC_CLK_STOP_REQ	R/W	0h	PRU_ICSS_INTC request to stop clock. 0h: Do not request to stop Clock 1h: Request to stop Clock
5	PRU1_CLK_EN	R/W	1h	PRU1 clock enable. 0h: Disable Clock 1h: Enable Clock
4	PRU1_CLK_STOP_ACK	R	0h	Acknowledgement that PRU1 clock can be stopped. 0h: Not Ready to Gate Clock 1h: Ready to Gate Clock
3	PRU1_CLK_STOP_REQ	R/W	0h	PRU1 request to stop clock. 0h: Do not request to stop Clock 1h: Request to stop Clock
2	PRU0_CLK_EN	R/W	1h	PRU0 clock enable. 0h: Disable Clock 1h: Enable Clock
1	PRU0_CLK_STOP_ACK	R	0h	Acknowledgement that PRU0 clock can be stopped. 0h: Not Ready to Gate Clock 1h: Ready to Gate Clock
0	PRU0_CLK_STOP_REQ	R/W	0h	PRU0 request to stop clock. 0h: Do not request to stop Clock 1h: Request to stop Clock

4.5.1.5 PRU_ICSS_PMAO Register (Offset = 28h) [reset = 0h]

PRU_ICSS_PMAO is shown in Table 4-35 and described in Table 4-36.

The PRU Master Address Offset Register enables for the PRU Master Port Address to have an offset of minus 0008_0000h. This enables the PRU to access External Host address space starting at 0000_0000h.

Table 4-35. PRU_ICSS_PMAO Instances

Instance	Physical Address
PRU_ICSS_CFG	4802 6028h

Figure 4-9. PRU_ICSS_PMAO Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						PMAO_PRU1	PMAO_PRU0
R-0h						R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-36. PRU_ICSS_PMAO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	PMAO_PRU1	R/W	0h	PRU1 Master Port Address Offset Enable. 0h: Disable address offset. 1h: Enable address offset of -0008_0000h.
0	PMAO_PRU0	R/W	0h	PRU0 Master Port Address Offset Enable. 0h: Disable address offset. 1h: Enable address offset of -0008_0000h.

4.5.1.6 PRU_ICSS_MII_RT Register (Offset = 2Ch) [reset = 1h]

PRU_ICSS_MII_RT is shown in Figure 4-10 and described in Table 4-38.

The MII_RT Event Enable Register enables MII_RT mode events to the PRU-ICSS_INTC.

Table 4-37. PRU_ICSS_MII_RT Instances

Instance	Physical Address
PRU_ICSS_CFG	4802 602Ch

Figure 4-10. PRU_ICSS_MII_RT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							MII_RT_EVENT_EN
R-0h							R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-38. PRU_ICSS_MII_RT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	MII_RT_EVENT_EN	R/W	1h	Enables the MII_RT Events to the PRU-ICSS_INTC. 0h: Disabled (use external events). 1h: Enabled (use MII_RT events).

4.5.1.7 PRU_ICSS_IEPCLK Register (Offset = 30h) [reset = 0h]

PRU_ICSS_IEPCLK is shown in Figure 4-11 and described in Table 4-40.

The IEP Clock Source Register defines the source of the IEP clock.

Table 4-39. PRU_ICSS_IEPCLK Instances

Instance	Physical Address
PRU_ICSS_CFG	4802 6030h

Figure 4-11. PRU_ICSS_IEPCLK Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							OCP_EN
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-40. PRU_ICSS_IEPCLK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	OCP_EN	R/W	0h	IEP clock source. 0h: ICSS_IEP_CLK is the source 1h: ICSS_VCLK_CLK is the source. While this is selected no transactions should be active. It can only be cleared by a hardware reset.

4.5.1.8 PRU_ICSS_SPP Register (Offset = 34h) [reset = 0h]

PRU_ICSS_SPP is shown in Figure 4-12 and described in Table 4-42.

The Scratch Pad Priority and Configuration Register defines the access priority assigned to the PRU cores and configures the scratch pad XFR shift functionality.

Table 4-41. PRU_ICSS_SPP Instances

Instance	Physical Address
PRU_ICSS_CFG	4802 6034h

Figure 4-12. PRU_ICSS_SPP Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						XFR_SHIFT_EN	PRU1_PAD_HP_EN
R-0h						R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-42. PRU_ICSS_SPP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	XFR_SHIFT_EN	R/W	0h	Enables XIN XOUT shift functionality. When enabled, R0[4-0] (internal to PRU) defines the 32-bit offset for XIN and XOUT operations with the scratch pad. 0h: Disabled. 1h: Enabled.
0	PRU1_PAD_HP_EN	R/W	0h	Defines which PRU wins write cycle arbitration to a common scratch pad bank. The PRU which has higher priority will always perform the write cycle with no wait states. The lower PRU will get stalled wait states until higher PRU is not performing write cycles. If the lower priority PRU writes to the same byte has the higher priority PRU, then the lower priority PRU will over write the bytes. 0h: PRU0 has highest priority. 1h: PRU1 has highest priority.

4.5.1.9 PRU_ICSS_PIN_MX Register (Offset = 40h) [reset = 0h]

PRU_ICSS_PIN_MX is shown in Figure 4-13 and described in Table 4-44.

The Pin Mux Select Register defines the state of the PRU-ICSS internal pinmuxing.

Table 4-43. PRU_ICSS_PIN_MX Instances

Instance	Physical Address
PRU_ICSS_CFG	4802 6040h

Figure 4-13. PRU_ICSS_PIN_MX Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED				PWM3_REMAP_EN		PWM0_REMAP_EN	
R-0h				R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-44. PRU_ICSS_PIN_MX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved. Always write 0.
11-10	PWM3_REMAP_EN	R/W	0h	Remaps the eHRPWM3_SYNCI to a PRU-ICSS Host Interrupt. This bit field is only controlled by PRU-ICSS_0. If enabled, PRU-ICSS Host Interrupt 7 controls eHRPWM3_SYNCI. See for more details about eHRPWM3_SYNCI signal. 0h: Disabled 1h: PRU-ICSS_0 Host Interrupt 7 controls eHRPWM3_SYNCI 2h: PRU-ICSS_1 Host Interrupt 7 controls eHRPWM3_SYNCI 3h: Reserved
9-8	PWM0_REMAP_EN	R/W	0h	Remaps the eHRPWM0_SYNCI to a PRU-ICSS Host Interrupt. This bit field is only controlled by PRU-ICSS_0. If enabled, PRU-ICSS Host Interrupt 6 controls eHRPWM0_SYNCI. See for more details about eHRPWM0_SYNCI signal. 0h: Disabled 1h: PRU-ICSS_0 Host Interrupt 6 controls eHRPWM0_SYNCI 2h: PRU-ICSS_1 Host Interrupt 6 controls eHRPWM0_SYNCI 3h: Reserved
7-0	RESERVED	R	0h	Reserved.

4.5.2 PRU_ICSS_ECC_CFG Registers

PRU_ICSS_ECC_CFG Registers lists the memory-mapped registers for the PRU_ICSS_ECC_CFG. All register offset addresses not listed in PRU_ICSS_ECC_CFG Registers should be considered as reserved locations and the register contents should not be modified.

Table 4-45. PRU_ICSS_ECC_CFG Instances

Module Name	Base Address
PRU_ICSS_ECC_CFG	5802 7000h

Table 4-46. PRU_ICSS_ECC_CFG Registers

Offset	Acronym	Register Name	PRU_ICSS_ECC_CFG Physical Address
0h	ECC_REVISION	The Revision Register contains the ID and revision information for the ECC Aggregator module. It does not support byte access.	4802 7000h
8h	ECC_VECTOR	ECC RAM ID to select the ECC RAM to control or read status.	4802 7008h
Ch	ECC_MISC_STATUS	Miscellaneous status register.	4802 700Ch
10h	ECC_WRAPPER_REVISION	The Revision Register contains the ID and revision information for the ECC wrapper.	4802 7010h
14h	ECC_CONTROL	The Control Register controls the ECC control bits for the selected ECC RAM.	4802 7014h
18h	ECC_ERROR_CONTROL1	This register contains ECC error control bits for the selected ECC RAM.	4802 7018h
1Ch	ECC_ERROR_CONTROL2	This register contains ECC error control bits for the selected ECC RAM.	4802 701Ch
20h	ECC_ERROR_STATUS1	This register contains ECC status bits for the selected ECC RAM.	4802 7020h
24h	ECC_ERROR_STATUS2	This register contains ECC status bits for the selected ECC RAM.	4802 7024h
3Ch	ECC_EOI	This is the ECC_EOI register for the interrupt to the host.	4802 703Ch
40h to 7Ch	ECC_INT_STATUS to ECC_INT_STATUS_15	These are the raw level interrupt status bits where each bit corresponds to the pending status from an ECC RAM.	4802 7040h to 4802 707Ch
80h to BCh	ECC_INT_ENABLE_0 to ECC_INT_ENABLE_15	These are interrupt enables associated with the interrupt from each of the ECC RAMs.	4802 7080h to 4802 70BCh
C0h to FCh	ECC_INT_CLEAR_0 to ECC_INT_CLEAR_15	These are interrupt enable clear bits associated with the interrupt from each of the ECC RAMs.	4802 70C0h to 4802 70FCh

4.5.2.1 ECC_REVISION Register (Offset = 0h) [reset = 0h]

ECC_REVISION is shown in Figure 4-14 and described in Table 4-48.

The Revision Register contains the ID and revision information for the module.

Table 4-47. ECC_REVISION Instances

Instance	Physical Address
PRU_ICSS_ECC_CFG	4802 7000h

Figure 4-14. ECC_REVISION Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV																															
R - 4E8A0107h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-48. ECC_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REV	R		TI internal data. Identifies revision of peripheral.

4.5.2.2 ECC_VECTOR Register (Offset = 8h) [reset = 0h]

ECC_VECTOR is shown in Figure 4-15 and described in Table 4-50.

ECC RAM ID to select the ECC RAM to control or read status.

Table 4-49. ECC_VECTOR Instances

Instance	Physical Address
PRU_ICSS_ECC_CFG	4802 7008h

Figure 4-15. ECC_VECTOR Register

31	30	29	28	27	26	25	24
RESERVED							READ_DONE
R-							R-
23	22	21	20	19	18	17	16
READ_ADDRESS							
R/W-							
15	14	13	12	11	10	9	8
TRIGGER_READ	RESERVED				RAM_ID		
R/W-	R-				R/W-		
7	6	5	4	3	2	1	0
RAM_ID							
R/W-							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-50. ECC_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	READ_DONE	R	0h	Status to indicate if read on the serial VBUS is complete.
23-16	READ_ADDRESS	R/W	0h	Read address. Can be any of the registers (10h – 24h).
15	TRIGGER_READ	R/W	0h	Write 1 to trigger a read on the serial VBUS.
14-11	RESERVED	R	0h	Reserved
10-0	RAM_ID	R/W	0h	Value written to select the corresponding ECC RAM for control or status. • 0h: 8KB Data RAM0 • 1h: 8KB Data RAM1 • 2h: 64KB RAM • 3h: 16KB IRAM0 • 4h: 16KB IRAM1 • 5h: Reserved

4.5.2.3 ECC_MISC_STATUS Register (Offset = Ch) [reset = 0h]

ECC_MISC_STATUS is shown in Figure 4-16 and described in Table 4-52.

Miscellaneous status register.

Table 4-51. ECC_MISC_STATUS Instances

Instance	Physical Address
PRU_ICSS_ECC_CFG	4802 700Ch

Figure 4-16. ECC_MISC_STATUS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					NUM_RAMS										
R-0h																					R-5h										

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-52. ECC_MISC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	NUM_RAMS	R	5h	Indicates the number of RAMs serviced by the ECC aggregator.

4.5.2.4 ECC_WRAPPER_REVISION Register (Offset = 10h) [reset = 0h]

ECC_WRAPPER_REVISION is shown in Figure 4-17 and described in Table 4-54.

The Revision Register contains the ID and revision information for the ECC wrapper.

Table 4-53. ECC_WRAPPER_REVISION Instances

Instance	Physical Address
PRU_ICSS_ECC_CFG	4802 7010h

Figure 4-17. ECC_WRAPPER_REVISION Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV																															
R -																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-54. ECC_WRAPPER_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REV	R		TI internal data. Identifies revision of peripheral.

4.5.2.5 ECC_CONTROL Register (Offset = 14h) [reset = 0h]

ECC_CONTROL is shown in Figure 4-18 and described in Table 4-56.

The Global Control Register controls the ECC control bits for the selected ECC RAM.

Table 4-55. ECC_CONTROL Instances

Instance	Physical Address
PRU_ICSS_ECC_CFG	4802 7014h

Figure 4-18. ECC_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R-							
23	22	21	20	19	18	17	16
RESERVED							
R-							
15	14	13	12	11	10	9	8
RESERVED							
R-							
7	6	5	4	3	2	1	0
RESERVED	ERROR_ONCE	FORCE_N_ROW	FORCE_DED	FORCE_SEC	ENABLE_RMW	ECC_CHECK	ECC_ENABLE
R-	R/W-	R/W-	R/W-	R/W-	R/W-	R/W-	R/W-

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-56. ECC_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	ERROR_ONCE	R/W	0h	If this bit is set, the FORCE_SEC/ FORCE_DED will inject an error to the specified row only once. The FORCE_SEC bit will be cleared once a writeback happens. If writeback is not enabled, this error will be cleared the cycle following the read when the data is corrected. For double-bit errors, the FORCE_DED bit will be cleared the cycle following the double-bit error. Any subsequent reads will not force an error.
5	FORCE_N_ROW	R/W	0h	Force single/double-bit error on the next RAM read.
4	FORCE_DED	R/W	0h	Force double-bit error. Cleared the cycle following the error if ERROR_ONCE is asserted.
3	FORCE_SEC	R/W	0h	Force single-bit error. Cleared on a writeback or the cycle following the error if ERROR_ONCE is asserted.
2	ENABLE_RMW	R/W	1h	Enable read-modify-write on partial word writes.
1	ECC_CHECK	R/W	1h	Enable ECC check. ECC is completely bypassed if both ECC_ENABLE and ECC_CHECK are 0.
0	ECC_ENABLE	R/W	1h	Enable ECC generation.

4.5.2.6 ECC_ERROR_CONTROL1 Register (Offset = 18h) [reset = 0h]

ECC_ERROR_CONTROL1 is shown in Figure 4-19 and described in Table 4-58.

This register contains ECC error control bits for the selected ECC RAM.

Table 4-57. ECC_ERROR_CONTROL1 Instances

Instance	Physical Address
PRU_ICSS_ECC_CFG	4802 7018h

Figure 4-19. ECC_ERROR_CONTROL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_BIT1																ECC_ROW															
R/W-																R/W-															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-58. ECC_ERROR_CONTROL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ECC_BIT1	R/W	0h	Column/ Data bit that needs to be flipped when FORCE_SEC or FORCE_DED is set.
15-0	ECC_ROW	R/W	0h	Row address where FORCE_SEC or FORCE_DED needs to be applied. This is ignored if FORCE_N_ROW is set.

4.5.2.7 ECC_ERROR_CONTROL2 Register (Offset = 1Ch) [reset = 0h]

ECC_ERROR_CONTROL2 is shown in Figure 4-20 and described in Table 4-60.

This register contains ECC error control bits for the selected ECC RAM.

Table 4-59. ECC_ERROR_CONTROL2 Instances

Instance	Physical Address
PRU_ICSS_ECC_CFG	4802 701Ch

Figure 4-20. ECC_ERROR_CONTROL2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ECC_BIT2															
R-																R/W-															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-60. ECC_ERROR_CONTROL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	ECC_BIT2	R/W	0h	Data bit that needs to be flipped when FORCE_DED is set

4.5.2.8 ECC_ERROR_STATUS1 Register (Offset = 20h) [reset = 0h]

ECC_ERROR_STATUS1 is shown in Figure 4-21 and described in Table 4-62.

This register contains ECC status bits for the selected ECC RAM.

Table 4-61. ECC_ERROR_STATUS1 Instances

Instance	Physical Address
PRU_ICSS_ECC_CFG	4802 7020h

Figure 4-21. ECC_ERROR_STATUS1 Register

31	30	29	28	27	26	25	24
ECC_ROW							
R-							
23	22	21	20	19	18	17	16
ECC_ROW							
R-							
15	14	13	12	11	10	9	8
RESERVED					CLR_ECC_OTHER	CLR_ECC_DED	CLR_ECC_SEC
R-					R/W1C	R/W1C	R/W1C
7	6	5	4	3	2	1	0
RESERVED					ECC_OTHER	ECC_DED	ECC_SEC
R-					R/W1S	R/W1S	R/W1S

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-62. ECC_ERROR_STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ECC_ROW	R	0h	Indicates the row/address where the single or double-bit error occurred.
15-11	RESERVED	R	0h	Reserved
10	CLR_ECC_OTHER	R/W1C	0h	1 indicates a successive single-bit error. Writing a 1 clears the status bit.
9	CLR_ECC_DED	R/W1C	0h	1 indicates a pending double-bit error. Writing a 1 clears the status bit.
8	CLR_ECC_SEC	R/W1C	0h	1 indicates a pending single-bit error. Writing a 1 clears the status bit.
7-3	RESERVED	R	0h	Reserved
2	ECC_OTHER	R/W1S	0h	1 indicates that successive single-bit errors have occurred while a writeback is still pending. Software can also write a 1 to set the pending status and write a ‘1’ to the corresponding clear bit to clear the status.
1	ECC_DED	R/W1S	0h	1 indicates pending double-bit error. Since the double-bit error from the ECC logic is a pulsed interrupt, this is also a status set register. The software can also write a ‘1’ to set the pending status and write a ‘1’ to the corresponding clear bit to clear the status.
0	ECC_SEC	R/W1S	0h	1 indicates pending single-bit error status. Since the single-bit error from the ECC logic is a pulsed interrupt, this is also a status set register. The software can also write a ‘1’ to set the pending status and write a ‘1’ to the corresponding clear bit to clear the status.

4.5.2.9 ECC_ERROR_STATUS2 Register (Offset = 24h) [reset = 0h]

ECC_ERROR_STATUS2 is shown in Figure 4-22 and described in Table 4-64.

This register contains ECC status bits for the selected ECC RAM.

Table 4-63. ECC_ERROR_STATUS2 Instances

Instance	Physical Address
PRU_ICSS_ECC_CFG	4802 7024h

Figure 4-22. ECC_ERROR_STATUS2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ECC_BIT1															
R-																R-															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-64. ECC_ERROR_STATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	ECC_BIT1	R	0h	Indicates the bit position in the RAM data that is in error. For eg: a value of 1 indicates that bit 1 in the data is in error. This is valid only for single bit errors (sec).

4.5.2.10 ECC_EOI Register (Offset = 3Ch) [reset = 0h]

ECC_EOI is shown in Figure 4-23 and described in Table 4-66.

This is the ECC_EOI register for the interrupt to the host.

Table 4-65. ECC_EOI Instances

Instance	Physical Address
PRU_ICSS_ECC_CFG	4802 703Ch

Figure 4-23. ECC_EOI Register

31	30	29	28	27	26	25	24
RESERVED							
R-							
23	22	21	20	19	18	17	16
RESERVED							
R-							
15	14	13	12	11	10	9	8
RESERVED							
R-							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R-							R/W1S

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-66. ECC_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EOI_WR	R/W1S	0h	Write to this register indicates that software has acknowledged the pending interrupt and the next interrupt can be sent to the host.

4.5.2.11 ECC_INT_STATUS_0 to ECC_INT_STATUS_15 Register (Offset = 40h to 7Ch) [reset = 0h]

ECC_INT_STATUS_0 to ECC_INT_STATUS_15 is shown in Figure 4-24 and described in Table 4-68.

These are the raw level interrupt status bits where each bit corresponds to the pending status from an ECC RAM. The bit associations with the ECC RAMs are assigned by the ECC aggregator module. There is 1 register for upto 32 ECC RAMs. The addresses increment for every additional 32-bit register required to hold the interrupt status for all the ECC RAMs (0 to N-1).

Table 4-67. ECC_INT_STATUS_0 to ECC_INT_STATUS_15 Instances

Instance	Physical Address
PRU_ICSS_ECC_CFG	4802 7040h to 4802 707Ch

Figure 4-24. ECC_INT_STATUS_0 to ECC_INT_STATUS_15 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											SRC_INTR			
R-																											R-			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-68. ECC_INT_STATUS_0 to ECC_INT_STATUS_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	SRC_INTR	R	0h	Level interrupt status from each ECC RAM. • 0h: Not pending status. • 1h: Pending status.

4.5.2.12 ECC_INT_ENABLE_0 to ECC_INT_ENABLE_15 Register (Offset = 80h to BCh) [reset = 0h]

ECC_INT_ENABLE_0 to ECC_INT_ENABLE_15 is shown in Figure 4-25 and described in Table 4-70.

These are interrupt enables associated with the interrupt from each of the ECC RAMs. Writing a 1 to a bit position in the register enables the interrupt from the associated ECC RAM. There is 1 register for upto 32 ECC RAMs. The addresses increment for every additional 32-bit register required for all ECC RAMs (0 to N-1).

Table 4-69. ECC_INT_ENABLE_0 to ECC_INT_ENABLE_15 Instances

Instance	Physical Address
PRU_ICSS_ECC_CFG	4802 7080h to 4802 70BCh

Figure 4-25. ECC_INT_ENABLE_0 to ECC_INT_ENABLE_15 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														ENABLE	
R-																														R/W1S	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-70. ECC_INT_ENABLE_0 to ECC_INT_ENABLE_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	ENABLE	R/W1S	0h	Write 1 to enable interrupt from the associated ECC RAM.

4.5.2.13 ECC_INT_CLEAR_0 to ECC_INT_CLEAR_15 Register (Offset = C0h to FCh) [reset = 0h]

ECC_INT_CLEAR_0 to ECC_INT_CLEAR_15 is shown in Figure 4-26 and described in Table 4-72.

These are interrupt enable clear bits associated with the interrupt from each of the ECC RAMs. Writing a 1 to a bit position in the register disables the interrupt from the associated ECC RAM. There is 1 register for upto 32 ECC RAMs. The addresses increment for every additional 32-bit register required for all the ECC RAMs (0 to N-1).

Table 4-71. ECC_INT_CLEAR_0 to ECC_INT_CLEAR_15 Instances

Instance	Physical Address
PRU_ICSS_ECC_CFG	4802 70C0h to 4802 70FCh

Figure 4-26. ECC_INT_CLEAR_0 to ECC_INT_CLEAR_15 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														ENABLE_CLEAR	
R-																														R/W1C	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 4-72. ECC_INT_CLEAR_0 to ECC_INT_CLEAR_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	ENABLE_CLEAR	R/W1C	0h	Write 1 to disable interrupt from the associated ECC RAM.

4.5.3 PRU_ICSS_PRU_CTRL Registers

PRU_ICSS_PRU_CTRL lists the memory-mapped registers for the PRU-ICSS PRU0 and PRU1 cores. All register offset addresses not listed in PRU_ICSS_PRU_CTRL should be considered as reserved locations and the register contents should not be modified.

Table 4-73. PRU-ICSS_PRU_CTRL Instances

Instance	Base Address
PRU_ICSS_PRU0_CTRL	4802 2000h
PRU_ICSS_PRU1_CTRL	4802 4000h

Table 4-74. PRU_ICSS_PRU_CTRL Registers

Offset	Acronym	Register Name	PRU_ICSS_PRU0_CTRL Physical Address	PRU_ICSS_PRU1_CTRL Physical Address
0h	PRU_CONTROL	Control register	4802 2000h	4802 4000h
4h	PRU_STATUS	Status register	4802 2004h	4802 4004h
8h	PRU_WAKEUP_EN	Wakeup enable register	4802 2008h	4802 4008h
Ch	PRU_CYCLE	Cycle count	4802 200Ch	4802 400Ch
10h	PRU_STALL	Stall count	4802 2010h	4802 4010h
20h	PRU_CTBIR0	Constant Table Block Index Register 0	4802 2020h	4802 4020h
24h	PRU_CTBIR1	Constant Table Block Index Register 1	4802 2024h	4802 4024h
28h	PRU_CTPPR0	Constant Table Programmable Pointer Register 0	4802 2028h	4802 4028h
2Ch	PRU_CTPPR1	Constant Table Programmable Pointer Register 1	4802 202Ch	4802 402Ch

4.5.3.1 PRU_CONTROL Register (Offset = 0h) [reset = 1h]

PRU_CONTROL is shown in Figure 4-27 and described in Table 4-76.

CONTROL REGISTER

Table 4-75. PRU_CONTROL Instances

Instance	Physical Address
PRU_ICSS_PRU0_CTRL	4802 2000h
PRU_ICSS_PRU1_CTRL	4802 4000h

Figure 4-27. PRU_CONTROL Register

31	30	29	28	27	26	25	24
PCOUNTER_RST_VAL							
R/W-0h							
23	22	21	20	19	18	17	16
PCOUNTER_RST_VAL							
R/W-0h							
15	14	13	12	11	10	9	8
RUNSTATE	BIG_ENDIAN	RESERVED					SINGLE_STEP
R-0h	R-0h	R-0h					R/W-0h
7	6	5	4	3	2	1	0
RESERVED				COUNTER_ENABLE	SLEEPING	ENABLE	SOFT_RST_N
R-0h				R/W-0h	R/W-0h	R/W-0h	R-1h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-76. PRU_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PCOUNTER_RST_VAL	R/W	0h	Program Counter Reset Value: This field controls the address where the PRU will start executing code from after it is taken out of reset.
15	RUNSTATE	R	0h	Run State: This bit indicates whether the PRU is currently executing an instruction or is halted. 0 = PRU is halted and host has access to the instruction RAM and debug registers regions. 1 = PRU is currently running and the host is locked out of the instruction RAM and debug registers regions. This bit is used by an external debug agent to know when the PRU has actually halted when waiting for a HALT instruction to execute, a single step to finish, or any other time when the pru_enable has been cleared.
14	BIG_ENDIAN	R	0h	
13-9	RESERVED	R	0h	Reserved
8	SINGLE_STEP	R/W	0h	Single Step Enable: This bit controls whether or not the PRU will only execute a single instruction when enabled. 0 = PRU will free run when enabled. 1 = PRU will execute a single instruction and then the pru_enable bit will be cleared. Note that this bit does not actually enable the PRU, it only sets the policy for how much code will be run after the PRU is enabled. The pru_enable bit must be explicitly asserted. It is legal to initialize both the single_step and pru_enable bits simultaneously. (Two independent writes are not required to cause the stated functionality.)
7-4	RESERVED	R	0h	Reserved

Table 4-76. PRU_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	COUNTER_ENABLE	R/W	0h	PRU Cycle Counter Enable: Enables PRU cycle counters. 0 = Counters not enabled 1 = Counters enabled
2	SLEEPING	R/W	0h	PRU Sleep Indicator: This bit indicates whether or not the PRU is currently asleep. 0 = PRU is not asleep 1 = PRU is asleep If this bit is written to a 0, the PRU will be forced to power up from sleep mode.
1	ENABLE	R/W	0h	Processor Enable: This bit controls whether or not the PRU is allowed to fetch new instructions. 0 = PRU is disabled. 1 = PRU is enabled. If this bit is de-asserted while the PRU is currently running and has completed the initial cycle of a multi-cycle instruction (LBxO,SBxO,SCAN, etc.), the current instruction will be allowed to complete before the PRU pauses execution. Otherwise, the PRU will halt immediately. Because of the unpredictability timing sensitivity of the instruction execution loop, this bit is not a reliable indication of whether or not the PRU is currently running. The pru_state bit should be consulted for an absolute indication of the run state of the core. When the PRU is halted, its internal state remains coherent therefore this bit can be reasserted without issuing a software reset and the PRU will resume processing exactly where it left off in the instruction stream.
0	SOFT_RST_N	R/W	1h	Soft Reset: When this bit is cleared, the PRU will be reset. This bit is set back to 1 on the next cycle after it has been cleared.

4.5.3.2 PRU_STATUS Register (Offset = 4h) [reset = 0h]

PRU_STATUS is shown in Figure 4-28 and described in Table 4-78.

STATUS REGISTER

Table 4-77. PRU_STATUS Instances

Instance	Physical Address
PRU_ICSS_PRU0_CTRL	4802 2004h
PRU_ICSS_PRU1_CTRL	4802 4004h

Figure 4-28. PRU_STATUS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PCOUNTER															
R-0h																R-0h															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-78. PRU_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	PCOUNTER	R	0h	Program Counter: This field is a registered (1 cycle delayed) reflection of the PRU program counter. Note that the PC is an instruction address where each instruction is a 32 bit word. This is not a byte address and to compute the byte address just multiply the PC by 4 (PC of 2 = byte address of 8h, or PC of 8 = byte address of 20h).

4.5.3.3 PRU_WAKEUP_EN Register (Offset = 8h) [reset = 0h]

PRU_WAKEUP_EN is shown in Figure 4-29 and described in Table 4-80.

WAKEUP ENABLE REGISTER

Table 4-79. PRU_WAKEUP_EN Instances

Instance	Physical Address
PRU_ICSS_PRU0_CTRL	4802 2008h
PRU_ICSS_PRU1_CTRL	4802 4008h

Figure 4-29. PRU_WAKEUP_EN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BITWISE_ENABLES																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-80. PRU_WAKEUP_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BITWISE_ENABLES	R/W	0h	Wakeup Enables: This field is ANDed with the incoming R31 status inputs (whose bit positions were specified in the stmap parameter) to produce a vector which is unary ORed to produce the status_wakeup source for the core. Setting any bit in this vector will allow the corresponding status input to wake up the core when it is asserted high. The PRU should set this enable vector prior to executing a SLP (sleep) instruction to ensure that the desired sources can wake up the core.

4.5.3.4 PRU_CYCLE Register (Offset = Ch) [reset = 0h]

PRU_CYCLE is shown in Figure 4-30 and described in Table 4-82.

CYCLE COUNT. This register counts the number of cycles for which the PRU has been enabled.

Table 4-81. PRU_CYCLE Instances

Instance	Physical Address
PRU_ICSS_PRU0_CTRL	4802 200Ch
PRU_ICSS_PRU1_CTRL	4802 400Ch

Figure 4-30. PRU_CYCLE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CYCLECOUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-82. PRU_CYCLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CYCLECOUNT	R/W	0h	This value is incremented by 1 for every cycle during which the PRU is enabled and the counter is enabled (both bits ENABLE and COUNTENABLE set in the PRU control register). Counting halts while the PRU is disabled or counter is disabled, and resumes when re-eneabled. Counter clears the COUNTENABLE bit in the PRU control register when the count reaches FFFFFFFFh. (Count does does not wrap). The register can be read at any time. The register can be cleared when the counter or PRU is disabled. Clearing this register also clears the PRU Stall Count Register.

4.5.3.5 PRU_STALL Register (Offset = 10h) [reset = 0h]

PRU_STALL is shown in Figure 4-31 and described in Table 4-84.

STALL COUNT. This register counts the number of cycles for which the PRU has been enabled, but unable to fetch a new instruction. It is linked to the Cycle Count Register (0Ch) such that this register reflects the stall cycles measured over the same cycles as counted by the cycle count register. Thus the value of this register is always less than or equal to cycle count.

Table 4-83. PRU_STALL Instances

Instance	Physical Address
PRU_ICSS_PRU0_CTRL	4802 2010h
PRU_ICSS_PRU1_CTRL	4802 4010h

Figure 4-31. PRU_STALL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STALLCOUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-84. PRU_STALL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	STALLCOUNT	R/W	0h	This value is incremented by 1 for every cycle during which the PRU is enabled and the counter is enabled (both bits ENABLE and COUNTENABLE set in the PRU control register), and the PRU was unable to fetch a new instruction for any reason.

4.5.3.6 PRU_CTBIR0 Register (Offset = 20h) [reset = 0h]

PRU_CTBIR0 is shown in Figure 4-32 and described in Table 4-86.

CONSTANT TABLE BLOCK INDEX REGISTER 0. This register is used to set the block indices which are used to modify entries 24 and 25 in the PRU Constant Table. This register can be written by the PRU whenever it needs to change to a new base pointer for a block in the State Scratchpad RAM. This function is useful since the PRU is often processing multiple processing threads which require it to change contexts. The PRU can use this register to avoid requiring excessive amounts of code for repetitive context switching.

Table 4-85. PRU_CTBIR0 Instances

Instance	Physical Address
PRU_ICSS_PRU0_CTRL	4802 2020h
PRU_ICSS_PRU1_CTRL	4802 4020h

Figure 4-32. PRU_CTBIR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								C25_BLK_INDEX							
R-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								C24_BLK_INDEX							
R-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-86. PRU_CTBIR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	C25_BLK_INDEX	R/W	0h	PRU Constant Entry 25 Block Index: This field sets the value that will appear in bits 11:8 of entry 25 in the PRU Constant Table.
15-8	RESERVED	R	0h	Reserved
7-0	C24_BLK_INDEX	R/W	0h	PRU Constant Entry 24 Block Index: This field sets the value that will appear in bits 11:8 of entry 24 in the PRU Constant Table.

4.5.3.7 PRU_CTBIR1 Register (Offset = 24h) [reset = 0h]

PRU_CTBIR1 is shown in Figure 4-33 and described in Table 4-88.

CONSTANT TABLE BLOCK INDEX REGISTER 1. This register is used to set the block indices which are used to modify entries 26 and 27 in the PRU Constant Table. This register can be written by the PRU whenever it needs to change to a new base pointer for a block in the State Scratchpad RAM. This function is useful since the PRU is often processing multiple processing threads which require it to change contexts. The PRU can use this register to avoid requiring excessive amounts of code for repetitive context switching.

Table 4-87. PRU_CTBIR1 Instances

Instance	Physical Address
PRU_ICSS_PRU0_CTRL	4802 2024h
PRU_ICSS_PRU1_CTRL	4802 4024h

Figure 4-33. PRU_CTBIR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								C27_BLK_INDEX							
R-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								C26_BLK_INDEX							
R-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-88. PRU_CTBIR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	C27_BLK_INDEX	R/W	0h	PRU Constant Entry 27 Block Index: This field sets the value that will appear in bits 11:8 of entry 27 in the PRU Constant Table.
15-8	RESERVED	R	0h	Reserved
7-0	C26_BLK_INDEX	R/W	0h	PRU Constant Entry 26 Block Index: This field sets the value that will appear in bits 11:8 of entry 26 in the PRU Constant Table.

4.5.3.8 PRU_CTPPR0 Register (Offset = 28h) [reset = 0h]

PRU_CTPPR0 is shown in Figure 4-34 and described in Table 4-90.

CONSTANT TABLE PROGRAMMABLE POINTER REGISTER 0. This register allows the PRU to set up the 256-byte page index for entries 28 and 29 in the PRU Constant Table which serve as general purpose pointers which can be configured to point to any locations inside the session router address map. This register is useful when the PRU needs to frequently access certain structures inside the session router address space whose locations are not hard coded such as tables in scratchpad memory.

Table 4-89. PRU_CTPPR0 Instances

Instance	Physical Address
PRU_ICSS_PRU0_CTRL	4802 2028h
PRU_ICSS_PRU1_CTRL	4802 4028h

Figure 4-34. PRU_CTPPR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C29_POINTER																C28_POINTER															
R/W-0h																R/W-0h															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-90. PRU_CTPPR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	C29_POINTER	R/W	0h	PRU Constant Entry 29 Pointer: This field sets the value that will appear in bits 23:8 of entry 29 in the PRU Constant Table.
15-0	C28_POINTER	R/W	0h	PRU Constant Entry 28 Pointer: This field sets the value that will appear in bits 23:8 of entry 28 in the PRU Constant Table.

4.5.3.9 PRU_CTPPR1 Register (Offset = 2Ch) [reset = 0h]

PRU_CTPPR1 is shown in Figure 4-35 and described in Table 4-92.

CONSTANT TABLE PROGRAMMABLE POINTER REGISTER 1. This register functions the same as the PRU Constant Table Programmable Pointer Register 0 but allows the PRU to control entries 30 and 31 in the PRU Constant Table.

Table 4-91. PRU_CTPPR1 Instances

Instance	Physical Address
PRU_ICSS_PRU0_CTRL	4802 202Ch
PRU_ICSS_PRU1_CTRL	4802 402Ch

Figure 4-35. PRU_CTPPR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C31_POINTER																C30_POINTER															
R/W-0h																R/W-0h															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-92. PRU_CTPPR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	C31_POINTER	R/W	0h	PRU Constant Entry 31 Pointer: This field sets the value that will appear in bits 23:8 of entry 31 in the PRU Constant Table.
15-0	C30_POINTER	R/W	0h	PRU Constant Entry 30 Pointer: This field sets the value that will appear in bits 23:8 of entry 30 in the PRU Constant Table.

4.5.4 PRU_ICSS_PRU_DEBUG Registers

PRU_ICSS_PRU_DEBUG Registers lists the memory-mapped registers for the PRU_ICSS_PRU_DEBUG. All register offset addresses not listed in PRU_ICSS_PRU_DEBUG Registers should be considered as reserved locations and the register contents should not be modified.

Table 4-93. PRU-ICSS_PRU_DEBUG Instances

Instance	Base Address
PRU_ICSS_PRU_DEBUG_0	4802 2400h
PRU_ICSS_PRU_DEBUG_1	4802 4400h

Table 4-94. PRU_ICSS_PRU_DEBUG Registers

Offset	Acronym	Register Name	PRU_ICSS_PRU_DEBUG_0 Physical Address	PRU_ICSS_PRU_DEBUG_1 Physical Address
0h	PRU_ICSS_DBG_GPREG0	DEBUG PRU GENERAL PURPOSE REGISTER 0	4802 2400h	4802 4400h
4h	PRU_ICSS_DBG_GPREG1	DEBUG PRU GENERAL PURPOSE REGISTER 1	4802 2404h	4802 4404h
8h	PRU_ICSS_DBG_GPREG2	DEBUG PRU GENERAL PURPOSE REGISTER 2	4802 2408h	4802 4408h
Ch	PRU_ICSS_DBG_GPREG3	DEBUG PRU GENERAL PURPOSE REGISTER 3	4802 240Ch	4802 440Ch
10h	PRU_ICSS_DBG_GPREG4	DEBUG PRU GENERAL PURPOSE REGISTER 4	4802 2410h	4802 4410h
14h	PRU_ICSS_DBG_GPREG5	DEBUG PRU GENERAL PURPOSE REGISTER 5	4802 2414h	4802 4414h
18h	PRU_ICSS_DBG_GPREG6	DEBUG PRU GENERAL PURPOSE REGISTER 6	4802 2418h	4802 4418h
1Ch	PRU_ICSS_DBG_GPREG7	DEBUG PRU GENERAL PURPOSE REGISTER 7	4802 241Ch	4802 441Ch
20h	PRU_ICSS_DBG_GPREG8	DEBUG PRU GENERAL PURPOSE REGISTER 8	4802 2420h	4802 4420h
24h	PRU_ICSS_DBG_GPREG9	DEBUG PRU GENERAL PURPOSE REGISTER 9	4802 2424h	4802 4424h
28h	PRU_ICSS_DBG_GPREG10	DEBUG PRU GENERAL PURPOSE REGISTER 10	4802 2428h	4802 4428h
2Ch	PRU_ICSS_DBG_GPREG11	DEBUG PRU GENERAL PURPOSE REGISTER 11	4802 242Ch	4802 442Ch
30h	PRU_ICSS_DBG_GPREG12	DEBUG PRU GENERAL PURPOSE REGISTER 12	4802 2430h	4802 4430h
34h	PRU_ICSS_DBG_GPREG13	DEBUG PRU GENERAL PURPOSE REGISTER 13	4802 2434h	4802 4434h
38h	PRU_ICSS_DBG_GPREG14	DEBUG PRU GENERAL PURPOSE REGISTER 14	4802 2438h	4802 4438h
3Ch	PRU_ICSS_DBG_GPREG15	DEBUG PRU GENERAL PURPOSE REGISTER 15	4802 243Ch	4802 443Ch
40h	PRU_ICSS_DBG_GPREG16	DEBUG PRU GENERAL PURPOSE REGISTER 16	4802 2440h	4802 4440h
44h	PRU_ICSS_DBG_GPREG17	DEBUG PRU GENERAL PURPOSE REGISTER 17	4802 2444h	4802 4444h
48h	PRU_ICSS_DBG_GPREG18	DEBUG PRU GENERAL PURPOSE REGISTER 18	4802 2448h	4802 4448h
4Ch	PRU_ICSS_DBG_GPREG19	DEBUG PRU GENERAL PURPOSE REGISTER 19	4802 244Ch	4802 444Ch
50h	PRU_ICSS_DBG_GPREG20	DEBUG PRU GENERAL PURPOSE REGISTER 20	4802 2450h	4802 4450h

Table 4-94. PRU_ICSS_PRU_DEBUG Registers (continued)

Offset	Acronym	Register Name	PRU_ICSS_PRU_DEBUG_0 Physical Address	PRU_ICSS_PRU_DEBUG_1 Physical Address
54h	PRU_ICSS_DBG_GPREG21	DEBUG PRU GENERAL PURPOSE REGISTER 21	4802 2454h	4802 4454h
58h	PRU_ICSS_DBG_GPREG22	DEBUG PRU GENERAL PURPOSE REGISTER 22	4802 2458h	4802 4458h
5Ch	PRU_ICSS_DBG_GPREG23	DEBUG PRU GENERAL PURPOSE REGISTER 23	4802 245Ch	4802 445Ch
60h	PRU_ICSS_DBG_GPREG24	DEBUG PRU GENERAL PURPOSE REGISTER 24	4802 2460h	4802 4460h
64h	PRU_ICSS_DBG_GPREG25	DEBUG PRU GENERAL PURPOSE REGISTER 25	4802 2464h	4802 4464h
68h	PRU_ICSS_DBG_GPREG26	DEBUG PRU GENERAL PURPOSE REGISTER 26	4802 2468h	4802 4468h
6Ch	PRU_ICSS_DBG_GPREG27	DEBUG PRU GENERAL PURPOSE REGISTER 27	4802 246Ch	4802 446Ch
70h	PRU_ICSS_DBG_GPREG28	DEBUG PRU GENERAL PURPOSE REGISTER 28	4802 2470h	4802 4470h
74h	PRU_ICSS_DBG_GPREG29	DEBUG PRU GENERAL PURPOSE REGISTER 29	4802 2474h	4802 4474h
78h	PRU_ICSS_DBG_GPREG30	DEBUG PRU GENERAL PURPOSE REGISTER 30	4802 2478h	4802 4478h
7Ch	PRU_ICSS_DBG_GPREG31	DEBUG PRU GENERAL PURPOSE REGISTER 31	4802 247Ch	4802 447Ch
80h	PRU_ICSS_DBG_CT_REG0	DEBUG PRU CONSTANTS TABLE ENTRY 0	4802 2480h	4802 4480h
84h	PRU_ICSS_DBG_CT_REG1	DEBUG PRU CONSTANTS TABLE ENTRY 1	4802 2484h	4802 4484h
88h	PRU_ICSS_DBG_CT_REG2	DEBUG PRU CONSTANTS TABLE ENTRY 2	4802 2488h	4802 4488h
8Ch	PRU_ICSS_DBG_CT_REG3	DEBUG PRU CONSTANTS TABLE ENTRY 3	4802 248Ch	4802 448Ch
90h	PRU_ICSS_DBG_CT_REG4	DEBUG PRU CONSTANTS TABLE ENTRY 4	4802 2490h	4802 4490h
94h	PRU_ICSS_DBG_CT_REG5	DEBUG PRU CONSTANTS TABLE ENTRY 5	4802 2494h	4802 4494h
98h	PRU_ICSS_DBG_CT_REG6	DEBUG PRU CONSTANTS TABLE ENTRY 6	4802 2498h	4802 4498h
9Ch	PRU_ICSS_DBG_CT_REG7	DEBUG PRU CONSTANTS TABLE ENTRY 7	4802 249Ch	4802 449Ch
A0h	PRU_ICSS_DBG_CT_REG8	DEBUG PRU CONSTANTS TABLE ENTRY 8	4802 24A0h	4802 44A0h
A4h	PRU_ICSS_DBG_CT_REG9	DEBUG PRU CONSTANTS TABLE ENTRY 9	4802 24A4h	4802 44A4h
A8h	PRU_ICSS_DBG_CT_REG10	DEBUG PRU CONSTANTS TABLE ENTRY 10	4802 24A8h	4802 44A8h
ACh	PRU_ICSS_DBG_CT_REG11	DEBUG PRU CONSTANTS TABLE ENTRY 11	4802 24ACh	4802 44ACh
B0h	PRU_ICSS_DBG_CT_REG12	DEBUG PRU CONSTANTS TABLE ENTRY 12	4802 24B0h	4802 44B0h
B4h	PRU_ICSS_DBG_CT_REG13	DEBUG PRU CONSTANTS TABLE ENTRY 13	4802 24B4h	4802 44B4h
B8h	PRU_ICSS_DBG_CT_REG14	DEBUG PRU CONSTANTS TABLE ENTRY 14	4802 24B8h	4802 44B8h
BCh	PRU_ICSS_DBG_CT_REG15	DEBUG PRU CONSTANTS TABLE ENTRY 15	4802 24BCh	4802 44BCh

Table 4-94. PRU_ICSS_PRU_DEBUG Registers (continued)

Offset	Acronym	Register Name	PRU_ICSS_PRU_DEBUG_0 Physical Address	PRU_ICSS_PRU_DEBUG_1 Physical Address
C0h	PRU_ICSS_DBG_CT_REG16	DEBUG PRU CONSTANTS TABLE ENTRY 16	4802 24C0h	4802 44C0h
C4h	PRU_ICSS_DBG_CT_REG17	DEBUG PRU CONSTANTS TABLE ENTRY 17	4802 24C4h	4802 44C4h
C8h	PRU_ICSS_DBG_CT_REG18	DEBUG PRU CONSTANTS TABLE ENTRY 18	4802 24C8h	4802 44C8h
CCh	PRU_ICSS_DBG_CT_REG19	DEBUG PRU CONSTANTS TABLE ENTRY 19	4802 24CCh	4802 44CCh
D0h	PRU_ICSS_DBG_CT_REG20	DEBUG PRU CONSTANTS TABLE ENTRY 20	4802 24D0h	4802 44D0h
D4h	PRU_ICSS_DBG_CT_REG21	DEBUG PRU CONSTANTS TABLE ENTRY 21	4802 24D4h	4802 44D4h
D8h	PRU_ICSS_DBG_CT_REG22	DEBUG PRU CONSTANTS TABLE ENTRY 22	4802 24D8h	4802 44D8h
DCh	PRU_ICSS_DBG_CT_REG23	DEBUG PRU CONSTANTS TABLE ENTRY 23	4802 24DCh	4802 44DCh
E0h	PRU_ICSS_DBG_CT_REG24	DEBUG PRU CONSTANTS TABLE ENTRY 24	4802 24E0h	4802 44E0h
E4h	PRU_ICSS_DBG_CT_REG25	DEBUG PRU CONSTANTS TABLE ENTRY 25	4802 24E4h	4802 44E4h
E8h	PRU_ICSS_DBG_CT_REG26	DEBUG PRU CONSTANTS TABLE ENTRY 26	4802 24E8h	4802 44E8h
ECh	PRU_ICSS_DBG_CT_REG27	DEBUG PRU CONSTANTS TABLE ENTRY 27	4802 24ECh	4802 44ECh
F0h	PRU_ICSS_DBG_CT_REG28	DEBUG PRU CONSTANTS TABLE ENTRY 28	4802 24F0h	4802 44F0h
F4h	PRU_ICSS_DBG_CT_REG29	DEBUG PRU CONSTANTS TABLE ENTRY 29	4802 24F4h	4802 44F4h
F8h	PRU_ICSS_DBG_CT_REG30	DEBUG PRU CONSTANTS TABLE ENTRY 30	4802 24F8h	4802 44F8h
FCh	PRU_ICSS_DBG_CT_REG31	DEBUG PRU CONSTANTS TABLE ENTRY 31	4802 24FCh	4802 44FCh

4.5.4.1 PRU_ICSS_DBG_GPREG0 Register (Offset = 0h) [reset = 0h]

PRU_ICSS_DBG_GPREG0 is shown in Figure 4-36 and described in Table 4-96.

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DEBUG PRU GENERAL PURPOSE REGISTER 0. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-95. PRU_ICSS_DBG_GPREG0 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2400h
PRU_ICSS_PRU_DEBUG_1	4802 4400h

Figure 4-36. PRU_ICSS_DBG_GPREG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG0																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-96. PRU_ICSS_DBG_GPREG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG0	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

4.5.4.2 PRU_ICSS_DBG_GPREG1 Register (Offset = 4h) [reset = 0h]

PRU_ICSS_DBG_GPREG1 is shown in Figure 4-37 and described in Table 4-98.

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DEBUG PRU GENERAL PURPOSE REGISTER 1. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-97. PRU_ICSS_DBG_GPREG1 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2404h
PRU_ICSS_PRU_DEBUG_1	4802 4404h

Figure 4-37. PRU_ICSS_DBG_GPREG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG1																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-98. PRU_ICSS_DBG_GPREG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG1	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

4.5.4.3 PRU_ICSS_DBG_GPREG2 Register (Offset = 8h) [reset = 0h]

PRU_ICSS_DBG_GPREG2 is shown in Figure 4-38 and described in Table 4-100.

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DEBUG PRU GENERAL PURPOSE REGISTER 2. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-99. PRU_ICSS_DBG_GPREG2 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2408h
PRU_ICSS_PRU_DEBUG_1	4802 4408h

Figure 4-38. PRU_ICSS_DBG_GPREG2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG2																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-100. PRU_ICSS_DBG_GPREG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG2	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

4.5.4.4 PRU_ICSS_DBG_GPREG3 Register (Offset = Ch) [reset = 0h]

PRU_ICSS_DBG_GPREG3 is shown in Figure 4-39 and described in Table 4-102.

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DEBUG PRU GENERAL PURPOSE REGISTER 3. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-101. PRU_ICSS_DBG_GPREG3 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 240Ch
PRU_ICSS_PRU_DEBUG_1	4802 440Ch

Figure 4-39. PRU_ICSS_DBG_GPREG3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG3																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-102. PRU_ICSS_DBG_GPREG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG3	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

4.5.4.5 PRU_ICSS_DBG_GPREG4 Register (Offset = 10h) [reset = 0h]

PRU_ICSS_DBG_GPREG4 is shown in Figure 4-40 and described in Table 4-104.

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DEBUG PRU GENERAL PURPOSE REGISTER 4. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-103. PRU_ICSS_DBG_GPREG4 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2410h
PRU_ICSS_PRU_DEBUG_1	4802 4410h

Figure 4-40. PRU_ICSS_DBG_GPREG4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG4																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-104. PRU_ICSS_DBG_GPREG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG4	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

4.5.4.6 PRU_ICSS_DBG_GPREG5 Register (Offset = 14h) [reset = 0h]

PRU_ICSS_DBG_GPREG5 is shown in Figure 4-41 and described in Table 4-106.

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DEBUG PRU GENERAL PURPOSE REGISTER 5. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-105. PRU_ICSS_DBG_GPREG5 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2414h
PRU_ICSS_PRU_DEBUG_1	4802 4414h

Figure 4-41. PRU_ICSS_DBG_GPREG5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG5																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-106. PRU_ICSS_DBG_GPREG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG5	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

4.5.4.7 PRU_ICSS_DBG_GPREG6 Register (Offset = 18h) [reset = 0h]

PRU_ICSS_DBG_GPREG6 is shown in Figure 4-42 and described in Table 4-108.

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DEBUG PRU GENERAL PURPOSE REGISTER 6. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-107. PRU_ICSS_DBG_GPREG6 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2418h
PRU_ICSS_PRU_DEBUG_1	4802 4418h

Figure 4-42. PRU_ICSS_DBG_GPREG6 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG6																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-108. PRU_ICSS_DBG_GPREG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG6	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

4.5.4.8 PRU_ICSS_DBG_GPREG7 Register (Offset = 1Ch) [reset = 0h]

PRU_ICSS_DBG_GPREG7 is shown in Figure 4-43 and described in Table 4-110.

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DEBUG PRU GENERAL PURPOSE REGISTER 7. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-109. PRU_ICSS_DBG_GPREG7 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 241Ch
PRU_ICSS_PRU_DEBUG_1	4802 441Ch

Figure 4-43. PRU_ICSS_DBG_GPREG7 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG7																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-110. PRU_ICSS_DBG_GPREG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG7	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

4.5.4.9 PRU_ICSS_DBG_GPREG8 Register (Offset = 20h) [reset = 0h]

PRU_ICSS_DBG_GPREG8 is shown in Figure 4-44 and described in Table 4-112.

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DEBUG PRU GENERAL PURPOSE REGISTER 8. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-111. PRU_ICSS_DBG_GPREG8 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2420h
PRU_ICSS_PRU_DEBUG_1	4802 4420h

Figure 4-44. PRU_ICSS_DBG_GPREG8 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG8																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-112. PRU_ICSS_DBG_GPREG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG8	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

4.5.4.10 PRU_ICSS_DBG_GPREG9 Register (Offset = 24h) [reset = 0h]

PRU_ICSS_DBG_GPREG9 is shown in Figure 4-45 and described in Table 4-114.

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DEBUG PRU GENERAL PURPOSE REGISTER 9. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-113. PRU_ICSS_DBG_GPREG9 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2424h
PRU_ICSS_PRU_DEBUG_1	4802 4424h

Figure 4-45. PRU_ICSS_DBG_GPREG9 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG9																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-114. PRU_ICSS_DBG_GPREG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG9	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

4.5.4.11 PRU_ICSS_DBG_GPREG10 Register (Offset = 28h) [reset = 0h]

PRU_ICSS_DBG_GPREG10 is shown in Figure 4-46 and described in Table 4-116.

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DEBUG PRU GENERAL PURPOSE REGISTER 10. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-115. PRU_ICSS_DBG_GPREG10 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2428h
PRU_ICSS_PRU_DEBUG_1	4802 4428h

Figure 4-46. PRU_ICSS_DBG_GPREG10 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG10																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 4-116. PRU_ICSS_DBG_GPREG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG10	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

4.5.4.12 PRU_ICSS_DBG_GPREG11 Register (Offset = 2Ch) [reset = 0h]

PRU_ICSS_DBG_GPREG11 is shown in Figure 4-47 and described in Table 4-118.

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DEBUG PRU GENERAL PURPOSE REGISTER 11. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-117. PRU_ICSS_DBG_GPREG11 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 242Ch
PRU_ICSS_PRU_DEBUG_1	4802 442Ch

Figure 4-47. PRU_ICSS_DBG_GPREG11 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG11																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-118. PRU_ICSS_DBG_GPREG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG11	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

4.5.4.13 PRU_ICSS_DBG_GPREG12 Register (Offset = 30h) [reset = 0h]

PRU_ICSS_DBG_GPREG12 is shown in Figure 4-48 and described in Table 4-120.

Return to Summary Table.

DEBUG PRU GENERAL PURPOSE REGISTER 12. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-119. PRU_ICSS_DBG_GPREG12 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2430h
PRU_ICSS_PRU_DEBUG_1	4802 4430h

Figure 4-48. PRU_ICSS_DBG_GPREG12 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG12																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 4-120. PRU_ICSS_DBG_GPREG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG12	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

4.5.4.14 PRU_ICSS_DBG_GPREG13 Register (Offset = 34h) [reset = 0h]

PRU_ICSS_DBG_GPREG13 is shown in Figure 4-49 and described in Table 4-122.

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DEBUG PRU GENERAL PURPOSE REGISTER 13. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-121. PRU_ICSS_DBG_GPREG13 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2434h
PRU_ICSS_PRU_DEBUG_1	4802 4434h

Figure 4-49. PRU_ICSS_DBG_GPREG13 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG13																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-122. PRU_ICSS_DBG_GPREG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG13	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

4.5.4.15 PRU_ICSS_DBG_GPREG14 Register (Offset = 38h) [reset = 0h]

PRU_ICSS_DBG_GPREG14 is shown in Figure 4-50 and described in Table 4-124.

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DEBUG PRU GENERAL PURPOSE REGISTER 14. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-123. PRU_ICSS_DBG_GPREG14 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2438h
PRU_ICSS_PRU_DEBUG_1	4802 4438h

Figure 4-50. PRU_ICSS_DBG_GPREG14 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG14																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 4-124. PRU_ICSS_DBG_GPREG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG14	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

4.5.4.16 PRU_ICSS_DBG_GPREG15 Register (Offset = 3Ch) [reset = 0h]

PRU_ICSS_DBG_GRPREG15 is shown in Figure 4-51 and described in Table 4-126.

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DEBUG PRU GENERAL PURPOSE REGISTER 15. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-125. PRU_ICSS_DBG_GPREG15 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 243Ch
PRU_ICSS_PRU_DEBUG_1	4802 443Ch

Figure 4-51. PRU_ICSS_DBG_GPREG15 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG15																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 4-126. PRU_ICSS_DBG_GPREG15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG15	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

4.5.4.17 PRU_ICSS_DBG_GPREG16 Register (Offset = 40h) [reset = 0h]

PRU_ICSS_DBG_GPREG16 is shown in Figure 4-52 and described in Table 4-128.

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DEBUG PRU GENERAL PURPOSE REGISTER 16. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-127. PRU_ICSS_DBG_GPREG16 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2440h
PRU_ICSS_PRU_DEBUG_1	4802 4440h

Figure 4-52. PRU_ICSS_DBG_GPREG16 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG16																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-128. PRU_ICSS_DBG_GPREG16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG16	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

4.5.4.18 PRU_ICSS_DBG_GPREG17 Register (Offset = 44h) [reset = 0h]

PRU_ICSS_DBG_GPREG17 is shown in Figure 4-53 and described in Table 4-130.

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DEBUG PRU GENERAL PURPOSE REGISTER 17. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-129. PRU_ICSS_DBG_GPREG17 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2444h
PRU_ICSS_PRU_DEBUG_1	4802 4444h

Figure 4-53. PRU_ICSS_DBG_GPREG17 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG17																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-130. PRU_ICSS_DBG_GPREG17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG17	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

4.5.4.19 PRU_ICSS_DBG_GPREG18 Register (Offset = 48h) [reset = 0h]

PRU_ICSS_DBG_GPREG18 is shown in Figure 4-54 and described in Table 4-132.

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DEBUG PRU GENERAL PURPOSE REGISTER 18. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-131. PRU_ICSS_DBG_GPREG18 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2448h
PRU_ICSS_PRU_DEBUG_1	4802 4448h

Figure 4-54. PRU_ICSS_DBG_GPREG18 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG18																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-132. PRU_ICSS_DBG_GPREG18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG18	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

4.5.4.20 PRU_ICSS_DBG_GPREG19 Register (Offset = 4Ch) [reset = 0h]

PRU_ICSS_DBG_GPREG19 is shown in Figure 4-55 and described in Table 4-134.

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DEBUG PRU GENERAL PURPOSE REGISTER 19. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-133. PRU_ICSS_DBG_GPREG19 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 244Ch
PRU_ICSS_PRU_DEBUG_1	4802 444Ch

Figure 4-55. PRU_ICSS_DBG_GPREG19 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG19																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-134. PRU_ICSS_DBG_GPREG19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG19	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

4.5.4.21 PRU_ICSS_DBG_GPREG20 Register (Offset = 50h) [reset = 0h]

PRU_ICSS_DBG_GPREG20 is shown in Figure 4-56 and described in Table 4-136.

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DEBUG PRU GENERAL PURPOSE REGISTER 20. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-135. PRU_ICSS_DBG_GPREG20 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2450h
PRU_ICSS_PRU_DEBUG_1	4802 4450h

Figure 4-56. PRU_ICSS_DBG_GPREG20 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG20																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-136. PRU_ICSS_DBG_GPREG20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG20	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

4.5.4.22 PRU_ICSS_DBG_GPREG21 Register (Offset = 54h) [reset = 0h]

PRU_ICSS_DBG_GPREG21 is shown in Figure 4-57 and described in Table 4-138.

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DEBUG PRU GENERAL PURPOSE REGISTER 21. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-137. PRU_ICSS_DBG_GPREG21 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2454h
PRU_ICSS_PRU_DEBUG_1	4802 4454h

Figure 4-57. PRU_ICSS_DBG_GPREG21 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG21																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-138. PRU_ICSS_DBG_GPREG21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG21	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

4.5.4.23 PRU_ICSS_DBG_GPREG22 Register (Offset = 58h) [reset = 0h]

PRU_ICSS_DBG_GPREG22 is shown in Figure 4-58 and described in Table 4-140.

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DEBUG PRU GENERAL PURPOSE REGISTER 22. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-139. PRU_ICSS_DBG_GPREG22 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2458h
PRU_ICSS_PRU_DEBUG_1	4802 4458h

Figure 4-58. PRU_ICSS_DBG_GPREG22 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG22																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-140. PRU_ICSS_DBG_GPREG22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG22	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

4.5.4.24 PRU_ICSS_DBG_GPREG23 Register (Offset = 5Ch) [reset = 0h]

PRU_ICSS_DBG_GPREG23 is shown in Figure 4-59 and described in Table 4-142.

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DEBUG PRU GENERAL PURPOSE REGISTER 23. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-141. PRU_ICSS_DBG_GPREG23 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 245Ch
PRU_ICSS_PRU_DEBUG_1	4802 445Ch

Figure 4-59. PRU_ICSS_DBG_GPREG23 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG23																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-142. PRU_ICSS_DBG_GPREG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG23	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

4.5.4.25 PRU_ICSS_DBG_GPREG24 Register (Offset = 60h) [reset = 0h]

PRU_ICSS_DBG_GPREG24 is shown in Figure 4-60 and described in Table 4-144.

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DEBUG PRU GENERAL PURPOSE REGISTER 24. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-143. PRU_ICSS_DBG_GPREG24 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2460h
PRU_ICSS_PRU_DEBUG_1	4802 4460h

Figure 4-60. PRU_ICSS_DBG_GPREG24 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG24																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 4-144. PRU_ICSS_DBG_GPREG24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG24	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

4.5.4.26 PRU_ICSS_DBG_GPREG25 Register (Offset = 64h) [reset = 0h]

PRU_ICSS_DBG_GPREG25 is shown in Figure 4-61 and described in Table 4-146.

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DEBUG PRU GENERAL PURPOSE REGISTER 25. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-145. PRU_ICSS_DBG_GPREG25 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2464h
PRU_ICSS_PRU_DEBUG_1	4802 4464h

Figure 4-61. PRU_ICSS_DBG_GPREG25 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG25																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 4-146. PRU_ICSS_DBG_GPREG25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG25	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

4.5.4.27 PRU_ICSS_DBG_GPREG26 Register (Offset = 68h) [reset = 0h]

PRU_ICSS_DBG_GPREG26 is shown in Figure 4-62 and described in Table 4-148.

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DEBUG PRU GENERAL PURPOSE REGISTER 26. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-147. PRU_ICSS_DBG_GPREG26 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2468h
PRU_ICSS_PRU_DEBUG_1	4802 4468h

Figure 4-62. PRU_ICSS_DBG_GPREG26 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG26																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 4-148. PRU_ICSS_DBG_GPREG26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG26	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

4.5.4.28 PRU_ICSS_DBG_GPREG27 Register (Offset = 6Ch) [reset = 0h]

PRU_ICSS_DBG_GPREG27 is shown in Figure 4-63 and described in Table 4-150.

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DEBUG PRU GENERAL PURPOSE REGISTER 27. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-149. PRU_ICSS_DBG_GPREG27 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 246Ch
PRU_ICSS_PRU_DEBUG_1	4802 446Ch

Figure 4-63. PRU_ICSS_DBG_GPREG27 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG27																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-150. PRU_ICSS_DBG_GPREG27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG27	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

4.5.4.29 PRU_ICSS_DBG_GPREG28 Register (Offset = 70h) [reset = 0h]

PRU_ICSS_DBG_GPREG28 is shown in Figure 4-64 and described in Table 4-152.

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DEBUG PRU GENERAL PURPOSE REGISTER 28. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-151. PRU_ICSS_DBG_GPREG28 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2470h
PRU_ICSS_PRU_DEBUG_1	4802 4470h

Figure 4-64. PRU_ICSS_DBG_GPREG28 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG28																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-152. PRU_ICSS_DBG_GPREG28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG28	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

4.5.4.30 PRU_ICSS_DBG_GPREG29 Register (Offset = 74h) [reset = 0h]

PRU_ICSS_DBG_GPREG29 is shown in Figure 4-65 and described in Table 4-154.

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DEBUG PRU GENERAL PURPOSE REGISTER 29. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-153. PRU_ICSS_DBG_GPREG29 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2474h
PRU_ICSS_PRU_DEBUG_1	4802 4474h

Figure 4-65. PRU_ICSS_DBG_GPREG29 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG29																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-154. PRU_ICSS_DBG_GPREG29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG29	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

4.5.4.31 PRU_ICSS_DBG_GPREG30 Register (Offset = 78h) [reset = 0h]

PRU_ICSS_DBG_GPREG30 is shown in Figure 4-66 and described in Table 4-156.

Return to Summary Table.

DEBUG PRU GENERAL PURPOSE REGISTER 30. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-155. PRU_ICSS_DBG_GPREG30 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2478h
PRU_ICSS_PRU_DEBUG_1	4802 4478h

Figure 4-66. PRU_ICSS_DBG_GPREG30 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG30																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-156. PRU_ICSS_DBG_GPREG30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG30	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

4.5.4.32 PRU_ICSS_DBG_GPREG31 Register (Offset = 7Ch) [reset = 0h]

PRU_ICSS_DBG_GPREG31 is shown in Figure 4-67 and described in Table 4-158.

Return to Summary Table.

DEBUG PRU GENERAL PURPOSE REGISTER 31. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-157. PRU_ICSS_DBG_GPREG31 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 247Ch
PRU_ICSS_PRU_DEBUG_1	4802 447Ch

Figure 4-67. PRU_ICSS_DBG_GPREG31 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPREG31																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-158. PRU_ICSS_DBG_GPREG31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GPREG31	R/W	0h	

4.5.4.33 PRU_ICSS_DBG_CT_REG0 Register (Offset = 80h) [reset = 00020000h]

PRU_ICSS_DBG_CT_REG0 is shown in Figure 4-68 and described in Table 4-160.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 0. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-159. PRU_ICSS_DBG_CT_REG0 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2480h
PRU_ICSS_PRU_DEBUG_1	4802 4480h

Figure 4-68. PRU_ICSS_DBG_CT_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG0																															
R-00020000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-160. PRU_ICSS_DBG_CT_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG0	R	00020000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

4.5.4.34 PRU_ICSS_DBG_CT_REG1 Register (Offset = 84h) [reset = 48040000h]

PRU_ICSS_DBG_CT_REG1 is shown in Figure 4-69 and described in Table 4-162.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 1. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-161. PRU_ICSS_DBG_CT_REG1 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2484h
PRU_ICSS_PRU_DEBUG_1	4802 4484h

Figure 4-69. PRU_ICSS_DBG_CT_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG1																															
R-48040000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-162. PRU_ICSS_DBG_CT_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG1	R	48040000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

4.5.4.35 PRU_ICSS_DBG_CT_REG2 Register (Offset = 88h) [reset = 4802A000h]

PRU_ICSS_DBG_CT_REG2 is shown in Figure 4-70 and described in Table 4-164.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 2. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-163. PRU_ICSS_DBG_CT_REG2 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2488h
PRU_ICSS_PRU_DEBUG_1	4802 4488h

Figure 4-70. PRU_ICSS_DBG_CT_REG2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG2																															
R-4802A000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-164. PRU_ICSS_DBG_CT_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG2	R	4802A000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

4.5.4.36 PRU_ICSS_DBG_CT_REG3 Register (Offset = 8Ch) [reset = 00030000h]

PRU_ICSS_DBG_CT_REG3 is shown in Figure 4-71 and described in Table 4-166.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 3. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-165. PRU_ICSS_DBG_CT_REG3 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 248Ch
PRU_ICSS_PRU_DEBUG_1	4802 448Ch

Figure 4-71. PRU_ICSS_DBG_CT_REG3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG3																															
R-00030000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-166. PRU_ICSS_DBG_CT_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG3	R	00030000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

4.5.4.37 PRU_ICSS_DBG_CT_REG4 Register (Offset = 90h) [reset = 00026000h]

PRU_ICSS_DBG_CT_REG4 is shown in Figure 4-72 and described in Table 4-168.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 4. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-167. PRU_ICSS_DBG_CT_REG4 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2490h
PRU_ICSS_PRU_DEBUG_1	4802 4490h

Figure 4-72. PRU_ICSS_DBG_CT_REG4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG4																															
R-00026000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-168. PRU_ICSS_DBG_CT_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG4	R	00026000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

4.5.4.38 PRU_ICSS_DBG_CT_REG5 Register (Offset = 94h) [reset = 48060000h]

PRU_ICSS_DBG_CT_REG5 is shown in Figure 4-73 and described in Table 4-170.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 5. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-169. PRU_ICSS_DBG_CT_REG5 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2494h
PRU_ICSS_PRU_DEBUG_1	4802 4494h

Figure 4-73. PRU_ICSS_DBG_CT_REG5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG5																															
R-48060000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-170. PRU_ICSS_DBG_CT_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG5	R	48060000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

4.5.4.39 PRU_ICSS_DBG_CT_REG6 Register (Offset = 98h) [reset = 48030000h]

PRU_ICSS_DBG_CT_REG6 is shown in Figure 4-74 and described in Table 4-172.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 6. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-171. PRU_ICSS_DBG_CT_REG6 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2498h
PRU_ICSS_PRU_DEBUG_1	4802 4498h

Figure 4-74. PRU_ICSS_DBG_CT_REG6 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG6																															
R-48030000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-172. PRU_ICSS_DBG_CT_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG6	R	48030000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

4.5.4.40 PRU_ICSS_DBG_CT_REG7 Register (Offset = 9Ch) [reset = 00028000h]

PRU_ICSS_DBG_CT_REG7 is shown in Figure 4-75 and described in Table 4-174.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 7. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-173. PRU_ICSS_DBG_CT_REG7 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 249Ch
PRU_ICSS_PRU_DEBUG_1	4802 449Ch

Figure 4-75. PRU_ICSS_DBG_CT_REG7 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG7																															
R-00028000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-174. PRU_ICSS_DBG_CT_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG7	R	00028000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

4.5.4.41 PRU_ICSS_DBG_CT_REG8 Register (Offset = A0h) [reset = 46000000h]

PRU_ICSS_DBG_CT_REG8 is shown in Figure 4-76 and described in Table 4-176.

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DEBUG PRU CONSTANTS TABLE ENTRY 8. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-175. PRU_ICSS_DBG_CT_REG8 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24A0h
PRU_ICSS_PRU_DEBUG_1	4802 44A0h

Figure 4-76. PRU_ICSS_DBG_CT_REG8 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG8																															
R-46000000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-176. PRU_ICSS_DBG_CT_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG8	R	46000000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

4.5.4.42 PRU_ICSS_DBG_CT_REG9 Register (Offset = A4h) [reset = 4A100000h]

PRU_ICSS_DBG_CT_REG9 is shown in Figure 4-77 and described in Table 4-178.

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DEBUG PRU CONSTANTS TABLE ENTRY 9. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-177. PRU_ICSS_DBG_CT_REG9 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24A4h
PRU_ICSS_PRU_DEBUG_1	4802 44A4h

Figure 4-77. PRU_ICSS_DBG_CT_REG9 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG9																															
R-4A100000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-178. PRU_ICSS_DBG_CT_REG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG9	R	4A100000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

4.5.4.43 PRU_ICSS_DBG_CT_REG10 Register (Offset = A8h) [reset = 48318000h]

PRU_ICSS_DBG_CT_REG10 is shown in Figure 4-78 and described in Table 4-180.

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DEBUG PRU CONSTANTS TABLE ENTRY 10. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-179. PRU_ICSS_DBG_CT_REG10 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24A8h
PRU_ICSS_PRU_DEBUG_1	4802 44A8h

Figure 4-78. PRU_ICSS_DBG_CT_REG10 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG10																															
R-48318000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 4-180. PRU_ICSS_DBG_CT_REG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG10	R	48318000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

4.5.4.44 PRU_ICSS_DBG_CT_REG11 Register (Offset = ACh) [reset = 48022000h]

PRU_ICSS_DBG_CT_REG11 is shown in Figure 4-79 and described in Table 4-182.

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DEBUG PRU CONSTANTS TABLE ENTRY 11. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-181. PRU_ICSS_DBG_CT_REG11 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24ACh
PRU_ICSS_PRU_DEBUG_1	4802 44ACh

Figure 4-79. PRU_ICSS_DBG_CT_REG11 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG11																															
R-48022000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-182. PRU_ICSS_DBG_CT_REG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG11	R	48022000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

4.5.4.45 PRU_ICSS_DBG_CT_REG12 Register (Offset = B0h) [reset = 48024000h]

PRU_ICSS_DBG_CT_REG12 is shown in Figure 4-80 and described in Table 4-184.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 12. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-183. PRU_ICSS_DBG_CT_REG12 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24B0h
PRU_ICSS_PRU_DEBUG_1	4802 44B0h

Figure 4-80. PRU_ICSS_DBG_CT_REG12 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG12																															
R-48024000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-184. PRU_ICSS_DBG_CT_REG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG12	R	48024000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

4.5.4.46 PRU_ICSS_DBG_CT_REG13 Register (Offset = B4h) [reset = 48310000h]

PRU_ICSS_DBG_CT_REG13 is shown in Figure 4-81 and described in Table 4-186.

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DEBUG PRU CONSTANTS TABLE ENTRY 13. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-185. PRU_ICSS_DBG_CT_REG13 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24B4h
PRU_ICSS_PRU_DEBUG_1	4802 44B4h

Figure 4-81. PRU_ICSS_DBG_CT_REG13 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG13																															
R-48310000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-186. PRU_ICSS_DBG_CT_REG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG13	R	48310000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

4.5.4.47 PRU_ICSS_DBG_CT_REG14 Register (Offset = B8h) [reset = 481CC000h]

PRU_ICSS_DBG_CT_REG14 is shown in Figure 4-82 and described in Table 4-188.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 14. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-187. PRU_ICSS_DBG_CT_REG14 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24B8h
PRU_ICSS_PRU_DEBUG_1	4802 44B8h

Figure 4-82. PRU_ICSS_DBG_CT_REG14 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG14																															
R-481CC000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-188. PRU_ICSS_DBG_CT_REG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG14	R	481CC000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

4.5.4.48 PRU_ICSS_DBG_CT_REG15 Register (Offset = BCh) [reset = 481D0000h]

PRU_ICSS_DBG_CT_REG15 is shown in Figure 4-83 and described in Table 4-190.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 15. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-189. PRU_ICSS_DBG_CT_REG15 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24BCh
PRU_ICSS_PRU_DEBUG_1	4802 44BCh

Figure 4-83. PRU_ICSS_DBG_CT_REG15 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG15																															
R-481D0000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-190. PRU_ICSS_DBG_CT_REG15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG15	R	481D0000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

4.5.4.49 PRU_ICSS_DBG_CT_REG16 Register (Offset = C0h) [reset = 481A0000h]

PRU_ICSS_DBG_CT_REG16 is shown in Figure 4-84 and described in Table 4-192.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 16. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-191. PRU_ICSS_DBG_CT_REG16 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24C0h
PRU_ICSS_PRU_DEBUG_1	4802 44C0h

Figure 4-84. PRU_ICSS_DBG_CT_REG16 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG16																															
R-481A0000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-192. PRU_ICSS_DBG_CT_REG16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG16	R	481A0000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

4.5.4.50 PRU_ICSS_DBG_CT_REG17 Register (Offset = C4h) [reset = 4819C000h]

PRU_ICSS_DBG_CT_REG17 is shown in Figure 4-85 and described in Table 4-194.

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DEBUG PRU CONSTANTS TABLE ENTRY 17. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-193. PRU_ICSS_DBG_CT_REG17 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24C4h
PRU_ICSS_PRU_DEBUG_1	4802 44C4h

Figure 4-85. PRU_ICSS_DBG_CT_REG17 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG17																															
R-4819C000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-194. PRU_ICSS_DBG_CT_REG17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG17	R	4819C000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

4.5.4.51 PRU_ICSS_DBG_CT_REG18 Register (Offset = C8h) [reset = 48300000h]

PRU_ICSS_DBG_CT_REG18 is shown in Figure 4-86 and described in Table 4-196.

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DEBUG PRU CONSTANTS TABLE ENTRY 18. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-195. PRU_ICSS_DBG_CT_REG18 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24C8h
PRU_ICSS_PRU_DEBUG_1	4802 44C8h

Figure 4-86. PRU_ICSS_DBG_CT_REG18 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG18																															
R-48300000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-196. PRU_ICSS_DBG_CT_REG18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG18	R	48300000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

4.5.4.52 PRU_ICSS_DBG_CT_REG19 Register (Offset = CCh) [reset = 48302000h]

PRU_ICSS_DBG_CT_REG19 is shown in Figure 4-87 and described in Table 4-198.

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DEBUG PRU CONSTANTS TABLE ENTRY 19. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-197. PRU_ICSS_DBG_CT_REG19 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24CCh
PRU_ICSS_PRU_DEBUG_1	4802 44CCh

Figure 4-87. PRU_ICSS_DBG_CT_REG19 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG19																															
R-48302000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-198. PRU_ICSS_DBG_CT_REG19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG19	R	48302000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

4.5.4.53 PRU_ICSS_DBG_CT_REG20 Register (Offset = D0h) [reset = 48304000h]

PRU_ICSS_DBG_CT_REG20 is shown in Figure 4-88 and described in Table 4-200.

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DEBUG PRU CONSTANTS TABLE ENTRY 20. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-199. PRU_ICSS_DBG_CT_REG20 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24D0h
PRU_ICSS_PRU_DEBUG_1	4802 44D0h

Figure 4-88. PRU_ICSS_DBG_CT_REG20 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG20																															
R-48304000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-200. PRU_ICSS_DBG_CT_REG20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG20	R	48304000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

4.5.4.54 PRU_ICSS_DBG_CT_REG21 Register (Offset = D4h) [reset = 00032400h]

PRU_ICSS_DBG_CT_REG21 is shown in Figure 4-89 and described in Table 4-202.

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DEBUG PRU CONSTANTS TABLE ENTRY 21. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-201. PRU_ICSS_DBG_CT_REG21 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24D4h
PRU_ICSS_PRU_DEBUG_1	4802 44D4h

Figure 4-89. PRU_ICSS_DBG_CT_REG21 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG21																															
R-00032400h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-202. PRU_ICSS_DBG_CT_REG21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG21	R	00032400h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

4.5.4.55 PRU_ICSS_DBG_CT_REG22 Register (Offset = D8h) [reset = 480C8000h]

PRU_ICSS_DBG_CT_REG22 is shown in Figure 4-90 and described in Table 4-204.

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DEBUG PRU CONSTANTS TABLE ENTRY 22. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-203. PRU_ICSS_DBG_CT_REG22 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24D8h
PRU_ICSS_PRU_DEBUG_1	4802 44D8h

Figure 4-90. PRU_ICSS_DBG_CT_REG22 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG22																															
R-480C8000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-204. PRU_ICSS_DBG_CT_REG22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG22	R	480C8000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

4.5.4.56 PRU_ICSS_DBG_CT_REG23 Register (Offset = DCh) [reset = 480CA000h]

PRU_ICSS_DBG_CT_REG23 is shown in Figure 4-91 and described in Table 4-206.

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DEBUG PRU CONSTANTS TABLE ENTRY 23. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-205. PRU_ICSS_DBG_CT_REG23 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24DCh
PRU_ICSS_PRU_DEBUG_1	4802 44DCh

Figure 4-91. PRU_ICSS_DBG_CT_REG23 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG23																															
R-480CA000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-206. PRU_ICSS_DBG_CT_REG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG23	R	480CA000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

4.5.4.57 PRU_ICSS_DBG_CT_REG24 Register (Offset = E0h) [reset = 0h]

PRU_ICSS_DBG_CT_REG24 is shown in Figure 4-92 and described in Table 4-208.

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DEBUG PRU CONSTANTS TABLE ENTRY 24. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-207. PRU_ICSS_DBG_CT_REG24 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24E0h
PRU_ICSS_PRU_DEBUG_1	4802 44E0h

Figure 4-92. PRU_ICSS_DBG_CT_REG24 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG24																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 4-208. PRU_ICSS_DBG_CT_REG24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG24	R	0h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table. This entry is partially programmable through the C24_BLK_INDEX in the PRU Control register. The reset value for this Constant Table Entry is 0x00000n00, n=C24_BLK_INDEX[3:0].

4.5.4.58 PRU_ICSS_DBG_CT_REG25 Register (Offset = E4h) [reset = 0h]

PRU_ICSS_DBG_CT_REG25 is shown in Figure 4-93 and described in Table 4-210.

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DEBUG PRU CONSTANTS TABLE ENTRY 25. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-209. PRU_ICSS_DBG_CT_REG25 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24E4h
PRU_ICSS_PRU_DEBUG_1	4802 44E4h

Figure 4-93. PRU_ICSS_DBG_CT_REG25 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG25																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-210. PRU_ICSS_DBG_CT_REG25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG25	R	0h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table. This entry is partially programmable through the C25_BLK_INDEX in the PRU Control register. The reset value for this Constant Table Entry is 0x00002n00, n=C25_BLK_INDEX[3:0].

4.5.4.59 PRU_ICSS_DBG_CT_REG26 Register (Offset = E8h) [reset = 0h]

PRU_ICSS_DBG_CT_REG26 is shown in Figure 4-94 and described in Table 4-212.

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DEBUG PRU CONSTANTS TABLE ENTRY 26. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-211. PRU_ICSS_DBG_CT_REG26 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24E8h
PRU_ICSS_PRU_DEBUG_1	4802 44E8h

Figure 4-94. PRU_ICSS_DBG_CT_REG26 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG26																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 4-212. PRU_ICSS_DBG_CT_REG26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG26	R	0h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table. This entry is partially programmable through the C26_BLK_INDEX in the PRU Control register. The reset value for this Constant Table Entry is 0x0002En00, n=C26_BLK_INDEX[3:0].

4.5.4.60 PRU_ICSS_DBG_CT_REG27 Register (Offset = ECh) [reset = 0h]

PRU_ICSS_DBG_CT_REG27 is shown in Figure 4-95 and described in Table 4-214.

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DEBUG PRU CONSTANTS TABLE ENTRY 27. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-213. PRU_ICSS_DBG_CT_REG27 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24ECh
PRU_ICSS_PRU_DEBUG_1	4802 44ECh

Figure 4-95. PRU_ICSS_DBG_CT_REG27 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG27																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-214. PRU_ICSS_DBG_CT_REG27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG27	R	0h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table. This entry is partially programmable through the C27_BLK_INDEX in the PRU Control register. The reset value for this Constant Table Entry is 0x00032n00, n=C27_BLK_INDEX[3:0].

4.5.4.61 PRU_ICSS_DBG_CT_REG28 Register (Offset = F0h) [reset = 0h]

PRU_ICSS_DBG_CT_REG28 is shown in Figure 4-96 and described in Table 4-216.

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DEBUG PRU CONSTANTS TABLE ENTRY 28. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-215. PRU_ICSS_DBG_CT_REG28 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24F0h
PRU_ICSS_PRU_DEBUG_1	4802 44F0h

Figure 4-96. PRU_ICSS_DBG_CT_REG28 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG28																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 4-216. PRU_ICSS_DBG_CT_REG28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG28	R	0h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table. This entry is partially programmable through the C28_POINTER in the PRU Control register. The reset value for this Constant Table Entry is 0x00nnnn00, nnnn=C28_POINTER[15:0].

4.5.4.62 PRU_ICSS_DBG_CT_REG29 Register (Offset = F4h) [reset = 0h]

PRU_ICSS_DBG_CT_REG29 is shown in Figure 4-97 and described in Table 4-218.

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DEBUG PRU CONSTANTS TABLE ENTRY 29. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-217. PRU_ICSS_DBG_CT_REG29 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24F4h
PRU_ICSS_PRU_DEBUG_1	4802 44F4h

Figure 4-97. PRU_ICSS_DBG_CT_REG29 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG29																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-218. PRU_ICSS_DBG_CT_REG29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG29	R	0h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table. This entry is partially programmable through the C29_POINTER in the PRU Control register. The reset value for this Constant Table Entry is 0x49nnnn00, nnnn=C29_POINTER[15:0].

4.5.4.63 PRU_ICSS_DBG_CT_REG30 Register (Offset = F8h) [reset = 0h]

PRU_ICSS_DBG_CT_REG30 is shown in Figure 4-98 and described in Table 4-220.

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DEBUG PRU CONSTANTS TABLE ENTRY 30. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-219. PRU_ICSS_DBG_CT_REG30 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24F8h
PRU_ICSS_PRU_DEBUG_1	4802 44F8h

Figure 4-98. PRU_ICSS_DBG_CT_REG30 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG30																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 4-220. PRU_ICSS_DBG_CT_REG30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG30	R	0h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table. This entry is partially programmable through the C30_POINTER in the PRU Control register. The reset value for this Constant Table Entry is 0x40nnnn00, nnnn=C30_POINTER[15:0].

4.5.4.64 PRU_ICSS_DBG_CT_REG31 Register (Offset = FCh) [reset = 0h]

PRU_ICSS_DBG_CT_REG31 is shown in Figure 4-99 and described in Table 4-222.

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DEBUG PRU CONSTANTS TABLE ENTRY 31. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-221. PRU_ICSS_DBG_CT_REG31 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24FCh
PRU_ICSS_PRU_DEBUG_1	4802 44FCh

Figure 4-99. PRU_ICSS_DBG_CT_REG31 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG31																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-222. PRU_ICSS_DBG_CT_REG31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG31	R	0h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table. This entry is partially programmable through the C31_POINTER in the PRU Control register. The reset value for this Constant Table Entry is 0x80nnnn00, nnnn=C31_POINTER[15:0].

4.5.5 PRU_ICSS Interrupt Contoller Registers

PRU_ICSS_INTC Registers lists the memory-mapped registers for the PRU-ICSS interrupt controller. All register offset addresses not listed in PRU_ICSS_INTC Registers should be considered as reserved locations and the register contents should not be modified.

Table 4-223. PRU_ICSS_INTC Instances

Instance	Base Address
PRU_ICSS_INTC	4802 0000h

Table 4-224. PRU_ICSS_INTC Registers

Offset	Acronym	Register Name	PRU_ICSS_INTC Physical Address
0h	PRU_ICSS_INTC_REVID	Revision ID Register	4802 0000h
4h	PRU_ICSS_INTC_CR	Control Register	4802 0004h
10h	PRU_ICSS_INTC_GER	Global Host Interrupt Enable Register	4802 0010h
1Ch	PRU_ICSS_INTC_GNLR	Global Nesting Level Register	4802 001Ch
20h	PRU_ICSS_INTC_SISR	System Interrupt Status Indexed Set Register	4802 0020h
24h	PRU_ICSS_INTC_SICR	System Interrupt Status Indexed Clear Register	4802 0024h
28h	PRU_ICSS_INTC_EISR	System Interrupt Enable Indexed Set Register	4802 0028h
2Ch	PRU_ICSS_INTC_EICR	System Interrupt Enable Indexed Clear Register	4802 002Ch
34h	PRU_ICSS_INTC_HIEISR	Host Interrupt Enable Indexed Set Register	4802 0034h
38h	PRU_ICSS_INTC_HIEICR	Host Interrupt Enable Indexed Clear Register	4802 0038h
80h	PRU_ICSS_INTC_GPIR	Global Prioritized Index Register	4802 0080h
200h	PRU_ICSS_INTC_SRS0	System Interrupt Status Raw Set Register0	4802 0200h
204h	PRU_ICSS_INTC_SRS1	System Interrupt Status Raw Set Register1	4802 0204h
280h	PRU_ICSS_INTC_SECR0	System Interrupt Status Enabled Clear Register0	4802 0280h
284h	PRU_ICSS_INTC_SECR1	System Interrupt Status Enabled Clear Register1	4802 0284h
300h	PRU_ICSS_INTC_ESR0	System Interrupt Enable Set Register0	4802 0300h
304h	PRU_ICSS_INTC_ESR1	System Interrupt Enable Set Register1	4802 0304h
380h	PRU_ICSS_INTC_ECR0	System Interrupt Enable Clear Register0	4802 0380h
384h	PRU_ICSS_INTC_ECR1	System Interrupt Enable Clear Register1	4802 0384h
400h	PRU_ICSS_INTC_CMR_0	Channel Map Register_0	4802 0400h
404h	PRU_ICSS_INTC_CMR_1	Channel Map Register_1	4802 0404h
408h	PRU_ICSS_INTC_CMR_2	Channel Map Register_2	4802 0408h
40Ch	PRU_ICSS_INTC_CMR_3	Channel Map Register_3	4802 040Ch
410h	PRU_ICSS_INTC_CMR_4	Channel Map Register_4	4802 0410h
414h	PRU_ICSS_INTC_CMR_5	Channel Map Register_5	4802 0414h
418h	PRU_ICSS_INTC_CMR_6	Channel Map Register_6	4802 0418h
41Ch	PRU_ICSS_INTC_CMR_7	Channel Map Register_7	4802 041Ch
420h	PRU_ICSS_INTC_CMR_8	Channel Map Register_8	4802 0420h
424h	PRU_ICSS_INTC_CMR_9	Channel Map Register_9	4802 0424h
428h	PRU_ICSS_INTC_CMR_10	Channel Map Register_10	4802 0428h
42Ch	PRU_ICSS_INTC_CMR_11	Channel Map Register_11	4802 042Ch
430h	PRU_ICSS_INTC_CMR_12	Channel Map Register_12	4802 0430h
434h	PRU_ICSS_INTC_CMR_13	Channel Map Register_13	4802 0434h
438h	PRU_ICSS_INTC_CMR_14	Channel Map Register_14	4802 0438h
43Ch	PRU_ICSS_INTC_CMR_15	Channel Map Register_15	4802 043Ch
800h	PRU_ICSS_INTC_HMR0	Host Interrupt Map Register0	4802 0800h
804h	PRU_ICSS_INTC_HMR1	Host Interrupt Map Register1	4802 0804h
808h	PRU_ICSS_INTC_HMR2	Host Interrupt Map Register2	4802 0808h

Table 4-224. PRU_ICSS_INTC Registers (continued)

Offset	Acronym	Register Name	PRU_ICSS_INTC Physical Address
900h	PRU_ICSS_INTC_HIPIR_0	Host Interrupt Prioritized Index Register_0	4802 0900h
904h	PRU_ICSS_INTC_HIPIR_1	Host Interrupt Prioritized Index Register_1	4802 0904h
908h	PRU_ICSS_INTC_HIPIR_2	Host Interrupt Prioritized Index Register_2	4802 0908h
90Ch	PRU_ICSS_INTC_HIPIR_3	Host Interrupt Prioritized Index Register_3	4802 090Ch
910h	PRU_ICSS_INTC_HIPIR_4	Host Interrupt Prioritized Index Register_4	4802 0910h
914h	PRU_ICSS_INTC_HIPIR_5	Host Interrupt Prioritized Index Register_5	4802 0914h
918h	PRU_ICSS_INTC_HIPIR_6	Host Interrupt Prioritized Index Register_6	4802 0918h
91Ch	PRU_ICSS_INTC_HIPIR_7	Host Interrupt Prioritized Index Register_7	4802 091Ch
920h	PRU_ICSS_INTC_HIPIR_8	Host Interrupt Prioritized Index Register_8	4802 0920h
924h	PRU_ICSS_INTC_HIPIR_9	Host Interrupt Prioritized Index Register_9	4802 0924h
D00h	PRU_ICSS_INTC_SIPR0	System Interrupt Polarity Register0	4802 0D00h
D04h	PRU_ICSS_INTC_SIPR1	System Interrupt Polarity Register1	4802 0D04h
D80h	PRU_ICSS_INTC_SITR0	System Interrupt Type Register0	4802 0D80h
D84h	PRU_ICSS_INTC_SITR1	System Interrupt Type Register1	4802 0D84h
1100h	PRU_ICSS_INTC_HINLR_0	Host Interrupt Nesting Level Register_0	4802 1100h
1104h	PRU_ICSS_INTC_HINLR_1	Host Interrupt Nesting Level Register_1	4802 1104h
1108h	PRU_ICSS_INTC_HINLR_2	Host Interrupt Nesting Level Register_2	4802 1108h
110Ch	PRU_ICSS_INTC_HINLR_3	Host Interrupt Nesting Level Register_3	4802 110Ch
1110h	PRU_ICSS_INTC_HINLR_4	Host Interrupt Nesting Level Register_4	4802 1110h
1114h	PRU_ICSS_INTC_HINLR_5	Host Interrupt Nesting Level Register_5	4802 1114h
1118h	PRU_ICSS_INTC_HINLR_6	Host Interrupt Nesting Level Register_6	4802 1118h
111Ch	PRU_ICSS_INTC_HINLR_7	Host Interrupt Nesting Level Register_7	4802 111Ch
1120h	PRU_ICSS_INTC_HINLR_8	Host Interrupt Nesting Level Register_8	4802 1120h
1124h	PRU_ICSS_INTC_HINLR_9	Host Interrupt Nesting Level Register_9	4802 1124h
1500h	PRU_ICSS_INTC_HIER	Host Interrupt Enable Registers	4802 1500h

4.5.5.1 PRU_ICSS_INTC_REVID Register (Offset = 0h) [reset = 0h]

PRU_ICSS_INTC_REVID is shown in Figure 4-100 and described in .

Revision ID Register

Table 4-225. PRU_ICSS_INTC_REVID Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0000h

Figure 4-100. PRU_ICSS_INTC_REVID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															
R--h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-226. PRU_ICSS_INTC_REVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REVISION	R	-h	IP Revision

4.5.5.2 PRU_ICSS_INTC_CR Register (Offset = 4h) [reset = 0h]

PRU_ICSS_INTC_CR is shown in Figure 4-101 and described in Table 4-228.

The Control Register holds global control parameters and can forces a soft reset on the module.

Table 4-227. PRU_ICSS_INTC_CR Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0004h

Figure 4-101. PRU_ICSS_INTC_CR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			PRIORITY_HOLD_MODE	NEST_MODE		WAKEUP_MODE	RESERVED
R-0h			R/W-0h	R/W-0h		R/W-0h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-228. PRU_ICSS_INTC_CR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	PRIORITY_HOLD_MODE	R/W	0h	Reserved
3-2	NEST_MODE	R/W	0h	The nesting mode. 0h: No nesting 1h: Automatic individual nesting (per host interrupt) 2h: Automatic global nesting (over all host interrupts) 3h: Manual nesting
1	WAKEUP_MODE	R/W	0h	Reserved
0	RESERVED	R	0h	Reserved

4.5.5.3 PRU_ICSS_INTC_GER Register (Offset = 10h) [reset = 0h]

PRU_ICSS_INTC_GER is shown in Figure 4-102 and described in Table 4-230.

The Global Host Interrupt Enable Register enables all the host interrupts. Individual host interrupts are still enabled or disabled from their individual enables and are not overridden by the global enable.

Table 4-229. PRU_ICSS_INTC_GER Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0010h

Figure 4-102. PRU_ICSS_INTC_GER Register

31	30	29	28	27	26	25	24
RESERVED							
R-0000 000h							
23	22	21	20	19	18	17	16
RESERVED							
R-0000 000h							
15	14	13	12	11	10	9	8
RESERVED							
R-0000 000h							
7	6	5	4	3	2	1	0
RESERVED							ENABLE_HINT_ANY
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-230. PRU_ICSS_INTC_GER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0000 000h	Reserved
0	ENABLE_HINT_ANY	R/W	0h	The current global enable value when read. Writes set the global enable.

4.5.5.4 PRU_ICSS_INTC_GNLR Register (Offset = 1Ch) [reset = 100h]

PRU_ICSS_INTC_GNLR is shown in Figure 4-103 and described in Table 4-232.

The Global Nesting Level Register allows the checking and setting of the global nesting level across all host interrupts when automatic global nesting mode is set. The nesting level is the channel (and all of lower priority) that are nested out because of a current interrupt. This register is only available when nesting is configured.

Table 4-231. PRU_ICSS_INTC_GNLR Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 001Ch

Figure 4-103. PRU_ICSS_INTC_GNLR Register

31	30	29	28	27	26	25	24
AUTO_OVERRIDE	RESERVED						
W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							GLB_NEST_LEVEL
R-0h							R/W-100h
7	6	5	4	3	2	1	0
GLB_NEST_LEVEL							
R/W-100h							

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; *-n* = value after reset

Table 4-232. PRU_ICSS_INTC_GNLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AUTO_OVERRIDE	W	0h	Always read as 0. Writes of 1 override the automatic nesting and set the nesting_level to the written data.
30-9	RESERVED	R	0h	Reserved
8-0	GLB_NEST_LEVEL	R/W	100h	The current global nesting level (highest channel that is nested). Writes set the nesting level. In auto nesting mode this value is updated internally unless the auto_override bit is set.

4.5.5.5 PRU_ICSS_INTC_SISR Register (Offset = 20h) [reset = 0h]

PRU_ICSS_INTC_SISR is shown in Figure 4-104 and described in Table 4-234.

The System Interrupt Status Indexed Set Register allows setting the status of an interrupt. The interrupt to set is the index value written. This sets the Raw Status Register bit of the given index.

Table 4-233. PRU_ICSS_INTC_SISR Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0020h

Figure 4-104. PRU_ICSS_INTC_SISR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0000 00h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						STATUS_SET_INDEX									
R-0000 00h						W-0h									

LEGEND: R = Read Only; W = Write Only; *-n* = value after reset

Table 4-234. PRU_ICSS_INTC_SISR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0000 00h	Reserved
9-0	STATUS_SET_INDEX	W	0h	Writes set the status of the interrupt given in the index value. Reads return 0.

4.5.5.6 PRU_ICSS_INTC_SICR Register (Offset = 24h) [reset = 0h]

PRU_ICSS_INTC_SICR is shown in Figure 4-105 and described in Table 4-236.

The System Interrupt Status Indexed Clear Register allows clearing the status of an interrupt. The interrupt to clear is the index value written. This clears the Raw Status Register bit of the given index.

Table 4-235. PRU_ICSS_INTC_SICR Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0024h

Figure 4-105. PRU_ICSS_INTC_SICR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0000 00h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						STATUS_CLR_INDEX									
R-0000 00h						W-0h									

LEGEND: R = Read Only; W = Write Only; *-n* = value after reset

Table 4-236. PRU_ICSS_INTC_SICR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0000 00h	Reserved
9-0	STATUS_CLR_INDEX	W	0h	Writes clear the status of the interrupt given in the index value. Reads return 0.

4.5.5.7 PRU_ICSS_INTC_EISR Register (Offset = 28h) [reset = 0h]

PRU_ICSS_INTC_EISR is shown in Figure 4-106 and described in Table 4-238.

The System Interrupt Enable Indexed Set Register allows enabling an interrupt. The interrupt to enable is the index value written. This sets the Enable Register bit of the given index.

Table 4-237. PRU_ICSS_INTC_EISR Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0028h

Figure 4-106. PRU_ICSS_INTC_EISR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0000 00h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						ENABLE_SET_INDEX									
R-0000 00h						W-0h									

LEGEND: R = Read Only; W = Write Only; *-n* = value after reset

Table 4-238. PRU_ICSS_INTC_EISR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0000 00h	Reserved
9-0	ENABLE_SET_INDEX	W	0h	Writes set the enable of the interrupt given in the index value. Reads return 0.

4.5.5.8 PRU_ICSS_INTC_EICR Register (Offset = 2Ch) [reset = 0h]

PRU_ICSS_INTC_EICR is shown in Figure 4-107 and described in Table 4-240.

The System Interrupt Enable Indexed Clear Register allows disabling an interrupt. The interrupt to disable is the index value written. This clears the Enable Register bit of the given index.

Table 4-239. PRU_ICSS_INTC_EICR Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 002Ch

Figure 4-107. PRU_ICSS_INTC_EICR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0000 00h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						ENABLE_CLR_INDEX									
R-0000 00h						W-0h									

LEGEND: R = Read Only; W = Write Only; *-n* = value after reset

Table 4-240. PRU_ICSS_INTC_EICR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0000 00h	Reserved
9-0	ENABLE_CLR_INDEX	W	0h	Writes clear the enable of the interrupt given in the index value. Reads return 0.

4.5.5.9 PRU_ICSS_INTC_HIEISR Register (Offset = 34h) [reset = 0h]

PRU_ICSS_INTC_HIEISR is shown in Figure 4-108 and described in Table 4-242.

The Host Interrupt Enable Indexed Set Register allows enabling a host interrupt output. The host interrupt to enable is the index value written. This enables the host interrupt output or triggers the output again if already enabled.

Table 4-241. PRU_ICSS_INTC_HIEISR Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0034h

Figure 4-108. PRU_ICSS_INTC_HIEISR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0000 00h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						HINT_ENABLE_SET_INDEX									
R-0000 00h						R/W-0h									

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-242. PRU_ICSS_INTC_HIEISR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0000 00h	Reserved
9-0	HINT_ENABLE_SET_INDEX	R/W	0h	Writes set the enable of the host interrupt given in the index value. Reads return 0.

4.5.5.10 PRU_ICSS_INTC_HIEICR Register (Offset = 38h) [reset = 0h]

PRU_ICSS_INTC_HIEICR is shown in Figure 4-109 and described in Table 4-244.

The Host Interrupt Enable Indexed Clear Register allows disabling a host interrupt output. The host interrupt to disable is the index value written. This disables the host interrupt output.

Table 4-243. PRU_ICSS_INTC_HIEICR Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0038h

Figure 4-109. PRU_ICSS_INTC_HIEICR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0000 00h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						HINT_ENABLE_CLR_INDEX									
R-0000 00h						R/W-0h									

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-244. PRU_ICSS_INTC_HIEICR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0000 00h	Reserved
9-0	HINT_ENABLE_CLR_INDEX	R/W	0h	Writes clear the enable of the host interrupt given in the index value. Reads return 0.

4.5.5.11 PRU_ICSS_INTC_GPIR Register (Offset = 80h) [reset = 80000000h]

PRU_ICSS_INTC_GPIR is shown in Figure 4-110 and described in Table 4-246.

The Global Prioritized Index Register shows the interrupt number of the highest priority interrupt pending across all the host interrupts.

Table 4-245. PRU_ICSS_INTC_GPIR Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0080h

Figure 4-110. PRU_ICSS_INTC_GPIR Register

31	30	29	28	27	26	25	24
GLB_NONE	RESERVED						
R-1h	R-0000 00h						
23	22	21	20	19	18	17	16
RESERVED							
R-0000 00h							
15	14	13	12	11	10	9	8
RESERVED						GLB_PRI_INTR	
R-0000 00h						R-0h	
7	6	5	4	3	2	1	0
GLB_PRI_INTR							
R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 4-246. PRU_ICSS_INTC_GPIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GLB_NONE	R	1h	No Interrupt is pending. Can be used by host to test for a negative value to see if no interrupts are pending.
30-10	RESERVED	R	0000 00h	Reserved
9-0	GLB_PRI_INTR	R	0h	The currently highest priority interrupt index pending across all the host interrupts.

4.5.5.12 PRU_ICSS_INTC_SRSR0 Register (Offset = 200h) [reset = 0h]

PRU_ICSS_INTC_SRSR0 is shown in Figure 4-111 and described in Table 4-248.

The System Interrupt Status Raw Set Register0 show the pending enabled status of the system interrupts 0 to 31. Software can write to the Status Set Registers to set a system interrupt without a hardware trigger. There is one bit per system interrupt.

Table 4-247. PRU_ICSS_INTC_SRSR0 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0200h

Figure 4-111. PRU_ICSS_INTC_SRSR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAW_STATUS_31_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-248. PRU_ICSS_INTC_SRSR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RAW_STATUS_31_0	R/W	0h	System interrupt raw status and setting of the system interrupts 0 to 31. Reads return the raw status. Write a 1 in a bit position to set the status of the system interrupt. Writing a 0 has no effect.

4.5.5.13 PRU_ICSS_INTC_SRSR1 Register (Offset = 204h) [reset = 0h]

PRU_ICSS_INTC_SRSR1 is shown in Figure 4-112 and described in Table 4-250.

The System Interrupt Status Raw Set Register1 show the pending enabled status of the system interrupts 32 to 63. Software can write to the Status Set Registers to set a system interrupt without a hardware trigger. There is one bit per system interrupt.

Table 4-249. PRU_ICSS_INTC_SRSR1 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0204h

Figure 4-112. PRU_ICSS_INTC_SRSR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAW_STATUS_63_32																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-250. PRU_ICSS_INTC_SRSR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RAW_STATUS_63_32	R/W	0h	System interrupt raw status and setting of the system interrupts 32 to 63. Reads return the raw status. Write a 1 in a bit position to set the status of the system interrupt. Writing a 0 has no effect.

4.5.5.14 PRU_ICSS_INTC_SECR0 Register (Offset = 280h) [reset = 0h]

PRU_ICSS_INTC_SECR0 is shown in Figure 4-113 and described in Table 4-252.

The System Interrupt Status Enabled Clear Register0 show the pending enabled status of the system interrupts 0 to 31. Software can write to the Status Clear Registers to clear a system interrupt after it has been serviced. If a system interrupt status is not cleared then another host interrupt may not be triggered or another host interrupt may be triggered incorrectly. There is one bit per system interrupt.

Table 4-251. PRU_ICSS_INTC_SECR0 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0280h

Figure 4-113. PRU_ICSS_INTC_SECR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENA_STATUS_31_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-252. PRU_ICSS_INTC_SECR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ENA_STATUS_31_0	R/W	0h	System interrupt enabled status and clearing of the system interrupts 0 to 31. Reads return the enabled status (before enabling with the Enable Registers). Write a 1 in a bit position to clear the status of the system interrupt. Writing a 0 has no effect.

4.5.5.15 PRU_ICSS_INTC_SECR1 Register (Offset = 284h) [reset = 0h]

PRU_ICSS_INTC_SECR1 is shown in Figure 4-114 and described in Table 4-254.

The System Interrupt Status Enabled Clear Register1 show the pending enabled status of the system interrupts 32 to 63. Software can write to the Status Clear Registers to clear a system interrupt after it has been serviced. If a system interrupt status is not cleared then another host interrupt may not be triggered or another host interrupt may be triggered incorrectly. There is one bit per system interrupt.

Table 4-253. PRU_ICSS_INTC_SECR1 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0284h

Figure 4-114. PRU_ICSS_INTC_SECR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENA_STATUS_63_32																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-254. PRU_ICSS_INTC_SECR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ENA_STATUS_63_32	R/W	0h	System interrupt enabled status and clearing of the system interrupts 32 to 63. Reads return the enabled status (before enabling with the Enable Registers). Write a 1 in a bit position to clear the status of the system interrupt. Writing a 0 has no effect.

4.5.5.16 PRU_ICSS_INTC_ESR0 Register (Offset = 300h) [reset = 0h]

PRU_ICSS_INTC_ESR0 is shown in Figure 4-115 and described in Table 4-256.

The System Interrupt Enable Set Register0 enables system interrupts 0 to 31 to trigger outputs. System interrupts that are not enabled do not interrupt the host. There is a bit per system interrupt.

Table 4-255. PRU_ICSS_INTC_ESR0 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0300h

Figure 4-115. PRU_ICSS_INTC_ESR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENABLE_SET_31_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-256. PRU_ICSS_INTC_ESR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ENABLE_SET_31_0	R/W	0h	System interrupt enables system interrupts 0 to 31. Read returns the enable value (0 = disabled, 1 = enabled). Write a 1 in a bit position to set that enable. Writing a 0 has no effect.

4.5.5.17 PRU_ICSS_INTC_ERS1 Register (Offset = 304h) [reset = 0h]

PRU_ICSS_INTC_ESR1 is shown in Figure 4-116 and described in Table 4-258.

The System Interrupt Enable Set Register1 enables system interrupts 32 to 63 to trigger outputs. System interrupts that are not enabled do not interrupt the host. There is a bit per system interrupt.

Table 4-257. PRU_ICSS_INTC_ERS1 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0304h

Figure 4-116. PRU_ICSS_INTC_ERS1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENABLE_SET_63_32																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-258. PRU_ICSS_INTC_ERS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ENABLE_SET_63_32	R/W	0h	System interrupt enables system interrupts 32 to 63. Read returns the enable value (0 = disabled, 1 = enabled). Write a 1 in a bit position to set that enable. Writing a 0 has no effect.

4.5.5.18 PRU_ICSS_INTC_ECR0 Register (Offset = 380h) [reset = 0h]

PRU_ICSS_INT_ECR0 is shown in Figure 4-117 and described in Table 4-260.

The System Interrupt Enable Clear Register0 disables system interrupts 0 to 31 to map to channels. System interrupts that are not enabled do not interrupt the host. There is a bit per system interrupt.

Table 4-259. PRU_ICSS_INTC_ECR0 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0380h

Figure 4-117. PRU_ICSS_INTC_ECR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENABLE_CLR_31_0																															
W-0h																															

LEGEND: W = Write Only; *-n* = value after reset

Table 4-260. PRU_ICSS_INTC_ECR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ENABLE_CLR_31_0	W	0h	System interrupt enables system interrupts 0 to 31. Write a 1 in a bit position to clear that enable. Writing a 0 has no effect.

4.5.5.19 PRU_ICSS_INTC_ECR1 Register (Offset = 384h) [reset = 0h]

PRU_ICSS_INTC_ECR1 is shown in Figure 4-118 and described in Table 4-262.

The System Interrupt Enable Clear Register1 disables system interrupts 32 to 63 to map to channels. System interrupts that are not enabled do not interrupt the host. There is a bit per system interrupt.

Table 4-261. PRU_ICSS_INTC_ECR1 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0384h

Figure 4-118. PRU_ICSS_INTC_ECR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENABLE_CLR_63_32																															
W-0h																															

LEGEND: W = Write Only; *-n* = value after reset

Table 4-262. PRU_ICSS_INTC_ECR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ENABLE_CLR_63_32	W	0h	System interrupt enables system interrupts 32 to 63. Write a 1 in a bit position to clear that enable. Writing a 0 has no effect.

4.5.5.20 PRU_ICSS_INTC_CMR_0 Register (Offset = 400h) [reset = 0h]

PRU_ICSS_INTC_CMR_0 is shown in Figure 4-119 and described in Table 4-264.

The Channel Map Register0 specify the channel for the system interrupts 0 to 3. There is one register per 4 system interrupts.

Table 4-263. PRU_ICSS_INTC_CMR_0 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0400h

Figure 4-119. PRU_ICSS_INTC_CMR_0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_3				RESERVED				CH_MAP_2			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_1				RESERVED				CH_MAP_0			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-264. PRU_ICSS_INTC_CMR_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	CH_MAP_3	R/W	0h	Sets the channel for the system interrupt 3
23-20	RESERVED	R	0h	Reserved
19-16	CH_MAP_2	R/W	0h	Sets the channel for the system interrupt 2
15-12	RESERVED	R	0h	Reserved
11-8	CH_MAP_1	R/W	0h	Sets the channel for the system interrupt 1
7-4	RESERVED	R	0h	Reserved
3-0	CH_MAP_0	R/W	0h	Sets the channel for the system interrupt 0

4.5.5.21 PRU_ICSS_INTC_CMR_1 Register (Offset = 404h) [reset = 0h]

PRU_ICSS_INTC_CMR_1 is shown in Figure 4-120 and described in Table 4-266.

The Channel Map Register1 specify the channel for the system interrupts 4 to 7. There is one register per 4 system interrupts.

Table 4-265. PRU_ICSS_INTC_CMR_1 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0404h

Figure 4-120. PRU_ICSS_INTC_CMR_1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_7				RESERVED				CH_MAP_6			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_5				RESERVED				CH_MAP_4			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-266. PRU_ICSS_INTC_CMR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	CH_MAP_7	R/W	0h	Sets the channel for the system interrupt 7
23-20	RESERVED	R	0h	Reserved
19-16	CH_MAP_6	R/W	0h	Sets the channel for the system interrupt 6
15-12	RESERVED	R	0h	Reserved
11-8	CH_MAP_5	R/W	0h	Sets the channel for the system interrupt 5
7-4	RESERVED	R	0h	Reserved
3-0	CH_MAP_4	R/W	0h	Sets the channel for the system interrupt 4

4.5.5.22 PRU_ICSS_INTC_CMR_2 Register (Offset = 408h) [reset = 0h]

PRU_ICSS_INTC_CMR_2 is shown in Figure 4-121 and described in Table 4-268.

The Channel Map Register2 specify the channel for the system interrupts 8 to 11. There is one register per 4 system interrupts.

Table 4-267. PRU_ICSS_INTC_CMR_2 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0408h

Figure 4-121. PRU_ICSS_INTC_CMR_2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_11				RESERVED				CH_MAP_10			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_9				RESERVED				CH_MAP_8			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-268. PRU_ICSS_INTC_CMR_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	CH_MAP_11	R/W	0h	Sets the channel for the system interrupt 11
23-20	RESERVED	R	0h	Reserved
19-16	CH_MAP_10	R/W	0h	Sets the channel for the system interrupt 10
15-12	RESERVED	R	0h	Reserved
11-8	CH_MAP_9	R/W	0h	Sets the channel for the system interrupt 9
7-4	RESERVED	R	0h	Reserved
3-0	CH_MAP_8	R/W	0h	Sets the channel for the system interrupt 8

4.5.5.23 PRU_ICSS_INTC_CMR_3 Register (Offset = 40Ch) [reset = 0h]

PRU_ICSS_INTC_CMR_3 is shown in Figure 4-122 and described in Table 4-270.

The Channel Map Register3 specify the channel for the system interrupts 12 to 15. There is one register per 4 system interrupts.

Table 4-269. PRU_ICSS_INTC_CMR_3 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 040Ch

Figure 4-122. PRU_ICSS_INTC_CMR_3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_15				RESERVED				CH_MAP_14			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_13				RESERVED				CH_MAP_12			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-270. PRU_ICSS_INTC_CMR_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	CH_MAP_15	R/W	0h	Sets the channel for the system interrupt 15
23-20	RESERVED	R	0h	Reserved
19-16	CH_MAP_14	R/W	0h	Sets the channel for the system interrupt 14
15-12	RESERVED	R	0h	Reserved
11-8	CH_MAP_13	R/W	0h	Sets the channel for the system interrupt 13
7-4	RESERVED	R	0h	Reserved
3-0	CH_MAP_12	R/W	0h	Sets the channel for the system interrupt 12

4.5.5.24 PRU_ICSS_INTC_CMR_4 Register (Offset = 410h) [reset = 0h]

PRU_ICSS_INTC_CMR_4 is shown in Figure 4-123 and described in Table 4-272.

The Channel Map Register4 specify the channel for the system interrupts 16 to 19. There is one register per 4 system interrupts.

Table 4-271. PRU_ICSS_INTC_CMR_4 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0410h

Figure 4-123. PRU_ICSS_INTC_CMR_4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_19				RESERVED				CH_MAP_18			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_17				RESERVED				CH_MAP_16			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-272. PRU_ICSS_INTC_CMR_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	CH_MAP_19	R/W	0h	Sets the channel for the system interrupt 19
23-20	RESERVED	R	0h	Reserved
19-16	CH_MAP_18	R/W	0h	Sets the channel for the system interrupt 18
15-12	RESERVED	R	0h	Reserved
11-8	CH_MAP_17	R/W	0h	Sets the channel for the system interrupt 17
7-4	RESERVED	R	0h	Reserved
3-0	CH_MAP_16	R/W	0h	Sets the channel for the system interrupt 16

4.5.5.25 PRU_ICSS_INTC_CMR_5 Register (Offset = 414h) [reset = 0h]

PRU_ICSS_INTC_CMR_5 is shown in Figure 4-124 and described in Table 4-274.

The Channel Map Register5 specify the channel for the system interrupts 20 to 23. There is one register per 4 system interrupts.

Table 4-273. PRU_ICSS_INTC_CMR_5 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0414h

Figure 4-124. PRU_ICSS_INTC_CMR_5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_23				RESERVED				CH_MAP_22			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_21				RESERVED				CH_MAP_20			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-274. PRU_ICSS_INTC_CMR_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	CH_MAP_23	R/W	0h	Sets the channel for the system interrupt 23
23-20	RESERVED	R	0h	Reserved
19-16	CH_MAP_22	R/W	0h	Sets the channel for the system interrupt 22
15-12	RESERVED	R	0h	Reserved
11-8	CH_MAP_21	R/W	0h	Sets the channel for the system interrupt 21
7-4	RESERVED	R	0h	Reserved
3-0	CH_MAP_20	R/W	0h	Sets the channel for the system interrupt 20

4.5.5.26 PRU_ICSS_INTC_CMR_6 Register (Offset = 418h) [reset = 0h]

PRU_ICSS_INTC_CMR_6 is shown in Figure 4-125 and described in Table 4-276.

The Channel Map Register6 specify the channel for the system interrupts 24 to 27. There is one register per 4 system interrupts.

Table 4-275. PRU_ICSS_INTC_CMR_6 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0418h

Figure 4-125. PRU_ICSS_INTC_CMR_6 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_27				RESERVED				CH_MAP_26			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_25				RESERVED				CH_MAP_24			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-276. PRU_ICSS_INTC_CMR_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	CH_MAP_27	R/W	0h	Sets the channel for the system interrupt 27
23-20	RESERVED	R	0h	Reserved
19-16	CH_MAP_26	R/W	0h	Sets the channel for the system interrupt 26
15-12	RESERVED	R	0h	Reserved
11-8	CH_MAP_25	R/W	0h	Sets the channel for the system interrupt 25
7-4	RESERVED	R	0h	Reserved
3-0	CH_MAP_24	R/W	0h	Sets the channel for the system interrupt 24

4.5.5.27 PRU_ICSS_INTC_CMR_7 Register (Offset = 41Ch) [reset = 0h]

PRU_ICSS_INTC_CMR_7 is shown in Figure 4-126 and described in Table 4-278.

The Channel Map Register7 specify the channel for the system interrupts 28 to 31. There is one register per 4 system interrupts.

Table 4-277. PRU_ICSS_INTC_CMR_7 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 041Ch

Figure 4-126. PRU_ICSS_INTC_CMR_7 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_31				RESERVED				CH_MAP_30			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_29				RESERVED				CH_MAP_28			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-278. PRU_ICSS_INTC_CMR_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	CH_MAP_31	R/W	0h	Sets the channel for the system interrupt 31
23-20	RESERVED	R	0h	Reserved
19-16	CH_MAP_30	R/W	0h	Sets the channel for the system interrupt 30
15-12	RESERVED	R	0h	Reserved
11-8	CH_MAP_29	R/W	0h	Sets the channel for the system interrupt 29
7-4	RESERVED	R	0h	Reserved
3-0	CH_MAP_28	R/W	0h	Sets the channel for the system interrupt 28

4.5.5.28 PRU_ICSS_INTC_CMR_8 Register (Offset = 420h) [reset = 0h]

PRU_ICSS_INTC_CMR_8 is shown in Figure 4-127 and described in Table 4-280.

The Channel Map Register8 specify the channel for the system interrupts 32 to 35. There is one register per 4 system interrupts.

Table 4-279. PRU_ICSS_INTC_CMR_8 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0420h

Figure 4-127. PRU_ICSS_INTC_CMR_8 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_35				RESERVED				CH_MAP_34			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_33				RESERVED				CH_MAP_32			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-280. PRU_ICSS_INTC_CMR_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	CH_MAP_35	R/W	0h	Sets the channel for the system interrupt 35
23-20	RESERVED	R	0h	Reserved
19-16	CH_MAP_34	R/W	0h	Sets the channel for the system interrupt 34
15-12	RESERVED	R	0h	Reserved
11-8	CH_MAP_33	R/W	0h	Sets the channel for the system interrupt 33
7-4	RESERVED	R	0h	Reserved
3-0	CH_MAP_32	R/W	0h	Sets the channel for the system interrupt 32

4.5.5.29 PRU_ICSS_INTC_CMR_9 Register (Offset = 424h) [reset = 0h]

PRU_ICSS_INTC_CMR_9 is shown in Figure 4-128 and described in Table 4-282.

The Channel Map Register9 specify the channel for the system interrupts 36 to 39. There is one register per 4 system interrupts.

Table 4-281. PRU_ICSS_INTC_CMR_9 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0424h

Figure 4-128. PRU_ICSS_INTC_CMR_9 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_39				RESERVED				CH_MAP_38			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_37				RESERVED				CH_MAP_36			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-282. PRU_ICSS_INTC_CMR_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	CH_MAP_39	R/W	0h	Sets the channel for the system interrupt 39
23-20	RESERVED	R	0h	Reserved
19-16	CH_MAP_38	R/W	0h	Sets the channel for the system interrupt 38
15-12	RESERVED	R	0h	Reserved
11-8	CH_MAP_37	R/W	0h	Sets the channel for the system interrupt 37
7-4	RESERVED	R	0h	Reserved
3-0	CH_MAP_36	R/W	0h	Sets the channel for the system interrupt 36

4.5.5.30 PRU_ICSS_INTC_CMR_10 Register (Offset = 428h) [reset = 0h]

PRU_ICSS_INTC_CMR_10 is shown in Figure 4-129 and described in Table 4-284.

The Channel Map Register10 specify the channel for the system interrupts 40 to 43. There is one register per 4 system interrupts.

Table 4-283. PRU_ICSS_INTC_CMR_10 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0428h

Figure 4-129. PRU_ICSS_INTC_CMR_10 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_43				RESERVED				CH_MAP_42			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_41				RESERVED				CH_MAP_40			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-284. PRU_ICSS_INTC_CMR_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	CH_MAP_43	R/W	0h	Sets the channel for the system interrupt 43
23-20	RESERVED	R	0h	Reserved
19-16	CH_MAP_42	R/W	0h	Sets the channel for the system interrupt 42
15-12	RESERVED	R	0h	Reserved
11-8	CH_MAP_41	R/W	0h	Sets the channel for the system interrupt 41
7-4	RESERVED	R	0h	Reserved
3-0	CH_MAP_40	R/W	0h	Sets the channel for the system interrupt 40

4.5.5.31 PRU_ICSS_INTC_CMR_11 Register (Offset = 42Ch) [reset = 0h]

PRU_ICSS_INTC_CMR_11 is shown in Figure 4-130 and described in Table 4-286.

The Channel Map Register11 specify the channel for the system interrupts 44 to 47. There is one register per 4 system interrupts.

Table 4-285. PRU_ICSS_INTC_CMR_11 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 042Ch

Figure 4-130. PRU_ICSS_INTC_CMR_11 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_47				RESERVED				CH_MAP_46			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_45				RESERVED				CH_MAP_44			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-286. PRU_ICSS_INTC_CMR_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	CH_MAP_47	R/W	0h	Sets the channel for the system interrupt 47
23-20	RESERVED	R	0h	Reserved
19-16	CH_MAP_46	R/W	0h	Sets the channel for the system interrupt 46
15-12	RESERVED	R	0h	Reserved
11-8	CH_MAP_45	R/W	0h	Sets the channel for the system interrupt 45
7-4	RESERVED	R	0h	Reserved
3-0	CH_MAP_44	R/W	0h	Sets the channel for the system interrupt 44

4.5.5.32 PRU_ICSS_INTC_CMR_12 Register (Offset = 430h) [reset = 0h]

PRU_ICSS_INTC_CMR_12 is shown in Figure 4-131 and described in Table 4-288.

The Channel Map Register12 specify the channel for the system interrupts 48 to 51. There is one register per 4 system interrupts.

Table 4-287. PRU_ICSS_INTC_CMR_12 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0430h

Figure 4-131. PRU_ICSS_INTC_CMR_12 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_51				RESERVED				CH_MAP_50			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_49				RESERVED				CH_MAP_48			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-288. PRU_ICSS_INTC_CMR_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	CH_MAP_51	R/W	0h	Sets the channel for the system interrupt 51
23-20	RESERVED	R	0h	Reserved
19-16	CH_MAP_50	R/W	0h	Sets the channel for the system interrupt 50
15-12	RESERVED	R	0h	Reserved
11-8	CH_MAP_49	R/W	0h	Sets the channel for the system interrupt 49
7-4	RESERVED	R	0h	Reserved
3-0	CH_MAP_48	R/W	0h	Sets the channel for the system interrupt 48

4.5.5.33 PRU_ICSS_INTC_CMR_13 Register (Offset = 434h) [reset = 0h]

PRU_ICSS_INTC_CMR_13 is shown in Figure 4-132 and described in Table 4-290.

The Channel Map Register13 specify the channel for the system interrupts 52 to 55. There is one register per 4 system interrupts.

Table 4-289. PRU_ICSS_INTC_CMR_13 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0434h

Figure 4-132. PRU_ICSS_INTC_CMR_13 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_55				RESERVED				CH_MAP_54			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_53				RESERVED				CH_MAP_52			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-290. PRU_ICSS_INTC_CMR_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	CH_MAP_55	R/W	0h	Sets the channel for the system interrupt 55
23-20	RESERVED	R	0h	Reserved
19-16	CH_MAP_54	R/W	0h	Sets the channel for the system interrupt 54
15-12	RESERVED	R	0h	Reserved
11-8	CH_MAP_53	R/W	0h	Sets the channel for the system interrupt 53
7-4	RESERVED	R	0h	Reserved
3-0	CH_MAP_52	R/W	0h	Sets the channel for the system interrupt 52

4.5.5.34 PRU_ICSS_INTC_CMR_14 Register (Offset = 438h) [reset = 0h]

PRU_ICSS_INTC_CMR_14 is shown in Figure 4-133 and described in Table 4-292.

The Channel Map Register14 specify the channel for the system interrupts 56 to 59. There is one register per 4 system interrupts.

Table 4-291. PRU_ICSS_INTC_CMR_14 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0438h

Figure 4-133. PRU_ICSS_INTC_CMR_14 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_59				RESERVED				CH_MAP_58			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_57				RESERVED				CH_MAP_56			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-292. PRU_ICSS_INTC_CMR_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	CH_MAP_59	R/W	0h	Sets the channel for the system interrupt 59
23-20	RESERVED	R	0h	Reserved
19-16	CH_MAP_58	R/W	0h	Sets the channel for the system interrupt 58
15-12	RESERVED	R	0h	Reserved
11-8	CH_MAP_57	R/W	0h	Sets the channel for the system interrupt 57
7-4	RESERVED	R	0h	Reserved
3-0	CH_MAP_56	R/W	0h	Sets the channel for the system interrupt 56

4.5.5.35 PRU_ICSS_INTC_CMR_15 Register (Offset = 43Ch) [reset = 0h]

PRU_ICSS_INTC_CMR_15 is shown in Figure 4-134 and described in Table 4-294.

The Channel Map Register15 specify the channel for the system interrupts 60 to 63. There is one register per 4 system interrupts.

Table 4-293. PRU_ICSS_INTC_CMR_15 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 043Ch

Figure 4-134. PRU_ICSS_INTC_CMR_15 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_63				RESERVED				CH_MAP_62			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_61				RESERVED				CH_MAP_60			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-294. PRU_ICSS_INTC_CMR_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	CH_MAP_63	R/W	0h	Sets the channel for the system interrupt 63
23-20	RESERVED	R	0h	Reserved
19-16	CH_MAP_62	R/W	0h	Sets the channel for the system interrupt 62
15-12	RESERVED	R	0h	Reserved
11-8	CH_MAP_61	R/W	0h	Sets the channel for the system interrupt 61
7-4	RESERVED	R	0h	Reserved
3-0	CH_MAP_60	R/W	0h	Sets the channel for the system interrupt 60

4.5.5.36 PRU_ICSS_INTC_HMR0 Register (Offset = 800h) [reset = 0h]

PRU_ICSS_INTC_HMR0 is shown in Figure 4-135 and described in Table 4-296.

The Host Interrupt Map Register0 define the host interrupt for channels 0 to 3. There is one register per 4 channels. Channels with forced host interrupt mappings will have their fields read-only.

Table 4-295. PRU_ICSS_INTC_HMR0 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0800h

Figure 4-135. PRU_ICSS_INTC_HMR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				HINT_MAP_3				RESERVED				HINT_MAP_2			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				HINT_MAP_1				RESERVED				HINT_MAP_0			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-296. PRU_ICSS_INTC_HMR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	HINT_MAP_3	R/W	0h	HOST INTERRUPT MAP FOR CHANNEL 3
23-20	RESERVED	R	0h	Reserved
19-16	HINT_MAP_2	R/W	0h	HOST INTERRUPT MAP FOR CHANNEL 2
15-12	RESERVED	R	0h	Reserved
11-8	HINT_MAP_1	R/W	0h	HOST INTERRUPT MAP FOR CHANNEL 1
7-4	RESERVED	R	0h	Reserved
3-0	HINT_MAP_0	R/W	0h	HOST INTERRUPT MAP FOR CHANNEL 0

4.5.5.37 PRU_ICSS_INTC_HMR1 Register (Offset = 804h) [reset = 0h]

PRU_ICSS_INTC_HMR1 is shown in Figure 4-136 and described in Table 4-298.

The Host Interrupt Map Register1 define the host interrupt for channels 4 to 7. There is one register per 4 channels. Channels with forced host interrupt mappings will have their fields read-only.

Table 4-297. PRU_ICSS_INTC_HMR1 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0804h

Figure 4-136. PRU_ICSS_INTC_HMR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				HINT_MAP_7				RESERVED				HINT_MAP_6			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				HINT_MAP_5				RESERVED				HINT_MAP_4			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-298. PRU_ICSS_INTC_HMR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	HINT_MAP_7	R/W	0h	HOST INTERRUPT MAP FOR CHANNEL 7
23-20	RESERVED	R	0h	Reserved
19-16	HINT_MAP_6	R/W	0h	HOST INTERRUPT MAP FOR CHANNEL 6
15-12	RESERVED	R	0h	Reserved
11-8	HINT_MAP_5	R/W	0h	HOST INTERRUPT MAP FOR CHANNEL 5
7-4	RESERVED	R	0h	Reserved
3-0	HINT_MAP_4	R/W	0h	HOST INTERRUPT MAP FOR CHANNEL 4

4.5.5.38 PRU_ICSS_INTC_HMR2 Register (Offset = 808h) [reset = 0h]

PRU_ICSS_INTC_HMR2 is shown in Figure 4-137 and described in Table 4-300.

The Host Interrupt Map Register2 define the host interrupt for channels 8 to 9. There is one register per 4 channels. Channels with forced host interrupt mappings will have their fields read-only.

Table 4-299. PRU_ICSS_INTC_HMR2 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0808h

Figure 4-137. PRU_ICSS_INTC_HMR2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				HINT_MAP_9				RESERVED				HINT_MAP_8			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-300. PRU_ICSS_INTC_HMR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-8	HINT_MAP_9	R/W	0h	HOST INTERRUPT MAP FOR CHANNEL 9
7-4	RESERVED	R	0h	Reserved
3-0	HINT_MAP_8	R/W	0h	HOST INTERRUPT MAP FOR CHANNEL 8

4.5.5.39 PRU_ICSS_INTC_HIPIR_0 Register (Offset = 900h) [reset = 80000000h]

PRU_ICSS_INTC_HIPIR is shown in Figure 4-138 and described in Table 4-302.

The Host Interrupt Prioritized Index Register_j (where j=0 to 9) shows the highest priority current pending interrupt for the host interrupt j. There is one register per host interrupt.

Table 4-301. PRU_ICSS_INTC_HIPIR_0 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0900h

Figure 4-138. PRU_ICSS_INTC_HIPIR_0 Register

31	30	29	28	27	26	25	24
NONE_HINT	RESERVED						
R-1h	R-0000 00h						
23	22	21	20	19	18	17	16
RESERVED							
R-0000 00h							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT	
R-0000 00h						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT							
R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 4-302. PRU_ICSS_INTC_HIPIR_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT	R	1h	No pending interrupt.
30-10	RESERVED	R	0000 00h	Reserved
9-0	PRI_HINT	R	0h	HOST INT j PRIORITIZED INTERRUPT. Interrupt number of the highest priority pending interrupt for this host interrupt.

4.5.5.40 PRU_ICSS_INTC_HIPIR_1 Register (Offset = 904h) [reset = 80000000h]

PRU_ICSS_INTC_HIPIR_1 is shown in Figure 4-139 and described in Table 4-304.

The Host Interrupt Prioritized Index Register_j (where j=0 to 9) shows the highest priority current pending interrupt for the host interrupt j. There is one register per host interrupt.

Table 4-303. PRU_ICSS_INTC_HIPIR_1 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0904h

Figure 4-139. PRU_ICSS_INTC_HIPIR_1 Register

31	30	29	28	27	26	25	24
NONE_HINT	RESERVED						
R-1h	R-0000 00h						
23	22	21	20	19	18	17	16
RESERVED							
R-0000 00h							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT	
R-0000 00h						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT							
R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 4-304. PRU_ICSS_INTC_HIPIR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT	R	1h	No pending interrupt.
30-10	RESERVED	R	0000 00h	Reserved
9-0	PRI_HINT	R	0h	HOST INT j PRIORITIZED INTERRUPT. Interrupt number of the highest priority pending interrupt for this host interrupt.

4.5.5.41 PRU_ICSS_INTC_HIPIR_2 Register (Offset = 908h) [reset = 80000000h]

PRU_ICSS_INTC_HIPIR_2 is shown in Figure 4-140 and described in Table 4-306.

The Host Interrupt Prioritized Index Register_j (where j=0 to 9) shows the highest priority current pending interrupt for the host interrupt j. There is one register per host interrupt.

Table 4-305. PRU_ICSS_INTC_HIPIR_2 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0908h

Figure 4-140. PRU_ICSS_INTC_HIPIR_2 Register

31	30	29	28	27	26	25	24
NONE_HINT	RESERVED						
R-1h	R-0000 00h						
23	22	21	20	19	18	17	16
RESERVED							
R-0000 00h							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT	
R-0000 00h						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT							
R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 4-306. PRU_ICSS_INTC_HIPIR_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT	R	1h	No pending interrupt.
30-10	RESERVED	R	0000 00h	Reserved
9-0	PRI_HINT	R	0h	HOST INT j PRIORITIZED INTERRUPT. Interrupt number of the highest priority pending interrupt for this host interrupt.

4.5.5.42 PRU_ICSS_INTC_HIPIR_3 Register (Offset = 90Ch) [reset = 80000000h]

PRU_ICSS_INTC_HIPIR_3 is shown in Figure 4-141 and described in Table 4-308.

The Host Interrupt Prioritized Index Register_j (where j=0 to 9) shows the highest priority current pending interrupt for the host interrupt j. There is one register per host interrupt.

Table 4-307. PRU_ICSS_INTC_HIPIR_3 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 090Ch

Figure 4-141. PRU_ICSS_INTC_HIPIR_3 Register

31	30	29	28	27	26	25	24
NONE_HINT	RESERVED						
R-1h	R-0000 00h						
23	22	21	20	19	18	17	16
RESERVED							
R-0000 00h							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT	
R-0000 00h						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT							
R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 4-308. PRU_ICSS_INTC_HIPIR_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT	R	1h	No pending interrupt.
30-10	RESERVED	R	0000 00h	Reserved
9-0	PRI_HINT	R	0h	HOST INT j PRIORITIZED INTERRUPT. Interrupt number of the highest priority pending interrupt for this host interrupt.

4.5.5.43 PRU_ICSS_INTC_HIPIR_4 Register (Offset = 910h) [reset = 80000000h]

PRU_ICSS_INTC_HIPIR_4 is shown in Figure 4-142 and described in Table 4-310.

The Host Interrupt Prioritized Index Register_j (where j=0 to 9) shows the highest priority current pending interrupt for the host interrupt j. There is one register per host interrupt.

Table 4-309. PRU_ICSS_INTC_HIPIR_4 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0910h

Figure 4-142. PRU_ICSS_INTC_HIPIR_4 Register

31	30	29	28	27	26	25	24
NONE_HINT	RESERVED						
R-1h	R-0000 00h						
23	22	21	20	19	18	17	16
RESERVED							
R-0000 00h							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT	
R-0000 00h						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT							
R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 4-310. PRU_ICSS_INTC_HIPIR_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT	R	1h	No pending interrupt.
30-10	RESERVED	R	0000 00h	Reserved
9-0	PRI_HINT	R	0h	HOST INT j PRIORITIZED INTERRUPT. Interrupt number of the highest priority pending interrupt for this host interrupt.

4.5.5.44 PRU_ICSS_INTC_HIPIR_5 Register (Offset = 914h) [reset = 80000000h]

PRU_ICSS_INTC_HIPIR_5 is shown in Figure 4-143 and described in Table 4-312.

The Host Interrupt Prioritized Index Register_j (where j=0 to 9) shows the highest priority current pending interrupt for the host interrupt j. There is one register per host interrupt.

Table 4-311. PRU_ICSS_INTC_HIPIR_5 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0914h

Figure 4-143. PRU_ICSS_INTC_HIPIR_5 Register

31	30	29	28	27	26	25	24
NONE_HINT	RESERVED						
R-1h	R-0000 00h						
23	22	21	20	19	18	17	16
RESERVED							
R-0000 00h							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT	
R-0000 00h						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT							
R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 4-312. PRU_ICSS_INTC_HIPIR_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT	R	1h	No pending interrupt.
30-10	RESERVED	R	0000 00h	Reserved
9-0	PRI_HINT	R	0h	HOST INT j PRIORITIZED INTERRUPT. Interrupt number of the highest priority pending interrupt for this host interrupt.

4.5.5.45 PRU_ICSS_INTC_HIPIR_6 Register (Offset = 918h) [reset = 80000000h]

PRU_ICSS_INTC_HIPIR_6 is shown in Figure 4-144 and described in Table 4-314.

The Host Interrupt Prioritized Index Register_j (where j=0 to 9) shows the highest priority current pending interrupt for the host interrupt j. There is one register per host interrupt.

Table 4-313. PRU_ICSS_INTC_HIPIR_6 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0918h

Figure 4-144. PRU_ICSS_INTC_HIPIR_6 Register

31	30	29	28	27	26	25	24
NONE_HINT	RESERVED						
R-1h	R-0000 00h						
23	22	21	20	19	18	17	16
RESERVED							
R-0000 00h							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT	
R-0000 00h						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT							
R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 4-314. PRU_ICSS_INTC_HIPIR_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT	R	1h	No pending interrupt.
30-10	RESERVED	R	0000 00h	Reserved
9-0	PRI_HINT	R	0h	HOST INT j PRIORITIZED INTERRUPT. Interrupt number of the highest priority pending interrupt for this host interrupt.

4.5.5.46 PRU_ICSS_INTC_HIPIR_7 Register (Offset = 91Ch) [reset = 80000000h]

PRU_ICSS_INTC_HIPIR_7 is shown in Figure 4-145 and described in Table 4-316.

The Host Interrupt Prioritized Index Register_j (where j=0 to 9) shows the highest priority current pending interrupt for the host interrupt j. There is one register per host interrupt.

Table 4-315. PRU_ICSS_INTC_HIPIR_7 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 091Ch

Figure 4-145. PRU_ICSS_INTC_HIPIR_7 Register

31	30	29	28	27	26	25	24
NONE_HINT	RESERVED						
R-1h	R-0000 00h						
23	22	21	20	19	18	17	16
RESERVED							
R-0000 00h							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT	
R-0000 00h						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT							
R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 4-316. PRU_ICSS_INTC_HIPIR_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT	R	1h	No pending interrupt.
30-10	RESERVED	R	0000 00h	Reserved
9-0	PRI_HINT	R	0h	HOST INT j PRIORITIZED INTERRUPT. Interrupt number of the highest priority pending interrupt for this host interrupt.

4.5.5.47 PRU_ICSS_INTC_HIPIR_8 Register (Offset = 920h) [reset = 80000000h]

PRU_ICSS_INTC_HIPIR_8 is shown in Figure 4-146 and described in Table 4-318.

The Host Interrupt Prioritized Index Register_j (where j=0 to 9) shows the highest priority current pending interrupt for the host interrupt j. There is one register per host interrupt.

Table 4-317. PRU_ICSS_INTC_HIPIR_8 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0920h

Figure 4-146. PRU_ICSS_INTC_HIPIR_8 Register

31	30	29	28	27	26	25	24
NONE_HINT	RESERVED						
R-1h	R-0000 00h						
23	22	21	20	19	18	17	16
RESERVED							
R-0000 00h							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT	
R-0000 00h						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT							
R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 4-318. PRU_ICSS_INTC_HIPIR_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT	R	1h	No pending interrupt.
30-10	RESERVED	R	0000 00h	Reserved
9-0	PRI_HINT	R	0h	HOST INT j PRIORITIZED INTERRUPT. Interrupt number of the highest priority pending interrupt for this host interrupt.

4.5.5.48 PRU_ICSS_INTC_HIPIR_9 Register (Offset = 924h) [reset = 80000000h]

PRU_ICS_INTC_HIPIR_9 is shown in Figure 4-147 and described in Table 4-320.

The Host Interrupt Prioritized Index Register_j (where j=0 to 9) shows the highest priority current pending interrupt for the host interrupt j. There is one register per host interrupt.

Table 4-319. PRU_ICSS_INTC_HIPIR_9 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0924h

Figure 4-147. PRU_ICSS_INTC_HIPIR_9 Register

31	30	29	28	27	26	25	24
NONE_HINT	RESERVED						
R-1h	R-0000 00h						
23	22	21	20	19	18	17	16
RESERVED							
R-0000 00h							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT	
R-0000 00h						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT							
R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 4-320. PRU_ICSS_INTC_HIPIR_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT	R	1h	No pending interrupt.
30-10	RESERVED	R	0000 00h	Reserved
9-0	PRI_HINT	R	0h	HOST INT j PRIORITIZED INTERRUPT. Interrupt number of the highest priority pending interrupt for this host interrupt.

4.5.5.49 PRU_ICSS_INTC_SIPR0 Register (Offset = D00h) [reset = 1h]

PRU_ICSS_INTC_SIPR0 is shown in Figure 4-148 and described in Table 4-322.

The System Interrupt Polarity Register0 define the polarity of the system interrupts 0 to 31. There is a polarity for each system interrupt. The polarity of all system interrupts is active high; always write 1 to the bits of this register.

Table 4-321. PRU_ICSS_INTC_SIPR0 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0D00h

Figure 4-148. PRU_ICSS_INTC_SIPR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POLARITY_31_0																															
R/W-1h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-322. PRU_ICSS_INTC_SIPR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	POLARITY_31_0	R/W	1h	Interrupt polarity of the system interrupts 0 to 31. 0h: Active low. 1h: Active high.

4.5.5.50 PRU_ICSS_INTC_SIPR1 Register (Offset = D04h) [reset = 1h]

PRU_ICSS_INTC_SIPR1 is shown in Figure 4-149 and described in Table 4-324.

The System Interrupt Polarity Register1 define the polarity of the system interrupts 32 to 63. There is a polarity for each system interrupt. The polarity of all system interrupts is active high; always write 1 to the bits of this register.

Table 4-323. PRU_ICSS_INTC_SIPR1 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0D04h

Figure 4-149. PRU_ICSS_INTC_SIPR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POLARITY_63_32																															
R/W-1h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-324. PRU_ICSS_INTC_SIPR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	POLARITY_63_32	R/W	1h	Interrupt polarity of the system interrupts 32 to 63. 0h: Active low. 1h: Active high.

4.5.5.51 PRU_ICSS_INTC_SITR0 Register (Offset = D80h) [reset = 0h]

PRU_ICSS_INTC_SITR0 is shown in Figure 4-150 and described in Table 4-326.

The System Interrupt Type Register0 define the type of the system interrupts 0 to 31. There is a type for each system interrupt. The type of all system interrupts is pulse; always write 0 to the bits of this register.

Table 4-325. PRU_ICSS_INTC_SITR0 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0D80h

Figure 4-150. PRU_ICSS_INTC_SITR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TYPE_31_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-326. PRU_ICSS_INTC_SITR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TYPE_31_0	R/W	0h	Interrupt type of the system interrupts 0 to 31. 0h: Level or pulse interrupt. 1h: Edge interrupt (required edge detect).

4.5.5.52 PRU_ICSS_INTC_SITR1 Register (Offset = D84h) [reset = 0h]

PRU_ICSS_INTC_SITR1 is shown in Figure 4-151 and described in Table 4-328.

The System Interrupt Type Register1 define the type of the system interrupts 32 to 63. There is a type for each system interrupt. The type of all system interrupts is pulse; always write 0 to the bits of this register.

Table 4-327. PRU_ICSS_INTC_SITR1 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0D84h

Figure 4-151. PRU_ICSS_INTC_SITR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TYPE_63_32																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-328. PRU_ICSS_INTC_SITR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TYPE_63_32	R/W	0h	Interrupt type of the system interrupts 32 to 63. 0h Level or pulse interrupt. 1h: Edge interrupt (required edge detect).

4.5.5.53 PRU_ICSS_INTC_HINLR_0 Register (Offset = 1100h) [reset = 100h]

PRU_ICSS_INTC_HINLR_0 is shown in Figure 4-152 and described in Table 4-330.

The Host Interrupt Nesting Level Register_j (where j=0 to 9) display and control the nesting level for host interrupt j. The nesting level controls which channel and lower priority channels are nested. There is one register per host interrupt.

Table 4-329. PRU_ICSS_INTC_HINLR_0 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 1100h

Figure 4-152. PRU_ICSS_INTC_HINLR_0 Register

31	30	29	28	27	26	25	24
AUTO_OVERRIDE	RESERVED						
W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT
R-0h							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT							
R/W-100h							

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; *-n* = value after reset

Table 4-330. PRU_ICSS_INTC_HINLR_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AUTO_OVERRIDE	W	0h	Reads return 0. Writes of a 1 override the auto updating of the nesting_level and use the write data.
30-9	RESERVED	R	0h	Reserved
8-0	NEST_HINT	R/W	100h	Reads return the current nesting level for the host interrupt. Writes set the nesting level for the host interrupt. In auto mode the value is updated internally unless the auto_override is set and then the write data is used.

4.5.5.54 PRU_ICSS_INTC_HINLR_1 Register (Offset = 1104h) [reset = 100h]

PRU_ICSS_INTC_HINLR_1 is shown in Figure 4-153 and described in Table 4-332.

The Host Interrupt Nesting Level Register_j (where j=0 to 9) display and control the nesting level for host interrupt j. The nesting level controls which channel and lower priority channels are nested. There is one register per host interrupt.

Table 4-331. PRU_ICSS_INTC_HINLR_1 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 1104h

Figure 4-153. PRU_ICSS_INTC_HINLR_1 Register

31	30	29	28	27	26	25	24
AUTO_OVERRIDE	RESERVED						
W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT
R-0h							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT							
R/W-100h							

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; *-n* = value after reset

Table 4-332. PRU_ICSS_INTC_HINLR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AUTO_OVERRIDE	W	0h	Reads return 0. Writes of a 1 override the auto updating of the nesting_level and use the write data.
30-9	RESERVED	R	0h	Reserved
8-0	NEST_HINT	R/W	100h	Reads return the current nesting level for the host interrupt. Writes set the nesting level for the host interrupt. In auto mode the value is updated internally unless the auto_override is set and then the write data is used.

4.5.5.55 PRU_ICSS_INTC_HINLR_2 Register (Offset = 1108h) [reset = 100h]

PRU_ICSS_INTC_HINLR_2 is shown in Figure 4-154 and described in Table 4-334.

The Host Interrupt Nesting Level Register_j (where j=0 to 9) display and control the nesting level for host interrupt j. The nesting level controls which channel and lower priority channels are nested. There is one register per host interrupt.

Table 4-333. PRU_ICSS_INTC_HINLR_2 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 1108h

Figure 4-154. PRU_ICSS_INTC_HINLR_2 Register

31	30	29	28	27	26	25	24
AUTO_OVERRIDE	RESERVED						
W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT
R-0h							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT							
R/W-100h							

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; *-n* = value after reset

Table 4-334. PRU_ICSS_INTC_HINLR_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AUTO_OVERRIDE	W	0h	Reads return 0. Writes of a 1 override the auto updating of the nesting_level and use the write data.
30-9	RESERVED	R	0h	Reserved
8-0	NEST_HINT	R/W	100h	Reads return the current nesting level for the host interrupt. Writes set the nesting level for the host interrupt. In auto mode the value is updated internally unless the auto_override is set and then the write data is used.

4.5.5.56 PRU_ICSS_INTC_HINLR_3 Register (Offset = 110Ch) [reset = 100h]

PRU_ICSS_INTC_HINLR_3 is shown in Figure 4-155 and described in Table 4-336.

The Host Interrupt Nesting Level Register_j (where j=0 to 9) display and control the nesting level for host interrupt j. The nesting level controls which channel and lower priority channels are nested. There is one register per host interrupt.

Table 4-335. PRU_ICSS_INTC_HINLR_3 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 110Ch

Figure 4-155. PRU_ICSS_INTC_HINLR_3 Register

31	30	29	28	27	26	25	24
AUTO_OVERRIDE	RESERVED						
W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT
R-0h							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT							
R/W-100h							

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; *-n* = value after reset

Table 4-336. PRU_ICSS_INTC_HINLR_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AUTO_OVERRIDE	W	0h	Reads return 0. Writes of a 1 override the auto updating of the nesting_level and use the write data.
30-9	RESERVED	R	0h	Reserved
8-0	NEST_HINT	R/W	100h	Reads return the current nesting level for the host interrupt. Writes set the nesting level for the host interrupt. In auto mode the value is updated internally unless the auto_override is set and then the write data is used.

4.5.5.57 PRU_ICSS_INTC_HINLR_4 Register (Offset = 1110h) [reset = 100h]

PRU_ICSS_INTC_HINLR_4 is shown in Figure 4-156 and described in Table 4-338.

The Host Interrupt Nesting Level Register_j (where j=0 to 9) display and control the nesting level for host interrupt j. The nesting level controls which channel and lower priority channels are nested. There is one register per host interrupt.

Table 4-337. PRU_ICSS_INTC_HINLR_4 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 1110h

Figure 4-156. PRU_ICSS_INTC_HINLR_4 Register

31	30	29	28	27	26	25	24
AUTO_OVERRIDE	RESERVED						
W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT
R-0h							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT							
R/W-100h							

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; *-n* = value after reset

Table 4-338. PRU_ICSS_INTC_HINLR_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AUTO_OVERRIDE	W	0h	Reads return 0. Writes of a 1 override the auto updating of the nesting_level and use the write data.
30-9	RESERVED	R	0h	Reserved
8-0	NEST_HINT	R/W	100h	Reads return the current nesting level for the host interrupt. Writes set the nesting level for the host interrupt. In auto mode the value is updated internally unless the auto_override is set and then the write data is used.

4.5.5.58 PRU_ICSS_INTC_HINLR_5 Register (Offset = 1114h) [reset = 100h]

PRU_ICSS_INTC_HINLR_5 is shown in Figure 4-157 and described in Table 4-340.

The Host Interrupt Nesting Level Register_j (where j=0 to 9) display and control the nesting level for host interrupt j. The nesting level controls which channel and lower priority channels are nested. There is one register per host interrupt.

Table 4-339. PRU_ICSS_INTC_HINLR_5 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 1114h

Figure 4-157. PRU_ICSS_INTC_HINLR_5 Register

31	30	29	28	27	26	25	24
AUTO_OVERRIDE	RESERVED						
W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT
R-0h							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT							
R/W-100h							

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; *-n* = value after reset

Table 4-340. PRU_ICSS_INTC_HINLR_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AUTO_OVERRIDE	W	0h	Reads return 0. Writes of a 1 override the auto updating of the nesting_level and use the write data.
30-9	RESERVED	R	0h	Reserved
8-0	NEST_HINT	R/W	100h	Reads return the current nesting level for the host interrupt. Writes set the nesting level for the host interrupt. In auto mode the value is updated internally unless the auto_override is set and then the write data is used.

4.5.5.59 PRU_ICSS_INTC_HINLR_6 Register (Offset = 1118h) [reset = 100h]

PRU_ICSS_INTC_HINLR_6 is shown in Figure 4-158 and described in Table 4-342.

The Host Interrupt Nesting Level Register_j (where j=0 to 9) display and control the nesting level for host interrupt j. The nesting level controls which channel and lower priority channels are nested. There is one register per host interrupt.

Table 4-341. PRU_ICSS_INTC_HINLR_6 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 1118h

Figure 4-158. PRU_ICSS_INTC_HINLR_6 Register

31	30	29	28	27	26	25	24
AUTO_OVERRIDE	RESERVED						
W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT
R-0h							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT							
R/W-100h							

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; *-n* = value after reset

Table 4-342. PRU_ICSS_INTC_HINLR_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AUTO_OVERRIDE	W	0h	Reads return 0. Writes of a 1 override the auto updating of the nesting_level and use the write data.
30-9	RESERVED	R	0h	Reserved
8-0	NEST_HINT	R/W	100h	Reads return the current nesting level for the host interrupt. Writes set the nesting level for the host interrupt. In auto mode the value is updated internally unless the auto_override is set and then the write data is used.

4.5.5.60 PRU_ICSS_INTC_HINLR_7 Register (Offset = 111Ch) [reset = 100h]

PRU_ICSS_INTC_HINLR_7 is shown in Figure 4-159 and described in Table 4-344.

The Host Interrupt Nesting Level Register_j (where j=0 to 9) display and control the nesting level for host interrupt j. The nesting level controls which channel and lower priority channels are nested. There is one register per host interrupt.

Table 4-343. PRU_ICSS_INTC_HINLR_7 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 111Ch

Figure 4-159. PRU_ICSS_INTC_HINLR_7 Register

31	30	29	28	27	26	25	24
AUTO_OVERRIDE	RESERVED						
W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT
R-0h							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT							
R/W-100h							

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; *-n* = value after reset

Table 4-344. PRU_ICSS_INTC_HINLR_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AUTO_OVERRIDE	W	0h	Reads return 0. Writes of a 1 override the auto updating of the nesting_level and use the write data.
30-9	RESERVED	R	0h	Reserved
8-0	NEST_HINT	R/W	100h	Reads return the current nesting level for the host interrupt. Writes set the nesting level for the host interrupt. In auto mode the value is updated internally unless the auto_override is set and then the write data is used.

4.5.5.61 PRU_ICSS_INTC_HINLR_8 Register (Offset = 1120h) [reset = 100h]

PRU_ICSS_INTC_HINLR_8 is shown in Figure 4-160 and described in Table 4-346.

The Host Interrupt Nesting Level Register_j (where j=0 to 9) display and control the nesting level for host interrupt j. The nesting level controls which channel and lower priority channels are nested. There is one register per host interrupt.

Table 4-345. PRU_ICSS_INTC_HINLR_8 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 1120h

Figure 4-160. PRU_ICSS_INTC_HINLR_8 Register

31	30	29	28	27	26	25	24
AUTO_OVERRIDE	RESERVED						
W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT
R-0h							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT							
R/W-100h							

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; *-n* = value after reset

Table 4-346. PRU_ICSS_INTC_HINLR_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AUTO_OVERRIDE	W	0h	Reads return 0. Writes of a 1 override the auto updating of the nesting_level and use the write data.
30-9	RESERVED	R	0h	Reserved
8-0	NEST_HINT	R/W	100h	Reads return the current nesting level for the host interrupt. Writes set the nesting level for the host interrupt. In auto mode the value is updated internally unless the auto_override is set and then the write data is used.

4.5.5.62 PRU_ICSS_INTC_HINLR_9 Register (Offset = 1124h) [reset = 100h]

PRU_ICSS_INTC_HINLR_9 is shown in Figure 4-161 and described in Table 4-348.

The Host Interrupt Nesting Level Register_j (where j=0 to 9) display and control the nesting level for host interrupt j. The nesting level controls which channel and lower priority channels are nested. There is one register per host interrupt.

Table 4-347. PRU_ICSS_INTC_HINLR_9 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 1124h

Figure 4-161. PRU_ICSS_INTC_HINLR_9 Register

31	30	29	28	27	26	25	24
AUTO_OVERRIDE	RESERVED						
W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT
R-0h							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT							
R/W-100h							

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; *-n* = value after reset

Table 4-348. PRU_ICSS_INTC_HINLR_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AUTO_OVERRIDE	W	0h	Reads return 0. Writes of a 1 override the auto updating of the nesting_level and use the write data.
30-9	RESERVED	R	0h	Reserved
8-0	NEST_HINT	R/W	100h	Reads return the current nesting level for the host interrupt. Writes set the nesting level for the host interrupt. In auto mode the value is updated internally unless the auto_override is set and then the write data is used.

4.5.5.63 PRU_ICSS_INTC_HIER Register (Offset = 1500h) [reset = 0h]

PRU_ICSS_INTC_HIER is shown in Figure 4-162 and described in Table 4-350.

The Host Interrupt Enable Registers enable or disable individual host interrupts. These work separately from the global enables. There is one bit per host interrupt. These bits are updated when writing to the Host Interrupt Enable Index Set and Host Interrupt Enable Index Clear registers.

Table 4-349. PRU_ICSS_INTC_HIER Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 1500h

Figure 4-162. PRU_ICSS_INTC_HIER Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0000 00h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						ENABLE_HINT									
R-0000 00h						R/W-0h									

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-350. PRU_ICSS_INTC_HIER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0000 00h	Reserved
9-0	ENABLE_HINT	R/W	0h	The enable of the host interrupts (one per bit). 0h: Disabled 1h: Enabled

4.5.6 PRU_ICSS_UART Registers

PRU_ICSS_UART Registers lists the memory-mapped registers for the PRU-ICSS_UART module. All register offset addresses not listed in PRU_ICSS_UART Registers should be considered as reserved locations and the register contents should not be modified.

Table 4-351. PRU-ICSS_UART Instances

Instance	Base Address
PRU_ICSS_UART	4802 8000h

Table 4-352. PRU-ICSS_UART Registers

Offset	Acronym	Register Name	PRU_ICSS_UART Physical Address
0h	PRU_ICSS_UART_RBR_THR	Transmitter Holding Register	4802 8000h
4h	PRU_ICSS_UART_INTERRUPT_ENABLE	Interrupt Enable Register	4802 8004h
8h	PRU_ICSS_UART_INTERRUPT_IDENTIFICATION_FIFO_CONTROL	Interrupt Identification Register/ FIFO Control Register	4802 8008h
Ch	PRU_ICSS_UART_LINE_CONTROL	Line Control Register	4802 800Ch
10h	PRU_ICSS_UART_MODEM_CONTROL	Modem Control Register	4802 8010h
14h	PRU_ICSS_UART_LINE_STATUS	Line Status Register	4802 8014h
18h	PRU_ICSS_UART_MODEM_STATUS	Modem Status Register	4802 8018h
1Ch	PRU_ICSS_UART_SCRATCH	Scratch Register	4802 801Ch
20h	PRU_ICSS_UART_DIVISOR_LSB	Divisor Latch (LSB)	4802 8020h
24h	PRU_ICSS_UART_UART_DIVISOR_MSB	Divisor Latch (MSB)	4802 8024h
28h	PRU_ICSS_UART_PERIPHERAL_ID	Peripheral ID Register	4802 8028h
2Ch	RESERVED		4802 802Ch
30h	PRU_ICSS_UART_POWER_MANAGEMENT_AND_EMULATION	Power Management and Emulation Register	4802 8030h
34h	PRU_ICSS_UART_MODE_DEFINITION	Mode Definition Register	4802 8034h

4.5.6.1 PRU_ICSS_UART_RBR_THR Register (Offset = 0h) [reset = 0h]

PRU_ICSS_UART_RBR_THR is shown in Figure 4-163 and described in Table 4-354.

Return to Summary Table.

In the non-FIFO mode, when a character is placed in Receiver buffer register and the receiver data-ready interrupt is enabled (DR = 1 in Interrupt identification register), an interrupt is generated. This interrupt is cleared when the character is read from Receiver buffer register. In the FIFO mode, the interrupt is generated when the FIFO is filled to the trigger level selected in the FIFO control register, and it is cleared when the FIFO contents drop below the trigger level.
In the non-FIFO mode, if Transmitter holding register is empty and the THR empty (THRE) interrupt is enabled (ETBEI = 1 in Interrupt enable register), an interrupt is generated. This interrupt is cleared when a character is loaded into Transmitter holding register or the Interrupt identification register is read. In the FIFO mode, the interrupt is generated when the transmitter FIFO is empty, and it is cleared when at least one byte is loaded into the FIFO or Interrupt identification register is read.

Table 4-353. PRU_ICSS_UART_RBR_THR Instances

Instance	Physical Address
PRU_ICSS_UART	4802 8000h

Figure 4-163. PRU_ICSS_UART_RBR_THR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DATA							
R-0h																								RW-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-354. PRU_ICSS_UART_RBR_THR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	DATA	RW	0h	**Read:** Read Receive Buffer Register **Write:** Write Transmitter Holding Register

4.5.6.2 PRU_ICSS_UART_INTERRUPT_ENABLE Register (Offset = 4h) [reset = 0h]

PRU_ICSS_UART_INTERRUPT_ENABLE is shown in Figure 4-164 and described in Table 4-356.

Return to Summary Table.

The Interrupt enable register is used to individually enable or disable each type of interrupt request that can be generated by the UART. Each interrupt request that is enabled in Interrupt enable register is forwarded to the CPU.

Table 4-355.
PRU_ICSS_UART_INTERRUPT_ENABLE Instances

Instance	Physical Address
PRU_ICSS_UART	4802 8004h

Figure 4-164. PRU_ICSS_UART_INTERRUPT_ENABLE Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				EDSSI	ELSI	ETBEI	ERBI
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-356. PRU_ICSS_UART_INTERRUPT_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	EDSSI	R/W	0h	Enable Modem Status Interrupt
2	ELSI	R/W	0h	Receiver line status interrupt enable. 0h: Receiver line status interrupt is disabled. 1h: Receiver line status interrupt is enabled.
1	ETBEI	R/W	0h	Transmitter holding register empty interrupt enable. 0h: Transmitter holding register empty interrupt is disabled. 1h: Transmitter holding register empty interrupt is enabled.
0	ERBI	R/W	0h	Receiver data available interrupt and character timeout indication interrupt enable. 0h: Receiver data available interrupt and character timeout indication interrupt is disabled. 1h: Receiver data available interrupt and character timeout indication interrupt is enabled.

4.5.6.3 PRU_ICSS_UART_INTERRUPT_IDENTIFICATION_FIFO_CONTROL Register (Offset = 8h) [reset = 1h]

PRU_ICSS_UART_INTERRUPT_IDENTIFICATION_FIFO_CONTROL is shown in Figure 4-165 and described in Table 4-358.

Return to Summary Table.

The Interrupt identification register is a read-only register at the same address as the FIFO control register, which is a write-only register. When an interrupt is generated and enabled in the Interrupt enable register, Interrupt identification register indicates that an interrupt is pending in the IPEND bit and encodes the type of interrupt in the INTID bits. Reading Interrupt identification register clears any THR empty (THRE) interrupts that are pending. The FIFOEN bit in Interrupt identification register can be checked to determine whether the UART is in the FIFO mode or the non-FIFO mode.
Use FIFO control register to enable and clear the FIFOs and to select the receiver FIFO trigger level. The FIFOEN bit in FIFO control register must be set to 1 before other FIFO control register bits are written to or the FIFO control register bits are not programmed.

Table 4-357. PRU_ICSS_UART_INTERRUPT_IDENTIFICATION_FIFO_CONTROL Instances

Instance	Physical Address
PRU_ICSS_UART	4802 8008h

Figure 4-165. PRU_ICSS_UART_INTERRUPT_IDENTIFICATION_FIFO_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
FIFOEN_RXFIFTL		RESERVED		INTID			IPEND_FIFOEN
RW-0h		R-0h		RW-0h			RW-1h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-358. PRU_ICSS_UART_INTERRUPT_IDENTIFICATION_FIFO_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved

Table 4-358. PRU_ICSS_UART_INTERRUPT_IDENTIFICATION_FIFO_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	FIFOEN_RXFIFTL	RW	0h	**Read:** FIFOs enabled. 0h: Non-FIFO mode 1h-2h: Reserved 3h: FIFOs are enabled. FIFOEN bit in the FIFO control register (FCR) is set to 1.
				Write: Receiver FIFO trigger level. RXFIFTL sets the trigger level for the receiver FIFO. When the trigger level is reached, a receiver data-ready interrupt is generated (if the interrupt request is enabled). Once the FIFO drops below the trigger level, the interrupt is cleared. 0h: 1 byte 1h: 4 bytes 2h: 8 bytes 3h: 14 bytes
5-4	RESERVED	R	0h	Reserved
3-1	INTID	RW	0h	**Read:** Interrupt type. See . 0h: Reserved 1h: Transmitter holding register empty (priority 3) 2h: Receiver data available (priority 2) 3h: Receiver line status (priority 1, highest) 4h-5h: Reserved 6h: Character timeout indication (priority 2) 7h: Reserved
				Write: **Bit 3: DMAMODE1:** DMA MODE1 enable if FIFOs are enabled. Always write 1 to DMAMODE1. After a hardware reset, change DMAMODE1 from 0 to 1. DMAMODE1 = 1 is a requirement for proper communication between the UART and the EDMA controller. 0h: DMA MODE1 is disabled. 1h: DMA MODE1 is enabled. **Bit 2: TXCLR:** Transmitter FIFO clear. Write a 1 to TXCLR to clear the bit. 0h: No effect. 1h: Clears transmitter FIFO and resets the transmitter FIFO counter. The shift register is not cleared. **Bit 1: RXCLR:** Receiver FIFO clear. Write a 1 to RXCLR to clear the bit. 0h: No effect. 1h: Clears receiver FIFO and resets the receiver FIFO counter. The shift register is not cleared.
0	IPEND_FIFOEN	RW	1h	**Read:** Interrupt pending. When any UART interrupt is generated and is enabled in IER, IPEND is forced to 0. IPEND remains 0 until all pending interrupts are cleared or until a hardware reset occurs. If no interrupts are enabled, IPEND is never forced to 0. 0h: Interrupts pending. 1h: No interrupts pending.
				Write: Transmitter and receiver FIFOs mode enable. FIFOEN must be set before other FCR bits are written to or the FCR bits are not programmed. Clearing this bit clears the FIFO counters. 0h: Non-FIFO mode. The transmitter and receiver FIFOs are disabled, and the FIFO pointers are cleared. 1h: FIFO mode. The transmitter and receiver FIFOs are enabled.

4.5.6.4 PRU_ICSS_UART_LINE_CONTROL Register (Offset = Ch) [reset = 0h]

PRU_ICSS_UART_LINE_CONTROL is shown in Figure 4-166 and described in Table 4-360.

Return to Summary Table.

The system programmer controls the format of the asynchronous data communication exchange by using Line control register. In addition, the programmer can retrieve, inspect, and modify the content of line control register; this eliminates the need for separate storage of the line characteristics in system memory.

Table 4-359. PRU_ICSS_UART_LINE_CONTROL Instances

Instance	Physical Address
PRU_ICSS_UART	4802 800Ch

Figure 4-166. PRU_ICSS_UART_LINE_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
DLAB	BC	SP	EPS	PEN	STB	WLS1	WLS0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-360. PRU_ICSS_UART_LINE_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	DLAB	R/W	0h	Divisor latch access bit. The divisor latch registers (DLL and DLH) can be accessed at dedicated addresses or at addresses shared by RBR, THR, and IER. Using the shared addresses requires toggling DLAB to change which registers are selected. If you use the dedicated addresses, you can keep DLAB = 0. 0h: Allows access to the receiver buffer register (RBR), the transmitter holding register (THR), and the interrupt enable register (IER) selected. At the address shared by RBR, THR, and DLL, the CPU can read from RBR and write to THR. At the address shared by IER and DLH, the CPU can read from and write to IER. 1h: Allows access to the divisor latches of the baud generator during a read or write operation (DLL and DLH). At the address shared by RBR, THR, and DLL, the CPU can read from and write to DLL. At the address shared by IER and DLH, the CPU can read from and write to DLH.
6	BC	R/W	0h	Break Control. 0h: Break condition is disabled. 1h: Break condition is transmitted to the receiving UART. A break condition is a condition where the UARTn_TXD signal is forced to the spacing (cleared) state.

Table 4-360. PRU_ICSS_UART_LINE_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	SP	R/W	0h	Stick parity. The SP bit works in conjunction with the EPS and PEN bits. The relationship between the SP, EPS, and PEN bits is summarized in . 0h: Stick parity is disabled. 1h: Stick parity is enabled. • When odd parity is selected (EPS = 0), the PARITY bit is transmitted and checked as set. • When even parity is selected (EPS = 1), the PARITY bit is transmitted and checked as cleared.
4	EPS	R/W	0h	Even parity select. Selects the parity when parity is enabled (PEN = 1). The EPS bit works in conjunction with the SP and PEN bits. The relationship between the SP, EPS, and PEN bits is summarized in . 0h: Odd parity is selected (an odd number of logic 1s is transmitted or checked in the data and PARITY bits). 1h: Even parity is selected (an even number of logic 1s is transmitted or checked in the data and PARITY bits).
3	PEN	R/W	0h	Parity enable. The PEN bit works in conjunction with the SP and EPS bits. The relationship between the SP, EPS, and PEN bits is summarized in . 0h: No PARITY bit is transmitted or checked. 1h: Parity bit is generated in transmitted data and is checked in received data between the last data word bit and the first STOP bit.
2	STB	R/W	0h	Number of STOP bits generated. STB specifies 1, 1.5, or 2 STOP bits in each transmitted character. When STB = 1, the WLS bit determines the number of STOP bits. The receiver clocks only the first STOP bit, regardless of the number of STOP bits selected. The number of STOP bits generated is summarized in . 0h: 1 STOP bit is generated. 1h: WLS bit determines the number of STOP bits: • When WLS = 0, 1.5 STOP bits are generated. • When WLS = 1h, 2h, or 3h, 2 STOP bits are generated.
1-0	WLS	R/W	0h	Word length select. Number of bits in each transmitted or received serial character. When STB = 1, the WLS bit determines the number of STOP bits. 0h: 5 bits 1h: 6 bits 2h: 7 bits 3h: 8 bits

4.5.6.5 PRU_ICSS_UART_MODEM_CONTROL Register (Offset = 10h) [reset = 0h]

PRU_ICSS_UART_MODEM_CONTROL is shown in Figure 4-167 and described in Table 4-362.

Return to Summary Table.

The Modem control register provides the ability to enable/disable the autoflow functions, and enable/disable the loopback function for diagnostic purposes.

Table 4-361. PRU_ICSS_UART_MODEM_CONTROL Instances

Instance	Physical Address
PRU_ICSS_UART	4802 8010h

Figure 4-167. PRU_ICSS_UART_MODEM_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED		AFE	LOOP	OUT2	OUT1	RTS	RESERVED
R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-362. PRU_ICSS_UART_MODEM_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5	AFE	R/W	0h	Autoflow control enable. Autoflow control allows the $\overline{\text{UARTn\_RTS}}$ and $\overline{\text{UARTn\_CTS}}$ signals to provide handshaking between UARTs during data transfer. When AFE = 1, the RTS bit determines the autoflow control enabled. Note that all UARTs do not support this feature, see your device-specific data manual for supported features. If this feature is not available, this bit is reserved in this device and should be cleared to 0. 0h: Autoflow control is disabled. 1h:Autoflow control is enabled: • When RTS = 0, $\overline{\text{UARTn\_CTS}}$ is only enabled. • When RTS = 1, $\overline{\text{UARTn\_RTS}}$ and $\overline{\text{UARTn\_CTS}}$ are enabled.
4	LOOP	R/W	0h	Loop back mode enable. LOOP is used for the diagnostic testing using the loop back feature. 0h: Loop back mode is disabled. 1h: Loop back mode is enabled. When LOOP is set, the following occur: • The UARTn_TXD signal is set high. • The UARTn_RXD pin is disconnected. • The output of the transmitter shift register (TSR) is lopped back in to the receiver shift register (RSR) input.

Table 4-362. PRU_ICSS_UART_MODEM_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	OUT2	R/W	0h	OUT2 Control Bit
2	OUT1	R/W	0h	OUT1 Control Bit
1	RTS	R/W	0h	RTS control. When AFE = 1, the RTS bit determines the autoflow control enabled. Note that all UARTs do not support this feature, see your device-specific data manual for supported features. If this feature is not available, this bit is reserved in this device and should be cleared to 0. 0h: $\overline{\text{UARTn\_RTS}}$ is disabled, $\overline{\text{UARTn\_CTS}}$ is only enabled. 1h: $\overline{\text{UARTn\_RTS}}$ and $\overline{\text{UARTn\_CTS}}$ are enabled.
0	RESERVED	R	0h	Reserved

4.5.6.6 PRU_ICSS_UART_LINE_STATUS Register (Offset = 14h) [reset = 60h]

PRU_ICSS_UART_LINE_STATUS is shown in Figure 4-168 and described in Table 4-364.

Return to Summary Table.

The Line status register provides information to the CPU concerning the status of data transfers. Line status register is intended for read operations only; do not write to this register. Bits 1 through 4 record the error conditions that produce a receiver line status interrupt.

Table 4-363. PRU_ICSS_UART_LINE_STATUS Instances

Instance	Physical Address
PRU_ICSS_UART	4802 8014h

Figure 4-168. PRU_ICSS_UART_LINE_STATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RXFIFOE	TEMT	THRE	BI	FE	PE	OE	DR
R-0h	R-1h	R-1h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-364. PRU_ICSS_UART_LINE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	RXFIFOE	R	0h	Receiver FIFO error. **In non-FIFO mode:** 0h: There has been no error, or RXFIFOE was cleared because the CPU read the erroneous character from the receiver buffer register (RBR). 1h: There is a parity error, framing error, or break indicator in the receiver buffer register (RBR). **In FIFO mode:** 0h: There has been no error, or RXFIFOE was cleared because the CPU read the erroneous character from the receiver FIFO and there are no more errors in the receiver FIFO. 1h: At least one parity error, framing error, or break indicator in the receiver FIFO.

Table 4-364. PRU_ICSS_UART_LINE_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	TEMT	R	1h	Transmitter empty (TEMT) indicator. **In non-FIFO mode:** 0h: Either the transmitter holding register (THR) or the transmitter shift register (TSR) contains a data character. 1h: Both the transmitter holding register (THR) and the transmitter shift register (TSR) are empty.
				In FIFO mode: 0h: Either the transmitter FIFO or the transmitter shift register (TSR) contains a data character. 1h: Both the transmitter FIFO and the transmitter shift register (TSR) are empty.
5	THRE	R	1h	Transmitter holding register empty (THRE) indicator. If the THRE bit is set and the corresponding interrupt enable bit is set (ETBEI = 1 in IER), an interrupt request is generated. **In non-FIFO mode:** 0h: Transmitter holding register (THR) is not empty. THR has been loaded by the CPU. 1h: Transmitter holding register (THR) is empty (ready to accept a new character). The content of THR has been transferred to the transmitter shift register (TSR).
				In FIFO mode: 0h: Transmitter FIFO is not empty. At least one character has been written to the transmitter FIFO. You can write to the transmitter FIFO if it is not full. 1h: Transmitter FIFO is empty. The last character in the FIFO has been transferred to the transmitter shift register (TSR).
4	BI	R	0h	Break indicator. The BI bit is set whenever the receive data input (UARTn_RXD) was held low for longer than a full-word transmission time. A full-word transmission time is defined as the total time to transmit the START, data, PARITY, and STOP bits. If the BI bit is set and the corresponding interrupt enable bit is set (ELSI = 1 in IER), an interrupt request is generated. **In non-FIFO mode:** 0h: No break has been detected, or the BI bit was cleared because the CPU read the erroneous character from the receiver buffer register (RBR). 1h: A break has been detected with the character in the receiver buffer register (RBR).
				In FIFO mode: 0h: No break has been detected, or the BI bit was cleared because the CPU read the erroneous character from the receiver FIFO and the next character to be read from the FIFO has no break indicator. 1h: A break has been detected with the character at the top of the receiver FIFO.

Table 4-364. PRU_ICSS_UART_LINE_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	FE	R	0h	Framing error (FE) indicator. A framing error occurs when the received character does not have a valid STOP bit. In response to a framing error, the UART sets the FE bit and waits until the signal on the RX pin goes high. Once the RX signal goes high, the receiver is ready to detect a new START bit and receive new data. If the FE bit is set and the corresponding interrupt enable bit is set (ELSI = 1 in IER), an interrupt request is generated. **In non-FIFO mode:** 0h: No framing error has been detected, or the FE bit was cleared because the CPU read the erroneous data from the receiver buffer register (RBR). 1h: A framing error has been detected with the character in the receiver buffer register (RBR).
				In FIFO mode: 0h: No framing error has been detected, or the FE bit was cleared because the CPU read the erroneous data from the receiver FIFO and the next character to be read from the FIFO has no framing error. 1h: A framing error has been detected with the character at the top of the receiver FIFO.
2	PE	R	0h	Parity error (PE) indicator. A parity error occurs when the parity of the received character does not match the parity selected with the EPS bit in the line control register (LCR). If the PE bit is set and the corresponding interrupt enable bit is set (ELSI = 1 in IER), an interrupt request is generated. **In non-FIFO mode:** 0h: No parity error has been detected, or the PE bit was cleared because the CPU read the erroneous data from the receiver buffer register (RBR). 1h: A parity error has been detected with the character in the receiver buffer register (RBR).
				In FIFO mode: 0h: No parity error has been detected, or the PE bit was cleared because the CPU read the erroneous data from the receiver FIFO and the next character to be read from the FIFO has no parity error. 1h: A parity error has been detected with the character at the top of the receiver FIFO.

Table 4-364. PRU_ICSS_UART_LINE_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	OE	R	0h	Overrun error (OE) indicator. An overrun error in the non-FIFO mode is different from an overrun error in the FIFO mode. If the OE bit is set and the corresponding interrupt enable bit is set (ELSI = 1 in IER), an interrupt request is generated. **In non-FIFO mode:** 0h: No overrun error has been detected, or the OE bit was cleared because the CPU read the content of the line status register (LSR). 1h: Overrun error has been detected. Before the character in the receiver buffer register (RBR) could be read, it was overwritten by the next character arriving in RBR.
				In FIFO mode: 0h: No overrun error has been detected, or the OE bit was cleared because the CPU read the content of the line status register (LSR). 1h: Overrun error has been detected. If data continues to fill the FIFO beyond the trigger level, an overrun error occurs only after the FIFO is full and the next character has been completely received in the shift register. An overrun error is indicated to the CPU as soon as it happens. The new character overwrites the character in the shift register, but it is not transferred to the FIFO.
0	DR	R	0h	Data-ready (DR) indicator for the receiver. If the DR bit is set and the corresponding interrupt enable bit is set (ERBI = 1 in IER), an interrupt request is generated. **In non-FIFO mode:** 0h: Data is not ready, or the DR bit was cleared because the character was read from the receiver buffer register (RBR). 1h: Data is ready. A complete incoming character has been received and transferred into the receiver buffer register (RBR).
				In FIFO mode: 0h: Data is not ready, or the DR bit was cleared because all of the characters in the receiver FIFO have been read. 1h: Data is ready. There is at least one unread character in the receiver FIFO. If the FIFO is empty, the DR bit is set as soon as a complete incoming character has been received and transferred into the FIFO. The DR bit remains set until the FIFO is empty again.

4.5.6.7 PRU_ICSS_UART_MODEM_STATUS Register (Offset = 18h) [reset = 0h]

PRU_ICSS_UART_MODEM_STATUS is shown in Figure 4-169 and described in Table 4-366.

Return to Summary Table.

The Modem status register provides information to the CPU concerning the status of modem control signals. Modem status register is intended for read operations only; do not write to this register.

Table 4-365. PRU_ICSS_UART_MODEM_STATUS Instances

Instance	Physical Address
PRU_ICSS_UART	4802 8018h

Figure 4-169. PRU_ICSS_UART_MODEM_STATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
CD	RI	DSR	CTS	DCD	TERI	DDSR	DCTS
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-366. PRU_ICSS_UART_MODEM_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	CD	R	0h	Complement of the Carrier Detect input. When the UART is in the diagnostic test mode (loopback mode MCR[4] = 1), this bit is equal to the MCR bit 3 (OUT2)..
6	RI	R	0h	Complement of the Ring Indicator input. When the UART is in the diagnostic test mode (loopback mode MCR[4] = 1), this bit is equal to the MCR bit 2 (OUT1).
5	DSR	R	0h	Complement of the Data Set Ready input. When the UART is in the diagnostic test mode (loopback mode MCR[4] = 1), this bit is equal to the MCR bit 0 (DTR).
4	CTS	R	0h	Complement of the Clear To Send input. When the UART is in the diagnostic test mode (loopback mode MCR[4] = 1), this bit is equal to the MCR bit 1 (RTS).
3	DCD	R	0h	Change in DCD indicator bit. DCD indicates that the DCD input has changed state since the last time it was read by the CPU. When DCD is set and the modem status interrupt is enabled, a modem status interrupt is generated.
2	TERI	R	0h	Trailing edge of RI (TERI) indicator bit. TERI indicates that the RI input has changed from a low to a high. When TERI is set and the modem status interrupt is enabled, a modem status interrupt is generated.

Table 4-366. PRU_ICSS_UART_MODEM_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DDSR	R	0h	Change in DSR indicator bit. DDSR indicates that the DSR input has changed state since the last time it was read by the CPU. When DDSR is set and the modem status interrupt is enabled, a modem status interrupt is generated.
0	DCTS	R	0h	Change in CTS indicator bit. DCTS indicates that the CTS input has changed state since the last time it was read by the CPU. When DCTS is set (autoflow control is not enabled and the modem status interrupt is enabled), a modem status interrupt is generated. When autoflow control is enabled, no interrupt is generated.

4.5.6.8 PRU_ICSS_UART_SCRATCH Register (Offset = 1Ch) [reset = 0h]

PRU_ICSS_UART_SCRATCH is shown in Figure 4-170 and described in Table 4-368.

Return to Summary Table.

The Scratch Pad register is intended for programmer's use as a scratch pad. It temporarily holds the programmer's data without affecting UART operation.

Table 4-367. PRU_ICSS_UART_SCRATCH Instances

Instance	Physical Address
PRU_ICSS_UART	4802 801Ch

Figure 4-170. PRU_ICSS_UART_SCRATCH Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DATA							
R-0h																								R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-368. PRU_ICSS_UART_SCRATCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	DATA	R/W	0h	These bits are intended for the programmer's use as a scratch pad in the sense that it temporarily holds the programmer's data without affecting any other UART operation.

4.5.6.9 PRU_ICSS_UART_DIVISOR_LSB Register (Offset = 20h) [reset = 0h]

PRU_ICSS_UART_DIVISOR_LSB is shown in Figure 4-171 and described in Table 4-370.

Return to Summary Table.

Two 8-bit register fields (DLL and DLH), called divisor latches, store the 16-bit divisor for generation of the baud clock in the baud generator. DLH holds the most-significant bits of the divisor, and DLL holds the least-significant bits of the divisor. These divisor latches must be loaded during initialization of the UART in order to ensure desired operation of the baud generator. Writing to the divisor latches results in two wait states being inserted during the write access while the baud generator is loaded with the new value.

Table 4-369. PRU_ICSS_UART_DIVISOR_LSB Instances

Instance	Physical Address
PRU_ICSS_UART	4802 8020h

Figure 4-171. PRU_ICSS_UART_DIVISOR_LSB Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DLL							
R-0h																								R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-370. PRU_ICSS_UART_DIVISOR_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	DLL	R/W	0h	The 8 least-significant bits (LSBs) of the 16-bit divisor for generation of the baud clock in the baud rate generator.

4.5.6.10 PRU_ICSS_UART_DIVISOR_MSB Register (Offset = 24h) [reset = 0h]

PRU_ICSS_UART_DIVISOR_MSB is shown in Figure 4-172 and described in Table 4-372.

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Two 8-bit register fields (DLL and DLH), called divisor latches, store the 16-bit divisor for generation of the baud clock in the baud generator. DLH holds the most-significant bits of the divisor, and DLL holds the least-significant bits of the divisor. These divisor latches must be loaded during initialization of the UART in order to ensure desired operation of the baud generator. Writing to the divisor latches results in two wait states being inserted during the write access while the baud generator is loaded with the new value.

Table 4-371. PRU_ICSS_UART_DIVISOR_MSB_ Instances

Instance	Physical Address
PRU_ICSS_UART	4802 8024h

Figure 4-172. PRU_ICSS_UART_DIVISOR_MSB_ Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DLH							
R-0h																								R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-372. PRU_ICSS_UART_DIVISOR_MSB_ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	DLH	R/W	0h	The 8 most-significant bits (MSBs) of the 16-bit divisor for generation of the baud clock in the baud rate generator.

4.5.6.11 PRU_ICSS_UART_PERIPHERAL_ID Register (Offset = 28h) [reset = 44141102h]

PRU_ICSS_UART_PERIPHERAL_ID is shown in Figure 4-173 and described in Table 4-374.

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Peripheral Identification register.

Table 4-373. PRU_ICSS_UART_PERIPHERAL_ID Instances

Instance	Physical Address
PRU_ICSS_UART	4802 8028h

Figure 4-173. PRU_ICSS_UART_PERIPHERAL_ID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID																															
R-44141102h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-374. PRU_ICSS_UART_PERIPHERAL_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PID	R	44141102h	

4.5.6.12 PRU_ICSS_UART_POWER_MANAGEMENT_AND_EMULATION Register (Offset = 30h) [reset = 0h]

PRU_ICSS_UART_POWER_MANAGEMENT_AND_EMULATION is shown in Figure 4-174 and described in Table 4-376.

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Power and emulation management register.

Table 4-375. PRU_ICSS_UART_POWER_MANAGEMENT_AND_EMULATION Instances

Instance	Physical Address
PRU_ICSS_UART	4802 8030h

Figure 4-174. PRU_ICSS_UART_POWER_MANAGEMENT_AND_EMULATION Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED	UTRST	URRST	RESERVED				
R/W-0h	R/W-0h	R/W-0h	R-0h				
7	6	5	4	3	2	1	0
RESERVED							FREE
R-0h							R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-376. PRU_ICSS_UART_POWER_MANAGEMENT_AND_EMULATION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	RESERVED	R/W	0h	Reserved. This bit must always be written with a 0.
14	UTRST	R/W	0h	UART transmitter reset. Resets and enables the transmitter. 0h: Transmitter is disabled and in reset state. 1h: Transmitter is enabled.
13	URRST	R/W	0h	UART receiver reset. Resets and enables the receiver. 0h: Receiver is disabled and in reset state. 1h: Receiver is enabled.
12-1	RESERVED	R	0h	Reserved
0	FREE	R/W	0h	Free-running enable mode bit. This bit determines the emulation mode functionality of the UART. When halted, the UART can handle register read/write requests, but does not generate any transmission/reception, interrupts or events. 0h: If a transmission is not in progress, the UART halts immediately. If a transmission is in progress, the UART halts after completion of the one-word transmission. 1h: Free-running mode is enabled; UART continues to run normally.

4.5.6.13 PRU_ICSS_UART_MODE_DEFINITION Register (Offset = 34h) [reset = 0h]

PRU_ICSS_UART_MODE_DEFINITION is shown in Figure 4-175 and described in Table 4-378.

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The Mode definition register determines the over-sampling mode for the UART.

Table 4-377. PRU_ICSS_UART_MODE_DEFINITION Instances

Instance	Physical Address
PRU_ICSS_UART	4802 8034h

Figure 4-175. PRU_ICSS_UART_MODE_DEFINITION Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							OSM_SEL
R-0h							R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 4-378. PRU_ICSS_UART_MODE_DEFINITION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	OSM_SEL	R/W	0h	Over-Sampling Mode Select. 0h: 16× over-sampling. 1h: 13× over-sampling.

4.5.7 PRU_ICSS_ECAP Registers

PRU_ICSS_ECAP Registers lists the memory-mapped registers for the PRU_ICSS_eCAP0 module. All register offset addresses not listed in PRU_ICSS_ECAP Registers should be considered as reserved locations and the register contents should not be modified.

Table 4-379. PRU_ICSS_ECAP Instances

Instance	Base Address
PRU_ICSS_ECAP	4803 0000h

Table 4-380. PRU_ICSS_ECAP Registers

Offset	Acronym	Register Name	PRU_ICSS_ECAP Physical Address	Section
0h	PRU_ICSS_ECAP_TSCNT	Time Stamp Counter Register	4803 0000h	
4h	PRU_ICSS_ECAP_CNTPHS	Counter Phase Control Register	4803 0004h	
8h	PRU_ICSS_ECAP_CAP1	Capture-1 Register	4803 0008h	
Ch	PRU_ICSS_ECAP_CAP2	Capture-2 Register	4803 000Ch	
10h	PRU_ICSS_ECAP_CAP3	Capture-3 Register	4803 0010h	
14h	PRU_ICSS_ECAP_CAP4	Capture-4 Register	4803 0014h	
28h	PRU_ICSS_ECAP_ECCTL1	ECAP Control Register1	4803 0028h	
2Ah	PRU_ICSS_ECAP_ECCTL2	ECAP Control Register 2	4803 002Ah	
2Ch	PRU_ICSS_ECAP_ECEINT	ECAP Interrupt Enable Register	4803 002Ch	
2Eh	PRU_ICSS_ECAP_ECFLG	ECAP Interrupt Flag Register	4803 002Eh	
30h	PRU_ICSS_ECAP_ECCLR	ECAP Interrupt Clear Register	4803 0030h	
34h	PRU_ICSS_ECAP_ECFRC	ECAP Interrupt Forcing Register	4803 0034h	
5Ch	PRU_ICSS_ECAP_PID	ECAP Revision ID	4803 005Ch	

4.5.7.1 PRU_ICSS_ECAP_TSCNT Register (Offset = 0h) [reset = 0h]

PRU_ICSS_ECAP_TSCNT is shown in Figure 4-176 and described in Table 4-382.

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Time Stamp Counter Register

Table 4-381. PRU_ICSS_ECAP_TSCNT Instances

Instance	Physical Address
PRU_ICSS_ECAP	4803 0000h

Figure 4-176. PRU_ICSS_ECAP_TSCNT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSCNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-382. PRU_ICSS_ECAP_TSCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TSCNT	R/W	0h	Active 32 bit-counter register that is used as the capture time-base

4.5.7.2 PRU_ICSS_ECAP_CNTPHS Register (Offset = 4h) [reset = 0h]

PRU_ICSS_ECAP_CNTPHS is shown in Figure 4-177 and described in Table 4-384.

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Counter Phase Control Register

Table 4-383. PRU_ICSS_ECAP_CNTPHS Instances

Instance	Physical Address
PRU_ICSS_ECAP	4803 0004h

Figure 4-177. PRU_ICSS_ECAP_CNTPHS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNTPHS																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-384. PRU_ICSS_ECAP_CNTPHS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CNTPHS	R/W	0h	Counter phase value register that can be programmed for phase lag/lead. This register shadows TSCNT and is loaded into PRU_ICSS_ECAP_TSCNT upon either a SYNCI event or S/W force via a control bit. Used to achieve phase control synchronization with respect to other eCAP and EPWM time-bases.

4.5.7.3 PRU_ICSS_ECAP_CAP1 Register (Offset = 8h) [reset = 0h]

PRU_ICSS_ECAP_CAP1 is shown in Figure 4-178 and described in Table 4-386.

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Capture-1 Register

Table 4-385. PRU_ICSS_ECAP_CAP1 Instances

Instance	Physical Address
PRU_ICSS_ECAP	4803 0008h

Figure 4-178. PRU_ICSS_ECAP_CAP1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAP1																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-386. PRU_ICSS_ECAP_CAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAP1	R/W	0h	This register can be loaded (written) by the following. (a) Time-Stamp (that is, counter value) during a capture event. (b) Software may be useful for test purposes. (c) APRD active register when used in APWM mode.

4.5.7.4 PRU_ICSS_ECAP_CAP2 Register (Offset = Ch) [reset = 0h]

PRU_ICSS_ECAP_CAP2 is shown in Figure 4-179 and described in Table 4-388.

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Capture-2 Register

Table 4-387. PRU_ICSS_ECAP_CAP2 Instances

Instance	Physical Address
PRU_ICSS_ECAP	4803 000Ch

Figure 4-179. PRU_ICSS_ECAP_CAP2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAP2																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-388. PRU_ICSS_ECAP_CAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAP2	R/W	0h	This register can be loaded (written) by the following. (a) Time-Stamp (that is, counter value) during a capture event. (b) Software may be useful for test purposes. (c) APRD active register when used in APWM mode.

4.5.7.5 PRU_ICSS_ECAP_CAP3 Register (Offset = 10h) [reset = 0h]

PRU_ICSS_ECAP_CAP3 is shown in Figure 4-180 and described in Table 4-390.

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Capture-3 Register

Table 4-389. PRU_ICSS_ECAP_CAP3 Instances

Instance	Physical Address
PRU_ICSS_ECAP	4803 0010h

Figure 4-180. PRU_ICSS_ECAP_CAP3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAP3																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-390. PRU_ICSS_ECAP_CAP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAP3	R/W	0h	In CMP mode, this is a time-stamp capture register. In APWM mode, this is the period shadow (APRD) register. User software updates the PWM period value through this register. In this mode, CAP3 shadows CAP1.

4.5.7.6 PRU_ICSS_ECAP_CAP4 Register (Offset = 14h) [reset = 0h]

PRU_ICSS_ECAP_CAP4 is shown in Figure 4-181 and described in Table 4-392.

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Capture-4 Register

Table 4-391. PRU_ICSS_ECAP_CAP4 Instances

Instance	Physical Address
PRU_ICSS_ECAP	4803 0014h

Figure 4-181. PRU_ICSS_ECAP_CAP4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAP4																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-392. PRU_ICSS_ECAP_CAP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAP4	R/W	0h	In CMP mode, this is a time-stamp capture register. In APWM mode, this is the compare shadow (ACMP) register. User software updates the PWM compare value through this register. In this mode, CAP4 shadows CAP2.

4.5.7.7 PRU_ICSS_ECAP_ECCTL1 Register (Offset = 28h) [reset = 0h]

PRU_ICSS_ECAP_ECCTL1 is shown in Figure 4-182 and described in Table 4-394.

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ECAP Control Register1

Table 4-393. PRU_ICSS_ECAP_ECCTL1 Instances

Instance	Physical Address
PRU_ICSS_ECAP	4803 0028h

Figure 4-182. PRU_ICSS_ECAP_ECCTL1 Register

15	14	13	12	11	10	9	8
FREE_SOFT		EVTFLTPS					CAPLDEN
R/W-0h		R/W-0h					R/W-0h
7	6	5	4	3	2	1	0
CTRRST4	CAP4POL	CTRRST3	CAP3POL	CTRRST2	CAP2POL	CTRRST1	CAP1POL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-394. PRU_ICSS_ECAP_ECCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	FREE_SOFT	R/W	0h	Emulation Control 0h: TSCNT counter stops immediately on emulation suspend. 1h: TSCNT counter runs until = 0. 2h: TSCNT counter is unaffected by emulation suspend (Run Free). 3h: TSCNT counter is unaffected by emulation suspend (Run Free).
13-9	EVTFLTPS	R/W	0h	Event Filter prescale select: 0h: Divide by 1 (i.e,. no prescale, by-pass the prescaler) 1h: Divide by 2 2h: Divide by 4 3h: Divide by 6 4h: Divide by 8 5h: Divide by 10 1Eh: Divide by 60 1Fh: Divide by 62
8	CAPLDEN	R/W	0h	Enable Loading of PRU_ICSS_ECAP_CAP1 to PRU_ICSS_ECAP_CAP4 registers on a capture event 0h: Disable PRU_ICSS_ECAP_CAP1-PRU_ICSS_ECAP_CAP4 register loads at capture event time. 1h: Enable PRU_ICSS_ECAP_CAP1-PRU_ICSS_ECAP_CAP4 register loads at capture event time.
7	CTRRST4	R/W	0h	Counter Reset on Capture Event 4 0h: Do not reset counter on Capture Event 4 (absolute time stamp operation) 1h: Reset counter after Capture Event 4 time-stamp has been captured (used in difference mode operation)
6	CAP4POL	R/W	0h	Capture Event 4 Polarity select 0h: Capture Event 4 triggered on a rising edge (RE) 1h: Capture Event 4 triggered on a falling edge (FE)

Table 4-394. PRU_ICSS_ECAP_ECCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CTRRST3	R/W	0h	Counter Reset on Capture Event 3 0h: Do not reset counter on Capture Event 3 (absolute time stamp) 1h: Reset counter after Event 3 time-stamp has been captured (used in difference mode operation)
4	CAP3POL	R/W	0h	Capture Event 3 Polarity select 0h: Capture Event 3 triggered on a rising edge (RE) 1h: Capture Event 3 triggered on a falling edge (FE)
3	CTRRST2	R/W	0h	Counter Reset on Capture Event 2 0h: Do not reset counter on Capture Event 2 (absolute time stamp) 1h: Reset counter after Event 2 time-stamp has been captured (used in difference mode operation)
2	CAP2POL	R/W	0h	Capture Event 2 Polarity select 0h: Capture Event 2 triggered on a rising edge (RE) 1h: Capture Event 2 triggered on a falling edge (FE)
1	CTRRST1	R/W	0h	Counter Reset on Capture Event 1 0h: Do not reset counter on Capture Event 1 (absolute time stamp) 1h: Reset counter after Event 1 time-stamp has been captured (used in difference mode operation)
0	CAP1POL	R/W	0h	Capture Event 1 Polarity select 0h: Capture Event 1 triggered on a rising edge (RE) 1h: Capture Event 1 triggered on a falling edge (FE)

4.5.7.8 PRU_ICSS_ECAP_ECCTL2 Register (Offset = 2Ah) [reset = 6h]

PRU_ICSS_ECAP_ECCTL2 is shown in Figure 4-183 and described in Table 4-396.

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ECAP Control Register 2

Table 4-395. PRU_ICSS_ECAP_ECCTL2 Instances

Instance	Physical Address
PRU_ICSS_ECAP	4803 002Ah

Figure 4-183. PRU_ICSS_ECAP_ECCTL2 Register

15	14	13	12	11	10	9	8
RESERVED					APWMPOL	CAPAPWM	SWSYNC
R-0h					R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SYNCO_SEL		SYNCI_EN	TSCNTSTP	REARMRESET	STOPVALUE		CONTONESHT
R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-3h		R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-396. PRU_ICSS_ECAP_ECCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	Reserved
10	APWMPOL	R/W	0h	APWM output polarity select. This is applicable only in APWM operating mode 0h: Output is active high (Compare value defines high time) 1h: Output is active low (Compare value defines low time)
9	CAPAPWM	R/W	0h	CAP/APWM operating mode select 0h: ECAP module operates in capture mode. This mode forces the following configuration. (a) Inhibits TSCNT resets via CTR = PRD event. (b) Inhibits shadow loads on PRU_ICSS_ECAP_CAP1 and PRU_ICSS_ECAP_CAP2 registers. (c) Permits user to enable PRU_ICSS_ECAP_CAP1-PRU_ICSS_ECAP_CAP4 register load. (d) ECAP input/APWM output pin operates as a capture input. 1h: ECAP module operates in APWM mode. This mode forces the following configuration. (a) Resets TSCNT on CTR = PRD event (period boundary). (b) Permits shadow loading on PRU_ICSS_ECAP_CAP1 and PRU_ICSS_ECAP_CAP2 registers. (c) Disables loading of time-stamps into PRU_ICSS_ECAP_CAP1 - PRU_ICSS_ECAP_CAP4 registers. (d) ECAP input/APWM ouput pin operates as a APWM output.

Table 4-396. PRU_ICSS_ECAP_ECCTL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	SWSYNC	R/W	0h	Software-forced Counter (TSCNT) Synchronizing. This provides a convenient software method to synchronize some or all ECAP time bases. In APWM mode, the synchronizing can also be done via the CTR = PRD event. Note: Selection CTR = PRD is meaningful only in APWM mode. However, you can choose it in CAP mode if you find doing so useful. 0h: Writing a zero has no effect. Reading always returns a zero 1h: Writing a one forces a TSCNT shadow load of current ECAP module and any ECAP modules down-stream providing the SYNCO_SEL bits are 1'b00. After writing a 1, this bit returns to a zero.
7-6	SYNCO_SEL	R/W	0h	Sync-Out Select 0h: Select sync-in event to be the sync-out signal (pass through) 1h: Select CTR = PRD event to be the sync-out signal 2h: Disable sync out signal 3h: Disable sync out signal
5	SYNCI_EN	R/W	0h	Counter (TSCNT) Sync-In select mode 0h: Disable sync-in option 1h: Enable counter (TSCNT) to be loaded from PRU_ICSS_ECAP_CNTPHS register upon either a SYNCI signal or a S/W force event.
4	TSCNTSTP	R/W	0h	Time Stamp (TSCNT) Counter Stop (freeze) Control 0h: TSCNT stopped 1h: TSCNT free-running
3	REARMRESET	R/W	0h	One-Shot Re-Arming Control, that is, wait for stop trigger. Note: The re-arm function is valid in one shot or continuous mode. 0h: Has no effect (reading always returns a 0) 1h: Arms the one-shot sequence as follows: 1) Resets the Mod4 counter to zero. 2) Unfreezes the Mod4 counter. 3) Enables capture register loads.

Table 4-396. PRU_ICSS_ECAP_ECCTL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-1	STOPVALUE	R/W	3h	Stop value for one-shot mode. This is the number (between 1 and 4) of captures allowed to occur before the CAP (1 through 4) registers are frozen, that is, capture sequence is stopped. Wrap value for continuous mode. This is the number (between 1 and 4) of the capture register in which the circular buffer wraps around and starts again. Notes: STOPVALUE is compared to Mod4 counter and, when equal, the following two actions occur. (1) Mod4 counter is stopped (frozen). (2) Capture register loads are inhibited. In one-shot mode, further interrupt events are blocked until re-armed. 0h: Stop after Capture Event 1 in one-shot mode. Wrap after Capture Event 1 in continuous mode. 1h: Stop after Capture Event 2 in one-shot mode. Wrap after Capture Event 2 in continuous mode. 2h: Stop after Capture Event 3 in one-shot mode. Wrap after Capture Event 3 in continuous mode. 3h: Stop after Capture Event 4 in one-shot mode. Wrap after Capture Event 4 in continuous mode.
0	CONTONESHT	R/W	0h	Continuous or one-shot mode control (applicable only in capture mode) 0h: Operate in continuous mode 1h: Operate in one-shot mode

4.5.7.9 PRU_ICSS_ECAP_ECEINT Register (Offset = 2Ch) [reset = 0h]

PRU_ICSS_ECAP_ECEINT is shown in Figure 4-184 and described in Table 4-398.

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ECAP Interrupt Enable Register

Table 4-397. PRU_ICSS_ECAP_ECEINT Instances

Instance	Physical Address
PRU_ICSS_ECAP	4803 002Ch

Figure 4-184. PRU_ICSS_ECAP_ECEINT Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
CMPEQ	PRDEQ	CNTOVF	CEVT4	CEVT3	CEVT2	CEVT1	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-398. PRU_ICSS_ECAP_ECEINT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	CMPEQ	R/W	0h	Counter Equal **Compare** Interrupt Enable. 0h: Disable Compare Equal as an Interrupt source. 1h: Enable Compare Equal as an Interrupt source.
6	PRDEQ	R/W	0h	Counter Equal **Period** Interrupt Enable. 0h: Disable Period Equal as an Interrupt source. 1h: Enable Period Equal as an Interrupt source.
5	CNTOVF	R/W	0h	Counter Overflow Interrupt Enable. 0h: Disable counter Overflow as an Interrupt source. 1h: Enable counter Overflow as an Interrupt source.
4	CEVT4	R/W	0h	Capture Event 4 Interrupt Enable. 0h: Disable Capture Event 4 as an Interrupt source. 1h: Enable Capture Event 4 as an Interrupt source.
3	CEVT3	R/W	0h	Capture Event 3 Interrupt Enable. 0h: Disable Capture Event 3 as an Interrupt source. 1h: Enable Capture Event 3 as an Interrupt source.
2	CEVT2	R/W	0h	Capture Event 2 Interrupt Enable. 0h: Disable Capture Event 2 as an Interrupt source. 1h: Enable Capture Event 2 as an Interrupt source.

Table 4-398. PRU_ICSS_ECAP_ECEINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CEVT1	R/W	0h	Capture Event 1 Interrupt Enable . 0h: Disable Capture Event 1 as an Interrupt source. 1h: Enable Capture Event 1 as an Interrupt source.
0	RESERVED	R	0h	Reserved

4.5.7.10 PRU_ICSS_ECAP_ECFLG Register (Offset = 2Eh) [reset = 0h]

PRU_ICSS_ECAP_ECFLG is shown in Figure 4-185 and described in Table 4-400.

Return to Summary Table.

ECAP Interrupt Flag Register

Table 4-399. PRU_ICSS_ECAP_ECFLG Instances

Instance	Physical Address
PRU_ICSS_ECAP	4803 002Eh

Figure 4-185. PRU_ICSS_ECAP_ECFLG Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
CMPEQ	PRDEQ	CNTOVF	CEVT4	CEVT3	CEVT2	CEVT1	INT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-400. PRU_ICSS_ECAP_ECFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	CMPEQ	R	0h	Compare Equal Compare Status Flag. This flag is only active in APWM mode. 0h: Indicates no event occurred 1h: Indicates the counter (TSCNT) reached the compare register value (ACMP)
6	PRDEQ	R	0h	Counter Equal Period Status Flag. This flag is only active in APWM mode. 0h: Indicates no event occurred 1h: Indicates the counter (TSCNT) reached the period register value (APRD) and was reset.
5	CNTOVF	R	0h	Counter Overflow Status Flag. This flag is active in CAP and APWM mode. 0h: Indicates no event occurred. 1h: Indicates the counter (TSCNT) has made the transition from FFFFFFFFh to 00000000h
4	CEVT4	R	0h	Capture Event 4 Status Flag This flag is only active in CAP mode. 0h: Indicates no event occurred 1h: Indicates the fourth event occurred at ECAPn pin
3	CEVT3	R	0h	Capture Event 3 Status Flag. This flag is active only in CAP mode. 0h: Indicates no event occurred. 1h: Indicates the third event occurred at ECAPn pin.

Table 4-400. PRU_ICSS_ECAP_ECFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CEVT2	R	0h	Capture Event 2 Status Flag. This flag is only active in CAP mode. 0h: Indicates no event occurred. 1h: Indicates the second event occurred at ECAPn pin.
1	CEVT1	R	0h	Capture Event 1 Status Flag. This flag is only active in CAP mode. 0h: Indicates no event occurred. 1h: Indicates the first event occurred at ECAPn pin.
0	INT	R	0h	Global Interrupt Status Flag 0h: Indicates no interrupt generated. 1h: Indicates that an interrupt was generated.

4.5.7.11 PRU_ICSS_ECAP_ECCLR Register (Offset = 30h) [reset = 0h]

PRU_ICSS_ECAP_ECCLR is shown in Figure 4-186 and described in Table 4-402.

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ECAP Interrupt Clear Register

Table 4-401. PRU_ICSS_ECAP_ECCLR Instances

Instance	Physical Address
PRU_ICSS_ECAP	4803 0030h

Figure 4-186. PRU_ICSS_ECAP_ECCLR Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
CMPEQ	PRDEQ	CNTOVF	CEVT4	CEVT3	CEVT2	CEVT1	INT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-402. PRU_ICSS_ECAP_ECCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	CMPEQ	R/W	0h	Counter Equal Compare Status Flag 0h: Writing a 0 has no effect. Always reads back a 0 1h: Writing a 1 clears the CTR=CMP flag condition
6	PRDEQ	R/W	0h	Counter Equal Period Status Flag 0h: Writing a 0 has no effect. Always reads back a 0 1h: Writing a 1 clears the CTR=PRD flag condition
5	CNTOVF	R/W	0h	Counter Overflow Status Flag 0h: Writing a 0 has no effect. Always reads back a 0 1h: Writing a 1 clears the CNTOVF flag condition
4	CEVT4	R/W	0h	Capture Event 4 Status Flag 0h: Writing a 0 has no effect. Always reads back a 0. 1h: Writing a 1 clears the CEVT3 flag condition.
3	CEVT3	R/W	0h	Capture Event 3 Status Flag 0h: Writing a 0 has no effect. Always reads back a 0. 1h: Writing a 1 clears the CEVT3 flag condition.
2	CEVT2	R/W	0h	Capture Event 2 Status Flag 0h: Writing a 0 has no effect. Always reads back a 0. 1h: Writing a 1 clears the CEVT2 flag condition.

Table 4-402. PRU_ICSS_ECAP_ECCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CEVT1	R/W	0h	Capture Event 1 Status Flag 0h: Writing a 0 has no effect. Always reads back a 0. 1h: Writing a 1 clears the CEVT1 flag condition.
0	INT	R/W	0h	Global Interrupt Clear Flag 0h: Writing a 0 has no effect. Always reads back a 0. 1h: Writing a 1 clears the INT flag and enable further interrupts to be generated if any of the event flags are set to 1.

4.5.7.12 PRU_ICSS_ECAP_ECFRC Register (Offset = 34h) [reset = 0h]

PRU_ICSS_ECAP_ECFRC is shown in Figure 4-187 and described in Table 4-404.

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ECAP Interrupt Forcing Register

Table 4-403. PRU_ICSS_ECAP_ECFRC Instances

Instance	Physical Address
PRU_ICSS_ECAP	4803 0034h

Figure 4-187. PRU_ICSS_ECAP_ECFRC Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
CMPEQ	PRDEQ	CNTOVF	CEVT4	CEVT3	CEVT2	CEVT1	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-404. PRU_ICSS_ECAP_ECFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	CMPEQ	R/W	0h	Force Counter Equal Compare Interrupt 0h: No effect. Always reads back a 0. 1h: Writing a 1 sets the CTR=CMP flag bit.
6	PRDEQ	R/W	0h	Force Counter Equal Period Interrupt 0h: No effect. Always reads back a 0. 1h: Writing a 1 sets the CTR=PRD flag bit.
5	CNTOVF	R/W	0h	Force Counter Overflow 0h: No effect. Always reads back a 0. 1h: Writing a 1 to this bit sets the CNTOVF flag bit.
4	CEVT4	R/W	0h	Force Capture Event 4 0h: No effect. Always reads back a 0. 1h: Writing a 1 sets the CEVT4 flag bit
3	CEVT3	R/W	0h	Force Capture Event 3 0h: No effect. Always reads back a 0. 1h: Writing a 1 sets the CEVT3 flag bit
2	CEVT2	R/W	0h	Force Capture Event 2 0h: No effect. Always reads back a 0. 1h: Writing a 1 sets the CEVT2 flag bit.

Table 4-404. PRU_ICSS_ECAP_ECFRC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CEVT1	R/W	0h	Always reads back a 0. Force Capture Event 1 0h: No effect. 1h: Writing a 1 sets the CEVT1 flag bit.
0	RESERVED	R	0h	Reserved

4.5.7.13 PRU_ICSS_ECAP_PID Register (Offset = 5Ch) [reset = -h]

PRU_ICSS_ECAP_PID is shown in Figure 4-188 and described in Table 4-406.

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ECAP Revision ID

Table 4-405. PRU_ICSS_ECAP_PID Instances

Instance	Physical Address
PRU_ICSS_ECAP	4803 005Ch

Figure 4-188. PRU_ICSS_ECAP_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															
R--h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-406. PRU_ICSS_ECAP_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REVISION	R	-h	IP Revision

4.5.8 PRU_ICSS_MII_RT Registers

PRU_ICSS_MII_RT Registers lists the memory-mapped registers for the PRU_ICSS MII_RT module. All register offset addresses not listed in PRU_ICSS_MII_RT Registers should be considered as reserved locations and the register contents should not be modified.

Table 4-407. PRU_ICSS MII RT Instances

Instance	Base Address
PRU_ICSS_MII_RT	4803 2000h

Table 4-408. PRU_ICSS MII RT Registers

Offset	Acronym	Register Name	PRU_ICSS_MII_RT Physical Address
0h	PRU_ICSS_MII_RT_RXCFG0	MII RXCFG 0 Register	4803 2000h
4h	PRU_ICSS_MII_RT_RXCFG1	MII RXCFG 1 Register	4803 2004h
10h	PRU_ICSS_MII_RT_TXCFG0	MII TXCFG 0 Register	4803 2010h
14h	PRU_ICSS_MII_RT_TXCFG1	MII TXCFG 1 Register	4803 2014h
20h	PRU_ICSS_MII_RT_TX_CRC0	MII TXCRC 0 Register	4803 2020h
24h	PRU_ICSS_MII_RT_TX_CRC1	MII TXCRC 1 Register	4803 2024h
30h	PRU_ICSS_MII_RT_TX_IPG0	MII TXIPG 0 Register	4803 2030h
34h	PRU_ICSS_MII_RT_TX_IPG1	MII TXIPG 1 Register	4803 2034h
38h	PRU_ICSS_MII_RT_PRS0	MII PORT STATUS 0 Register	4803 2038h
3Ch	PRU_ICSS_MII_RT_PRS1	MII PORT STATUS 1 Register	4803 203Ch
40h	PRU_ICSS_MII_RT_RX_FRMS0	MII RXFRMS 0 Register	4803 2040h
44h	PRU_ICSS_MII_RT_RX_FRMS1	MII RXFRMS 1 Register	4803 2044h
48h	PRU_ICSS_MII_RT_RX_PCNT0	MII RXPCNT 0 Register	4803 2048h
4Ch	PRU_ICSS_MII_RT_RX_PCNT1	MII RXPCNT 1 Register	4803 204Ch
50h	PRU_ICSS_MII_RT_RX_ERR0	MII RXERR 0 Register	4803 2050h
54h	PRU_ICSS_MII_RT_RX_ERR1	MII RXERR 1 Register	4803 2054h
60h	PRU_ICSS_MII_RT_RXFLV0	MII RX FIFO Level 0 Register	4803 2060h
64h	PRU_ICSS_MII_RT_RXFLV1	MII RX FIFO Level 1 Register	4803 2064h
68h	PRU_ICSS_MII_RT_TXFLV0	MII TX FIFO Level 0 Register	4803 2068h
6Ch	PRU_ICSS_MII_RT_TXFLV1	MII TX FIFO Level 1 Register	4803 206Ch

4.5.8.1 PRU_ICSS_MII_RT_RXCFG0 Register (Offset = 0h) [reset = 0h]

PRU_ICSS_MII_RT_RXCFG0 is shown in Figure 4-189 and described in Table 4-410.

MII RXCFG 0 REGISTER
This register contains the PRU0 RXCFG configuration variables (RXCFG0) for the RX path.
PRU_ICSS_MII_RT_RXCFG0 is attached to PRU0.
PRU_ICSS_MII_RT_RXCFG0 controls which RX port is attached to PRU0.

Table 4-409. PRU_ICSS_MII_RT_RXCFG0 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 2000h

Figure 4-189. PRU_ICSS_MII_RT_RXCFG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED						RX_L2_EOF_SCLR_DIS	RX_ERR_RAW
R-0h						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RX_SFD_RAW	RX_AUTO_FWD_PRE	RX_BYTE_SWAP	RX_L2_EN	RX_MUX_SEL	RX_CUT_PREAMBLE	RX_DATA_RDY_MODE_DIS	RX_ENABLE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-410. PRU_ICSS_MII_RT_RXCFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9	RX_L2_EOF_SCLR_DIS	R/W	0h	0h: RX_EOF flag in R31 and RXL2 is self cleared by hardware when RXL2 is enabled 1h: RX_EOF flag in R31 and RXL2 is not self cleared by hardware when RXL2 is enabled. To clear this flag, RX_EOF_CLR must be set.
8	RX_ERR_RAW	R/W	0h	0h: Error Raw Mode Disabled. RX_ERR is qualified with RX_DV, meaning RX_DV = 1 before RX_ERR action/event is generated. 1h: Error Raw Mode Enabled. RX_ERR is not qualified with RX_DV, meaning RX_ERR action/event is generated even if RX_DV = 0.
7	RX_SFD_RAW	R/W	0h	0h: SFD Raw Mode Disabled. RX_SFD requires a pattern of 5D. 1h: SFD Raw Mode Enable. The first byte of any pattern after RX_DV assertion will trigger RX_SFD event. The first nibble of the frame (RX_DV = 1) will be in the RX FIFO.

Table 4-410. PRU_ICSS_MII_RT_RXCFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	RX_AUTO_FWD_PRE	R/W	0h	Enables auto-forward of received preamble. When enabled, this will forward the preamble nibbles including the SFD to the TX L1 FIFO that is attached to the PRU. First data byte seen by PRU R31 and/or RX L2 is destination address (DA). **Note: Odd number of preamble nibbles is supported in this mode. For example, 0x55D Note that new RX should only occur after the current TX completes** 0h: Disable 1h: Enable, it must disable RX_CUT_PREAMBLE and TX_AUTO_PREAMBLE
5	RX_BYTE_SWAP	R/W	0h	Defines the order of Byte0/1 placement for RX R31 and RX L2. **Note: that if TX_AUTO_SEQUENCE enabled, this bit cannot get enable since TX_BYTE_SWAP on swaps the PRU output. This bit must be selected/updated when the port is disabled or there is no traffic.** 0h: R31 [15:8]/RXL2 [15:8] = Byte1{Nibble3,Nibble2} R31[7:0]/RXL2 [7:0] = Byte0{Nibble1,Nibble0} 1h: R31 [15:8]/RXL2 [15:8] = Byte0{Nibble1,Nibble0} R31[7:0]/RXL2 [7:0] = Byte1{Nibble3,Nibble2} Nibble0 is the first nibble received.
4	RX_L2_EN	R/W	0h	Enables RX L2 buffer. 0h: Disable (RX L2 can function as generic scratch pad) 1h: Enable
3	RX_MUX_SEL	R/W	0h	Selects receive data source. Typically, the setting for this will not be identical for the two MII receive configuration registers. 0h: MII RX Data from Port 0 (default for PRU_ICSS_MII_RT_RXCFG0) 1h: MII RX Data from Port 1 (default for PRU_ICSS_MII_RT_RXCFG1)
2	RX_CUT_PREAMBLE	R/W	0h	Removes received preamble. 0h: All data from Ethernet PHY are passed on to PRU register. This assumes Ethernet PHY which does not shorten the preamble. 1h: MII interface suppresses preamble and sync frame delimiter. First data byte seen by PRU register is destination address.
1	RX_DATA_RDY_MODE_DIS	R/W	0h	0h: R31, Bit 16 is configured for DATA_RDY mode. 1h: R31, Bit 16 is configured for TX_EOF mode.
0	RX_ENABLE	R/W	0h	Enables the receive traffic currently selected by RX_MUX_SELECT. 0h: Disable 1h: Enable

4.5.8.2 PRU_ICSS_MII_RT_RXCFG1 Register (Offset = 4h) [reset = 8h]

PRU_ICSS_MII_RT_RXCFG1 is shown in Figure 4-190 and described in Table 4-412.

MII RXCFG 1 REGISTER
This register contains the PRU1 RXCFG configuration variables (PRU_ICSS_MII_RT_RXCFG1) for the RX path.
PRU_ICSS_MII_RT_RXCFG1 is attached to PRU1.
PRU_ICSS_MII_RT_RXCFG1 controls which RX port is attached to PRU1.

Table 4-411. PRU_ICSS_MII_RT_RXCFG1 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 2004h

Figure 4-190. PRU_ICSS_MII_RT_RXCFG1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED						RX_L2_EOF_SCLR_DIS	RX_ERR_RAW
R-0h						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RX_SFD_RAW	RX_AUTO_FWD_PRE	RX_BYTE_SWAP	RX_L2_EN	RX_MUX_SEL	RX_CUT_PREAMBLE	RX_DATA_RDY_MODE_DIS	RX_ENABLE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-412. PRU_ICSS_MII_RT_RXCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9	RX_L2_EOF_SCLR_DIS	R/W	0h	0h: RX_EOF flag in R31 and RXL2 is self cleared by hardware when RXL2 is enabled 1h: RX_EOF flag in R31 and RXL2 is not self cleared by hardware when RXL2 is enabled. To clear this flag, RX_EOF_CLR must be set.
8	RX_ERR_RAW	R/W	0h	0h: Error Raw Mode Disabled. RX_ERR is qualified with RX_DV, meaning RX_DV = 1 before RX_ERR action/event is generated. 1h: Error Raw Mode Enabled. RX_ERR is not qualified with RX_DV, meaning RX_ERR action/event is generated even if RX_DV = 0.
7	RX_SFD_RAW	R/W	0h	0h: SFD Raw Mode Disabled. RX_SFD requires a pattern of 5D. 1h: SFD Raw Mode Enable. The first byte of any pattern after RX_DV assertion will trigger RX_SFD event. The first nibble of the frame (RX_DV = 1) will be in the RX FIFO.

Table 4-412. PRU_ICSS_MII_RT_RXCFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	RX_AUTO_FWD_PRE	R/W	0h	Enables auto-forward of received preamble. When enabled, this will forward the preamble nibbles including the SFD to the TX L1 FIFO that is attached to the PRU. First data byte seen by PRU R31 and/or RX L2 is destination address (DA). **Note: Odd number of preamble nibbles is supported in this mode. For example, 0x55D Note that new RX should only occur after the current TX completes** 0h: Disable 1h: Enable, it must disable RX_CUT_PREAMBLE and TX_AUTO_PREAMBLE
5	RX_BYTE_SWAP	R/W	0h	Defines the order of Byte0/1 placement for RX R31 and RX L2. **Note: that if TX_AUTO_SEQUENCE enabled, this bit cannot get enable since TX_BYTE_SWAP on swaps the PRU output. This bit must be selected/updated when the port is disabled or there is no traffic.** 0h: R31 [15:8]/RXL2 [15:8] = Byte1{Nibble3,Nibble2} R31[7:0]/RXL2 [7:0] = Byte0{Nibble1,Nibble0} 1h: R31 [15:8]/RXL2 [15:8] = Byte0{Nibble1,Nibble0} R31[7:0]/RXL2 [7:0] = Byte1{Nibble3,Nibble2} Nibble0 is the first nibble received.
4	RX_L2_EN	R/W	0h	Enables RX L2 buffer. 0h: Disable (RX L2 can function as generic scratch pad) 1h: Enable
3	RX_MUX_SEL	R/W	1h	Selects receive data source. Typically, the setting for this will not be identical for the two MII receive configuration registers. 0h: MII RX Data from Port 0 (default for PRU_ICSS_MII_RT_RXCFG0) 1h: MII RX Data from Port 1 (default for PRU_ICSS_MII_RT_RXCFG1)
2	RX_CUT_PREAMBLE	R/W	0h	Removes received preamble. 0h: All data from Ethernet PHY are passed on to PRU register. This assumes Ethernet PHY which does not shorten the preamble. 1h: MII interface suppresses preamble and sync frame delimiter. First data byte seen by PRU register is destination address.
1	RX_DATA_RDY_MODE_DIS	R/W	0h	0h: R31, Bit 16 is configured for DATA_RDY mode. 1h: R31, Bit 16 is configured for TX_EOF mode.
0	RX_ENABLE	R/W	0h	Enables the receive traffic currently selected by RX_MUX_SELECT. 0h: Disable 1h: Enable

4.5.8.3 PRU_ICSS_MII_RT_TXCFG0 Register (Offset = 10h) [reset = 00400100h]

PRU_ICSS_MII_RT_TXCFG0 is shown in Figure 4-191 and described in Table 4-414.

MII TXCFG 0 REGISTER
This register contains the configuration variables for the transmit path on the MII interface port 0.
PRU_ICSS_MII_RT_TXCFG0 is attached to Port TX0.
PRU_ICSS_MII_RT_TXCFG0 controls which PRU is selected for TX0

Table 4-413. PRU_ICSS_MII_RT_TXCFG0 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 2010h

Figure 4-191. PRU_ICSS_MII_RT_TXCFG0 Register

31	30	29	28	27	26	25	24
RESERVED	TX_CLK_DELAY			RESERVED		TX_START_DELAY	
R-0h	R/W-0h			R-0h		R/W-40h	
23	22	21	20	19	18	17	16
TX_START_DELAY							
R/W-40h							
15	14	13	12	11	10	9	8
RESERVED				TX_32_MODE_EN	PRE_TX_AUTO_ESC_ERR	PRE_TX_AUTO_SEQUENCE	TX_MUX_SEL
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-1h
7	6	5	4	3	2	1	0
RESERVED				TX_BYTE_SWAP	TX_EN_MODE	TX_AUTO_PREAMBLE	TX_ENABLE
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-414. PRU_ICSS_MII_RT_TXCFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30-28	TX_CLK_DELAY	R/W	0h	In order to guarantee the MII_RT IO timing values published in the device data manual, the ICSS_i_VCLK_CLK (where i = 0 or 1) clock must be configured for 200MHz and TX_CLK_DELAY must be set to 6h.
27-26	RESERVED	R	0h	Reserved

Table 4-414. PRU_ICSS_MII_RT_TXCFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25-16	TX_START_DELAY	R/W	40h	Defines the minimum time interval (delay) between receiving the RXDV for the current frame and the start of the transmit interface sending data to the MII interface. Delay value is in units of MII_RT clock cycles, which uses the ICSS_i_VCLK_CLK (default is 200MHz, or 5ns). Default TX_START_DELAY value is 320ns, which is optimized for minimum latency at 16 bit processing. Counter is started with RX_DV signal going active. Transmit interface stops sending data when no more data is written into transmit interface by PRU along with TX_EOF marker bit set. If the TX FIFO has data when the delay expires, then TX will start sending data. But if the TX FIFO is empty, it will not start until the TX FIFO is not empty. It is possible to overflow the TX FIFO with the max delay setting when auto-forwarding is enabled since the time delay is larger than the amount of data it needs to store. As long as TX L1 FIFO overflows, software will need to issue a TX_RESET to reset the TX FIFO. The total delay is 96-byte times (size of TX FIFO), but you need to allow delays for synchronization. Do to this fact, the maximum delay should be 80ns less when auto forwarding is enabled. Therefore, 0x3F0 is the maximum in this configuration.
15-12	RESERVED	R	0h	Reserved
11	TX_32_MODE_EN	R/W	0h	0h: Disable 32-bit Data Push mode. 1h: Enable 32-bit, 16-bit, and 8-bit Data Push mode with TX_MASK disabled. In this mode, the internal PRU R30 byte write strobes are used and not the R31 CMD TX_PUSH mode. Any update to R30 will trigger an TX PUSH. See .
10	RESERVED	R	0h	Reserved
9	TX_AUTO_SEQUENCE	R/W	0h	Enables transmit auto-sequence. Note the transmit data source is determined by TX_MUX_SEL setting. 0h: Disable 1h: Enable, transmit state machine based on events on receiver path that is connected to the respective transmitter. Also, the masking logic is disabled and only the MII data is used.
8	TX_MUX_SEL	R/W	1h	Selects transmit data source. The default/reset setting for TX Port 0 is 1. This setting permits MII TX Port 0 to receive data from PRU1 and the MII TX Port 1 which is connected to PRU0 by default. 0h: Data from PRU0 (default for PRU_ICSS_MII_RT_TXCFG1) 1h: Data from PRU1 (default for PRU_ICSS_MII_RT_TXCFG0)
7-4	RESERVED	R	0h	Reserved

Table 4-414. PRU_ICSS_MII_RT_TXCFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	TX_BYTE_SWAP	R/W	0h	Defines the order of Byte0/1 placement for TX R30. This bit must be selected/updated when the port is disabled or there is no traffic. **0h: If** PRU_ICSS_MII_RT_TXCFG0**/1 [TX_32_MODE_EN] = 0,** R30[15:8] = Byte1{Nibble3,Nibble2} R30[7:0] = Byte0{Nibble1,Nibble0} R30[31:24] = TX_MASK[15:8] R30[23:16] = TX_MASK[7:0] **If** PRU_ICSS_MII_RT_TXCFG0**/1 [TX_32_MODE_EN] = 1,** R30[31:24] = Byte3{Nibble7,Nibble6} R30[23:16] = Byte2{Nibble5,Nibble4} R30[15:8] = Byte1{Nibble3,Nibble2} R30[7:0] = Byte0{Nibble1,Nibble0} **1h: If** PRU_ICSS_MII_RT_TXCFG0**/1 [TX_32_MODE_EN] = 0,** R30[15:8] = Byte0{Nibble1,Nibble0} R30[7:0] = Byte1{Nibble3,Nibble2} R30[31:24] = TX_MASK[7:0] R30[23:16] = TX_MASK[15:8] **If** PRU_ICSS_MII_RT_TXCFG0**/1 [TX_32_MODE_EN] = 1,** (ONLY SUPPORT 32bit push) R30[31:24] = Byte0{Nibble1,Nibble0} R30[23:16] = Byte1{Nibble3,Nibble2} R30[15:8] = Byte2{Nibble5,Nibble4} R30[7:0] = Byte3{Nibble7,Nibble6 **Note Nibble0 is the first nibble received.**
2	TX_EN_MODE	R/W	0h	Enables transmit self clear on TX_EOF event. **Note that iep.cmp[3] must be set before transmission will start for TX0, and iep_cmp[4] for TX1. This is a new dependency, in addition to TX L1 FIFO not empty and TX_START_DELAY expiration, to start transmission.** 0h: Disable 1h: Enable, TX_ENABLE will be clear for a TX_EOF event by itself.
1	TX_AUTO_PREAMBLE	R/W	0h	Transmit data auto-preamble. 0h: PRU will provide full preamble 1h: TX FIFO will insert pre-amble automatically **Note: the TX FIFO does not get preloaded with the preamble until the first write occurs. This can cause the latency to be larger the min latency.**
0	TX_ENABLE	R/W	0h	Enables transmit traffic on TX PORT. If TX_EN_MODE is set, then TX_ENABLE will self clear during a TX_EOF event. Note Software can use this to pre-fill the TX FIFO and then start the TX frame during non-ECS operations. 0h: TX PORT is disabled/stopped immediately 1h: TX PORT is enabled and the frame will start once the IPG counter expired and TX Start Delay counter has expired

4.5.8.4 PRU_ICSS_MII_RT_TXCFG1 Register (Offset = 14h) [reset = 00400000h]

PRU_ICSS_MII_RT_TXCFG1 is shown in Figure 4-192 and described in Table 4-416.

MII TXCFG 1 REGISTER
This register contains the configuration variables for the transmit path on the MII interface port 1.
PRU_ICSS_MII_RT_TXCFG1 is attached to Port TX1.
PRU_ICSS_MII_RT_TXCFG1 controls which PRU is selected for TX1

Table 4-415. PRU_ICSS_MII_RT_TXCFG1 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 2014h

Figure 4-192. PRU_ICSS_MII_RT_TXCFG1 Register

31	30	29	28	27	26	25	24
RESERVED	TX_CLK_DELAY			RESERVED		TX_START_DELAY	
R-0h	R/W-0h			R-0h		R/W-40h	
23	22	21	20	19	18	17	16
TX_START_DELAY							
R/W-40h							
15	14	13	12	11	10	9	8
RESERVED				TX_32_MODE_EN	PRE_TX_AUTO_ESC_ERR	PRE_TX_AUTO_SEQUENCE	TX_MUX_SEL
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED				TX_BYTE_SWAP	TX_EN_MODE	TX_AUTO_PREAMBLE	TX_ENABLE
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-416. PRU_ICSS_MII_RT_TXCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30-28	TX_CLK_DELAY	R/W	0h	In order to guarantee the MII_RT IO timing values published in the device data manual, the ICSS_i_VCLK_CLK (where i = 0 or 1) clock must be configured for 200MHz and TX_CLK_DELAY must be set to 6h.
27-26	RESERVED	R	0h	Reserved

Table 4-416. PRU_ICSS_MII_RT_TXCFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25-16	TX_START_DELAY	R/W	40h	Defines the minimum time interval (delay) between receiving the RXDV for the current frame and the start of the transmit interface sending data to the MII interface. Delay value is in units of MII_RT clock cycles, which uses the ICSS_i_VCLK_CLK, where i = 0 or 1 (default is 200MHz, or 5ns). Default TX_START_DELAY value is 320ns, which is optimized for minimum latency at 16 bit processing. Counter is started with RX_DV signal going active. Transmit interface stops sending data when no more data is written into transmit interface by PRU along with TX_EOF marker bit set. If the TX FIFO has data when the delay expires, then TX will start sending data. But if the TX FIFO is empty, it will not start until the TX FIFO is not empty. It is possible to overflow the TX FIFO with the max delay setting when auto-forwarding is enabled since the time delay is larger than the amount of data it needs to store. As long as TX L1 FIFO overflows, software will need to issue a TX_RESET to reset the TX FIFO. The total delay is 96-byte times (size of TX FIFO), but you need to allow delays for synchronization. Do to this fact, the maximum delay should be 80ns less when auto forwarding is enabled. Therefore, 0x3F0 is the maximum in this configuration.
15-12	RESERVED	R	0h	Reserved
11	TX_32_MODE_EN	R/W	0h	0h: Disable 32-bit Data Push mode. 1h: Enable 32-bit, 16-bit, and 8-bit Data Push mode with TX_MASK disabled. In this mode, the internal PRU R30 byte write strobes are used and not the R31 CMD TX_PUSH mode. Any update to R30 will trigger an TX PUSH.
10	RESERVED	R	0h	Reserved
9	TX_AUTO_SEQUENCE	R/W	0h	Enables transmit auto-sequence. Note the transmit data source is determined by TX_MUX_SEL setting. 0h: Disable 1h: Enable, transmit state machine based on events on receiver path that is connected to the respective transmitter. Also, the masking logic is disabled and only the MII data is used.
8	TX_MUX_SEL	R/W	0h	Selects transmit data source. The default/reset setting for TX Port 0 is 1. This setting permits MII TX Port 0 to receive data from PRU1 and the MII TX Port 1 which is connected to PRU0 by default. 0h: Data from PRU0 (default for PRU_ICSS_MII_RT_TXCFG1) 1h: Data from PRU1 (default for PRU_ICSS_MII_RT_TXCFG0)
7-4	RESERVED	R	0h	Reserved

Table 4-416. PRU_ICSS_MII_RT_TXCFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	TX_BYTE_SWAP	R/W	0h	Defines the order of Byte0/1 placement for TX R30. This bit must be selected/updated when the port is disabled or there is no traffic. 0h: If PRU_ICSS_MII_RT_TXCFG0/1 [TX_32_MODE_EN] = 0, R30[15:8] = Byte1{Nibble3,Nibble2} R30[7:0] = Byte0{Nibble1,Nibble0} R30[31:24] = TX_MASK[15:8] R30[23:16] = TX_MASK[7:0] If PRU_ICSS_MII_RT_TXCFG0/1 [TX_32_MODE_EN] = 1, R30[31:24] = Byte3{Nibble7,Nibble6} R30[23:16] = Byte2{Nibble5,Nibble4} R30[15:8] = Byte1{Nibble3,Nibble2} R30[7:0] = Byte0{Nibble1,Nibble0} 1h: If PRU_ICSS_MII_RT_TXCFG0/1 [TX_32_MODE_EN] = 0, R30[15:8] = Byte0{Nibble1,Nibble0} R30[7:0] = Byte1{Nibble3,Nibble2} R30[31:24] = TX_MASK[7:0] R30[23:16] = TX_MASK[15:8] If PRU_ICSS_MII_RT_TXCFG0/1 [TX_32_MODE_EN] = 1, (ONLY SUPPORT 32bit push) R30[31:24] = Byte0{Nibble1,Nibble0} R30[23:16] = Byte1{Nibble3,Nibble2} R30[15:8] = Byte2{Nibble5,Nibble4} R30[7:0] = Byte3{Nibble7,Nibble6 **Note Nibble0 is the first nibble received.**
2	TX_EN_MODE	R/W	0h	Enables transmit self clear on TX_EOF event. **Note that iep.cmp[3] must be set before transmission will start for TX0, and iep_cmp[4] for TX1. This is a new dependency, in addition to TX L1 FIFO not empty and TX_START_DELAY expiration, to start transmission.** 0h: Disable 1h: Enable, TX_ENABLE will be clear for a TX_EOF event by itself.
1	TX_AUTO_PREAMBLE	R/W	0h	Transmit data auto-preamble. 0h: PRU will provide full preamble 1h: TX FIFO will insert pre-amble automatically **Note: the TX FIFO does not get preloaded with the preamble until the first write occurs. This can cause the latency to be larger the min latency.**
0	TX_ENABLE	R/W	0h	Enables transmit traffic on TX PORT. If TX_EN_MODE is set, then TX_ENABLE will self clear during a TX_EOF event. Note Software can use this to pre-fill the TX FIFO and then start the TX frame during non-ECS operations. 0h: TX PORT is disabled/stopped immediately 1h: TX PORT is enabled and the frame will start once the IPG counter expired and TX Start Delay counter has expired

4.5.8.5 PRU_ICSS_MII_RT_TX_CRC0 Register (Offset = 20h) [reset = 0h]

PRU_ICSS_MII_RT_TX_CRC0 is shown in Figure 4-193 and described in Table 4-418.

MII TXCRC 0 REGISTER
It contains CRC32 which PRU0 reads

Table 4-417. PRU_ICSS_MII_RT_TX_CRC0 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 2020h

Figure 4-193. PRU_ICSS_MII_RT_TX_CRC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_CRC																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-418. PRU_ICSS_MII_RT_TX_CRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TX_CRC	R	0h	FCS (CRC32) data can be read by PRU for diagnostics. It is only valid after 6 clocks after a TX_CRC_HIGH command is given.

4.5.8.6 PRU_ICSS_MII_RT_TX_CRC1 Register (Offset = 24h) [reset = 0h]

PRU_ICSS_MII_RT_TX_CRC1 is shown in Figure 4-194 and described in Table 4-420.

MII TXCRC 1 REGISTER
It contains CRC32 which PRU1 reads

Table 4-419. PRU_ICSS_MII_RT_TX_CRC1 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 2024h

Figure 4-194. PRU_ICSS_MII_RT_TX_CRC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_CRC																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-420. PRU_ICSS_MII_RT_TX_CRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TX_CRC	R	0h	FCS (CRC32) data can be read by PRU for diagnostics. It is only valid after 6 clocks after a TX_CRC_HIGH command is given.

4.5.8.7 PRU_ICSS_MII_RT_TX_IPG0 Register (Offset = 30h) [reset = 28h]

PRU_ICSS_MII_RT_TX_IPG0 is shown in Figure 4-195 and described in Table 4-422.

MII TXIPG 0 REGISTER

Table 4-421. PRU_ICSS_MII_RT_TX_IPG0 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 2030h

Figure 4-195. PRU_ICSS_MII_RT_TX_IPG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						TX_IPG									
R-0h																						R/W-28h									

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-422. PRU_ICSS_MII_RT_TX_IPG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-0	TX_IPG	R/W	28h	Defines the minimum of transmit Inter Packet Gap (IPG) which is the number of ICSS_i_VCLK_CLK (where i = 0 or 1) cycles between the de-assertion of TX_EN and the assertion of TX_EN. The start of the TX will get delayed when the incoming packet IPG is less than defined minimum value. In general, software should program in increments of 8, 40ns to insure the extra delays takes effect.

4.5.8.8 PRU_ICSS_MII_RT_TX_IPG1 Register (Offset = 34h) [reset = 28h]

PRU_ICSS_MII_RT_TX_IPG1 is shown in Figure 4-196 and described in Table 4-424.

MII TXIPG 1 REGISTER

Table 4-423. PRU_ICSS_MII_RT_TX_IPG1 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 2034h

Figure 4-196. PRU_ICSS_MII_RT_TX_IPG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						TX_IPG									
R-0h																						R/W-28h									

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-424. PRU_ICSS_MII_RT_TX_IPG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-0	TX_IPG	R/W	28h	Defines the minimum of transmit Inter Packet Gap (IPG) which is the number of ICSS_i_VCLK_CLK (where i = 0 or 1) cycles between the de-assertion of TX_EN and the assertion of TX_EN. The start of the TX will get delayed when the incoming packet IPG is less than defined minimum value. In general, software should program in increments of 8, 40ns to insure the extra delays takes effect.

4.5.8.9 PRU_ICSS_MII_RT_PRS0 Register (Offset = 38h) [reset = 0h]

PRU_ICSS_MII_RT_PRS0 is shown in Figure 4-197 and described in Table 4-426.

MII PORT STATUS 0 REGISTER

Table 4-425. PRU_ICSS_MII_RT_PRS0 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 2038h

Figure 4-197. PRU_ICSS_MII_RT_PRS0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						MII_CRS	MII_COL
R-0h						R-0h	R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 4-426. PRU_ICSS_MII_RT_PRS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	MII_CRS	R	0h	Read the current state of pr1_mii0_crs
0	MII_COL	R	0h	Read the current state of pr1_mii0_col

4.5.8.10 PRU_ICSS_MII_RT_PRS1 Register (Offset = 3Ch) [reset = 0h]

PRU_ICSS_MII_RT_PRS1 is shown in Figure 4-198 and described in Table 4-428.

MII PORT STATUS 1 REGISTER

Table 4-427. PRU_ICSS_MII_RT_PRS1 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 203Ch

Figure 4-198. PRU_ICSS_MII_RT_PRS1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						MII_CRS	MII_COL
R-0h						R-0h	R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 4-428. PRU_ICSS_MII_RT_PRS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	MII_CRS	R	0h	Read the current state of pr1_mii1_crs
0	MII_COL	R	0h	Read the current state of pr1_mii1_col

4.5.8.11 PRU_ICSS_MII_RT_RX_FRMS0 Register (Offset = 40h) [reset = 05F1003Fh]

PRU_ICSS_MII_RT_RX_FRMS0 is shown in Figure 4-199 and described in Table 4-430.

MII RXFRMS 0 REGISTER

Table 4-429. PRU_ICSS_MII_RT_RX_FRMS0 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 2040h

Figure 4-199. PRU_ICSS_MII_RT_RX_FRMS0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_MAX_FRM																RX_MIN_FRM															
R/W-5F1h																R/W-3Fh															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-430. PRU_ICSS_MII_RT_RX_FRMS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_MAX_FRM	R/W	5F1h	Defines the maximum received frame count. If the total byte count of received frame is more than defined value, RX_MAX_FRM_ERR will get set. 0h = 1 byte after SFD and including CRC N= N+1 bytes after SFD and including CRC. Note if the incoming frame is truncated at the marker, RX_CRC and RX_NIBBLE_ODD will not get asserted.
15-0	RX_MIN_FRM	R/W	3Fh	Defines the minimum received frame count. If the total byte count of received frame is less than defined value, RX_MIN_FRM_ERR will get set. 0h = 1 byte after SFD and including CRC N=N+1 bytes after SFD and including CRC

4.5.8.12 PRU_ICSS_MII_RT_RX_FRMS1 Register (Offset = 44h) [reset = 05F1003Fh]

PRU_ICSS_MII_RT_RX_FRMS1 is shown in Figure 4-200 and described in Table 4-432.

MII RXFRMS 1 REGISTER

Table 4-431. PRU_ICSS_MII_RT_RX_FRMS1 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 2044h

Figure 4-200. PRU_ICSS_MII_RT_RX_FRMS1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_MAX_FRM																RX_MIN_FRM															
R/W-5F1h																R/W-3Fh															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-432. PRU_ICSS_MII_RT_RX_FRMS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_MAX_FRM	R/W	5F1h	Defines the maximum received frame count. If the total byte count of the received frame is more than defined value, RX_MAX_FRM_ERR will get set. 0h = 1 byte after SFD and including CRC N= N+1 bytes after SFD and including CRC Note if the incoming frame is truncated at the marker, RX_CRC and RX_NIBBLE_ODD will not get asserted.
15-0	RX_MIN_FRM	R/W	3Fh	Defines the minimum received frame count. If the total byte count of received frame is less than defined value, RX_MIN_FRM_ERR will get set. 0h = 1 byte after SFD and including CRC N=N+1 bytes after SFD and including CRC

4.5.8.13 PRU_ICSS_MII_RT_RX_PCNT0 Register (Offset = 48h) [reset = E1h]

PRU_ICSS_MII_RT_RX_PCNT0 is shown in Figure 4-201 and described in Table 4-434.

MII RXPCNT 0 REGISTER

Table 4-433. PRU_ICSS_MII_RT_RX_PCNT0 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 2048h

Figure 4-201. PRU_ICSS_MII_RT_RX_PCNT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RX_MAX_PCNT				RX_MIN_PCNT			
R-0h								R/W-Eh				R/W-1h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-434. PRU_ICSS_MII_RT_RX_PCNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-4	RX_MAX_PCNT	R/W	Eh	Defines the maximum number of nibbles until the start of frame delimiter (SFD) event occurred (i.e. matches 0xD5). RX_MAX_PRE_COUNT_ERR will be set if the preamble counts more than the value of RX_MAX_PCNT. If the SFD does not occur within 16 nibbles, the error will assert and the incoming frame will be truncated. 0h: Disabled 1h: Reserved 2h: 4th nibble needs to have built 0xD5 Eh: 16th nibble needs to have built 0xD5 **Note the 16th nibble is transmitted.** **Note for firmware enabling preamble error detection, it is recommended to keep RX_MAX_PCNT disabled (0x0). Otherwise, hardware can truncate a valid frame with too long of a preamble.**
3-0	RX_MIN_PCNT	R/W	1h	Defines the minimum number of nibbles until the start of frame delimiter (SFD) event occurred, which is matched the value 0xD5. RX_MIN_PRE_COUNT_ERR will be set if the preamble counts less than the value of RX_MIN_PCNT. 0h: Disabled 1h: 1 0x5 before 0xD5 2h: 2 0x5 before 0xD5 N min of N 0x5 before 0xD5 **Note it does not need to be "0x5"**

4.5.8.14 PRU_ICSS_MII_RT_RX_PCNT1 Register (Offset = 4Ch) [reset = E1h]

PRU_ICSS_MII_RT_RX_PCNT1 is shown in Figure 4-202 and described in Table 4-436.

MII RXPCNT 1 REGISTER

Table 4-435. PRU_ICSS_MII_RT_RX_PCNT1 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 204Ch

Figure 4-202. PRU_ICSS_MII_RT_RX_PCNT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RX_MAX_PCNT				RX_MIN_PCNT			
R-0h								R/W-Eh				R/W-1h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-436. PRU_ICSS_MII_RT_RX_PCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-4	RX_MAX_PCNT	R/W	Eh	Defines the maximum number of nibbles until the start of frame delimiter (SFD) event occurred (i.e. matches 0xD5). RX_MAX_PRE_COUNT_ERR will be set if the preamble counts more than the value of RX_MAX_PCNT. If the SFD does not occur within 16 nibbles, the error will assert and the incoming frame will be truncated. 0h: Disabled 1h: Reserved 2h: 4th nibble needs to have built 0xD5 Eh: 16th nibble needs to have built 0xD5 **Note the 16th nibble is transmitted** Note for firmware enabling preamble error detection, it is recommended to keep RX_MAX_PCNT disabled (0x0). Otherwise, hardware can truncate a valid frame with too long of a preamble.
3-0	RX_MIN_PCNT	R/W	1h	Defines the minimum number of nibbles until the start of frame delimiter (SFD) event occurred, which is matched the value 0xD5. RX_MIN_PRE_COUNT_ERR will be set if the preamble counts less than the value of RX_MIN_PCNT. 0h Disabled 1h: 1 0x5 before 0xD5 2h: 2 0x5 before 0xD5 N: N 0x5 before 0xD5 **Note it does not need to be "0x5"**

4.5.8.15 PRU_ICSS_MII_RT_RX_ERR0 Register (Offset = 50h) [reset = 0h]

PRU_ICSS_MII_RT_RX_ERR0 is shown in Figure 4-203 and described in Table 4-438.

MII RXERR 0 REGISTER

Table 4-437. PRU_ICSS_MII_RT_RX_ERR0 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 2050h

Figure 4-203. PRU_ICSS_MII_RT_RX_ERR0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				RX_MAX_FRM_ERR	RX_MIN_FRM_ERR	RX_MAX_PCNT_ERR	RX_MIN_PCNT_ERR
R-0h				RWr1Clr-0h	RWr1Clr-0h	RWr1Clr-0h	RWr1Clr-0h

LEGEND: R = Read Only; RWr1Clr = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 4-438. PRU_ICSS_MII_RT_RX_ERR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	RX_MAX_FRM_ERR	RWr1Clr	0h	Error status of received frame is more than the value of RX_MAX_FRM. 0h: No error occurred 1h: Error occurred Write 1 to Clear
2	RX_MIN_FRM_ERR	RWr1Clr	0h	Error status of received frame is less than the value of RX_MIN_FRM. 0h: No error occurred 1h: Error occurred Write 1 to Clear
1	RX_MAX_PCNT_ERR	RWr1Clr	0h	Error status of received preamble nibble is more than the value of RX_MAX_PCNT. 0h: No error occurred 1h: Error occurred Write 1 to Clear
0	RX_MIN_PCNT_ERR	RWr1Clr	0h	Error status of received preamble nibble is less than the value of RX_MIN_PCNT. 0h: No error occurred 1h: Error occurred Write 1 to Clear

4.5.8.16 PRU_ICSS_MII_RT_RX_ERR1 Register (Offset = 54h) [reset = 0h]

PRU_ICSS_MII_RT_RX_ERR1 is shown in Figure 4-204 and described in Table 4-440.

MII RXERR 1 REGISTER

Table 4-439. PRU_ICSS_MII_RT_RX_ERR1 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 2054h

Figure 4-204. PRU_ICSS_MII_RT_RX_ERR1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				RX_MAX_FRM_ERR	RX_MIN_FRM_ERR	RX_MAX_PCNT_ERR	RX_MIN_PCNT_ERR
R-0h				RWr1Clr-0h	RWr1Clr-0h	RWr1Clr-0h	RWr1Clr-0h

LEGEND: R = Read Only; RWr1Clr = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 4-440. PRU_ICSS_MII_RT_RX_ERR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	RX_MAX_FRM_ERR	RWr1Clr	0h	Error status of received frame is more than the value of RX_MAX_FRM_CNT. 0h: No error occurred 1h: Error occurred Write 1 to Clear
2	RX_MIN_FRM_ERR	RWr1Clr	0h	Error status of received frame is less than the value of RX_MIN_FRM_CNT. 0h: No error occurred 1h: Error occurred Write 1 to Clear
1	RX_MAX_PCNT_ERR	RWr1Clr	0h	Error status of received preamble nibble is more than the value of RX_MAX_PCNT. 0h: No error occurred 1h: Error occurred Write 1 to Clear
0	RX_MIN_PCNT_ERR	RWr1Clr	0h	Error status of received preamble nibble is less than the value of RX_MIN_PCNT. 0h: No error occurred 1h: Error occurred Write 1 to Clear

4.5.8.17 PRU_ICSS_MII_RT_RXFLV0 Register (Offset = 60h) [reset = 0h]

PRU_ICSS_MII_RT_RXFLV0 is shown in Figure 4-205 and described in Table 4-442.

MII PRU_ICSS_MII_RT_RXFLV0 REGISTER
This register defines the number of valid bytes in the RX FIFO MII interface port 0.
PRU_ICSS_MII_RT_RXFLV0 is attached to Port RX0.
PRU_ICSS_MII_RT_RXFLV0 controls which PRU is selected for RX0

Table 4-441. PRU_ICSS_MII_RT_RXFLV0 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 2060h

Figure 4-205. PRU_ICSS_MII_RT_RXFLV0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RX_FIFO_LEVEL							
R-0h								RWr1Clr-0h							

LEGEND: R = Read Only; RWr1Clr = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 4-442. PRU_ICSS_MII_RT_RXFLV0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	RX_FIFO_LEVEL	RWr1Clr	0h	Define the number of valid bytes in the RX FIFO. 0h: Empty 1h: 1 Byte/ 2 Nibbles 2h: 2 Byte/ 4 Nibbles .... 32h: 32 Bytes/ 64 Nibbles

4.5.8.18 PRU_ICSS_MII_RT_RXFLV1 Register (Offset = 64h) [reset = 0h]

PRU_ICSS_MII_RT_RXFLV1 is shown in Figure 4-206 and described in Table 4-444.

MII PRU_ICSS_MII_RT_RXFLV1 REGISTER
This register defines the number of valid bytes in the RX FIFO MII interface port 1.
PRU_ICSS_MII_RT_RXFLV1 is attached to Port RX1.
PRU_ICSS_MII_RT_RXFLV1 controls which PRU is selected for RX1

Table 4-443. PRU_ICSS_MII_RT_RXFLV1 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 2064h

Figure 4-206. PRU_ICSS_MII_RT_RXFLV1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RX_FIFO_LEVEL							
R-0h								RWr1Clr-0h							

LEGEND: R = Read Only; RWr1Clr = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 4-444. PRU_ICSS_MII_RT_RXFLV1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	RX_FIFO_LEVEL	RWr1Clr	0h	Define the number of valid bytes in the RX FIFO. 0h: Empty 1h: 1 Byte/ 2 Nibbles 2h: 2 Byte/ 4 Nibbles .... 32h: 32 Bytes/ 64 Nibbles

4.5.8.19 PRU_ICSS_MII_RT_TXFLV0 Register (Offset = 68h) [reset = 0h]

PRU_ICSS_MII_RT_TXFLV0 is shown in Figure 4-207 and described in Table 4-446.

MII PRU_ICSS_MII_RT_TXFLV0 REGISTER
This register defines the number of valid bytes in the TX FIFO MII interface port 0.
PRU_ICSS_MII_RT_TXFLV0 is attached to Port TX0.
PRU_ICSS_MII_RT_TXFLV0 controls which PRU is selected for TX0.

Table 4-445. PRU_ICSS_MII_RT_TXFLV0 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 2068h

Figure 4-207. PRU_ICSS_MII_RT_TXFLV0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TX_FIFO_LEVEL							
R-0h								RWr1Clr-0h							

LEGEND: R = Read Only; RWr1Clr = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 4-446. PRU_ICSS_MII_RT_TXFLV0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	TX_FIFO_LEVEL	RWr1Clr	0h	Define the number of valid nibbles in the TX FIFO. 0h: Empty 1h: 1 Nibble 2h: 1 Byte/ 2 Nibbles .... 128h: 64 Bytes/ 128 Nibbles .... 192h: 96 Bytes/ 192 Nibbles

4.5.8.20 PRU_ICSS_MII_RT_TXFLV1 Register (Offset = 6Ch) [reset = 0h]

PRU_ICSS_MII_RT_TXFLV1 is shown in Figure 4-208 and described in Table 4-448.

MII PRU_ICSS_MII_RT_TXFLV1 REGISTER
This register defines the number of valid bytes in the TX FIFO MII interface port 1.
PRU_ICSS_MII_RT_TXFLV1 is attached to Port TX1.
PRU_ICSS_MII_RT_TXFLV1 controls which PRU is selected for TX1.

Table 4-447. PRU_ICSS_MII_RT_TXFLV1 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 206Ch

Figure 4-208. PRU_ICSS_MII_RT_TXFLV1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TX_FIFO_LEVEL							
R-0h								RWr1Clr-0h							

LEGEND: R = Read Only; RWr1Clr = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 4-448. PRU_ICSS_MII_RT_TXFLV1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	TX_FIFO_LEVEL	RWr1Clr	0h	Define the number of valid nibbles in the TX FIFO. 0h: Empty 1h: 1 Nibble 2h: 1 Byte/ 2 Nibble .... 128h: 64 Bytes/ 128 Nibbles .... 192h: 96 Bytes/ 192 Nibbles

4.5.9 PRU_ICSS_MII_MDIO Registers

PRU_ICSS_MII_MDIO Registers lists the memory-mapped registers for the PRU_ICSS MII MDIO. All register offset addresses not listed in PRU_ICSS_MII_MDIO Registers should be considered as reserved locations and the register contents should not be modified.

Table 4-449. PRU_ICSS MII MDIO Instances

Instance	Base Address
PRU_ICSS_MII_MDIO	4803 2400h

Table 4-450. PRU_ICSS MII MDIO Registers

Offset	Acronym	Register Name	PRU_ICSS_MII_MDIO Physical Address
0h	PRU_ICSS_MII_MDIO_VER	MDIO MODULE VERSION REGISTER	4803 2400h
4h	PRU_ICSS_MII_MDIO_CONTROL	MDIO MODULE CONTROL REGISTER	4803 2404h
8h	PRU_ICSS_MII_MDIO_ALIV	PHY ACKNOWLEDGE STATUS REGISTER	4803 2408h
Ch	PRU_ICSS_MII_MDIO_LINK	PHY LINK STATUS REGISTER	4803 240Ch
10h	PRU_ICSS_MII_MDIO_LINKINTRAW	LINK STATUS CHANGE INTERRUPT REGISTER (RAW VALUE)	4803 2410h
14h	PRU_ICSS_MII_MDIO_LINKINTMASKED	LINK STATUS CHANGE INTERRUPT REGISTER (MASKED VALUE)	4803 2414h
20h	PRU_ICSS_MII_MDIO_USERINTRAW	USER COMMAND COMPLETE INTERRUPT REGISTER (RAW VALUE)	4803 2420h
24h	PRU_ICSS_MII_MDIO_USERINTMASKED	USER COMMAND COMPLETE INTERRUPT REGISTER (MASKED VALUE)	4803 2424h
28h	PRU_ICSS_MII_MDIO_USERINTMASKSET	USER INTERRUPT MASK SET REGISTER	4803 2428h
2Ch	PRU_ICSS_MII_MDIO_USERINTMASKCLR	USER INTERRUPT MASK CLEAR REGISTER	4803 242Ch
80h	PRU_ICSS_MII_MDIO_USERACCESS0	USER ACCESS REGISTER0	4803 2480h
84h	PRU_ICSS_MII_MDIO_USERPHYSEL0	USER PHY SELECT REGISTER0	4803 2484h
88h	PRU_ICSS_MII_MDIO_USERACCESS1	USER ACCESS REGISTER1	4803 2488h
8Ch	PRU_ICSS_MII_MDIO_USERPHYSEL1	USER PHY SELECT REGISTER1	4803 248Ch

4.5.9.1 PRU_ICSS_MII_MDIO_VER Register (Offset = 0h) [reset = -h]

PRU_ICSS_MII_MDIO_VER is shown in Figure 4-209 and described in Table 4-452.

MDIO MODULE VERSION REGISTER

Table 4-451. PRU_ICSS_MII_MDIO_VER Instances

Instance	Physical Address
PRU_ICSS_MII_MDIO	4803 2400h

Figure 4-209. PRU_ICSS_MII_MDIO_VER Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															
R--h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-452. PRU_ICSS_MII_MDIO_VER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REVISION	R	-h	IP Revision.

4.5.9.2 PRU_ICSS_MII_MDIO_CONTROL Register (Offset = 4h) [reset = 810000FFh]

PRU_ICSS_MII_MDIO_CONTROL is shown in Figure 4-210 and described in Table 4-454.

MDIO MODULE CONTROL REGISTER

Table 4-453. PRU_ICSS_MII_MDIO_CONTROL Instances

Instance	Physical Address
PRU_ICSS_MII_MDIO	4803 2404h

Figure 4-210. PRU_ICSS_MII_MDIO_CONTROL Register

31	30	29	28	27	26	25	24
IDLE	ENABLE	RESERVED	HIGHEST_USER_CHANNEL				
R-1h	R/W-0h	R-0h	R-1h				
23	22	21	20	19	18	17	16
RESERVED			PREAMBLE	FAULT	FAULT_DETECT_ENABLE	INT_TEST_ENABLE	RESERVED
R-0h			R/W-0h	RWr1Clr-0h	R/W-0h	R/W-0h	R-0h
15	14	13	12	11	10	9	8
CLKDIV							
R/W-FFh							
7	6	5	4	3	2	1	0
CLKDIV							
R/W-FFh							

LEGEND: R = Read Only; R/W = Read/Write; RWr1Clr = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 4-454. PRU_ICSS_MII_MDIO_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IDLE	R	1h	MDIO state machine IDLE. Set to 1 when the state machine is in the idle state.
30	ENABLE	R/W	0h	Enable control. Writing a 1 to this bit enables the MDIO state machine, writing a 0 disables it. If the MDIO state machine is active at the time it is disabled, it will complete the current operation before halting and setting the idle bit. If using byte access, the enable bit has to be the last bit written in this register.
29	RESERVED	R	0h	Reserved
28-24	HIGHEST_USER_CHANNEL	R	1h	Highest user channel. This field specifies the highest useraccess channel that is available in the module and is currently set to 1. This implies that **MDIOUserAccess1** is the highest available user access channel.
23-21	RESERVED	R	0h	Reserved
20	PREAMBLE	R/W	0h	Preamble disable. Writing a 1 to this bit disables this device from sending MDIO frame preambles.
19	FAULT	RWr1Clr	0h	Fault indicator. This bit is set to 1 if the MDIO pins fail to read back what the device is driving onto them. This indicates a physical layer fault and the module state machine is reset. Writing a 1 to it clears this bit.
18	FAULT_DETECT_ENABLE	R/W	0h	Fault detect enable. This bit has to be set to 1 to enable the physical layer fault detection.

Table 4-454. PRU_ICSS_MII_MDIO_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	INT_TEST_ENABLE	R/W	0h	Interrupt test enable. This bit can be set to 1 to enable the host to set the userint and linkint bits for test purposes.
16	RESERVED	R	0h	Reserved
15-0	CLKDIV	R/W	FFh	Clock Divider. This field specifies the division ratio between CLK and the frequency of MDCLK. MDCLK is disabled when clkdiv is set to 0. MDCLK frequency = clk frequency/(clkdiv+1).

4.5.9.3 PRU_ICSS_MII_MDIO_ALIVE Register (Offset = 8h) [reset = 0h]

PRU_ICSS_MII_MDIO_ALIVE is shown in Figure 4-211 and described in Table 4-456.

PHY ACKNOWLEDGE STATUS REGISTER

Table 4-455. PRU_ICSS_MII_MDIO_ALIVE Instances

Instance	Physical Address
PRU_ICSS_MII_MDIO	4803 2408h

Figure 4-211. PRU_ICSS_MII_MDIO_ALIVE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALIVE																															
RWr1Clr-0h																															

LEGEND: RWr1Clr = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 4-456. PRU_ICSS_MII_MDIO_ALIVE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ALIVE	RWr1Clr	0h	MDIO Alive bitfield. Each of the 32 bits of this register is set if the most recent access to the PHY with address corresponding to the register bit number was acknowledged by the PHY, the bit is reset if the PHY fails to acknowledge the access. Both the user and polling accesses to a PHY will cause the corresponding alive bit to be updated. The alive bits are only meant to be used to give an indication of the presence or not of a PHY with the corresponding address. Writing a 1 to any bit will clear it, writing a 0 has no effect.

4.5.9.4 PRU_ICSS_MII_MDIO_LINK Register (Offset = Ch) [reset = 0h]

PRU_ICSS_MII_MDIO_LINK is shown in Figure 4-212 and described in Table 4-458.

PHY LINK STATUS REGISTER

Table 4-457. PRU_ICSS_MII_MDIO_LINK Instances

Instance	Physical Address
PRU_ICSS_MII_MDIO	4803 240Ch

Figure 4-212. PRU_ICSS_MII_MDIO_LINK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LINK																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-458. PRU_ICSS_MII_MDIO_LINK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LINK	R	0h	MDIO Link state. This register is updated after a read of the Generic Status Register of a PHY. The bit is set if the PHY with the corresponding address has link and the PHY acknowledges the read transaction. The bit is reset if the PHY indicates it does not have link or fails to acknowledge the read transaction. Writes to the register have no effect. In addition, the status of the two PHYs specified in the **MDIOUserPhySel** registers can be determined using the **MLINK** input pins. This is determined by the **linksel** bit in the **MDIOUserPhySel** register.

4.5.9.5 PRU_ICSS_MII_MDIO_LINKINTRAW Register (Offset = 10h) [reset = 0h]

PRU_ICSS_MII_MDIO_LINKINTRAW is shown in Figure 4-213 and described in Table 4-460.

LINK STATUS CHANGE INTERRUPT REGISTER (RAW VALUE)

Table 4-459. PRU_ICSS_MII_MDIO_LINKINTRAW Instances

Instance	Physical Address
PRU_ICSS_MII_MDIO	4803 2410h

Figure 4-213. PRU_ICSS_MII_MDIO_LINKINTRAW Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						LINKINTRAW	
R-0h						RWr1Clr-0h	

LEGEND: R = Read Only; RWr1Clr = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 4-460. PRU_ICSS_MII_MDIO_LINKINTRAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	LINKINTRAW	RWr1Clr	0h	MDIO link change event, raw value. When asserted 1 , a bit indicates that there was an **MDIO link** change event (i.e. change in the MDIOLink register) corresponding to the PHY address in the **MDIOUserPhySel** register. **linkintraw[0] and linkintraw[1]** correspond to **MDIOUserPhySel0 and MDIOUserPhysel1**, respectively. Writing a 1 will clear the event and writing 0 has no effect.**If the int_test bit in the MDIOControl register is set, the host may set the linkintraw bits to a 1 .**This mode may be used for test purposes.

4.5.9.6 PRU_ICSS_MII_MDIO_LINKINTMASKED Register (Offset = 14h) [reset = 0h]

PRU_ICSS_MII_MDIO_LINKINTMASKED is shown in Figure 4-214 and described in Table 4-462.

LINK STATUS CHANGE INTERRUPT REGISTER (MASKED VALUE)

Table 4-461. PRU_ICSS_MII_MDIO_LINKINTMASKED Instances

Instance	Physical Address
PRU_ICSS_MII_MDIO	4803 2414h

Figure 4-214. PRU_ICSS_MII_MDIO_LINKINTMASKED Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						LINKINTMASKED	
R-0h						RWr1Clr-0h	

LEGEND: R = Read Only; RWr1Clr = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 4-462. PRU_ICSS_MII_MDIO_LINKINTMASKED Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	LINKINTMASKED	RWr1Clr	0h	MDIO link change interrupt, masked value. When asserted 1 , a bit indicates that there was an MDIO link change event (i.e. change in the MDIOLink register) corresponding to the PHY address in the MDIOUserPhySel register and the corresponding linkint_enable bit was set. linkintmasked[0] and linkintmasked[1] correspond to MDIOUserPhySel0 and MDIOUserPhysel1, respectively. Writing a 1 will clear the interrupt and writing 0 has no effect. If the int_test bit in the MDIOControl register is set, the host may set the linkint bits to a 1 . This mode may be used for test purposes.

4.5.9.7 PRU_ICSS_MII_MDIO_USERINTRAW Register (Offset = 20h) [reset = 0h]

PRU_ICSS_MII_MDIO_USERINTRAW is shown in Figure 4-215 and described in Table 4-464.

USER COMMAND COMPLETE INTERRUPT REGISTER (RAW VALUE)

Table 4-463. PRU_ICSS_MII_MDIO_USERINTRAW Instances

Instance	Physical Address
PRU_ICSS_MII_MDIO	4803 2420h

Figure 4-215. PRU_ICSS_MII_MDIO_USERINTRAW Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						USERINTRAW	
R-0h						RWr1Clr-0h	

LEGEND: R = Read Only; RWr1Clr = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 4-464. PRU_ICSS_MII_MDIO_USERINTRAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	USERINTRAW	RWr1Clr	0h	Raw value of MDIO user command complete event for MDIOUserAccess1 through MDIOUserAccess0, respectively. When asserted 1 , a bit indicates that the previously scheduled PHY read or write command using that particular MDIOUserAccess register has completed. Writing a 1 will clear the event and writing 0 has no effect. . If the int_test bit in the MDIOControl register is set, the host may set the userintraw bits to a 1 . This mode may be used for test purposes.

4.5.9.8 PRU_ICSS_MII_MDIO_USERINTMASKED Register (Offset = 24h) [reset = 0h]

PRU_ICSS_MII_MDIO_USERINTMASKED is shown in Figure 4-216 and described in Table 4-466.

USER COMMAND COMPLETE INTERRUPT REGISTER (MASKED VALUE)

Table 4-465. PRU_ICSS_MII_MDIO_USERINTMASKED Instances

Instance	Physical Address
PRU_ICSS_MII_MDIO	4803 2424h

Figure 4-216. PRU_ICSS_MII_MDIO_USERINTMASKED Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						USERINTMASKED	
R-0h						RWr1Clr-0h	

LEGEND: R = Read Only; RWr1Clr = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 4-466. PRU_ICSS_MII_MDIO_USERINTMASKED Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	USERINTMASKED	RWr1Clr	0h	Masked value of MDIO user command complete interrupt for MDIOUserAccess1 through MDIOUserAccess0, respectively. When asserted 1 , a bit indicates that the previously scheduled PHY read or write command using that particular MDIOUserAccess register has completed and the corresponding userintmaskset bit is set to 1 . . Writing a 1 will clear the interrupt and writing 0 has no effect. . If the int_test bit in the MDIOControl register is set, the host may set the userintmasked bits to a 1 . This mode may be used for test purposes.

4.5.9.9 PRU_ICSS_MII_MDIO_USERINTMASKSET Register (Offset = 28h) [reset = 0h]

PRU_ICSS_MII_MDIO_USERINTMASKSET is shown in Figure 4-217 and described in Table 4-468.

USER INTERRUPT MASK SET REGISTER

Table 4-467. PRU_ICSS_MII_MDIO_USERINTMASKSET Instances

Instance	Physical Address
PRU_ICSS_MII_MDIO	4803 2428h

Figure 4-217. PRU_ICSS_MII_MDIO_USERINTMASKSET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						USERINTMASKEDSET	
R-0h						R/W1S-0h	

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; *-n* = value after reset

Table 4-468. PRU_ICSS_MII_MDIO_USERINTMASKSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	USERINTMASKEDSET	R/W1S	0h	MDIO user interrupt mask set for userintmasked[1:0], respectively. Writing a bit to 1 will enable MDIO user command complete interrupts for that particular MDIOUserAccess register. MDIO user interrupt for a particular MDIOUserAccess register is disabled if the corresponding bit is 0 . Writing a 0 to this register has no effect.

4.5.9.10 PRU_ICSS_MII_MDIO_USERINTMASKCLR Register (Offset = 2Ch) [reset = 0h]

PRU_ICSS_MII_MDIO_USERINTMASKCLR is shown in Figure 4-218 and described in Table 4-470.

USER INTERRUPT MASK CLEAR REGISTER

Table 4-469. PRU_ICSS_MII_MDIO_USERINTMASKCLR Instances

Instance	Physical Address
PRU_ICSS_MII_MDIO	4803 242Ch

Figure 4-218. PRU_ICSS_MII_MDIO_USERINTMASKCLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						USERINTMASKEDCLR	
R-0h						RWr1Clr-0h	

LEGEND: R = Read Only; RWr1Clr = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 4-470. PRU_ICSS_MII_MDIO_USERINTMASKCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	USERINTMASKEDCLR	RWr1Clr	0h	MDIO user command complete interrupt mask clear for userintmasked[1:0], respectively. Writing a bit to 1 will disable further user command complete interrupts for that particular MDIOUserAccess register. Writing a 0 to this register has no effect.

4.5.9.11 PRU_ICSS_MII_MDIO_USERACCESS0 Register (Offset = 80h) [reset = 0h]

PRU_ICSS_MII_MDIO_USERACCESS0 is shown in Figure 4-219 and described in Table 4-472.

USER ACCESS REGISTER0

Table 4-471. PRU_ICSS_MII_MDIO_USERACCESS0 Instances

Instance	Physical Address
PRU_ICSS_MII_MDIO	4803 2480h

Figure 4-219. PRU_ICSS_MII_MDIO_USERACCESS0 Register

31	30	29	28	27	26	25	24
GO	WRITE	ACK	RESERVED			REGADR	
R/W1S-0h	R/W-0h	R/W-0h	R-0h			R/W-0h	
23	22	21	20	19	18	17	16
REGADR			PHYADR				
R/W-0h			R/W-0h				
15	14	13	12	11	10	9	8
DATA							
R/W-0h							
7	6	5	4	3	2	1	0
DATA							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; *-n* = value after reset

Table 4-472. PRU_ICSS_MII_MDIO_USERACCESS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GO	R/W1S	0h	Go. Writing a 1 to this bit causes the MDIO state machine to perform an MDIO access when it is convenient for it to do so, this is not an instantaneous process. Writing a 0 to this bit has no effect. This bit is write able only if the MDIO state machine is enabled. This bit will self clear when the requested access has been completed. Any writes to the MDIOUserAccess0 register are blocked when the go bit is 1 . If byte access is being used, the go bit should be written last.
30	WRITE	R/W	0h	Write enable. Setting this bit to a 1 causes the MDIO transaction to be a register write, otherwise it is a register read.
29	ACK	R/W	0h	Acknowledge. This bit is set if the PHY acknowledged the read transaction.
28-26	RESERVED	R	0h	Reserved
25-21	REGADR	R/W	0h	Register address. This field specifies the PHY register to be accessed for this transaction.
20-16	PHYADR	R/W	0h	PHY address. This field specifies the PHY to be accessed for this transaction.
15-0	DATA	R/W	0h	User data. The data value read from or to be written to the specified PHY register.

4.5.9.12 PRU_ICSS_MII_MDIO_USERPHYSEL0 Register (Offset = 84h) [reset = 0h]

PRU_ICSS_MII_MDIO_USERPHYSEL0 is shown in Figure 4-220 and described in Table 4-474.

USER PHY SELECT REGISTER0

Table 4-473. PRU_ICSS_MII_MDIO_USERPHYSEL0 Instances

Instance	Physical Address
PRU_ICSS_MII_MDIO	4803 2484h

Figure 4-220. PRU_ICSS_MII_MDIO_USERPHYSEL0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
LINKSEL	LINKINT_ENABLE	RESERVED	PHYADR_MON				
R/W-0h	R/W-0h	R-0h	R/W-0h				

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-474. PRU_ICSS_MII_MDIO_USERPHYSEL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	LINKSEL	R/W	0h	Link status determination select. Set to 1 to determine link status using the MLINK pin. Default value is 0 which implies that the link status is determined by the MDIO state machine.
6	LINKINT_ENABLE	R/W	0h	Link change interrupt enable. Set to 1 to enable link change status interrupts for PHY address specified in phyadr_mon. Link change interrupts are disabled if this bit is set to 0 .
5	RESERVED	R	0h	Reserved
4-0	PHYADR_MON	R/W	0h	PHY address whose link status is to be monitored.

4.5.9.13 PRU_ICSS_MII_MDIO_USERACCESS1 Register (Offset = 88h) [reset = 0h]

PRU_ICSS_MII_MDIO_USERACCESS1 is shown in Figure 4-221 and described in Table 4-476.

USER ACCESS REGISTER1

Table 4-475. PRU_ICSS_MII_MDIO_USERACCESS1 Instances

Instance	Physical Address
PRU_ICSS_MII_MDIO	4803 2488h

Figure 4-221. PRU_ICSS_MII_MDIO_USERACCESS1 Register

31	30	29	28	27	26	25	24
GO	WRITE	ACK	RESERVED			REGADR	
R/W-0h	R/W-0h	R/W-0h	R-0h			R/W-0h	
23	22	21	20	19	18	17	16
REGADR			PHYADR				
R/W-0h			R/W-0h				
15	14	13	12	11	10	9	8
DATA							
R/W-0h							
7	6	5	4	3	2	1	0
DATA							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-476. PRU_ICSS_MII_MDIO_USERACCESS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GO	R/W	0h	Go. Writing a 1 to this bit causes the MDIO state machine to perform an MDIO access when it is convenient for it to do so, this is not an instantaneous process. Writing a 0 to this bit has no effect. This bit is write able only if the MDIO state machine is enabled. This bit will self clear when the requested access has been completed. Any writes to the MDIOUserAccess0 register are blocked when the go bit is 1 . If byte access is being used, the go bit should be written last.
30	WRITE	R/W	0h	Write enable. Setting this bit to a 1 causes the MDIO transaction to be a register write, otherwise it is a register read.
29	ACK	R/W	0h	Acknowledge. This bit is set if the PHY acknowledged the read transaction.
28-26	RESERVED	R	0h	Reserved
25-21	REGADR	R/W	0h	Register address. This field specifies the PHY register to be accessed for this transaction.
20-16	PHYADR	R/W	0h	PHY address. This field specifies the PHY to be accessed for this transaction.
15-0	DATA	R/W	0h	User data. The data value read from or to be written to the specified PHY register.

4.5.9.14 PRU_ICSS_MII_MDIO_USERPHYSEL1 Register (Offset = 8Ch) [reset = 0h]

PRU_ICSS_MII_MDIO_USERPHYSEL1 is shown in Figure 4-222 and described in Table 4-478.

USER PHY SELECT REGISTER1

Table 4-477. PRU_ICSS_MII_MDIO_USERPHYSEL1 Instances

Instance	Physical Address
PRU_ICSS_MII_MDIO	4803 248Ch

Figure 4-222. PRU_ICSS_MII_MDIO_USERPHYSEL1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
LINKSEL	LINKINT_ENABLE	RESERVED	PHYADR_MON				
R/W-0h	R/W-0h	R-0h	R/W-0h				

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-478. PRU_ICSS_MII_MDIO_USERPHYSEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	LINKSEL	R/W	0h	Link status determination select. Set to 1 to determine link status using the MLINK pin. Default value is 0 which implies that the link status is determined by the MDIO state machine.
6	LINKINT_ENABLE	R/W	0h	Link change interrupt enable. Set to 1 to enable link change status interrupts for PHY address specified in phyadr_mon. Link change interrupts are disabled if this bit is set to 0 .
5	RESERVED	R	0h	Reserved
4-0	PHYADR_MON	R/W	0h	PHY address whose link status is to be monitored.

4.5.10 PRU_ICSS_IEP Registers

PRU_ICSS_IEP Registers lists the memory-mapped registers for the PRU_ICSS_IEP module. All register offset addresses not listed in PRU_ICSS_IEP Registers should be considered as reserved locations and the register contents should not be modified.

Table 4-479. PRU_ICSS_IEP Instances

Instance	Base Address
PRU_ICSS_IEP	4802 E000h

Table 4-480. PRU_ICSS_IEP Registers

Offset	Acronym	Register Name	PRU_ICSS_IEP Physical Address
0h	PRU_ICSS_IEP_GLOBAL_CFG	GLOBAL CFG	4802 E000h
4h	PRU_ICSS_IEP_STATUS	STATUS	4802 E004h
8h	PRU_ICSS_IEP_COMPENSATION	COMPENSATION	4802 E008h
Ch	PRU_ICSS_IEP_SLOW_COMPENSATION	SLOW COMPENSATION	4802 E00Ch
10h	PRU_ICSS_IEP_LOW_COUNTER	64 bit count value low	4802 E010h
14h	PRU_ICSS_IEP_HIGH_COUNTER	64 bit count value high	4802 E014h
18h	PRU_ICSS_IEP_CAPTURE_CFG	CAPTURE CFG	4802 E018h
1Ch	PRU_ICSS_IEP_CAPTURE_STATUS	CAPTURE STATUS	4802 E01Ch
20h	PRU_ICSS_IEP_CAPTURE_RISE00	CAPTURE RISE0 low	4802 E020h
24h	PRU_ICSS_IEP_CAPTURE_RISE10	CAPTURE RISE0 high	4802 E024h
28h	PRU_ICSS_IEP_CAPTURE_RISE01	CAPTURE RISE1 low	4802 E028h
2Ch	PRU_ICSS_IEP_CAPTURE_RISE11	CAPTURE RISE1 high	4802 E02Ch
30h	PRU_ICSS_IEP_CAPTURE_RISE02	CAPTURE RISE2 low	4802 E030h
34h	PRU_ICSS_IEP_CAPTURE_RISE12	CAPTURE RISE2 high	4802 E034h
38h	PRU_ICSS_IEP_CAPTURE_RISE03	CAPTURE RISE3 low	4802 E038h
3Ch	PRU_ICSS_IEP_CAPTURE_RISE13	CAPTURE RISE3 high	4802 E03Ch
40h	PRU_ICSS_IEP_CAPTURE_RISE04	CAPTURE RISE4 low	4802 E040h
44h	PRU_ICSS_IEP_CAPTURE_RISE14	CAPTURE RISE4 high	4802 E044h
48h	PRU_ICSS_IEP_CAPTURE_RISE05	CAPTURE RISE5 low	4802 E048h
4Ch	PRU_ICSS_IEP_CAPTURE_RISE15	CAPTURE RISE5 high	4802 E04Ch
50h	PRU_ICSS_IEP_CAPTURE_RISE06	CAPTURE RISE6 low	4802 E050h
54h	PRU_ICSS_IEP_CAPTURE_RISE16	CAPTURE RISE6 high	4802 E054h
58h	PRU_ICSS_IEP_CAPTURE_FALL06	CAPTURE FALL6 low	4802 E058h
5Ch	PRU_ICSS_IEP_CAPTURE_FALL16	CAPTURE FALL6 high	4802 E05Ch
60h	PRU_ICSS_IEP_CAPTURE_RISE07	CAPTURE RISE7 low	4802 E060h
64h	PRU_ICSS_IEP_CAPTURE_RISE17	CAPTURE RISE7 high	4802 E064h
68h	PRU_ICSS_IEP_CAPTURE_FALL07	CAPTURE FALL7 low	4802 E068h
6Ch	PRU_ICSS_IEP_CAPTURE_FALL17	CAPTURE FALL7 high	4802 E06Ch
70h	PRU_ICSS_IEP_COMPARE_CFG	COMPARE CFG	4802 E070h
74h	PRU_ICSS_IEP_COMPARE_STATUS	COMPARE STATUS	4802 E074h
78h	PRU_ICSS_IEP_COMPARE00	COMPARE0 low	4802 E078h
7Ch	PRU_ICSS_IEP_COMPARE10	COMPARE0 high	4802 E07Ch
80h	PRU_ICSS_IEP_COMPARE01	COMPARE1 low	4802 E080h
84h	PRU_ICSS_IEP_COMPARE11	COMPARE1 high	4802 E084h
88h	PRU_ICSS_IEP_COMPARE02	COMPARE2 low	4802 E088h
8Ch	PRU_ICSS_IEP_COMPARE12	COMPARE2 high	4802 E08Ch
90h	PRU_ICSS_IEP_COMPARE03	COMPARE3 low	4802 E090h
94h	PRU_ICSS_IEP_COMPARE13	COMPARE3 high	4802 E094h

Table 4-480. PRU_ICSS_IEP Registers (continued)

Offset	Acronym	Register Name	PRU_ICSS_IEP Physical Address
98h	PRU_ICSS_IEP_COMPARE04	COMPARE4 low	4802 E098h
9Ch	PRU_ICSS_IEP_COMPARE14	COMPARE4 high	4802 E09Ch
A0h	PRU_ICSS_IEP_COMPARE05	COMPARE5 low	4802 E0A0h
A4h	PRU_ICSS_IEP_COMPARE15	COMPARE5 high	4802 E0A4h
A8h	PRU_ICSS_IEP_COMPARE06	COMPARE6 low	4802 E0A8h
ACh	PRU_ICSS_IEP_COMPARE16	COMPARE6 high	4802 E0ACh
B0h	PRU_ICSS_IEP_COMPARE07	COMPARE7 low	4802 E0B0h
B4h	PRU_ICSS_IEP_COMPARE17	COMPARE7 high	4802 E0B4h
B8h	PRU_ICSS_IEP_RXIPG0	Status for the RX port which is attached to PRU0	4802 E0B8h
BCh	PRU_ICSS_IEP_RXIPG1	Status for the RX port which is attached to PRU1	4802 E0BCh
C0h	PRU_ICSS_IEP_COMPARE08	COMPARE8 low	4802 E0C0h
C4h	PRU_ICSS_IEP_COMPARE18	COMPARE8 high	4802 E0C4h
C8h	PRU_ICSS_IEP_COMPARE09	COMPARE9 low	4802 E0C8h
CCh	PRU_ICSS_IEP_COMPARE19	COMPARE9 high	4802 E0CCh
D0h	PRU_ICSS_IEP_COMPARE010	COMPARE10 low	4802 E0D0h
D4h	PRU_ICSS_IEP_COMPARE110	COMPARE10 high	4802 E0D4h
D8h	PRU_ICSS_IEP_COMPARE011	COMPARE11 low	4802 E0D8h
DCh	PRU_ICSS_IEP_COMPARE111	COMPARE11 high	4802 E0DCh
E0h	PRU_ICSS_IEP_COMPARE012	COMPARE12 low	4802 E0E0h
E4h	PRU_ICSS_IEP_COMPARE112	COMPARE12 high	4802 E0E4h
E8h	PRU_ICSS_IEP_COMPARE013	COMPARE13 low	4802 E0E8h
ECh	PRU_ICSS_IEP_COMPARE113	COMPARE13 high	4802 E0ECh
F0h	PRU_ICSS_IEP_COMPARE014	COMPARE14 low	4802 E0F0h
F4h	PRU_ICSS_IEP_COMPARE114	COMPARE14 high	4802 E0F4h
F8h	PRU_ICSS_IEP_COMPARE015	COMPARE15 low	4802 E0F8h
FCh	PRU_ICSS_IEP_COMPARE115	COMPARE15 high	4802 E0FCh
100h	PRU_ICSS_IEP_LOW_COUNTER_RESET_VALUE	Reset value of the Master Counter (lower 32-bits)	4802 E100h
104h	PRU_ICSS_IEP_HIGH_COUNTER_RESET_VALUE	Reset value of the Master Counter (upper 32-bits)	4802 E104h
108h	PRU_ICSS_IEP_PWM	PWM Sync Out	4802 E108h
180h	PRU_ICSS_IEP_SYNC_CTRL	SYNC GENERATION CONTROL	4802 E180h
184h	PRU_ICSS_IEP_SYNC_FIRST_STAT	SYNC GENERATION FIRST EVENT STATUS	4802 E184h
188h	PRU_ICSS_IEP_SYNC0_STAT	SYNC0 STATUS	4802 E188h
18Ch	PRU_ICSS_IEP_SYNC1_STAT	SYNC1 STATUS	4802 E18Ch
190h	PRU_ICSS_IEP_SYNC_PWIDTH	SYNC PULSE WIDTH CONFIGURE	4802 E190h
194h	PRU_ICSS_IEP_SYNC0_PERIOD	SYNC0 PERIOD CONFIGURE	4802 E194h
198h	PRU_ICSS_IEP_SYNC1_DELAY	SYNC1 DELAY	4802 E198h
19Ch	PRU_ICSS_IEP_SYNC_START	SYNC START CONFIGURE	4802 E19Ch
200h	PRU_ICSS_IEP_WD_PREDIV	WATCHDOG PRE-DIVIDER	4802 E200h
204h	PRU_ICSS_IEP_PDI_WD_TIM	PDI WATCHDOG TIMER CONFIGURE	4802 E204h
208h	PRU_ICSS_IEP_PD_WD_TIM	PD WATCHDOG TIMER CONFIGURE	4802 E208h
20Ch	PRU_ICSS_IEP_WD_STATUS	WATCHDOG STATUS	4802 E20Ch
210h	PRU_ICSS_IEP_WD_EXP_CNT	WATCHDOG TIMER EXPIRATION COUNTER	4802 E210h

Table 4-480. PRU_ICSS_IEP Registers (continued)

Offset	Acronym	Register Name	PRU_ICSS_IEP Physical Address
214h	PRU_ICSS_IEP_IEP_WD_CTRL	WATCHDOG CONTROL	4802 E214h
300h	PRU_ICSS_IEP_DIGIO_CTRL	DIGIO Control	4802 E300h
304h	PRU_ICSS_IEP_DIGIO_STATUS	DIGIO Status	4802 E304h
308h	PRU_ICSS_IEP_DIGIO_DATA_IN	DIGIO Data Input	4802 E308h
30Ch	PRU_ICSS_IEP_DIGIO_DATA_IN_RAW	DIGIO Data Input. Direct Sample.	4802 E30Ch
310h	PRU_ICSS_IEP_DIGIO_DATA_OUT	DIGIO Data Output	4802 E310h
314h	PRU_ICSS_IEP_DIGIO_DATA_OUT_EN	DIGIO Data Input which controls tri-state of pr<k>_edio_data_out_en[3:0]	4802 E314h
318h	PRU_ICSS_IEP_DIGIO_EXP	DIGIO, Defines which RX_EOF is used	4802 E318h

4.5.10.1 PRU_ICSS_IEP_GLOBAL_CFG Register (Offset = 0h) [reset = 550h]

PRU_ICSS_IEP_GLOBAL_CFG is shown in Figure 4-223 and described in Table 4-482.

GLOBAL CFG

Table 4-481. PRU_ICSS_IEP_GLOBAL_CFG Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E000h

Figure 4-223. PRU_ICSS_IEP_GLOBAL_CFG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED				CMP_INC			
R-0h				R/W-5h			
15	14	13	12	11	10	9	8
CMP_INC							
R/W-5h							
7	6	5	4	3	2	1	0
DEFAULT_INC				RESERVED			CNT_ENABLE
R/W-5h				R-0h			R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-482. PRU_ICSS_IEP_GLOBAL_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-8	CMP_INC	R/W	5h	Defines the increment value when compensation is active
7-4	DEFAULT_INC	R/W	5h	Defines the default increment value
3-1	RESERVED	R	0h	Reserved
0	CNT_ENABLE	R/W	0h	Counter enable. 0h: Disables the counter. The counter maintains the current count. 1h: Enables the counter.

4.5.10.2 PRU_ICSS_IEP_STATUS Register (Offset = 4h) [reset = 0h]

PRU_ICSS_IEP_STATUS is shown in Figure 4-224 and described in Table 4-484.

STATUS

Table 4-483. PRU_ICSS_IEP_STATUS Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E004h

Figure 4-224. PRU_ICSS_IEP_STATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							CNT_OVF
R-0h							RWr1Clr-0h

LEGEND: R = Read Only; RWr1Clr = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 4-484. PRU_ICSS_IEP_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	CNT_OVF	RWr1Clr	0h	Counter overflow status. 0h: No overflow 1h: Overflow occurred

4.5.10.3 PRU_ICSS_IEP_COMPENSATION Register (Offset = 8h) [reset = 0h]

PRU_ICSS_IEP_COMPENSATION is shown in Figure 4-225 and described in Table 4-486.

COMPENSATION

Table 4-485. PRU_ICSS_IEP_COMPENSATION Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E008h

Figure 4-225. PRU_ICSS_IEP_COMPENSATION Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COMPEN_CNT																							
R-0h								R/W-0h																							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-486. PRU_ICSS_IEP_COMPENSATION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-0	COMPEN_CNT	R/W	0h	Compensation counter. Read returns the current COMPEN_CNT value. 0h: Compensation is disabled and counter will increment by DEFAULT_INC. Nh: Compensation is enabled until COMPEN_CNT decrements to 0. The COMPEN_CNT value decrements on every IEP_CLK cycle. When COMPEN_CNT is greater than 0, then count value increments by CMP_INC. **Note** NOTE: SLOW_COMPEN_CNT MUST be set to zero IF COMPEN_CNT is not zero.

4.5.10.4 PRU_ICSS_IEP_SLOW_COMPENSATION Register (Offset = Ch) [reset = 0h]

PRU_ICSS_IEP_SLOW_COMPENSATION is shown in Figure 4-226 and described in Table 4-488.

SLOW COMPENSATION

Table 4-487. PRU_ICSS_IEP_SLOW_COMPENSATION Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E00Ch

Figure 4-226. PRU_ICSS_IEP_SLOW_COMPENSATION Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLOW_COMPEN_CNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-488. PRU_ICSS_IEP_SLOW_COMPENSATION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SLOW_COMPEN_CNT	R/W	0h	Slow compensation counter. Write 0h: Slow compensation is disabled and counter will increment by DEFAULT_INC. Write Nh: Compensation is enabled for 1 count for every SLOW_COMPEN_CNT cycle, this is free running and continuous until software clears the MMR. For example, SLOW_COMPEN_CNT = 16, every 16 clock cycles the compensation value is used for 1 count. Note: COMPEN_CNT MUST be set to zero IF SLOW_COMPEN_CNT is not zero. Software can read the number of cycles left until the compensation event. For example, software writes SLOW_COMPEN_CNT = 100h and reads SLOW_COMPEN_CNT = 7h. This means in 6 more IEP_CLK cycles before the counter reaches 1h for the compensation event. If software writes SLOW_COMPEN_CNT = 8000h before compensation event, then the counter will reset to 8000h.

4.5.10.5 PRU_ICSS_IEP_LOW_COUNTER Register (Offset = 10h) [reset = 0h]

PRU_ICSS_IEP_LOW_COUNTER is shown in Figure 4-227 and described in Table 4-490.

64 bit count value low

Table 4-489. PRU_ICSS_IEP_LOW_COUNTER Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E010h

Figure 4-227. PRU_ICSS_IEP_LOW_COUNTER Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-490. PRU_ICSS_IEP_LOW_COUNTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	64 bit count value (lower 32-bits). Increments by (DEFAULT_INC or CMP_INC) on every positive edge of ICSS_IEP_CLK (200MHz) or ICSS_VCLK_CLK.

4.5.10.6 PRU_ICSS_IEP_HIGH_COUNTER Register (Offset = 14h) [reset = 0h]

PRU_ICSS_HIGH_COUNTER is shown in Figure 4-228 and described in Table 4-492.

64 bit count value high

Table 4-491. PRU_ICSS_IEP_HIGH_COUNTER Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E014h

Figure 4-228. PRU_ICSS_IEP_HIGH_COUNTER Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-492. PRU_ICSS_IEP_HIGH_COUNTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	64 bit count value (upper 32-bits). Increments by (DEFAULT_INC or CMP_INC) on every positive edge of ICSS_IEP_CLK (200MHz) or ICSS_VCLK_CLK.

4.5.10.7 PRU_ICSS_IEP_CAPTURE_CFG Register (Offset = 18h) [reset = 0001FC00h]

PRU_ICSS_IEP_CAPTURE_CFG is shown in Figure 4-229 and described in Table 4-494.

CAPTURE CFG

Table 4-493. PRU_ICSS_IEP_CAPTURE_CFG Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E018h

Figure 4-229. PRU_ICSS_IEP_CAPTURE_CFG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED						CAP_ASYNC_EN	
R-0h						R/W-7Fh	
15	14	13	12	11	10	9	8
CAP_ASYNC_EN						CAP7F_1ST_EVENT_EN	CAP7R_1ST_EVENT_EN
R/W-7Fh						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
CAP6F_1ST_EVENT_EN	CAP6R_1ST_EVENT_EN	CAP_1ST_EVENT_EN					
R/W-0h	R/W-0h	R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-494. PRU_ICSS_IEP_CAPTURE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	Reserved
17-10	CAP_ASYNC_EN	R/W	7Fh	Synchronization of the capture inputs to the ICSS_IEP_CLK/ ICSS_VCLK_CLK enable. Note if input capture signal is asynchronous to ICSS_IEP_CLK, enabling synchronization will cause the capture contents to be invalid. CAP_ASYNC_EN[n] maps to CAPR[n]. 0h: Disable synchronization 1h: Enable synchronization
9	CAP7F_1ST_EVENT_EN	R/W	0h	Capture 1st Event Enable for CAP7F. 0h: Continues mode. The capture status is not set when events occur. 1h: First Event mode. The capture status is set when the first event occurs and must be cleared before new data will fill buffer. Time value is captured when first event occurs and held until time is read.
8	CAP7R_1ST_EVENT_EN	R/W	0h	Capture 1st Event Enable for CAP7R. 0h: Continues mode. The capture status is not set when events occur. 1h: First Event mode. The capture status is set when the first event occurs and must be cleared before new data will fill buffer. Time value is captured when first event occurs and held until time is read.

Table 4-494. PRU_ICSS_IEP_CAPTURE_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CAP6F_1ST_EVENT_EN	R/W	0h	Capture 1st Event Enable for CAP6F. 0h: Continues mode. The capture status is not set when events occur. 1h: First Event mode. The capture status is set when the first event occurs and must be cleared before new data will fill buffer. Time value is captured when first event occurs and held until time is read.
6	CAP6R_1ST_EVENT_EN	R/W	0h	Capture 1st Event Enable for CAP6R. 0h: Continues mode. The capture status is not set when events occur. 1h: First Event mode. The capture status is set when the first event occurs and must be cleared before new data will fill buffer. Time value is captured when first event occurs and held until time is read.
5-0	CAP_1ST_EVENT_EN	R/W	0h	Capture 1st Event Enable for registers. CAP_1ST_EVENT_EN[n] maps to CAPR[n]. 0h: Continues mode. The capture status is not set when events occur. 1h: First Event mode. The capture status is set when the first event occurs and must be cleared before new data will fill buffer. Time value is captured when first event occurs and held until time is read.

4.5.10.8 PRU_ICSS_IEP_CAPTURE_STATUS Register (Offset = 1Ch) [reset = 0h]

PRU_ICSS_IEP_CAPTURE_STATUS is shown in Figure 4-230 and described in Table 4-496.

CAPTURE STATUS

Table 4-495. PRU_ICSS_IEP_CAPTURE_STATUS Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E01Ch

Figure 4-230. PRU_ICSS_IEP_CAPTURE_STATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
CAP_RAW							
R-0h							
15	14	13	12	11	10	9	8
RESERVED					CAP_VALID	CAPF7_VALID	CAPR7_VALID
R-0h					R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
CAPF6_VALID	CAPR6_VALID	CAPR_VALID					
R-0h	R-0h	R-0h					

LEGEND: R = Read Only; *-n* = value after reset

Table 4-496. PRU_ICSS_IEP_CAPTURE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	CAP_RAW	R	0h	Raw/Current status bit for each of the capture registers, where CAP_RAW[n] maps to CAPR[n]. 0h: Current state is low. 1h: Current state is high.
15-11	RESERVED	R	0h	Reserved
10	CAP_VALID	R	0h	Valid status for capture function. Reflects the ORed result from CAP_STATUS[9:0]. 0h: No Hit for any capture event, i.e., there are all 0 in CAP_STATUS[9:0]. 1h: Hit for 1 or more captures events is pending, i.e., there has at least one value equal to 1 in CAP_STATUS[9:0].
9	CAPF7_VALID	R	0h	Valid status for CAPF7 (fall). 0h: No Hit, no capture event occurred 1h: Hit, capture event occurred
8	CAPR7_VALID	R	0h	Valid status for CAPR7 (rise). 0h: No Hit, no capture event occurred 1h: Hit, capture event occurred
7	CAPF6_VALID	R	0h	Valid status for CAPF6 (fall). 0h: No Hit, no capture event occurred 1h: Hit, capture event occurred
6	CAPR6_VALID	R	0h	Valid status for CAPR6 (rise). 0h: No Hit, no capture event occurred 1h: Hit, capture event occurred

Table 4-496. PRU_ICSS_IEP_CAPTURE_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	CAPR_VALID	R	0h	Valid status bit for each compare register, where CAPR_VALID[n] maps to CAPR[n] (rise). 0h: No Hit, no capture event occurred 1h: Hit, capture event occurred

4.5.10.9 PRU_ICSS_IEP_CAPTURE_RISE00 Register (Offset = 20h) [reset = 0h]

PRU_ICSS_IEP_CAPTURE_RISE00 is shown in Figure 4-231 and described in Table 4-498.

CAPTURE RISE0 low

Table 4-497. PRU_ICSS_IEP_CAPTURE_RISE00 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E020h

Figure 4-231. PRU_ICSS_IEP_CAPTURE_RISE00 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-498. PRU_ICSS_IEP_CAPTURE_RISE00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR	R	0h	Value captured for CAPR<i> (fall) event, where i = 0 to 5. Lower 32-bits.

4.5.10.10 PRU_ICSS_IEP_CAPTURE_RISE10 Register (Offset = 24h) [reset = 0h]

PRU_ICSS_IEP_CAPTURE_RISE10 is shown in Figure 4-232 and described in Table 4-500.

CAPTURE RISE0 high

Table 4-499. PRU_ICSS_IEP_CAPTURE_RISE10 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E024h

Figure 4-232. PRU_ICSS_IEP_CAPTURE_RISE10 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-500. PRU_ICSS_IEP_CAPTURE_RISE10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR	R	0h	Value captured for CAPR<i> (rise) event, where i = 0 to 5. Upper 32-bits.

4.5.10.11 PRU_ICSS_IEP_CAPTURE_RISE01 Register (Offset = 28h) [reset = 0h]

PRU_ICSS_IEP_CAPTURE_RISE01 is shown in Figure 4-233 and described in Table 4-502.

CAPTURE RISE1 low

Table 4-501. PRU_ICSS_IEP_CAPTURE_RISE01 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E028h

Figure 4-233. PRU_ICSS_IEP_CAPTURE_RISE01 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-502. PRU_ICSS_IEP_CAPTURE_RISE01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR	R	0h	Value captured for CAPR<i> (fall) event, where i = 0 to 5. Lower 32-bits.

4.5.10.12 PRU_ICSS_IEP_CAPTURE_RISE11 Register (Offset = 2Ch) [reset = 0h]

PRU_ICSS_IEP_CAPTURE_RISE11 is shown in Figure 4-234 and described in Table 4-504.

CAPTURE RISE1 high

Table 4-503. PRU_ICSS_IEP_CAPTURE_RISE11 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E02Ch

Figure 4-234. PRU_ICSS_IEP_CAPTURE_RISE11 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-504. PRU_ICSS_IEP_CAPTURE_RISE11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR	R	0h	Value captured for CAPR<i> (rise) event, where i = 0 to 5. Upper 32-bits.

4.5.10.13 PRU_ICSS_IEP_CAPTURE_RISE02 Register (Offset = 30h) [reset = 0h]

PRU_ICSS_IEP_CAPTURE_RISE02 is shown in Figure 4-235 and described in Table 4-506.

CAPTURE RISE2 low

Table 4-505. PRU_ICSS_IEP_CAPTURE_RISE02 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E030h

Figure 4-235. PRU_ICSS_IEP_CAPTURE_RISE02 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-506. PRU_ICSS_IEP_CAPTURE_RISE02 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR	R	0h	Value captured for CAPR<i> (fall) event, where i = 0 to 5. Lower 32-bits.

4.5.10.14 PRU_ICSS_IEP_CAPTURE_RISE12 Register (Offset = 34h) [reset = 0h]

PRU_ICSS_IEP_CAPTURE_RISE12 is shown in Figure 4-236 and described in Table 4-508.

CAPTURE RISE2 high

Table 4-507. PRU_ICSS_IEP_CAPTURE_RISE12 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E034h

Figure 4-236. PRU_ICSS_IEP_CAPTURE_RISE12 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-508. PRU_ICSS_IEP_CAPTURE_RISE12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR	R	0h	Value captured for CAPR<i> (rise) event, where i = 0 to 5. Upper 32-bits.

4.5.10.15 PRU_ICSS_IEP_CAPTURE_RISE03 Register (Offset = 38h) [reset = 0h]

PRU_ICSS_IEP_CAPTURE_RISE03 is shown in Figure 4-237 and described in Table 4-510.

CAPTURE RISE3 low

Table 4-509. PRU_ICSS_IEP_CAPTURE_RISE03 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E038h

Figure 4-237. PRU_ICSS_IEP_CAPTURE_RISE03 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-510. PRU_ICSS_IEP_CAPTURE_RISE03 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR	R	0h	Value captured for CAPR<i> (fall) event, where i = 0 to 5. Lower 32-bits.

4.5.10.16 PRU_ICSS_IEP_CAPTURE_RISE13 Register (Offset = 3Ch) [reset = 0h]

PRU_ICSS_IEP_CAPTURE_RISE13 is shown in Figure 4-238 and described in Table 4-512.

CAPTURE RISE3 high

Table 4-511. PRU_ICSS_IEP_CAPTURE_RISE13 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E03Ch

Figure 4-238. PRU_ICSS_IEP_CAPTURE_RISE13 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-512. PRU_ICSS_IEP_CAPTURE_RISE13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR	R	0h	Value captured for CAPR<i> (rise) event, where i = 0 to 5. Upper 32-bits.

4.5.10.17 PRU_ICSS_IEP_CAPTURE_RISE04 Register (Offset = 40h) [reset = 0h]

PRU_ICSS_IEP_CAPTURE_RISE04 is shown in Figure 4-239 and described in Table 4-514.

CAPTURE RISE4 low

Table 4-513. PRU_ICSS_IEP_CAPTURE_RISE04 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E040h

Figure 4-239. PRU_ICSS_IEP_CAPTURE_RISE04 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-514. PRU_ICSS_IEP_CAPTURE_RISE04 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR	R	0h	Value captured for CAPR<i> (fall) event, where i = 0 to 5. Lower 32-bits.

4.5.10.18 PRU_ICSS_IEP_CAPTURE_RISE14 Register (Offset = 44h) [reset = 0h]

PRU_ICSS_IEP_CAPTURE_RISE14 is shown in Figure 4-240 and described in Table 4-516.

CAPTURE RISE4 high

Table 4-515. PRU_ICSS_IEP_CAPTURE_RISE14 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E044h

Figure 4-240. PRU_ICSS_IEP_CAPTURE_RISE14 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-516. PRU_ICSS_IEP_CAPTURE_RISE14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR	R	0h	Value captured for CAPR<i> (rise) event, where i = 0 to 5. Upper 32-bits.

4.5.10.19 PRU_ICSS_IEP_CAPTURE_RISE05 Register (Offset = 48h) [reset = 0h]

PRU_ICSS_IEP_CAPTURE_RISE05 is shown in Figure 4-241 and described in Table 4-518.

CAPTURE RISE5 low

Table 4-517. PRU_ICSS_IEP_CAPTURE_RISE05 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E048h

Figure 4-241. PRU_ICSS_IEP_CAPTURE_RISE05 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-518. PRU_ICSS_IEP_CAPTURE_RISE05 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR	R	0h	Value captured for CAPR<i> (fall) event, where i = 0 to 5. Lower 32-bits.

4.5.10.20 PRU_ICSS_IEP_CAPTURE_RISE15 Register (Offset = 4Ch) [reset = 0h]

PRU_ICSS_IEP_CAPTURE_RISE15 is shown in Figure 4-242 and described in Table 4-520.

CAPTURE RISE5 high

Table 4-519. PRU_ICSS_IEP_CAPTURE_RISE15 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E04Ch

Figure 4-242. PRU_ICSS_IEP_CAPTURE_RISE15 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-520. PRU_ICSS_IEP_CAPTURE_RISE15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR	R	0h	Value captured for CAPR<i> (rise) event, where i = 0 to 5. Upper 32-bits.

4.5.10.21 PRU_ICSS_IEP_CAPTURE_RISE06 Register (Offset = 50h) [reset = 0h]

PRU_ICSS_IEP_CAPTURE_RISE06 is shown in Figure 4-243 and described in Table 4-522.

CAPTURE RISE6 low

Table 4-521. PRU_ICSS_IEP_CAPTURE_RISE06 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E050h

Figure 4-243. PRU_ICSS_IEP_CAPTURE_RISE06 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-522. PRU_ICSS_IEP_CAPTURE_RISE06 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR	R	0h	Value captured for CAPR6 event. Lower 32-bits.

4.5.10.22 PRU_ICSS_IEP_CAPTURE_RISE16 Register (Offset = 54h) [reset = 0h]

PRU_ICSS_IEP_CAPTURE_RISE16 is shown in and described in .

CAPTURE RISE6 high

Table 4-523. PRU_ICSS_IEP_CAPTURE_RISE16 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E054h

Figure 4-244. PRU_ICSS_IEP_CAPTURE_RISE16 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-524. PRU_ICSS_IEP_CAPTURE_RISE16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR	R	0h	Value captured for CAPR6 event. Upper 32-bits.

4.5.10.23 PRU_ICSS_IEP_CAPTURE_FALL06 Register (Offset = 58h) [reset = 0h]

PRU_ICSS_IEP_CAPTURE_FALL06 is shown in Figure 4-245 and described in Table 4-526.

CAPTURE FALL6 low

Table 4-525. PRU_ICSS_IEP_CAPTURE_FALL06 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E058h

Figure 4-245. PRU_ICSS_IEP_CAPTURE_FALL06 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPF																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-526. PRU_ICSS_IEP_CAPTURE_FALL06 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPF	R	0h	Value captured for CAPF6 (fall) event. Lower 32-bits.

4.5.10.24 PRU_ICSS_IEP_CAPTURE_FALL16 Register (Offset = 5Ch) [reset = 0h]

PRU_ICSS_IEP_CAPTURE_FALL16 is shown in Figure 4-246 and described in Table 4-528.

CAPTURE FALL6 high

Table 4-527. PRU_ICSS_IEP_CAPTURE_FALL16 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E05Ch

Figure 4-246. PRU_ICSS_IEP_CAPTURE_FALL16 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPF																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-528. PRU_ICSS_IEP_CAPTURE_FALL16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPF	R	0h	Value captured for CAPF6 (fall) event. Lower 32-bits.

4.5.10.25 PRU_ICSS_IEP_CAPTURE_RISE07 Register (Offset = 60h) [reset = 0h]

PRU_ICSS_IEP_COMPARE_RISE07 is shown in Figure 4-247 and described in Table 4-530.

CAPTURE RISE7 low

Table 4-529. PRU_ICSS_IEP_CAPTURE_RISE07 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E060h

Figure 4-247. PRU_ICSS_IEP_CAPTURE_RISE07 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-530. PRU_ICSS_IEP_CAPTURE_RISE07 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR	R	0h	Value captured for CAPR7 (rise) event. Lower 32-bits.

4.5.10.26 PRU_ICSS_IEP_CAPTURE_RISE17 Register (Offset = 64h) [reset = 0h]

PRU_ICSS_IEP_COMPARE_RISE17 is shown in Figure 4-248 and described in Table 4-532.

CAPTURE RISE7 high

Table 4-531. PRU_ICSS_IEP_CAPTURE_RISE17 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E064h

Figure 4-248. PRU_ICSS_IEP_CAPTURE_RISE17 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-532. PRU_ICSS_IEP_CAPTURE_RISE17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR	R	0h	Value captured for CAPR7 (rise) event. Upper 32-bits.

4.5.10.27 PRU_ICSS_IEP_CAPTURE_FALL07 Register (Offset = 68h) [reset = 0h]

PRU_ICSS_IEP_COMPARE_FALL07 is shown in Figure 4-249 and described in Table 4-534.

CAPTURE FALL7 low

Table 4-533. PRU_ICSS_IEP_CAPTURE_FALL07 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E068h

Figure 4-249. PRU_ICSS_IEP_CAPTURE_FALL07 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPF																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-534. PRU_ICSS_IEP_CAPTURE_FALL07 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPF	R	0h	Value captured for CAPF7 (fall) event. Lower 32-bits.

4.5.10.28 PRU_ICSS_IEP_CAPTURE_FALL17 Register (Offset = 6Ch) [reset = 0h]

PRU_ICSS_IEP_COMPARE_FALL17 is shown in Figure 4-250 and described in Table 4-536.

CAPTURE FALL7 high

Table 4-535. PRU_ICSS_IEP_CAPTURE_FALL17 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E06Ch

Figure 4-250. PRU_ICSS_IEP_CAPTURE_FALL17 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPF																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-536. PRU_ICSS_IEP_CAPTURE_FALL17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPF	R	0h	Value captured for CAPF7 (fall) event. Upper 32-bits.

4.5.10.29 PRU_ICSS_IEP_COMPARE_CFG Register (Offset = 70h) [reset = 0h]

PRU_ICSS_IEP_COMPARE_CFG is shown in Figure 4-251 and described in Table 4-538.

COMPARE CFG

Table 4-537. PRU_ICSS_IEP_COMPARE_CFG Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E070h

Figure 4-251. PRU_ICSS_IEP_COMPARE_CFG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							CMP_EN
R-0h							R/W-0h
15	14	13	12	11	10	9	8
CMP_EN							
R/W-0h							
7	6	5	4	3	2	1	0
CMP_EN							CMP0_RST_CNT_EN
R/W-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-538. PRU_ICSS_IEP_COMPARE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16-1	CMP_EN	R/W	0h	Enable bits for each of the compare registers CMP_EN =0 : Disables CMPj/k Event CMP_EN=1: Enables CMPj/k Event CMP_EN[0] (bit 1 of register) maps to CMP0 event
0	CMP0_RST_CNT_EN	R/W	0h	Enable the reset of the counter 0h: Disable 1h: Enable the reset of the counter if a CMP0 event occurs

4.5.10.30 PRU_ICSS_IEP_COMPARE_STATUS Register (Offset = 74h) [reset = 0h]

PRU_ICSS_IEP_COMPARE_STATUS is shown in Figure 4-252 and described in Table 4-540.

COMPARE STATUS

Table 4-539. PRU_ICSS_IEP_COMPARE_STATUS Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E074h

Figure 4-252. PRU_ICSS_IEP_COMPARE_STATUS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CMP_HIT															
R-0h																RWr1Clr-0h															

LEGEND: R = Read Only; RWr1Clr = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 4-540. PRU_ICSS_IEP_COMPARE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	CMP_HIT	RWr1Clr	0h	Status bit for each of the compare registers. "Match" indicates the current counter is greater than or equal to the compare value. Note it is the firmware's responsibility to handle the IEP overflow. CMP_HITj/k = 0: No match has occured CMP_HITj/k = 1: A match occured. The associated hardware event signal will assert and remain high until the status is cleared.

4.5.10.31 PRU_ICSS_IEP_COMPARE00 Register (Offset = 78h) [reset = 0h]

PRU_ICSS_IEP_COMPARE00 is shown in Figure 4-253 and described in Table 4-542.

COMPARE0 low

Table 4-541. PRU_ICSS_IEP_COMPARE00 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E078h

Figure 4-253. PRU_ICSS_IEP_COMPARE00 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-542. PRU_ICSS_IEP_COMPARE00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 0 low value

4.5.10.32 PRU_ICSS_IEP_COMPARE10 Register (Offset = 7Ch) [reset = 0h]

PRU_ICSS_IEP_COMPARE10 is shown in Figure 4-254 and described in Table 4-544.

COMPARE0 high

Table 4-543. PRU_ICSS_IEP_COMPARE10 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E07Ch

Figure 4-254. PRU_ICSS_IEP_COMPARE10 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-544. PRU_ICSS_IEP_COMPARE10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 0 high value

4.5.10.33 PRU_ICSS_IEP_COMPARE01 Register (Offset = 80h) [reset = 0h]

PRU_ICSS_IEP_COMPARE01 is shown in Figure 4-255 and described in Table 4-546.

COMPARE1 low

Table 4-545. PRU_ICSS_IEP_COMPARE01 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E080h

Figure 4-255. PRU_ICSS_IEP_COMPARE01 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-546. PRU_ICSS_IEP_COMPARE01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 1 low value

4.5.10.34 PRU_ICSS_IEP_COMPARE11 Register (Offset = 84h) [reset = 0h]

PRU_ICSS_IEP_COMPARE11 is shown in Figure 4-256 and described in Table 4-548.

COMPARE1 high

Table 4-547. PRU_ICSS_IEP_COMPARE11 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E084h

Figure 4-256. PRU_ICSS_IEP_COMPARE11 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-548. PRU_ICSS_IEP_COMPARE11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 1 high value

4.5.10.35 PRU_ICSS_IEP_COMPARE02 Register (Offset = 88h) [reset = 0h]

PRU_ICSS_IEP_COMPARE02 is shown in Figure 4-257 and described in Table 4-550.

COMPARE2 low

Table 4-549. PRU_ICSS_IEP_COMPARE02 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E088h

Figure 4-257. PRU_ICSS_IEP_COMPARE02 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-550. PRU_ICSS_IEP_COMPARE02 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 2 low value

4.5.10.36 PRU_ICSS_IEP_COMPARE12 Register (Offset = 8Ch) [reset = 0h]

PRU_ICSS_IEP_COMPARE12 is shown in Figure 4-258 and described in Table 4-552.

COMPARE2 high

Table 4-551. PRU_ICSS_IEP_COMPARE12 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E08Ch

Figure 4-258. PRU_ICSS_IEP_COMPARE12 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-552. PRU_ICSS_IEP_COMPARE12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 2 high value

4.5.10.37 PRU_ICSS_IEP_COMPARE03 Register (Offset = 90h) [reset = 0h]

PRU_ICSS_IEP_COMPARE03 is shown in Figure 4-259 and described in Table 4-554.

COMPARE3 low

Table 4-553. PRU_ICSS_IEP_COMPARE03 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E090h

Figure 4-259. PRU_ICSS_IEP_COMPARE03 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-554. PRU_ICSS_IEP_COMPARE03 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 3 low value

4.5.10.38 PRU_ICSS_IEP_COMPARE13 Register (Offset = 94h) [reset = 0h]

PRU_ICSS_IEP_COMPARE13 is shown in Figure 4-260 and described in Table 4-556.

COMPARE3 high

Table 4-555. PRU_ICSS_IEP_COMPARE13 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E094h

Figure 4-260. PRU_ICSS_IEP_COMPARE13 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-556. PRU_ICSS_IEP_COMPARE13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 3 high value

4.5.10.39 PRU_ICSS_IEP_COMPARE04 Register (Offset = 98h) [reset = 0h]

PRU_ICSS_IEP_COMPARE04 is shown in Figure 4-261 and described in Table 4-558.

COMPARE4 low

Table 4-557. PRU_ICSS_IEP_COMPARE04 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E098h

Figure 4-261. PRU_ICSS_IEP_COMPARE04 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-558. PRU_ICSS_IEP_COMPARE04 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 4 low value

4.5.10.40 PRU_ICSS_IEP_COMPARE14 Register (Offset = 9Ch) [reset = 0h]

PRU_ICSS_IEP_COMPARE14 is shown in Figure 4-262 and described in Table 4-560.

COMPARE4 high

Table 4-559. PRU_ICSS_IEP_COMPARE14 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E09Ch

Figure 4-262. PRU_ICSS_IEP_COMPARE14 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-560. PRU_ICSS_IEP_COMPARE14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 4 high value

4.5.10.41 PRU_ICSS_IEP_COMPARE05 Register (Offset = A0h) [reset = 0h]

PRU_ICSS_IEP_COMPARE05 is shown in Figure 4-263 and described in Table 4-562.

COMPARE5 low

Table 4-561. PRU_ICSS_IEP_COMPARE05 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0A0h

Figure 4-263. PRU_ICSS_IEP_COMPARE05 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-562. PRU_ICSS_IEP_COMPARE05 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 5 low value

4.5.10.42 PRU_ICSS_IEP_COMPARE15 Register (Offset = A4h) [reset = 0h]

PRU_ICSS_IEP_COMPARE15 is shown in Figure 4-264 and described in Table 4-564.

COMPARE5 high

Table 4-563. PRU_ICSS_IEP_COMPARE15 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0A4h

Figure 4-264. PRU_ICSS_IEP_COMPARE15 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-564. PRU_ICSS_IEP_COMPARE15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 5 high value

4.5.10.43 PRU_ICSS_IEP_COMPARE06 Register (Offset = A8h) [reset = 0h]

PRU_ICSS_IEP_COMPARE06 is shown in Figure 4-265 and described in Table 4-566.

COMPARE6 low

Table 4-565. PRU_ICSS_IEP_COMPARE06 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0A8h

Figure 4-265. PRU_ICSS_IEP_COMPARE06 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-566. PRU_ICSS_IEP_COMPARE06 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 6 low value

4.5.10.44 PRU_ICSS_IEP_COMPARE16 Register (Offset = ACh) [reset = 0h]

PRU_ICSS_IEP_COMPARE16 is shown in Figure 4-266 and described in Table 4-568.

COMPARE6 high

Table 4-567. PRU_ICSS_IEP_COMPARE16 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0ACh

Figure 4-266. PRU_ICSS_IEP_COMPARE16 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-568. PRU_ICSS_IEP_COMPARE16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 6 high value

4.5.10.45 PRU_ICSS_IEP_COMPARE07 Register (Offset = B0h) [reset = 0h]

PRU_ICSS_IEP_COMPARE07 is shown in Figure 4-267 and described in Table 4-570.

COMPARE7 low

Table 4-569. PRU_ICSS_IEP_COMPARE07 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0B0h

Figure 4-267. PRU_ICSS_IEP_COMPARE07 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-570. PRU_ICSS_IEP_COMPARE07 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 7 low value

4.5.10.46 PRU_ICSS_IEP_COMPARE17 Register (Offset = B4h) [reset = 0h]

PRU_ICSS_IEP_COMPARE17 is shown in Figure 4-268 and described in Table 4-572.

COMPARE7 high

Table 4-571. PRU_ICSS_IEP_COMPARE17 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0B4h

Figure 4-268. PRU_ICSS_IEP_COMPARE17 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-572. PRU_ICSS_IEP_COMPARE17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 7 high value

4.5.10.47 PRU_ICSS_IEP_RXIPG0 Register (Offset = B8h) [reset = FFFF0000h]

PRU_ICSS_IEP_RXIPG0 is shown in Figure 4-269 and described in Table 4-574.

This register can be used to determine the last RX IPG and the smallest RX IPG. RXIPG0 is the status for the RX port which is attached to PRU0.

Table 4-573. PRU_ICSS_IEP_RXIPG0 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0B8h

Figure 4-269. PRU_ICSS_IEP_RXIPG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_MIN_IPG																RX_IPG															
R/W-FFFFh																R-0h															

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-574. PRU_ICSS_IEP_RXIPG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_MIN_IPG	R/W	FFFFh	Defines the minimum number of ICSS_IEP_CLK/ICCS_VCLK_CLK cycles that is RX_DV is sampled low. It stores the smallest RX_IPG duration. It can be read at any time and gets updated after RX_IPG is updated, if RX_MIN_IPG is greater than RX_IPG.
15-0	RX_IPG	R	0h	Records the current number of ICSS_IEP_CLK/ICSS_VCLK_CLK cycles RX_DV is sampled low. Value is updated after RX_DV transitions from low to high. It will saturate at FFFFh.

4.5.10.48 PRU_ICSS_IEP_RXIPG1 Register (Offset = BCh) [reset = FFFF0000h]

PRU_ICSS_IEP_RXIPG1 is shown in Figure 4-270 and described in Table 4-576.

This register can be used to determine the last RX IPG and the smallest RX IPG. RXIPG1 is the status for the RX port which is attached to PRU1

Table 4-575. PRU_ICSS_IEP_RXIPG1 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0BCh

Figure 4-270. PRU_ICSS_IEP_RXIPG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_MIN_IPG																RX_IPG															
R/W-FFFFh																R-0h															

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-576. PRU_ICSS_IEP_RXIPG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_MIN_IPG	R/W	FFFFh	Defines the minimum number of ICSS_IEP_CLK/ICSS_VCLK_CLK cycles that is RX_DV is sampled low. It stores the smallest RX_IPG duration. It can be read at any time and gets updated after RX_IPG is updated, if RX_MIN_IPG is greater than RX_IPG.
15-0	RX_IPG	R	0h	Records the current number of ICSS_IEP_CLK/ICSS_VCLK_CLK cycles RX_DV is sampled low. Value is updated after RX_DV transitions from low to high. It will saturate at FFFFh.

4.5.10.49 PRU_ICSS_IEP_COMPARE08 Register (Offset = C0h) [reset = 0h]

PRU_ICSS_IEP_COMPARE08 is shown in Figure 4-271 and described in Table 4-578.

COMPARE8 low

Table 4-577. PRU_ICSS_IEP_COMPARE08 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0C0h

Figure 4-271. PRU_ICSS_IEP_COMPARE08 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-578. PRU_ICSS_IEP_COMPARE08 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 8 low value

4.5.10.50 PRU_ICSS_IEP_COMPARE18 Register (Offset = C4h) [reset = 0h]

PRU_ICSS_IEP_COMPARE18 is shown in Figure 4-272 and described in Table 4-580.

COMPARE8 high

Table 4-579. PRU_ICSS_IEP_COMPARE18 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0C4h

Figure 4-272. PRU_ICSS_IEP_COMPARE18 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-580. PRU_ICSS_IEP_COMPARE18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Reset value (upper 32-bits). This register enables SW to define the reset state of the Master Counter, which can be reset by the following events (if enabled): CMP0 event; eHRPWM0_SYNCO event; eHRPWM3_SYNCO event. The RESET_VAL should be in increments of the DEFAULT_INC (default state is 5). For example, 0000_000Ah.

4.5.10.51 PRU_ICSS_IEP_COMPARE09 Register (Offset = C8h) [reset = 0h]

PRU_ICSS_IEP_COMPARE09 is shown in Figure 4-273 and described in Table 4-582.

COMPARE9 low

Table 4-581. PRU_ICSS_IEP_COMPARE09 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0C8h

Figure 4-273. PRU_ICSS_IEP_COMPARE09 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-582. PRU_ICSS_IEP_COMPARE09 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 9 low value

4.5.10.52 PRU_ICSS_IEP_COMPARE19 Register (Offset = CCh) [reset = 0h]

PRU_ICSS_IEP_COMPARE19 is shown in Figure 4-274 and described in Table 4-584.

COMPARE9 high

Table 4-583. PRU_ICSS_IEP_COMPARE19 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0CCh

Figure 4-274. PRU_ICSS_IEP_COMPARE19 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-584. PRU_ICSS_IEP_COMPARE19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 9 high value

4.5.10.53 PRU_ICSS_IEP_COMPARE010 Register (Offset = D0h) [reset = 0h]

PRU_ICSS_IEP_COMPARE010 is shown in Figure 4-275 and described in Table 4-586.

COMPARE10 low

Table 4-585. PRU_ICSS_IEP_COMPARE010 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0D0h

Figure 4-275. PRU_ICSS_IEP_COMPARE010 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-586. PRU_ICSS_IEP_COMPARE010 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 10 low value

4.5.10.54 PRU_ICSS_IEP_COMPARE110 Register (Offset = D4h) [reset = 0h]

PRU_ICSS_IEP_COMPARE110 is shown in Figure 4-276 and described in Table 4-588.

COMPARE10 high

Table 4-587. PRU_ICSS_IEP_COMPARE110 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0D4h

Figure 4-276. PRU_ICSS_IEP_COMPARE110 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-588. PRU_ICSS_IEP_COMPARE110 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 10 high value

4.5.10.55 PRU_ICSS_IEP_COMPARE011 Register (Offset = D8h) [reset = 0h]

PRU_ICSS_IEP_COMPARE011 is shown in Figure 4-277 and described in Table 4-590.

COMPARE11 low

Table 4-589. PRU_ICSS_IEP_COMPARE011 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0D8h

Figure 4-277. PRU_ICSS_IEP_COMPARE011 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-590. PRU_ICSS_IEP_COMPARE011 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 11 low value

4.5.10.56 PRU_ICSS_IEP_COMPARE111 Register (Offset = DCh) [reset = 0h]

PRU_ICSS_IEP_COMPARE111 is shown in Figure 4-278 and described in Table 4-592.

COMPARE11 high

Table 4-591. PRU_ICSS_IEP_COMPARE111 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0DCh

Figure 4-278. PRU_ICSS_IEP_COMPARE111 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-592. PRU_ICSS_IEP_COMPARE111 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 11 high value

4.5.10.57 PRU_ICSS_IEP_COMPARE012 Register (Offset = E0h) [reset = 0h]

PRU_ICSS_IEP_COMPARE012 is shown in Figure 4-279 and described in Table 4-594.

COMPARE12 low

Table 4-593. PRU_ICSS_IEP_COMPARE012 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0E0h

Figure 4-279. PRU_ICSS_IEP_COMPARE012 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-594. PRU_ICSS_IEP_COMPARE012 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 12 low value

4.5.10.58 PRU_ICSS_IEP_COMPARE112 Register (Offset = E4h) [reset = 0h]

PRU_ICSS_IEP_COMPARE112 is shown in Figure 4-280 and described in Table 4-596.

COMPARE12 high

Table 4-595. PRU_ICSS_IEP_COMPARE112 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0E4h

Figure 4-280. PRU_ICSS_IEP_COMPARE112 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-596. PRU_ICSS_IEP_COMPARE112 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 12 high value

4.5.10.59 PRU_ICSS_IEP_COMPARE013 Register (Offset = E8h) [reset = 0h]

PRU_ICSS_IEP_COMPARE013 is shown in Figure 4-281 and described in Table 4-598.

COMPARE13 low

Table 4-597. PRU_ICSS_IEP_COMPARE013 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0E8h

Figure 4-281. PRU_ICSS_IEP_COMPARE013 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-598. PRU_ICSS_IEP_COMPARE013 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 13 low value

4.5.10.60 PRU_ICSS_IEP_COMPARE113 Register (Offset = ECh) [reset = 0h]

PRU_ICSS_IEP_COMPARE113 is shown in Figure 4-282 and described in Table 4-600.

COMPARE13 high

Table 4-599. PRU_ICSS_IEP_COMPARE113 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0ECh

Figure 4-282. PRU_ICSS_IEP_COMPARE113 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-600. PRU_ICSS_IEP_COMPARE113 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 13 high value

4.5.10.61 PRU_ICSS_IEP_COMPARE014 Register (Offset = F0h) [reset = 0h]

PRU_ICSS_IEP_COMPARE014 is shown in Figure 4-283 and described in Table 4-602.

COMPARE14 low

Table 4-601. PRU_ICSS_IEP_COMPARE014 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0F0h

Figure 4-283. PRU_ICSS_IEP_COMPARE014 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-602. PRU_ICSS_IEP_COMPARE014 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 14 low value

4.5.10.62 PRU_ICSS_IEP_COMPARE114 Register (Offset = F4h) [reset = 0h]

PRU_ICSS_IEP_COMPARE114 is shown in Figure 4-284 and described in Table 4-604.

COMPARE14 high

Table 4-603. PRU_ICSS_IEP_COMPARE114 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0F4h

Figure 4-284. PRU_ICSS_IEP_COMPARE114 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-604. PRU_ICSS_IEP_COMPARE114 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 14 high value

4.5.10.63 PRU_ICSS_IEP_COMPARE015 Register (Offset = F8h) [reset = 0h]

PRU_ICSS_IEP_COMPARE015 is shown in Figure 4-285 and described in Table 4-606.

COMPARE15 low

Table 4-605. PRU_ICSS_IEP_COMPARE015 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0F8h

Figure 4-285. PRU_ICSS_IEP_COMPARE015 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-606. PRU_ICSS_IEP_COMPARE015 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 15 low value

4.5.10.64 PRU_ICSS_IEP_COMPARE115 Register (Offset = FCh) [reset = 0h]

PRU_ICSS_IEP_COMPARE115 is shown in Figure 4-286 and described in Table 4-608.

COMPARE15 high

Table 4-607. PRU_ICSS_IEP_COMPARE115 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0FCh

Figure 4-286. PRU_ICSS_IEP_COMPARE115 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-608. PRU_ICSS_IEP_COMPARE115 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 15 high value

4.5.10.65 PRU_ICSS_IEP_LOW_COUNTER_RESET_VALUE Register (Offset = 100h) [reset = 0h]

PRU_ICSS_IEP_LOW_COUNTER_RESET_VALUE is shown in Figure 4-287 and described in Table 4-610.

Reset value of the Master Counter (lower 32-bits).

Table 4-609. PRU_ICSS_IEP_LOW_COUNTER_RESET_VALUE Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E100h

Figure 4-287. PRU_ICSS_IEP_LOW_COUNTER_RESET_VALUE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-610. PRU_ICSS_IEP_LOW_COUNTER_RESET_VALUE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESET_VAL	R/W	0h	Reset value (lower 32-bits). This register enables SW to define the reset state of the Master Counter, which can be reset by the following events (if enabled): CMP0 event; eHRPWM0_SYNCO event; eHRPWM3_SYNCO event. The RESET_VAL should be in increments of the DEFAULT_INC (default state is 5). For example, 0000_000Ah.

4.5.10.66 PRU_ICSS_IEP_HIGH_COUNTER_RESET_VALUE Register (Offset = 104h) [reset = 0h]

PRU_ICSS_IEP_HIGH_COUNTER_RESET is shown in Figure 4-288 and described in Table 4-612.

Reset value of the Master Counter (upper 32-bits).

Table 4-611. PRU_ICSS_IEP_HIGH_COUNTER_RESET_VALUE Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E104h

Figure 4-288. PRU_ICSS_IEP_HIGH_COUNTER_RESET_VALUE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-612. PRU_ICSS_IEP_HIGH_COUNTER_RESET_VALUE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESET_VAL	R/W	0h	This enables SW to define the reset state of the Master counter when it gets reset do to the following 3 possible events if enabled: CMP0 event; eHRPWM0_SYNCO event; eHRPWM3_SYNCO event. It should be in increments of the DEFAULT_INC, default state is 5 For example, 0000_000Ah

4.5.10.67 PRU_ICSS_IEP_PWM Register (Offset = 108h) [reset = 0h]

PRU_ICSS_IEP_PWM is shown in Figure 4-289 and described in Table 4-614.

PWM Sync Out

Table 4-613. PRU_ICSS_IEP_PWM Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E108h

Figure 4-289. PRU_ICSS_IEP_PWM Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				PWM3_HIT	PWM3_RST_CNT_EN	PWM0_HIT	PWM0_RST_CNT_EN
R-0h				RW1Clr-0h	R/W-0h	RW1Clr-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; RW1Clr = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 4-614. PRU_ICSS_IEP_PWM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	PWM3_HIT	RW1Clr	0h	The raw status bit of eHRPWM3_SYNCO event. 0h: No eHRPWM3_SYNCO event 1h: eHRPWM3_SYNCO event occurred Write 1h to Clear.
2	PWM3_RST_CNT_EN	R/W	0h	Enable the reset of the counter by a eHRPWM3_SYNCO event. 0h: Disable 1h: Enable the reset of the counter if a eHRPWM3_SYNCO event occurs
1	PWM0_HIT	RW1Clr	0h	The raw status bit of eHRPWM0_SYNCO event. 0h: No eHRPWM0_SYNCO event 1h: eHRPWM0_SYNCO event occurred Write 1 to Clear.
0	PWM0_RST_CNT_EN	R/W	0h	Enable the reset of the counter by a eHRPWM0_SYNCO event. 0h: Disable 1h: Enable the reset of the counter if a eHRPWM0_SYNCO event occurs

4.5.10.68 PRU_ICSS_IEP_SYNC_CTRL Register (Offset = 180h) [reset = 0h]

PRU_ICSS_IEP_SYNC_CTRL is shown in Figure 4-290 and described in Table 4-616.

SYNC GENERATION CONTROL

Table 4-615. PRU_ICSS_IEP_SYNC_CTRL Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E180h

Figure 4-290. PRU_ICSS_IEP_SYNC_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							SYNC1_IND_EN
R-0h							R/W-0h
7	6	5	4	3	2	1	0
SYNC1_CYCLIC_EN	SYNC1_ACK_EN	SYNC0_CYCLIC_EN	SYNC0_ACK_EN	RESERVED	SYNC1_EN	SYNC0_EN	SYNC_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-616. PRU_ICSS_IEP_SYNC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	SYNC1_IND_EN	R/W	0h	SYNC1 independent mode enable. Independent mode means the SYNC1 signal can be different from SYNC0. 0h: Dependent mode 1h: Independent mode
7	SYNC1_CYCLIC_EN	R/W	0h	SYNC1 single shot or cyclic/auto generation mode enable 0h: Disable, single shot mode 1h: Enable, cyclic generation mode
6	SYNC1_ACK_EN	R/W	0h	SYNC1 acknowledgement mode enable 0h: Disable, SYNC1 will go low after pulse width is met. 1h: Enable, SYNC1 will remain asserted until receiving software acknowledges by reading PRU_ICSS_IEP_SYNC1_STAT which clears on read.
5	SYNC0_CYCLIC_EN	R/W	0h	SYNC0 single shot or cyclic/auto generation mode enable 0h: Disable, single shot mode 1h: Enable, cyclic generation mode
4	SYNC0_ACK_EN	R/W	0h	SYNC0 acknowledgement mode enable 0h: Disable, SYNC0 will go low after pulse width is met. 1h: Enable, SYNC0 will remain asserted until receiving software acknowledges by reading PRU_ICSS_IEP_SYNC0_STAT which clears on read.
3	RESERVED	R	0h	Reserved

Table 4-616. PRU_ICSS_IEP_SYNC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SYNC1_EN	R/W	0h	SYNC1 generation enable 0h: Disable SYNC1 generation. If SYNC1 is low, it will stop immediately. If SYNC1 is high, it will stop after SYNC1 goes low 1h: Enable SYNC1 generation
1	SYNC0_EN	R/W	0h	SYNC0 generation enable 0h: Disable SYNC0 generation. If SYNC0 is low, it will stop immediately If SYNC0 is high, it will stop after SYNC0 goes low 1h: Enable SYNC0 generation
0	SYNC_EN	R/W	0h	SYNC generation enable 0h: Disable the generation and clocking of SYNC0 and SYNC1 logic. If SYNC0 AND SYNC1 is low, it will stop immediately. If SYNC0 OR SYNC1 is high, it will stop after SYCN0 AND SYNC1 goes low. Note that you might get 1 extra high pulse if this is disabled during a high pulse of one and the 2nd pulse goes high before the last pulse low if you do not de-assert sync0_en and sync1_en at the same time. SW should always de-assert both sync1_en and sync0_en at the same time as sync_en is de-asserted 1h: Enables SYNC0 and SYNC1 generation

4.5.10.69 PRU_ICSS_IEP_SYNC_FIRST_STAT Register (Offset = 184h) [reset = 0h]

PRU_ICSS_IEP_SYNC_FIRST_STAT is shown in Figure 4-291 and described in Table 4-618.

SYNC GENERATION FIRST EVENT STATUS

Table 4-617. PRU_ICSS_IEP_SYNC_FIRST_STAT Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E184h

Figure 4-291. PRU_ICSS_IEP_SYNC_FIRST_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						FIRST_SYNC1	FIRST_SYNC0
R-0h						R-0h	R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 4-618. PRU_ICSS_IEP_SYNC_FIRST_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	FIRST_SYNC1	R	0h	SYNC1 First Event status 0h: SYNC1 first event has NOT occurred 1h: SYNC1 first event has occurred. This bits is cleared when sync1_en = 0
0	FIRST_SYNC0	R	0h	SYNC0 First Event status 0h: SYNC0 first event has not occurred 1h: SYNC0 first event has occurred. This bits is cleared when sync0_en = 0

4.5.10.70 PRU_ICSS_IEP_SYNC0_STAT Register (Offset = 188h) [reset = 0h]

PRU_ICSS_IEP_SYNC0_STAT is shown in Figure 4-292 and described in Table 4-620.

SYNC0 STATUS

Table 4-619. PRU_ICSS_IEP_SYNC0_STAT Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E188h

Figure 4-292. PRU_ICSS_IEP_SYNC0_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							SYNC0_PEND
R-0h							RWr1Clr-0h

LEGEND: R = Read Only; RWr1Clr = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 4-620. PRU_ICSS_IEP_SYNC0_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	SYNC0_PEND	RWr1Clr	0h	SYNC0 pending state 0h: SYNC0 is not pending 1h: SYNC0 is pending or has occurred when SYNC0_ACK_EN = 0 (Disable). Write "1" to clear

4.5.10.71 PRU_ICSS_IEP_SYNC1_STAT Register (Offset = 18Ch) [reset = 0h]

PRU_ICSS_IEP_SYNC1_STAT is shown in Figure 4-293 and described in Table 4-622.

SYNC1 STATUS

Table 4-621. PRU_ICSS_IEP_SYNC1_STAT Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E18Ch

Figure 4-293. PRU_ICSS_IEP_SYNC1_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							SYNC1_PEND
R-0h							RWr1Clr-0h

LEGEND: R = Read Only; RWr1Clr = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 4-622. PRU_ICSS_IEP_SYNC1_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	SYNC1_PEND	RWr1Clr	0h	SYNC1 pending state 0h: SYNC1 is not pending 1h: SYNC1 is pending or has occurred when SYNC1_ACK_EN = 0 (Disable). Write "1" to Clear

4.5.10.72 PRU_ICSS_IEP_SYNC_PWIDTH Register (Offset = 190h) [reset = 0h]

PRU_ICSS_IEP_SYNC_PWIDTH is shown in Figure 4-294 and described in Table 4-624.

SYNC PULSE WIDTH CONFIGURE

Table 4-623. PRU_ICSS_IEP_SYNC_PWIDTH Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E190h

Figure 4-294. PRU_ICSS_IEP_SYNC_PWIDTH Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNC_HPW																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-624. PRU_ICSS_IEP_SYNC_PWIDTH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SYNC_HPW	R/W	0h	Defines the number of clock cycles SYNC0/1 will be high. Note if SYNC0/1 is disabled during pulse width time (that is, SYNC_CTRL[SYNC0_EN | SYNC1_EN | SYNC_EN] = 0), the ongoing pulse will be terminated. 0h: 1 clock cycle. 1h: 2 clock cycles. Nh: N+1 clock cycles.

4.5.10.73 PRU_ICSS_IEP_SYNC0_PERIOD Register (Offset = 194h) [reset = 1h]

PRU_ICSS_IEP_SYNC0_PERIOD is shown in Figure 4-295 and described in Table 4-626.

SYNC0 PERIOD CONFIGURE

Table 4-625. PRU_ICSS_IEP_SYNC0_PERIOD Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E194h

Figure 4-295. PRU_ICSS_IEP_SYNC0_PERIOD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNC0_PERIOD																															
R/W-1h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-626. PRU_ICSS_IEP_SYNC0_PERIOD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SYNC0_PERIOD	R/W	1h	Defines the period between the rising edges of SYNC0. 0h: Reserved 1h: 2 clk cycles period N: N+1 clk cycles period

4.5.10.74 PRU_ICSS_IEP_SYNC1_DELAY Register (Offset = 198h) [reset = 0h]

PRU_ICSS_IEP_SYNC1_DELAY is shown in Figure 4-296 and described in Table 4-628.

SYNC1 DELAY

Table 4-627. PRU_ICSS_IEP_SYNC1_DELAY Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E198h

Figure 4-296. PRU_ICSS_IEP_SYNC1_DELAY Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNC1_DELAY																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-628. PRU_ICSS_IEP_SYNC1_DELAY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SYNC1_DELAY	R/W	0h	When SYNC1_IND_EN = 0, defines number of clock cycles from the start of SYNC0 to the start of SYNC1. Note this is the delay before the start of SYNC1. 0h: No delay. 1h: 1 clock cycle delay. Nh: N clock cycles delay. When SYNC1_IND_EN = 1, defines the period between the rising edges of SYNC1. 0h: Reserved. 1h: 2 clock cycles period. Nh: N+1 clock cycles period.

4.5.10.75 PRU_ICSS_IEP_SYNC_START Register (Offset = 19Ch) [reset = 0h]

PRU_ICSS_IEP_SYNC_START is shown in Figure 4-297 and described in Table 4-630.

SYNC START CONFIGURE

Table 4-629. PRU_ICSS_IEP_SYNC_START Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E19Ch

Figure 4-297. PRU_ICSS_IEP_SYNC_START Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNC_START																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-630. PRU_ICSS_IEP_SYNC_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SYNC_START	R/W	0h	Defines the start time after the activation event. 0h: 1 clock cycle delay. Nh: N+1 clock cycles delay.

4.5.10.76 PRU_ICSS_IEP_WD_PREDIV Register (Offset = 200h) [reset = 4E20h]

PRU_ICSS_IEP_WD_PREDIV is shown in Figure 4-298 and described in Table 4-632.

WATCHDOG PRE-DIVIDER

Table 4-631. PRU_ICSS_IEP_WD_PREDIV Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E200h

Figure 4-298. PRU_ICSS_IEP_WD_PREDIV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PRE_DIV															
R-0h																R/W-4E20h															

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-632. PRU_ICSS_IEP_WD_PREDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	PRE_DIV	R/W	4E20h	Defines the number of ICSS_IEP_CLK cycles per WD clock event. Note that the WD clock is a free-running clock. The value 0x4e20 (or 20000) generates a rate of 100 us if ICSS_IEP_CLK is 200 MHz. seconds/(WD event) = (clock cycles per WD event)/(clock cycles per second) = 20000/(200 x [10]^6) = 100us

4.5.10.77 PRU_ICSS_IEP_PDI_WD_TIM Register (Offset = 204h) [reset = 3E8h]

PRU_ICSS_IEP_PDI_WD_TIM is shown in Figure 4-299 and described in Table 4-634.

PDI WATCHDOG TIMER CONFIGURE

Table 4-633. PRU_ICSS_IEP_PDI_WD_TIM Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E204h

Figure 4-299. PRU_ICSS_IEP_PDI_WD_TIM Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PDI_WD_TIME															
R-0h																R/W-3E8h															

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-634. PRU_ICSS_IEP_PDI_WD_TIM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	PDI_WD_TIME	R/W	3E8h	Defines the number of WD ticks (or increments) for PDI WD, that is, the number of WD increments. If PRU_ICSS_IEP_WD_PREDIV[15-0] PRE_DIV is set to 100us, then the value 0x03e8 (or 1000) provides a rate of 100ms. Read returns the current count. Counter is reset by software write to register or when Digital Data In capture occurs. WD is disabled if WD time is set to 0x0. Note when an expiration event occurs, the expiration counter (PDI_EXP_CNT) increments and status (PDI_WD_STAT) clears.

4.5.10.78 PRU_ICSS_IEP_PD_WD_TIM Register (Offset = 208h) [reset = 3E8h]

PRU_ICSS_IEP_PD_WD_TIM is shown in Figure 4-300 and described in Table 4-636.

PD WATCHDOG TIMER CONFIGURE

Table 4-635. PRU_ICSS_IEP_PD_WD_TIM Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E208h

Figure 4-300. PRU_ICSS_IEP_PD_WD_TIM Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PD_WD_TIME															
R-0h																R/W-3E8h															

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-636. PRU_ICSS_IEP_PD_WD_TIM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	PD_WD_TIME	R/W	3E8h	Defines the number of WD ticks (or increments) for PD WD, that is, the number of WD increments. If PRU_ICSS_IEP_WD_PREDIV[15-0] PRE_DIV is set to 100us, then 0x03e8 (or 1000) provides a rate of 100ms. Read returns the current count. Counter is reset by software write to register or every write access to Sync Managers with WD trigger enable bit set. WD is disabled if WD time is set to 0x0. Expiration actions: Increment expiration counter, clear status. Digital Data out forced to zero if pr[k]_edio_oe_ext = 1 and PRU_ICSS_IEP_DIGIO_EXP[0] SW_DATA_OUT_UPDATE = 0.

4.5.10.79 PRU_ICSS_IEP_WD_STATUS Register (Offset = 20Ch) [reset = 00010001h]

PRU_ICSS_IEP_WD_STATUS is shown in Figure 4-301 and described in Table 4-638.

WATCHDOG STATUS

Table 4-637. PRU_ICSS_IEP_WD_STATUS Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E20Ch

Figure 4-301. PRU_ICSS_IEP_WD_STATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							PDI_WD_STAT
R-0h							R-1h
15	14	13	12	11	10	9	8
Galileo BCM 047:RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							PD_WD_STAT
R-0h							R-1h

LEGEND: R = Read Only; *-n* = value after reset

Table 4-638. PRU_ICSS_IEP_WD_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	PDI_WD_STAT	R	1h	WD PDI status. 0h: Expired (PDI_WD_EXP event generated) 1h: Active or disabled
15-1	RESERVED	R	0h	Reserved
0	PD_WD_STAT	R	1h	WD PD status (triggered by Sync Mangers status). 0h: Expired (PD_WD_EXP event generated) 1h: Active or disabled

4.5.10.80 PRU_ICSS_IEP_WD_EXP_CNT Register (Offset = 210h) [reset = 0h]

PRU_ICSS_IEP_WD_EXP_CNT is shown in Figure 4-302 and described in Table 4-640.

WATCHDOG TIMER EXPIRATION COUNTER

Table 4-639. PRU_ICSS_IEP_WD_EXP_CNT Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E210h

Figure 4-302. PRU_ICSS_IEP_WD_EXP_CNT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PD_EXP_CNT								PDI_EXP_CNT							
RWrClr-0h								RWrClr-0h							

LEGEND: R = Read Only; RWrClr = Read/Cleared upon Write; *-n* = value after reset

Table 4-640. PRU_ICSS_IEP_WD_EXP_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	PD_EXP_CNT	RWrClr	0h	WD PD expiration counter. Counter increments on every PD time out and stops at FFh.
7-0	PDI_EXP_CNT	RWrClr	0h	WD PDI expiration counter. Counter increments on every PDI time out and stops at FFh.

4.5.10.81 PRU_ICSS_IEP_WD_CTRL Register (Offset = 214h) [reset = 0h]

PRU_ICSS_IEP_WD_CTRL is shown in Figure 4-303 and described in Table 4-642.

WATCHDOG CONTROL

Table 4-641. PRU_ICSS_IEP_WD_CTRL Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E214h

Figure 4-303. PRU_ICSS_IEP_WD_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							PDI_WD_EN
R-0h							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							PD_WD_EN
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-642. PRU_ICSS_IEP_WD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	PDI_WD_EN	R/W	0h	Watchdog PDI 0h: Disable 1h: Enable
15-1	RESERVED	R	0h	Reserved
0	PD_WD_EN	R/W	0h	Watchdog PD 0h: Disable 1h: Enable

4.5.10.82 PRU_ICSS_IEP_DIGIO_CTRL Register (Offset = 300h) [reset = 4h]

PRU_ICSS_IEP_DIGIO_CTRL is shown in Figure 4-304 and described in Table 4-644.

DIGITAL INPUT OUTPUT CONTROL

Table 4-643. PRU_ICSS_IEP_DIGIO_CTRL Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E300h

Figure 4-304. PRU_ICSS_IEP_DIGIO_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
OUT_MODE		IN_MODE		WD_MODE	BIDI_MODE	OUTVALID_MODE	OUTVALID_POL
R/W-0h		R/W-0h		R/W-0h	R-1h	R/W-0h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-644. PRU_ICSS_IEP_DIGIO_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-6	OUT_MODE	R/W	0h	Defines events that triggers data out to be updated. Note if OUTVALID_MODE is set, then data out is forced to zero if a WD PD expiration occurs (PD_WD_EXP) from the WD block and pr<k>_edio_oe_ext = 1. 0h: PRU0/1_RX_EOF 1h: Reserved 2h: DC SYNC0 event 3h: DC SYNC1 event
5-4	IN_MODE	R/W	0h	Defines event that triggers data in to be sampled 0h: PRU0/1_RX_SOF 1h: Rising edge of external PR<k>_EDC_LATCH0_IN signal 2h: DC rising edge of SYNC0 event 3h: DC rising edge of SYNC1 event
3	WD_MODE	R/W	0h	Defines Watchdog behavior 0h: Outputs are reset immediately after watchdog expires 1h: Outputs are reset with next output event that follows watchdog expiration

Table 4-644. PRU_ICSS_IEP_DIGIO_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	BIDI_MODE	R	1h	Defines the digital input/output direction. NOTE THAT DUE TO INTEGRATION, ACTUAL MODE IS UNIDIRECTIONAL IN THIS DEVICE. 0h: Unidirectional mode: digital input/output direction of pins configured individually 1h: Bidirectional mode: all I/O pins are bidirectional and direction configuration is ignored
1	OUTVALID_MODE	R/W	0h	Defines the outvalid mode behavior. 0h: Output event signaling 1h: Output data is updated if watchdog is triggered. Output data is forced to zero if PD_WD_EXP from the WD block and pr1_edio_oe_ext = 1
0	OUTVALID_POL	R	0h	Defines OUTVALID polarity 0h: Active High 1h: Active Low

4.5.10.83 PRU_ICSS_IEP_DIGIO_STATUS Register (Offset = 304h) [reset = 0h]

PRU_ICSS_IEP_DIGIO_STATUS is shown in Figure 4-305 and described in Table 4-646.

DIGITAL INPUT OUTPUT STATUS

Table 4-645. PRU_ICSS_IEP_DIGIO_STATUS Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E304h

Figure 4-305. PRU_ICSS_IEP_DIGIO_STATUS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIGIO_STAT																															
R-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-646. PRU_ICSS_IEP_DIGIO_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DIGIO_STAT	R	0h	Reserved

4.5.10.84 PRU_ICSS_IEP_DIGIO_DATA_IN Register (Offset = 308h) [reset = -h]

PRU_ICSS_IEP_DIGIO_DATA_IN is shown in Figure 4-306 and described in Table 4-648.

DIGITAL DATA INPUT

Table 4-647. PRU_ICSS_IEP_DIGIO_DATA_IN Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E308h

Figure 4-306. PRU_ICSS_IEP_DIGIO_DATA_IN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA_IN																															
R--h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-648. PRU_ICSS_IEP_DIGIO_DATA_IN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA_IN	R	-h	Data input. Digital inputs can be configured to be sampled in four ways. 1h: Digital inputs are sampled at the start of each frame. The SOF signal can be used externally to update the input data, because the SOF is signaled before input data is sampled. 2h: The sample time can be controlled externally by using them PR<k>_EDC_LATCH0_IN signal. 3h: Digital inputs are sampled at SYNC0 events. 4h: Digital inputs are sampled at SYNC1 events. These can be configured by [5-4] IN_MODE bit field in the PRU_ICSS_IEP_DIGIO_CTRL register.

4.5.10.85 PRU_ICSS_IEP_DIGIO_DATA_IN_RAW Register (Offset = 30Ch) [reset = -h]

PRU_ICSS_IEP_DIGIO_DATA_IN_RAW is shown in Figure 4-307 and described in Table 4-650.

DIGITAL DATA INPUT DIRECT SAMPLE

Table 4-649. PRU_ICSS_IEP_DIGIO_DATA_IN_RAW Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E30Ch

Figure 4-307. PRU_ICSS_IEP_DIGIO_DATA_IN_RAW Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA_IN_RAW																															
R--h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-650. PRU_ICSS_IEP_DIGIO_DATA_IN_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA_IN_RAW	R	-h	Data input which direct sample of PR<k>_EDIO_DATA[0:31]. Only PR<k>_EDIO_DATA[0:3] are exported to device pins in this device.

4.5.10.86 PRU_ICSS_IEP_DIGIO_DATA_OUT Register (Offset = 310h) [reset = 0h]

PRU_ICSS_IEP_DIGIO_DATA_OUT is shown in Figure 4-308 and described in Table 4-652.

DIGITAL DATA OUTPUT

Table 4-651. PRU_ICSS_IEP_DIGIO_DATA_OUT Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E310h

Figure 4-308. PRU_ICSS_IEP_DIGIO_DATA_OUT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA_OUT																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-652. PRU_ICSS_IEP_DIGIO_DATA_OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA_OUT	R/W	0h	Data output. Digital outputs can be configured to be updated in four ways. 1h: Digital outputs are updated at the end of each frame (EOF mode). 2h: Digital outputs are updated with SYNC0 events 3h: Digital outputs are updated SYNC1 events. 4h: Digital outputs are updated at the end of a frame which triggered the Process Data Watchdog. Digital Outputs are only updated if the frame was correct (WD_TRIG mode). These can be configured by [7-6] OUT_MODE bit field in the PRU_ICSS_IEP_DIGIO_CTRL.

4.5.10.87 PRU_ICSS_IEP_DIGIO_DATA_OUT_EN Register (Offset = 314h) [reset = 0h]

PRU_ICSS_IEP_DIGIO_DATA_OUT_EN is shown in Figure 4-309 and described in Table 4-654.

DIGITAL DATA OUT ENABLE

Table 4-653. PRU_ICSS_IEP_DIGIO_DATA_OUT_EN Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E314h

Figure 4-309. PRU_ICSS_IEP_DIGIO_DATA_OUT_EN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA_OUT_EN																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-654. PRU_ICSS_IEP_DIGIO_DATA_OUT_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA_OUT_EN	R/W	0h	Data input which controls tri-state of PR<k>_EDIO_DATA[0:3] 0h: Driver enabled. 1h: Sets outputs to HiZ.

4.5.10.88 PRU_ICSS_IEP_DIGIO_EXP Register (Offset = 318h) [reset = 20h]

PRU_ICSS_IEP_DIGIO_EXP is shown in Figure 4-310 and described in Table 4-656.

DIGIO EXPANSION REGISTER

Table 4-655. PRU_ICSS_IEP_DIGIO_EXP Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E318h

Figure 4-310. PRU_ICSS_IEP_DIGIO_EXP Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED		EOF_SEL	SOF_SEL	SOF_DLY			
R-0h		R/W-0h	R/W-0h	R/W-0h			
7	6	5	4	3	2	1	0
OUTVALID_DLY				RESERVED	SW_OUTVALID	OUTVALID_OVR_EN	SW_DATA_OUT_UPDATE
R/W-2h				R-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-656. PRU_ICSS_IEP_DIGIO_EXP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0h	Reserved
13	EOF_SEL	R/W	0h	Defines which RX_EOF is used for PR<k>_EDIO_DATA_IN[0:3] capture 0h: PRU0_RX_EOF 1h: PRU1_RX_EOF
12	SOF_SEL	R/W	0h	Defines which RX_SOF is used for PR<k>_EDIO_DATA_IN[0:3] capture 0h: PRU0_RX_SOF 1h: PRU1_RX_SOF
11-8	SOF_DLY	R/W	0h	Define the number of iep_clk (ICSS_IEP_CLK) cycle delay of SOF PR<k>_EDIO_DATA_IN[0:3] capture
7-4	OUTVALID_DLY	R/W	2h	Define the number of iep_clk (ICSS_IEP_CLK) cycle delay on assertion of PR<k>_EDIO_OUTVALID. Min is 2 clock cycles. Max is 16 clock cycles
3	RESERVED	R	0h	Reserved
2	SW_OUTVALID	R/W	0h	PR<k>_EDIO_OUTVALID = SW_OUTVALID, only if OUTVALID_OVR_EN is set.
1	OUTVALID_OVR_EN	R/W	0h	Software override enable 0h: Disable override 1h: Enable override

Table 4-656. PRU_ICSS_IEP_DIGIO_EXP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SW_DATA_OUT_UPDATE	R/W	0h	Defines the value of pr<k>_edio_data_out when OUTVALID_OVR_EN = 1. Read 0: Start bit event has not occurred Read 1: Start bit event occurred Write 0: No effect Write 1: Causes an update of pr<k>_edio_data_out by software data out

4.6 R5SS_CORE Registers

Table 4-657. TCMA_CORE0_ROM, TCMA_CORE0_ROM Registers, Base Address=0X0000000000000000, Length=131072

Offset	Length	Register Name	r5ss_core0 Physical Address
0h	32	ROM_START_TCMA	0000 0000h
1FFFCh	32	ROM_END_TCMA	0001 FFFCh

Table 4-658. TCMA_CORE0_RAM, TCMA_CORE0_RAM Registers, Base Address=0X0000000000020000, Length=32768

Offset	Length	Register Name	r5ss_core0 Physical Address	r5ss_core1 Physical Address
0h	32	RAM_START_TCMA	0002 0000h	0002 0000h
7FFCh	32	RAM_END_TCMA	0002 7FFCh	0002 7FFCh

Table 4-659. TCMA_CORE1_RAM, TCMA_CORE1_RAM Registers, Base Address=0X0000000000020000, Length=32768

Offset	Length	Register Name	r5ss_core0 Physical Address	r5ss_core1 Physical Address
0h	32	RAM_START_TCMA	0002 0000h	0002 0000h
7FFCh	32	RAM_END_TCMA	0002 7FFCh	0002 7FFCh

Table 4-660. TCMB_CORE0_RAM, TCMB_CORE0_RAM Registers, Base Address=0X0000000000080000, Length=32768

Offset	Length	Register Name	r5ss_core0 Physical Address	r5ss_core1 Physical Address
0h	32	START	0008 0000h	0008 0000h
17FFCh	32	END	0009 7FFCh	0009 7FFCh

Table 4-661. TCMB_CORE1_RAM, TCMB_CORE1_RAM Registers, Base Address=0X0000000000080000, Length=32768

Offset	Length	Register Name	r5ss_core0 Physical Address	r5ss_core1 Physical Address
0h	32	START	0008 0000h	0008 0000h
17FFCh	32	END	0009 7FFCh	0009 7FFCh

Table 4-662. ECC_AGG_CORE0, ECC_AGG_CORE0 Registers, Base Address=0X0000000053000000, Length=1024

Offset	Length	Register Name	r5ss_core0 Physical Address	r5ss_core1 Physical Address
0h	32	aggr_revision	5300 0000h	5300 4000h
8h	32	ecc_vector	5300 0008h	5300 4008h
Ch	32	misc_status	5300 000Ch	5300 400Ch
10h	32	ecc_wrap_revision	5300 0010h	5300 4010h
14h	32	control	5300 0014h	5300 4014h
18h	32	error_ctrl1	5300 0018h	5300 4018h
1Ch	32	error_ctrl2	5300 001Ch	5300 401Ch
20h	32	error_status1	5300 0020h	5300 4020h
24h	32	error_status2	5300 0024h	5300 4024h
28h	32	error_status3	5300 0028h	5300 4028h
3Ch	32	sec_eoi_reg	5300 003Ch	5300 403Ch
40h	32	sec_status_reg0	5300 0040h	5300 4040h

Table 4-662. ECC_AGG_CORE0, ECC_AGG_CORE0 Registers, Base Address=0X0000000053000000, Length=1024 (continued)

Offset	Length	Register Name	r5ss_core0 Physical Address	r5ss_core1 Physical Address
80h	32	sec_enable_set_reg0	5300 0080h	5300 4080h
C0h	32	sec_enable_clr_reg0	5300 00C0h	5300 40C0h
13Ch	32	ded_eoi_reg	5300 013Ch	5300 413Ch
140h	32	ded_status_reg0	5300 0140h	5300 4140h
180h	32	ded_enable_set_reg0	5300 0180h	5300 4180h
1C0h	32	ded_enable_clr_reg0	5300 01C0h	5300 41C0h
200h	32	aggr_enable_set	5300 0200h	5300 4200h
204h	32	aggr_enable_clr	5300 0204h	5300 4204h
208h	32	aggr_status_set	5300 0208h	5300 4208h
20Ch	32	aggr_status_clr	5300 020Ch	5300 420Ch

Table 4-663. ECC_AGG_CORE1, ECC_AGG_CORE1 Registers, Base Address=0X0000000053003000, Length=1024

Offset	Length	Register Name	r5ss_core0 Physical Address	r5ss_core1 Physical Address
0h	32	aggr_revision	5300 3000h	5300 7000h
8h	32	ecc_vector	5300 3008h	5300 7008h
Ch	32	misc_status	5300 300Ch	5300 700Ch
10h	32	ecc_wrap_revision	5300 3010h	5300 7010h
14h	32	control	5300 3014h	5300 7014h
18h	32	error_ctrl1	5300 3018h	5300 7018h
1Ch	32	error_ctrl2	5300 301Ch	5300 701Ch
20h	32	error_status1	5300 3020h	5300 7020h
24h	32	error_status2	5300 3024h	5300 7024h
28h	32	error_status3	5300 3028h	5300 7028h
3Ch	32	sec_eoi_reg	5300 303Ch	5300 703Ch
40h	32	sec_status_reg0	5300 3040h	5300 7040h
80h	32	sec_enable_set_reg0	5300 3080h	5300 7080h
C0h	32	sec_enable_clr_reg0	5300 30C0h	5300 70C0h
13Ch	32	ded_eoi_reg	5300 313Ch	5300 713Ch
140h	32	ded_status_reg0	5300 3140h	5300 7140h
180h	32	ded_enable_set_reg0	5300 3180h	5300 7180h
1C0h	32	ded_enable_clr_reg0	5300 31C0h	5300 71C0h
200h	32	aggr_enable_set	5300 3200h	5300 7200h
204h	32	aggr_enable_clr	5300 3204h	5300 7204h
208h	32	aggr_status_set	5300 3208h	5300 7208h
20Ch	32	aggr_status_clr	5300 320Ch	5300 720Ch

Table 4-664. CCMR, CCMR Registers, Base Address=0X0000000053210000, Length=4096

Offset	Length	Register Name	r5ss_core0 Physical Address	r5ss_core1 Physical Address
0h	32	CCMSR1	5321 0000h	5321 1000h
4h	32	CCMKEYR1	5321 0004h	5321 1004h
8h	32	CCMSR2	5321 0008h	5321 1008h
Ch	32	CCMKEYR2	5321 000Ch	5321 100Ch
10h	32	CCMSR3	5321 0010h	5321 1010h
14h	32	CCMKEYR3	5321 0014h	5321 1014h

Table 4-664. CCMR, CCMR Registers, Base Address=0X0000000053210000, Length=4096 (continued)

Offset	Length	Register Name	r5ss_core0 Physical Address	r5ss_core1 Physical Address
18h	32	CCMPOLCNTRL	5321 0018h	5321 1018h
2Ch	32	CCMSR5	5321 002Ch	5321 102Ch
30h	32	CCMKEYR5	5321 0030h	5321 1030h
34h	32	CCMSR6	5321 0034h	5321 1034h
38h	32	CCMKEYR6	5321 0038h	5321 1038h

Table 4-665. STC, STC Registers, Base Address=0X0000000053500000, Length=512

Offset	Length	Register Name	r5ss_core0 Physical Address	r5ss_core1 Physical Address
0h	32	STCGCR0	5350 0000h	5351 0000h
4h	32	STCGCR1	5350 0004h	5351 0004h
8h	32	STCTPR	5350 0008h	5351 0008h
Ch	32	STC_CADDR	5350 000Ch	5351 000Ch
10h	32	STCCICR	5350 0010h	5351 0010h
14h	32	STCGSTAT	5350 0014h	5351 0014h
18h	32	STCFSTAT	5350 0018h	5351 0018h
1Ch	32	STCSCSCR	5350 001Ch	5351 001Ch
20h	32	STC_CADDR2	5350 0020h	5351 0020h
24h	32	STC_CLKDIV	5350 0024h	5351 0024h
28h	32	STC_SEGPLR	5350 0028h	5351 0028h
2Ch	32	SEG0_START_ADDR	5350 002Ch	5351 002Ch
30h	32	SEG1_START_ADDR	5350 0030h	5351 0030h
34h	32	SEG2_START_ADDR	5350 0034h	5351 0034h
38h	32	SEG3_START_ADDR	5350 0038h	5351 0038h
3Ch	32	CORE1_CURMISR_0	5350 003Ch	5351 003Ch
40h	32	CORE1_CURMISR_1	5350 0040h	5351 0040h
44h	32	CORE1_CURMISR_2	5350 0044h	5351 0044h
48h	32	CORE1_CURMISR_3	5350 0048h	5351 0048h
4Ch	32	CORE1_CURMISR_4	5350 004Ch	5351 004Ch
50h	32	CORE1_CURMISR_5	5350 0050h	5351 0050h
54h	32	CORE1_CURMISR_6	5350 0054h	5351 0054h
58h	32	CORE1_CURMISR_7	5350 0058h	5351 0058h
5Ch	32	CORE1_CURMISR_8	5350 005Ch	5351 005Ch
60h	32	CORE1_CURMISR_9	5350 0060h	5351 0060h
64h	32	CORE1_CURMISR_10	5350 0064h	5351 0064h
68h	32	CORE1_CURMISR_11	5350 0068h	5351 0068h
6Ch	32	CORE1_CURMISR_12	5350 006Ch	5351 006Ch
70h	32	CORE1_CURMISR_13	5350 0070h	5351 0070h
74h	32	CORE1_CURMISR_14	5350 0074h	5351 0074h
78h	32	CORE1_CURMISR_15	5350 0078h	5351 0078h
7Ch	32	CORE1_CURMISR_16	5350 007Ch	5351 007Ch
80h	32	CORE1_CURMISR_17	5350 0080h	5351 0080h
84h	32	CORE1_CURMISR_18	5350 0084h	5351 0084h
88h	32	CORE1_CURMISR_19	5350 0088h	5351 0088h
8Ch	32	CORE1_CURMISR_20	5350 008Ch	5351 008Ch
90h	32	CORE1_CURMISR_21	5350 0090h	5351 0090h
94h	32	CORE1_CURMISR_22	5350 0094h	5351 0094h

Table 4-665. STC, STC Registers, Base Address=0X0000000053500000, Length=512 (continued)

Offset	Length	Register Name	r5ss_core0 Physical Address	r5ss_core1 Physical Address
98h	32	CORE1_CURMISR_23	5350 0098h	5351 0098h
9Ch	32	CORE1_CURMISR_24	5350 009Ch	5351 009Ch
A0h	32	CORE1_CURMISR_25	5350 00A0h	5351 00A0h
A4h	32	CORE1_CURMISR_26	5350 00A4h	5351 00A4h
A8h	32	CORE1_CURMISR_27	5350 00A8h	5351 00A8h
ACh	32	CORE2_CURMISR_0	5350 00ACh	5351 00ACh
B0h	32	CORE2_CURMISR_1	5350 00B0h	5351 00B0h
B4h	32	CORE2_CURMISR_2	5350 00B4h	5351 00B4h
B8h	32	CORE2_CURMISR_3	5350 00B8h	5351 00B8h
BCh	32	CORE2_CURMISR_4	5350 00BCh	5351 00BCh
C0h	32	CORE2_CURMISR_5	5350 00C0h	5351 00C0h
C4h	32	CORE2_CURMISR_6	5350 00C4h	5351 00C4h
C8h	32	CORE2_CURMISR_7	5350 00C8h	5351 00C8h
CCh	32	CORE2_CURMISR_8	5350 00CCh	5351 00CCh
D0h	32	CORE2_CURMISR_9	5350 00D0h	5351 00D0h
D4h	32	CORE2_CURMISR_10	5350 00D4h	5351 00D4h
D8h	32	CORE2_CURMISR_11	5350 00D8h	5351 00D8h
DCh	32	CORE2_CURMISR_12	5350 00DCh	5351 00DCh
E0h	32	CORE2_CURMISR_13	5350 00E0h	5351 00E0h
E4h	32	CORE2_CURMISR_14	5350 00E4h	5351 00E4h
E8h	32	CORE2_CURMISR_15	5350 00E8h	5351 00E8h
ECh	32	CORE2_CURMISR_16	5350 00ECh	5351 00ECh
F0h	32	CORE2_CURMISR_17	5350 00F0h	5351 00F0h
F4h	32	CORE2_CURMISR_18	5350 00F4h	5351 00F4h
F8h	32	CORE2_CURMISR_19	5350 00F8h	5351 00F8h
FCh	32	CORE2_CURMISR_20	5350 00FCh	5351 00FCh
100h	32	CORE2_CURMISR_21	5350 0100h	5351 0100h
104h	32	CORE2_CURMISR_22	5350 0104h	5351 0104h
108h	32	CORE2_CURMISR_23	5350 0108h	5351 0108h
10Ch	32	CORE2_CURMISR_24	5350 010Ch	5351 010Ch
110h	32	CORE2_CURMISR_25	5350 0110h	5351 0110h
114h	32	CORE2_CURMISR_26	5350 0114h	5351 0114h
118h	32	CORE2_CURMISR_27	5350 0118h	5351 0118h

Table 4-666. ICACHE_CORE0, ICACHE_CORE0 Registers, Base Address=0X0000000074000000, Length=8388608

Offset	Length	Register Name	r5ss_core0 Physical Address	r5ss_core1 Physical Address
0h	32	START	7400 0000h	7600 0000h
7FFFFCh	32	END	747F FFFCh	767F FFFCh

Table 4-667. DCACHE_CORE0, DCACHE_CORE0 Registers, Base Address=0X0000000074800000, Length=8388608

Offset	Length	Register Name	r5ss_core0 Physical Address	r5ss_core1 Physical Address
0h	32	START	7480 0000h	7680 0000h
7FFFFCh	32	END	74FF FFFCh	76FF FFFCh

Table 4-668. ICACHE_CORE1, ICACHE_CORE1 Registers, Base Address=0X0000000075000000, Length=8388608

Offset	Length	Register Name	r5ss_core0 Physical Address	r5ss_core1 Physical Address
0h	32	START	7500 0000h	7700 0000h
7FFFFCh	32	END	757F FFFCh	777F FFFCh

Table 4-669. DCACHE_CORE1, DCACHE_CORE1 Registers, Base Address=0X0000000075800000, Length=8388608

Offset	Length	Register Name	r5ss_core0 Physical Address	r5ss_core1 Physical Address
0h	32	START	7580 0000h	7780 0000h
7FFFFCh	32	END	75FF FFFCh	77FF FFFCh

Table 4-670. TCMA_CR5A, TCMA_CR5A Registers, Base Address=0X0000000078000000, Length=65536

Offset	Length	Register Name	r5ss_core0 Physical Address	r5ss_core1 Physical Address
0h	32	START	7800 0000h	7840 0000h
27FFCh	32	END	7802 7FFCh	7842 7FFCh

Table 4-671. TCMB_CR5A, TCMB_CR5A Registers, Base Address=0X0000000078100000, Length=65536

Offset	Length	Register Name	r5ss_core0 Physical Address	r5ss_core1 Physical Address
0h	32	START	7810 0000h	7850 0000h
2FFFCh	32	END	7812 FFFCh	7852 FFFCh

Table 4-672. TCMA_CR5B, TCMA_CR5B Registers, Base Address=0X0000000078200000, Length=32768

Offset	Length	Register Name	r5ss_core0 Physical Address	r5ss_core1 Physical Address
0h	32	START	7820 0000h	7860 0000h
7FFCh	32	END	7820 7FFCh	7860 7FFCh

Table 4-673. TCMB_CR5B, TCMB_CR5B Registers, Base Address=0X0000000078300000, Length=32768

Offset	Length	Register Name	r5ss_core0 Physical Address	r5ss_core1 Physical Address
0h	32	START	7830 0000h	7870 0000h
17FFCh	32	END	7831 7FFCh	7871 7FFCh

4.6.1 TCMA_CORE0_ROM_ROM_START_TCMA Registers

4.6.1.1 TCMA_ROM_ROM_START_TCMA Register (Offset = 0h) [reset = 0h]

Short Description:

Long Description:

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Table 4-674. Instance Table

Instance Name	Physical Address
R5SS_CORE0	0000 0000h

Figure 4-311. ROM_START_TCMA Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ROM_START															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROM_START															
R															
0h															

Access Types Legend

Table 4-675. ROM_START_TCMA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_START	R	0h	ROM start address of master sub system tcma Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.2 TCMA_CORE0_ROM_ROM_END_TCMA Registers

4.6.2.1 TCMA_ROM_ROM_END_TCMA Register (Offset = 1FFFCh) [reset = 0h]

Short Description:

Long Description:

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Table 4-676. Instance Table

Instance Name	Physical Address
R5SS_CORE0	0001 FFFCh

Figure 4-312. ROM_END_TCMA Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ROM_END															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROM_END															
R															
0h															

Access Types Legend

Table 4-677. ROM_END_TCMA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_END	R	0h	ROM end address of master sub system tcma Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.3 TCMA_CORE0_RAM_RAM_START_TCMA Registers

4.6.3.1 TCMA_RAM_RAM_START_TCMA Register (Offset = 0h) [reset = 0h]

Short Description:

Long Description:

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Table 4-678. Instance Table

Instance Name	Physical Address
R5SS_CORE0	0002 0000h
R5SS_CORE1	0002 0000h

Figure 4-313. RAM_START_TCMA Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RAM_START															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAM_START															
R/W															
0h															

Access Types Legend

Table 4-679. RAM_START_TCMA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAM_START	R/W	0h	RAM start address of master sub system tcma Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.4 TCMA_CORE0_RAM_RAM_END_TCMA Registers

4.6.4.1 TCMA_RAM_RAM_END_TCMA Register (Offset = 7FFCh) [reset = 0h]

Short Description:

Long Description:

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Table 4-680. Instance Table

Instance Name	Physical Address
R5SS_CORE0	0002 7FFCh
R5SS_CORE1	0002 7FFCh

Figure 4-314. RAM_END_TCMA Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RAM_END															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAM_END															
R/W															
0h															

Access Types Legend

Table 4-681. RAM_END_TCMA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAM_END	R/W	0h	RAM end address of master sub system tcma Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.5 TCMA_CORE1_RAM_RAM_START_TCMA Registers

4.6.5.1 TCMA_RAM_RAM_START_TCMA Register (Offset = 0h) [reset = 0h]

Short Description:

Long Description:

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Table 4-682. Instance Table

Instance Name	Physical Address
R5SS_CORE0	0002 0000h
R5SS_CORE1	0002 0000h

Figure 4-315. RAM_START_TCMA Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RAM_START															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAM_START															
R/W															
0h															

Access Types Legend

Table 4-683. RAM_START_TCMA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAM_START	R/W	0h	RAM start address of master sub system tcma Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.6 TCMA_CORE1_RAM_RAM_END_TCMA Registers

4.6.6.1 TCMA_RAM_RAM_END_TCMA Register (Offset = 7FFCh) [reset = 0h]

Short Description:

Long Description:

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Table 4-684. Instance Table

Instance Name	Physical Address
R5SS_CORE0	0002 7FFCh
R5SS_CORE1	0002 7FFCh

Figure 4-316. RAM_END_TCMA Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RAM_END															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAM_END															
R/W															
0h															

Access Types Legend

Table 4-685. RAM_END_TCMA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAM_END	R/W	0h	RAM end address of master sub system tcma Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.7 TCMB_CORE0_RAM_START Registers

4.6.7.1 TCMB_RAM_START Register (Offset = 0h) [reset = 0h]

Short Description:

Long Description:

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Table 4-686. Instance Table

Instance Name	Physical Address
R5SS_CORE0	0008 0000h
R5SS_CORE1	0008 0000h

Figure 4-317. START Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START															
R/W															
0h															

Access Types Legend

Table 4-687. START Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START	R/W	0h	TCMB start address Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.8 TCMB_CORE0_RAM_END Registers

4.6.8.1 TCMB_RAM_END Register (Offset = 17FFCh) [reset = 0h]

Short Description:

Long Description:

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Table 4-688. Instance Table

Instance Name	Physical Address
R5SS_CORE0	0009 7FFCh
R5SS_CORE1	0009 7FFCh

Figure 4-318. END Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END															
R/W															
0h															

Access Types Legend

Table 4-689. END Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END	R/W	0h	TCMB end address Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.9 TCMB_CORE1_RAM_START Registers

4.6.9.1 TCMB_RAM_START Register (Offset = 0h) [reset = 0h]

Short Description:

Long Description:

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Table 4-690. Instance Table

Instance Name	Physical Address
R5SS_CORE0	0008 0000h
R5SS_CORE1	0008 0000h

Figure 4-319. START Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START															
R/W															
0h															

Access Types Legend

Table 4-691. START Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START	R/W	0h	TCMB start address Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.10 TCMB_CORE1_RAM_END Registers

4.6.10.1 TCMB_RAM_END Register (Offset = 17FFCh) [reset = 0h]

Short Description:

Long Description:

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Table 4-692. Instance Table

Instance Name	Physical Address
R5SS_CORE0	0009 7FFCh
R5SS_CORE1	0009 7FFCh

Figure 4-320. END Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END															
R/W															
0h															

Access Types Legend

Table 4-693. END Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END	R/W	0h	TCMB end address Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.11 ECC_AGG_CORE0_AGGR_REVISION Registers

4.6.11.1 ECC_CORE0_AGGR_REVISION Register (Offset = 0h) [reset = 66a0c200h]

Short Description: Revision parameters

Long Description: Revision parameters

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Table 4-694. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 0000h
R5SS_CORE1	5300 4000h

Figure 4-321. AGGR_REVISION Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R		R		R											
1h		2h		6a0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
R					R			R		R					
18h					2h			0h		0h					

Access Types Legend

Table 4-695. AGGR_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme Reset Source: r5ss_core_rst_mod_g_rst_n
29:28	BU	R	2h	bu Reset Source: r5ss_core_rst_mod_g_rst_n
27:16	MODULE_ID	R	6A0h	Module ID Reset Source: r5ss_core_rst_mod_g_rst_n
15:11	REVRTL	R	18h	RTL version Reset Source: r5ss_core_rst_mod_g_rst_n
10:8	REVMAJ	R	2h	Major version Reset Source: r5ss_core_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom version Reset Source: r5ss_core_rst_mod_g_rst_n
5:0	REVMIN	R	0h	Minor version Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.12 ECC_AGG_CORE0_ECC_VECTOR Registers

4.6.12.1 ECC_CORE0_ECC_VECTOR Register (Offset = 8h) [reset = 0h]

Short Description: ECC Vector Register

Long Description: ECC Vector Register

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Table 4-696. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 0008h
R5SS_CORE1	5300 4008h

Figure 4-322. ECC_VECTOR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							RD_SVBUS_DONE	RD_SVBUS_ADDRESS							
NONE							R	R/W							
0							0h	0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RD_SVBUS	RESERVED				ECC_VECTOR										
R/W1TS	NONE				R/W										
0h	0				0h										

Access Types Legend

Table 4-697. ECC_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24	RD_SVBUS_DONE	R	0h	Status to indicate if read on serial VBUS is complete Reset Source: r5ss_core_rst_mod_g_rst_n
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address Reset Source: r5ss_core_rst_mod_g_rst_n
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS Reset Source: r5ss_core_rst_mod_g_rst_n
14:11	RESERVED	NONE		Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.13 ECC_AGG_CORE0_MISC_STATUS Registers

4.6.13.1 ECC_CORE0_MISC_STATUS Register (Offset = Ch) [reset = 1ch]

Short Description: Misc Status

Long Description: Misc Status

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Table 4-698. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 000Ch
R5SS_CORE1	5300 400Ch

Figure 4-323. MISC_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
456															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					NUM_RAMS										
NONE					R										
456					1ch										

Access Types Legend

Table 4-699. MISC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE		Reserved
10:0	NUM_RAMS	R	1Ch	Indicates the number of RAMS serviced by the ECC aggregator Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.14 ECC_AGG_CORE0_ECC_WRAP_REVISION Registers

4.6.14.1 ECC_CORE0_ECC_WRAP_REVISION Register (Offset = 10h) [reset = 66a40202h]

Short Description: Revision parameters

Long Description: Revision parameters

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Table 4-700. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 0010h
R5SS_CORE1	5300 4010h

Figure 4-324. ECC_WRAP_REVISION Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R		R		R											
1h		2h		6a4h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
R					R			R		R					
0h					2h			0h		2h					

Access Types Legend

Table 4-701. ECC_WRAP_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme Reset Source: r5ss_core_rst_mod_g_rst_n
29:28	BU	R	2h	bu Reset Source: r5ss_core_rst_mod_g_rst_n
27:16	MODULE_ID	R	6A4h	Module ID Reset Source: r5ss_core_rst_mod_g_rst_n
15:11	REVRTL	R	0h	RTL version Reset Source: r5ss_core_rst_mod_g_rst_n
10:8	REVMAJ	R	2h	Major version Reset Source: r5ss_core_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom version Reset Source: r5ss_core_rst_mod_g_rst_n
5:0	REVMIN	R	2h	Minor version Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.15 ECC_AGG_CORE0_CONTROL Registers

4.6.15.1 ECC_CORE0_CONTROL Register (Offset = 14h) [reset = 187h]

Short Description: ECC Control Register

Long Description: ECC Control Register

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Table 4-702. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 0014h
R5SS_CORE1	5300 4014h

Figure 4-325. CONTROL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
a7d8cb															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CHECK_SVBUS_TIMEOUT	CHECK_PARITY	ERROR_ONCE	FORCE_N_ROW	FORCE_DED	FORCE_SEC	ENABLE_RMW	ECC_CHECK	ECC_ENABLE
NONE							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
a7d8cb							1h	1h	0h	0h	0h	0h	1h	1h	1h

Access Types Legend

Table 4-703. CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE		Reserved
8	CHECK_SVBUS_TIMEOUT	R/W	1h	check for svbus timeout errors Reset Source: r5ss_core_rst_mod_g_rst_n
7	CHECK_PARITY	R/W	1h	check for parity errors Reset Source: r5ss_core_rst_mod_g_rst_n
6	ERROR_ONCE	R/W	0h	Force Error only once Reset Source: r5ss_core_rst_mod_g_rst_n
5	FORCE_N_ROW	R/W	0h	Force Error on any RAM read Reset Source: r5ss_core_rst_mod_g_rst_n
4	FORCE_DED	R/W	0h	Force Double Bit Error Reset Source: r5ss_core_rst_mod_g_rst_n
3	FORCE_SEC	R/W	0h	Force Single Bit Error Reset Source: r5ss_core_rst_mod_g_rst_n
2	ENABLE_RMW	R/W	1h	Enable rmw Reset Source: r5ss_core_rst_mod_g_rst_n
1	ECC_CHECK	R/W	1h	Enable ECC check Reset Source: r5ss_core_rst_mod_g_rst_n
0	ECC_ENABLE	R/W	1h	Enable ECC Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.16 ECC_AGG_CORE0_ERROR_CTRL1 Registers

4.6.16.1 ECC_CORE0_ERROR_CTRL1 Register (Offset = 18h) [reset = 0h]

Short Description: ECC Error Control1 Regis

Long Description: ECC Error Control1 Register

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Table 4-704. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 0018h
R5SS_CORE1	5300 4018h

Figure 4-326. ERROR_CTRL1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_ROW															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_ROW															
R/W															
0h															

Access Types Legend

Table 4-705. ERROR_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ECC_ROW	R/W	0h	Row address where single or double-bit error needs to be applied. This is ignored if force_n_row is set Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.17 ECC_AGG_CORE0_ERROR_CTRL2 Registers

4.6.17.1 ECC_CORE0_ERROR_CTRL2 Register (Offset = 1Ch) [reset = 0h]

Short Description: ECC Error Control2 Regis

Long Description: ECC Error Control2 Register

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Table 4-706. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 001Ch
R5SS_CORE1	5300 401Ch

Figure 4-327. ERROR_CTRL2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_BIT2															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_BIT1															
R/W															
0h															

Access Types Legend

Table 4-707. ERROR_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ECC_BIT2	R/W	0h	Data bit that needs to be flipped if double bit error needs to be forced Reset Source: r5ss_core_rst_mod_g_rst_n
15:0	ECC_BIT1	R/W	0h	Data bit that needs to be flipped when force_sec is set Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.18 ECC_AGG_CORE0_ERROR_STATUS1 Registers

4.6.18.1 ECC_CORE0_ERROR_STATUS1 Register (Offset = 20h) [reset = 0h]

Short Description: ECC Error Status1 Regist

Long Description: ECC Error Status1 Register

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Table 4-708. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 0020h
R5SS_CORE1	5300 4020h

Figure 4-328. ERROR_STATUS1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_BIT1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR_CTRL_REG_ERR	CLR_PARITY_ERR		CLR_ECC_OTHER	CLR_ECC_DED		CLR_ECC_SEC		CTR_REG_ERR	PARITY_ERR		ECC_OTHER	ECC_DED		ECC_SEC	
R/W1TC	R/WD		R/W1TC	R/WD		R/WD		R/W1TS	R/W1TS		R/W1TS	R/WI		R/WI	
0h	0h		0h	0h		0h		0h	0h		0h	0h		0h	

Access Types Legend

Table 4-709. ERROR_STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ECC_BIT1	R	0h	Data bit that corresponds to the single-bit error Reset Source: r5ss_core_rst_mod_g_rst_n
15	CLR_CTRL_REG_ERR	R/W1TC	0h	Clear control reg error Error Status, you must also re write the contorl ergister itself to clear this Reset Source: r5ss_core_rst_mod_g_rst_n
14:13	CLR_PARITY_ERR	R/WD	0h	Clear parity Error Status Reset Source: r5ss_core_rst_mod_g_rst_n
12	CLR_ECC_OTHER	R/W1TC	0h	Clear other Error Status Reset Source: r5ss_core_rst_mod_g_rst_n
11:10	CLR_ECC_DED	R/WD	0h	Clear Double Bit Error Status Reset Source: r5ss_core_rst_mod_g_rst_n
9:8	CLR_ECC_SEC	R/WD	0h	Clear Single Bit Error Status Reset Source: r5ss_core_rst_mod_g_rst_n
7	CTR_REG_ERR	R/W1TS	0h	control register error pending, Level interrupt Reset Source: r5ss_core_rst_mod_g_rst_n
6:5	PARITY_ERR	R/W1TS	0h	Level parity error Error Status Reset Source: r5ss_core_rst_mod_g_rst_n
4	ECC_OTHER	R/W1TS	0h	successive single-bit errors have occurred while a writeback is still pending, Level interrupt Reset Source: r5ss_core_rst_mod_g_rst_n
3:2	ECC_DED	R/WI	0h	Level Double Bit Error Status Reset Source: r5ss_core_rst_mod_g_rst_n
1:0	ECC_SEC	R/WI	0h	Level Single Bit Error Status Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.19 ECC_AGG_CORE0_ERROR_STATUS2 Registers

4.6.19.1 ECC_CORE0_ERROR_STATUS2 Register (Offset = 24h) [reset = 0h]

Short Description: ECC Error Status2 Regist

Long Description: ECC Error Status2 Register

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Table 4-710. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 0024h
R5SS_CORE1	5300 4024h

Figure 4-329. ERROR_STATUS2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_ROW															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_ROW															
R															
0h															

Access Types Legend

Table 4-711. ERROR_STATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ECC_ROW	R	0h	Row address where the single or double-bit error has occurred Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.20 ECC_AGG_CORE0_ERROR_STATUS3 Registers

4.6.20.1 ECC_CORE0_ERROR_STATUS3 Register (Offset = 28h) [reset = 0h]

Short Description: ECC Error Status3 Regist

Long Description: ECC Error Status3 Register

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Table 4-712. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 0028h
R5SS_CORE1	5300 4028h

Figure 4-330. ERROR_STATUS3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						CLR_SVBUS_TIMEOUT_ERR	RESERVED							SVBUS_TIMEOUT_ERR	WB_PEND
NONE						R/W1TC	NONE							R/W1TS	R
0						0h	0							0h	0h

Access Types Legend

Table 4-713. ERROR_STATUS3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9	CLR_SVBUS_TIMEOUT_ERR	R/W1TC	0h	Clear svbus timeout Error Status Reset Source: r5ss_core_rst_mod_g_rst_n
8:2	RESERVED	NONE		Reserved
1	SVBUS_TIMEOUT_ERR	R/W1TS	0h	Level svbus timeout error Error Status Reset Source: r5ss_core_rst_mod_g_rst_n
0	WB_PEND	R	0h	delayed write back pending Status Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.21 ECC_AGG_CORE0_SEC_EOI_REG Registers

4.6.21.1 ECC_CORE0_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

Short Description: EOI Register

Long Description: EOI Register

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Table 4-714. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 003Ch
R5SS_CORE1	5300 403Ch

Figure 4-331. SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															EOI_WR
NONE															R/W1TS
0															0h

Access Types Legend

Table 4-715. SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	EOI_WR	R/W1TS	0h	EOI Register Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.22 ECC_AGG_CORE0_SEC_STATUS_REG0 Registers

4.6.22.1 ECC_CORE0_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Short Description: Interrupt Status Registe

Long Description: Interrupt Status Register 0

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Table 4-716. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 0040h
R5SS_CORE1	5300 4040h

Figure 4-332. SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU0_KS_VIM_RAMECC_PEND	B1TCM0_BANK1_PEND	B1TCM0_BANK0_PEND	B0TCM0_BANK1_PEND	B0TCM0_BANK0_PEND	ATCM0_BANK1_PEND	ATCM0_BANK0_PEND	CPU0_DDATA_RAM7_PEND	CPU0_DDATA_RAM6_PEND	CPU0_DDATA_RAM5_PEND	CPU0_DDATA_RAM4_PEND	CPU0_DDATA_RAM3_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0				0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU0_DDATA_RAM2_PEND	CPU0_DDATA_RAM1_PEND	CPU0_DDATA_RAM0_PEND	CPU0_DDIRTY_RAM_PEND	CPU0_DTAG_RAM3_PEND	CPU0_DTAG_RAM2_PEND	CPU0_DTAG_RAM1_PEND	CPU0_DTAG_RAM0_PEND	CPU0_IDATA_BANK3_PEND	CPU0_IDATA_BANK2_PEND	CPU0_IDATA_BANK1_PEND	CPU0_IDATA_BANK0_PEND	CPU0_ITAG_RAM3_PEND	CPU0_ITAG_RAM2_PEND	CPU0_ITAG_RAM1_PEND	CPU0_ITAG_RAM0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-717. SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE		Reserved
27	CPU0_KS_VIM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ks_vim_ramecc_pend Reset Source: r5ss_core_rst_mod_g_rst_n
26	B1TCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm0_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
25	B1TCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm0_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
24	B0TCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm0_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
23	B0TCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm0_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
22	ATCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for atcm0_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
21	ATCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for atcm0_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
20	CPU0_DDATA_RAM7_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram7_pend Reset Source: r5ss_core_rst_mod_g_rst_n
19	CPU0_DDATA_RAM6_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram6_pend Reset Source: r5ss_core_rst_mod_g_rst_n

Table 4-717. SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	CPU0_DDATA_RAM5_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram5_pend Reset Source: r5ss_core_rst_mod_g_rst_n
17	CPU0_DDATA_RAM4_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram4_pend Reset Source: r5ss_core_rst_mod_g_rst_n
16	CPU0_DDATA_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
15	CPU0_DDATA_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
14	CPU0_DDATA_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
13	CPU0_DDATA_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
12	CPU0_DDIRTY_RAM_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddirty_ram_pend Reset Source: r5ss_core_rst_mod_g_rst_n
11	CPU0_DTAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
10	CPU0_DTAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
9	CPU0_DTAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
8	CPU0_DTAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
7	CPU0_IDATA_BANK3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
6	CPU0_IDATA_BANK2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
5	CPU0_IDATA_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
4	CPU0_IDATA_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
3	CPU0_ITAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
2	CPU0_ITAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
1	CPU0_ITAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
0	CPU0_ITAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.23 ECC_AGG_CORE0_SEC_ENABLE_SET_REG0 Registers

4.6.23.1 ECC_CORE0_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Short Description: Interrupt Enable Set Reg

Long Description: Interrupt Enable Set Register 0

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Table 4-718. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 0080h
R5SS_CORE1	5300 4080h

Figure 4-333. SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU0_KS_VIM_RAMECC_ENABLE_SET	B1TCM0_BANK1_ENABLE_SET	B1TCM0_BANK0_ENABLE_SET	B0TCM0_BANK1_ENABLE_SET	B0TCM0_BANK0_ENABLE_SET	ATCM0_BANK1_ENABLE_SET	ATCM0_BANK0_ENABLE_SET	CPU0_DDATA_RAM7_ENABLE_SET	CPU0_DDATA_RAM6_ENABLE_SET	CPU0_DDATA_RAM5_ENABLE_SET	CPU0_DDATA_RAM4_ENABLE_SET	CPU0_DDATA_RAM3_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0				0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU0_DDATA_RAM2_ENABLE_SET	CPU0_DDATA_RAM1_ENABLE_SET	CPU0_DDATA_RAM0_ENABLE_SET	CPU0_DDIRTY_RAM_ENABLE_SET	CPU0_DTAG_RAM3_ENABLE_SET	CPU0_DTAG_RAM2_ENABLE_SET	CPU0_DTAG_RAM1_ENABLE_SET	CPU0_DTAG_RAM0_ENABLE_SET	CPU0_IDATA_BANK3_ENABLE_SET	CPU0_IDATA_BANK2_ENABLE_SET	CPU0_IDATA_BANK1_ENABLE_SET	CPU0_IDATA_BANK0_ENABLE_SET	CPU0_ITAG_RAM3_ENABLE_SET	CPU0_ITAG_RAM2_ENABLE_SET	CPU0_ITAG_RAM1_ENABLE_SET	CPU0_ITAG_RAM0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-719. SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE		Reserved
27	CPU0_KS_VIM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ks_vim_ramecc_pend Reset Source: r5ss_core_rst_mod_g_rst_n
26	B1TCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm0_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
25	B1TCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm0_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
24	B0TCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm0_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
23	B0TCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm0_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
22	ATCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm0_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
21	ATCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm0_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
20	CPU0_DDATA_RAM7_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram7_pend Reset Source: r5ss_core_rst_mod_g_rst_n

Table 4-719. SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	CPU0_DDATA_RAM6_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram6_pend Reset Source: r5ss_core_rst_mod_g_rst_n
18	CPU0_DDATA_RAM5_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram5_pend Reset Source: r5ss_core_rst_mod_g_rst_n
17	CPU0_DDATA_RAM4_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram4_pend Reset Source: r5ss_core_rst_mod_g_rst_n
16	CPU0_DDATA_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
15	CPU0_DDATA_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
14	CPU0_DDATA_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
13	CPU0_DDATA_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
12	CPU0_DDIRTY_RAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddirty_ram_pend Reset Source: r5ss_core_rst_mod_g_rst_n
11	CPU0_DTAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
10	CPU0_DTAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
9	CPU0_DTAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
8	CPU0_DTAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
7	CPU0_IDATA_BANK3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
6	CPU0_IDATA_BANK2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
5	CPU0_IDATA_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
4	CPU0_IDATA_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
3	CPU0_ITAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
2	CPU0_ITAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
1	CPU0_ITAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
0	CPU0_ITAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.24 ECC_AGG_CORE0_SEC_ENABLE_CLR_REG0 Registers

4.6.24.1 ECC_CORE0_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Short Description: Interrupt Enable Clear R

Long Description: Interrupt Enable Clear Register 0

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Table 4-720. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 00C0h
R5SS_CORE1	5300 40C0h

Figure 4-334. SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU0_KS_VIM_RAMECC_ENABLE_CLR	B1TCM0_BANK1_ENABLE_CLR	B1TCM0_BANK0_ENABLE_CLR	B0TCM0_BANK1_ENABLE_CLR	B0TCM0_BANK0_ENABLE_CLR	ATCM0_BANK1_ENABLE_CLR	ATCM0_BANK0_ENABLE_CLR	CPU0_DDATA_RAM7_ENABLE_CLR	CPU0_DDATA_RAM6_ENABLE_CLR	CPU0_DDATA_RAM5_ENABLE_CLR	CPU0_DDATA_RAM4_ENABLE_CLR	CPU0_DDATA_RAM3_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0				0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU0_DDATA_RAM2_ENABLE_CLR	CPU0_DDATA_RAM1_ENABLE_CLR	CPU0_DDATA_RAM0_ENABLE_CLR	CPU0_DDIRTY_RAM_ENABLE_CLR	CPU0_DTAG_RAM3_ENABLE_CLR	CPU0_DTAG_RAM2_ENABLE_CLR	CPU0_DTAG_RAM1_ENABLE_CLR	CPU0_DTAG_RAM0_ENABLE_CLR	CPU0_IDATA_BANK3_ENABLE_CLR	CPU0_IDATA_BANK2_ENABLE_CLR	CPU0_IDATA_BANK1_ENABLE_CLR	CPU0_IDATA_BANK0_ENABLE_CLR	CPU0_ITAG_RAM3_ENABLE_CLR	CPU0_ITAG_RAM2_ENABLE_CLR	CPU0_ITAG_RAM1_ENABLE_CLR	CPU0_ITAG_RAM0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-721. SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE		Reserved
27	CPU0_KS_VIM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ks_vim_ramecc_pend Reset Source: r5ss_core_rst_mod_g_rst_n
26	B1TCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm0_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
25	B1TCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm0_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
24	B0TCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm0_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
23	B0TCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm0_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
22	ATCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm0_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
21	ATCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm0_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
20	CPU0_DDATA_RAM7_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram7_pend Reset Source: r5ss_core_rst_mod_g_rst_n

Table 4-721. SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	CPU0_DDATA_RAM6_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram6_pend Reset Source: r5ss_core_rst_mod_g_rst_n
18	CPU0_DDATA_RAM5_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram5_pend Reset Source: r5ss_core_rst_mod_g_rst_n
17	CPU0_DDATA_RAM4_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram4_pend Reset Source: r5ss_core_rst_mod_g_rst_n
16	CPU0_DDATA_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
15	CPU0_DDATA_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
14	CPU0_DDATA_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
13	CPU0_DDATA_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
12	CPU0_DDIRTY_RAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddirty_ram_pend Reset Source: r5ss_core_rst_mod_g_rst_n
11	CPU0_DTAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
10	CPU0_DTAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
9	CPU0_DTAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
8	CPU0_DTAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
7	CPU0_IDATA_BANK3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
6	CPU0_IDATA_BANK2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
5	CPU0_IDATA_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
4	CPU0_IDATA_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
3	CPU0_ITAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
2	CPU0_ITAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
1	CPU0_ITAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
0	CPU0_ITAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.25 ECC_AGG_CORE0_DED_EOI_REG Registers

4.6.25.1 ECC_CORE0_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

Short Description: EOI Register

Long Description: EOI Register

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Table 4-722. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 013Ch
R5SS_CORE1	5300 413Ch

Figure 4-335. DED_EOI_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															EOI_WR
NONE															R/W1TS
0															0h

Access Types Legend

Table 4-723. DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	EOI_WR	R/W1TS	0h	EOI Register Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.26 ECC_AGG_CORE0_DED_STATUS_REG0 Registers

4.6.26.1 ECC_CORE0_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Short Description: Interrupt Status Registe

Long Description: Interrupt Status Register 0

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Table 4-724. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 0140h
R5SS_CORE1	5300 4140h

Figure 4-336. DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU0_KS_VIM_RAMECC_PEND	B1TCM0_BANK1_PEND	B1TCM0_BANK0_PEND	B0TCM0_BANK1_PEND	B0TCM0_BANK0_PEND	ATCM0_BANK1_PEND	ATCM0_BANK0_PEND	CPU0_DDATA_RAM7_PEND	CPU0_DDATA_RAM6_PEND	CPU0_DDATA_RAM5_PEND	CPU0_DDATA_RAM4_PEND	CPU0_DDATA_RAM3_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0				0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU0_DDATA_RAM2_PEND	CPU0_DDATA_RAM1_PEND	CPU0_DDATA_RAM0_PEND	CPU0_DDIRTY_RAM_PEND	CPU0_DTAG_RAM3_PEND	CPU0_DTAG_RAM2_PEND	CPU0_DTAG_RAM1_PEND	CPU0_DTAG_RAM0_PEND	CPU0_IDATA_BANK3_PEND	CPU0_IDATA_BANK2_PEND	CPU0_IDATA_BANK1_PEND	CPU0_IDATA_BANK0_PEND	CPU0_ITAG_RAM3_PEND	CPU0_ITAG_RAM2_PEND	CPU0_ITAG_RAM1_PEND	CPU0_ITAG_RAM0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-725. DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE		Reserved
27	CPU0_KS_VIM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ks_vim_ramecc_pend Reset Source: r5ss_core_rst_mod_g_rst_n
26	B1TCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm0_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
25	B1TCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm0_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
24	B0TCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm0_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
23	B0TCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm0_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
22	ATCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for atcm0_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
21	ATCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for atcm0_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
20	CPU0_DDATA_RAM7_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram7_pend Reset Source: r5ss_core_rst_mod_g_rst_n
19	CPU0_DDATA_RAM6_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram6_pend Reset Source: r5ss_core_rst_mod_g_rst_n

Table 4-725. DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	CPU0_DDATA_RAM5_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram5_pend Reset Source: r5ss_core_rst_mod_g_rst_n
17	CPU0_DDATA_RAM4_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram4_pend Reset Source: r5ss_core_rst_mod_g_rst_n
16	CPU0_DDATA_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
15	CPU0_DDATA_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
14	CPU0_DDATA_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
13	CPU0_DDATA_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
12	CPU0_DDIRTY_RAM_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddirty_ram_pend Reset Source: r5ss_core_rst_mod_g_rst_n
11	CPU0_DTAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
10	CPU0_DTAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
9	CPU0_DTAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
8	CPU0_DTAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
7	CPU0_IDATA_BANK3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
6	CPU0_IDATA_BANK2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
5	CPU0_IDATA_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
4	CPU0_IDATA_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
3	CPU0_ITAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
2	CPU0_ITAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
1	CPU0_ITAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
0	CPU0_ITAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.27 ECC_AGG_CORE0_DED_ENABLE_SET_REG0 Registers

4.6.27.1 ECC_CORE0_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Short Description: Interrupt Enable Set Reg

Long Description: Interrupt Enable Set Register 0

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Table 4-726. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 0180h
R5SS_CORE1	5300 4180h

Figure 4-337. DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU0_KS_VIM_RAMECC_ENABLE_SET	B1TCM0_BANK1_ENABLE_SET	B1TCM0_BANK0_ENABLE_SET	B0TCM0_BANK1_ENABLE_SET	B0TCM0_BANK0_ENABLE_SET	ATCM0_BANK1_ENABLE_SET	ATCM0_BANK0_ENABLE_SET	CPU0_DDATA_RAM7_ENABLE_SET	CPU0_DDATA_RAM6_ENABLE_SET	CPU0_DDATA_RAM5_ENABLE_SET	CPU0_DDATA_RAM4_ENABLE_SET	CPU0_DDATA_RAM3_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0				0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU0_DDATA_RAM2_ENABLE_SET	CPU0_DDATA_RAM1_ENABLE_SET	CPU0_DDATA_RAM0_ENABLE_SET	CPU0_DDIRTY_RAM_ENABLE_SET	CPU0_DTAG_RAM3_ENABLE_SET	CPU0_DTAG_RAM2_ENABLE_SET	CPU0_DTAG_RAM1_ENABLE_SET	CPU0_DTAG_RAM0_ENABLE_SET	CPU0_IDATA_BANK3_ENABLE_SET	CPU0_IDATA_BANK2_ENABLE_SET	CPU0_IDATA_BANK1_ENABLE_SET	CPU0_IDATA_BANK0_ENABLE_SET	CPU0_ITAG_RAM3_ENABLE_SET	CPU0_ITAG_RAM2_ENABLE_SET	CPU0_ITAG_RAM1_ENABLE_SET	CPU0_ITAG_RAM0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-727. DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE		Reserved
27	CPU0_KS_VIM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ks_vim_ramecc_pend Reset Source: r5ss_core_rst_mod_g_rst_n
26	B1TCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm0_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
25	B1TCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm0_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
24	B0TCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm0_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
23	B0TCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm0_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
22	ATCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm0_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
21	ATCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm0_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
20	CPU0_DDATA_RAM7_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram7_pend Reset Source: r5ss_core_rst_mod_g_rst_n

Table 4-727. DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	CPU0_DDATA_RAM6_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram6_pend Reset Source: r5ss_core_rst_mod_g_rst_n
18	CPU0_DDATA_RAM5_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram5_pend Reset Source: r5ss_core_rst_mod_g_rst_n
17	CPU0_DDATA_RAM4_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram4_pend Reset Source: r5ss_core_rst_mod_g_rst_n
16	CPU0_DDATA_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
15	CPU0_DDATA_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
14	CPU0_DDATA_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
13	CPU0_DDATA_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
12	CPU0_DDIRTY_RAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddirty_ram_pend Reset Source: r5ss_core_rst_mod_g_rst_n
11	CPU0_DTAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
10	CPU0_DTAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
9	CPU0_DTAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
8	CPU0_DTAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
7	CPU0_IDATA_BANK3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
6	CPU0_IDATA_BANK2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
5	CPU0_IDATA_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
4	CPU0_IDATA_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
3	CPU0_ITAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
2	CPU0_ITAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
1	CPU0_ITAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
0	CPU0_ITAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.28 ECC_AGG_CORE0_DED_ENABLE_CLR_REG0 Registers

4.6.28.1 ECC_CORE0_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Short Description: Interrupt Enable Clear R

Long Description: Interrupt Enable Clear Register 0

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Table 4-728. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 01C0h
R5SS_CORE1	5300 41C0h

Figure 4-338. DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU0_KS_VIM_RAMECC_ENABLE_CLR	B1TCM0_BANK1_ENABLE_CLR	B1TCM0_BANK0_ENABLE_CLR	B0TCM0_BANK1_ENABLE_CLR	B0TCM0_BANK0_ENABLE_CLR	ATCM0_BANK1_ENABLE_CLR	ATCM0_BANK0_ENABLE_CLR	CPU0_DDATA_RAM7_ENABLE_CLR	CPU0_DDATA_RAM6_ENABLE_CLR	CPU0_DDATA_RAM5_ENABLE_CLR	CPU0_DDATA_RAM4_ENABLE_CLR	CPU0_DDATA_RAM3_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0				0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU0_DDATA_RAM2_ENABLE_CLR	CPU0_DDATA_RAM1_ENABLE_CLR	CPU0_DDATA_RAM0_ENABLE_CLR	CPU0_DDIRTY_RAM_ENABLE_CLR	CPU0_DTAG_RAM3_ENABLE_CLR	CPU0_DTAG_RAM2_ENABLE_CLR	CPU0_DTAG_RAM1_ENABLE_CLR	CPU0_DTAG_RAM0_ENABLE_CLR	CPU0_IDATA_BANK3_ENABLE_CLR	CPU0_IDATA_BANK2_ENABLE_CLR	CPU0_IDATA_BANK1_ENABLE_CLR	CPU0_IDATA_BANK0_ENABLE_CLR	CPU0_ITAG_RAM3_ENABLE_CLR	CPU0_ITAG_RAM2_ENABLE_CLR	CPU0_ITAG_RAM1_ENABLE_CLR	CPU0_ITAG_RAM0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-729. DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE		Reserved
27	CPU0_KS_VIM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ks_vim_ramecc_pend Reset Source: r5ss_core_rst_mod_g_rst_n
26	B1TCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm0_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
25	B1TCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm0_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
24	B0TCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm0_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
23	B0TCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm0_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
22	ATCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm0_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
21	ATCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm0_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
20	CPU0_DDATA_RAM7_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram7_pend Reset Source: r5ss_core_rst_mod_g_rst_n

Table 4-729. DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	CPU0_DDATA_RAM6_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram6_pend Reset Source: r5ss_core_rst_mod_g_rst_n
18	CPU0_DDATA_RAM5_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram5_pend Reset Source: r5ss_core_rst_mod_g_rst_n
17	CPU0_DDATA_RAM4_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram4_pend Reset Source: r5ss_core_rst_mod_g_rst_n
16	CPU0_DDATA_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
15	CPU0_DDATA_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
14	CPU0_DDATA_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
13	CPU0_DDATA_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
12	CPU0_DDIRTY_RAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddirty_ram_pend Reset Source: r5ss_core_rst_mod_g_rst_n
11	CPU0_DTAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
10	CPU0_DTAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
9	CPU0_DTAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
8	CPU0_DTAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
7	CPU0_IDATA_BANK3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
6	CPU0_IDATA_BANK2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
5	CPU0_IDATA_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
4	CPU0_IDATA_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
3	CPU0_ITAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
2	CPU0_ITAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
1	CPU0_ITAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
0	CPU0_ITAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.29 ECC_AGG_CORE0_AGGR_ENABLE_SET Registers

4.6.29.1 ECC_CORE0_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

Short Description: AGGR interrupt enable se

Long Description: AGGR interrupt enable set Register

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Table 4-730. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 0200h
R5SS_CORE1	5300 4200h

Figure 4-339. AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														TIMEOUT	PARITY
NONE														R/W1TS	R/W1TS
0														0h	0h

Access Types Legend

Table 4-731. AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors Reset Source: r5ss_core_rst_mod_g_rst_n
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.30 ECC_AGG_CORE0_AGGR_ENABLE_CLR Registers

4.6.30.1 ECC_CORE0_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

Short Description: AGGR interrupt enable cl

Long Description: AGGR interrupt enable clear Register

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Table 4-732. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 0204h
R5SS_CORE1	5300 4204h

Figure 4-340. AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														TIMEOUT	PARITY
NONE														R/W1TC	R/W1TC
0														0h	0h

Access Types Legend

Table 4-733. AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors Reset Source: r5ss_core_rst_mod_g_rst_n
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.31 ECC_AGG_CORE0_AGGR_STATUS_SET Registers

4.6.31.1 ECC_CORE0_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

Short Description: AGGR interrupt status se

Long Description: AGGR interrupt status set Register

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Table 4-734. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 0208h
R5SS_CORE1	5300 4208h

Figure 4-341. AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												TIMEOUT		PARITY	
NONE												R/WI		R/WI	
0												0h		0h	

Access Types Legend

Table 4-735. AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors Reset Source: r5ss_core_rst_mod_g_rst_n
1:0	PARITY	R/WI	0h	interrupt status set for parity errors Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.32 ECC_AGG_CORE0_AGGR_STATUS_CLR Registers

4.6.32.1 ECC_CORE0_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

Short Description: AGGR interrupt status cl

Long Description: AGGR interrupt status clear Register

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Table 4-736. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 020Ch
R5SS_CORE1	5300 420Ch

Figure 4-342. AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												TIMEOUT		PARITY	
NONE												R/WD		R/WD	
0												0h		0h	

Access Types Legend

Table 4-737. AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors Reset Source: r5ss_core_rst_mod_g_rst_n
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.33 ECC_AGG_CORE1_AGGR_REVISION Registers

4.6.33.1 ECC_CORE1_AGGR_REVISION Register (Offset = 0h) [reset = 66a0c200h]

Short Description: Revision parameters

Long Description: Revision parameters

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Table 4-738. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 3000h
R5SS_CORE1	5300 7000h

Figure 4-343. AGGR_REVISION Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R		R		R											
1h		2h		6a0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
R					R			R		R					
18h					2h			0h		0h					

Access Types Legend

Table 4-739. AGGR_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme Reset Source: r5ss_core_rst_mod_g_rst_n
29:28	BU	R	2h	bu Reset Source: r5ss_core_rst_mod_g_rst_n
27:16	MODULE_ID	R	6A0h	Module ID Reset Source: r5ss_core_rst_mod_g_rst_n
15:11	REVRTL	R	18h	RTL version Reset Source: r5ss_core_rst_mod_g_rst_n
10:8	REVMAJ	R	2h	Major version Reset Source: r5ss_core_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom version Reset Source: r5ss_core_rst_mod_g_rst_n
5:0	REVMIN	R	0h	Minor version Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.34 ECC_AGG_CORE1_ECC_VECTOR Registers

4.6.34.1 ECC_CORE1_ECC_VECTOR Register (Offset = 8h) [reset = 0h]

Short Description: ECC Vector Register

Long Description: ECC Vector Register

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Table 4-740. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 3008h
R5SS_CORE1	5300 7008h

Figure 4-344. ECC_VECTOR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							RD_SVBUS_DONE	RD_SVBUS_ADDRESS							
NONE							R	R/W							
0							0h	0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RD_SVBUS	RESERVED				ECC_VECTOR										
R/W1TS	NONE				R/W										
0h	0				0h										

Access Types Legend

Table 4-741. ECC_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24	RD_SVBUS_DONE	R	0h	Status to indicate if read on serial VBUS is complete Reset Source: r5ss_core_rst_mod_g_rst_n
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address Reset Source: r5ss_core_rst_mod_g_rst_n
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS Reset Source: r5ss_core_rst_mod_g_rst_n
14:11	RESERVED	NONE		Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.35 ECC_AGG_CORE1_MISC_STATUS Registers

4.6.35.1 ECC_CORE1_MISC_STATUS Register (Offset = Ch) [reset = 1ch]

Short Description: Misc Status

Long Description: Misc Status

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Table 4-742. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 300Ch
R5SS_CORE1	5300 700Ch

Figure 4-345. MISC_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
456															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					NUM_RAMS										
NONE					R										
456					1ch										

Access Types Legend

Table 4-743. MISC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE		Reserved
10:0	NUM_RAMS	R	1Ch	Indicates the number of RAMS serviced by the ECC aggregator Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.36 ECC_AGG_CORE1_ECC_WRAP_REVISION Registers

4.6.36.1 ECC_CORE1_ECC_WRAP_REVISION Register (Offset = 10h) [reset = 66a40202h]

Short Description: Revision parameters

Long Description: Revision parameters

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Table 4-744. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 3010h
R5SS_CORE1	5300 7010h

Figure 4-346. ECC_WRAP_REVISION Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R		R		R											
1h		2h		6a4h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
R					R			R		R					
0h					2h			0h		2h					

Access Types Legend

Table 4-745. ECC_WRAP_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme Reset Source: r5ss_core_rst_mod_g_rst_n
29:28	BU	R	2h	bu Reset Source: r5ss_core_rst_mod_g_rst_n
27:16	MODULE_ID	R	6A4h	Module ID Reset Source: r5ss_core_rst_mod_g_rst_n
15:11	REVRTL	R	0h	RTL version Reset Source: r5ss_core_rst_mod_g_rst_n
10:8	REVMAJ	R	2h	Major version Reset Source: r5ss_core_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom version Reset Source: r5ss_core_rst_mod_g_rst_n
5:0	REVMIN	R	2h	Minor version Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.37 ECC_AGG_CORE1_CONTROL Registers

4.6.37.1 ECC_CORE1_CONTROL Register (Offset = 14h) [reset = 187h]

Short Description: ECC Control Register

Long Description: ECC Control Register

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Table 4-746. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 3014h
R5SS_CORE1	5300 7014h

Figure 4-347. CONTROL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
a7d8cb															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CHECK_SVBUS_TIMEOUT	CHECK_PARITY	ERROR_ONCE	FORCE_N_ROW	FORCE_DED	FORCE_SEC	ENABLE_RMW	ECC_CHECK	ECC_ENABLE
NONE							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
a7d8cb							1h	1h	0h	0h	0h	0h	1h	1h	1h

Access Types Legend

Table 4-747. CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE		Reserved
8	CHECK_SVBUS_TIMEOUT	R/W	1h	check for svbus timeout errors Reset Source: r5ss_core_rst_mod_g_rst_n
7	CHECK_PARITY	R/W	1h	check for parity errors Reset Source: r5ss_core_rst_mod_g_rst_n
6	ERROR_ONCE	R/W	0h	Force Error only once Reset Source: r5ss_core_rst_mod_g_rst_n
5	FORCE_N_ROW	R/W	0h	Force Error on any RAM read Reset Source: r5ss_core_rst_mod_g_rst_n
4	FORCE_DED	R/W	0h	Force Double Bit Error Reset Source: r5ss_core_rst_mod_g_rst_n
3	FORCE_SEC	R/W	0h	Force Single Bit Error Reset Source: r5ss_core_rst_mod_g_rst_n
2	ENABLE_RMW	R/W	1h	Enable rmw Reset Source: r5ss_core_rst_mod_g_rst_n
1	ECC_CHECK	R/W	1h	Enable ECC check Reset Source: r5ss_core_rst_mod_g_rst_n
0	ECC_ENABLE	R/W	1h	Enable ECC Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.38 ECC_AGG_CORE1_ERROR_CTRL1 Registers

4.6.38.1 ECC_CORE1_ERROR_CTRL1 Register (Offset = 18h) [reset = 0h]

Short Description: ECC Error Control1 Regis

Long Description: ECC Error Control1 Register

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Table 4-748. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 3018h
R5SS_CORE1	5300 7018h

Figure 4-348. ERROR_CTRL1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_ROW															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_ROW															
R/W															
0h															

Access Types Legend

Table 4-749. ERROR_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ECC_ROW	R/W	0h	Row address where single or double-bit error needs to be applied. This is ignored if force_n_row is set Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.39 ECC_AGG_CORE1_ERROR_CTRL2 Registers

4.6.39.1 ECC_CORE1_ERROR_CTRL2 Register (Offset = 1Ch) [reset = 0h]

Short Description: ECC Error Control2 Regis

Long Description: ECC Error Control2 Register

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Table 4-750. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 301Ch
R5SS_CORE1	5300 701Ch

Figure 4-349. ERROR_CTRL2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_BIT2															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_BIT1															
R/W															
0h															

Access Types Legend

Table 4-751. ERROR_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ECC_BIT2	R/W	0h	Data bit that needs to be flipped if double bit error needs to be forced Reset Source: r5ss_core_rst_mod_g_rst_n
15:0	ECC_BIT1	R/W	0h	Data bit that needs to be flipped when force_sec is set Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.40 ECC_AGG_CORE1_ERROR_STATUS1 Registers

4.6.40.1 ECC_CORE1_ERROR_STATUS1 Register (Offset = 20h) [reset = 0h]

Short Description: ECC Error Status1 Regist

Long Description: ECC Error Status1 Register

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Table 4-752. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 3020h
R5SS_CORE1	5300 7020h

Figure 4-350. ERROR_STATUS1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_BIT1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR_CTRL_REG_ERR	CLR_PARITY_ERR		CLR_ECC_OTHER	CLR_ECC_DED		CLR_ECC_SEC		CTR_REG_ERR	PARITY_ERR		ECC_OTHER	ECC_DED		ECC_SEC	
R/W1TC	R/WD		R/W1TC	R/WD		R/WD		R/W1TS	R/W1TS		R/W1TS	R/WI		R/WI	
0h	0h		0h	0h		0h		0h	0h		0h	0h		0h	

Access Types Legend

Table 4-753. ERROR_STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ECC_BIT1	R	0h	Data bit that corresponds to the single-bit error Reset Source: r5ss_core_rst_mod_g_rst_n
15	CLR_CTRL_REG_ERR	R/W1TC	0h	Clear control reg error Error Status, you must also re write the contorl ergister itself to clear this Reset Source: r5ss_core_rst_mod_g_rst_n
14:13	CLR_PARITY_ERR	R/WD	0h	Clear parity Error Status Reset Source: r5ss_core_rst_mod_g_rst_n
12	CLR_ECC_OTHER	R/W1TC	0h	Clear other Error Status Reset Source: r5ss_core_rst_mod_g_rst_n
11:10	CLR_ECC_DED	R/WD	0h	Clear Double Bit Error Status Reset Source: r5ss_core_rst_mod_g_rst_n
9:8	CLR_ECC_SEC	R/WD	0h	Clear Single Bit Error Status Reset Source: r5ss_core_rst_mod_g_rst_n
7	CTR_REG_ERR	R/W1TS	0h	control register error pending, Level interrupt Reset Source: r5ss_core_rst_mod_g_rst_n
6:5	PARITY_ERR	R/W1TS	0h	Level parity error Error Status Reset Source: r5ss_core_rst_mod_g_rst_n
4	ECC_OTHER	R/W1TS	0h	successive single-bit errors have occurred while a writeback is still pending, Level interrupt Reset Source: r5ss_core_rst_mod_g_rst_n
3:2	ECC_DED	R/WI	0h	Level Double Bit Error Status Reset Source: r5ss_core_rst_mod_g_rst_n
1:0	ECC_SEC	R/WI	0h	Level Single Bit Error Status Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.41 ECC_AGG_CORE1_ERROR_STATUS2 Registers

4.6.41.1 ECC_CORE1_ERROR_STATUS2 Register (Offset = 24h) [reset = 0h]

Short Description: ECC Error Status2 Regist

Long Description: ECC Error Status2 Register

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Table 4-754. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 3024h
R5SS_CORE1	5300 7024h

Figure 4-351. ERROR_STATUS2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_ROW															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_ROW															
R															
0h															

Access Types Legend

Table 4-755. ERROR_STATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ECC_ROW	R	0h	Row address where the single or double-bit error has occurred Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.42 ECC_AGG_CORE1_ERROR_STATUS3 Registers

4.6.42.1 ECC_CORE1_ERROR_STATUS3 Register (Offset = 28h) [reset = 0h]

Short Description: ECC Error Status3 Regist

Long Description: ECC Error Status3 Register

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Table 4-756. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 3028h
R5SS_CORE1	5300 7028h

Figure 4-352. ERROR_STATUS3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						CLR_SVBUS_TIMEOUT_ERR	RESERVED							SVBUS_TIMEOUT_ERR	WB_PEND
NONE						R/W1TC	NONE							R/W1TS	R
0						0h	0							0h	0h

Access Types Legend

Table 4-757. ERROR_STATUS3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9	CLR_SVBUS_TIMEOUT_ERR	R/W1TC	0h	Clear svbus timeout Error Status Reset Source: r5ss_core_rst_mod_g_rst_n
8:2	RESERVED	NONE		Reserved
1	SVBUS_TIMEOUT_ERR	R/W1TS	0h	Level svbus timeout error Error Status Reset Source: r5ss_core_rst_mod_g_rst_n
0	WB_PEND	R	0h	delayed write back pending Status Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.43 ECC_AGG_CORE1_SEC_EOI_REG Registers

4.6.43.1 ECC_CORE1_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

Short Description: EOI Register

Long Description: EOI Register

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Table 4-758. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 303Ch
R5SS_CORE1	5300 703Ch

Figure 4-353. SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															EOI_WR
NONE															R/W1TS
0															0h

Access Types Legend

Table 4-759. SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	EOI_WR	R/W1TS	0h	EOI Register Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.44 ECC_AGG_CORE1_SEC_STATUS_REG0 Registers

4.6.44.1 ECC_CORE1_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Short Description: Interrupt Status Registe

Long Description: Interrupt Status Register 0

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Table 4-760. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 3040h
R5SS_CORE1	5300 7040h

Figure 4-354. SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU1_KS_VIM_RAMECC_PEND	B1TCM1_BANK1_PEND	B1TCM1_BANK0_PEND	B0TCM1_BANK1_PEND	B0TCM1_BANK0_PEND	ATCM1_BANK1_PEND	ATCM1_BANK0_PEND	CPU1_DDATA_RAM7_PEND	CPU1_DDATA_RAM6_PEND	CPU1_DDATA_RAM5_PEND	CPU1_DDATA_RAM4_PEND	CPU1_DDATA_RAM3_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0				0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU1_DDATA_RAM2_PEND	CPU1_DDATA_RAM1_PEND	CPU1_DDATA_RAM0_PEND	CPU1_DDIRTY_RAM_PEND	CPU1_DTAG_RAM3_PEND	CPU1_DTAG_RAM2_PEND	CPU1_DTAG_RAM1_PEND	CPU1_DTAG_RAM0_PEND	CPU1_IDATA_BANK3_PEND	CPU1_IDATA_BANK2_PEND	CPU1_IDATA_BANK1_PEND	CPU1_IDATA_BANK0_PEND	CPU1_ITAG_RAM3_PEND	CPU1_ITAG_RAM2_PEND	CPU1_ITAG_RAM1_PEND	CPU1_ITAG_RAM0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-761. SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE		Reserved
27	CPU1_KS_VIM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ks_vim_ramecc_pend Reset Source: r5ss_core_rst_mod_g_rst_n
26	B1TCM1_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm1_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
25	B1TCM1_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm1_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
24	B0TCM1_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm1_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
23	B0TCM1_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm1_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
22	ATCM1_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for atcm1_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
21	ATCM1_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for atcm1_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
20	CPU1_DDATA_RAM7_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddata_ram7_pend Reset Source: r5ss_core_rst_mod_g_rst_n
19	CPU1_DDATA_RAM6_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddata_ram6_pend Reset Source: r5ss_core_rst_mod_g_rst_n

Table 4-761. SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	CPU1_DDATA_RAM5_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddata_ram5_pend Reset Source: r5ss_core_rst_mod_g_rst_n
17	CPU1_DDATA_RAM4_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddata_ram4_pend Reset Source: r5ss_core_rst_mod_g_rst_n
16	CPU1_DDATA_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddata_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
15	CPU1_DDATA_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddata_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
14	CPU1_DDATA_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddata_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
13	CPU1_DDATA_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddata_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
12	CPU1_DDIRTY_RAM_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddirty_ram_pend Reset Source: r5ss_core_rst_mod_g_rst_n
11	CPU1_DTAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_dtag_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
10	CPU1_DTAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_dtag_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
9	CPU1_DTAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_dtag_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
8	CPU1_DTAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_dtag_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
7	CPU1_IDATA_BANK3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_idata_bank3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
6	CPU1_IDATA_BANK2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_idata_bank2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
5	CPU1_IDATA_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_idata_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
4	CPU1_IDATA_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_idata_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
3	CPU1_ITAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_itag_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
2	CPU1_ITAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_itag_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
1	CPU1_ITAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_itag_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
0	CPU1_ITAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_itag_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.45 ECC_AGG_CORE1_SEC_ENABLE_SET_REG0 Registers

4.6.45.1 ECC_CORE1_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Short Description: Interrupt Enable Set Reg

Long Description: Interrupt Enable Set Register 0

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Table 4-762. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 3080h
R5SS_CORE1	5300 7080h

Figure 4-355. SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU1_KS_VIM_RAMECC_ENABLE_SET	B1TCM1_BANK1_ENABLE_SET	B1TCM1_BANK0_ENABLE_SET	B0TCM1_BANK1_ENABLE_SET	B0TCM1_BANK0_ENABLE_SET	ATCM1_BANK1_ENABLE_SET	ATCM1_BANK0_ENABLE_SET	CPU1_DDATA_RAM7_ENABLE_SET	CPU1_DDATA_RAM6_ENABLE_SET	CPU1_DDATA_RAM5_ENABLE_SET	CPU1_DDATA_RAM4_ENABLE_SET	CPU1_DDATA_RAM3_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0				0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU1_DDATA_RAM2_ENABLE_SET	CPU1_DDATA_RAM1_ENABLE_SET	CPU1_DDATA_RAM0_ENABLE_SET	CPU1_DDIRTY_RAM_ENABLE_SET	CPU1_DTAG_RAM3_ENABLE_SET	CPU1_DTAG_RAM2_ENABLE_SET	CPU1_DTAG_RAM1_ENABLE_SET	CPU1_DTAG_RAM0_ENABLE_SET	CPU1_IDATA_BANK3_ENABLE_SET	CPU1_IDATA_BANK2_ENABLE_SET	CPU1_IDATA_BANK1_ENABLE_SET	CPU1_IDATA_BANK0_ENABLE_SET	CPU1_ITAG_RAM3_ENABLE_SET	CPU1_ITAG_RAM2_ENABLE_SET	CPU1_ITAG_RAM1_ENABLE_SET	CPU1_ITAG_RAM0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-763. SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE		Reserved
27	CPU1_KS_VIM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ks_vim_ramecc_pend Reset Source: r5ss_core_rst_mod_g_rst_n
26	B1TCM1_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm1_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
25	B1TCM1_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm1_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
24	B0TCM1_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm1_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
23	B0TCM1_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm1_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
22	ATCM1_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm1_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
21	ATCM1_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm1_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
20	CPU1_DDATA_RAM7_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddata_ram7_pend Reset Source: r5ss_core_rst_mod_g_rst_n

Table 4-763. SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	CPU1_DDATA_RAM6_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddata_ram6_pend Reset Source: r5ss_core_rst_mod_g_rst_n
18	CPU1_DDATA_RAM5_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddata_ram5_pend Reset Source: r5ss_core_rst_mod_g_rst_n
17	CPU1_DDATA_RAM4_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddata_ram4_pend Reset Source: r5ss_core_rst_mod_g_rst_n
16	CPU1_DDATA_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddata_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
15	CPU1_DDATA_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddata_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
14	CPU1_DDATA_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddata_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
13	CPU1_DDATA_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddata_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
12	CPU1_DDIRTY_RAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddirty_ram_pend Reset Source: r5ss_core_rst_mod_g_rst_n
11	CPU1_DTAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_dtag_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
10	CPU1_DTAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_dtag_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
9	CPU1_DTAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_dtag_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
8	CPU1_DTAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_dtag_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
7	CPU1_IDATA_BANK3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_idata_bank3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
6	CPU1_IDATA_BANK2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_idata_bank2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
5	CPU1_IDATA_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_idata_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
4	CPU1_IDATA_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_idata_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
3	CPU1_ITAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_itag_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
2	CPU1_ITAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_itag_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
1	CPU1_ITAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_itag_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
0	CPU1_ITAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_itag_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.46 ECC_AGG_CORE1_SEC_ENABLE_CLR_REG0 Registers

4.6.46.1 ECC_CORE1_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Short Description: Interrupt Enable Clear R

Long Description: Interrupt Enable Clear Register 0

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Table 4-764. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 30C0h
R5SS_CORE1	5300 70C0h

Figure 4-356. SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU1_KS_VIM_RAMECC_ENABLE_CLR	B1TCM1_BANK1_ENABLE_CLR	B1TCM1_BANK0_ENABLE_CLR	B0TCM1_BANK1_ENABLE_CLR	B0TCM1_BANK0_ENABLE_CLR	ATCM1_BANK1_ENABLE_CLR	ATCM1_BANK0_ENABLE_CLR	CPU1_DDATA_RAM7_ENABLE_CLR	CPU1_DDATA_RAM6_ENABLE_CLR	CPU1_DDATA_RAM5_ENABLE_CLR	CPU1_DDATA_RAM4_ENABLE_CLR	CPU1_DDATA_RAM3_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0				0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU1_DDATA_RAM2_ENABLE_CLR	CPU1_DDATA_RAM1_ENABLE_CLR	CPU1_DDATA_RAM0_ENABLE_CLR	CPU1_DDIRTY_RAM_ENABLE_CLR	CPU1_DTAG_RAM3_ENABLE_CLR	CPU1_DTAG_RAM2_ENABLE_CLR	CPU1_DTAG_RAM1_ENABLE_CLR	CPU1_DTAG_RAM0_ENABLE_CLR	CPU1_IDATA_BANK3_ENABLE_CLR	CPU1_IDATA_BANK2_ENABLE_CLR	CPU1_IDATA_BANK1_ENABLE_CLR	CPU1_IDATA_BANK0_ENABLE_CLR	CPU1_ITAG_RAM3_ENABLE_CLR	CPU1_ITAG_RAM2_ENABLE_CLR	CPU1_ITAG_RAM1_ENABLE_CLR	CPU1_ITAG_RAM0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-765. SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE		Reserved
27	CPU1_KS_VIM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ks_vim_ramecc_pend Reset Source: r5ss_core_rst_mod_g_rst_n
26	B1TCM1_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm1_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
25	B1TCM1_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm1_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
24	B0TCM1_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm1_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
23	B0TCM1_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm1_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
22	ATCM1_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm1_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
21	ATCM1_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm1_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
20	CPU1_DDATA_RAM7_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddata_ram7_pend Reset Source: r5ss_core_rst_mod_g_rst_n

Table 4-765. SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	CPU1_DDATA_RAM6_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddata_ram6_pend Reset Source: r5ss_core_rst_mod_g_rst_n
18	CPU1_DDATA_RAM5_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddata_ram5_pend Reset Source: r5ss_core_rst_mod_g_rst_n
17	CPU1_DDATA_RAM4_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddata_ram4_pend Reset Source: r5ss_core_rst_mod_g_rst_n
16	CPU1_DDATA_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddata_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
15	CPU1_DDATA_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddata_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
14	CPU1_DDATA_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddata_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
13	CPU1_DDATA_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddata_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
12	CPU1_DDIRTY_RAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddirty_ram_pend Reset Source: r5ss_core_rst_mod_g_rst_n
11	CPU1_DTAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_dtag_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
10	CPU1_DTAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_dtag_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
9	CPU1_DTAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_dtag_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
8	CPU1_DTAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_dtag_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
7	CPU1_IDATA_BANK3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_idata_bank3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
6	CPU1_IDATA_BANK2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_idata_bank2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
5	CPU1_IDATA_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_idata_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
4	CPU1_IDATA_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_idata_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
3	CPU1_ITAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_itag_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
2	CPU1_ITAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_itag_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
1	CPU1_ITAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_itag_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
0	CPU1_ITAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_itag_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.47 ECC_AGG_CORE1_DED_EOI_REG Registers

4.6.47.1 ECC_CORE1_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

Short Description: EOI Register

Long Description: EOI Register

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Table 4-766. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 313Ch
R5SS_CORE1	5300 713Ch

Figure 4-357. DED_EOI_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															EOI_WR
NONE															R/W1TS
0															0h

Access Types Legend

Table 4-767. DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	EOI_WR	R/W1TS	0h	EOI Register Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.48 ECC_AGG_CORE1_DED_STATUS_REG0 Registers

4.6.48.1 ECC_CORE1_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Short Description: Interrupt Status Registe

Long Description: Interrupt Status Register 0

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Table 4-768. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 3140h
R5SS_CORE1	5300 7140h

Figure 4-358. DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU1_KS_VIM_RAMECC_PEND	B1TCM1_BANK1_PEND	B1TCM1_BANK0_PEND	B0TCM1_BANK1_PEND	B0TCM1_BANK0_PEND	ATCM1_BANK1_PEND	ATCM1_BANK0_PEND	CPU1_DDATA_RAM7_PEND	CPU1_DDATA_RAM6_PEND	CPU1_DDATA_RAM5_PEND	CPU1_DDATA_RAM4_PEND	CPU1_DDATA_RAM3_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0				0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU1_DDATA_RAM2_PEND	CPU1_DDATA_RAM1_PEND	CPU1_DDATA_RAM0_PEND	CPU1_DDIRTY_RAM_PEND	CPU1_DTAG_RAM3_PEND	CPU1_DTAG_RAM2_PEND	CPU1_DTAG_RAM1_PEND	CPU1_DTAG_RAM0_PEND	CPU1_IDATA_BANK3_PEND	CPU1_IDATA_BANK2_PEND	CPU1_IDATA_BANK1_PEND	CPU1_IDATA_BANK0_PEND	CPU1_ITAG_RAM3_PEND	CPU1_ITAG_RAM2_PEND	CPU1_ITAG_RAM1_PEND	CPU1_ITAG_RAM0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-769. DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE		Reserved
27	CPU1_KS_VIM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ks_vim_ramecc_pend Reset Source: r5ss_core_rst_mod_g_rst_n
26	B1TCM1_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm1_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
25	B1TCM1_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm1_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
24	B0TCM1_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm1_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
23	B0TCM1_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm1_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
22	ATCM1_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for atcm1_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
21	ATCM1_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for atcm1_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
20	CPU1_DDATA_RAM7_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddata_ram7_pend Reset Source: r5ss_core_rst_mod_g_rst_n
19	CPU1_DDATA_RAM6_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddata_ram6_pend Reset Source: r5ss_core_rst_mod_g_rst_n

Table 4-769. DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	CPU1_DDATA_RAM5_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddata_ram5_pend Reset Source: r5ss_core_rst_mod_g_rst_n
17	CPU1_DDATA_RAM4_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddata_ram4_pend Reset Source: r5ss_core_rst_mod_g_rst_n
16	CPU1_DDATA_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddata_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
15	CPU1_DDATA_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddata_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
14	CPU1_DDATA_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddata_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
13	CPU1_DDATA_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddata_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
12	CPU1_DDIRTY_RAM_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddirty_ram_pend Reset Source: r5ss_core_rst_mod_g_rst_n
11	CPU1_DTAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_dtag_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
10	CPU1_DTAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_dtag_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
9	CPU1_DTAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_dtag_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
8	CPU1_DTAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_dtag_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
7	CPU1_IDATA_BANK3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_idata_bank3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
6	CPU1_IDATA_BANK2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_idata_bank2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
5	CPU1_IDATA_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_idata_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
4	CPU1_IDATA_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_idata_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
3	CPU1_ITAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_itag_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
2	CPU1_ITAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_itag_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
1	CPU1_ITAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_itag_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
0	CPU1_ITAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_itag_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.49 ECC_AGG_CORE1_DED_ENABLE_SET_REG0 Registers

4.6.49.1 ECC_CORE1_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Short Description: Interrupt Enable Set Reg

Long Description: Interrupt Enable Set Register 0

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Table 4-770. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 3180h
R5SS_CORE1	5300 7180h

Figure 4-359. DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU1_KS_VIM_RAMECC_ENABLE_SET	B1TCM1_BANK1_ENABLE_SET	B1TCM1_BANK0_ENABLE_SET	B0TCM1_BANK1_ENABLE_SET	B0TCM1_BANK0_ENABLE_SET	ATCM1_BANK1_ENABLE_SET	ATCM1_BANK0_ENABLE_SET	CPU1_DDATA_RAM7_ENABLE_SET	CPU1_DDATA_RAM6_ENABLE_SET	CPU1_DDATA_RAM5_ENABLE_SET	CPU1_DDATA_RAM4_ENABLE_SET	CPU1_DDATA_RAM3_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0				0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU1_DDATA_RAM2_ENABLE_SET	CPU1_DDATA_RAM1_ENABLE_SET	CPU1_DDATA_RAM0_ENABLE_SET	CPU1_DDIRTY_RAM_ENABLE_SET	CPU1_DTAG_RAM3_ENABLE_SET	CPU1_DTAG_RAM2_ENABLE_SET	CPU1_DTAG_RAM1_ENABLE_SET	CPU1_DTAG_RAM0_ENABLE_SET	CPU1_IDATA_BANK3_ENABLE_SET	CPU1_IDATA_BANK2_ENABLE_SET	CPU1_IDATA_BANK1_ENABLE_SET	CPU1_IDATA_BANK0_ENABLE_SET	CPU1_ITAG_RAM3_ENABLE_SET	CPU1_ITAG_RAM2_ENABLE_SET	CPU1_ITAG_RAM1_ENABLE_SET	CPU1_ITAG_RAM0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-771. DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE		Reserved
27	CPU1_KS_VIM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ks_vim_ramecc_pend Reset Source: r5ss_core_rst_mod_g_rst_n
26	B1TCM1_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm1_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
25	B1TCM1_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm1_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
24	B0TCM1_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm1_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
23	B0TCM1_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm1_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
22	ATCM1_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm1_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
21	ATCM1_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm1_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
20	CPU1_DDATA_RAM7_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddata_ram7_pend Reset Source: r5ss_core_rst_mod_g_rst_n

Table 4-771. DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	CPU1_DDATA_RAM6_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddata_ram6_pend Reset Source: r5ss_core_rst_mod_g_rst_n
18	CPU1_DDATA_RAM5_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddata_ram5_pend Reset Source: r5ss_core_rst_mod_g_rst_n
17	CPU1_DDATA_RAM4_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddata_ram4_pend Reset Source: r5ss_core_rst_mod_g_rst_n
16	CPU1_DDATA_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddata_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
15	CPU1_DDATA_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddata_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
14	CPU1_DDATA_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddata_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
13	CPU1_DDATA_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddata_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
12	CPU1_DDIRTY_RAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddirty_ram_pend Reset Source: r5ss_core_rst_mod_g_rst_n
11	CPU1_DTAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_dtag_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
10	CPU1_DTAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_dtag_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
9	CPU1_DTAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_dtag_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
8	CPU1_DTAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_dtag_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
7	CPU1_IDATA_BANK3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_idata_bank3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
6	CPU1_IDATA_BANK2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_idata_bank2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
5	CPU1_IDATA_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_idata_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
4	CPU1_IDATA_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_idata_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
3	CPU1_ITAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_itag_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
2	CPU1_ITAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_itag_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
1	CPU1_ITAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_itag_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
0	CPU1_ITAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_itag_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.50 ECC_AGG_CORE1_DED_ENABLE_CLR_REG0 Registers

4.6.50.1 ECC_CORE1_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Short Description: Interrupt Enable Clear R

Long Description: Interrupt Enable Clear Register 0

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Table 4-772. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 31C0h
R5SS_CORE1	5300 71C0h

Figure 4-360. DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU1_KS_VIM_RAMECC_ENABLE_CLR	B1TCM1_BANK1_ENABLE_CLR	B1TCM1_BANK0_ENABLE_CLR	B0TCM1_BANK1_ENABLE_CLR	B0TCM1_BANK0_ENABLE_CLR	ATCM1_BANK1_ENABLE_CLR	ATCM1_BANK0_ENABLE_CLR	CPU1_DDATA_RAM7_ENABLE_CLR	CPU1_DDATA_RAM6_ENABLE_CLR	CPU1_DDATA_RAM5_ENABLE_CLR	CPU1_DDATA_RAM4_ENABLE_CLR	CPU1_DDATA_RAM3_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0				0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU1_DDATA_RAM2_ENABLE_CLR	CPU1_DDATA_RAM1_ENABLE_CLR	CPU1_DDATA_RAM0_ENABLE_CLR	CPU1_DDIRTY_RAM_ENABLE_CLR	CPU1_DTAG_RAM3_ENABLE_CLR	CPU1_DTAG_RAM2_ENABLE_CLR	CPU1_DTAG_RAM1_ENABLE_CLR	CPU1_DTAG_RAM0_ENABLE_CLR	CPU1_IDATA_BANK3_ENABLE_CLR	CPU1_IDATA_BANK2_ENABLE_CLR	CPU1_IDATA_BANK1_ENABLE_CLR	CPU1_IDATA_BANK0_ENABLE_CLR	CPU1_ITAG_RAM3_ENABLE_CLR	CPU1_ITAG_RAM2_ENABLE_CLR	CPU1_ITAG_RAM1_ENABLE_CLR	CPU1_ITAG_RAM0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-773. DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE		Reserved
27	CPU1_KS_VIM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ks_vim_ramecc_pend Reset Source: r5ss_core_rst_mod_g_rst_n
26	B1TCM1_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm1_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
25	B1TCM1_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm1_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
24	B0TCM1_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm1_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
23	B0TCM1_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm1_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
22	ATCM1_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm1_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
21	ATCM1_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm1_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
20	CPU1_DDATA_RAM7_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddata_ram7_pend Reset Source: r5ss_core_rst_mod_g_rst_n

Table 4-773. DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	CPU1_DDATA_RAM6_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddata_ram6_pend Reset Source: r5ss_core_rst_mod_g_rst_n
18	CPU1_DDATA_RAM5_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddata_ram5_pend Reset Source: r5ss_core_rst_mod_g_rst_n
17	CPU1_DDATA_RAM4_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddata_ram4_pend Reset Source: r5ss_core_rst_mod_g_rst_n
16	CPU1_DDATA_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddata_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
15	CPU1_DDATA_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddata_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
14	CPU1_DDATA_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddata_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
13	CPU1_DDATA_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddata_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
12	CPU1_DDIRTY_RAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddirty_ram_pend Reset Source: r5ss_core_rst_mod_g_rst_n
11	CPU1_DTAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_dtag_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
10	CPU1_DTAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_dtag_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
9	CPU1_DTAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_dtag_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
8	CPU1_DTAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_dtag_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
7	CPU1_IDATA_BANK3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_idata_bank3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
6	CPU1_IDATA_BANK2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_idata_bank2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
5	CPU1_IDATA_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_idata_bank1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
4	CPU1_IDATA_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_idata_bank0_pend Reset Source: r5ss_core_rst_mod_g_rst_n
3	CPU1_ITAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_itag_ram3_pend Reset Source: r5ss_core_rst_mod_g_rst_n
2	CPU1_ITAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_itag_ram2_pend Reset Source: r5ss_core_rst_mod_g_rst_n
1	CPU1_ITAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_itag_ram1_pend Reset Source: r5ss_core_rst_mod_g_rst_n
0	CPU1_ITAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_itag_ram0_pend Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.51 ECC_AGG_CORE1_AGGR_ENABLE_SET Registers

4.6.51.1 ECC_CORE1_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

Short Description: AGGR interrupt enable se

Long Description: AGGR interrupt enable set Register

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Table 4-774. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 3200h
R5SS_CORE1	5300 7200h

Figure 4-361. AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														TIMEOUT	PARITY
NONE														R/W1TS	R/W1TS
0														0h	0h

Access Types Legend

Table 4-775. AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors Reset Source: r5ss_core_rst_mod_g_rst_n
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.52 ECC_AGG_CORE1_AGGR_ENABLE_CLR Registers

4.6.52.1 ECC_CORE1_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

Short Description: AGGR interrupt enable cl

Long Description: AGGR interrupt enable clear Register

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Table 4-776. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 3204h
R5SS_CORE1	5300 7204h

Figure 4-362. AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														TIMEOUT	PARITY
NONE														R/W1TC	R/W1TC
0														0h	0h

Access Types Legend

Table 4-777. AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors Reset Source: r5ss_core_rst_mod_g_rst_n
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.53 ECC_AGG_CORE1_AGGR_STATUS_SET Registers

4.6.53.1 ECC_CORE1_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

Short Description: AGGR interrupt status se

Long Description: AGGR interrupt status set Register

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Table 4-778. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 3208h
R5SS_CORE1	5300 7208h

Figure 4-363. AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												TIMEOUT		PARITY	
NONE												R/WI		R/WI	
0												0h		0h	

Access Types Legend

Table 4-779. AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors Reset Source: r5ss_core_rst_mod_g_rst_n
1:0	PARITY	R/WI	0h	interrupt status set for parity errors Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.54 ECC_AGG_CORE1_AGGR_STATUS_CLR Registers

4.6.54.1 ECC_CORE1_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

Short Description: AGGR interrupt status cl

Long Description: AGGR interrupt status clear Register

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Table 4-780. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5300 320Ch
R5SS_CORE1	5300 720Ch

Figure 4-364. AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												TIMEOUT		PARITY	
NONE												R/WD		R/WD	
0												0h		0h	

Access Types Legend

Table 4-781. AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors Reset Source: r5ss_core_rst_mod_g_rst_n
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.55 CCMR_CCMSR1 Registers

4.6.55.1 CCMR_CCMSR1 Register (Offset = 0h) [reset = 0h]

Short Description: CPU Compare Status Regist

Long Description: CPU Compare Status Register

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Table 4-782. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5321 0000h
R5SS_CORE1	5321 1000h

Figure 4-365. CCMSR1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU2															CMPE1
R/W															R/W
0h															0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU1							STC1	NU0						STET1	STE1
R/W							R/W	R/W						R/W	R
0h							0h	0h						0h	0h

Access Types Legend

Table 4-783. CCMSR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	NU2	R/W	0h	Reserved Reset Source: r5ss_core_rst_mod_g_rst_n
16	CMPE1	R/W	0h	Compare Error 0 = CPU signals are identical 1= CPU signal compare mismatch Writes '1' to clear this bit Reset Source: r5ss_core_rst_mod_g_rst_n
15:9	NU1	R/W	0h	Reserved Reset Source: r5ss_core_rst_mod_g_rst_n
8	STC1	R/W	0h	Self Test Complete 0 = self test on-going if self test mode asserted 1 = self test is complete Writes have no effect Reset Source: r5ss_core_rst_mod_g_rst_n
7:2	NU0	R/W	0h	Reserved Reset Source: r5ss_core_rst_mod_g_rst_n
1	STET1	R/W	0h	Self Test Error Type 0 = self test failed during Compare Match test 1 = self test failed during Compare mismatch test Writes have no effect Reset Source: r5ss_core_rst_mod_g_rst_n
0	STE1	R	0h	Self Test Error 0 = self test passed 1 = self test failed Writes have no effect Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.56 CCMR_CCMKEYR1 Registers

4.6.56.1 CCMR_CCMKEYR1 Register (Offset = 4h) [reset = 0h]

Short Description: CPU Compare Key Register

Long Description: CPU Compare Key Register

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Table 4-784. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5321 0004h
R5SS_CORE1	5321 1004h

Figure 4-366. CCMKEYR1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU3															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU3												MKEY1			
R/W												R/W			
0h												0h			

Access Types Legend

Table 4-785. CCMKEYR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	NU3	R/W	0h	Reserved Reset Source: r5ss_core_rst_mod_g_rst_n
3:0	MKEY1	R/W	0h	Mode Key 0000 = lock step mode 0110 = self test mode 1001 = error forcing mode 1111 = self test error forcing mode Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.57 CCMR_CCMSR2 Registers

4.6.57.1 CCMR_CCMSR2 Register (Offset = 8h) [reset = 0h]

Short Description: VIM Compare Status Regist

Long Description: VIM Compare Status Register

Return to Summary Table

Table 4-786. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5321 0008h
R5SS_CORE1	5321 1008h

Figure 4-367. CCMSR2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU6															CMPE2
R/W															R/W
0h															0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU5							STC2	NU4						STET2	STE2
R/W							R/W	R/W						R/W	R/W
0h							0h	0h						0h	0h

Access Types Legend

Table 4-787. CCMSR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	NU6	R/W	0h	Reserved Reset Source: r5ss_core_rst_mod_g_rst_n
16	CMPE2	R/W	0h	Compare Error 0 = VIM signals are identical 1= VIM signal compare mismatch Writes '1' to clear this bit Reset Source: r5ss_core_rst_mod_g_rst_n
15:9	NU5	R/W	0h	Reserved Reset Source: r5ss_core_rst_mod_g_rst_n
8	STC2	R/W	0h	Self Test Complete 0 = self test on-going if self test mode asserted 1 = self test is complete Writes have no effect Reset Source: r5ss_core_rst_mod_g_rst_n
7:2	NU4	R/W	0h	Reserved Reset Source: r5ss_core_rst_mod_g_rst_n
1	STET2	R/W	0h	Self Test Error Type 0 = self test failed during Compare Match test 1 = self test failed during Compare mismatch test Writes have no effect Reset Source: r5ss_core_rst_mod_g_rst_n
0	STE2	R/W	0h	Self Test Error 0 = self test passed 1 = self test failed Writes have no effect Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.58 CCMR_CCMKEYR2 Registers

4.6.58.1 CCMR_CCMKEYR2 Register (Offset = Ch) [reset = 0h]

Short Description: VIM Compare Key Register

Long Description: VIM Compare Key Register

Return to Summary Table

Table 4-788. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5321 000Ch
R5SS_CORE1	5321 100Ch

Figure 4-368. CCMKEYR2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU7															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU7												MKEY2			
R/W												R/W			
0h												0h			

Access Types Legend

Table 4-789. CCMKEYR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	NU7	R/W	0h	Reserved Reset Source: r5ss_core_rst_mod_g_rst_n
3:0	MKEY2	R/W	0h	Mode Key 0000 = lock step mode 0110 = self test mode 1001 = error forcing mode 1111 = self test error forcing mode Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.59 CCMR_CCMSR3 Registers

4.6.59.1 CCMR_CCMSR3 Register (Offset = 10h) [reset = 0h]

Short Description: Inactivity Monitor Status

Long Description: Inactivity Monitor Status Register

Return to Summary Table

Table 4-790. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5321 0010h
R5SS_CORE1	5321 1010h

Figure 4-369. CCMSR3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU10															CMPE3
R/W															R/W
0h															0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU9							STC3	NU8						STET3	STE3
R/W							R/W	R/W						R/W	R
0h							0h	0h						0h	0h

Access Types Legend

Table 4-791. CCMSR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	NU10	R/W	0h	Reserved Reset Source: r5ss_core_rst_mod_g_rst_n
16	CMPE3	R/W	0h	Compare Error 0 = Inactivity monitor signals are identical 1= Inactivity monitor signal compare mismatch Writes '1' to clear this bit Reset Source: r5ss_core_rst_mod_g_rst_n
15:9	NU9	R/W	0h	Reserved Reset Source: r5ss_core_rst_mod_g_rst_n
8	STC3	R/W	0h	Self Test Complete 0 = self test on-going if self test mode asserted 1 = self test is complete Writes have no effect Reset Source: r5ss_core_rst_mod_g_rst_n
7:2	NU8	R/W	0h	Reserved Reset Source: r5ss_core_rst_mod_g_rst_n
1	STET3	R/W	0h	Self Test Error Type 0 = self test failed during Compare Match test 1 = self test failed during Compare mismatch test Writes have no effect Reset Source: r5ss_core_rst_mod_g_rst_n
0	STE3	R	0h	Self Test Error 0 = self test passed 1 = self test failed Writes have no effect Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.60 CCMR_CCMKEYR3 Registers

4.6.60.1 CCMR_CCMKEYR3 Register (Offset = 14h) [reset = 0h]

Short Description: Inactivity Monitor Key Re

Long Description: Inactivity Monitor Key Register

Return to Summary Table

Table 4-792. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5321 0014h
R5SS_CORE1	5321 1014h

Figure 4-370. CCMKEYR3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU11															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU11												MKEY3			
R/W												R/W			
0h												0h			

Access Types Legend

Table 4-793. CCMKEYR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	NU11	R/W	0h	Reserved Reset Source: r5ss_core_rst_mod_g_rst_n
3:0	MKEY3	R/W	0h	Mode Key 0000 = lock step mode 0110 = self test mode 1001 = error forcing mode 1111 = self test error forcing mode Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.61 CCMR_CCMPOLCNTRL Registers

4.6.61.1 CCMR_CCMPOLCNTRL Register (Offset = 18h) [reset = 0h]

Short Description: CPU Compare Polarity Cont

Long Description: CPU Compare Polarity Control Register

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Table 4-794. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5321 0018h
R5SS_CORE1	5321 1018h

Figure 4-371. CCMPOLCNTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU12															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU12								POL_INV							
R/W								R							
0h								0h							

Access Types Legend

Table 4-795. CCMPOLCNTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	NU12	R/W	0h	Reserved Reset Source: r5ss_core_rst_mod_g_rst_n
7:0	POL_INV	R	0h	This value is used to invert the 8 XOR of the CPU1 to create compare fail in functional active compare mode. User and privilege mode read = Returns current value of the POL INV Privilege mode write = Update the values of POL INV Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.62 CCMR_CCMSR5 Registers

4.6.62.1 CCMR_CCMSR5 Register (Offset = 2Ch) [reset = 0h]

Short Description: TMU Compare Status Regist

Long Description: TMU Compare Status Register

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Table 4-796. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5321 002Ch
R5SS_CORE1	5321 102Ch

Figure 4-372. CCMSR5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU15															CMPE5
R/W															R/W
0h															0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU14							STC5	NU13						STET5	STE5
R/W							R/W	R/W						R/W	R
0h							0h	0h						0h	0h

Access Types Legend

Table 4-797. CCMSR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	NU15	R/W	0h	Reserved Reset Source: r5ss_core_rst_mod_g_rst_n
16	CMPE5	R/W	0h	Compare Error 0 = Inactivity monitor signals are identical 1= Inactivity monitor signal compare mismatch Writes '1' to clear this bit Reset Source: r5ss_core_rst_mod_g_rst_n
15:9	NU14	R/W	0h	Reserved Reset Source: r5ss_core_rst_mod_g_rst_n
8	STC5	R/W	0h	Self Test Complete 0 = self test on-going if self test mode asserted 1 = self test is complete Writes have no effect Reset Source: r5ss_core_rst_mod_g_rst_n
7:2	NU13	R/W	0h	Reserved Reset Source: r5ss_core_rst_mod_g_rst_n
1	STET5	R/W	0h	Self Test Error Type 0 = self test failed during Compare Match test 1 = self test failed during Compare mismatch test Writes have no effect Reset Source: r5ss_core_rst_mod_g_rst_n
0	STE5	R	0h	Self Test Error 0 = self test passed 1 = self test failed Writes have no effect Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.63 CCMR_CCMKEYR5 Registers

4.6.63.1 CCMR_CCMKEYR5 Register (Offset = 30h) [reset = 0h]

Short Description: TMU Compare Key Register

Long Description: TMU Compare Key Register

Return to Summary Table

Table 4-798. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5321 0030h
R5SS_CORE1	5321 1030h

Figure 4-373. CCMKEYR5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU16															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU16												MKEY5			
R/W												R/W			
0h												0h			

Access Types Legend

Table 4-799. CCMKEYR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	NU16	R/W	0h	Reserved Reset Source: r5ss_core_rst_mod_g_rst_n
3:0	MKEY5	R/W	0h	Mode Key 0000 = lock step mode 0110 = self test mode 1001 = error forcing mode 1111 = self test error forcing mode Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.64 CCMR_CCMSR6 Registers

4.6.64.1 CCMR_CCMSR6 Register (Offset = 34h) [reset = 0h]

Short Description: RL2 Compare Status Regist

Long Description: RL2 Compare Status Register

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Table 4-800. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5321 0034h
R5SS_CORE1	5321 1034h

Figure 4-374. CCMSR6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU19															CMPE6
R/W															R/W
0h															0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU18							STC6	NU17						STET6	STE6
R/W							R/W	R/W						R/W	R
0h							0h	0h						0h	0h

Access Types Legend

Table 4-801. CCMSR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	NU19	R/W	0h	Reserved Reset Source: r5ss_core_rst_mod_g_rst_n
16	CMPE6	R/W	0h	Compare Error 0 = Inactivity monitor signals are identical 1= Inactivity monitor signal compare mismatch Writes '1' to clear this bit Reset Source: r5ss_core_rst_mod_g_rst_n
15:9	NU18	R/W	0h	Reserved Reset Source: r5ss_core_rst_mod_g_rst_n
8	STC6	R/W	0h	Self Test Complete 0 = self test on-going if self test mode asserted 1 = self test is complete Writes have no effect Reset Source: r5ss_core_rst_mod_g_rst_n
7:2	NU17	R/W	0h	Reserved Reset Source: r5ss_core_rst_mod_g_rst_n
1	STET6	R/W	0h	Self Test Error Type 0 = self test failed during Compare Match test 1 = self test failed during Compare mismatch test Writes have no effect Reset Source: r5ss_core_rst_mod_g_rst_n
0	STE6	R	0h	Self Test Error 0 = self test passed 1 = self test failed Writes have no effect Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.65 CCMR_CCMKEYR6 Registers

4.6.65.1 CCMR_CCMKEYR6 Register (Offset = 38h) [reset = 0h]

Short Description: RL2 Compare Key Register

Long Description: RL2 Compare Key Register

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Table 4-802. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5321 0038h
R5SS_CORE1	5321 1038h

Figure 4-375. CCMKEYR6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU20															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU20												MKEY6			
R/W												R/W			
0h												0h			

Access Types Legend

Table 4-803. CCMKEYR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	NU20	R/W	0h	Reserved Reset Source: r5ss_core_rst_mod_g_rst_n
3:0	MKEY6	R/W	0h	Mode Key 0000 = lock step mode 0110 = self test mode 1001 = error forcing mode 1111 = self test error forcing mode Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.66 STC_STCGCR0 Registers

4.6.66.1 STC_STCGCR0 Register (Offset = 0h) [reset = 10120h]

Short Description: Self test Global control

Long Description: Self test Global control Reg0. *NOT BYTE ACCESSIBLE

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Table 4-804. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0000h
R5SS_CORE1	5351 0000h

Figure 4-376. STCGCR0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTCOUNT_B16															
R/W															
1h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU0					CAP_IDLE_CYCLE			SCANEN_HIGH_CAP_IDLE_CYCLE			NU1			RS_CNT_B1	
R					R/W			R/W			R			R/W	
0h					1h			1h			0h			0h	

Access Types Legend

Table 4-805. STCGCR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	INTCOUNT_B16	R/W	1h	Number of intervals of the self test run [RWP - Read, Priviledge Mode Write only] Count of intervals that need to be covered for a specific selftest run. The selftest controller sends out complete indication once it runs all of the intervals programmed in this field. INTCOUNT_B16=0 is an invalid configuration for a selftest. Reset Source: r5ss_core_rst_mod_g_rst_n
15:11	NU0	R	0h	Reserved bits Reset Source: r5ss_core_rst_mod_g_rst_n
10:8	CAP_IDLE_CYCLE	R/W	1h	Idle cycles before and after capture clock [RWP - Read, Priviledge Mode Write only] Idle Cycles before and after capture clock. This value is used to insert that many idle cycles in the Capture phase. Programmable idle cycles allow implementation flexibility on SCAN_EN signal at chip level based on the size of the UUT and timing requirements. Reset Source: r5ss_core_rst_mod_g_rst_n
7:5	SCANEN_HIGH_CAP_IDLE_CYCLE	R/W	1h	Idle cycles before and after capture clock [RWP - Read, Priviledge Mode Write only]. *NOT BYTE ACCESSIBLE Idle Cycles between scan_en going high to func_clk_en generation and scan_en going high to misr_log_en generation. This value is used to insert that many idle cycles in the shift clock [scan_en going high to func_clk_en generation] and misr_log_clk [scan_en going high to misr_log_en generation] generation. Programmable idle cycles allow implementation flexibility on SCAN_EN signal at chip level based on the size of the UUT and timing requirements. Reset Source: r5ss_core_rst_mod_g_rst_n
4:2	NU1	R	0h	Reserved bits Reset Source: r5ss_core_rst_mod_g_rst_n

Table 4-805. STCGCR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	RS_CNT_B1	R/W	0h	Restart/Continue or preload [RWP - Read, Priviledge Mode Write only] This bit specifies the selftest controller whether to continue the run from next interval onwards, restart from ROM address 0 or preload from a prescribed interval. This bit gets reset after the completion of selftest run. 00 = Continue NSTC run from previous interval 01 = Restart NSTC run from ROM address 0 1X = Start from segment number specified in STC_SEGPLR register Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.67 STC_STCGCR1 Registers

4.6.67.1 STC_STCGCR1 Register (Offset = 4h) [reset = 25h]

Short Description: Self test Global control

Long Description: Self test Global control Reg1

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Table 4-806. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0004h
R5SS_CORE1	5351 0004h

Figure 4-377. STCGCR1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU2															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU2				SEG0_CORE_SEL				NU3	CODEC_SPREAD_MODE	LP_SCAN_MODE	ROM_ACCESS_INV	ST_ENA_B4			
R				R/W				R	R/W	R/W	R/W	R/W			
0h				0h				0h	0h	1h	0h	5h			

Access Types Legend

Table 4-807. STCGCR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	NU2	R	0h	Reserved bits Reset Source: r5ss_core_rst_mod_g_rst_n
11:8	SEG0_CORE_SEL	R/W	0h	Selects the Segment0 CORE for self test [RWP - Read, Priviledge Mode Write only] Select the Segment0 CORE for Self -Test 0001 = Select CORE for selftest Other = CORE not selected. Reset Source: r5ss_core_rst_mod_g_rst_n
7	NU3	R	0h	Reserved bits Reset Source: r5ss_core_rst_mod_g_rst_n
6	CODEC_SPREAD_MODE	R/W	0h	Codec Spread Mode control signal [RWP - Read, Priviledge Mode Write only] This bit is used to configure the codec in spread / X-OR mode. 1 = Spread mode 0 = XOR mode Reset Source: r5ss_core_rst_mod_g_rst_n
5	LP_SCAN_MODE	R/W	1h	LP scan mode [RWP - Read, Priviledge Mode Write only] This bit is used to decide the scan configuration: 1 = Operates in Low Power Scan Mode. 0 = Operates in Normal Scan Mode. Reset Source: r5ss_core_rst_mod_g_rst_n
4	ROM_ACCESS_INV	R/W	0h	Rom access inversion mode [RWP - Read, Priviledge Mode Write only] - NOT SUPPORTED Reset Source: r5ss_core_rst_mod_g_rst_n
3:0	ST_ENA_B4	R/W	5h	Self test enable key [RWP - Read, Priviledge Mode Write only] 1010 = Self test run enabled All values other than 1010 = Self test run disabled Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.68 STC_STCTPR Registers

4.6.68.1 STC_STCTPR Register (Offset = 8h) [reset = ffffffffh]

Short Description: Time out counter preload

Long Description: Time out counter preload register

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Table 4-808. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0008h
R5SS_CORE1	5351 0008h

Figure 4-378. STCTPR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TO_PRELOAD															
R/W															
ffffffffh															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TO_PRELOAD															
R/W															
ffffffffh															

Access Types Legend

Table 4-809. STCTPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TO_PRELOAD	R/W	FFFFFFFFh	Self test time out preload [RWP - Read, Priviledge Mode Write only] This register contains the total number of STC clock cycles it will take before a self-test timeout error will be triggered after the initiation of the self-test run. This is a fail safe feature to avoid system hang-up situation on account of any run away self test issues. This register should be loaded with a meaningful count value for this feature to be effective. This register value [preload count value] gets loaded into the self test timeout down counter whenever a self test run is initiated [ST_ENA is enabled]. and gets disabled on completion of a self test run. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.69 STC_STC_CADDR Registers

4.6.69.1 STC_CADDR Register (Offset = Ch) [reset = 0h]

Short Description: Current Address register

Long Description: Current Address register for CORE1

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Table 4-810. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 000Ch
R5SS_CORE1	5351 000Ch

Figure 4-379. STC_CADDR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR															
R															
0h															

Access Types Legend

Table 4-811. STC_CADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR	R	0h	Current ROM Address for CORE1 This register reflects the current ROM address [for micro code load] accessed during selftest for CORE1 in of case segment0 and all the remaining segmentsn where n = 1 to 3]. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.70 STC_STCCICR Registers

4.6.70.1 STC_STCCICR Register (Offset = 10h) [reset = 0h]

Short Description: Current Interval count re

Long Description: Current Interval count register

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Table 4-812. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0010h
R5SS_CORE1	5351 0010h

Figure 4-380. STCCICR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CORE2_ICOUNT															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CORE1_ICOUNT															
R															
0h															

Access Types Legend

Table 4-813. STCCICR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CORE2_ICOUNT	R	0h	Specifies the last interval number for CORE2 This specifies the Last executed Interval number for CORE2 of Segment0 if self test is being executed for secondary core as well. This field is applicable only for Segment 0. Reset Source: r5ss_core_rst_mod_g_rst_n
15:0	CORE1_ICOUNT	R	0h	Specifies the last interval number for CORE1 This specifies the Last executed Interval number of a self-test run. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.71 STC_STCGSTAT Registers

4.6.71.1 STC_STCGSTAT Register (Offset = 14h) [reset = 500h]

Short Description: Global Status Register

Long Description: Global Status Register

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Table 4-814. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0014h
R5SS_CORE1	5351 0014h

Figure 4-381. STCGSTAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU4															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU4				ST_ACTIVE				NU5						TEST_FAIL	TEST_DONE
R				R				R						R	R
0h				5h				0h						0h	0h

Access Types Legend

Table 4-815. STCGSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	NU4	R	0h	Reserved bits Reset Source: r5ss_core_rst_mod_g_rst_n
11:8	ST_ACTIVE	R	5h	Tells whether self test is currently active or not. 1010 = Self test is active Others = SelfTest is not active Once the self-test completes and ST_ENA_B4 key is cleared, this field will reflect the inactive value. Reset Source: r5ss_core_rst_mod_g_rst_n
7:2	NU5	R	0h	Reserved bits Reset Source: r5ss_core_rst_mod_g_rst_n
1	TEST_FAIL	R	0h	Test_fail flag [RCP - Read, Clear on Writing in Priviledge Mode] 0 = Self test run has not failed 1 = SelfTest run has failed. Write Clear. Reset Source: r5ss_core_rst_mod_g_rst_n
0	TEST_DONE	R	0h	Test_done_flag [RCP - Read, Clear on Writing in Priviledge Mode] 0 = Not completed 1 = SelfTest run Completed Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.72 STC_STCFSTAT Registers

4.6.72.1 STC_STCFSTAT Register (Offset = 18h) [reset = 0h]

Short Description: Fail Status Register

Long Description: Fail Status Register

Return to Summary Table

Table 4-816. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0018h
R5SS_CORE1	5351 0018h

Figure 4-382. STCFSTAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU6															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU6											FSEG_ID		TO_ER_B1	CPU2_FAIL_B1	CPU1_FAIL_B1
R											R		R	R	R
0h											0h		0h	0h	0h

Access Types Legend

Table 4-817. STCFSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	NU6	R	0h	Reserved bits Reset Source: r5ss_core_rst_mod_g_rst_n
4:3	FSEG_ID	R	0h	Failed Segment ID [RCP - Read, Clear on Writing in Priviledge Mode] This field captures the Segment number for which any of the failures like TO_ER_B1, CPU1_FAIL_B1 and CPU2_FAIL_B1 occur. 00 = Failure on Segment 0 01 = Failure on Segment 1 10 = Failure on Segment 2 11 = Failure on Segment 3 Reset Source: r5ss_core_rst_mod_g_rst_n
2	TO_ER_B1	R	0h	Tells whether self test failed because of time out error [RCP - Read, Clear on Writing in Priviledge Mode] 0 = No time out error occurred 1 = SelfTest run failed due to a timeout error Reset Source: r5ss_core_rst_mod_g_rst_n
1	CPU2_FAIL_B1	R	0h	Tells whether MISR mismatch happenned in CORE2 when in Segment0 mode [RCP - Read, Clear on Writing in Priviledge Mode] 0 = No MISR mismatch for CORE2 1 = Self test run failed due to MISR mismatch for CORE2 Reset Source: r5ss_core_rst_mod_g_rst_n
0	CPU1_FAIL_B1	R	0h	Tells whether MISR mismatch happenned in CORE1 [RCP - Read, Clear on Writing in Priviledge Mode] Applicable to all segments. 0 = No MISR mismatch for CORE1 1 = Self test run failed due to MISR mismatch for CORE1 Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.73 STC_STCSCSCR Registers

4.6.73.1 STC_STCSCSCR Register (Offset = 1Ch) [reset = 5h]

Short Description: Signature compare Self Ch

Long Description: Signature compare Self Check Register

Return to Summary Table

Table 4-818. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 001Ch
R5SS_CORE1	5351 001Ch

Figure 4-383. STCSCSCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU7															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU7											FAULT_INS_B1	SELF_CHECK_KEY_B4			
R											R/W	R/W			
0h											0h	5h			

Access Types Legend

Table 4-819. STCSCSCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	NU7	R	0h	Reserved bits Reset Source: r5ss_core_rst_mod_g_rst_n
4	FAULT_INS_B1	R/W	0h	Fault Insertion bit [RWP - Read, Priviledge Mode Write only] 0 = No fault insertion. 1 = Inserts fault in the logic unedr test which will make signature compare fail. This feature is used as diagnostic check of the STC IP. Reset Source: r5ss_core_rst_mod_g_rst_n
3:0	SELF_CHECK_KEY_B4	R/W	5h	Signature compare logic self check key enable/disable [RWP - Read, Priviledge Mode Write only] 1010 = Signature compare logic Self Check is enabled All values other than 1010 = Signature compare logic Self Check is disabled Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.74 STC_STC_CADDR2 Registers

4.6.74.1 STC_CADDR2 Register (Offset = 20h) [reset = 0h]

Short Description: Current Address register

Long Description: Current Address register for CORE2

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Table 4-820. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0020h
R5SS_CORE1	5351 0020h

Figure 4-384. STC_CADDR2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR															
R															
0h															

Access Types Legend

Table 4-821. STC_CADDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR	R	0h	Current ROM Address for CORE2 This register reflects the current ROM address[for micro code load] accessed during selftest for CORE2 in of case segment0. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.75 STC_STC_CLKDIV Registers

4.6.75.1 STC_CLKDIV Register (Offset = 24h) [reset = 0h]

Short Description: Clock Divider Register

Long Description: Clock Divider Register

Return to Summary Table

Table 4-822. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0024h
R5SS_CORE1	5351 0024h

Figure 4-385. STC_CLKDIV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU8					CLKDIV0			NU9					CLKDIV1		
R					R/W			R					R/W		
0h					0h			0h					0h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU10					CLKDIV2			NU11					CLKDIV3		
R					R/W			R					R/W		
0h					0h			0h					0h		

Access Types Legend

Table 4-823. STC_CLKDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	NU8	R	0h	Reserved bits Reset Source: r5ss_core_rst_mod_g_rst_n
26:24	CLKDIV0	R/W	0h	Clock division for Seg0 [RWP - Read, Priviledge Mode Write only] *NOT SUPPORTED X = Division ratio is X+1 for Segment 0 Reset Source: r5ss_core_rst_mod_g_rst_n
23:19	NU9	R	0h	Reserved bits Reset Source: r5ss_core_rst_mod_g_rst_n
18:16	CLKDIV1	R/W	0h	Clock division for Seg1 [RWP - Read, Priviledge Mode Write only] *NOT SUPPORTED X = Division ratio is X+1 for Segment 1 Reset Source: r5ss_core_rst_mod_g_rst_n
15:11	NU10	R	0h	Reserved bits Reset Source: r5ss_core_rst_mod_g_rst_n
10:8	CLKDIV2	R/W	0h	Clock division for Seg2 [RWP - Read, Priviledge Mode Write only] *NOT SUPPORTED X = Division ratio is X+1 for Segment 2 Reset Source: r5ss_core_rst_mod_g_rst_n
7:3	NU11	R	0h	Reserved bits Reset Source: r5ss_core_rst_mod_g_rst_n
2:0	CLKDIV3	R/W	0h	Clock division for Seg3 [RWP - Read, Priviledge Mode Write only] *NOT SUPPORTED X = Division ratio is X+1 for Segment 3 Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.76 STC_STC_SEGPLR Registers

4.6.76.1 STC_SEGPLR Register (Offset = 28h) [reset = 0h]

Short Description: Segment 1st interval Prel

Long Description: Segment 1st interval Preload Register

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Table 4-824. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0028h
R5SS_CORE1	5351 0028h

Figure 4-386. STC_SEGPLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU12															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU12														SEGID_PLOAD	
R														R/W	
0h														0h	

Access Types Legend

Table 4-825. STC_SEGPLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	NU12	R	0h	Reserved bits Reset Source: r5ss_core_rst_mod_g_rst_n
1:0	SEGID_PLOAD	R/W	0h	Segment number for which preload is to be started [RWP - Read, Priviledge Mode Write only] This specifies the segment for which the address of its First interval will be pre-loaded into the NSTC ROM address counter. The 1st address of each segment are defined in SEGx_START_ADDR register.The address of the 1st interval of the selected segment is loaded into the NSTC ROM address counter when the RS_CNT_B1 bits of STC_GCR0 are set to 1X 00 = Preload the address of the 1st interval of segment 0. 01 = Preload the address of the 1st interval of segment 1. 10 = Preload the address of the 1st interval of segment 2. 11 = Preload the address of the 1st interval of segment 3. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.77 STC_SEG0_START_ADDR Registers

4.6.77.1 STC_START_ADDR Register (Offset = 2Ch) [reset = 0h]

Short Description: ROM Start address for Seg

Long Description: ROM Start address for Segment0

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Table 4-826. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 002Ch
R5SS_CORE1	5351 002Ch

Figure 4-387. SEG0_START_ADDR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU13												SEG_START_ADDR			
R												R/W			
0h												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEG_START_ADDR															
R/W															
0h															

Access Types Legend

Table 4-827. SEG0_START_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	NU13	R	0h	Reserved bits Reset Source: r5ss_core_rst_mod_g_rst_n
19:0	SEG_START_ADDR	R/W	0h	Segment 0 Start Address [RWP - Read, Priviledge Mode Write only] This register holds the ROM address for the start of first interval of the segment. When STC_GCR0.RS_CNT_B1 field is set to [1x] PRELOAD option, this register is used to determine the ROM start address for the Segment selected in ST_SEGPLR register. Valid number of bits depends on RTL paramerter ADDR Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.78 STC_SEG1_START_ADDR Registers

4.6.78.1 STC_START_ADDR Register (Offset = 30h) [reset = 0h]

Short Description: ROM Start address for Seg

Long Description: ROM Start address for Segment1

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Table 4-828. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0030h
R5SS_CORE1	5351 0030h

Figure 4-388. SEG1_START_ADDR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU14												SEG_START_ADDR			
R												R/W			
0h												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEG_START_ADDR															
R/W															
0h															

Access Types Legend

Table 4-829. SEG1_START_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	NU14	R	0h	Reserved bits Reset Source: r5ss_core_rst_mod_g_rst_n
19:0	SEG_START_ADDR	R/W	0h	Segment 1 Start Address [RWP - Read, Priviledge Mode Write only] This register holds the ROM address for the start of first interval of the segment. When STC_GCR0.RS_CNT_B1 field is set to [1x] PRELOAD option, this register is used to determine the ROM start address for the Segment selected in ST_SEGPLR register. Valid number of bits depends on RTL paramerter ADDR. This register is present only when RTL parameter NUM_SEG = 1. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.79 STC_SEG2_START_ADDR Registers

4.6.79.1 STC_START_ADDR Register (Offset = 34h) [reset = 0h]

Short Description: ROM Start address for Seg

Long Description: ROM Start address for Segment2

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Table 4-830. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0034h
R5SS_CORE1	5351 0034h

Figure 4-389. SEG2_START_ADDR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU15												SEG_START_ADDR			
R												R/W			
0h												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEG_START_ADDR															
R/W															
0h															

Access Types Legend

Table 4-831. SEG2_START_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	NU15	R	0h	Reserved bits Reset Source: r5ss_core_rst_mod_g_rst_n
19:0	SEG_START_ADDR	R/W	0h	Segment 2 Start Address [RWP - Read, Priviledge Mode Write only] This register holds the ROM address for the start of first interval of the segment. When STC_GCR0.RS_CNT_B1 field is set to [1x] PRELOAD option, this register is used to determine the ROM start address for the Segment selected in ST_SEGPLR register. Valid number of bits depends on RTL paramerter ADDR. This register is present only when RTL parameter NUM_SEG = 2. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.80 STC_SEG3_START_ADDR Registers

4.6.80.1 STC_START_ADDR Register (Offset = 38h) [reset = 0h]

Short Description: ROM Start address for Seg

Long Description: ROM Start address for Segment3

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Table 4-832. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0038h
R5SS_CORE1	5351 0038h

Figure 4-390. SEG3_START_ADDR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU16												SEG_START_ADDR			
R												R/W			
0h												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEG_START_ADDR															
R/W															
0h															

Access Types Legend

Table 4-833. SEG3_START_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	NU16	R	0h	Reserved bits Reset Source: r5ss_core_rst_mod_g_rst_n
19:0	SEG_START_ADDR	R/W	0h	Segment 3 Start Address [RWP - Read, Priviledge Mode Write only] This register holds the ROM address for the start of first interval of the segment. When STC_GCR0.RS_CNT_B1 field is set to [1x] PRELOAD option, this register is used to determine the ROM start address for the Segment selected in ST_SEGPLR register. Valid number of bits depends on RTL paramerter ADDR. This register is present only when RTL parameter NUM_SEG = 3. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.81 STC_CORE1_CURMISR_0 Registers

4.6.81.1 STC_CURMISR_0 Register (Offset = 3Ch) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE1

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Table 4-834. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 003Ch
R5SS_CORE1	5351 003Ch

Figure 4-391. CORE1_CURMISR_0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR0															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR0															
R															
0h															

Access Types Legend

Table 4-835. CORE1_CURMISR_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR0	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.82 STC_CORE1_CURMISR_1 Registers

4.6.82.1 STC_CURMISR_1 Register (Offset = 40h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE1

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Table 4-836. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0040h
R5SS_CORE1	5351 0040h

Figure 4-392. CORE1_CURMISR_1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR1															
R															
0h															

Access Types Legend

Table 4-837. CORE1_CURMISR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR1	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.83 STC_CORE1_CURMISR_2 Registers

4.6.83.1 STC_CURMISR_2 Register (Offset = 44h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE1

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Table 4-838. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0044h
R5SS_CORE1	5351 0044h

Figure 4-393. CORE1_CURMISR_2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR2															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR2															
R															
0h															

Access Types Legend

Table 4-839. CORE1_CURMISR_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR2	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.84 STC_CORE1_CURMISR_3 Registers

4.6.84.1 STC_CURMISR_3 Register (Offset = 48h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE1

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Table 4-840. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0048h
R5SS_CORE1	5351 0048h

Figure 4-394. CORE1_CURMISR_3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR3															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR3															
R															
0h															

Access Types Legend

Table 4-841. CORE1_CURMISR_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR3	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.85 STC_CORE1_CURMISR_4 Registers

4.6.85.1 STC_CURMISR_4 Register (Offset = 4Ch) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE1

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Table 4-842. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 004Ch
R5SS_CORE1	5351 004Ch

Figure 4-395. CORE1_CURMISR_4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR4															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR4															
R															
0h															

Access Types Legend

Table 4-843. CORE1_CURMISR_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR4	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.86 STC_CORE1_CURMISR_5 Registers

4.6.86.1 STC_CURMISR_5 Register (Offset = 50h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE1

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Table 4-844. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0050h
R5SS_CORE1	5351 0050h

Figure 4-396. CORE1_CURMISR_5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR5															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR5															
R															
0h															

Access Types Legend

Table 4-845. CORE1_CURMISR_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR5	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.87 STC_CORE1_CURMISR_6 Registers

4.6.87.1 STC_CURMISR_6 Register (Offset = 54h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE1

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Table 4-846. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0054h
R5SS_CORE1	5351 0054h

Figure 4-397. CORE1_CURMISR_6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR6															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR6															
R															
0h															

Access Types Legend

Table 4-847. CORE1_CURMISR_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR6	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.88 STC_CORE1_CURMISR_7 Registers

4.6.88.1 STC_CURMISR_7 Register (Offset = 58h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE1

Return to Summary Table

Table 4-848. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0058h
R5SS_CORE1	5351 0058h

Figure 4-398. CORE1_CURMISR_7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR7															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR7															
R															
0h															

Access Types Legend

Table 4-849. CORE1_CURMISR_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR7	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.89 STC_CORE1_CURMISR_8 Registers

4.6.89.1 STC_CURMISR_8 Register (Offset = 5Ch) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE1

Return to Summary Table

Table 4-850. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 005Ch
R5SS_CORE1	5351 005Ch

Figure 4-399. CORE1_CURMISR_8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR8															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR8															
R															
0h															

Access Types Legend

Table 4-851. CORE1_CURMISR_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR8	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.90 STC_CORE1_CURMISR_9 Registers

4.6.90.1 STC_CURMISR_9 Register (Offset = 60h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE1

Return to Summary Table

Table 4-852. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0060h
R5SS_CORE1	5351 0060h

Figure 4-400. CORE1_CURMISR_9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR9															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR9															
R															
0h															

Access Types Legend

Table 4-853. CORE1_CURMISR_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR9	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.91 STC_CORE1_CURMISR_10 Registers

4.6.91.1 STC_CURMISR_10 Register (Offset = 64h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE1

Return to Summary Table

Table 4-854. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0064h
R5SS_CORE1	5351 0064h

Figure 4-401. CORE1_CURMISR_10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR10															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR10															
R															
0h															

Access Types Legend

Table 4-855. CORE1_CURMISR_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR10	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.92 STC_CORE1_CURMISR_11 Registers

4.6.92.1 STC_CURMISR_11 Register (Offset = 68h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE1

Return to Summary Table

Table 4-856. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0068h
R5SS_CORE1	5351 0068h

Figure 4-402. CORE1_CURMISR_11 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR11															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR11															
R															
0h															

Access Types Legend

Table 4-857. CORE1_CURMISR_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR11	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.93 STC_CORE1_CURMISR_12 Registers

4.6.93.1 STC_CURMISR_12 Register (Offset = 6Ch) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE1

Return to Summary Table

Table 4-858. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 006Ch
R5SS_CORE1	5351 006Ch

Figure 4-403. CORE1_CURMISR_12 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR12															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR12															
R															
0h															

Access Types Legend

Table 4-859. CORE1_CURMISR_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR12	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.94 STC_CORE1_CURMISR_13 Registers

4.6.94.1 STC_CURMISR_13 Register (Offset = 70h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE1

Return to Summary Table

Table 4-860. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0070h
R5SS_CORE1	5351 0070h

Figure 4-404. CORE1_CURMISR_13 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR13															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR13															
R															
0h															

Access Types Legend

Table 4-861. CORE1_CURMISR_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR13	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.95 STC_CORE1_CURMISR_14 Registers

4.6.95.1 STC_CURMISR_14 Register (Offset = 74h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE1

Return to Summary Table

Table 4-862. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0074h
R5SS_CORE1	5351 0074h

Figure 4-405. CORE1_CURMISR_14 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR14															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR14															
R															
0h															

Access Types Legend

Table 4-863. CORE1_CURMISR_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR14	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.96 STC_CORE1_CURMISR_15 Registers

4.6.96.1 STC_CURMISR_15 Register (Offset = 78h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE1

Return to Summary Table

Table 4-864. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0078h
R5SS_CORE1	5351 0078h

Figure 4-406. CORE1_CURMISR_15 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR15															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR15															
R															
0h															

Access Types Legend

Table 4-865. CORE1_CURMISR_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR15	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.97 STC_CORE1_CURMISR_16 Registers

4.6.97.1 STC_CURMISR_16 Register (Offset = 7Ch) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE1

Return to Summary Table

Table 4-866. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 007Ch
R5SS_CORE1	5351 007Ch

Figure 4-407. CORE1_CURMISR_16 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR16															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR16															
R															
0h															

Access Types Legend

Table 4-867. CORE1_CURMISR_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR16	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.98 STC_CORE1_CURMISR_17 Registers

4.6.98.1 STC_CURMISR_17 Register (Offset = 80h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE1

Return to Summary Table

Table 4-868. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0080h
R5SS_CORE1	5351 0080h

Figure 4-408. CORE1_CURMISR_17 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR17															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR17															
R															
0h															

Access Types Legend

Table 4-869. CORE1_CURMISR_17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR17	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.99 STC_CORE1_CURMISR_18 Registers

4.6.99.1 STC_CURMISR_18 Register (Offset = 84h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE1

Return to Summary Table

Table 4-870. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0084h
R5SS_CORE1	5351 0084h

Figure 4-409. CORE1_CURMISR_18 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR18															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR18															
R															
0h															

Access Types Legend

Table 4-871. CORE1_CURMISR_18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR18	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.100 STC_CORE1_CURMISR_19 Registers

4.6.100.1 STC_CURMISR_19 Register (Offset = 88h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE1

Return to Summary Table

Table 4-872. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0088h
R5SS_CORE1	5351 0088h

Figure 4-410. CORE1_CURMISR_19 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR19															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR19															
R															
0h															

Access Types Legend

Table 4-873. CORE1_CURMISR_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR19	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.101 STC_CORE1_CURMISR_20 Registers

4.6.101.1 STC_CURMISR_20 Register (Offset = 8Ch) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE1

Return to Summary Table

Table 4-874. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 008Ch
R5SS_CORE1	5351 008Ch

Figure 4-411. CORE1_CURMISR_20 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR20															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR20															
R															
0h															

Access Types Legend

Table 4-875. CORE1_CURMISR_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR20	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.102 STC_CORE1_CURMISR_21 Registers

4.6.102.1 STC_CURMISR_21 Register (Offset = 90h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE1

Return to Summary Table

Table 4-876. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0090h
R5SS_CORE1	5351 0090h

Figure 4-412. CORE1_CURMISR_21 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR21															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR21															
R															
0h															

Access Types Legend

Table 4-877. CORE1_CURMISR_21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR21	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.103 STC_CORE1_CURMISR_22 Registers

4.6.103.1 STC_CURMISR_22 Register (Offset = 94h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE1

Return to Summary Table

Table 4-878. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0094h
R5SS_CORE1	5351 0094h

Figure 4-413. CORE1_CURMISR_22 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR22															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR22															
R															
0h															

Access Types Legend

Table 4-879. CORE1_CURMISR_22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR22	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.104 STC_CORE1_CURMISR_23 Registers

4.6.104.1 STC_CURMISR_23 Register (Offset = 98h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE1

Return to Summary Table

Table 4-880. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0098h
R5SS_CORE1	5351 0098h

Figure 4-414. CORE1_CURMISR_23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR23															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR23															
R															
0h															

Access Types Legend

Table 4-881. CORE1_CURMISR_23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR23	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.105 STC_CORE1_CURMISR_24 Registers

4.6.105.1 STC_CURMISR_24 Register (Offset = 9Ch) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE1

Return to Summary Table

Table 4-882. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 009Ch
R5SS_CORE1	5351 009Ch

Figure 4-415. CORE1_CURMISR_24 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR24															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR24															
R															
0h															

Access Types Legend

Table 4-883. CORE1_CURMISR_24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR24	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.106 STC_CORE1_CURMISR_25 Registers

4.6.106.1 STC_CURMISR_25 Register (Offset = A0h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE1

Return to Summary Table

Table 4-884. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 00A0h
R5SS_CORE1	5351 00A0h

Figure 4-416. CORE1_CURMISR_25 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR25															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR25															
R															
0h															

Access Types Legend

Table 4-885. CORE1_CURMISR_25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR25	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.107 STC_CORE1_CURMISR_26 Registers

4.6.107.1 STC_CURMISR_26 Register (Offset = A4h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE1

Return to Summary Table

Table 4-886. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 00A4h
R5SS_CORE1	5351 00A4h

Figure 4-417. CORE1_CURMISR_26 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR26															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR26															
R															
0h															

Access Types Legend

Table 4-887. CORE1_CURMISR_26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR26	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.108 STC_CORE1_CURMISR_27 Registers

4.6.108.1 STC_CURMISR_27 Register (Offset = A8h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE1

Return to Summary Table

Table 4-888. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 00A8h
R5SS_CORE1	5351 00A8h

Figure 4-418. CORE1_CURMISR_27 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR27															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR27															
R															
0h															

Access Types Legend

Table 4-889. CORE1_CURMISR_27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR27	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.109 STC_CORE2_CURMISR_0 Registers

4.6.109.1 STC_CURMISR_0 Register (Offset = ACh) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE2

Return to Summary Table

Table 4-890. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 00ACh
R5SS_CORE1	5351 00ACh

Figure 4-419. CORE2_CURMISR_0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR0															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR0															
R															
0h															

Access Types Legend

Table 4-891. CORE2_CURMISR_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR0	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.110 STC_CORE2_CURMISR_1 Registers

4.6.110.1 STC_CURMISR_1 Register (Offset = B0h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE2

Return to Summary Table

Table 4-892. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 00B0h
R5SS_CORE1	5351 00B0h

Figure 4-420. CORE2_CURMISR_1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR1															
R															
0h															

Access Types Legend

Table 4-893. CORE2_CURMISR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR1	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.111 STC_CORE2_CURMISR_2 Registers

4.6.111.1 STC_CURMISR_2 Register (Offset = B4h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE2

Return to Summary Table

Table 4-894. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 00B4h
R5SS_CORE1	5351 00B4h

Figure 4-421. CORE2_CURMISR_2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR2															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR2															
R															
0h															

Access Types Legend

Table 4-895. CORE2_CURMISR_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR2	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.112 STC_CORE2_CURMISR_3 Registers

4.6.112.1 STC_CURMISR_3 Register (Offset = B8h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE2

Return to Summary Table

Table 4-896. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 00B8h
R5SS_CORE1	5351 00B8h

Figure 4-422. CORE2_CURMISR_3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR3															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR3															
R															
0h															

Access Types Legend

Table 4-897. CORE2_CURMISR_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR3	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.113 STC_CORE2_CURMISR_4 Registers

4.6.113.1 STC_CURMISR_4 Register (Offset = BCh) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE2

Return to Summary Table

Table 4-898. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 00BCh
R5SS_CORE1	5351 00BCh

Figure 4-423. CORE2_CURMISR_4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR4															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR4															
R															
0h															

Access Types Legend

Table 4-899. CORE2_CURMISR_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR4	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.114 STC_CORE2_CURMISR_5 Registers

4.6.114.1 STC_CURMISR_5 Register (Offset = C0h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE2

Return to Summary Table

Table 4-900. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 00C0h
R5SS_CORE1	5351 00C0h

Figure 4-424. CORE2_CURMISR_5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR5															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR5															
R															
0h															

Access Types Legend

Table 4-901. CORE2_CURMISR_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR5	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.115 STC_CORE2_CURMISR_6 Registers

4.6.115.1 STC_CURMISR_6 Register (Offset = C4h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE2

Return to Summary Table

Table 4-902. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 00C4h
R5SS_CORE1	5351 00C4h

Figure 4-425. CORE2_CURMISR_6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR6															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR6															
R															
0h															

Access Types Legend

Table 4-903. CORE2_CURMISR_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR6	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.116 STC_CORE2_CURMISR_7 Registers

4.6.116.1 STC_CURMISR_7 Register (Offset = C8h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE2

Return to Summary Table

Table 4-904. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 00C8h
R5SS_CORE1	5351 00C8h

Figure 4-426. CORE2_CURMISR_7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR7															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR7															
R															
0h															

Access Types Legend

Table 4-905. CORE2_CURMISR_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR7	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.117 STC_CORE2_CURMISR_8 Registers

4.6.117.1 STC_CURMISR_8 Register (Offset = CCh) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE2

Return to Summary Table

Table 4-906. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 00CCh
R5SS_CORE1	5351 00CCh

Figure 4-427. CORE2_CURMISR_8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR8															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR8															
R															
0h															

Access Types Legend

Table 4-907. CORE2_CURMISR_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR8	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.118 STC_CORE2_CURMISR_9 Registers

4.6.118.1 STC_CURMISR_9 Register (Offset = D0h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE2

Return to Summary Table

Table 4-908. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 00D0h
R5SS_CORE1	5351 00D0h

Figure 4-428. CORE2_CURMISR_9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR9															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR9															
R															
0h															

Access Types Legend

Table 4-909. CORE2_CURMISR_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR9	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.119 STC_CORE2_CURMISR_10 Registers

4.6.119.1 STC_CURMISR_10 Register (Offset = D4h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE2

Return to Summary Table

Table 4-910. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 00D4h
R5SS_CORE1	5351 00D4h

Figure 4-429. CORE2_CURMISR_10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR10															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR10															
R															
0h															

Access Types Legend

Table 4-911. CORE2_CURMISR_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR10	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.120 STC_CORE2_CURMISR_11 Registers

4.6.120.1 STC_CURMISR_11 Register (Offset = D8h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE2

Return to Summary Table

Table 4-912. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 00D8h
R5SS_CORE1	5351 00D8h

Figure 4-430. CORE2_CURMISR_11 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR11															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR11															
R															
0h															

Access Types Legend

Table 4-913. CORE2_CURMISR_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR11	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.121 STC_CORE2_CURMISR_12 Registers

4.6.121.1 STC_CURMISR_12 Register (Offset = DCh) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE2

Return to Summary Table

Table 4-914. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 00DCh
R5SS_CORE1	5351 00DCh

Figure 4-431. CORE2_CURMISR_12 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR12															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR12															
R															
0h															

Access Types Legend

Table 4-915. CORE2_CURMISR_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR12	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.122 STC_CORE2_CURMISR_13 Registers

4.6.122.1 STC_CURMISR_13 Register (Offset = E0h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE2

Return to Summary Table

Table 4-916. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 00E0h
R5SS_CORE1	5351 00E0h

Figure 4-432. CORE2_CURMISR_13 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR13															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR13															
R															
0h															

Access Types Legend

Table 4-917. CORE2_CURMISR_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR13	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.123 STC_CORE2_CURMISR_14 Registers

4.6.123.1 STC_CURMISR_14 Register (Offset = E4h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE2

Return to Summary Table

Table 4-918. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 00E4h
R5SS_CORE1	5351 00E4h

Figure 4-433. CORE2_CURMISR_14 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR14															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR14															
R															
0h															

Access Types Legend

Table 4-919. CORE2_CURMISR_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR14	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.124 STC_CORE2_CURMISR_15 Registers

4.6.124.1 STC_CURMISR_15 Register (Offset = E8h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE2

Return to Summary Table

Table 4-920. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 00E8h
R5SS_CORE1	5351 00E8h

Figure 4-434. CORE2_CURMISR_15 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR15															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR15															
R															
0h															

Access Types Legend

Table 4-921. CORE2_CURMISR_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR15	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.125 STC_CORE2_CURMISR_16 Registers

4.6.125.1 STC_CURMISR_16 Register (Offset = ECh) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE2

Return to Summary Table

Table 4-922. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 00ECh
R5SS_CORE1	5351 00ECh

Figure 4-435. CORE2_CURMISR_16 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR16															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR16															
R															
0h															

Access Types Legend

Table 4-923. CORE2_CURMISR_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR16	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.126 STC_CORE2_CURMISR_17 Registers

4.6.126.1 STC_CURMISR_17 Register (Offset = F0h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE2

Return to Summary Table

Table 4-924. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 00F0h
R5SS_CORE1	5351 00F0h

Figure 4-436. CORE2_CURMISR_17 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR17															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR17															
R															
0h															

Access Types Legend

Table 4-925. CORE2_CURMISR_17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR17	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.127 STC_CORE2_CURMISR_18 Registers

4.6.127.1 STC_CURMISR_18 Register (Offset = F4h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE2

Return to Summary Table

Table 4-926. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 00F4h
R5SS_CORE1	5351 00F4h

Figure 4-437. CORE2_CURMISR_18 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR18															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR18															
R															
0h															

Access Types Legend

Table 4-927. CORE2_CURMISR_18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR18	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.128 STC_CORE2_CURMISR_19 Registers

4.6.128.1 STC_CURMISR_19 Register (Offset = F8h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE2

Return to Summary Table

Table 4-928. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 00F8h
R5SS_CORE1	5351 00F8h

Figure 4-438. CORE2_CURMISR_19 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR19															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR19															
R															
0h															

Access Types Legend

Table 4-929. CORE2_CURMISR_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR19	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.129 STC_CORE2_CURMISR_20 Registers

4.6.129.1 STC_CURMISR_20 Register (Offset = FCh) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE2

Return to Summary Table

Table 4-930. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 00FCh
R5SS_CORE1	5351 00FCh

Figure 4-439. CORE2_CURMISR_20 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR20															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR20															
R															
0h															

Access Types Legend

Table 4-931. CORE2_CURMISR_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR20	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.130 STC_CORE2_CURMISR_21 Registers

4.6.130.1 STC_CURMISR_21 Register (Offset = 100h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE2

Return to Summary Table

Table 4-932. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0100h
R5SS_CORE1	5351 0100h

Figure 4-440. CORE2_CURMISR_21 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR21															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR21															
R															
0h															

Access Types Legend

Table 4-933. CORE2_CURMISR_21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR21	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.131 STC_CORE2_CURMISR_22 Registers

4.6.131.1 STC_CURMISR_22 Register (Offset = 104h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE2

Return to Summary Table

Table 4-934. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0104h
R5SS_CORE1	5351 0104h

Figure 4-441. CORE2_CURMISR_22 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR22															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR22															
R															
0h															

Access Types Legend

Table 4-935. CORE2_CURMISR_22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR22	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.132 STC_CORE2_CURMISR_23 Registers

4.6.132.1 STC_CURMISR_23 Register (Offset = 108h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE2

Return to Summary Table

Table 4-936. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0108h
R5SS_CORE1	5351 0108h

Figure 4-442. CORE2_CURMISR_23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR23															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR23															
R															
0h															

Access Types Legend

Table 4-937. CORE2_CURMISR_23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR23	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.133 STC_CORE2_CURMISR_24 Registers

4.6.133.1 STC_CURMISR_24 Register (Offset = 10Ch) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE2

Return to Summary Table

Table 4-938. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 010Ch
R5SS_CORE1	5351 010Ch

Figure 4-443. CORE2_CURMISR_24 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR24															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR24															
R															
0h															

Access Types Legend

Table 4-939. CORE2_CURMISR_24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR24	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.134 STC_CORE2_CURMISR_25 Registers

4.6.134.1 STC_CURMISR_25 Register (Offset = 110h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE2

Return to Summary Table

Table 4-940. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0110h
R5SS_CORE1	5351 0110h

Figure 4-444. CORE2_CURMISR_25 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR25															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR25															
R															
0h															

Access Types Legend

Table 4-941. CORE2_CURMISR_25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR25	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.135 STC_CORE2_CURMISR_26 Registers

4.6.135.1 STC_CURMISR_26 Register (Offset = 114h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE2

Return to Summary Table

Table 4-942. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0114h
R5SS_CORE1	5351 0114h

Figure 4-445. CORE2_CURMISR_26 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR26															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR26															
R															
0h															

Access Types Legend

Table 4-943. CORE2_CURMISR_26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR26	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.136 STC_CORE2_CURMISR_27 Registers

4.6.136.1 STC_CURMISR_27 Register (Offset = 118h) [reset = 0h]

Short Description: Holds the MISR signature

Long Description: Holds the MISR signature for CORE2

Return to Summary Table

Table 4-944. Instance Table

Instance Name	Physical Address
R5SS_CORE0	5350 0118h
R5SS_CORE1	5351 0118h

Figure 4-446. CORE2_CURMISR_27 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR27															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR27															
R															
0h															

Access Types Legend

Table 4-945. CORE2_CURMISR_27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR27	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.137 ICACHE_CORE0_START Registers

4.6.137.1 ICACHE_START Register (Offset = 0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 4-946. Instance Table

Instance Name	Physical Address
R5SS_CORE0	7400 0000h
R5SS_CORE1	7600 0000h

Figure 4-447. START Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START															
R/W															
0h															

Access Types Legend

Table 4-947. START Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START	R/W	0h	Memory start address Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.138 ICACHE_CORE0_END Registers

4.6.138.1 ICACHE_END Register (Offset = 7FFFFCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 4-948. Instance Table

Instance Name	Physical Address
R5SS_CORE0	747F FFFCh
R5SS_CORE1	767F FFFCh

Figure 4-448. END Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END															
R/W															
0h															

Access Types Legend

Table 4-949. END Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END	R/W	0h	Memory end address Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.139 DCACHE_CORE0_START Registers

4.6.139.1 DCACHE_START Register (Offset = 0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 4-950. Instance Table

Instance Name	Physical Address
R5SS_CORE0	7480 0000h
R5SS_CORE1	7680 0000h

Figure 4-449. START Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START															
R/W															
0h															

Access Types Legend

Table 4-951. START Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START	R/W	0h	Memory start address Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.140 DCACHE_CORE0_END Registers

4.6.140.1 DCACHE_END Register (Offset = 7FFFFCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 4-952. Instance Table

Instance Name	Physical Address
R5SS_CORE0	74FF FFFCh
R5SS_CORE1	76FF FFFCh

Figure 4-450. END Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END															
R/W															
0h															

Access Types Legend

Table 4-953. END Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END	R/W	0h	Memory end address Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.141 ICACHE_CORE1_START Registers

4.6.141.1 ICACHE_START Register (Offset = 0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 4-954. Instance Table

Instance Name	Physical Address
R5SS_CORE0	7500 0000h
R5SS_CORE1	7700 0000h

Figure 4-451. START Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START															
R/W															
0h															

Access Types Legend

Table 4-955. START Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START	R/W	0h	Memory start address Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.142 ICACHE_CORE1_END Registers

4.6.142.1 ICACHE_END Register (Offset = 7FFFFCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 4-956. Instance Table

Instance Name	Physical Address
R5SS_CORE0	757F FFFCh
R5SS_CORE1	777F FFFCh

Figure 4-452. END Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END															
R/W															
0h															

Access Types Legend

Table 4-957. END Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END	R/W	0h	Memory end address Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.143 DCACHE_CORE1_START Registers

4.6.143.1 DCACHE_START Register (Offset = 0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 4-958. Instance Table

Instance Name	Physical Address
R5SS_CORE0	7580 0000h
R5SS_CORE1	7780 0000h

Figure 4-453. START Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START															
R/W															
0h															

Access Types Legend

Table 4-959. START Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START	R/W	0h	Memory start address Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.144 DCACHE_CORE1_END Registers

4.6.144.1 DCACHE_END Register (Offset = 7FFFFCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 4-960. Instance Table

Instance Name	Physical Address
R5SS_CORE0	75FF FFFCh
R5SS_CORE1	77FF FFFCh

Figure 4-454. END Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END															
R/W															
0h															

Access Types Legend

Table 4-961. END Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END	R/W	0h	Memory end address Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.145 TCMA_CR5A_START Registers

4.6.145.1 TCMA_START Register (Offset = 0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 4-962. Instance Table

Instance Name	Physical Address
R5SS_CORE0	7800 0000h
R5SS_CORE1	7840 0000h

Figure 4-455. START Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START															
R/W															
0h															

Access Types Legend

Table 4-963. START Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START	R/W	0h	TCMA start address Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.146 TCMA_CR5A_END Registers

4.6.146.1 TCMA_END Register (Offset = 27FFCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 4-964. Instance Table

Instance Name	Physical Address
R5SS_CORE0	7802 7FFCh
R5SS_CORE1	7842 7FFCh

Figure 4-456. END Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END															
R/W															
0h															

Access Types Legend

Table 4-965. END Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END	R/W	0h	TCMA end address Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.147 TCMB_CR5A_START Registers

4.6.147.1 TCMB_START Register (Offset = 0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 4-966. Instance Table

Instance Name	Physical Address
R5SS_CORE0	7810 0000h
R5SS_CORE1	7850 0000h

Figure 4-457. START Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START															
R/W															
0h															

Access Types Legend

Table 4-967. START Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START	R/W	0h	TCMB start address Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.148 TCMB_CR5A_END Registers

4.6.148.1 TCMB_END Register (Offset = 2FFFCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 4-968. Instance Table

Instance Name	Physical Address
R5SS_CORE0	7812 FFFCh
R5SS_CORE1	7852 FFFCh

Figure 4-458. END Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END															
R/W															
0h															

Access Types Legend

Table 4-969. END Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END	R/W	0h	TCMB end address Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.149 TCMA_CR5B_START Registers

4.6.149.1 TCMA_START Register (Offset = 0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 4-970. Instance Table

Instance Name	Physical Address
R5SS_CORE0	7820 0000h
R5SS_CORE1	7860 0000h

Figure 4-459. START Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START															
R/W															
0h															

Access Types Legend

Table 4-971. START Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START	R/W	0h	TCMA start address Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.150 TCMA_CR5B_END Registers

4.6.150.1 TCMA_END Register (Offset = 7FFCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 4-972. Instance Table

Instance Name	Physical Address
R5SS_CORE0	7820 7FFCh
R5SS_CORE1	7860 7FFCh

Figure 4-460. END Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END															
R/W															
0h															

Access Types Legend

Table 4-973. END Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END	R/W	0h	TCMA end address Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.151 TCMB_CR5B_START Registers

4.6.151.1 TCMB_START Register (Offset = 0h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 4-974. Instance Table

Instance Name	Physical Address
R5SS_CORE0	7830 0000h
R5SS_CORE1	7870 0000h

Figure 4-461. START Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START															
R/W															
0h															

Access Types Legend

Table 4-975. START Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START	R/W	0h	TCMB start address Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.152 TCMB_CR5B_END Registers

4.6.152.1 TCMB_END Register (Offset = 17FFCh) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 4-976. Instance Table

Instance Name	Physical Address
R5SS_CORE0	7831 7FFCh
R5SS_CORE1	7871 7FFCh

Figure 4-462. END Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END															
R/W															
0h															

Access Types Legend

Table 4-977. END Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END	R/W	0h	TCMB end address Reset Source: r5ss_core_rst_mod_g_rst_n

4.6.153 Access Table

Table 4-978. Access Type Codes

Access Type	Code	Description
R	R	Read
R/W	R/W	Read / Write
R/W1TS	R/W1TS	Read/Write 1 To Set
R/W1TC	R/W1TC	Read/Write 1 To Clear
R/WD	R/WD	Read/Write Decrement. A write to this bit field decrements the specified register bit field by the amount written.
R/WI	R/WI	Read/Write Increment. A write to this bit field increments the specified register bit field by the amount written.

4.7 PBIST Registers

Table 4-979. MEM, MEM Registers, Base Address=0X0000000053300200, Length=512

Offset	Length	Register Name	pbist0 Physical Address
100h	32	PBIST_A0	5330 0300h
104h	32	PBIST_A1	5330 0304h
108h	32	PBIST_A2	5330 0308h
10Ch	32	PBIST_A3	5330 030Ch
110h	32	PBIST_L0	5330 0310h
114h	32	PBIST_L1	5330 0314h
118h	32	PBIST_L2	5330 0318h
11Ch	32	PBIST_L3	5330 031Ch
120h	32	PBIST_DD10	5330 0320h
124h	32	PBIST_DE10	5330 0324h
130h	32	PBIST_CA0	5330 0330h
134h	32	PBIST_CA1	5330 0334h
138h	32	PBIST_CA2	5330 0338h
13Ch	32	PBIST_CA3	5330 033Ch
140h	32	PBIST_CL0	5330 0340h
144h	32	PBIST_CL1	5330 0344h
148h	32	PBIST_CL2	5330 0348h
14Ch	32	PBIST_CL3	5330 034Ch
150h	32	PBIST_CI0	5330 0350h
154h	32	PBIST_CI1	5330 0354h
158h	16	PBIST_CI2	5330 0358h
15Ch	16	PBIST_CI3	5330 035Ch
160h	32	PBIST_RAMT	5330 0360h
164h	16	PBIST_DLR	5330 0364h
168h	8	PBIST_CMS	5330 0368h
16Ch	8	PBIST_PC	5330 036Ch
170h	32	PBIST_SCR1	5330 0370h
174h	32	PBIST_SCR4	5330 0374h
178h	32	PBIST_CS	5330 0378h
17Ch	8	PBIST_FDLY	5330 037Ch
180h	8	PBIST_PACT	5330 0380h
184h	8	PBIST_ID	5330 0384h
188h	32	PBIST_OVR	5330 0388h
190h	8	PBIST_FSFR0	5330 0390h
194h	8	PBIST_FSFR1	5330 0394h
198h	8	PBIST_FSRCR0	5330 0398h
19Ch	8	PBIST_FSRCR1	5330 039Ch
1A0h	32	PBIST_FSRA0	5330 03A0h
1A4h	16	PBIST_FSRA1	5330 03A4h
1A8h	32	PBIST_FSRDL0	5330 03A8h
1B0h	32	PBIST_FSRDL1	5330 03B0h
1B4h	32	PBIST_MARGIN	5330 03B4h
1B8h	32	PBIST_WRENZ	5330 03B8h
1BCh	32	PBIST_PGS	5330 03BCh
1C0h	8	PBIST_ROM	5330 03C0h

Table 4-979. MEM, MEM Registers, Base Address=0X0000000053300200, Length=512 (continued)

Offset	Length	Register Name	pbist0 Physical Address
1C4h	32	PBIST_ALGO	5330 03C4h
1C8h	32	PBIST_RINFOL	5330 03C8h
1CCh	32	PBIST_RINFOU	5330 03CCh

4.7.1 MEM_PBIST_A0 Registers

4.7.1.1 MEM_A0 Register (Offset = 100h) [reset = 0h]

Short Description: Variable Address Register

Long Description: Variable Address Register0

Return to Summary Table

Table 4-980. Instance Table

Instance Name	Physical Address
PBIST0	5330 0300h

Figure 4-463. PBIST_A0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
NONE															
0															

Access Types Legend

Table 4-981. PBIST_A0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE		Reserved

4.7.2 MEM_PBIST_A1 Registers

4.7.2.1 MEM_A1 Register (Offset = 104h) [reset = 0h]

Short Description: Variable Address Register

Long Description: Variable Address Register1

Return to Summary Table

Table 4-982. Instance Table

Instance Name	Physical Address
PBIST0	5330 0304h

Figure 4-464. PBIST_A1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
NONE															
0															

Access Types Legend

Table 4-983. PBIST_A1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE		Reserved

4.7.3 MEM_PBIST_A2 Registers

4.7.3.1 MEM_A2 Register (Offset = 108h) [reset = 0h]

Short Description: Variable Address Register

Long Description: Variable Address Register2

Return to Summary Table

Table 4-984. Instance Table

Instance Name	Physical Address
PBIST0	5330 0308h

Figure 4-465. PBIST_A2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
NONE															
0															

Access Types Legend

Table 4-985. PBIST_A2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE		Reserved

4.7.4 MEM_PBIST_A3 Registers

4.7.4.1 MEM_A3 Register (Offset = 10Ch) [reset = 0h]

Short Description: Variable Address Register

Long Description: Variable Address Register3

Return to Summary Table

Table 4-986. Instance Table

Instance Name	Physical Address
PBIST0	5330 030Ch

Figure 4-466. PBIST_A3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
NONE															
0															

Access Types Legend

Table 4-987. PBIST_A3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE		Reserved

4.7.5 MEM_PBIST_L0 Registers

4.7.5.1 MEM_L0 Register (Offset = 110h) [reset = 0h]

Short Description: Variable Loop Count Regis

Long Description: Variable Loop Count Register L0

Return to Summary Table

Table 4-988. Instance Table

Instance Name	Physical Address
PBIST0	5330 0310h

Figure 4-467. PBIST_L0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
NONE															
0															

Access Types Legend

Table 4-989. PBIST_L0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE		Reserved

4.7.6 MEM_PBIST_L1 Registers

4.7.6.1 MEM_L1 Register (Offset = 114h) [reset = 0h]

Short Description: Variable Loop Count Regis

Long Description: Variable Loop Count Register L1

Return to Summary Table

Table 4-990. Instance Table

Instance Name	Physical Address
PBIST0	5330 0314h

Figure 4-468. PBIST_L1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
NONE															
0															

Access Types Legend

Table 4-991. PBIST_L1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE		Reserved

4.7.7 MEM_PBIST_L2 Registers

4.7.7.1 MEM_L2 Register (Offset = 118h) [reset = 0h]

Short Description: Variable Loop Count Regis

Long Description: Variable Loop Count Register L2

Return to Summary Table

Table 4-992. Instance Table

Instance Name	Physical Address
PBIST0	5330 0318h

Figure 4-469. PBIST_L2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
NONE															
0															

Access Types Legend

Table 4-993. PBIST_L2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE		Reserved

4.7.8 MEM_PBIST_L3 Registers

4.7.8.1 MEM_L3 Register (Offset = 11Ch) [reset = 0h]

Short Description: Variable Loop Count Regis

Long Description: Variable Loop Count Register L3

Return to Summary Table

Table 4-994. Instance Table

Instance Name	Physical Address
PBIST0	5330 031Ch

Figure 4-470. PBIST_L3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
NONE															
0															

Access Types Legend

Table 4-995. PBIST_L3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE		Reserved

4.7.9 MEM_PBIST_DD10 Registers

4.7.9.1 MEM_DD10 Register (Offset = 120h) [reset = 0h]

Short Description: DD0 Data Register 16 (D0

Long Description: DD0 Data Register 16 (D0)

Return to Summary Table

Table 4-996. Instance Table

Instance Name	Physical Address
PBIST0	5330 0320h

Figure 4-471. PBIST_DD10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
NONE															
0															

Access Types Legend

Table 4-997. PBIST_DD10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE		Reserved

4.7.10 MEM_PBIST_DE10 Registers

4.7.10.1 MEM_DE10 Register (Offset = 124h) [reset = 0h]

Short Description: DE0 Data Register 16 (D0

Long Description: DE0 Data Register 16 (D0)

Return to Summary Table

Table 4-998. Instance Table

Instance Name	Physical Address
PBIST0	5330 0324h

Figure 4-472. PBIST_DE10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
NONE															
0															

Access Types Legend

Table 4-999. PBIST_DE10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE		Reserved

4.7.11 MEM_PBIST_CA0 Registers

4.7.11.1 MEM_CA0 Register (Offset = 130h) [reset = 0h]

Short Description: Constant Address Register

Long Description: Constant Address Register0

Return to Summary Table

Table 4-1000. Instance Table

Instance Name	Physical Address
PBIST0	5330 0330h

Figure 4-473. PBIST_CA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
NONE															
0															

Access Types Legend

Table 4-1001. PBIST_CA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE		Reserved

4.7.12 MEM_PBIST_CA1 Registers

4.7.12.1 MEM_CA1 Register (Offset = 134h) [reset = 0h]

Short Description: Constant Address Register

Long Description: Constant Address Register1

Return to Summary Table

Table 4-1002. Instance Table

Instance Name	Physical Address
PBIST0	5330 0334h

Figure 4-474. PBIST_CA1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
NONE															
0															

Access Types Legend

Table 4-1003. PBIST_CA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE		Reserved

4.7.13 MEM_PBIST_CA2 Registers

4.7.13.1 MEM_CA2 Register (Offset = 138h) [reset = 0h]

Short Description: Constant Address Register

Long Description: Constant Address Register2

Return to Summary Table

Table 4-1004. Instance Table

Instance Name	Physical Address
PBIST0	5330 0338h

Figure 4-475. PBIST_CA2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
NONE															
0															

Access Types Legend

Table 4-1005. PBIST_CA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE		Reserved

4.7.14 MEM_PBIST_CA3 Registers

4.7.14.1 MEM_CA3 Register (Offset = 13Ch) [reset = 0h]

Short Description: Constant Address Register

Long Description: Constant Address Register3

Return to Summary Table

Table 4-1006. Instance Table

Instance Name	Physical Address
PBIST0	5330 033Ch

Figure 4-476. PBIST_CA3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
NONE															
0															

Access Types Legend

Table 4-1007. PBIST_CA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE		Reserved

4.7.15 MEM_PBIST_CL0 Registers

4.7.15.1 MEM_CL0 Register (Offset = 140h) [reset = 0h]

Short Description: Constant Loop Count Regis

Long Description: Constant Loop Count Register0

Return to Summary Table

Table 4-1008. Instance Table

Instance Name	Physical Address
PBIST0	5330 0340h

Figure 4-477. PBIST_CL0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
NONE															
0															

Access Types Legend

Table 4-1009. PBIST_CL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE		Reserved

4.7.16 MEM_PBIST_CL1 Registers

4.7.16.1 MEM_CL1 Register (Offset = 144h) [reset = 0h]

Short Description: Constant Loop Count Regis

Long Description: Constant Loop Count Register1

Return to Summary Table

Table 4-1010. Instance Table

Instance Name	Physical Address
PBIST0	5330 0344h

Figure 4-478. PBIST_CL1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
NONE															
0															

Access Types Legend

Table 4-1011. PBIST_CL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE		Reserved

4.7.17 MEM_PBIST_CL2 Registers

4.7.17.1 MEM_CL2 Register (Offset = 148h) [reset = 0h]

Short Description: Constant Loop Count Regis

Long Description: Constant Loop Count Register2

Return to Summary Table

Table 4-1012. Instance Table

Instance Name	Physical Address
PBIST0	5330 0348h

Figure 4-479. PBIST_CL2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
NONE															
0															

Access Types Legend

Table 4-1013. PBIST_CL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE		Reserved

4.7.18 MEM_PBIST_CL3 Registers

4.7.18.1 MEM_CL3 Register (Offset = 14Ch) [reset = 0h]

Short Description: Constant Loop Count Regis

Long Description: Constant Loop Count Register3

Return to Summary Table

Table 4-1014. Instance Table

Instance Name	Physical Address
PBIST0	5330 034Ch

Figure 4-480. PBIST_CL3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
NONE															
0															

Access Types Legend

Table 4-1015. PBIST_CL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE		Reserved

4.7.19 MEM_PBIST_CI0 Registers

4.7.19.1 MEM_CI0 Register (Offset = 150h) [reset = 0h]

Short Description: Constant Increment Regist

Long Description: Constant Increment Register0

Return to Summary Table

Table 4-1016. Instance Table

Instance Name	Physical Address
PBIST0	5330 0350h

Figure 4-481. PBIST_CI0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
NONE															
0															

Access Types Legend

Table 4-1017. PBIST_CI0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE		Reserved

4.7.20 MEM_PBIST_CI1 Registers

4.7.20.1 MEM_CI1 Register (Offset = 154h) [reset = 0h]

Short Description: Constant Increment Regist

Long Description: Constant Increment Register1

Return to Summary Table

Table 4-1018. Instance Table

Instance Name	Physical Address
PBIST0	5330 0354h

Figure 4-482. PBIST_CI1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
NONE															
0															

Access Types Legend

Table 4-1019. PBIST_CI1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE		Reserved

4.7.21 MEM_PBIST_CI2 Registers

4.7.21.1 MEM_CI2 Register (Offset = 158h) [reset = 0h]

Short Description: Constant Increment Regist

Long Description: Constant Increment Register2

Return to Summary Table

Table 4-1020. Instance Table

Instance Name	Physical Address
PBIST0	5330 0358h

Figure 4-483. PBIST_CI2 Name Register

15	14	13	12	11	10	9	8
PBIST_CI2							
R/W							
0h							
7	6	5	4	3	2	1	0
PBIST_CI2							
R/W							
0h							

Access Types Legend

Table 4-1021. PBIST_CI2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	PBIST_CI2	R/W	0h	TI Internal Register.Reserved for HW RnD

4.7.22 MEM_PBIST_CI3 Registers

4.7.22.1 MEM_CI3 Register (Offset = 15Ch) [reset = 0h]

Short Description: Constant Increment Regist

Long Description: Constant Increment Register3

Return to Summary Table

Table 4-1022. Instance Table

Instance Name	Physical Address
PBIST0	5330 035Ch

Figure 4-484. PBIST_CI3 Name Register

15	14	13	12	11	10	9	8
PBIST_CI3							
R/W							
0h							
7	6	5	4	3	2	1	0
PBIST_CI3							
R/W							
0h							

Access Types Legend

Table 4-1023. PBIST_CI3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	PBIST_CI3	R/W	0h	TI Internal Register.Reserved for HW RnD

4.7.23 MEM_PBIST_RAMT Registers

4.7.23.1 MEM_RAMT Register (Offset = 160h) [reset = 0h]

Short Description: RAM Configuration (RAMT -

Long Description: RAM Configuration (RAMT -RAM)

Return to Summary Table

Table 4-1024. Instance Table

Instance Name	Physical Address
PBIST0	5330 0360h

Figure 4-485. PBIST_RAMT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RGS								RDS							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DWR								RAM							
R/W								R/W							
0h								0h							

Access Types Legend

Table 4-1025. PBIST_RAMT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RGS	R/W	0h	TI Internal Register.Reserved for HW RnD These registers do not have a default value after reset.
23:16	RDS	R/W	0h	TI Internal Register.Reserved for HW RnD These registers do not have a default value after reset.
15:8	DWR	R/W	0h	TI Internal Register.Reserved for HW RnD These registers do not have a default value after reset.
7:0	RAM	R/W	0h	TI Internal Register.Reserved for HW RnD These registers do not have a default value after reset.

4.7.24 MEM_PBIST_DLR Registers

4.7.24.1 MEM_DLR Register (Offset = 164h) [reset = 208h]

Short Description: Datalogger 0

Long Description: Datalogger 0

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Table 4-1026. Instance Table

Instance Name	Physical Address
PBIST0	5330 0364h

Figure 4-486. PBIST_DLR Name Register

15	14	13	12	11	10	9	8
DLR1							
R/W							
2h							
7	6	5	4	3	2	1	0
DLR0							
R/W							
8h							

Access Types Legend

Table 4-1027. PBIST_DLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	DLR1	R/W	2h	Datalogger Register [8] : Reserevd [9] : Default Testing Mode. When in this mode, ROM-based testing is kicked off. If the intention is to perform go/no-go testing via config, write to both this bit and bit [2] of the Datalogger Register simultaneously [15:10] : Reserevd
7:0	DLR0	R/W	8h	Datalogger Register [1:0] : Reserved [2] : ROM-based testing mode. Setting this bit to 1 enables the PBIST controller to execute test algorithms that are stored in the PBIST ROM [3] : Do not change this bit from its default value of 1 [4] : Config access mode. Setting this bit allows the host processor to configure the PBIST controller registers [7:5] : Reserved

4.7.25 MEM_PBIST_CMS Registers

4.7.25.1 MEM_CMS Register (Offset = 168h) [reset = 0h]

Short Description: Clock mux select

Long Description: Clock mux select

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Table 4-1028. Instance Table

Instance Name	Physical Address
PBIST0	5330 0368h

Figure 4-487. PBIST_CMS Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				PBIST_CMS			
NONE				R/W			
0				0h			

Access Types Legend

Table 4-1029. PBIST_CMS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	NONE		Reserved
3:0	PBIST_CMS	R/W	0h	TI Internal Register.Reserved for HW RnD These registers do not have a default value after reset.

4.7.26 MEM_PBIST_PC Registers

4.7.26.1 MEM_PC Register (Offset = 16Ch) [reset = 0h]

Short Description: Program Control

Long Description: Program Control

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Table 4-1030. Instance Table

Instance Name	Physical Address
PBIST0	5330 036Ch

Figure 4-488. PBIST_PC Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			PBIST_PC				
NONE			R/W				
0			0h				

Access Types Legend

Table 4-1031. PBIST_PC Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	NONE		Reserved
4:0	PBIST_PC	R/W	0h	TI Internal Register.Reserved for HW RnD

4.7.27 MEM_PBIST_SCR1 Registers

4.7.27.1 MEM_SCR1 Register (Offset = 170h) [reset = 76543210h]

Short Description: Address Scramble 0 -3

Long Description: Address Scramble 0 -3

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Table 4-1032. Instance Table

Instance Name	Physical Address
PBIST0	5330 0370h

Figure 4-489. PBIST_SCR1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCR3								SCR2							
R/W								R/W							
76h								54h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCR1								SCR0							
R/W								R/W							
32h								10h							

Access Types Legend

Table 4-1033. PBIST_SCR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SCR3	R/W	76h	TI Internal Register.Reserved for HW RnD
23:16	SCR2	R/W	54h	TI Internal Register.Reserved for HW RnD
15:8	SCR1	R/W	32h	TI Internal Register.Reserved for HW RnD
7:0	SCR0	R/W	10h	TI Internal Register.Reserved for HW RnD

4.7.28 MEM_PBIST_SCR4 Registers

4.7.28.1 MEM_SCR4 Register (Offset = 174h) [reset = fedcba98h]

Short Description: Address Scramble 4-7

Long Description: Address Scramble 4-7

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Table 4-1034. Instance Table

Instance Name	Physical Address
PBIST0	5330 0374h

Figure 4-490. PBIST_SCR4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCR7								SCR6							
R/W								R/W							
feh								dch							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCR5								SCR4							
R/W								R/W							
bah								98h							

Access Types Legend

Table 4-1035. PBIST_SCR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SCR7	R/W	FEh	TI Internal Register.Reserved for HW RnD
23:16	SCR6	R/W	DCh	TI Internal Register.Reserved for HW RnD
15:8	SCR5	R/W	BAh	TI Internal Register.Reserved for HW RnD
7:0	SCR4	R/W	98h	TI Internal Register.Reserved for HW RnD

4.7.29 MEM_PBIST_CS Registers

4.7.29.1 MEM_CS Register (Offset = 178h) [reset = 0h]

Short Description: Chip Select 0

Long Description: Chip Select 0

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Table 4-1036. Instance Table

Instance Name	Physical Address
PBIST0	5330 0378h

Figure 4-491. PBIST_CS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CS3								CS2							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CS1								CS0							
R/W								R/W							
0h								0h							

Access Types Legend

Table 4-1037. PBIST_CS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	CS3	R/W	0h	TI Internal Register.Reserved for HW RnD
23:16	CS2	R/W	0h	TI Internal Register.Reserved for HW RnD
15:8	CS1	R/W	0h	TI Internal Register.Reserved for HW RnD
7:0	CS0	R/W	0h	TI Internal Register.Reserved for HW RnD

4.7.30 MEM_PBIST_FDLY Registers

4.7.30.1 MEM_FDLY Register (Offset = 17Ch) [reset = 48h]

Short Description: Fail Delay

Long Description: Fail Delay

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Table 4-1038. Instance Table

Instance Name	Physical Address
PBIST0	5330 037Ch

Figure 4-492. PBIST_FDLY Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
PBIST_FDLY							
R/W							
48h							

Access Types Legend

Table 4-1039. PBIST_FDLY Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PBIST_FDLY	R/W	48h	TI Internal Register.Reserved for HW RnD

4.7.31 MEM_PBIST_PACT Registers

4.7.31.1 MEM_PACT Register (Offset = 180h) [reset = 0h]

Short Description: Pbist Active

Long Description: Pbist Active

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Table 4-1040. Instance Table

Instance Name	Physical Address
PBIST0	5330 0380h

Figure 4-493. PBIST_PACT Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED							PBIST_PACT
NONE							R/W
0							0h

Access Types Legend

Table 4-1041. PBIST_PACT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	NONE		Reserved
0	PBIST_PACT	R/W	0h	Pbist Active/ROM Clock Enable Register [0]: This bit must be set to turn on internal PBIST clocks. Setting this bit asserts an internal signal that is used as the clock gate enable. As long as this bit is 0, any access to PBIST will not go through, and PBIST will remain in an almost zero-power mode. Value 0 = Disable internal PBIST clocks Value 1 = Enable internal PBIST clocks

4.7.32 MEM_PBIST_ID Registers

4.7.32.1 MEM_ID Register (Offset = 184h) [reset = 1h]

Short Description: PBIST ID

Long Description: PBIST ID

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Table 4-1042. Instance Table

Instance Name	Physical Address
PBIST0	5330 0384h

Figure 4-494. PBIST_ID Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			PBIST_ID				
NONE			R/W				
0			1h				

Access Types Legend

Table 4-1043. PBIST_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	NONE		Reserved
4:0	PBIST_ID	R/W	1h	PBIST ID. This is a unique ID assigned to each PBIST controller in a device with multiple PBIST controllers. The value of this register does not affect the functionality of the CPU interface.

4.7.33 MEM_PBIST_OVR Registers

4.7.33.1 MEM_OVR Register (Offset = 188h) [reset = 0h]

Short Description: PBIST Overrides

Long Description: PBIST Overrides

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Table 4-1044. Instance Table

Instance Name	Physical Address
PBIST0	5330 0388h

Figure 4-495. PBIST_OVR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
NONE															
0															

Access Types Legend

Table 4-1045. PBIST_OVR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE		Reserved

4.7.34 MEM_PBIST_FSFR0 Registers

4.7.34.1 MEM_FSFR0 Register (Offset = 190h) [reset = 0h]

Short Description: Fail status fail - port 0

Long Description: Fail status fail - port 0

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Table 4-1046. Instance Table

Instance Name	Physical Address
PBIST0	5330 0390h

Figure 4-496. PBIST_FSFR0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED							PBIST_FSFR0
NONE							R
0							0h

Access Types Legend

Table 4-1047. PBIST_FSFR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	NONE		Reserved
0	PBIST_FSFR0	R	0h	Fail Status Fail Register- Port 0 This register indicates if a failure occurred during a memory self-test. Value 0 = No failure occurred Value 1 = Indicates a failure

4.7.35 MEM_PBIST_FSFR1 Registers

4.7.35.1 MEM_FSFR1 Register (Offset = 194h) [reset = 0h]

Short Description: Fail status fail - port 1

Long Description: Fail status fail - port 1

Return to Summary Table

Table 4-1048. Instance Table

Instance Name	Physical Address
PBIST0	5330 0394h

Figure 4-497. PBIST_FSFR1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED							PBIST_FSFR1
NONE							R
0							0h

Access Types Legend

Table 4-1049. PBIST_FSFR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	NONE		Reserved
0	PBIST_FSFR1	R	0h	Fail Status Fail Register- Port 1 This register indicates if a failure occurred during a memory self-test. Value 0 = No failure occurred Value 1 = Indicates a failure

4.7.36 MEM_PBIST_FSRCR0 Registers

4.7.36.1 MEM_FSRCR0 Register (Offset = 198h) [reset = 0h]

Short Description: Fail Count fail - port 0

Long Description: Fail Count fail - port 0

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Table 4-1050. Instance Table

Instance Name	Physical Address
PBIST0	5330 0398h

Figure 4-498. PBIST_FSRCR0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				PBIST_FSRCR0			
NONE				R			
0				0h			

Access Types Legend

Table 4-1051. PBIST_FSRCR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	NONE		Reserved
3:0	PBIST_FSRCR0	R	0h	Fail Status Count - Port 0 These registers keep count of the number of failures observed during the memory self-test. The PBIST controller stops executing the memory self-test whenever a failure occurs in any memory instance for any of the test algorithms. The value in gets incremented by one whenever a failure occurs

4.7.37 MEM_PBIST_FSRCR1 Registers

4.7.37.1 MEM_FSRCR1 Register (Offset = 19Ch) [reset = 0h]

Short Description: Fail Count fail - port 1

Long Description: Fail Count fail - port 1

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Table 4-1052. Instance Table

Instance Name	Physical Address
PBIST0	5330 039Ch

Figure 4-499. PBIST_FSRCR1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				PBIST_FSRCR1			
NONE				R			
0				0h			

Access Types Legend

Table 4-1053. PBIST_FSRCR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	NONE		Reserved
3:0	PBIST_FSRCR1	R	0h	Fail Status Count - Port 1 These registers keep count of the number of failures observed during the memory self-test. The PBIST controller stops executing the memory self-test whenever a failure occurs in any memory instance for any of the test algorithms. The value in gets incremented by one whenever a failure occurs

4.7.38 MEM_PBIST_FSRA0 Registers

4.7.38.1 MEM_FSRA0 Register (Offset = 1A0h) [reset = 0h]

Short Description: Fail status address - por

Long Description: Fail status address - port 0

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Table 4-1054. Instance Table

Instance Name	Physical Address
PBIST0	5330 03A0h

Figure 4-500. PBIST_FSRA0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
NONE															
0															

Access Types Legend

Table 4-1055. PBIST_FSRA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE		Reserved

4.7.39 MEM_PBIST_FSRA1 Registers

4.7.39.1 MEM_FSRA1 Register (Offset = 1A4h) [reset = 0h]

Short Description: Fail status address - por

Long Description: Fail status address - port 1

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Table 4-1056. Instance Table

Instance Name	Physical Address
PBIST0	5330 03A4h

Figure 4-501. PBIST_FSRA1 Name Register

15	14	13	12	11	10	9	8
PBIST_FSRA1							
R							
0h							
7	6	5	4	3	2	1	0
PBIST_FSRA1							
R							
0h							

Access Types Legend

Table 4-1057. PBIST_FSRA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	PBIST_FSRA1	R	0h	TI Internal Register.Reserved for HW RnD

4.7.40 MEM_PBIST_FSRDL0 Registers

4.7.40.1 MEM_FSRDL0 Register (Offset = 1A8h) [reset = aaaaaaaah]

Short Description: Fail status Data - port 0

Long Description: Fail status Data - port 0

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Table 4-1058. Instance Table

Instance Name	Physical Address
PBIST0	5330 03A8h

Figure 4-502. PBIST_FSRDL0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PBIST_FSRDL0															
R															
aaaaaaaah															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PBIST_FSRDL0															
R															
aaaaaaaah															

Access Types Legend

Table 4-1059. PBIST_FSRDL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PBIST_FSRDL0	R	AAAAAAAAh	TI Internal Register.Reserved for HW RnD

4.7.41 MEM_PBIST_FSRDL1 Registers

4.7.41.1 MEM_FSRDL1 Register (Offset = 1B0h) [reset = aaaaaaaah]

Short Description: Fail status Data - port 1

Long Description: Fail status Data - port 1

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Table 4-1060. Instance Table

Instance Name	Physical Address
PBIST0	5330 03B0h

Figure 4-503. PBIST_FSRDL1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PBIST_FSRDL1															
R															
aaaaaaaah															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PBIST_FSRDL1															
R															
aaaaaaaah															

Access Types Legend

Table 4-1061. PBIST_FSRDL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PBIST_FSRDL1	R	AAAAAAAAh	TI Internal Register.Reserved for HW RnD

4.7.42 MEM_PBIST_MARGIN Registers

4.7.42.1 MEM_MARGIN Register (Offset = 1B4h) [reset = 0h]

Short Description: Margin Mode

Long Description: Margin Mode

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Table 4-1062. Instance Table

Instance Name	Physical Address
PBIST0	5330 03B4h

Figure 4-504. PBIST_MARGIN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
NONE															
0															

Access Types Legend

Table 4-1063. PBIST_MARGIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE		Reserved

4.7.43 MEM_PBIST_WRENZ Registers

4.7.43.1 MEM_WRENZ Register (Offset = 1B8h) [reset = 0h]

Short Description: WRENZ

Long Description: WRENZ

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Table 4-1064. Instance Table

Instance Name	Physical Address
PBIST0	5330 03B8h

Figure 4-505. PBIST_WRENZ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
NONE															
0															

Access Types Legend

Table 4-1065. PBIST_WRENZ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE		Reserved

4.7.44 MEM_PBIST_PGS Registers

4.7.44.1 MEM_PGS Register (Offset = 1BCh) [reset = 0h]

Short Description: PAGE/PGS

Long Description: PAGE/PGS

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Table 4-1066. Instance Table

Instance Name	Physical Address
PBIST0	5330 03BCh

Figure 4-506. PBIST_PGS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
NONE															
0															

Access Types Legend

Table 4-1067. PBIST_PGS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE		Reserved

4.7.45 MEM_PBIST_ROM Registers

4.7.45.1 MEM_ROM Register (Offset = 1C0h) [reset = 3h]

Short Description: Rom Mask

Long Description: Rom Mask

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Table 4-1068. Instance Table

Instance Name	Physical Address
PBIST0	5330 03C0h

Figure 4-507. PBIST_ROM Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						PBIST_ROM	
NONE						R/W	
1						3h	

Access Types Legend

Table 4-1069. PBIST_ROM Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	NONE		Reserved
1:0	PBIST_ROM	R/W	3h	Rom Mask . This two-bit register sets appropriate ROM access modes for the PBIST controller. Value 0h = No information is used from ROM Value 1h = Only RAM Group information from ROM Vaule 2h = Only Algorithm information from ROM Value 3h = Both Algorithm and RAM information from ROM. This option should be selected for application self-test.

4.7.46 MEM_PBIST_ALGO Registers

4.7.46.1 MEM_ALGO Register (Offset = 1C4h) [reset = ffffffffh]

Short Description: ROM Algorithm Mask 0

Long Description: ROM Algorithm Mask 0

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Table 4-1070. Instance Table

Instance Name	Physical Address
PBIST0	5330 03C4h

Figure 4-508. PBIST_ALGO Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ALGO3								ALGO2							
R/W								R/W							
ffh								ffh							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALGO1								ALGO0							
R/W								R/W							
ffh								ffh							

Access Types Legend

Table 4-1071. PBIST_ALGO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	ALGO3	R/W	FFh	This register is used to indicate the algorithm[s] to be used for the memory self-test routine. Each bit corresponds to a specific algorithm. Writing a value 1 to the particular bit, enables the corresponding algorithm. Writing a value 0 to the particular bit, disables the corresponding algorithm.
23:16	ALGO2	R/W	FFh	This register is used to indicate the algorithm[s] to be used for the memory self-test routine. Each bit corresponds to a specific algorithm. Writing a value 1 to the particular bit, enables the corresponding algorithm. Writing a value 0 to the particular bit, disables the corresponding algorithm.
15:8	ALGO1	R/W	FFh	This register is used to indicate the algorithm[s] to be used for the memory self-test routine. Each bit corresponds to a specific algorithm. Writing a value 1 to the particular bit, enables the corresponding algorithm. Writing a value 0 to the particular bit, disables the corresponding algorithm.
7:0	ALGO0	R/W	FFh	This register is used to indicate the algorithm[s] to be used for the memory self-test routine. Each bit corresponds to a specific algorithm. Writing a value 1 to the particular bit, enables the corresponding algorithm. Writing a value 0 to the particular bit, disables the corresponding algorithm.

4.7.47 MEM_PBIST_RINFOL Registers

4.7.47.1 MEM_RINFOL Register (Offset = 1C8h) [reset = ffffffffh]

Short Description: RAM Info Mask Lower 0

Long Description: RAM Info Mask Lower 0

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Table 4-1072. Instance Table

Instance Name	Physical Address
PBIST0	5330 03C8h

Figure 4-509. PBIST_RINFOL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RINFOL3								RINFOL2							
R/W								R/W							
ffh								ffh							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RINFOL1								RINFOL0							
R/W								R/W							
ffh								ffh							

Access Types Legend

Table 4-1073. PBIST_RINFOL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RINFOL3	R/W	FFh	This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithmto be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group.
23:16	RINFOL2	R/W	FFh	This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithmto be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group.
15:8	RINFOL1	R/W	FFh	This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithmto be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group.
7:0	RINFOL0	R/W	FFh	This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithmto be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group.

4.7.48 MEM_PBIST_RINFOU Registers

4.7.48.1 MEM_RINFOU Register (Offset = 1CCh) [reset = ffffffffh]

Short Description: RAM Info Mask Upper 0

Long Description: RAM Info Mask Upper 0

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Table 4-1074. Instance Table

Instance Name	Physical Address
PBIST0	5330 03CCh

Figure 4-510. PBIST_RINFOU Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RINFOU3								RINFOU2							
R/W								R/W							
ffh								ffh							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RINFOU1								RINFOU0							
R/W								R/W							
ffh								ffh							

Access Types Legend

Table 4-1075. PBIST_RINFOU Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RINFOU3	R/W	FFh	This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithmto be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group.
23:16	RINFOU2	R/W	FFh	This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithmto be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group.
15:8	RINFOU1	R/W	FFh	This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithmto be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group.
7:0	RINFOU0	R/W	FFh	This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithmto be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group.

4.7.49 Access Table

Table 4-1076. Access Type Codes

Access Type	Code	Description
R/W	R/W	Read / Write
R	R	Read

4.8 DCC Registers

Table 4-1077. Registers, Base Address=0X0000000052B00000, Length=64

Offset	Length	Register Name	DCC0 Physical Address	DCC1 Physical Address	DCC2 Physical Address
0h	32	DCC_DCCGCTRL	52B0 0000h	52B0 1000h	52B0 2000h
4h	32	DCC_DCCREV	52B0 0004h	52B0 1004h	52B0 2004h
8h	32	DCC_DCCCNTSEED0	52B0 0008h	52B0 1008h	52B0 2008h
Ch	32	DCC_DCCVALIDSEED0	52B0 000Ch	52B0 100Ch	52B0 200Ch
10h	32	DCC_DCCCNTSEED1	52B0 0010h	52B0 1010h	52B0 2010h
14h	32	DCC_DCCSTATUS	52B0 0014h	52B0 1014h	52B0 2014h
18h	32	DCC_DCCCNT0	52B0 0018h	52B0 1018h	52B0 2018h
1Ch	32	DCC_DCCVALID0	52B0 001Ch	52B0 101Ch	52B0 201Ch
20h	32	DCC_DCCCNT1	52B0 0020h	52B0 1020h	52B0 2020h
24h	32	DCC_DCCCLKSRC1	52B0 0024h	52B0 1024h	52B0 2024h
28h	32	DCC_DCCCLKSRC0	52B0 0028h	52B0 1028h	52B0 2028h
2Ch	32	DCC_DCCGCTRL2	52B0 002Ch	52B0 102Ch	52B0 202Ch
30h	32	DCC_DCCSTATUS2	52B0 0030h	52B0 1030h	52B0 2030h
34h	32	DCC_DCCERRCNT	52B0 0034h	52B0 1034h	52B0 2034h

Table 4-1078. Registers, Base Address=0X0000000052B00000, Length=64

Offset	Length	Register Name	DCC3 Physical Address
0h	32	DCC_DCCGCTRL	52B0 3000h
4h	32	DCC_DCCREV	52B0 3004h
8h	32	DCC_DCCCNTSEED0	52B0 3008h
Ch	32	DCC_DCCVALIDSEED0	52B0 300Ch
10h	32	DCC_DCCCNTSEED1	52B0 3010h
14h	32	DCC_DCCSTATUS	52B0 3014h
18h	32	DCC_DCCCNT0	52B0 3018h
1Ch	32	DCC_DCCVALID0	52B0 301Ch
20h	32	DCC_DCCCNT1	52B0 3020h
24h	32	DCC_DCCCLKSRC1	52B0 3024h
28h	32	DCC_DCCCLKSRC0	52B0 3028h
2Ch	32	DCC_DCCGCTRL2	52B0 302Ch
30h	32	DCC_DCCSTATUS2	52B0 3030h
34h	32	DCC_DCCERRCNT	52B0 3034h

4.8.1 DCC_DCCGCTRL Registers

4.8.1.1 DCCGCTRL Register (Offset = 0h) [reset = 5555h]

Short Description: DCC Global Control Register

Long Description: Starts / stops the counters. Clears the error signal.

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Table 4-1079. Instance Table

Instance Name	Physical Address
DCC0	52B0 0000h
DCC1	52B0 1000h
DCC2	52B0 2000h
DCC3	52B0 3000h

Figure 4-511. DCC_DCCGCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
92fd31e7312															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DONEENA				SINGLESHOT				ERRENA				DCCENA			
R/W				R/W				R/W				R/W			
5h				5h				5h				5h			

Access Types Legend

Table 4-1080. DCC_DCCGCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:12	DONEENA	R/W	5h	The DONEENA bit enables/disables the done interrupt signal, but has no effect on the done status flag in DCCSTAT register. User, privilege, and debug mode (read): 0101 = the done signal is disabled others = the done signal is enabled Privilege and debug mode (write): 0101 = disable done signal generation others = enable done signal generation
11:8	SINGLESHOT	R/W	5h	The SINGLESHOT bit enables/disables repetitive operation of the DCC. User, privilege, and debug mode (read): 1010 = stop counting when counter0 and valid0 both reach zero 1011 = stop counting when counter1 reaches zero others = continuously repeat (until error) Privilege and debug mode (write): 1010 = stop counting when counter0 and valid0 both reach zero 1011 = stop counting when counter1 reaches zero others = continuously repeat (until error)
7:4	ERRENA	R/W	5h	The ERRENA bit enables/disables the error signal. User, privilege, and debug mode (read): 0101 = the error signal is disabled others = the error signal is enabled Privilege and debug mode (write): 0101 = disable error signal generation others = enable error signal generation
3:0	DCCENA	R/W	5h	The DCCENA bit starts and stops the operation of the dcc. User, privilege, and debug mode (read): 0101 = counters are stopped others = counters are running Privilege and debug mode (write): 0101 = stop counters and error-checking others = load the counters with their seed values and begin counting

4.8.2 DCC_DCCREV Registers

4.8.2.1 DCCREV Register (Offset = 4h) [reset = 40010b00h]

Short Description: DCC Revision ID

Long Description: Specifies the module version.

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Table 4-1081. Instance Table

Instance Name	Physical Address
DCC0	52B0 0004h
DCC1	52B0 1004h
DCC2	52B0 2004h
DCC3	52B0 3004h

Figure 4-512. DCC_DCCREV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		RESERVED		FUNC											
R		NONE		R											
1h		0		1h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL				MAJOR				CUSTOM		MINOR					
R				R				R		R					
1h				3h				0h		0h					

Access Types Legend

Table 4-1082. DCC_DCCREV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	User, privilege, and debug mode (read): Returns 01. Privilege and debug mode (write): Writes have no effect.
29:28	RESERVED	NONE		Reserved
27:16	FUNC	R	1h	Reflects software-compatability. If there is no level of software compatability, a unique func number is assigned; for compatible modules, the same number is maintained. User, privilege, and debug mode (read): 0x0 Privilege and debug mode (write): Writes have no effect.
15:11	RTL	R	1h	Incremented for releases due to spec changes or post-release design changes. Reset to 0 when either MAJOR or MINOR is incremented. User, privilege, and debug mode (read): 0x1 Privilege and debug mode (write): Writes have no effect.
10:8	MAJOR	R	3h	Represents major changes to the module (e.g. entirely new features are added/changed). The major revision number for this module. User, privilege, and debug mode (read): 0x2 Privilege and debug mode (write): Writes have no effect.
7:6	CUSTOM	R	0h	Indicates a special version of the module. May not be supported by standard software. User, privilege, and debug mode (read): 0x0 Privilege and debug mode (write): Writes have no effect.
5:0	MINOR	R	0h	Represents minor changes to the module (e.g. enhancements to existing features). The minor revision number for this module. User, privilege, and debug mode (read): 0x4 Privilege and debug mode (write): Writes have no effect.

4.8.3 DCC_DCCCNTSEED0 Registers

4.8.3.1 DCCCNTSEED0 Register (Offset = 8h) [reset = 0h]

Short Description: Count0 Seed Value Register

Long Description: Seed value for the counter attached to clock source 0

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Table 4-1083. Instance Table

Instance Name	Physical Address
DCC0	52B0 0008h
DCC1	52B0 1008h
DCC2	52B0 2008h
DCC3	52B0 3008h

Figure 4-513. DCC_DCCCNTSEED0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												COUNTSEED0			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNTSEED0															
R/W															
0h															

Access Types Legend

Table 4-1084. DCC_DCCCNTSEED0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	COUNTSEED0	R/W	0h	This field contains the seed value that gets loaded into counter 0 (clock source 0). User, privilege, and debug mode (read): Returns the current seed value for counter 0. Privilege and debug mode (write): Sets the current seed value for counter 0.

4.8.4 DCC_DCCVALIDSEED0 Registers

4.8.4.1 DCCVALIDSEED0 Register (Offset = Ch) [reset = 0h]

Short Description: Valid0 Seed Value Register

Long Description: Seed value for the timeout counter attached to clock source 0.

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Table 4-1085. Instance Table

Instance Name	Physical Address
DCC0	52B0 000Ch
DCC1	52B0 100Ch
DCC2	52B0 200Ch
DCC3	52B0 300Ch

Figure 4-514. DCC_DCCVALIDSEED0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALIDSEED0															
R/W															
0h															

Access Types Legend

Table 4-1086. DCC_DCCVALIDSEED0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	VALIDSEED0	R/W	0h	This field contains the seed value that gets loaded into the valid duration counter for clock source 0. User, privilege, and debug mode (read): Returns the current seed value for VALID0. Privilege and debug mode (write): Sets the current seed value for VALID0.

4.8.5 DCC_DCCCNTSEED1 Registers

4.8.5.1 DCCCNTSEED1 Register (Offset = 10h) [reset = 0h]

Short Description: Count1 Seed Value Register

Long Description: Seed value for the counter attached to clock source 1.

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Table 4-1087. Instance Table

Instance Name	Physical Address
DCC0	52B0 0010h
DCC1	52B0 1010h
DCC2	52B0 2010h
DCC3	52B0 3010h

Figure 4-515. DCC_DCCCNTSEED1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												COUNTSEED1			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNTSEED1															
R/W															
0h															

Access Types Legend

Table 4-1088. DCC_DCCCNTSEED1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	COUNTSEED1	R/W	0h	This field contains the seed value that gets loaded into counter 1 (clock source 1). User, privilege, and debug mode (read): Returns the current seed value for counter 1. Privilege and debug mode (write): Sets the current seed value for counter 1.

4.8.6 DCC_DCCSTATUS Registers

4.8.6.1 DCCSTATUS Register (Offset = 14h) [reset = 0h]

Short Description: DCC Status Register

Long Description: Specifies the status of the DCC Module.

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Table 4-1089. Instance Table

Instance Name	Physical Address
DCC0	52B0 0014h
DCC1	52B0 1014h
DCC2	52B0 2014h
DCC3	52B0 3014h

Figure 4-516. DCC_DCCSTATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														DONEFLG	ERRFLG
NONE														R/W1TC	R/W1TC
0														0h	0h

Access Types Legend

Table 4-1090. DCC_DCCSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1	DONEFLG	R/W1TC	0h	Indicates when single-shot mode is complete without error. Writing a 1 to this bit clears the flag. User, privilege, and debug mode (read): 0 = single-shot mode is not done 1 = single-shot mode is done Privilege and debug mode (write): 0 = no effect 1 = clear the done flag
0	ERRFLG	R/W1TC	0h	Indicates whether or not an error has occured. Writing a 1 to this bit clears the flag. User, privilege, and debug mode (read): 0 = an error has not occurred 1 = an error has occurred Privilege and debug mode (write): 0 = no effect 1 = clear the error flag

4.8.7 DCC_DCCCNT0 Registers

4.8.7.1 DCCCNT0 Register (Offset = 18h) [reset = 0h]

Short Description: Count0 Value Register

Long Description: Value of the counter attached to clock source 0.

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Table 4-1091. Instance Table

Instance Name	Physical Address
DCC0	52B0 0018h
DCC1	52B0 1018h
DCC2	52B0 2018h
DCC3	52B0 3018h

Figure 4-517. DCC_DCCCNT0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												COUNT0			
NONE												R			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT0															
R															
0h															

Access Types Legend

Table 4-1092. DCC_DCCCNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	COUNT0	R	0h	This field contains the current value of counter 0. User, privilege, and debug mode (read): Returns the current value for counter 0. Privilege and debug mode (write): Writes have no effect.

4.8.8 DCC_DCCVALID0 Registers

4.8.8.1 DCCVALID0 Register (Offset = 1Ch) [reset = 0h]

Short Description: Valid0 Value Register

Long Description: Value of the valid counter attached to clock source 0.

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Table 4-1093. Instance Table

Instance Name	Physical Address
DCC0	52B0 001Ch
DCC1	52B0 101Ch
DCC2	52B0 201Ch
DCC3	52B0 301Ch

Figure 4-518. DCC_DCCVALID0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALID0															
R															
0h															

Access Types Legend

Table 4-1094. DCC_DCCVALID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	VALID0	R	0h	This field contains the current value of valid counter 0. User, privilege, and debug mode (read): Returns the current value for valid counter 0. Privilege and debug mode (write): writes have no effect.

4.8.9 DCC_DCCCNT1 Registers

4.8.9.1 DCCCNT1 Register (Offset = 20h) [reset = 0h]

Short Description: Count1 Value Register

Long Description: Value of the counter attached to clock source 1.

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Table 4-1095. Instance Table

Instance Name	Physical Address
DCC0	52B0 0020h
DCC1	52B0 1020h
DCC2	52B0 2020h
DCC3	52B0 3020h

Figure 4-519. DCC_DCCCNT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												COUNT1			
NONE												R			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT1															
R															
0h															

Access Types Legend

Table 4-1096. DCC_DCCCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	COUNT1	R	0h	This field contains the current value of counter 1. User, privilege, and debug mode (read): Returns the current value for counter 1. Privilege and debug mode (write): writes have no effect.

4.8.10 DCC_DCCCLKSRC1 Registers

4.8.10.1 DCCCLKSRC1 Register (Offset = 24h) [reset = 0h]

Short Description: Clock Source Selection Register 1

Long Description: Selects the clock source for counter 1.

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Table 4-1097. Instance Table

Instance Name	Physical Address
DCC0	52B0 0024h
DCC1	52B0 1024h
DCC2	52B0 2024h
DCC3	52B0 3024h

Figure 4-520. DCC_DCCCLKSRC1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY				RESERVED							CLKSRC1				
R/W				NONE							R/W				
0h				0							0h				

Access Types Legend

Table 4-1098. DCC_DCCCLKSRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:12	KEY	R/W	0h	This field enables or disables clock source selection for counter 1. User, privilege, and debug mode (read): Returns the current value of the key. Privilege and debug mode (write): Sets the key value. Key values: 1010: The CLKSRC field selects the clock source for counter 1. others: Clock source selection is disabled. The secondary oscillator (clock source 1) is selected for counter 1.
11:5	RESERVED	NONE		Reserved
4:0	CLKSRC1	R/W	0h	This field specifies the clock source for counter 1, when the KEY field enables this feature. User, privilege, and debug mode (read): Returns the current value of CLKSRC. Privilege and debug mode (write): Sets the value of CLKSRC.

4.8.11 DCC_DCCCLKSRC0 Registers

4.8.11.1 DCCCLKSRC0 Register (Offset = 28h) [reset = 0h]

Short Description: Clock Source Selection Register 0

Long Description: Selects the clock source for counter 0.

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Table 4-1099. Instance Table

Instance Name	Physical Address
DCC0	52B0 0028h
DCC1	52B0 1028h
DCC2	52B0 2028h
DCC3	52B0 3028h

Figure 4-521. DCC_DCCCLKSRC0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY				RESERVED								CLKSRC0			
R/W				NONE								R/W			
0h				0								0h			

Access Types Legend

Table 4-1100. DCC_DCCCLKSRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:12	KEY	R/W	0h	This field enables or disables clock source selection for counter 0. User, privilege, and debug mode (read): Returns the current value of the key. Privilege and debug mode (write): Sets the key value. Key values: 1010: The CLKSRC field selects the clock source for counter 0. others: Clock source selection is disabled. The external oscillator (XTAL) is selected for counter 0.
11:4	RESERVED	NONE		Reserved
3:0	CLKSRC0	R/W	0h	This field specifies the clock source for counter 0. User, privilege, and debug mode (read): Returns the current value of CLKSRC0. Privilege and debug mode (write): Sets the value of CLKSRC0.

4.8.12 DCC_DCCGCTRL2 Registers

4.8.12.1 DCCGCTRL2 Register (Offset = 2Ch) [reset = 555h]

Short Description: DCC Global Control Register 2

Long Description: Allows configuring different modes of operation for DCC.

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Table 4-1101. Instance Table

Instance Name	Physical Address
DCC0	52B0 002Ch
DCC1	52B0 102Ch
DCC2	52B0 202Ch
DCC3	52B0 302Ch

Figure 4-522. DCC_DCCGCTRL2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
3c34eb12															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				FIFO_NONERR				FIFO_READ				CONT_ON_ERR			
NONE				R/W				R/W				R/W			
3c34eb12				5h				5h				5h			

Access Types Legend

Table 4-1102. DCC_DCCGCTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:8	FIFO_NONERR	R/W	5h	Enables/disables FIFO writes without the error event on completion of comparison window. User, privilege, and debug mode (read): Returns the current field value. Privilege and debug mode (write): Sets the value of field value. Source values: 0101: Counter values are captured to non-full FIFO only upon Error event. Others: Write counter values to non-full FIFO upon completion of comparison window regardless of error or not.
7:4	FIFO_READ	R/W	5h	Enables the counter read registers reflect FIFO output instead of the live counter value. User, privilege, and debug mode (read): Returns the current field value. Privilege and debug mode (write): Sets the value of field value. Source values: 0101: Counter value is read directly. Others: Counters FIFO output is read.
3:0	CONT_ON_ERR	R/W	5h	Continues to next window of comparison despite the error condition. User, privilege, and debug mode (read): Returns the current field value. Privilege and debug mode (write): Sets the value of field value. Enable values: 0101: Comparison and counter reload is stopped from advancing if error is detected. Others: Counters get reloaded with seed and continue counting despite the error condition.

4.8.13 DCC_DCCSTATUS2 Registers

4.8.13.1 DCCSTATUS2 Register (Offset = 30h) [reset = 7h]

Short Description: DCC FIFO Status Register

Long Description: Specifies the status of the DCC FIFOs.

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Table 4-1103. Instance Table

Instance Name	Physical Address
DCC0	52B0 0030h
DCC1	52B0 1030h
DCC2	52B0 2030h
DCC3	52B0 3030h

Figure 4-523. DCC_DCCSTATUS2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
b															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										COUNT1_FIFO_FULL	VALID0_FIFO_FULL	COUNT0_FIFO_FULL	COUNT1_FIFO_EMPTY	VALID0_FIFO_EMPTY	COUNT0_FIFO_EMPTY
NONE										R	R	R	R	R	R
b										0h	0h	0h	1h	1h	1h

Access Types Legend

Table 4-1104. DCC_DCCSTATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE		Reserved
5	COUNT1_FIFO_FULL	R	0h	Count1 FIFO Full. Indicates whether Count1 FIFO is full. User, privilege, and debug mode (read): 0: Count1 FIFO is not full 1: Count1 FIFO is full. Privilege and debug mode (write): Writes have no effect.
4	VALID0_FIFO_FULL	R	0h	Valid0 FIFO Full. Indicates whether Valid0 FIFO is full. User, privilege, and debug mode (read): 0: Valid0 FIFO is not full 1: Valid0 FIFO is full. Privilege and debug mode (write): Writes have no effect.
3	COUNT0_FIFO_FULL	R	0h	Count0 FIFO Full. Indicates whether Count0 FIFO is full. User, privilege, and debug mode (read): 0: Count0 FIFO is not full 1: Count0 FIFO is full. Privilege and debug mode (write): Writes have no effect.
2	COUNT1_FIFO_EMPTY	R	1h	Count1 FIFO Empty. Indicates whether Count1 FIFO is empty. User, privilege, and debug mode (read): 0: Count1 FIFO is not empty 1: Count1 FIFO is empty. Privilege and debug mode (write): Writes have no effect.
1	VALID0_FIFO_EMPTY	R	1h	Valid0 FIFO Empty. Indicates whether Valid0 FIFO is empty. User, privilege, and debug mode (read): 0: Valid0 FIFO is not empty 1: Valid0 FIFO is empty. Privilege and debug mode (write): Writes have no effect.
0	COUNT0_FIFO_EMPTY	R	1h	Count0 FIFO Empty. Indicates whether Count0 FIFO is empty. User, privilege, and debug mode (read): 0: Count0 FIFO is not empty 1: Count0 FIFO is empty. Privilege and debug mode (write): Writes have no effect.

4.8.14 DCC_DCCERRCNT Registers

4.8.14.1 DCCERRCNT Register (Offset = 34h) [reset = 0h]

Short Description: Error Count Register

Long Description: Counts number of errors since last clear.

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Table 4-1105. Instance Table

Instance Name	Physical Address
DCC0	52B0 0034h
DCC1	52B0 1034h
DCC2	52B0 2034h
DCC3	52B0 3034h

Figure 4-524. DCC_DCCERRCNT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						ERRCNT									
NONE						R/W									
0						0h									

Access Types Legend

Table 4-1106. DCC_DCCERRCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	ERRCNT	R/W	0h	Counts the number of errors after the last write to this register or reset. If reached terminal count the count freezes. User needs to clear it.

4.8.15 Access Table

Table 4-1107. Access Type Codes

Access Type	Code	Description
R/W	R/W	Read / Write
R	R	Read
R/W1TC	R/W1TC	Read/Write 1 To Clear

4.9 ECC_AGG_TOP Registers

Table 4-1108. MSS_ECC_AGG_TOP Registers Base Address Table

Offset	Length	Acronym	MSS_ECC_AGG_TOP Physical Address
0h	32	ECC_AGG_TOP_REV	5301 0000h
8h	24	ECC_AGG_TOP_VECTOR	5301 0008h
Ch	16	ECC_AGG_TOP_STAT	5301 000Ch
14h	8	ECC_AGG_TOP_CTRL	5301 0014h
18h	32	ECC_AGG_TOP_ERR_CTRL1	5301 0018h
1Ch	32	ECC_AGG_TOP_ERR_CTRL2	5301 001Ch
20h	32	ECC_AGG_TOP_ERR_STAT1	5301 0020h

Table 4-1108. MSS_ECC_AGG_TOP Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_ECC_AGG_TOP Physical Address
24h	32	ECC_AGG_TOP_ERR_STAT2	5301 0024h
28h	16	ECC_AGG_TOP_ERR_STAT3	5301 0028h
3Ch	0	ECC_AGG_TOP_SEC_EOI_REG	5301 003Ch
40h	8	ECC_AGG_TOP_SEC_STATUS_REG0	5301 0040h
80h	8	ECC_AGG_TOP_SEC_ENABLE_SET_REG0	5301 0080h
C0h	8	ECC_AGG_TOP_SEC_ENABLE_CLR_REG0	5301 00C0h
13Ch	0	ECC_AGG_TOP_DED_EOI_REG	5301 013Ch
140h	8	ECC_AGG_TOP_DED_STATUS_REG0	5301 0140h
180h	8	ECC_AGG_TOP_DED_ENABLE_SET_REG0	5301 0180h
1C0h	8	ECC_AGG_TOP_DED_ENABLE_CLR_REG0	5301 01C0h
200h	8	ECC_AGG_TOP_AGGR_ENABLE_SET	5301 0200h
204h	8	ECC_AGG_TOP_AGGR_ENABLE_CLR	5301 0204h
208h	8	ECC_AGG_TOP_AGGR_STATUS_SET	5301 0208h
20Ch	8	ECC_AGG_TOP_AGGR_STATUS_CLR	5301 020Ch

4.9.1 MSS_ECC_AGG_TOP_REV Registers

4.9.1.1 ECC_AGG_TOP_REV Register (Offset = 0h) [reset = h]

Short Description: Revision parameters

Long Description:

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Table 4-1109. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0000h

Access Types Legend

Table 4-1110. REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	Scheme
29 - 28	BU	RO	2h	bu
27 - 16	MODULE_ID	RO	6A0h	Module ID
15 - 11	REVRTL	RO	1Dh	RTL version
10 - 8	REVMAJ	RO	Ah	Major version
7 - 6	CUSTOM	RO	0h	Custom version
5 - 0	REVMIN	RO	0h	Minor version

4.9.2 MSS_ECC_AGG_TOP_VECTOR Registers

4.9.2.1 ECC_AGG_TOP_VECTOR Register (Offset = 8h) [reset = h]

Short Description: ECC Vector Register

Long Description:

Return to Summary Table

Table 4-1111. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0008h

Access Types Legend

Table 4-1112. VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
24	RD_SVBUS_DONE	RW	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23 - 16	RD_SVBUS_ADDRESS	RW	0h	Read address
15	RD_SVBUS	RW	0h	Write 1 to trigger a read on the serial VBUS
	RESERVED	NONE		Reserved
10 - 0	ECC_VECTOR	RW	0h	Value written to select the corresponding ECC RAM for control or status

4.9.3 MSS_ECC_AGG_TOP_STAT Registers

4.9.3.1 ECC_AGG_TOP_STAT Register (Offset = Ch) [reset = h]

Short Description: Misc Status

Long Description:

Return to Summary Table

Table 4-1113. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 000Ch

Access Types Legend

Table 4-1114. STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
10 - 0	NUM_RAMS	RO	9h	Indicates the number of RAMS serviced by the ECC aggregator

4.9.4 MSS_ECC_AGG_TOP_CTRL Registers

4.9.4.1 ECC_AGG_TOP_CTRL Register (Offset = 14h) [reset = h]

Short Description: ECC Control Register

Long Description:

Return to Summary Table

Table 4-1115. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0014h

Access Types Legend

Table 4-1116. CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
8	CHECK_SVBUS_TIMEOUT	RW	1h	check for svbus timeout errors
7	CHECK_PARITY	RW	1h	check for parity errors
6	ERROR_ONCE	RW	0h	Force Error only once
5	FORCE_N_ROW	RW	0h	Force Error on any RAM read
4	FORCE_DED	RW	0h	Force Double Bit Error
3	FORCE_SEC	RW	0h	Force Single Bit Error
2	ENABLE_RMW	RW	1h	Enable rmw
1	ECC_CHECK	RW	1h	Enable ECC check
0	ECC_ENABLE	RW	1h	Enable ECC

4.9.5 MSS_ECC_AGG_TOP_ERR_CTRL1 Registers

4.9.5.1 ECC_AGG_TOP_ERR_CTRL1 Register (Offset = 18h) [reset = h]

Short Description: ECC Error Control1 Register

Long Description:

Return to Summary Table

Table 4-1117. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0018h

Access Types Legend

Table 4-1118. ERR_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ECC_ROW	RW	0h	Row address where single or double-bit error needs to be applied. This is ignored if force_n_row is set

4.9.6 MSS_ECC_AGG_TOP_ERR_CTRL2 Registers

4.9.6.1 ECC_AGG_TOP_ERR_CTRL2 Register (Offset = 1Ch) [reset = h]

Short Description: ECC Error Control2 Register

Long Description:

Return to Summary Table

Table 4-1119. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 001Ch

Access Types Legend

Table 4-1120. ERR_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	ECC_BIT2	RW	0h	Data bit that needs to be flipped if double bit error needs to be forced
15 - 0	ECC_BIT1	RW	0h	Data bit that needs to be flipped when force_sec is set

4.9.7 MSS_ECC_AGG_TOP_ERR_STAT1 Registers

4.9.7.1 ECC_AGG_TOP_ERR_STAT1 Register (Offset = 20h) [reset = h]

Short Description: ECC Error Status1 Register

Long Description:

Return to Summary Table

Table 4-1121. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0020h

Access Types Legend

Table 4-1122. ERR_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	ECC_BIT1	RO	0h	Data bit that corresponds to the single-bit error
15	CLR_CTRL_REG_ERR	RW	0h	Clear control reg error Error Status, you must also re write the contorl ergister itself to clear this
14 - 13	CLR_PARITY_ERR	RW DECR	0h	Clear parity Error Status
12	CLR_ECC_OTHER	RW	0h	Clear other Error Status
11 - 10	CLR_ECC_DED	RW DECR	0h	Clear Double Bit Error Status
9 - 8	CLR_ECC_SEC	RW DECR	0h	Clear Single Bit Error Status
7	CTR_REG_ERR	RW	0h	control register error pending, Level interrupt
6 - 5	PARITY_ERR	RW	0h	Level parity error Error Status
4	ECC_OTHER	RW	0h	successive single-bit errors have occurred while a writeback is still pending, Level interrupt
3 - 2	ECC_DED	RW INCR	0h	Level Double Bit Error Status
1 - 0	ECC_SEC	RW INCR	0h	Level Single Bit Error Status

4.9.8 MSS_ECC_AGG_TOP_ERR_STAT2 Registers

4.9.8.1 ECC_AGG_TOP_ERR_STAT2 Register (Offset = 24h) [reset = h]

Short Description: ECC Error Status2 Register

Long Description:

Return to Summary Table

Table 4-1123. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0024h

Access Types Legend

Table 4-1124. ERR_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ECC_ROW	RO	0h	Row address where the single or double-bit error has occurred

4.9.9 MSS_ECC_AGG_TOP_ERR_STAT3 Registers

4.9.9.1 ECC_AGG_TOP_ERR_STAT3 Register (Offset = 28h) [reset = h]

Short Description: ECC Error Status3 Register

Long Description:

Return to Summary Table

Table 4-1125. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0028h

Access Types Legend

Table 4-1126. ERR_STAT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9	CLR_SVBUS_TIMEOUT_ERR	RW	0h	Clear svbus timeout Error Status
	RESERVED	NONE		Reserved
1	SVBUS_TIMEOUT_ERR	RW	0h	Level svbus timeout error Error Status
0	WB_PEND	RO	0h	delayed write back pending Status

4.9.10 MSS_ECC_AGG_TOP_SEC_EOI_REG Registers

4.9.10.1 ECC_AGG_TOP_SEC_EOI_REG Register (Offset = 3Ch) [reset = h]

Short Description: EOI Register

Long Description:

Return to Summary Table

Table 4-1127. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 003Ch

Access Types Legend

Table 4-1128. SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
0	EOI_WR	RW	0h	EOI Register

4.9.11 MSS_ECC_AGG_TOP_SEC_STATUS_REG0 Registers

4.9.11.1 ECC_AGG_TOP_SEC_STATUS_REG0 Register (Offset = 40h) [reset = h]

Short Description: Interrupt Status Register 0

Long Description:

Return to Summary Table

Table 4-1129. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0040h

Access Types Legend

Table 4-1130. SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	TPTC_A1_PEND	RW	0h	Interrupt Pending Status for tptc_a1_pend
5	TPTC_A0_PEND	RW	0h	Interrupt Pending Status for tptc_a0_pend
4	MSS_MBOX_PEND	RW	0h	Interrupt Pending Status for mss_mbox_pend
3	MSS_L2SLV3_PEND	RW	0h	Interrupt Pending Status for mss_l2slv3_pend
2	MSS_L2SLV2_PEND	RW	0h	Interrupt Pending Status for mss_l2slv2_pend
1	MSS_L2SLV1_PEND	RW	0h	Interrupt Pending Status for mss_l2slv1_pend
0	MSS_L2SLV0_PEND	RW	0h	Interrupt Pending Status for mss_l2slv0_pend

4.9.12 MSS_ECC_AGG_TOP_SEC_ENABLE_SET_REG0 Registers

4.9.12.1 ECC_AGG_TOP_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = h]

Short Description: Interrupt Enable Set Register 0

Long Description:

Return to Summary Table

Table 4-1131. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0080h

Access Types Legend

Table 4-1132. SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	TPTC_A1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for tptc_a1_pend
5	TPTC_A0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for tptc_a0_pend
4	MSS_MBOX_ENABLE_SET	RW	0h	Interrupt Enable Set Register for mss_mbox_pend
3	MSS_L2SLV3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for mss_l2slv3_pend
2	MSS_L2SLV2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for mss_l2slv2_pend
1	MSS_L2SLV1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for mss_l2slv1_pend
0	MSS_L2SLV0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for mss_l2slv0_pend

4.9.13 MSS_ECC_AGG_TOP_SEC_ENABLE_CLR_REG0 Registers

4.9.13.1 ECC_AGG_TOP_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = h]

Short Description: Interrupt Enable Clear Register 0

Long Description:

Return to Summary Table

Table 4-1133. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 00C0h

Access Types Legend

Table 4-1134. SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	TPTC_A1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for tptc_a1_pend
5	TPTC_A0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for tptc_a0_pend
4	MSS_MBOX_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for mss_mbox_pend
3	MSS_L2SLV3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for mss_l2slv3_pend
2	MSS_L2SLV2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for mss_l2slv2_pend
1	MSS_L2SLV1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for mss_l2slv1_pend
0	MSS_L2SLV0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for mss_l2slv0_pend

4.9.14 MSS_ECC_AGG_TOP_DED_EOI_REG Registers

4.9.14.1 ECC_AGG_TOP_DED_EOI_REG Register (Offset = 13Ch) [reset = h]

Short Description: EOI Register

Long Description:

Return to Summary Table

Table 4-1135. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 013Ch

Access Types Legend

Table 4-1136. DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
0	EOI_WR	RW	0h	EOI Register

4.9.15 MSS_ECC_AGG_TOP_DED_STATUS_REG0 Registers

4.9.15.1 ECC_AGG_TOP_DED_STATUS_REG0 Register (Offset = 140h) [reset = h]

Short Description: Interrupt Status Register 0

Long Description:

Return to Summary Table

Table 4-1137. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0140h

Access Types Legend

Table 4-1138. DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	TPTC_A1_PEND	RW	0h	Interrupt Pending Status for tptc_a1_pend
5	TPTC_A0_PEND	RW	0h	Interrupt Pending Status for tptc_a0_pend
4	MSS_MBOX_PEND	RW	0h	Interrupt Pending Status for mss_mbox_pend
3	MSS_L2SLV3_PEND	RW	0h	Interrupt Pending Status for mss_l2slv3_pend
2	MSS_L2SLV2_PEND	RW	0h	Interrupt Pending Status for mss_l2slv2_pend
1	MSS_L2SLV1_PEND	RW	0h	Interrupt Pending Status for mss_l2slv1_pend
0	MSS_L2SLV0_PEND	RW	0h	Interrupt Pending Status for mss_l2slv0_pend

4.9.16 MSS_ECC_AGG_TOP_DED_ENABLE_SET_REG0 Registers

4.9.16.1 ECC_AGG_TOP_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = h]

Short Description: Interrupt Enable Set Register 0

Long Description:

Return to Summary Table

Table 4-1139. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0180h

Access Types Legend

Table 4-1140. DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	TPTC_A1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for tptc_a1_pend
5	TPTC_A0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for tptc_a0_pend
4	MSS_MBOX_ENABLE_SET	RW	0h	Interrupt Enable Set Register for mss_mbox_pend
3	MSS_L2SLV3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for mss_l2slv3_pend
2	MSS_L2SLV2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for mss_l2slv2_pend
1	MSS_L2SLV1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for mss_l2slv1_pend
0	MSS_L2SLV0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for mss_l2slv0_pend

4.9.17 MSS_ECC_AGG_TOP_DED_ENABLE_CLR_REG0 Registers

4.9.17.1 ECC_AGG_TOP_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = h]

Short Description: Interrupt Enable Clear Register 0

Long Description:

Return to Summary Table

Table 4-1141. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 01C0h

Access Types Legend

Table 4-1142. DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	TPTC_A1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for tptc_a1_pend
5	TPTC_A0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for tptc_a0_pend
4	MSS_MBOX_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for mss_mbox_pend
3	MSS_L2SLV3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for mss_l2slv3_pend
2	MSS_L2SLV2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for mss_l2slv2_pend
1	MSS_L2SLV1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for mss_l2slv1_pend
0	MSS_L2SLV0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for mss_l2slv0_pend

4.9.18 MSS_ECC_AGG_TOP_AGGR_ENABLE_SET Registers

4.9.18.1 ECC_AGG_TOP_AGGR_ENABLE_SET Register (Offset = 200h) [reset = h]

Short Description: AGGR interrupt enable set Register

Long Description:

Return to Summary Table

Table 4-1143. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0200h

Access Types Legend

Table 4-1144. AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	TIMEOUT	RW	0h	interrupt enable set for svbus timeout errors
0	PARITY	RW	0h	interrupt enable set for parity errors

4.9.19 MSS_ECC_AGG_TOP_AGGR_ENABLE_CLR Registers

4.9.19.1 ECC_AGG_TOP_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = h]

Short Description: AGGR interrupt enable clear Register

Long Description:

Return to Summary Table

Table 4-1145. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0204h

Access Types Legend

Table 4-1146. AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	TIMEOUT	RW	0h	interrupt enable clear for svbus timeout errors
0	PARITY	RW	0h	interrupt enable clear for parity errors

4.9.20 MSS_ECC_AGG_TOP_AGGR_STATUS_SET Registers

4.9.20.1 ECC_AGG_TOP_AGGR_STATUS_SET Register (Offset = 208h) [reset = h]

Short Description: AGGR interrupt status set Register

Long Description:

Return to Summary Table

Table 4-1147. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0208h

Access Types Legend

Table 4-1148. AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 2	TIMEOUT	RW INCR	0h	interrupt status set for svbus timeout errors
1 - 0	PARITY	RW INCR	0h	interrupt status set for parity errors

4.9.21 MSS_ECC_AGG_TOP_AGGR_STATUS_CLR Registers

4.9.21.1 ECC_AGG_TOP_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = h]

Short Description: AGGR interrupt status clear Register

Long Description:

Return to Summary Table

Table 4-1149. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 020Ch

Access Types Legend

Table 4-1150. AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 2	TIMEOUT	RW DECR	0h	interrupt status clear for svbus timeout errors
1 - 0	PARITY	RW DECR	0h	interrupt status clear for parity errors

4.9.22 Access Table

Table 4-1151. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write
RW DECR	RW DECR	Read / Write to Decrement
RW INCR	RW INCR	Read / Write to Increment

4.10 I2C Registers

Table 4-1152. MSS_I2C[0:2] Registers Base Address Table

Offset	Length	Acronym	MSS_I2C0 Physical Address	MSS_I2C1 Physical Address	MSS_I2C2 Physical Address
0h	32	I2C_ICOAR	5250 0000h	5250 1000h	5250 2000h
4h	32	I2C_ICIMR	5250 0004h	5250 1004h	5250 2004h
8h	32	I2C_ICSTR	5250 0008h	5250 1008h	5250 2008h
Ch	32	I2C_ICCLKL	5250 000Ch	5250 100Ch	5250 200Ch
10h	32	I2C_ICCLKH	5250 0010h	5250 1010h	5250 2010h
14h	32	I2C_ICCNT	5250 0014h	5250 1014h	5250 2014h
18h	32	I2C_ICDRR	5250 0018h	5250 1018h	5250 2018h
1Ch	32	I2C_ICSAR	5250 001Ch	5250 101Ch	5250 201Ch
20h	32	I2C_ICDXR	5250 0020h	5250 1020h	5250 2020h
24h	32	I2C_ICMDR	5250 0024h	5250 1024h	5250 2024h
28h	32	I2C_ICIVR	5250 0028h	5250 1028h	5250 2028h
2Ch	32	I2C_ICEMDR	5250 002Ch	5250 102Ch	5250 202Ch
30h	32	I2C_ICPSC	5250 0030h	5250 1030h	5250 2030h
34h	32	I2C_ICPID1	5250 0034h	5250 1034h	5250 2034h
38h	32	I2C_ICPID2	5250 0038h	5250 1038h	5250 2038h
3Ch	32	I2C_ICDMAC	5250 003Ch	5250 103Ch	5250 203Ch
40h	32	I2C_I2C_RESERVED1	5250 0040h	5250 1040h	5250 2040h
44h	32	I2C_I2C_RESERVED2	5250 0044h	5250 1044h	5250 2044h

Table 4-1152. MSS_I2C[0:2] Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_I2C0 Physical Address	MSS_I2C1 Physical Address	MSS_I2C2 Physical Address
48h	32	I2C_ICPFUNC	5250 0048h	5250 1048h	5250 2048h
4Ch	32	I2C_ICPDIR	5250 004Ch	5250 104Ch	5250 204Ch
50h	32	I2C_ICPDIN	5250 0050h	5250 1050h	5250 2050h
54h	32	I2C_ICPDOUT	5250 0054h	5250 1054h	5250 2054h
58h	32	I2C_ICPDSET	5250 0058h	5250 1058h	5250 2058h
5Ch	32	I2C_ICPDCLR	5250 005Ch	5250 105Ch	5250 205Ch
60h	32	I2C_ICPDRV	5250 0060h	5250 1060h	5250 2060h

Table 4-1153. MSS_I2C3 Registers Base Address Table

Offset	Length	Acronym	MSS_I2C3 Physical Address
0h	32	I2C_ICOAR	5250 3000h
4h	32	I2C_ICIMR	5250 3004h
8h	32	I2C_ICSTR	5250 3008h
Ch	32	I2C_ICCLKL	5250 300Ch
10h	32	I2C_ICCLKH	5250 3010h
14h	32	I2C_ICCNT	5250 3014h
18h	32	I2C_ICDRR	5250 3018h
1Ch	32	I2C_ICSAR	5250 301Ch
20h	32	I2C_ICDXR	5250 3020h
24h	32	I2C_ICMDR	5250 3024h
28h	32	I2C_ICIVR	5250 3028h
2Ch	32	I2C_ICEMDR	5250 302Ch
30h	32	I2C_ICPSC	5250 3030h
34h	32	I2C_ICPID1	5250 3034h
38h	32	I2C_ICPID2	5250 3038h
3Ch	32	I2C_ICDMAC	5250 303Ch
40h	32	I2C_I2C_RESERVED1	5250 3040h
44h	32	I2C_I2C_RESERVED2	5250 3044h
48h	32	I2C_ICPFUNC	5250 3048h
4Ch	32	I2C_ICPDIR	5250 304Ch
50h	32	I2C_ICPDIN	5250 3050h
54h	32	I2C_ICPDOUT	5250 3054h
58h	32	I2C_ICPDSET	5250 3058h
5Ch	32	I2C_ICPDCLR	5250 305Ch
60h	32	I2C_ICPDRV	5250 3060h

4.10.1 I2C Instance Count Note

Note

n = 0 to 3 for the I2C registers defined below.

4.10.2 MSS_I2Cn_ICOAR Registers

4.10.2.1 I2Cn_ICOAR Register (Offset = 0h) [reset = h]

Short Description: I2C Own Address register

Long Description:

Return to Summary Table

Table 4-1154. Instance Table

Instance Name	Physical Address
I2C0	5250 0000h
I2C1	5250 1000h
I2C2	5250 2000h
I2C3	5250 3000h

Access Types Legend

Table 4-1155. ICOAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 10	NU	RW	0h	Reserved
9 - 0	A9_A0	RW	0h	Own address. Use in both 7- and 10-bit address mode. Note that usercan program the I2C own address to any value as long as it does notconflict with other components in the system.

4.10.3 MSS_I2Cn_ICIMR Registers

4.10.3.1 I2Cn_ICIMR Register (Offset = 4h) [reset = h]

Short Description: I2C Interrupt Mask/Status register

Long Description:

Return to Summary Table

Table 4-1156. Instance Table

Instance Name	Physical Address
I2C0	5250 0004h
I2C1	5250 1004h
I2C2	5250 2004h
I2C3	5250 3004h

Access Types Legend

Table 4-1157. ICIMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 7	NU	RW	0h	Reserved
6	AAS	RW	0h	Address As Slave interrupt mask bit. Setting a"1" to this bit unmasks the Address As Slave interrupt. Setting a"0" to this bit masks the Address As Slave interrupt.
5	SCD	RW	0h	Stop Condition Detection mask bit. Setting a"1" to this bit unmasks the Stop Condition Detection interrupt. Setting a "0" to this bit masks the Stop Condition Detection interrupt.
4	ICXRDY	RW	0h	Transmit Data Ready interrupt mask bit. Setting a"1" to this bit unmasks the Transmit Data Ready interrupt. Setting a"0" to this bit masks the Transmit Data Ready interrupt.
3	ICRRDY	RW	0h	Receive Data Ready interrupt mask bit. Setting a"1" to this bit unmasks the Receive Data Ready interrupt. Setting a"0" to this bit masks the Receive Data Ready interrupt.
2	ARDY	RW	0h	Register access ready interrupt mask bit. Setting a"1" to this bit unmasks the Register access ready interrupt. Setting a"0" to this bit masks the Register access ready interrupt.
1	NACK	RW	0h	No Acknowledgement interrupt mask bit. Setting a"1" to this bit unmasks the No Acknowledgement interrupt. Setting a"0" to this bit masks the No Acknowledgement interrupt.
0	AL	RW	0h	Arbitration Lost interrupt mask bit. Setting a"1" to this bit unmasks the Arbitration Lost interrupt. Setting a"0" to this bit masks the Arbitration Lost interrupt.

4.10.4 MSS_I2Cn_ICSTR Registers

4.10.4.1 I2Cn_ICSTR Register (Offset = 8h) [reset = h]

Short Description: I2C Interrupt Status register

Long Description:

Return to Summary Table

Table 4-1158. Instance Table

Instance Name	Physical Address
I2C0	5250 0008h
I2C1	5250 1008h
I2C2	5250 2008h
I2C3	5250 3008h

Access Types Legend

Table 4-1159. ICSTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 15	NU2	RW	0h	Reserved
14	SDIR	RW	0h	Slave Direction. This bit is clear to '0' indicating the I2C is a master transmitter/receiver or a slave receiver. This bit is also clear by STOP condition or START condition. It is set to '1' when the I2C slave is a transmitter. In DLB mode (which the configuration should be master-transmitter slave-receiver) this bit is clear to '0'. Writing a"1" to this bit to clear it.
13	NACKSNT	RW	0h	A No Acknowledge is sent due to NACKMOD is set to a"1". NACKSNT =0: A No Acknowledge is not sent. NACKSNT =1: A No Acknowledge is sent. Writing a"1" to this bit to clear it.
12	BB	RW	0h	Bus Busy. This bit indicates the state of the serial bus. BB=0: The bus is free. BB=1: The bus is occupied. On reception of a"start" condition the device sets BB to 1. This bit is also set if the I2C detects SCL low state. BB is clear to 0 after reception of a"stop" condition. BB is kept to"0" regardless SCL state when the I2C is in reset (IRS_=0). If the IRS_ is set to"1" during transaction between other I2C devices the BB bit is set at the first falling edge of SCL or START condition. - (RW)
11	RSFULL	RW	0h	Receive shift full. This bit indicates whether the receiver has experienced overrun. Overrun occurs when the receive shift register (ICRSR) is full and ICDRR has not been read since the ICRSR-to-ICDRR transfer. The FSM is holding for ICDRR read access. RSFULL is clear when reading the ICDRR. RSFULL is set to"1" when the I2C has recognized an overrun. The contents of ICDRR are NOT lost in this case. In repeat mode since double buffer (ICRSR and ICDRR) behaves like a single buffer RSFULL is set to"1" every time the data is received. RSFULL is clear as a result of reading the ICDRR. - (RW)
10	XSMT	RW	0h	Transmit shift empty not. This bit indicates whether the transmitter has experienced underflow. Underflow occurs when the transmit shift register (ICXSR) is empty and ICDXR has not been loaded. The FSM is holding for ICDXR write access. XSMT_ is cleared when underflow has occurred. XSMT_ is set to"1" as a result of writing to ICDXR. In repeat mode if the I2C in master transmitter mode is holding transfer with XSMT_=0 (i.e. waiting for further action) and the STT or STP bit is set XSMT_ is set to"1" by hardware.
9	AAS	RW	0h	Address As Slave. This bit is set to 1 by the device when it has recognized its own slave address or an address of all (8) zeros. The AAS bit is reset by stop condition or detection of any address byte that does not match ICOAR. - (RW)

Table 4-1159. ICSTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	AD0	RW	0h	Address Zero Status: This bit is set to 1 by device if it detects the address of all (8) zeros (i.e. general call). The AD0 bit is reset to 0 (default value) when a"start" or"stop" condition is detected. - (RW)
7 - 6	NU1	RW	0h	Reserved
5	SCD	RW	0h	Stop Condition Detection bit SCD is set when the I2C sends or receives STOP condition. This bit is cleared by reading ICIVR (as 110) or writing '1' to itself.
4	ICXRDY	RW	0h	Transmit Data Ready interrupt flag bit. ICXRDY is set to"1" is generated when the transmitted data has been copied from ICDXR to the transmit-shift register (ICXSR). ICRXDY is clear to"0" when the ICDXR is written. This bit can also be polled by the CPU to write a new transmitted data into the ICDXR. Write '1' to this bit will set it and DXR Write will clear it.
3	ICRRDY	RW	0h	Receive Data Ready interrupt flag bit. ICRRDY is set to"1" when the received data has been copied from ICRSR into the ICDRR. ICRRDY is cleared to"0" when the ICDRR is read. This bit can also be polled by the CPU to read the received data in the ICDRR. Write '1' or DRR Read will clear it.
2	ARDY	RW	0h	Register-access-ready interrupt flag bit. ARDY is generated by the hardware if the I2C is in the master mode when the previously programmed data and command has been performed and status bit has been updated. This flag is used by the CPU to let it knows that the I2C registers are ready to be accessed again. When RM=0 ARDY is set when the internal data count is passed 0 if STP register bit has not been set. When RM=1 ARDY is set at each byte end. If the I2C is in FDF mode(FDF=1) ARDY is set just after Start condition. This bit is automatically cleared by hardware when writing data to ICDXR in transmit mode reading data from ICDRR in receive mode or setting STT or STP bit. Write '1' will clear it.
1	NACK	RW	0h	No-Acknowledgement interrupt flag bit. The No Acknowledge flag bit is set when the hardware in "master" mode detects no acknowledge has been received. This bit is NOT set by no-acknowledgement after Start byte Write '1' or Read the ICIVR (as 010) will clear it.
0	AL	RW	0h	Arbitration-Lost interrupt flag bit. The Arbitration Lost flag bit is set to 1 when the device in the "master" mode senses it has lost an arbitration when two or more transmitters start a transmission almost simultaneously or when the I2C attempts to start a transfer while BB (bus busy) is 1. When this is set to 1 due to arbitration lost the MST/STT/STP bits are clear the I2C becomes a slave. Write '1' or Read the ICIVR (as 001) will clear it.

4.10.5 MSS_I2Cn_ICCLKL Registers

4.10.5.1 I2Cn_ICCLKL Register (Offset = Ch) [reset = h]

Short Description: I2C Clock Divider Low register

Long Description:

Return to Summary Table

Table 4-1160. Instance Table

Instance Name	Physical Address
I2C0	5250 000Ch
I2C1	5250 100Ch
I2C2	5250 200Ch
I2C3	5250 300Ch

Access Types Legend

Table 4-1161. ICCLKL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU	RW	0h	Reserved
15 - 0	ICCL15_ICCL0	RW	0h	Low time I 2 C SCL Clock Division Factor. They are used to divide down the master clock to create the SCL low time transition frequency. This register must be configured while the I2C is still in reset (IRS_=0).

4.10.6 MSS_I2Cn_ICCLKH Registers

4.10.6.1 I2Cn_ICCLKH Register (Offset = 10h) [reset = h]

Short Description: I2C Clock Divider High register

Long Description:

Return to Summary Table

Table 4-1162. Instance Table

Instance Name	Physical Address
I2C0	5250 0010h
I2C1	5250 1010h
I2C2	5250 2010h
I2C3	5250 3010h

Access Types Legend

Table 4-1163. ICCLKH Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU	RW	0h	Reserved
15 - 0	ICCH15_ICCLH0	RW	0h	High time I 2 C SCL Clock Division Factor. They are used to divide down the master clock to create the SCL high time transition frequency. This register must be configured while the I2C is still in reset (IRS_=0).

4.10.7 MSS_I2Cn_ICCNT Registers

4.10.7.1 I2Cn_ICCNT Register (Offset = 14h) [reset = h]

Short Description: I2C Data Count register

Long Description:

Return to Summary Table

Table 4-1164. Instance Table

Instance Name	Physical Address
I2C0	5250 0014h
I2C1	5250 1014h
I2C2	5250 2014h
I2C3	5250 3014h

Access Types Legend

Table 4-1165. ICCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU	RW	0h	Reserved
15 - 0	ICDC15_ICDC0	RW	0h	Data count. This data count register is used to generate a Stop condition if a Stop condition is specified (STP=1). . ICCNT=1 data count is 1 :: :: ICCNT=0FFFFh data count is 65535 ICCNT=0data counter is 65536 Note that ICCNT is a don"t care when RM is set to 1.

4.10.8 MSS_I2Cn_ICDRR Registers

4.10.8.1 I2Cn_ICDRR Register (Offset = 18h) [reset = h]

Short Description: I2C Data Receive register

Long Description:

Return to Summary Table

Table 4-1166. Instance Table

Instance Name	Physical Address
I2C0	5250 0018h
I2C1	5250 1018h
I2C2	5250 2018h
I2C3	5250 3018h

Access Types Legend

Table 4-1167. ICDRR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	NU	RW	0h	Reserved
7 - 0	D7_D0	RW	0h	Receive data

4.10.9 MSS_I2Cn_ICSAR Registers

4.10.9.1 I2Cn_ICSAR Register (Offset = 1Ch) [reset = h]

Short Description: I2C Slave Address register

Long Description:

Return to Summary Table

Table 4-1168. Instance Table

Instance Name	Physical Address
I2C0	5250 001Ch
I2C1	5250 101Ch
I2C2	5250 201Ch
I2C3	5250 301Ch

Access Types Legend

Table 4-1169. ICSAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 10	NU	RW	0h	Reserved
9 - 0	A9_A0	RW	0h	Slave address. Use in both 7- and 10-bit address mode.

4.10.10 MSS_I2Cn_ICDXR Registers

4.10.10.1 I2Cn_ICDXR Register (Offset = 20h) [reset = h]

Short Description: I2C Data Transmit register

Long Description:

Return to Summary Table

Table 4-1170. Instance Table

Instance Name	Physical Address
I2C0	5250 0020h
I2C1	5250 1020h
I2C2	5250 2020h
I2C3	5250 3020h

Access Types Legend

Table 4-1171. ICDXR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	NU	RW	0h	Reserved
7 - 0	D7_D0	RW	0h	Transmit data

4.10.11 MSS_I2Cn_ICMDR Registers

4.10.11.1 I2Cn_ICMDR Register (Offset = 24h) [reset = h]

Short Description: I2C Mode register

Long Description:

Return to Summary Table

Table 4-1172. Instance Table

Instance Name	Physical Address
I2C0	5250 0024h
I2C1	5250 1024h
I2C2	5250 2024h
I2C3	5250 3024h

Access Types Legend

Table 4-1173. ICMDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU2	RW	0h	Reserved
15	NACKMOD	RW	0h	No Acknowledge (NACK) mode. This bit is used to send an Acknowledge (ACK) or a No Acknowledge (NACK) to the transmitter. This bit is only applicable when the I2C is in receiver mode. In master receiver mode when the internal data count counter decrements to zero the I2C sends a NACK. The master receiver I2C finishes a transfer when it sends a NACK. The I2C ignores ICCNT when NACKMOD is '1'. The NACKMOD bit should be set before the rising edge of the last data bit (bit 8) if a NACK must be sent and this bit is cleared once a NACK has been sent. NACKMOD=0 the I2C sends an ACK to the transmitter during the acknowledge cycle. NACKMOD=1 the I2C sends a NACK to the transmitter during the acknowledge cycle.
14	FREE	RW	0h	Free Running. This bit is used to determine the state of the I2C when a breakpoint is encountered in the HLL debugger. FREE=0: (default) Stops immediately if SCL is low and keep driving SCL low whether I2C is master transmitter/receiver. If SCL is high I2C waits until SCL becomes low and then stops. If the I2C is a slave it will stop when the transmission/receiving completes. FREE=1: The I2C runs free.
13	STT	RW	0h	Start Condition (Master only mode). This bit can be set to a"1" by the CPU to generate a Start condition. In master mode when setting Start to"1" generates a Start condition. It is reset to "0" by the hardware after the Start condition has been generated. The Start/ Stop bits can be configured to generate different transfer formats. Note that the STT and STP can be used to terminate the repeat mode. ST T STP Conditions Bus Activities 1 0 Start S-A-D 0 1 Stop P 1 1 Start-Stop (ICCNT= n) S-A-D..(n)..D-P 1 0 Start (ICCNT= n) S-A-D..(n)..D
12	NU1	RW	0h	Reserved for IDLEEN (IDLE Enable on 5509). - (RW)
11	STP	RW	0h	Stop Condition (Master mode only). This bit can be set to a"1" by the CPU to generate a Stop condition. It is reset to "0" by the hardware after the Stop condition has been generated. The Stop condition is generated when ICCNT passes 0 when the I2C is in non-repeat mode(RM=0).

Table 4-1173. ICMDR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	MST	RW	0h	Master. MST=0: The I 2 C peripheral is in the"slave" mode and clock is received from the"master" device. MST=1: The I 2 C peripheral is in the"master" mode and it generates the clock. This bit is clear when the transfer completed.
9	TRX	RW	0h	Transmitter. TRX=0: The I 2 C is in the"receiver" mode and data on data line SDA is shifted into the data register ICDRR. TRX=1: The I 2 C is in the"transmitter" mode and the data in ICDXR is shifted out on data line SDA. The operating modes (not in FDF mode) are defined as follows. In FDF mode TRX must be configured even if the I2C is in slave mode because there is no address/direction byte in FDF mode. _____MST___TRX___Operating Modes _0_____x_____"slave receiver" _0_____x_____"slave transmitter" _1_____0_____"master receiver" _1_____1_____"master transmitter" _____
8	XA	RW	0h	Expanded Address. XA=0: (default) 7-bit address mode (normal address mode). XA=1: 10-bit address mode (expanded address mode) Please note that XA needs to be configured even if the I2C is in slave mode.
7	RM	RW	0h	Repeat Mode. This bit is set to a"1" by the CPU to put the I2C in the repeat mode. In this mode data is continuously transmitted out of the ICDXR until the STP bit is set to"1" regardless of ICCNT value. This bit is don"t care if the I2C is configured in slave mode. _____ __RM___STT___STP___Conditions_____Bus Activities_____Mode _0_____0_____0_____Idle_____None_____NA _0_____0_____1_____Stop_____P_____NA _0_____1_____0_____(Re)Start_____S-A-D..(n)..D____Repeat n _0_____1_____1_____(Re)Start-Stop___S-A-D..(n)..D-P__Repeat n _1_____0_____0_____Idle_____none_____NA _1_____0_____1_____Stop_____P _____NA _1_____1_____0_____(Re)Start_____S-A-D-D-D..____Continuous _1_____1_____1_____Reserved_____None_____NA _____ __
6	DLB	RW	0h	Digital Loop Back (in master transmit mode only). This bit is set to a"1" by the CPU to put the I2C in the loop back mode. In this mode data transmitted out of the ICDXR will be received in the ICDRR after ((CPU freq/I2C freq)8) CPU cycles via an internal path. The address of the ICOAR is output on SDA.
5	IRS	RW	0h	I2C Reset Not. This can be set to a"0" by the CPU to put the I2C in reset or to a"1" to take the I2C out of reset. When this bit is reset to 0 all status bits in ICSTR and ICIVR are set to default values. Note that if this bit is reset during a transfer it can cause the I2C bus hang (SDA and SCL are tri-stated).
4	STB	RW	0h	Start Byte (Master only mode). The Start Byte mode bit is set to 1 by the CPU to configure the I2C in Start byte mode the I2C sends "00000001"? regardless ICSAR value. Refer to the Philip I2C spec for more details.
3	FDF	RW	0h	Free Data Format. This bit can be set to"1" by the CPU to configure the I2C in Free Data Format mode. _____FDF___M ST___TRX_____Operating mode _0_____0_____ x____Slave in non FDF mode _0_____1_____0____Master receive in non FDF mode _0_____1_____1____Master transmit in non FDF mode _1_____0_____0____Slave receiver in FDF mode _1_____0_____1____Slave transmitter in FDF mode _1_____1_____0____Master receiver in FDF mode _1_____1_____1____Master transmitter in FDF mode _____

Table 4-1173. ICMDR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2 - 0	BC2_BC1_BC0	RW	0h	Bit Count : Bit Count 2, Bit Count 1 and Bit Count 0 define the number of bits starting from the lsb (excluding the acknowledge bit) of the next byte which are yet to be received or transmitted. BC2_BC1_BC0 Bits/byte in FDF Bits/byte w/ ACK 0 0 0 8 9 0 0 1 1 NA (reserved) 0 1 0 2 3 0 1 1 3 4 1 0 0 4 5 1 0 1 5 6 1 1 0 6 7 1 1 1 7 8 NA (reserved)

4.10.12 MSS_I2Cn_ICIVR Registers

4.10.12.1 I2Cn_ICIVR Register (Offset = 28h) [reset = h]

Short Description: I2C Interrupt Vector register

Long Description:

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Table 4-1174. Instance Table

Instance Name	Physical Address
I2C0	5250 0028h
I2C1	5250 1028h
I2C2	5250 2028h
I2C3	5250 3028h

Access Types Legend

Table 4-1175. ICIVR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 12	NU2	RW	0h	Reserved.
11 - 8	TESTMD	RW	0h	Reserved for internal testing.
7 - 3	NU1	RW	0h	Reserved.
2 - 0	INTCODE	RW	0h	Interrupt code. The binary-coded-interrupt vector indicates which interrupt has occurred. Reading the ICIVR clears the interrupt code except ARDY(011) RRDY(100) and XRDY(101). Interrupt code for ARDY RRDY and XRDY is cleared when ARDY ICRRDY and ICXRDY bits in the ICSTR is cleared to default value respectively. If other interrupts are pending a new interrupt is generated. If there are more than one interrupt flag reading the ICIVR clears the highest priority interrupt code. Reading the ICIVR also clears corresponding status bit in the ICSTR except ARDY ICRRDY ICXRDY and AAS. Note that users must read (clear) the ICIVR before doing another start otherwise the ICIVR could contain incorrect (old interrupt flags) value. Interrupt Code Interrupt Occurred 000 (default) None 001 (highest priority) Arbitration Lost interrupt 010 No Acknowledgement interrupt 011 Register Access Ready interrupt 100 Receive Data Ready interrupt 101 Transmit Data Ready interrupt 110 Stop Condition Detection 111 (lowest priority) Address As Slave - (RW)

4.10.13 MSS_I2Cn_ICEMDR Registers

4.10.13.1 I2Cn_ICEMDR Register (Offset = 2Ch) [reset = h]

Short Description: I2C Extended Mode register

Long Description:

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Table 4-1176. Instance Table

Instance Name	Physical Address
I2C0	5250 002Ch
I2C1	5250 102Ch
I2C2	5250 202Ch
I2C3	5250 302Ch

Access Types Legend

Table 4-1177. ICEMDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU	RW	0h	Reserved. - (RW)
1	IGNACK	RW	0h	Ignore NACK mode IGNACK=0 The master transmitter will operate normally discontinue the data transfer and set the ARDY and NACK status bits when a NACK signal is received from the slave. IGNACK=1 The master transmitter will ignore a NACK received from the slave.
0	BCM	RW	0h	Backward Compatibility Mode. This bit affects the I2C interrupt behavior.

4.10.14 MSS_I2Cn_ICPSC Registers

4.10.14.1 I2Cn_ICPSC Register (Offset = 30h) [reset = h]

Short Description: I2C Prescaler register

Long Description:

Return to Summary Table

Table 4-1178. Instance Table

Instance Name	Physical Address
I2C0	5250 0030h
I2C1	5250 1030h
I2C2	5250 2030h
I2C3	5250 3030h

Access Types Legend

Table 4-1179. ICPSC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	NU	RW	0h	Reserved.
7 - 0	IPSC7_IPSC0	RW	0h	8-bit prescaler to divide the system clock down to 4/8/12Mhz clock and used by the I2C module. This register must be initialized while the I2C is still in reset (IRS_=0). The value takes effect on the rising edge of IRS_.

4.10.15 MSS_I2Cn_ICPID1 Registers

4.10.15.1 I2Cn_ICPID1 Register (Offset = 34h) [reset = h]

Short Description: I2C Peripheral ID register 1

Long Description:

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Table 4-1180. Instance Table

Instance Name	Physical Address
I2C0	5250 0034h
I2C1	5250 1034h
I2C2	5250 2034h
I2C3	5250 3034h

Access Types Legend

Table 4-1181. ICPID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU	RW	0h	Reserved.
15 - 8	CLASS	RW	0h	Identifies the class of peripheral. This value should be 0x01 - (RW)
7 - 0	REVISION	RW	0h	Identifies the revision level of the I2C. This value should be incremented each time the design is revised. - (RW)

4.10.16 MSS_I2Cn_ICPID2 Registers

4.10.16.1 I2Cn_ICPID2 Register (Offset = 38h) [reset = h]

Short Description: I2C Peripheral ID register 2

Long Description:

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Table 4-1182. Instance Table

Instance Name	Physical Address
I2C0	5250 0038h
I2C1	5250 1038h
I2C2	5250 2038h
I2C3	5250 3038h

Access Types Legend

Table 4-1183. ICPID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	NU	RW	0h	Reserved.
7 - 0	TYPE	RW	0h	Identifies the type of peripheral. This value should be 0x05 - (RW)

4.10.17 MSS_I2Cn_ICDMAC Registers

4.10.17.1 I2Cn_ICDMAC Register (Offset = 3Ch) [reset = h]

Short Description: I2C DMA Control Register

Long Description:

Return to Summary Table

Table 4-1184. Instance Table

Instance Name	Physical Address
I2C0	5250 003Ch
I2C1	5250 103Ch
I2C2	5250 203Ch
I2C3	5250 303Ch

Access Types Legend

Table 4-1185. ICDMAC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU	RW	0h	Reserved. - (RW)
1	TXDMAEN	RW	0h	Transmit DMA enable. This bit controls the receive DMA event pin to the system. When this bit is 1 the DMA event is enabled and ICTEVT_POR pin is asserted when the DMA transfer is required. When this bit is 0 the ICTEVT_POR pin is never asserted. RXDMAEN=0: DMA transmit event is disabled. RXDMAEN=1: DMA transmit event is enabled. (Default)
0	RXDMAEN	RW	0h	Receive DMA enable. This bit controls the receive DMA event pin to the system. When this bit is 1 the DMA event is enabled and ICREVT_POR pin is asserted when the DMA transfer is required. When this bit is 0 the ICREVT_POR pin is never asserted. RXDMAEN=0: DMA receive event is disabled. RXDMAEN=1: DMA receive event is enabled. (Default)

4.10.18 MSS_I2Cn_I2C_RESERVED1 Registers

4.10.18.1 I2Cn_RESERVED1 Register (Offset = 40h) [reset = h]

Short Description: Reserved

Long Description:

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Table 4-1186. Instance Table

Instance Name	Physical Address
I2C0	5250 0040h
I2C1	5250 1040h
I2C2	5250 2040h
I2C3	5250 3040h

Access Types Legend

Table 4-1187. I2C_RESERVED1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU	RW	0h	Reserved.

4.10.19 MSS_I2Cn_I2C_RESERVED2 Registers

4.10.19.1 I2Cn_RESERVED2 Register (Offset = 44h) [reset = h]

Short Description: Reserved

Long Description:

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Table 4-1188. Instance Table

Instance Name	Physical Address
I2C0	5250 0044h
I2C1	5250 1044h
I2C2	5250 2044h
I2C3	5250 3044h

Access Types Legend

Table 4-1189. I2C_RESERVED2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU	RW	0h	Reserved.

4.10.20 MSS_I2Cn_ICPFUNC Registers

4.10.20.1 I2Cn_ICPFUNC Register (Offset = 48h) [reset = h]

Short Description: I2C Pin Function register

Long Description:

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Table 4-1190. Instance Table

Instance Name	Physical Address
I2C0	5250 0048h
I2C1	5250 1048h
I2C2	5250 2048h
I2C3	5250 3048h

Access Types Legend

Table 4-1191. ICPFUNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU	RW	0h	Reserved.
0	PFUNC0	RW	0h	Controls the function of the I2C SCL and SDA pins. 0 = Pins function as SCL and SDA 1 = Pins functions as GPIO Note: No hardware protection is required to disable I2C function when the PFUNC[0] and IRS_ bits are both set to one. When PFUNC[0] is"1" (GPIO mode) the sub-module which controls the I2C function receives the value"1" for SCL and SDA. IRS_ can be set to"1" regardless of PFUNC[0] and the I2C function works whenever the IRS_ bit is"1". The user is expected to hold I2C in reset via IRS_ bit when changing to/from GPIO mode via the PFUNC[0] bit.

4.10.21 MSS_I2Cn_ICPDIR Registers

4.10.21.1 I2Cn_ICPDIR Register (Offset = 4Ch) [reset = h]

Short Description: I2C Pin Direction register

Long Description:

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Table 4-1192. Instance Table

Instance Name	Physical Address
I2C0	5250 004Ch
I2C1	5250 104Ch
I2C2	5250 204Ch
I2C3	5250 304Ch

Access Types Legend

Table 4-1193. ICPDIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU	RW	0h	Reserved
1	PDIR1	RW	0h	Controls the direction of the I2C SDA pin when configured as GPIO. 0 = SDA pin functions as input 1 = SDA pin functions as output
0	PDIR0	RW	0h	Controls the direction of the I2C SCL pin when configured as GPIO. 0 = SCL pin functions as input 1 = SCL pin functions as output

4.10.22 MSS_I2Cn_ICPDIN Registers

4.10.22.1 I2Cn_ICPDIN Register (Offset = 50h) [reset = h]

Short Description: I2C Pin Data In register

Long Description:

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Table 4-1194. Instance Table

Instance Name	Physical Address
I2C0	5250 0050h
I2C1	5250 1050h
I2C2	5250 2050h
I2C3	5250 3050h

Access Types Legend

Table 4-1195. ICPDIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU	RW	0h	Reserved
1	PDIN1	RW	0h	Indicates the logic level present on the SDA pin. Reads: 0 = Logic low present at SDA pin regardless of PFUNC setting. 1 = Logic high present at SDA pin regardless of PFUNC setting. Writes: Writes have no effect. - (RW)
0	PDIN0	RW	0h	Indicates the logic level present on the SCL pin. Reads: 0 = Logic low present at SCL pin regardless of PFUNC setting. 1 = Logic high present at SCL pin regardless of PFUNC setting. Writes: Writes have no effect - (RW)

4.10.23 MSS_I2Cn_ICPDOUT Registers

4.10.23.1 I2Cn_ICPDOUT Register (Offset = 54h) [reset = h]

Short Description: I2C Pin Data Out register

Long Description:

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Table 4-1196. Instance Table

Instance Name	Physical Address
I2C0	5250 0054h
I2C1	5250 1054h
I2C2	5250 2054h
I2C3	5250 3054h

Access Types Legend

Table 4-1197. ICPDOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU	RW	0h	Reserved
1	PDOUT1	RW	0h	Controls the level driven on the SDA pin when configured as GPIO output. Reads: Reads return register values not GPIO pin levels. Writes: 0 = SDA pin driven low 1 = SDA pin driven high. Note: If SDA is connected to an open-drain buffer at the chiplevel the I2C cannot drive SDA to high.
0	PDOUT0	RW	0h	Controls the level driven on the SCL pin when configured as GPIO output. Reads: Reads return register values not GPIO pin levels. Writes: 0 = SCL pin driven low 1 = SCL pin driven high Note: If SCL is connected to an open-drain buffer at the chiplevel the I2C cannot drive SCL to high.

4.10.24 MSS_I2Cn_ICPDSET Registers

4.10.24.1 I2Cn_ICPDSET Register (Offset = 58h) [reset = h]

Short Description: I2C Pin Data Set register

Long Description:

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Table 4-1198. Instance Table

Instance Name	Physical Address
I2C0	5250 0058h
I2C1	5250 1058h
I2C2	5250 2058h
I2C3	5250 3058h

Access Types Legend

Table 4-1199. ICPDSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU	RW	0h	Reserved
1	PDSET1	RW	0h	Used to set PDOUT[1] bit which corresponds to the SDA GPIO pin. Reads: Reads should return 0. User documentation should say reads are indeterminate. Writes: 0 = no effect 1 = PDOUT[1] bit is set to logic high.
0	PDSET0	RW	0h	Used to set PDOUT[0] bit which corresponds to the SCL GPIO pin. Reads: Reads should return 0. User documentation should say reads are indeterminate. Writes: 0 = no effect 1 = PDOUT[0] bit is set to logic high.

4.10.25 MSS_I2Cn_ICPDCLR Registers

4.10.25.1 I2Cn_ICPDCLR Register (Offset = 5Ch) [reset = h]

Short Description: I2C Pin Data Clear register

Long Description:

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Table 4-1200. Instance Table

Instance Name	Physical Address
I2C0	5250 005Ch
I2C1	5250 105Ch
I2C2	5250 205Ch
I2C3	5250 305Ch

Access Types Legend

Table 4-1201. ICPDCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU	RW	0h	Reserved
1	PDCLR1	RW	0h	Used to clear PDOUT[1] bit which corresponds to the SDA pin. Reads: Reads should return 0. User documentation should say reads are indeterminate. Writes: 0 = no effect 1 = PDOUT[1] bit is cleared to logic low.
0	PDCLR0	RW	0h	Used to clear PDOUT[0] bit which corresponds to the SCL pin. Reads: Reads should return 0. User documentation should say reads are indeterminate. Writes: 0 = no effect 1 = PDOUT[0] bit is cleared to logic low.

4.10.26 MSS_I2Cn_ICPDRV Registers

4.10.26.1 I2Cn_ICPDRV Register (Offset = 60h) [reset = h]

Short Description: I2C Pin Driver Mode Register

Long Description:

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Table 4-1202. Instance Table

Instance Name	Physical Address
I2C0	5250 0060h
I2C1	5250 1060h
I2C2	5250 2060h
I2C3	5250 3060h

Access Types Legend

Table 4-1203. ICPDRV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU	RW	0h	Reserved
1	PDRV1	RW	0h	Used to select driver mode of output buffer for SDA pin. 0 = I2C mode. 1 = GPIO mode. Note: Value of this register is reflected on the PDRV_SDA_POR port. Actual function depends on I/O buffer and chip implementation.
0	PDRV0	RW	0h	Used to select driver mode of output buffer for SCL pin. 0 = I2C mode. 1 = GPIO mode. Note: Value of this register is reflected on the PDRV_SCL_POR port. Actual function depends on I/O buffer and chip implementation.

4.10.27 Access Table

Table 4-1204. Access Type Codes

Access Type	Code	Description
RW	RW	Read / Write

4.11 L2 Registers

Table 4-1205. MSS_L2 Registers Base Address Table

Offset	Length	Acronym	MSS_L2 Physical Address
0h	32	L2_START	7000 0000h
1FFFFCh	32	L2_END	701F FFFCh

4.11.1 MSS_L2_START Registers

4.11.1.1 L2_START Register (Offset = 0h) [reset = h]

Short Description: RW

Long Description:

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Table 4-1206. Instance Table

Instance Name	Physical Address
L2OCRAM	7000 0000h

Figure 4-525. MSS_L2_START Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START															
RW															
0															

Access Types Legend

Table 4-1207. START Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	START	RW	0h	L2 Memory start address

4.11.2 MSS_L2_END Registers

4.11.2.1 L2_END Register (Offset = 1FFFFCh) [reset = h]

Short Description: RW

Long Description:

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Table 4-1208. Instance Table

Instance Name	Physical Address
L2OCRAM	701F FFFCh

Figure 4-526. MSS_L2_END Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END															
RW															
0															

Access Types Legend

Table 4-1209. END Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	END	RW	0h	L2 Memory end address

4.11.3 Access Table

Table 4-1210. Access Type Codes

Access Type	Code	Description
RW	RW	Read / Write

4.12 MSS_LIN Registers

Table 4-1211. LIN, LIN Registers, Base Address=0X52400000, Length=2

Offset	Length	Register Name	LIN0 Physical Address	LIN1 Physical Address	LIN2 Physical Address
0h	32	SCIGCR0	5240 0000h	5240 1000h	5240 2000h
4h	32	SCIGCR1	5240 0004h	5240 1004h	5240 2004h
8h	32	SCIGCR2	5240 0008h	5240 1008h	5240 2008h
Ch	32	SCISETINT	5240 000Ch	5240 100Ch	5240 200Ch
10h	32	SCICLEARINT	5240 0010h	5240 1010h	5240 2010h
14h	32	SCISETINTLVL	5240 0014h	5240 1014h	5240 2014h
18h	32	SCICLEARINTLVL	5240 0018h	5240 1018h	5240 2018h
1Ch	32	SCIFLR	5240 001Ch	5240 101Ch	5240 201Ch
20h	32	SCIINTVECT0	5240 0020h	5240 1020h	5240 2020h
24h	32	SCIINTVECT1	5240 0024h	5240 1024h	5240 2024h
28h	32	SCIFORMAT	5240 0028h	5240 1028h	5240 2028h
2Ch	32	BRSR	5240 002Ch	5240 102Ch	5240 202Ch
30h	32	SCIED	5240 0030h	5240 1030h	5240 2030h
34h	32	SCIRD	5240 0034h	5240 1034h	5240 2034h
38h	32	SCITD	5240 0038h	5240 1038h	5240 2038h
3Ch	32	SCIPIO0	5240 003Ch	5240 103Ch	5240 203Ch
40h	32	SCIPIO1	5240 0040h	5240 1040h	5240 2040h
44h	32	SCIPIO2	5240 0044h	5240 1044h	5240 2044h
48h	32	SCIPIO3	5240 0048h	5240 1048h	5240 2048h
4Ch	32	SCIPIO4	5240 004Ch	5240 104Ch	5240 204Ch
50h	32	SCIPIO5	5240 0050h	5240 1050h	5240 2050h
54h	32	SCIPIO6	5240 0054h	5240 1054h	5240 2054h
58h	32	SCIPIO7	5240 0058h	5240 1058h	5240 2058h
5Ch	32	SCIPIO8	5240 005Ch	5240 105Ch	5240 205Ch
60h	32	LINCOMP	5240 0060h	5240 1060h	5240 2060h
64h	32	LINRD0	5240 0064h	5240 1064h	5240 2064h
68h	32	LINRD1	5240 0068h	5240 1068h	5240 2068h
6Ch	32	LINMASK	5240 006Ch	5240 106Ch	5240 206Ch
70h	32	LINID	5240 0070h	5240 1070h	5240 2070h
74h	32	LINTD0	5240 0074h	5240 1074h	5240 2074h
78h	32	LINTD1	5240 0078h	5240 1078h	5240 2078h
7Ch	32	MBRSR	5240 007Ch	5240 107Ch	5240 207Ch
80h + Formula	32	Reserved_N	5240 0080h + Formula	5240 1080h + Formula	5240 2080h + Formula
90h	32	IODFTCTRL	5240 0090h	5240 1090h	5240 2090h
94h + Formula	32	Reserved_N	5240 0094h + Formula	5240 1094h + Formula	5240 2094h + Formula
E0h	32	LIN_GLB_INT_EN	5240 00E0h	5240 10E0h	5240 20E0h
E4h	32	LIN_GLB_INT_FLG	5240 00E4h	5240 10E4h	5240 20E4h
E8h	32	LIN_GLB_INT_CLR	5240 00E8h	5240 10E8h	5240 20E8h

Table 4-1212. LIN, LIN Registers, Base Address=0X52400000, Length=2

Offset	Length	Register Name	LIN3 Physical Address	LIN4 Physical Address
0h	32	SCIGCR0	5240 3000h	5240 4000h
4h	32	SCIGCR1	5240 3004h	5240 4004h
8h	32	SCIGCR2	5240 3008h	5240 4008h
Ch	32	SCISETINT	5240 300Ch	5240 400Ch
10h	32	SCICLEARINT	5240 3010h	5240 4010h
14h	32	SCISETINTLVL	5240 3014h	5240 4014h
18h	32	SCICLEARINTLVL	5240 3018h	5240 4018h
1Ch	32	SCIFLR	5240 301Ch	5240 401Ch
20h	32	SCIINTVECT0	5240 3020h	5240 4020h
24h	32	SCIINTVECT1	5240 3024h	5240 4024h
28h	32	SCIFORMAT	5240 3028h	5240 4028h
2Ch	32	BRSR	5240 302Ch	5240 402Ch
30h	32	SCIED	5240 3030h	5240 4030h
34h	32	SCIRD	5240 3034h	5240 4034h
38h	32	SCITD	5240 3038h	5240 4038h
3Ch	32	SCIPIO0	5240 303Ch	5240 403Ch
40h	32	SCIPIO1	5240 3040h	5240 4040h
44h	32	SCIPIO2	5240 3044h	5240 4044h
48h	32	SCIPIO3	5240 3048h	5240 4048h
4Ch	32	SCIPIO4	5240 304Ch	5240 404Ch
50h	32	SCIPIO5	5240 3050h	5240 4050h
54h	32	SCIPIO6	5240 3054h	5240 4054h
58h	32	SCIPIO7	5240 3058h	5240 4058h
5Ch	32	SCIPIO8	5240 305Ch	5240 405Ch
60h	32	LINCOMP	5240 3060h	5240 4060h
64h	32	LINRD0	5240 3064h	5240 4064h
68h	32	LINRD1	5240 3068h	5240 4068h
6Ch	32	LINMASK	5240 306Ch	5240 406Ch
70h	32	LINID	5240 3070h	5240 4070h
74h	32	LINTD0	5240 3074h	5240 4074h
78h	32	LINTD1	5240 3078h	5240 4078h
7Ch	32	MBRSR	5240 307Ch	5240 407Ch
80h + Formula	32	Reserved_N	5240 3080h + Formula	5240 4080h + Formula
90h	32	IODFTCTRL	5240 3090h	5240 4090h
94h + Formula	32	Reserved_N	5240 3094h + Formula	5240 4094h + Formula
E0h	32	LIN_GLB_INT_EN	5240 30E0h	5240 40E0h
E4h	32	LIN_GLB_INT_FLG	5240 30E4h	5240 40E4h
E8h	32	LIN_GLB_INT_CLR	5240 30E8h	5240 40E8h

4.12.1 LIN_SCIGCR0 Registers

4.12.1.1 LIN_SCIGCR0 Register (Offset = 0h) [reset = 0h]

Short Description: The SCIGCR0 register defi

Long Description: The SCIGCR0 register defines the module reset.

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Table 4-1213. Instance Table

Instance Name	Physical Address
LIN0	5240 0000h
LIN1	5240 1000h
LIN2	5240 2000h
LIN3	5240 3000h
LIN4	5240 4000h

Figure 4-527. SCIGCR0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_2															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1															RESET
R															R/W
0h															0h

Access Types Legend

Table 4-1214. SCIGCR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_2	R	0h	Reserved
15:1	RESERVED_1	R	0h	Reserved
0	RESET	R/W	0h	This bit resets the SCI/LIN module. This bit is effective in LIN or SCI-compatible mode.. This bit affects the reset state of the SCI/LIN module. 1 RESET_OFF SCI/LIN module is out of reset.

4.12.2 LIN_SCIGCR1 Registers

4.12.2.1 LIN_SCIGCR1 Register (Offset = 4h) [reset = 0h]

Short Description: The SCIGCR1 register defi

Long Description: The SCIGCR1 register defines the frame format, protocol, and communication mode used by the SCI.

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Table 4-1215. Instance Table

Instance Name	Physical Address
LIN0	5240 0004h
LIN1	5240 1004h
LIN2	5240 2004h
LIN3	5240 3004h
LIN4	5240 4004h

Figure 4-528. SCIGCR1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3						TXENA	RXENA	RESERVED_2						CONT	LOOPBACK
R						R/W	R/W	R						R/W	R/W
0h						0h	0h	0h						0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1		STOPEXTFRAME	HGENCTRL	CTYPE	MBUFMODE	ADAPT	SLEEP	SWNRST	LINMODE	CLK_MASTER	STOP	PARITY	PARITYENA	TIMINGMODE	COMMMODE
R		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-1216. SCIGCR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED_3	R	0h	Reserved
25	TXENA	R/W	0h	Transmit enable. This bit is effective in LIN and SCI modes. Data is transferred from SCITD or the TDy [with y=0, 1,...7] buffers in LIN mode to the SCITXSHF shift out register only when the TXENA bit is set. Note: Data written to SCITD or the transmit multi-buffer before TXENA is set is not transmitted. If TXENA is cleared while transmission is ongoing, the data previously written to SCITD is sent [including the checksum byte in LIN mode]. 1 TXENA_ENABLE Enable transfers of data from SCITD or TDy to SCITXSHF

Table 4-1216. SCIGCR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	RXENA	R/W	0h	Receive enable. This bit is effective in LIN or SCI-compatible mode. RXENA allows or prevents the transfer of data from SCIRXSHF to SCIRD or the receive multibuffers. Note: Clearing RXENA stops received characters from being transferred into the receive buffer or multi-buffers, prevents the RX status flags [see Table 7] from being updated by receive data, and inhibits both receive and error interrupts. However, the shift register continues to assemble data regardless of the state of RXENA. Note: If RXENA is cleared before the time the reception of a frame is complete, the data from the frame is not transferred into the receive buffer. Note: If RXENA is set before the time the reception of a frame is complete, the data from the frame is transferred into the receive buffer. If RXENA is set while SCIRXSHF is in the process of assembling a frame, the status flags are not guaranteed to be accurate for that frame. To ensure that the status flags correctly reflect what was detected on the bus during a particular frame, RXENA should be set before the detection of that frame 1 RXENA_RUN Allows the receiver to transfer data from the shift buffer to the receive buffer or multi-buffers
23:18	RESERVED_2	R	0h	Reserved
17	CONT	R/W	0h	Continue on suspend. This bit has an effect only when a program is being debugged with an emulator, and it determines how the SCI/LIN operates when the program is suspended. This bit affects the LIN counters. When this bit is set, the counters are not stopped during debug. When this bit is cleared, the counters are stopped during debug. 1 CONT_RUN When debug mode is entered, the SCI/LIN continues to operate until the current transmit and receive functions are complete.
16	LOOPBACK	R/W	0h	Loopback bit. This bit is effective in LIN or SCI-compatible mode. The self-checking option for the SCI/LIN can be selected with this bit. If the LINTX and LINRX pins are configured with SCI/LIN functionality, then the LINTX pin is internally connected to the LINRX pin. Externally, during loop back operation, the LINTX pin outputs a high value and the LINRX pin is in a high-impedance state. If this bit value is changed while the SCI/LIN is transmitting or receiving data, errors may result. 1 LOOPBACK_ENABLE Loopback mode is enabled.
15:14	RESERVED_1	R	0h	Reserved
13	STOPEXTFRAME	R/W	0h	Stop extended frame communication. This bit is effective in LIN mode only. This bit can be written only during extended frame communication. When the extended frame communication is stopped, this bit is cleared automatically. 1 STOPEXTFRAME_EFFECT Extended frame communication will be stopped, once current frame transmission/reception is completed.
12	HGENCTRL	R/W	0h	HGEN control bit. This bit is effective in LIN mode only. This bit controls the type of mask filtering comparison. 1 HGENCTRL_IDSLAVE ID filtering using ID- SlaveTask byte (Recommended). RECEIVEDID and IDSLAVETASKBYTE fields in the LINID register are used for detecting a match (using TX/RXMASK values). Mask of 0xFF in LINMASK register will result in ALWAYS match
11	CTYPE	R/W	0h	Checksum type. This bit is effective in LIN mode only. This bit controls the type of checksum to be used: classic or enhanced. 1 CTYPE_ENHANCED Enhanced checksum is used. The enhanced checksum is compatible with LIN 2.0 and newer slave nodes. The enhanced checksum contains the modulo-256 sum with carry over all data bytes AND the protected Identifier.
10	MBUFMODE	R/W	0h	Multibuffer mode. This bit is effective in LIN or SCI-compatible mode. This bit controls receive/transmit buffer usage, that is, whether the RX/TX multibuffers are used or a single register, RD0/TD0, is used. 1 MBUFMODE_ENABLED The multi-buffer mode is enabled.

Table 4-1216. SCIGCR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	ADAPT	R/W	0h	Adapt mode enable. This mode is effective in LIN mode only. This bit has an effect during the detection of the Sync Field. There are two LIN protocol bit rate modes that could be enabled with this bit according to the Node capability file definition: automatic or select. Software and network configuration will decide which of the previous two modes. When this bit is cleared, the LIN 2.0 protocol fixed bit rate should be used. If the ADAPT bit is set, a LIN slave node detecting the baudrate will compare it to the prescalers in BRSR register and update it if they are different. The BRSR register will be updated with the new value. If this bit is not set there will be no adjustment to the BRSR register. This field is writable in LIN mode only. 1 ADAPT_ENABLE Automatic baudrate adjustment is enabled.
8	SLEEP	R/W	0h	SCI sleep. SCI compatibility mode only. In a multiprocessor configuration, this bit controls the receive sleep function. Clearing this bit brings the SCI out of sleep mode. The receiver still operates when the SLEEP bit is set; however, RXRDY is updated and SCIRD is loaded with new data only when an address frame is detected. The remaining receiver status flags are updated and an error interrupt is requested if the corresponding interrupt enable bit is set, regardless of the value of the SLEEP bit. In this way, if an error is detected on the receive data line while the SCI is asleep, software can promptly deal with the error condition. The SLEEP bit is not automatically cleared when an address byte is detected. This field is writable in SCI mode only. 1 SLEEP_ENABLE Sleep mode is enabled.
7	SWNRST	R/W	0h	Software reset [active low]. This bit is effective in LIN or SCI-compatible mode. The SCI/LIN should only be configured while SWnRST = 0. Only the following configuration bits can be changed in runtime [i.e., while SWnRESET = 1]: - STOP EXT Frame [SCIGCR1[13]] - CC bit [SCIGCR2[17]] - SC bit [SCIGCR2[16]] 1 SWnRST_READY The SCI/LIN is in its ready state; transmission and reception can occur. After this bit is set to 1, the configuration of the module should not change.
6	LINMODE	R/W	0h	LIN mode This bit controls the mode of operation of the module. 1 LINMODE_ENABLE LIN mode is enabled; SCI compatibility mode is disabled.
5	CLK_MASTER	R/W	0h	SCI internal clock enable or LIN Master/Slave configuration. In the SCI mode, this bit enables the clock to the SCI module. In LIN mode, this bit determines whether a LIN node is a slave or master. 1 CLK_MASTER_ON SCI-compatible mode: Enable clock to the SCI module. LIN mode: The node is in master mode.
4	STOP	R/W	0h	SCI number of stop bits. This bit is effective in SCI-compatible mode only. Note: The receiver checks for only one stop bit. However in idle-line mode, the receiver waits until the end of the second stop bit [if STOP = 1] to begin checking for an idle period. This field is writable in SCI mode only. 1 STOP_TWO Two stop bits are used.
3	PARITY	R/W	0h	SCI parity odd/even selection. This bit is effective in SCI-compatible mode only. If the PARITY ENA bit [SCIGCR1.2] is set, PARITY designates odd or even parity. The parity bit is calculated based on the data bits in each frame and the address bit [in address-bit mode]. The start and stop fields in the frame are not included in the parity calculation. This field is writable in SCI mode only. 1 PARITY_EVEN Even parity is used. The SCI transmits and expects to receive a value in the parity bit that makes even the total number of bits in the frame with the value of 1.
2	PARITYENA	R/W	0h	Parity enable. Enables or disables the parity function. 1 PARITYENA_ENABLE SCI compatible mode: Parity enabled. A parity bit is generated during transmission and is expected during reception. LIN mode: ID- parity verification is enabled.
1	TIMINGMODE	R/W	0h	SCI timing mode bit. This bit is effective in SCI-compatible mode only. It must be set to 1 when the SCI mode is used. This bit configures the SCI for asynchronous operation. 1 TIMINGMODE_SET Must be set to 1 when module is configured for SCI operation

Table 4-1216. SCIGCR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	COMMMODE	R/W	0h	SCI/LIN communication mode bit. In compatibility mode, it selects the SCI communication mode. In LIN mode it selects length control option for ID-field bits ID4 and ID5. 1 COMMMODE_USE SCI-compatible mode: Address- bit mode is used. LIN mode: ID4 and ID5 are used for length control.

4.12.3 LIN_SCIGCR2 Registers

4.12.3.1 LIN_SCIGCR2 Register (Offset = 8h) [reset = 0h]

Short Description: The SCIGCR2 register is u

Long Description: The SCIGCR2 register is used to send or compare a checksum byte during extended frames, to generate a wakeup and for low-power mode control of the LIN module.

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Table 4-1217. Instance Table

Instance Name	Physical Address
LIN0	5240 0008h
LIN1	5240 1008h
LIN2	5240 2008h
LIN3	5240 3008h
LIN4	5240 4008h

Figure 4-529. SCIGCR2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3														CC	SC
R														R/W	R/W
0h														0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2							GENWU	RESERVED_1							POWERDOWN
R							R/W	R							R/W
0h							0h	0h							0h

Access Types Legend

Table 4-1218. SCIGCR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED_3	R	0h	Reserved
17	CC	R/W	0h	Compare Checksum. This mode is effective in LIN mode only. This bit is used by the receiver for extended frames to trigger a checksum compare. The user will initiate this transaction by writing a one to this bit. In non multibuffer mode, once the CC bit is set, the checksum will be compared on the byte that is currently being received, expected to be the checkbyte. During Multi-buffer mode, following are the scenarios associated with the CC bit : - If CC bit is set during the reception of the data, then the byte that is received after the reception of the programmed no. of data bytes indicated by SCIFORMAT[18:16], is treated as a checksum byte. - If CC bit is set during the IDLE period [i.e. during inter-frame space], then the next immediate byte will be treated as a checksum byte. A CE will immediatly be flagged if there is a checksum error. This bit is automatically cleared once the checksum is successfully compared. 1 CC_EFFECT Compare checksum on expected checkbyte
16	SC	R/W	0h	Send Checksum This mode is effective in LIN mode only. This bit is used by the transmitter with extended frames to send a checkbyte. In non multibuffer mode the checkbyte will be sent after the current byte transmission. In multibuffer mode the checkbyte will be sent after the last byte count, indicated by the SCIFORMAT[18:16]]. This field is writable in LIN mode only. 1 SC_CHECK A checkbyte will be sent. This bit will automatically get cleared after the checkbyte is transmitted. The checksum will not be sent if this bit is set before transmitting the very first byte, that is, during interframe space.

Table 4-1218. SCIGCR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:9	RESERVED_2	R	0h	Reserved
8	GENWU	R/W	0h	Generate wakeup signal. This bit controls the generation of a wakeup signal, by transmitting the TDO buffer value. This bit is cleared on reception of a valid sync break. 1 GENWU_EFFECT Transmit TDO for wakeup. This bit will be cleared on a SWnRST (SCIGCR1.7)
7:1	RESERVED_1	R	0h	Reserved
0	POWERDOWN	R/W	0h	Power down. This bit is effective in LIN or SCI-compatible mode. When the powerdown bit is set, the SCI/LIN module attempts to enter local low-power mode. If the POWERDOWN bit is set while the receiver is actively receiving data and the wakeup interrupt is disabled, then the SCI/LIN will delay low-power mode from being entered until completion of reception. In LIN mode the user may set the POWERDOWN bit on Sleep Command reception or on idle bus detection [more than 4 seconds, i.e. 80,000 cycles at 20kHz] 1 POWERDOWN_LOW Request local low-power mode

4.12.4 LIN_SCISETINT Registers

4.12.4.1 LIN_SCISETINT Register (Offset = Ch) [reset = 0h]

Short Description: The SCISETINT register is

Long Description: The SCISETINT register is used to enable the various interrupts available in the LIN module.

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Table 4-1219. Instance Table

Instance Name	Physical Address
LIN0	5240 000Ch
LIN1	5240 100Ch
LIN2	5240 200Ch
LIN3	5240 300Ch
LIN4	5240 400Ch

Figure 4-530. SCISETINT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SETBEINT	SETPBEINT	SETCEINT	SETISFEINT	SETNREINT	SETFEINT	SETOEINT	SETPEINT	RESERVED_5					SET_RX_DMA_ALL	SET_RX_DMA	SET_TX_DMA
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R					R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h	0h					0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_4		SETIDINT	RESERVED_3			SETRXINT	SETTXINT	SETTOA3WUSINT	SETTOAWUSINT	RESERVED_2	SETTIMEOUTINT	RESERVED_1		SETWAKEUPINT	SETBRKDTINT
R		R/W1TS	R			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R	R/W1TS	R		R/W1TS	R/W1TS
0h		0h	0h			0h	0h	0h	0h	0h	0h	0h		0h	0h

Access Types Legend

Table 4-1220. SCISETINT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SETBEINT	R/W1TS	0h	Set bit error interrupt. This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN module to generate an interrupt when there is a bit error. This field is writable in LIN mode only. 1 SETBEINT_ENABLE Interrupt is enabled.
30	SETPBEINT	R/W1TS	0h	Set physical bus error interrupt. This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN module to generate an interrupt when a physical bus error occurs. This field is writable in LIN mode only. 1 SETPBEINT_ENABLE Interrupt is enabled.
29	SETCEINT	R/W1TS	0h	Set checksum-error Interrupt. This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN module to generate an interrupt when there is a checksum error. This field is writable in LIN mode only. 1 SETCEINT_DEABLE Interrupt is enabled.
28	SETISFEINT	R/W1TS	0h	Set inconsistent-sync-field-error interrupt. This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN module to generate an interrupt when there is an inconsistent sync field error. This field is writable in LIN mode only. 1 SETISFEINT_ENABLE Interrupt is enabled.
27	SETNREINT	R/W1TS	0h	Set no-response-error interrupt. This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN module to generate an interrupt when a no-response error occurs. This field is writable in LIN mode only. 1 SETNREINT_ENABLE Interrupt is enabled.

Table 4-1220. SCISETINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	SETFEINT	R/W1TS	0h	Set framing-error interrupt. This bit is effective in LIN or SCI-compatible mode. Setting this bit enables the SCI/LIN module to generate an interrupt when a framing error occurs. 1 SETFEINT_ENABLE Interrupt is enabled.
25	SETOEINT	R/W1TS	0h	Set overrun-error interrupt. This bit is effective in LIN or SCI-compatible mode. Setting this bit enables the SCI/LIN module to generate an interrupt when an overrun error occurs. 1 SETOEINT_ENABLE Interrupt is enabled.
24	SETPEINT	R/W1TS	0h	Set parity interrupt. This bit is effective in LIN or SCI-compatible mode. Setting this bit enables the SCI/LIN module to generate an interrupt when a parity error occurs. 1 SETPEINT_ENABLE Interrupt is enabled.
23:19	RESERVED_5	R	0h	Reserved
18	SET_RX_DMA_ALL	R/W1TS	0h	Set receiver DMA for Address & Data frames. This bit is effective in LIN or SCI-compatible mode. To enable RX DMA request for address and data frames this bit must be set. If it is cleared, RX interrupt request is generated for address frames and DMA requests are generated for data frames. 1 SERXDMAALL_ENABLE Receiver DMA request is enabled for address and data frames
17	SET_RX_DMA	R/W1TS	0h	Set receiver DMA. This bit is effective in LIN or SCI-compatible mode. To enable DMA requests for the receiver this bit must be set. If it is cleared, interrupt requests are generated depending on SETRXINT. 1 SERXDMA_ENABLE Receiver DMA request is enabled.
16	SET_TX_DMA	R/W1TS	0h	Set transmit DMA. This bit is effective in LIN or SCI-compatible mode. To enable DMA requests for the transmitter, this bit must be set. If it is cleared, interrupt requests are generated depending on SETTXINT. 1 SETXDMA_ENABLE Transmit DMA request is enabled
15:14	RESERVED_4	R	0h	Reserved
13	SETIDINT	R/W1TS	0h	Set Identification interrupt. This bit is effective in LIN mode only. This bit is set to enable interrupt once a valid matching identifier is received. 1 SETIDINT_ENABLE Interrupt is enabled.
12:10	RESERVED_3	R	0h	Reserved
9	SETRXINT	R/W1TS	0h	Set Receiver interrupt. Setting this bit enables the SCI/LIN to generate a receive interrupt after a frame has been completely received and the data is being transferred from SCIRXSHF to SCIRD. 1 SETRXINT_ENABLE Interrupt is enabled.
8	SETTXINT	R/W1TS	0h	Set Transmitter interrupt. Setting this bit enables the SCI/LIN to generate a transmit interrupt as data is being transferred from SCITD to SCITXSHF and the TXRDY bit is being set. 1 SETTXINT_ENABLE Interrupt is enabled.
7	SETTOA3WUSINT	R/W1TS	0h	Set Timeout After 3 Wakeup Signals interrupt. This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN to generate an interrupt when there is a timeout after 3 wakeup signals have been sent. This field is writable in LIN mode only. 1 SETTOA3WUSINT_ENABLE Interrupt is enabled.
6	SETTOAWUSINT	R/W1TS	0h	Set Timeout After Wakeup Signal interrupt. This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN to generate an interrupt when there is a timeout after one wakeup signal has been sent. This field is writable in LIN mode only. 1 SETTOAWUSINT_ENABLE Interrupt is enabled.
5	RESERVED_2	R	0h	Reserved
4	SETTIMEOUTINT	R/W1TS	0h	Set timeout interrupt. This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN to generate an interrupt when no LIN bus activity [bus idle] occurs for at least 4 seconds. This field is writable in LIN mode only. 1 SETTIMEOUTINT_ENABLE Interrupt is enabled.
3:2	RESERVED_1	R	0h	Reserved

Table 4-1220. SCISETINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SETWAKEUPINT	R/W1TS	0h	Set wake-up interrupt. This bit is effective in LIN or SCI-compatible mode. Setting this bit enables the SCI/LIN to generate a wake-up interrupt and thereby exit low-power mode. The wake-up interrupt is asserted on falling edge of the wake-up pulse. If enabled, the wake-up interrupt is asserted when local low-power mode is requested while the receiver is busy or if a low level is detected on the SCIRX pin during low-power mode. Wake-up interrupt is not asserted upon a wakeup pulse if the module is not in power down mode. 1 SETWAKEUPINT_ENABLE Interrupt is enabled.
0	SETBRKDTINT	R/W1TS	0h	Set break-detect interrupt. This bit is effective in SCI-compatible mode only. Setting this bit enables the SCI/LIN to generate an interrupt if a break condition is detected on the LINRX pin. This field is writable in SCI mode only. 1 SETBRKDTINT_ENABLE Interrupt is enabled.

4.12.5 LIN_SCICLEARINT Registers

4.12.5.1 LIN_SCICLEARINT Register (Offset = 10h) [reset = 0h]

Short Description: The SCICLEARINT register

Long Description: The SCICLEARINT register is used to disable the enabled interrupts without accessing the SCISETINT register.

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Table 4-1221. Instance Table

Instance Name	Physical Address
LIN0	5240 0010h
LIN1	5240 1010h
LIN2	5240 2010h
LIN3	5240 3010h
LIN4	5240 4010h

Figure 4-531. SCICLEARINT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLRBEINT	CLRPBEINT	CLRCEINT	CLRISFEINT	CLRNREINT	CLRFEINT	CLROEINT	CLRPEINT	RESERVED_6					RESERVED_5	SETRXDMA	CLRTXDMA
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R					R	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h					0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_4		CLRIDINT	RESERVED_3			CLRRXINT	CLRTXINT	CLRTOA3WUSINT	CLRTOAWUSINT	RESERVED_2	CLRTIMEOUTINT	RESERVED_1		CLRWAKEUPINT	CLRBRKDTINT
R		R/W1TC	R			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R	R/W1TC	R		R/W1TC	R/W1TC
0h		0h	0h			0h	0h	0h	0h	0h	0h	0h		0h	0h

Access Types Legend

Table 4-1222. SCICLEARINT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CLRBEINT	R/W1TC	0h	Clear Bit Error Interrupt. This bit is effective in LIN mode only. Setting this bit disables the bit error interrupt. This field is writable in LIN mode only. 1 CLRBEINT_ENABLE Interrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
30	CLRPBEINT	R/W1TC	0h	Clear Physical Bus Error Interrupt. This bit is effective in LIN mode only. Setting this bit disables the physical-bus error interrupt. This field is writable in LIN mode only. 1 CLRPBEINT_ENABLE Interrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
29	CLRCEINT	R/W1TC	0h	Clear checksum-error Interrupt. This bit is effective in LIN mode only. Setting this bit disables the checksum-error interrupt. This field is writable in LIN mode only. 1 CLRCEINT_ENABLE Interrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
28	CLRISFEINT	R/W1TC	0h	Clear Inconsistent-Sync-Field-Error Interrupt. This bit is effective in LIN mode only. Setting this bit disables the ISFE interrupt. This field is writable in LIN mode only. 1 CLRISFEINT_ENABLE Interrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.

Table 4-1222. SCICLEARINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	CLRNREINT	R/W1TC	0h	Clear No-Reponse-Error Interrupt. This bit is effective in LIN mode only. Setting this bit disables the no-response error interrupt. This field is writable in LIN mode only. 1 CLRNREINT_ENABLE Interrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
26	CLRFEINT	R/W1TC	0h	Clear Framing-Error Interrupt. This bit is effective in LIN or SCI-compatible mode. Setting this bit disables framing-error interrupt. 1 CLRFEINT_ENABLE Interrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
25	CLROEINT	R/W1TC	0h	Clear Overrun-Error Interrupt. This bit is effective in LIN or SCI-compatible mode. Setting this bit disables the overrun interrupt. 1 CLROEINT_ENABLE Interrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
24	CLRPEINT	R/W1TC	0h	Clear Parity Interrupt. This bit is effective in LIN or SCI-compatible mode. Setting this bit disables the parity error interrupt. 1 CLRPEINT_ENABLE Interrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
23:19	RESERVED_6	R	0h	Reserved
18	RESERVED_5	R	0h	Reserved
17	SETRXDMA	R/W1TC	0h	Clear receiver DMA. This bit is effective in LIN or SCI-compatible mode. Setting this bit disables the receive DMA request. 1 CLRRXDMA_ENABLE Receiver DMA request is enabled. Writing a 1 to this bit will disable the DMA request and clear this bit.
16	CLRTXDMA	R/W1TC	0h	Clear transmit DMA. This bit is effective in LIN or SCI-compatible mode. Setting this bit disables the transmit DMA request. 1 CLRTXDMA_ENABLE Transmit DMA request is enabled. Writing a 1 to this bit will disable the DMA request and clear this bit.
15:14	RESERVED_4	R	0h	Reserved
13	CLRIDINT	R/W1TC	0h	Clear Identifier interrupt. This bit is effective in LIN mode only. Setting this bit disables the ID interrupt. 1 CLRIDINT_ENABLE Interrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
12:10	RESERVED_3	R	0h	Reserved
9	CLRRXINT	R/W1TC	0h	Clear Receiver interrupt. This bit is effective in LIN or SCI-compatible mode. Setting this bit disables the receiver interrupt. 1 CLRRXINT_ENABLE Interrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
8	CLRTXINT	R/W1TC	0h	Clear Transmitter interrupt. This bit is effective in LIN or SCI-compatible mode. Setting this bit disables the transmitter interrupt. 1 CLRTXINT_ENABLE Interrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
7	CLRTOA3WUSINT	R/W1TC	0h	Clear Timeout After 3 Wakeup Signals interrupt. This bit is effective in LIN mode only. Setting this bit disables the timeout after 3 wakeup signals interrupt. This field is writable in LIN mode only. 1 CLRTOA3WUSINT_ENABLE Interrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
6	CLRTOAWUSINT	R/W1TC	0h	Clear Timeout After Wakeup Signal interrupt. This bit is effective in LIN mode only. Setting this bit disables the timeout after one wakeup signal interrupt. This field is writable in LIN mode only. 1 CLRTOAWUSINT_ENABLE Interrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
5	RESERVED_2	R	0h	Reserved
4	CLRTIMEOUTINT	R/W1TC	0h	Clear Timeout interrupt. This bit is effective in LIN mode only. Setting this bit disables the timeout [LIN bus idle] interrupt. This field is writable in LIN mode only. 1 CLRTIMEOUTINT_ENABLE Interrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
3:2	RESERVED_1	R	0h	Reserved

Table 4-1222. SCICLEARINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CLRWAKEUPINT	R/W1TC	0h	Clear Wake-up interrupt. This bit is effective in LIN or SCI-compatible mode. Setting this bit disables the wake-up interrupt. 1 CLRWAKEUPINT_ENABLE Interrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
0	CLRBRKDTINT	R/W1TC	0h	Clear Break-detect interrupt. This bit is effective in SCI-compatible mode only. Setting this bit disables the Break-detect interrupt. This field is writable in SCI mode only. 1 CLRBRKDTINT_ENABLE Interrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.

4.12.6 LIN_SCISETINTLVL Registers

4.12.6.1 LIN_SCISETINTLVL Register (Offset = 14h) [reset = 0h]

Short Description: The SCISETINTLVL register

Long Description: The SCISETINTLVL register is used to map individual interrupt sources to the INT1 interrupt line.

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Table 4-1223. Instance Table

Instance Name	Physical Address
LIN0	5240 0014h
LIN1	5240 1014h
LIN2	5240 2014h
LIN3	5240 3014h
LIN4	5240 4014h

Figure 4-532. SCISETINTLVL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SETBEINTLVL	SETPBEINTLVL	SETCEINTLVL	SETISFEINTLVL	SETNREINTLVL	SETFEINTLVL	SETOEINTLVL	SETPEINTLVL	RESERVED_7					RESERVED_6	RESERVED_5	
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R					R	R	
0h	0h	0h	0h	0h	0h	0h	0h	0h					0h	0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_4		SETIDINTLVL	RESERVED_3			SETRXINTOVO	SETTXINTLVL	SETTOA3WUSINTLVL	SETTOAWUSINTLVL	RESERVED_2	SETTIMEOUTINTLVL	RESERVED_1		SETWAKEUPINTLVL	SETBRKDTINTLVL
R		R/W1TS	R			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R	R/W1TS	R		R/W1TS	R/W1TS
0h		0h	0h			0h	0h	0h	0h	0h	0h	0h		0h	0h

Access Types Legend

Table 4-1224. SCISETINTLVL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SETBEINTLVL	R/W1TS	0h	Set Bit Error interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the Bit Error interrupt level to the INT1 line. This field is writable in LIN mode only. 1 SETBEINTLVL_INT1 Interrupt level mapped to INT1 line.
30	SETPBEINTLVL	R/W1TS	0h	Set Physical Bus Error interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the Physical Bus Error interrupt level to the INT1 line. This field is writable in LIN mode only. 1 SETPBEINTLVL_INT1 Interrupt level mapped to INT1 line.
29	SETCEINTLVL	R/W1TS	0h	Set Checksum-error interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the Checksum-error interrupt level to the INT1 line. This field is writable in LIN mode only. 1 SETCEINTLVL_INT1 Interrupt level mapped to INT1 line.
28	SETISFEINTLVL	R/W1TS	0h	Set Inconsistent-Sync-Field-Error interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the Inconsistent-Sync-Field-Error interrupt level to the INT1 line. This field is writable in LIN mode only. 1 SETISFEINTLVL_INT1 Interrupt level mapped to INT1 line.

Table 4-1224. SCISETINTLVL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	SETNREINTLVL	R/W1TS	0h	Set No-Reponse-Error interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the No-Response-Error interrupt level to the INT1 line. This field is writable in LIN mode only. 1 SETNREINTLVL_INT1 Interrupt level mapped to INT1 line.
26	SETFEINTLVL	R/W1TS	0h	Set Framing-Error interrupt level. This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Framing-Error interrupt level to the INT1 line. 1 SETFEINTLVL_INT1 Interrupt level mapped to INT1 line.
25	SETOEINTLVL	R/W1TS	0h	Set Overrun-Error Interrupt Level. This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Overrun-Error interrupt level to the INT1 line. 1 SETOEINTLVL_INT1 Interrupt level mapped to INT1 line.
24	SETPEINTLVL	R/W1TS	0h	Set Parity Error interrupt level. This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Parity error interrupt level to the INT1 line. 1 SETPEINTLVL_INT1 Interrupt level mapped to INT1 line.
23:19	RESERVED_7	R	0h	Reserved
18	RESERVED_6	R	0h	Reserved
17:16	RESERVED_5	R	0h	Reserved
15:14	RESERVED_4	R	0h	Reserved
13	SETIDINTLVL	R/W1TS	0h	Set ID interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the ID interrupt level to the INT1 line. This field is writable in LIN mode only. 1 SETIDINTLVL_INT1 Interrupt level mapped to INT1 line.
12:10	RESERVED_3	R	0h	Reserved
9	SETRXINTOVO	R/W1TS	0h	Set Receiver interrupt level. This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the receiver interrupt level to the INT1 line. 1 SETRXINTOVO_INT1 Interrupt level mapped to INT1 line.
8	SETTXINTLVL	R/W1TS	0h	Set Transmitter interrupt level. This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the transmitter interrupt level to the INT1 line. 1 SETTXINTLVL_INT1 Interrupt level mapped to INT1 line.
7	SETTOA3WUSINTLVL	R/W1TS	0h	Set Timeout After 3 Wakeup Signals interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the timeout after 3 wakeup signals interrupt level to the INT1 line. This field is writable in LIN mode only. 1 SETTOA3WUSINTLVL_INT Interrupt level mapped to INT1 1 line.
6	SETTOAWUSINTLVL	R/W1TS	0h	Set Timeout After Wakeup Signal interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the the timeout after wakeup interrupt level to the INT1 line. This field is writable in LIN mode only. 1 SETTOAWUSINTLVL_INT1 Interrupt level mapped to INT1 line.
5	RESERVED_2	R	0h	Reserved
4	SETTIMEOUTINTLVL	R/W1TS	0h	Set Timeout interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the timeout interrupt level to the INT1 line. This field is writable in LIN mode only. 1 SETTIMEOUTINTLVL_INT Interrupt level mapped to INT1 1 line.
3:2	RESERVED_1	R	0h	Reserved
1	SETWAKEUPINTLVL	R/W1TS	0h	Set Wake-up interrupt level. This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Wake-up interrupt level to the INT1 line. 1 SETWAKEUPINTLVL_INT1 Interrupt level mapped to INT1 line.
0	SETBRKDTINTLVL	R/W1TS	0h	Set Break-detect interrupt level. This bit is effective in SCI-compatible mode only. Writing to this bit maps the Break-detect interrupt level to the INT1 line. This field is writable in SCI mode only. 1 SETBRKDTINTLVL_INT1 Interrupt level mapped to INT1 line.

4.12.7 LIN_SCICLEARINTLVL Registers

4.12.7.1 LIN_SCICLEARINTLVL Register (Offset = 18h) [reset = 0h]

Short Description: The SCICLEARINTLVL regist

Long Description: The SCICLEARINTLVL register is used to map individual interrupt sources to the INT0 line.

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Table 4-1225. Instance Table

Instance Name	Physical Address
LIN0	5240 0018h
LIN1	5240 1018h
LIN2	5240 2018h
LIN3	5240 3018h
LIN4	5240 4018h

Figure 4-533. SCICLEARINTLVL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLRBEINTLVL	CLRPBEINTLVL	CLRCEINTLVL	CLRISFEINTLVL	CLRNREINTLVL	CLRFEINTLVL	CLROEINTLVL	CLRPEINTLVL	RESERVED_7					RESERVED_6	RESERVED_5	
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R					R	R	
0h	0h	0h	0h	0h	0h	0h	0h	0h					0h	0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_4		CLRIDINTLVL	RESERVED_3			CLRRXINTLVL	CLRTXINTLVL	CLRTOA3WUSINTLVL	CLRTOAWUSINTLVL	RESERVED_2	CLRTIMEOUTINTLVL	RESERVED_1		CLRWAKEUPINTLVL	CLRBRKDTINTLVL
R		R/W1TC	R			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R	R/W1TC	R		R/W1TC	R/W1TC
0h		0h	0h			0h	0h	0h	0h	0h	0h	0h		0h	0h

Access Types Legend

Table 4-1226. SCICLEARINTLVL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CLRBEINTLVL	R/W1TC	0h	Clear Bit Error interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the Bit Error interrupt level to the INT0 line. This field is writable in LIN mode only. 1 CLRBEINTLVL_INT1 Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
30	CLRPBEINTLVL	R/W1TC	0h	Clear Physical Bus Error interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the Physical Bus Error interrupt level to the INT0 line. This field is writable in LIN mode only. 1 CLRPBEINTLVL_INT1 Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
29	CLRCEINTLVL	R/W1TC	0h	Clear Checksum-error interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the Checksum-error interrupt level to the INT0 line. This field is writable in LIN mode only. 1 CLRCEINTLVL_INT1 Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
28	CLRISFEINTLVL	R/W1TC	0h	Clear Inconsistent-Sync-Field-Error interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the Inconsistent-Sync-Field-Error interrupt level to the INT0 line. This field is writable in LIN mode only. 1 CLRISFEINTLVL_INT1 Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.

Table 4-1226. SCICLEARINTLVL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	CLRNREINTLVL	R/W1TC	0h	Clear No-Reponse-Error interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the No-Response-Error interrupt level to the INT0 line. This field is writable in LIN mode only. 1 CLRNREINTLVL_INT1 Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
26	CLRFEINTLVL	R/W1TC	0h	Clear Framing-Error interrupt level. This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Framing-Error interrupt level to the INT0 line. 1 CLRFEINTLVL_INT1 Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
25	CLROEINTLVL	R/W1TC	0h	Clear Overrun-Error Interrupt Level. This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Overrun-Error interrupt level to the INT0 line. 1 CLROEINTLVL_INT1 Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
24	CLRPEINTLVL	R/W1TC	0h	Clear Parity Error interrupt level. This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Parity Error interrupt level to the INT0 line. 1 CLRPEINTLVL_INT1 Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
23:19	RESERVED_7	R	0h	Reserved
18	RESERVED_6	R	0h	Reserved
17:16	RESERVED_5	R	0h	Reserved
15:14	RESERVED_4	R	0h	Reserved
13	CLRIDINTLVL	R/W1TC	0h	Clear ID interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the ID interrupt level to the INT0 line. This field is writable in LIN mode only. 1 CLRIDINTLVL_INT1 Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
12:10	RESERVED_3	R	0h	Reserved
9	CLRRXINTLVL	R/W1TC	0h	Clear Receiver interrupt level. This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the receiver interrupt level to the INT0 line. 1 CLRRXINTLVL_INT1 Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
8	CLRTXINTLVL	R/W1TC	0h	Clear Transmitter interrupt level. This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the transmitter interrupt level to the INT0 line. 1 CLRTXINTLVL_INT1 Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
7	CLRTOA3WUSINTLVL	R/W1TC	0h	Clear Timeout After 3 Wakeup Signals interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the timeout after 3 wakeup signals interrupt level to the INT0 line. This field is writable in LIN mode only. 1 CLRTOA3WUSINTLVL_INT Interrupt level mapped to INT1 1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
6	CLRTOAWUSINTLVL	R/W1TC	0h	Clear Timeout After Wakeup Signal interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the the timeout after wakeup interrupt level to the INT0 line. This field is writable in LIN mode only. 1 CLRTOAWUSINTLVL_INT1 Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
5	RESERVED_2	R	0h	Reserved
4	CLRTIMEOUTINTLVL	R/W1TC	0h	Clear Timeout interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the timeout interrupt level to the INT0 line. This field is writable in LIN mode only. 1 CLRTIMEOUTINTLVL_INT Interrupt level mapped to INT1 1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
3:2	RESERVED_1	R	0h	Reserved

Table 4-1226. SCICLEARINTLVL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CLRWAKEUPINTLVL	R/W1TC	0h	Clear Wake-up interrupt level. This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Wake-up interrupt level to the INT0 line. 1 CLRWAKEUPINTLVL_INT1 Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
0	CLRBRKDTINTLVL	R/W1TC	0h	Clear Break-detect interrupt level. This bit is effective in SCI-compatible mode only. Writing to this bit maps the Break-detect interrupt level to the INT0 line. This field is writable in SCI mode only. 1 CLRBRKDTINTLVL_INT1 Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.

4.12.8 LIN_SCIFLR Registers

4.12.8.1 LIN_SCIFLR Register (Offset = 1Ch) [reset = 904h]

Short Description: The SCIFLR register indic

Long Description: The SCIFLR register indicates the current status of the various interrupt sources of the LIN module.

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Table 4-1227. Instance Table

Instance Name	Physical Address
LIN0	5240 001Ch
LIN1	5240 101Ch
LIN2	5240 201Ch
LIN3	5240 301Ch
LIN4	5240 401Ch

Figure 4-534. SCIFLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BE	PBE	CE	ISFE	NRE	FE	OE	PE	RESERVED_3							
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R							
0h	0h	0h	0h	0h	0h	0h	0h	0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2	IDRXFLAG	IDTXFLAG	RXWAKE	TXEMPTY	TXWAKE	RXRDY	TXRDY	TOA3WUS	TOAWUS	RESERVED_1	TIMEOUT	BUSY	IDLE	WAKEUP	BRKDT
R	R/W1TC	R/W1TC	R	R	R/W	R/W1TC	R	R/W1TC	R/W1TC	R	R/W1TC	R	R	R/W1TC	R/W1TC
0h	0h	0h	0h	1h	0h	0h	1h	0h	0h	0h	0h	0h	1h	0h	0h

Access Types Legend

Table 4-1228. SCIFLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BE	R/W1TC	0h	Bit Error Flag. This bit is effective in LIN mode only. This bit is set when there has been a bit error. This is detected by the bit monitor in the internal bit monitor. This bit is cleared by: - Reading the corresponding interrupt offset in the SCIINTVECT0/1 register - Setting the SWnRESET bit [SCIGCR1.7] - RESET bit [SCIGCR0.0] - System reset - Writing a 1 to this bit - Reception of a new sync break This field is writable in LIN mode only. 1 BE_EFFECT Bit error detected.
30	PBE	R/W1TC	0h	Physical Bus Error Flag. This bit is effective in LIN mode only. This bit is set when there has been a physical bus error. This is detected by the bit monitor in TED. This bit is cleared by: - Reading the corresponding interrupt offset in the SCIINTVECT0/1 register - Setting the SWnRESET bit [SCIGCR1.7] - RESET bit [SCIGCR0.0] - System reset - Writing a 1 to this bit - Reception of a new sync break Note: thie PBE will ony be flagged if no sync break can be generated. [because of a bus shortage to VBAT] or if no sync break delimeter can be generated [because of a bus shortage to GND]. This field is writable in LIN mode only. 1 PBE_EFFECT Physical bus error detected.

Table 4-1228. SCIFLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	CE	R/W1TC	0h	Checksum Error Flag. This bit is effective in LIN mode only. This bit is set when there is checksum error detected by a receiving node. The type of checksum to be used depends on the SCIGCR1.CTYPE bit. This bit is cleared by: - Reading the corresponding interrupt offset in the SCIINTVECT0/1 register - Setting the SWnRESET bit [SCIGCR1.7] - RESET bit [SCIGCR0.0] - System reset - Writing a 1 to this bit - Reception of a new sync break This field is writable in LIN mode only. 1 CE_EFFECT Checksum error detected.
28	ISFE	R/W1TC	0h	Inconsistent Sync Field Error Flag. This bit is effective in LIN mode only. This bit is set when there has been an inconsistent Sync Field error detected by the synchronizer during header reception. See the "Header Reception and Adaptive Baudrate" section for more information. This bit is cleared by: - Reading the corresponding interrupt offset in the SCIINTVECT0/1 register - Setting the SWnRESET bit [SCIGCR1.7] - RESET bit [SCIGCR0.0] - System reset - Writing a 1 to this bit - Reception of a new sync break This field is writable in LIN mode only. 1 ISFE_EFFECT Inconsistent Sync Field error detected.
27	NRE	R/W1TC	0h	No-Response Error Flag. This bit is effective in LIN mode only. This bit is set when there is no response to a master's header completed within TFRAME_MAX. This timeout period is applied for message frames of unknown length [identifiers 0 to 61]. This error is detected by the synchronizer of the module. This bit is cleared by: - Reading the corresponding interrupt offset in the SCIINTVECT0/1 register - Setting the SWnRESET bit [SCIGCR1.7] - RESET bit [SCIGCR0.0] - System reset - Writing a 1 to this bit - Reception of a new sync break This field is writable in LIN mode only. 1 NRE_EFFECT No-Response error detected.
26	FE	R/W1TC	0h	Framing error flag. This bit is effective in LIN or SCI-compatible mode. This bit is set when an expected stop bit is not found. In SCI compatible mode, only the first stop bit is checked. The missing stop bit indicates that synchronization with the start bit has been lost and that the character is incorrectly framed. Detection of a framing error causes the SCI to generate an error interrupt if the RXERR INT ENA bit is set. This bit is cleared by: - Reading the corresponding interrupt offset in the SCIINTVECT0/1 register - Setting the SWnRESET bit [SCIGCR1.7] - RESET bit [SCIGCR0.0] - System reset - Writing a 1 to this bit - Reception of a new character [SCI-compatible mode], or frame [LIN mode] In multibuffer mode the frame is defined in the SCIFORMAT register. 1 FE_EFFECT Framing error detected.
25	OE	R/W1TC	0h	Overrun error flag. This bit is effective in LIN or SCI-compatible mode. This bit is set when the transfer of data from SCIRXSHF to SCIRD overwrites unread data already in SCIRD or the RDy buffers. Detection of an overrun error causes the LIN to generate an error interrupt if the SET OE INT bit is one. This bit is cleared by: - Reading the corresponding interrupt offset in the SCIINTVECT0/1 register - Setting the SWnRESET bit [SCIGCR1.7] - RESET bit [SCIGCR0.0] - System reset - Writing a 1 to this bit 1 OE_EFFECT Overrun error detected.
24	PE	R/W1TC	0h	Parity error flag. This bit is effective in LIN or SCI-compatible mode. This bit is set when a parity error is detected in the received data. In SCI address-bit mode, the parity is calculated on the data and address bit fields of the received frame. In idle-line mode, only the data is used to calculate parity. An error is generated when a character is received with a mismatch between the number of 1s and its parity bit. For more information on parity checking, see the "SCI Global Control Register [SCIGCR1]" description. If the parity function is disabled [that is, SCIGCR1.2 = 0], the PE flag is disabled and read as 0. Detection of a parity error causes the LIN to generate an error interrupt if the SET PE INT bit = 1. This bit is cleared by: - Reading the corresponding interrupt offset in the SCIINTVECT0/1 register - Setting the SWnRESET bit [SCIGCR1.7] - RESET bit [SCIGCR0.0] - System reset - Reception of a new charcter [SCI-compatible mode] or frame [LIN mode] - Writing a 1 to this bit 1 PE_EFFECT Parity error detected.

Table 4-1228. SCIFLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:16	RESERVED_3	R	0h	Reserved
15	RESERVED_2	R	0h	Reserved
14	IDRXFLAG	R/W1TC	0h	Identifier On Receive Flag. This bit is effective in LIN mode only. This flag is set once an identifier is received with an RX match and no ID-parity error. See the "Message Filtering and Validation" section for more details. When this flag is set it indicates that a new valid identifier has been received on an RX match. This bit is cleared by: - Reading the corresponding interrupt offset in the SCIINTVECT0/1 register - Setting the SWnRESET bit [SCIGCR1.7] - RESET bit [SCIGCR0.0] - System reset - Reading the LINID register - Writing a 1 to this bit This field is writable in LIN mode only. 1 IDRXFLAG_EFFECT Valid ID RX received in LINID[23:16] on RX match.
13	IDTXFLAG	R/W1TC	0h	Identifier On Transmit Flag. This bit is effective in LIN mode only. This flag is set once an identifier is received with a TX match and no ID-parity error. See the "Message Filtering and Validation" section for more details. When this flag is set it indicates that a new valid identifier has been received on a TX match. This bit is cleared by: - Reading the corresponding interrupt offset in the SCIINTVECT0/1 register - RESET bit [SCIGCR0.0] - Setting SWnRESET - System reset - Reading the LINID register - Writing a 1 to this bit This field is writable in LIN mode only. 1 IDTXFLAG_EFFECT Valid ID received in LINID[23:16] on TX match.
12	RXWAKE	R	0h	Receiver wakeup detect flag. This bit is effective in SCI-compatible mode only. The SCI sets this bit to indicate that the data currently in SCIRD is an address. This bit is cleared by: - RESET bit - Setting the SWnRESET bit [SCIGCR1.7] - System reset - Receipt of a data frame This bit is writable in SCI mode only. 1 RXWAKE_EFFECT The data in SCIRD is an address. See [1] Section 3.4.4, Sleep Mode for Multiprocessor Communication, on page 16 for more information on using the RXWAKE bit with sleep mode.
11	TXEMPTY	R	1h	Transmitter Empty flag. The value of this flag indicates the contents of the transmitter's buffer register[s] [SCITD/TDy] and shift register [SCITXSHF]. In multibuffer mode, this flag indicates the value of the TDx registers and shift register [SCITXSHF]. In non multibuffer mode, this flag indicates the value of LINTD0 [byte] and shift register [SCITXSHF]. This bit is set by: - RESET bit [SCIGCR0.0] - Setting the SWnRESET bit [SCIGCR1.7] - System reset. Note: This bit does not cause an interrupt request. 1 TXEMPTY_EFFECT Compatible mode or LIN with no multibuffer: Transmitter buffer and shift registers are both empty. In LIN mode using multibuffer mode: Multibuffer and shift registers are all empty.
10	TXWAKE	R/W	0h	SCI transmitter wakeup method select. This bit is effective in SCI-compatible mode only. The TXWAKE bit controls whether the data in SCITD should be sent as an address or data frame using multiprocessor communication format. This bit is set to 1 or 0 by software before a byte is written to SCITD and is cleared by the SCI when data is transferred from SCITD to SCITXSHF or by a system reset. TXWAKE is not cleared by the SWnRESET bit [SCIGCR1.7]. 1 TXWAKE_ADDR1 Address-bit mode: Frame to be transmitted will be an address (address bit=1). Idle-line mode: Following frame to be transmitted will be an address (writing a 1 to this bit followed by writing dummy data to the SCITD will result in a idle period of 11 bit periods before the next frame is transmitted).

Table 4-1228. SCIFLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	RXRDY	R/W1TC	0h	Receiver ready flag. In SCI compatibility mode, the receiver sets this bit to indicate that the SCIRD contains new data and is ready to be read by the CPU. In LIN mode, RXRDY is set once a valid frame is received in multibuffer mode, a valid frame being a message frame received with no errors. In non multibuffer mode RXRDY is set for each received byte and will be set for the last byte of the frame if there are no errors. The SCI/LIN generates a receive interrupt when RXRDY flag bit is set if the interrupt-enable bit is set [SCISETINT.9]. RXRDY is cleared by: - RESET bit [SCIGCR0.0] - Setting the SWnRESET - System reset - Writing a 1 to this bit - Reading SCIRD in while in SCI compatibility mode - Reading last data byte RDy of the response in LIN mode Note: The RXRDY flag cannot be cleared by reading the corresponding interrupt offset in the SCIINTVECT0/1 register. 1 RXRDY_EFFECT New data ready to be read from SCIRD.
8	TXRDY	R	1h	Transmitter buffer register ready flag. When set, this bit indicates that the transmit buffer[s] register [SCITD in compatibility mode and LINTD0, LINTD1 in MBUF mode] is/are ready to get another character from a CPU write. In SCI compatibility mode, writing data to SCITD automatically clears this bit. In LIN mode, this bit is cleared once byte 0 [TD0] is written to LINTD0. This bit is set after the data of the TX buffer are shifted into the SCITXSHF register. This event can trigger a transmit DMA event if the DMA enable bit is set. This bit is set to 1 by: - RESET bit [SCIGCR0.0] - Setting the SWnRESET [SCIGCR1.7] - System reset Note: The TXRDY flag cannot be cleared by reading the corresponding interrupt offset in the SCIINTVECT0/1 register. Note: The transmit interrupt request can be eliminated until the next series of data is written into the transmit buffers LINTD0 and LINTD1, by disaLINg the corresponding interrupt via the SCICLEARINT register or by disaLINg the transmitter via the TXENA bit [SCIGCR1.25=0]. 1 TXRDY_EMPTY Compatible mode: SCITD is ready to receive the next character. LIN mode: The multibuffers are ready to receive the next character(s).
7	TOA3WUS	R/W1TC	0h	Timeout After 3 Wakeup Signals flag. This bit is effective in LIN mode only. This flag is set if there is no Sync Break received after 3 wakeup signals and a period of 1.5 seconds have passed. Such expiration time is used before issuing another round of wakeup signals. This bit is cleared by: - Reading the corresponding interrupt offset in the SCIINTVECT0/1 register - Setting the SWnRESET bit [SCIGCR1.7] - RESET bit [SCIGCR0.0] - System reset - Writing a 1 to this bit This field is writable in LIN mode only. 1 TOA3WUS_EFFECT Timeout after 3 wakeup signals and 1.5s time.
6	TOAWUS	R/W1TC	0h	Timeout After Wakeup Signal flag. This bit is effective in LIN mode only. This bit is set if there is no Sync Break received after a wakeup signal has been sent. A minimum of 150 ms expiration time is used before issuing another wakeup signal. This bit is cleared by: - Reading the corresponding interrupt offset in the SCIINTVECT0/1 register - Setting the SWnRESET bit [SCIGCR1.7] - RESET bit [SCIGCR0.0] - System reset - Writing a 1 to this bit This field is writable in LIN mode only. 1 TOAWUS_EFFECT Timeout after one wakeup signal.
5	RESERVED_1	R	0h	Reserved
4	TIMEOUT	R/W1TC	0h	LIN Bus IDLE timeout flag. This bit is effective in LIN mode only. This bit is set if there is no LIN bus activity for at least 4 seconds. LIN bus activity being a transition from recessive to dominant. This bit is cleared by: - Reading the corresponding interrupt offset in the SCIINTVECT0/1 register - Setting the SWnRESET bit [SCIGCR1.7] - RESET bit [SCIGCR0.0] - System reset - Writing a 1 to this bit This field is writable in LIN mode only. 1 TIMEOUT_EFFECT LIN bus idle detected.

Table 4-1228. SCIFLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	BUSY	R	0h	Bus BUSY flag. This bit is effective in LIN mode and SCI-compatible mode. This bit indicates whether the receiver is in the process of receiving a frame. As soon as the receiver detects the beginning of a start bit, the BUSY bit is set to 1. When the reception of a frame is complete, the BUSY bit is cleared. If SET WAKEUP INT is set and power down is requested while this bit is set, the SCI/LIN automatically prevents low-power mode from being entered and generates wakeup interrupt. The BUSY bit is controlled directly by the SCI receiver but can be cleared by: - Setting the SWnRESET bit [SCIGCR1.7] - RESET bit [SCIGCR0.0] - System reset. 1 BUSY_EFFECT Receiver is currently receiving a frame.
2	IDLE	R	1h	SCI receiver in idle state. This bit is effective in SCI-compatible mode only. While this bit is set, the SCI looks for an idle period to resynchronize itself with the bit stream. The receiver does not receive any data while the bit is set. The bus must be idle for 11 bit periods to clear this bit. The SCI enters this state: - After a system reset - Setting the SWnRESET bit [SCIGCR1.7] - After coming out of power down This bit is writable in SCI mode only. 1 IDLE_EFFECT Idle period not detected, the SCI will not receive any data.
1	WAKEUP	R/W1TC	0h	Wake-up flag. This bit is effective in LIN mode only. This bit is set by the SCI/LIN when receiver or transmitter activity has taken the module out of power-down mode. An interrupt is generated if the SET WAKEUP INT bit [SCISETINT.1] is set. This bit is cleared by: - Reading the corresponding interrupt offset in the SCIINTVECT0/1 register. - Setting the SWnRESET bit [SCIGCR1.7] - RESET bit [SCIGCR0.0] - System reset - Writing a 1 to this bit. This field is writable in LIN mode only. 1 WAKEUP_EFFECT Wake up from power-down mode.
0	BRKDT	R/W1TC	0h	SCI break-detect flag. This bit is effective in SCI-compatible mode only. This bit is set when the SCI detects a break condition on the LINRX pin. A break condition occurs when the LINRX pin remains continuously low for at least 10 bits after a missing first stop bit, that is, after a framing error. Detection of a break condition causes the SCI to generate an error interrupt if the BRKDT INT ENA bit is set. The BRKDT bit is cleared by the following: - Reading the corresponding interrupt offset in the SCIINTVECT0/1 register. - Setting the SWnRESET bit [SCIGCR1.7] - RESET bit [SCIGCR0.0] - System reset - By writing a 1 to this bit. This bit is writable in SCI mode only. 1 BRKDT_EFFECT Break condition detected.

4.12.9 LIN_SCIINTVECT0 Registers

4.12.9.1 LIN_SCIINTVECT0 Register (Offset = 20h) [reset = 0h]

Short Description: The SCIINTVECT0 register

Long Description: The SCIINTVECT0 register indicates the offset for the INT0 interrupt line.

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Table 4-1229. Instance Table

Instance Name	Physical Address
LIN0	5240 0020h
LIN1	5240 1020h
LIN2	5240 2020h
LIN3	5240 3020h
LIN4	5240 4020h

Figure 4-535. SCIINTVECT0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_2															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1											INTVECT0				
R											R				
0h											0h				

Access Types Legend

Table 4-1230. SCIINTVECT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_2	R	0h	Reserved
15:5	RESERVED_1	R	0h	Reserved
4:0	INTVECT0	R	0h	Interrupt vector offset for INT0. This register indicates the offset for interrupt line INT0. A read to this register updates its value to the next highest priority pending interrupt in SCIFLR and clears the flag corresponding to the offset that was read. Note: The flags for the receive [SCIFLR.9] and the transmit [SCIFLR.8] interrupts cannot be cleared by reading the corresponding offset vector in this register [see detailed description in SCIFLR register].

4.12.10 LIN_SCIINTVECT1 Registers

4.12.10.1 LIN_SCIINTVECT1 Register (Offset = 24h) [reset = 0h]

Short Description: The SCIINTVECT1 register

Long Description: The SCIINTVECT1 register indicates the offset for the INT1 interrupt line.

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Table 4-1231. Instance Table

Instance Name	Physical Address
LIN0	5240 0024h
LIN1	5240 1024h
LIN2	5240 2024h
LIN3	5240 3024h
LIN4	5240 4024h

Figure 4-536. SCIINTVECT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_2															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1											INTVECT1				
R											R				
0h											0h				

Access Types Legend

Table 4-1232. SCIINTVECT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_2	R	0h	Reserved
15:5	RESERVED_1	R	0h	Reserved
4:0	INTVECT1	R	0h	Interrupt vector offset for INT1. This register indicates the offset for interrupt line INT1. A read to this register updates its value to the next highest priority pending interrupt in SCIFLR and clears the flag corresponding to the offset that was read. Note: The flags for the receive [SCIFLR.9] and the transmit [SCIFLR.8] interrupts cannot be cleared by reading the corresponding offset vector in this register [see detailed description in SCIFLR register].

4.12.11 LIN_SCIFORMAT Registers

4.12.11.1 LIN_SCIFORMAT Register (Offset = 28h) [reset = 0h]

Short Description: The SCIFORMAT register is

Long Description: The SCIFORMAT register is used to set up the character and frame lengths.

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Table 4-1233. Instance Table

Instance Name	Physical Address
LIN0	5240 0028h
LIN1	5240 1028h
LIN2	5240 2028h
LIN3	5240 3028h
LIN4	5240 4028h

Figure 4-537. SCIFORMAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_2													LENGTH		
R													R/W		
0h													0h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1													CHAR		
R													R/W		
0h													0h		

Access Types Legend

Table 4-1234. SCIFORMAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED_2	R	0h	Reserved
18:16	LENGTH	R/W	0h	Frame length control bits. In LIN mode, these bits indicate the number of bytes in the response field from 1 to 8 bytes. In buffered SCI mode, these bits indicate the number of characters. When these bits are used to indicate LIN response length [SCIGCR1[0] = 1], then when there is an ID RX match, this value should be updated with the expected length of the response. In buffered SCI mode, these bits indicate the number of characters with SCIFORMAT[2:0] bits per character. i.e. these bits indicate the transmitter/receiver format for the number of characters: 1 to 8. There can be up to eight characters with eight bits each. 7 FIELD_8 The response field has 8 bytes/ characters. 6 FIELD_7 The response field has 7 bytes/characters. 5 FIELD_6 The response field has 6 bytes/characters. 4 FIELD_5 The response field has 5 bytes/characters. 3 FIELD_4 The response field has 4 bytes/characters. 2 FIELD_3 The response field has 3 bytes/ characters. 1 FIELD_2 The response field has 2 bytes/characters.
15:3	RESERVED_1	R	0h	Reserved

Table 4-1234. SCIFORMAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	CHAR	R/W	0h	Character length control bits. These bits are effective in SCI compatible mode only. These bits set the SCI character length from 1 to 8 bits. Note: In compatibility mode or buffered SCI mode, when data of fewer than eight bits in length is received, it is left justified in SCIRD/RDy and padded with trailing zeros. Data read from the SCIRD should be shifted by software to make the received data right justified. Note: Data written to the SCITD should be right justified but does not need to be padded with leading zeros. These bits are witable in SCI mode only. 7 CHAR_8 The character is 8 bits long. 6 CHAR_7 The character is 7 bits long. 5 CHAR_6 The character is 6 bits long. 4 CHAR_5 The character is 5 bits long. 3 CHAR_4 The character is 4 bits long. 2 CHAR_3 The character is 3 bits long. 1 CHAR_2 The character is 2 bits long.

4.12.12 LIN_BRSR Registers

4.12.12.1 LIN_BRSR Register (Offset = 2Ch) [reset = 0h]

Short Description: The BRSR register is used

Long Description: The BRSR register is used to configure the baud rate of the LIN module.

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Table 4-1235. Instance Table

Instance Name	Physical Address
LIN0	5240 002Ch
LIN1	5240 102Ch
LIN2	5240 202Ch
LIN3	5240 302Ch
LIN4	5240 402Ch

Figure 4-538. BRSR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1	U			M				SCI_LIN_PSH							
R	R/W			R/W				R/W							
0h	0h			0h				0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCI_LIN_PSL															
R/W															
0h															

Access Types Legend

Table 4-1236. BRSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED_1	R	0h	Reserved
30:28	U	R/W	0h	Superfractional Divider Selection. [U] These bits are an additional fractional part for the baudrate specification. These bits allow a super fine tuning of the fractional baudrate with 7 more intermediate values for each of the M fractional divider values. See the Superfractional Divider section for more details.
27:24	M	R/W	0h	SCI/LIN 4-bit Fractional Divider Selection. [M] These bits are effective in LIN or SCI asynchronous mode. These bits are used to select a baud rate for the SCI/LIN module, and they are a fractional part for the baud rate specification. The M divider allows fine-tuning of the baud rate over the P prescaler with 15 additional intermediate values for each of the P integer values.
23:16	SCI_LIN_PSH	R/W	0h	PRESCALER P [High Bits]. SCI/LIN 24-bit Integer Prescaler Selection. These bits are used to select a baudrate for the SCI/LIN module. These bits are effective in LIN mode and SCI compatible mode. The SCI/LIN has an internally generated serial clock determined by the LIN module input clock and the prescalers P and M in this register. The SCI/LIN uses the 24-bit integer prescaler P value to select 1 of over 16,700,000 available baud rates. The additional 4-bit fractional prescaler M refines the baudate selection.

Table 4-1236. BRSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:0	SCI_LIN_PSL	R/W	0h	PRESCALER P [Low Bits]. SCI/LIN 24-bit Integer Prescaler Selection. These bits are used to select a baudrate for the SCI/LIN module. These bits are effective in LIN mode and SCI compatible mode. The SCI/LIN has an internally generated serial clock determined by the LIN module input clock and the prescalers P and M in this register. The SCI/LIN uses the 24-bit integer prescaler P value to select 1 of over 16,700,000 available baud rates. The additional 4-bit fractional prescaler M refines the baudate selection.

4.12.13 LIN_SCIED Registers

4.12.13.1 LIN_SCIED Register (Offset = 30h) [reset = 0h]

Short Description: The SCIED register is a d

Long Description: The SCIED register is a duplicate copy of SCIRD register that has no affect on the RXRDY flag for use with an emulator.

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Table 4-1237. Instance Table

Instance Name	Physical Address
LIN0	5240 0030h
LIN1	5240 1030h
LIN2	5240 2030h
LIN3	5240 3030h
LIN4	5240 4030h

Figure 4-539. SCIED Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1								ED							
R								R							
0h								0h							

Access Types Legend

Table 4-1238. SCIED Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_1	R	0h	Reserved
7:0	ED	R	0h	Receiver Emulation Data. This bit is effective in SCI-compatible mode only. Reading SCIED[7-0] does not clear the RXRDY flag. This register should be used only by an emulator that must continually read the data buffer without affecting the RXRDY flag.

4.12.14 LIN_SCIRD Registers

4.12.14.1 LIN_SCIRD Register (Offset = 34h) [reset = 0h]

Short Description: The SCIRD register is whe

Long Description: The SCIRD register is where received data is stored and can be read from.

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Table 4-1239. Instance Table

Instance Name	Physical Address
LIN0	5240 0034h
LIN1	5240 1034h
LIN2	5240 2034h
LIN3	5240 3034h
LIN4	5240 4034h

Figure 4-540. SCIRD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1								RD							
R								R							
0h								0h							

Access Types Legend

Table 4-1240. SCIRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_1	R	0h	Reserved
7:0	RD	R	0h	Received Data. This bit is effective in SCI-compatible mode only. When a frame has been completely received, the data in the frame is transferred from the receiver shift register SCIRXSHF to this register. As this transfer occurs, the RXRDY flag is set and a receive interrupt is generated if RX INT ENA [SCISETINT0.9] is set. When the data is read from SCIRD, the RXRDY flag is automatically cleared. When the SCI receives data that is fewer than eight bits in length, it loads the data into this register in a left justified format padded with trailing zeros. Therefore, your software should perform a logical shift on the data by the correct number of positions to make it right justified.

4.12.15 LIN_SCITD Registers

4.12.15.1 LIN_SCITD Register (Offset = 38h) [reset = 0h]

Short Description: The SCITD register is whe

Long Description: The SCITD register is where data to be transmitted is written to by application software.

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Table 4-1241. Instance Table

Instance Name	Physical Address
LIN0	5240 0038h
LIN1	5240 1038h
LIN2	5240 2038h
LIN3	5240 3038h
LIN4	5240 4038h

Figure 4-541. SCITD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1								TD							
R								R/W							
0h								0h							

Access Types Legend

Table 4-1242. SCITD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_1	R	0h	Reserved
7:0	TD	R/W	0h	Transmit data This bit is effective in SCI-compatible mode only. Data to be transmitted is written to this register. The transfer of data from this register to the transmit shift register SCITXSHF sets the TXRDY flag [SCIFLR.23], which indicates that SCITD is ready to be loaded with another byte of data. Note: If TX INT ENA [SCISETINT.8] is set, this data transfer also causes an interrupt. Note: Data written to the SCIRD register that is fewer than eight bits long must be right justified, but it does not need to be padded with leading zeros.

4.12.16 LIN_SCIPIO0 Registers

4.12.16.1 LIN_SCIPIO0 Register (Offset = 3Ch) [reset = 0h]

Short Description: The SCIPIO0 register is u

Long Description: The SCIPIO0 register is used to enable the LINTX and LINRX pins.

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Table 4-1243. Instance Table

Instance Name	Physical Address
LIN0	5240 003Ch
LIN1	5240 103Ch
LIN2	5240 203Ch
LIN3	5240 303Ch
LIN4	5240 403Ch

Figure 4-542. SCIPIO0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2													TXFUNC	RXFUNC	RESERVED_1
R													R/W	R/W	R
0h													0h	0h	0h

Access Types Legend

Table 4-1244. SCIPIO0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_3	R	0h	Reserved
15:3	RESERVED_2	R	0h	Reserved
2	TXFUNC	R/W	0h	Transmit pin function. This bit is effective in LIN or SCI mode. This bit defines the function of LINTX pin. 1 LINTX_ENABLED LINTX pin is enabled.
1	RXFUNC	R/W	0h	Receive pin function. This bit is effective in LIN or SCI mode. This bit defines the function of the LINRX pin. 1 LINRX_ENABLED LINRX pin is enabled.
0	RESERVED_1	R	0h	Reserved

4.12.17 LIN_SCIPIO1 Registers

4.12.17.1 LIN_SCIPIO1 Register (Offset = 40h) [reset = 0h]

Short Description: Pin control Register 1

Long Description: Pin control Register 1

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Table 4-1245. Instance Table

Instance Name	Physical Address
LIN0	5240 0040h
LIN1	5240 1040h
LIN2	5240 2040h
LIN3	5240 3040h
LIN4	5240 4040h

Figure 4-543. SCIPIO1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2													TXDIR	RXDIR	RESERVED_1
R													R/W	R/W	R
0h													0h	0h	0h

Access Types Legend

Table 4-1246. SCIPIO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_3	R	0h	Reserved
15:3	RESERVED_2	R	0h	Reserved
2	TXDIR	R/W	0h	Transmit pin direction. This bit is effective in LIN or SCI mode. This bit determines the data direction on the LINTX pin if it is configured with general-purpose I/O functionality [TX FUNC = 0]. 0: general purpose input pin. 1: general-purpose output pin
1	RXDIR	R/W	0h	Receive pin direction. This bit is effective in LIN or SCI mode. This bit determines the data direction on the LINRX pin if it is configured with general-purpose I/O functionality [RX FUNC = 0]. 0: general purpose input pin. 1: general-purpose output pin
0	RESERVED_1	R	0h	Reserved

4.12.18 LIN_SCIPIO2 Registers

4.12.18.1 LIN_SCIPIO2 Register (Offset = 44h) [reset = 0h]

Short Description: The SCIPIO2 register indi

Long Description: The SCIPIO2 register indicates the current status of the LINTX and LINRX pins.

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Table 4-1247. Instance Table

Instance Name	Physical Address
LIN0	5240 0044h
LIN1	5240 1044h
LIN2	5240 2044h
LIN3	5240 3044h
LIN4	5240 4044h

Figure 4-544. SCIPIO2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2													TXIN	RXIN	RESERVED_1
R													R	R	R
0h													0h	0h	0h

Access Types Legend

Table 4-1248. SCIPIO2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_3	R	0h	Reserved
15:3	RESERVED_2	R	0h	Reserved
2	TXIN	R	0h	Transmit data in. This bit is effective in LIN or SCI-compatible mode. This bit contains the current value on the LINTX pin.
1	RXIN	R	0h	Receive data in. This bit is effective in LIN or SCI-compatible mode. This bit contains the current value on the LINRX pin.
0	RESERVED_1	R	0h	Reserved

4.12.19 LIN_SCIPIO3 Registers

4.12.19.1 LIN_SCIPIO3 Register (Offset = 48h) [reset = 0h]

Short Description: Pin control Register 3

Long Description: Pin control Register 3

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Table 4-1249. Instance Table

Instance Name	Physical Address
LIN0	5240 0048h
LIN1	5240 1048h
LIN2	5240 2048h
LIN3	5240 3048h
LIN4	5240 4048h

Figure 4-545. SCIPIO3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2													TXOUT	RXOUT	RESERVED_1
R													R/W	R/W	R
0h													0h	0h	0h

Access Types Legend

Table 4-1250. SCIPIO3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_3	R	0h	Reserved
15:3	RESERVED_2	R	0h	Reserved
2	TXOUT	R/W	0h	Transmit pin out. This bit is effective in LIN or SCI mode. This pin specifies the logic to be output on pin LINTX.
1	RXOUT	R/W	0h	Receive pin out. This bit is effective in LIN or SCI mode. This pin specifies the logic to be output on pin LINRX.
0	RESERVED_1	R	0h	Reserved

4.12.20 LIN_SCIPIO4 Registers

4.12.20.1 LIN_SCIPIO4 Register (Offset = 4Ch) [reset = 0h]

Short Description: Pin control Register 4

Long Description: Pin control Register 4

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Table 4-1251. Instance Table

Instance Name	Physical Address
LIN0	5240 004Ch
LIN1	5240 104Ch
LIN2	5240 204Ch
LIN3	5240 304Ch
LIN4	5240 404Ch

Figure 4-546. SCIPIO4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2													TXSET	RXSET	RESERVED_1
R													R/W1TS	R/W1TS	R
0h													0h	0h	0h

Access Types Legend

Table 4-1252. SCIPIO4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_3	R	0h	Reserved
15:3	RESERVED_2	R	0h	Reserved
2	TXSET	R/W1TS	0h	Transmit pin set. This bit is effective in LIN or SCI mode. This bit sets the logic to be output on pin LINTX.
1	RXSET	R/W1TS	0h	Receive pin set. This bit is effective in LIN or SCI mode. This bit sets the logic to be output on pin LINRX.
0	RESERVED_1	R	0h	Reserved

4.12.21 LIN_SCIPIO5 Registers

4.12.21.1 LIN_SCIPIO5 Register (Offset = 50h) [reset = 0h]

Short Description: Pin control Register 5

Long Description: Pin control Register 5

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Table 4-1253. Instance Table

Instance Name	Physical Address
LIN0	5240 0050h
LIN1	5240 1050h
LIN2	5240 2050h
LIN3	5240 3050h
LIN4	5240 4050h

Figure 4-547. SCIPIO5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2													TXCLR	RXCLR	RESERVED_1
R													R/W1TC	R/W1TC	R
0h													0h	0h	0h

Access Types Legend

Table 4-1254. SCIPIO5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_3	R	0h	Reserved
15:3	RESERVED_2	R	0h	Reserved
2	TXCLR	R/W1TC	0h	Transmit pin clear. This bit is effective in LIN or SCI mode. This bit clears the logic to be output on pin LINTX.
1	RXCLR	R/W1TC	0h	Receive pin clear. This bit is effective in LIN or SCI mode. This bit clears the logic to be output on pin LINRX.
0	RESERVED_1	R	0h	Reserved

4.12.22 LIN_SCIPIO6 Registers

4.12.22.1 LIN_SCIPIO6 Register (Offset = 54h) [reset = 0h]

Short Description: Pin control Register 6

Long Description: Pin control Register 6

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Table 4-1255. Instance Table

Instance Name	Physical Address
LIN0	5240 0054h
LIN1	5240 1054h
LIN2	5240 2054h
LIN3	5240 3054h
LIN4	5240 4054h

Figure 4-548. SCIPIO6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2													TXPDR	RXPDR	RESERVED_1
R													R/W	R/W	R
0h													0h	0h	0h

Access Types Legend

Table 4-1256. SCIPIO6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_3	R	0h	Reserved
15:3	RESERVED_2	R	0h	Reserved
2	TXPDR	R/W	0h	Transmit pin open drain enable. This bit is effective in LIN or SCI mode. This bit enables open-drain capability in the output pin LINTX.
1	RXPDR	R/W	0h	Receive pin open drain enable. This bit is effective in LIN or SCI mode. This bit enables open-drain capability in the output pin LINRX.
0	RESERVED_1	R	0h	Reserved

4.12.23 LIN_SCIPIO7 Registers

4.12.23.1 LIN_SCIPIO7 Register (Offset = 58h) [reset = 0h]

Short Description: Pin control Register 7

Long Description: Pin control Register 7

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Table 4-1257. Instance Table

Instance Name	Physical Address
LIN0	5240 0058h
LIN1	5240 1058h
LIN2	5240 2058h
LIN3	5240 3058h
LIN4	5240 4058h

Figure 4-549. SCIPIO7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2													TXPD	RXPD	RESERVED_1
R													R/W	R/W	R
0h													0h	0h	0h

Access Types Legend

Table 4-1258. SCIPIO7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_3	R	0h	Reserved
15:3	RESERVED_2	R	0h	Reserved
2	TXPD	R/W	0h	Transmit pin pull control disable. This bit is effective in LIN or SCI mode. This bit disables pull control capability on the input pin LINTX.
1	RXPD	R/W	0h	Receive pin pull control disable. This bit is effective in LIN or SCI mode. This bit disables pull control capability on the input pin LINRX.
0	RESERVED_1	R	0h	Reserved

4.12.24 LIN_SCIPIO8 Registers

4.12.24.1 LIN_SCIPIO8 Register (Offset = 5Ch) [reset = 7h]

Short Description: Pin control Register 8

Long Description: Pin control Register 8

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Table 4-1259. Instance Table

Instance Name	Physical Address
LIN0	5240 005Ch
LIN1	5240 105Ch
LIN2	5240 205Ch
LIN3	5240 305Ch
LIN4	5240 405Ch

Figure 4-550. SCIPIO8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2													TXPSL	RXPSL	RESERVED_1
R													R/W	R/W	R
0h													1h	1h	1h

Access Types Legend

Table 4-1260. SCIPIO8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_3	R	0h	Reserved
15:3	RESERVED_2	R	0h	Reserved
2	TXPSL	R/W	1h	TX pin pull select. This bit is effective in LIN or SCI mode. This bit selects pull type in the input pin LINTX.
1	RXPSL	R/W	1h	RX pin pull select. This bit is effective in LIN or SCI mode. This bit selects pull type in the input pin LINRX.
0	RESERVED_1	R	1h	Reserved

4.12.25 LIN_LINCOMP Registers

4.12.25.1 LIN_LINCOMP Register (Offset = 60h) [reset = 0h]

Short Description: The LINCOMPARE register i

Long Description: The LINCOMPARE register is used to configure the sync delimeter and sync break extension.

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Table 4-1261. Instance Table

Instance Name	Physical Address
LIN0	5240 0060h
LIN1	5240 1060h
LIN2	5240 2060h
LIN3	5240 3060h
LIN4	5240 4060h

Figure 4-551. LINCOMP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2						SDEL		RESERVED_1					SBREAK		
R						R/W		R					R/W		
0h						0h		0h					0h		

Access Types Legend

Table 4-1262. LINCOMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_3	R	0h	Reserved
15:10	RESERVED_2	R	0h	Reserved
9:8	SDEL	R/W	0h	2-bit Sync Delimiter compare. These bits are effective in LIN mode only. These bits are used to configure the number of Tbit for the sync delimiter in the sync field. The time delay calculation for the synchronization delimiter is: TSDEL = [SDEL + 1]Tbit These bits are writable in LIN mode only. 3 SDEL_4 The sync delimiter has 4 Tbit. 2 SDEL_3 The sync delimiter has 3 Tbit. 1 SDEL_2 The sync delimiter has 2 Tbit.
7:3	RESERVED_1	R	0h	Reserved
2:0	SBREAK	R/W	0h	3-bit Sync Break extend. LIN mode only. These bits are used to configure the number of Tbits for the sync break to extend the minimum 13 Tbit in the Sync Field to a maximum of 20 Tbit. The time delay calculation for the sync break is: TSYNBRK = 13Tbit + SBREAK x Tbit These bits are writable in LIN mode only. 7 SBREAK_7 The sync break has 7 additional Tbit. 6 SBREAK_6 The sync break has 6 additional Tbit. 5 SBREAK_5 The sync break has 5 additional Tbit. 4 SBREAK_4 The sync break has 4 additional Tbit. 3 SBREAK_3 The sync break has 3 additional Tbit. 2 SBREAK_2 The sync break has 2 additional Tbit. 1 SBREAK_1 The sync break has 1 additional Tbit.

4.12.26 LIN_LINRD0 Registers

4.12.26.1 LIN_LINRD0 Register (Offset = 64h) [reset = 0h]

Short Description: The LINRD0 register conta

Long Description: The LINRD0 register contains the lower 4 bytes of the received LIN frame data.

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Table 4-1263. Instance Table

Instance Name	Physical Address
LIN0	5240 0064h
LIN1	5240 1064h
LIN2	5240 2064h
LIN3	5240 3064h
LIN4	5240 4064h

Figure 4-552. LINRD0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RD0								RD1							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RD2								RD3							
R								R							
0h								0h							

Access Types Legend

Table 4-1264. LINRD0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RD0	R	0h	8-bit Receive Buffer 0 Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received. A read of this byte clears the RXDY byte. Note: RD<x-1> is equivalent to Data byte <x> of the LIN frame.
23:16	RD1	R	0h	8-bit Receive Buffer 1. Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.
15:8	RD2	R	0h	8-bit Receive Buffer 2. Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.
7:0	RD3	R	0h	8-bit Receive Buffer 3. Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.

4.12.27 LIN_LINRD1 Registers

4.12.27.1 LIN_LINRD1 Register (Offset = 68h) [reset = 0h]

Short Description: The LINRD1 regsiter conta

Long Description: The LINRD1 regsiter contains the upper 4 bytes of the received LIN frame data.

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Table 4-1265. Instance Table

Instance Name	Physical Address
LIN0	5240 0068h
LIN1	5240 1068h
LIN2	5240 2068h
LIN3	5240 3068h
LIN4	5240 4068h

Figure 4-553. LINRD1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RD4								RD5							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RD6								RD7							
R								R							
0h								0h							

Access Types Legend

Table 4-1266. LINRD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RD4	R	0h	8-bit Receive Buffer 4 Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.
23:16	RD5	R	0h	8-bit Receive Buffer 5. Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.
15:8	RD6	R	0h	8-bit Receive Buffer 6. Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.
7:0	RD7	R	0h	8-bit Receive Buffer 7. Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.

4.12.28 LIN_LINMASK Registers

4.12.28.1 LIN_LINMASK Register (Offset = 6Ch) [reset = 0h]

Short Description: The LINMASK register is u

Long Description: The LINMASK register is used to configure the masks used for filtering incoming ID messages for receive and transmit frames.

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Table 4-1267. Instance Table

Instance Name	Physical Address
LIN0	5240 006Ch
LIN1	5240 106Ch
LIN2	5240 206Ch
LIN3	5240 306Ch
LIN4	5240 406Ch

Figure 4-554. LINMASK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_2								RXIDMASK							
R								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1								TXIDMASK							
R								R/W							
0h								0h							

Access Types Legend

Table 4-1268. LINMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_2	R	0h	Reserved
23:16	RXIDMASK	R/W	0h	Receive ID mask. This field is effective in LIN mode only.This 8-bit mask is used for filtering an incoming ID message and compare it to the ID-byte. A compare match of the received ID witht the RX ID mask will set the ID RX flag and trigger and ID interrupt if enabled. A 0 bit in the mask indicates that bit is compared to the ID-byte. A 1 bit in the mask indicates that that bit is filtered and therefore not used in the compare. When HGENCTRL is set to 1, this field must be set to 0xFF.
15:8	RESERVED_1	R	0h	Reserved
7:0	TXIDMASK	R/W	0h	Transmit ID mask. This field is effective in LIN mode only. This 8-bit mask is used for filtering an incoming ID message and compare it to the ID-byte. A compare match of the received ID with the TX ID Mask will set the ID TX flag and trigger an ID interrupt if enabled. A 0 bit in the mask indicates that bit is compared to the ID-byte. A 1 bit in the mask indicates that bit is filtered and therefore not used for the compare. When HGENCTRL is set to 1, this field must be set to 0xFF.

4.12.29 LIN_LINID Registers

4.12.29.1 LIN_LINID Register (Offset = 70h) [reset = 0h]

Short Description: The LINID register contai

Long Description: The LINID register contains the identification fields for LIN communication.
NOTE: For software compatibility with future LIN modules, the HGEN CTRL bit must be set to 1, the RX ID MASK field must be set to FFh, and the TX ID MASK field must be set to FFh.

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Table 4-1269. Instance Table

Instance Name	Physical Address
LIN0	5240 0070h
LIN1	5240 1070h
LIN2	5240 2070h
LIN3	5240 3070h
LIN4	5240 4070h

Figure 4-555. LINID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1								RECEIVEDID							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IDSLAVETASKBYTE								IDBYTE							
R/W								R/W							
0h								0h							

Access Types Legend

Table 4-1270. LINID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_1	R	0h	Reserved
23:16	RECEIVEDID	R	0h	Received ID. This bit is effective in LIN mode only. This byte contains the current message identifier. During header reception the received ID is copied from the SCIRXSHF register to this byte if there is no ID-parity error and there has been an RX/TX match. Note: If a framing error [FE] is detected during ID reception, the received ID will also not be copied to the LINID register.
15:8	IDSLAVETASKBYTE	R/W	0h	ID Slave Task byte. This field is effective in LIN mode only. This byte contains the identifier to which the received ID of an incoming header will be compared in order to decide whether a RX response, a TX response, or no action needs to be done by the LIN node. These bits are writable in LIN mode only.
7:0	IDBYTE	R/W	0h	ID byte. This field is effective in LIN mode only. This byte is the LIN mode message ID. On a master node, a write to this register by the CPU initiates a header transmission. For a slave task, this byte is used for message filtering when HGENCTRL [SCIGCR1.12] is '0'. These bits are writable in LIN mode only.

4.12.30 LIN_LINTD0 Registers

4.12.30.1 LIN_LINTD0 Register (Offset = 74h) [reset = 0h]

Short Description: The LINTD0 register conta

Long Description: The LINTD0 register contains the lower 4 bytes of the data to be transmitted.
NOTE: TD<x-1> is equivalent to Data byte <x> of the LIN frame.

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Table 4-1271. Instance Table

Instance Name	Physical Address
LIN0	5240 0074h
LIN1	5240 1074h
LIN2	5240 2074h
LIN3	5240 3074h
LIN4	5240 4074h

Figure 4-556. LINTD0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TD0								TD1							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TD2								TD3							
R/W								R/W							
0h								0h							

Access Types Legend

Table 4-1272. LINTD0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TD0	R/W	0h	8-bit Transmit Buffer 0. Byte 0 to be transmitted is written into this register and then copied to SCITXSHF for transmission. Once byte 0 is written in TDO buffer, transmission will be initiated.
23:16	TD1	R/W	0h	8-bit Transmit Buffer 3. Byte 1 to be transmitted is written into this register and then copied to SCITXSHF for transmission.
15:8	TD2	R/W	0h	8-bit Transmit Buffer 2. Byte 2 to be transmitted is written into this register and then copied to SCITXSHF for transmission.
7:0	TD3	R/W	0h	8-bit Transmit Buffer 3. Byte 3 to be transmitted is written into this register and then copied to SCITXSHF for transmission.

4.12.31 LIN_LINTD1 Registers

4.12.31.1 LIN_LINTD1 Register (Offset = 78h) [reset = 0h]

Short Description: The LINTD1 register conta

Long Description: The LINTD1 register contains the upper 4 bytes of the data to be transmitted.
NOTE: TD<x-1> is equivalent to Data byte <x> of the LIN frame.

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Table 4-1273. Instance Table

Instance Name	Physical Address
LIN0	5240 0078h
LIN1	5240 1078h
LIN2	5240 2078h
LIN3	5240 3078h
LIN4	5240 4078h

Figure 4-557. LINTD1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TD4								TD5							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TD6								TD7							
R/W								R/W							
0h								0h							

Access Types Legend

Table 4-1274. LINTD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TD4	R/W	0h	8-bit Transmit Buffer 4. Byte4 to be transmitted is written into this register and then copied to SCITXSHF for transmission.
23:16	TD5	R/W	0h	8-bit Transmit Buffer 5. Byte 5 to be transmitted is written into this register and then copied to SCITXSHF for transmission.
15:8	TD6	R/W	0h	8-bit Transmit Buffer 6. Byte 6 to be transmitted is written into this register and then copied to SCITXSHF for transmission.
7:0	TD7	R/W	0h	8-bit Transmit Buffer 7. Byte 7 to be transmitted is written into this register and then copied to SCITXSHF for transmission.

4.12.32 LIN_MBRSR Registers

4.12.32.1 LIN_MBRSR Register (Offset = 7Ch) [reset = dach]

Short Description: The MBRSR register is use

Long Description: The MBRSR register is used to configure the expected maximum baud rate of the LIN network.

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Table 4-1275. Instance Table

Instance Name	Physical Address
LIN0	5240 007Ch
LIN1	5240 107Ch
LIN2	5240 207Ch
LIN3	5240 307Ch
LIN4	5240 407Ch

Figure 4-558. MBRSR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1			MBR												
R			R/W												
0h			dach												

Access Types Legend

Table 4-1276. MBRSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_1	R	0h	Reserved
12:0	MBR	R/W	DACh	Maximum Baud Rate Prescaler. This field is effective in LIN mode only. This 13-bit prescaler is used during the synchronization phase [see the "Header Reception and Adaptive Baudrate" section] of a slave module if the ADAPT bit is set. In this way, a SCI/LIN slave using an automatic or select bit rate modes detects any LIN bus legal rate automatically. The MBR value should be programmed to allow a maximum baud rate that is not more than 10% above the expected operating baud rate in the LIN network. Otherwise a s 0x00 data byte could mistakenly be detected as sync break. The default value is for a 70MHz LINCLK [0xDAC]. This MBR prescaler is used by the wake-up and idle time counters for a constant expiration time relative to a 20kHz rate.

4.12.33 LIN_RESERVED_N Registers

4.12.33.1 LIN_N Register (Offset = 94h) [reset = 0h]

Short Description: tbd

Long Description: tbd

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Offset = 94h + (j * 4h); where j = 0h to 12h

Table 4-1277. Instance Table

Instance Name	Physical Address
LIN0	5240 0094h
LIN1	5240 1094h
LIN2	5240 2094h
LIN3	5240 3094h
LIN4	5240 4094h

Figure 4-559. RESERVED_N Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
NONE															
0															

Access Types Legend

Table 4-1278. RESERVED_N Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE		Reserved

4.12.34 LIN_IODFTCTRL Registers

4.12.34.1 LIN_IODFTCTRL Register (Offset = 90h) [reset = 500h]

Short Description: The IODFTCTRL register is

Long Description: The IODFTCTRL register is used to emulate various error and test conditions.

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Table 4-1279. Instance Table

Instance Name	Physical Address
LIN0	5240 0090h
LIN1	5240 1090h
LIN2	5240 2090h
LIN3	5240 3090h
LIN4	5240 4090h

Figure 4-560. IODFTCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BERRENA	PBERRENA	CERRENA	ISFERRENA	RESERVED_4	FERRENA	PERRENA	BRKDTERRENA	RESERVED_3			PINSAMPLEMASK		TXSHIFT		
R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W			R/W		R/W		
0h	0h	0h	0h	0h	0h	0h	0h	0h			0h		0h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2				IODFTENA				RESERVED_1						LPBENA	RXPENA
R				R/W				R						R/W	R/W
0h				5h				0h						0h	0h

Access Types Legend

Table 4-1280. IODFTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BERRENA	R/W	0h	Bit Errror Enable bit. This bit is effective in LIN mode only. This bit is used to create a Bit error. When this bit is set, the bit received is ORed with 1 and passed to the Bit monitor circuitry.
30	PBERRENA	R/W	0h	Physical Bus Error Enable bit. This bit is effective in LIN mode only. This bit is used to create a Physical Bus Error. When this bit is set, the bit received during Sync Break field transmission is ORed with 1 and passed to the Bit monitor circuitry
29	CERRENA	R/W	0h	Checksum Error Enable bit. This bit is effective in LIN mode only. This bit is used to create a checksum error. When this bit is set, the polarity of the CTYPE [checksum type] in the receive checksum calculator is changed so that a checksum error is generated.
28	ISFERRENA	R/W	0h	Inconsistent Sync Field Error Enable bit. This bit is effective in LIN mode only. This bit is used to create an ISF error. When this bit is set, the bit widths in the sync field are varied so that the ISF check fails and the error flag is set.
27	RESERVED_4	R	0h	Reserved
26	FERRENA	R/W	0h	This bit is used to create a Frame Error. This bit is effective in SCI-compatible mode only. When this bit is set, the stop bit received is ANDed with '0' and passed to the stop bit check circuitry.
25	PERRENA	R/W	0h	Compatible Mode only This bit is effective in SCI-compatible mode only. This bit is used to create a Parity Error. When this bit is set, in compatible mode, the parity bit received is toggled so that a parity error occurs.

Table 4-1280. IODFTCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	BRKDTERRENA	R/W	0h	Compatible Mode only This bit is effective in SCI-compatible mode only. This bit is used to create BRKDT error [SCI mode only]. When this bit is set, the stop bit of the frame is ANDed with '0' and passed to the RSM so that a frame error occurs. Then the RX Pin is forced to continuous low for 10 Tbits so that a BRKDT error occurs.
23:21	RESERVED_3	R/W	0h	Reserved
20:19	PINSAMPLEMASK	R/W	0h	Pin sample mask. These bits define the sample number at which the TX Pin value that is being transmitted will be inverted to verify the receive pin samples correctly with the majority detection circuitry. Note: During IODFT mode testing for the pin sample mask, the prescalar P must be programmed to be greater than 2. 3 PINSAMPLEMASK_2SCLK Invert the TX Pin value at TBIT_CENTER + 2 SCLK 2 PINSAMPLEMASK_SCLK Invert the TX Pin value at TBIT_CENTER + SCLK 1 PINSAMPLEMASK_TBIT Invert the TX Pin value at TBIT_CENTER
18:16	TXSHIFT	R/W	0h	Transmit shift. These bits define the delay by which the value on LINTX is delayed so that the value on LINRX is asynchronous. [Not applicable to Start Bit] 7 TXSHIFT_DELAY_7 Delay by 7 SCLK 6 TXSHIFT_DELAY_6 Delay by 6 SCLK 5 TXSHIFT_DELAY_5 Delay by 5 SCLK 4 TXSHIFT_DELAY_4 Delay by 4 SCLK 3 TXSHIFT_DELAY_3 Delay by 3 SCLK 2 TXSHIFT_DELAY_2 Delay by 2 SCLK 1 TXSHIFT_DELAY_1 Delay by 1 SCLK
15:12	RESERVED_2	R	0h	Reserved
11:8	IODFTENA	R/W	5h	IO DFT Enable Key This field is used to enable the IODFT mode of the SCI/LIN module for testing. 15 IODFTENA_DISABLE_15 IODFT is disabled 14 IODFTENA_DISABLE_14 IODFT is disabled 13 IODFTENA_DISABLE_13 IODFT is disabled 12 IODFTENA_DISABLE_12 IODFT is disabled 11 IODFTENA_DISABLE_11 IODFT is disabled 10 IODFTENA_DISABLE_10 IODFT is enabled 9 IODFTENA_DISABLE_9 IODFT is disabled 8 IODFTENA_DISABLE_8 IODFT is disabled 7 IODFTENA_DISABLE_7 IODFT is disabled 6 IODFTENA_DISABLE_6 IODFT is disabled 5 IODFTENA_DISABLE_5 IODFT is disabled 4 IODFTENA_DISABLE_4 IODFT is disabled 3 IODFTENA_DISABLE_3 IODFT is disabled 2 IODFTENA_DISABLE_2 IODFT is disabled 1 IODFTENA_DISABLE_1 IODFT is disabled
7:2	RESERVED_1	R	0h	Reserved
1	LPBENA	R/W	0h	Module loopback enable. In analog loopback mode the complete communication path through the I/Os can be tested, whereas in digital loopback mode the I/O buffers are excluded from this path. 1 LPBENA_ANALOG Analog loopback is enabled in module I/O DFT mode (when IODFTENA = 1010)
0	RXPENA	R/W	0h	Module Analog loopback through receive pin enable. This bit defines whether the I/O buffers for the transmit or the receive pin are included in the communication path in analog loopback mode only. 1 RXPENA_RECEIVE Analog loopback through the receive pin is enabled.

4.12.35 LIN_LIN_GLB_INT_EN Registers

4.12.35.1 LIN_GLB_INT_EN Register (Offset = E0h) [reset = 0h]

Short Description: The LIN_GLB_INT_EN regist

Long Description: The LIN_GLB_INT_EN register is used to enable the INT0 and INT1 interrupt lines to propagate to the PIE block.

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Table 4-1281. Instance Table

Instance Name	Physical Address
LIN0	5240 00E0h
LIN1	5240 10E0h
LIN2	5240 20E0h
LIN3	5240 30E0h
LIN4	5240 40E0h

Figure 4-561. LIN_GLB_INT_EN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1														GLBINT1_EN	GLBINT0_EN
R														R/W	R/W
0h														0h	0h

Access Types Legend

Table 4-1282. LIN_GLB_INT_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED_1	R	0h	Reserved
1	GLBINT1_EN	R/W	0h	Global Interrupt Enable for LIN INT1. This bit determines whether the INT1 interrupt line generates an interrupt to the PIE or not 1 GLBINT1_ENABLED LIN INT1 line generates an interrupt to the PIE if an enabled interrupt condition occurs.
0	GLBINT0_EN	R/W	0h	Global Interrupt Enable for LIN INT0. This bit determines whether the INT0 interrupt line generates an interrupt to the PIE or not. 1 GLBINT0_ENABLED LIN INT0 line generates an interrupt to the PIE if an enabled interrupt condition occurs.

4.12.36 LIN_LIN_GLB_INT_FLG Registers

4.12.36.1 LIN_GLB_INT_FLG Register (Offset = E4h) [reset = 0h]

Short Description: The LIN_GLB_INT_FLG regis

Long Description: The LIN_GLB_INT_FLG register contains the current status of the INT0 and INT1 flags.

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Table 4-1283. Instance Table

Instance Name	Physical Address
LIN0	5240 00E4h
LIN1	5240 10E4h
LIN2	5240 20E4h
LIN3	5240 30E4h
LIN4	5240 40E4h

Figure 4-562. LIN_GLB_INT_FLG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1														INT1_FLG	INT0_FLG
R														R	R
0h														0h	0h

Access Types Legend

Table 4-1284. LIN_GLB_INT_FLG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED_1	R	0h	Reserved
1	INT1_FLG	R	0h	Global Interrupt Flag for LIN INT1. This bit indicates if an interrupt was generated to the PIE due to an enabled interrupt on the INT1 interrupt line. Refer to the LIN Interrupt Status Register for the condition that generated the interrupt. This bit can be cleared by writing a 1 to the corresponding bit in the LIN_GLB_INT_CLR register. 1 INT1_FLG_GENERATED An interrupt was generated due to an enabled interrupt on the INT1 interrupt line.
0	INT0_FLG	R	0h	Global Interrupt Flag for LIN INT0. This bit indicates if an interrupt was generated to the PIE due to an enabled interrupt on the INT0 interrupt line. Refer to the LIN Interrupt Status Register for the condition that generated the interrupt. This bit can be cleared by writing a 1 to the corresponding bit in the LIN_GLB_INT_CLR register. 1 INT0_FLG_GENERATED An interrupt was generated due to an enabled interrupt on the INT0 interrupt line.

4.12.37 LIN_LIN_GLB_INT_CLR Registers

4.12.37.1 LIN_GLB_INT_CLR Register (Offset = E8h) [reset = 0h]

Short Description: The LIN_GLB_INT_CLR regis

Long Description: The LIN_GLB_INT_CLR register is used to clear the interrupt flags in LIN_GLB_INT_FLG register.

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Table 4-1285. Instance Table

Instance Name	Physical Address
LIN0	5240 00E8h
LIN1	5240 10E8h
LIN2	5240 20E8h
LIN3	5240 30E8h
LIN4	5240 40E8h

Figure 4-563. LIN_GLB_INT_CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1														INT1_FLG_CLR	INT0_FLG_CLR
R														R/W1TC	R/W1TC
0h														0h	0h

Access Types Legend

Table 4-1286. LIN_GLB_INT_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED_1	R	0h	Reserved
1	INT1_FLG_CLR	R/W1TC	0h	Global Interrupt flag clear for LIN INT1. This bit is used to clear the corresponding bit in the LIN_GLB_INT_FLG register. Write 1 to clear the INT1_FLG bit. Writing 0 has no effect.
0	INT0_FLG_CLR	R/W1TC	0h	Global Interrupt flag clear for LIN INT0. This bit is used to clear the corresponding bit in the LIN_GLB_INT_FLG register. Write 1 to clear the INT0_FLG bit. Writing 0 has no effect.

4.12.38 Access Table

Table 4-1287. Access Type Codes

Access Type	Code	Description
R	R	Read
R/W	R/W	Read / Write
R/W1TS	R/W1TS	Read/Write 1 To Set
R/W1TC	R/W1TC	Read/Write 1 To Clear

4.13 MCAN Registers

Table 4-1288. MSG_RAM, MSG_RAM Registers, Base Address=0X0000000052600000, Length=32768

Offset	Length	Register Name	MCAN0 Physical Address	MCAN1 Physical Address	MCAN2 Physical Address
0h	32	START	5260 0000h	5261 0000h	5262 0000h
10FFCh	32	END	5261 0FFCh	5262 0FFCh	5263 0FFCh

Table 4-1289. CFG, CFG Registers, Base Address=0X0000000052608000, Length=1024

Offset	Length	Register Name	MCAN0 Physical Address	MCAN1 Physical Address	MCAN2 Physical Address
0h	32	SS_PID	5260 8000h	5261 8000h	5262 8000h
4h	32	SS_CTRL	5260 8004h	5261 8004h	5262 8004h
8h	32	SS_STAT	5260 8008h	5261 8008h	5262 8008h
Ch	32	SS_ICS	5260 800Ch	5261 800Ch	5262 800Ch
10h	32	SS_IRS	5260 8010h	5261 8010h	5262 8010h
14h	32	SS_IECS	5260 8014h	5261 8014h	5262 8014h
18h	32	SS_IE	5260 8018h	5261 8018h	5262 8018h
1Ch	32	SS_IES	5260 801Ch	5261 801Ch	5262 801Ch
20h	32	SS_EOI	5260 8020h	5261 8020h	5262 8020h
24h	32	SS_EXT_TS_PS	5260 8024h	5261 8024h	5262 8024h
28h	32	SS_EXT_TS_USIC	5260 8028h	5261 8028h	5262 8028h
200h	32	CREL	5260 8200h	5261 8200h	5262 8200h
204h	32	ENDN	5260 8204h	5261 8204h	5262 8204h
208h	32	CUST	5260 8208h	5261 8208h	5262 8208h
20Ch	32	DBTP	5260 820Ch	5261 820Ch	5262 820Ch
210h	32	TEST	5260 8210h	5261 8210h	5262 8210h
214h	32	RWD	5260 8214h	5261 8214h	5262 8214h
218h	32	CCCR	5260 8218h	5261 8218h	5262 8218h
21Ch	32	NBTP	5260 821Ch	5261 821Ch	5262 821Ch
220h	32	TSCC	5260 8220h	5261 8220h	5262 8220h
224h	32	TSCV	5260 8224h	5261 8224h	5262 8224h
228h	32	TOCC	5260 8228h	5261 8228h	5262 8228h
22Ch	32	TOCV	5260 822Ch	5261 822Ch	5262 822Ch
230h	32	RES00	5260 8230h	5261 8230h	5262 8230h
234h	32	RES01	5260 8234h	5261 8234h	5262 8234h
238h	32	RES02	5260 8238h	5261 8238h	5262 8238h
23Ch	32	RES03	5260 823Ch	5261 823Ch	5262 823Ch
240h	32	ECR	5260 8240h	5261 8240h	5262 8240h
244h	32	PSR	5260 8244h	5261 8244h	5262 8244h
248h	32	TDCR	5260 8248h	5261 8248h	5262 8248h
24Ch	32	RES04	5260 824Ch	5261 824Ch	5262 824Ch
250h	32	IR	5260 8250h	5261 8250h	5262 8250h
254h	32	IE	5260 8254h	5261 8254h	5262 8254h
258h	32	ILS	5260 8258h	5261 8258h	5262 8258h
25Ch	32	ILE	5260 825Ch	5261 825Ch	5262 825Ch
260h	32	RES05	5260 8260h	5261 8260h	5262 8260h
264h	32	RES06	5260 8264h	5261 8264h	5262 8264h

Table 4-1289. CFG, CFG Registers, Base Address=0X0000000052608000, Length=1024 (continued)

Offset	Length	Register Name	MCAN0 Physical Address	MCAN1 Physical Address	MCAN2 Physical Address
268h	32	RES07	5260 8268h	5261 8268h	5262 8268h
26Ch	32	RES08	5260 826Ch	5261 826Ch	5262 826Ch
270h	32	RES09	5260 8270h	5261 8270h	5262 8270h
274h	32	RES10	5260 8274h	5261 8274h	5262 8274h
278h	32	RES11	5260 8278h	5261 8278h	5262 8278h
27Ch	32	RES12	5260 827Ch	5261 827Ch	5262 827Ch
280h	32	GFC	5260 8280h	5261 8280h	5262 8280h
284h	32	SIDFC	5260 8284h	5261 8284h	5262 8284h
288h	32	XIDFC	5260 8288h	5261 8288h	5262 8288h
28Ch	32	RES13	5260 828Ch	5261 828Ch	5262 828Ch
290h	32	XIDAM	5260 8290h	5261 8290h	5262 8290h
294h	32	HPMS	5260 8294h	5261 8294h	5262 8294h
298h	32	NDAT1	5260 8298h	5261 8298h	5262 8298h
29Ch	32	NDAT2	5260 829Ch	5261 829Ch	5262 829Ch
2A0h	32	RXF0C	5260 82A0h	5261 82A0h	5262 82A0h
2A4h	32	RXF0S	5260 82A4h	5261 82A4h	5262 82A4h
2A8h	32	RXF0A	5260 82A8h	5261 82A8h	5262 82A8h
2ACh	32	RXBC	5260 82ACh	5261 82ACh	5262 82ACh
2B0h	32	RXF1C	5260 82B0h	5261 82B0h	5262 82B0h
2B4h	32	RXF1S	5260 82B4h	5261 82B4h	5262 82B4h
2B8h	32	RXF1A	5260 82B8h	5261 82B8h	5262 82B8h
2BCh	32	RXESC	5260 82BCh	5261 82BCh	5262 82BCh
2C0h	32	TXBC	5260 82C0h	5261 82C0h	5262 82C0h
2C4h	32	TXFQS	5260 82C4h	5261 82C4h	5262 82C4h
2C8h	32	TXESC	5260 82C8h	5261 82C8h	5262 82C8h
2CCh	32	TXBRP	5260 82CCh	5261 82CCh	5262 82CCh
2D0h	32	TXBAR	5260 82D0h	5261 82D0h	5262 82D0h

Table 4-1290. ECC, ECC Registers, Base Address=0X0000000052700000, Length=1024

Offset	Length	Register Name	MCAN0 Physical Address	MCAN1 Physical Address	MCAN2 Physical Address
0h	32	REV	5270 0000h	5270 1000h	5270 2000h
8h	32	VECTOR	5270 0008h	5270 1008h	5270 2008h
Ch	32	STAT	5270 000Ch	5270 100Ch	5270 200Ch
14h	32	CTRL	5270 0014h	5270 1014h	5270 2014h
18h	32	ERR_CTRL1	5270 0018h	5270 1018h	5270 2018h
1Ch	32	ERR_CTRL2	5270 001Ch	5270 101Ch	5270 201Ch
20h	32	ERR_STAT1	5270 0020h	5270 1020h	5270 2020h
24h	32	ERR_STAT2	5270 0024h	5270 1024h	5270 2024h
28h	32	ERR_STAT3	5270 0028h	5270 1028h	5270 2028h
3Ch	32	SEC_EOI_REG	5270 003Ch	5270 103Ch	5270 203Ch
40h	32	SEC_STATUS_REG0	5270 0040h	5270 1040h	5270 2040h
80h	32	SEC_ENABLE_SET_REG0	5270 0080h	5270 1080h	5270 2080h
C0h	32	SEC_ENABLE_CLR_REG0	5270 00C0h	5270 10C0h	5270 20C0h
13Ch	32	DED_EOI_REG	5270 013Ch	5270 113Ch	5270 213Ch
140h	32	DED_STATUS_REG0	5270 0140h	5270 1140h	5270 2140h

Table 4-1290. ECC, ECC Registers, Base Address=0X0000000052700000, Length=1024 (continued)

Offset	Length	Register Name	MCAN0 Physical Address	MCAN1 Physical Address	MCAN2 Physical Address
180h	32	DED_ENABLE_SET_REG0	5270 0180h	5270 1180h	5270 2180h
1C0h	32	DED_ENABLE_CLR_REG0	5270 01C0h	5270 11C0h	5270 21C0h
200h	32	AGGR_ENABLE_SET	5270 0200h	5270 1200h	5270 2200h
204h	32	AGGR_ENABLE_CLR	5270 0204h	5270 1204h	5270 2204h
208h	32	AGGR_STATUS_SET	5270 0208h	5270 1208h	5270 2208h
20Ch	32	AGGR_STATUS_CLR	5270 020Ch	5270 120Ch	5270 220Ch

4.13.1 MSG_RAM_START Registers

4.13.1.1 MSG_START Register (Offset = 0h) [reset = 0h]

Short Description: START

Long Description: START

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Table 4-1291. Instance Table

Instance Name	Physical Address
MCAN0	5260 0000h
MCAN1	5261 0000h
MCAN2	5262 0000h
MCAN3	5263 0000h

Figure 4-564. START Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START															
R/W															
0h															

Access Types Legend

Table 4-1292. START Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START	R/W	0h	MCAN message mem Start address Reset Source: canfd_rst_mod_g_rst_n

4.13.2 MSG_RAM_END Registers

4.13.2.1 MSG_END Register (Offset = 10FFCh) [reset = 0h]

Short Description: END

Long Description: END

Return to Summary Table

Table 4-1293. Instance Table

Instance Name	Physical Address
MCAN0	5261 0FFCh
MCAN1	5262 0FFCh
MCAN2	5263 0FFCh
MCAN3	5264 0FFCh

Figure 4-565. END Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END															
R/W															
0h															

Access Types Legend

Table 4-1294. END Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END	R/W	0h	MCAN message mem End address Reset Source: canfd_rst_mod_g_rst_n

4.13.3 CFG_SS_PID Registers

4.13.3.1 CFG_PID Register (Offset = 0h) [reset = 68e05901h]

Short Description: SS_PID

Long Description: SS_PID

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Table 4-1295. Instance Table

Instance Name	Physical Address
MCAN0	5260 8000h
MCAN1	5261 8000h
MCAN2	5262 8000h
MCAN3	5263 8000h

Figure 4-566. SS_PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R		R		R											
1h		2h		8e0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
R					R			R		R					
bh					1h			0h		1h					

Access Types Legend

Table 4-1296. SS_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme Reset Source: canfd_rst_mod_g_rst_n
29:28	BU	R	2h	Business Unit: 10 = Processors Reset Source: canfd_rst_mod_g_rst_n
27:16	MODULE_ID	R	8E0h	Module ID Reset Source: canfd_rst_mod_g_rst_n
15:11	RTL	R	Bh	RTL revision. Will vary depending on release. Reset Source: canfd_rst_mod_g_rst_n
10:8	MAJOR	R	1h	Major revision Reset Source: canfd_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom Reset Source: canfd_rst_mod_g_rst_n
5:0	MINOR	R	1h	Minor revision Reset Source: canfd_rst_mod_g_rst_n

4.13.4 CFG_SS_CTRL Registers

4.13.4.1 CFG_CTRL Register (Offset = 4h) [reset = 8h]

Short Description: SS_CTRL

Long Description: SS_CTRL

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Table 4-1297. Instance Table

Instance Name	Physical Address
MCAN0	5260 8004h
MCAN1	5261 8004h
MCAN2	5262 8004h
MCAN3	5263 8004h

Figure 4-567. SS_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU0															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU0									EXT_TS_CNTR_EN	AUTOWAKEUP	WAKEUPREGEN	DBGSUSP_FREE	NU		
R									R/W	R/W	R/W	R/W	R		
0h									0h	0h	0h	1h	0h		

Access Types Legend

Table 4-1298. SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	NU0	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
6	EXT_TS_CNTR_EN	R/W	0h	External TimeStamp Counter Enable Reset Source: canfd_rst_mod_g_rst_n
5	AUTOWAKEUP	R/W	0h	Automatic Wakeup Enable Reset Source: canfd_rst_mod_g_rst_n
4	WAKEUPREGEN	R/W	0h	Wakeup Request Enable Reset Source: canfd_rst_mod_g_rst_n
3	DBGSUSP_FREE	R/W	1h	0-Honor Debug Suspend, 1-Disregard debug suspend Reset Source: canfd_rst_mod_g_rst_n
2:0	NU	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n

4.13.5 CFG_SS_STAT Registers

4.13.5.1 CFG_STAT Register (Offset = 8h) [reset = 6h]

Short Description: SS_STAT

Long Description: SS_STAT

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Table 4-1299. Instance Table

Instance Name	Physical Address
MCAN0	5260 8008h
MCAN1	5261 8008h
MCAN2	5262 8008h
MCAN3	5263 8008h

Figure 4-568. SS_STAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU1													EN_FDOE	MMI_DONE	NU
R													R	R	R
0h													1h	1h	0h

Access Types Legend

Table 4-1300. SS_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	NU1	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
2	EN_FDOE	R	1h	Reflects the value of mcanss_enable_fdoe configuration port x=mcanss_enable_fdoe Reset Source: canfd_rst_mod_g_rst_n
1	MMI_DONE	R	1h	0:Memory Initialization is in progress, 1:Memory Intialization Done Reset Source: canfd_rst_mod_g_rst_n
0	NU	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n

4.13.6 CFG_SS_ICS Registers

4.13.6.1 CFG_ICS Register (Offset = Ch) [reset = 0h]

Short Description: SS_ICS

Long Description: SS_ICS

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Table 4-1301. Instance Table

Instance Name	Physical Address
MCAN0	5260 800Ch
MCAN1	5261 800Ch
MCAN2	5262 800Ch
MCAN3	5263 800Ch

Figure 4-569. SS_ICS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU2															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU2															ICS
R															W
0h															0h

Access Types Legend

Table 4-1302. SS_ICS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	NU2	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
0	ICS	W	0h	This bit contains the External TimeStamp Counter Overflow Interrupt status. Write '1' to clear bits. [ICS - Interrupt Clear Shadow Register] Reset Source: canfd_rst_mod_g_rst_n

4.13.7 CFG_SS_IRS Registers

4.13.7.1 CFG_IRS Register (Offset = 10h) [reset = 0h]

Short Description: SS_IRS

Long Description: SS_IRS

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Table 4-1303. Instance Table

Instance Name	Physical Address
MCAN0	5260 8010h
MCAN1	5261 8010h
MCAN2	5262 8010h
MCAN3	5263 8010h

Figure 4-570. SS_IRS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU3															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU3															IRS
R															R
0h															0h

Access Types Legend

Table 4-1304. SS_IRS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	NU3	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
0	IRS	R	0h	External TimeStamp Counter Overflow Interrupt status. Read raw interrupt status. [IRS - Interrupt Raw Status Register] Reset Source: canfd_rst_mod_g_rst_n

4.13.8 CFG_SS_IECS Registers

4.13.8.1 CFG_IECS Register (Offset = 14h) [reset = 0h]

Short Description: SS_IECS

Long Description: SS_IECS

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Table 4-1305. Instance Table

Instance Name	Physical Address
MCAN0	5260 8014h
MCAN1	5261 8014h
MCAN2	5262 8014h
MCAN3	5263 8014h

Figure 4-571. SS_IECS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU4															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU4															IECS
R															W
0h															0h

Access Types Legend

Table 4-1306. SS_IECS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	NU4	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
0	IECS	W	0h	External TimeStamp Counter Overflow Interrupt. Write '1' to clear bits. [IECS - Interrupt Enable Clear Shadow Register] Reset Source: canfd_rst_mod_g_rst_n

4.13.9 CFG_SS_IE Registers

4.13.9.1 CFG_IE Register (Offset = 18h) [reset = 0h]

Short Description: SS_IE

Long Description: SS_IE

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Table 4-1307. Instance Table

Instance Name	Physical Address
MCAN0	5260 8018h
MCAN1	5261 8018h
MCAN2	5262 8018h
MCAN3	5263 8018h

Figure 4-572. SS_IE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU5															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU5															IE
R															R/W
0h															0h

Access Types Legend

Table 4-1308. SS_IE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	NU5	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
0	IE	R/W	0h	External TimeStamp Counter Overflow Interrupt. Write '1' to set interrupt enable. Read returns interrupt enable. [IE - Interrupt Enable Register] Reset Source: canfd_rst_mod_g_rst_n

4.13.10 CFG_SS_IES Registers

4.13.10.1 CFG_IES Register (Offset = 1Ch) [reset = 0h]

Short Description: SS_IES

Long Description: SS_IES

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Table 4-1309. Instance Table

Instance Name	Physical Address
MCAN0	5260 801Ch
MCAN1	5261 801Ch
MCAN2	5262 801Ch
MCAN3	5263 801Ch

Figure 4-573. SS_IES Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU6															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU6															IES
R															R
0h															0h

Access Types Legend

Table 4-1310. SS_IES Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	NU6	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
0	IES	R	0h	External TimeStamp Counter Overflow Interrupt. Read Enabled Interrupts. [IES - Interrupt Enable Status] Reset Source: canfd_rst_mod_g_rst_n

4.13.11 CFG_SS_EOI Registers

4.13.11.1 CFG_EOI Register (Offset = 20h) [reset = 0h]

Short Description: SS_EOI

Long Description: SS_EOI

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Table 4-1311. Instance Table

Instance Name	Physical Address
MCAN0	5260 8020h
MCAN1	5261 8020h
MCAN2	5262 8020h
MCAN3	5263 8020h

Figure 4-574. SS_EOI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU7															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU7								EOI							
R								W							
0h								0h							

Access Types Legend

Table 4-1312. SS_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	NU7	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
7:0	EOI	W	0h	Write with bit position of targeted interrupt. [E.g. Ext TS is bit 0]. Upon write, level interrupt will clear and if unserviced interrupt counter > 1 will issue another pulse interrupt. Field values: ext_ts_eoi[0]: EOI value for External TS interrupt mcan_0_eoi[1]: EOI value for mcan[0] interrupt mcan_1_eoi[2]: EOI value for mcan[1] interrupt [EOI - End Of Interrupt] Reset Source: canfd_rst_mod_g_rst_n

4.13.12 CFG_SS_EXT_TS_PS Registers

4.13.12.1 CFG_EXT_TS_PS Register (Offset = 24h) [reset = 0h]

Short Description: SS_EXT_TS_PS

Long Description: SS_EXT_TS_PS

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Table 4-1313. Instance Table

Instance Name	Physical Address
MCAN0	5260 8024h
MCAN1	5261 8024h
MCAN2	5262 8024h
MCAN3	5263 8024h

Figure 4-575. SS_EXT_TS_PS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU8								PRESCALE							
R								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRESCALE															
R/W															
0h															

Access Types Legend

Table 4-1314. SS_EXT_TS_PS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	NU8	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
23:0	PRESCALE	R/W	0h	External Timestamp Prescaler reload value. External Timestamp count rate is host clock rate divided by this value with one exception: a value of 0 has the same effect as 1 . Reset Source: canfd_rst_mod_g_rst_n

4.13.13 CFG_SS_EXT_TS_USIC Registers

4.13.13.1 CFG_EXT_TS_USIC Register (Offset = 28h) [reset = 0h]

Short Description: SS_EXT_TS_USIC

Long Description: SS_EXT_TS_USIC

Return to Summary Table

Table 4-1315. Instance Table

Instance Name	Physical Address
MCAN0	5260 8028h
MCAN1	5261 8028h
MCAN2	5262 8028h
MCAN3	5263 8028h

Figure 4-576. SS_EXT_TS_USIC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU9															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU9											EXT_TS_INTR_CNTR				
R											R				
0h											0h				

Access Types Legend

Table 4-1316. SS_EXT_TS_USIC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	NU9	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
4:0	EXT_TS_INTR_CNTR	R	0h	Number of unserviced rollover interrupts. If >1 an EOI write will issue another pulse interrupt [EXT_TS_USIC - External TImeStamp Unserviced Interrupts Counter] Reset Source: canfd_rst_mod_g_rst_n

4.13.14 CFG_CREL Registers

4.13.14.1 CFG_CREL Register (Offset = 200h) [reset = 32380608h]

Short Description: CREL

Long Description: CREL

Return to Summary Table

Table 4-1317. Instance Table

Instance Name	Physical Address
MCAN0	5260 8200h
MCAN1	5261 8200h
MCAN2	5262 8200h
MCAN3	5263 8200h

Figure 4-577. CREL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
REL				STEP				SUBSTEP				YEAR			
R				R				R				R			
3h				2h				3h				8h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MON								DAY							
R								R							
6h								8h							

Access Types Legend

Table 4-1318. CREL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REL	R	3h	Core Release Reset Source: canfd_rst_mod_g_rst_n
27:24	STEP	R	2h	Step of Core Release Reset Source: canfd_rst_mod_g_rst_n
23:20	SUBSTEP	R	3h	Sub-Step of Core Release Reset Source: canfd_rst_mod_g_rst_n
19:16	YEAR	R	8h	Time Stamp Year Reset Source: canfd_rst_mod_g_rst_n
15:8	MON	R	6h	Time Stamp Month Reset Source: canfd_rst_mod_g_rst_n
7:0	DAY	R	8h	Time Stamp Day Reset Source: canfd_rst_mod_g_rst_n

4.13.15 CFG_ENDN Registers

4.13.15.1 CFG_ENDN Register (Offset = 204h) [reset = 87654321h]

Short Description: ENDN

Long Description: ENDN

Return to Summary Table

Table 4-1319. Instance Table

Instance Name	Physical Address
MCAN0	5260 8204h
MCAN1	5261 8204h
MCAN2	5262 8204h
MCAN3	5263 8204h

Figure 4-578. ENDN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ETV															
R															
87654321h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ETV															
R															
87654321h															

Access Types Legend

Table 4-1320. ENDN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ETV	R	87654321h	Endianess test value Reset Source: canfd_rst_mod_g_rst_n

4.13.16 CFG_CUST Registers

4.13.16.1 CFG_CUST Register (Offset = 208h) [reset = 0h]

Short Description: CUST

Long Description: CUST

Return to Summary Table

Table 4-1321. Instance Table

Instance Name	Physical Address
MCAN0	5260 8208h
MCAN1	5261 8208h
MCAN2	5262 8208h
MCAN3	5263 8208h

Figure 4-579. CUST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CUST															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CUST															
R															
0h															

Access Types Legend

Table 4-1322. CUST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CUST	R	0h	Custom Reset Source: canfd_rst_mod_g_rst_n

4.13.17 CFG_DBTP Registers

4.13.17.1 CFG_DBTP Register (Offset = 20Ch) [reset = a33h]

Short Description: DBTP

Long Description: DBTP

Return to Summary Table

Table 4-1323. Instance Table

Instance Name	Physical Address
MCAN0	5260 820Ch
MCAN1	5261 820Ch
MCAN2	5262 820Ch
MCAN3	5263 820Ch

Figure 4-580. DBTP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU13								TDC	NU12		DBRP				
R								R/W	R		R/W				
0h								0h	0h		0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU11			DTSEG1					DTSEG2				DSJW			
R			R/W					R/W				R/W			
0h			ah					3h				3h			

Access Types Legend

Table 4-1324. DBTP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	NU13	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
23	TDC	R/W	0h	Transmitter Delay Compensation Reset Source: canfd_rst_mod_g_rst_n
22:21	NU12	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
20:16	DBRP	R/W	0h	Data Baud Rate Prescaler Reset Source: canfd_rst_mod_g_rst_n
15:13	NU11	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
12:8	DTSEG1	R/W	Ah	Data time segment before smaple point Reset Source: canfd_rst_mod_g_rst_n
7:4	DTSEG2	R/W	3h	Data time segment after sample point Reset Source: canfd_rst_mod_g_rst_n
3:0	DSJW	R/W	3h	Data resynchronization Jump Width Reset Source: canfd_rst_mod_g_rst_n

4.13.18 CFG_TEST Registers

4.13.18.1 CFG_TEST Register (Offset = 210h) [reset = 0h]

Short Description: TEST

Long Description: TEST

Return to Summary Table

Table 4-1325. Instance Table

Instance Name	Physical Address
MCAN0	5260 8210h
MCAN1	5261 8210h
MCAN2	5262 8210h
MCAN3	5263 8210h

Figure 4-581. TEST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU15															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU15								RX	TX		LBCK	NU14			
R								R	R/W		R/W	R			
0h								0h	0h		0h	0h			

Access Types Legend

Table 4-1326. TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	NU15	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
7	RX	R	0h	Receive Pin Reset Source: canfd_rst_mod_g_rst_n
6:5	TX	R/W	0h	Control of Transmit Pin Reset Source: canfd_rst_mod_g_rst_n
4	LBCK	R/W	0h	Loop Back Mode Reset Source: canfd_rst_mod_g_rst_n
3:0	NU14	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n

4.13.19 CFG_RWD Registers

4.13.19.1 CFG_RWD Register (Offset = 214h) [reset = 0h]

Short Description: RWD

Long Description: RWD

Return to Summary Table

Table 4-1327. Instance Table

Instance Name	Physical Address
MCAN0	5260 8214h
MCAN1	5261 8214h
MCAN2	5262 8214h
MCAN3	5263 8214h

Figure 4-582. RWD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU16															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDV								WDC							
R								R/W							
0h								0h							

Access Types Legend

Table 4-1328. RWD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	NU16	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
15:8	WDV	R	0h	Watchdog Value Reset Source: canfd_rst_mod_g_rst_n
7:0	WDC	R/W	0h	Watchdog Counter Value Reset Source: canfd_rst_mod_g_rst_n

4.13.20 CFG_CCCR Registers

4.13.20.1 CFG_CCCR Register (Offset = 218h) [reset = 1h]

Short Description: CCCR

Long Description: CCCR

Return to Summary Table

Table 4-1329. Instance Table

Instance Name	Physical Address
MCAN0	5260 8218h
MCAN1	5261 8218h
MCAN2	5262 8218h
MCAN3	5263 8218h

Figure 4-583. CCCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU18															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU18	TXP	EFBI	PXHD	NU17		BRSE	FDOE	TEST	DAR	MON	CSR	CSA	ASM	CCE	INIT
R/W	R/W	R/W	R/W	R		R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
0h	0h	0h	0h	0h		0h	0h	0h	0h	0h	0h	0h	0h	0h	1h

Access Types Legend

Table 4-1330. CCCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	NU18	R/W	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
14	TXP	R/W	0h	Transmit Pause Reset Source: canfd_rst_mod_g_rst_n
13	EFBI	R/W	0h	Edge Filtering durign Bus Integration Reset Source: canfd_rst_mod_g_rst_n
12	PXHD	R/W	0h	Protocol Exception Handling Disable Reset Source: canfd_rst_mod_g_rst_n
11:10	NU17	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
9	BRSE	R/W	0h	Bit Rate Switch Enable Reset Source: canfd_rst_mod_g_rst_n
8	FDOE	R/W	0h	FD Operation Enable Reset Source: canfd_rst_mod_g_rst_n
7	TEST	R/W	0h	Test Mode enable Reset Source: canfd_rst_mod_g_rst_n
6	DAR	R/W	0h	Disable Automatic Regransmission Reset Source: canfd_rst_mod_g_rst_n
5	MON	R/W	0h	Bus Monitoring Mode Reset Source: canfd_rst_mod_g_rst_n
4	CSR	R/W	0h	Clock Stop Request Reset Source: canfd_rst_mod_g_rst_n
3	CSA	R	0h	Clock Stop Acknowledge Reset Source: canfd_rst_mod_g_rst_n
2	ASM	R/W	0h	Restriced Operation Mode Reset Source: canfd_rst_mod_g_rst_n
1	CCE	R/W	0h	Configuration Change Enable Reset Source: canfd_rst_mod_g_rst_n
0	INIT	R/W	1h	Initialization Reset Source: canfd_rst_mod_g_rst_n

4.13.21 CFG_NBTP Registers

4.13.21.1 CFG_NBTP Register (Offset = 21Ch) [reset = 6000a03h]

Short Description: NBTP

Long Description: NBTP

Return to Summary Table

Table 4-1331. Instance Table

Instance Name	Physical Address
MCAN0	5260 821Ch
MCAN1	5261 821Ch
MCAN2	5262 821Ch
MCAN3	5263 821Ch

Figure 4-584. NBTP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NSJW							NBRP								
R/W							R/W								
3h							0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NTSEG1								NU19	NTSEG2						
R/W								R	R/W						
ah								0h	3h						

Access Types Legend

Table 4-1332. NBTP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	NSJW	R/W	3h	Nominal Resynchronization Jump Width Reset Source: canfd_rst_mod_g_rst_n
24:16	NBRP	R/W	0h	Nominal Baud Rate Prescaler Reset Source: canfd_rst_mod_g_rst_n
15:8	NTSEG1	R/W	Ah	Nominal Time segment before sample point Reset Source: canfd_rst_mod_g_rst_n
7	NU19	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
6:0	NTSEG2	R/W	3h	Nominal Time segment after sample point Reset Source: canfd_rst_mod_g_rst_n

4.13.22 CFG_TSCC Registers

4.13.22.1 CFG_TSCC Register (Offset = 220h) [reset = 0h]

Short Description: TSCC

Long Description: TSCC

Return to Summary Table

Table 4-1333. Instance Table

Instance Name	Physical Address
MCAN0	5260 8220h
MCAN1	5261 8220h
MCAN2	5262 8220h
MCAN3	5263 8220h

Figure 4-585. TSCC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU21												TCP			
R												R/W			
0h												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU20														TSS	
R														R/W	
0h														0h	

Access Types Legend

Table 4-1334. TSCC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	NU21	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
19:16	TCP	R/W	0h	Timestamp Counter Prescaler Reset Source: canfd_rst_mod_g_rst_n
15:2	NU20	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
1:0	TSS	R/W	0h	Timestamp Select Reset Source: canfd_rst_mod_g_rst_n

4.13.23 CFG_TSCV Registers

4.13.23.1 CFG_TSCV Register (Offset = 224h) [reset = 0h]

Short Description: TSCV

Long Description: TSCV

Return to Summary Table

Table 4-1335. Instance Table

Instance Name	Physical Address
MCAN0	5260 8224h
MCAN1	5261 8224h
MCAN2	5262 8224h
MCAN3	5263 8224h

Figure 4-586. TSCV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU22															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSC															
R/W															
0h															

Access Types Legend

Table 4-1336. TSCV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	NU22	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
15:0	TSC	R/W	0h	Timestamp Counter Reset Source: canfd_rst_mod_g_rst_n

4.13.24 CFG_TOCC Registers

4.13.24.1 CFG_TOCC Register (Offset = 228h) [reset = ffff0000h]

Short Description: TOCC

Long Description: TOCC

Return to Summary Table

Table 4-1337. Instance Table

Instance Name	Physical Address
MCAN0	5260 8228h
MCAN1	5261 8228h
MCAN2	5262 8228h
MCAN3	5263 8228h

Figure 4-587. TOCC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TOP															
R/W															
ffffh															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU23													TOS		ETOC
R													R/W		R/W
0h													0h		0h

Access Types Legend

Table 4-1338. TOCC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TOP	R/W	FFFFh	Timeout Period Reset Source: canfd_rst_mod_g_rst_n
15:3	NU23	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
2:1	TOS	R/W	0h	Timeout Select Reset Source: canfd_rst_mod_g_rst_n
0	ETOC	R/W	0h	Enable Timeout Counter Reset Source: canfd_rst_mod_g_rst_n

4.13.25 CFG_TOCV Registers

4.13.25.1 CFG_TOCV Register (Offset = 22Ch) [reset = ffffh]

Short Description: TOCV

Long Description: TOCV

Return to Summary Table

Table 4-1339. Instance Table

Instance Name	Physical Address
MCAN0	5260 822Ch
MCAN1	5261 822Ch
MCAN2	5262 822Ch
MCAN3	5263 822Ch

Figure 4-588. TOCV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU24															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOC															
R/W															
ffffh															

Access Types Legend

Table 4-1340. TOCV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	NU24	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
15:0	TOC	R/W	FFFFh	Timeout Counter Reset Source: canfd_rst_mod_g_rst_n

4.13.26 CFG_RES00 Registers

4.13.26.1 CFG_RES00 Register (Offset = 230h) [reset = 0h]

Short Description: RES00

Long Description: RES00

Return to Summary Table

Table 4-1341. Instance Table

Instance Name	Physical Address
MCAN0	5260 8230h
MCAN1	5261 8230h
MCAN2	5262 8230h
MCAN3	5263 8230h

Figure 4-589. RES00 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES00															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES00															
R															
0h															

Access Types Legend

Table 4-1342. RES00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES00	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n

4.13.27 CFG_RES01 Registers

4.13.27.1 CFG_RES01 Register (Offset = 234h) [reset = 0h]

Short Description: RES01

Long Description: RES01

Return to Summary Table

Table 4-1343. Instance Table

Instance Name	Physical Address
MCAN0	5260 8234h
MCAN1	5261 8234h
MCAN2	5262 8234h
MCAN3	5263 8234h

Figure 4-590. RES01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES01															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES01															
R															
0h															

Access Types Legend

Table 4-1344. RES01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES01	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n

4.13.28 CFG_RES02 Registers

4.13.28.1 CFG_RES02 Register (Offset = 238h) [reset = 0h]

Short Description: RES02

Long Description: RES02

Return to Summary Table

Table 4-1345. Instance Table

Instance Name	Physical Address
MCAN0	5260 8238h
MCAN1	5261 8238h
MCAN2	5262 8238h
MCAN3	5263 8238h

Figure 4-591. RES02 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES02															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES02															
R															
0h															

Access Types Legend

Table 4-1346. RES02 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES02	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n

4.13.29 CFG_RES03 Registers

4.13.29.1 CFG_RES03 Register (Offset = 23Ch) [reset = 0h]

Short Description: RES03

Long Description: RES03

Return to Summary Table

Table 4-1347. Instance Table

Instance Name	Physical Address
MCAN0	5260 823Ch
MCAN1	5261 823Ch
MCAN2	5262 823Ch
MCAN3	5263 823Ch

Figure 4-592. RES03 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES03															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES03															
R															
0h															

Access Types Legend

Table 4-1348. RES03 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES03	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n

4.13.30 CFG_ECR Registers

4.13.30.1 CFG_ECR Register (Offset = 240h) [reset = 0h]

Short Description: ECR

Long Description: ECR

Return to Summary Table

Table 4-1349. Instance Table

Instance Name	Physical Address
MCAN0	5260 8240h
MCAN1	5261 8240h
MCAN2	5262 8240h
MCAN3	5263 8240h

Figure 4-593. ECR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU25								CEL							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RP	REC							TEC							
R	R							R							
0h	0h							0h							

Access Types Legend

Table 4-1350. ECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	NU25	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
23:16	CEL	R	0h	CAN Error Logging Reset Source: canfd_rst_mod_g_rst_n
15	RP	R	0h	Recieve Error Passive Reset Source: canfd_rst_mod_g_rst_n
14:8	REC	R	0h	Recieve Error Counter Reset Source: canfd_rst_mod_g_rst_n
7:0	TEC	R	0h	Transmit Error Counter Reset Source: canfd_rst_mod_g_rst_n

4.13.31 CFG_PSR Registers

4.13.31.1 CFG_PSR Register (Offset = 244h) [reset = 707h]

Short Description: PSR

Long Description: PSR

Return to Summary Table

Table 4-1351. Instance Table

Instance Name	Physical Address
MCAN0	5260 8244h
MCAN1	5261 8244h
MCAN2	5262 8244h
MCAN3	5263 8244h

Figure 4-594. PSR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU27									TDCV						
R									R						
0h									0h						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU26	PXE	RFDF	RBRS	RESI	DLEC			BO	EW	EP	ACT		LEC		
R	R	R	R	R	R			R	R	R	R		R		
0h	0h	0h	0h	0h	7h			0h	0h	0h	0h		7h		

Access Types Legend

Table 4-1352. PSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	NU27	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
22:16	TDCV	R	0h	Transmitter Delay Compensation Value Reset Source: canfd_rst_mod_g_rst_n
15	NU26	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
14	PXE	R	0h	Protocol Exception Event Reset Source: canfd_rst_mod_g_rst_n
13	RFDF	R	0h	Recieved a CAN FD Message Reset Source: canfd_rst_mod_g_rst_n
12	RBRS	R	0h	BRS flag of last recieved CAN FD Message Reset Source: canfd_rst_mod_g_rst_n
11	RESI	R	0h	ESI flag of last recieved CAN FD Message Reset Source: canfd_rst_mod_g_rst_n
10:8	DLEC	R	7h	Data Phase Last Error Code Reset Source: canfd_rst_mod_g_rst_n
7	BO	R	0h	Bus_Off status Reset Source: canfd_rst_mod_g_rst_n
6	EW	R	0h	Warning Status Reset Source: canfd_rst_mod_g_rst_n
5	EP	R	0h	Error Passive Reset Source: canfd_rst_mod_g_rst_n
4:3	ACT	R	0h	Activity Reset Source: canfd_rst_mod_g_rst_n
2:0	LEC	R	7h	Last Error Code Reset Source: canfd_rst_mod_g_rst_n

4.13.32 CFG_TDCR Registers

4.13.32.1 CFG_TDCR Register (Offset = 248h) [reset = 0h]

Short Description: TDCR

Long Description: TDCR

Return to Summary Table

Table 4-1353. Instance Table

Instance Name	Physical Address
MCAN0	5260 8248h
MCAN1	5261 8248h
MCAN2	5262 8248h
MCAN3	5263 8248h

Figure 4-595. TDCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU29															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU29	TDCO							NU28	TDCF						
R	R/W							R	R/W						
0h	0h							0h	0h						

Access Types Legend

Table 4-1354. TDCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	NU29	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
14:8	TDCO	R/W	0h	Transmitter Delay Compensation Offset Reset Source: canfd_rst_mod_g_rst_n
7	NU28	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
6:0	TDCF	R/W	0h	Transmitter Delay Compensation Filter Window Length Reset Source: canfd_rst_mod_g_rst_n

4.13.33 CFG_RES04 Registers

4.13.33.1 CFG_RES04 Register (Offset = 24Ch) [reset = 0h]

Short Description: RES04

Long Description: RES04

Return to Summary Table

Table 4-1355. Instance Table

Instance Name	Physical Address
MCAN0	5260 824Ch
MCAN1	5261 824Ch
MCAN2	5262 824Ch
MCAN3	5263 824Ch

Figure 4-596. RES04 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES04															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES04															
R															
0h															

Access Types Legend

Table 4-1356. RES04 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES04	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n

4.13.34 CFG_IR Registers

4.13.34.1 CFG_IR Register (Offset = 250h) [reset = 0h]

Short Description: IR

Long Description: IR

Return to Summary Table

Table 4-1357. Instance Table

Instance Name	Physical Address
MCAN0	5260 8250h
MCAN1	5261 8250h
MCAN2	5262 8250h
MCAN3	5263 8250h

Figure 4-597. IR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU30		ARA	PED	PEA	WDI	BO	EW	EP	ELO	BEU	BEC	DRX	TOO	MRAF	TSW
R		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEFL	TEFF	TEFW	TEFN	TFE	TCF	TC	HPM	RF1L	RF1F	RF1W	RF1N	RF0L	RF0F	RF0W	RF0N
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-1358. IR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	NU30	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
29	ARA	R/W	0h	Access to Reserved Address Reset Source: canfd_rst_mod_g_rst_n
28	PED	R/W	0h	Protocol Error in data Phase Reset Source: canfd_rst_mod_g_rst_n
27	PEA	R/W	0h	Protocol Error in Arbitration Phase Reset Source: canfd_rst_mod_g_rst_n
26	WDI	R/W	0h	Watchdog Interrupt Reset Source: canfd_rst_mod_g_rst_n
25	BO	R/W	0h	Bus_Off Status Reset Source: canfd_rst_mod_g_rst_n
24	EW	R/W	0h	Warning Status Reset Source: canfd_rst_mod_g_rst_n
23	EP	R/W	0h	Error Passive Reset Source: canfd_rst_mod_g_rst_n
22	ELO	R/W	0h	Error Logging Overflow Reset Source: canfd_rst_mod_g_rst_n
21	BEU	R/W	0h	Bit Error Uncorrected Reset Source: canfd_rst_mod_g_rst_n
20	BEC	R/W	0h	Bit Error Corrected Reset Source: canfd_rst_mod_g_rst_n
19	DRX	R/W	0h	Message stored to Dedicated Rx Buffer Reset Source: canfd_rst_mod_g_rst_n
18	TOO	R/W	0h	Timeout Occurred Reset Source: canfd_rst_mod_g_rst_n
17	MRAF	R/W	0h	Message RAM Access Failure Reset Source: canfd_rst_mod_g_rst_n
16	TSW	R/W	0h	Timestamp Wraparound Reset Source: canfd_rst_mod_g_rst_n
15	TEFL	R/W	0h	Tx Event FIFO Element Lost Reset Source: canfd_rst_mod_g_rst_n
14	TEFF	R/W	0h	Tx Event FIFO Full Reset Source: canfd_rst_mod_g_rst_n
13	TEFW	R/W	0h	Tx Event FIFO Watermark Reached Reset Source: canfd_rst_mod_g_rst_n
12	TEFN	R/W	0h	Tx Event FIFO New Entry Reset Source: canfd_rst_mod_g_rst_n

Table 4-1358. IR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	TFE	R/W	0h	Tx FIFO Empty Reset Source: canfd_rst_mod_g_rst_n
10	TCF	R/W	0h	Transmission Cancellation Finished Reset Source: canfd_rst_mod_g_rst_n
9	TC	R/W	0h	Transmission Complete Reset Source: canfd_rst_mod_g_rst_n
8	HPM	R/W	0h	High Priority Message Reset Source: canfd_rst_mod_g_rst_n
7	RF1L	R/W	0h	Rx FIFO 1 Message Lost Reset Source: canfd_rst_mod_g_rst_n
6	RF1F	R/W	0h	Rx FIFO 1 Full Reset Source: canfd_rst_mod_g_rst_n
5	RF1W	R/W	0h	Rx FIFO 1 Watermark Reached Reset Source: canfd_rst_mod_g_rst_n
4	RF1N	R/W	0h	Rx FIFO 1 New Message Reset Source: canfd_rst_mod_g_rst_n
3	RF0L	R/W	0h	Rx FIFO 0 Message Lost Reset Source: canfd_rst_mod_g_rst_n
2	RF0F	R/W	0h	Rx FIFO 0 Full Reset Source: canfd_rst_mod_g_rst_n
1	RF0W	R/W	0h	Rx FIFO 0 Watermark Reached Reset Source: canfd_rst_mod_g_rst_n
0	RF0N	R/W	0h	Rx FIFO 0 New Message Reset Source: canfd_rst_mod_g_rst_n

4.13.35 CFG_IE Registers

4.13.35.1 CFG_IE Register (Offset = 254h) [reset = 0h]

Short Description: IE

Long Description: IE

Return to Summary Table

Table 4-1359. Instance Table

Instance Name	Physical Address
MCAN0	5260 8254h
MCAN1	5261 8254h
MCAN2	5262 8254h
MCAN3	5263 8254h

Figure 4-598. IE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU31		ARAE	PEDE	PEAE	WDIE	BOE	EWE	EPE	ELOE	BEUE	BECE	DRX	TOOE	MRAFE	TSWE
R		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEFLE	TEFFE	TEFWE	TEFNE	TFEE	TCFE	TCE	HPME	RF1LE	RF1FE	RF1WE	RF1NE	RF0LE	RF0FE	RF0WE	RF0NE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-1360. IE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	NU31	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
29	ARAE	R/W	0h	Accees to Reserve Address Interrupt Enable Reset Source: canfd_rst_mod_g_rst_n
28	PEDE	R/W	0h	Protocol Error in Data Phase Interrupt Enable Reset Source: canfd_rst_mod_g_rst_n
27	PEAE	R/W	0h	Protocol Error in Arbitration Phase Interrupt Enable Reset Source: canfd_rst_mod_g_rst_n
26	WDIE	R/W	0h	Watchdog Interrupt Enable Reset Source: canfd_rst_mod_g_rst_n
25	BOE	R/W	0h	Bus_Off Status Interrupt Enable Reset Source: canfd_rst_mod_g_rst_n
24	EWE	R/W	0h	Warning Status Interrupt Enable Reset Source: canfd_rst_mod_g_rst_n
23	EPE	R/W	0h	Error Passive Interrupt Enable Reset Source: canfd_rst_mod_g_rst_n
22	ELOE	R/W	0h	Error Logging Overflow Interrupt Enable Reset Source: canfd_rst_mod_g_rst_n
21	BEUE	R/W	0h	Bit Error Uncorrected Interrupt Enable Reset Source: canfd_rst_mod_g_rst_n
20	BECE	R/W	0h	Bit Error Corrected Interrupt Enable Reset Source: canfd_rst_mod_g_rst_n
19	DRX	R/W	0h	Message stored to Dedicated Rx Buffer Interrupt Enable Reset Source: canfd_rst_mod_g_rst_n
18	TOOE	R/W	0h	Timeout Occurred Interrupt Enable Reset Source: canfd_rst_mod_g_rst_n

Table 4-1360. IE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	MRAFE	R/W	0h	Message RAM Access Failure Interrupt Enable Reset Source: canfd_rst_mod_g_rst_n
16	TSWE	R/W	0h	Timestamp Wraparound Interrupt Enable Reset Source: canfd_rst_mod_g_rst_n
15	TEFLE	R/W	0h	Tx Event FIFO Event Lost Interrupt Enable Reset Source: canfd_rst_mod_g_rst_n
14	TEFFE	R/W	0h	Tx Event FIFO Full Interrupt Enable Reset Source: canfd_rst_mod_g_rst_n
13	TEFWE	R/W	0h	Tx Event FIFO Watermark Reached Interrupt enable Reset Source: canfd_rst_mod_g_rst_n
12	TEFNE	R/W	0h	Tx Event FIFO New Entry Interrupt Enable Reset Source: canfd_rst_mod_g_rst_n
11	TFEE	R/W	0h	Tx FIFO Empty Interrupt Enable Reset Source: canfd_rst_mod_g_rst_n
10	TCFE	R/W	0h	Transmission Cancellation Finishied Interrupt Enable Reset Source: canfd_rst_mod_g_rst_n
9	TCE	R/W	0h	Transmission Completed Interrupt Enable Reset Source: canfd_rst_mod_g_rst_n
8	HPME	R/W	0h	High Priority message Interrupt Enable Reset Source: canfd_rst_mod_g_rst_n
7	RF1LE	R/W	0h	rx FIFO 1 Message Lost Interrupt Enable Reset Source: canfd_rst_mod_g_rst_n
6	RF1FE	R/W	0h	Rx FIFO 1 Full Interrupt Enable Reset Source: canfd_rst_mod_g_rst_n
5	RF1WE	R/W	0h	Rx FIFO 1 Watermark Reached Interrupt Enable Reset Source: canfd_rst_mod_g_rst_n
4	RF1NE	R/W	0h	Rx FIFO 1 New Message Interrupt Enable Reset Source: canfd_rst_mod_g_rst_n
3	RF0LE	R/W	0h	Rx FIFO 0 Message Lost Interrupt Enable Reset Source: canfd_rst_mod_g_rst_n
2	RF0FE	R/W	0h	Rx FIFO 0 Full Interrupt Enable Reset Source: canfd_rst_mod_g_rst_n
1	RF0WE	R/W	0h	Rx FIFO 0 Watermark Reached Interrupt Enable Reset Source: canfd_rst_mod_g_rst_n
0	RF0NE	R/W	0h	Rx FIFO 0 New Message Interrupt Enable Reset Source: canfd_rst_mod_g_rst_n

4.13.36 CFG_ILS Registers

4.13.36.1 CFG_ILS Register (Offset = 258h) [reset = 0h]

Short Description: ILS

Long Description: ILS

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Table 4-1361. Instance Table

Instance Name	Physical Address
MCAN0	5260 8258h
MCAN1	5261 8258h
MCAN2	5262 8258h
MCAN3	5263 8258h

Figure 4-599. ILS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU32		ARAL	PEDL	PEAL	WDIL	BOL	EWL	EPL	ELOL	BEUL	BECL	DRXL	TOOL	MRAFL	TSWL
R		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEFLL	TEFFL	TEFWL	TEFNL	TFEL	TCFL	TCL	HPML	RF1LL	RF1FL	RF1WL	RF1NL	RF0LL	RF0FL	RF0WL	RF0NL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-1362. ILS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	NU32	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
29	ARAL	R/W	0h	Accees to Reserve Address Interrupt Line Reset Source: canfd_rst_mod_g_rst_n
28	PEDL	R/W	0h	Protocol Error in Data Phase Interrupt Line Reset Source: canfd_rst_mod_g_rst_n
27	PEAL	R/W	0h	Protocol Error in Arbitration Phase Interrupt Line Reset Source: canfd_rst_mod_g_rst_n
26	WDIL	R/W	0h	Watchdog Interrupt Line Reset Source: canfd_rst_mod_g_rst_n
25	BOL	R/W	0h	Bus_Off Status Interrupt Line Reset Source: canfd_rst_mod_g_rst_n
24	EWL	R/W	0h	Warning Status Interrupt Line Reset Source: canfd_rst_mod_g_rst_n
23	EPL	R/W	0h	Error Passive Interrupt Line Reset Source: canfd_rst_mod_g_rst_n
22	ELOL	R/W	0h	Error Logging Overflow Interrupt Line Reset Source: canfd_rst_mod_g_rst_n
21	BEUL	R/W	0h	Bit Error Uncorrected Interrupt Line Reset Source: canfd_rst_mod_g_rst_n
20	BECL	R/W	0h	Bit Error Corrected Interrupt Line Reset Source: canfd_rst_mod_g_rst_n
19	DRXL	R/W	0h	Message stored to Dedicated Rx Buffer Interrupt Line Reset Source: canfd_rst_mod_g_rst_n
18	TOOL	R/W	0h	Timeout Occurred Interrupt Line Reset Source: canfd_rst_mod_g_rst_n
17	MRAFL	R/W	0h	Message RAM Access Failure Interrupt Line Reset Source: canfd_rst_mod_g_rst_n

Table 4-1362. ILS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	TSWL	R/W	0h	Timestamp Wraparound Interrupt Line Reset Source: canfd_rst_mod_g_rst_n
15	TEFLL	R/W	0h	Tx Event FIFO Event Lost Interrupt Line Reset Source: canfd_rst_mod_g_rst_n
14	TEFFL	R/W	0h	Tx Event FIFO Full Interrupt Line Reset Source: canfd_rst_mod_g_rst_n
13	TEFWL	R/W	0h	Tx Event FIFO Watermark Reached Interrupt Line Reset Source: canfd_rst_mod_g_rst_n
12	TEFNL	R/W	0h	Tx Event FIFO New Entry Interrupt Line Reset Source: canfd_rst_mod_g_rst_n
11	TFEL	R/W	0h	Tx FIFO Empty Interrupt Line Reset Source: canfd_rst_mod_g_rst_n
10	TCFL	R/W	0h	Transmission Cancellation Finishied Interrupt Line Reset Source: canfd_rst_mod_g_rst_n
9	TCL	R/W	0h	Transmission Completed Interrupt Line Reset Source: canfd_rst_mod_g_rst_n
8	HPML	R/W	0h	High Priority message Interrupt Line Reset Source: canfd_rst_mod_g_rst_n
7	RF1LL	R/W	0h	rx FIFO 1 Message Lost Interrupt Line Reset Source: canfd_rst_mod_g_rst_n
6	RF1FL	R/W	0h	Rx FIFO 1 Full Interrupt Line Reset Source: canfd_rst_mod_g_rst_n
5	RF1WL	R/W	0h	Rx FIFO 1 Watermark Reached Interrupt Line Reset Source: canfd_rst_mod_g_rst_n
4	RF1NL	R/W	0h	Rx FIFO 1 New Message Interrupt Line Reset Source: canfd_rst_mod_g_rst_n
3	RF0LL	R/W	0h	Rx FIFO 0 Message Lost Interrupt Line Reset Source: canfd_rst_mod_g_rst_n
2	RF0FL	R/W	0h	Rx FIFO 0 Full Interrupt Line Reset Source: canfd_rst_mod_g_rst_n
1	RF0WL	R/W	0h	Rx FIFO 0 Watermark Reached Interrupt Line Reset Source: canfd_rst_mod_g_rst_n
0	RF0NL	R/W	0h	Rx FIFO 0 New Message Interrupt Line Reset Source: canfd_rst_mod_g_rst_n

4.13.37 CFG_ILE Registers

4.13.37.1 CFG_ILE Register (Offset = 25Ch) [reset = 0h]

Short Description: ILE

Long Description: ILE

Return to Summary Table

Table 4-1363. Instance Table

Instance Name	Physical Address
MCAN0	5260 825Ch
MCAN1	5261 825Ch
MCAN2	5262 825Ch
MCAN3	5263 825Ch

Figure 4-600. ILE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU33															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU33														EINT1	EINT0
R														R/W	R/W
0h														0h	0h

Access Types Legend

Table 4-1364. ILE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	NU33	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
1	EINT1	R/W	0h	Enable Interrupt Line 1 Reset Source: canfd_rst_mod_g_rst_n
0	EINT0	R/W	0h	Enable Interrupt Line 0 Reset Source: canfd_rst_mod_g_rst_n

4.13.38 CFG_RES05 Registers

4.13.38.1 CFG_RES05 Register (Offset = 260h) [reset = 0h]

Short Description: RES05

Long Description: RES05

Return to Summary Table

Table 4-1365. Instance Table

Instance Name	Physical Address
MCAN0	5260 8260h
MCAN1	5261 8260h
MCAN2	5262 8260h
MCAN3	5263 8260h

Figure 4-601. RES05 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES05															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES05															
R															
0h															

Access Types Legend

Table 4-1366. RES05 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES05	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n

4.13.39 CFG_RES06 Registers

4.13.39.1 CFG_RES06 Register (Offset = 264h) [reset = 0h]

Short Description: RES06

Long Description: RES06

Return to Summary Table

Table 4-1367. Instance Table

Instance Name	Physical Address
MCAN0	5260 8264h
MCAN1	5261 8264h
MCAN2	5262 8264h
MCAN3	5263 8264h

Figure 4-602. RES06 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES06															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES06															
R															
0h															

Access Types Legend

Table 4-1368. RES06 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES06	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n

4.13.40 CFG_RES07 Registers

4.13.40.1 CFG_RES07 Register (Offset = 268h) [reset = 0h]

Short Description: RES07

Long Description: RES07

Return to Summary Table

Table 4-1369. Instance Table

Instance Name	Physical Address
MCAN0	5260 8268h
MCAN1	5261 8268h
MCAN2	5262 8268h
MCAN3	5263 8268h

Figure 4-603. RES07 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES07															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES07															
R															
0h															

Access Types Legend

Table 4-1370. RES07 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES07	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n

4.13.41 CFG_RES08 Registers

4.13.41.1 CFG_RES08 Register (Offset = 26Ch) [reset = 0h]

Short Description: RES08

Long Description: RES08

Return to Summary Table

Table 4-1371. Instance Table

Instance Name	Physical Address
MCAN0	5260 826Ch
MCAN1	5261 826Ch
MCAN2	5262 826Ch
MCAN3	5263 826Ch

Figure 4-604. RES08 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES08															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES08															
R															
0h															

Access Types Legend

Table 4-1372. RES08 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES08	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n

4.13.42 CFG_RES09 Registers

4.13.42.1 CFG_RES09 Register (Offset = 270h) [reset = 0h]

Short Description: RES09

Long Description: RES09

Return to Summary Table

Table 4-1373. Instance Table

Instance Name	Physical Address
MCAN0	5260 8270h
MCAN1	5261 8270h
MCAN2	5262 8270h
MCAN3	5263 8270h

Figure 4-605. RES09 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES09															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES09															
R															
0h															

Access Types Legend

Table 4-1374. RES09 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES09	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n

4.13.43 CFG_RES10 Registers

4.13.43.1 CFG_RES10 Register (Offset = 274h) [reset = 0h]

Short Description: RES10

Long Description: RES10

Return to Summary Table

Table 4-1375. Instance Table

Instance Name	Physical Address
MCAN0	5260 8274h
MCAN1	5261 8274h
MCAN2	5262 8274h
MCAN3	5263 8274h

Figure 4-606. RES10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES10															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES10															
R															
0h															

Access Types Legend

Table 4-1376. RES10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES10	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n

4.13.44 CFG_RES11 Registers

4.13.44.1 CFG_RES11 Register (Offset = 278h) [reset = 0h]

Short Description: RES11

Long Description: RES11

Return to Summary Table

Table 4-1377. Instance Table

Instance Name	Physical Address
MCAN0	5260 8278h
MCAN1	5261 8278h
MCAN2	5262 8278h
MCAN3	5263 8278h

Figure 4-607. RES11 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES11															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES11															
R															
0h															

Access Types Legend

Table 4-1378. RES11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES11	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n

4.13.45 CFG_RES12 Registers

4.13.45.1 CFG_RES12 Register (Offset = 27Ch) [reset = 0h]

Short Description: RES12

Long Description: RES12

Return to Summary Table

Table 4-1379. Instance Table

Instance Name	Physical Address
MCAN0	5260 827Ch
MCAN1	5261 827Ch
MCAN2	5262 827Ch
MCAN3	5263 827Ch

Figure 4-608. RES12 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES12															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES12															
R															
0h															

Access Types Legend

Table 4-1380. RES12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES12	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n

4.13.46 CFG_GFC Registers

4.13.46.1 CFG_GFC Register (Offset = 280h) [reset = 0h]

Short Description: GFC

Long Description: GFC

Return to Summary Table

Table 4-1381. Instance Table

Instance Name	Physical Address
MCAN0	5260 8280h
MCAN1	5261 8280h
MCAN2	5262 8280h
MCAN3	5263 8280h

Figure 4-609. GFC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU34															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU34										ANFS		ANFE		RRFS	RRFE
R										R/W		R/W		R/W	R/W
0h										0h		0h		0h	0h

Access Types Legend

Table 4-1382. GFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	NU34	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
5:4	ANFS	R/W	0h	Accept Non-matching Frames Standard Reset Source: canfd_rst_mod_g_rst_n
3:2	ANFE	R/W	0h	Accept Non-matching Frames Extended Reset Source: canfd_rst_mod_g_rst_n
1	RRFS	R/W	0h	reject Remote Frames Standard Reset Source: canfd_rst_mod_g_rst_n
0	RRFE	R/W	0h	reject Remote Frames Extended Reset Source: canfd_rst_mod_g_rst_n

4.13.47 CFG_SIDFC Registers

4.13.47.1 CFG_SIDFC Register (Offset = 284h) [reset = 0h]

Short Description: SIDFC

Long Description: SIDFC

Return to Summary Table

Table 4-1383. Instance Table

Instance Name	Physical Address
MCAN0	5260 8284h
MCAN1	5261 8284h
MCAN2	5262 8284h
MCAN3	5263 8284h

Figure 4-610. SIDFC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU36								LSS_S							
R								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLSSA_S														NU35	
R/W														R	
0h														0h	

Access Types Legend

Table 4-1384. SIDFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	NU36	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
23:16	LSS_S	R/W	0h	List Size Standard Reset Source: canfd_rst_mod_g_rst_n
15:2	FLSSA_S	R/W	0h	Filter List Standard Start Address Reset Source: canfd_rst_mod_g_rst_n
1:0	NU35	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n

4.13.48 CFG_XIDFC Registers

4.13.48.1 CFG_XIDFC Register (Offset = 288h) [reset = 0h]

Short Description: XIDFC

Long Description: XIDFC

Return to Summary Table

Table 4-1385. Instance Table

Instance Name	Physical Address
MCAN0	5260 8288h
MCAN1	5261 8288h
MCAN2	5262 8288h
MCAN3	5263 8288h

Figure 4-611. XIDFC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU38								LSS_X							
R								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLSSA_X														NU37	
R/W														R	
0h														0h	

Access Types Legend

Table 4-1386. XIDFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	NU38	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
23:16	LSS_X	R/W	0h	List Size Standard Reset Source: canfd_rst_mod_g_rst_n
15:2	FLSSA_X	R/W	0h	Filter List Standard Start Address Reset Source: canfd_rst_mod_g_rst_n
1:0	NU37	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n

4.13.49 CFG_RES13 Registers

4.13.49.1 CFG_RES13 Register (Offset = 28Ch) [reset = 0h]

Short Description: RES13

Long Description: RES13

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Table 4-1387. Instance Table

Instance Name	Physical Address
MCAN0	5260 828Ch
MCAN1	5261 828Ch
MCAN2	5262 828Ch
MCAN3	5263 828Ch

Figure 4-612. RES13 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES13															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES13															
R															
0h															

Access Types Legend

Table 4-1388. RES13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RES13	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n

4.13.50 CFG_XIDAM Registers

4.13.50.1 CFG_XIDAM Register (Offset = 290h) [reset = 1fffffffh]

Short Description: XIDAM

Long Description: XIDAM

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Table 4-1389. Instance Table

Instance Name	Physical Address
MCAN0	5260 8290h
MCAN1	5261 8290h
MCAN2	5262 8290h
MCAN3	5263 8290h

Figure 4-613. XIDAM Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU39			EIDM												
R			R/W												
0h			1fffffffh												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EIDM															
R/W															
1fffffffh															

Access Types Legend

Table 4-1390. XIDAM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	NU39	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
28:0	EIDM	R/W	1FFFFFFFh	Extended ID Mask Reset Source: canfd_rst_mod_g_rst_n

4.13.51 CFG_HPMS Registers

4.13.51.1 CFG_HPMS Register (Offset = 294h) [reset = 0h]

Short Description: HPMS

Long Description: HPMS

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Table 4-1391. Instance Table

Instance Name	Physical Address
MCAN0	5260 8294h
MCAN1	5261 8294h
MCAN2	5262 8294h
MCAN3	5263 8294h

Figure 4-614. HPMS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU40															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLST	FIDX							MSI		BIDX					
R	R							R		R					
0h	0h							0h		0h					

Access Types Legend

Table 4-1392. HPMS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	NU40	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
15	FLST	R	0h	Filter List Reset Source: canfd_rst_mod_g_rst_n
14:8	FIDX	R	0h	Filter Index Reset Source: canfd_rst_mod_g_rst_n
7:6	MSI	R	0h	Message Storeage Indicator Reset Source: canfd_rst_mod_g_rst_n
5:0	BIDX	R	0h	Buffer Index Reset Source: canfd_rst_mod_g_rst_n

4.13.52 CFG_NDAT1 Registers

4.13.52.1 CFG_NDAT1 Register (Offset = 298h) [reset = 0h]

Short Description: NDAT1

Long Description: NDAT1

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Table 4-1393. Instance Table

Instance Name	Physical Address
MCAN0	5260 8298h
MCAN1	5261 8298h
MCAN2	5262 8298h
MCAN3	5263 8298h

Figure 4-615. NDAT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ND0_31															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ND0_31															
R/W															
0h															

Access Types Legend

Table 4-1394. NDAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ND0_31	R/W	0h	New Data 0-31 Reset Source: canfd_rst_mod_g_rst_n

4.13.53 CFG_NDAT2 Registers

4.13.53.1 CFG_NDAT2 Register (Offset = 29Ch) [reset = 0h]

Short Description: NDAT2

Long Description: NDAT2

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Table 4-1395. Instance Table

Instance Name	Physical Address
MCAN0	5260 829Ch
MCAN1	5261 829Ch
MCAN2	5262 829Ch
MCAN3	5263 829Ch

Figure 4-616. NDAT2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ND32_63															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ND32_63															
R/W															
0h															

Access Types Legend

Table 4-1396. NDAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ND32_63	R/W	0h	New Data 32-63 Reset Source: canfd_rst_mod_g_rst_n

4.13.54 CFG_RXF0C Registers

4.13.54.1 CFG_RXF0C Register (Offset = 2A0h) [reset = 0h]

Short Description: RXF0C

Long Description: RXF0C

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Table 4-1397. Instance Table

Instance Name	Physical Address
MCAN0	5260 82A0h
MCAN1	5261 82A0h
MCAN2	5262 82A0h
MCAN3	5263 82A0h

Figure 4-617. RXF0C Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
F0OM	F0WM							NU42_1	F0S						
R/W	R/W							R	R/W						
0h	0h							0h	0h						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU42	F0SA													NU41	
R	R/W													R	
0h	0h													0h	

Access Types Legend

Table 4-1398. RXF0C Register Field Descriptions

Bit	Field	Type	Reset	Description
31	F0OM	R/W	0h	Rx FIFO 0 Operation Mode Reset Source: canfd_rst_mod_g_rst_n
30:24	F0WM	R/W	0h	Rx FIFO 0 Watermark Reset Source: canfd_rst_mod_g_rst_n
23	NU42_1	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
22:16	F0S	R/W	0h	Rx FIFO 0 Size Reset Source: canfd_rst_mod_g_rst_n
15	NU42	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
14:2	F0SA	R/W	0h	Rx FIFO 0 Start Address Reset Source: canfd_rst_mod_g_rst_n
1:0	NU41	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n

4.13.55 CFG_RXF0S Registers

4.13.55.1 CFG_RXF0S Register (Offset = 2A4h) [reset = 0h]

Short Description: RXF0S

Long Description: RXF0S

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Table 4-1399. Instance Table

Instance Name	Physical Address
MCAN0	5260 82A4h
MCAN1	5261 82A4h
MCAN2	5262 82A4h
MCAN3	5263 82A4h

Figure 4-618. RXF0S Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU46						RF0L	F0F	NU45		F0PI					
R						R	R	R		R					
0h						0h	0h	0h		0h					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU44		F0GI						NU43	F0FL						
R		R						R	R						
0h		0h						0h	0h						

Access Types Legend

Table 4-1400. RXF0S Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	NU46	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
25	RF0L	R	0h	Rx FIFO 0 Message Lost Reset Source: canfd_rst_mod_g_rst_n
24	F0F	R	0h	Rx FIFO 0 Full Reset Source: canfd_rst_mod_g_rst_n
23:22	NU45	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
21:16	F0PI	R	0h	Rx FIFO 0 Put Index Reset Source: canfd_rst_mod_g_rst_n
15:14	NU44	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
13:8	F0GI	R	0h	Rx FIFO 0 Get Index Reset Source: canfd_rst_mod_g_rst_n
7	NU43	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
6:0	F0FL	R	0h	Rx FIFO 0 Fill Level Reset Source: canfd_rst_mod_g_rst_n

4.13.56 CFG_RXF0A Registers

4.13.56.1 CFG_RXF0A Register (Offset = 2A8h) [reset = 0h]

Short Description: RXF0A

Long Description: RXF0A

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Table 4-1401. Instance Table

Instance Name	Physical Address
MCAN0	5260 82A8h
MCAN1	5261 82A8h
MCAN2	5262 82A8h
MCAN3	5263 82A8h

Figure 4-619. RXF0A Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU47															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU47										F0AI					
R										R/W					
0h										0h					

Access Types Legend

Table 4-1402. RXF0A Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	NU47	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
5:0	F0AI	R/W	0h	Rx FIFO 0 Acknowledge Index Reset Source: canfd_rst_mod_g_rst_n

4.13.57 CFG_RXBC Registers

4.13.57.1 CFG_RXBC Register (Offset = 2ACh) [reset = 0h]

Short Description: RXBC

Long Description: RXBC

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Table 4-1403. Instance Table

Instance Name	Physical Address
MCAN0	5260 82ACh
MCAN1	5261 82ACh
MCAN2	5262 82ACh
MCAN3	5263 82ACh

Figure 4-620. RXBC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU49															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RBSA														NU48	
R/W														R	
0h														0h	

Access Types Legend

Table 4-1404. RXBC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	NU49	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
15:2	RBSA	R/W	0h	Rx Buffer Start Address Reset Source: canfd_rst_mod_g_rst_n
1:0	NU48	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n

4.13.58 CFG_RXF1C Registers

4.13.58.1 CFG_RXF1C Register (Offset = 2B0h) [reset = 0h]

Short Description: RXF1C

Long Description: RXF1C

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Table 4-1405. Instance Table

Instance Name	Physical Address
MCAN0	5260 82B0h
MCAN1	5261 82B0h
MCAN2	5262 82B0h
MCAN3	5263 82B0h

Figure 4-621. RXF1C Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
F1OM	F1WM							NU50_1	F1S						
R/W	R/W							R	R/W						
0h	0h							0h	0h						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU50	F1SA													NU499	
R	R/W													R	
0h	0h													0h	

Access Types Legend

Table 4-1406. RXF1C Register Field Descriptions

Bit	Field	Type	Reset	Description
31	F1OM	R/W	0h	Rx FIFO 0 Operation Mode Reset Source: canfd_rst_mod_g_rst_n
30:24	F1WM	R/W	0h	Rx FIFO 0 Watermark Reset Source: canfd_rst_mod_g_rst_n
23	NU50_1	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
22:16	F1S	R/W	0h	Rx FIFO 0 Size Reset Source: canfd_rst_mod_g_rst_n
15	NU50	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
14:2	F1SA	R/W	0h	Rx FIFO 0 Start Address Reset Source: canfd_rst_mod_g_rst_n
1:0	NU499	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n

4.13.59 CFG_RXF1S Registers

4.13.59.1 CFG_RXF1S Register (Offset = 2B4h) [reset = 0h]

Short Description: RXF1S

Long Description: RXF1S

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Table 4-1407. Instance Table

Instance Name	Physical Address
MCAN0	5260 82B4h
MCAN1	5261 82B4h
MCAN2	5262 82B4h
MCAN3	5263 82B4h

Figure 4-622. RXF1S Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU54						RF1L	F1F	NU53		F1PI					
R						R	R	R		R					
0h						0h	0h	0h		0h					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU52		F1GI						NU51	F1FL						
R		R						R	R						
0h		0h						0h	0h						

Access Types Legend

Table 4-1408. RXF1S Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	NU54	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
25	RF1L	R	0h	Rx FIFO 0 Message Lost Reset Source: canfd_rst_mod_g_rst_n
24	F1F	R	0h	Rx FIFO 0 Full Reset Source: canfd_rst_mod_g_rst_n
23:22	NU53	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
21:16	F1PI	R	0h	Rx FIFO 0 Put Index Reset Source: canfd_rst_mod_g_rst_n
15:14	NU52	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
13:8	F1GI	R	0h	Rx FIFO 0 Get Index Reset Source: canfd_rst_mod_g_rst_n
7	NU51	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
6:0	F1FL	R	0h	Rx FIFO 0 Fill Level Reset Source: canfd_rst_mod_g_rst_n

4.13.60 CFG_RXF1A Registers

4.13.60.1 CFG_RXF1A Register (Offset = 2B8h) [reset = 0h]

Short Description: RXF1A

Long Description: RXF1A

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Table 4-1409. Instance Table

Instance Name	Physical Address
MCAN0	5260 82B8h
MCAN1	5261 82B8h
MCAN2	5262 82B8h
MCAN3	5263 82B8h

Figure 4-623. RXF1A Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU55															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU55										F1AI					
R										R/W					
0h										0h					

Access Types Legend

Table 4-1410. RXF1A Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	NU55	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
5:0	F1AI	R/W	0h	Rx FIFO 0 Acknowledge Index Reset Source: canfd_rst_mod_g_rst_n

4.13.61 CFG_RXESC Registers

4.13.61.1 CFG_RXESC Register (Offset = 2BCh) [reset = 0h]

Short Description: RXESC

Long Description: RXESC

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Table 4-1411. Instance Table

Instance Name	Physical Address
MCAN0	5260 82BCh
MCAN1	5261 82BCh
MCAN2	5262 82BCh
MCAN3	5263 82BCh

Figure 4-624. RXESC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU58															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU58					RBDS			NU57	F1DS			NU56	F0DS		
R					R/W			R	R/W			R	R/W		
0h					0h			0h	0h			0h	0h		

Access Types Legend

Table 4-1412. RXESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	NU58	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
10:8	RBDS	R/W	0h	Rx Buffer data Field Size Reset Source: canfd_rst_mod_g_rst_n
7	NU57	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
6:4	F1DS	R/W	0h	Rx FIFO 1 Data Field Size Reset Source: canfd_rst_mod_g_rst_n
3	NU56	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
2:0	F0DS	R/W	0h	Rx FIFO 0 Data Field Size Reset Source: canfd_rst_mod_g_rst_n

4.13.62 CFG_TXBC Registers

4.13.62.1 CFG_TXBC Register (Offset = 2C0h) [reset = 0h]

Short Description: TXBC

Long Description: TXBC

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Table 4-1413. Instance Table

Instance Name	Physical Address
MCAN0	5260 82C0h
MCAN1	5261 82C0h
MCAN2	5262 82C0h
MCAN3	5263 82C0h

Figure 4-625. TXBC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU61	TFQM	TFQS						NU60		NDTB					
R	R	R						R		R					
0h	0h	0h						0h		0h					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBSA														NU59	
R														R	
0h														0h	

Access Types Legend

Table 4-1414. TXBC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NU61	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
30	TFQM	R	0h	Tx FIFO/Queue Mode Reset Source: canfd_rst_mod_g_rst_n
29:24	TFQS	R	0h	Transmit FIFO/Queue Size Reset Source: canfd_rst_mod_g_rst_n
23:22	NU60	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
21:16	NDTB	R	0h	Number of Dedicated Transmit Buffers Reset Source: canfd_rst_mod_g_rst_n
15:2	TBSA	R	0h	Tx Buffers Start Address Reset Source: canfd_rst_mod_g_rst_n
1:0	NU59	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n

4.13.63 CFG_TXFQS Registers

4.13.63.1 CFG_TXFQS Register (Offset = 2C4h) [reset = 0h]

Short Description: TXFQS

Long Description: TXFQS

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Table 4-1415. Instance Table

Instance Name	Physical Address
MCAN0	5260 82C4h
MCAN1	5261 82C4h
MCAN2	5262 82C4h
MCAN3	5263 82C4h

Figure 4-626. TXFQS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU64										TFQF	TFQPI				
R										R	R				
0h										0h	0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU63			TFGI					NU62		TFFL					
R			R					R		R					
0h			0h					0h		0h					

Access Types Legend

Table 4-1416. TXFQS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	NU64	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
21	TFQF	R	0h	Tx FIFO/Queue Full Reset Source: canfd_rst_mod_g_rst_n
20:16	TFQPI	R	0h	Tx FIFO/Queue Put Index Reset Source: canfd_rst_mod_g_rst_n
15:13	NU63	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
12:8	TFGI	R	0h	Tx Queue Get Index Reset Source: canfd_rst_mod_g_rst_n
7:6	NU62	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
5:0	TFFL	R	0h	Tx FIFO Free Level Reset Source: canfd_rst_mod_g_rst_n

4.13.64 CFG_TXESC Registers

4.13.64.1 CFG_TXESC Register (Offset = 2C8h) [reset = 0h]

Short Description: TXESC

Long Description: TXESC

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Table 4-1417. Instance Table

Instance Name	Physical Address
MCAN0	5260 82C8h
MCAN1	5261 82C8h
MCAN2	5262 82C8h
MCAN3	5263 82C8h

Figure 4-627. TXESC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU65															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU65													TBDS		
R													R/W		
0h													0h		

Access Types Legend

Table 4-1418. TXESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	NU65	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
2:0	TBDS	R/W	0h	Tx Buffer Data Field Size Reset Source: canfd_rst_mod_g_rst_n

4.13.65 CFG_TXBRP Registers

4.13.65.1 CFG_TXBRP Register (Offset = 2CCh) [reset = 0h]

Short Description: TXBRP

Long Description: TXBRP

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Table 4-1419. Instance Table

Instance Name	Physical Address
MCAN0	5260 82CCh
MCAN1	5261 82CCh
MCAN2	5262 82CCh
MCAN3	5263 82CCh

Figure 4-628. TXBRP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TRP															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRP															
R															
0h															

Access Types Legend

Table 4-1420. TXBRP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TRP	R	0h	Transmission Request Pending Reset Source: canfd_rst_mod_g_rst_n

4.13.66 CFG_TXBAR Registers

4.13.66.1 CFG_TXBAR Register (Offset = 2D0h) [reset = 0h]

Short Description: TXBAR

Long Description: TXBAR

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Table 4-1421. Instance Table

Instance Name	Physical Address
MCAN0	5260 82D0h
MCAN1	5261 82D0h
MCAN2	5262 82D0h
MCAN3	5263 82D0h

Figure 4-629. TXBAR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
NONE															
0															

Access Types Legend

Table 4-1422. TXBAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE		Reserved

4.13.67 ECC_REV Registers

4.13.67.1 ECC_REV Register (Offset = 0h) [reset = 66a0ea00h]

Short Description: Aggregator Revision Regis

Long Description: Aggregator Revision Register

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Table 4-1423. Instance Table

Instance Name	Physical Address
MCAN0	5270 0000h
MCAN1	5270 1000h
MCAN2	5270 2000h
MCAN3	5270 3000h

Figure 4-630. REV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R		R		R											
1h		2h		6a0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
R					R			R		R					
1dh					2h			0h		0h					

Access Types Legend

Table 4-1424. REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme Reset Source: canfd_rst_mod_g_rst_n
29:28	BU	R	2h	bu Reset Source: canfd_rst_mod_g_rst_n
27:16	MODULE_ID	R	6A0h	Module ID Reset Source: canfd_rst_mod_g_rst_n
15:11	REVRTL	R	1Dh	RTL version Reset Source: canfd_rst_mod_g_rst_n
10:8	REVMAJ	R	2h	Major version Reset Source: canfd_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom version Reset Source: canfd_rst_mod_g_rst_n
5:0	REVMIN	R	0h	Minor version Reset Source: canfd_rst_mod_g_rst_n

4.13.68 ECC_VECTOR Registers

4.13.68.1 ECC_VECTOR Register (Offset = 8h) [reset = 0h]

Short Description: ECC Vector Register

Long Description: ECC Vector Register

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Table 4-1425. Instance Table

Instance Name	Physical Address
MCAN0	5270 0008h
MCAN1	5270 1008h
MCAN2	5270 2008h
MCAN3	5270 3008h

Figure 4-631. VECTOR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU1							RD_SVBUS_DONE	RD_SVBUS_ADDR							
R							R/W	R/W							
0h							0h	0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RD_SVBUS	NU0				ECC_VEC										
R/W	R				R/W										
0h	0h				0h										

Access Types Legend

Table 4-1426. VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	NU1	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
24	RD_SVBUS_DONE	R/W	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reset Source: canfd_rst_mod_g_rst_n
23:16	RD_SVBUS_ADDR	R/W	0h	Read address Reset Source: canfd_rst_mod_g_rst_n
15	RD_SVBUS	R/W	0h	Write 1 to trigger a read on the serial VBUS. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field. Reset Source: canfd_rst_mod_g_rst_n
14:11	NU0	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
10:0	ECC_VEC	R/W	0h	Value written to select the corresponding ECC RAM for control or status Reset Source: canfd_rst_mod_g_rst_n

4.13.69 ECC_STAT Registers

4.13.69.1 ECC_STAT Register (Offset = Ch) [reset = 2h]

Short Description: Misc Status

Long Description: Misc Status

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Table 4-1427. Instance Table

Instance Name	Physical Address
MCAN0	5270 000Ch
MCAN1	5270 100Ch
MCAN2	5270 200Ch
MCAN3	5270 300Ch

Figure 4-632. STAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU2															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU2					NUM_RAMS										
R					R										
0h					2h										

Access Types Legend

Table 4-1428. STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	NU2	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
10:0	NUM_RAMS	R	2h	Indicates the number of RAMS serviced by the ECC aggregator Reset Source: canfd_rst_mod_g_rst_n

4.13.70 ECC_CTRL Registers

4.13.70.1 ECC_CTRL Register (Offset = 14h) [reset = 107h]

Short Description: CTRL

Long Description: CTRL

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Table 4-1429. Instance Table

Instance Name	Physical Address
MCAN0	5270 0014h
MCAN1	5270 1014h
MCAN2	5270 2014h
MCAN3	5270 3014h

Figure 4-633. CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU3															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU3							CHECK	RESERVED	ERROR_ONCE	FORCE_N_ROW	FORCE_DED	FORCE_SEC	EN_RMW	ECC_CHK	ECC_EN
R							R/W	NONE	W	W	W	W	W	W	W
0h							1h	0	0h	0h	0h	0h	1h	1h	1h

Access Types Legend

Table 4-1430. CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	NU3	R	0h	TI Internal : Reserved Reset Source: canfd_rst_mod_g_rst_n
8	CHECK	R/W	1h	TI Internal : Check Parity TI Internal : Check timeout Reset Source: canfd_rst_mod_g_rst_n
7	RESERVED	NONE		Reserved
6	ERROR_ONCE	W	0h	TI Internal : Force Error only once Reset Source: canfd_rst_mod_g_rst_n
5	FORCE_N_ROW	W	0h	TI Internal : Force Error on any RAM read Reset Source: canfd_rst_mod_g_rst_n
4	FORCE_DED	W	0h	TI Internal : Force Double Bit Error Reset Source: canfd_rst_mod_g_rst_n
3	FORCE_SEC	W	0h	TI Internal : Force Single Bit Error Reset Source: canfd_rst_mod_g_rst_n
2	EN_RMW	W	1h	TI Internal : Enable rmw Reset Source: canfd_rst_mod_g_rst_n
1	ECC_CHK	W	1h	TI Internal : Enable ECC check Reset Source: canfd_rst_mod_g_rst_n
0	ECC_EN	W	1h	TI Internal : Enable ECC Reset Source: canfd_rst_mod_g_rst_n

4.13.71 ECC_ERR_CTRL1 Registers

4.13.71.1 ECC_CTRL1 Register (Offset = 18h) [reset = 0h]

Short Description: ERR_CTRL1

Long Description: ERR_CTRL1

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Table 4-1431. Instance Table

Instance Name	Physical Address
MCAN0	5270 0018h
MCAN1	5270 1018h
MCAN2	5270 2018h
MCAN3	5270 3018h

Figure 4-634. ERR_CTRL1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_ROW															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_ROW															
R/W															
0h															

Access Types Legend

Table 4-1432. ERR_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ECC_ROW	R/W	0h	TI Internal : Row address where single or double-bit error needs to be applied. This is ignored if force_n_row is set Reset Source: canfd_rst_mod_g_rst_n

4.13.72 ECC_ERR_CTRL2 Registers

4.13.72.1 ECC_CTRL2 Register (Offset = 1Ch) [reset = 0h]

Short Description: ERR_CTRL2

Long Description: ERR_CTRL2

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Table 4-1433. Instance Table

Instance Name	Physical Address
MCAN0	5270 001Ch
MCAN1	5270 101Ch
MCAN2	5270 201Ch
MCAN3	5270 301Ch

Figure 4-635. ERR_CTRL2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_BIT2															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_BIT1															
R/W															
0h															

Access Types Legend

Table 4-1434. ERR_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ECC_BIT2	R/W	0h	TI Internal : Data bit that needs to be flipped if double bit error needs to be forced Reset Source: canfd_rst_mod_g_rst_n
15:0	ECC_BIT1	R/W	0h	TI Internal : Data bit that needs to be flipped when force_sec is set Reset Source: canfd_rst_mod_g_rst_n

4.13.73 ECC_ERR_STAT1 Registers

4.13.73.1 ECC_STAT1 Register (Offset = 20h) [reset = 0h]

Short Description: ERR_STAT1

Long Description: ERR_STAT1

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Table 4-1435. Instance Table

Instance Name	Physical Address
MCAN0	5270 0020h
MCAN1	5270 1020h
MCAN2	5270 2020h
MCAN3	5270 3020h

Figure 4-636. ERR_STAT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_BIT1_STS															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR_ECC_CTRL_REG	CLR_ECC_PAR		CLR_ECC_OTHER	CLR_ECC_DED		CLR_ECC_SEC		ECC_CTRL_REG	ECC_PAR		ECC_OTHER	ECC_DED		ECC_SEC	
W	W		W	W		W		W	W		W	W		W	
0h	0h		0h	0h		0h		0h	0h		0h	0h		0h	

Access Types Legend

Table 4-1436. ERR_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ECC_BIT1_STS	R	0h	TI Internal : Data bit that corresponds to the single-bit error Reset Source: canfd_rst_mod_g_rst_n
15	CLR_ECC_CTRL_REG	W	0h	TI Internal : Clear Ctrl Reg Error Status. Write 1 to clear. This bit is self clearing. Reset Source: canfd_rst_mod_g_rst_n
14:13	CLR_ECC_PAR	W	0h	TI Internal : Clear Parity Error Status. Write 1 to clear. This bit is self clearing. Reset Source: canfd_rst_mod_g_rst_n
12	CLR_ECC_OTHER	W	0h	TI Internal : Clear Other Error Status. Write 1 to clear. This bit is self clearing. Reset Source: canfd_rst_mod_g_rst_n
11:10	CLR_ECC_DED	W	0h	TI Internal : Clear Double Bit Error Status. Write 1 to clear. This bit is self clearing. Reset Source: canfd_rst_mod_g_rst_n
9:8	CLR_ECC_SEC	W	0h	TI Internal : Clear Single Bit Error Status. Write 1 to clear. This bit is self clearing. Reset Source: canfd_rst_mod_g_rst_n
7	ECC_CTRL_REG	W	0h	TI Internal : Force ctrl reg pending interrupt. Write 1 to set. This bit is self clearing. Reset Source: canfd_rst_mod_g_rst_n
6:5	ECC_PAR	W	0h	TI Internal : Force ECC parity pending interrupt. Write 1 to set. This bit is self clearing. Reset Source: canfd_rst_mod_g_rst_n
4	ECC_OTHER	W	0h	TI Internal : Force ECC other pending interrupt. Write 1 to set. This bit is self clearing. Reset Source: canfd_rst_mod_g_rst_n
3:2	ECC_DED	W	0h	TI Internal : Force ECC DED pending interrupt. Write 1 to set. This bit is self clearing. Reset Source: canfd_rst_mod_g_rst_n
1:0	ECC_SEC	W	0h	TI Internal : Force ECC SEC pending interrupt. Write 1 to set. This bit is self clearing. Reset Source: canfd_rst_mod_g_rst_n

4.13.74 ECC_ERR_STAT2 Registers

4.13.74.1 ECC_STAT2 Register (Offset = 24h) [reset = 0h]

Short Description: ERR_STAT2

Long Description: ERR_STAT2

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Table 4-1437. Instance Table

Instance Name	Physical Address
MCAN0	5270 0024h
MCAN1	5270 1024h
MCAN2	5270 2024h
MCAN3	5270 3024h

Figure 4-637. ERR_STAT2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_ROW															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_ROW															
R															
0h															

Access Types Legend

Table 4-1438. ERR_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ECC_ROW	R	0h	TI Internal : Row address where the single or double-bit error has occurred Reset Source: canfd_rst_mod_g_rst_n

4.13.75 ECC_ERR_STAT3 Registers

4.13.75.1 ECC_STAT3 Register (Offset = 28h) [reset = 0h]

Short Description: ERR_STAT3

Long Description: ERR_STAT3

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Table 4-1439. Instance Table

Instance Name	Physical Address
MCAN0	5270 0028h
MCAN1	5270 1028h
MCAN2	5270 2028h
MCAN3	5270 3028h

Figure 4-638. ERR_STAT3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU6															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU6						CLR_TIMEOUT_PEND		NU5						TIMEOUT_PEND	NU4
R						W		R						W	R
0h						0h		0h						0h	0h

Access Types Legend

Table 4-1440. ERR_STAT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	NU6	R	0h	TI Internal : Reserved Reset Source: canfd_rst_mod_g_rst_n
9	CLR_TIMEOUT_PEND	W	0h	TI Internal : Clear timeout pending Reset Source: canfd_rst_mod_g_rst_n
8:2	NU5	R	0h	TI Internal : Reserved Reset Source: canfd_rst_mod_g_rst_n
1	TIMEOUT_PEND	W	0h	TI Internal : Timeout pending Reset Source: canfd_rst_mod_g_rst_n
0	NU4	R	0h	TI Internal : Reserved Reset Source: canfd_rst_mod_g_rst_n

4.13.76 ECC_SEC_EOI_REG Registers

4.13.76.1 ECC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

Short Description: EOI Register

Long Description: EOI Register

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Table 4-1441. Instance Table

Instance Name	Physical Address
MCAN0	5270 003Ch
MCAN1	5270 103Ch
MCAN2	5270 203Ch
MCAN3	5270 303Ch

Figure 4-639. SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU7															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU7															SEC_EOI_WR
R															R/W
0h															0h

Access Types Legend

Table 4-1442. SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	NU7	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
0	SEC_EOI_WR	R/W	0h	EOI Register. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field. This bit is self clearing, reading this bit will return 0. Reset Source: canfd_rst_mod_g_rst_n

4.13.77 ECC_SEC_STATUS_REG0 Registers

4.13.77.1 ECC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Short Description: Interrupt Status Register

Long Description: Interrupt Status Register 0

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Table 4-1443. Instance Table

Instance Name	Physical Address
MCAN0	5270 0040h
MCAN1	5270 1040h
MCAN2	5270 2040h
MCAN3	5270 3040h

Figure 4-640. SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU8															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU8														CTRL_EDC_VBUSS_PEND	SEC_PEND
R														R	R
0h														0h	0h

Access Types Legend

Table 4-1444. SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	NU8	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
1	CTRL_EDC_VBUSS_PEND	R	0h	Interrupt Pending Status for ctrl_edc_vbuss_pend. Reset Source: canfd_rst_mod_g_rst_n
0	SEC_PEND	R	0h	Interrupt Pending Status for msgmem_pend. Reset Source: canfd_rst_mod_g_rst_n

4.13.78 ECC_SEC_ENABLE_SET_REG0 Registers

4.13.78.1 ECC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Short Description: Interrupt Enable Set Regi

Long Description: Interrupt Enable Set Register 0

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Table 4-1445. Instance Table

Instance Name	Physical Address
MCAN0	5270 0080h
MCAN1	5270 1080h
MCAN2	5270 2080h
MCAN3	5270 3080h

Figure 4-641. SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU9															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU9														CTRL_EDC_VBUSS_ENABLE_SET	SEC_EN_SET
R														R/W	R/W
0h														0h	0h

Access Types Legend

Table 4-1446. SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	NU9	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
1	CTRL_EDC_VBUSS_ENABLE_SET	R/W	0h	Interrupt Enable Set Register for ctrl_edc_vbuss_pend. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field. Reset Source: canfd_rst_mod_g_rst_n
0	SEC_EN_SET	R/W	0h	Interrupt Enable Set Register for msgmem_pend. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field. Reset Source: canfd_rst_mod_g_rst_n

4.13.79 ECC_SEC_ENABLE_CLR_REG0 Registers

4.13.79.1 ECC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Short Description: Interrupt Enable Clear Re

Long Description: Interrupt Enable Clear Register 0

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Table 4-1447. Instance Table

Instance Name	Physical Address
MCAN0	5270 00C0h
MCAN1	5270 10C0h
MCAN2	5270 20C0h
MCAN3	5270 30C0h

Figure 4-642. SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU10															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU10														CTRL_EDC_VBUSS_ENABLE_CLR	SEC_EN_CLR
R														R/W	R/W
0h														0h	0h

Access Types Legend

Table 4-1448. SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	NU10	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
1	CTRL_EDC_VBUSS_ENABLE_CLR	R/W	0h	Interrupt Enable Clear Register for ctrl_edc_vbuss_pend. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0. Reset Source: canfd_rst_mod_g_rst_n
0	SEC_EN_CLR	R/W	0h	Interrupt Enable Clear Register for msgmem_pend. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0. Reset Source: canfd_rst_mod_g_rst_n

4.13.80 ECC_DED_EOI_REG Registers

4.13.80.1 ECC_EOI_REG Register (Offset = 13Ch) [reset = 0h]

Short Description: EOI Register

Long Description: EOI Register

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Table 4-1449. Instance Table

Instance Name	Physical Address
MCAN0	5270 013Ch
MCAN1	5270 113Ch
MCAN2	5270 213Ch
MCAN3	5270 313Ch

Figure 4-643. DED_EOI_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU11															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU11															DED_EOI_WR
R															R/W
0h															0h

Access Types Legend

Table 4-1450. DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	NU11	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
0	DED_EOI_WR	R/W	0h	EOI Register. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field. This bit is self clearing, reading this bit will return 0. Reset Source: canfd_rst_mod_g_rst_n

4.13.81 ECC_DED_STATUS_REG0 Registers

4.13.81.1 ECC_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Short Description: Interrupt Status Register

Long Description: Interrupt Status Register 0

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Table 4-1451. Instance Table

Instance Name	Physical Address
MCAN0	5270 0140h
MCAN1	5270 1140h
MCAN2	5270 2140h
MCAN3	5270 3140h

Figure 4-644. DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU12															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU12														CTRL_EDC_VBUSS_PEND	DED_PEND
R														R	R
0h														0h	0h

Access Types Legend

Table 4-1452. DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	NU12	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
1	CTRL_EDC_VBUSS_PEND	R	0h	Interrupt Pending Status for ctrl_edc_vbuss_pend. Reset Source: canfd_rst_mod_g_rst_n
0	DED_PEND	R	0h	Interrupt Pending Status for msgmem_pend. Reset Source: canfd_rst_mod_g_rst_n

4.13.82 ECC_DED_ENABLE_SET_REG0 Registers

4.13.82.1 ECC_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Short Description: Interrupt Enable Set Regi

Long Description: Interrupt Enable Set Register 0

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Table 4-1453. Instance Table

Instance Name	Physical Address
MCAN0	5270 0180h
MCAN1	5270 1180h
MCAN2	5270 2180h
MCAN3	5270 3180h

Figure 4-645. DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU13															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU13														CTRL_EDC_VBUSS_ENABLE_SET	DED_EN_SET
R														R/W	R/W
0h														0h	0h

Access Types Legend

Table 4-1454. DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	NU13	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
1	CTRL_EDC_VBUSS_ENABLE_SET	R/W	0h	Interrupt Enable Set Register for ctrl_edc_vbuss_pend. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field. Reset Source: canfd_rst_mod_g_rst_n
0	DED_EN_SET	R/W	0h	Interrupt Enable Set Register for msgmem_pend. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field. Reset Source: canfd_rst_mod_g_rst_n

4.13.83 ECC_DED_ENABLE_CLR_REG0 Registers

4.13.83.1 ECC_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Short Description: Interrupt Enable Clear Re

Long Description: Interrupt Enable Clear Register 0

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Table 4-1455. Instance Table

Instance Name	Physical Address
MCAN0	5270 01C0h
MCAN1	5270 11C0h
MCAN2	5270 21C0h
MCAN3	5270 31C0h

Figure 4-646. DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU14															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU14														CTRL_EDC_VBUSS_ENABLE_CLR	DED_EN_CLR
R														R/W	R/W
0h														0h	0h

Access Types Legend

Table 4-1456. DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	NU14	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
1	CTRL_EDC_VBUSS_ENABLE_CLR	R/W	0h	Interrupt Enable Clear Register for ctrl_edc_vbuss_pend. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0. Reset Source: canfd_rst_mod_g_rst_n
0	DED_EN_CLR	R/W	0h	Interrupt Enable Clear Register for msgmem_pend. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0. Reset Source: canfd_rst_mod_g_rst_n

4.13.84 ECC_AGGR_ENABLE_SET Registers

4.13.84.1 ECC_ENABLE_SET Register (Offset = 200h) [reset = 0h]

Short Description: AGGR interrupt enable set

Long Description: AGGR interrupt enable set Register

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Table 4-1457. Instance Table

Instance Name	Physical Address
MCAN0	5270 0200h
MCAN1	5270 1200h
MCAN2	5270 2200h
MCAN3	5270 3200h

Figure 4-647. AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU15															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU15														TIMEOUT	PARITY
R														R/W	R/W
0h														0h	0h

Access Types Legend

Table 4-1458. AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	NU15	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
1	TIMEOUT	R/W	0h	Interrupt Enable Set Register for svbus timeout errors. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field. Reset Source: canfd_rst_mod_g_rst_n
0	PARITY	R/W	0h	Interrupt Enable Set Register for parity errors. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field. Reset Source: canfd_rst_mod_g_rst_n

4.13.85 ECC_AGGR_ENABLE_CLR Registers

4.13.85.1 ECC_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

Short Description: AGGR interrupt enable cle

Long Description: AGGR interrupt enable clear Register

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Table 4-1459. Instance Table

Instance Name	Physical Address
MCAN0	5270 0204h
MCAN1	5270 1204h
MCAN2	5270 2204h
MCAN3	5270 3204h

Figure 4-648. AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU16															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU16														TIMEOUT	PARITY
R														R/W	R/W
0h														0h	0h

Access Types Legend

Table 4-1460. AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	NU16	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
1	TIMEOUT	R/W	0h	Interrupt Enable Clear for svbus timeout errors. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0. Reset Source: canfd_rst_mod_g_rst_n
0	PARITY	R/W	0h	Interrupt Enable Clear for parity errors. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0. Reset Source: canfd_rst_mod_g_rst_n

4.13.86 ECC_AGGR_STATUS_SET Registers

4.13.86.1 ECC_STATUS_SET Register (Offset = 208h) [reset = 0h]

Short Description: AGGR interrupt status set

Long Description: AGGR interrupt status set Register

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Table 4-1461. Instance Table

Instance Name	Physical Address
MCAN0	5270 0208h
MCAN1	5270 1208h
MCAN2	5270 2208h
MCAN3	5270 3208h

Figure 4-649. AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU17															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU17												TIMEOUT		PARITY	
R												R/W		R/W	
0h												0h		0h	

Access Types Legend

Table 4-1462. AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	NU17	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
3:2	TIMEOUT	R/W	0h	Interrupt status set for svbus timeout errors. A write to increment field. Writing a value to this field increment the field value by the value written. Reads do not alter the value of the field. Reset Source: canfd_rst_mod_g_rst_n
1:0	PARITY	R/W	0h	Interrupt status set for parity errors. A write to increment field. Writing a value to this field increment the field value by the value written. Reads do not alter the value of the field. Reset Source: canfd_rst_mod_g_rst_n

4.13.87 ECC_AGGR_STATUS_CLR Registers

4.13.87.1 ECC_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

Short Description: AGGR interrupt status cle

Long Description: AGGR interrupt status clear Register

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Table 4-1463. Instance Table

Instance Name	Physical Address
MCAN0	5270 020Ch
MCAN1	5270 120Ch
MCAN2	5270 220Ch
MCAN3	5270 320Ch

Figure 4-650. AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU18															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU18												TIMEOUT		PARITY	
R												R/W		R/W	
0h												0h		0h	

Access Types Legend

Table 4-1464. AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	NU18	R	0h	Reserved Reset Source: canfd_rst_mod_g_rst_n
3:2	TIMEOUT	R/W	0h	Interrupt status clear for svbus timeout errors. A write to decrement field. Writing a value to this field decrements the field value by the value written. Reads do not alter the value of the field. Reset Source: canfd_rst_mod_g_rst_n
1:0	PARITY	R/W	0h	Interrupt status clear for parity errors. A write to decrement field. Writing a value to this field decrements the field value by the value written. Reads do not alter the value of the field. Reset Source: canfd_rst_mod_g_rst_n

4.13.88 Access Table

Table 4-1465. Access Type Codes

Access Type	Code	Description
R/W	R/W	Read / Write
R	R	Read
W	W	Write

4.14 MCRC Registers

Table 4-1466. MEM, MEM Registers, Base Address=0X0000000035000000, Length=4096

Offset	Length	Register Name	mcrc0 Physical Address
0h	32	CRC_CTRL0	3500 0000h
8h	32	CRC_CTRL1	3500 0008h
10h	32	CRC_CTRL2	3500 0010h
18h	32	CRC_INTS	3500 0018h
20h	32	CRC_INTR	3500 0020h
28h	32	CRC_STATUS_REG	3500 0028h
30h	32	CRC_INT_OFFSET_REG	3500 0030h
38h	32	CRC_BUSY	3500 0038h
40h	32	CRC_PCOUNT_REG1	3500 0040h
44h	32	CRC_SCOUNT_REG1	3500 0044h
48h	32	CRC_CURSEC_REG1	3500 0048h
4Ch	32	CRC_WDTOPLD1	3500 004Ch
50h	32	CRC_BCTOPLD1	3500 0050h
60h	32	PSA_SIGREGL1	3500 0060h
64h	32	PSA_SIGREGH1	3500 0064h
68h	32	CRC_REGL1	3500 0068h
6Ch	32	CRC_REGH1	3500 006Ch
70h	32	PSA_SECSIGREGL1	3500 0070h
74h	32	PSA_SECSIGREGH1	3500 0074h
78h	32	RAW_DATAREGL1	3500 0078h
7Ch	32	RAW_DATAREGH1	3500 007Ch
80h	32	CRC_PCOUNT_REG2	3500 0080h
84h	32	CRC_SCOUNT_REG2	3500 0084h
88h	32	CRC_CURSEC_REG2	3500 0088h
8Ch	32	CRC_WDTOPLD2	3500 008Ch
90h	32	CRC_BCTOPLD2	3500 0090h
A0h	32	PSA_SIGREGL2	3500 00A0h
A4h	32	PSA_SIGREGH2	3500 00A4h
A8h	32	CRC_REGL2	3500 00A8h
ACh	32	CRC_REGH2	3500 00ACh
B0h	32	PSA_SECSIGREGL2	3500 00B0h
B4h	32	PSA_SECSIGREGH2	3500 00B4h
B8h	32	RAW_DATAREGL2	3500 00B8h
BCh	32	RAW_DATAREGH2	3500 00BCh
C0h	32	CRC_PCOUNT_REG3	3500 00C0h
C4h	32	CRC_SCOUNT_REG3	3500 00C4h
C8h	32	CRC_CURSEC_REG3	3500 00C8h
CCh	32	CRC_WDTOPLD3	3500 00CCh
D0h	32	CRC_BCTOPLD3	3500 00D0h
E0h	32	PSA_SIGREGL3	3500 00E0h
E4h	32	PSA_SIGREGH3	3500 00E4h
E8h	32	CRC_REGL3	3500 00E8h
ECh	32	CRC_REGH3	3500 00ECh
F0h	32	PSA_SECSIGREGL3	3500 00F0h
F4h	32	PSA_SECSIGREGH3	3500 00F4h

Table 4-1466. MEM, MEM Registers, Base Address=0X0000000035000000, Length=4096 (continued)

Offset	Length	Register Name	mcrc0 Physical Address
F8h	32	RAW_DATAREGL3	3500 00F8h
FCh	32	RAW_DATAREGH3	3500 00FCh
100h	32	CRC_PCOUNT_REG4	3500 0100h
104h	32	CRC_SCOUNT_REG4	3500 0104h
108h	32	CRC_CURSEC_REG4	3500 0108h
10Ch	32	CRC_WDTOPLD4	3500 010Ch
110h	32	CRC_BCTOPLD4	3500 0110h
120h	32	PSA_SIGREGL4	3500 0120h
124h	32	PSA_SIGREGH4	3500 0124h
128h	32	CRC_REGL4	3500 0128h
12Ch	32	CRC_REGH4	3500 012Ch
130h	32	PSA_SECSIGREGL4	3500 0130h
134h	32	PSA_SECSIGREGH4	3500 0134h
138h	32	RAW_DATAREGL4	3500 0138h
13Ch	32	RAW_DATAREGH4	3500 013Ch
140h	32	MCRC_BUS_SEL	3500 0140h
144h	32	MCRC_RESERVED	3500 0144h

4.14.1 MEM_CRC_CTRL0 Registers

4.14.1.1 MEM_CTRL0 Register (Offset = 0h) [reset = 0h]

Short Description: Contains sw reset control

Long Description: Contains sw reset control bit to reset PSA

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Table 4-1467. Instance Table

Instance Name	Physical Address
MCRC0	3500 0000h

Figure 4-651. CRC_CTRL0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU12	NU11	NU10	NU9		NU8		NU7	NU6	NU5	NU4	NU3		NU2		NU1
R	R	R	R		R		R	R	R	R	R		R		R
0h	0h	0h	0h		0h		0h	0h	0h	0h	0h		0h		0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH2_CRC_SEL2	CH2_BYTE_SWAP	CH2_BIT_SWAP	CH2_CRC_SEL		CH2_DW_SEL		CH2_PSA_SWREST	CH1_CRC_SEL2	CH1_BYTE_SWAP	CH1_BIT_SWAP	CH1_CRC_SEL		CH1_DW_SEL		CH1_PSA_SWREST
R/W	R/W	R/W	R/W		R/W		R/W	R/W	R/W	R/W	R/W		R/W		R/W
0h	0h	0h	0h		0h		0h	0h	0h	0h	0h		0h		0h

Access Types Legend

Table 4-1468. CRC_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NU12	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
30	NU11	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
29	NU10	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
28:27	NU9	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
26:25	NU8	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
24	NU7	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
23	NU6	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
22	NU5	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
21	NU4	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
20:19	NU3	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
18:17	NU2	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
16	NU1	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
15	CH2_CRC_SEL2	R/W	0h	Refer "CH2_DW_SEL" field description Reset Source: mcrc_rst_mod_g_rst_n
14	CH2_BYTE_SWAP	R/W	0h	BYTE SWAP Enable across Data Size 0 Byte Swap Disabled 1 Byte Swap enabled. Reset Source: mcrc_rst_mod_g_rst_n
13	CH2_BIT_SWAP	R/W	0h	msb/lsb SWAPPING 0 msb [most significant bit First] 1 lsb [least significant bit First] Reset Source: mcrc_rst_mod_g_rst_n
12:11	CH2_CRC_SEL	R/W	0h	CRC type select. {CH1_CRC_SEL2,CH1_CRC_SEL[1:0]} 000 CRC-64 001 - CRC-16 010 CRC-32 100 - VDA CAN, SAE-J1850 CRC-8 101 - H2F, Autosar 4.0 110 - CASTAGNOLI, iSCSI 111 / 011 - E2E Profile 4 Reset Source: mcrc_rst_mod_g_rst_n
10:9	CH2_DW_SEL	R/W	0h	CRC Data Size select. 000 64 bit Data Size 001 - 16 bit Data Size 010 32 Bit Data Size Reset Source: mcrc_rst_mod_g_rst_n

Table 4-1468. CRC_CTRL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	CH2_PSA_SWREST	R/W	0h	Channel 2 PSA Software Reset. When set, the PSA Signature Register is reset to all zero. Software reset does not reset software reset bit itself. Therefore, CPU is required to clear this bit by writing a 0. 0 = PSA Signature Register not reset 1 = PSA Signature Register reset Reset Source: mcrc_rst_mod_g_rst_n
7	CH1_CRC_SEL2	R/W	0h	Refer "CH1_DW_SEL" field description Reset Source: mcrc_rst_mod_g_rst_n
6	CH1_BYTE_SWAP	R/W	0h	BYTE SWAP Enable across Data Size 0 Byte Swap Disabled 1 Byte Swap enabled. Reset Source: mcrc_rst_mod_g_rst_n
5	CH1_BIT_SWAP	R/W	0h	msb/lsb SWAPPING 0 msb [most significant bit First] 1 lsb [least significant bit First] Reset Source: mcrc_rst_mod_g_rst_n
4:3	CH1_CRC_SEL	R/W	0h	CRC type select. {CH1_CRC_SEL2,CH1_CRC_SEL[1:0]} 000 CRC-64 001 - CRC-16 010 CRC-32 100 - VDA CAN, SAE-J1850 CRC-8 101 - H2F, Autosar 4.0 110 - CASTAGNOLI, iSCSI 111 / 011 - E2E Profile 4 Reset Source: mcrc_rst_mod_g_rst_n
2:1	CH1_DW_SEL	R/W	0h	CRC Data Size select. 000 64 bit Data Size 001 - 16 bit Data Size 010 32 Bit Data Size Reset Source: mcrc_rst_mod_g_rst_n
0	CH1_PSA_SWREST	R/W	0h	Channel 1 PSA Software Reset. When set, the PSA Signature Register is reset to all zero. Software reset does not reset software reset bit itself. Therefore, CPU is required to clear this bit by writing a 0. 0 = PSA Signature Register not reset 1 = PSA Signature Register reset Reset Source: mcrc_rst_mod_g_rst_n

4.14.2 MEM_CRC_CTRL1 Registers

4.14.2.1 MEM_CTRL1 Register (Offset = 8h) [reset = 0h]

Short Description: Contains power down contr

Long Description: Contains power down control bit

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Table 4-1469. Instance Table

Instance Name	Physical Address
MCRC0	3500 0008h

Figure 4-652. CRC_CTRL1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED1															PWDN
R															R/W
0h															0h

Access Types Legend

Table 4-1470. CRC_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED1	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
0	PWDN	R/W	0h	Power Down. When set, MCRC moduleMCRC Module is put in power down mode. 0 = MCRC is not in power down mode 1 = MCRC is in power down mode Reset Source: mcrc_rst_mod_g_rst_n

4.14.3 MEM_CRC_CTRL2 Registers

4.14.3.1 MEM_CTRL2 Register (Offset = 10h) [reset = 0h]

Short Description: Contains channel mode, da

Long Description: Contains channel mode, data trace enable control bits

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Table 4-1471. Instance Table

Instance Name	Physical Address
MCRC0	3500 0010h

Figure 4-653. CRC_CTRL2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED5						NU14		RESERVED4						NU13	
R						R		R						R	
0h						0h		0h						0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED3						CH2_MODE		RESERVED2			CH1_TRACEEN	RESERVED1		CH1_MODE	
R						R/W		R			R/W	R		R/W	
0h						0h		0h			0h	0h		0h	

Access Types Legend

Table 4-1472. CRC_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED5	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
25:24	NU14	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
23:18	RESERVED4	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
17:16	NU13	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
15:10	RESERVED3	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
9:8	CH2_MODE	R/W	0h	Channel 2 Mode: 0 0 = Data Capture mode. In this mode, the PSA Signature Register does not compress data when it is written. Any data written to PSA Signature Register is simply captured by PSA Signature Register without any compression. This mode can be used to plant seed value into the PSA register 0 1 = AUTO mode 1 0 = reserved 1 1 = Full-CPU mode Reset Source: mcrc_rst_mod_g_rst_n
7:5	RESERVED2	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
4	CH1_TRACEEN	R/W	0h	Channel 1 Data Trace Enable. When set, the channel is put into data trace mode. The channel snoops on the CPU VBUSM, ITCM, DTCM buses for any read transaction. Any read data on these buses is compressed by the PSA Signature Register. When suspend is on, the PSA Signature Register does not compress any read data on these buses. 0 = Data Trace disable 1 = Data Trace enable Reset Source: mcrc_rst_mod_g_rst_n
3:2	RESERVED1	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
1:0	CH1_MODE	R/W	0h	Channel 1 Mode: 0 0 = Data Capture mode. In this mode, the PSA Signature Register does not compress data when it is written. Any data written to PSA Signature Register is simply captured by PSA Signature Register without any compression. This mode can be used to plant seed value into the PSA register 0 1 = AUTO mode 1 0 = reserved 1 1 = Full-CPU mode Reset Source: mcrc_rst_mod_g_rst_n

4.14.4 MEM_CRC_INTS Registers

4.14.4.1 MEM_INTS Register (Offset = 18h) [reset = 0h]

Short Description: Write one to a bit to ena

Long Description: Write one to a bit to enable a interrupt

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Table 4-1473. Instance Table

Instance Name	Physical Address
MCRC0	3500 0018h

Figure 4-654. CRC_INTS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED5			NU22	NU21	NU20	NU19	RESERVED4				NU18	NU17	NU16	NU15	RESERVED3
R			R	R	R	R	R				R	R	R	R	R
0h			0h	0h	0h	0h	0h				0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED3			CH2_TIMEOUTENS	CH2_UNDERENS	CH2_OVERENS	CH2_CRCFAILENS	RESERVED2				CH1_TIMEOUTENS	CH1_UNDERENS	CH1_OVERENS	CH1_CRCFAILENS	RESERVED1
R			R/W	R/W	R/W	R/W	R				R/W	R/W	R/W	R/W	R
0h			0h	0h	0h	0h	0h				0h	0h	0h	0h	0h

Access Types Legend

Table 4-1474. CRC_INTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED5	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
28	NU22	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
27	NU21	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
26	NU20	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
25	NU19	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
24:21	RESERVED4	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
20	NU18	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
19	NU17	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
18	NU16	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
17	NU15	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
16:13	RESERVED3	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
12	CH2_TIMEOUTENS	R/W	0h	Channel 2 Timeout Interrupt Enable Bit. Writing a one to this bit enable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable Reset Source: mcrc_rst_mod_g_rst_n
11	CH2_UNDERENS	R/W	0h	Channel 2 Underrun Interrupt Enable Bit. Writing a one to this bit enable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable Reset Source: mcrc_rst_mod_g_rst_n

Table 4-1474. CRC_INTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	CH2_OVERENS	R/W	0h	Channel 2 Overrun Interrupt Enable Bit. Writing a one to this bit enable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable Reset Source: mcrc_rst_mod_g_rst_n
9	CH2_CRCFAILENS	R/W	0h	Channel 2 CRC Fail Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable Reset Source: mcrc_rst_mod_g_rst_n
8:5	RESERVED2	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
4	CH1_TIMEOUTENS	R/W	0h	Channel 1 Timeout Interrupt Enable Bit. Writing a one to this bit enable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable Reset Source: mcrc_rst_mod_g_rst_n
3	CH1_UNDERENS	R/W	0h	Channel 1 Underrun Interrupt Enable Bit. Writing a one to this bit enable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable Reset Source: mcrc_rst_mod_g_rst_n
2	CH1_OVERENS	R/W	0h	Channel 1 Overrun Interrupt Enable Bit. Writing a one to this bit enable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable Reset Source: mcrc_rst_mod_g_rst_n
1	CH1_CRCFAILENS	R/W	0h	Channel 1 CRC Fail Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable Reset Source: mcrc_rst_mod_g_rst_n
0	RESERVED1	R	0h	Reset Source: mcrc_rst_mod_g_rst_n

4.14.5 MEM_CRC_INTR Registers

4.14.5.1 MEM_INTR Register (Offset = 20h) [reset = 0h]

Short Description: Write one to a bit to dis

Long Description: Write one to a bit to disable a interrupt

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Table 4-1475. Instance Table

Instance Name	Physical Address
MCRC0	3500 0020h

Figure 4-655. CRC_INTR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED5			NU30	NU29	NU28	NU27	RESERVED4				NU26	NU25	NU24	NU23	RESERVED3
R			R	R	R	R	R				R	R	R	R	R
0h			0h	0h	0h	0h	0h				0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED3			CH2_TIMEOUTENR	CH2_UNDERENR	CH2_OVERENR	CH2_CRCFAILENR	RESERVED2				CH1_TIMEOUTENR	CH1_UNDERENR	CH1_OVERENR	CH1_CRCFAILENR	RESERVED1
R			R/W	R/W	R/W	R/W	R				R/W	R/W	R/W	R/W	R
0h			0h	0h	0h	0h	0h				0h	0h	0h	0h	0h

Access Types Legend

Table 4-1476. CRC_INTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED5	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
28	NU30	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
27	NU29	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
26	NU28	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
25	NU27	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
24:21	RESERVED4	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
20	NU26	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
19	NU25	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
18	NU24	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
17	NU23	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
16:13	RESERVED3	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
12	CH2_TIMEOUTENR	R/W	0h	Channel 2 Timeout Interrupt Disable Bit. Writing a one to this bit disable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt disable Reset Source: mcrc_rst_mod_g_rst_n
11	CH2_UNDERENR	R/W	0h	Channel 2 Underrun Interrupt Disable Bit. Writing a one to this bit disable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/dis- able]. User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt disable Reset Source: mcrc_rst_mod_g_rst_n

Table 4-1476. CRC_INTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	CH2_OVERENR	R/W	0h	Channel 2 Overrun Interrupt Disable Bit. Writing a one to this bit disable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt disable Reset Source: mcrc_rst_mod_g_rst_n
9	CH2_CRCFAILENR	R/W	0h	Channel 2 CRC Fail Interrupt Disable Bit. Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt disable Reset Source: mcrc_rst_mod_g_rst_n
8:5	RESERVED2	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
4	CH1_TIMEOUTENR	R/W	0h	Channel 1 Timeout Interrupt Disable Bit. Writing a one to this bit disable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt disable Reset Source: mcrc_rst_mod_g_rst_n
3	CH1_UNDERENR	R/W	0h	Channel 1 Underrun Interrupt Disable Bit. Writing a one to this bit disable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/dis- able]. User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt disable Reset Source: mcrc_rst_mod_g_rst_n
2	CH1_OVERENR	R/W	0h	Channel 1 Overrun Interrupt Disable Bit. Writing a one to this bit disable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt disable Reset Source: mcrc_rst_mod_g_rst_n
1	CH1_CRCFAILENR	R/W	0h	Channel 1 CRC Fail Interrupt Disable Bit. Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt disable Reset Source: mcrc_rst_mod_g_rst_n
0	RESERVED1	R	0h	Reset Source: mcrc_rst_mod_g_rst_n

4.14.6 MEM_CRC_STATUS_REG Registers

4.14.6.1 MEM_STATUS_REG Register (Offset = 28h) [reset = 0h]

Short Description: Contains interrupt flags

Long Description: Contains interrupt flags for different types of interrupt

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Table 4-1477. Instance Table

Instance Name	Physical Address
MCRC0	3500 0028h

Figure 4-656. CRC_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED5			NU38	NU37	NU36	NU35	RESERVED4				NU34	NU33	NU32	NU31	RESERVED3
R			R	R	R	R	R				R	R	R	R	R
0h			0h	0h	0h	0h	0h				0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED3			CH2_TIMEOUT	CH2_UNDER	CH2_OVER	CH2_CRCFAIL	RESERVED2				CH1_TIMEOUT	CH1_UNDER	CH1_OVER	CH1_CRCFAIL	RESERVED1
R			R/W	R/W	R/W	R/W	R				R/W	R/W	R/W	R/W	R
0h			0h	0h	0h	0h	0h				0h	0h	0h	0h	0h

Access Types Legend

Table 4-1478. CRC_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED5	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
28	NU38	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
27	NU37	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
26	NU36	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
25	NU35	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
24:21	RESERVED4	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
20	NU34	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
19	NU33	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
18	NU32	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
17	NU31	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
16:13	RESERVED3	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
12	CH2_TIMEOUT	R/W	0h	Channel 2 CRC Timeout Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode. 0 = No timeout interrupt is active 1 = Timeout interrupt is active Reset Source: mcrc_rst_mod_g_rst_n
11	CH2_UNDER	R/W	0h	Channel 2 CRC Underrun Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only 0 = No underrun interrupt is active 1 = Underrun interrupt is active Reset Source: mcrc_rst_mod_g_rst_n
10	CH2_OVER	R/W	0h	Channel 2 CRC Overrun Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode 0 = No overrun interrupt is active 1 = Overrun interrupt is active Reset Source: mcrc_rst_mod_g_rst_n

Table 4-1478. CRC_STATUS_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	CH2_CRCFAIL	R/W	0h	Channel 2 CRC Compare Fail Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only. 0 = No CRC compare fail interrupt is active 1 = CRC compare fail interrupt is active Reset Source: mcrc_rst_mod_g_rst_n
8:5	RESERVED2	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
4	CH1_TIMEOUT	R/W	0h	Channel 1 CRC Timeout Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode. 0 = No timeout interrupt is active 1 = Timeout interrupt is active Reset Source: mcrc_rst_mod_g_rst_n
3	CH1_UNDER	R/W	0h	Channel 1 CRC Underrun Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only 0 = No underrun interrupt is active 1 = Underrun interrupt is active Reset Source: mcrc_rst_mod_g_rst_n
2	CH1_OVER	R/W	0h	Channel 1 CRC Overrun Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode 0 = No overrun interrupt is active 1 = Overrun interrupt is active Reset Source: mcrc_rst_mod_g_rst_n
1	CH1_CRCFAIL	R/W	0h	Channel 1 CRC Compare Fail Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only. 0 = No CRC compare fail interrupt is active 1 = CRC compare fail interrupt is active Reset Source: mcrc_rst_mod_g_rst_n
0	RESERVED1	R	0h	Reset Source: mcrc_rst_mod_g_rst_n

4.14.7 MEM_CRC_INT_OFFSET_REG Registers

4.14.7.1 MEM_INT_OFFSET_REG Register (Offset = 30h) [reset = 0h]

Short Description: Contains the interrupt of

Long Description: Contains the interrupt offset vector address

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Table 4-1479. Instance Table

Instance Name	Physical Address
MCRC0	3500 0030h

Figure 4-657. CRC_INT_OFFSET_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED1								OFSTREG							
R								R/W							
0h								0h							

Access Types Legend

Table 4-1480. CRC_INT_OFFSET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
7:0	OFSTREG	R/W	0h	CRC Interrupt Offset. This register indicates the highest priority pending interrupt vector address. Reading the offset register automatically clear the respective interrupt flag. Please reference Table 13. for details. Reset Source: mcrc_rst_mod_g_rst_n

4.14.8 MEM_CRC_BUSY Registers

4.14.8.1 MEM_BUSY Register (Offset = 38h) [reset = 0h]

Short Description: Contains the busy flag fo

Long Description: Contains the busy flag for each channel

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Table 4-1481. Instance Table

Instance Name	Physical Address
MCRC0	3500 0038h

Figure 4-658. CRC_BUSY Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED4							NU40	RESERVED3							NU39
R							R	R							R
0h							0h	0h							0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED2							CH2_BUSY	RESERVED1							CH1_BUSY
R							R	R							R
0h							0h	0h							0h

Access Types Legend

Table 4-1482. CRC_BUSY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED4	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
24	NU40	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
23:17	RESERVED3	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
16	NU39	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
15:9	RESERVED2	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
8	CH2_BUSY	R	0h	Ch2_BUSY. During AUTO mode, the busy flag is set when the first data pattern of the block is compressed and remains set until the the last data pattern of the block is compressed. The flag is cleared when the last data pattern of the block is compressed. Reset Source: mcrc_rst_mod_g_rst_n
7:1	RESERVED1	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
0	CH1_BUSY	R	0h	CH1_BUSY. During AUTO mode, the busy flag is set when the first data pattern of the block is compressed and remains set until the the last data pattern of the block is compressed. The flag is cleared when the last data pattern of the block is compressed. Reset Source: mcrc_rst_mod_g_rst_n

4.14.9 MEM_CRC_PCOUNT_REG1 Registers

4.14.9.1 MEM_PCOUNT_REG1 Register (Offset = 40h) [reset = 0h]

Short Description: Channel 1 preload registe

Long Description: Channel 1 preload register for the pattern count

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Table 4-1483. Instance Table

Instance Name	Physical Address
MCRC0	3500 0040h

Figure 4-659. CRC_PCOUNT_REG1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1												CRC_PAT_COUNT1			
R												R/W			
0h												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC_PAT_COUNT1															
R/W															
0h															

Access Types Legend

Table 4-1484. CRC_PCOUNT_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED1	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
19:0	CRC_PAT_COUNT1	R/W	0h	Channel 1 Pattern Counter Preload Register. This register con- tains the number of data patterns in one sector to be compressed before a CRC is performed. Reset Source: mcrc_rst_mod_g_rst_n

4.14.10 MEM_CRC_SCOUNT_REG1 Registers

4.14.10.1 MEM_SCOUNT_REG1 Register (Offset = 44h) [reset = 0h]

Short Description: Channel 1 preload registe

Long Description: Channel 1 preload register for the sector count

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Table 4-1485. Instance Table

Instance Name	Physical Address
MCRC0	3500 0044h

Figure 4-660. CRC_SCOUNT_REG1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC_SEC_COUNT1															
R/W															
0h															

Access Types Legend

Table 4-1486. CRC_SCOUNT_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED1	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
15:0	CRC_SEC_COUNT1	R/W	0h	Channel 1 Sector Counter Preload Register. This register con- tains the number of sectors in one block of memory. Reset Source: mcrc_rst_mod_g_rst_n

4.14.11 MEM_CRC_CURSEC_REG1 Registers

4.14.11.1 MEM_CURSEC_REG1 Register (Offset = 48h) [reset = 0h]

Short Description: Channel 1 current sector

Long Description: Channel 1 current sector register contains the sector number which causes CRC failure

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Table 4-1487. Instance Table

Instance Name	Physical Address
MCRC0	3500 0048h

Figure 4-661. CRC_CURSEC_REG1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC_CURSEC1															
R/W															
0h															

Access Types Legend

Table 4-1488. CRC_CURSEC_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED1	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
15:0	CRC_CURSEC1	R/W	0h	Channel 1 Current Sector ID Register. In AUTO mode, this register contains the current sector number of which the signature verification fails. The sector counter is a free running up counter. When a sector fails, the erroneous sector number is logged into current sector ID register and the CRC fail interrupt is generated The sector ID register is frozen until it is read and the CRC fail status bit is cleared by CPU. While it is frozen, it does not capture another erroneous sector number. When this condition happens, an overrun interrupt is generated instead. Once the register is read and the CRC fail interrupt flag is cleared it can capture new erro- neous sector number. Reset Source: mcrc_rst_mod_g_rst_n

4.14.12 MEM_CRC_WDTOPLD1 Registers

4.14.12.1 MEM_WDTOPLD1 Register (Offset = 4Ch) [reset = 0h]

Short Description: Channel 1 timeout pre-loa

Long Description: Channel 1 timeout pre-load value to check if within a given time DMA initiates a block transfer

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Table 4-1489. Instance Table

Instance Name	Physical Address
MCRC0	3500 004Ch

Figure 4-662. CRC_WDTOPLD1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1								CRC_WDTOPLD1							
R								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC_WDTOPLD1															
R/W															
0h															

Access Types Legend

Table 4-1490. CRC_WDTOPLD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED1	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
23:0	CRC_WDTOPLD1	R/W	0h	Channel 1 Watchdog Timeout Counter Preload Register. This register contains the number of clock cycles within which the DMA must transfer the next block of data patterns. Reset Source: mcrc_rst_mod_g_rst_n

4.14.13 MEM_CRC_BCTOPLD1 Registers

4.14.13.1 MEM_BCTOPLD1 Register (Offset = 50h) [reset = 0h]

Short Description: Channel 1 timeout pre-loa

Long Description: Channel 1 timeout pre-load value to check if one block of patterns are compressed with a given time

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Table 4-1491. Instance Table

Instance Name	Physical Address
MCRC0	3500 0050h

Figure 4-663. CRC_BCTOPLD1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1								CRC_BCTOPLD1							
R								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC_BCTOPLD1															
R/W															
0h															

Access Types Legend

Table 4-1492. CRC_BCTOPLD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED1	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
23:0	CRC_BCTOPLD1	R/W	0h	Channel 1 Block Complete Timeout Counter Preload Regis- ter. This register contains the number of clock cycles within which the CRC for an entire block needs to complete before a timeout interrupt is generated. Reset Source: mcrc_rst_mod_g_rst_n

4.14.14 MEM_PSA_SIGREGL1 Registers

4.14.14.1 MEM_SIGREGL1 Register (Offset = 60h) [reset = 0h]

Short Description: Channel 1 PSA signature l

Long Description: Channel 1 PSA signature low register

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Table 4-1493. Instance Table

Instance Name	Physical Address
MCRC0	3500 0060h

Figure 4-664. PSA_SIGREGL1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PSASIG1_31_0															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSASIG1_31_0															
R/W															
0h															

Access Types Legend

Table 4-1494. PSA_SIGREGL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASIG1_31_0	R/W	0h	Channel 1 PSA Signature Low Register. This register contains the value stored at PSASIG1[31:0] register. Reset Source: mcrc_rst_mod_g_rst_n

4.14.15 MEM_PSA_SIGREGH1 Registers

4.14.15.1 MEM_SIGREGH1 Register (Offset = 64h) [reset = 0h]

Short Description: Channel 1 PSA signature h

Long Description: Channel 1 PSA signature high register

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Table 4-1495. Instance Table

Instance Name	Physical Address
MCRC0	3500 0064h

Figure 4-665. PSA_SIGREGH1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PSA_SIG1_63_32															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSA_SIG1_63_32															
R/W															
0h															

Access Types Legend

Table 4-1496. PSA_SIGREGH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSA_SIG1_63_32	R/W	0h	Channel 1 PSA Signature High Register. This register contains the value stored at PSASIG1[63:32] register. Reset Source: mcrc_rst_mod_g_rst_n

4.14.16 MEM_CRC_REGL1 Registers

4.14.16.1 MEM_REGL1 Register (Offset = 68h) [reset = 0h]

Short Description: Channel 1 CRC value low r

Long Description: Channel 1 CRC value low register

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Table 4-1497. Instance Table

Instance Name	Physical Address
MCRC0	3500 0068h

Figure 4-666. CRC_REGL1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CRC1_31_0															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC1_31_0															
R/W															
0h															

Access Types Legend

Table 4-1498. CRC_REGL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC1_31_0	R/W	0h	Channel 1 CRC Value Low Register. This register contains the current known good signature value stored at CRC1[31:0] regis- ter. Reset Source: mcrc_rst_mod_g_rst_n

4.14.17 MEM_CRC_REGH1 Registers

4.14.17.1 MEM_REGH1 Register (Offset = 6Ch) [reset = 0h]

Short Description: Channel 1 CRC value high

Long Description: Channel 1 CRC value high register

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Table 4-1499. Instance Table

Instance Name	Physical Address
MCRC0	3500 006Ch

Figure 4-667. CRC_REGH1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CRC1_63_32															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC1_63_32															
R/W															
0h															

Access Types Legend

Table 4-1500. CRC_REGH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC1_63_32	R/W	0h	Channel 1 CRC Value High Register. This register contains the current known good signature value stored at CRC1[63:32] register. Reset Source: mcrc_rst_mod_g_rst_n

4.14.18 MEM_PSA_SECSIGREGL1 Registers

4.14.18.1 MEM_SECSIGREGL1 Register (Offset = 70h) [reset = 0h]

Short Description: Channel 1 PSA sector sign

Long Description: Channel 1 PSA sector signature low regis-ter

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Table 4-1501. Instance Table

Instance Name	Physical Address
MCRC0	3500 0070h

Figure 4-668. PSA_SECSIGREGL1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PSASECSIG1_31_0															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSASECSIG1_31_0															
R															
0h															

Access Types Legend

Table 4-1502. PSA_SECSIGREGL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG1_31_0	R	0h	Channel 1 PSA Sector Signature Low Register. This register contains the value stored at PSASECSIG1[31:0] register. Reset Source: mcrc_rst_mod_g_rst_n

4.14.19 MEM_PSA_SECSIGREGH1 Registers

4.14.19.1 MEM_SECSIGREGH1 Register (Offset = 74h) [reset = 0h]

Short Description: Channel 1 PSA sector sign

Long Description: Channel 1 PSA sector signature high regis-ter

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Table 4-1503. Instance Table

Instance Name	Physical Address
MCRC0	3500 0074h

Figure 4-669. PSA_SECSIGREGH1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PSASECSIG1_63_32															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSASECSIG1_63_32															
R															
0h															

Access Types Legend

Table 4-1504. PSA_SECSIGREGH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG1_63_32	R	0h	Channel 1 PSA Sector Signature High Register. This register contains the value stored at PSASECSIG1[63:32] register. Reset Source: mcrc_rst_mod_g_rst_n

4.14.20 MEM_RAW_DATAREGL1 Registers

4.14.20.1 MEM_DATAREGL1 Register (Offset = 78h) [reset = 0h]

Short Description: Channel 1 un-compressed r

Long Description: Channel 1 un-compressed raw data low register

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Table 4-1505. Instance Table

Instance Name	Physical Address
MCRC0	3500 0078h

Figure 4-670. RAW_DATAREGL1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RAW_DATA1_31_0															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAW_DATA1_31_0															
R															
0h															

Access Types Legend

Table 4-1506. RAW_DATAREGL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA1_31_0	R	0h	Channel 1 Raw Data Low Register. This register contains bit 31:0 of the un-compressed raw data. Reset Source: mcrc_rst_mod_g_rst_n

4.14.21 MEM_RAW_DATAREGH1 Registers

4.14.21.1 MEM_DATAREGH1 Register (Offset = 7Ch) [reset = 0h]

Short Description: Channel 1 un-compressed r

Long Description: Channel 1 un-compressed raw data high register

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Table 4-1507. Instance Table

Instance Name	Physical Address
MCRC0	3500 007Ch

Figure 4-671. RAW_DATAREGH1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RAW_DATA1_63_32															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAW_DATA1_63_32															
R															
0h															

Access Types Legend

Table 4-1508. RAW_DATAREGH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA1_63_32	R	0h	Channel 1 Raw Data High Register. This register contains bit 63:32 of the un-compressed raw data. Reset Source: mcrc_rst_mod_g_rst_n

4.14.22 MEM_CRC_PCOUNT_REG2 Registers

4.14.22.1 MEM_PCOUNT_REG2 Register (Offset = 80h) [reset = 0h]

Short Description: Channel 2 preload registe

Long Description: Channel 2 preload register for the pattern count

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Table 4-1509. Instance Table

Instance Name	Physical Address
MCRC0	3500 0080h

Figure 4-672. CRC_PCOUNT_REG2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1												CRC_PAT_COUNT2			
R												R/W			
0h												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC_PAT_COUNT2															
R/W															
0h															

Access Types Legend

Table 4-1510. CRC_PCOUNT_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED1	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
19:0	CRC_PAT_COUNT2	R/W	0h	Channel 2 Pattern Counter Preload Register. This register con- tains the number of data patterns in one sector to be compressed before a CRC is performed. Reset Source: mcrc_rst_mod_g_rst_n

4.14.23 MEM_CRC_SCOUNT_REG2 Registers

4.14.23.1 MEM_SCOUNT_REG2 Register (Offset = 84h) [reset = 0h]

Short Description: Channel 2 preload registe

Long Description: Channel 2 preload register for the sector count

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Table 4-1511. Instance Table

Instance Name	Physical Address
MCRC0	3500 0084h

Figure 4-673. CRC_SCOUNT_REG2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC_SEC_COUNT2															
R/W															
0h															

Access Types Legend

Table 4-1512. CRC_SCOUNT_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED1	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
15:0	CRC_SEC_COUNT2	R/W	0h	Channel 2 Sector Counter Preload Register. This register con- tains the number of sectors in one block of memory. Reset Source: mcrc_rst_mod_g_rst_n

4.14.24 MEM_CRC_CURSEC_REG2 Registers

4.14.24.1 MEM_CURSEC_REG2 Register (Offset = 88h) [reset = 0h]

Short Description: Channel 2 current sector

Long Description: Channel 2 current sector register contains the sector number which causes CRC fail-ure

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Table 4-1513. Instance Table

Instance Name	Physical Address
MCRC0	3500 0088h

Figure 4-674. CRC_CURSEC_REG2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC_CURSEC2															
R/W															
0h															

Access Types Legend

Table 4-1514. CRC_CURSEC_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED1	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
15:0	CRC_CURSEC2	R/W	0h	Channel 2 Current Sector ID Register. In AUTO mode, this register contains the current sector number of which the signature verification fails. The sector counter is a free running up counter. When a sector fails, the erroneous sector number is logged into current sector ID register and the CRC fail interrupt is generated The sector ID register is frozen until it is read and the CRC fail status bit is cleared by CPU. While it is frozen, it does not capture another erroneous sector number. When this condition happens, an overrun interrupt is generated instead. Once the register is read and the CRC fail interrupt flag is cleared it can capture new erro- neous sector number. Reset Source: mcrc_rst_mod_g_rst_n

4.14.25 MEM_CRC_WDTOPLD2 Registers

4.14.25.1 MEM_WDTOPLD2 Register (Offset = 8Ch) [reset = 0h]

Short Description: Channel 2 timeout pre-loa

Long Description: Channel 2 timeout pre-load value to check if within a given time DMA initiates a block transfer

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Table 4-1515. Instance Table

Instance Name	Physical Address
MCRC0	3500 008Ch

Figure 4-675. CRC_WDTOPLD2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1								CRC_WDTOPLD2							
R								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC_WDTOPLD2															
R/W															
0h															

Access Types Legend

Table 4-1516. CRC_WDTOPLD2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED1	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
23:0	CRC_WDTOPLD2	R/W	0h	Channel 2 Watchdog Timeout Counter Preload Register. This register contains the number of clock cycles within which the DMA must transfer the next block of data patterns. Reset Source: mcrc_rst_mod_g_rst_n

4.14.26 MEM_CRC_BCTOPLD2 Registers

4.14.26.1 MEM_BCTOPLD2 Register (Offset = 90h) [reset = 0h]

Short Description: Channel 2 timeout pre-loa

Long Description: Channel 2 timeout pre-load value to check if one block of patterns are compressed with a given time

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Table 4-1517. Instance Table

Instance Name	Physical Address
MCRC0	3500 0090h

Figure 4-676. CRC_BCTOPLD2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1								CRC_BCTOPLD2							
R								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC_BCTOPLD2															
R/W															
0h															

Access Types Legend

Table 4-1518. CRC_BCTOPLD2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED1	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
23:0	CRC_BCTOPLD2	R/W	0h	Channel 2 Block Complete Timeout Counter Preload Regis- ter. This register contains the number of clock cycles within which the CRC for an entire block needs to complete before a timeout interrupt is generated. Reset Source: mcrc_rst_mod_g_rst_n

4.14.27 MEM_PSA_SIGREGL2 Registers

4.14.27.1 MEM_SIGREGL2 Register (Offset = A0h) [reset = 0h]

Short Description: Channel 2 PSA signature l

Long Description: Channel 2 PSA signature low register

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Table 4-1519. Instance Table

Instance Name	Physical Address
MCRC0	3500 00A0h

Figure 4-677. PSA_SIGREGL2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PSASIG2_31_0															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSASIG2_31_0															
R/W															
0h															

Access Types Legend

Table 4-1520. PSA_SIGREGL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASIG2_31_0	R/W	0h	Channel 2 PSA Signature Low Register. This register contains the value stored at PSASIG2[31:0] register. Reset Source: mcrc_rst_mod_g_rst_n

4.14.28 MEM_PSA_SIGREGH2 Registers

4.14.28.1 MEM_SIGREGH2 Register (Offset = A4h) [reset = 0h]

Short Description: Channel 2 PSA signature h

Long Description: Channel 2 PSA signature high register

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Table 4-1521. Instance Table

Instance Name	Physical Address
MCRC0	3500 00A4h

Figure 4-678. PSA_SIGREGH2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PSA_SIG2_63_32															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSA_SIG2_63_32															
R/W															
0h															

Access Types Legend

Table 4-1522. PSA_SIGREGH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSA_SIG2_63_32	R/W	0h	Channel 2 PSA Signature High Register. This register contains the value stored at PSASIG2[63:32] register. Reset Source: mcrc_rst_mod_g_rst_n

4.14.29 MEM_CRC_REGL2 Registers

4.14.29.1 MEM_REGL2 Register (Offset = A8h) [reset = 0h]

Short Description: Channel 2 CRC value low r

Long Description: Channel 2 CRC value low register

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Table 4-1523. Instance Table

Instance Name	Physical Address
MCRC0	3500 00A8h

Figure 4-679. CRC_REGL2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CRC2_31_0															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC2_31_0															
R/W															
0h															

Access Types Legend

Table 4-1524. CRC_REGL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC2_31_0	R/W	0h	Channel 2 CRC Value Low Register. This register contains the current known good signature value stored at CRC2[31:0] regis- ter. Reset Source: mcrc_rst_mod_g_rst_n

4.14.30 MEM_CRC_REGH2 Registers

4.14.30.1 MEM_REGH2 Register (Offset = ACh) [reset = 0h]

Short Description: Channel 2 CRC value high

Long Description: Channel 2 CRC value high register

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Table 4-1525. Instance Table

Instance Name	Physical Address
MCRC0	3500 00ACh

Figure 4-680. CRC_REGH2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CRC2_63_32															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC2_63_32															
R/W															
0h															

Access Types Legend

Table 4-1526. CRC_REGH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC2_63_32	R/W	0h	Channel 2 CRC Value High Register. This register contains the current known good signature value stored at CRC2[63:32] register. Reset Source: mcrc_rst_mod_g_rst_n

4.14.31 MEM_PSA_SECSIGREGL2 Registers

4.14.31.1 MEM_SECSIGREGL2 Register (Offset = B0h) [reset = 0h]

Short Description: Channel 2 PSA sector sign

Long Description: Channel 2 PSA sector signature low regis-ter

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Table 4-1527. Instance Table

Instance Name	Physical Address
MCRC0	3500 00B0h

Figure 4-681. PSA_SECSIGREGL2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PSASECSIG2_31_0															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSASECSIG2_31_0															
R															
0h															

Access Types Legend

Table 4-1528. PSA_SECSIGREGL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG2_31_0	R	0h	Channel 2 PSA Sector Signature Low Register. This register contains the value stored at PSASECSIG2[31:0] register. Reset Source: mcrc_rst_mod_g_rst_n

4.14.32 MEM_PSA_SECSIGREGH2 Registers

4.14.32.1 MEM_SECSIGREGH2 Register (Offset = B4h) [reset = 0h]

Short Description: Channel 2 PSA sector sign

Long Description: Channel 2 PSA sector signature high regis-ter

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Table 4-1529. Instance Table

Instance Name	Physical Address
MCRC0	3500 00B4h

Figure 4-682. PSA_SECSIGREGH2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PSASECSIG2_63_32															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSASECSIG2_63_32															
R															
0h															

Access Types Legend

Table 4-1530. PSA_SECSIGREGH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG2_63_32	R	0h	Channel 2 PSA Sector Signature High Register. This register contains the value stored at PSASECSIG2[63:32] register. Reset Source: mcrc_rst_mod_g_rst_n

4.14.33 MEM_RAW_DATAREGL2 Registers

4.14.33.1 MEM_DATAREGL2 Register (Offset = B8h) [reset = 0h]

Short Description: Channel 2 un-compressed r

Long Description: Channel 2 un-compressed raw data low register

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Table 4-1531. Instance Table

Instance Name	Physical Address
MCRC0	3500 00B8h

Figure 4-683. RAW_DATAREGL2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RAW_DATA2_31_0															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAW_DATA2_31_0															
R															
0h															

Access Types Legend

Table 4-1532. RAW_DATAREGL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA2_31_0	R	0h	Channel 2 Raw Data Low Register. This register contains bit 31:0 of the un-compressed raw data. Reset Source: mcrc_rst_mod_g_rst_n

4.14.34 MEM_RAW_DATAREGH2 Registers

4.14.34.1 MEM_DATAREGH2 Register (Offset = BCh) [reset = 0h]

Short Description: Channel 2 un-compressed r

Long Description: Channel 2 un-compressed raw data high Register

Return to Summary Table

Table 4-1533. Instance Table

Instance Name	Physical Address
MCRC0	3500 00BCh

Figure 4-684. RAW_DATAREGH2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RAW_DATA2_63_32															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAW_DATA2_63_32															
R															
0h															

Access Types Legend

Table 4-1534. RAW_DATAREGH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA2_63_32	R	0h	Channel 2 Raw Data High Register. This register contains bit 63:32 of the un-compressed raw data. Reset Source: mcrc_rst_mod_g_rst_n

4.14.35 MEM_CRC_PCOUNT_REG3 Registers

4.14.35.1 MEM_PCOUNT_REG3 Register (Offset = C0h) [reset = 0h]

Short Description: Channel 3 preload registe

Long Description: Channel 3 preload register for the pattern count

Return to Summary Table

Table 4-1535. Instance Table

Instance Name	Physical Address
MCRC0	3500 00C0h

Figure 4-685. CRC_PCOUNT_REG3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1												NU41			
R												R			
0h												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU41															
R															
0h															

Access Types Legend

Table 4-1536. CRC_PCOUNT_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED1	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
19:0	NU41	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n

4.14.36 MEM_CRC_SCOUNT_REG3 Registers

4.14.36.1 MEM_SCOUNT_REG3 Register (Offset = C4h) [reset = 0h]

Short Description: Channel 3 preload registe

Long Description: Channel 3 preload register for the sector count

Return to Summary Table

Table 4-1537. Instance Table

Instance Name	Physical Address
MCRC0	3500 00C4h

Figure 4-686. CRC_SCOUNT_REG3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU42															
R															
0h															

Access Types Legend

Table 4-1538. CRC_SCOUNT_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED1	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
15:0	NU42	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n

4.14.37 MEM_CRC_CURSEC_REG3 Registers

4.14.37.1 MEM_CURSEC_REG3 Register (Offset = C8h) [reset = 0h]

Short Description: Channel 3 current sector

Long Description: Channel 3 current sector register contains the sector number which causes CRC fail-ure

Return to Summary Table

Table 4-1539. Instance Table

Instance Name	Physical Address
MCRC0	3500 00C8h

Figure 4-687. CRC_CURSEC_REG3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU43															
R															
0h															

Access Types Legend

Table 4-1540. CRC_CURSEC_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED1	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
15:0	NU43	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n

4.14.38 MEM_CRC_WDTOPLD3 Registers

4.14.38.1 MEM_WDTOPLD3 Register (Offset = CCh) [reset = 0h]

Short Description: Channel 3 timeout pre-loa

Long Description: Channel 3 timeout pre-load value to check if within a given time DMA initiates a block transfer

Return to Summary Table

Table 4-1541. Instance Table

Instance Name	Physical Address
MCRC0	3500 00CCh

Figure 4-688. CRC_WDTOPLD3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1								NU44							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU44															
R															
0h															

Access Types Legend

Table 4-1542. CRC_WDTOPLD3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED1	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
23:0	NU44	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n

4.14.39 MEM_CRC_BCTOPLD3 Registers

4.14.39.1 MEM_BCTOPLD3 Register (Offset = D0h) [reset = 0h]

Short Description: Channel 3 timeout pre-loa

Long Description: Channel 3 timeout pre-load value to check if one block of patterns are compressed with a given time

Return to Summary Table

Table 4-1543. Instance Table

Instance Name	Physical Address
MCRC0	3500 00D0h

Figure 4-689. CRC_BCTOPLD3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1								NU45							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU45															
R															
0h															

Access Types Legend

Table 4-1544. CRC_BCTOPLD3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED1	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
23:0	NU45	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n

4.14.40 MEM_PSA_SIGREGL3 Registers

4.14.40.1 MEM_SIGREGL3 Register (Offset = E0h) [reset = 0h]

Short Description: Channel 3 PSA signature l

Long Description: Channel 3 PSA signature low register

Return to Summary Table

Table 4-1545. Instance Table

Instance Name	Physical Address
MCRC0	3500 00E0h

Figure 4-690. PSA_SIGREGL3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU46															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU46															
R															
0h															

Access Types Legend

Table 4-1546. PSA_SIGREGL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NU46	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n

4.14.41 MEM_PSA_SIGREGH3 Registers

4.14.41.1 MEM_SIGREGH3 Register (Offset = E4h) [reset = 0h]

Short Description: Channel 3 PSA signature h

Long Description: Channel 3 PSA signature high register

Return to Summary Table

Table 4-1547. Instance Table

Instance Name	Physical Address
MCRC0	3500 00E4h

Figure 4-691. PSA_SIGREGH3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU47															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU47															
R															
0h															

Access Types Legend

Table 4-1548. PSA_SIGREGH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NU47	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n

4.14.42 MEM_CRC_REGL3 Registers

4.14.42.1 MEM_REGL3 Register (Offset = E8h) [reset = 0h]

Short Description: Channel 3 CRC value low r

Long Description: Channel 3 CRC value low register

Return to Summary Table

Table 4-1549. Instance Table

Instance Name	Physical Address
MCRC0	3500 00E8h

Figure 4-692. CRC_REGL3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU48															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU48															
R															
0h															

Access Types Legend

Table 4-1550. CRC_REGL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NU48	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n

4.14.43 MEM_CRC_REGH3 Registers

4.14.43.1 MEM_REGH3 Register (Offset = ECh) [reset = 0h]

Short Description: Channel 3 CRC value high

Long Description: Channel 3 CRC value high register

Return to Summary Table

Table 4-1551. Instance Table

Instance Name	Physical Address
MCRC0	3500 00ECh

Figure 4-693. CRC_REGH3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU49															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU49															
R															
0h															

Access Types Legend

Table 4-1552. CRC_REGH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NU49	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n

4.14.44 MEM_PSA_SECSIGREGL3 Registers

4.14.44.1 MEM_SECSIGREGL3 Register (Offset = F0h) [reset = 0h]

Short Description: Channel 3 PSA sector sign

Long Description: Channel 3 PSA sector signature low regis-ter

Return to Summary Table

Table 4-1553. Instance Table

Instance Name	Physical Address
MCRC0	3500 00F0h

Figure 4-694. PSA_SECSIGREGL3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU50															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU50															
R															
0h															

Access Types Legend

Table 4-1554. PSA_SECSIGREGL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NU50	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n

4.14.45 MEM_PSA_SECSIGREGH3 Registers

4.14.45.1 MEM_SECSIGREGH3 Register (Offset = F4h) [reset = 0h]

Short Description: Channel 3 PSA sector sign

Long Description: Channel 3 PSA sector signature high regis-ter

Return to Summary Table

Table 4-1555. Instance Table

Instance Name	Physical Address
MCRC0	3500 00F4h

Figure 4-695. PSA_SECSIGREGH3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU51															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU51															
R															
0h															

Access Types Legend

Table 4-1556. PSA_SECSIGREGH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NU51	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n

4.14.46 MEM_RAW_DATAREGL3 Registers

4.14.46.1 MEM_DATAREGL3 Register (Offset = F8h) [reset = 0h]

Short Description: Channel 3 un-compressed r

Long Description: Channel 3 un-compressed raw data low register

Return to Summary Table

Table 4-1557. Instance Table

Instance Name	Physical Address
MCRC0	3500 00F8h

Figure 4-696. RAW_DATAREGL3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU52															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU52															
R															
0h															

Access Types Legend

Table 4-1558. RAW_DATAREGL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NU52	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n

4.14.47 MEM_RAW_DATAREGH3 Registers

4.14.47.1 MEM_DATAREGH3 Register (Offset = FCh) [reset = 0h]

Short Description: Channel 3 un-compressed r

Long Description: Channel 3 un-compressed raw data high Register

Return to Summary Table

Table 4-1559. Instance Table

Instance Name	Physical Address
MCRC0	3500 00FCh

Figure 4-697. RAW_DATAREGH3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU53															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU53															
R															
0h															

Access Types Legend

Table 4-1560. RAW_DATAREGH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NU53	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n

4.14.48 MEM_CRC_PCOUNT_REG4 Registers

4.14.48.1 MEM_PCOUNT_REG4 Register (Offset = 100h) [reset = 0h]

Short Description: Channel 4 preload registe

Long Description: Channel 4 preload register for the pattern count

Return to Summary Table

Table 4-1561. Instance Table

Instance Name	Physical Address
MCRC0	3500 0100h

Figure 4-698. CRC_PCOUNT_REG4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1												NU54			
R												R			
0h												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU54															
R															
0h															

Access Types Legend

Table 4-1562. CRC_PCOUNT_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED1	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
19:0	NU54	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n

4.14.49 MEM_CRC_SCOUNT_REG4 Registers

4.14.49.1 MEM_SCOUNT_REG4 Register (Offset = 104h) [reset = 0h]

Short Description: Channel 4 preload registe

Long Description: Channel 4 preload register for the sector count

Return to Summary Table

Table 4-1563. Instance Table

Instance Name	Physical Address
MCRC0	3500 0104h

Figure 4-699. CRC_SCOUNT_REG4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU55															
R															
0h															

Access Types Legend

Table 4-1564. CRC_SCOUNT_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED1	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
15:0	NU55	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n

4.14.50 MEM_CRC_CURSEC_REG4 Registers

4.14.50.1 MEM_CURSEC_REG4 Register (Offset = 108h) [reset = 0h]

Short Description: Channel 4 current sector

Long Description: Channel 4 current sector register contains the sector number which causes CRC fail-ure

Return to Summary Table

Table 4-1565. Instance Table

Instance Name	Physical Address
MCRC0	3500 0108h

Figure 4-700. CRC_CURSEC_REG4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU56															
R															
0h															

Access Types Legend

Table 4-1566. CRC_CURSEC_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED1	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
15:0	NU56	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n

4.14.51 MEM_CRC_WDTOPLD4 Registers

4.14.51.1 MEM_WDTOPLD4 Register (Offset = 10Ch) [reset = 0h]

Short Description: Channel 4 timeout pre-loa

Long Description: Channel 4 timeout pre-load value to check if within a given time DMA initiates a block transfer

Return to Summary Table

Table 4-1567. Instance Table

Instance Name	Physical Address
MCRC0	3500 010Ch

Figure 4-701. CRC_WDTOPLD4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1								NU57							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU57															
R															
0h															

Access Types Legend

Table 4-1568. CRC_WDTOPLD4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED1	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
23:0	NU57	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n

4.14.52 MEM_CRC_BCTOPLD4 Registers

4.14.52.1 MEM_BCTOPLD4 Register (Offset = 110h) [reset = 0h]

Short Description: Channel 4 timeout pre-loa

Long Description: Channel 4 timeout pre-load value to check if one block of patterns are compressed with a given time

Return to Summary Table

Table 4-1569. Instance Table

Instance Name	Physical Address
MCRC0	3500 0110h

Figure 4-702. CRC_BCTOPLD4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1								NU58							
R								R							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU58															
R															
0h															

Access Types Legend

Table 4-1570. CRC_BCTOPLD4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED1	R	0h	Reset Source: mcrc_rst_mod_g_rst_n
23:0	NU58	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n

4.14.53 MEM_PSA_SIGREGL4 Registers

4.14.53.1 MEM_SIGREGL4 Register (Offset = 120h) [reset = 0h]

Short Description: Channel 4 PSA signature l

Long Description: Channel 4 PSA signature low register

Return to Summary Table

Table 4-1571. Instance Table

Instance Name	Physical Address
MCRC0	3500 0120h

Figure 4-703. PSA_SIGREGL4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU59															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU59															
R															
0h															

Access Types Legend

Table 4-1572. PSA_SIGREGL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NU59	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n

4.14.54 MEM_PSA_SIGREGH4 Registers

4.14.54.1 MEM_SIGREGH4 Register (Offset = 124h) [reset = 0h]

Short Description: Channel 4 PSA signature h

Long Description: Channel 4 PSA signature high register

Return to Summary Table

Table 4-1573. Instance Table

Instance Name	Physical Address
MCRC0	3500 0124h

Figure 4-704. PSA_SIGREGH4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU60															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU60															
R															
0h															

Access Types Legend

Table 4-1574. PSA_SIGREGH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NU60	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n

4.14.55 MEM_CRC_REGL4 Registers

4.14.55.1 MEM_REGL4 Register (Offset = 128h) [reset = 0h]

Short Description: Channel 4 CRC value low r

Long Description: Channel 4 CRC value low register

Return to Summary Table

Table 4-1575. Instance Table

Instance Name	Physical Address
MCRC0	3500 0128h

Figure 4-705. CRC_REGL4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU61															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU61															
R															
0h															

Access Types Legend

Table 4-1576. CRC_REGL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NU61	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n

4.14.56 MEM_CRC_REGH4 Registers

4.14.56.1 MEM_REGH4 Register (Offset = 12Ch) [reset = 0h]

Short Description: Channel 4 CRC value high

Long Description: Channel 4 CRC value high register

Return to Summary Table

Table 4-1577. Instance Table

Instance Name	Physical Address
MCRC0	3500 012Ch

Figure 4-706. CRC_REGH4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU62															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU62															
R															
0h															

Access Types Legend

Table 4-1578. CRC_REGH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NU62	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n

4.14.57 MEM_PSA_SECSIGREGL4 Registers

4.14.57.1 MEM_SECSIGREGL4 Register (Offset = 130h) [reset = 0h]

Short Description: Channel 4 PSA sector sign

Long Description: Channel 4 PSA sector signature low regis-ter

Return to Summary Table

Table 4-1579. Instance Table

Instance Name	Physical Address
MCRC0	3500 0130h

Figure 4-707. PSA_SECSIGREGL4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU63															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU63															
R															
0h															

Access Types Legend

Table 4-1580. PSA_SECSIGREGL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NU63	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n

4.14.58 MEM_PSA_SECSIGREGH4 Registers

4.14.58.1 MEM_SECSIGREGH4 Register (Offset = 134h) [reset = 0h]

Short Description: Channel 4 PSA sector sign

Long Description: Channel 4 PSA sector signature high regis-ter

Return to Summary Table

Table 4-1581. Instance Table

Instance Name	Physical Address
MCRC0	3500 0134h

Figure 4-708. PSA_SECSIGREGH4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU64															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU64															
R															
0h															

Access Types Legend

Table 4-1582. PSA_SECSIGREGH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NU64	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n

4.14.59 MEM_RAW_DATAREGL4 Registers

4.14.59.1 MEM_DATAREGL4 Register (Offset = 138h) [reset = 0h]

Short Description: Channel 4 un-compressed r

Long Description: Channel 4 un-compressed raw data low register

Return to Summary Table

Table 4-1583. Instance Table

Instance Name	Physical Address
MCRC0	3500 0138h

Figure 4-709. RAW_DATAREGL4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU65															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU65															
R															
0h															

Access Types Legend

Table 4-1584. RAW_DATAREGL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NU65	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n

4.14.60 MEM_RAW_DATAREGH4 Registers

4.14.60.1 MEM_DATAREGH4 Register (Offset = 13Ch) [reset = 0h]

Short Description: Channel 4 un-compressed r

Long Description: Channel 4 un-compressed raw data high Register

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Table 4-1585. Instance Table

Instance Name	Physical Address
MCRC0	3500 013Ch

Figure 4-710. RAW_DATAREGH4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU66															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU66															
R															
0h															

Access Types Legend

Table 4-1586. RAW_DATAREGH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NU66	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n

4.14.61 MEM_MCRC_BUS_SEL Registers

4.14.61.1 MEM_BUS_SEL Register (Offset = 140h) [reset = 7h]

Short Description: Disables either or all tr

Long Description: Disables either or all tracing of data buses

Return to Summary Table

Table 4-1587. Instance Table

Instance Name	Physical Address
MCRC0	3500 0140h

Figure 4-711. MCRC_BUS_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU67															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU67													MEN	DTCMEN	ITCMEN
R													R/W	R/W	R/W
0h													1h	1h	1h

Access Types Legend

Table 4-1588. MCRC_BUS_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	NU67	R	0h	Reserved Reset Source: mcrc_rst_mod_g_rst_n
2	MEN	R/W	1h	MEn. Enable/disables the tracing of VBUSM 0: Tracing of VBUSM master bus has been disabled 1: Tracing of VBUSM master bus has been enabled Reset Source: mcrc_rst_mod_g_rst_n
1	DTCMEN	R/W	1h	DTCMEn. Enable/disables the tracing of data TCM 0: Tracing of DTCM_ODD and DTCM_EVEN buses have been disabled 1: Tracing of DTCM_ODD and DTCM_EVEN buses have been enabled Reset Source: mcrc_rst_mod_g_rst_n
0	ITCMEN	R/W	1h	ITCMEn. Enable/disables the tracing of instruction TCM 0: Tracing of ITCM bus has been disabled 1: Tracing of ITCM bus has been enabled Reset Source: mcrc_rst_mod_g_rst_n

4.14.62 MEM_MCRC_RESERVED Registers

4.14.62.1 MEM_RESERVED Register (Offset = 144h) [reset = 0h]

Short Description: 0x144 to 0x1FF is reserve

Long Description: 0x144 to 0x1FF is reserved area.

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Table 4-1589. Instance Table

Instance Name	Physical Address
MCRC0	3500 0144h

Figure 4-712. MCRC_RESERVED Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU68															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU68															
R															
0h															

Access Types Legend

Table 4-1590. MCRC_RESERVED Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NU68	R	0h	0x144 to 0x1FF is reserved area. Reset Source: mcrc_rst_mod_g_rst_n

4.14.63 Access Table

Table 4-1591. Access Type Codes

Access Type	Code	Description
R	R	Read
R/W	R/W	Read / Write

4.15 QSPI Registers

Table 4-1592. MEM, MEM Registers, Base Address=0X0000000048200000, Length=256

Offset	Length	Register Name	qspi0 Physical Address
0h	32	PID	4820 0000h
4h	32	MSS_QSPI_Reserved1	4820 0004h
8h	32	MSS_QSPI_Reserved2	4820 0008h
Ch	32	MSS_QSPI_Reserved3	4820 000Ch
10h	32	SYSCONFIG	4820 0010h
14h	32	MSS_QSPI_Reserved4	4820 0014h
18h	32	MSS_QSPI_Reserved5	4820 0018h
1Ch	32	MSS_QSPI_Reserved6	4820 001Ch
20h	32	INTR_STATUS_RAW_SET	4820 0020h
24h	32	INTR_STATUS_ENABLED_CLEAR	4820 0024h
28h	32	INTR_ENABLE_SET	4820 0028h
2Ch	32	INTR_ENABLE_CLEAR	4820 002Ch
30h	32	INTC_EOI	4820 0030h
34h	32	MSS_QSPI_Reserved7	4820 0034h
38h	32	MSS_QSPI_Reserved8	4820 0038h
3Ch	32	MSS_QSPI_Reserved9	4820 003Ch
40h	32	SPI_CLOCK_CNTRL	4820 0040h
44h	32	SPI_DC	4820 0044h
48h	32	SPI_CMD	4820 0048h
4Ch	32	SPI_STATUS	4820 004Ch
50h	32	SPI_DATA	4820 0050h
54h	32	SPI_SETUP0	4820 0054h
58h	32	SPI_SETUP1	4820 0058h
5Ch	32	SPI_SETUP2	4820 005Ch
60h	32	SPI_SETUP3	4820 0060h
64h	32	SPI_SWITCH	4820 0064h
68h	32	SPI_DATA1	4820 0068h
6Ch	32	SPI_DATA2	4820 006Ch
70h	32	SPI_DATA3	4820 0070h

4.15.1 MEM_PID Registers

4.15.1.1 MEM_PID Register (Offset = 0h) [reset = 4f400000h]

Short Description: PID

Long Description: PID

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Table 4-1593. Instance Table

Instance Name	Physical Address
QSPI0	4820 0000h

Figure 4-713. PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		RESERVED		FUNC											
R		R		R											
1h		0h		f40h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL				MAJOR				CUSTOM		MINOR					
R				R				R		R					
0h				0h				0h		0h					

Access Types Legend

Table 4-1594. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	The scheme of the register used. This indicates the PDR3.5 Method Reset Source: qspi_rst_mod_g_rst_n
29:28	RESERVED	R		Always read as 0 Reset Source: qspi_rst_mod_g_rst_n
27:16	FUNC	R	F40h	The function of the module being used Reset Source: qspi_rst_mod_g_rst_n
15:11	RTL	R	0h	RTL Release Version The PDR release number of this IP Reset Source: qspi_rst_mod_g_rst_n
10:8	MAJOR	R	0h	Major Release Number Reset Source: qspi_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom IP Reset Source: qspi_rst_mod_g_rst_n
5:0	MINOR	R	0h	Minor Release Number Reset Source: qspi_rst_mod_g_rst_n

4.15.2 MEM_MSS_QSPI_RESERVED1 Registers

4.15.2.1 MEM_QSPI_RESERVED1 Register (Offset = 4h) [reset = 0h]

Short Description: Reserved

Long Description: Reserved

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Table 4-1595. Instance Table

Instance Name	Physical Address
QSPI0	4820 0004h

Figure 4-714. MSS_QSPI_RESERVED1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1															
R															
0h															

Access Types Legend

Table 4-1596. MSS_QSPI_RESERVED1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_1	R	0h	Reserved Reset Source: qspi_rst_mod_g_rst_n

4.15.3 MEM_MSS_QSPI_RESERVED2 Registers

4.15.3.1 MEM_QSPI_RESERVED2 Register (Offset = 8h) [reset = 0h]

Short Description: Reserved

Long Description: Reserved

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Table 4-1597. Instance Table

Instance Name	Physical Address
QSPI0	4820 0008h

Figure 4-715. MSS_QSPI_RESERVED2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_2															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2															
R															
0h															

Access Types Legend

Table 4-1598. MSS_QSPI_RESERVED2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_2	R	0h	Reserved Reset Source: qspi_rst_mod_g_rst_n

4.15.4 MEM_MSS_QSPI_RESERVED3 Registers

4.15.4.1 MEM_QSPI_RESERVED3 Register (Offset = Ch) [reset = 0h]

Short Description: Reserved

Long Description: Reserved

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Table 4-1599. Instance Table

Instance Name	Physical Address
QSPI0	4820 000Ch

Figure 4-716. MSS_QSPI_RESERVED3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_3															
R															
0h															

Access Types Legend

Table 4-1600. MSS_QSPI_RESERVED3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_3	R	0h	Reserved Reset Source: qspi_rst_mod_g_rst_n

4.15.5 MEM_SYSCONFIG Registers

4.15.5.1 MEM_SYSCONFIG Register (Offset = 10h) [reset = 8h]

Short Description: SYSCONFIG

Long Description: SYSCONFIG

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Table 4-1601. Instance Table

Instance Name	Physical Address
QSPI0	4820 0010h

Figure 4-717. SYSCONFIG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED3															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED3										RESERVED2		IDLEMODE		RESERVED1	
R										R		R/W		R	
0h										0h		2h		0h	

Access Types Legend

Table 4-1602. SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED3	R	0h	Always read as 0 Reset Source: qspi_rst_mod_g_rst_n
5:4	RESERVED2	R	0h	Always read as 0 Reset Source: qspi_rst_mod_g_rst_n
3:2	IDLEMODE	R/W	2h	Configuration of the local target state management mode. By definition, target can handle read/write transaction as long as it is out of IDLE state 0x0 : Force-idle mode: local target's idle state follows [acknowledges] the system's idle requests unconditionally, i.e. regardless of the IP module's internal requirements. Backup mode, for debug only 0x1 : No-idle mode: local target never enters idle state. Backup mode, for debug only 0x2 : Smart-idle mode: local target's idle state eventually follows [acknowledges] the system's idle requests, depending on the IP module's internal requirements. IP module shall not generate [IRQ- or DMA-request-related] wakeup events 0x3 : Smart-idle wakeup-capable mode: local target's idle state eventually follows [acknowledges] the system's idle requests, depending on the IP module's internal requirements. IP module may generate [IRQ- or DMA-request-related] wakeup events when in idle state. Mode is only relevant if the appropriate IP module "swakeup" output[s] is [are] implemented Reset Source: qspi_rst_mod_g_rst_n
1:0	RESERVED1	R	0h	Always read as 0 Reset Source: qspi_rst_mod_g_rst_n

4.15.6 MEM_MSS_QSPI_RESERVED4 Registers

4.15.6.1 MEM_QSPI_RESERVED4 Register (Offset = 14h) [reset = 0h]

Short Description: Reserved

Long Description: Reserved

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Table 4-1603. Instance Table

Instance Name	Physical Address
QSPI0	4820 0014h

Figure 4-718. MSS_QSPI_RESERVED4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_4															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_4															
R															
0h															

Access Types Legend

Table 4-1604. MSS_QSPI_RESERVED4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_4	R	0h	Reserved Reset Source: qspi_rst_mod_g_rst_n

4.15.7 MEM_MSS_QSPI_RESERVED5 Registers

4.15.7.1 MEM_QSPI_RESERVED5 Register (Offset = 18h) [reset = 0h]

Short Description: Reserved

Long Description: Reserved

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Table 4-1605. Instance Table

Instance Name	Physical Address
QSPI0	4820 0018h

Figure 4-719. MSS_QSPI_RESERVED5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_5															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_5															
R															
0h															

Access Types Legend

Table 4-1606. MSS_QSPI_RESERVED5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_5	R	0h	Reserved Reset Source: qspi_rst_mod_g_rst_n

4.15.8 MEM_MSS_QSPI_RESERVED6 Registers

4.15.8.1 MEM_QSPI_RESERVED6 Register (Offset = 1Ch) [reset = 0h]

Short Description: Reserved

Long Description: Reserved

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Table 4-1607. Instance Table

Instance Name	Physical Address
QSPI0	4820 001Ch

Figure 4-720. MSS_QSPI_RESERVED6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_6															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_6															
R															
0h															

Access Types Legend

Table 4-1608. MSS_QSPI_RESERVED6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_6	R	0h	Reserved Reset Source: qspi_rst_mod_g_rst_n

4.15.9 MEM_INTR_STATUS_RAW_SET Registers

4.15.9.1 MEM_STATUS_RAW_SET Register (Offset = 20h) [reset = 0h]

Short Description: INTR Interrupt Status Raw

Long Description: INTR Interrupt Status Raw/Set Register

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Table 4-1609. Instance Table

Instance Name	Physical Address
QSPI0	4820 0020h

Figure 4-721. INTR_STATUS_RAW_SET Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														WIRQ_RAW	FIRQ_RAW
R														R/W	R/W
0h														0h	0h

Access Types Legend

Table 4-1610. INTR_STATUS_RAW_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R		Always read as 0 Reset Source: qspi_rst_mod_g_rst_n
1	WIRQ_RAW	R/W	0h	Word Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect Reset Source: qspi_rst_mod_g_rst_n
0	FIRQ_RAW	R/W	0h	Frame Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect Reset Source: qspi_rst_mod_g_rst_n

4.15.10 MEM_INTR_STATUS_ENABLED_CLEAR Registers

4.15.10.1 MEM_STATUS_ENABLED_CLEAR Register (Offset = 24h) [reset = 0h]

Short Description: INTR Interrupt Status Ena

Long Description: INTR Interrupt Status Enabled/Clear Register

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Table 4-1611. Instance Table

Instance Name	Physical Address
QSPI0	4820 0024h

Figure 4-722. INTR_STATUS_ENABLED_CLEAR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														WIRQ_ENA	FIRQ_ENA
R														R/W	R/W
0h														0h	0h

Access Types Legend

Table 4-1612. INTR_STATUS_ENABLED_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R		Always read as 0 Reset Source: qspi_rst_mod_g_rst_n
1	WIRQ_ENA	R/W	0h	Word Interrupt Enabled Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect Reset Source: qspi_rst_mod_g_rst_n
0	FIRQ_ENA	R/W	0h	Frame Interrupt Enabled Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect Reset Source: qspi_rst_mod_g_rst_n

4.15.11 MEM_INTR_ENABLE_SET Registers

4.15.11.1 MEM_ENABLE_SET Register (Offset = 28h) [reset = 0h]

Short Description: INTR Interrupt Enable/Set

Long Description: INTR Interrupt Enable/Set Register

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Table 4-1613. Instance Table

Instance Name	Physical Address
QSPI0	4820 0028h

Figure 4-723. INTR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														WIRQ_ENA_SET	FIRQ_ENA_SET
R														R/W	R/W
0h														0h	0h

Access Types Legend

Table 4-1614. INTR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R		Always read as 0 Reset Source: qspi_rst_mod_g_rst_n
1	WIRQ_ENA_SET	R/W	0h	Word Interrupt Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect Reset Source: qspi_rst_mod_g_rst_n
0	FIRQ_ENA_SET	R/W	0h	Frame Interrupt Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect Reset Source: qspi_rst_mod_g_rst_n

4.15.12 MEM_INTR_ENABLE_CLEAR Registers

4.15.12.1 MEM_ENABLE_CLEAR Register (Offset = 2Ch) [reset = 0h]

Short Description: INTR Interrupt Enable/Cle

Long Description: INTR Interrupt Enable/Clear Register

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Table 4-1615. Instance Table

Instance Name	Physical Address
QSPI0	4820 002Ch

Figure 4-724. INTR_ENABLE_CLEAR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														WIRQ_ENA_CLR	FIRQ_ENA_CLR
R														R/W	R/W
0h														0h	0h

Access Types Legend

Table 4-1616. INTR_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R		Always read as 0 Reset Source: qspi_rst_mod_g_rst_n
1	WIRQ_ENA_CLR	R/W	0h	Word Interrupt Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect Reset Source: qspi_rst_mod_g_rst_n
0	FIRQ_ENA_CLR	R/W	0h	Frame Interrupt Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect Reset Source: qspi_rst_mod_g_rst_n

4.15.13 MEM_INTC_EOI Registers

4.15.13.1 MEM_EOI Register (Offset = 30h) [reset = 0h]

Short Description: EOI Register

Long Description: EOI Register

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Table 4-1617. Instance Table

Instance Name	Physical Address
QSPI0	4820 0030h

Figure 4-725. INTC_EOI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EOI_VECTOR															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EOI_VECTOR															
R/W															
0h															

Access Types Legend

Table 4-1618. INTC_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EOI_VECTOR	R/W	0h	Number associated with the ipgenericirq for intr output. There are 1 interrupt outputs Write 0x0 : Write to intr IP Generic Any other write value is ignored. Reset Source: qspi_rst_mod_g_rst_n

4.15.14 MEM_MSS_QSPI_RESERVED7 Registers

4.15.14.1 MEM_QSPI_RESERVED7 Register (Offset = 34h) [reset = 0h]

Short Description: Reserved

Long Description: Reserved

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Table 4-1619. Instance Table

Instance Name	Physical Address
QSPI0	4820 0034h

Figure 4-726. MSS_QSPI_RESERVED7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_7															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_7															
R															
0h															

Access Types Legend

Table 4-1620. MSS_QSPI_RESERVED7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_7	R	0h	Reserved Reset Source: qspi_rst_mod_g_rst_n

4.15.15 MEM_MSS_QSPI_RESERVED8 Registers

4.15.15.1 MEM_QSPI_RESERVED8 Register (Offset = 38h) [reset = 0h]

Short Description: Reserved

Long Description: Reserved

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Table 4-1621. Instance Table

Instance Name	Physical Address
QSPI0	4820 0038h

Figure 4-727. MSS_QSPI_RESERVED8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_8															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_8															
R															
0h															

Access Types Legend

Table 4-1622. MSS_QSPI_RESERVED8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_8	R	0h	Reserved Reset Source: qspi_rst_mod_g_rst_n

4.15.16 MEM_MSS_QSPI_RESERVED9 Registers

4.15.16.1 MEM_QSPI_RESERVED9 Register (Offset = 3Ch) [reset = 0h]

Short Description: Reserved

Long Description: Reserved

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Table 4-1623. Instance Table

Instance Name	Physical Address
QSPI0	4820 003Ch

Figure 4-728. MSS_QSPI_RESERVED9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_9															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_9															
R															
0h															

Access Types Legend

Table 4-1624. MSS_QSPI_RESERVED9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED_9	R	0h	Reserved Reset Source: qspi_rst_mod_g_rst_n

4.15.17 MEM_SPI_CLOCK_CNTRL Registers

4.15.17.1 MEM_CLOCK_CNTRL Register (Offset = 40h) [reset = 0h]

Short Description: SPI Clock Control Registe

Long Description: SPI Clock Control Register (SPICC)

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Table 4-1625. Instance Table

Instance Name	Physical Address
QSPI0	4820 0040h

Figure 4-729. SPI_CLOCK_CNTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLKEN	RESERVED														
R/W	R														
0h	0h														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DCLK_DIV															
R/W															
0h															

Access Types Legend

Table 4-1626. SPI_CLOCK_CNTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CLKEN	R/W	0h	Clock Enable. 0- Data clock is turned off 1- Data clock is enabled Reset Source: qspi_rst_mod_g_rst_n
30:16	RESERVED	R		Always read as 0 Reset Source: qspi_rst_mod_g_rst_n
15:0	DCLK_DIV	R/W	0h	Serial data clock divide by ratio Reset Source: qspi_rst_mod_g_rst_n

4.15.18 MEM_SPI_DC Registers

4.15.18.1 MEM_DC Register (Offset = 44h) [reset = 0h]

Short Description: SPI Data Control Register

Long Description: SPI Data Control Register (SPIDC)

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Table 4-1627. Instance Table

Instance Name	Physical Address
QSPI0	4820 0044h

Figure 4-730. SPI_DC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED4			DD3		CKPH3	CSP3	CKP3	RESERVED3			DD2		CKPH2	CSP2	CKP2
R			R/W		R/W	R/W	R/W	R			R/W		R/W	R/W	R/W
0h			0h		0h	0h	0h	0h			0h		0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED2			DD1		CKPH1	CSP1	CKP1	RESERVED1			DD0		CKPH0	CSP0	CKP0
R			R/W		R/W	R/W	R/W	R			R/W		R/W	R/W	R/W
0h			0h		0h	0h	0h	0h			0h		0h	0h	0h

Access Types Legend

Table 4-1628. SPI_DC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED4	R	0h	Always read as 0 Reset Source: qspi_rst_mod_g_rst_n
28:27	DD3	R/W	0h	Data delay for chip select 3 00- Data is output on the same cycle as the CS_N goes active 01- Data is output 1 DCLK cycle after the CS_N goes active 10- Data is output 2 DCLK cycles after the CS_N goes active 11- Data is output 3 DCLK cycles after the CS_N goes active Reset Source: qspi_rst_mod_g_rst_n
26	CKPH3	R/W	0h	Clock phase for chip select 3 If CKP0 = 0 0- Data shifted out on falling edge; input on rising edge 1- Data shifted out on rising edge; input on falling edge If CKP0 = 1 1- Data shifted out on falling edge; input on rising edge 0- Data shifted out on rising edge; input on falling edge Reset Source: qspi_rst_mod_g_rst_n
25	CSP3	R/W	0h	Chip select polarity for chip select 3 0- Active low 1- Active high Reset Source: qspi_rst_mod_g_rst_n
24	CKP3	R/W	0h	Clock polarity for chip select 3 0- When data is not being transferred, SCK = 0 1- When data is not being transferred, SCK = 1 Reset Source: qspi_rst_mod_g_rst_n
23:21	RESERVED3	R	0h	Always read as 0 Reset Source: qspi_rst_mod_g_rst_n
20:19	DD2	R/W	0h	Data delay for chip select 2 00- Data is output on the same cycle as the CS_N goes active 01- Data is output 1 DCLK cycle after the CS_N goes active 10- Data is output 2 DCLK cycles after the CS_N goes active 11- Data is output 3 DCLK cycles after the CS_N goes active Reset Source: qspi_rst_mod_g_rst_n
18	CKPH2	R/W	0h	Clock phase for chip select 2. If CKP0 = 0 0- Data shifted out on falling edge; input on rising edge 1- Data shifted out on rising edge; input on falling edge If CKP0 = 1 1- Data shifted out on falling edge; input on rising edge 0- Data shifted out on rising edge; input on falling edge Reset Source: qspi_rst_mod_g_rst_n
17	CSP2	R/W	0h	Chip select polarity for chip select 2 0- Active low 1- Active high Reset Source: qspi_rst_mod_g_rst_n

Table 4-1628. SPI_DC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	CKP2	R/W	0h	Clock polarity for chip select 2 0- When data is not being transferred, SCK = 0 1- When data is not being transferred, SCK = 1 Reset Source: qspi_rst_mod_g_rst_n
15:13	RESERVED2	R	0h	Always read as 0 Reset Source: qspi_rst_mod_g_rst_n
12:11	DD1	R/W	0h	Data delay for chip select 1 00- Data is output on the same cycle as the CS_N goes active 01- Data is output 1 DCLK cycle after the CS_N goes active 10- Data is output 2 DCLK cycles after the CS_N goes active 11- Data is output 3 DCLK cycles after the CS_N goes active Reset Source: qspi_rst_mod_g_rst_n
10	CKPH1	R/W	0h	Clock phase for chip select 1. If CKP0 = 0 0- Data shifted out on falling edge; input on rising edge 1- Data shifted out on rising edge; input on falling edge If CKP0 = 1 1- Data shifted out on falling edge; input on rising edge 0- Data shifted out on rising edge; input on falling edge Reset Source: qspi_rst_mod_g_rst_n
9	CSP1	R/W	0h	Chip select polarity for chip select 1 0- Active low 1- Active high Reset Source: qspi_rst_mod_g_rst_n
8	CKP1	R/W	0h	Clock polarity for chip select 1 0- When data is not being transferred, SCK = 0 1- When data is not being transferred, SCK = 1 Reset Source: qspi_rst_mod_g_rst_n
7:5	RESERVED1	R	0h	Always read as 0 Reset Source: qspi_rst_mod_g_rst_n
4:3	DD0	R/W	0h	Data delay for chip select 0 00- Data is output on the same cycle as the CS_N goes active 01- Data is output 1 DCLK cycle after the CS_N goes active 10- Data is output 2 DCLK cycles after the CS_N goes active 11- Data is output 3 DCLK cycles after the CS_N goes active Reset Source: qspi_rst_mod_g_rst_n
2	CKPH0	R/W	0h	Clock phase for chip select 0. If CKP0 = 0 0- Data shifted out on falling edge; input on rising edge 1- Data shifted out on rising edge; input on falling edge If CKP0 = 1 1- Data shifted out on falling edge; input on rising edge 0- Data shifted out on rising edge; input on falling edge Reset Source: qspi_rst_mod_g_rst_n
1	CSP0	R/W	0h	Chip select polarity for chip select 0 0- Active low 1- Active high Reset Source: qspi_rst_mod_g_rst_n
0	CKP0	R/W	0h	Clock polarity for chip select 0 0- When data is not being transferred, SCK = 0 1- When data is not being transferred, SCK = 1 Reset Source: qspi_rst_mod_g_rst_n

4.15.19 MEM_SPI_CMD Registers

4.15.19.1 MEM_CMD Register (Offset = 48h) [reset = 0h]

Short Description: SPI Command Register (SPI

Long Description: SPI Command Register (SPICR)

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Table 4-1629. Instance Table

Instance Name	Physical Address
QSPI0	4820 0048h

Figure 4-731. SPI_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED3		CSNUM		RESERVED2		WLEN							CMD		
R		R/W		R		R/W							R/W		
0h		0h		0h		0h							0h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIRQ	WIRQ	RESERVED1		FLEN											
R/W	R/W	R		R/W											
0h	0h	0h		0h											

Access Types Legend

Table 4-1630. SPI_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED3	R	0h	Always read as 0 Reset Source: qspi_rst_mod_g_rst_n
29:28	CSNUM	R/W	0h	Device select. Sets the active chip select for the transfer 00- Chip Select 0 active 01- Chip Select 1 active 10- Chip Select 2 active 11- Chip Select 3 active Reset Source: qspi_rst_mod_g_rst_n
27:26	RESERVED2	R	0h	Always read as 0 Reset Source: qspi_rst_mod_g_rst_n
25:19	WLEN	R/W	0h	Word length. Sets the size of the individual transfers from 1 128 bits 0- 1 bit 1- 2 bits 127 128 bits Reset Source: qspi_rst_mod_g_rst_n
18:16	CMD	R/W	0h	Transfer command 000- Reserved 001- 4 pin Read Single 010- 4 pin Write Single 011- 4 pin Read Dual 100 Reserved 101 3 pin Read Single 110 3 pin Write Single 111 6 pin Read Quad Reset Source: qspi_rst_mod_g_rst_n
15	FIRQ	R/W	0h	Frame count interrupt enable Reset Source: qspi_rst_mod_g_rst_n
14	WIRQ	R/W	0h	Word count interrupt enable Reset Source: qspi_rst_mod_g_rst_n
13:12	RESERVED1	R	0h	Always read as 0 Reset Source: qspi_rst_mod_g_rst_n
11:0	FLEN	R/W	0h	Frame Length 0- 1 word 1- 2 words 4095 4096 words Reset Source: qspi_rst_mod_g_rst_n

4.15.20 MEM_SPI_STATUS Registers

4.15.20.1 MEM_STATUS Register (Offset = 4Ch) [reset = 0h]

Short Description: SPI Status Register (SPIS

Long Description: SPI Status Register (SPISR)

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Table 4-1631. Instance Table

Instance Name	Physical Address
QSPI0	4820 004Ch

Figure 4-732. SPI_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED2				WDCNT											
R				R											
0h				0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED1													FC	WC	BUSY
R													R	R	R
0h													0h	0h	0h

Access Types Legend

Table 4-1632. SPI_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED2	R	0h	Always read as 0 Reset Source: qspi_rst_mod_g_rst_n
27:16	WDCNT	R	0h	Word count. This field will reflect the 1-4096 words transferred Reset Source: qspi_rst_mod_g_rst_n
15:3	RESERVED1	R	0h	Always read as 0 Reset Source: qspi_rst_mod_g_rst_n
2	FC	R	0h	Frame complete. This bit is set after all of the requested words have been transmitted. 0- Transfer is not complete 1- Transfer is complete This bit is reset when the SPI Status Register is read Reset Source: qspi_rst_mod_g_rst_n
1	WC	R	0h	Word complete. This bit is set after each word transfer is completed. 0- Word transfer is not complete 1- Word transfer is complete This bit is reset when the SPI Status Register is read Reset Source: qspi_rst_mod_g_rst_n
0	BUSY	R	0h	Busy bit. Active transfer in progress. This bit is only set during an active word transfer. Between words, the bit will clear to signal that it is ok to read/write the data registers. 0- Idle 1- Busy Reset Source: qspi_rst_mod_g_rst_n

4.15.21 MEM_SPI_DATA Registers

4.15.21.1 MEM_DATA Register (Offset = 50h) [reset = 0h]

Short Description: SPI Data Register (SPIDR)

Long Description: SPI Data Register (SPIDR)

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Table 4-1633. Instance Table

Instance Name	Physical Address
QSPI0	4820 0050h

Figure 4-733. SPI_DATA Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA															
R/W															
0h															

Access Types Legend

Table 4-1634. SPI_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Data register for read and write operations Reset Source: qspi_rst_mod_g_rst_n

4.15.22 MEM_SPI_SETUP0 Registers

4.15.22.1 MEM_SETUP0 Register (Offset = 54h) [reset = 20203h]

Short Description: Memory Mapped SPI Setup0

Long Description: Memory Mapped SPI Setup0 Register

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Table 4-1635. Instance Table

Instance Name	Physical Address
QSPI0	4820 0054h

Figure 4-734. SPI_SETUP0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED2			NUM_D_BITS					WCMD							
R			R/W					R/W							
0h			0h					2h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED1		READ_TYPE		NUM_D_BYTES		NUM_A_BYTES		RCMD							
R		R/W		R/W		R/W		R/W							
0h		0h		0h		2h		3h							

Access Types Legend

Table 4-1636. SPI_SETUP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED2	R	0h	Always read as 0 Reset Source: qspi_rst_mod_g_rst_n
28:24	NUM_D_BITS	R/W	0h	Number of dummy bits to use if NUM_D_BYTES = 0 Reset Source: qspi_rst_mod_g_rst_n
23:16	WCMD	R/W	2h	Write Command Reset Source: qspi_rst_mod_g_rst_n
15:14	RESERVED1	R	0h	Always read as 0 Reset Source: qspi_rst_mod_g_rst_n
13:12	READ_TYPE	R/W	0h	Determines if the read command is a single, dual or quad read mode command 00 Normal read [all data input on spi_din] 01 Dual read [odd bytes input on spi_din; even on spi_dout] 10 Normal read [all data input on spi_din] 11 Quad read [uses spi_qdin0/1] Reset Source: qspi_rst_mod_g_rst_n
11:10	NUM_D_BYTES	R/W	0h	Number of dummy bytes to be used for fast read. 0 = use the value in NUM_D_BITS 1 = use 8 bits; 2 = use 16 bits; 3 = use 24 bits Reset Source: qspi_rst_mod_g_rst_n
9:8	NUM_A_BYTES	R/W	2h	Number of address bytes to be sent. 0 = 1 byte; 1 = 2 bytes; 2 = 3 bytes; 3 = 4 bytes Reset Source: qspi_rst_mod_g_rst_n
7:0	RCMD	R/W	3h	Read Command Reset Source: qspi_rst_mod_g_rst_n

4.15.23 MEM_SPI_SETUP1 Registers

4.15.23.1 MEM_SETUP1 Register (Offset = 58h) [reset = 20203h]

Short Description: Memory Mapped SPI Setup1

Long Description: Memory Mapped SPI Setup1 Register

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Table 4-1637. Instance Table

Instance Name	Physical Address
QSPI0	4820 0058h

Figure 4-735. SPI_SETUP1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED2			NUM_D_BITS					WCMD							
R			R/W					R/W							
0h			0h					2h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED1		READ_TYPE		NUM_D_BYTES		NUM_A_BYTES		RCMD							
R		R/W		R/W		R/W		R/W							
0h		0h		0h		2h		3h							

Access Types Legend

Table 4-1638. SPI_SETUP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED2	R	0h	Always read as 0 Reset Source: qspi_rst_mod_g_rst_n
28:24	NUM_D_BITS	R/W	0h	Number of dummy bits to use if NUM_D_BYTES = 0 Reset Source: qspi_rst_mod_g_rst_n
23:16	WCMD	R/W	2h	Write Command Reset Source: qspi_rst_mod_g_rst_n
15:14	RESERVED1	R	0h	Always read as 0 Reset Source: qspi_rst_mod_g_rst_n
13:12	READ_TYPE	R/W	0h	Determines if the read command is a single, dual or quad read mode command 00 Normal read [all data input on spi_din] 01 Dual read [odd bytes input on spi_din; even on spi_dout] 10 Normal read [all data input on spi_din] 11 Quad read [uses spi_qdin0/1] Reset Source: qspi_rst_mod_g_rst_n
11:10	NUM_D_BYTES	R/W	0h	Number of dummy bytes to be used for fast read. 0 = use the value in NUM_D_BITS 1 = use 8 bits; 2 = use 16 bits; 3 = use 24 bits Reset Source: qspi_rst_mod_g_rst_n
9:8	NUM_A_BYTES	R/W	2h	Number of address bytes to be sent. 0 = 1 byte; 1 = 2 bytes; 2 = 3 bytes; 3 = 4 bytes Reset Source: qspi_rst_mod_g_rst_n
7:0	RCMD	R/W	3h	Read Command Reset Source: qspi_rst_mod_g_rst_n

4.15.24 MEM_SPI_SETUP2 Registers

4.15.24.1 MEM_SETUP2 Register (Offset = 5Ch) [reset = 20203h]

Short Description: Memory Mapped SPI Setup2

Long Description: Memory Mapped SPI Setup2 Register

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Table 4-1639. Instance Table

Instance Name	Physical Address
QSPI0	4820 005Ch

Figure 4-736. SPI_SETUP2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED2			NUM_D_BITS					WCMD							
R			R/W					R/W							
0h			0h					2h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED1		READ_TYPE		NUM_D_BYTES		NUM_A_BYTES		RCMD							
R		R/W		R/W		R/W		R/W							
0h		0h		0h		2h		3h							

Access Types Legend

Table 4-1640. SPI_SETUP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED2	R	0h	Always read as 0 Reset Source: qspi_rst_mod_g_rst_n
28:24	NUM_D_BITS	R/W	0h	Number of dummy bits to use if NUM_D_BYTES = 0 Reset Source: qspi_rst_mod_g_rst_n
23:16	WCMD	R/W	2h	Write Command Reset Source: qspi_rst_mod_g_rst_n
15:14	RESERVED1	R	0h	Always read as 0 Reset Source: qspi_rst_mod_g_rst_n
13:12	READ_TYPE	R/W	0h	Determines if the read command is a single, dual or quad read mode command 00 Normal read [all data input on spi_din] 01 Dual read [odd bytes input on spi_din; even on spi_dout] 10 Normal read [all data input on spi_din] 11 Quad read [uses spi_qdin0/1] Reset Source: qspi_rst_mod_g_rst_n
11:10	NUM_D_BYTES	R/W	0h	Number of dummy bytes to be used for fast read. 0 = use the value in NUM_D_BITS 1 = use 8 bits; 2 = use 16 bits; 3 = use 24 bits Reset Source: qspi_rst_mod_g_rst_n
9:8	NUM_A_BYTES	R/W	2h	Number of address bytes to be sent. 0 = 1 byte; 1 = 2 bytes; 2 = 3 bytes; 3 = 4 bytes Reset Source: qspi_rst_mod_g_rst_n
7:0	RCMD	R/W	3h	Read Command Reset Source: qspi_rst_mod_g_rst_n

4.15.25 MEM_SPI_SETUP3 Registers

4.15.25.1 MEM_SETUP3 Register (Offset = 60h) [reset = 20203h]

Short Description: Memory Mapped SPI Setup3

Long Description: Memory Mapped SPI Setup3 Register

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Table 4-1641. Instance Table

Instance Name	Physical Address
QSPI0	4820 0060h

Figure 4-737. SPI_SETUP3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED2			NUM_D_BITS					WCMD							
R			R/W					R/W							
0h			0h					2h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED1		READ_TYPE		NUM_D_BYTES		NUM_A_BYTES		RCMD							
R		R/W		R/W		R/W		R/W							
0h		0h		0h		2h		3h							

Access Types Legend

Table 4-1642. SPI_SETUP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED2	R	0h	Always read as 0 Reset Source: qspi_rst_mod_g_rst_n
28:24	NUM_D_BITS	R/W	0h	Number of dummy bits to use if NUM_D_BYTES = 0 Reset Source: qspi_rst_mod_g_rst_n
23:16	WCMD	R/W	2h	Write Command Reset Source: qspi_rst_mod_g_rst_n
15:14	RESERVED1	R	0h	Always read as 0 Reset Source: qspi_rst_mod_g_rst_n
13:12	READ_TYPE	R/W	0h	Determines if the read command is a single, dual or quad read mode command 00 Normal read [all data input on spi_din] 01 Dual read [odd bytes input on spi_din; even on spi_dout] 10 Normal read [all data input on spi_din] 11 Quad read [uses spi_qdin0/1] Reset Source: qspi_rst_mod_g_rst_n
11:10	NUM_D_BYTES	R/W	0h	Number of dummy bytes to be used for fast read. 0 = use the value in NUM_D_BITS 1 = use 8 bits; 2 = use 16 bits; 3 = use 24 bits Reset Source: qspi_rst_mod_g_rst_n
9:8	NUM_A_BYTES	R/W	2h	Number of address bytes to be sent. 0 = 1 byte; 1 = 2 bytes; 2 = 3 bytes; 3 = 4 bytes Reset Source: qspi_rst_mod_g_rst_n
7:0	RCMD	R/W	3h	Read Command Reset Source: qspi_rst_mod_g_rst_n

4.15.26 MEM_SPI_SWITCH Registers

4.15.26.1 MEM_SWITCH Register (Offset = 64h) [reset = 0h]

Short Description: Memory Mapped SPI Switch

Long Description: Memory Mapped SPI Switch Register

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Table 4-1643. Instance Table

Instance Name	Physical Address
QSPI0	4820 0064h

Figure 4-738. SPI_SWITCH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														MM_INT_EN	MMPT_S
R														R/W	R/W
0h														0h	0h

Access Types Legend

Table 4-1644. SPI_SWITCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R		Always read as 0 Reset Source: qspi_rst_mod_g_rst_n
1	MM_INT_EN	R/W	0h	Memory Mapped mode interrupt enable. 0 Interrupts are disabled during memory mapped operations 1 Word Count interrupt is enabled for memory mapped operations Reset Source: qspi_rst_mod_g_rst_n
0	MMPT_S	R/W	0h	MMPT select. If 0 [default] config port has is selected to control config of core SPI module. If 1, Memory Mapped Protocol Translator is selected to control config port of core SPI module. Reset Source: qspi_rst_mod_g_rst_n

4.15.27 MEM_SPI_DATA1 Registers

4.15.27.1 MEM_DATA1 Register (Offset = 68h) [reset = 0h]

Short Description: SPI Data Register (SPIDR1

Long Description: SPI Data Register (SPIDR1)

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Table 4-1645. Instance Table

Instance Name	Physical Address
QSPI0	4820 0068h

Figure 4-739. SPI_DATA1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA															
R/W															
0h															

Access Types Legend

Table 4-1646. SPI_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Data register for read and write operations Reset Source: qspi_rst_mod_g_rst_n

4.15.28 MEM_SPI_DATA2 Registers

4.15.28.1 MEM_DATA2 Register (Offset = 6Ch) [reset = 0h]

Short Description: SPI Data Register (SPIDR2

Long Description: SPI Data Register (SPIDR2)

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Table 4-1647. Instance Table

Instance Name	Physical Address
QSPI0	4820 006Ch

Figure 4-740. SPI_DATA2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA															
R/W															
0h															

Access Types Legend

Table 4-1648. SPI_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Data register for read and write operations Reset Source: qspi_rst_mod_g_rst_n

4.15.29 MEM_SPI_DATA3 Registers

4.15.29.1 MEM_DATA3 Register (Offset = 70h) [reset = 0h]

Short Description: SPI Data Register (SPIDR3

Long Description: SPI Data Register (SPIDR3)

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Table 4-1649. Instance Table

Instance Name	Physical Address
QSPI0	4820 0070h

Figure 4-741. SPI_DATA3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA															
R/W															
0h															

Access Types Legend

Table 4-1650. SPI_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Data register for read and write operations Reset Source: qspi_rst_mod_g_rst_n

4.15.30 Access Table

Table 4-1651. Access Type Codes

Access Type	Code	Description
R	R	Read
R/W	R/W	Read / Write

4.16 MCSPI Registers

Table 4-1652. CFG, CFG Registers, Base Address=0X0000000052200000, Length=1024

Offset	Length	Register Name	MCSPI0 Physical Address	MCSPI1 Physical Address	MCSPI2 Physical Address
0h	32	HL_REV	5220 0000h	5220 1000h	5220 2000h
4h	32	HL_HWINFO	5220 0004h	5220 1004h	5220 2004h
10h	32	HL_SYSCONFIG	5220 0010h	5220 1010h	5220 2010h
100h	32	REVISION	5220 0100h	5220 1100h	5220 2100h
110h	32	SYSCONFIG	5220 0110h	5220 1110h	5220 2110h
114h	32	SYSSTATUS	5220 0114h	5220 1114h	5220 2114h
118h	32	IRQSTATUS	5220 0118h	5220 1118h	5220 2118h
11Ch	32	IRQENABLE	5220 011Ch	5220 111Ch	5220 211Ch
120h	32	WAKEUPENABLE	5220 0120h	5220 1120h	5220 2120h
124h	32	SYST	5220 0124h	5220 1124h	5220 2124h
128h	32	MODULCTRL	5220 0128h	5220 1128h	5220 2128h
12Ch	32	CH0CONF	5220 012Ch	5220 112Ch	5220 212Ch
130h	32	CH0STAT	5220 0130h	5220 1130h	5220 2130h
134h	32	CH0CTRL	5220 0134h	5220 1134h	5220 2134h
138h	32	TX0	5220 0138h	5220 1138h	5220 2138h
13Ch	32	RX0	5220 013Ch	5220 113Ch	5220 213Ch
140h	32	CH1CONF	5220 0140h	5220 1140h	5220 2140h
144h	32	CH1STAT	5220 0144h	5220 1144h	5220 2144h
148h	32	CH1CTRL	5220 0148h	5220 1148h	5220 2148h
14Ch	32	TX1	5220 014Ch	5220 114Ch	5220 214Ch
150h	32	RX1	5220 0150h	5220 1150h	5220 2150h
154h	32	CH2CONF	5220 0154h	5220 1154h	5220 2154h
158h	32	CH2STAT	5220 0158h	5220 1158h	5220 2158h
15Ch	32	CH2CTRL	5220 015Ch	5220 115Ch	5220 215Ch
160h	32	TX2	5220 0160h	5220 1160h	5220 2160h
164h	32	RX2	5220 0164h	5220 1164h	5220 2164h
168h	32	CH3CONF	5220 0168h	5220 1168h	5220 2168h
16Ch	32	CH3STAT	5220 016Ch	5220 116Ch	5220 216Ch
170h	32	CH3CTRL	5220 0170h	5220 1170h	5220 2170h
174h	32	TX3	5220 0174h	5220 1174h	5220 2174h
178h	32	RX3	5220 0178h	5220 1178h	5220 2178h
17Ch	32	XFERLEVEL	5220 017Ch	5220 117Ch	5220 217Ch
180h	32	DAFTX	5220 0180h	5220 1180h	5220 2180h
1A0h	32	DAFRX	5220 01A0h	5220 11A0h	5220 21A0h

Table 4-1653. CFG, CFG Registers, Base Address=0X0000000052200000, Length=1024

Offset	Length	Register Name	MCSPI3 Physical Address	MCSPI4 Physical Address
0h	32	HL_REV	5220 3000h	5220 4000h
4h	32	HL_HWINFO	5220 3004h	5220 4004h
10h	32	HL_SYSCONFIG	5220 3010h	5220 4010h
100h	32	REVISION	5220 3100h	5220 4100h
110h	32	SYSCONFIG	5220 3110h	5220 4110h
114h	32	SYSSTATUS	5220 3114h	5220 4114h

Table 4-1653. CFG, CFG Registers, Base Address=0X0000000052200000, Length=1024 (continued)

Offset	Length	Register Name	MCSPI3 Physical Address	MCSPI4 Physical Address
118h	32	IRQSTATUS	5220 3118h	5220 4118h
11Ch	32	IRQENABLE	5220 311Ch	5220 411Ch
120h	32	WAKEUPENABLE	5220 3120h	5220 4120h
124h	32	SYST	5220 3124h	5220 4124h
128h	32	MODULCTRL	5220 3128h	5220 4128h
12Ch	32	CH0CONF	5220 312Ch	5220 412Ch
130h	32	CH0STAT	5220 3130h	5220 4130h
134h	32	CH0CTRL	5220 3134h	5220 4134h
138h	32	TX0	5220 3138h	5220 4138h
13Ch	32	RX0	5220 313Ch	5220 413Ch
140h	32	CH1CONF	5220 3140h	5220 4140h
144h	32	CH1STAT	5220 3144h	5220 4144h
148h	32	CH1CTRL	5220 3148h	5220 4148h
14Ch	32	TX1	5220 314Ch	5220 414Ch
150h	32	RX1	5220 3150h	5220 4150h
154h	32	CH2CONF	5220 3154h	5220 4154h
158h	32	CH2STAT	5220 3158h	5220 4158h
15Ch	32	CH2CTRL	5220 315Ch	5220 415Ch
160h	32	TX2	5220 3160h	5220 4160h
164h	32	RX2	5220 3164h	5220 4164h
168h	32	CH3CONF	5220 3168h	5220 4168h
16Ch	32	CH3STAT	5220 316Ch	5220 416Ch
170h	32	CH3CTRL	5220 3170h	5220 4170h
174h	32	TX3	5220 3174h	5220 4174h
178h	32	RX3	5220 3178h	5220 4178h
17Ch	32	XFERLEVEL	5220 317Ch	5220 417Ch
180h	32	DAFTX	5220 3180h	5220 4180h
1A0h	32	DAFRX	5220 31A0h	5220 41A0h

4.16.1 CFG_HL_REV Registers

4.16.1.1 CFG_REV Register (Offset = 0h) [reset = 40301a0bh]

Short Description: IP Revision Identifier (X

Long Description: IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility

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Table 4-1654. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0000h
MCSPI1	5220 1000h
MCSPI2	5220 2000h
MCSPI3	5220 3000h
MCSPI4	5220 4000h

Figure 4-742. HL_REV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		RSVD		FUNC											
R		R		R											
1h		0h		30h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R_RTL				X_MAJOR				CUSTOM		Y_MINOR					
R				R				R		R					
3h				2h				0h		bh					

Access Types Legend

Table 4-1655. HL_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish between old scheme and current
29:28	RSVD	R	0h	Reserved These bits are initialized to zero, and writes to them are ignored
27:16	FUNC	R	30h	Function indicates a software compatible module family If there is no level of software compatibility a new Func number [and hence REVISION] should be assigned
15:11	R_RTL	R	3h	RTL Version [R], maintained by IP design owner RTL follows a numbering such as XYRZ which are explained in this table R changes ONLY when: [1] PDS uploads occur which may have been due to spec changes [2] Bug fixes occur [3] Resets to '0' when X or Y changes Design team has an internal 'Z' [customer invisible] number which increments on every drop that happens due to DV and RTL updates Z resets to 0 when R increments
10:8	X_MAJOR	R	2h	Major Revision [X], maintained by IP specification owner X changes ONLY when: [1] There is a major feature addition An example would be adding Master Mode to Utopia Level2 The Func field [or Class/ Type in old PID format] will remain the same X does NOT change due to: [1] Bug fixes [2] Change in feature parameters
7:6	CUSTOM	R	0h	Indicates a special version for a particular device Consequence of use may avoid use of standard Chip Support Library [CSL] / Drivers

Table 4-1655. HL_REV Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	Y_MINOR	R	Bh	Minor Revision [Y], maintained by IP specification owner Y changes ONLY when: [1] Features are scaled [up or down] Flexibility exists in that this feature scalability may either be represented in the Y change or a specific register in the IP that indicates which features are exactly available [2] When feature creeps from Is-Not list to Is list But this may not be the case once it sees silicon; in which case X will change Y does NOT change due to: [1] Bug fixes [2] Typos or clarifications [3] major functional/feature change/addition/ deletion Instead these changes may be reflected via R, S, X as applicable Spec owner maintains a customer-invisible number 'S' which changes due to: [1] Typos/clarifications [2] Bug documentation Note that this bug is not due to a spec change but due to implementation Nevertheless, the spec tracks the IP bugs An RTL release [say for silicon PG11] that occurs due to bug fix should document the corresponding spec number [XYS] in its release notes

4.16.2 CFG_HL_HWINFO Registers

4.16.2.1 CFG_HWINFO Register (Offset = 4h) [reset = 9h]

Short Description: Information about the IP

Long Description: Information about the IP module's hardware configuration, i.e. typically the module's HDL generics (if any). Actual field format and encoding is up to the module's designer to decide.

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Table 4-1656. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0004h
MCSPI1	5220 1004h
MCSPI2	5220 2004h
MCSPI3	5220 3004h
MCSPI4	5220 4004h

Figure 4-743. HL_HWINFO Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									RETMODE	FFNBYTE					USEFIFO
R									R	R					R
0h									0h	4h					1h

Access Types Legend

Table 4-1657. HL_HWINFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RSVD	R	0h	Reserved These bits are initialized to zero, and writes to them are ignored
6	RETMODE	R	0h	This bit field indicates whether the retention mode is supported using the pin PIRFFRET
5:1	FFNBYTE	R	4h	FIFO number of byte generic parameter This register defines the value of FFNBYTE generic parameter, only MSB bits from 8 down to 4 are taken into account
0	USEFIFO	R	1h	Use of a FIFO enable: This bit field indicates if a FIFO is integrated within controller design with its management

4.16.3 CFG_HL_SYSCONFIG Registers

4.16.3.1 CFG_SYSCONFIG Register (Offset = 10h) [reset = 8h]

Short Description: Clock management configur

Long Description: Clock management configuration

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Table 4-1658. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0010h
MCSPI1	5220 1010h
MCSPI2	5220 2010h
MCSPI3	5220 3010h
MCSPI4	5220 4010h

Figure 4-744. HL_SYSCONFIG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD												IDLEMODE		FREEEMU	SOFTRESET
R												R/W		R/W	R/W
0h												2h		0h	0h

Access Types Legend

Table 4-1659. HL_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RSVD	R	0h	Reserved
3:2	IDLEMODE	R/W	2h	Configuration of the local target state management mode By definition, target can handle read/write transaction as long as it is out of IDLE state
1	FREEEMU	R/W	0h	Sensitivity to emulation [debug] suspend input signal
0	SOFTRESET	R/W	0h	Software reset [Optional]

4.16.4 CFG_REVISION Registers

4.16.4.1 CFG_REVISION Register (Offset = 100h) [reset = 2bh]

Short Description: This register contains th

Long Description: This register contains the hard coded RTL revision number.

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Table 4-1660. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0100h
MCSPI1	5220 1100h
MCSPI2	5220 2100h
MCSPI3	5220 3100h
MCSPI4	5220 4100h

Figure 4-745. REVISION Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_13															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_13								REV							
R								R							
0h								2bh							

Access Types Legend

Table 4-1661. REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_13	R	0h	Reads returns 0
7:0	REV	R	2Bh	IP revision [7:4] Major revision [3:0] Minor revision Examples: 0x10 for 10, 0x21 for 21

4.16.5 CFG_SYSCONFIG Registers

4.16.5.1 CFG_SYSCONFIG Register (Offset = 110h) [reset = 15h]

Short Description: This register allows cont

Long Description: This register allows controlling various parameters of the OCP interface.

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Table 4-1662. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0110h
MCSPI1	5220 1110h
MCSPI2	5220 2110h
MCSPI3	5220 3110h
MCSPI4	5220 4110h

Figure 4-746. SYSCONFIG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_14															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_14						CLOCKACTIVITY		RESERVED_15			SIDLEMODE		ENAWAKEUP	SOFTRESET	AUTOIDLE
R						R/W		R			R/W		R/W	R/W	R/W
0h						0h		0h			2h		1h	0h	1h

Access Types Legend

Table 4-1663. SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED_14	R	0h	Reads returns 0
9:8	CLOCKACTIVITY	R/W	0h	Clocks activity during wake up mode period
7:5	RESERVED_15	R	0h	Reads returns 0
4:3	SIDLEMODE	R/W	2h	Power management
2	ENAWAKEUP	R/W	1h	WakeUp feature control
1	SOFTRESET	R/W	0h	Software reset During reads it always returns 0
0	AUTOIDLE	R/W	1h	Internal OCP Clock gating strategy

4.16.6 CFG_SYSSTATUS Registers

4.16.6.1 CFG_SYSSTATUS Register (Offset = 114h) [reset = 1h]

Short Description: This register provides st

Long Description: This register provides status information about the module excluding the interrupt status information

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Table 4-1664. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0114h
MCSPI1	5220 1114h
MCSPI2	5220 2114h
MCSPI3	5220 3114h
MCSPI4	5220 4114h

Figure 4-747. SYSSTATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
N/A															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															RESETDONE
N/A															R
0h															1h

Access Types Legend

Table 4-1665. SYSSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	N/A		Reserved for module specific status information Read returns 0
0	RESETDONE	R	1h	Internal Reset Monitoring

4.16.7 CFG_IRQSTATUS Registers

4.16.7.1 CFG_IRQSTATUS Register (Offset = 118h) [reset = 0h]

Short Description: The interrupt status regr

Long Description: The interrupt status regroups all the status of the module internal events that can generate an interrupt

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Table 4-1666. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0118h
MCSPI1	5220 1118h
MCSPI2	5220 2118h
MCSPI3	5220 3118h
MCSPI4	5220 4118h

Figure 4-748. IRQSTATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														EOW	WKS
N/A														R/W1TS	R/W1TS
0h														0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RX3_FULL	TX3_UNDERFLOW	TX3_EMPTY	RESERVED	RX2_FULL	TX2_UNDERFLOW	TX2_EMPTY	RESERVED	RX1_FULL	TX1_UNDERFLOW	TX1_EMPTY	RX0_OVERFLOW	RX0_FULL	TX0_UNDERFLOW	TX0_EMPTY
N/A	R/W1TS	R/W1TS	R/W1TS	N/A	R/W1TS	R/W1TS	R/W1TS	N/A	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-1667. IRQSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	N/A		Reads returns 0
17	EOW	R/W1TS	0h	End of word count event when a channel is enabled using the FIFO buffer and the channel had sent the number of SPI word defined by MCSPI_XFERLEVEL[WCNT]
16	WKS	R/W1TS	0h	Wake Up event in slave mode when an active control signal is detected on the SPIEN line programmed in the field MCSPI_CH0CONF[SPIENSLV]
15	RESERVED	N/A		Reads returns 0
14	RX3_FULL	R/W1TS	0h	Receiver register is full or almost full Only when Channel 3 is enabled
13	TX3_UNDERFLOW	R/W1TS	0h	Transmitter register underflow Only when Channel 3 is enabled The transmitter register is empty [not updated by Host or DMA with new data] before its time slot assignment Exception: No TX_underflow event when no data has been loaded into the transmitter register since channel has been enabled
12	TX3_EMPTY	R/W1TS	0h	Transmitter register is empty or almost empty Note: Enabling the channel automatically rises this event
11	RESERVED	N/A		Reads returns 0
10	RX2_FULL	R/W1TS	0h	Receiver register full or almost full Channel 2
9	TX2_UNDERFLOW	R/W1TS	0h	Transmitter register underflow Channel 2

Table 4-1667. IRQSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	TX2_EMPTY	R/W1TS	0h	Transmitter register empty or almost empty Channel 2
7	RESERVED	N/A		Reads returns 0
6	RX1_FULL	R/W1TS	0h	Receiver register full or almost full Channel 1
5	TX1_UNDERFLOW	R/W1TS	0h	Transmitter register underflow Channel 1
4	TX1_EMPTY	R/W1TS	0h	Transmitter register empty or almost empty Channel 1
3	RX0_OVERFLOW	R/W1TS	0h	Receiver register overflow [slave mode only] Channel 0
2	RX0_FULL	R/W1TS	0h	Receiver register full or almost full Channel 0
1	TX0_UNDERFLOW	R/W1TS	0h	Transmitter register underflow Channel 0
0	TX0_EMPTY	R/W1TS	0h	Transmitter register empty or almost empty Channel 0

4.16.8 CFG_IRQENABLE Registers

4.16.8.1 CFG_IRQENABLE Register (Offset = 11Ch) [reset = 0h]

Short Description: This register allows to e

Long Description: This register allows to enable/disable the module internal sources of interrupt, on an event-by-event basis.

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Table 4-1668. Instance Table

Instance Name	Physical Address
MCSPI0	5220 011Ch
MCSPI1	5220 111Ch
MCSPI2	5220 211Ch
MCSPI3	5220 311Ch
MCSPI4	5220 411Ch

Figure 4-749. IRQENABLE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														EOW_ENABLE	WKE
N/A														R/W	R/W
0h														0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RX3_FULL_ENABLE	TX3_UNDERFLOW_ENABLE	TX3_EMPTY_ENABLE	RESERVED	RX2_FULL_ENABLE	TX2_UNDERFLOW_ENABLE	TX2_EMPTY_ENABLE	RESERVED	RX1_FULL_ENABLE	TX1_UNDERFLOW_ENABLE	TX1_EMPTY_ENABLE	RX0_OVERFLOW_ENABLE	RX0_FULL_ENABLE	TX0_UNDERFLOW_ENABLE	TX0_EMPTY_ENABLE
N/A	R/W	R/W	R/W	N/A	R/W	R/W	R/W	N/A	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-1669. IRQENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	N/A		Reads return 0
17	EOW_ENABLE	R/W	0h	End of Word count Interrupt Enable
16	WKE	R/W	0h	Wake Up event interrupt Enable in slave mode when an active control signal is detected on the SPIEN line programmed in the field MCSPI_CH0CONF[SPIENSLV]
15	RESERVED	N/A		Reads returns 0
14	RX3_FULL_ENABLE	R/W	0h	Receiver register Full Interrupt Enable Ch 3
13	TX3_UNDERFLOW_ENABLE	R/W	0h	Transmitter register Underflow Interrupt Enable Ch 3
12	TX3_EMPTY_ENABLE	R/W	0h	Transmitter register Empty Interrupt Enable Ch3
11	RESERVED	N/A		Reads return 0
10	RX2_FULL_ENABLE	R/W	0h	Receiver register Full Interrupt Enable Ch 2
9	TX2_UNDERFLOW_ENABLE	R/W	0h	Transmitter register Underflow Interrupt Enable Ch 2
8	TX2_EMPTY_ENABLE	R/W	0h	Transmitter register Empty Interrupt Enable Ch 2
7	RESERVED	N/A		Reads return 0
6	RX1_FULL_ENABLE	R/W	0h	Receiver register Full Interrupt Enable Ch 1

Table 4-1669. IRQENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	TX1_UNDERFLOW_ENABLE	R/W	0h	Transmitter register Underflow Interrupt Enable Ch 1
4	TX1_EMPTY_ENABLE	R/W	0h	Transmitter register Empty Interrupt Enable Ch 1
3	RX0_OVERFLOW_ENABLE	R/W	0h	Receiver register Overflow Interrupt Enable Ch 0
2	RX0_FULL_ENABLE	R/W	0h	Receiver register Full Interrupt Enable Ch 0
1	TX0_UNDERFLOW_ENABLE	R/W	0h	Transmitter register Underflow Interrupt Enable Ch 0
0	TX0_EMPTY_ENABLE	R/W	0h	Transmitter register Empty Interrupt Enable Ch 0

4.16.9 CFG_WAKEUPENABLE Registers

4.16.9.1 CFG_WAKEUPENABLE Register (Offset = 120h) [reset = 0h]

Short Description: The wakeup enable registe

Long Description: The wakeup enable register allows to enable/disable the module internal sources of wakeup on event-by-event basis.

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Table 4-1670. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0120h
MCSPI1	5220 1120h
MCSPI2	5220 2120h
MCSPI3	5220 3120h
MCSPI4	5220 4120h

Figure 4-750. WAKEUPENABLE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_18															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_18															WKEN
R															R/W
0h															0h

Access Types Legend

Table 4-1671. WAKEUPENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED_18	R	0h	Reads returns 0
0	WKEN	R/W	0h	WakeUp functionality in slave mode when an active control signal is detected on the SPIEN line programmed in the field MCSPI_CH0CONF[SPIENSLV]

4.16.10 CFG_SYST Registers

4.16.10.1 CFG_SYST Register (Offset = 124h) [reset = 0h]

Short Description: This register is used to

Long Description: This register is used to check the correctness of the system interconnect either internally to peripheral bus, or externally to device IO pads, when the module is configured in system test (SYSTEST) mode.

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Table 4-1672. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0124h
MCSPI1	5220 1124h
MCSPI2	5220 2124h
MCSPI3	5220 3124h
MCSPI4	5220 4124h

Figure 4-751. SYST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
N/A															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				SSB	SPIENDIR	SPIDATDIR1	SPIDATDIR0	WAKD	SPICLK	SPIDAT_1	SPIDAT_0	SPIEN_3	SPIEN_2	SPIEN_1	SPIEN_0
N/A				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-1673. SYST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	N/A		Reads returns 0
11	SSB	R/W	0h	Set status bit
10	SPIENDIR	R/W	0h	Set the direction of the SPIEN[3:0] lines and SPICLK line
9	SPIDATDIR1	R/W	0h	Set the direction of the SPIDAT[1]
8	SPIDATDIR0	R/W	0h	Set the direction of the SPIDAT[0]
7	WAKD	R/W	0h	SWAKEUP output [signal data value of internal signal to system] The signal is driven high or low according to the value written into this register bit
6	SPICLK	R/W	0h	SPICLK line [signal data value] If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the CLKSPI line [high or low], and a write into this bit has no effect If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the CLKSPI line is driven high or low according to the value written into this register
5	SPIDAT_1	R/W	0h	SPIDAT[1] line [signal data value] If MCSPI_SYST[SPIDATDIR1] = 0 [output mode direction], the SPIDAT[1] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIDATDIR1] = 1 [input mode direction], this bit returns the value on the SPIDAT[1] line [high or low], and a write into this bit has no effect

Table 4-1673. SYST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SPIDAT_0	R/W	0h	SPIDAT[0] line [signal data value] If MCSPI_SYST[SPIDATDIR0] = 0 [output mode direction], the SPIDAT[0] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIDATDIR0] = 1 [input mode direction], this bit returns the value on the SPIDAT[0] line [high or low], and a write into this bit has no effect
3	SPIEN_3	R/W	0h	SPIEN[3] line [signal data value] If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the SPIENT[3] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the SPIEN[3] line [high or low], and a write into this bit has no effect
2	SPIEN_2	R/W	0h	SPIEN[2] line [signal data value] If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the SPIENT[2] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the SPIEN[2] line [high or low], and a write into this bit has no effect
1	SPIEN_1	R/W	0h	SPIEN[1] line [signal data value] If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the SPIENT[1] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the SPIEN[1] line [high or low], and a write into this bit has no effect
0	SPIEN_0	R/W	0h	SPIEN[0] line [signal data value] If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the SPIENT[0] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the SPIEN[0] line [high or low], and a write into this bit has no effect

4.16.11 CFG_MODULCTRL Registers

4.16.11.1 CFG_MODULCTRL Register (Offset = 128h) [reset = 4h]

Short Description: This register is dedicate

Long Description: This register is dedicated to the configuration of the serial port interface.

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Table 4-1674. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0128h
MCSPI1	5220 1128h
MCSPI2	5220 2128h
MCSPI3	5220 3128h
MCSPI4	5220 4128h

Figure 4-752. MODULCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
N/A															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							FDAA	MOA	INITDLY			SYSTEM_TEST	MS	PIN34	SINGLE
N/A							R/W	R/W	R/W			R/W	R/W	R/W	R/W
0h							0h	0h	0h			0h	1h	0h	0h

Access Types Legend

Table 4-1675. MODULCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	N/A		Reads returns 0
8	FDAA	R/W	0h	FIFO DMA Address 256-bit aligned This register is used when a FIFO is managed by the module and DMA connected to the controller provides only 256 bit aligned address If this bit is set the enabled channel which uses the FIFO has its datas managed through MCSPI_DAFTX and MCSPI_DAFRX registers instead of MCSPI_TX[i] and MCSPI_RX[i] registers
7	MOA	R/W	0h	Multiple word ocp access: This register can only be used when a channel is enabled using a FIFO It allows the system to perform multiple SPI word access for a single 32-bit OCP word access This is possible for WL < 16
6:4	INITDLY	R/W	0h	Initial spi delay for first transfer: This register is an option only available in SINGLE master mode, The controller waits for a delay to transmit the first spi word after channel enabled and corresponding TX register filled This Delay is based on SPI output frequency clock, No clock output provided to the boundary and chip select is not active in 4 pin mode within this period
3	SYSTEM_TEST	R/W	0h	Enables the system test mode
2	MS	R/W	1h	Master/ Slave
1	PIN34	R/W	0h	Pin mode selection: This register is used to configure the SPI pin mode, in master or slave mode If asserted the controller only use SIMO,SOMI and SPICLK clock pin for spi transfers
0	SINGLE	R/W	0h	Single channel / Multi Channel [master mode only]

4.16.12 CFG_CH0CONF Registers

4.16.12.1 CFG_CH0CONF Register (Offset = 12Ch) [reset = 60000h]

Short Description: This register is dedicate

Long Description: This register is dedicated to the configuration of the channel 0

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Table 4-1676. Instance Table

Instance Name	Physical Address
MCSPI0	5220 012Ch
MCSPI1	5220 112Ch
MCSPI2	5220 212Ch
MCSPI3	5220 312Ch
MCSPI4	5220 412Ch

Figure 4-753. CH0CONF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		CLKG	FFER	FFEW	TCS0		SBPOL	SBE	SPIENSLV		FORCE	TURBO	IS	DPE1	DPE0
N/A		R/W	R/W	R/W	R/W		R/W	R/W	R/W		R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h		0h	0h	0h		0h	0h	1h	1h	0h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMAR	DMAW	TRM		WL					EPOL	CLKD				POL	PHA
R/W	R/W	R/W		R/W					R/W	R/W				R/W	R/W
0h	0h	0h		0h					0h	0h				0h	0h

Access Types Legend

Table 4-1677. CH0CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	N/A		read returns 0
29	CLKG	R/W	0h	Clock divider granularity This register defines the granularity of channel clock divider: power of two or one clock cycle granularity When this bit is set the register MCSPI_CHCTRL[EXTCLK] must be configured to reach a maximum of 4096 clock divider ratio Then The clock divider ratio is a concatenation of MCSPI_CHCONF[CLKD] and MCSPI_CHCTRL[EXTCLK] values
28	FFER	R/W	0h	FIFO enabled for receive:Only one channel can have this bit field set
27	FFEW	R/W	0h	FIFO enabled for Transmit:Only one channel can have this bit field set
26:25	TCS0	R/W	0h	Chip Select Time Control This 2-bits field defines the number of interface clock cycles between CS toggling and first or last edge of SPI clock
24	SBPOL	R/W	0h	Start bit polarity
23	SBE	R/W	0h	Start bit enable for SPI transfer
22:21	SPIENSLV	R/W	0h	Channel 0 only and slave mode only: SPI slave select signal detection Reserved bits for other cases
20	FORCE	R/W	0h	Manual SPIEN assertion to keep SPIEN active between SPI words [single channel master mode only]
19	TURBO	R/W	0h	Turbo mode
18	IS	R/W	1h	Input Select
17	DPE1	R/W	1h	Transmission Enable for data line 1 [SPIDATAGZEN[1]]
16	DPE0	R/W	0h	Transmission Enable for data line 0 [SPIDATAGZEN[0]]

Table 4-1677. CH0CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	DMAR	R/W	0h	DMA Read request The DMA Read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel The DMA Read request line is deasserted on read completion of the receive register of the channel
14	DMAW	R/W	0h	DMA Write request The DMA Write request line is asserted when The channel is enabled and the transmitter register of the channel is empty The DMA Write request line is deasserted on load completion of the transmitter register of the channel
13:12	TRM	R/W	0h	Transmit/Receive modes
11:7	WL	R/W	0h	SPI word length
6	EPOL	R/W	0h	SPIEN polarity
5:2	CLKD	R/W	0h	Frequency divider for SPICLK [only when the module is a Master SPI device] A programmable clock divider divides the SPI reference clock [CLKSPIREF] with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data By default the clock divider ratio has a power of two granularity when MCSPI_CHCONF[CLKG] is cleared, Otherwise this register is the 4 LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL[EXTCLK] registerThe value description below defines the clock ratio when MCSPI_CHCONF[CLKG] is set to 0
1	POL	R/W	0h	SPICLK polarity
0	PHA	R/W	0h	SPICLK phase

4.16.13 CFG_CH0STAT Registers

4.16.13.1 CFG_CH0STAT Register (Offset = 130h) [reset = 0h]

Short Description: This register provides st

Long Description: This register provides status information about transmitter and receiver registers of channel 0

Return to Summary Table

Table 4-1678. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0130h
MCSPI1	5220 1130h
MCSPI2	5220 2130h
MCSPI3	5220 3130h
MCSPI4	5220 4130h

Figure 4-754. CH0STAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
N/A															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									RXFFF	RXFFE	TXFFF	TXFFE	EOT	TXS	RXS
N/A									R	R	R	R	R	R	R
0h									0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-1679. CH0STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	N/A		Read returns 0
6	RXFFF	R	0h	Channel "i" FIFO Receive Buffer Full Status
5	RXFFE	R	0h	Channel "i" FIFO Receive Buffer Empty Status
4	TXFFF	R	0h	Channel "i" FIFO Transmit Buffer Full Status
3	TXFFE	R	0h	Channel "i" FIFO Transmit Buffer Empty Status
2	EOT	R	0h	Channel "i" End of transfer Status The definitions of beginning and end of transfer vary with master versus slave and the transfer format [Transmit/Receive modes, Turbo mode] See dedicated chapters for details
1	TXS	R	0h	Channel "i" Transmitter Register Status
0	RXS	R	0h	Channel "i" Receiver Register Status

4.16.14 CFG_CH0CTRL Registers

4.16.14.1 CFG_CH0CTRL Register (Offset = 134h) [reset = 0h]

Short Description: This register is dedicate

Long Description: This register is dedicated to enable the channel 0

Return to Summary Table

Table 4-1680. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0134h
MCSPI1	5220 1134h
MCSPI2	5220 2134h
MCSPI3	5220 3134h
MCSPI4	5220 4134h

Figure 4-755. CH0CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
N/A															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTCLK								RESERVED							EN
R/W								N/A							R/W
0h								0h							0h

Access Types Legend

Table 4-1681. CH0CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	N/A		Read returns 0
15:8	EXTCLK	R/W	0h	Clock ratio extension: This register is used to concatenate with MCSPI_CHCONF[CLKD] register for clock ratio only when granularity is one clock cycle [MCSPI_CHCONF[CLKG] set to 1] Then the max value reached is 4096 clock divider ratio
7:1	RESERVED	N/A		Read returns 0
0	EN	R/W	0h	Channel Enable

4.16.15 CFG_TX0 Registers

4.16.15.1 CFG_TX0 Register (Offset = 138h) [reset = 0h]

Short Description: This register contains a

Long Description: This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.

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Table 4-1682. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0138h
MCSPI1	5220 1138h
MCSPI2	5220 2138h
MCSPI3	5220 3138h
MCSPI4	5220 4138h

Figure 4-756. TX0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TDATA															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDATA															
R/W															
0h															

Access Types Legend

Table 4-1683. TX0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDATA	R/W	0h	Channel 0 Data to transmit

4.16.16 CFG_RX0 Registers

4.16.16.1 CFG_RX0 Register (Offset = 13Ch) [reset = 0h]

Short Description: This register contains a

Long Description: This register contains a single SPI word received through the serial link, what ever SPI word length is.

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Table 4-1684. Instance Table

Instance Name	Physical Address
MCSPI0	5220 013Ch
MCSPI1	5220 113Ch
MCSPI2	5220 213Ch
MCSPI3	5220 313Ch
MCSPI4	5220 413Ch

Figure 4-757. RX0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RDATA															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDATA															
R															
0h															

Access Types Legend

Table 4-1685. RX0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RDATA	R	0h	Channel 0 Received Data

4.16.17 CFG_CH1CONF Registers

4.16.17.1 CFG_CH1CONF Register (Offset = 140h) [reset = 60000h]

Short Description: This register is dedicate

Long Description: This register is dedicated to the configuration of the channel.

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Table 4-1686. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0140h
MCSPI1	5220 1140h
MCSPI2	5220 2140h
MCSPI3	5220 3140h
MCSPI4	5220 4140h

Figure 4-758. CH1CONF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		CLKG	FFER	FFEW	TCS1		SBPOL	SBE	RESERVED		FORCE	TURBO	IS	DPE1	DPE0
N/A		R/W	R/W	R/W	R/W		R/W	R/W	N/A		R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h		0h	0h	0h		0h	0h	1h	1h	0h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMAR	DMAW	TRM		WL					EPOL	CLKD				POL	PHA
R/W	R/W	R/W		R/W					R/W	R/W				R/W	R/W
0h	0h	0h		0h					0h	0h				0h	0h

Access Types Legend

Table 4-1687. CH1CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	N/A		read returns 0
29	CLKG	R/W	0h	Clock divider granularity This register defines the granularity of channel clock divider: power of two or one clock cycle granularity When this bit is set the register MCSPI_CHCTRL[EXTCLK] must be configured to reach a maximum of 4096 clock divider ratio Then The clock divider ratio is a concatenation of MCSPI_CHCONF[CLKD] and MCSPI_CHCTRL[EXTCLK] values
28	FFER	R/W	0h	FIFO enabled for receive:Only one channel can have this bit field set
27	FFEW	R/W	0h	FIFO enabled for Transmit:Only one channel can have this bit field set
26:25	TCS1	R/W	0h	Chip Select Time Control This 2-bits field defines the number of interface clock cycles between CS toggling and first or last edge of SPI clock
24	SBPOL	R/W	0h	Start bit polarity
23	SBE	R/W	0h	Start bit enable for SPI transfer
22:21	RESERVED	N/A		read returns 0
20	FORCE	R/W	0h	Manual SPIEN assertion to keep SPIEN active between SPI words [single channel master mode only]
19	TURBO	R/W	0h	Turbo mode
18	IS	R/W	1h	Input Select
17	DPE1	R/W	1h	Transmission Enable for data line 1 [SPIDATAGZEN[1]]
16	DPE0	R/W	0h	Transmission Enable for data line 0 [SPIDATAGZEN[0]]

Table 4-1687. CH1CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	DMAR	R/W	0h	DMA Read request The DMA Read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel The DMA Read request line is deasserted on read completion of the receive register of the channel
14	DMAW	R/W	0h	DMA Write request The DMA Write request line is asserted when The channel is enabled and the transmitter register of the channel is empty The DMA Write request line is deasserted on load completion of the transmitter register of the channel
13:12	TRM	R/W	0h	Transmit/Receive modes
11:7	WL	R/W	0h	SPI word length
6	EPOL	R/W	0h	SPIEN polarity
5:2	CLKD	R/W	0h	Frequency divider for SPICLK [only when the module is a Master SPI device] A programmable clock divider divides the SPI reference clock [CLKSPIREF] with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data By default the clock divider ratio has a power of two granularity when MCSPI_CHCONF[CLKG] is cleared, Otherwise this register is the 4 LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL[EXTCLK] registerThe value description below defines the clock ratio when MCSPI_CHCONF[CLKG] is set to 0
1	POL	R/W	0h	SPICLK polarity
0	PHA	R/W	0h	SPICLK phase

4.16.18 CFG_CH1STAT Registers

4.16.18.1 CFG_CH1STAT Register (Offset = 144h) [reset = 0h]

Short Description: This register provides st

Long Description: This register provides status information about transmitter and receiver registers of channel 1

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Table 4-1688. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0144h
MCSPI1	5220 1144h
MCSPI2	5220 2144h
MCSPI3	5220 3144h
MCSPI4	5220 4144h

Figure 4-759. CH1STAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
N/A															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									RXFFF	RXFFE	TXFFF	TXFFE	EOT	TXS	RXS
N/A									R	R	R	R	R	R	R
0h									0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-1689. CH1STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	N/A		Read returns 0
6	RXFFF	R	0h	Channel "i" FIFO Receive Buffer Full Status
5	RXFFE	R	0h	Channel "i" FIFO Receive Buffer Empty Status
4	TXFFF	R	0h	Channel "i" FIFO Transmit Buffer Full Status
3	TXFFE	R	0h	Channel "i" FIFO Transmit Buffer Empty Status
2	EOT	R	0h	Channel "i" End of transfer Status The definitions of beginning and end of transfer vary with master versus slave and the transfer format [Transmit/Receive modes, Turbo mode] See dedicated chapters for details
1	TXS	R	0h	Channel "i" Transmitter Register Status
0	RXS	R	0h	Channel "i" Receiver Register Status

4.16.19 CFG_CH1CTRL Registers

4.16.19.1 CFG_CH1CTRL Register (Offset = 148h) [reset = 0h]

Short Description: This register is dedicate

Long Description: This register is dedicated to enable the channel 1

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Table 4-1690. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0148h
MCSPI1	5220 1148h
MCSPI2	5220 2148h
MCSPI3	5220 3148h
MCSPI4	5220 4148h

Figure 4-760. CH1CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
N/A															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTCLK								RESERVED							EN
R/W								N/A							R/W
0h								0h							0h

Access Types Legend

Table 4-1691. CH1CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	N/A		Read returns 0
15:8	EXTCLK	R/W	0h	Clock ratio extension: This register is used to concatenate with MCSPI_CHCONF[CLKD] register for clock ratio only when granularity is one clock cycle [MCSPI_CHCONF[CLKG] set to 1] Then the max value reached is 4096 clock divider ratio
7:1	RESERVED	N/A		Read returns 0
0	EN	R/W	0h	Channel Enable

4.16.20 CFG_TX1 Registers

4.16.20.1 CFG_TX1 Register (Offset = 14Ch) [reset = 0h]

Short Description: This register contains a

Long Description: This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.

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Table 4-1692. Instance Table

Instance Name	Physical Address
MCSPI0	5220 014Ch
MCSPI1	5220 114Ch
MCSPI2	5220 214Ch
MCSPI3	5220 314Ch
MCSPI4	5220 414Ch

Figure 4-761. TX1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TDATA															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDATA															
R/W															
0h															

Access Types Legend

Table 4-1693. TX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDATA	R/W	0h	Channel 1 Data to transmit

4.16.21 CFG_RX1 Registers

4.16.21.1 CFG_RX1 Register (Offset = 150h) [reset = 0h]

Short Description: This register contains a

Long Description: This register contains a single SPI word received through the serial link, what ever SPI word length is.

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Table 4-1694. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0150h
MCSPI1	5220 1150h
MCSPI2	5220 2150h
MCSPI3	5220 3150h
MCSPI4	5220 4150h

Figure 4-762. RX1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RDATA															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDATA															
R															
0h															

Access Types Legend

Table 4-1695. RX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RDATA	R	0h	Channel 1 Received Data

4.16.22 CFG_CH2CONF Registers

4.16.22.1 CFG_CH2CONF Register (Offset = 154h) [reset = 60000h]

Short Description: This register is dedicate

Long Description: This register is dedicated to the configuration of the channel 2

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Table 4-1696. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0154h
MCSPI1	5220 1154h
MCSPI2	5220 2154h
MCSPI3	5220 3154h
MCSPI4	5220 4154h

Figure 4-763. CH2CONF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		CLKG	FFER	FFEW	TCS2		SBPOL	SBE	RESERVED		FORCE	TURBO	IS	DPE1	DPE0
N/A		R/W	R/W	R/W	R/W		R/W	R/W	N/A		R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h		0h	0h	0h		0h	0h	1h	1h	0h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMAR	DMAW	TRM		WL					EPOL	CLKD				POL	PHA
R/W	R/W	R/W		R/W					R/W	R/W				R/W	R/W
0h	0h	0h		0h					0h	0h				0h	0h

Access Types Legend

Table 4-1697. CH2CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	N/A		read returns 0
29	CLKG	R/W	0h	Clock divider granularity This register defines the granularity of channel clock divider: power of two or one clock cycle granularity When this bit is set the register MCSPI_CHCTRL[EXTCLK] must be configured to reach a maximum of 4096 clock divider ratio Then The clock divider ratio is a concatenation of MCSPI_CHCONF[CLKD] and MCSPI_CHCTRL[EXTCLK] values
28	FFER	R/W	0h	FIFO enabled for receive:Only one channel can have this bit field set
27	FFEW	R/W	0h	FIFO enabled for Transmit:Only one channel can have this bit field set
26:25	TCS2	R/W	0h	Chip Select Time Control This 2-bits field defines the number of interface clock cycles between CS toggling and first or last edge of SPI clock
24	SBPOL	R/W	0h	Start bit polarity
23	SBE	R/W	0h	Start bit enable for SPI transfer
22:21	RESERVED	N/A		read returns 0
20	FORCE	R/W	0h	Manual SPIEN assertion to keep SPIEN active between SPI words [single channel master mode only]
19	TURBO	R/W	0h	Turbo mode
18	IS	R/W	1h	Input Select
17	DPE1	R/W	1h	Transmission Enable for data line 1 [SPIDATAGZEN[1]]
16	DPE0	R/W	0h	Transmission Enable for data line 0 [SPIDATAGZEN[0]]

Table 4-1697. CH2CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	DMAR	R/W	0h	DMA Read request The DMA Read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel The DMA Read request line is deasserted on read completion of the receive register of the channel
14	DMAW	R/W	0h	DMA Write request The DMA Write request line is asserted when The channel is enabled and the transmitter register of the channel is empty The DMA Write request line is deasserted on load completion of the transmitter register of the channel
13:12	TRM	R/W	0h	Transmit/Receive modes
11:7	WL	R/W	0h	SPI word length
6	EPOL	R/W	0h	SPIEN polarity
5:2	CLKD	R/W	0h	Frequency divider for SPICLK [only when the module is a Master SPI device] A programmable clock divider divides the SPI reference clock [CLKSPIREF] with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data By default the clock divider ratio has a power of two granularity when MCSPI_CHCONF[CLKG] is cleared, Otherwise this register is the 4 LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL[EXTCLK] registerThe value description below defines the clock ratio when MCSPI_CHCONF[CLKG] is set to 0
1	POL	R/W	0h	SPICLK polarity
0	PHA	R/W	0h	SPICLK phase

4.16.23 CFG_CH2STAT Registers

4.16.23.1 CFG_CH2STAT Register (Offset = 158h) [reset = 0h]

Short Description: This register provides st

Long Description: This register provides status information about transmitter and receiver registers of channel 2

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Table 4-1698. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0158h
MCSPI1	5220 1158h
MCSPI2	5220 2158h
MCSPI3	5220 3158h
MCSPI4	5220 4158h

Figure 4-764. CH2STAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
N/A															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									RXFFF	RXFFE	TXFFF	TXFFE	EOT	TXS	RXS
N/A									R	R	R	R	R	R	R
0h									0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-1699. CH2STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	N/A		Read returns 0
6	RXFFF	R	0h	Channel "i" FIFO Receive Buffer Full Status
5	RXFFE	R	0h	Channel "i" FIFO Receive Buffer Empty Status
4	TXFFF	R	0h	Channel "i" FIFO Transmit Buffer Full Status
3	TXFFE	R	0h	Channel "i" FIFO Transmit Buffer Empty Status
2	EOT	R	0h	Channel "i" End of transfer Status The definitions of beginning and end of transfer vary with master versus slave and the transfer format [Transmit/Receive modes, Turbo mode] See dedicated chapters for details
1	TXS	R	0h	Channel "i" Transmitter Register Status
0	RXS	R	0h	Channel "i" Receiver Register Status

4.16.24 CFG_CH2CTRL Registers

4.16.24.1 CFG_CH2CTRL Register (Offset = 15Ch) [reset = 0h]

Short Description: This register is dedicate

Long Description: This register is dedicated to enable the channel 2

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Table 4-1700. Instance Table

Instance Name	Physical Address
MCSPI0	5220 015Ch
MCSPI1	5220 115Ch
MCSPI2	5220 215Ch
MCSPI3	5220 315Ch
MCSPI4	5220 415Ch

Figure 4-765. CH2CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
N/A															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTCLK								RESERVED							EN
R/W								N/A							R/W
0h								0h							0h

Access Types Legend

Table 4-1701. CH2CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	N/A		Read returns 0
15:8	EXTCLK	R/W	0h	Clock ratio extension: This register is used to concatenate with MCSPI_CHCONF[CLKD] register for clock ratio only when granularity is one clock cycle [MCSPI_CHCONF[CLKG] set to 1] Then the max value reached is 4096 clock divider ratio
7:1	RESERVED	N/A		Read returns 0
0	EN	R/W	0h	Channel Enable

4.16.25 CFG_TX2 Registers

4.16.25.1 CFG_TX2 Register (Offset = 160h) [reset = 0h]

Short Description: This register contains a

Long Description: This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.

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Table 4-1702. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0160h
MCSPI1	5220 1160h
MCSPI2	5220 2160h
MCSPI3	5220 3160h
MCSPI4	5220 4160h

Figure 4-766. TX2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TDATA															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDATA															
R/W															
0h															

Access Types Legend

Table 4-1703. TX2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDATA	R/W	0h	Channel 2 Data to transmit

4.16.26 CFG_RX2 Registers

4.16.26.1 CFG_RX2 Register (Offset = 164h) [reset = 0h]

Short Description: This register contains a

Long Description: This register contains a single SPI word received through the serial link, what ever SPI word length is.

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Table 4-1704. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0164h
MCSPI1	5220 1164h
MCSPI2	5220 2164h
MCSPI3	5220 3164h
MCSPI4	5220 4164h

Figure 4-767. RX2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RDATA															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDATA															
R															
0h															

Access Types Legend

Table 4-1705. RX2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RDATA	R	0h	Channel 2 Received Data

4.16.27 CFG_CH3CONF Registers

4.16.27.1 CFG_CH3CONF Register (Offset = 168h) [reset = 60000h]

Short Description: This register is dedicate

Long Description: This register is dedicated to the configuration of the channel 3

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Table 4-1706. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0168h
MCSPI1	5220 1168h
MCSPI2	5220 2168h
MCSPI3	5220 3168h
MCSPI4	5220 4168h

Figure 4-768. CH3CONF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		CLKG	FFER	FFEW	TCS3		SBPOL	SBE	RESERVED		FORCE	TURBO	IS	DPE1	DPE0
N/A		R/W	R/W	R/W	R/W		R/W	R/W	N/A		R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h		0h	0h	0h		0h	0h	1h	1h	0h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMAR	DMAW	TRM		WL					EPOL	CLKD				POL	PHA
R/W	R/W	R/W		R/W					R/W	R/W				R/W	R/W
0h	0h	0h		0h					0h	0h				0h	0h

Access Types Legend

Table 4-1707. CH3CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	N/A		read returns 0
29	CLKG	R/W	0h	Clock divider granularity This register defines the granularity of channel clock divider: power of two or one clock cycle granularity When this bit is set the register MCSPI_CHCTRL[EXTCLK] must be configured to reach a maximum of 4096 clock divider ratio Then The clock divider ratio is a concatenation of MCSPI_CHCONF[CLKD] and MCSPI_CHCTRL[EXTCLK] values
28	FFER	R/W	0h	FIFO enabled for receive:Only one channel can have this bit field set
27	FFEW	R/W	0h	FIFO enabled for Transmit:Only one channel can have this bit field set
26:25	TCS3	R/W	0h	Chip Select Time Control This 2-bits field defines the number of interface clock cycles between CS toggling and first or last edge of SPI clock
24	SBPOL	R/W	0h	Start bit polarity
23	SBE	R/W	0h	Start bit enable for SPI transfer
22:21	RESERVED	N/A		read returns 0
20	FORCE	R/W	0h	Manual SPIEN assertion to keep SPIEN active between SPI words [single channel master mode only]
19	TURBO	R/W	0h	Turbo mode
18	IS	R/W	1h	Input Select
17	DPE1	R/W	1h	Transmission Enable for data line 1 [SPIDATAGZEN[1]]
16	DPE0	R/W	0h	Transmission Enable for data line 0 [SPIDATAGZEN[0]]

Table 4-1707. CH3CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	DMAR	R/W	0h	DMA Read request The DMA Read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel The DMA Read request line is deasserted on read completion of the receive register of the channel
14	DMAW	R/W	0h	DMA Write request The DMA Write request line is asserted when The channel is enabled and the transmitter register of the channel is empty The DMA Write request line is deasserted on load completion of the transmitter register of the channel
13:12	TRM	R/W	0h	Transmit/Receive modes
11:7	WL	R/W	0h	SPI word length
6	EPOL	R/W	0h	SPIEN polarity
5:2	CLKD	R/W	0h	Frequency divider for SPICLK [only when the module is a Master SPI device] A programmable clock divider divides the SPI reference clock [CLKSPIREF] with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data By default the clock divider ratio has a power of two granularity when MCSPI_CHCONF[CLKG] is cleared, Otherwise this register is the 4 LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL[EXTCLK] registerThe value description below defines the clock ratio when MCSPI_CHCONF[CLKG] is set to 0
1	POL	R/W	0h	SPICLK polarity
0	PHA	R/W	0h	SPICLK phase

4.16.28 CFG_CH3STAT Registers

4.16.28.1 CFG_CH3STAT Register (Offset = 16Ch) [reset = 0h]

Short Description: This register provides st

Long Description: This register provides status information about transmitter and receiver registers of channel 3

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Table 4-1708. Instance Table

Instance Name	Physical Address
MCSPI0	5220 016Ch
MCSPI1	5220 116Ch
MCSPI2	5220 216Ch
MCSPI3	5220 316Ch
MCSPI4	5220 416Ch

Figure 4-769. CH3STAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
N/A															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									RXFFF	RXFFE	TXFFF	TXFFE	EOT	TXS	RXS
N/A									R	R	R	R	R	R	R
0h									0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-1709. CH3STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	N/A		Read returns 0
6	RXFFF	R	0h	Channel "i" FIFO Receive Buffer Full Status
5	RXFFE	R	0h	Channel "i" FIFO Receive Buffer Empty Status
4	TXFFF	R	0h	Channel "i" FIFO Transmit Buffer Full Status
3	TXFFE	R	0h	Channel "i" FIFO Transmit Buffer Empty Status
2	EOT	R	0h	Channel "i" End of transfer Status The definitions of beginning and end of transfer vary with master versus slave and the transfer format [Transmit/Receive modes, Turbo mode] See dedicated chapters for details
1	TXS	R	0h	Channel "i" Transmitter Register Status
0	RXS	R	0h	Channel "i" Receiver Register Status

4.16.29 CFG_CH3CTRL Registers

4.16.29.1 CFG_CH3CTRL Register (Offset = 170h) [reset = 0h]

Short Description: This register is dedicate

Long Description: This register is dedicated to enable the channel 3

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Table 4-1710. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0170h
MCSPI1	5220 1170h
MCSPI2	5220 2170h
MCSPI3	5220 3170h
MCSPI4	5220 4170h

Figure 4-770. CH3CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
N/A															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTCLK								RESERVED							EN
R/W								N/A							R/W
0h								0h							0h

Access Types Legend

Table 4-1711. CH3CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	N/A		Read returns 0
15:8	EXTCLK	R/W	0h	Clock ratio extension: This register is used to concatenate with MCSPI_CHCONF[CLKD] register for clock ratio only when granularity is one clock cycle [MCSPI_CHCONF[CLKG] set to 1] Then the max value reached is 4096 clock divider ratio
7:1	RESERVED	N/A		Read returns 0
0	EN	R/W	0h	Channel Enable

4.16.30 CFG_TX3 Registers

4.16.30.1 CFG_TX3 Register (Offset = 174h) [reset = 0h]

Short Description: This register contains a

Long Description: This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.

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Table 4-1712. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0174h
MCSPI1	5220 1174h
MCSPI2	5220 2174h
MCSPI3	5220 3174h
MCSPI4	5220 4174h

Figure 4-771. TX3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TDATA															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDATA															
R/W															
0h															

Access Types Legend

Table 4-1713. TX3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDATA	R/W	0h	Channel 3 Data to transmit

4.16.31 CFG_RX3 Registers

4.16.31.1 CFG_RX3 Register (Offset = 178h) [reset = 0h]

Short Description: This register contains a

Long Description: This register contains a single SPI word received through the serial link, what ever SPI word length is.

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Table 4-1714. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0178h
MCSPI1	5220 1178h
MCSPI2	5220 2178h
MCSPI3	5220 3178h
MCSPI4	5220 4178h

Figure 4-772. RX3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RDATA															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDATA															
R															
0h															

Access Types Legend

Table 4-1715. RX3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RDATA	R	0h	Channel 3 Received Data

4.16.32 CFG_XFERLEVEL Registers

4.16.32.1 CFG_XFERLEVEL Register (Offset = 17Ch) [reset = 0h]

Short Description: This register provides tr

Long Description: This register provides transfer levels needed while using FIFO buffer during transfer.

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Table 4-1716. Instance Table

Instance Name	Physical Address
MCSPI0	5220 017Ch
MCSPI1	5220 117Ch
MCSPI2	5220 217Ch
MCSPI3	5220 317Ch
MCSPI4	5220 417Ch

Figure 4-773. XFERLEVEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WCNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AFL								AEL							
R/W								R/W							
0h								0h							

Access Types Legend

Table 4-1717. XFERLEVEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	WCNT	R/W	0h	Spi word counterThis register holds the programmable value of number of SPI word to be transferred on channel which is using the FIFO bufferWhen transfer had started, a read back in this register returns the current SPI word transfer index
15:8	AFL	R/W	0h	Buffer Almost Full This register holds the programmable almost full level value used to determine almost full buffer condition If the user wants an interrupt or a DMA read request to be issued during a receive operation when the data buffer holds at least n bytes, then the buffer MCSPI_MODULCTRL[AFL] must be set with n-1The size of this register is defined by the generic parameter FFNBYTE
7:0	AEL	R/W	0h	Buffer Almost EmptyThis register holds the programmable almost empty level value used to determine almost empty buffer condition If the user wants an interrupt or a DMA write request to be issued during a transmit operation when the data buffer is able to receive n bytes, then the buffer MCSPI_MODULCTRL[AEL] must be set with n-1

4.16.33 CFG_DAFTX Registers

4.16.33.1 CFG_DAFTX Register (Offset = 180h) [reset = 0h]

Short Description: This register contains th

Long Description: This register contains the SPI words to transmit on the serial link when FIFO used and DMA address is aligned on 256 bit.This register is an image of one of MCSPI_TX(i) register corresponding to the channel which have its FIFO enabled.

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Table 4-1718. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0180h
MCSPI1	5220 1180h
MCSPI2	5220 2180h
MCSPI3	5220 3180h
MCSPI4	5220 4180h

Figure 4-774. DAFTX Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DAFTDATA															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAFTDATA															
R/W															
0h															

Access Types Legend

Table 4-1719. DAFTX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DAFTDATA	R/W	0h	FIFO Data to transmit with DMA 256 bit aligned address This Register is only is used when MCSPI_MODULCTRL[FDAA] is set to "1" and only one of the MCSPI_CH[i]CONF[FFEW] of enabled channels is set If these conditions are not respected any access to this register return a null value

4.16.34 CFG_DAFRX Registers

4.16.34.1 CFG_DAFRX Register (Offset = 1A0h) [reset = 0h]

Short Description: This register contains th

Long Description: This register contains the SPI words to received on the serial link when FIFO used and DMA address is aligned on 256 bit.This register is an image of one of MCSPI_RX(i) register corresponding to the channel which have its FIFO enabled.

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Table 4-1720. Instance Table

Instance Name	Physical Address
MCSPI0	5220 01A0h
MCSPI1	5220 11A0h
MCSPI2	5220 21A0h
MCSPI3	5220 31A0h
MCSPI4	5220 41A0h

Figure 4-775. DAFRX Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DAFRDATA															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAFRDATA															
R															
0h															

Access Types Legend

Table 4-1721. DAFRX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DAFRDATA	R	0h	FIFO Data to transmit with DMA 256 bit aligned address This Register is only is used when MCSPI_MODULCTRL[FDAA] is set to "1" and only one of the MCSPI_CH[i]CONF[FFEW] of enabled channels is set If these conditions are not respected any access to this register return a null value

4.16.35 Access Table

Table 4-1722. Access Type Codes

Access Type	Code	Description
R	R	Read
R/W	R/W	Read / Write
N/A	N/A	Undefined
R/W1TS	R/W1TS	Read/Write 1 To Set

4.17 GPIO Registers

Table 4-1723. MEM, MEM Registers, Base Address=0X0000000052000000, Length=256

Offset	Length	Register Name	GPIO0 Physical Address	GPIO1 Physical Address	GPIO2 Physical Address
0h	32	pid	5200 0000h	5200 1000h	5200 2000h
4h	32	PCR	5200 0004h	5200 1004h	5200 2004h
8h	32	BINTEN	5200 0008h	5200 1008h	5200 2008h
10h	32	DIR01	5200 0010h	5200 1010h	5200 2010h
14h	32	OUT_DATA01	5200 0014h	5200 1014h	5200 2014h
18h	32	SET_DATA01	5200 0018h	5200 1018h	5200 2018h
1Ch	32	CLR_DATA01	5200 001Ch	5200 101Ch	5200 201Ch
20h	32	IN_DATA01	5200 0020h	5200 1020h	5200 2020h
24h	32	SET_RIS_TRIG01	5200 0024h	5200 1024h	5200 2024h
28h	32	CLR_RIS_TRIG01	5200 0028h	5200 1028h	5200 2028h
2Ch	32	SET_FAL_TRIG01	5200 002Ch	5200 102Ch	5200 202Ch
30h	32	CLR_FAL_TRIG01	5200 0030h	5200 1030h	5200 2030h
34h	32	INTSTAT01	5200 0034h	5200 1034h	5200 2034h
38h	32	DIR23	5200 0038h	5200 1038h	5200 2038h
3Ch	32	OUT_DATA23	5200 003Ch	5200 103Ch	5200 203Ch
40h	32	SET_DATA23	5200 0040h	5200 1040h	5200 2040h
44h	32	CLR_DATA23	5200 0044h	5200 1044h	5200 2044h
48h	32	IN_DATA23	5200 0048h	5200 1048h	5200 2048h
4Ch	32	SET_RIS_TRIG23	5200 004Ch	5200 104Ch	5200 204Ch
50h	32	CLR_RIS_TRIG23	5200 0050h	5200 1050h	5200 2050h
54h	32	SET_FAL_TRIG23	5200 0054h	5200 1054h	5200 2054h
58h	32	CLR_FAL_TRIG23	5200 0058h	5200 1058h	5200 2058h
5Ch	32	INTSTAT23	5200 005Ch	5200 105Ch	5200 205Ch
60h	32	DIR45	5200 0060h	5200 1060h	5200 2060h
64h	32	OUT_DATA45	5200 0064h	5200 1064h	5200 2064h
68h	32	SET_DATA45	5200 0068h	5200 1068h	5200 2068h
6Ch	32	CLR_DATA45	5200 006Ch	5200 106Ch	5200 206Ch
70h	32	IN_DATA45	5200 0070h	5200 1070h	5200 2070h
74h	32	SET_RIS_TRIG45	5200 0074h	5200 1074h	5200 2074h
78h	32	CLR_RIS_TRIG45	5200 0078h	5200 1078h	5200 2078h
7Ch	32	SET_FAL_TRIG45	5200 007Ch	5200 107Ch	5200 207Ch
80h	32	CLR_FAL_TRIG45	5200 0080h	5200 1080h	5200 2080h
84h	32	INTSTAT45	5200 0084h	5200 1084h	5200 2084h
88h	32	DIR67	5200 0088h	5200 1088h	5200 2088h
8Ch	32	OUT_DATA67	5200 008Ch	5200 108Ch	5200 208Ch
90h	32	SET_DATA67	5200 0090h	5200 1090h	5200 2090h
94h	32	CLR_DATA67	5200 0094h	5200 1094h	5200 2094h
98h	32	IN_DATA67	5200 0098h	5200 1098h	5200 2098h
9Ch	32	SET_RIS_TRIG67	5200 009Ch	5200 109Ch	5200 209Ch
A0h	32	CLR_RIS_TRIG67	5200 00A0h	5200 10A0h	5200 20A0h
A4h	32	SET_FAL_TRIG67	5200 00A4h	5200 10A4h	5200 20A4h
A8h	32	CLR_FAL_TRIG67	5200 00A8h	5200 10A8h	5200 20A8h
ACh	32	INTSTAT67	5200 00ACh	5200 10ACh	5200 20ACh
B0h	32	DIR8	5200 00B0h	5200 10B0h	5200 20B0h
B4h	32	OUT_DATA8	5200 00B4h	5200 10B4h	5200 20B4h

Table 4-1723. MEM, MEM Registers, Base Address=0X0000000052000000, Length=256 (continued)

Offset	Length	Register Name	GPIO0 Physical Address	GPIO1 Physical Address	GPIO2 Physical Address
B8h	32	SET_DATA8	5200 00B8h	5200 10B8h	5200 20B8h
BCh	32	CLR_DATA8	5200 00BCh	5200 10BCh	5200 20BCh
C0h	32	IN_DATA8	5200 00C0h	5200 10C0h	5200 20C0h
C4h	32	SET_RIS_TRIG8	5200 00C4h	5200 10C4h	5200 20C4h
C8h	32	CLR_RIS_TRIG8	5200 00C8h	5200 10C8h	5200 20C8h
CCh	32	SET_FAL_TRIG8	5200 00CCh	5200 10CCh	5200 20CCh
D0h	32	CLR_FAL_TRIG8	5200 00D0h	5200 10D0h	5200 20D0h
D4h	32	INTSTAT8	5200 00D4h	5200 10D4h	5200 20D4h

Table 4-1724. MEM, MEM Registers, Base Address=0X0000000052000000, Length=256

Offset	Length	Register Name	GPIO3 Physical Address
0h	32	pid	5200 3000h
4h	32	PCR	5200 3004h
8h	32	BINTEN	5200 3008h
10h	32	DIR01	5200 3010h
14h	32	OUT_DATA01	5200 3014h
18h	32	SET_DATA01	5200 3018h
1Ch	32	CLR_DATA01	5200 301Ch
20h	32	IN_DATA01	5200 3020h
24h	32	SET_RIS_TRIG01	5200 3024h
28h	32	CLR_RIS_TRIG01	5200 3028h
2Ch	32	SET_FAL_TRIG01	5200 302Ch
30h	32	CLR_FAL_TRIG01	5200 3030h
34h	32	INTSTAT01	5200 3034h
38h	32	DIR23	5200 3038h
3Ch	32	OUT_DATA23	5200 303Ch
40h	32	SET_DATA23	5200 3040h
44h	32	CLR_DATA23	5200 3044h
48h	32	IN_DATA23	5200 3048h
4Ch	32	SET_RIS_TRIG23	5200 304Ch
50h	32	CLR_RIS_TRIG23	5200 3050h
54h	32	SET_FAL_TRIG23	5200 3054h
58h	32	CLR_FAL_TRIG23	5200 3058h
5Ch	32	INTSTAT23	5200 305Ch
60h	32	DIR45	5200 3060h
64h	32	OUT_DATA45	5200 3064h
68h	32	SET_DATA45	5200 3068h
6Ch	32	CLR_DATA45	5200 306Ch
70h	32	IN_DATA45	5200 3070h
74h	32	SET_RIS_TRIG45	5200 3074h
78h	32	CLR_RIS_TRIG45	5200 3078h
7Ch	32	SET_FAL_TRIG45	5200 307Ch
80h	32	CLR_FAL_TRIG45	5200 3080h
84h	32	INTSTAT45	5200 3084h
88h	32	DIR67	5200 3088h
8Ch	32	OUT_DATA67	5200 308Ch
90h	32	SET_DATA67	5200 3090h

Table 4-1724. MEM, MEM Registers, Base Address=0X0000000052000000, Length=256 (continued)

Offset	Length	Register Name	GPIO3 Physical Address
94h	32	CLR_DATA67	5200 3094h
98h	32	IN_DATA67	5200 3098h
9Ch	32	SET_RIS_TRIG67	5200 309Ch
A0h	32	CLR_RIS_TRIG67	5200 30A0h
A4h	32	SET_FAL_TRIG67	5200 30A4h
A8h	32	CLR_FAL_TRIG67	5200 30A8h
ACh	32	INTSTAT67	5200 30ACh
B0h	32	DIR8	5200 30B0h
B4h	32	OUT_DATA8	5200 30B4h
B8h	32	SET_DATA8	5200 30B8h
BCh	32	CLR_DATA8	5200 30BCh
C0h	32	IN_DATA8	5200 30C0h
C4h	32	SET_RIS_TRIG8	5200 30C4h
C8h	32	CLR_RIS_TRIG8	5200 30C8h
CCh	32	SET_FAL_TRIG8	5200 30CCh
D0h	32	CLR_FAL_TRIG8	5200 30D0h
D4h	32	INTSTAT8	5200 30D4h

4.17.1 MEM_PID Registers

4.17.1.1 MEM_PID Register (Offset = 0h) [reset = 44832905h]

Short Description: GPIO Peripheral ID Registe

Long Description: GPIO Peripheral ID Register

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Table 4-1725. Instance Table

Instance Name	Physical Address
GPIO0	5200 0000h
GPIO1	5200 1000h
GPIO2	5200 2000h
GPIO3	5200 3000h

Figure 4-776. PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		RESERVED		FUNC											
R		R		R											
1h		0h		483h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
R					R			R		R					
5h					1h			0h		5h					

Access Types Legend

Table 4-1726. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Current scheme Reset Source: mod_g_srst_n
29:28	RESERVED	R		RESERVED Reset Source: mod_g_srst_n
27:16	FUNC	R	483h	Function code assigned to TCP3 Reset Source: mod_g_srst_n
15:11	RTL	R	5h	RTL Version R code Reset Source: mod_g_srst_n
10:8	MAJOR	R	1h	Major revision X code Reset Source: mod_g_srst_n
7:6	CUSTOM	R	0h	Custom version code Reset Source: mod_g_srst_n
5:0	MINOR	R	5h	Minor revision Y code Reset Source: mod_g_srst_n

4.17.2 MEM_PCR Registers

4.17.2.1 MEM_PCR Register (Offset = 4h) [reset = 1h]

Short Description: Peripheral Control Regist

Long Description: Peripheral Control Register

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Table 4-1727. Instance Table

Instance Name	Physical Address
GPIO0	5200 0004h
GPIO1	5200 1004h
GPIO2	5200 2004h
GPIO3	5200 3004h

Figure 4-777. PCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														SOFT	FREE
NONE														R	R
0														0h	1h

Access Types Legend

Table 4-1728. PCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1	SOFT	R	0h	Used in conjunction with FREE bit to determine the emulation suspend mode. Reset Source: mod_g_srst_n
0	FREE	R	1h	For GPIO, the FREE bit is fixed at 1, which means GPIO runs free in emulation suspend. Reset Source: mod_g_srst_n

4.17.3 MEM_BINTEN Registers

4.17.3.1 MEM_BINTEN Register (Offset = 8h) [reset = 0h]

Short Description: Bit Interrupt Enable Regi

Long Description: Bit Interrupt Enable Register

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Table 4-1729. Instance Table

Instance Name	Physical Address
GPIO0	5200 0008h
GPIO1	5200 1008h
GPIO2	5200 2008h
GPIO3	5200 3008h

Figure 4-778. BINTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN															
R/W															
0h															

Access Types Legend

Table 4-1730. BINTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R		RESERVED Reset Source: mod_g_srst_n
15:0	EN	R/W	0h	Per bank interrupt enable. 0 = disable, 1 = enable. Reset Source: mod_g_srst_n

4.17.4 MEM_DIR01 Registers

4.17.4.1 MEM_DIR01 Register (Offset = 10h) [reset = ffffffffh]

Short Description: Direction Register

Long Description: Direction Register

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Table 4-1731. Instance Table

Instance Name	Physical Address
GPIO0	5200 0010h
GPIO1	5200 1010h
GPIO2	5200 2010h
GPIO3	5200 3010h

Figure 4-779. DIR01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DIR1															
R/W															
ffffh															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIR0															
R/W															
ffffh															

Access Types Legend

Table 4-1732. DIR01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DIR1	R/W	FFFFh	Direction of GPIO bank 1 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n
15:0	DIR0	R/W	FFFFh	Direction of GPIO bank 0 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n

4.17.5 MEM_OUT_DATA01 Registers

4.17.5.1 MEM_DATA01 Register (Offset = 14h) [reset = 0h]

Short Description: Output Drive State Regist

Long Description: Output Drive State Register

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Table 4-1733. Instance Table

Instance Name	Physical Address
GPIO0	5200 0014h
GPIO1	5200 1014h
GPIO2	5200 2014h
GPIO3	5200 3014h

Figure 4-780. OUT_DATA01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUT1															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUT0															
R/W															
0h															

Access Types Legend

Table 4-1734. OUT_DATA01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	OUT1	R/W	0h	Output drive state of GPIO bank 1 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	OUT0	R/W	0h	Output drive state of GPIO bank 0 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n

4.17.6 MEM_SET_DATA01 Registers

4.17.6.1 MEM_DATA01 Register (Offset = 18h) [reset = 0h]

Short Description: Set Output Drive State Re

Long Description: Set Output Drive State Register

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Table 4-1735. Instance Table

Instance Name	Physical Address
GPIO0	5200 0018h
GPIO1	5200 1018h
GPIO2	5200 2018h
GPIO3	5200 3018h

Figure 4-781. SET_DATA01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SET1															
R/W1TS															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SET0															
R/W1TS															
0h															

Access Types Legend

Table 4-1736. SET_DATA01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SET1	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 1 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	SET0	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 0 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n

4.17.7 MEM_CLR_DATA01 Registers

4.17.7.1 MEM_DATA01 Register (Offset = 1Ch) [reset = 0h]

Short Description: Clear Output Drive State

Long Description: Clear Output Drive State Register

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Table 4-1737. Instance Table

Instance Name	Physical Address
GPIO0	5200 001Ch
GPIO1	5200 101Ch
GPIO2	5200 201Ch
GPIO3	5200 301Ch

Figure 4-782. CLR_DATA01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLR1															
R/W1TC															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR0															
R/W1TC															
0h															

Access Types Legend

Table 4-1738. CLR_DATA01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLR1	R/W1TC	0h	Writing 1 clears the output drive state of GPIO bank 1. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	CLR0	R/W1TC	0h	Writing 1 clears the output drive state of GPIO bank 0. Reading it returns the output drive state. Reset Source: mod_g_srst_n

4.17.8 MEM_IN_DATA01 Registers

4.17.8.1 MEM_DATA01 Register (Offset = 20h) [reset = 0h]

Short Description: Bank Status Register

Long Description: Bank Status Register

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Table 4-1739. Instance Table

Instance Name	Physical Address
GPIO0	5200 0020h
GPIO1	5200 1020h
GPIO2	5200 2020h
GPIO3	5200 3020h

Figure 4-783. IN_DATA01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IN1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IN0															
R															
0h															

Access Types Legend

Table 4-1740. IN_DATA01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IN1	R	0h	Status of GPIO bank 1 bits. Reset Source: mod_g_srst_n
15:0	IN0	R	0h	Status of GPIO bank 0 bits. Reset Source: mod_g_srst_n

4.17.9 MEM_SET_RIS_TRIG01 Registers

4.17.9.1 MEM_RIS_TRIG01 Register (Offset = 24h) [reset = 0h]

Short Description: Set Rising Edge Detection

Long Description: Set Rising Edge Detection Register

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Table 4-1741. Instance Table

Instance Name	Physical Address
GPIO0	5200 0024h
GPIO1	5200 1024h
GPIO2	5200 2024h
GPIO3	5200 3024h

Figure 4-784. SET_RIS_TRIG01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SETRIS1															
R/W1TS															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETRIS0															
R/W1TS															
0h															

Access Types Legend

Table 4-1742. SET_RIS_TRIG01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETRIS1	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 1 bits. Reset Source: mod_g_srst_n
15:0	SETRIS0	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 0 bits. Reset Source: mod_g_srst_n

4.17.10 MEM_CLR_RIS_TRIG01 Registers

4.17.10.1 MEM_RIS_TRIG01 Register (Offset = 28h) [reset = 0h]

Short Description: Clear Rising Edge Detecti

Long Description: Clear Rising Edge Detection Register

Return to Summary Table

Table 4-1743. Instance Table

Instance Name	Physical Address
GPIO0	5200 0028h
GPIO1	5200 1028h
GPIO2	5200 2028h
GPIO3	5200 3028h

Figure 4-785. CLR_RIS_TRIG01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLRRIS1															
R/W1TC															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRRIS0															
R/W1TC															
0h															

Access Types Legend

Table 4-1744. CLR_RIS_TRIG01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRRIS1	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 1 bits. Reset Source: mod_g_srst_n
15:0	CLRRIS0	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 0 bits. Reset Source: mod_g_srst_n

4.17.11 MEM_SET_FAL_TRIG01 Registers

4.17.11.1 MEM_FAL_TRIG01 Register (Offset = 2Ch) [reset = 0h]

Short Description: Set Falling Edge Detectio

Long Description: Set Falling Edge Detection Register

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Table 4-1745. Instance Table

Instance Name	Physical Address
GPIO0	5200 002Ch
GPIO1	5200 102Ch
GPIO2	5200 202Ch
GPIO3	5200 302Ch

Figure 4-786. SET_FAL_TRIG01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SETFAL1															
R/W1TS															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETFAL0															
R/W1TS															
0h															

Access Types Legend

Table 4-1746. SET_FAL_TRIG01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETFAL1	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 1 bits. Reset Source: mod_g_srst_n
15:0	SETFAL0	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 0 bits. Reset Source: mod_g_srst_n

4.17.12 MEM_CLR_FAL_TRIG01 Registers

4.17.12.1 MEM_FAL_TRIG01 Register (Offset = 30h) [reset = 0h]

Short Description: Clear Falling Edge Detect

Long Description: Clear Falling Edge Detection Register

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Table 4-1747. Instance Table

Instance Name	Physical Address
GPIO0	5200 0030h
GPIO1	5200 1030h
GPIO2	5200 2030h
GPIO3	5200 3030h

Figure 4-787. CLR_FAL_TRIG01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLRFAL1															
R/W1TC															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRFAL0															
R/W1TC															
0h															

Access Types Legend

Table 4-1748. CLR_FAL_TRIG01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRFAL1	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 1 bits. Reset Source: mod_g_srst_n
15:0	CLRFAL0	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 0 bits. Reset Source: mod_g_srst_n

4.17.13 MEM_INTSTAT01 Registers

4.17.13.1 MEM_INTSTAT01 Register (Offset = 34h) [reset = 0h]

Short Description: Bank Interrupt Status Reg

Long Description: Bank Interrupt Status Register

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Table 4-1749. Instance Table

Instance Name	Physical Address
GPIO0	5200 0034h
GPIO1	5200 1034h
GPIO2	5200 2034h
GPIO3	5200 3034h

Figure 4-788. INTSTAT01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STAT1															
R/W1TC															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STAT0															
R/W1TC															
0h															

Access Types Legend

Table 4-1750. INTSTAT01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	STAT1	R/W1TC	0h	Status of GPIO bank 1 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n
15:0	STAT0	R/W1TC	0h	Status of GPIO bank 0 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n

4.17.14 MEM_DIR23 Registers

4.17.14.1 MEM_DIR23 Register (Offset = 38h) [reset = ffffffffh]

Short Description: Direction Register

Long Description: Direction Register

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Table 4-1751. Instance Table

Instance Name	Physical Address
GPIO0	5200 0038h
GPIO1	5200 1038h
GPIO2	5200 2038h
GPIO3	5200 3038h

Figure 4-789. DIR23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DIR3															
R/W															
ffffh															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIR2															
R/W															
ffffh															

Access Types Legend

Table 4-1752. DIR23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DIR3	R/W	FFFFh	Direction of GPIO bank 3 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n
15:0	DIR2	R/W	FFFFh	Direction of GPIO bank 2 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n

4.17.15 MEM_OUT_DATA23 Registers

4.17.15.1 MEM_DATA23 Register (Offset = 3Ch) [reset = 0h]

Short Description: Output Drive State Regist

Long Description: Output Drive State Register

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Table 4-1753. Instance Table

Instance Name	Physical Address
GPIO0	5200 003Ch
GPIO1	5200 103Ch
GPIO2	5200 203Ch
GPIO3	5200 303Ch

Figure 4-790. OUT_DATA23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUT3															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUT2															
R/W															
0h															

Access Types Legend

Table 4-1754. OUT_DATA23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	OUT3	R/W	0h	Output drive state of GPIO bank 3 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	OUT2	R/W	0h	Output drive state of GPIO bank 2 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n

4.17.16 MEM_SET_DATA23 Registers

4.17.16.1 MEM_DATA23 Register (Offset = 40h) [reset = 0h]

Short Description: Set Output Drive State Re

Long Description: Set Output Drive State Register

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Table 4-1755. Instance Table

Instance Name	Physical Address
GPIO0	5200 0040h
GPIO1	5200 1040h
GPIO2	5200 2040h
GPIO3	5200 3040h

Figure 4-791. SET_DATA23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SET3															
R/W1TS															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SET2															
R/W1TS															
0h															

Access Types Legend

Table 4-1756. SET_DATA23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SET3	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 3 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	SET2	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 2 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n

4.17.17 MEM_CLR_DATA23 Registers

4.17.17.1 MEM_DATA23 Register (Offset = 44h) [reset = 0h]

Short Description: Clear Output Drive State

Long Description: Clear Output Drive State Register

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Table 4-1757. Instance Table

Instance Name	Physical Address
GPIO0	5200 0044h
GPIO1	5200 1044h
GPIO2	5200 2044h
GPIO3	5200 3044h

Figure 4-792. CLR_DATA23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLR3															
R/W1TC															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR2															
R/W1TC															
0h															

Access Types Legend

Table 4-1758. CLR_DATA23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLR3	R/W1TC	0h	Writing 1 clears the output drive state of GPIO bank 3. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	CLR2	R/W1TC	0h	Writing 1 clears the output drive state of GPIO bank 2. Reading it returns the output drive state. Reset Source: mod_g_srst_n

4.17.18 MEM_IN_DATA23 Registers

4.17.18.1 MEM_DATA23 Register (Offset = 48h) [reset = 0h]

Short Description: Bank Status Register

Long Description: Bank Status Register

Return to Summary Table

Table 4-1759. Instance Table

Instance Name	Physical Address
GPIO0	5200 0048h
GPIO1	5200 1048h
GPIO2	5200 2048h
GPIO3	5200 3048h

Figure 4-793. IN_DATA23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IN3															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IN2															
R															
0h															

Access Types Legend

Table 4-1760. IN_DATA23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IN3	R	0h	Status of GPIO bank 3 bits. Reset Source: mod_g_srst_n
15:0	IN2	R	0h	Status of GPIO bank 2 bits. Reset Source: mod_g_srst_n

4.17.19 MEM_SET_RIS_TRIG23 Registers

4.17.19.1 MEM_RIS_TRIG23 Register (Offset = 4Ch) [reset = 0h]

Short Description: Set Rising Edge Detection

Long Description: Set Rising Edge Detection Register

Return to Summary Table

Table 4-1761. Instance Table

Instance Name	Physical Address
GPIO0	5200 004Ch
GPIO1	5200 104Ch
GPIO2	5200 204Ch
GPIO3	5200 304Ch

Figure 4-794. SET_RIS_TRIG23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SETRIS3															
R/W1TS															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETRIS2															
R/W1TS															
0h															

Access Types Legend

Table 4-1762. SET_RIS_TRIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETRIS3	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 3 bits. Reset Source: mod_g_srst_n
15:0	SETRIS2	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 2 bits. Reset Source: mod_g_srst_n

4.17.20 MEM_CLR_RIS_TRIG23 Registers

4.17.20.1 MEM_RIS_TRIG23 Register (Offset = 50h) [reset = 0h]

Short Description: Clear Rising Edge Detecti

Long Description: Clear Rising Edge Detection Register

Return to Summary Table

Table 4-1763. Instance Table

Instance Name	Physical Address
GPIO0	5200 0050h
GPIO1	5200 1050h
GPIO2	5200 2050h
GPIO3	5200 3050h

Figure 4-795. CLR_RIS_TRIG23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLRRIS3															
R/W1TC															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRRIS2															
R/W1TC															
0h															

Access Types Legend

Table 4-1764. CLR_RIS_TRIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRRIS3	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 3 bits. Reset Source: mod_g_srst_n
15:0	CLRRIS2	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 2 bits. Reset Source: mod_g_srst_n

4.17.21 MEM_SET_FAL_TRIG23 Registers

4.17.21.1 MEM_FAL_TRIG23 Register (Offset = 54h) [reset = 0h]

Short Description: Set Falling Edge Detectio

Long Description: Set Falling Edge Detection Register

Return to Summary Table

Table 4-1765. Instance Table

Instance Name	Physical Address
GPIO0	5200 0054h
GPIO1	5200 1054h
GPIO2	5200 2054h
GPIO3	5200 3054h

Figure 4-796. SET_FAL_TRIG23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SETFAL3															
R/W1TS															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETFAL2															
R/W1TS															
0h															

Access Types Legend

Table 4-1766. SET_FAL_TRIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETFAL3	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 3 bits. Reset Source: mod_g_srst_n
15:0	SETFAL2	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 2 bits. Reset Source: mod_g_srst_n

4.17.22 MEM_CLR_FAL_TRIG23 Registers

4.17.22.1 MEM_FAL_TRIG23 Register (Offset = 58h) [reset = 0h]

Short Description: Clear Falling Edge Detect

Long Description: Clear Falling Edge Detection Register

Return to Summary Table

Table 4-1767. Instance Table

Instance Name	Physical Address
GPIO0	5200 0058h
GPIO1	5200 1058h
GPIO2	5200 2058h
GPIO3	5200 3058h

Figure 4-797. CLR_FAL_TRIG23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLRFAL3															
R/W1TC															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRFAL2															
R/W1TC															
0h															

Access Types Legend

Table 4-1768. CLR_FAL_TRIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRFAL3	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 3 bits. Reset Source: mod_g_srst_n
15:0	CLRFAL2	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 2 bits. Reset Source: mod_g_srst_n

4.17.23 MEM_INTSTAT23 Registers

4.17.23.1 MEM_INTSTAT23 Register (Offset = 5Ch) [reset = 0h]

Short Description: Bank Interrupt Status Reg

Long Description: Bank Interrupt Status Register

Return to Summary Table

Table 4-1769. Instance Table

Instance Name	Physical Address
GPIO0	5200 005Ch
GPIO1	5200 105Ch
GPIO2	5200 205Ch
GPIO3	5200 305Ch

Figure 4-798. INTSTAT23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STAT3															
R/W1TC															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STAT2															
R/W1TC															
0h															

Access Types Legend

Table 4-1770. INTSTAT23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	STAT3	R/W1TC	0h	Status of GPIO bank 3 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n
15:0	STAT2	R/W1TC	0h	Status of GPIO bank 2 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n

4.17.24 MEM_DIR45 Registers

4.17.24.1 MEM_DIR45 Register (Offset = 60h) [reset = ffffffffh]

Short Description: Direction Register

Long Description: Direction Register

Return to Summary Table

Table 4-1771. Instance Table

Instance Name	Physical Address
GPIO0	5200 0060h
GPIO1	5200 1060h
GPIO2	5200 2060h
GPIO3	5200 3060h

Figure 4-799. DIR45 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DIR5															
R/W															
ffffh															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIR4															
R/W															
ffffh															

Access Types Legend

Table 4-1772. DIR45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DIR5	R/W	FFFFh	Direction of GPIO bank 5 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n
15:0	DIR4	R/W	FFFFh	Direction of GPIO bank 4 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n

4.17.25 MEM_OUT_DATA45 Registers

4.17.25.1 MEM_DATA45 Register (Offset = 64h) [reset = 0h]

Short Description: Output Drive State Regist

Long Description: Output Drive State Register

Return to Summary Table

Table 4-1773. Instance Table

Instance Name	Physical Address
GPIO0	5200 0064h
GPIO1	5200 1064h
GPIO2	5200 2064h
GPIO3	5200 3064h

Figure 4-800. OUT_DATA45 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUT5															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUT4															
R/W															
0h															

Access Types Legend

Table 4-1774. OUT_DATA45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	OUT5	R/W	0h	Output drive state of GPIO bank 5 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	OUT4	R/W	0h	Output drive state of GPIO bank 4 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n

4.17.26 MEM_SET_DATA45 Registers

4.17.26.1 MEM_DATA45 Register (Offset = 68h) [reset = 0h]

Short Description: Set Output Drive State Re

Long Description: Set Output Drive State Register

Return to Summary Table

Table 4-1775. Instance Table

Instance Name	Physical Address
GPIO0	5200 0068h
GPIO1	5200 1068h
GPIO2	5200 2068h
GPIO3	5200 3068h

Figure 4-801. SET_DATA45 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SET5															
R/W1TS															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SET4															
R/W1TS															
0h															

Access Types Legend

Table 4-1776. SET_DATA45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SET5	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 5 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	SET4	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 4 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n

4.17.27 MEM_CLR_DATA45 Registers

4.17.27.1 MEM_DATA45 Register (Offset = 6Ch) [reset = 0h]

Short Description: Clear Output Drive State

Long Description: Clear Output Drive State Register

Return to Summary Table

Table 4-1777. Instance Table

Instance Name	Physical Address
GPIO0	5200 006Ch
GPIO1	5200 106Ch
GPIO2	5200 206Ch
GPIO3	5200 306Ch

Figure 4-802. CLR_DATA45 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLR5															
R/W1TC															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR4															
R/W1TC															
0h															

Access Types Legend

Table 4-1778. CLR_DATA45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLR5	R/W1TC	0h	Writing 1 clears the output drive state of GPIO bank 5. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	CLR4	R/W1TC	0h	Writing 1 clears the output drive state of GPIO bank 4. Reading it returns the output drive state. Reset Source: mod_g_srst_n

4.17.28 MEM_IN_DATA45 Registers

4.17.28.1 MEM_DATA45 Register (Offset = 70h) [reset = 0h]

Short Description: Bank Status Register

Long Description: Bank Status Register

Return to Summary Table

Table 4-1779. Instance Table

Instance Name	Physical Address
GPIO0	5200 0070h
GPIO1	5200 1070h
GPIO2	5200 2070h
GPIO3	5200 3070h

Figure 4-803. IN_DATA45 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IN5															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IN4															
R															
0h															

Access Types Legend

Table 4-1780. IN_DATA45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IN5	R	0h	Status of GPIO bank 5 bits. Reset Source: mod_g_srst_n
15:0	IN4	R	0h	Status of GPIO bank 4 bits. Reset Source: mod_g_srst_n

4.17.29 MEM_SET_RIS_TRIG45 Registers

4.17.29.1 MEM_RIS_TRIG45 Register (Offset = 74h) [reset = 0h]

Short Description: Set Rising Edge Detection

Long Description: Set Rising Edge Detection Register

Return to Summary Table

Table 4-1781. Instance Table

Instance Name	Physical Address
GPIO0	5200 0074h
GPIO1	5200 1074h
GPIO2	5200 2074h
GPIO3	5200 3074h

Figure 4-804. SET_RIS_TRIG45 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SETRIS5															
R/W1TS															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETRIS4															
R/W1TS															
0h															

Access Types Legend

Table 4-1782. SET_RIS_TRIG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETRIS5	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 5 bits. Reset Source: mod_g_srst_n
15:0	SETRIS4	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 4 bits. Reset Source: mod_g_srst_n

4.17.30 MEM_CLR_RIS_TRIG45 Registers

4.17.30.1 MEM_RIS_TRIG45 Register (Offset = 78h) [reset = 0h]

Short Description: Clear Rising Edge Detecti

Long Description: Clear Rising Edge Detection Register

Return to Summary Table

Table 4-1783. Instance Table

Instance Name	Physical Address
GPIO0	5200 0078h
GPIO1	5200 1078h
GPIO2	5200 2078h
GPIO3	5200 3078h

Figure 4-805. CLR_RIS_TRIG45 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLRRIS5															
R/W1TC															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRRIS4															
R/W1TC															
0h															

Access Types Legend

Table 4-1784. CLR_RIS_TRIG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRRIS5	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 5 bits. Reset Source: mod_g_srst_n
15:0	CLRRIS4	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 4 bits. Reset Source: mod_g_srst_n

4.17.31 MEM_SET_FAL_TRIG45 Registers

4.17.31.1 MEM_FAL_TRIG45 Register (Offset = 7Ch) [reset = 0h]

Short Description: Set Falling Edge Detectio

Long Description: Set Falling Edge Detection Register

Return to Summary Table

Table 4-1785. Instance Table

Instance Name	Physical Address
GPIO0	5200 007Ch
GPIO1	5200 107Ch
GPIO2	5200 207Ch
GPIO3	5200 307Ch

Figure 4-806. SET_FAL_TRIG45 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SETFAL5															
R/W1TS															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETFAL4															
R/W1TS															
0h															

Access Types Legend

Table 4-1786. SET_FAL_TRIG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETFAL5	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 5 bits. Reset Source: mod_g_srst_n
15:0	SETFAL4	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 4 bits. Reset Source: mod_g_srst_n

4.17.32 MEM_CLR_FAL_TRIG45 Registers

4.17.32.1 MEM_FAL_TRIG45 Register (Offset = 80h) [reset = 0h]

Short Description: Clear Falling Edge Detect

Long Description: Clear Falling Edge Detection Register

Return to Summary Table

Table 4-1787. Instance Table

Instance Name	Physical Address
GPIO0	5200 0080h
GPIO1	5200 1080h
GPIO2	5200 2080h
GPIO3	5200 3080h

Figure 4-807. CLR_FAL_TRIG45 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLRFAL5															
R/W1TC															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRFAL4															
R/W1TC															
0h															

Access Types Legend

Table 4-1788. CLR_FAL_TRIG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRFAL5	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 5 bits. Reset Source: mod_g_srst_n
15:0	CLRFAL4	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 4 bits. Reset Source: mod_g_srst_n

4.17.33 MEM_INTSTAT45 Registers

4.17.33.1 MEM_INTSTAT45 Register (Offset = 84h) [reset = 0h]

Short Description: Bank Interrupt Status Reg

Long Description: Bank Interrupt Status Register

Return to Summary Table

Table 4-1789. Instance Table

Instance Name	Physical Address
GPIO0	5200 0084h
GPIO1	5200 1084h
GPIO2	5200 2084h
GPIO3	5200 3084h

Figure 4-808. INTSTAT45 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STAT5															
R/W1TC															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STAT4															
R/W1TC															
0h															

Access Types Legend

Table 4-1790. INTSTAT45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	STAT5	R/W1TC	0h	Status of GPIO bank 5 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n
15:0	STAT4	R/W1TC	0h	Status of GPIO bank 4 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n

4.17.34 MEM_DIR67 Registers

4.17.34.1 MEM_DIR67 Register (Offset = 88h) [reset = ffffffffh]

Short Description: Direction Register

Long Description: Direction Register

Return to Summary Table

Table 4-1791. Instance Table

Instance Name	Physical Address
GPIO0	5200 0088h
GPIO1	5200 1088h
GPIO2	5200 2088h
GPIO3	5200 3088h

Figure 4-809. DIR67 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DIR7															
R/W															
ffffh															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIR6															
R/W															
ffffh															

Access Types Legend

Table 4-1792. DIR67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DIR7	R/W	FFFFh	Direction of GPIO bank 7 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n
15:0	DIR6	R/W	FFFFh	Direction of GPIO bank 6 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n

4.17.35 MEM_OUT_DATA67 Registers

4.17.35.1 MEM_DATA67 Register (Offset = 8Ch) [reset = 0h]

Short Description: Output Drive State Regist

Long Description: Output Drive State Register

Return to Summary Table

Table 4-1793. Instance Table

Instance Name	Physical Address
GPIO0	5200 008Ch
GPIO1	5200 108Ch
GPIO2	5200 208Ch
GPIO3	5200 308Ch

Figure 4-810. OUT_DATA67 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUT7															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUT6															
R/W															
0h															

Access Types Legend

Table 4-1794. OUT_DATA67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	OUT7	R/W	0h	Output drive state of GPIO bank 7 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	OUT6	R/W	0h	Output drive state of GPIO bank 6 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n

4.17.36 MEM_SET_DATA67 Registers

4.17.36.1 MEM_DATA67 Register (Offset = 90h) [reset = 0h]

Short Description: Set Output Drive State Re

Long Description: Set Output Drive State Register

Return to Summary Table

Table 4-1795. Instance Table

Instance Name	Physical Address
GPIO0	5200 0090h
GPIO1	5200 1090h
GPIO2	5200 2090h
GPIO3	5200 3090h

Figure 4-811. SET_DATA67 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SET7															
R/W1TS															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SET6															
R/W1TS															
0h															

Access Types Legend

Table 4-1796. SET_DATA67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SET7	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 7 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	SET6	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 6 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n

4.17.37 MEM_CLR_DATA67 Registers

4.17.37.1 MEM_DATA67 Register (Offset = 94h) [reset = 0h]

Short Description: Clear Output Drive State

Long Description: Clear Output Drive State Register

Return to Summary Table

Table 4-1797. Instance Table

Instance Name	Physical Address
GPIO0	5200 0094h
GPIO1	5200 1094h
GPIO2	5200 2094h
GPIO3	5200 3094h

Figure 4-812. CLR_DATA67 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLR7															
R/W1TC															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR6															
R/W1TC															
0h															

Access Types Legend

Table 4-1798. CLR_DATA67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLR7	R/W1TC	0h	Writing 1 clears the output drive state of GPIO bank 7. Reading it returns the output drive state. Reset Source: mod_g_srst_n
15:0	CLR6	R/W1TC	0h	Writing 1 clears the output drive state of GPIO bank 6. Reading it returns the output drive state. Reset Source: mod_g_srst_n

4.17.38 MEM_IN_DATA67 Registers

4.17.38.1 MEM_DATA67 Register (Offset = 98h) [reset = 0h]

Short Description: Bank Status Register

Long Description: Bank Status Register

Return to Summary Table

Table 4-1799. Instance Table

Instance Name	Physical Address
GPIO0	5200 0098h
GPIO1	5200 1098h
GPIO2	5200 2098h
GPIO3	5200 3098h

Figure 4-813. IN_DATA67 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IN7															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IN6															
R															
0h															

Access Types Legend

Table 4-1800. IN_DATA67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IN7	R	0h	Status of GPIO bank 7 bits. Reset Source: mod_g_srst_n
15:0	IN6	R	0h	Status of GPIO bank 6 bits. Reset Source: mod_g_srst_n

4.17.39 MEM_SET_RIS_TRIG67 Registers

4.17.39.1 MEM_RIS_TRIG67 Register (Offset = 9Ch) [reset = 0h]

Short Description: Set Rising Edge Detection

Long Description: Set Rising Edge Detection Register

Return to Summary Table

Table 4-1801. Instance Table

Instance Name	Physical Address
GPIO0	5200 009Ch
GPIO1	5200 109Ch
GPIO2	5200 209Ch
GPIO3	5200 309Ch

Figure 4-814. SET_RIS_TRIG67 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SETRIS7															
R/W1TS															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETRIS6															
R/W1TS															
0h															

Access Types Legend

Table 4-1802. SET_RIS_TRIG67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETRIS7	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 7 bits. Reset Source: mod_g_srst_n
15:0	SETRIS6	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 6 bits. Reset Source: mod_g_srst_n

4.17.40 MEM_CLR_RIS_TRIG67 Registers

4.17.40.1 MEM_RIS_TRIG67 Register (Offset = A0h) [reset = 0h]

Short Description: Clear Rising Edge Detecti

Long Description: Clear Rising Edge Detection Register

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Table 4-1803. Instance Table

Instance Name	Physical Address
GPIO0	5200 00A0h
GPIO1	5200 10A0h
GPIO2	5200 20A0h
GPIO3	5200 30A0h

Figure 4-815. CLR_RIS_TRIG67 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLRRIS7															
R/W1TC															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRRIS6															
R/W1TC															
0h															

Access Types Legend

Table 4-1804. CLR_RIS_TRIG67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRRIS7	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 7 bits. Reset Source: mod_g_srst_n
15:0	CLRRIS6	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 6 bits. Reset Source: mod_g_srst_n

4.17.41 MEM_SET_FAL_TRIG67 Registers

4.17.41.1 MEM_FAL_TRIG67 Register (Offset = A4h) [reset = 0h]

Short Description: Set Falling Edge Detectio

Long Description: Set Falling Edge Detection Register

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Table 4-1805. Instance Table

Instance Name	Physical Address
GPIO0	5200 00A4h
GPIO1	5200 10A4h
GPIO2	5200 20A4h
GPIO3	5200 30A4h

Figure 4-816. SET_FAL_TRIG67 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SETFAL7															
R/W1TS															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETFAL6															
R/W1TS															
0h															

Access Types Legend

Table 4-1806. SET_FAL_TRIG67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETFAL7	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 7 bits. Reset Source: mod_g_srst_n
15:0	SETFAL6	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 6 bits. Reset Source: mod_g_srst_n

4.17.42 MEM_CLR_FAL_TRIG67 Registers

4.17.42.1 MEM_FAL_TRIG67 Register (Offset = A8h) [reset = 0h]

Short Description: Clear Falling Edge Detect

Long Description: Clear Falling Edge Detection Register

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Table 4-1807. Instance Table

Instance Name	Physical Address
GPIO0	5200 00A8h
GPIO1	5200 10A8h
GPIO2	5200 20A8h
GPIO3	5200 30A8h

Figure 4-817. CLR_FAL_TRIG67 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLRFAL7															
R/W1TC															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRFAL6															
R/W1TC															
0h															

Access Types Legend

Table 4-1808. CLR_FAL_TRIG67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRFAL7	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 7 bits. Reset Source: mod_g_srst_n
15:0	CLRFAL6	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 6 bits. Reset Source: mod_g_srst_n

4.17.43 MEM_INTSTAT67 Registers

4.17.43.1 MEM_INTSTAT67 Register (Offset = ACh) [reset = 0h]

Short Description: Bank Interrupt Status Reg

Long Description: Bank Interrupt Status Register

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Table 4-1809. Instance Table

Instance Name	Physical Address
GPIO0	5200 00ACh
GPIO1	5200 10ACh
GPIO2	5200 20ACh
GPIO3	5200 30ACh

Figure 4-818. INTSTAT67 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STAT7															
R/W1TC															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STAT6															
R/W1TC															
0h															

Access Types Legend

Table 4-1810. INTSTAT67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	STAT7	R/W1TC	0h	Status of GPIO bank 7 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n
15:0	STAT6	R/W1TC	0h	Status of GPIO bank 6 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n

4.17.44 MEM_DIR8 Registers

4.17.44.1 MEM_DIR8 Register (Offset = B0h) [reset = ffffffffh]

Short Description: Direction Register

Long Description: Direction Register

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Table 4-1811. Instance Table

Instance Name	Physical Address
GPIO0	5200 00B0h
GPIO1	5200 10B0h
GPIO2	5200 20B0h
GPIO3	5200 30B0h

Figure 4-819. DIR8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R															
ffffh															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIR8															
R/W															
ffffh															

Access Types Legend

Table 4-1812. DIR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R		RESERVED Reset Source: mod_g_srst_n
15:0	DIR8	R/W	FFFFh	Direction of GPIO bank 8 bits, 0 = output, 1 = input. Reset Source: mod_g_srst_n

4.17.45 MEM_OUT_DATA8 Registers

4.17.45.1 MEM_DATA8 Register (Offset = B4h) [reset = 0h]

Short Description: Output Drive State Regist

Long Description: Output Drive State Register

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Table 4-1813. Instance Table

Instance Name	Physical Address
GPIO0	5200 00B4h
GPIO1	5200 10B4h
GPIO2	5200 20B4h
GPIO3	5200 30B4h

Figure 4-820. OUT_DATA8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUT8															
R/W															
0h															

Access Types Legend

Table 4-1814. OUT_DATA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R		RESERVED Reset Source: mod_g_srst_n
15:0	OUT8	R/W	0h	Output drive state of GPIO bank 8 bits, does not affect operation when it is configured as input. Reading it returns the output drive state. Reset Source: mod_g_srst_n

4.17.46 MEM_SET_DATA8 Registers

4.17.46.1 MEM_DATA8 Register (Offset = B8h) [reset = 0h]

Short Description: Set Output Drive State Re

Long Description: Set Output Drive State Register

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Table 4-1815. Instance Table

Instance Name	Physical Address
GPIO0	5200 00B8h
GPIO1	5200 10B8h
GPIO2	5200 20B8h
GPIO3	5200 30B8h

Figure 4-821. SET_DATA8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SET8															
R/W1TS															
0h															

Access Types Legend

Table 4-1816. SET_DATA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R		RESERVED Reset Source: mod_g_srst_n
15:0	SET8	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 8 bits. Reading it returns the output drive state. Reset Source: mod_g_srst_n

4.17.47 MEM_CLR_DATA8 Registers

4.17.47.1 MEM_DATA8 Register (Offset = BCh) [reset = 0h]

Short Description: Clear Output Drive State

Long Description: Clear Output Drive State Register

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Table 4-1817. Instance Table

Instance Name	Physical Address
GPIO0	5200 00BCh
GPIO1	5200 10BCh
GPIO2	5200 20BCh
GPIO3	5200 30BCh

Figure 4-822. CLR_DATA8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR8															
R/W1TC															
0h															

Access Types Legend

Table 4-1818. CLR_DATA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R		RESERVED Reset Source: mod_g_srst_n
15:0	CLR8	R/W1TC	0h	Writing 1 clears the output drive state of GPIO bank 8. Reading it returns the output drive state. Reset Source: mod_g_srst_n

4.17.48 MEM_IN_DATA8 Registers

4.17.48.1 MEM_DATA8 Register (Offset = C0h) [reset = 0h]

Short Description: Bank Status Register

Long Description: Bank Status Register

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Table 4-1819. Instance Table

Instance Name	Physical Address
GPIO0	5200 00C0h
GPIO1	5200 10C0h
GPIO2	5200 20C0h
GPIO3	5200 30C0h

Figure 4-823. IN_DATA8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IN8															
R															
0h															

Access Types Legend

Table 4-1820. IN_DATA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R		RESERVED Reset Source: mod_g_srst_n
15:0	IN8	R	0h	Status of GPIO bank 8 bits. Reset Source: mod_g_srst_n

4.17.49 MEM_SET_RIS_TRIG8 Registers

4.17.49.1 MEM_RIS_TRIG8 Register (Offset = C4h) [reset = 0h]

Short Description: Set Rising Edge Detection

Long Description: Set Rising Edge Detection Register

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Table 4-1821. Instance Table

Instance Name	Physical Address
GPIO0	5200 00C4h
GPIO1	5200 10C4h
GPIO2	5200 20C4h
GPIO3	5200 30C4h

Figure 4-824. SET_RIS_TRIG8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETRIS8															
R/W1TS															
0h															

Access Types Legend

Table 4-1822. SET_RIS_TRIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	SETRIS8	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 8 bits. Reset Source: mod_g_srst_n

4.17.50 MEM_CLR_RIS_TRIG8 Registers

4.17.50.1 MEM_RIS_TRIG8 Register (Offset = C8h) [reset = 0h]

Short Description: Clear Rising Edge Detecti

Long Description: Clear Rising Edge Detection Register

Return to Summary Table

Table 4-1823. Instance Table

Instance Name	Physical Address
GPIO0	5200 00C8h
GPIO1	5200 10C8h
GPIO2	5200 20C8h
GPIO3	5200 30C8h

Figure 4-825. CLR_RIS_TRIG8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRRIS8															
R/W1TC															
0h															

Access Types Legend

Table 4-1824. CLR_RIS_TRIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	CLRRIS8	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 8 bits. Reset Source: mod_g_srst_n

4.17.51 MEM_SET_FAL_TRIG8 Registers

4.17.51.1 MEM_FAL_TRIG8 Register (Offset = CCh) [reset = 0h]

Short Description: Set Falling Edge Detectio

Long Description: Set Falling Edge Detection Register

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Table 4-1825. Instance Table

Instance Name	Physical Address
GPIO0	5200 00CCh
GPIO1	5200 10CCh
GPIO2	5200 20CCh
GPIO3	5200 30CCh

Figure 4-826. SET_FAL_TRIG8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETFAL8															
R/W1TS															
0h															

Access Types Legend

Table 4-1826. SET_FAL_TRIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	SETFAL8	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 8 bits. Reset Source: mod_g_srst_n

4.17.52 MEM_CLR_FAL_TRIG8 Registers

4.17.52.1 MEM_FAL_TRIG8 Register (Offset = D0h) [reset = 0h]

Short Description: Clear Falling Edge Detect

Long Description: Clear Falling Edge Detection Register

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Table 4-1827. Instance Table

Instance Name	Physical Address
GPIO0	5200 00D0h
GPIO1	5200 10D0h
GPIO2	5200 20D0h
GPIO3	5200 30D0h

Figure 4-827. CLR_FAL_TRIG8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRFAL8															
R/W1TC															
0h															

Access Types Legend

Table 4-1828. CLR_FAL_TRIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	CLRFAL8	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 8 bits. Reset Source: mod_g_srst_n

4.17.53 MEM_INTSTAT8 Registers

4.17.53.1 MEM_INTSTAT8 Register (Offset = D4h) [reset = 0h]

Short Description: Bank Interrupt Status Reg

Long Description: Bank Interrupt Status Register

Return to Summary Table

Table 4-1829. Instance Table

Instance Name	Physical Address
GPIO0	5200 00D4h
GPIO1	5200 10D4h
GPIO2	5200 20D4h
GPIO3	5200 30D4h

Figure 4-828. INTSTAT8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STAT8															
R/W1TC															
0h															

Access Types Legend

Table 4-1830. INTSTAT8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R		RESERVED Reset Source: mod_g_srst_n
15:0	STAT8	R/W1TC	0h	Status of GPIO bank 8 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. Reset Source: mod_g_srst_n

4.17.54 Access Table

Table 4-1831. Access Type Codes

Access Type	Code	Description
R	R	Read
R/W	R/W	Read / Write
R/W1TS	R/W1TS	Read/Write 1 To Set
R/W1TC	R/W1TC	Read/Write 1 To Clear

4.18 CPSW Registers

Table 4-1832. CPSW_NCSS_VBUSP, CPSW_NCSS_VBUSP Registers, Base Address=0X0000000052800000, Length=2097152

Offset	Length	Register Name	CPSW Physical Address
F14h	32	MDIO_MDIO_LINK_INT_MASKED_REG	5280 0F14h
F18h	32	MDIO_MDIO_LINK_INT_MASK_SET_REG	5280 0F18h
F1Ch	32	MDIO_MDIO_LINK_INT_MASK_CLEAR_REG	5280 0F1Ch
F20h	32	MDIO_MDIO_USER_INT_RAW_REG	5280 0F20h
F24h	32	MDIO_MDIO_USER_INT_MASKED_REG	5280 0F24h
F28h	32	MDIO_MDIO_USER_INT_MASK_SET_REG	5280 0F28h
F2Ch	32	MDIO_MDIO_USER_INT_MASK_CLEAR_REG	5280 0F2Ch
F30h	32	MDIO_MDIO_MANUAL_IF_REG	5280 0F30h
F34h	32	MDIO_MDIO_POLL_REG	5280 0F34h
F38h	32	MDIO_MDIO_POLL_EN_REG	5280 0F38h
F3Ch	32	MDIO_MDIO_CLAUS45_REG	5280 0F3Ch
F40h	32	MDIO_MDIO_USER_ADDR0_REG	5280 0F40h
F44h	32	MDIO_MDIO_USER_ADDR1_REG	5280 0F44h
F80h + Formula	32	MDIO_MDIO_USER_GROUP_USER_ACCESS_REG_j	5280 0F80h + Formula
F84h + Formula	32	MDIO_MDIO_USER_GROUP_USER_PHY_SEL_REG_j	5280 0F84h + Formula
1800h	32	REGS_INT_REGS_INT_SS_C0_TH_THRESH_PULSE_EN_REG	5280 1800h
1804h	32	REGS_INT_REGS_INT_SS_C0_TH_PULSE_EN_REG	5280 1804h
1808h	32	REGS_INT_REGS_INT_SS_C0_FH_PULSE_EN_REG	5280 1808h
180Ch	32	REGS_INT_REGS_INT_SS_C0_MISC_EN_REG	5280 180Ch
1810h	32	REGS_INT_REGS_INT_SS_C0_TH_THRESH_PULSE_STATUS_REG	5280 1810h
1814h	32	REGS_INT_REGS_INT_SS_C0_TH_PULSE_STATUS_REG	5280 1814h
1818h	32	REGS_INT_REGS_INT_SS_C0_FH_PULSE_STATUS_REG	5280 1818h
181Ch	32	REGS_INT_REGS_INT_SS_C0_MISC_STATUS_REG	5280 181Ch
1820h	32	REGS_INT_REGS_INT_SS_C0_TH_IMAX_REG	5280 1820h
1824h	32	REGS_INT_REGS_INT_SS_C0_FH_IMAX_REG	5280 1824h
1840h	32	REGS_INT_REGS_INT_SS_C1_TH_THRESH_PULSE_EN_REG	5280 1840h
1844h	32	REGS_INT_REGS_INT_SS_C1_TH_PULSE_EN_REG	5280 1844h
1848h	32	REGS_INT_REGS_INT_SS_C1_FH_PULSE_EN_REG	5280 1848h
184Ch	32	REGS_INT_REGS_INT_SS_C1_MISC_EN_REG	5280 184Ch
1850h	32	REGS_INT_REGS_INT_SS_C1_TH_THRESH_PULSE_STATUS_REG	5280 1850h
1854h	32	REGS_INT_REGS_INT_SS_C1_TH_PULSE_STATUS_REG	5280 1854h
1858h	32	REGS_INT_REGS_INT_SS_C1_FH_PULSE_STATUS_REG	5280 1858h
185Ch	32	REGS_INT_REGS_INT_SS_C1_MISC_STATUS_REG	5280 185Ch
1860h	32	REGS_INT_REGS_INT_SS_C1_TH_IMAX_REG	5280 1860h
1864h	32	REGS_INT_REGS_INT_SS_C1_FH_IMAX_REG	5280 1864h
1880h	32	REGS_INT_REGS_INT_SS_C2_TH_THRESH_PULSE_EN_REG	5280 1880h

Table 4-1832. CPSW_NCSS_VBUSP, CPSW_NCSS_VBUSP Registers, Base Address=0X0000000052800000, Length=2097152 (continued)

Offset	Length	Register Name	CPSW Physical Address
1884h	32	REGS_INT_REGS_INT_SS_C2_TH_PULSE_EN_REG	5280 1884h
1888h	32	REGS_INT_REGS_INT_SS_C2_FH_PULSE_EN_REG	5280 1888h
188Ch	32	REGS_INT_REGS_INT_SS_C2_MISC_EN_REG	5280 188Ch
1890h	32	REGS_INT_REGS_INT_SS_C2_TH_THRESH_PULSE_STATUS_REG	5280 1890h
1894h	32	REGS_INT_REGS_INT_SS_C2_TH_PULSE_STATUS_REG	5280 1894h
1898h	32	REGS_INT_REGS_INT_SS_C2_FH_PULSE_STATUS_REG	5280 1898h
189Ch	32	REGS_INT_REGS_INT_SS_C2_MISC_STATUS_REG	5280 189Ch
18A0h	32	REGS_INT_REGS_INT_SS_C2_TH_IMAX_REG	5280 18A0h
18A4h	32	REGS_INT_REGS_INT_SS_C2_FH_IMAX_REG	5280 18A4h
18C0h	32	REGS_INT_REGS_INT_SS_C3_TH_THRESH_PULSE_EN_REG	5280 18C0h
18C4h	32	REGS_INT_REGS_INT_SS_C3_TH_PULSE_EN_REG	5280 18C4h
18C8h	32	REGS_INT_REGS_INT_SS_C3_FH_PULSE_EN_REG	5280 18C8h
18CCh	32	REGS_INT_REGS_INT_SS_C3_MISC_EN_REG	5280 18CCh
18D0h	32	REGS_INT_REGS_INT_SS_C3_TH_THRESH_PULSE_STATUS_REG	5280 18D0h
18D4h	32	REGS_INT_REGS_INT_SS_C3_TH_PULSE_STATUS_REG	5280 18D4h
18D8h	32	REGS_INT_REGS_INT_SS_C3_FH_PULSE_STATUS_REG	5280 18D8h
18DCh	32	REGS_INT_REGS_INT_SS_C3_MISC_STATUS_REG	5280 18DCh
18E0h	32	REGS_INT_REGS_INT_SS_C3_TH_IMAX_REG	5280 18E0h
18E4h	32	REGS_INT_REGS_INT_SS_C3_FH_IMAX_REG	5280 18E4h
20000h	32	CPSW_NC_CPSW_NC_CPSW_ID_VER_REG	5282 0000h
20004h	32	CPSW_NC_CPSW_NC_CONTROL_REG	5282 0004h
20010h	32	CPSW_NC_CPSW_NC_EM_CONTROL_REG	5282 0010h
20014h	32	CPSW_NC_CPSW_NC_STAT_PORT_EN_REG	5282 0014h
20018h	32	CPSW_NC_CPSW_NC_PTYPE_REG	5282 0018h
2001Ch	32	CPSW_NC_CPSW_NC_SOFT_IDLE_REG	5282 001Ch
20020h	32	CPSW_NC_CPSW_NC_THRU_RATE_REG	5282 0020h
20024h	32	CPSW_NC_CPSW_NC_GAP_THRESH_REG	5282 0024h
20028h	32	CPSW_NC_CPSW_NC_TX_START_WDS_REG	5282 0028h
2002Ch	32	CPSW_NC_CPSW_NC_EEE_PRESCALE_REG	5282 002Ch
20030h	32	CPSW_NC_CPSW_NC_TX_G_OFLOW_THRESH_SET_REG	5282 0030h
20034h	32	CPSW_NC_CPSW_NC_TX_G_OFLOW_THRESH_CLR_REG	5282 0034h
20038h	32	CPSW_NC_CPSW_NC_TX_G_BUF_THRESH_SET_L_REG	5282 0038h
2003Ch	32	CPSW_NC_CPSW_NC_TX_G_BUF_THRESH_SET_H_REG	5282 003Ch
20040h	32	CPSW_NC_CPSW_NC_TX_G_BUF_THRESH_CLR_L_REG	5282 0040h
20044h	32	CPSW_NC_CPSW_NC_TX_G_BUF_THRESH_CLR_H_REG	5282 0044h
20050h	32	CPSW_NC_CPSW_NC_VLAN_LTYPE_REG	5282 0050h
20054h	32	CPSW_NC_CPSW_NC_EST_TS_DOMAIN_REG	5282 0054h

Table 4-1832. CPSW_NCSS_VBUSP, CPSW_NCSS_VBUSP Registers, Base Address=0X0000000052800000, Length=2097152 (continued)

Offset	Length	Register Name	CPSW Physical Address
20100h	32	CPSW_NC_CPSW_NC_TX_PRI0_MAXLEN_REG	5282 0100h
20104h	32	CPSW_NC_CPSW_NC_TX_PRI1_MAXLEN_REG	5282 0104h
20108h	32	CPSW_NC_CPSW_NC_TX_PRI2_MAXLEN_REG	5282 0108h
2010Ch	32	CPSW_NC_CPSW_NC_TX_PRI3_MAXLEN_REG	5282 010Ch
20110h	32	CPSW_NC_CPSW_NC_TX_PRI4_MAXLEN_REG	5282 0110h
20114h	32	CPSW_NC_CPSW_NC_TX_PRI5_MAXLEN_REG	5282 0114h
20118h	32	CPSW_NC_CPSW_NC_TX_PRI6_MAXLEN_REG	5282 0118h
2011Ch	32	CPSW_NC_CPSW_NC_TX_PRI7_MAXLEN_REG	5282 011Ch
21004h	32	CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_CONTROL_REG	5282 1004h
21008h	32	CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_FLOW_ID_OFFSET_REG	5282 1008h
21010h	32	CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_BLK_CNT_REG	5282 1010h
21014h	32	CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_PORT_VLAN_REG	5282 1014h
21018h	32	CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_PRI_MAP_REG	5282 1018h
2101Ch	32	CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_PRI_CTL_REG	5282 101Ch
21020h	32	CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_RX_PRI_MAP_REG	5282 1020h
21024h	32	CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_RX_MAXLEN_REG	5282 1024h
21028h	32	CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_BLKS_PRI_REG	5282 1028h
21030h	32	CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_IDLE2LPI_REG	5282 1030h
21034h	32	CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_LPI2WAKE_REG	5282 1034h
21038h	32	CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_EEE_STATUS_REG	5282 1038h
21050h	32	CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_FIFO_STATUS_REG	5282 1050h
21120h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_RX_DSCP_MAP_REG_N	5282 1120h + Formula
21140h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_PRI_CIR_REG_N	5282 1140h + Formula
21160h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_PRI_EIR_REG_N	5282 1160h + Formula
21180h	32	CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_D_THRESH_SET_L_REG	5282 1180h
21184h	32	CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_D_THRESH_SET_H_REG	5282 1184h
21188h	32	CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_D_THRESH_CLR_L_REG	5282 1188h
2118Ch	32	CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_D_THRESH_CLR_H_REG	5282 118Ch
21190h	32	CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_G_BUF_THRESH_SET_L_REG	5282 1190h
21194h	32	CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_G_BUF_THRESH_SET_H_REG	5282 1194h

Table 4-1832. CPSW_NCSS_VBUSP, CPSW_NCSS_VBUSP Registers, Base Address=0X0000000052800000, Length=2097152 (continued)

Offset	Length	Register Name	CPSW Physical Address
21198h	32	CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_G_BUF_THRESH_CLR_L_REG	5282 1198h
2119Ch	32	CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_G_BUF_THRESH_CLR_H_REG	5282 119Ch
21300h	32	CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_SRC_ID_A_REG	5282 1300h
21304h	32	CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_SRC_ID_B_REG	5282 1304h
21320h	32	CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_HOST_BLKS_PRI_REG	5282 1320h
22000h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_RESERVED_REG	5282 2000h
22004h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_CONTROL_REG	5282 2004h
22008h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAX_BLKS_REG	5282 2008h
22010h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_BLK_CNT_REG	5282 2010h
22014h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_PORT_VLAN_REG	5282 2014h
22018h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_PRI_MAP_REG	5282 2018h
2201Ch	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_PRI_CTL_REG	5282 201Ch
22020h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_RX_PRI_MAP_REG	5282 2020h
22024h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_RX_MAXLEN_REG	5282 2024h
22028h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_BLKS_PRI_REG	5282 2028h
22030h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_IDLE2LPI_REG	5282 2030h
22034h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_LPI2WAKE_REG	5282 2034h
22038h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_EEE_STATUS_REG	5282 2038h
22050h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_FIFO_STATUS_REG	5282 2050h
22060h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_EST_CONTROL_REG	5282 2060h
22120h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_RX_DSCP_MAP_REG_N	5282 2120h + Formula
22140h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_PRI_CIR_REG_N	5282 2140h + Formula
22160h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_PRI_EIR_REG_N	5282 2160h + Formula
22180h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_D_THRESH_SET_L_REG	5282 2180h
22184h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_D_THRESH_SET_H_REG	5282 2184h
22188h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_D_THRESH_CLR_L_REG	5282 2188h
2218Ch	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_D_THRESH_CLR_H_REG	5282 218Ch

Table 4-1832. CPSW_NCSS_VBUSP, CPSW_NCSS_VBUSP Registers, Base Address=0X0000000052800000, Length=2097152 (continued)

Offset	Length	Register Name	CPSW Physical Address
22190h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_L_REG	5282 2190h
22194h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_H_REG	5282 2194h
22198h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_L_REG	5282 2198h
2219Ch	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_H_REG	5282 219Ch
22300h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_L_REG	5282 2300h
22304h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_H_REG	5282 2304h
22308h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_SA_L_REG	5282 2308h
2230Ch	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_SA_H_REG	5282 230Ch
22310h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TS_CTL_REG	5282 2310h
22314h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TS_SEQ_LTYPE_REG	5282 2314h
22318h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TS_VLAN_LTYPE_REG	5282 2318h
2231Ch	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TS_CTL_LTYPE2_REG	5282 231Ch
22320h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TS_CTL2_REG	5282 2320h
22330h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_CONTROL_REG	5282 2330h
22334h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_STATUS_REG	5282 2334h
22338h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_SOFT_RESET_REG	5282 2338h
2233Ch	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_BOFFTEST_REG	5282 233Ch
22340h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_RX_PAUSETIMER_REG	5282 2340h
22350h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_RXN_PAUSETIMER_REG_N	5282 2350h + Formula
22370h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_TX_PAUSETIMER_REG	5282 2370h
22380h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_TXN_PAUSETIMER_REG_N	5282 2380h + Formula
223A0h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_EMCONTROL_REG	5282 23A0h
223A4h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_TX_GAP_REG	5282 23A4h
223A8h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_PORT_CONFIG	5282 23A8h
223ACh	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_INTERVLAN_OPX_POINTER_REG	5282 23ACh
223B0h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_INTERVLAN_OPX_A_REG	5282 23B0h
223B4h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_INTERVLAN_OPX_B_REG	5282 23B4h

Table 4-1832. CPSW_NCSS_VBUSP, CPSW_NCSS_VBUSP Registers, Base Address=0X0000000052800000, Length=2097152 (continued)

Offset	Length	Register Name	CPSW Physical Address
223B8h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_INTERVLAN_OPX_C_REG	5282 23B8h
223BCh	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_INTERVLAN_OPX_D_REG	5282 23BCh
23000h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_RESERVED_REG	5282 3000h
23004h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_CONTROL_REG	5282 3004h
23008h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAX_BLKS_REG	5282 3008h
23010h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_BLK_CNT_REG	5282 3010h
23014h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_PORT_VLAN_REG	5282 3014h
23018h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_PRI_MAP_REG	5282 3018h
2301Ch	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_PRI_CTL_REG	5282 301Ch
23020h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_RX_PRI_MAP_REG	5282 3020h
23024h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_RX_MAXLEN_REG	5282 3024h
23028h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_BLKS_PRI_REG	5282 3028h
23030h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_IDLE2LPI_REG	5282 3030h
23034h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_LPI2WAKE_REG	5282 3034h
23038h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_EEE_STATUS_REG	5282 3038h
23050h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_FIFO_STATUS_REG	5282 3050h
23060h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_EST_CONTROL_REG	5282 3060h
23120h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_RX_DSCP_MAP_REG_N	5282 3120h + Formula
23140h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_PRI_CIR_REG_N	5282 3140h + Formula
23160h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_PRI_EIR_REG_N	5282 3160h + Formula
23180h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_D_THRESH_SET_L_REG	5282 3180h
23184h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_D_THRESH_SET_H_REG	5282 3184h
23188h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_D_THRESH_CLR_L_REG	5282 3188h
2318Ch	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_D_THRESH_CLR_H_REG	5282 318Ch
23190h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_L_REG	5282 3190h
23194h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_H_REG	5282 3194h
23198h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_L_REG	5282 3198h

Table 4-1832. CPSW_NCSS_VBUSP, CPSW_NCSS_VBUSP Registers, Base Address=0X0000000052800000, Length=2097152 (continued)

Offset	Length	Register Name	CPSW Physical Address
2319Ch	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_H_REG	5282 319Ch
23300h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_L_REG	5282 3300h
23304h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_H_REG	5282 3304h
23308h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_SA_L_REG	5282 3308h
2330Ch	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_SA_H_REG	5282 330Ch
23310h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TS_CTL_REG	5282 3310h
23314h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TS_SEQ_LTYPE_REG	5282 3314h
23318h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TS_VLAN_LTYPE_REG	5282 3318h
2331Ch	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TS_CTL_LTYPE2_REG	5282 331Ch
23320h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TS_CTL2_REG	5282 3320h
23330h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_CONTROL_REG	5282 3330h
23334h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_STATUS_REG	5282 3334h
23338h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_SOFT_RESET_REG	5282 3338h
2333Ch	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_BOFFTEST_REG	5282 333Ch
23340h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_RX_PAUSETIMER_REG	5282 3340h
23350h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_RXN_PAUSETIMER_REG_N	5282 3350h + Formula
23370h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_TX_PAUSETIMER_REG	5282 3370h
23380h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_TXN_PAUSETIMER_REG_N	5282 3380h + Formula
233A0h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_EMCONTROL_REG	5282 33A0h
233A4h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_TX_GAP_REG	5282 33A4h
233A8h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_PORT_CONFIG	5282 33A8h
233ACh	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_INTERVLAN_OPX_POINTER_REG	5282 33ACh
233B0h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_INTERVLAN_OPX_A_REG	5282 33B0h
233B4h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_INTERVLAN_OPX_B_REG	5282 33B4h
233B8h	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_INTERVLAN_OPX_C_REG	5282 33B8h
233BCh	32	CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_INTERVLAN_OPX_D_REG	5282 33BCh
32000h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_EST_FETCH_LOC_N	5283 2000h + Formula

Table 4-1832. CPSW_NCSS_VBUSP, CPSW_NCSS_VBUSP Registers, Base Address=0X0000000052800000, Length=2097152 (continued)

Offset	Length	Register Name	CPSW Physical Address
34000h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_FH_IDVER_REG	5283 4000h
34004h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_FH_CONTROL_REG	5283 4004h
34008h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_FH_TEARDOWN_REG	5283 4008h
34010h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_TH_IDVER_REG	5283 4010h
34014h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_TH_CONTROL_REG	5283 4014h
34018h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_TH_TEARDOWN_REG	5283 4018h
3401Ch	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_SOFT_RESET_REG	5283 401Ch
34020h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_CONTROL_REG	5283 4020h
34024h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_STATUS_REG	5283 4024h
34028h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_TH_BUFFER_OFFSET_REG	5283 4028h
3402Ch	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_EMULATION_CONTROL_REG	5283 402Ch
34080h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_FH_INTSTAT_RAW_REG	5283 4080h
34084h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_FH_INTSTAT_MASKED_REG	5283 4084h
34088h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_FH_INTMASK_SET_REG	5283 4088h
3408Ch	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_FH_INTMASK_CLEAR_REG	5283 408Ch
34090h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_IN_VECTOR_REG	5283 4090h
34094h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_EOI_VECTOR_REG	5283 4094h
340A0h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH_INTSTAT_RAW_REG	5283 40A0h
340A4h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH_INTSTAT_MASKED_REG	5283 40A4h
340A8h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH_INTMASK_SET_REG	5283 40A8h
340ACh	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH_INTMASK_CLEAR_REG	5283 40ACh
340B0h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_INTSTAT_RAW_REG	5283 40B0h
340B4h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_INTSTAT_MASKED_REG	5283 40B4h
340B8h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_INTMASK_SET_REG	5283 40B8h
340BCh	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_INTMASK_CLEAR_REG	5283 40BCh
340C0h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH0_PENDTHRESH_REG	5283 40C0h
340C4h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH1_PENDTHRESH_REG	5283 40C4h

Table 4-1832. CPSW_NCSS_VBUSP, CPSW_NCSS_VBUSP Registers, Base Address=0X0000000052800000, Length=2097152 (continued)

Offset	Length	Register Name	CPSW Physical Address
340C8h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH2_PENDTHRESH_REG	5283 40C8h
340CCh	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH3_PENDTHRESH_REG	5283 40CCh
340D0h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH4_PENDTHRESH_REG	5283 40D0h
340D4h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH5_PENDTHRESH_REG	5283 40D4h
340D8h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH6_PENDTHRESH_REG	5283 40D8h
340DCh	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH7_PENDTHRESH_REG	5283 40DCh
340E0h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH0_FREEBUFFER_REG	5283 40E0h
340E4h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH1_FREEBUFFER_REG	5283 40E4h
340E8h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH2_FREEBUFFER_REG	5283 40E8h
340ECh	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH3_FREEBUFFER_REG	5283 40ECh
340F0h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH4_FREEBUFFER_REG	5283 40F0h
340F4h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH5_FREEBUFFER_REG	5283 40F4h
340F8h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH6_FREEBUFFER_REG	5283 40F8h
340FCh	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH7_FREEBUFFER_REG	5283 40FCh
34200h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH0_HDP_REG	5283 4200h
34204h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH1_HDP_REG	5283 4204h
34208h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH2_HDP_REG	5283 4208h
3420Ch	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH3_HDP_REG	5283 420Ch
34210h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH4_HDP_REG	5283 4210h
34214h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH5_HDP_REG	5283 4214h
34218h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH6_HDP_REG	5283 4218h
3421Ch	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH7_HDP_REG	5283 421Ch
34220h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH0_HDP_REG	5283 4220h
34224h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH1_HDP_REG	5283 4224h
34228h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH2_HDP_REG	5283 4228h
3422Ch	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH3_HDP_REG	5283 422Ch
34230h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH4_HDP_REG	5283 4230h

Table 4-1832. CPSW_NCSS_VBUSP, CPSW_NCSS_VBUSP Registers, Base Address=0X0000000052800000, Length=2097152 (continued)

Offset	Length	Register Name	CPSW Physical Address
34234h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH5_HDP_REG	5283 4234h
34238h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH6_HDP_REG	5283 4238h
3423Ch	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH7_HDP_REG	5283 423Ch
34240h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH0_CP_REG	5283 4240h
34244h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH1_CP_REG	5283 4244h
34248h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH2_CP_REG	5283 4248h
3424Ch	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH3_CP_REG	5283 424Ch
34250h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH4_CP_REG	5283 4250h
34254h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH5_CP_REG	5283 4254h
34258h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH6_CP_REG	5283 4258h
3425Ch	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH7_CP_REG	5283 425Ch
34260h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH0_CP_REG	5283 4260h
34264h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH1_CP_REG	5283 4264h
34268h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH2_CP_REG	5283 4268h
3426Ch	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH3_CP_REG	5283 426Ch
34270h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH4_CP_REG	5283 4270h
34274h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH5_CP_REG	5283 4274h
34278h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH6_CP_REG	5283 4278h
3427Ch	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH7_CP_REG	5283 427Ch
34300h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH0_HDP_REG	5283 4300h
34304h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH1_HDP_REG	5283 4304h
34308h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH2_HDP_REG	5283 4308h
3430Ch	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH3_HDP_REG	5283 430Ch
34310h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH4_HDP_REG	5283 4310h
34314h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH5_HDP_REG	5283 4314h
34318h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH6_HDP_REG	5283 4318h
3431Ch	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH7_HDP_REG	5283 431Ch

Table 4-1832. CPSW_NCSS_VBUSP, CPSW_NCSS_VBUSP Registers, Base Address=0X0000000052800000, Length=2097152 (continued)

Offset	Length	Register Name	CPSW Physical Address
34320h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH0_HDP_REG	5283 4320h
34324h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH1_HDP_REG	5283 4324h
34328h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH2_HDP_REG	5283 4328h
3432Ch	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH3_HDP_REG	5283 432Ch
34330h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH4_HDP_REG	5283 4330h
34334h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH5_HDP_REG	5283 4334h
34338h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH6_HDP_REG	5283 4338h
3433Ch	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH7_HDP_REG	5283 433Ch
34340h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH0_CP_REG	5283 4340h
34344h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH1_CP_REG	5283 4344h
34348h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH2_CP_REG	5283 4348h
3434Ch	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH3_CP_REG	5283 434Ch
34350h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH4_CP_REG	5283 4350h
34354h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH5_CP_REG	5283 4354h
34358h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH6_CP_REG	5283 4358h
3435Ch	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH7_CP_REG	5283 435Ch
34360h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH0_CP_REG	5283 4360h
34364h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH1_CP_REG	5283 4364h
34368h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH2_CP_REG	5283 4368h
3436Ch	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH3_CP_REG	5283 436Ch
34370h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH4_CP_REG	5283 4370h
34374h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH5_CP_REG	5283 4374h
34378h	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH6_CP_REG	5283 4378h
3437Ch	32	CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH7_CP_REG	5283 437Ch
3A000h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXGOODFRAMES_j	5283 A000h + Formula
3A004h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXBROADCASTFRAMES_j	5283 A004h + Formula
3A008h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXMULTICASTFRAMES_j	5283 A008h + Formula

Table 4-1832. CPSW_NCSS_VBUSP, CPSW_NCSS_VBUSP Registers, Base Address=0X0000000052800000, Length=2097152 (continued)

Offset	Length	Register Name	CPSW Physical Address
3A00Ch + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXPAUSEFRAMES_j	5283 A00Ch + Formula
3A010h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXCRCERRORS_j	5283 A010h + Formula
3A014h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXALIGNCODEERRORS_j	5283 A014h + Formula
3A018h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXOVERSIZEDFRAMES_j	5283 A018h + Formula
3A01Ch + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXJABBERFRAMES_j	5283 A01Ch + Formula
3A020h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXUNDERSIZEDFRAMES_j	5283 A020h + Formula
3A024h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXFRAGMENTS_j	5283 A024h + Formula
3A028h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_DROP_j	5283 A028h + Formula
3A02Ch + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_OVERRUN_DROP_j	5283 A02Ch + Formula
3A030h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXOCTETS_j	5283 A030h + Formula
3A034h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXGOODFRAMES_j	5283 A034h + Formula
3A038h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXBROADCASTFRAMES_j	5283 A038h + Formula
3A03Ch + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXMULTICASTFRAMES_j	5283 A03Ch + Formula
3A040h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXPAUSEFRAMES_j	5283 A040h + Formula
3A044h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXDEFERREDFRAMES_j	5283 A044h + Formula
3A048h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXCOLLISIONFRAMES_j	5283 A048h + Formula
3A04Ch + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXSINGLECOLLFRAMES_j	5283 A04Ch + Formula
3A050h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXMULTCOLLFRAMES_j	5283 A050h + Formula
3A054h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXEXCESSIVECOLLISIONS_j	5283 A054h + Formula
3A058h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXLATECOLLISIONS_j	5283 A058h + Formula
3A05Ch + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXIPGERROR_j	5283 A05Ch + Formula
3A060h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXCARRIERSENSEERRORS_j	5283 A060h + Formula
3A064h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXOCTETS_j	5283 A064h + Formula
3A068h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_OCTETFRAMES64_j	5283 A068h + Formula
3A06Ch + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_OCTETFRAMES65T127_j	5283 A06Ch + Formula
3A070h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_OCTETFRAMES128T255_j	5283 A070h + Formula
3A074h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_OCTETFRAMES256T511_j	5283 A074h + Formula

Table 4-1832. CPSW_NCSS_VBUSP, CPSW_NCSS_VBUSP Registers, Base Address=0X0000000052800000, Length=2097152 (continued)

Offset	Length	Register Name	CPSW Physical Address
3A078h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_OCTETFRAMES512T1023_j	5283 A078h + Formula
3A07Ch + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_OCTETFRAMES1024TUP_j	5283 A07Ch + Formula
3A080h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_NETOCTETS_j	5283 A080h + Formula
3A084h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_RX_BOTTOM_OF_FIFO_DROP_j	5283 A084h + Formula
3A088h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_PORTMASK_DROP_j	5283 A088h + Formula
3A08Ch + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_RX_TOP_OF_FIFO_DROP_j	5283 A08Ch + Formula
3A090h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_RATE_LIMIT_DROP_j	5283 A090h + Formula
3A094h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_VID_INGRESS_DROP_j	5283 A094h + Formula
3A098h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_DA_EQ_SA_DROP_j	5283 A098h + Formula
3A09Ch + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_BLOCK_DROP_j	5283 A09Ch + Formula
3A0A0h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_SECURE_DROP_j	5283 A0A0h + Formula
3A0A4h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_AUTH_DROP_j	5283 A0A4h + Formula
3A0A8h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_UNKN_UNI_j	5283 A0A8h + Formula
3A0ACh + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_UNKN_UNI_BCNT_j	5283 A0ACh + Formula
3A0B0h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_UNKN_MLT_j	5283 A0B0h + Formula
3A0B4h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_UNKN_MLT_BCNT_j	5283 A0B4h + Formula
3A0B8h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_UNKN_BRD_j	5283 A0B8h + Formula
3A0BCh + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_UNKN_BRD_BCNT_j	5283 A0BCh + Formula
3A0C0h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_POL_MATCH_j	5283 A0C0h + Formula
3A0C4h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_POL_MATCH_RED_j	5283 A0C4h + Formula
3A0C8h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_POL_MATCH_YELLOW_j	5283 A0C8h + Formula
3A0CCh + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_MULT_SA_DROP_j	5283 A0CCh + Formula
3A0D0h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_DUAL_VLAN_DROP_j	5283 A0D0h + Formula
3A0D4h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_LEN_ERROR_DROP_j	5283 A0D4h + Formula
3A0D8h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_IP_NEXT_HDR_DROP_j	5283 A0D8h + Formula
3A0DCh + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_IPV4_FRAG_DROP_j	5283 A0DCh + Formula
3A17Ch + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_TX_MEMORY_PROTECT_ERROR_j	5283 A17Ch + Formula

Table 4-1832. CPSW_NCSS_VBUSP, CPSW_NCSS_VBUSP Registers, Base Address=0X0000000052800000, Length=2097152 (continued)

Offset	Length	Register Name	CPSW Physical Address
3A180h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_ENET_PN_TX_PRI_REG_j_N	5283 A180h + Formula
3A1A0h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_ENET_PN_TX_PRI_BCNT_REG_j_N	5283 A1A0h + Formula
3A1C0h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_ENET_PN_TX_PRI_DROP_REG_j_N	5283 A1C0h + Formula
3A1E0h + Formula	32	CPSW_NC_CPSW_NC_CPSW_NC_STAT_ENET_PN_TX_PRI_DROP_BCNT_REG_j_N	5283 A1E0h + Formula
3D000h	32	CPSW_NC_CPSW_NC_CPTS_IDVER_REG	5283 D000h
3D004h	32	CPSW_NC_CPSW_NC_CPTS_CONTROL_REG	5283 D004h
3D008h	32	CPSW_NC_CPSW_NC_CPTS_RFTCLK_SEL_REG	5283 D008h
3D00Ch	32	CPSW_NC_CPSW_NC_CPTS_TS_PUSH_REG	5283 D00Ch
3D010h	32	CPSW_NC_CPSW_NC_CPTS_TS_LOAD_VAL_REG	5283 D010h
3D014h	32	CPSW_NC_CPSW_NC_CPTS_TS_LOAD_EN_REG	5283 D014h
3D018h	32	CPSW_NC_CPSW_NC_CPTS_TS_COMP_VAL_REG	5283 D018h
3D01Ch	32	CPSW_NC_CPSW_NC_CPTS_TS_COMP_LEN_REG	5283 D01Ch
3D020h	32	CPSW_NC_CPSW_NC_CPTS_INTSTAT_RAW_REG	5283 D020h
3D024h	32	CPSW_NC_CPSW_NC_CPTS_INTSTAT_MASKED_REG	5283 D024h
3D028h	32	CPSW_NC_CPSW_NC_CPTS_INT_ENABLE_REG	5283 D028h
3D02Ch	32	CPSW_NC_CPSW_NC_CPTS_TS_COMP_NUDGE_REG	5283 D02Ch
3D030h	32	CPSW_NC_CPSW_NC_CPTS_EVENT_POP_REG	5283 D030h
3D034h	32	CPSW_NC_CPSW_NC_CPTS_EVENT_0_REG	5283 D034h
3D038h	32	CPSW_NC_CPSW_NC_CPTS_EVENT_1_REG	5283 D038h
3D03Ch	32	CPSW_NC_CPSW_NC_CPTS_EVENT_2_REG	5283 D03Ch
3D040h	32	CPSW_NC_CPSW_NC_CPTS_EVENT_3_REG	5283 D040h
3D044h	32	CPSW_NC_CPSW_NC_CPTS_TS_LOAD_HIGH_VAL_REG	5283 D044h
3D048h	32	CPSW_NC_CPSW_NC_CPTS_TS_COMP_HIGH_VAL_REG	5283 D048h
3D04Ch	32	CPSW_NC_CPSW_NC_CPTS_TS_ADD_VAL_REG	5283 D04Ch
3D050h	32	CPSW_NC_CPSW_NC_CPTS_TS_PPM_LOW_VAL_REG	5283 D050h
3D054h	32	CPSW_NC_CPSW_NC_CPTS_TS_PPM_HIGH_VAL_REG	5283 D054h
3D058h	32	CPSW_NC_CPSW_NC_CPTS_TS_NUDGE_VAL_REG	5283 D058h
3D0D0h	32	CPSW_NC_CPSW_NC_CPTS_TS_CONFIG	5283 D0D0h
3D0E0h + Formula	32	CPSW_NC_CPSW_NC_CPTS_TS_GENF_COMP_LOW_REG_j	5283 D0E0h + Formula
3D0E4h + Formula	32	CPSW_NC_CPSW_NC_CPTS_TS_GENF_COMP_HIGH_REG_j	5283 D0E4h + Formula
3D0E8h + Formula	32	CPSW_NC_CPSW_NC_CPTS_TS_GENF_CONTROL_REG_j	5283 D0E8h + Formula
3D0ECh + Formula	32	CPSW_NC_CPSW_NC_CPTS_TS_GENF_LENGTH_REG_j	5283 D0ECh + Formula
3D0F0h + Formula	32	CPSW_NC_CPSW_NC_CPTS_TS_GENF_PPM_LOW_REG_j	5283 D0F0h + Formula
3D0F4h + Formula	32	CPSW_NC_CPSW_NC_CPTS_TS_GENF_PPM_HIGH_REG_j	5283 D0F4h + Formula
3D0F8h + Formula	32	CPSW_NC_CPSW_NC_CPTS_TS_GENF_NUDGE_REG_j	5283 D0F8h + Formula
3D200h + Formula	32	CPSW_NC_CPSW_NC_CPTS_TS_ESTF_COMP_LOW_REG_j	5283 D200h + Formula

Table 4-1832. CPSW_NCSS_VBUSP, CPSW_NCSS_VBUSP Registers, Base Address=0X0000000052800000, Length=2097152 (continued)

Offset	Length	Register Name	CPSW Physical Address
3D204h + Formula	32	CPSW_NC_CPSW_NC_CPTS_TS_ESTF_COMP_HIGH_REG_j	5283 D204h + Formula
3D208h + Formula	32	CPSW_NC_CPSW_NC_CPTS_TS_ESTF_CONTROL_REG_j	5283 D208h + Formula
3D20Ch + Formula	32	CPSW_NC_CPSW_NC_CPTS_TS_ESTF_LENGTH_REG_j	5283 D20Ch + Formula
3D210h + Formula	32	CPSW_NC_CPSW_NC_CPTS_TS_ESTF_PPM_LOW_REG_j	5283 D210h + Formula
3D214h + Formula	32	CPSW_NC_CPSW_NC_CPTS_TS_ESTF_PPM_HIGH_REG_j	5283 D214h + Formula
3D218h + Formula	32	CPSW_NC_CPSW_NC_CPTS_TS_ESTF_NUDGE_REG_j	5283 D218h + Formula
3E000h	32	CPSW_NC_CPSW_NC_ALE_MOD_VER	5283 E000h
3E004h	32	CPSW_NC_CPSW_NC_ALE_ALE_STATUS	5283 E004h
3E008h	32	CPSW_NC_CPSW_NC_ALE_ALE_CONTROL	5283 E008h
3E00Ch	32	CPSW_NC_CPSW_NC_ALE_ALE_CTRL2	5283 E00Ch
3E010h	32	CPSW_NC_CPSW_NC_ALE_ALE_PRESCALE	5283 E010h
3E014h	32	CPSW_NC_CPSW_NC_ALE_ALE_AGING_CTRL	5283 E014h
3E01Ch	32	CPSW_NC_CPSW_NC_ALE_ALE_NXT_HDR	5283 E01Ch
3E020h	32	CPSW_NC_CPSW_NC_ALE_ALE_TBLCTL	5283 E020h
3E034h	32	CPSW_NC_CPSW_NC_ALE_ALE_TBLW2	5283 E034h
3E038h	32	CPSW_NC_CPSW_NC_ALE_ALE_TBLW1	5283 E038h
3E03Ch	32	CPSW_NC_CPSW_NC_ALE_ALE_TBLW0	5283 E03Ch
3E040h + Formula	32	CPSW_NC_CPSW_NC_ALE_l0_ALE_PORTCTL0_N	5283 E040h + Formula
3E090h	32	CPSW_NC_CPSW_NC_ALE_ALE_UVLAN_MEMBER	5283 E090h
3E094h	32	CPSW_NC_CPSW_NC_ALE_ALE_UVLAN_URCAST	5283 E094h
3E098h	32	CPSW_NC_CPSW_NC_ALE_ALE_UVLAN_RMCAST	5283 E098h
3E09Ch	32	CPSW_NC_CPSW_NC_ALE_ALE_UVLAN_UNTAG	5283 E09Ch
3E0B4h	32	CPSW_NC_CPSW_NC_ALE_ALE_FAST_LUT	5283 E0B4h
3E0B8h	32	CPSW_NC_CPSW_NC_ALE_ALE_STAT_DIAG	5283 E0B8h
3E0BCh	32	CPSW_NC_CPSW_NC_ALE_ALE_OAM_LB_CTRL	5283 E0BCh
3E0FCh	32	CPSW_NC_CPSW_NC_ALE_EGRESSOP	5283 E0FCh
3E100h	32	CPSW_NC_CPSW_NC_ALE_POLICECFG0	5283 E100h
3E104h	32	CPSW_NC_CPSW_NC_ALE_POLICECFG1	5283 E104h
3E108h	32	CPSW_NC_CPSW_NC_ALE_POLICECFG2	5283 E108h
3E10Ch	32	CPSW_NC_CPSW_NC_ALE_POLICECFG3	5283 E10Ch
3E110h	32	CPSW_NC_CPSW_NC_ALE_POLICECFG4	5283 E110h
3E118h	32	CPSW_NC_CPSW_NC_ALE_POLICECFG6	5283 E118h
3E11Ch	32	CPSW_NC_CPSW_NC_ALE_POLICECFG7	5283 E11Ch
3E120h	32	CPSW_NC_CPSW_NC_ALE_POLICETBLCTL	5283 E120h
3E124h	32	CPSW_NC_CPSW_NC_ALE_POLICECONTROL	5283 E124h
3E128h	32	CPSW_NC_CPSW_NC_ALE_POLICETESTCTL	5283 E128h
3E12Ch	32	CPSW_NC_CPSW_NC_ALE_POLICEHSTAT	5283 E12Ch
3E134h	32	CPSW_NC_CPSW_NC_ALE_THREADMAPDEF	5283 E134h
3E138h	32	CPSW_NC_CPSW_NC_ALE_THREADMAPCTL	5283 E138h
3E13Ch	32	CPSW_NC_CPSW_NC_ALE_THREADMAPVAL	5283 E13Ch
3F000h	32	CPSW_NC_CPSW_NC_ECC_rev	5283 F000h

Table 4-1832. CPSW_NCSS_VBUSP, CPSW_NCSS_VBUSP Registers, Base Address=0X0000000052800000, Length=2097152 (continued)

Offset	Length	Register Name	CPSW Physical Address
3F008h	32	CPSW_NC_CPSW_NC_ECC_vector	5283 F008h
3F00Ch	32	CPSW_NC_CPSW_NC_ECC_stat	5283 F00Ch
3F010h + Formula	32	CPSW_NC_CPSW_NC_ECC_reserved_svbus_N	5283 F010h + Formula
3F03Ch	32	CPSW_NC_CPSW_NC_ECC_sec_eoi_reg	5283 F03Ch
3F040h	32	CPSW_NC_CPSW_NC_ECC_sec_status_reg0	5283 F040h
3F080h	32	CPSW_NC_CPSW_NC_ECC_sec_enable_set_reg0	5283 F080h
3F0C0h	32	CPSW_NC_CPSW_NC_ECC_sec_enable_clr_reg0	5283 F0C0h
3F13Ch	32	CPSW_NC_CPSW_NC_ECC_ded_eoi_reg	5283 F13Ch
3F140h	32	CPSW_NC_CPSW_NC_ECC_ded_status_reg0	5283 F140h
3F180h	32	CPSW_NC_CPSW_NC_ECC_ded_enable_set_reg0	5283 F180h
3F1C0h	32	CPSW_NC_CPSW_NC_ECC_ded_enable_clr_reg0	5283 F1C0h
3F200h	32	CPSW_NC_CPSW_NC_ECC_aggr_enable_set	5283 F200h
3F204h	32	CPSW_NC_CPSW_NC_ECC_aggr_enable_clr	5283 F204h
3F208h	32	CPSW_NC_CPSW_NC_ECC_aggr_status_set	5283 F208h
3F20Ch	32	CPSW_NC_CPSW_NC_ECC_aggr_status_clr	5283 F20Ch

4.18.1 CPSW_NCSS_VBUSP_CPSW_NUSS_IDVER_REG Registers

4.18.1.1 CPSW_VBUSP_CPSW_NUSS_IDVER_REG Register (Offset = 0h) [reset = 6ba01903h]

Short Description: ID Version Register

Long Description: ID Version Register

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Table 4-1833. Instance Table

Instance Name	Physical Address
CPSW	5280 0000h

Figure 4-829. CPSW_NUSS_IDVER_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IDENT															
R															
6ba0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL_VER					MAJOR_VER			MINOR_VER							
R					R			R							
3h					1h			3h							

Access Types Legend

Table 4-1834. CPSW_NUSS_IDVER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IDENT	R	6BA0h	Identification value
15:11	RTL_VER	R	3h	RTL version value
10:8	MAJOR_VER	R	1h	Major version value
7:0	MINOR_VER	R	3h	Minor version value

4.18.2 CPSW_NCSS_VBUSP_SS_SYNCE_COUNT_REG Registers

4.18.2.1 CPSW_VBUSP_SS_SYNCE_COUNT_REG Register (Offset = 4h) [reset = 0h]

Short Description: SyncE Count Register

Long Description: SS SYNCE Count Register

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Table 4-1835. Instance Table

Instance Name	Physical Address
CPSW	5280 0004h

Figure 4-830. SS_SYNCE_COUNT_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SYNCE_CNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNCE_CNT															
R/W															
0h															

Access Types Legend

Table 4-1836. SS_SYNCE_COUNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SYNCE_CNT	R/W	0h	Sync E Count Value

4.18.3 CPSW_NCSS_VBUSP_SS_SYNCE_MUX_REG Registers

4.18.3.1 CPSW_VBUSP_SS_SYNCE_MUX_REG Register (Offset = 8h) [reset = 0h]

Short Description: SyncE Mux Register

Long Description: SS Synce Mux Register

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Table 4-1837. Instance Table

Instance Name	Physical Address
CPSW	5280 0008h

Figure 4-831. SS_SYNCE_MUX_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										SYNCE_SEL					
NONE										R/W					
0										0h					

Access Types Legend

Table 4-1838. SS_SYNCE_MUX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE		Reserved
5:0	SYNCE_SEL	R/W	0h	Sync E Select Value

4.18.4 CPSW_NCSS_VBUSP_SS_CONTROL_REG Registers

4.18.4.1 CPSW_VBUSP_SS_CONTROL_REG Register (Offset = Ch) [reset = 0h]

Short Description: Control Register

Long Description: SS Control Register

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Table 4-1839. Instance Table

Instance Name	Physical Address
CPSW	5280 000Ch

Figure 4-832. SS_CONTROL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														EEE_PHY_ONLY	EEE_EN
NONE														R/W	R/W
0														0h	0h

Access Types Legend

Table 4-1840. SS_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1	EEE_PHY_ONLY	R/W	0h	Energy Efficient Enable Phy Only Mode: 0=The low power indicate state includes gating off the CPPI_GCLK to the CPSW, 1=The low power indicate state does not gate the clock to the CPSW
0	EEE_EN	R/W	0h	Energy Efficient Ethernet Enable: 0=EEE is disabled, 1=EEE is enabled

4.18.5 CPSW_NCSS_VBUSP_SS_INT_CONTROL_REG Registers

4.18.5.1 CPSW_VBUSP_SS_INT_CONTROL_REG Register (Offset = 18h) [reset = 0h]

Short Description: Interrupt Control Register

Long Description: SS Interrupt Control Register

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Table 4-1841. Instance Table

Instance Name	Physical Address
CPSW	5280 0018h

Figure 4-833. SS_INT_CONTROL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INT_TEST	INT_SEL_VEC_EN	RESERVED								INT_BYPASS					
R/W	R/W	NONE								R/W					
0h	0h	0								0h					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				INT_PRESCALE											
NONE				R/W											
0				0h											

Access Types Legend

Table 4-1842. SS_INT_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_TEST	R/W	0h	Interrupt Test
30	INT_SEL_VEC_EN	R/W	0h	Interrupt Sel Vector Enable
29:22	RESERVED	NONE		Reserved
21:16	INT_BYPASS	R/W	0h	Interrupt Bypass Value
15:12	RESERVED	NONE		Reserved
11:0	INT_PRESCALE	R/W	0h	Interrupt Prescale Value

4.18.6 CPSW_NCSS_VBUSP_SS_STATUS_REG Registers

4.18.6.1 CPSW_VBUSP_SS_STATUS_REG Register (Offset = 1Ch) [reset = 0h]

Short Description: Subsystem Status Register

Long Description: SS Status Register

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Table 4-1843. Instance Table

Instance Name	Physical Address
CPSW	5280 001Ch

Figure 4-834. SS_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															EEE_CLKSTOP_ACK
NONE															R
0															0h

Access Types Legend

Table 4-1844. SS_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	EEE_CLKSTOP_ACK	R	0h	Energy Efficient Ethernet clockstop acknowledge from CPSW

4.18.7 CPSW_NCSS_VBUSP_SUBSYSTEM_CONFIG_REG Registers

4.18.7.1 CPSW_VBUSP_SUBSYSTEM_CONFIG_REG Register (Offset = 20h) [reset = 30203h]

Short Description: Subsystem Configuration Register

Long Description: Subsystem Configuration Register

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Table 4-1845. Instance Table

Instance Name	Physical Address
CPSW	5280 0020h

Figure 4-835. SUBSYSTEM_CONFIG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				XGMII								QSGMII	SGMII	RGMII	RMII
NONE				R								R	R	R	R
1				0h								0h	0h	1h	1h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				NUM_GENF				NUM_PORTS							
NONE				R				R							
1				2h				3h							

Access Types Legend

Table 4-1846. SUBSYSTEM_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE		Reserved
27:20	XGMII	R	0h	The Number of XGMII Ports included in the CPSW_NUSS
19	QSGMII	R	0h	QSGMII is included in the CPSW_NUSS
18	SGMII	R	0h	SGMII is included in the CPSW_NUSS
17	RGMII	R	1h	RGMII is included in the CPSW_NUSS
16	RMII	R	1h	RMII is included in the CPSW_NUSS
15:13	RESERVED	NONE		Reserved
12:8	NUM_GENF	R	2h	The number of CPTS GENF outputs
7:0	NUM_PORTS	R	3h	The total number of ports including the host port 0

4.18.8 CPSW_NCSS_VBUSP_RGMII1_STATUS_REG Registers

4.18.8.1 CPSW_VBUSP_RGMII1_STATUS_REG Register (Offset = 30h) [reset = 0h]

Short Description: RGMII1 Status Register

Long Description: RGMII1 Status Register

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Table 4-1847. Instance Table

Instance Name	Physical Address
CPSW	5280 0030h

Figure 4-836. RGMII1_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												FULLDUPLEX	SPEED		LINK
NONE												R	R		R
0												0h	0h		0h

Access Types Legend

Table 4-1848. RGMII1_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	FULLDUPLEX	R	0h	Rgmii1 full dulex: 0=Half-duplex, 1=Full-duplex
2:1	SPEED	R	0h	Rgmii1 speed: 00=10Mbps, 01=100Mbps, 10=1000Mbps, 11=reserved
0	LINK	R	0h	Rgmii1 link indicator: 0=Link is down, 1=Link is up

4.18.9 CPSW_NCSS_VBUSP_RGMII2_STATUS_REG Registers

4.18.9.1 CPSW_VBUSP_RGMII2_STATUS_REG Register (Offset = 34h) [reset = 0h]

Short Description: RGMII2 Status Register

Long Description: RGMII2 Status Register

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Table 4-1849. Instance Table

Instance Name	Physical Address
CPSW	5280 0034h

Figure 4-837. RGMII2_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												FULLDUPLEX	SPEED		LINK
NONE												R	R		R
0												0h	0h		0h

Access Types Legend

Table 4-1850. RGMII2_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	FULLDUPLEX	R	0h	Rgmii2 full dulex: 0=Half-duplex, 1=Full-duplex
2:1	SPEED	R	0h	Rgmii2 speed: 00=10Mbps, 01=100Mbps, 10=1000Mbps, 11=reserved
0	LINK	R	0h	Rgmii2 link indicator: 0=Link is down, 1=Link is up

4.18.10 CPSW_NCSS_VBUSP_MDIO_MDIO_MDIO_VERSION_REG Registers

4.18.10.1 CPSW_VBUSP_MDIO_MDIO_MDIO_VERSION_REG Register (Offset = F00h) [reset = 70907h]

Short Description: version_reg

Long Description: MDIO Version Register

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Table 4-1851. Instance Table

Instance Name	Physical Address
CPSW	5280 0F00h

Figure 4-838. MDIO_MDIO_MDIO_VERSION_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R		R		R											
0h		0h		7h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL				REVMAJ				CUSTOM		REVMIN					
R				R				R		R					
1h				1h				0h		7h					

Access Types Legend

Table 4-1852. MDIO_MDIO_MDIO_VERSION_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	0h	Scheme
29:28	BU	R	0h	bu
27:16	MODULE_ID	R	7h	Module ID
15:11	REVRTL	R	1h	RTL version
10:8	REVMAJ	R	1h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	7h	Minor version

4.18.11 CPSW_NCSS_VBUSP_MDIO_MDIO_CONTROL_REG Registers

4.18.11.1 CPSW_VBUSP_MDIO_MDIO_CONTROL_REG Register (Offset = F04h) [reset = 810000ffh]

Short Description: control_reg

Long Description: MDIO Control Register

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Table 4-1853. Instance Table

Instance Name	Physical Address
CPSW	5280 0F04h

Figure 4-839. MDIO_MDIO_CONTROL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IDLE	ENABLE	RESERVED	HIGHEST_USER_CHANNEL					RESERVED			PREAMBLE	FAULT	FAULT_DETECT_ENABLE	INT_TEST_ENABLE	RESERVED
R	R/W	NONE	R					NONE			R/W	R/W	R/W	R/W	NONE
1h	0h	1	1h					0			0h	0h	0h	0h	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLKDIV															
R/W															
ffh															

Access Types Legend

Table 4-1854. MDIO_MDIO_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IDLE	R	1h	MDIO state machine idle
30	ENABLE	R/W	0h	Enable control
29	RESERVED	NONE		Reserved
28:24	HIGHEST_USER_CHANNEL	R	1h	Highest user channel
23:21	RESERVED	NONE		Reserved
20	PREAMBLE	R/W	0h	Preamble disable
19	FAULT	R/W	0h	Fault indicator
18	FAULT_DETECT_ENABLE	R/W	0h	Fault detect enable
17	INT_TEST_ENABLE	R/W	0h	Interrupt test enable
16	RESERVED	NONE		Reserved
15:0	CLKDIV	R/W	FFh	Clock divider

4.18.12 CPSW_NCSS_VBUSP_MDIO_MDIO_ALIVE_REG Registers

4.18.12.1 CPSW_VBUSP_MDIO_MDIO_ALIVE_REG Register (Offset = F08h) [reset = 0h]

Short Description: alive_reg

Long Description: MDIO Alive Register

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Table 4-1855. Instance Table

Instance Name	Physical Address
CPSW	5280 0F08h

Figure 4-840. MDIO_MDIO_ALIVE_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ALIVE															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALIVE															
R/W															
0h															

Access Types Legend

Table 4-1856. MDIO_MDIO_ALIVE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ALIVE	R/W	0h	MDIO alive

4.18.13 CPSW_NCSS_VBUSP_MDIO_MDIO_LINK_REG Registers

4.18.13.1 CPSW_VBUSP_MDIO_MDIO_LINK_REG Register (Offset = F0Ch) [reset = 0h]

Short Description: link_reg

Long Description: MDIO Link Register

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Table 4-1857. Instance Table

Instance Name	Physical Address
CPSW	5280 0F0Ch

Figure 4-841. MDIO_MDIO_LINK_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LINK															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LINK															
R															
0h															

Access Types Legend

Table 4-1858. MDIO_MDIO_LINK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LINK	R	0h	MDIO link state

4.18.14 CPSW_NCSS_VBUSP_MDIO_MDIO_LINK_INT_RAW_REG Registers

4.18.14.1 CPSW_VBUSP_MDIO_MDIO_LINK_INT_RAW_REG Register (Offset = F10h) [reset = 0h]

Short Description: link_int_raw_reg

Long Description: MDIO Link Interrupt Raw Register

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Table 4-1859. Instance Table

Instance Name	Physical Address
CPSW	5280 0F10h

Figure 4-842. MDIO_MDIO_LINK_INT_RAW_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														LINKINTRAW	
NONE														R/W	
0														0h	

Access Types Legend

Table 4-1860. MDIO_MDIO_LINK_INT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1:0	LINKINTRAW	R/W	0h	MDIO link change event raw value

4.18.15 CPSW_NCSS_VBUSP_MDIO_MDIO_LINK_INT_MASKED_REG Registers

4.18.15.1 CPSW_VBUSP_MDIO_MDIO_LINK_INT_MASKED_REG Register (Offset = F14h) [reset = 0h]

Short Description: link_int_masked_reg

Long Description: MDIO Link Interrupt Masked Register

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Table 4-1861. Instance Table

Instance Name	Physical Address
CPSW	5280 0F14h

Figure 4-843. MDIO_MDIO_LINK_INT_MASKED_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														LINKINTMASKED	
NONE														R/W	
0														0h	

Access Types Legend

Table 4-1862. MDIO_MDIO_LINK_INT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1:0	LINKINTMASKED	R/W	0h	MDIO link change interrupt masked value

4.18.16 CPSW_NCSS_VBUSP_MDIO_MDIO_LINK_INT_MASK_SET_REG Registers

4.18.16.1 CPSW_VBUSP_MDIO_MDIO_LINK_INT_MASK_SET_REG Register (Offset = F18h) [reset = 0h]

Short Description: link_int_mask_set_reg

Long Description: MDIO Link Interrupt Mask Set Register

Return to Summary Table

Table 4-1863. Instance Table

Instance Name	Physical Address
CPSW	5280 0F18h

Figure 4-844. MDIO_MDIO_LINK_INT_MASK_SET_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															LINKINTMASKSET
NONE															R/W
0															0h

Access Types Legend

Table 4-1864. MDIO_MDIO_LINK_INT_MASK_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	LINKINTMASKSET	R/W	0h	MDIO link interrupt mask set

4.18.17 CPSW_NCSS_VBUSP_MDIO_MDIO_LINK_INT_MASK_CLEAR_REG Registers

4.18.17.1 CPSW_VBUSP_MDIO_MDIO_LINK_INT_MASK_CLEAR_REG Register (Offset = F1Ch) [reset = 0h]

Short Description: link_int_mask_clear_reg

Long Description: MDIO Link Interrupt Mask Clear Register

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Table 4-1865. Instance Table

Instance Name	Physical Address
CPSW	5280 0F1Ch

Figure 4-845. MDIO_MDIO_LINK_INT_MASK_CLEAR_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															LINKINTMASKCLR
NONE															R/W
0															0h

Access Types Legend

Table 4-1866. MDIO_MDIO_LINK_INT_MASK_CLEAR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	LINKINTMASKCLR	R/W	0h	MDIO link interrupt mask clear

4.18.18 CPSW_NCSS_VBUSP_MDIO_MDIO_USER_INT_RAW_REG Registers

4.18.18.1 CPSW_VBUSP_MDIO_MDIO_USER_INT_RAW_REG Register (Offset = F20h) [reset = 0h]

Short Description: user_int_raw_reg

Long Description: MDIO User Interrupt Raw Register

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Table 4-1867. Instance Table

Instance Name	Physical Address
CPSW	5280 0F20h

Figure 4-846. MDIO_MDIO_USER_INT_RAW_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														USERINTRAW	
NONE														R/W	
0														0h	

Access Types Legend

Table 4-1868. MDIO_MDIO_USER_INT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1:0	USERINTRAW	R/W	0h	User interrupt raw

4.18.19 CPSW_NCSS_VBUSP_MDIO_MDIO_USER_INT_MASKED_REG Registers

4.18.19.1 CPSW_VBUSP_MDIO_MDIO_USER_INT_MASKED_REG Register (Offset = F24h) [reset = 0h]

Short Description: user_int_masked_reg

Long Description: MDIO User Interrupt Masked Register

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Table 4-1869. Instance Table

Instance Name	Physical Address
CPSW	5280 0F24h

Figure 4-847. MDIO_MDIO_USER_INT_MASKED_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														USERINTMASKED	
NONE														R/W	
0														0h	

Access Types Legend

Table 4-1870. MDIO_MDIO_USER_INT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1:0	USERINTMASKED	R/W	0h	User interrupt masked

4.18.20 CPSW_NCSS_VBUSP_MDIO_MDIO_USER_INT_MASK_SET_REG Registers

4.18.20.1 CPSW_VBUSP_MDIO_MDIO_USER_INT_MASK_SET_REG Register (Offset = F28h) [reset = 0h]

Short Description: user_int_mask_set_reg

Long Description: MDIO User Interrupt Mask Set Register

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Table 4-1871. Instance Table

Instance Name	Physical Address
CPSW	5280 0F28h

Figure 4-848. MDIO_MDIO_USER_INT_MASK_SET_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														USERINTMASKSET	
NONE														R/W	
0														0h	

Access Types Legend

Table 4-1872. MDIO_MDIO_USER_INT_MASK_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1:0	USERINTMASKSET	R/W	0h	MDIO user interrupt mask set

4.18.21 CPSW_NCSS_VBUSP_MDIO_MDIO_USER_INT_MASK_CLEAR_REG Registers

4.18.21.1 CPSW_VBUSP_MDIO_MDIO_USER_INT_MASK_CLEAR_REG Register (Offset = F2Ch) [reset = 0h]

Short Description: user_int_mask_clear_reg

Long Description: MDIO User Interrupt Mask Clear Register

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Table 4-1873. Instance Table

Instance Name	Physical Address
CPSW	5280 0F2Ch

Figure 4-849. MDIO_MDIO_USER_INT_MASK_CLEAR_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														USERINTMASK CLR	
NONE														R/W	
0														0h	

Access Types Legend

Table 4-1874. MDIO_MDIO_USER_INT_MASK_CLEAR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1:0	USERINTMASKCLR	R/W	0h	MDIO user interrupt mask clear

4.18.22 CPSW_NCSS_VBUSP_MDIO_MDIO_MANUAL_IF_REG Registers

4.18.22.1 CPSW_VBUSP_MDIO_MDIO_MANUAL_IF_REG Register (Offset = F30h) [reset = 0h]

Short Description: manual_if_reg

Long Description: MDIO Manual Interface Register

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Table 4-1875. Instance Table

Instance Name	Physical Address
CPSW	5280 0F30h

Figure 4-850. MDIO_MDIO_MANUAL_IF_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MDIO_MDCLK_O	MDIO_OE	MDIO_PIN
NONE													R/W	R/W	R/W
0													0h	0h	0h

Access Types Legend

Table 4-1876. MDIO_MDIO_MANUAL_IF_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2	MDIO_MDCLK_O	R/W	0h	MDIO Clock Output
1	MDIO_OE	R/W	0h	MDIO Output Enable
0	MDIO_PIN	R/W	0h	MDIO Pin

4.18.23 CPSW_NCSS_VBUSP_MDIO_MDIO_POLL_REG Registers

4.18.23.1 CPSW_VBUSP_MDIO_MDIO_POLL_REG Register (Offset = F34h) [reset = 0h]

Short Description: poll_reg

Long Description: MDIO Poll Register

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Table 4-1877. Instance Table

Instance Name	Physical Address
CPSW	5280 0F34h

Figure 4-851. MDIO_MDIO_POLL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MANUALMODE	STATECHANGEMODE	RESERVED													
R/W	R/W	NONE													
0h	0h	0													

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								IPG							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-1878. MDIO_MDIO_POLL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MANUALMODE	R/W	0h	MDIO Manual Mode
30	STATECHANGEMODE	R/W	0h	MDIO State Change Mode
29:8	RESERVED	NONE		Reserved
7:0	IPG	R/W	0h	MDIO IPG

4.18.24 CPSW_NCSS_VBUSP_MDIO_MDIO_POLL_EN_REG Registers

4.18.24.1 CPSW_VBUSP_MDIO_MDIO_POLL_EN_REG Register (Offset = F38h) [reset = ffffffffh]

Short Description: poll_reg

Long Description: MDIO Poll Enable Register

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Table 4-1879. Instance Table

Instance Name	Physical Address
CPSW	5280 0F38h

Figure 4-852. MDIO_MDIO_POLL_EN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
POLL_EN															
R/W															
ffffffffh															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POLL_EN															
R/W															
ffffffffh															

Access Types Legend

Table 4-1880. MDIO_MDIO_POLL_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	POLL_EN	R/W	FFFFFFFFh	MDIO Poll Enable

4.18.25 CPSW_NCSS_VBUSP_MDIO_MDIO_CLAUS45_REG Registers

4.18.25.1 CPSW_VBUSP_MDIO_MDIO_CLAUS45_REG Register (Offset = F3Ch) [reset = 0h]

Short Description: poll_reg

Long Description: MDIO Clause45 Register

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Table 4-1881. Instance Table

Instance Name	Physical Address
CPSW	5280 0F3Ch

Figure 4-853. MDIO_MDIO_CLAUS45_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLAUSE45															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLAUSE45															
R/W															
0h															

Access Types Legend

Table 4-1882. MDIO_MDIO_CLAUS45_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAUSE45	R/W	0h	MDIO Clause 45

4.18.26 CPSW_NCSS_VBUSP_MDIO_MDIO_USER_ADDR0_REG Registers

4.18.26.1 CPSW_VBUSP_MDIO_MDIO_USER_ADDR0_REG Register (Offset = F40h) [reset = 0h]

Short Description: poll_reg

Long Description: MDIO Address 0 Register

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Table 4-1883. Instance Table

Instance Name	Physical Address
CPSW	5280 0F40h

Figure 4-854. MDIO_MDIO_USER_ADDR0_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USER_ADDR0															
R/W															
0h															

Access Types Legend

Table 4-1884. MDIO_MDIO_USER_ADDR0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	USER_ADDR0	R/W	0h	MDIO USER Address 0

4.18.27 CPSW_NCSS_VBUSP_MDIO_MDIO_USER_ADDR1_REG Registers

4.18.27.1 CPSW_VBUSP_MDIO_MDIO_USER_ADDR1_REG Register (Offset = F44h) [reset = 0h]

Short Description: poll_reg

Long Description: MDIO Address 1 Register

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Table 4-1885. Instance Table

Instance Name	Physical Address
CPSW	5280 0F44h

Figure 4-855. MDIO_MDIO_USER_ADDR1_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USER_ADDR1															
R/W															
0h															

Access Types Legend

Table 4-1886. MDIO_MDIO_USER_ADDR1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	USER_ADDR1	R/W	0h	MDIO USER Address 1

4.18.28 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C0_TH_THRESH_PULSE_EN_REG Registers

4.18.28.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C0_TH_THRESH_PULSE_EN_REG Register (Offset = 1800h) [reset = 0h]

Short Description: Core 0 THost Threshold Pulse Interrupt Enable Register

Long Description: Core 0 THost Threshold Pulse Interrupt Enable Register

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Table 4-1887. Instance Table

Instance Name	Physical Address
CPSW	5280 1800h

Figure 4-856. REGS_INT_REGS_INT_SS_C0_TH_THRESH_PULSE_EN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TH_THRESH_PULSE_EN							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-1888. REGS_INT_REGS_INT_SS_C0_TH_THRESH_PULSE_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	TH_THRESH_PULSE_EN	R/W	0h	THost Threshold Pulse Interrupt Enable Register

4.18.29 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C0_TH_PULSE_EN_REG Registers

4.18.29.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C0_TH_PULSE_EN_REG Register (Offset = 1804h) [reset = 0h]

Short Description: Core 0 THost Pulse Interrupt Enable Register

Long Description: Core 0 THost Pulse Interrupt Enable Register

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Table 4-1889. Instance Table

Instance Name	Physical Address
CPSW	5280 1804h

Figure 4-857. REGS_INT_REGS_INT_SS_C0_TH_PULSE_EN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TH_PULSE_EN							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-1890. REGS_INT_REGS_INT_SS_C0_TH_PULSE_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	TH_PULSE_EN	R/W	0h	Core 0 THost Pulse Interrupt Enable Register

4.18.30 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C0_FH_PULSE_EN_REG Registers

4.18.30.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C0_FH_PULSE_EN_REG Register (Offset = 1808h) [reset = 0h]

Short Description: Core 0 FHost Pulse Interrupt Enable Register

Long Description: Core 0 FHost Pulse Interrupt Enable Register

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Table 4-1891. Instance Table

Instance Name	Physical Address
CPSW	5280 1808h

Figure 4-858. REGS_INT_REGS_INT_SS_C0_FH_PULSE_EN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FH_PULSE_EN							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-1892. REGS_INT_REGS_INT_SS_C0_FH_PULSE_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	FH_PULSE_EN	R/W	0h	Core 0 FHost Pulse Interrupt Enable Register

4.18.31 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C0_MISC_EN_REG Registers

4.18.31.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C0_MISC_EN_REG Register (Offset = 180Ch) [reset = 0h]

Short Description: Core 0 Misc Interrupt Enable Register

Long Description: Core 0 Misc Interrupt Enable Register

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Table 4-1893. Instance Table

Instance Name	Physical Address
CPSW	5280 180Ch

Figure 4-859. REGS_INT_REGS_INT_SS_C0_MISC_EN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									DED_PEND_EN	SEC_PEND_EN	EVNT_PEND_EN	STAT_PEND_EN	HOST_PEND_EN	MDIO_LINKINT_EN	MDIO_USERINT_EN
NONE									R/W	R/W	R/W	R/W	R/W	R/W	R/W
0									0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-1894. REGS_INT_REGS_INT_SS_C0_MISC_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE		Reserved
6	DED_PEND_EN	R/W	0h	Core 0 MISC DED Memory Protect Error Interrupt Enable
5	SEC_PEND_EN	R/W	0h	Core 0 MISC SEC Memory Protect Error Interrupt Enable
4	EVNT_PEND_EN	R/W	0h	Core 0 MISC CPTS Event Interrupt Enable
3	STAT_PEND_EN	R/W	0h	Core 0 MISC Statistics Interrupt Enable - OR of bits n downto 0
2	HOST_PEND_EN	R/W	0h	Core 0 MISC Host Interrupt Enable
1	MDIO_LINKINT_EN	R/W	0h	Core 0 MISC MDIO linkint - OR of bits 1 and 0
0	MDIO_USERINT_EN	R/W	0h	Core 0 MISC_MDIO userint interrupt enable - OR of bits 1 and 0

4.18.32 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C0_TH_THRESH_PULSE_STATUS_REG Registers

4.18.32.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C0_TH_THRESH_PULSE_STATUS_REG Register (Offset = 1810h) [reset = 0h]

Short Description: Core 0 THost Threshold Pulse Interrupt Status Register

Long Description: THost Threshold Pulse Interrupt Status Register

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Table 4-1895. Instance Table

Instance Name	Physical Address
CPSW	5280 1810h

Figure 4-860. REGS_INT_REGS_INT_SS_C0_TH_THRESH_PULSE_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TH_THRESH_PULSE_STATUS							
NONE								R							
0								0h							

Access Types Legend

Table 4-1896. REGS_INT_REGS_INT_SS_C0_TH_THRESH_PULSE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	TH_THRESH_PULSE_STATUS	R	0h	Core 0 THost Threshold Pulse Interrupt Status Register

4.18.33 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C0_TH_PULSE_STATUS_REG Registers

4.18.33.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C0_TH_PULSE_STATUS_REG Register (Offset = 1814h) [reset = 0h]

Short Description: Core 0 THost Pulse Interrupt Status Register

Long Description: THost Pulse Interrupt Status Register

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Table 4-1897. Instance Table

Instance Name	Physical Address
CPSW	5280 1814h

Figure 4-861. REGS_INT_REGS_INT_SS_C0_TH_PULSE_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TH_PULSE_STATUS							
NONE								R							
0								0h							

Access Types Legend

Table 4-1898. REGS_INT_REGS_INT_SS_C0_TH_PULSE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	TH_PULSE_STATUS	R	0h	Core 0 THost Pulse Interrupt Status Register

4.18.34 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C0_FH_PULSE_STATUS_REG Registers

4.18.34.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C0_FH_PULSE_STATUS_REG Register (Offset = 1818h) [reset = 0h]

Short Description: Core 0 FHost Pulse Interrupt Status Register

Long Description: FHost Pulse Interrupt Status Register

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Table 4-1899. Instance Table

Instance Name	Physical Address
CPSW	5280 1818h

Figure 4-862. REGS_INT_REGS_INT_SS_C0_FH_PULSE_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FH_PULSE_STATUS							
NONE								R							
0								0h							

Access Types Legend

Table 4-1900. REGS_INT_REGS_INT_SS_C0_FH_PULSE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	FH_PULSE_STATUS	R	0h	Core 0 FHost Pulse Interrupt Status Register

4.18.35 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C0_MISC_STATUS_REG Registers

4.18.35.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C0_MISC_STATUS_REG Register (Offset = 181Ch) [reset = 0h]

Short Description: Core 0 Misc Interrupt Status Register

Long Description: Misc Interrupt Status Register - Set bits in this register indicate that an enabled interrupt is asserted

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Table 4-1901. Instance Table

Instance Name	Physical Address
CPSW	5280 181Ch

Figure 4-863. REGS_INT_REGS_INT_SS_C0_MISC_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									DED_PEND	SEC_PEND	EVNT_PEND	STAT_PEND	HOST_PEND	MDIO_LINKINT	MDIO_USERINT
NONE									R/W	R/W	R/W	R/W	R/W	R/W	R/W
0									0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-1902. REGS_INT_REGS_INT_SS_C0_MISC_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE		Reserved
6	DED_PEND	R/W	0h	Core 0 MISC DED Memory Protect Error Interrupt
5	SEC_PEND	R/W	0h	Core 0 MISC SEC Memory Protect Error Interrupt
4	EVNT_PEND	R/W	0h	Core 0 MISC CPTS Event Interrupt
3	STAT_PEND	R/W	0h	Core 0 MISC Statistics Interrupt - OR of bits n downto 0
2	HOST_PEND	R/W	0h	Core 0 MISC Host Interrupt Enable
1	MDIO_LINKINT	R/W	0h	Core 0 MISC MDIO linkint - OR of bits 1 and 0
0	MDIO_USERINT	R/W	0h	Core 0 MISC_MDIO userint interrupt - OR of bits 1 and 0

4.18.36 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C0_TH_IMAX_REG Registers

4.18.36.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C0_TH_IMAX_REG Register (Offset = 1820h) [reset = 0h]

Short Description: Core 0 THost Interrupt Max Register Register

Long Description: Core 0 THost Interrupt Max Register Register

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Table 4-1903. Instance Table

Instance Name	Physical Address
CPSW	5280 1820h

Figure 4-864. REGS_INT_REGS_INT_SS_C0_TH_IMAX_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										TH_IMAX					
NONE										R/W					
0										0h					

Access Types Legend

Table 4-1904. REGS_INT_REGS_INT_SS_C0_TH_IMAX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE		Reserved
5:0	TH_IMAX	R/W	0h	Core 0 THost Interrupt Max Register Register

4.18.37 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C0_FH_IMAX_REG Registers

4.18.37.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C0_FH_IMAX_REG Register (Offset = 1824h) [reset = 0h]

Short Description: Core 0 FHost Interrupt Max Register Register

Long Description: Core 0 FHost Interrupt Max Register Register

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Table 4-1905. Instance Table

Instance Name	Physical Address
CPSW	5280 1824h

Figure 4-865. REGS_INT_REGS_INT_SS_C0_FH_IMAX_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										FH_IMAX					
NONE										R/W					
0										0h					

Access Types Legend

Table 4-1906. REGS_INT_REGS_INT_SS_C0_FH_IMAX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE		Reserved
5:0	FH_IMAX	R/W	0h	Core 0 FHost Interrupt Max Register Register

4.18.38 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C1_TH_THRESH_PULSE_EN_REG Registers

4.18.38.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C1_TH_THRESH_PULSE_EN_REG Register (Offset = 1840h) [reset = 0h]

Short Description: Core 1 THost Threshold Pulse Interrupt Enable Register

Long Description: Core 1 THost Threshold Pulse Interrupt Enable Register

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Table 4-1907. Instance Table

Instance Name	Physical Address
CPSW	5280 1840h

Figure 4-866. REGS_INT_REGS_INT_SS_C1_TH_THRESH_PULSE_EN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TH_THRESH_PULSE_EN							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-1908. REGS_INT_REGS_INT_SS_C1_TH_THRESH_PULSE_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	TH_THRESH_PULSE_EN	R/W	0h	THost Threshold Pulse Interrupt Enable Register

4.18.39 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C1_TH_PULSE_EN_REG Registers

4.18.39.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C1_TH_PULSE_EN_REG Register (Offset = 1844h) [reset = 0h]

Short Description: Core 1 THost Pulse Interrupt Enable Register

Long Description: Core 1 THost Pulse Interrupt Enable Register

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Table 4-1909. Instance Table

Instance Name	Physical Address
CPSW	5280 1844h

Figure 4-867. REGS_INT_REGS_INT_SS_C1_TH_PULSE_EN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TH_PULSE_EN							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-1910. REGS_INT_REGS_INT_SS_C1_TH_PULSE_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	TH_PULSE_EN	R/W	0h	Core 1 THost Pulse Interrupt Enable Register

4.18.40 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C1_FH_PULSE_EN_REG Registers

4.18.40.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C1_FH_PULSE_EN_REG Register (Offset = 1848h) [reset = 0h]

Short Description: Core 1 FHost Pulse Interrupt Enable Register

Long Description: Core 1 FHost Pulse Interrupt Enable Register

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Table 4-1911. Instance Table

Instance Name	Physical Address
CPSW	5280 1848h

Figure 4-868. REGS_INT_REGS_INT_SS_C1_FH_PULSE_EN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FH_PULSE_EN							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-1912. REGS_INT_REGS_INT_SS_C1_FH_PULSE_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	FH_PULSE_EN	R/W	0h	Core 1 FHost Pulse Interrupt Enable Register

4.18.41 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C1_MISC_EN_REG Registers

4.18.41.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C1_MISC_EN_REG Register (Offset = 184Ch) [reset = 0h]

Short Description: Core 1 Misc Interrupt Enable Register

Long Description: Core 1 Misc Interrupt Enable Register

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Table 4-1913. Instance Table

Instance Name	Physical Address
CPSW	5280 184Ch

Figure 4-869. REGS_INT_REGS_INT_SS_C1_MISC_EN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									DED_PEND_EN	SEC_PEND_EN	EVNT_PEND_EN	STAT_PEND_EN	HOST_PEND_EN	MDIO_LINKINT_EN	MDIO_USERINT_EN
NONE									R/W	R/W	R/W	R/W	R/W	R/W	R/W
0									0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-1914. REGS_INT_REGS_INT_SS_C1_MISC_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE		Reserved
6	DED_PEND_EN	R/W	0h	Core 1 MISC DED Memory Protect Error Interrupt Enable
5	SEC_PEND_EN	R/W	0h	Core 1 MISC SEC Memory Protect Error Interrupt Enable
4	EVNT_PEND_EN	R/W	0h	Core 1 MISC CPTS Event Interrupt Enable
3	STAT_PEND_EN	R/W	0h	Core 1 MISC Statistics Interrupt Enable - OR of bits n downto 0
2	HOST_PEND_EN	R/W	0h	Core 1 MISC Host Interrupt Enable
1	MDIO_LINKINT_EN	R/W	0h	Core 1 MISC MDIO linkint - OR of bits 1 and 0
0	MDIO_USERINT_EN	R/W	0h	Core 1 MISC_MDIO userint interrupt enable - OR of bits 1 and 0

4.18.42 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C1_TH_THRESH_PULSE_STATUS_REG Registers

4.18.42.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C1_TH_THRESH_PULSE_STATUS_REG Register (Offset = 1850h) [reset = 0h]

Short Description: Core 1 THost Threshold Pulse Interrupt Status Register

Long Description: THost Threshold Pulse Interrupt Status Register

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Table 4-1915. Instance Table

Instance Name	Physical Address
CPSW	5280 1850h

Figure 4-870. REGS_INT_REGS_INT_SS_C1_TH_THRESH_PULSE_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TH_THRESH_PULSE_STATUS							
NONE								R							
0								0h							

Access Types Legend

Table 4-1916. REGS_INT_REGS_INT_SS_C1_TH_THRESH_PULSE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	TH_THRESH_PULSE_STATUS	R	0h	Core 1 THost Threshold Pulse Interrupt Status Register

4.18.43 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C1_TH_PULSE_STATUS_REG Registers

4.18.43.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C1_TH_PULSE_STATUS_REG Register (Offset = 1854h) [reset = 0h]

Short Description: Core 1 THost Pulse Interrupt Status Register

Long Description: THost Pulse Interrupt Status Register

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Table 4-1917. Instance Table

Instance Name	Physical Address
CPSW	5280 1854h

Figure 4-871. REGS_INT_REGS_INT_SS_C1_TH_PULSE_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TH_PULSE_STATUS							
NONE								R							
0								0h							

Access Types Legend

Table 4-1918. REGS_INT_REGS_INT_SS_C1_TH_PULSE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	TH_PULSE_STATUS	R	0h	Core 1 THost Pulse Interrupt Status Register

4.18.44 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C1_FH_PULSE_STATUS_REG Registers

4.18.44.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C1_FH_PULSE_STATUS_REG Register (Offset = 1858h) [reset = 0h]

Short Description: Core 1 FHost Pulse Interrupt Status Register

Long Description: FHost Pulse Interrupt Status Register

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Table 4-1919. Instance Table

Instance Name	Physical Address
CPSW	5280 1858h

Figure 4-872. REGS_INT_REGS_INT_SS_C1_FH_PULSE_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FH_PULSE_STATUS							
NONE								R							
0								0h							

Access Types Legend

Table 4-1920. REGS_INT_REGS_INT_SS_C1_FH_PULSE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	FH_PULSE_STATUS	R	0h	Core 1 FHost Pulse Interrupt Status Register

4.18.45 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C1_MISC_STATUS_REG Registers

4.18.45.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C1_MISC_STATUS_REG Register (Offset = 185Ch) [reset = 0h]

Short Description: Core 1 Misc Interrupt Status Register

Long Description: Misc Interrupt Status Register - Set bits in this register indicate that an enabled interrupt is asserted

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Table 4-1921. Instance Table

Instance Name	Physical Address
CPSW	5280 185Ch

Figure 4-873. REGS_INT_REGS_INT_SS_C1_MISC_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									DED_PEND	SEC_PEND	EVNT_PEND	STAT_PEND	HOST_PEND	MDIO_LINKINT	MDIO_USERINT
NONE									R/W	R/W	R/W	R/W	R/W	R/W	R/W
0									0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-1922. REGS_INT_REGS_INT_SS_C1_MISC_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE		Reserved
6	DED_PEND	R/W	0h	Core 1 MISC DED Memory Protect Error Interrupt
5	SEC_PEND	R/W	0h	Core 1 MISC SEC Memory Protect Error Interrupt
4	EVNT_PEND	R/W	0h	Core 1 MISC CPTS Event Interrupt
3	STAT_PEND	R/W	0h	Core 1 MISC Statistics Interrupt - OR of bits n downto 0
2	HOST_PEND	R/W	0h	Core 1 MISC Host Interrupt Enable
1	MDIO_LINKINT	R/W	0h	Core 1 MISC MDIO linkint - OR of bits 1 and 0
0	MDIO_USERINT	R/W	0h	Core 1 MISC_MDIO userint interrupt - OR of bits 1 and 0

4.18.46 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C1_TH_IMAX_REG Registers

4.18.46.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C1_TH_IMAX_REG Register (Offset = 1860h) [reset = 0h]

Short Description: Core 1 THost Interrupt Max Register Register

Long Description: Core 1 THost Interrupt Max Register Register

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Table 4-1923. Instance Table

Instance Name	Physical Address
CPSW	5280 1860h

Figure 4-874. REGS_INT_REGS_INT_SS_C1_TH_IMAX_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										TH_IMAX					
NONE										R/W					
0										0h					

Access Types Legend

Table 4-1924. REGS_INT_REGS_INT_SS_C1_TH_IMAX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE		Reserved
5:0	TH_IMAX	R/W	0h	Core 1 THost Interrupt Max Register Register

4.18.47 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C1_FH_IMAX_REG Registers

4.18.47.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C1_FH_IMAX_REG Register (Offset = 1864h) [reset = 0h]

Short Description: Core 1 FHost Interrupt Max Register Register

Long Description: Core 1 FHost Interrupt Max Register Register

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Table 4-1925. Instance Table

Instance Name	Physical Address
CPSW	5280 1864h

Figure 4-875. REGS_INT_REGS_INT_SS_C1_FH_IMAX_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										FH_IMAX					
NONE										R/W					
0										0h					

Access Types Legend

Table 4-1926. REGS_INT_REGS_INT_SS_C1_FH_IMAX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE		Reserved
5:0	FH_IMAX	R/W	0h	Core 1 FHost Interrupt Max Register Register

4.18.48 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C2_TH_THRESH_PULSE_EN_REG Registers

4.18.48.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C2_TH_THRESH_PULSE_EN_REG Register (Offset = 1880h) [reset = 0h]

Short Description: Core 2 THost Threshold Pulse Interrupt Enable Register

Long Description: Core 2 THost Threshold Pulse Interrupt Enable Register

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Table 4-1927. Instance Table

Instance Name	Physical Address
CPSW	5280 1880h

Figure 4-876. REGS_INT_REGS_INT_SS_C2_TH_THRESH_PULSE_EN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TH_THRESH_PULSE_EN							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-1928. REGS_INT_REGS_INT_SS_C2_TH_THRESH_PULSE_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	TH_THRESH_PULSE_EN	R/W	0h	THost Threshold Pulse Interrupt Enable Register

4.18.49 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C2_TH_PULSE_EN_REG Registers

4.18.49.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C2_TH_PULSE_EN_REG Register (Offset = 1884h) [reset = 0h]

Short Description: Core 2 THost Pulse Interrupt Enable Register

Long Description: Core 2 THost Pulse Interrupt Enable Register

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Table 4-1929. Instance Table

Instance Name	Physical Address
CPSW	5280 1884h

Figure 4-877. REGS_INT_REGS_INT_SS_C2_TH_PULSE_EN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TH_PULSE_EN							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-1930. REGS_INT_REGS_INT_SS_C2_TH_PULSE_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	TH_PULSE_EN	R/W	0h	Core 2 THost Pulse Interrupt Enable Register

4.18.50 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C2_FH_PULSE_EN_REG Registers

4.18.50.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C2_FH_PULSE_EN_REG Register (Offset = 1888h) [reset = 0h]

Short Description: Core 2 FHost Pulse Interrupt Enable Register

Long Description: Core 2 FHost Pulse Interrupt Enable Register

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Table 4-1931. Instance Table

Instance Name	Physical Address
CPSW	5280 1888h

Figure 4-878. REGS_INT_REGS_INT_SS_C2_FH_PULSE_EN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FH_PULSE_EN							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-1932. REGS_INT_REGS_INT_SS_C2_FH_PULSE_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	FH_PULSE_EN	R/W	0h	Core 2 FHost Pulse Interrupt Enable Register

4.18.51 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C2_MISC_EN_REG Registers

4.18.51.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C2_MISC_EN_REG Register (Offset = 188Ch) [reset = 0h]

Short Description: Core 2 Misc Interrupt Enable Register

Long Description: Core 2 Misc Interrupt Enable Register

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Table 4-1933. Instance Table

Instance Name	Physical Address
CPSW	5280 188Ch

Figure 4-879. REGS_INT_REGS_INT_SS_C2_MISC_EN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									DED_PEND_EN	SEC_PEND_EN	EVNT_PEND_EN	STAT_PEND_EN	HOST_PEND_EN	MDIO_LINKINT_EN	MDIO_USERINT_EN
NONE									R/W	R/W	R/W	R/W	R/W	R/W	R/W
0									0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-1934. REGS_INT_REGS_INT_SS_C2_MISC_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE		Reserved
6	DED_PEND_EN	R/W	0h	Core 2 MISC DED Memory Protect Error Interrupt Enable
5	SEC_PEND_EN	R/W	0h	Core 2 MISC SEC Memory Protect Error Interrupt Enable
4	EVNT_PEND_EN	R/W	0h	Core 2 MISC CPTS Event Interrupt Enable
3	STAT_PEND_EN	R/W	0h	Core 2 MISC Statistics Interrupt Enable - OR of bits n downto 0
2	HOST_PEND_EN	R/W	0h	Core 2 MISC Host Interrupt Enable
1	MDIO_LINKINT_EN	R/W	0h	Core 2 MISC MDIO linkint - OR of bits 1 and 0
0	MDIO_USERINT_EN	R/W	0h	Core 2 MISC_MDIO userint interrupt enable - OR of bits 1 and 0

4.18.52 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C2_TH_THRESH_PULSE_STATUS_REG Registers

4.18.52.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C2_TH_THRESH_PULSE_STATUS_REG Register (Offset = 1890h) [reset = 0h]

Short Description: Core 2 THost Threshold Pulse Interrupt Status Register

Long Description: THost Threshold Pulse Interrupt Status Register

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Table 4-1935. Instance Table

Instance Name	Physical Address
CPSW	5280 1890h

Figure 4-880. REGS_INT_REGS_INT_SS_C2_TH_THRESH_PULSE_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TH_THRESH_PULSE_STATUS							
NONE								R							
0								0h							

Access Types Legend

Table 4-1936. REGS_INT_REGS_INT_SS_C2_TH_THRESH_PULSE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	TH_THRESH_PULSE_STATUS	R	0h	Core 2 THost Threshold Pulse Interrupt Status Register

4.18.53 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C2_TH_PULSE_STATUS_REG Registers

4.18.53.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C2_TH_PULSE_STATUS_REG Register (Offset = 1894h) [reset = 0h]

Short Description: Core 2 THost Pulse Interrupt Status Register

Long Description: THost Pulse Interrupt Status Register

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Table 4-1937. Instance Table

Instance Name	Physical Address
CPSW	5280 1894h

Figure 4-881. REGS_INT_REGS_INT_SS_C2_TH_PULSE_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TH_PULSE_STATUS							
NONE								R							
0								0h							

Access Types Legend

Table 4-1938. REGS_INT_REGS_INT_SS_C2_TH_PULSE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	TH_PULSE_STATUS	R	0h	Core 2 THost Pulse Interrupt Status Register

4.18.54 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C2_FH_PULSE_STATUS_REG Registers

4.18.54.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C2_FH_PULSE_STATUS_REG Register (Offset = 1898h) [reset = 0h]

Short Description: Core 2 FHost Pulse Interrupt Status Register

Long Description: FHost Pulse Interrupt Status Register

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Table 4-1939. Instance Table

Instance Name	Physical Address
CPSW	5280 1898h

Figure 4-882. REGS_INT_REGS_INT_SS_C2_FH_PULSE_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FH_PULSE_STATUS							
NONE								R							
0								0h							

Access Types Legend

Table 4-1940. REGS_INT_REGS_INT_SS_C2_FH_PULSE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	FH_PULSE_STATUS	R	0h	Core 2 FHost Pulse Interrupt Status Register

4.18.55 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C2_MISC_STATUS_REG Registers

4.18.55.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C2_MISC_STATUS_REG Register (Offset = 189Ch) [reset = 0h]

Short Description: Core 2 Misc Interrupt Status Register

Long Description: Misc Interrupt Status Register - Set bits in this register indicate that an enabled interrupt is asserted

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Table 4-1941. Instance Table

Instance Name	Physical Address
CPSW	5280 189Ch

Figure 4-883. REGS_INT_REGS_INT_SS_C2_MISC_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									DED_PEND	SEC_PEND	EVNT_PEND	STAT_PEND	HOST_PEND	MDIO_LINKINT	MDIO_USERINT
NONE									R/W	R/W	R/W	R/W	R/W	R/W	R/W
0									0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-1942. REGS_INT_REGS_INT_SS_C2_MISC_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE		Reserved
6	DED_PEND	R/W	0h	Core 2 MISC DED Memory Protect Error Interrupt
5	SEC_PEND	R/W	0h	Core 2 MISC SEC Memory Protect Error Interrupt
4	EVNT_PEND	R/W	0h	Core 2 MISC CPTS Event Interrupt
3	STAT_PEND	R/W	0h	Core 2 MISC Statistics Interrupt - OR of bits n downto 0
2	HOST_PEND	R/W	0h	Core 2 MISC Host Interrupt Enable
1	MDIO_LINKINT	R/W	0h	Core 2 MISC MDIO linkint - OR of bits 1 and 0
0	MDIO_USERINT	R/W	0h	Core 2 MISC_MDIO userint interrupt - OR of bits 1 and 0

4.18.56 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C2_TH_IMAX_REG Registers

4.18.56.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C2_TH_IMAX_REG Register (Offset = 18A0h) [reset = 0h]

Short Description: Core 2 THost Interrupt Max Register Register

Long Description: Core 2 THost Interrupt Max Register Register

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Table 4-1943. Instance Table

Instance Name	Physical Address
CPSW	5280 18A0h

Figure 4-884. REGS_INT_REGS_INT_SS_C2_TH_IMAX_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										TH_IMAX					
NONE										R/W					
0										0h					

Access Types Legend

Table 4-1944. REGS_INT_REGS_INT_SS_C2_TH_IMAX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE		Reserved
5:0	TH_IMAX	R/W	0h	Core 2 THost Interrupt Max Register Register

4.18.57 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C2_FH_IMAX_REG Registers

4.18.57.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C2_FH_IMAX_REG Register (Offset = 18A4h) [reset = 0h]

Short Description: Core 2 FHost Interrupt Max Register Register

Long Description: Core 2 FHost Interrupt Max Register Register

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Table 4-1945. Instance Table

Instance Name	Physical Address
CPSW	5280 18A4h

Figure 4-885. REGS_INT_REGS_INT_SS_C2_FH_IMAX_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										FH_IMAX					
NONE										R/W					
0										0h					

Access Types Legend

Table 4-1946. REGS_INT_REGS_INT_SS_C2_FH_IMAX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE		Reserved
5:0	FH_IMAX	R/W	0h	Core 2 FHost Interrupt Max Register Register

4.18.58 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C3_TH_THRESH_PULSE_EN_REG Registers

4.18.58.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C3_TH_THRESH_PULSE_EN_REG Register (Offset = 18C0h) [reset = 0h]

Short Description: Core 3 THost Threshold Pulse Interrupt Enable Register

Long Description: Core 3 THost Threshold Pulse Interrupt Enable Register

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Table 4-1947. Instance Table

Instance Name	Physical Address
CPSW	5280 18C0h

Figure 4-886. REGS_INT_REGS_INT_SS_C3_TH_THRESH_PULSE_EN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TH_THRESH_PULSE_EN							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-1948. REGS_INT_REGS_INT_SS_C3_TH_THRESH_PULSE_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	TH_THRESH_PULSE_EN	R/W	0h	THost Threshold Pulse Interrupt Enable Register

4.18.59 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C3_TH_PULSE_EN_REG Registers

4.18.59.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C3_TH_PULSE_EN_REG Register (Offset = 18C4h) [reset = 0h]

Short Description: Core 3 THost Pulse Interrupt Enable Register

Long Description: Core 3 THost Pulse Interrupt Enable Register

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Table 4-1949. Instance Table

Instance Name	Physical Address
CPSW	5280 18C4h

Figure 4-887. REGS_INT_REGS_INT_SS_C3_TH_PULSE_EN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TH_PULSE_EN							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-1950. REGS_INT_REGS_INT_SS_C3_TH_PULSE_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	TH_PULSE_EN	R/W	0h	Core 3 THost Pulse Interrupt Enable Register

4.18.60 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C3_FH_PULSE_EN_REG Registers

4.18.60.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C3_FH_PULSE_EN_REG Register (Offset = 18C8h) [reset = 0h]

Short Description: Core 3 FHost Pulse Interrupt Enable Register

Long Description: Core 3 FHost Pulse Interrupt Enable Register

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Table 4-1951. Instance Table

Instance Name	Physical Address
CPSW	5280 18C8h

Figure 4-888. REGS_INT_REGS_INT_SS_C3_FH_PULSE_EN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FH_PULSE_EN							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-1952. REGS_INT_REGS_INT_SS_C3_FH_PULSE_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	FH_PULSE_EN	R/W	0h	Core 3 FHost Pulse Interrupt Enable Register

4.18.61 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C3_MISC_EN_REG Registers

4.18.61.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C3_MISC_EN_REG Register (Offset = 18CCh) [reset = 0h]

Short Description: Core 3 Misc Interrupt Enable Register

Long Description: Core 3 Misc Interrupt Enable Register

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Table 4-1953. Instance Table

Instance Name	Physical Address
CPSW	5280 18CCh

Figure 4-889. REGS_INT_REGS_INT_SS_C3_MISC_EN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									DED_PEND_EN	SEC_PEND_EN	EVNT_PEND_EN	STAT_PEND_EN	HOST_PEND_EN	MDIO_LINKINT_EN	MDIO_USERINT_EN
NONE									R/W	R/W	R/W	R/W	R/W	R/W	R/W
0									0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-1954. REGS_INT_REGS_INT_SS_C3_MISC_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE		Reserved
6	DED_PEND_EN	R/W	0h	Core 3 MISC DED Memory Protect Error Interrupt Enable
5	SEC_PEND_EN	R/W	0h	Core 3 MISC SEC Memory Protect Error Interrupt Enable
4	EVNT_PEND_EN	R/W	0h	Core 3 MISC CPTS Event Interrupt Enable
3	STAT_PEND_EN	R/W	0h	Core 3 MISC Statistics Interrupt Enable - OR of bits n downto 0
2	HOST_PEND_EN	R/W	0h	Core 3 MISC Host Interrupt Enable
1	MDIO_LINKINT_EN	R/W	0h	Core 3 MISC MDIO linkint - OR of bits 1 and 0
0	MDIO_USERINT_EN	R/W	0h	Core 3 MISC_MDIO userint interrupt enable - OR of bits 1 and 0

4.18.62 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C3_TH_THRESH_PULSE_STATUS_REG Registers

4.18.62.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C3_TH_THRESH_PULSE_STATUS_REG Register (Offset = 18D0h) [reset = 0h]

Short Description: Core 3 THost Threshold Pulse Interrupt Status Register

Long Description: THost Threshold Pulse Interrupt Status Register

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Table 4-1955. Instance Table

Instance Name	Physical Address
CPSW	5280 18D0h

Figure 4-890. REGS_INT_REGS_INT_SS_C3_TH_THRESH_PULSE_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TH_THRESH_PULSE_STATUS							
NONE								R							
0								0h							

Access Types Legend

Table 4-1956. REGS_INT_REGS_INT_SS_C3_TH_THRESH_PULSE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	TH_THRESH_PULSE_STATUS	R	0h	Core 3 THost Threshold Pulse Interrupt Status Register

4.18.63 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C3_TH_PULSE_STATUS_REG Registers

4.18.63.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C3_TH_PULSE_STATUS_REG Register (Offset = 18D4h) [reset = 0h]

Short Description: Core 3 THost Pulse Interrupt Status Register

Long Description: THost Pulse Interrupt Status Register

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Table 4-1957. Instance Table

Instance Name	Physical Address
CPSW	5280 18D4h

Figure 4-891. REGS_INT_REGS_INT_SS_C3_TH_PULSE_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TH_PULSE_STATUS							
NONE								R							
0								0h							

Access Types Legend

Table 4-1958. REGS_INT_REGS_INT_SS_C3_TH_PULSE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	TH_PULSE_STATUS	R	0h	Core 3 THost Pulse Interrupt Status Register

4.18.64 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C3_FH_PULSE_STATUS_REG Registers

4.18.64.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C3_FH_PULSE_STATUS_REG Register (Offset = 18D8h) [reset = 0h]

Short Description: Core 3 FHost Pulse Interrupt Status Register

Long Description: FHost Pulse Interrupt Status Register

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Table 4-1959. Instance Table

Instance Name	Physical Address
CPSW	5280 18D8h

Figure 4-892. REGS_INT_REGS_INT_SS_C3_FH_PULSE_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FH_PULSE_STATUS							
NONE								R							
0								0h							

Access Types Legend

Table 4-1960. REGS_INT_REGS_INT_SS_C3_FH_PULSE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	FH_PULSE_STATUS	R	0h	Core 3 FHost Pulse Interrupt Status Register

4.18.65 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C3_MISC_STATUS_REG Registers

4.18.65.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C3_MISC_STATUS_REG Register (Offset = 18DCh) [reset = 0h]

Short Description: Core 3 Misc Interrupt Status Register

Long Description: Misc Interrupt Status Register - Set bits in this register indicate that an enabled interrupt is asserted

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Table 4-1961. Instance Table

Instance Name	Physical Address
CPSW	5280 18DCh

Figure 4-893. REGS_INT_REGS_INT_SS_C3_MISC_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									DED_PEND	SEC_PEND	EVNT_PEND	STAT_PEND	HOST_PEND	MDIO_LINKINT	MDIO_USERINT
NONE									R/W	R/W	R/W	R/W	R/W	R/W	R/W
0									0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-1962. REGS_INT_REGS_INT_SS_C3_MISC_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE		Reserved
6	DED_PEND	R/W	0h	Core 3 MISC DED Memory Protect Error Interrupt
5	SEC_PEND	R/W	0h	Core 3 MISC SEC Memory Protect Error Interrupt
4	EVNT_PEND	R/W	0h	Core 3 MISC CPTS Event Interrupt
3	STAT_PEND	R/W	0h	Core 3 MISC Statistics Interrupt - OR of bits n downto 0
2	HOST_PEND	R/W	0h	Core 3 MISC Host Interrupt Enable
1	MDIO_LINKINT	R/W	0h	Core 3 MISC MDIO linkint - OR of bits 1 and 0
0	MDIO_USERINT	R/W	0h	Core 3 MISC_MDIO userint interrupt - OR of bits 1 and 0

4.18.66 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C3_TH_IMAX_REG Registers

4.18.66.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C3_TH_IMAX_REG Register (Offset = 18E0h) [reset = 0h]

Short Description: Core 3 THost Interrupt Max Register Register

Long Description: Core 3 THost Interrupt Max Register Register

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Table 4-1963. Instance Table

Instance Name	Physical Address
CPSW	5280 18E0h

Figure 4-894. REGS_INT_REGS_INT_SS_C3_TH_IMAX_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										TH_IMAX					
NONE										R/W					
0										0h					

Access Types Legend

Table 4-1964. REGS_INT_REGS_INT_SS_C3_TH_IMAX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE		Reserved
5:0	TH_IMAX	R/W	0h	Core 3 THost Interrupt Max Register Register

4.18.67 CPSW_NCSS_VBUSP_REGS_INT_REGS_INT_SS_C3_FH_IMAX_REG Registers

4.18.67.1 CPSW_VBUSP_REGS_INT_REGS_INT_SS_C3_FH_IMAX_REG Register (Offset = 18E4h) [reset = 0h]

Short Description: Core 3 FHost Interrupt Max Register Register

Long Description: Core 3 FHost Interrupt Max Register Register

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Table 4-1965. Instance Table

Instance Name	Physical Address
CPSW	5280 18E4h

Figure 4-895. REGS_INT_REGS_INT_SS_C3_FH_IMAX_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										FH_IMAX					
NONE										R/W					
0										0h					

Access Types Legend

Table 4-1966. REGS_INT_REGS_INT_SS_C3_FH_IMAX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE		Reserved
5:0	FH_IMAX	R/W	0h	Core 3 FHost Interrupt Max Register Register

4.18.68 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_ID_VER_REG Registers

4.18.68.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_ID_VER_REG Register (Offset = 20000h) [reset = 6b901103h]

Short Description: idver_reg

Long Description: CPSW ID Version

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Table 4-1967. Instance Table

Instance Name	Physical Address
CPSW	5282 0000h

Figure 4-896. CPSW_NC_CPSW_NC_CPSW_ID_VER_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IDENT															
R															
6b90h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL_VER					MAJOR_VER			MINOR_VER							
R					R			R							
2h					1h			3h							

Access Types Legend

Table 4-1968. CPSW_NC_CPSW_NC_CPSW_ID_VER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IDENT	R	6B90h	Identification Value
15:11	RTL_VER	R	2h	RTL Version Value
10:8	MAJOR_VER	R	1h	Major Version Value
7:0	MINOR_VER	R	3h	Minor Version Value

4.18.69 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CONTROL_REG Registers

4.18.69.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CONTROL_REG Register (Offset = 20004h) [reset = 0h]

Short Description: control_reg

Long Description: CPSW Switch Control

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Table 4-1969. Instance Table

Instance Name	Physical Address
CPSW	5282 0004h

Figure 4-897. CPSW_NC_CPSW_NC_CONTROL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_CRC_MODE	RESERVED												EST_ENABLE	RESERVED	EEE_ENABLE
R/W	NONE												R/W	R/W	R/W
0h	0												0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P0_RX_PASS_CRC_ERR	P0_RX_PAD	P0_TX_CRC_REMOVE	RESERVED	P8_PASS_PRI_TAGGED	P7_PASS_PRI_TAGGED	P6_PASS_PRI_TAGGED	P5_PASS_PRI_TAGGED	P4_PASS_PRI_TAGGED	P3_PASS_PRI_TAGGED	P2_PASS_PRI_TAGGED	P1_PASS_PRI_TAGGED	P0_PASS_PRI_TAGGED	P0_ENABLE	VLAN_AWARE	S_CN_SWITCH
R/W	R/W	R/W	NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-1970. CPSW_NC_CPSW_NC_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ECC_CRC_MODE	R/W	0h	ECC CRC Mode
30:19	RESERVED	NONE		Reserved
18	EST_ENABLE	R/W	0h	Intersperced Express Traffic enable
17	RESERVED	R/W		RESERVED
16	EEE_ENABLE	R/W	0h	Energy Efficient Ethernet enable
15	P0_RX_PASS_CRC_ERR	R/W	0h	Port 0 Pass Received CRC errors
14	P0_RX_PAD	R/W	0h	Port 0 Receive Short Packet Pad
13	P0_TX_CRC_REMOVE	R/W	0h	Port 0 Transmit CRC remove
12	RESERVED	NONE		Reserved
11	P8_PASS_PRI_TAGGED	R/W	0h	Port 8 Pass Priority Tagged
10	P7_PASS_PRI_TAGGED	R/W	0h	Port 7 Pass Priority Tagged
9	P6_PASS_PRI_TAGGED	R/W	0h	Port 6 Pass Priority Tagged
8	P5_PASS_PRI_TAGGED	R/W	0h	Port 5 Pass Priority Tagged
7	P4_PASS_PRI_TAGGED	R/W	0h	Port 4 Pass Priority Tagged
6	P3_PASS_PRI_TAGGED	R/W	0h	Port 3 Pass Priority Tagged
5	P2_PASS_PRI_TAGGED	R/W	0h	Port 2 Pass Priority Tagged
4	P1_PASS_PRI_TAGGED	R/W	0h	Port 1 Pass Priority Tagged
3	P0_PASS_PRI_TAGGED	R/W	0h	Port 0 Pass Priority Tagged
2	P0_ENABLE	R/W	0h	Port 0 Enable
1	VLAN_AWARE	R/W	0h	VLAN Aware Mode

Table 4-1970. CPSW_NC_CPSW_NC_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	S_CN_SWITCH	R/W	0h	VLAN Aware Mode

4.18.70 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_EM_CONTROL_REG Registers

4.18.70.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_EM_CONTROL_REG Register (Offset = 20010h) [reset = 0h]

Short Description: em_control_reg

Long Description: CPSW Emulation Control

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Table 4-1971. Instance Table

Instance Name	Physical Address
CPSW	5282 0010h

Figure 4-898. CPSW_NC_CPSW_NC_EM_CONTROL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														SOFT	FREE
NONE														R/W	R/W
0														0h	0h

Access Types Legend

Table 4-1972. CPSW_NC_CPSW_NC_EM_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1	SOFT	R/W	0h	Emulation Soft Bit
0	FREE	R/W	0h	Emulation Free Bit

4.18.71 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_STAT_PORT_EN_REG Registers

4.18.71.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_STAT_PORT_EN_REG Register (Offset = 20014h) [reset = 0h]

Short Description: stat_port_en_reg

Long Description: CPSW Statistics Port Enable

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Table 4-1973. Instance Table

Instance Name	Physical Address
CPSW	5282 0014h

Figure 4-899. CPSW_NC_CPSW_NC_STAT_PORT_EN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							P8_STAT_EN	P7_STAT_EN	P6_STAT_EN	P5_STAT_EN	P4_STAT_EN	P3_STAT_EN	P2_STAT_EN	P1_STAT_EN	P0_STAT_EN
NONE							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0							0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-1974. CPSW_NC_CPSW_NC_STAT_PORT_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE		Reserved
8	P8_STAT_EN	R/W	0h	Port 8 Statistics Enable
7	P7_STAT_EN	R/W	0h	Port 7 Statistics Enable
6	P6_STAT_EN	R/W	0h	Port 6 Statistics Enable
5	P5_STAT_EN	R/W	0h	Port 5 Statistics Enable
4	P4_STAT_EN	R/W	0h	Port 4 Statistics Enable
3	P3_STAT_EN	R/W	0h	Port 3 Statistics Enable
2	P2_STAT_EN	R/W	0h	Port 2 Statistics Enable
1	P1_STAT_EN	R/W	0h	Port 1 Statistics Enable
0	P0_STAT_EN	R/W	0h	Port 0 Statistics Enable

4.18.72 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_PTYPE_REG Registers

4.18.72.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_PTYPE_REG Register (Offset = 20018h) [reset = 0h]

Short Description: ptype_reg

Long Description: CPSW Transmit Priority Type

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Table 4-1975. Instance Table

Instance Name	Physical Address
CPSW	5282 0018h

Figure 4-900. CPSW_NC_CPSW_NC_PTYPE_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															P8_PTYPE_ESC
NONE															R/W
0															0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P7_PTYPE_ESC	P6_PTYPE_ESC	P5_PTYPE_ESC	P4_PTYPE_ESC	P3_PTYPE_ESC	P2_PTYPE_ESC	P1_PTYPE_ESC	P0_PTYPE_ESC	RESERVED			ESC_PRI_LD_VAL				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	NONE			R/W				
0h	0h	0h	0h	0h	0h	0h	0h	0			0h				

Access Types Legend

Table 4-1976. CPSW_NC_CPSW_NC_PTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE		Reserved
16	P8_PTYPE_ESC	R/W	0h	Port 8 Priority Type Escalate
15	P7_PTYPE_ESC	R/W	0h	Port 7 Priority Type Escalate
14	P6_PTYPE_ESC	R/W	0h	Port 6 Priority Type Escalate
13	P5_PTYPE_ESC	R/W	0h	Port 5 Priority Type Escalate
12	P4_PTYPE_ESC	R/W	0h	Port 4 Priority Type Escalate
11	P3_PTYPE_ESC	R/W	0h	Port 3 Priority Type Escalate
10	P2_PTYPE_ESC	R/W	0h	Port 2 Priority Type Escalate
9	P1_PTYPE_ESC	R/W	0h	Port 1 Priority Type Escalate
8	P0_PTYPE_ESC	R/W	0h	Port 0 Priority Type Escalate
7:5	RESERVED	NONE		Reserved
4:0	ESC_PRI_LD_VAL	R/W	0h	Escalate Priority Load Value

4.18.73 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_SOFT_IDLE_REG Registers

4.18.73.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_SOFT_IDLE_REG Register (Offset = 2001Ch) [reset = 0h]

Short Description: soft_idle_reg

Long Description: CPSW Software Idle

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Table 4-1977. Instance Table

Instance Name	Physical Address
CPSW	5282 001Ch

Figure 4-901. CPSW_NC_CPSW_NC_SOFT_IDLE_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															SOFT_IDLE
NONE															R/W
0															0h

Access Types Legend

Table 4-1978. CPSW_NC_CPSW_NC_SOFT_IDLE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	SOFT_IDLE	R/W	0h	Software Idle

4.18.74 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_THRU_RATE_REG Registers

4.18.74.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_THRU_RATE_REG Register (Offset = 20020h) [reset = 3001h]

Short Description: thru_rate_reg

Long Description: CPSW Thru Rate

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Table 4-1979. Instance Table

Instance Name	Physical Address
CPSW	5282 0020h

Figure 4-902. CPSW_NC_CPSW_NC_THRU_RATE_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
1001d1bf800															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SL_RX_THRU_RATE				RESERVED								P0_RX_THRU_RATE			
R/W				NONE								R/W			
3h				0								1h			

Access Types Legend

Table 4-1980. CPSW_NC_CPSW_NC_THRU_RATE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:12	SL_RX_THRU_RATE	R/W	3h	Switch FIFO receive through rate
11:4	RESERVED	NONE		Reserved
3:0	P0_RX_THRU_RATE	R/W	1h	CPPI FIFO receive through rate

4.18.75 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_GAP_THRESH_REG Registers

4.18.75.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_GAP_THRESH_REG Register (Offset = 20024h) [reset = bh]

Short Description: gap_thresh_reg

Long Description: CPSW Transmit FIFO Short Gap Threshold

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Table 4-1981. Instance Table

Instance Name	Physical Address
CPSW	5282 0024h

Figure 4-903. CPSW_NC_CPSW_NC_GAP_THRESH_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
65															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											GAP_THRESH				
NONE											R/W				
65											bh				

Access Types Legend

Table 4-1982. CPSW_NC_CPSW_NC_GAP_THRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	GAP_THRESH	R/W	Bh	Short Gap Threshold

4.18.76 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_TX_START_WDS_REG Registers

4.18.76.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_TX_START_WDS_REG Register (Offset = 20028h) [reset = 8h]

Short Description: tx_start_wds_reg

Long Description: Transmit Start Words

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Table 4-1983. Instance Table

Instance Name	Physical Address
CPSW	5282 0028h

Figure 4-904. CPSW_NC_CPSW_NC_TX_START_WDS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
64															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					TX_START_WDS										
NONE					R/W										
64					8h										

Access Types Legend

Table 4-1984. CPSW_NC_CPSW_NC_TX_START_WDS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE		Reserved
10:0	TX_START_WDS	R/W	8h	Transmit Start Words

4.18.77 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_EEE_PRESCALE_REG Registers

4.18.77.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_EEE_PRESCALE_REG Register (Offset = 2002Ch) [reset = 0h]

Short Description: eee_prescale_reg

Long Description: CPSW Energy Efficient Ethernet Prescale Value

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Table 4-1985. Instance Table

Instance Name	Physical Address
CPSW	5282 002Ch

Figure 4-905. CPSW_NC_CPSW_NC_EEE_PRESCALE_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				EEE_PRESCALE											
NONE				R/W											
0				0h											

Access Types Legend

Table 4-1986. CPSW_NC_CPSW_NC_EEE_PRESCALE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE		Reserved
11:0	EEE_PRESCALE	R/W	0h	Energy Efficient Ethernet Pre-scale count load value

4.18.78 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_TX_G_OFLOW_THRESH_SET_REG Registers

4.18.78.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_TX_G_OFLOW_THRESH_SET_REG Register (Offset = 20030h) [reset = ffffffffh]

Short Description: tx_g_oflow_thresh_set_reg

Long Description: CPSW PFC Tx Global Out Flow Threshold Set

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Table 4-1987. Instance Table

Instance Name	Physical Address
CPSW	5282 0030h

Figure 4-906. CPSW_NC_CPSW_NC_TX_G_OFLOW_THRESH_SET_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRI7				PRI6				PRI5				PRI4			
R/W				R/W				R/W				R/W			
fh				fh				fh				fh			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI3				PRI2				PRI1				PRI0			
R/W				R/W				R/W				R/W			
fh				fh				fh				fh			

Access Types Legend

Table 4-1988. CPSW_NC_CPSW_NC_TX_G_OFLOW_THRESH_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PRI7	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 7
27:24	PRI6	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 6
23:20	PRI5	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 5
19:16	PRI4	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 4
15:12	PRI3	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 3
11:8	PRI2	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 2
7:4	PRI1	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 1
3:0	PRI0	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 0

4.18.79 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_TX_G_OFLOW_THRESH_CLR_REG Registers

4.18.79.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_TX_G_OFLOW_THRESH_CLR_REG Register (Offset = 20034h) [reset = 0h]

Short Description: tx_g_oflow_thresh_clr_reg

Long Description: CPSW PFC Tx Global Out Flow Threshold Clear

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Table 4-1989. Instance Table

Instance Name	Physical Address
CPSW	5282 0034h

Figure 4-907. CPSW_NC_CPSW_NC_TX_G_OFLOW_THRESH_CLR_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRI7				PRI6				PRI5				PRI4			
R/W				R/W				R/W				R/W			
0h				0h				0h				0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI3				PRI2				PRI1				PRI0			
R/W				R/W				R/W				R/W			
0h				0h				0h				0h			

Access Types Legend

Table 4-1990. CPSW_NC_CPSW_NC_TX_G_OFLOW_THRESH_CLR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PRI7	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 7
27:24	PRI6	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 6
23:20	PRI5	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 5
19:16	PRI4	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 4
15:12	PRI3	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 3
11:8	PRI2	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 2
7:4	PRI1	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 1
3:0	PRI0	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 0

4.18.80 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_TX_G_BUF_THRESH_SET_L_REG Registers

4.18.80.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_TX_G_BUF_THRESH_SET_L_REG Register (Offset = 20038h) [reset = ffffffffh]

Short Description: tx_g_buf_thresh_set_l_reg

Long Description: CPSW PFC Global Tx Buffer Threshold Set Low

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Table 4-1991. Instance Table

Instance Name	Physical Address
CPSW	5282 0038h

Figure 4-908. CPSW_NC_CPSW_NC_TX_G_BUF_THRESH_SET_L_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRI3								PRI2							
R/W								R/W							
ffh								ffh							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI1								PRI0							
R/W								R/W							
ffh								ffh							

Access Types Legend

Table 4-1992. CPSW_NC_CPSW_NC_TX_G_BUF_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PRI3	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 3
23:16	PRI2	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 2
15:8	PRI1	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 1
7:0	PRI0	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 0

4.18.81 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_TX_G_BUF_THRESH_SET_H_REG Registers

4.18.81.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_TX_G_BUF_THRESH_SET_H_REG Register (Offset = 2003Ch) [reset = ffffffffh]

Short Description: tx_g_buf_thresh_set_h_reg

Long Description: CPSW PFC Global Tx Buffer Threshold Set High

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Table 4-1993. Instance Table

Instance Name	Physical Address
CPSW	5282 003Ch

Figure 4-909. CPSW_NC_CPSW_NC_TX_G_BUF_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRI7								PRI6							
R/W								R/W							
ffh								ffh							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI5								PRI4							
R/W								R/W							
ffh								ffh							

Access Types Legend

Table 4-1994. CPSW_NC_CPSW_NC_TX_G_BUF_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PRI7	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 7
23:16	PRI6	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 6
15:8	PRI5	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 5
7:0	PRI4	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 4

4.18.82 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_TX_G_BUF_THRESH_CLR_L_REG Registers

4.18.82.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_TX_G_BUF_THRESH_CLR_L_REG Register (Offset = 20040h) [reset = 0h]

Short Description: tx_g_buf_thresh_clr_l_reg

Long Description: CPSW PFC Global Tx Buffer Threshold Clear Low

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Table 4-1995. Instance Table

Instance Name	Physical Address
CPSW	5282 0040h

Figure 4-910. CPSW_NC_CPSW_NC_TX_G_BUF_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRI3								PRI2							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI1								PRI0							
R/W								R/W							
0h								0h							

Access Types Legend

Table 4-1996. CPSW_NC_CPSW_NC_TX_G_BUF_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PRI3	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 3
23:16	PRI2	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 2
15:8	PRI1	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 1
7:0	PRI0	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 0

4.18.83 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_TX_G_BUF_THRESH_CLR_H_REG Registers

4.18.83.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_TX_G_BUF_THRESH_CLR_H_REG Register (Offset = 20044h) [reset = 0h]

Short Description: tx_g_buf_thresh_clr_h_reg

Long Description: CPSW PFC Global Tx Buffer Threshold Clear High

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Table 4-1997. Instance Table

Instance Name	Physical Address
CPSW	5282 0044h

Figure 4-911. CPSW_NC_CPSW_NC_TX_G_BUF_THRESH_CLR_H_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRI7								PRI6							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI5								PRI4							
R/W								R/W							
0h								0h							

Access Types Legend

Table 4-1998. CPSW_NC_CPSW_NC_TX_G_BUF_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PRI7	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 7
23:16	PRI6	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 6
15:8	PRI5	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 5
7:0	PRI4	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 4

4.18.84 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_VLAN_LTYPE_REG Registers

4.18.84.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_VLAN_LTYPE_REG Register (Offset = 20050h) [reset = 88a88100h]

Short Description: vlan_ltype_reg

Long Description: VLAN Length/type

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Table 4-1999. Instance Table

Instance Name	Physical Address
CPSW	5282 0050h

Figure 4-912. CPSW_NC_CPSW_NC_VLAN_LTYPE_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VLAN_LTYPE_OUTER															
R/W															
88a8h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VLAN_LTYPE_INNER															
R/W															
8100h															

Access Types Legend

Table 4-2000. CPSW_NC_CPSW_NC_VLAN_LTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	VLAN_LTYPE_OUTER	R/W	88A8h	Outer VLAN LType
15:0	VLAN_LTYPE_INNER	R/W	8100h	Inner VLAN LType

4.18.85 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_EST_TS_DOMAIN_REG Registers

4.18.85.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_EST_TS_DOMAIN_REG Register (Offset = 20054h) [reset = 0h]

Short Description: est_ts_domain_reg

Long Description: Enhanced Scheduled Traffic Host Event Domain

Return to Summary Table

Table 4-2001. Instance Table

Instance Name	Physical Address
CPSW	5282 0054h

Figure 4-913. CPSW_NC_CPSW_NC_EST_TS_DOMAIN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								EST_TS_DOMAIN							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-2002. CPSW_NC_CPSW_NC_EST_TS_DOMAIN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	EST_TS_DOMAIN	R/W	0h	Enhanced Scheduled Traffic Host Event Domain

4.18.86 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_TX_PRI0_MAXLEN_REG Registers

4.18.86.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_TX_PRI0_MAXLEN_REG Register (Offset = 20100h) [reset = 7e8h]

Short Description: tx_pri0_maxlen_reg

Long Description: Transmit Priority 0 Maximum Length

Return to Summary Table

Table 4-2003. Instance Table

Instance Name	Physical Address
CPSW	5282 0100h

Figure 4-914. CPSW_NC_CPSW_NC_TX_PRI0_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
423a31d4															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TX_PRI0_MAXLEN													
NONE		R/W													
423a31d4		7e8h													

Access Types Legend

Table 4-2004. CPSW_NC_CPSW_NC_TX_PRI0_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE		Reserved
13:0	TX_PRI0_MAXLEN	R/W	7E8h	Transmit Priority 0 Maximum Length

4.18.87 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_TX_PRI1_MAXLEN_REG Registers

4.18.87.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_TX_PRI1_MAXLEN_REG Register (Offset = 20104h) [reset = 7e8h]

Short Description: tx_pri1_maxlen_reg

Long Description: Transmit Priority 1 Maximum Length

Return to Summary Table

Table 4-2005. Instance Table

Instance Name	Physical Address
CPSW	5282 0104h

Figure 4-915. CPSW_NC_CPSW_NC_TX_PRI1_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
423a31d4															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TX_PRI1_MAXLEN													
NONE		R/W													
423a31d4		7e8h													

Access Types Legend

Table 4-2006. CPSW_NC_CPSW_NC_TX_PRI1_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE		Reserved
13:0	TX_PRI1_MAXLEN	R/W	7E8h	Transmit Priority 1 Maximum Length

4.18.88 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_TX_PRI2_MAXLEN_REG Registers

4.18.88.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_TX_PRI2_MAXLEN_REG Register (Offset = 20108h) [reset = 7e8h]

Short Description: tx_pri2_maxlen_reg

Long Description: Transmit Priority 2 Maximum Length

Return to Summary Table

Table 4-2007. Instance Table

Instance Name	Physical Address
CPSW	5282 0108h

Figure 4-916. CPSW_NC_CPSW_NC_TX_PRI2_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
423a31d4															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TX_PRI2_MAXLEN													
NONE		R/W													
423a31d4		7e8h													

Access Types Legend

Table 4-2008. CPSW_NC_CPSW_NC_TX_PRI2_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE		Reserved
13:0	TX_PRI2_MAXLEN	R/W	7E8h	Transmit Priority 2 Maximum Length

4.18.89 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_TX_PRI3_MAXLEN_REG Registers

4.18.89.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_TX_PRI3_MAXLEN_REG Register (Offset = 2010Ch) [reset = 7e8h]

Short Description: tx_pri3_maxlen_reg

Long Description: Transmit Priority 3 Maximum Length

Return to Summary Table

Table 4-2009. Instance Table

Instance Name	Physical Address
CPSW	5282 010Ch

Figure 4-917. CPSW_NC_CPSW_NC_TX_PRI3_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
423a31d4															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TX_PRI3_MAXLEN													
NONE		R/W													
423a31d4		7e8h													

Access Types Legend

Table 4-2010. CPSW_NC_CPSW_NC_TX_PRI3_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE		Reserved
13:0	TX_PRI3_MAXLEN	R/W	7E8h	Transmit Priority 3 Maximum Length

4.18.90 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_TX_PRI4_MAXLEN_REG Registers

4.18.90.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_TX_PRI4_MAXLEN_REG Register (Offset = 20110h) [reset = 7e8h]

Short Description: tx_pri4_maxlen_reg

Long Description: Transmit Priority 4 Maximum Length

Return to Summary Table

Table 4-2011. Instance Table

Instance Name	Physical Address
CPSW	5282 0110h

Figure 4-918. CPSW_NC_CPSW_NC_TX_PRI4_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
423a31d4															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TX_PRI4_MAXLEN													
NONE		R/W													
423a31d4		7e8h													

Access Types Legend

Table 4-2012. CPSW_NC_CPSW_NC_TX_PRI4_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE		Reserved
13:0	TX_PRI4_MAXLEN	R/W	7E8h	Transmit Priority 4 Maximum Length

4.18.91 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_TX_PRI5_MAXLEN_REG Registers

4.18.91.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_TX_PRI5_MAXLEN_REG Register (Offset = 20114h) [reset = 7e8h]

Short Description: tx_pri5_maxlen_reg

Long Description: Transmit Priority 5 Maximum Length

Return to Summary Table

Table 4-2013. Instance Table

Instance Name	Physical Address
CPSW	5282 0114h

Figure 4-919. CPSW_NC_CPSW_NC_TX_PRI5_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
423a31d4															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TX_PRI5_MAXLEN													
NONE		R/W													
423a31d4		7e8h													

Access Types Legend

Table 4-2014. CPSW_NC_CPSW_NC_TX_PRI5_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE		Reserved
13:0	TX_PRI5_MAXLEN	R/W	7E8h	Transmit Priority 5 Maximum Length

4.18.92 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_TX_PRI6_MAXLEN_REG Registers

4.18.92.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_TX_PRI6_MAXLEN_REG Register (Offset = 20118h) [reset = 7e8h]

Short Description: tx_pri6_maxlen_reg

Long Description: Transmit Priority 6 Maximum Length

Return to Summary Table

Table 4-2015. Instance Table

Instance Name	Physical Address
CPSW	5282 0118h

Figure 4-920. CPSW_NC_CPSW_NC_TX_PRI6_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
423a31d4															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TX_PRI6_MAXLEN													
NONE		R/W													
423a31d4		7e8h													

Access Types Legend

Table 4-2016. CPSW_NC_CPSW_NC_TX_PRI6_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE		Reserved
13:0	TX_PRI6_MAXLEN	R/W	7E8h	Transmit Priority 6 Maximum Length

4.18.93 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_TX_PRI7_MAXLEN_REG Registers

4.18.93.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_TX_PRI7_MAXLEN_REG Register (Offset = 2011Ch) [reset = 7e8h]

Short Description: tx_pri7_maxlen_reg

Long Description: Transmit Priority 7 Maximum Length

Return to Summary Table

Table 4-2017. Instance Table

Instance Name	Physical Address
CPSW	5282 011Ch

Figure 4-921. CPSW_NC_CPSW_NC_TX_PRI7_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
423a31d4															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TX_PRI7_MAXLEN													
NONE		R/W													
423a31d4		7e8h													

Access Types Legend

Table 4-2018. CPSW_NC_CPSW_NC_TX_PRI7_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE		Reserved
13:0	TX_PRI7_MAXLEN	R/W	7E8h	Transmit Priority 7 Maximum Length

4.18.94 CPSW_NCSS_VBUSP_MDIO_MDIO_USER_GROUP_USER_ACCESS_REG_J Registers

4.18.94.1 CPSW_VBUSP_MDIO_MDIO_USER_GROUP_USER_ACCESS_REG_J Register (Offset = F80h) [reset = 0h]

Short Description: user_access_reg

Long Description: MDIO User Access Register

Return to Summary Table

Offset = f80h + (j * 8h); where j = 0h to 1h

Table 4-2019. Instance Table

Instance Name	Physical Address
CPSW	5280 0F80h

Figure 4-922. MDIO_MDIO_USER_GROUP_USER_ACCESS_REG_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GO	WRITE	ACK	RESERVED			REGADR					PHYADR				
R/W	R/W	R/W	NONE			R/W					R/W				
0h	0h	0h	0			0h					0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA															
R/W															
0h															

Access Types Legend

Table 4-2020. MDIO_MDIO_USER_GROUP_USER_ACCESS_REG_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GO	R/W	0h	Go
30	WRITE	R/W	0h	Write
29	ACK	R/W	0h	Acknowledge
28:26	RESERVED	NONE		Reserved
25:21	REGADR	R/W	0h	Register address
20:16	PHYADR	R/W	0h	PHY address
15:0	DATA	R/W	0h	User data

4.18.95 CPSW_NCSS_VBUSP_MDIO_MDIO_USER_GROUP_USER_PHY_SEL_REG_J Registers

4.18.95.1 CPSW_VBUSP_MDIO_MDIO_USER_GROUP_USER_PHY_SEL_REG_J Register (Offset = F84h) [reset = 0h]

Short Description: user_phy_sel_reg

Long Description: MDIO User PHY Select Register

Return to Summary Table

Offset = f84h + (j * 8h); where j = 0h to 1h

Table 4-2021. Instance Table

Instance Name	Physical Address
CPSW	5280 0F84h

Figure 4-923. MDIO_MDIO_USER_GROUP_USER_PHY_SEL_REG_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								LINKSEL	LINKINT_ENABLE	RESERVED	PHYADR_MON				
NONE								R/W	R/W	NONE	R/W				
0								0h	0h	0	0h				

Access Types Legend

Table 4-2022. MDIO_MDIO_USER_GROUP_USER_PHY_SEL_REG_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7	LINKSEL	R/W	0h	Link status determination select
6	LINKINT_ENABLE	R/W	0h	Link change interrupt enable
5	RESERVED	NONE		Reserved
4:0	PHYADR_MON	R/W	0h	PHY address whose link status is monitored

4.18.96 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_CONTROL_REG Registers

4.18.96.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_CONTROL_REG Register (Offset = 21004h) [reset = 0h]

Short Description: p0_control_reg

Long Description: CPPI Port 0 Control

Return to Summary Table

Table 4-2023. Instance Table

Instance Name	Physical Address
CPSW	5282 1004h

Figure 4-924. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_CONTROL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED													RX_REMAP_DSCP_V6	RX_REMAP_DSCP_V4	RX_REMAP_VLAN
NONE													R/W	R/W	R/W
0													0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_ECC_ERR_EN	TX_ECC_ERR_EN	RESERVED										TX_CHECKSUM_EN	DSCP_IPV6_EN	DSCP_IPV4_EN	RX_CHECKSUM_EN
R/W	R/W	NONE										R/W	R/W	R/W	R/W
0h	0h	0										0h	0h	0h	0h

Access Types Legend

Table 4-2024. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE		Reserved
18	RX_REMAP_DSCP_V6	R/W	0h	Port 0 Remap DSCP_V6 Enable
17	RX_REMAP_DSCP_V4	R/W	0h	Port 0 Remap DSCP_V4 Enable
16	RX_REMAP_VLAN	R/W	0h	Port 0 Remap VLAN Enable
15	RX_ECC_ERR_EN	R/W	0h	Port 0 Receive ECC Error Enable
14	TX_ECC_ERR_EN	R/W	0h	Port 0 Transmit ECC Error Enable
13:4	RESERVED	NONE		Reserved
3	TX_CHECKSUM_EN	R/W	0h	Port 0 Transmit Checksum Enable
2	DSCP_IPV6_EN	R/W	0h	Port 0 IPv6 DSCP enable
1	DSCP_IPV4_EN	R/W	0h	Port 0 IPv4 DSCP enable
0	RX_CHECKSUM_EN	R/W	0h	Port 0 Receive Checksum Enable

4.18.97 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_FLOW_ID_OFFSET_REG Registers

4.18.97.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_FLOW_ID_OFFSET_REG Register (Offset = 21008h) [reset = 0h]

Short Description: p0_flow_id_offset_reg

Long Description: CPPI Port 0 Flow ID Offset

Return to Summary Table

Table 4-2025. Instance Table

Instance Name	Physical Address
CPSW	5282 1008h

Figure 4-925. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_FLOW_ID_OFFSET_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		VALUE													
NONE		R/W													
0		0h													

Access Types Legend

Table 4-2026. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_FLOW_ID_OFFSET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE		Reserved
13:0	VALUE	R/W	0h	This value is added to the thread/Flow_ID in CPPI transmit PSI Info Word 0

4.18.98 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_BLK_CNT_REG Registers

4.18.98.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_BLK_CNT_REG Register (Offset = 21010h) [reset = 1h]

Short Description: p0_blk_cnt_reg

Long Description: CPPI Port 0 FIFO Block Usage Count

Return to Summary Table

Table 4-2027. Instance Table

Instance Name	Physical Address
CPSW	5282 1010h

Figure 4-926. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_BLK_CNT_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			TX_BLK_CNT					RESERVED		RX_BLK_CNT					
NONE			R					NONE		R					
0			0h					0		1h					

Access Types Legend

Table 4-2028. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_BLK_CNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE		Reserved
12:8	TX_BLK_CNT	R	0h	Port 0 Transmit Block Count Usage
7:6	RESERVED	NONE		Reserved
5:0	RX_BLK_CNT	R	1h	Port 0 Receive Block Count Usage

4.18.99 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_PORT_VLAN_REG Registers

4.18.99.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_PORT_VLAN_REG Register (Offset = 21014h) [reset = 0h]

Short Description: p0_port_vlan_reg

Long Description: CPPI Port 0 VLAN

Return to Summary Table

Table 4-2029. Instance Table

Instance Name	Physical Address
CPSW	5282 1014h

Figure 4-927. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_PORT_VLAN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PORT_PRI			PORT_CFI	PORT_VID											
R/W			R/W	R/W											
0h			0h	0h											

Access Types Legend

Table 4-2030. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_PORT_VLAN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:13	PORT_PRI	R/W	0h	Port VLAN Priority
12	PORT_CFI	R/W	0h	Port CFI bit
11:0	PORT_VID	R/W	0h	Port VLAN ID

4.18.100 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_PRI_MAP_REG Registers

4.18.100.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_PRI_MAP_REG Register (Offset = 21018h) [reset = 76543210h]

Short Description: p0_tx_pri_map_reg

Long Description: CPPI Port 0 Tx Header Pri to Switch Pri Mapping

Return to Summary Table

Table 4-2031. Instance Table

Instance Name	Physical Address
CPSW	5282 1018h

Figure 4-928. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		PRI7		RESERVED		PRI6		RESERVED		PRI5		RESERVED		PRI4	
NONE		R/W		NONE		R/W		NONE		R/W		NONE		R/W	
0		7h		1		6h		0		5h		1		4h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		PRI3		RESERVED		PRI2		RESERVED		PRI1		RESERVED		PRI0	
NONE		R/W		NONE		R/W		NONE		R/W		NONE		R/W	
0		3h		1		2h		0		1h		1		0h	

Access Types Legend

Table 4-2032. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE		Reserved
30:28	PRI7	R/W	7h	Priority 7
27	RESERVED	NONE		Reserved
26:24	PRI6	R/W	6h	Priority 6
23	RESERVED	NONE		Reserved
22:20	PRI5	R/W	5h	Priority 5
19	RESERVED	NONE		Reserved
18:16	PRI4	R/W	4h	Priority 4
15	RESERVED	NONE		Reserved
14:12	PRI3	R/W	3h	Priority 3
11	RESERVED	NONE		Reserved
10:8	PRI2	R/W	2h	Priority 2
7	RESERVED	NONE		Reserved
6:4	PRI1	R/W	1h	Priority 1
3	RESERVED	NONE		Reserved
2:0	PRI0	R/W	0h	Priority 0

4.18.101 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_PRI_CTL_REG Registers

4.18.101.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_PRI_CTL_REG Register (Offset = 2101Ch) [reset = 0h]

Short Description: p0_pri_ctl_reg

Long Description: CPPI Port 0 Priority Control

Return to Summary Table

Table 4-2033. Instance Table

Instance Name	Physical Address
CPSW	5282 101Ch

Figure 4-929. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_PRI_CTL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								RX_FLOW_PRI							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							RX_PTYPE	RESERVED							
NONE							R/W	NONE							
0							0h	0							

Access Types Legend

Table 4-2034. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_PRI_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:16	RX_FLOW_PRI	R/W	0h	Receive Priority Based Flow Control Enable (per priority)
15:9	RESERVED	NONE		Reserved
8	RX_PTYPE	R/W	0h	Receive Priority Type
7:0	RESERVED	NONE		Reserved

4.18.102 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_RX_PRI_MAP_REG Registers

4.18.102.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_RX_PRI_MAP_REG Register (Offset = 21020h) [reset = 76543210h]

Short Description: p0_rx_pri_map_reg

Long Description: CPPI Port 0 RX Pkt Pri to Header Pri Map

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Table 4-2035. Instance Table

Instance Name	Physical Address
CPSW	5282 1020h

Figure 4-930. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_RX_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		PRI7		RESERVED		PRI6		RESERVED		PRI5		RESERVED		PRI4	
NONE		R/W		NONE		R/W		NONE		R/W		NONE		R/W	
0		7h		1		6h		0		5h		1		4h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		PRI3		RESERVED		PRI2		RESERVED		PRI1		RESERVED		PRI0	
NONE		R/W		NONE		R/W		NONE		R/W		NONE		R/W	
0		3h		1		2h		0		1h		1		0h	

Access Types Legend

Table 4-2036. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_RX_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE		Reserved
30:28	PRI7	R/W	7h	Priority 7
27	RESERVED	NONE		Reserved
26:24	PRI6	R/W	6h	Priority 6
23	RESERVED	NONE		Reserved
22:20	PRI5	R/W	5h	Priority 5
19	RESERVED	NONE		Reserved
18:16	PRI4	R/W	4h	Priority 4
15	RESERVED	NONE		Reserved
14:12	PRI3	R/W	3h	Priority 3
11	RESERVED	NONE		Reserved
10:8	PRI2	R/W	2h	Priority 2
7	RESERVED	NONE		Reserved
6:4	PRI1	R/W	1h	Priority 1
3	RESERVED	NONE		Reserved
2:0	PRI0	R/W	0h	Priority 0

4.18.103 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_RX_MAXLEN_REG Registers

4.18.103.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_RX_MAXLEN_REG Register (Offset = 21024h) [reset = 5eeh]

Short Description: p0_rx_maxlen_reg

Long Description: CPPI Port 0 Receive Frame Max Length

Return to Summary Table

Table 4-2037. Instance Table

Instance Name	Physical Address
CPSW	5282 1024h

Figure 4-931. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_RX_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
3c4450df															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		RX_MAXLEN													
NONE		R/W													
3c4450df		5eeh													

Access Types Legend

Table 4-2038. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_RX_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE		Reserved
13:0	RX_MAXLEN	R/W	5EEh	Rx Maximum Frame Length

4.18.104 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_BLKS_PRI_REG Registers

4.18.104.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_BLKS_PRI_REG Register (Offset = 21028h) [reset = 1245678h]

Short Description: p0_tx_blks_pri_reg

Long Description: CPPI Port 0 Transmit Block Sub Per Priority

Return to Summary Table

Table 4-2039. Instance Table

Instance Name	Physical Address
CPSW	5282 1028h

Figure 4-932. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_BLKS_PRI_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRI7				PRI6				PRI5				PRI4			
R/W				R/W				R/W				R/W			
0h				1h				2h				4h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI3				PRI2				PRI1				PRI0			
R/W				R/W				R/W				R/W			
5h				6h				7h				8h			

Access Types Legend

Table 4-2040. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_BLKS_PRI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PRI7	R/W	0h	Priority 7 Port Transmit Blocks
27:24	PRI6	R/W	1h	Priority 6 Port Transmit Blocks
23:20	PRI5	R/W	2h	Priority 5 Port Transmit Blocks
19:16	PRI4	R/W	4h	Priority 4 Port Transmit Blocks
15:12	PRI3	R/W	5h	Priority 3 Port Transmit Blocks
11:8	PRI2	R/W	6h	Priority 2 Port Transmit Blocks
7:4	PRI1	R/W	7h	Priority 1 Port Transmit Blocks
3:0	PRI0	R/W	8h	Priority 0 Port Transmit Blocks

4.18.105 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_IDLE2LPI_REG Registers

4.18.105.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_IDLE2LPI_REG Register (Offset = 21030h) [reset = 0h]

Short Description: p0_idle2lpi_reg

Long Description: Port 0 EEE Idle to LPI counter

Return to Summary Table

Table 4-2041. Instance Table

Instance Name	Physical Address
CPSW	5282 1030h

Figure 4-933. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_IDLE2LPI_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								COUNT							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2042. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_IDLE2LPI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	COUNT	R/W	0h	Port 0 EEE Idle to LPI counter load value

4.18.106 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_LPI2WAKE_REG Registers

4.18.106.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_LPI2WAKE_REG Register (Offset = 21034h) [reset = 0h]

Short Description: p0_lpi2wake_reg

Long Description: Port 0 EEE LPI to wake counter

Return to Summary Table

Table 4-2043. Instance Table

Instance Name	Physical Address
CPSW	5282 1034h

Figure 4-934. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_LPI2WAKE_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								COUNT							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2044. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_LPI2WAKE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	COUNT	R/W	0h	Port 0 EEE LPI to wake counter load value

4.18.107 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_EEE_STATUS_REG Registers

4.18.107.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_EEE_STATUS_REG Register (Offset = 21038h) [reset = 60h]

Short Description: p0_eee_status_reg

Long Description: Port 0 EEE status

Return to Summary Table

Table 4-2045. Instance Table

Instance Name	Physical Address
CPSW	5282 1038h

Figure 4-935. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_EEE_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
1adb0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									TX_FIFO_EMPTY	RX_FIFO_EMPTY	TX_FIFO_HOLD	TX_WAKE	TX_LPI	RX_LPI	WAIT_IDLE2LPI
NONE									R	R	R	R	R	R	R
1adb0									1h	1h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-2046. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_EEE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE		Reserved
6	TX_FIFO_EMPTY	R	1h	CPPI port 0 transmit FIFO (switch egress) is empty - contains no packets
5	RX_FIFO_EMPTY	R	1h	CPPI port 0 receive FIFO (switch ingress) is empty - contains no packets
4	TX_FIFO_HOLD	R	0h	CPPI port 0 transmit FIFO hold - asserted in the LPI state and during the LPI2WAKE count time
3	TX_WAKE	R	0h	CPPI port 0 transmit wakeup - asserted in the transmit LPI2WAKE count time
2	TX_LPI	R	0h	CPPI port 0 transmit LPI state - asserted when the port 0 transmit is in the LPI state
1	RX_LPI	R	0h	CPPI port 0 receive LPI state - asserted when the port 0 receive is in the LPI state
0	WAIT_IDLE2LPI	R	0h	CPPI port 0 wait idle to LPI - asserted when port 0 is counting the IDLE2LPI time

4.18.108 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_FIFO_STATUS_REG Registers

4.18.108.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_FIFO_STATUS_REG Register (Offset = 21050h) [reset = 0h]

Short Description: p0_fifo_status_reg

Long Description: Port 0 FIFO Status

Return to Summary Table

Table 4-2047. Instance Table

Instance Name	Physical Address
CPSW	5282 1050h

Figure 4-936. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_FIFO_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TX_PRI_ACTIVE							
NONE								R							
0								0h							

Access Types Legend

Table 4-2048. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_FIFO_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	TX_PRI_ACTIVE	R	0h	Port 0 FIFO Status

4.18.109 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_RX_DSCP_MAP_REG_N Registers

4.18.109.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_RX_DSCP_MAP_REG_N Register (Offset = 21120h) [reset = 0h]

Short Description: p0_rx_dscp_map_reg

Long Description: CPPI Port 0 Receive IPV4/IPV6 DSCP Map N

Return to Summary Table

Offset = 21120h + (j * 4h); where j = 0h to 7h

Table 4-2049. Instance Table

Instance Name	Physical Address
CPSW	5282 1120h

Figure 4-937. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_RX_DSCP_MAP_REG_N Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		PRI7		RESERVED		PRI6		RESERVED		PRI5		RESERVED		PRI4	
NONE		R/W		NONE		R/W		NONE		R/W		NONE		R/W	
0		0h		0		0h		0		0h		0		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		PRI3		RESERVED		PRI2		RESERVED		PRI1		RESERVED		PRI0	
NONE		R/W		NONE		R/W		NONE		R/W		NONE		R/W	
0		0h		0		0h		0		0h		0		0h	

Access Types Legend

Table 4-2050. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_RX_DSCP_MAP_REG_N Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE		Reserved
30:28	PRI7	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+7 is mapped to this received priority
27	RESERVED	NONE		Reserved
26:24	PRI6	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+6 is mapped to this received priority
23	RESERVED	NONE		Reserved
22:20	PRI5	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+5 is mapped to this received priority
19	RESERVED	NONE		Reserved
18:16	PRI4	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+4 is mapped to this received priority
15	RESERVED	NONE		Reserved
14:12	PRI3	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+3 is mapped to this received priority
11	RESERVED	NONE		Reserved
10:8	PRI2	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+2 is mapped to this received priority
7	RESERVED	NONE		Reserved
6:4	PRI1	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+1 is mapped to this received priority

Table 4-2050. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_RX_DSCP_MAP_REG_N Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	NONE		Reserved
2:0	PRI0	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+0 is mapped to this received priority

4.18.110 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_PRI_CIR_REG_N Registers

4.18.110.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_PRI_CIR_REG_N Register (Offset = 21140h) [reset = 0h]

Short Description: p0_pri_cir_reg

Long Description: CPPI Port 0 Rx Priority P Committed Information Rate

Return to Summary Table

Offset = 21140h + (j * 4h); where j = 0h to 7h

Table 4-2051. Instance Table

Instance Name	Physical Address
CPSW	5282 1140h

Figure 4-938. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_PRI_CIR_REG_N Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI_CIR											
NONE				R/W											
0				0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI_CIR															
R/W															
0h															

Access Types Legend

Table 4-2052. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_PRI_CIR_REG_N Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE		Reserved
27:0	PRI_CIR	R/W	0h	Priority N CIR

4.18.111 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_PRI_EIR_REG_N Registers

4.18.111.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_PRI_EIR_REG_N Register (Offset = 21160h) [reset = 0h]

Short Description: p0_pri_eir_reg

Long Description: CPPI Port 0 Rx Priority P Excess Information Rate

Return to Summary Table

Offset = 21160h + (j * 4h); where j = 0h to 7h

Table 4-2053. Instance Table

Instance Name	Physical Address
CPSW	5282 1160h

Figure 4-939. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_PRI_EIR_REG_N Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI_EIR											
NONE				R/W											
0				0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI_EIR															
R/W															
0h															

Access Types Legend

Table 4-2054. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_PRI_EIR_REG_N Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE		Reserved
27:0	PRI_EIR	R/W	0h	Priority N EIR

4.18.112 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_D_THRESH_SET_L_REG Registers

4.18.112.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_D_THRESH_SET_L_REG Register (Offset = 21180h) [reset = 1f1f1f1fh]

Short Description: p0_tx_d_thresh_set_l_reg

Long Description: CPPI Port 0 Tx PFC Destination Threshold Set Low

Return to Summary Table

Table 4-2055. Instance Table

Instance Name	Physical Address
CPSW	5282 1180h

Figure 4-940. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_D_THRESH_SET_L_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI3					RESERVED			PRI2				
NONE			R/W					NONE			R/W				
b			1fh					b			1fh				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI1					RESERVED			PRI0				
NONE			R/W					NONE			R/W				
b			1fh					b			1fh				

Access Types Legend

Table 4-2056. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_D_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23:21	RESERVED	NONE		Reserved
20:16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15:13	RESERVED	NONE		Reserved
12:8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7:5	RESERVED	NONE		Reserved
4:0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

4.18.113 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_D_THRESH_SET_H_REG Registers

4.18.113.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_D_THRESH_SET_H_REG Register (Offset = 21184h) [reset = 1f1f1f1fh]

Short Description: p0_tx_d_thresh_set_h_reg

Long Description: CPPI Port 0 Tx PFC Destination Threshold Set High

Return to Summary Table

Table 4-2057. Instance Table

Instance Name	Physical Address
CPSW	5282 1184h

Figure 4-941. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_D_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI7					RESERVED			PRI6				
NONE			R/W					NONE			R/W				
b			1fh					b			1fh				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI5					RESERVED			PRI4				
NONE			R/W					NONE			R/W				
b			1fh					b			1fh				

Access Types Legend

Table 4-2058. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_D_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23:21	RESERVED	NONE		Reserved
20:16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15:13	RESERVED	NONE		Reserved
12:8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7:5	RESERVED	NONE		Reserved
4:0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

4.18.114 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_D_THRESH_CLR_L_REG Registers

4.18.114.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_D_THRESH_CLR_L_REG Register (Offset = 21188h) [reset = 0h]

Short Description: p0_tx_d_thresh_clr_l_reg

Long Description: CPPI Port 0 Tx PFC Destination Threshold Clr Low

Return to Summary Table

Table 4-2059. Instance Table

Instance Name	Physical Address
CPSW	5282 1188h

Figure 4-942. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_D_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI3					RESERVED			PRI2				
NONE			R/W					NONE			R/W				
0			0h					0			0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI1					RESERVED			PRI0				
NONE			R/W					NONE			R/W				
0			0h					0			0h				

Access Types Legend

Table 4-2060. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_D_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23:21	RESERVED	NONE		Reserved
20:16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15:13	RESERVED	NONE		Reserved
12:8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7:5	RESERVED	NONE		Reserved
4:0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

4.18.115 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_D_THRESH_CLR_H_REG Registers

4.18.115.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_D_THRESH_CLR_H_REG Register (Offset = 2118Ch) [reset = 0h]

Short Description: p0_tx_d_thresh_clr_h_reg

Long Description: CPPI Port 0 Tx PFC Destination Threshold Clr High

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Table 4-2061. Instance Table

Instance Name	Physical Address
CPSW	5282 118Ch

Figure 4-943. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_D_THRESH_CLR_H_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI7					RESERVED			PRI6				
NONE			R/W					NONE			R/W				
0			0h					0			0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI5					RESERVED			PRI4				
NONE			R/W					NONE			R/W				
0			0h					0			0h				

Access Types Legend

Table 4-2062. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_D_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23:21	RESERVED	NONE		Reserved
20:16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15:13	RESERVED	NONE		Reserved
12:8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7:5	RESERVED	NONE		Reserved
4:0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

4.18.116 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_G_BUF_THRESH_SET_L_REG Registers

4.18.116.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_G_BUF_THRESH_SET_L_REG Register (Offset = 21190h) [reset = 1f1f1f1fh]

Short Description: p0_tx_g_buf_thresh_set_l_reg

Long Description: CPPI Port 0 Tx PFC Global Buffer Threshold Set Low

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Table 4-2063. Instance Table

Instance Name	Physical Address
CPSW	5282 1190h

Figure 4-944. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_G_BUF_THRESH_SET_L_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI3					RESERVED			PRI2				
NONE			R/W					NONE			R/W				
b			1fh					b			1fh				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI1					RESERVED			PRI0				
NONE			R/W					NONE			R/W				
b			1fh					b			1fh				

Access Types Legend

Table 4-2064. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_G_BUF_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23:21	RESERVED	NONE		Reserved
20:16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15:13	RESERVED	NONE		Reserved
12:8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7:5	RESERVED	NONE		Reserved
4:0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

4.18.117 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_G_BUF_THRESH_SET_H_REG Registers

4.18.117.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_G_BUF_THRESH_SET_H_REG Register (Offset = 21194h) [reset = 1f1f1f1fh]

Short Description: p0_tx_g_buf_thresh_set_h_reg

Long Description: CPPI Port 0 Tx PFC Global Buffer Threshold Set High

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Table 4-2065. Instance Table

Instance Name	Physical Address
CPSW	5282 1194h

Figure 4-945. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_G_BUF_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI7					RESERVED			PRI6				
NONE			R/W					NONE			R/W				
b			1fh					b			1fh				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI5					RESERVED			PRI4				
NONE			R/W					NONE			R/W				
b			1fh					b			1fh				

Access Types Legend

Table 4-2066. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_G_BUF_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23:21	RESERVED	NONE		Reserved
20:16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15:13	RESERVED	NONE		Reserved
12:8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7:5	RESERVED	NONE		Reserved
4:0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

4.18.118 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_G_BUF_THRESH_CLR_L_REG Registers

4.18.118.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_G_BUF_THRESH_CLR_L_REG Register (Offset = 21198h) [reset = 0h]

Short Description: p0_tx_g_buf_thresh_clr_l_reg

Long Description: CPPI Port 0 Tx PFC Global Buffer Threshold Clr Low

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Table 4-2067. Instance Table

Instance Name	Physical Address
CPSW	5282 1198h

Figure 4-946. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_G_BUF_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI3					RESERVED			PRI2				
NONE			R/W					NONE			R/W				
0			0h					0			0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI1					RESERVED			PRI0				
NONE			R/W					NONE			R/W				
0			0h					0			0h				

Access Types Legend

Table 4-2068. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_G_BUF_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23:21	RESERVED	NONE		Reserved
20:16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15:13	RESERVED	NONE		Reserved
12:8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7:5	RESERVED	NONE		Reserved
4:0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

4.18.119 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_G_BUF_THRESH_CLR_H_REG Registers

4.18.119.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_G_BUF_THRESH_CLR_H_REG Register (Offset = 2119Ch) [reset = 0h]

Short Description: p0_tx_g_buf_thresh_clr_h_reg

Long Description: CPPI Port 0 Tx PFC Global Buffer Threshold Clr High

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Table 4-2069. Instance Table

Instance Name	Physical Address
CPSW	5282 119Ch

Figure 4-947. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_G_BUF_THRESH_CLR_H_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI7					RESERVED			PRI6				
NONE			R/W					NONE			R/W				
0			0h					0			0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI5					RESERVED			PRI4				
NONE			R/W					NONE			R/W				
0			0h					0			0h				

Access Types Legend

Table 4-2070. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_TX_G_BUF_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23:21	RESERVED	NONE		Reserved
20:16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15:13	RESERVED	NONE		Reserved
12:8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7:5	RESERVED	NONE		Reserved
4:0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

4.18.120 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_SRC_ID_A_REG Registers

4.18.120.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_SRC_ID_A_REG Register (Offset = 21300h) [reset = 4030201h]

Short Description: p0_src_id_a_reg

Long Description: CPPI Port 0 CPPI Source ID A

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Table 4-2071. Instance Table

Instance Name	Physical Address
CPSW	5282 1300h

Figure 4-948. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_SRC_ID_A_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PORT4								PORT3							
R/W								R/W							
4h								3h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PORT2								PORT1							
R/W								R/W							
2h								1h							

Access Types Legend

Table 4-2072. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_SRC_ID_A_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PORT4	R/W	4h	Port 4 CPPI Info Word0 Source ID Value
23:16	PORT3	R/W	3h	Port 3 CPPI Info Word0 Source ID Value
15:8	PORT2	R/W	2h	Port 2 CPPI Info Word0 Source ID Value
7:0	PORT1	R/W	1h	Port 1 CPPI Info Word0 Source ID Value

4.18.121 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_SRC_ID_B_REG Registers

4.18.121.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_SRC_ID_B_REG Register (Offset = 21304h) [reset = 8070605h]

Short Description: p0_src_id_b_reg

Long Description: CPPI Port 0 CPPI Source ID B

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Table 4-2073. Instance Table

Instance Name	Physical Address
CPSW	5282 1304h

Figure 4-949. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_SRC_ID_B_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PORT8								PORT7							
R/W								R/W							
8h								7h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PORT6								PORT5							
R/W								R/W							
6h								5h							

Access Types Legend

Table 4-2074. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_SRC_ID_B_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PORT8	R/W	8h	Port 8 CPPI Info Word0 Source ID Value
23:16	PORT7	R/W	7h	Port 7 CPPI Info Word0 Source ID Value
15:8	PORT6	R/W	6h	Port 6 CPPI Info Word0 Source ID Value
7:0	PORT5	R/W	5h	Port 5 CPPI Info Word0 Source ID Value

4.18.122 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_HOST_BLKS_PRI_REG Registers

4.18.122.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_HOST_BLKS_PRI_REG Register (Offset = 21320h) [reset = 0h]

Short Description: p0_host_blks_pri_reg

Long Description: CPPI Port 0 Host Blocks Priority

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Table 4-2075. Instance Table

Instance Name	Physical Address
CPSW	5282 1320h

Figure 4-950. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_HOST_BLKS_PRI_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRI7				PRI6				PRI5				PRI4			
R/W				R/W				R/W				R/W			
0h				0h				0h				0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI3				PRI2				PRI1				PRI0			
R/W				R/W				R/W				R/W			
0h				0h				0h				0h			

Access Types Legend

Table 4-2076. CPSW_NC_CPSW_NC_CPSW_NC_CPPI_P0_HOST_BLKS_PRI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PRI7	R/W	0h	Priority 7 Host Blocks
27:24	PRI6	R/W	0h	Priority 6 Host Blocks
23:20	PRI5	R/W	0h	Priority 5 Host Blocks
19:16	PRI4	R/W	0h	Priority 4 Host Blocks
15:12	PRI3	R/W	0h	Priority 3 Host Blocks
11:8	PRI2	R/W	0h	Priority 2 Host Blocks
7:4	PRI1	R/W	0h	Priority 1 Host Blocks
3:0	PRI0	R/W	0h	Priority 0 Host Blocks

4.18.123 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_RESERVED_REG Registers

4.18.123.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_RESERVED_REG Register (Offset = 22000h) [reset = 0h]

Short Description: pn_reserved_reg

Long Description: Reserved

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Table 4-2077. Instance Table

Instance Name	Physical Address
CPSW	5282 2000h

Figure 4-951. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_RESERVED_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R															
0h															

Access Types Legend

Table 4-2078. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_RESERVED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R		Reserved register for memory map alignment

4.18.124 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_CONTROL_REG Registers

4.18.124.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_CONTROL_REG Register (Offset = 22004h) [reset = 0h]

Short Description: pn_control_reg

Long Description: Enet Port N Control

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Table 4-2079. Instance Table

Instance Name	Physical Address
CPSW	5282 2004h

Figure 4-952. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_CONTROL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														EST_PORT_EN	RESERVED
NONE														R/W	NONE
0														0h	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_ECC_ERR_EN	TX_ECC_ERR_EN	RESERVED	TX_LPI_CLKSTOP_EN	RESERVED									DSCP_IPV6_EN	DSCP_IPV4_EN	RESERVED
R/W	R/W	NONE	R/W	NONE									R/W	R/W	NONE
0h	0h	0	0h	0									0h	0h	0

Access Types Legend

Table 4-2080. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE		Reserved
17	EST_PORT_EN	R/W	0h	EST Port Enable
16	RESERVED	NONE		Reserved
15	RX_ECC_ERR_EN	R/W	0h	Port 0 Receive ECC Error Enable
14	TX_ECC_ERR_EN	R/W	0h	Port 0 Transmit ECC Error Enable
13	RESERVED	NONE		Reserved
12	TX_LPI_CLKSTOP_EN	R/W	0h	Transmit LPI clockstop enable
11:3	RESERVED	NONE		Reserved
2	DSCP_IPV6_EN	R/W	0h	IPv6 DSCP enable
1	DSCP_IPV4_EN	R/W	0h	IPv4 DSCP enable
0	RESERVED	NONE		Reserved

4.18.125 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAX_BLKS_REG Registers

4.18.125.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAX_BLKS_REG Register (Offset = 22008h) [reset = 1004h]

Short Description: pn_max_blks_reg

Long Description: Enet Port N FIFO Max Blocks

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Table 4-2081. Instance Table

Instance Name	Physical Address
CPSW	5282 2008h

Figure 4-953. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAX_BLKS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
174876e80a															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_MAX_BLKS								RX_MAX_BLKS							
R/W								R/W							
10h								4h							

Access Types Legend

Table 4-2082. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAX_BLKS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	TX_MAX_BLKS	R/W	10h	Transmit FIFO maximum blocks
7:0	RX_MAX_BLKS	R/W	4h	Receive FIFO maximum blocks

4.18.126 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_BLK_CNT_REG Registers

4.18.126.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_BLK_CNT_REG Register (Offset = 22010h) [reset = 1h]

Short Description: pn_blk_cnt_reg

Long Description: Enet Port N FIFO Block Usage Count

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Table 4-2083. Instance Table

Instance Name	Physical Address
CPSW	5282 2010h

Figure 4-954. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_BLK_CNT_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										RX_BLK_CNT_P					
NONE										R					
0										0h					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			TX_BLK_CNT					RESERVED		RX_BLK_CNT_E					
NONE			R					NONE		R					
0			0h					0		1h					

Access Types Legend

Table 4-2084. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_BLK_CNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE		Reserved
21:16	RX_BLK_CNT_P	R	0h	Receive Prempt Queue Block Count Usage
15:13	RESERVED	NONE		Reserved
12:8	TX_BLK_CNT	R	0h	Transmit Block Count Usage
7:6	RESERVED	NONE		Reserved
5:0	RX_BLK_CNT_E	R	1h	Receive Block Count Usage

4.18.127 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_PORT_VLAN_REG Registers

4.18.127.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_PORT_VLAN_REG Register (Offset = 22014h) [reset = 0h]

Short Description: pn_port_vlan_reg

Long Description: Enet Port N VLAN

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Table 4-2085. Instance Table

Instance Name	Physical Address
CPSW	5282 2014h

Figure 4-955. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_PORT_VLAN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PORT_PRI			PORT_CFI	PORT_VID											
R/W			R/W	R/W											
0h			0h	0h											

Access Types Legend

Table 4-2086. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_PORT_VLAN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:13	PORT_PRI	R/W	0h	Port VLAN Priority
12	PORT_CFI	R/W	0h	Port CFI bit
11:0	PORT_VID	R/W	0h	Port VLAN ID

4.18.128 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_PRI_MAP_REG Registers

4.18.128.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_PRI_MAP_REG Register (Offset = 22018h) [reset = 76543210h]

Short Description: pn_tx_pri_map_reg

Long Description: Enet Port N Tx Header Pri to Switch Pri Mapping

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Table 4-2087. Instance Table

Instance Name	Physical Address
CPSW	5282 2018h

Figure 4-956. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		PRI7		RESERVED		PRI6		RESERVED		PRI5		RESERVED		PRI4	
NONE		R/W		NONE		R/W		NONE		R/W		NONE		R/W	
0		7h		1		6h		0		5h		1		4h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		PRI3		RESERVED		PRI2		RESERVED		PRI1		RESERVED		PRI0	
NONE		R/W		NONE		R/W		NONE		R/W		NONE		R/W	
0		3h		1		2h		0		1h		1		0h	

Access Types Legend

Table 4-2088. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE		Reserved
30:28	PRI7	R/W	7h	Priority 7
27	RESERVED	NONE		Reserved
26:24	PRI6	R/W	6h	Priority 6
23	RESERVED	NONE		Reserved
22:20	PRI5	R/W	5h	Priority 5
19	RESERVED	NONE		Reserved
18:16	PRI4	R/W	4h	Priority 4
15	RESERVED	NONE		Reserved
14:12	PRI3	R/W	3h	Priority 3
11	RESERVED	NONE		Reserved
10:8	PRI2	R/W	2h	Priority 2
7	RESERVED	NONE		Reserved
6:4	PRI1	R/W	1h	Priority 1
3	RESERVED	NONE		Reserved
2:0	PRI0	R/W	0h	Priority 0

4.18.129 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_PRI_CTL_REG Registers

4.18.129.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_PRI_CTL_REG Register (Offset = 2201Ch) [reset = 9000h]

Short Description: pn_pri_ctl_reg

Long Description: Enet Port N Priority Control

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Table 4-2089. Instance Table

Instance Name	Physical Address
CPSW	5282 201Ch

Figure 4-957. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_PRI_CTL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TX_FLOW_PRI								RX_FLOW_PRI							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_HOST_BLKS_REM				RESERVED											
R/W				NONE											
9h				0											

Access Types Legend

Table 4-2090. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_PRI_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TX_FLOW_PRI	R/W	0h	Transmit Priority Based Flow Control Enable (per priority)
23:16	RX_FLOW_PRI	R/W	0h	Receive Priority Based Flow Control Enable (per priority)
15:12	TX_HOST_BLKS_REM	R/W	9h	Transmit FIFO Blocks that must be free before a non rate-limited CPPI Port 0 receive thread can begin sending a packet
11:0	RESERVED	NONE		Reserved

4.18.130 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_RX_PRI_MAP_REG Registers

4.18.130.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_RX_PRI_MAP_REG Register (Offset = 22020h) [reset = 76543210h]

Short Description: pn_rx_pri_map_reg

Long Description: Enet Port N RX Pkt Pri to Header Pri Map

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Table 4-2091. Instance Table

Instance Name	Physical Address
CPSW	5282 2020h

Figure 4-958. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_RX_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	PRI7			RESERVED	PRI6			RESERVED	PRI5			RESERVED	PRI4		
NONE	R/W			NONE	R/W			NONE	R/W			NONE	R/W		
0	7h			1	6h			0	5h			1	4h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	PRI3			RESERVED	PRI2			RESERVED	PRI1			RESERVED	PRI0		
NONE	R/W			NONE	R/W			NONE	R/W			NONE	R/W		
0	3h			1	2h			0	1h			1	0h		

Access Types Legend

Table 4-2092. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_RX_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE		Reserved
30:28	PRI7	R/W	7h	Priority 7
27	RESERVED	NONE		Reserved
26:24	PRI6	R/W	6h	Priority 6
23	RESERVED	NONE		Reserved
22:20	PRI5	R/W	5h	Priority 5
19	RESERVED	NONE		Reserved
18:16	PRI4	R/W	4h	Priority 4
15	RESERVED	NONE		Reserved
14:12	PRI3	R/W	3h	Priority 3
11	RESERVED	NONE		Reserved
10:8	PRI2	R/W	2h	Priority 2
7	RESERVED	NONE		Reserved
6:4	PRI1	R/W	1h	Priority 1
3	RESERVED	NONE		Reserved
2:0	PRI0	R/W	0h	Priority 0

4.18.131 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_RX_MAXLEN_REG Registers

4.18.131.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_RX_MAXLEN_REG Register (Offset = 22024h) [reset = 5eeh]

Short Description: pn_rx_maxlen_reg

Long Description: Enet Port N Receive Frame Max Length

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Table 4-2093. Instance Table

Instance Name	Physical Address
CPSW	5282 2024h

Figure 4-959. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_RX_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
3c4450df															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		RX_MAXLEN													
NONE		R/W													
3c4450df		5eeh													

Access Types Legend

Table 4-2094. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_RX_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE		Reserved
13:0	RX_MAXLEN	R/W	5EEh	Rx Maximum Frame Length

4.18.132 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_BLKS_PRI_REG Registers

4.18.132.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_BLKS_PRI_REG Register (Offset = 22028h) [reset = 1245678h]

Short Description: pn_tx_blks_pri_reg

Long Description: Enet Port N Transmit Block Sub Per Priority

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Table 4-2095. Instance Table

Instance Name	Physical Address
CPSW	5282 2028h

Figure 4-960. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_BLKS_PRI_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRI7				PRI6				PRI5				PRI4			
R/W				R/W				R/W				R/W			
0h				1h				2h				4h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI3				PRI2				PRI1				PRI0			
R/W				R/W				R/W				R/W			
5h				6h				7h				8h			

Access Types Legend

Table 4-2096. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_BLKS_PRI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PRI7	R/W	0h	Priority 7 Port Transmit Blocks
27:24	PRI6	R/W	1h	Priority 6 Port Transmit Blocks
23:20	PRI5	R/W	2h	Priority 5 Port Transmit Blocks
19:16	PRI4	R/W	4h	Priority 4 Port Transmit Blocks
15:12	PRI3	R/W	5h	Priority 3 Port Transmit Blocks
11:8	PRI2	R/W	6h	Priority 2 Port Transmit Blocks
7:4	PRI1	R/W	7h	Priority 1 Port Transmit Blocks
3:0	PRI0	R/W	8h	Priority 0 Port Transmit Blocks

4.18.133 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_IDLE2LPI_REG Registers

4.18.133.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_IDLE2LPI_REG Register (Offset = 22030h) [reset = 0h]

Short Description: pn_idle2lpi_reg

Long Description: Enet Port N EEE Idle to LPI counter

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Table 4-2097. Instance Table

Instance Name	Physical Address
CPSW	5282 2030h

Figure 4-961. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_IDLE2LPI_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								COUNT							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2098. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_IDLE2LPI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	COUNT	R/W	0h	EEE Idle to LPI counter load value

4.18.134 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_LPI2WAKE_REG Registers

4.18.134.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_LPI2WAKE_REG Register (Offset = 22034h) [reset = 0h]

Short Description: pn_lpi2wake_reg

Long Description: Enet Port N EEE LPI to wake counter

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Table 4-2099. Instance Table

Instance Name	Physical Address
CPSW	5282 2034h

Figure 4-962. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_LPI2WAKE_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								COUNT							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2100. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_LPI2WAKE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	COUNT	R/W	0h	EEE LPI to wake counter load value

4.18.135 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_EEE_STATUS_REG Registers

4.18.135.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_EEE_STATUS_REG Register (Offset = 22038h) [reset = 62h]

Short Description: pn_eee_status_reg

Long Description: Enet Port N EEE status

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Table 4-2101. Instance Table

Instance Name	Physical Address
CPSW	5282 2038h

Figure 4-963. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_EEE_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
1adb1															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									TX_FIFO_EMPTY	RX_FIFO_EMPTY	TX_FIFO_HOLD	TX_WAKE	TX_LPI	RX_LPI	WAIT_IDLE2LPI
NONE									R	R	R	R	R	R	R
1adb1									1h	1h	0h	0h	0h	1h	0h

Access Types Legend

Table 4-2102. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_EEE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE		Reserved
6	TX_FIFO_EMPTY	R	1h	Transmit FIFO (switch egress) is empty - contains no packets
5	RX_FIFO_EMPTY	R	1h	Receive FIFO (switch ingress) is empty - contains no packets
4	TX_FIFO_HOLD	R	0h	Transmit FIFO hold - asserted in the LPI state and during the LPI2WAKE count time
3	TX_WAKE	R	0h	Transmit wakeup - asserted in the transmit LPI2WAKE count time
2	TX_LPI	R	0h	Transmit LPI state - asserted when the port 0 transmit is in the LPI state
1	RX_LPI	R	1h	Receive LPI state - asserted when the port 0 receive is in the LPI state
0	WAIT_IDLE2LPI	R	0h	CPPI port 0 wait idle to LPI - asserted when port 0 is counting the IDLE2LPI time

4.18.136 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_FIFO_STATUS_REG Registers

4.18.136.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_FIFO_STATUS_REG Register (Offset = 22050h) [reset = ff00h]

Short Description: pn_fifo_status_reg

Long Description: Enet Port N FIFO STATUS

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Table 4-2103. Instance Table

Instance Name	Physical Address
CPSW	5282 2050h

Figure 4-964. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_FIFO_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED													EST_BUFACT	EST_ADD_ERR	EST_CNT_ERR
NONE													R	R	R
19deac0d80													0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_E_MAC_ALLOW								TX_PRI_ACTIVE							
R								R							
ffh								0h							

Access Types Legend

Table 4-2104. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_FIFO_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE		Reserved
18	EST_BUFACT	R	0h	Transmit FIFO EST Buffer Active
17	EST_ADD_ERR	R	0h	Transmit FIFO EST Address Error
16	EST_CNT_ERR	R	0h	Transmit FIFO EST Count Error
15:8	TX_E_MAC_ALLOW	R	FFh	Transmit FIFO Express Queue Priority Allow
7:0	TX_PRI_ACTIVE	R	0h	Transmit FIFO Priority Active

4.18.137 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_EST_CONTROL_REG Registers

4.18.137.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_EST_CONTROL_REG Register (Offset = 22060h) [reset = 0h]

Short Description: pn_est_control_reg

Long Description: Enet Port N EST CONTROL

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Table 4-2105. Instance Table

Instance Name	Physical Address
CPSW	5282 2060h

Figure 4-965. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_EST_CONTROL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								EST_FILL_MARGIN							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EST_PREMPT_COMP							EST_FILL_EN	EST_TS_PRI			EST_TS_ONEPRI	EST_TS_FIRST	EST_TS_EN	EST_BUFSEL	EST_ONEBUF
R/W							R/W	R/W			R/W	R/W	R/W	R/W	R/W
0h							0h	0h			0h	0h	0h	0h	0h

Access Types Legend

Table 4-2106. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_EST_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE		Reserved
25:16	EST_FILL_MARGIN	R/W	0h	Transmit FIFO EST Fill Margin
15:9	EST_PREMPT_COMP	R/W	0h	Transmit FIFO EST Prempt Comparison Value to Clear wire
8	EST_FILL_EN	R/W	0h	Transmit FIFO EST Fill Enable
7:5	EST_TS_PRI	R/W	0h	Transmit FIFO EST TimeStamp Priority
4	EST_TS_ONEPRI	R/W	0h	Transmit FIFO EST TimeStamp One Priority
3	EST_TS_FIRST	R/W	0h	Transmit FIFO EST TimeStamp First Express Packet
2	EST_TS_EN	R/W	0h	Transmit FIFO EST TimeStamp Enable
1	EST_BUFSEL	R/W	0h	Transmit FIFO EST Buffer Select
0	EST_ONEBUF	R/W	0h	Transmit FIFO EST One Buffer

4.18.138 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_RX_DSCP_MAP_REG_N Registers

4.18.138.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_RX_DSCP_MAP_REG_N Register (Offset = 22120h) [reset = 0h]

Short Description: pn_rx_dscp_map_reg

Long Description: Enet Port N Receive IPV4/IPV6 DSCP Map M

Return to Summary Table

Offset = 22120h + (j * 4h); where j = 0h to 7h

Table 4-2107. Instance Table

Instance Name	Physical Address
CPSW	5282 2120h

Figure 4-966. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_RX_DSCP_MAP_REG_N Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		PRI7		RESERVED		PRI6		RESERVED		PRI5		RESERVED		PRI4	
NONE		R/W		NONE		R/W		NONE		R/W		NONE		R/W	
0		0h		0		0h		0		0h		0		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		PRI3		RESERVED		PRI2		RESERVED		PRI1		RESERVED		PRI0	
NONE		R/W		NONE		R/W		NONE		R/W		NONE		R/W	
0		0h		0		0h		0		0h		0		0h	

Access Types Legend

Table 4-2108. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_RX_DSCP_MAP_REG_N Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE		Reserved
30:28	PRI7	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+7 is mapped to this received priority
27	RESERVED	NONE		Reserved
26:24	PRI6	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+6 is mapped to this received priority
23	RESERVED	NONE		Reserved
22:20	PRI5	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+5 is mapped to this received priority
19	RESERVED	NONE		Reserved
18:16	PRI4	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+4 is mapped to this received priority
15	RESERVED	NONE		Reserved
14:12	PRI3	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+3 is mapped to this received priority
11	RESERVED	NONE		Reserved
10:8	PRI2	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+2 is mapped to this received priority
7	RESERVED	NONE		Reserved

Table 4-2108. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_RX_DSCP_MAP_REG_N Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:4	PRI1	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+1 is mapped to this received priority
3	RESERVED	NONE		Reserved
2:0	PRI0	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+0 is mapped to this received priority

4.18.139 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_PRI_CIR_REG_N Registers

4.18.139.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_PRI_CIR_REG_N Register (Offset = 22140h) [reset = 0h]

Short Description: pn_pri_send_reg

Long Description: Enet Port N Rx Priority P Committed Information Rate Value

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Offset = 22140h + (j * 4h); where j = 0h to 7h

Table 4-2109. Instance Table

Instance Name	Physical Address
CPSW	5282 2140h

Figure 4-967. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_PRI_CIR_REG_N Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI_CIR											
NONE				R/W											
0				0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI_CIR															
R/W															
0h															

Access Types Legend

Table 4-2110. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_PRI_CIR_REG_N Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE		Reserved
27:0	PRI_CIR	R/W	0h	Priority N committed information rate

4.18.140 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_PRI_EIR_REG_N Registers

4.18.140.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_PRI_EIR_REG_N Register (Offset = 22160h) [reset = 0h]

Short Description: pn_pri_idle_reg

Long Description: Enet Port N Rx Priority P Excess Informatoin Rate Value

Return to Summary Table

Offset = 22160h + (j * 4h); where j = 0h to 7h

Table 4-2111. Instance Table

Instance Name	Physical Address
CPSW	5282 2160h

Figure 4-968. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_PRI_EIR_REG_N Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI_EIR											
NONE				R/W											
0				0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI_EIR															
R/W															
0h															

Access Types Legend

Table 4-2112. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_PRI_EIR_REG_N Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE		Reserved
27:0	PRI_EIR	R/W	0h	Priority N Excess Information Rate count

4.18.141 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_D_THRESH_SET_L_REG Registers

4.18.141.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_D_THRESH_SET_L_REG Register (Offset = 22180h) [reset = 1f1f1f1fh]

Short Description: pn_tx_d_thresh_set_l_reg

Long Description: Enet Port N Tx PFC Destination Threshold Set Low

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Table 4-2113. Instance Table

Instance Name	Physical Address
CPSW	5282 2180h

Figure 4-969. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_D_THRESH_SET_L_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI3					RESERVED			PRI2				
NONE			R/W					NONE			R/W				
b			1fh					b			1fh				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI1					RESERVED			PRI0				
NONE			R/W					NONE			R/W				
b			1fh					b			1fh				

Access Types Legend

Table 4-2114. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_D_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23:21	RESERVED	NONE		Reserved
20:16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15:13	RESERVED	NONE		Reserved
12:8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7:5	RESERVED	NONE		Reserved
4:0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

4.18.142 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_D_THRESH_SET_H_REG Registers

4.18.142.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_D_THRESH_SET_H_REG Register (Offset = 22184h) [reset = 1f1f1f1fh]

Short Description: pn_tx_d_thresh_set_h_reg

Long Description: Enet Port N Tx PFC Destination Threshold Set High

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Table 4-2115. Instance Table

Instance Name	Physical Address
CPSW	5282 2184h

Figure 4-970. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_D_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI7					RESERVED			PRI6				
NONE			R/W					NONE			R/W				
b			1fh					b			1fh				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI5					RESERVED			PRI4				
NONE			R/W					NONE			R/W				
b			1fh					b			1fh				

Access Types Legend

Table 4-2116. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_D_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23:21	RESERVED	NONE		Reserved
20:16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15:13	RESERVED	NONE		Reserved
12:8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7:5	RESERVED	NONE		Reserved
4:0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

4.18.143 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_D_THRESH_CLR_L_REG Registers

4.18.143.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_D_THRESH_CLR_L_REG Register (Offset = 22188h) [reset = 0h]

Short Description: pn_tx_d_thresh_clr_l_reg

Long Description: Enet Port N Tx PFC Destination Threshold Clr Low

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Table 4-2117. Instance Table

Instance Name	Physical Address
CPSW	5282 2188h

Figure 4-971. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_D_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI3					RESERVED			PRI2				
NONE			R/W					NONE			R/W				
0			0h					0			0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI1					RESERVED			PRI0				
NONE			R/W					NONE			R/W				
0			0h					0			0h				

Access Types Legend

Table 4-2118. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_D_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23:21	RESERVED	NONE		Reserved
20:16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15:13	RESERVED	NONE		Reserved
12:8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7:5	RESERVED	NONE		Reserved
4:0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

4.18.144 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_D_THRESH_CLR_H_REG Registers

4.18.144.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_D_THRESH_CLR_H_REG Register (Offset = 2218Ch) [reset = 0h]

Short Description: pn_tx_d_thresh_clr_h_reg

Long Description: Enet Port N Tx PFC Destination Threshold Clr High

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Table 4-2119. Instance Table

Instance Name	Physical Address
CPSW	5282 218Ch

Figure 4-972. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_D_THRESH_CLR_H_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI7					RESERVED			PRI6				
NONE			R/W					NONE			R/W				
0			0h					0			0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI5					RESERVED			PRI4				
NONE			R/W					NONE			R/W				
0			0h					0			0h				

Access Types Legend

Table 4-2120. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_D_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23:21	RESERVED	NONE		Reserved
20:16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15:13	RESERVED	NONE		Reserved
12:8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7:5	RESERVED	NONE		Reserved
4:0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

4.18.145 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_L_REG Registers

4.18.145.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_L_REG Register (Offset = 22190h) [reset = 1f1f1f1fh]

Short Description: pn_tx_g_buf_thresh_set_l_reg

Long Description: Enet Port N Tx PFC Global Buffer Threshold Set Low

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Table 4-2121. Instance Table

Instance Name	Physical Address
CPSW	5282 2190h

Figure 4-973. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_L_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI3					RESERVED			PRI2				
NONE			R/W					NONE			R/W				
b			1fh					b			1fh				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI1					RESERVED			PRI0				
NONE			R/W					NONE			R/W				
b			1fh					b			1fh				

Access Types Legend

Table 4-2122. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23:21	RESERVED	NONE		Reserved
20:16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15:13	RESERVED	NONE		Reserved
12:8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7:5	RESERVED	NONE		Reserved
4:0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

4.18.146 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_H_REG Registers

4.18.146.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_H_REG Register (Offset = 22194h) [reset = 1f1f1f1fh]

Short Description: pn_tx_g_buf_thresh_set_h_reg

Long Description: Enet Port N Tx PFC Global Buffer Threshold Set High

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Table 4-2123. Instance Table

Instance Name	Physical Address
CPSW	5282 2194h

Figure 4-974. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI7					RESERVED			PRI6				
NONE			R/W					NONE			R/W				
b			1fh					b			1fh				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI5					RESERVED			PRI4				
NONE			R/W					NONE			R/W				
b			1fh					b			1fh				

Access Types Legend

Table 4-2124. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_G_BUF_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23:21	RESERVED	NONE		Reserved
20:16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15:13	RESERVED	NONE		Reserved
12:8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7:5	RESERVED	NONE		Reserved
4:0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

4.18.147 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_L_REG Registers

4.18.147.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_L_REG Register (Offset = 22198h) [reset = 0h]

Short Description: pn_tx_g_buf_thresh_clr_l_reg

Long Description: Enet Port N Tx PFC Global Buffer Threshold Clr Low

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Table 4-2125. Instance Table

Instance Name	Physical Address
CPSW	5282 2198h

Figure 4-975. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI3					RESERVED			PRI2				
NONE			R/W					NONE			R/W				
0			0h					0			0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI1					RESERVED			PRI0				
NONE			R/W					NONE			R/W				
0			0h					0			0h				

Access Types Legend

Table 4-2126. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23:21	RESERVED	NONE		Reserved
20:16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15:13	RESERVED	NONE		Reserved
12:8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7:5	RESERVED	NONE		Reserved
4:0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

4.18.148 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_H_REG Registers

4.18.148.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_H_REG Register (Offset = 2219Ch) [reset = 0h]

Short Description: pn_tx_g_buf_thresh_clr_h_reg

Long Description: Enet Port N Tx PFC Global Buffer Threshold Clr High

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Table 4-2127. Instance Table

Instance Name	Physical Address
CPSW	5282 219Ch

Figure 4-976. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_H_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI7					RESERVED			PRI6				
NONE			R/W					NONE			R/W				
0			0h					0			0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI5					RESERVED			PRI4				
NONE			R/W					NONE			R/W				
0			0h					0			0h				

Access Types Legend

Table 4-2128. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_G_BUF_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23:21	RESERVED	NONE		Reserved
20:16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15:13	RESERVED	NONE		Reserved
12:8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7:5	RESERVED	NONE		Reserved
4:0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

4.18.149 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_L_REG Registers

4.18.149.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_L_REG Register (Offset = 22300h) [reset = 0h]

Short Description: pn_tx_d_oflow_addval_l_reg

Long Description: Enet Port N Tx Destination Out Flow Add Values Low

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Table 4-2129. Instance Table

Instance Name	Physical Address
CPSW	5282 2300h

Figure 4-977. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_L_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI3					RESERVED			PRI2				
NONE			R/W					NONE			R/W				
0			0h					0			0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI1					RESERVED			PRI0				
NONE			R/W					NONE			R/W				
0			0h					0			0h				

Access Types Legend

Table 4-2130. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:24	PRI3	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 3
23:21	RESERVED	NONE		Reserved
20:16	PRI2	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 2
15:13	RESERVED	NONE		Reserved
12:8	PRI1	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 1
7:5	RESERVED	NONE		Reserved
4:0	PRI0	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 0

4.18.150 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_H_REG Registers

4.18.150.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_H_REG Register (Offset = 22304h) [reset = 0h]

Short Description: pn_tx_d_oflow_addval_h_reg

Long Description: Enet Port N Tx Destination Out Flow Add Values High

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Table 4-2131. Instance Table

Instance Name	Physical Address
CPSW	5282 2304h

Figure 4-978. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_H_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI7					RESERVED			PRI6				
NONE			R/W					NONE			R/W				
0			0h					0			0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI5					RESERVED			PRI4				
NONE			R/W					NONE			R/W				
0			0h					0			0h				

Access Types Legend

Table 4-2132. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TX_D_OFLOW_ADDVAL_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:24	PRI7	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 7
23:21	RESERVED	NONE		Reserved
20:16	PRI6	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 6
15:13	RESERVED	NONE		Reserved
12:8	PRI5	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 5
7:5	RESERVED	NONE		Reserved
4:0	PRI4	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 4

4.18.151 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_SA_L_REG Registers

4.18.151.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_SA_L_REG Register (Offset = 22308h) [reset = 0h]

Short Description: pn_sa_l_reg

Long Description: Enet Port N Tx Pause Frame Source Address Low

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Table 4-2133. Instance Table

Instance Name	Physical Address
CPSW	5282 2308h

Figure 4-979. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_SA_L_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MACSRCADDR_7_0								MACSRCADDR_15_8							
R/W								R/W							
0h								0h							

Access Types Legend

Table 4-2134. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_SA_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MACSRCADDR_7_0	R/W	0h	Source Address Lower 8 bits
7:0	MACSRCADDR_15_8	R/W	0h	Source Address bits 15:8

4.18.152 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_SA_H_REG Registers

4.18.152.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_SA_H_REG Register (Offset = 2230Ch) [reset = 0h]

Short Description: pn_sa_h_reg

Long Description: Enet Port N Tx Pause Frame Source Address High

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Table 4-2135. Instance Table

Instance Name	Physical Address
CPSW	5282 230Ch

Figure 4-980. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_SA_H_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MACSRCADDR_23_16								MACSRCADDR_31_24							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MACSRCADDR_39_32								MACSRCADDR_47_40							
R/W								R/W							
0h								0h							

Access Types Legend

Table 4-2136. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_SA_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MACSRCADDR_23_16	R/W	0h	Source Address bits 23:16
23:16	MACSRCADDR_31_24	R/W	0h	Source Address bits 31:24
15:8	MACSRCADDR_39_32	R/W	0h	Source Address bits 39:32
7:0	MACSRCADDR_47_40	R/W	0h	Source Address bits 47:40

4.18.153 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TS_CTL_REG Registers

4.18.153.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TS_CTL_REG Register (Offset = 22310h) [reset = 0h]

Short Description: pn_ts_ctl_reg

Long Description: Enet Port N Time Sync Control

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Table 4-2137. Instance Table

Instance Name	Physical Address
CPSW	5282 2310h

Figure 4-981. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TS_CTL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TS_MSG_TYPE_EN															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				TS_TX_HOST_TS_EN	TS_TX_ANNEX_E_EN	TS_RX_ANNEX_E_EN	TS_LTYPE2_EN	TS_TX_ANNEX_D_EN	TS_TX_VLAN_LTYPE2_EN	TS_TX_VLAN_LTYPE1_EN	TS_TX_ANNEX_F_EN	TS_RX_ANNEX_D_EN	TS_RX_VLAN_LTYPE2_EN	TS_RX_VLAN_LTYPE1_EN	TS_RX_ANNEX_F_EN
NONE				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0				0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-2138. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TS_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TS_MSG_TYPE_EN	R/W	0h	Time Sync Message Type Enable
15:12	RESERVED	NONE		Reserved
11	TS_TX_HOST_TS_EN	R/W	0h	Time Sync Transmit Host Time Stamp Enable
10	TS_TX_ANNEX_E_EN	R/W	0h	Time Synce Transmit Annex E Enable
9	TS_RX_ANNEX_E_EN	R/W	0h	Time Synce Receive Annex E Enable
8	TS_LTYPE2_EN	R/W	0h	Time Sync LTYPE 2 enable transmit and receive
7	TS_TX_ANNEX_D_EN	R/W	0h	Time Synce Transmit Annex D Enable
6	TS_TX_VLAN_LTYPE2_EN	R/W	0h	Time Sync Transmit VLAN LTYPE 2 enable
5	TS_TX_VLAN_LTYPE1_EN	R/W	0h	Time Sync Transmit VLAN LTYPE 1 enable
4	TS_TX_ANNEX_F_EN	R/W	0h	Time Synce Transmit Annex F Enable
3	TS_RX_ANNEX_D_EN	R/W	0h	Time Synce Receive Annex D Enable
2	TS_RX_VLAN_LTYPE2_EN	R/W	0h	Time Sync Receive VLAN LTYPE 2 enable
1	TS_RX_VLAN_LTYPE1_EN	R/W	0h	Time Sync Receive VLAN LTYPE 1 enable
0	TS_RX_ANNEX_F_EN	R/W	0h	Time Synce Receive Annex F Enable

4.18.154 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TS_SEQ_LTYPE_REG Registers

4.18.154.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TS_SEQ_LTYPE_REG Register (Offset = 22314h) [reset = 1e0000h]

Short Description: pn_ts_seq_ltype_reg

Long Description: Enet Port N Time Sync LTYPE (and SEQ_ID_OFFSET)

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Table 4-2139. Instance Table

Instance Name	Physical Address
CPSW	5282 2314h

Figure 4-982. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TS_SEQ_LTYPE_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										TS_SEQ_ID_OFFSET					
NONE										R/W					
0										1eh					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_LTYPE1															
R/W															
0h															

Access Types Legend

Table 4-2140. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TS_SEQ_LTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE		Reserved
21:16	TS_SEQ_ID_OFFSET	R/W	1Eh	Time Sync Sequence ID Offset
15:0	TS_LTYPE1	R/W	0h	Time Sync LTYPE1

4.18.155 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TS_VLAN_LTYPE_REG Registers

4.18.155.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TS_VLAN_LTYPE_REG Register (Offset = 22318h) [reset = 0h]

Short Description: pn_ts_vlan_ltype_reg

Long Description: Enet Port N Time Sync VLAN2 and VLAN2

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Table 4-2141. Instance Table

Instance Name	Physical Address
CPSW	5282 2318h

Figure 4-983. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TS_VLAN_LTYPE_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TS_VLAN_LTYPE2															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_VLAN_LTYPE1															
R/W															
0h															

Access Types Legend

Table 4-2142. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TS_VLAN_LTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TS_VLAN_LTYPE2	R/W	0h	Time Sync VLAN LTYPE2
15:0	TS_VLAN_LTYPE1	R/W	0h	Time Sync VLAN LTYPE1

4.18.156 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TS_CTL_LTYPE2_REG Registers

4.18.156.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TS_CTL_LTYPE2_REG Register (Offset = 2231Ch) [reset = 0h]

Short Description: pn_ts_ctl_ltype2_reg

Long Description: Enet Port N Time Sync Control and LTYPE 2

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Table 4-2143. Instance Table

Instance Name	Physical Address
CPSW	5282 231Ch

Figure 4-984. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TS_CTL_LTYPE2_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							TS_UNI_EN	TS_TTL_NONZERO	TS_320	TS_319	TS_132	TS_131	TS_130	TS_129	TS_107
NONE							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0							0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_LTYPE2															
R/W															
0h															

Access Types Legend

Table 4-2144. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TS_CTL_LTYPE2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24	TS_UNI_EN	R/W	0h	Time Sync Unicast Enable
23	TS_TTL_NONZERO	R/W	0h	Time Sync Time to Live Non-zero Enable
22	TS_320	R/W	0h	Time Sync Destination IP Address 320 Enable
21	TS_319	R/W	0h	Time Sync Destination IP Address 319 Enable
20	TS_132	R/W	0h	Time Sync Destination IP Address 132 Enable
19	TS_131	R/W	0h	Time Sync Destination IP Address 131 Enable
18	TS_130	R/W	0h	Time Sync Destination IP Address 130 Enable
17	TS_129	R/W	0h	Time Sync Destination IP Address 129 Enable
16	TS_107	R/W	0h	Time Sync Destination IP Address 107 Enable
15:0	TS_LTYPE2	R/W	0h	Time Sync LTYPE2

4.18.157 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TS_CTL2_REG Registers

4.18.157.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TS_CTL2_REG Register (Offset = 22320h) [reset = 40000h]

Short Description: pn_ts_ctl2_reg

Long Description: Enet Port N Time Sync Control 2

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Table 4-2145. Instance Table

Instance Name	Physical Address
CPSW	5282 2320h

Figure 4-985. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TS_CTL2_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										TS_DOMAIN_OFFSET					
NONE										R/W					
0										4h					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_MCAST_TYPE_EN															
R/W															
0h															

Access Types Legend

Table 4-2146. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_TS_CTL2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE		Reserved
21:16	TS_DOMAIN_OFFSET	R/W	4h	Time Sync Domain Offset
15:0	TS_MCAST_TYPE_EN	R/W	0h	Time Sync Multicast Destination Address Type Enable

4.18.158 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_CONTROL_REG Registers

4.18.158.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_CONTROL_REG Register (Offset = 22330h) [reset = 0h]

Short Description: pn_mac_control_reg

Long Description: Enet Port N Mac Control

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Table 4-2147. Instance Table

Instance Name	Physical Address
CPSW	5282 2330h

Figure 4-986. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_CONTROL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							RX_CMF_EN	RX_CSF_EN	RX_CEF_EN	TX_SHORT_GAP_LIM_EN	EXT_TX_FLOW_EN	EXT_RX_FLOW_EN	EXT_EN	GIG_FORCE	IFCTL_B
NONE							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0							0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IFCTL_A	RESERVED		CRC_TYPE	CMD_IDLE	TX_SHORT_GAP_ENABLE	RESERVED		GIG	TX_PACE	GMII_EN	TX_FLOW_EN	RX_FLOW_EN	MTEST	LOOPBACK	FULLDUPLEX
R/W	NONE		R/W	R/W	R/W	NONE		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0		0h	0h	0h	0		0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-2148. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24	RX_CMF_EN	R/W	0h	RX Copy MAC Control Frames Enable
23	RX_CSF_EN	R/W	0h	RX Copy Short Frames Enable
22	RX_CEF_EN	R/W	0h	RX Copy Error Frames Enable
21	TX_SHORT_GAP_LIM_EN	R/W	0h	Transmit Short Gap Limit Enable
20	EXT_TX_FLOW_EN	R/W	0h	External Transmit Flow Control Enable
19	EXT_RX_FLOW_EN	R/W	0h	External Receive Flow Control Enable
18	EXT_EN	R/W	0h	External Enable
17	GIG_FORCE	R/W	0h	Gigabit Mode Force
16	IFCTL_B	R/W	0h	Interface Control B
15	IFCTL_A	R/W	0h	Interface Control A
14:13	RESERVED	NONE		Reserved
12	CRC_TYPE	R/W	0h	Port CRC Type
11	CMD_IDLE	R/W	0h	Command Idle
10	TX_SHORT_GAP_ENABLE	R/W	0h	Transmit Short Gap Enable
9:8	RESERVED	NONE		Reserved

Table 4-2148. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	GIG	R/W	0h	Gigabit Mode
6	TX_PACE	R/W	0h	Transmit Pacing Enable
5	GMII_EN	R/W	0h	GMII Enable
4	TX_FLOW_EN	R/W	0h	Transmit Flow Control Enable
3	RX_FLOW_EN	R/W	0h	Receive Flow Control Enable
2	MTEST	R/W	0h	Manufacturing Test Mode
1	LOOPBACK	R/W	0h	Loop Back Mode
0	FULLDUPLEX	R/W	0h	Full Duplex mode

4.18.159 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_STATUS_REG Registers

4.18.159.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_STATUS_REG Register (Offset = 22334h) [reset = d0000000h]

Short Description: pn_mac_status_reg

Long Description: Enet Port N Mac Status

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Table 4-2149. Instance Table

Instance Name	Physical Address
CPSW	5282 2334h

Figure 4-987. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IDLE	E_IDLE	RESERVED	MAC_TX_IDLE	TORF	TORF_PRI			TX_PFC_FLOW_ACT							
R	R	NONE	R	R	R			R							
1h	1h	0	1h	0h	0h			0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_PFC_FLOW_ACT								RESERVED	EXT_RX_FLOW_EN	EXT_TX_FLOW_EN	EXT_GIG	EXT_FULLDUPLEX	RESERVED	RX_FLOW_ACT	TX_FLOW_ACT
R								NONE	R	R	R	R	NONE	R	R
0h								0	0h	0h	0h	0h	0	0h	0h

Access Types Legend

Table 4-2150. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IDLE	R	1h	cpxmac_sl IDLE
30	E_IDLE	R	1h	Express cpxmac_sl IDLE
29	RESERVED	NONE		Reserved
28	MAC_TX_IDLE	R	1h	Prempt and Express cpxmac_sl Transmit IDLE
27	TORF	R	0h	Top of receive FIFO flow control trigger occurred. This bit is write one to clear.
26:24	TORF_PRI	R	0h	The lowest priority that caused top of receive FIFO flow control trigger since the last write to clear. This field is write 0x7 to clear.
23:16	TX_PFC_FLOW_ACT	R	0h	Transmit Priority Based Flow Control Active (priority 7 down to 0)
15:8	RX_PFC_FLOW_ACT	R	0h	Receive Priority Based Flow Control Active (priority 7 down to 0)
7	RESERVED	NONE		Reserved
6	EXT_RX_FLOW_EN	R	0h	External Transmit Flow Control Enable
5	EXT_TX_FLOW_EN	R	0h	External Receive Flow Control Enable
4	EXT_GIG	R	0h	External GIG mode
3	EXT_FULLDUPLEX	R	0h	External Fullduplex
2	RESERVED	NONE		Reserved
1	RX_FLOW_ACT	R	0h	Receive Flow Control Active
0	TX_FLOW_ACT	R	0h	Transmit Flow Control Active

4.18.160 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_SOFT_RESET_REG Registers

4.18.160.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_SOFT_RESET_REG Register (Offset = 22338h) [reset = 0h]

Short Description: pn_mac_soft_reset_reg

Long Description: Enet Port N Mac Soft Reset

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Table 4-2151. Instance Table

Instance Name	Physical Address
CPSW	5282 2338h

Figure 4-988. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_SOFT_RESET_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															SOFT_RESET
NONE															R/W
0															0h

Access Types Legend

Table 4-2152. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_SOFT_RESET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	SOFT_RESET	R/W	0h	Software reset

4.18.161 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_BOFFTEST_REG Registers

4.18.161.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_BOFFTEST_REG Register (Offset = 2233Ch) [reset = 0h]

Short Description: pn_mac_bofftest_reg

Long Description: Enet Port N Mac Backoff Test

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Table 4-2153. Instance Table

Instance Name	Physical Address
CPSW	5282 233Ch

Figure 4-989. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_BOFFTEST_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	PACEVAL					RNDNUM									
NONE	R/W					R/W									
0	0h					0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COLL_COUNT				RESERVED		TX_BACKOFF									
R				NONE		R									
0h				0		0h									

Access Types Legend

Table 4-2154. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_BOFFTEST_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE		Reserved
30:26	PACEVAL	R/W	0h	Pacing Register Current Value
25:16	RNDNUM	R/W	0h	Backoff Random Number Generator
15:12	COLL_COUNT	R	0h	Collision Count
11:10	RESERVED	NONE		Reserved
9:0	TX_BACKOFF	R	0h	Backoff Count

4.18.162 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_RX_PAUSETIMER_REG Registers

4.18.162.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_RX_PAUSETIMER_REG Register (Offset = 22340h) [reset = 0h]

Short Description: pn_mac_rx_pausetimer_reg

Long Description: Enet Port N 802.3 Receive Pause Timer

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Table 4-2155. Instance Table

Instance Name	Physical Address
CPSW	5282 2340h

Figure 4-990. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_RX_PAUSETIMER_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_PAUSETIMER															
R/W															
0h															

Access Types Legend

Table 4-2156. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_RX_PAUSETIMER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	RX_PAUSETIMER	R/W	0h	RX Pause Timer Value

4.18.163 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_RXN_PAUSETIMER_REG_N Registers

4.18.163.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_RXN_PAUSETIMER_REG_N Register (Offset = 22350h) [reset = 0h]

Short Description: pn_mac_rxn_pausetimer_reg

Long Description: Enet Port N PFC Priority P Rx Pause Timer

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Offset = 22350h + (j * 4h); where j = 0h to 7h

Table 4-2157. Instance Table

Instance Name	Physical Address
CPSW	5282 2350h

Figure 4-991. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_RXN_PAUSETIMER_REG_N Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_PAUSETIMER															
R/W															
0h															

Access Types Legend

Table 4-2158. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_RXN_PAUSETIMER_REG_N Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	RX_PAUSETIMER	R/W	0h	RX Pause Timer Value

4.18.164 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_TX_PAUSETIMER_REG Registers

4.18.164.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_TX_PAUSETIMER_REG Register (Offset = 22370h) [reset = 0h]

Short Description: pn_mac_tx_pausetimer_reg

Long Description: Enet Port N 802.3 Tx Pause Timer

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Table 4-2159. Instance Table

Instance Name	Physical Address
CPSW	5282 2370h

Figure 4-992. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_TX_PAUSETIMER_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_PAUSETIMER															
R/W															
0h															

Access Types Legend

Table 4-2160. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_TX_PAUSETIMER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	TX_PAUSETIMER	R/W	0h	TX Pause Timer Value

4.18.165 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_TXN_PAUSETIMER_REG_N Registers

4.18.165.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_TXN_PAUSETIMER_REG_N Register (Offset = 22380h) [reset = 0h]

Short Description: pn_mac_txn_pausetimer_reg

Long Description: Enet Port N PFC Priority P Tx Pause Timer

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Offset = 22380h + (j * 4h); where j = 0h to 7h

Table 4-2161. Instance Table

Instance Name	Physical Address
CPSW	5282 2380h

Figure 4-993. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_TXN_PAUSETIMER_REG_N Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_PAUSETIMER															
R/W															
0h															

Access Types Legend

Table 4-2162. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_TXN_PAUSETIMER_REG_N Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	TX_PAUSETIMER	R/W	0h	TX Pause Timer Value

4.18.166 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_EMCONTROL_REG Registers

4.18.166.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_EMCONTROL_REG Register (Offset = 223A0h) [reset = 0h]

Short Description: pn_mac_emcontrol_reg

Long Description: Enet Port N Emulation Control

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Table 4-2163. Instance Table

Instance Name	Physical Address
CPSW	5282 23A0h

Figure 4-994. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_EMCONTROL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														SOFT	FREE
NONE														R/W	R/W
0														0h	0h

Access Types Legend

Table 4-2164. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_EMCONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1	SOFT	R/W	0h	Emulation Soft Bit
0	FREE	R/W	0h	Emulation Free Bit

4.18.167 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_TX_GAP_REG Registers

4.18.167.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_TX_GAP_REG Register (Offset = 223A4h) [reset = ch]

Short Description: pn_mac_tx_gap_reg

Long Description: Enet Port N Tx Inter Packet Gap

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Table 4-2165. Instance Table

Instance Name	Physical Address
CPSW	5282 23A4h

Figure 4-995. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_TX_GAP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
6e															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_GAP															
R/W															
ch															

Access Types Legend

Table 4-2166. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_TX_GAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	TX_GAP	R/W	Ch	Transmit Inter-Packet Gap

4.18.168 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_PORT_CONFIG Registers

4.18.168.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_PORT_CONFIG Register (Offset = 223A8h) [reset = 2h]

Short Description: Port Configuration

Long Description: Enet Port N Port Configuration

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Table 4-2167. Instance Table

Instance Name	Physical Address
CPSW	5282 23A8h

Figure 4-996. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_PORT_CONFIG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
1															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						IET	XGMII	INTERVLAN_ROUTES							
NONE						R	R	R							
1						0h	0h	2h							

Access Types Legend

Table 4-2168. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_MAC_PORT_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9	IET	R	0h	IET support
8	XGMII	R	0h	No XGMII support
7:0	INTERVLAN_ROUTES	R	2h	The number of InterVLAN routes

4.18.169 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_INTERVLAN_OPX_POINTER_REG Registers

4.18.169.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_INTERVLAN_OPX_POINTER_REG Register (Offset = 223ACh) [reset = 0h]

Short Description: pn_opx_pointer_reg

Long Description: Enet Port N Tx Egress InterVLAN Operation Pointer

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Table 4-2169. Instance Table

Instance Name	Physical Address
CPSW	5282 23ACh

Figure 4-997. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_INTERVLAN_OPX_POINTER_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														POINTER	
NONE														R/W	
0														0h	

Access Types Legend

Table 4-2170. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_INTERVLAN_OPX_POINTER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1:0	POINTER	R/W	0h	InterVLAN location pointer: This field points to the InterVLAN location that will be read/written by accesses to Enet_Pn_InterVLANx_A/B.

4.18.170 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_INTERVLAN_OPX_A_REG Registers

4.18.170.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_INTERVLAN_OPX_A_REG Register (Offset = 223B0h) [reset = 0h]

Short Description: pn_opx_a_reg

Long Description: Enet Port N Tx Egress InterVLAN A

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Table 4-2171. Instance Table

Instance Name	Physical Address
CPSW	5282 23B0h

Figure 4-998. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_INTERVLAN_OPX_A_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DA_23_16								DA_31_24							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DA_39_32								DA_47_40							
R/W								R/W							
0h								0h							

Access Types Legend

Table 4-2172. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_INTERVLAN_OPX_A_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	DA_23_16	R/W	0h	Destination Address bits 23:16
23:16	DA_31_24	R/W	0h	Destination Address bits 31:24
15:8	DA_39_32	R/W	0h	Destination Address bits 39:32
7:0	DA_47_40	R/W	0h	Destination Address bits 47:40

4.18.171 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_INTERVLAN_OPX_B_REG Registers

4.18.171.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_INTERVLAN_OPX_B_REG Register (Offset = 223B4h) [reset = 0h]

Short Description: pn_opx_b_reg

Long Description: Enet Port N Tx Egress InterVLAN B

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Table 4-2173. Instance Table

Instance Name	Physical Address
CPSW	5282 23B4h

Figure 4-999. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_INTERVLAN_OPX_B_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SA_39_32								SA_47_40							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DA_7_0								DA_15_8							
R/W								R/W							
0h								0h							

Access Types Legend

Table 4-2174. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_INTERVLAN_OPX_B_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SA_39_32	R/W	0h	Source Address bits 39:32
23:16	SA_47_40	R/W	0h	Source Address bits 47:40
15:8	DA_7_0	R/W	0h	Destination Address bits 7:0
7:0	DA_15_8	R/W	0h	Destination Address bits 15:8

4.18.172 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_INTERVLAN_OPX_C_REG Registers

4.18.172.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_INTERVLAN_OPX_C_REG Register (Offset = 223B8h) [reset = 0h]

Short Description: pn_opx_c_reg

Long Description: Enet Port N Tx Egress InterVLAN C

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Table 4-2175. Instance Table

Instance Name	Physical Address
CPSW	5282 23B8h

Figure 4-1000. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_INTERVLAN_OPX_C_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SA_7_0								SA_15_8							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SA_23_16								SA_31_24							
R/W								R/W							
0h								0h							

Access Types Legend

Table 4-2176. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_INTERVLAN_OPX_C_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SA_7_0	R/W	0h	Source Address bits 7:0
23:16	SA_15_8	R/W	0h	Source Address bits 15:8
15:8	SA_23_16	R/W	0h	Source Address bits 23:16
7:0	SA_31_24	R/W	0h	Source Address bits 31:24

4.18.173 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_INTERVLAN_OPX_D_REG Registers

4.18.173.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_INTERVLAN_OPX_D_REG Register (Offset = 223BCh) [reset = 0h]

Short Description: pn_opx_d_reg

Long Description: Enet Port N Tx Egress InterVLAN D

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Table 4-2177. Instance Table

Instance Name	Physical Address
CPSW	5282 23BCh

Figure 4-1001. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_INTERVLAN_OPX_D_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DECREMENT_TTL	DEST_FORCE_UNTAGGED_EGRESS	REPLACE_DA_SA	REPLACE_VID	VID											
R/W	R/W	R/W	R/W	R/W											
0h	0h	0h	0h	0h											

Access Types Legend

Table 4-2178. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_0_PN_INTERVLAN_OPX_D_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15	DECREMENT_TTL	R/W	0h	Decrement Time To Live: When set, the Time To Live (TTL) field in the header is decremented.
14	DEST_FORCE_UNTAGGED_EGRESS	R/W	0h	Destination VLAN Force Untagged Egress: When set, this bit indicates that the VLAN should be removed on egress for the routed packet.
13	REPLACE_DA_SA	R/W	0h	Replace Destination Address and Source Address: When set this bit indicates that the routed packet destination address should be replaced by da[47:0] and the source address should be replaced by sa[47:0].
12	REPLACE_VID	R/W	0h	Replace VLAN ID: When set this bit indicates that the VLAN ID should be replaced for the routed packet.
11:0	VID	R/W	0h	VLAN ID

4.18.174 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_RESERVED_REG Registers

4.18.174.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_RESERVED_REG Register (Offset = 23000h) [reset = 0h]

Short Description: pn_reserved_reg

Long Description: Reserved

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Table 4-2179. Instance Table

Instance Name	Physical Address
CPSW	5282 3000h

Figure 4-1002. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_RESERVED_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R															
0h															

Access Types Legend

Table 4-2180. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_RESERVED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R		Reserved register for memory map alignment

4.18.175 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_CONTROL_REG Registers

4.18.175.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_CONTROL_REG Register (Offset = 23004h) [reset = 0h]

Short Description: pn_control_reg

Long Description: Enet Port N Control

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Table 4-2181. Instance Table

Instance Name	Physical Address
CPSW	5282 3004h

Figure 4-1003. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_CONTROL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														EST_PORT_EN	RESERVED
NONE														R/W	NONE
0														0h	0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_ECC_ERR_EN	TX_ECC_ERR_EN	RESERVED	TX_LPI_CLKSTOP_EN	RESERVED									DSCP_IPV6_EN	DSCP_IPV4_EN	RESERVED
R/W	R/W	NONE	R/W	NONE									R/W	R/W	NONE
0h	0h	0	0h	0									0h	0h	0

Access Types Legend

Table 4-2182. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE		Reserved
17	EST_PORT_EN	R/W	0h	EST Port Enable
16	RESERVED	NONE		Reserved
15	RX_ECC_ERR_EN	R/W	0h	Port 0 Receive ECC Error Enable
14	TX_ECC_ERR_EN	R/W	0h	Port 0 Transmit ECC Error Enable
13	RESERVED	NONE		Reserved
12	TX_LPI_CLKSTOP_EN	R/W	0h	Transmit LPI clockstop enable
11:3	RESERVED	NONE		Reserved
2	DSCP_IPV6_EN	R/W	0h	IPv6 DSCP enable
1	DSCP_IPV4_EN	R/W	0h	IPv4 DSCP enable
0	RESERVED	NONE		Reserved

4.18.176 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAX_BLKS_REG Registers

4.18.176.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAX_BLKS_REG Register (Offset = 23008h) [reset = 1004h]

Short Description: pn_max_blks_reg

Long Description: Enet Port N FIFO Max Blocks

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Table 4-2183. Instance Table

Instance Name	Physical Address
CPSW	5282 3008h

Figure 4-1004. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAX_BLKS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
174876e80a															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_MAX_BLKS								RX_MAX_BLKS							
R/W								R/W							
10h								4h							

Access Types Legend

Table 4-2184. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAX_BLKS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	TX_MAX_BLKS	R/W	10h	Transmit FIFO maximum blocks
7:0	RX_MAX_BLKS	R/W	4h	Receive FIFO maximum blocks

4.18.177 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_BLK_CNT_REG Registers

4.18.177.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_BLK_CNT_REG Register (Offset = 23010h) [reset = 1h]

Short Description: pn_blk_cnt_reg

Long Description: Enet Port N FIFO Block Usage Count

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Table 4-2185. Instance Table

Instance Name	Physical Address
CPSW	5282 3010h

Figure 4-1005. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_BLK_CNT_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										RX_BLK_CNT_P					
NONE										R					
0										0h					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			TX_BLK_CNT					RESERVED		RX_BLK_CNT_E					
NONE			R					NONE		R					
0			0h					0		1h					

Access Types Legend

Table 4-2186. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_BLK_CNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE		Reserved
21:16	RX_BLK_CNT_P	R	0h	Receive Prempt Queue Block Count Usage
15:13	RESERVED	NONE		Reserved
12:8	TX_BLK_CNT	R	0h	Transmit Block Count Usage
7:6	RESERVED	NONE		Reserved
5:0	RX_BLK_CNT_E	R	1h	Receive Block Count Usage

4.18.178 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_PORT_VLAN_REG Registers

4.18.178.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_PORT_VLAN_REG Register (Offset = 23014h) [reset = 0h]

Short Description: pn_port_vlan_reg

Long Description: Enet Port N VLAN

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Table 4-2187. Instance Table

Instance Name	Physical Address
CPSW	5282 3014h

Figure 4-1006. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_PORT_VLAN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PORT_PRI			PORT_CFI	PORT_VID											
R/W			R/W	R/W											
0h			0h	0h											

Access Types Legend

Table 4-2188. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_PORT_VLAN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:13	PORT_PRI	R/W	0h	Port VLAN Priority
12	PORT_CFI	R/W	0h	Port CFI bit
11:0	PORT_VID	R/W	0h	Port VLAN ID

4.18.179 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_PRI_MAP_REG Registers

4.18.179.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_PRI_MAP_REG Register (Offset = 23018h) [reset = 76543210h]

Short Description: pn_tx_pri_map_reg

Long Description: Enet Port N Tx Header Pri to Switch Pri Mapping

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Table 4-2189. Instance Table

Instance Name	Physical Address
CPSW	5282 3018h

Figure 4-1007. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		PRI7		RESERVED		PRI6		RESERVED		PRI5		RESERVED		PRI4	
NONE		R/W		NONE		R/W		NONE		R/W		NONE		R/W	
0		7h		1		6h		0		5h		1		4h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		PRI3		RESERVED		PRI2		RESERVED		PRI1		RESERVED		PRI0	
NONE		R/W		NONE		R/W		NONE		R/W		NONE		R/W	
0		3h		1		2h		0		1h		1		0h	

Access Types Legend

Table 4-2190. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE		Reserved
30:28	PRI7	R/W	7h	Priority 7
27	RESERVED	NONE		Reserved
26:24	PRI6	R/W	6h	Priority 6
23	RESERVED	NONE		Reserved
22:20	PRI5	R/W	5h	Priority 5
19	RESERVED	NONE		Reserved
18:16	PRI4	R/W	4h	Priority 4
15	RESERVED	NONE		Reserved
14:12	PRI3	R/W	3h	Priority 3
11	RESERVED	NONE		Reserved
10:8	PRI2	R/W	2h	Priority 2
7	RESERVED	NONE		Reserved
6:4	PRI1	R/W	1h	Priority 1
3	RESERVED	NONE		Reserved
2:0	PRI0	R/W	0h	Priority 0

4.18.180 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_PRI_CTL_REG Registers

4.18.180.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_PRI_CTL_REG Register (Offset = 2301Ch) [reset = 9000h]

Short Description: pn_pri_ctl_reg

Long Description: Enet Port N Priority Control

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Table 4-2191. Instance Table

Instance Name	Physical Address
CPSW	5282 301Ch

Figure 4-1008. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_PRI_CTL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TX_FLOW_PRI								RX_FLOW_PRI							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_HOST_BLKS_REM				RESERVED											
R/W				NONE											
9h				0											

Access Types Legend

Table 4-2192. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_PRI_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TX_FLOW_PRI	R/W	0h	Transmit Priority Based Flow Control Enable (per priority)
23:16	RX_FLOW_PRI	R/W	0h	Receive Priority Based Flow Control Enable (per priority)
15:12	TX_HOST_BLKS_REM	R/W	9h	Transmit FIFO Blocks that must be free before a non rate-limited CPPI Port 0 receive thread can begin sending a packet
11:0	RESERVED	NONE		Reserved

4.18.181 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_RX_PRI_MAP_REG Registers

4.18.181.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_RX_PRI_MAP_REG Register (Offset = 23020h) [reset = 76543210h]

Short Description: pn_rx_pri_map_reg

Long Description: Enet Port N RX Pkt Pri to Header Pri Map

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Table 4-2193. Instance Table

Instance Name	Physical Address
CPSW	5282 3020h

Figure 4-1009. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_RX_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	PRI7			RESERVED	PRI6			RESERVED	PRI5			RESERVED	PRI4		
NONE	R/W			NONE	R/W			NONE	R/W			NONE	R/W		
0	7h			1	6h			0	5h			1	4h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	PRI3			RESERVED	PRI2			RESERVED	PRI1			RESERVED	PRI0		
NONE	R/W			NONE	R/W			NONE	R/W			NONE	R/W		
0	3h			1	2h			0	1h			1	0h		

Access Types Legend

Table 4-2194. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_RX_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE		Reserved
30:28	PRI7	R/W	7h	Priority 7
27	RESERVED	NONE		Reserved
26:24	PRI6	R/W	6h	Priority 6
23	RESERVED	NONE		Reserved
22:20	PRI5	R/W	5h	Priority 5
19	RESERVED	NONE		Reserved
18:16	PRI4	R/W	4h	Priority 4
15	RESERVED	NONE		Reserved
14:12	PRI3	R/W	3h	Priority 3
11	RESERVED	NONE		Reserved
10:8	PRI2	R/W	2h	Priority 2
7	RESERVED	NONE		Reserved
6:4	PRI1	R/W	1h	Priority 1
3	RESERVED	NONE		Reserved
2:0	PRI0	R/W	0h	Priority 0

4.18.182 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_RX_MAXLEN_REG Registers

4.18.182.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_RX_MAXLEN_REG Register (Offset = 23024h) [reset = 5eeh]

Short Description: pn_rx_maxlen_reg

Long Description: Enet Port N Receive Frame Max Length

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Table 4-2195. Instance Table

Instance Name	Physical Address
CPSW	5282 3024h

Figure 4-1010. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_RX_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
3c4450df															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		RX_MAXLEN													
NONE		R/W													
3c4450df		5eeh													

Access Types Legend

Table 4-2196. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_RX_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE		Reserved
13:0	RX_MAXLEN	R/W	5EEh	Rx Maximum Frame Length

4.18.183 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_BLKS_PRI_REG Registers

4.18.183.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_BLKS_PRI_REG Register (Offset = 23028h) [reset = 1245678h]

Short Description: pn_tx_blks_pri_reg

Long Description: Enet Port N Transmit Block Sub Per Priority

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Table 4-2197. Instance Table

Instance Name	Physical Address
CPSW	5282 3028h

Figure 4-1011. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_BLKS_PRI_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRI7				PRI6				PRI5				PRI4			
R/W				R/W				R/W				R/W			
0h				1h				2h				4h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI3				PRI2				PRI1				PRI0			
R/W				R/W				R/W				R/W			
5h				6h				7h				8h			

Access Types Legend

Table 4-2198. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_BLKS_PRI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PRI7	R/W	0h	Priority 7 Port Transmit Blocks
27:24	PRI6	R/W	1h	Priority 6 Port Transmit Blocks
23:20	PRI5	R/W	2h	Priority 5 Port Transmit Blocks
19:16	PRI4	R/W	4h	Priority 4 Port Transmit Blocks
15:12	PRI3	R/W	5h	Priority 3 Port Transmit Blocks
11:8	PRI2	R/W	6h	Priority 2 Port Transmit Blocks
7:4	PRI1	R/W	7h	Priority 1 Port Transmit Blocks
3:0	PRI0	R/W	8h	Priority 0 Port Transmit Blocks

4.18.184 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_IDLE2LPI_REG Registers

4.18.184.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_IDLE2LPI_REG Register (Offset = 23030h) [reset = 0h]

Short Description: pn_idle2lpi_reg

Long Description: Enet Port N EEE Idle to LPI counter

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Table 4-2199. Instance Table

Instance Name	Physical Address
CPSW	5282 3030h

Figure 4-1012. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_IDLE2LPI_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								COUNT							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2200. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_IDLE2LPI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	COUNT	R/W	0h	EEE Idle to LPI counter load value

4.18.185 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_LPI2WAKE_REG Registers

4.18.185.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_LPI2WAKE_REG Register (Offset = 23034h) [reset = 0h]

Short Description: pn_lpi2wake_reg

Long Description: Enet Port N EEE LPI to wake counter

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Table 4-2201. Instance Table

Instance Name	Physical Address
CPSW	5282 3034h

Figure 4-1013. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_LPI2WAKE_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								COUNT							
NONE								R/W							
0								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2202. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_LPI2WAKE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE		Reserved
23:0	COUNT	R/W	0h	EEE LPI to wake counter load value

4.18.186 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_EEE_STATUS_REG Registers

4.18.186.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_EEE_STATUS_REG Register (Offset = 23038h) [reset = 62h]

Short Description: pn_eee_status_reg

Long Description: Enet Port N EEE status

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Table 4-2203. Instance Table

Instance Name	Physical Address
CPSW	5282 3038h

Figure 4-1014. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_EEE_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
1adb1															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									TX_FIFO_EMPTY	RX_FIFO_EMPTY	TX_FIFO_HOLD	TX_WAKE	TX_LPI	RX_LPI	WAIT_IDLE2LPI
NONE									R	R	R	R	R	R	R
1adb1									1h	1h	0h	0h	0h	1h	0h

Access Types Legend

Table 4-2204. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_EEE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE		Reserved
6	TX_FIFO_EMPTY	R	1h	Transmit FIFO (switch egress) is empty - contains no packets
5	RX_FIFO_EMPTY	R	1h	Receive FIFO (switch ingress) is empty - contains no packets
4	TX_FIFO_HOLD	R	0h	Transmit FIFO hold - asserted in the LPI state and during the LPI2WAKE count time
3	TX_WAKE	R	0h	Transmit wakeup - asserted in the transmit LPI2WAKE count time
2	TX_LPI	R	0h	Transmit LPI state - asserted when the port 0 transmit is in the LPI state
1	RX_LPI	R	1h	Receive LPI state - asserted when the port 0 receive is in the LPI state
0	WAIT_IDLE2LPI	R	0h	CPPI port 0 wait idle to LPI - asserted when port 0 is counting the IDLE2LPI time

4.18.187 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_FIFO_STATUS_REG Registers

4.18.187.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_FIFO_STATUS_REG Register (Offset = 23050h) [reset = ff00h]

Short Description: pn_fifo_status_reg

Long Description: Enet Port N FIFO STATUS

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Table 4-2205. Instance Table

Instance Name	Physical Address
CPSW	5282 3050h

Figure 4-1015. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_FIFO_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED													EST_BUFACT	EST_ADD_ERR	EST_CNT_ERR
NONE													R	R	R
19deac0d80													0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_E_MAC_ALLOW								TX_PRI_ACTIVE							
R								R							
ffh								0h							

Access Types Legend

Table 4-2206. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_FIFO_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE		Reserved
18	EST_BUFACT	R	0h	Transmit FIFO EST Buffer Active
17	EST_ADD_ERR	R	0h	Transmit FIFO EST Address Error
16	EST_CNT_ERR	R	0h	Transmit FIFO EST Count Error
15:8	TX_E_MAC_ALLOW	R	FFh	Transmit FIFO Express Queue Priority Allow
7:0	TX_PRI_ACTIVE	R	0h	Transmit FIFO Priority Active

4.18.188 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_EST_CONTROL_REG Registers

4.18.188.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_EST_CONTROL_REG Register (Offset = 23060h) [reset = 0h]

Short Description: pn_est_control_reg

Long Description: Enet Port N EST CONTROL

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Table 4-2207. Instance Table

Instance Name	Physical Address
CPSW	5282 3060h

Figure 4-1016. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_EST_CONTROL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						EST_FILL_MARGIN									
NONE						R/W									
0						0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EST_PREMPT_COMP							EST_FILL_EN	EST_TS_PRI			EST_TS_ONEPRI	EST_TS_FIRST	EST_TS_EN	EST_BUFSEL	EST_ONEBUF
R/W							R/W	R/W			R/W	R/W	R/W	R/W	R/W
0h							0h	0h			0h	0h	0h	0h	0h

Access Types Legend

Table 4-2208. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_EST_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE		Reserved
25:16	EST_FILL_MARGIN	R/W	0h	Transmit FIFO EST Fill Margin
15:9	EST_PREMPT_COMP	R/W	0h	Transmit FIFO EST Prempt Comparison Value to Clear wire
8	EST_FILL_EN	R/W	0h	Transmit FIFO EST Fill Enable
7:5	EST_TS_PRI	R/W	0h	Transmit FIFO EST TimeStamp Priority
4	EST_TS_ONEPRI	R/W	0h	Transmit FIFO EST TimeStamp One Priority
3	EST_TS_FIRST	R/W	0h	Transmit FIFO EST TimeStamp First Express Packet
2	EST_TS_EN	R/W	0h	Transmit FIFO EST TimeStamp Enable
1	EST_BUFSEL	R/W	0h	Transmit FIFO EST Buffer Select
0	EST_ONEBUF	R/W	0h	Transmit FIFO EST One Buffer

4.18.189 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_RX_DSCP_MAP_REG_N Registers

4.18.189.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_RX_DSCP_MAP_REG_N Register (Offset = 23120h) [reset = 0h]

Short Description: pn_rx_dscp_map_reg

Long Description: Enet Port N Receive IPV4/IPV6 DSCP Map M

Return to Summary Table

Offset = 23120h + (j * 4h); where j = 0h to 7h

Table 4-2209. Instance Table

Instance Name	Physical Address
CPSW	5282 3120h

Figure 4-1017. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_RX_DSCP_MAP_REG_N Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		PRI7		RESERVED		PRI6		RESERVED		PRI5		RESERVED		PRI4	
NONE		R/W		NONE		R/W		NONE		R/W		NONE		R/W	
0		0h		0		0h		0		0h		0		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		PRI3		RESERVED		PRI2		RESERVED		PRI1		RESERVED		PRI0	
NONE		R/W		NONE		R/W		NONE		R/W		NONE		R/W	
0		0h		0		0h		0		0h		0		0h	

Access Types Legend

Table 4-2210. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_RX_DSCP_MAP_REG_N Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE		Reserved
30:28	PRI7	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+7 is mapped to this received priority
27	RESERVED	NONE		Reserved
26:24	PRI6	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+6 is mapped to this received priority
23	RESERVED	NONE		Reserved
22:20	PRI5	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+5 is mapped to this received priority
19	RESERVED	NONE		Reserved
18:16	PRI4	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+4 is mapped to this received priority
15	RESERVED	NONE		Reserved
14:12	PRI3	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+3 is mapped to this received priority
11	RESERVED	NONE		Reserved
10:8	PRI2	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+2 is mapped to this received priority
7	RESERVED	NONE		Reserved

Table 4-2210. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_RX_DSCP_MAP_REG_N Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:4	PRI1	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+1 is mapped to this received priority
3	RESERVED	NONE		Reserved
2:0	PRI0	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+0 is mapped to this received priority

4.18.190 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_PRI_CIR_REG_N Registers

4.18.190.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_PRI_CIR_REG_N Register (Offset = 23140h) [reset = 0h]

Short Description: pn_pri_send_reg

Long Description: Enet Port N Rx Priority P Committed Information Rate Value

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Offset = 23140h + (j * 4h); where j = 0h to 7h

Table 4-2211. Instance Table

Instance Name	Physical Address
CPSW	5282 3140h

Figure 4-1018. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_PRI_CIR_REG_N Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI_CIR											
NONE				R/W											
0				0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI_CIR															
R/W															
0h															

Access Types Legend

Table 4-2212. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_PRI_CIR_REG_N Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE		Reserved
27:0	PRI_CIR	R/W	0h	Priority N committed information rate

4.18.191 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_PRI_EIR_REG_N Registers

4.18.191.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_PRI_EIR_REG_N Register (Offset = 23160h) [reset = 0h]

Short Description: pn_pri_idle_reg

Long Description: Enet Port N Rx Priority P Excess Informatoin Rate Value

Return to Summary Table

Offset = 23160h + (j * 4h); where j = 0h to 7h

Table 4-2213. Instance Table

Instance Name	Physical Address
CPSW	5282 3160h

Figure 4-1019. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_PRI_EIR_REG_N Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI_EIR											
NONE				R/W											
0				0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI_EIR															
R/W															
0h															

Access Types Legend

Table 4-2214. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_PRI_EIR_REG_N Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE		Reserved
27:0	PRI_EIR	R/W	0h	Priority N Excess Information Rate count

4.18.192 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_D_THRESH_SET_L_REG Registers

4.18.192.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_D_THRESH_SET_L_REG Register (Offset = 23180h) [reset = 1f1f1f1fh]

Short Description: pn_tx_d_thresh_set_l_reg

Long Description: Enet Port N Tx PFC Destination Threshold Set Low

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Table 4-2215. Instance Table

Instance Name	Physical Address
CPSW	5282 3180h

Figure 4-1020. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_D_THRESH_SET_L_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI3					RESERVED			PRI2				
NONE			R/W					NONE			R/W				
b			1fh					b			1fh				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI1					RESERVED			PRI0				
NONE			R/W					NONE			R/W				
b			1fh					b			1fh				

Access Types Legend

Table 4-2216. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_D_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23:21	RESERVED	NONE		Reserved
20:16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15:13	RESERVED	NONE		Reserved
12:8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7:5	RESERVED	NONE		Reserved
4:0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

4.18.193 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_D_THRESH_SET_H_REG Registers

4.18.193.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_D_THRESH_SET_H_REG Register (Offset = 23184h) [reset = 1f1f1f1fh]

Short Description: pn_tx_d_thresh_set_h_reg

Long Description: Enet Port N Tx PFC Destination Threshold Set High

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Table 4-2217. Instance Table

Instance Name	Physical Address
CPSW	5282 3184h

Figure 4-1021. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_D_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI7					RESERVED			PRI6				
NONE			R/W					NONE			R/W				
b			1fh					b			1fh				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI5					RESERVED			PRI4				
NONE			R/W					NONE			R/W				
b			1fh					b			1fh				

Access Types Legend

Table 4-2218. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_D_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23:21	RESERVED	NONE		Reserved
20:16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15:13	RESERVED	NONE		Reserved
12:8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7:5	RESERVED	NONE		Reserved
4:0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

4.18.194 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_D_THRESH_CLR_L_REG Registers

4.18.194.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_D_THRESH_CLR_L_REG Register (Offset = 23188h) [reset = 0h]

Short Description: pn_tx_d_thresh_clr_l_reg

Long Description: Enet Port N Tx PFC Destination Threshold Clr Low

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Table 4-2219. Instance Table

Instance Name	Physical Address
CPSW	5282 3188h

Figure 4-1022. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_D_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI3					RESERVED			PRI2				
NONE			R/W					NONE			R/W				
0			0h					0			0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI1					RESERVED			PRI0				
NONE			R/W					NONE			R/W				
0			0h					0			0h				

Access Types Legend

Table 4-2220. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_D_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23:21	RESERVED	NONE		Reserved
20:16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15:13	RESERVED	NONE		Reserved
12:8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7:5	RESERVED	NONE		Reserved
4:0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

4.18.195 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_D_THRESH_CLR_H_REG Registers

4.18.195.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_D_THRESH_CLR_H_REG Register (Offset = 2318Ch) [reset = 0h]

Short Description: pn_tx_d_thresh_clr_h_reg

Long Description: Enet Port N Tx PFC Destination Threshold Clr High

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Table 4-2221. Instance Table

Instance Name	Physical Address
CPSW	5282 318Ch

Figure 4-1023. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_D_THRESH_CLR_H_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI7					RESERVED			PRI6				
NONE			R/W					NONE			R/W				
0			0h					0			0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI5					RESERVED			PRI4				
NONE			R/W					NONE			R/W				
0			0h					0			0h				

Access Types Legend

Table 4-2222. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_D_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23:21	RESERVED	NONE		Reserved
20:16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15:13	RESERVED	NONE		Reserved
12:8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7:5	RESERVED	NONE		Reserved
4:0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

4.18.196 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_L_REG Registers

4.18.196.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_L_REG Register (Offset = 23190h) [reset = 1f1f1f1fh]

Short Description: pn_tx_g_buf_thresh_set_l_reg

Long Description: Enet Port N Tx PFC Global Buffer Threshold Set Low

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Table 4-2223. Instance Table

Instance Name	Physical Address
CPSW	5282 3190h

Figure 4-1024. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_L_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI3					RESERVED			PRI2				
NONE			R/W					NONE			R/W				
b			1fh					b			1fh				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI1					RESERVED			PRI0				
NONE			R/W					NONE			R/W				
b			1fh					b			1fh				

Access Types Legend

Table 4-2224. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23:21	RESERVED	NONE		Reserved
20:16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15:13	RESERVED	NONE		Reserved
12:8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7:5	RESERVED	NONE		Reserved
4:0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

4.18.197 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_H_REG Registers

4.18.197.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_H_REG Register (Offset = 23194h) [reset = 1f1f1f1fh]

Short Description: pn_tx_g_buf_thresh_set_h_reg

Long Description: Enet Port N Tx PFC Global Buffer Threshold Set High

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Table 4-2225. Instance Table

Instance Name	Physical Address
CPSW	5282 3194h

Figure 4-1025. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI7					RESERVED			PRI6				
NONE			R/W					NONE			R/W				
b			1fh					b			1fh				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI5					RESERVED			PRI4				
NONE			R/W					NONE			R/W				
b			1fh					b			1fh				

Access Types Legend

Table 4-2226. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_G_BUF_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23:21	RESERVED	NONE		Reserved
20:16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15:13	RESERVED	NONE		Reserved
12:8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7:5	RESERVED	NONE		Reserved
4:0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

4.18.198 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_L_REG Registers

4.18.198.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_L_REG Register (Offset = 23198h) [reset = 0h]

Short Description: pn_tx_g_buf_thresh_clr_l_reg

Long Description: Enet Port N Tx PFC Global Buffer Threshold Clr Low

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Table 4-2227. Instance Table

Instance Name	Physical Address
CPSW	5282 3198h

Figure 4-1026. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI3					RESERVED			PRI2				
NONE			R/W					NONE			R/W				
0			0h					0			0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI1					RESERVED			PRI0				
NONE			R/W					NONE			R/W				
0			0h					0			0h				

Access Types Legend

Table 4-2228. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23:21	RESERVED	NONE		Reserved
20:16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15:13	RESERVED	NONE		Reserved
12:8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7:5	RESERVED	NONE		Reserved
4:0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

4.18.199 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_H_REG Registers

4.18.199.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_H_REG Register (Offset = 2319Ch) [reset = 0h]

Short Description: pn_tx_g_buf_thresh_clr_h_reg

Long Description: Enet Port N Tx PFC Global Buffer Threshold Clr High

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Table 4-2229. Instance Table

Instance Name	Physical Address
CPSW	5282 319Ch

Figure 4-1027. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_H_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI7					RESERVED			PRI6				
NONE			R/W					NONE			R/W				
0			0h					0			0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI5					RESERVED			PRI4				
NONE			R/W					NONE			R/W				
0			0h					0			0h				

Access Types Legend

Table 4-2230. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_G_BUF_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23:21	RESERVED	NONE		Reserved
20:16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15:13	RESERVED	NONE		Reserved
12:8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7:5	RESERVED	NONE		Reserved
4:0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

4.18.200 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_L_REG Registers

4.18.200.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_L_REG Register (Offset = 23300h) [reset = 0h]

Short Description: pn_tx_d_oflow_addval_l_reg

Long Description: Enet Port N Tx Destination Out Flow Add Values Low

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Table 4-2231. Instance Table

Instance Name	Physical Address
CPSW	5282 3300h

Figure 4-1028. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_L_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI3					RESERVED			PRI2				
NONE			R/W					NONE			R/W				
0			0h					0			0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI1					RESERVED			PRI0				
NONE			R/W					NONE			R/W				
0			0h					0			0h				

Access Types Legend

Table 4-2232. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:24	PRI3	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 3
23:21	RESERVED	NONE		Reserved
20:16	PRI2	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 2
15:13	RESERVED	NONE		Reserved
12:8	PRI1	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 1
7:5	RESERVED	NONE		Reserved
4:0	PRI0	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 0

4.18.201 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_H_REG Registers

4.18.201.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_H_REG Register (Offset = 23304h) [reset = 0h]

Short Description: pn_tx_d_oflow_addval_h_reg

Long Description: Enet Port N Tx Destination Out Flow Add Values High

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Table 4-2233. Instance Table

Instance Name	Physical Address
CPSW	5282 3304h

Figure 4-1029. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_H_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI7					RESERVED			PRI6				
NONE			R/W					NONE			R/W				
0			0h					0			0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI5					RESERVED			PRI4				
NONE			R/W					NONE			R/W				
0			0h					0			0h				

Access Types Legend

Table 4-2234. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TX_D_OFLOW_ADDVAL_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE		Reserved
28:24	PRI7	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 7
23:21	RESERVED	NONE		Reserved
20:16	PRI6	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 6
15:13	RESERVED	NONE		Reserved
12:8	PRI5	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 5
7:5	RESERVED	NONE		Reserved
4:0	PRI4	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 4

4.18.202 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_SA_L_REG Registers

4.18.202.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_SA_L_REG Register (Offset = 23308h) [reset = 0h]

Short Description: pn_sa_l_reg

Long Description: Enet Port N Tx Pause Frame Source Address Low

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Table 4-2235. Instance Table

Instance Name	Physical Address
CPSW	5282 3308h

Figure 4-1030. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_SA_L_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MACSRCADDR_7_0								MACSRCADDR_15_8							
R/W								R/W							
0h								0h							

Access Types Legend

Table 4-2236. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_SA_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	MACSRCADDR_7_0	R/W	0h	Source Address Lower 8 bits
7:0	MACSRCADDR_15_8	R/W	0h	Source Address bits 15:8

4.18.203 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_SA_H_REG Registers

4.18.203.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_SA_H_REG Register (Offset = 2330Ch) [reset = 0h]

Short Description: pn_sa_h_reg

Long Description: Enet Port N Tx Pause Frame Source Address High

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Table 4-2237. Instance Table

Instance Name	Physical Address
CPSW	5282 330Ch

Figure 4-1031. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_SA_H_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MACSRCADDR_23_16								MACSRCADDR_31_24							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MACSRCADDR_39_32								MACSRCADDR_47_40							
R/W								R/W							
0h								0h							

Access Types Legend

Table 4-2238. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_SA_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MACSRCADDR_23_16	R/W	0h	Source Address bits 23:16
23:16	MACSRCADDR_31_24	R/W	0h	Source Address bits 31:24
15:8	MACSRCADDR_39_32	R/W	0h	Source Address bits 39:32
7:0	MACSRCADDR_47_40	R/W	0h	Source Address bits 47:40

4.18.204 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TS_CTL_REG Registers

4.18.204.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TS_CTL_REG Register (Offset = 23310h) [reset = 0h]

Short Description: pn_ts_ctl_reg

Long Description: Enet Port N Time Sync Control

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Table 4-2239. Instance Table

Instance Name	Physical Address
CPSW	5282 3310h

Figure 4-1032. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TS_CTL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TS_MSG_TYPE_EN															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				TS_TX_HOST_TS_EN	TS_TX_ANNEX_E_EN	TS_RX_ANNEX_E_EN	TS_LTYPE2_EN	TS_TX_ANNEX_D_EN	TS_TX_VLAN_LTYPE2_EN	TS_TX_VLAN_LTYPE1_EN	TS_TX_ANNEX_F_EN	TS_RX_ANNEX_D_EN	TS_RX_VLAN_LTYPE2_EN	TS_RX_VLAN_LTYPE1_EN	TS_RX_ANNEX_F_EN
NONE				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0				0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-2240. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TS_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TS_MSG_TYPE_EN	R/W	0h	Time Sync Message Type Enable
15:12	RESERVED	NONE		Reserved
11	TS_TX_HOST_TS_EN	R/W	0h	Time Sync Transmit Host Time Stamp Enable
10	TS_TX_ANNEX_E_EN	R/W	0h	Time Synce Transmit Annex E Enable
9	TS_RX_ANNEX_E_EN	R/W	0h	Time Synce Receive Annex E Enable
8	TS_LTYPE2_EN	R/W	0h	Time Sync LTYPE 2 enable transmit and receive
7	TS_TX_ANNEX_D_EN	R/W	0h	Time Synce Transmit Annex D Enable
6	TS_TX_VLAN_LTYPE2_EN	R/W	0h	Time Sync Transmit VLAN LTYPE 2 enable
5	TS_TX_VLAN_LTYPE1_EN	R/W	0h	Time Sync Transmit VLAN LTYPE 1 enable
4	TS_TX_ANNEX_F_EN	R/W	0h	Time Synce Transmit Annex F Enable
3	TS_RX_ANNEX_D_EN	R/W	0h	Time Synce Receive Annex D Enable
2	TS_RX_VLAN_LTYPE2_EN	R/W	0h	Time Sync Receive VLAN LTYPE 2 enable
1	TS_RX_VLAN_LTYPE1_EN	R/W	0h	Time Sync Receive VLAN LTYPE 1 enable
0	TS_RX_ANNEX_F_EN	R/W	0h	Time Synce Receive Annex F Enable

4.18.205 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TS_SEQ_LTYPE_REG Registers

4.18.205.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TS_SEQ_LTYPE_REG Register (Offset = 23314h) [reset = 1e0000h]

Short Description: pn_ts_seq_ltype_reg

Long Description: Enet Port N Time Sync LTYPE (and SEQ_ID_OFFSET)

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Table 4-2241. Instance Table

Instance Name	Physical Address
CPSW	5282 3314h

Figure 4-1033. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TS_SEQ_LTYPE_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										TS_SEQ_ID_OFFSET					
NONE										R/W					
0										1eh					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_LTYPE1															
R/W															
0h															

Access Types Legend

Table 4-2242. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TS_SEQ_LTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE		Reserved
21:16	TS_SEQ_ID_OFFSET	R/W	1Eh	Time Sync Sequence ID Offset
15:0	TS_LTYPE1	R/W	0h	Time Sync LTYPE1

4.18.206 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TS_VLAN_LTYPE_REG Registers

4.18.206.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TS_VLAN_LTYPE_REG Register (Offset = 23318h) [reset = 0h]

Short Description: pn_ts_vlan_ltype_reg

Long Description: Enet Port N Time Sync VLAN2 and VLAN2

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Table 4-2243. Instance Table

Instance Name	Physical Address
CPSW	5282 3318h

Figure 4-1034. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TS_VLAN_LTYPE_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TS_VLAN_LTYPE2															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_VLAN_LTYPE1															
R/W															
0h															

Access Types Legend

Table 4-2244. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TS_VLAN_LTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TS_VLAN_LTYPE2	R/W	0h	Time Sync VLAN LTYPE2
15:0	TS_VLAN_LTYPE1	R/W	0h	Time Sync VLAN LTYPE1

4.18.207 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TS_CTL_LTYPE2_REG Registers

4.18.207.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TS_CTL_LTYPE2_REG Register (Offset = 2331Ch) [reset = 0h]

Short Description: pn_ts_ctl_ltype2_reg

Long Description: Enet Port N Time Sync Control and LTYPE 2

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Table 4-2245. Instance Table

Instance Name	Physical Address
CPSW	5282 331Ch

Figure 4-1035. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TS_CTL_LTYPE2_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							TS_UNI_EN	TS_TTL_NONZERO	TS_320	TS_319	TS_132	TS_131	TS_130	TS_129	TS_107
NONE							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0							0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_LTYPE2															
R/W															
0h															

Access Types Legend

Table 4-2246. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TS_CTL_LTYPE2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24	TS_UNI_EN	R/W	0h	Time Sync Unicast Enable
23	TS_TTL_NONZERO	R/W	0h	Time Sync Time to Live Non-zero Enable
22	TS_320	R/W	0h	Time Sync Destination IP Address 320 Enable
21	TS_319	R/W	0h	Time Sync Destination IP Address 319 Enable
20	TS_132	R/W	0h	Time Sync Destination IP Address 132 Enable
19	TS_131	R/W	0h	Time Sync Destination IP Address 131 Enable
18	TS_130	R/W	0h	Time Sync Destination IP Address 130 Enable
17	TS_129	R/W	0h	Time Sync Destination IP Address 129 Enable
16	TS_107	R/W	0h	Time Sync Destination IP Address 107 Enable
15:0	TS_LTYPE2	R/W	0h	Time Sync LTYPE2

4.18.208 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TS_CTL2_REG Registers

4.18.208.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TS_CTL2_REG Register (Offset = 23320h) [reset = 40000h]

Short Description: pn_ts_ctl2_reg

Long Description: Enet Port N Time Sync Control 2

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Table 4-2247. Instance Table

Instance Name	Physical Address
CPSW	5282 3320h

Figure 4-1036. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TS_CTL2_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										TS_DOMAIN_OFFSET					
NONE										R/W					
0										4h					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_MCAST_TYPE_EN															
R/W															
0h															

Access Types Legend

Table 4-2248. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_TS_CTL2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE		Reserved
21:16	TS_DOMAIN_OFFSET	R/W	4h	Time Sync Domain Offset
15:0	TS_MCAST_TYPE_EN	R/W	0h	Time Sync Multicast Destination Address Type Enable

4.18.209 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_CONTROL_REG Registers

4.18.209.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_CONTROL_REG Register (Offset = 23330h) [reset = 0h]

Short Description: pn_mac_control_reg

Long Description: Enet Port N Mac Control

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Table 4-2249. Instance Table

Instance Name	Physical Address
CPSW	5282 3330h

Figure 4-1037. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_CONTROL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							RX_CMF_EN	RX_CSF_EN	RX_CEF_EN	TX_SHORT_GAP_LIM_EN	EXT_TX_FLOW_EN	EXT_RX_FLOW_EN	EXT_EN	GIG_FORCE	IFCTL_B
NONE							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0							0h	0h	0h	0h	0h	0h	0h	0h	0h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IFCTL_A	RESERVED		CRC_TYPE	CMD_IDLE	TX_SHORT_GAP_ENABLE	RESERVED		GIG	TX_PACE	GMII_EN	TX_FLOW_EN	RX_FLOW_EN	MTEST	LOOPBACK	FULLDUPLEX
R/W	NONE		R/W	R/W	R/W	NONE		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0		0h	0h	0h	0		0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-2250. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24	RX_CMF_EN	R/W	0h	RX Copy MAC Control Frames Enable
23	RX_CSF_EN	R/W	0h	RX Copy Short Frames Enable
22	RX_CEF_EN	R/W	0h	RX Copy Error Frames Enable
21	TX_SHORT_GAP_LIM_EN	R/W	0h	Transmit Short Gap Limit Enable
20	EXT_TX_FLOW_EN	R/W	0h	External Transmit Flow Control Enable
19	EXT_RX_FLOW_EN	R/W	0h	External Receive Flow Control Enable
18	EXT_EN	R/W	0h	External Enable
17	GIG_FORCE	R/W	0h	Gigabit Mode Force
16	IFCTL_B	R/W	0h	Interface Control B
15	IFCTL_A	R/W	0h	Interface Control A
14:13	RESERVED	NONE		Reserved
12	CRC_TYPE	R/W	0h	Port CRC Type
11	CMD_IDLE	R/W	0h	Command Idle
10	TX_SHORT_GAP_ENABLE	R/W	0h	Transmit Short Gap Enable

Table 4-2250. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:8	RESERVED	NONE		Reserved
7	GIG	R/W	0h	Gigabit Mode
6	TX_PACE	R/W	0h	Transmit Pacing Enable
5	GMII_EN	R/W	0h	GMII Enable
4	TX_FLOW_EN	R/W	0h	Transmit Flow Control Enable
3	RX_FLOW_EN	R/W	0h	Receive Flow Control Enable
2	MTEST	R/W	0h	Manufacturing Test Mode
1	LOOPBACK	R/W	0h	Loop Back Mode
0	FULLDUPLEX	R/W	0h	Full Duplex mode

4.18.210 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_STATUS_REG Registers

4.18.210.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_STATUS_REG Register (Offset = 23334h) [reset = d0000000h]

Short Description: pn_mac_status_reg

Long Description: Enet Port N Mac Status

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Table 4-2251. Instance Table

Instance Name	Physical Address
CPSW	5282 3334h

Figure 4-1038. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IDLE	E_IDLE	RESERVED	MAC_TX_IDLE	TORF	TORF_PRI			TX_PFC_FLOW_ACT							
R	R	NONE	R	R	R			R							
1h	1h	0	1h	0h	0h			0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_PFC_FLOW_ACT								RESERVED	EXT_RX_FLOW_EN	EXT_TX_FLOW_EN	EXT_GIG	EXT_FULLDUPLEX	RESERVED	RX_FLOW_ACT	TX_FLOW_ACT
R								NONE	R	R	R	R	NONE	R	R
0h								0	0h	0h	0h	0h	0	0h	0h

Access Types Legend

Table 4-2252. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IDLE	R	1h	cpxmac_sl IDLE
30	E_IDLE	R	1h	Express cpxmac_sl IDLE
29	RESERVED	NONE		Reserved
28	MAC_TX_IDLE	R	1h	Prempt and Express cpxmac_sl Transmit IDLE
27	TORF	R	0h	Top of receive FIFO flow control trigger occurred. This bit is write one to clear.
26:24	TORF_PRI	R	0h	The lowest priority that caused top of receive FIFO flow control trigger since the last write to clear. This field is write 0x7 to clear.
23:16	TX_PFC_FLOW_ACT	R	0h	Transmit Priority Based Flow Control Active (priority 7 down to 0)
15:8	RX_PFC_FLOW_ACT	R	0h	Receive Priority Based Flow Control Active (priority 7 down to 0)
7	RESERVED	NONE		Reserved
6	EXT_RX_FLOW_EN	R	0h	External Transmit Flow Control Enable
5	EXT_TX_FLOW_EN	R	0h	External Receive Flow Control Enable
4	EXT_GIG	R	0h	External GIG mode
3	EXT_FULLDUPLEX	R	0h	External Fullduplex
2	RESERVED	NONE		Reserved
1	RX_FLOW_ACT	R	0h	Receive Flow Control Active
0	TX_FLOW_ACT	R	0h	Transmit Flow Control Active

4.18.211 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_SOFT_RESET_REG Registers

4.18.211.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_SOFT_RESET_REG Register (Offset = 23338h) [reset = 0h]

Short Description: pn_mac_soft_reset_reg

Long Description: Enet Port N Mac Soft Reset

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Table 4-2253. Instance Table

Instance Name	Physical Address
CPSW	5282 3338h

Figure 4-1039. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_SOFT_RESET_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															SOFT_RESET
NONE															R/W
0															0h

Access Types Legend

Table 4-2254. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_SOFT_RESET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	SOFT_RESET	R/W	0h	Software reset

4.18.212 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_BOFFTEST_REG Registers

4.18.212.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_BOFFTEST_REG Register (Offset = 2333Ch) [reset = 0h]

Short Description: pn_mac_bofftest_reg

Long Description: Enet Port N Mac Backoff Test

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Table 4-2255. Instance Table

Instance Name	Physical Address
CPSW	5282 333Ch

Figure 4-1040. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_BOFFTEST_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	PACEVAL					RNDNUM									
NONE	R/W					R/W									
0	0h					0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COLL_COUNT				RESERVED		TX_BACKOFF									
R				NONE		R									
0h				0		0h									

Access Types Legend

Table 4-2256. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_BOFFTEST_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE		Reserved
30:26	PACEVAL	R/W	0h	Pacing Register Current Value
25:16	RNDNUM	R/W	0h	Backoff Random Number Generator
15:12	COLL_COUNT	R	0h	Collision Count
11:10	RESERVED	NONE		Reserved
9:0	TX_BACKOFF	R	0h	Backoff Count

4.18.213 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_RX_PAUSETIMER_REG Registers

4.18.213.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_RX_PAUSETIMER_REG Register (Offset = 23340h) [reset = 0h]

Short Description: pn_mac_rx_pausetimer_reg

Long Description: Enet Port N 802.3 Receive Pause Timer

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Table 4-2257. Instance Table

Instance Name	Physical Address
CPSW	5282 3340h

Figure 4-1041. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_RX_PAUSETIMER_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_PAUSETIMER															
R/W															
0h															

Access Types Legend

Table 4-2258. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_RX_PAUSETIMER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	RX_PAUSETIMER	R/W	0h	RX Pause Timer Value

4.18.214 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_RXN_PAUSETIMER_REG_N Registers

4.18.214.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_RXN_PAUSETIMER_REG_N Register (Offset = 23350h) [reset = 0h]

Short Description: pn_mac_rxn_pausetimer_reg

Long Description: Enet Port N PFC Priority P Rx Pause Timer

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Offset = 23350h + (j * 4h); where j = 0h to 7h

Table 4-2259. Instance Table

Instance Name	Physical Address
CPSW	5282 3350h

Figure 4-1042. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_RXN_PAUSETIMER_REG_N Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_PAUSETIMER															
R/W															
0h															

Access Types Legend

Table 4-2260. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_RXN_PAUSETIMER_REG_N Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	RX_PAUSETIMER	R/W	0h	RX Pause Timer Value

4.18.215 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_TX_PAUSETIMER_REG Registers

4.18.215.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_TX_PAUSETIMER_REG Register (Offset = 23370h) [reset = 0h]

Short Description: pn_mac_tx_pausetimer_reg

Long Description: Enet Port N 802.3 Tx Pause Timer

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Table 4-2261. Instance Table

Instance Name	Physical Address
CPSW	5282 3370h

Figure 4-1043. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_TX_PAUSETIMER_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_PAUSETIMER															
R/W															
0h															

Access Types Legend

Table 4-2262. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_TX_PAUSETIMER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	TX_PAUSETIMER	R/W	0h	TX Pause Timer Value

4.18.216 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_TXN_PAUSETIMER_REG_N Registers

4.18.216.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_TXN_PAUSETIMER_REG_N Register (Offset = 23380h) [reset = 0h]

Short Description: pn_mac_txn_pausetimer_reg

Long Description: Enet Port N PFC Priority P Tx Pause Timer

Return to Summary Table

Offset = 23380h + (j * 4h); where j = 0h to 7h

Table 4-2263. Instance Table

Instance Name	Physical Address
CPSW	5282 3380h

Figure 4-1044. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_TXN_PAUSETIMER_REG_N Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_PAUSETIMER															
R/W															
0h															

Access Types Legend

Table 4-2264. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_TXN_PAUSETIMER_REG_N Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	TX_PAUSETIMER	R/W	0h	TX Pause Timer Value

4.18.217 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_EMCONTROL_REG Registers

4.18.217.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_EMCONTROL_REG Register (Offset = 233A0h) [reset = 0h]

Short Description: pn_mac_emcontrol_reg

Long Description: Enet Port N Emulation Control

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Table 4-2265. Instance Table

Instance Name	Physical Address
CPSW	5282 33A0h

Figure 4-1045. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_EMCONTROL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														SOFT	FREE
NONE														R/W	R/W
0														0h	0h

Access Types Legend

Table 4-2266. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_EMCONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1	SOFT	R/W	0h	Emulation Soft Bit
0	FREE	R/W	0h	Emulation Free Bit

4.18.218 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_TX_GAP_REG Registers

4.18.218.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_TX_GAP_REG Register (Offset = 233A4h) [reset = ch]

Short Description: pn_mac_tx_gap_reg

Long Description: Enet Port N Tx Inter Packet Gap

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Table 4-2267. Instance Table

Instance Name	Physical Address
CPSW	5282 33A4h

Figure 4-1046. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_TX_GAP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
6e															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_GAP															
R/W															
ch															

Access Types Legend

Table 4-2268. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_TX_GAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	TX_GAP	R/W	Ch	Transmit Inter-Packet Gap

4.18.219 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_PORT_CONFIG Registers

4.18.219.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_PORT_CONFIG Register (Offset = 233A8h) [reset = 2h]

Short Description: Port Configuration

Long Description: Enet Port N Port Configuration

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Table 4-2269. Instance Table

Instance Name	Physical Address
CPSW	5282 33A8h

Figure 4-1047. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_PORT_CONFIG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
1															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						IET	XGMII	INTERVLAN_ROUTES							
NONE						R	R	R							
1						0h	0h	2h							

Access Types Legend

Table 4-2270. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_MAC_PORT_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9	IET	R	0h	IET support
8	XGMII	R	0h	No XGMII support
7:0	INTERVLAN_ROUTES	R	2h	The number of InterVLAN routes

4.18.220 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_INTERVLAN_OPX_POINTER_REG Registers

4.18.220.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_INTERVLAN_OPX_POINTER_REG Register (Offset = 233ACh) [reset = 0h]

Short Description: pn_opx_pointer_reg

Long Description: Enet Port N Tx Egress InterVLAN Operation Pointer

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Table 4-2271. Instance Table

Instance Name	Physical Address
CPSW	5282 33ACh

Figure 4-1048. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_INTERVLAN_OPX_POINTER_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														POINTER	
NONE														R/W	
0														0h	

Access Types Legend

Table 4-2272. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_INTERVLAN_OPX_POINTER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1:0	POINTER	R/W	0h	InterVLAN location pointer: This field points to the InterVLAN location that will be read/written by accesses to Enet_Pn_InterVLANx_A/B.

4.18.221 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_INTERVLAN_OPX_A_REG Registers

4.18.221.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_INTERVLAN_OPX_A_REG Register (Offset = 233B0h) [reset = 0h]

Short Description: pn_opx_a_reg

Long Description: Enet Port N Tx Egress InterVLAN A

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Table 4-2273. Instance Table

Instance Name	Physical Address
CPSW	5282 33B0h

Figure 4-1049. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_INTERVLAN_OPX_A_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DA_23_16								DA_31_24							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DA_39_32								DA_47_40							
R/W								R/W							
0h								0h							

Access Types Legend

Table 4-2274. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_INTERVLAN_OPX_A_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	DA_23_16	R/W	0h	Destination Address bits 23:16
23:16	DA_31_24	R/W	0h	Destination Address bits 31:24
15:8	DA_39_32	R/W	0h	Destination Address bits 39:32
7:0	DA_47_40	R/W	0h	Destination Address bits 47:40

4.18.222 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_INTERVLAN_OPX_B_REG Registers

4.18.222.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_INTERVLAN_OPX_B_REG Register (Offset = 233B4h) [reset = 0h]

Short Description: pn_opx_b_reg

Long Description: Enet Port N Tx Egress InterVLAN B

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Table 4-2275. Instance Table

Instance Name	Physical Address
CPSW	5282 33B4h

Figure 4-1050. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_INTERVLAN_OPX_B_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SA_39_32								SA_47_40							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DA_7_0								DA_15_8							
R/W								R/W							
0h								0h							

Access Types Legend

Table 4-2276. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_INTERVLAN_OPX_B_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SA_39_32	R/W	0h	Source Address bits 39:32
23:16	SA_47_40	R/W	0h	Source Address bits 47:40
15:8	DA_7_0	R/W	0h	Destination Address bits 7:0
7:0	DA_15_8	R/W	0h	Destination Address bits 15:8

4.18.223 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_INTERVLAN_OPX_C_REG Registers

4.18.223.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_INTERVLAN_OPX_C_REG Register (Offset = 233B8h) [reset = 0h]

Short Description: pn_opx_c_reg

Long Description: Enet Port N Tx Egress InterVLAN C

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Table 4-2277. Instance Table

Instance Name	Physical Address
CPSW	5282 33B8h

Figure 4-1051. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_INTERVLAN_OPX_C_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SA_7_0								SA_15_8							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SA_23_16								SA_31_24							
R/W								R/W							
0h								0h							

Access Types Legend

Table 4-2278. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_INTERVLAN_OPX_C_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SA_7_0	R/W	0h	Source Address bits 7:0
23:16	SA_15_8	R/W	0h	Source Address bits 15:8
15:8	SA_23_16	R/W	0h	Source Address bits 23:16
7:0	SA_31_24	R/W	0h	Source Address bits 31:24

4.18.224 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_INTERVLAN_OPX_D_REG Registers

4.18.224.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_INTERVLAN_OPX_D_REG Register (Offset = 233BCh) [reset = 0h]

Short Description: pn_opx_d_reg

Long Description: Enet Port N Tx Egress InterVLAN D

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Table 4-2279. Instance Table

Instance Name	Physical Address
CPSW	5282 33BCh

Figure 4-1052. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_INTERVLAN_OPX_D_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DECREMENT_TTL	DEST_FORCE_UNTAGGED_EGRESS	REPLACE_DA_SA	REPLACE_VID	VID											
R/W	R/W	R/W	R/W	R/W											
0h	0h	0h	0h	0h											

Access Types Legend

Table 4-2280. CPSW_NC_CPSW_NC_CPSW_NC_ETH_MAC_1_PN_INTERVLAN_OPX_D_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15	DECREMENT_TTL	R/W	0h	Decrement Time To Live: When set, the Time To Live (TTL) field in the header is decremented.
14	DEST_FORCE_UNTAGGED_EGRESS	R/W	0h	Destination VLAN Force Untagged Egress: When set, this bit indicates that the VLAN should be removed on egress for the routed packet.
13	REPLACE_DA_SA	R/W	0h	Replace Destination Address and Source Address: When set this bit indicates that the routed packet destination address should be replaced by da[47:0] and the source address should be replaced by sa[47:0].
12	REPLACE_VID	R/W	0h	Replace VLAN ID: When set this bit indicates that the VLAN ID should be replaced for the routed packet.
11:0	VID	R/W	0h	VLAN ID

4.18.225 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_EST_FETCH_LOC_N Registers

4.18.225.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_EST_FETCH_LOC_N Register (Offset = 32000h) [reset = 0h]

Short Description: Revision Register

Long Description: The Revision Register contains the ID and revision information.

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Offset = 32000h + (j * 4h); where j = 0h to FFh

Table 4-2281. Instance Table

Instance Name	Physical Address
CPSW	5283 2000h

Figure 4-1053. CPSW_NC_CPSW_NC_CPSW_NC_EST_FETCH_LOC_N Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										LOC					
NONE										R/W					
0										0h					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOC															
R/W															
0h															

Access Types Legend

Table 4-2282. CPSW_NC_CPSW_NC_CPSW_NC_EST_FETCH_LOC_N Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE		Reserved
21:0	LOC	R/W	0h	RAM Location

4.18.226 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_FH_IDVER_REG Registers

4.18.226.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_FH_IDVER_REG Register (Offset = 34000h) [reset = 18010ah]

Short Description: CPDMA Transmit IDVER

Long Description: CPDMA Transmit IDVER

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Table 4-2283. Instance Table

Instance Name	Physical Address
CPSW	5283 4000h

Figure 4-1054. CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_FH_IDVER_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FH_IDVER															
R															
18010ah															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FH_IDVER															
R															
18010ah															

Access Types Legend

Table 4-2284. CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_FH_IDVER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FH_IDVER	R	18010Ah	CPDMA Transmit IDVER

4.18.227 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_FH_CONTROL_REG Registers

4.18.227.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_FH_CONTROL_REG Register (Offset = 34004h) [reset = 0h]

Short Description: CPDMA Transmit Control Register

Long Description: CPDMA Transmit Control Register

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Table 4-2285. Instance Table

Instance Name	Physical Address
CPSW	5283 4004h

Figure 4-1055. CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_FH_CONTROL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															FH_EN
NONE															R/W
0															0h

Access Types Legend

Table 4-2286. CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_FH_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	FH_EN	R/W	0h	CPDMA Transmit DMA Enable

4.18.228 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_FH_TEARDOWN_REG Registers

4.18.228.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_FH_TEARDOWN_REG Register (Offset = 34008h) [reset = 0h]

Short Description: CPDMA Transmit Teardown Register

Long Description: CPDMA Transmit Teardown Register

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Table 4-2287. Instance Table

Instance Name	Physical Address
CPSW	5283 4008h

Figure 4-1056. CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_FH_TEARDOWN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FH_TDN_RDY	RESERVED														
R/W	NONE														
0h	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													FH_TDN_CH		
NONE													R/W		
0													0h		

Access Types Legend

Table 4-2288. CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_FH_TEARDOWN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	FH_TDN_RDY	R/W	0h	CPDMA Transmit Teardown Ready
30:3	RESERVED	NONE		Reserved
2:0	FH_TDN_CH	R/W	0h	CPDMA Transmit Teardown Channel

4.18.229 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_TH_IDVER_REG Registers

4.18.229.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_TH_IDVER_REG Register (Offset = 34010h) [reset = 18010ah]

Short Description: CPDMA Receive IDVER

Long Description: CPDMA Receive IDVER

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Table 4-2289. Instance Table

Instance Name	Physical Address
CPSW	5283 4010h

Figure 4-1057. CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_TH_IDVER_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TH_IDVER															
R															
18010ah															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TH_IDVER															
R															
18010ah															

Access Types Legend

Table 4-2290. CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_TH_IDVER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TH_IDVER	R	18010Ah	CPDMA Receive IDVER

4.18.230 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_TH_CONTROL_REG Registers

4.18.230.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_TH_CONTROL_REG Register (Offset = 34014h) [reset = 0h]

Short Description: CPDMA Receive Control Register

Long Description: CPDMA Receive Control Register

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Table 4-2291. Instance Table

Instance Name	Physical Address
CPSW	5283 4014h

Figure 4-1058. CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_TH_CONTROL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															TH_EN
NONE															R/W
0															0h

Access Types Legend

Table 4-2292. CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_TH_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	TH_EN	R/W	0h	CPDMA Receive DMA Enable

4.18.231 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_TH_TEARDOWN_REG Registers

4.18.231.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_TH_TEARDOWN_REG Register (Offset = 34018h) [reset = 0h]

Short Description: CPDMA Receive Teardown Register

Long Description: CPDMA Receive Teardown Register

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Table 4-2293. Instance Table

Instance Name	Physical Address
CPSW	5283 4018h

Figure 4-1059. CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_TH_TEARDOWN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TH_TDN_RDY	RESERVED														
R/W	NONE														
0h	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													TH_TDN_CH		
NONE													R/W		
0													0h		

Access Types Legend

Table 4-2294. CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_TH_TEARDOWN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TH_TDN_RDY	R/W	0h	CPDMA Receive Teardown Ready
30:3	RESERVED	NONE		Reserved
2:0	TH_TDN_CH	R/W	0h	CPDMA Receive Teardown Channel

4.18.232 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_SOFT_RESET_REG Registers

4.18.232.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_SOFT_RESET_REG Register (Offset = 3401Ch) [reset = 0h]

Short Description: CPDMA Soft Reset Register

Long Description: CPDMA Soft Reset Register

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Table 4-2295. Instance Table

Instance Name	Physical Address
CPSW	5283 401Ch

Figure 4-1060. CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_SOFT_RESET_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															SOFT_RESET
NONE															R/W
0															0h

Access Types Legend

Table 4-2296. CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_SOFT_RESET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	SOFT_RESET	R/W	0h	CPDMA and CPSW Soft Reset Enable

4.18.233 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_CONTROL_REG Registers

4.18.233.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_CONTROL_REG Register (Offset = 34020h) [reset = 0h]

Short Description: CPDMA Control Register

Long Description: CPDMA Control Register

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Table 4-2297. Instance Table

Instance Name	Physical Address
CPSW	5283 4020h

Figure 4-1061. CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_CONTROL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TH_CH_OVERRIDE	TH_TS_ENCAP	TH_VLAN_ENCAP	TH_CEF	CMD_IDLE	TH_OFFLEN_BLOCK	TH_OWNERSHIP	FH_PTYPE
NONE								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-2298. CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7	TH_CH_OVERRIDE	R/W	0h	CPDMA Channel Thread Override Enable
6	TH_TS_ENCAP	R/W	0h	CPDMA Receive TimeStamp Encapsulated
5	TH_VLAN_ENCAP	R/W	0h	CPDMA Receive VLAN Encapsulated
4	TH_CEF	R/W	0h	CPDMA Receive Copy Error Frames
3	CMD_IDLE	R/W	0h	CPDMA Command Idle
2	TH_OFFLEN_BLOCK	R/W	0h	CPDMA Receive Offset/Length Word Write Block
1	TH_OWNERSHIP	R/W	0h	CPDMA Receive Ownership Write Bit Value
0	FH_PTYPE	R/W	0h	CPDMA Transmit Queue Priority Type

4.18.234 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_STATUS_REG Registers

4.18.234.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_STATUS_REG Register (Offset = 34024h) [reset = 80000000h]

Short Description: CPDMA Status Register

Long Description: CPDMA Status Register

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Table 4-2299. Instance Table

Instance Name	Physical Address
CPSW	5283 4024h

Figure 4-1062. CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IDLE	RESERVED							FH_HOST_ERROR_CODE				RESERVED	FH_ERR_CH		
R	NONE							R				NONE	R		
1h	0							0h				0	0h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TH_HOST_ERROR_CODE				RESERVED	TH_ERR_CH			RESERVED							
R				NONE	R			NONE							
0h				0	0h			f4240							

Access Types Legend

Table 4-2300. CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IDLE	R	1h	CPDMA Transmit Host Error Code
30:24	RESERVED	NONE		Reserved
23:20	FH_HOST_ERROR_CODE	R	0h	CPDMA Transmit Host Error Code
19	RESERVED	NONE		Reserved
18:16	FH_ERR_CH	R	0h	CPDMA Transmit Error Channel Number
15:12	TH_HOST_ERROR_CODE	R	0h	CPDMA Receive Host Error Code
11	RESERVED	NONE		Reserved
10:8	TH_ERR_CH	R	0h	CPDMA Receive Error Channel Number
7:0	RESERVED	NONE		Reserved

4.18.235 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_TH_BUFFER_OFFSET_REG Registers

4.18.235.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_TH_BUFFER_OFFSET_REG Register (Offset = 34028h) [reset = 0h]

Short Description: CPDMA Receive Buffer Offset Register

Long Description: CPDMA Receive Buffer Offset Register

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Table 4-2301. Instance Table

Instance Name	Physical Address
CPSW	5283 4028h

Figure 4-1063. CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_TH_BUFFER_OFFSET_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					TH_BUFFER_OFFSET										
NONE					R/W										
0					0h										

Access Types Legend

Table 4-2302. CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_TH_BUFFER_OFFSET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE		Reserved
10:0	TH_BUFFER_OFFSET	R/W	0h	CPDMA Receive Buffer Offset Register

4.18.236 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_EMULATION_CONTROL_REG Registers

4.18.236.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_EMULATION_CONTROL_REG Register (Offset = 3402Ch) [reset = 0h]

Short Description: CPDMA Receive Buffer Offset Register

Long Description: CPDMA Receive Buffer Offset Register

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Table 4-2303. Instance Table

Instance Name	Physical Address
CPSW	5283 402Ch

Figure 4-1064. CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_EMULATION_CONTROL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														FREE	SOFT
NONE														R/W	R/W
0														0h	0h

Access Types Legend

Table 4-2304. CPSW_NC_CPSW_NC_CPSW_CPDMA_REGS_CPDMA_EMULATION_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1	FREE	R/W	0h	CPDMA Receive Buffer Offset Register
0	SOFT	R/W	0h	CPDMA Receive Buffer Offset Register

4.18.237 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_FH_INTSTAT_RAW_REG Registers

4.18.237.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_FH_INTSTAT_RAW_REG Register (Offset = 34080h) [reset = 0h]

Short Description: CPDMA FHost Interrupt Status RAW

Long Description: CPDMA FHost Interrupt Status RAW

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Table 4-2305. Instance Table

Instance Name	Physical Address
CPSW	5283 4080h

Figure 4-1065. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_FH_INTSTAT_RAW_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FH7_PEND_RAW	FH6_PEND_RAW	FH5_PEND_RAW	FH4_PEND_RAW	FH3_PEND_RAW	FH2_PEND_RAW	FH1_PEND_RAW	FH0_PEND_RAW
NONE								R	R	R	R	R	R	R	R
0								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-2306. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_FH_INTSTAT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7	FH7_PEND_RAW	R	0h	CPDMA FHost Channel 7 Interrupt Pending RAW
6	FH6_PEND_RAW	R	0h	CPDMA FHost Channel 6 Interrupt Pending RAW
5	FH5_PEND_RAW	R	0h	CPDMA FHost Channel 5 Interrupt Pending RAW
4	FH4_PEND_RAW	R	0h	CPDMA FHost Channel 4 Interrupt Pending RAW
3	FH3_PEND_RAW	R	0h	CPDMA FHost Channel 3 Interrupt Pending RAW
2	FH2_PEND_RAW	R	0h	CPDMA FHost Channel 2 Interrupt Pending RAW
1	FH1_PEND_RAW	R	0h	CPDMA FHost Channel 1 Interrupt Pending RAW
0	FH0_PEND_RAW	R	0h	CPDMA FHost Channel 0 Interrupt Pending RAW

4.18.238 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_FH_INTSTAT_MASKED_REG Registers

4.18.238.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_FH_INTSTAT_MASKED_REG Register (Offset = 34084h) [reset = 0h]

Short Description: CPDMA FHost Interrupt Status MASKED

Long Description: CPDMA FHost Interrupt Status MASKED

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Table 4-2307. Instance Table

Instance Name	Physical Address
CPSW	5283 4084h

Figure 4-1066. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_FH_INTSTAT_MASKED_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FH7_PEND_MASKED	FH6_PEND_MASKED	FH5_PEND_MASKED	FH4_PEND_MASKED	FH3_PEND_MASKED	FH2_PEND_MASKED	FH1_PEND_MASKED	FH0_PEND_MASKED
NONE								R	R	R	R	R	R	R	R
0								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-2308. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_FH_INTSTAT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7	FH7_PEND_MASKED	R	0h	CPDMA FHost Channel 7 Interrupt Pending MASKED
6	FH6_PEND_MASKED	R	0h	CPDMA FHost Channel 6 Interrupt Pending MASKED
5	FH5_PEND_MASKED	R	0h	CPDMA FHost Channel 5 Interrupt Pending MASKED
4	FH4_PEND_MASKED	R	0h	CPDMA FHost Channel 4 Interrupt Pending MASKED
3	FH3_PEND_MASKED	R	0h	CPDMA FHost Channel 3 Interrupt Pending MASKED
2	FH2_PEND_MASKED	R	0h	CPDMA FHost Channel 2 Interrupt Pending MASKED
1	FH1_PEND_MASKED	R	0h	CPDMA FHost Channel 1 Interrupt Pending MASKED
0	FH0_PEND_MASKED	R	0h	CPDMA FHost Channel 0 Interrupt Pending MASKED

4.18.239 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_FH_INTMASK_SET_REG Registers

4.18.239.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_FH_INTMASK_SET_REG Register (Offset = 34088h) [reset = 0h]

Short Description: CPDMA FHost Interrupt Masked Set

Long Description: CPDMA FHost Interrupt Masked SET

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Table 4-2309. Instance Table

Instance Name	Physical Address
CPSW	5283 4088h

Figure 4-1067. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_FH_INTMASK_SET_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FH7_PEND_MASKED_SET	FH6_PEND_MASKED_SET	FH5_PEND_MASKED_SET	FH4_PEND_MASKED_SET	FH3_PEND_MASKED_SET	FH2_PEND_MASKED_SET	FH1_PEND_MASKED_SET	FH0_PEND_MASKED_SET
NONE								R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-2310. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_FH_INTMASK_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7	FH7_PEND_MASKED_SET	R/W1TS	0h	CPDMA FHost Channel 7 Interrupt Pending MASKED Set
6	FH6_PEND_MASKED_SET	R/W1TS	0h	CPDMA FHost Channel 6 Interrupt Pending MASKED Set
5	FH5_PEND_MASKED_SET	R/W1TS	0h	CPDMA FHost Channel 5 Interrupt Pending MASKED Set
4	FH4_PEND_MASKED_SET	R/W1TS	0h	CPDMA FHost Channel 4 Interrupt Pending MASKED Set
3	FH3_PEND_MASKED_SET	R/W1TS	0h	CPDMA FHost Channel 3 Interrupt Pending MASKED Set
2	FH2_PEND_MASKED_SET	R/W1TS	0h	CPDMA FHost Channel 2 Interrupt Pending MASKED Set
1	FH1_PEND_MASKED_SET	R/W1TS	0h	CPDMA FHost Channel 1 Interrupt Pending MASKED Set
0	FH0_PEND_MASKED_SET	R/W1TS	0h	CPDMA FHost Channel 0 Interrupt Pending MASKED Set

4.18.240 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_FH_INTMASK_CLEAR_REG Registers

4.18.240.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_FH_INTMASK_CLEAR_REG Register (Offset = 3408Ch) [reset = 0h]

Short Description: CPDMA FHost Interrupt Masked Clr

Long Description: CPDMA FHost Interrupt Masked CLR

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Table 4-2311. Instance Table

Instance Name	Physical Address
CPSW	5283 408Ch

Figure 4-1068. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_FH_INTMASK_CLEAR_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FH7_PEND_MASKED_CLR	FH6_PEND_MASKED_CLR	FH5_PEND_MASKED_CLR	FH4_PEND_MASKED_CLR	FH3_PEND_MASKED_CLR	FH2_PEND_MASKED_CLR	FH1_PEND_MASKED_CLR	FH0_PEND_MASKED_CLR
NONE								R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-2312. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_FH_INTMASK_CLEAR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7	FH7_PEND_MASKED_CLR	R/W1TC	0h	CPDMA FHost Channel 7 Interrupt Pending MASKED Clr
6	FH6_PEND_MASKED_CLR	R/W1TC	0h	CPDMA FHost Channel 6 Interrupt Pending MASKED Clr
5	FH5_PEND_MASKED_CLR	R/W1TC	0h	CPDMA FHost Channel 5 Interrupt Pending MASKED Clr
4	FH4_PEND_MASKED_CLR	R/W1TC	0h	CPDMA FHost Channel 4 Interrupt Pending MASKED Clr
3	FH3_PEND_MASKED_CLR	R/W1TC	0h	CPDMA FHost Channel 3 Interrupt Pending MASKED Clr
2	FH2_PEND_MASKED_CLR	R/W1TC	0h	CPDMA FHost Channel 2 Interrupt Pending MASKED Clr
1	FH1_PEND_MASKED_CLR	R/W1TC	0h	CPDMA FHost Channel 1 Interrupt Pending MASKED Clr
0	FH0_PEND_MASKED_CLR	R/W1TC	0h	CPDMA FHost Channel 0 Interrupt Pending MASKED Clr

4.18.241 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_IN_VECTOR_REG Registers

4.18.241.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_IN_VECTOR_REG Register (Offset = 34090h) [reset = 0h]

Short Description: CPDMA DMA IN Vector

Long Description: CPDMA DMA IN Vector

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Table 4-2313. Instance Table

Instance Name	Physical Address
CPSW	5283 4090h

Figure 4-1069. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_IN_VECTOR_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DMA_IN_VECTOR															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA_IN_VECTOR															
R															
0h															

Access Types Legend

Table 4-2314. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_IN_VECTOR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DMA_IN_VECTOR	R	0h	CPDMA DMA IN Vector

4.18.242 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_EOI_VECTOR_REG Registers

4.18.242.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_EOI_VECTOR_REG Register (Offset = 34094h) [reset = 0h]

Short Description: CPDMA DMA EOI Vector

Long Description: CPDMA DMA EOI Vector

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Table 4-2315. Instance Table

Instance Name	Physical Address
CPSW	5283 4094h

Figure 4-1070. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_EOI_VECTOR_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DMA_EOI_VECTOR				
NONE											R/W				
0											0h				

Access Types Legend

Table 4-2316. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_EOI_VECTOR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	DMA_EOI_VECTOR	R/W	0h	CPDMA DMA EOI Vector

4.18.243 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH_INTSTAT_RAW_REG Registers

4.18.243.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH_INTSTAT_RAW_REG Register (Offset = 340A0h) [reset = 0h]

Short Description: CPDMA receive Interrupt Status RAW

Long Description: CPDMA Receive Interrupt Status RAW

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Table 4-2317. Instance Table

Instance Name	Physical Address
CPSW	5283 40A0h

Figure 4-1071. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH_INTSTAT_RAW_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TH7_THRESH_PEND_RAW	TH6_THRESH_PEND_RAW	TH5_THRESH_PEND_RAW	TH4_THRESH_PEND_RAW	TH3_THRESH_PEND_RAW	TH2_THRESH_PEND_RAW	TH1_THRESH_PEND_RAW	TH0_THRESH_PEND_RAW	TH7_PEND_RAW	TH6_PEND_RAW	TH5_PEND_RAW	TH4_PEND_RAW	TH3_PEND_RAW	TH2_PEND_RAW	TH1_PEND_RAW	TH0_PEND_RAW
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-2318. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH_INTSTAT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15	TH7_THRESH_PEND_RAW	R	0h	CPDMA Receive Channel 7 Threshold Interrupt Pending RAW
14	TH6_THRESH_PEND_RAW	R	0h	CPDMA Receive Channel 6 Threshold Interrupt Pending RAW
13	TH5_THRESH_PEND_RAW	R	0h	CPDMA Receive Channel 5 Threshold Interrupt Pending RAW
12	TH4_THRESH_PEND_RAW	R	0h	CPDMA Receive Channel 4 Threshold Interrupt Pending RAW
11	TH3_THRESH_PEND_RAW	R	0h	CPDMA Receive Channel 3 Threshold Interrupt Pending RAW
10	TH2_THRESH_PEND_RAW	R	0h	CPDMA Receive Channel 2 Threshold Interrupt Pending RAW
9	TH1_THRESH_PEND_RAW	R	0h	CPDMA Receive Channel 1 Threshold Interrupt Pending RAW
8	TH0_THRESH_PEND_RAW	R	0h	CPDMA Receive Channel 0 Threshold Interrupt Pending RAW
7	TH7_PEND_RAW	R	0h	CPDMA Receive Channel 7 Interrupt Pending RAW
6	TH6_PEND_RAW	R	0h	CPDMA Receive Channel 6 Interrupt Pending RAW
5	TH5_PEND_RAW	R	0h	CPDMA Receive Channel 5 Interrupt Pending RAW

Table 4-2318. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH_INTSTAT_RAW_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	TH4_PEND_RAW	R	0h	CPDMA Receive Channel 4 Interrupt Pending RAW
3	TH3_PEND_RAW	R	0h	CPDMA Receive Channel 3 Interrupt Pending RAW
2	TH2_PEND_RAW	R	0h	CPDMA Receive Channel 2 Interrupt Pending RAW
1	TH1_PEND_RAW	R	0h	CPDMA Receive Channel 1 Interrupt Pending RAW
0	TH0_PEND_RAW	R	0h	CPDMA Receive Channel 0 Interrupt Pending RAW

4.18.244 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH_INTSTAT_MASKED_REG Registers

4.18.244.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH_INTSTAT_MASKED_REG Register (Offset = 340A4h) [reset = 0h]

Short Description: CPDMA receive Interrupt Status MASKED

Long Description: CPDMA Receive Interrupt Status MASKED

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Table 4-2319. Instance Table

Instance Name	Physical Address
CPSW	5283 40A4h

Figure 4-1072. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH_INTSTAT_MASKED_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TH7_THRESH_PEND_MASKED	TH6_THRESH_PEND_MASKED	TH5_THRESH_PEND_MASKED	TH4_THRESH_PEND_MASKED	TH3_THRESH_PEND_MASKED	TH2_THRESH_PEND_MASKED	TH1_THRESH_PEND_MASKED	TH0_THRESH_PEND_MASKED	TH7_PEND_MASKED	TH6_PEND_MASKED	TH5_PEND_MASKED	TH4_PEND_MASKED	TH3_PEND_MASKED	TH2_PEND_MASKED	TH1_PEND_MASKED	TH0_PEND_MASKED
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-2320. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH_INTSTAT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15	TH7_THRESH_PEND_MASKED	R	0h	CPDMA Receive Channel 7 Threshold Interrupt Pending MASKED
14	TH6_THRESH_PEND_MASKED	R	0h	CPDMA Receive Channel 6 Threshold Interrupt Pending MASKED
13	TH5_THRESH_PEND_MASKED	R	0h	CPDMA Receive Channel 5 Threshold Interrupt Pending MASKED
12	TH4_THRESH_PEND_MASKED	R	0h	CPDMA Receive Channel 4 Threshold Interrupt Pending MASKED
11	TH3_THRESH_PEND_MASKED	R	0h	CPDMA Receive Channel 3 Threshold Interrupt Pending MASKED
10	TH2_THRESH_PEND_MASKED	R	0h	CPDMA Receive Channel 2 Threshold Interrupt Pending MASKED
9	TH1_THRESH_PEND_MASKED	R	0h	CPDMA Receive Channel 1 Threshold Interrupt Pending MASKED
8	TH0_THRESH_PEND_MASKED	R	0h	CPDMA Receive Channel 0 Threshold Interrupt Pending MASKED
7	TH7_PEND_MASKED	R	0h	CPDMA Receive Channel 7 Interrupt Pending MASKED
6	TH6_PEND_MASKED	R	0h	CPDMA Receive Channel 6 Interrupt Pending MASKED

Table 4-2320. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH_INTSTAT_MASKED_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	TH5_PEND_MASKED	R	0h	CPDMA Receive Channel 5 Interrupt Pending MASKED
4	TH4_PEND_MASKED	R	0h	CPDMA Receive Channel 4 Interrupt Pending MASKED
3	TH3_PEND_MASKED	R	0h	CPDMA Receive Channel 3 Interrupt Pending MASKED
2	TH2_PEND_MASKED	R	0h	CPDMA Receive Channel 2 Interrupt Pending MASKED
1	TH1_PEND_MASKED	R	0h	CPDMA Receive Channel 1 Interrupt Pending MASKED
0	TH0_PEND_MASKED	R	0h	CPDMA Receive Channel 0 Interrupt Pending MASKED

4.18.245 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH_INTMASK_SET_REG Registers

4.18.245.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH_INTMASK_SET_REG Register (Offset = 340A8h) [reset = 0h]

Short Description: CPDMA receive Interrupt Status SET

Long Description: CPDMA THost Interrupt Masked SET

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Table 4-2321. Instance Table

Instance Name	Physical Address
CPSW	5283 40A8h

Figure 4-1073. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH_INTMASK_SET_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TH7_THRESH_PEND_MASKED_SET	TH6_THRESH_PEND_MASKED_SET	TH5_THRESH_PEND_MASKED_SET	TH4_THRESH_PEND_MASKED_SET	TH3_THRESH_PEND_MASKED_SET	TH2_THRESH_PEND_MASKED_SET	TH1_THRESH_PEND_MASKED_SET	TH0_THRESH_PEND_MASKED_SET	TH7_PEND_MASKED_SET	TH6_PEND_MASKED_SET	TH5_PEND_MASKED_SET	TH4_PEND_MASKED_SET	TH3_PEND_MASKED_SET	TH2_PEND_MASKED_SET	TH1_PEND_MASKED_SET	TH0_PEND_MASKED_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-2322. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH_INTMASK_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15	TH7_THRESH_PEND_MASKED_SET	R/W1TS	0h	CPDMA THost Channel 7 Threshold Interrupt Pending SET
14	TH6_THRESH_PEND_MASKED_SET	R/W1TS	0h	CPDMA THost Channel 6 Threshold Interrupt Pending SET
13	TH5_THRESH_PEND_MASKED_SET	R/W1TS	0h	CPDMA THost Channel 5 Threshold Interrupt Pending SET
12	TH4_THRESH_PEND_MASKED_SET	R/W1TS	0h	CPDMA THost Channel 4 Threshold Interrupt Pending SET
11	TH3_THRESH_PEND_MASKED_SET	R/W1TS	0h	CPDMA THost Channel 3 Threshold Interrupt Pending SET
10	TH2_THRESH_PEND_MASKED_SET	R/W1TS	0h	CPDMA THost Channel 2 Threshold Interrupt Pending SET
9	TH1_THRESH_PEND_MASKED_SET	R/W1TS	0h	CPDMA THost Channel 1 Threshold Interrupt Pending SET
8	TH0_THRESH_PEND_MASKED_SET	R/W1TS	0h	CPDMA THost Channel 0 Threshold Interrupt Pending SET
7	TH7_PEND_MASKED_SET	R/W1TS	0h	CPDMA THost Channel 7 Interrupt Pending SET

Table 4-2322. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH_INTMASK_SET_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	TH6_PEND_MASKED_SET	R/W1TS	0h	CPDMA THost Channel 6 Interrupt Pending SET
5	TH5_PEND_MASKED_SET	R/W1TS	0h	CPDMA THost Channel 5 Interrupt Pending SET
4	TH4_PEND_MASKED_SET	R/W1TS	0h	CPDMA THost Channel 4 Interrupt Pending SET
3	TH3_PEND_MASKED_SET	R/W1TS	0h	CPDMA THost Channel 3 Interrupt Pending SET
2	TH2_PEND_MASKED_SET	R/W1TS	0h	CPDMA THost Channel 2 Interrupt Pending SET
1	TH1_PEND_MASKED_SET	R/W1TS	0h	CPDMA THost Channel 1 Interrupt Pending SET
0	TH0_PEND_MASKED_SET	R/W1TS	0h	CPDMA THost Channel 0 Interrupt Pending SET

4.18.246 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH_INTMASK_CLEAR_REG Registers

4.18.246.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH_INTMASK_CLEAR_REG Register (Offset = 340ACh) [reset = 0h]

Short Description: CPDMA receive Interrupt Status CLR

Long Description: CPDMA THost Interrupt Masked CLR

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Table 4-2323. Instance Table

Instance Name	Physical Address
CPSW	5283 40ACh

Figure 4-1074. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH_INTMASK_CLEAR_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TH7_THRESH_PEND_MASKED_CLR	TH6_THRESH_PEND_MASKED_CLR	TH5_THRESH_PEND_MASKED_CLR	TH4_THRESH_PEND_MASKED_CLR	TH3_THRESH_PEND_MASKED_CLR	TH2_THRESH_PEND_MASKED_CLR	TH1_THRESH_PEND_MASKED_CLR	TH0_THRESH_PEND_MASKED_CLR	TH7_PEND_MASKED_CLR	TH6_PEND_MASKED_CLR	TH5_PEND_MASKED_CLR	TH4_PEND_MASKED_CLR	TH3_PEND_MASKED_CLR	TH2_PEND_MASKED_CLR	TH1_PEND_MASKED_CLR	TH0_PEND_MASKED_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-2324. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH_INTMASK_CLEAR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15	TH7_THRESH_PEND_MASKED_CLR	R/W1TC	0h	CPDMA THost Channel 7 Threshold Interrupt Pending CLR
14	TH6_THRESH_PEND_MASKED_CLR	R/W1TC	0h	CPDMA THost Channel 6 Threshold Interrupt Pending CLR
13	TH5_THRESH_PEND_MASKED_CLR	R/W1TC	0h	CPDMA THost Channel 5 Threshold Interrupt Pending CLR
12	TH4_THRESH_PEND_MASKED_CLR	R/W1TC	0h	CPDMA THost Channel 4 Threshold Interrupt Pending CLR
11	TH3_THRESH_PEND_MASKED_CLR	R/W1TC	0h	CPDMA THost Channel 3 Threshold Interrupt Pending CLR
10	TH2_THRESH_PEND_MASKED_CLR	R/W1TC	0h	CPDMA THost Channel 2 Threshold Interrupt Pending CLR
9	TH1_THRESH_PEND_MASKED_CLR	R/W1TC	0h	CPDMA THost Channel 1 Threshold Interrupt Pending CLR
8	TH0_THRESH_PEND_MASKED_CLR	R/W1TC	0h	CPDMA THost Channel 0 Threshold Interrupt Pending CLR

Table 4-2324. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH_INTMASK_CLEAR_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	TH7_PEND_MASKED_CLR	R/W1TC	0h	CPDMA THost Channel 7 Interrupt Pending CLR
6	TH6_PEND_MASKED_CLR	R/W1TC	0h	CPDMA THost Channel 6 Interrupt Pending CLR
5	TH5_PEND_MASKED_CLR	R/W1TC	0h	CPDMA THost Channel 5 Interrupt Pending CLR
4	TH4_PEND_MASKED_CLR	R/W1TC	0h	CPDMA THost Channel 4 Interrupt Pending CLR
3	TH3_PEND_MASKED_CLR	R/W1TC	0h	CPDMA THost Channel 3 Interrupt Pending CLR
2	TH2_PEND_MASKED_CLR	R/W1TC	0h	CPDMA THost Channel 2 Interrupt Pending CLR
1	TH1_PEND_MASKED_CLR	R/W1TC	0h	CPDMA THost Channel 1 Interrupt Pending CLR
0	TH0_PEND_MASKED_CLR	R/W1TC	0h	CPDMA THost Channel 0 Interrupt Pending CLR

4.18.247 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_INTSTAT_RAW_REG Registers

4.18.247.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_INTSTAT_RAW_REG Register (Offset = 340B0h) [reset = 0h]

Short Description: CPDMA DMA Interrupt Status RAW

Long Description: CPDMA DMA Interrupt Status RAW

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Table 4-2325. Instance Table

Instance Name	Physical Address
CPSW	5283 40B0h

Figure 4-1075. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_INTSTAT_RAW_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														HOST_PEND_RAW	STAT_PEND_RAW
NONE														R	R
0														0h	0h

Access Types Legend

Table 4-2326. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_INTSTAT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1	HOST_PEND_RAW	R	0h	CPDMA HOST Interrupt Pending RAW
0	STAT_PEND_RAW	R	0h	CPDMA Statistics Interrupt Pending RAW

4.18.248 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_INTSTAT_MASKED_REG Registers

4.18.248.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_INTSTAT_MASKED_REG Register (Offset = 340B4h) [reset = 0h]

Short Description: CPDMA DMA Interrupt Status MASKED

Long Description: CPDMA DMA Interrupt Status MASKED

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Table 4-2327. Instance Table

Instance Name	Physical Address
CPSW	5283 40B4h

Figure 4-1076. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_INTSTAT_MASKED_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														HOST_PEND	STAT_PEND
NONE														R	R
0														0h	0h

Access Types Legend

Table 4-2328. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_INTSTAT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1	HOST_PEND	R	0h	CPDMA HOST Interrupt Pending MASKED
0	STAT_PEND	R	0h	CPDMA Statistics Interrupt Pending MASKED

4.18.249 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_INTMASK_SET_REG Registers

4.18.249.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_INTMASK_SET_REG Register (Offset = 340B8h) [reset = 0h]

Short Description: CPDMA DMA Interrupt Status SET

Long Description: CPDMA DMA Interrupt Status SET

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Table 4-2329. Instance Table

Instance Name	Physical Address
CPSW	5283 40B8h

Figure 4-1077. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_INTMASK_SET_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														HOST_PEND_MASKED_SET	STAT_PEND_MASKED_SET
NONE														R/W1TS	R/W1TS
0														0h	0h

Access Types Legend

Table 4-2330. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_INTMASK_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1	HOST_PEND_MASKED_SET	R/W1TS	0h	CPDMA HOST Interrupt Masked SET
0	STAT_PEND_MASKED_SET	R/W1TS	0h	CPDMA Statistics Interrupt Masked SET

4.18.250 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_INTMASK_CLEAR_REG Registers

4.18.250.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_INTMASK_CLEAR_REG Register (Offset = 340BCh) [reset = 0h]

Short Description: CPDMA DMA Interrupt Status CLR

Long Description: CPDMA DMA Interrupt Status CLR

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Table 4-2331. Instance Table

Instance Name	Physical Address
CPSW	5283 40BCh

Figure 4-1078. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_INTMASK_CLEAR_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														HOST_PEND_MASKED_CLR	STAT_PEND_MASKED_CLR
NONE														R/W1TS	R/W1TS
0														0h	0h

Access Types Legend

Table 4-2332. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_INTMASK_CLEAR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1	HOST_PEND_MASKED_CLR	R/W1TS	0h	CPDMA HOST Interrupt Masked CLR
0	STAT_PEND_MASKED_CLR	R/W1TS	0h	CPDMA Statistics Interrupt Masked CLR

4.18.251 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH0_PENDTHRESH_REG Registers

4.18.251.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH0_PENDTHRESH_REG Register (Offset = 340C0h) [reset = 0h]

Short Description: CPDMA THost Threshold Pending Register

Long Description: CPDMA THost Threshold Pending Register

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Table 4-2333. Instance Table

Instance Name	Physical Address
CPSW	5283 40C0h

Figure 4-1079. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH0_PENDTHRESH_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TH0_PENDTHRESH							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-2334. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH0_PENDTHRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	TH0_PENDTHRESH	R/W	0h	CPDMA THost Threshold Pending Register

4.18.252 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH1_PENDTHRESH_REG Registers

4.18.252.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH1_PENDTHRESH_REG Register (Offset = 340C4h) [reset = 0h]

Short Description: CPDMA THost Threshold Pending Register

Long Description: CPDMA THost Threshold Pending Register

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Table 4-2335. Instance Table

Instance Name	Physical Address
CPSW	5283 40C4h

Figure 4-1080. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH1_PENDTHRESH_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TH1_PENDTHRESH							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-2336. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH1_PENDTHRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	TH1_PENDTHRESH	R/W	0h	CPDMA THost Threshold Pending Register

4.18.253 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH2_PENDTHRESH_REG Registers

4.18.253.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH2_PENDTHRESH_REG Register (Offset = 340C8h) [reset = 0h]

Short Description: CPDMA THost Threshold Pending Register

Long Description: CPDMA THost Threshold Pending Register

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Table 4-2337. Instance Table

Instance Name	Physical Address
CPSW	5283 40C8h

Figure 4-1081. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH2_PENDTHRESH_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TH2_PENDTHRESH							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-2338. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH2_PENDTHRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	TH2_PENDTHRESH	R/W	0h	CPDMA THost Threshold Pending Register

4.18.254 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH3_PENDTHRESH_REG Registers

4.18.254.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH3_PENDTHRESH_REG Register (Offset = 340CCh) [reset = 0h]

Short Description: CPDMA THost Threshold Pending Register

Long Description: CPDMA THost Threshold Pending Register

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Table 4-2339. Instance Table

Instance Name	Physical Address
CPSW	5283 40CCh

Figure 4-1082. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH3_PENDTHRESH_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TH3_PENDTHRESH							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-2340. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH3_PENDTHRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	TH3_PENDTHRESH	R/W	0h	CPDMA THost Threshold Pending Register

4.18.255 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH4_PENDTHRESH_REG Registers

4.18.255.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH4_PENDTHRESH_REG Register (Offset = 340D0h) [reset = 0h]

Short Description: CPDMA THost Threshold Pending Register

Long Description: CPDMA THost Threshold Pending Register

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Table 4-2341. Instance Table

Instance Name	Physical Address
CPSW	5283 40D0h

Figure 4-1083. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH4_PENDTHRESH_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TH4_PENDTHRESH							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-2342. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH4_PENDTHRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	TH4_PENDTHRESH	R/W	0h	CPDMA THost Threshold Pending Register

4.18.256 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH5_PENDTHRESH_REG Registers

4.18.256.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH5_PENDTHRESH_REG Register (Offset = 340D4h) [reset = 0h]

Short Description: CPDMA THost Threshold Pending Register

Long Description: CPDMA THost Threshold Pending Register

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Table 4-2343. Instance Table

Instance Name	Physical Address
CPSW	5283 40D4h

Figure 4-1084. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH5_PENDTHRESH_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TH5_PENDTHRESH							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-2344. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH5_PENDTHRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	TH5_PENDTHRESH	R/W	0h	CPDMA THost Threshold Pending Register

4.18.257 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH6_PENDTHRESH_REG Registers

4.18.257.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH6_PENDTHRESH_REG Register (Offset = 340D8h) [reset = 0h]

Short Description: CPDMA THost Threshold Pending Register

Long Description: CPDMA THost Threshold Pending Register

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Table 4-2345. Instance Table

Instance Name	Physical Address
CPSW	5283 40D8h

Figure 4-1085. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH6_PENDTHRESH_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TH6_PENDTHRESH							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-2346. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH6_PENDTHRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	TH6_PENDTHRESH	R/W	0h	CPDMA THost Threshold Pending Register

4.18.258 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH7_PENDTHRESH_REG Registers

4.18.258.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH7_PENDTHRESH_REG Register (Offset = 340DCh) [reset = 0h]

Short Description: CPDMA THost Threshold Pending Register

Long Description: CPDMA THost Threshold Pending Register

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Table 4-2347. Instance Table

Instance Name	Physical Address
CPSW	5283 40DCh

Figure 4-1086. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH7_PENDTHRESH_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TH7_PENDTHRESH							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-2348. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH7_PENDTHRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	TH7_PENDTHRESH	R/W	0h	CPDMA THost Threshold Pending Register

4.18.259 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH0_FREEBUFFER_REG Registers

4.18.259.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH0_FREEBUFFER_REG Register (Offset = 340E0h) [reset = 0h]

Short Description: CPDMA THost Free Buffer Register

Long Description: CPDMA THost Free Buffer Count Register

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Table 4-2349. Instance Table

Instance Name	Physical Address
CPSW	5283 40E0h

Figure 4-1087. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH0_FREEBUFFER_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	TH0_FREEBUFFER														
NONE	R/W														
0	0h														

Access Types Legend

Table 4-2350. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH0_FREEBUFFER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE		Reserved
14:0	TH0_FREEBUFFER	R/W	0h	CPDMA THost Free Buffer Count Register

4.18.260 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH1_FREEBUFFER_REG Registers

4.18.260.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH1_FREEBUFFER_REG Register (Offset = 340E4h) [reset = 0h]

Short Description: CPDMA THost Free Buffer Register

Long Description: CPDMA THost Free Buffer Count Register

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Table 4-2351. Instance Table

Instance Name	Physical Address
CPSW	5283 40E4h

Figure 4-1088. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH1_FREEBUFFER_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	TH1_FREEBUFFER														
NONE	R/W														
0	0h														

Access Types Legend

Table 4-2352. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH1_FREEBUFFER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE		Reserved
14:0	TH1_FREEBUFFER	R/W	0h	CPDMA THost Free Buffer Count Register

4.18.261 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH2_FREEBUFFER_REG Registers

4.18.261.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH2_FREEBUFFER_REG Register (Offset = 340E8h) [reset = 0h]

Short Description: CPDMA THost Free Buffer Register

Long Description: CPDMA THost Free Buffer Count Register

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Table 4-2353. Instance Table

Instance Name	Physical Address
CPSW	5283 40E8h

Figure 4-1089. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH2_FREEBUFFER_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	TH2_FREEBUFFER														
NONE	R/W														
0	0h														

Access Types Legend

Table 4-2354. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH2_FREEBUFFER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE		Reserved
14:0	TH2_FREEBUFFER	R/W	0h	CPDMA THost Free Buffer Count Register

4.18.262 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH3_FREEBUFFER_REG Registers

4.18.262.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH3_FREEBUFFER_REG Register (Offset = 340ECh) [reset = 0h]

Short Description: CPDMA THost Free Buffer Register

Long Description: CPDMA THost Free Buffer Count Register

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Table 4-2355. Instance Table

Instance Name	Physical Address
CPSW	5283 40ECh

Figure 4-1090. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH3_FREEBUFFER_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	TH3_FREEBUFFER														
NONE	R/W														
0	0h														

Access Types Legend

Table 4-2356. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH3_FREEBUFFER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE		Reserved
14:0	TH3_FREEBUFFER	R/W	0h	CPDMA THost Free Buffer Count Register

4.18.263 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH4_FREEBUFFER_REG Registers

4.18.263.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH4_FREEBUFFER_REG Register (Offset = 340F0h) [reset = 0h]

Short Description: CPDMA THost Free Buffer Register

Long Description: CPDMA THost Free Buffer Count Register

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Table 4-2357. Instance Table

Instance Name	Physical Address
CPSW	5283 40F0h

Figure 4-1091. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH4_FREEBUFFER_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	TH4_FREEBUFFER														
NONE	R/W														
0	0h														

Access Types Legend

Table 4-2358. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH4_FREEBUFFER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE		Reserved
14:0	TH4_FREEBUFFER	R/W	0h	CPDMA THost Free Buffer Count Register

4.18.264 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH5_FREEBUFFER_REG Registers

4.18.264.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH5_FREEBUFFER_REG Register (Offset = 340F4h) [reset = 0h]

Short Description: CPDMA THost Free Buffer Register

Long Description: CPDMA THost Free Buffer Count Register

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Table 4-2359. Instance Table

Instance Name	Physical Address
CPSW	5283 40F4h

Figure 4-1092. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH5_FREEBUFFER_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	TH5_FREEBUFFER														
NONE	R/W														
0	0h														

Access Types Legend

Table 4-2360. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH5_FREEBUFFER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE		Reserved
14:0	TH5_FREEBUFFER	R/W	0h	CPDMA THost Free Buffer Count Register

4.18.265 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH6_FREEBUFFER_REG Registers

4.18.265.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH6_FREEBUFFER_REG Register (Offset = 340F8h) [reset = 0h]

Short Description: CPDMA THost Free Buffer Register

Long Description: CPDMA THost Free Buffer Count Register

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Table 4-2361. Instance Table

Instance Name	Physical Address
CPSW	5283 40F8h

Figure 4-1093. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH6_FREEBUFFER_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	TH6_FREEBUFFER														
NONE	R/W														
0	0h														

Access Types Legend

Table 4-2362. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH6_FREEBUFFER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE		Reserved
14:0	TH6_FREEBUFFER	R/W	0h	CPDMA THost Free Buffer Count Register

4.18.266 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH7_FREEBUFFER_REG Registers

4.18.266.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH7_FREEBUFFER_REG Register (Offset = 340FCh) [reset = 0h]

Short Description: CPDMA THost Free Buffer Register

Long Description: CPDMA THost Free Buffer Count Register

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Table 4-2363. Instance Table

Instance Name	Physical Address
CPSW	5283 40FCh

Figure 4-1094. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH7_FREEBUFFER_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	TH7_FREEBUFFER														
NONE	R/W														
0	0h														

Access Types Legend

Table 4-2364. CPSW_NC_CPSW_NC_CPSW_CPDMA_INT_CPDMA_TH7_FREEBUFFER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE		Reserved
14:0	TH7_FREEBUFFER	R/W	0h	CPDMA THost Free Buffer Count Register

4.18.267 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH0_HDP_REG Registers

4.18.267.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH0_HDP_REG Register (Offset = 34200h) [reset = 0h]

Short Description: CPDMA FHost Channel 0 HDP

Long Description: CPDMA FHost Channel 0 Head Descriptor Pointer

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Table 4-2365. Instance Table

Instance Name	Physical Address
CPSW	5283 4200h

Figure 4-1095. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH0_HDP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FH0_HDP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FH0_HDP															
R/W															
0h															

Access Types Legend

Table 4-2366. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH0_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FH0_HDP	R/W	0h	CPDMA FHost Channel 0 Head Descriptor Pointer

4.18.268 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH1_HDP_REG Registers

4.18.268.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH1_HDP_REG Register (Offset = 34204h) [reset = 0h]

Short Description: CPDMA FHost Channel 1 HDP

Long Description: CPDMA FHost Channel 1 Head Descriptor Pointer

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Table 4-2367. Instance Table

Instance Name	Physical Address
CPSW	5283 4204h

Figure 4-1096. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH1_HDP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FH1_HDP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FH1_HDP															
R/W															
0h															

Access Types Legend

Table 4-2368. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH1_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FH1_HDP	R/W	0h	CPDMA FHost Channel 1 Head Descriptor Pointer

4.18.269 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH2_HDP_REG Registers

4.18.269.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH2_HDP_REG Register (Offset = 34208h) [reset = 0h]

Short Description: CPDMA FHost Channel 2 HDP

Long Description: CPDMA FHost Channel 2 Head Descriptor Pointer

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Table 4-2369. Instance Table

Instance Name	Physical Address
CPSW	5283 4208h

Figure 4-1097. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH2_HDP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FH2_HDP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FH2_HDP															
R/W															
0h															

Access Types Legend

Table 4-2370. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH2_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FH2_HDP	R/W	0h	CPDMA FHost Channel 2 Head Descriptor Pointer

4.18.270 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH3_HDP_REG Registers

4.18.270.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH3_HDP_REG Register (Offset = 3420Ch) [reset = 0h]

Short Description: CPDMA FHost Channel 3 HDP

Long Description: CPDMA FHost Channel 3 Head Descriptor Pointer

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Table 4-2371. Instance Table

Instance Name	Physical Address
CPSW	5283 420Ch

Figure 4-1098. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH3_HDP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FH3_HDP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FH3_HDP															
R/W															
0h															

Access Types Legend

Table 4-2372. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH3_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FH3_HDP	R/W	0h	CPDMA FHost Channel 3 Head Descriptor Pointer

4.18.271 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH4_HDP_REG Registers

4.18.271.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH4_HDP_REG Register (Offset = 34210h) [reset = 0h]

Short Description: CPDMA FHost Channel 4 HDP

Long Description: CPDMA FHost Channel 4 Head Descriptor Pointer

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Table 4-2373. Instance Table

Instance Name	Physical Address
CPSW	5283 4210h

Figure 4-1099. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH4_HDP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FH4_HDP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FH4_HDP															
R/W															
0h															

Access Types Legend

Table 4-2374. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH4_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FH4_HDP	R/W	0h	CPDMA FHost Channel 4 Head Descriptor Pointer

4.18.272 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH5_HDP_REG Registers

4.18.272.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH5_HDP_REG Register (Offset = 34214h) [reset = 0h]

Short Description: CPDMA FHost Channel 5 HDP

Long Description: CPDMA FHost Channel 5 Head Descriptor Pointer

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Table 4-2375. Instance Table

Instance Name	Physical Address
CPSW	5283 4214h

Figure 4-1100. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH5_HDP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FH5_HDP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FH5_HDP															
R/W															
0h															

Access Types Legend

Table 4-2376. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH5_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FH5_HDP	R/W	0h	CPDMA FHost Channel 5 Head Descriptor Pointer

4.18.273 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH6_HDP_REG Registers

4.18.273.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH6_HDP_REG Register (Offset = 34218h) [reset = 0h]

Short Description: CPDMA FHost Channel 6 HDP

Long Description: CPDMA FHost Channel 6 Head Descriptor Pointer

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Table 4-2377. Instance Table

Instance Name	Physical Address
CPSW	5283 4218h

Figure 4-1101. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH6_HDP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FH6_HDP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FH6_HDP															
R/W															
0h															

Access Types Legend

Table 4-2378. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH6_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FH6_HDP	R/W	0h	CPDMA FHost Channel 6 Head Descriptor Pointer

4.18.274 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH7_HDP_REG Registers

4.18.274.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH7_HDP_REG Register (Offset = 3421Ch) [reset = 0h]

Short Description: CPDMA FHost Channel 7 HDP

Long Description: CPDMA FHost Channel 7 Head Descriptor Pointer

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Table 4-2379. Instance Table

Instance Name	Physical Address
CPSW	5283 421Ch

Figure 4-1102. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH7_HDP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FH7_HDP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FH7_HDP															
R/W															
0h															

Access Types Legend

Table 4-2380. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH7_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FH7_HDP	R/W	0h	CPDMA FHost Channel 7 Head Descriptor Pointer

4.18.275 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH0_HDP_REG Registers

4.18.275.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH0_HDP_REG Register (Offset = 34220h) [reset = 0h]

Short Description: CPDMA THost Channel 0 HDP

Long Description: CPDMA THost Channel 0 Head Descriptor Pointer

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Table 4-2381. Instance Table

Instance Name	Physical Address
CPSW	5283 4220h

Figure 4-1103. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH0_HDP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TH0_HDP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TH0_HDP															
R/W															
0h															

Access Types Legend

Table 4-2382. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH0_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TH0_HDP	R/W	0h	CPDMA THost Channel 0 Head Descriptor Pointer

4.18.276 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH1_HDP_REG Registers

4.18.276.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH1_HDP_REG Register (Offset = 34224h) [reset = 0h]

Short Description: CPDMA THost Channel 1 HDP

Long Description: CPDMA THost Channel 1 Head Descriptor Pointer

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Table 4-2383. Instance Table

Instance Name	Physical Address
CPSW	5283 4224h

Figure 4-1104. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH1_HDP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TH1_HDP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TH1_HDP															
R/W															
0h															

Access Types Legend

Table 4-2384. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH1_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TH1_HDP	R/W	0h	CPDMA THost Channel 1 Head Descriptor Pointer

4.18.277 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH2_HDP_REG Registers

4.18.277.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH2_HDP_REG Register (Offset = 34228h) [reset = 0h]

Short Description: CPDMA THost Channel 2 HDP

Long Description: CPDMA THost Channel 2 Head Descriptor Pointer

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Table 4-2385. Instance Table

Instance Name	Physical Address
CPSW	5283 4228h

Figure 4-1105. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH2_HDP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TH2_HDP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TH2_HDP															
R/W															
0h															

Access Types Legend

Table 4-2386. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH2_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TH2_HDP	R/W	0h	CPDMA THost Channel 2 Head Descriptor Pointer

4.18.278 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH3_HDP_REG Registers

4.18.278.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH3_HDP_REG Register (Offset = 3422Ch) [reset = 0h]

Short Description: CPDMA THost Channel 3 HDP

Long Description: CPDMA THost Channel 3 Head Descriptor Pointer

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Table 4-2387. Instance Table

Instance Name	Physical Address
CPSW	5283 422Ch

Figure 4-1106. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH3_HDP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TH3_HDP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TH3_HDP															
R/W															
0h															

Access Types Legend

Table 4-2388. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH3_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TH3_HDP	R/W	0h	CPDMA THost Channel 3 Head Descriptor Pointer

4.18.279 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH4_HDP_REG Registers

4.18.279.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH4_HDP_REG Register (Offset = 34230h) [reset = 0h]

Short Description: CPDMA THost Channel 4 HDP

Long Description: CPDMA THost Channel 4 Head Descriptor Pointer

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Table 4-2389. Instance Table

Instance Name	Physical Address
CPSW	5283 4230h

Figure 4-1107. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH4_HDP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TH4_HDP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TH4_HDP															
R/W															
0h															

Access Types Legend

Table 4-2390. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH4_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TH4_HDP	R/W	0h	CPDMA THost Channel 4 Head Descriptor Pointer

4.18.280 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH5_HDP_REG Registers

4.18.280.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH5_HDP_REG Register (Offset = 34234h) [reset = 0h]

Short Description: CPDMA THost Channel 5 HDP

Long Description: CPDMA THost Channel 5 Head Descriptor Pointer

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Table 4-2391. Instance Table

Instance Name	Physical Address
CPSW	5283 4234h

Figure 4-1108. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH5_HDP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TH5_HDP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TH5_HDP															
R/W															
0h															

Access Types Legend

Table 4-2392. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH5_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TH5_HDP	R/W	0h	CPDMA THost Channel 5 Head Descriptor Pointer

4.18.281 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH6_HDP_REG Registers

4.18.281.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH6_HDP_REG Register (Offset = 34238h) [reset = 0h]

Short Description: CPDMA THost Channel 6 HDP

Long Description: CPDMA THost Channel 6 Head Descriptor Pointer

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Table 4-2393. Instance Table

Instance Name	Physical Address
CPSW	5283 4238h

Figure 4-1109. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH6_HDP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TH6_HDP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TH6_HDP															
R/W															
0h															

Access Types Legend

Table 4-2394. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH6_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TH6_HDP	R/W	0h	CPDMA THost Channel 6 Head Descriptor Pointer

4.18.282 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH7_HDP_REG Registers

4.18.282.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH7_HDP_REG Register (Offset = 3423Ch) [reset = 0h]

Short Description: CPDMA THost Channel 7 HDP

Long Description: CPDMA THost Channel 7 Head Descriptor Pointer

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Table 4-2395. Instance Table

Instance Name	Physical Address
CPSW	5283 423Ch

Figure 4-1110. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH7_HDP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TH7_HDP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TH7_HDP															
R/W															
0h															

Access Types Legend

Table 4-2396. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH7_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TH7_HDP	R/W	0h	CPDMA THost Channel 7 Head Descriptor Pointer

4.18.283 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH0_CP_REG Registers

4.18.283.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH0_CP_REG Register (Offset = 34240h) [reset = 0h]

Short Description: CPDMA FHost Channel 0 CP

Long Description: CPDMA FHost Channel 0 Completion Pointer

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Table 4-2397. Instance Table

Instance Name	Physical Address
CPSW	5283 4240h

Figure 4-1111. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH0_CP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FH0_CP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FH0_CP															
R/W															
0h															

Access Types Legend

Table 4-2398. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH0_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FH0_CP	R/W	0h	CPDMA FHost Channel 0 Completion Pointer

4.18.284 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH1_CP_REG Registers

4.18.284.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH1_CP_REG Register (Offset = 34244h) [reset = 0h]

Short Description: CPDMA FHost Channel 1 CP

Long Description: CPDMA FHost Channel 1 Completion Pointer

Return to Summary Table

Table 4-2399. Instance Table

Instance Name	Physical Address
CPSW	5283 4244h

Figure 4-1112. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH1_CP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FH1_CP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FH1_CP															
R/W															
0h															

Access Types Legend

Table 4-2400. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH1_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FH1_CP	R/W	0h	CPDMA FHost Channel 1 Completion Pointer

4.18.285 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH2_CP_REG Registers

4.18.285.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH2_CP_REG Register (Offset = 34248h) [reset = 0h]

Short Description: CPDMA FHost Channel 2 CP

Long Description: CPDMA FHost Channel 2 Completion Pointer

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Table 4-2401. Instance Table

Instance Name	Physical Address
CPSW	5283 4248h

Figure 4-1113. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH2_CP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FH2_CP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FH2_CP															
R/W															
0h															

Access Types Legend

Table 4-2402. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH2_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FH2_CP	R/W	0h	CPDMA FHost Channel 2 Completion Pointer

4.18.286 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH3_CP_REG Registers

4.18.286.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH3_CP_REG Register (Offset = 3424Ch) [reset = 0h]

Short Description: CPDMA FHost Channel 3 CP

Long Description: CPDMA FHost Channel 3 Completion Pointer

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Table 4-2403. Instance Table

Instance Name	Physical Address
CPSW	5283 424Ch

Figure 4-1114. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH3_CP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FH3_CP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FH3_CP															
R/W															
0h															

Access Types Legend

Table 4-2404. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH3_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FH3_CP	R/W	0h	CPDMA FHost Channel 3 Completion Pointer

4.18.287 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH4_CP_REG Registers

4.18.287.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH4_CP_REG Register (Offset = 34250h) [reset = 0h]

Short Description: CPDMA FHost Channel 4 CP

Long Description: CPDMA FHost Channel 4 Completion Pointer

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Table 4-2405. Instance Table

Instance Name	Physical Address
CPSW	5283 4250h

Figure 4-1115. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH4_CP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FH4_CP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FH4_CP															
R/W															
0h															

Access Types Legend

Table 4-2406. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH4_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FH4_CP	R/W	0h	CPDMA FHost Channel 4 Completion Pointer

4.18.288 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH5_CP_REG Registers

4.18.288.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH5_CP_REG Register (Offset = 34254h) [reset = 0h]

Short Description: CPDMA FHost Channel 5 CP

Long Description: CPDMA FHost Channel 5 Completion Pointer

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Table 4-2407. Instance Table

Instance Name	Physical Address
CPSW	5283 4254h

Figure 4-1116. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH5_CP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FH5_CP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FH5_CP															
R/W															
0h															

Access Types Legend

Table 4-2408. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH5_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FH5_CP	R/W	0h	CPDMA FHost Channel 5 Completion Pointer

4.18.289 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH6_CP_REG Registers

4.18.289.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH6_CP_REG Register (Offset = 34258h) [reset = 0h]

Short Description: CPDMA FHost Channel 6 CP

Long Description: CPDMA FHost Channel 6 Completion Pointer

Return to Summary Table

Table 4-2409. Instance Table

Instance Name	Physical Address
CPSW	5283 4258h

Figure 4-1117. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH6_CP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FH6_CP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FH6_CP															
R/W															
0h															

Access Types Legend

Table 4-2410. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH6_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FH6_CP	R/W	0h	CPDMA FHost Channel 6 Completion Pointer

4.18.290 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH7_CP_REG Registers

4.18.290.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH7_CP_REG Register (Offset = 3425Ch) [reset = 0h]

Short Description: CPDMA FHost Channel 7 CP

Long Description: CPDMA FHost Channel 7 Completion Pointer

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Table 4-2411. Instance Table

Instance Name	Physical Address
CPSW	5283 425Ch

Figure 4-1118. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH7_CP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FH7_CP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FH7_CP															
R/W															
0h															

Access Types Legend

Table 4-2412. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_FH7_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FH7_CP	R/W	0h	CPDMA FHost Channel 7 Completion Pointer

4.18.291 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH0_CP_REG Registers

4.18.291.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH0_CP_REG Register (Offset = 34260h) [reset = 0h]

Short Description: CPDMA THost Channel 0 CP

Long Description: CPDMA THost Channel 0 Completion Pointer

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Table 4-2413. Instance Table

Instance Name	Physical Address
CPSW	5283 4260h

Figure 4-1119. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH0_CP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TH0_CP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TH0_CP															
R/W															
0h															

Access Types Legend

Table 4-2414. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH0_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TH0_CP	R/W	0h	CPDMA THost Channel 0 Completion Pointer

4.18.292 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH1_CP_REG Registers

4.18.292.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH1_CP_REG Register (Offset = 34264h) [reset = 0h]

Short Description: CPDMA THost Channel 1 CP

Long Description: CPDMA THost Channel 1 Completion Pointer

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Table 4-2415. Instance Table

Instance Name	Physical Address
CPSW	5283 4264h

Figure 4-1120. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH1_CP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TH1_CP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TH1_CP															
R/W															
0h															

Access Types Legend

Table 4-2416. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH1_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TH1_CP	R/W	0h	CPDMA THost Channel 1 Completion Pointer

4.18.293 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH2_CP_REG Registers

4.18.293.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH2_CP_REG Register (Offset = 34268h) [reset = 0h]

Short Description: CPDMA THost Channel 2 CP

Long Description: CPDMA THost Channel 2 Completion Pointer

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Table 4-2417. Instance Table

Instance Name	Physical Address
CPSW	5283 4268h

Figure 4-1121. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH2_CP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TH2_CP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TH2_CP															
R/W															
0h															

Access Types Legend

Table 4-2418. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH2_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TH2_CP	R/W	0h	CPDMA THost Channel 2 Completion Pointer

4.18.294 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH3_CP_REG Registers

4.18.294.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH3_CP_REG Register (Offset = 3426Ch) [reset = 0h]

Short Description: CPDMA THost Channel 3 CP

Long Description: CPDMA THost Channel 3 Completion Pointer

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Table 4-2419. Instance Table

Instance Name	Physical Address
CPSW	5283 426Ch

Figure 4-1122. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH3_CP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TH3_CP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TH3_CP															
R/W															
0h															

Access Types Legend

Table 4-2420. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH3_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TH3_CP	R/W	0h	CPDMA THost Channel 3 Completion Pointer

4.18.295 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH4_CP_REG Registers

4.18.295.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH4_CP_REG Register (Offset = 34270h) [reset = 0h]

Short Description: CPDMA THost Channel 4 CP

Long Description: CPDMA THost Channel 4 Completion Pointer

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Table 4-2421. Instance Table

Instance Name	Physical Address
CPSW	5283 4270h

Figure 4-1123. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH4_CP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TH4_CP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TH4_CP															
R/W															
0h															

Access Types Legend

Table 4-2422. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH4_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TH4_CP	R/W	0h	CPDMA THost Channel 4 Completion Pointer

4.18.296 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH5_CP_REG Registers

4.18.296.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH5_CP_REG Register (Offset = 34274h) [reset = 0h]

Short Description: CPDMA THost Channel 5 CP

Long Description: CPDMA THost Channel 5 Completion Pointer

Return to Summary Table

Table 4-2423. Instance Table

Instance Name	Physical Address
CPSW	5283 4274h

Figure 4-1124. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH5_CP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TH5_CP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TH5_CP															
R/W															
0h															

Access Types Legend

Table 4-2424. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH5_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TH5_CP	R/W	0h	CPDMA THost Channel 5 Completion Pointer

4.18.297 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH6_CP_REG Registers

4.18.297.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH6_CP_REG Register (Offset = 34278h) [reset = 0h]

Short Description: CPDMA THost Channel 6 CP

Long Description: CPDMA THost Channel 6 Completion Pointer

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Table 4-2425. Instance Table

Instance Name	Physical Address
CPSW	5283 4278h

Figure 4-1125. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH6_CP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TH6_CP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TH6_CP															
R/W															
0h															

Access Types Legend

Table 4-2426. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH6_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TH6_CP	R/W	0h	CPDMA THost Channel 6 Completion Pointer

4.18.298 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH7_CP_REG Registers

4.18.298.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH7_CP_REG Register (Offset = 3427Ch) [reset = 0h]

Short Description: CPDMA THost Channel 7 CP

Long Description: CPDMA THost Channel 7 Completion Pointer

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Table 4-2427. Instance Table

Instance Name	Physical Address
CPSW	5283 427Ch

Figure 4-1126. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH7_CP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TH7_CP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TH7_CP															
R/W															
0h															

Access Types Legend

Table 4-2428. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_CPDMA_TH7_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TH7_CP	R/W	0h	CPDMA THost Channel 7 Completion Pointer

4.18.299 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH0_HDP_REG Registers

4.18.299.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH0_HDP_REG Register (Offset = 34300h) [reset = 0h]

Short Description: Test CPDMA FHost Channel 0 HDP

Long Description: Test CPDMA FHost Channel 0 Head Descriptor Pointer

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Table 4-2429. Instance Table

Instance Name	Physical Address
CPSW	5283 4300h

Figure 4-1127. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH0_HDP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TEST_FH0_HDP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEST_FH0_HDP															
R/W															
0h															

Access Types Legend

Table 4-2430. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH0_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_FH0_HDP	R/W	0h	Test CPDMA FHost Channel 0 Head Descriptor Pointer

4.18.300 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH1_HDP_REG Registers

4.18.300.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH1_HDP_REG Register (Offset = 34304h) [reset = 0h]

Short Description: Test CPDMA FHost Channel 1 HDP

Long Description: Test CPDMA FHost Channel 1 Head Descriptor Pointer

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Table 4-2431. Instance Table

Instance Name	Physical Address
CPSW	5283 4304h

Figure 4-1128. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH1_HDP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TEST_FH1_HDP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEST_FH1_HDP															
R/W															
0h															

Access Types Legend

Table 4-2432. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH1_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_FH1_HDP	R/W	0h	Test CPDMA FHost Channel 1 Head Descriptor Pointer

4.18.301 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH2_HDP_REG Registers

4.18.301.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH2_HDP_REG Register (Offset = 34308h) [reset = 0h]

Short Description: Test CPDMA FHost Channel 2 HDP

Long Description: Test CPDMA FHost Channel 2 Head Descriptor Pointer

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Table 4-2433. Instance Table

Instance Name	Physical Address
CPSW	5283 4308h

Figure 4-1129. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH2_HDP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TEST_FH2_HDP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEST_FH2_HDP															
R/W															
0h															

Access Types Legend

Table 4-2434. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH2_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_FH2_HDP	R/W	0h	Test CPDMA FHost Channel 2 Head Descriptor Pointer

4.18.302 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH3_HDP_REG Registers

4.18.302.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH3_HDP_REG Register (Offset = 3430Ch) [reset = 0h]

Short Description: Test CPDMA FHost Channel 3 HDP

Long Description: Test CPDMA FHost Channel 3 Head Descriptor Pointer

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Table 4-2435. Instance Table

Instance Name	Physical Address
CPSW	5283 430Ch

Figure 4-1130. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH3_HDP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TEST_FH3_HDP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEST_FH3_HDP															
R/W															
0h															

Access Types Legend

Table 4-2436. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH3_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_FH3_HDP	R/W	0h	Test CPDMA FHost Channel 3 Head Descriptor Pointer

4.18.303 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH4_HDP_REG Registers

4.18.303.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH4_HDP_REG Register (Offset = 34310h) [reset = 0h]

Short Description: Test CPDMA FHost Channel 4 HDP

Long Description: Test CPDMA FHost Channel 4 Head Descriptor Pointer

Return to Summary Table

Table 4-2437. Instance Table

Instance Name	Physical Address
CPSW	5283 4310h

Figure 4-1131. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH4_HDP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TEST_FH4_HDP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEST_FH4_HDP															
R/W															
0h															

Access Types Legend

Table 4-2438. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH4_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_FH4_HDP	R/W	0h	Test CPDMA FHost Channel 4 Head Descriptor Pointer

4.18.304 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH5_HDP_REG Registers

4.18.304.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH5_HDP_REG Register (Offset = 34314h) [reset = 0h]

Short Description: Test CPDMA FHost Channel 5 HDP

Long Description: Test CPDMA FHost Channel 5 Head Descriptor Pointer

Return to Summary Table

Table 4-2439. Instance Table

Instance Name	Physical Address
CPSW	5283 4314h

Figure 4-1132. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH5_HDP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TEST_FH5_HDP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEST_FH5_HDP															
R/W															
0h															

Access Types Legend

Table 4-2440. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH5_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_FH5_HDP	R/W	0h	Test CPDMA FHost Channel 5 Head Descriptor Pointer

4.18.305 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH6_HDP_REG Registers

4.18.305.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH6_HDP_REG Register (Offset = 34318h) [reset = 0h]

Short Description: Test CPDMA FHost Channel 6 HDP

Long Description: Test CPDMA FHost Channel 6 Head Descriptor Pointer

Return to Summary Table

Table 4-2441. Instance Table

Instance Name	Physical Address
CPSW	5283 4318h

Figure 4-1133. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH6_HDP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TEST_FH6_HDP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEST_FH6_HDP															
R/W															
0h															

Access Types Legend

Table 4-2442. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH6_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_FH6_HDP	R/W	0h	Test CPDMA FHost Channel 6 Head Descriptor Pointer

4.18.306 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH7_HDP_REG Registers

4.18.306.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH7_HDP_REG Register (Offset = 3431Ch) [reset = 0h]

Short Description: Test CPDMA FHost Channel 7 HDP

Long Description: Test CPDMA FHost Channel 7 Head Descriptor Pointer

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Table 4-2443. Instance Table

Instance Name	Physical Address
CPSW	5283 431Ch

Figure 4-1134. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH7_HDP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TEST_FH7_HDP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEST_FH7_HDP															
R/W															
0h															

Access Types Legend

Table 4-2444. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH7_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_FH7_HDP	R/W	0h	Test CPDMA FHost Channel 7 Head Descriptor Pointer

4.18.307 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH0_HDP_REG Registers

4.18.307.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH0_HDP_REG Register (Offset = 34320h) [reset = 0h]

Short Description: Test CPDMA THost Channel 0 HDP

Long Description: Test CPDMA THost Channel 0 Head Descriptor Pointer

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Table 4-2445. Instance Table

Instance Name	Physical Address
CPSW	5283 4320h

Figure 4-1135. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH0_HDP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TEST_TH0_HDP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEST_TH0_HDP															
R/W															
0h															

Access Types Legend

Table 4-2446. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH0_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_TH0_HDP	R/W	0h	Test CPDMA THost Channel 0 Head Descriptor Pointer

4.18.308 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH1_HDP_REG Registers

4.18.308.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH1_HDP_REG Register (Offset = 34324h) [reset = 0h]

Short Description: Test CPDMA THost Channel 1 HDP

Long Description: Test CPDMA THost Channel 1 Head Descriptor Pointer

Return to Summary Table

Table 4-2447. Instance Table

Instance Name	Physical Address
CPSW	5283 4324h

Figure 4-1136. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH1_HDP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TEST_TH1_HDP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEST_TH1_HDP															
R/W															
0h															

Access Types Legend

Table 4-2448. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH1_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_TH1_HDP	R/W	0h	Test CPDMA THost Channel 1 Head Descriptor Pointer

4.18.309 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH2_HDP_REG Registers

4.18.309.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH2_HDP_REG Register (Offset = 34328h) [reset = 0h]

Short Description: Test CPDMA THost Channel 2 HDP

Long Description: Test CPDMA THost Channel 2 Head Descriptor Pointer

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Table 4-2449. Instance Table

Instance Name	Physical Address
CPSW	5283 4328h

Figure 4-1137. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH2_HDP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TEST_TH2_HDP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEST_TH2_HDP															
R/W															
0h															

Access Types Legend

Table 4-2450. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH2_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_TH2_HDP	R/W	0h	Test CPDMA THost Channel 2 Head Descriptor Pointer

4.18.310 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH3_HDP_REG Registers

4.18.310.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH3_HDP_REG Register (Offset = 3432Ch) [reset = 0h]

Short Description: Test CPDMA THost Channel 3 HDP

Long Description: Test CPDMA THost Channel 3 Head Descriptor Pointer

Return to Summary Table

Table 4-2451. Instance Table

Instance Name	Physical Address
CPSW	5283 432Ch

Figure 4-1138. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH3_HDP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TEST_TH3_HDP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEST_TH3_HDP															
R/W															
0h															

Access Types Legend

Table 4-2452. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH3_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_TH3_HDP	R/W	0h	Test CPDMA THost Channel 3 Head Descriptor Pointer

4.18.311 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH4_HDP_REG Registers

4.18.311.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH4_HDP_REG Register (Offset = 34330h) [reset = 0h]

Short Description: Test CPDMA THost Channel 4 HDP

Long Description: Test CPDMA THost Channel 4 Head Descriptor Pointer

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Table 4-2453. Instance Table

Instance Name	Physical Address
CPSW	5283 4330h

Figure 4-1139. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH4_HDP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TEST_TH4_HDP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEST_TH4_HDP															
R/W															
0h															

Access Types Legend

Table 4-2454. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH4_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_TH4_HDP	R/W	0h	Test CPDMA THost Channel 4 Head Descriptor Pointer

4.18.312 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH5_HDP_REG Registers

4.18.312.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH5_HDP_REG Register (Offset = 34334h) [reset = 0h]

Short Description: Test CPDMA THost Channel 5 HDP

Long Description: Test CPDMA THost Channel 5 Head Descriptor Pointer

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Table 4-2455. Instance Table

Instance Name	Physical Address
CPSW	5283 4334h

Figure 4-1140. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH5_HDP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TEST_TH5_HDP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEST_TH5_HDP															
R/W															
0h															

Access Types Legend

Table 4-2456. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH5_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_TH5_HDP	R/W	0h	Test CPDMA THost Channel 5 Head Descriptor Pointer

4.18.313 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH6_HDP_REG Registers

4.18.313.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH6_HDP_REG Register (Offset = 34338h) [reset = 0h]

Short Description: Test CPDMA THost Channel 6 HDP

Long Description: Test CPDMA THost Channel 6 Head Descriptor Pointer

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Table 4-2457. Instance Table

Instance Name	Physical Address
CPSW	5283 4338h

Figure 4-1141. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH6_HDP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TEST_TH6_HDP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEST_TH6_HDP															
R/W															
0h															

Access Types Legend

Table 4-2458. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH6_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_TH6_HDP	R/W	0h	Test CPDMA THost Channel 6 Head Descriptor Pointer

4.18.314 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH7_HDP_REG Registers

4.18.314.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH7_HDP_REG Register (Offset = 3433Ch) [reset = 0h]

Short Description: Test CPDMA THost Channel 7 HDP

Long Description: Test CPDMA THost Channel 7 Head Descriptor Pointer

Return to Summary Table

Table 4-2459. Instance Table

Instance Name	Physical Address
CPSW	5283 433Ch

Figure 4-1142. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH7_HDP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TEST_TH7_HDP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEST_TH7_HDP															
R/W															
0h															

Access Types Legend

Table 4-2460. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH7_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_TH7_HDP	R/W	0h	Test CPDMA THost Channel 7 Head Descriptor Pointer

4.18.315 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH0_CP_REG Registers

4.18.315.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH0_CP_REG Register (Offset = 34340h) [reset = 0h]

Short Description: Test CPDMA FHost Channel 0 CP

Long Description: Test CPDMA FHost Channel 0 Completion Pointer

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Table 4-2461. Instance Table

Instance Name	Physical Address
CPSW	5283 4340h

Figure 4-1143. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH0_CP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TEST_FH0_CP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEST_FH0_CP															
R/W															
0h															

Access Types Legend

Table 4-2462. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH0_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_FH0_CP	R/W	0h	Test CPDMA FHost Channel 0 Completion Pointer

4.18.316 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH1_CP_REG Registers

4.18.316.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH1_CP_REG Register (Offset = 34344h) [reset = 0h]

Short Description: Test CPDMA FHost Channel 1 CP

Long Description: Test CPDMA FHost Channel 1 Completion Pointer

Return to Summary Table

Table 4-2463. Instance Table

Instance Name	Physical Address
CPSW	5283 4344h

Figure 4-1144. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH1_CP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TEST_FH1_CP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEST_FH1_CP															
R/W															
0h															

Access Types Legend

Table 4-2464. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH1_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_FH1_CP	R/W	0h	Test CPDMA FHost Channel 1 Completion Pointer

4.18.317 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH2_CP_REG Registers

4.18.317.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH2_CP_REG Register (Offset = 34348h) [reset = 0h]

Short Description: Test CPDMA FHost Channel 2 CP

Long Description: Test CPDMA FHost Channel 2 Completion Pointer

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Table 4-2465. Instance Table

Instance Name	Physical Address
CPSW	5283 4348h

Figure 4-1145. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH2_CP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TEST_FH2_CP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEST_FH2_CP															
R/W															
0h															

Access Types Legend

Table 4-2466. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH2_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_FH2_CP	R/W	0h	Test CPDMA FHost Channel 2 Completion Pointer

4.18.318 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH3_CP_REG Registers

4.18.318.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH3_CP_REG Register (Offset = 3434Ch) [reset = 0h]

Short Description: Test CPDMA FHost Channel 3 CP

Long Description: Test CPDMA FHost Channel 3 Completion Pointer

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Table 4-2467. Instance Table

Instance Name	Physical Address
CPSW	5283 434Ch

Figure 4-1146. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH3_CP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TEST_FH3_CP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEST_FH3_CP															
R/W															
0h															

Access Types Legend

Table 4-2468. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH3_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_FH3_CP	R/W	0h	Test CPDMA FHost Channel 3 Completion Pointer

4.18.319 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH4_CP_REG Registers

4.18.319.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH4_CP_REG Register (Offset = 34350h) [reset = 0h]

Short Description: Test CPDMA FHost Channel 4 CP

Long Description: Test CPDMA FHost Channel 4 Completion Pointer

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Table 4-2469. Instance Table

Instance Name	Physical Address
CPSW	5283 4350h

Figure 4-1147. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH4_CP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TEST_FH4_CP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEST_FH4_CP															
R/W															
0h															

Access Types Legend

Table 4-2470. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH4_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_FH4_CP	R/W	0h	Test CPDMA FHost Channel 4 Completion Pointer

4.18.320 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH5_CP_REG Registers

4.18.320.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH5_CP_REG Register (Offset = 34354h) [reset = 0h]

Short Description: Test CPDMA FHost Channel 5 CP

Long Description: Test CPDMA FHost Channel 5 Completion Pointer

Return to Summary Table

Table 4-2471. Instance Table

Instance Name	Physical Address
CPSW	5283 4354h

Figure 4-1148. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH5_CP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TEST_FH5_CP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEST_FH5_CP															
R/W															
0h															

Access Types Legend

Table 4-2472. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH5_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_FH5_CP	R/W	0h	Test CPDMA FHost Channel 5 Completion Pointer

4.18.321 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH6_CP_REG Registers

4.18.321.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH6_CP_REG Register (Offset = 34358h) [reset = 0h]

Short Description: Test CPDMA FHost Channel 6 CP

Long Description: Test CPDMA FHost Channel 6 Completion Pointer

Return to Summary Table

Table 4-2473. Instance Table

Instance Name	Physical Address
CPSW	5283 4358h

Figure 4-1149. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH6_CP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TEST_FH6_CP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEST_FH6_CP															
R/W															
0h															

Access Types Legend

Table 4-2474. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH6_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_FH6_CP	R/W	0h	Test CPDMA FHost Channel 6 Completion Pointer

4.18.322 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH7_CP_REG Registers

4.18.322.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH7_CP_REG Register (Offset = 3435Ch) [reset = 0h]

Short Description: Test CPDMA FHost Channel 7 CP

Long Description: Test CPDMA FHost Channel 7 Completion Pointer

Return to Summary Table

Table 4-2475. Instance Table

Instance Name	Physical Address
CPSW	5283 435Ch

Figure 4-1150. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH7_CP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TEST_FH7_CP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEST_FH7_CP															
R/W															
0h															

Access Types Legend

Table 4-2476. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_FH7_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_FH7_CP	R/W	0h	Test CPDMA FHost Channel 7 Completion Pointer

4.18.323 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH0_CP_REG Registers

4.18.323.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH0_CP_REG Register (Offset = 34360h) [reset = 0h]

Short Description: Test CPDMA THost Channel 0 CP

Long Description: Test CPDMA THost Channel 0 Completion Pointer

Return to Summary Table

Table 4-2477. Instance Table

Instance Name	Physical Address
CPSW	5283 4360h

Figure 4-1151. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH0_CP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TEST_TH0_CP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEST_TH0_CP															
R/W															
0h															

Access Types Legend

Table 4-2478. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH0_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_TH0_CP	R/W	0h	Test CPDMA THost Channel 0 Completion Pointer

4.18.324 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH1_CP_REG Registers

4.18.324.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH1_CP_REG Register (Offset = 34364h) [reset = 0h]

Short Description: Test CPDMA THost Channel 1 CP

Long Description: Test CPDMA THost Channel 1 Completion Pointer

Return to Summary Table

Table 4-2479. Instance Table

Instance Name	Physical Address
CPSW	5283 4364h

Figure 4-1152. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH1_CP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TEST_TH1_CP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEST_TH1_CP															
R/W															
0h															

Access Types Legend

Table 4-2480. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH1_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_TH1_CP	R/W	0h	Test CPDMA THost Channel 1 Completion Pointer

4.18.325 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH2_CP_REG Registers

4.18.325.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH2_CP_REG Register (Offset = 34368h) [reset = 0h]

Short Description: Test CPDMA THost Channel 2 CP

Long Description: Test CPDMA THost Channel 2 Completion Pointer

Return to Summary Table

Table 4-2481. Instance Table

Instance Name	Physical Address
CPSW	5283 4368h

Figure 4-1153. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH2_CP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TEST_TH2_CP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEST_TH2_CP															
R/W															
0h															

Access Types Legend

Table 4-2482. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH2_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_TH2_CP	R/W	0h	Test CPDMA THost Channel 2 Completion Pointer

4.18.326 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH3_CP_REG Registers

4.18.326.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH3_CP_REG Register (Offset = 3436Ch) [reset = 0h]

Short Description: Test CPDMA THost Channel 3 CP

Long Description: Test CPDMA THost Channel 3 Completion Pointer

Return to Summary Table

Table 4-2483. Instance Table

Instance Name	Physical Address
CPSW	5283 436Ch

Figure 4-1154. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH3_CP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TEST_TH3_CP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEST_TH3_CP															
R/W															
0h															

Access Types Legend

Table 4-2484. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH3_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_TH3_CP	R/W	0h	Test CPDMA THost Channel 3 Completion Pointer

4.18.327 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH4_CP_REG Registers

4.18.327.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH4_CP_REG Register (Offset = 34370h) [reset = 0h]

Short Description: Test CPDMA THost Channel 4 CP

Long Description: Test CPDMA THost Channel 4 Completion Pointer

Return to Summary Table

Table 4-2485. Instance Table

Instance Name	Physical Address
CPSW	5283 4370h

Figure 4-1155. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH4_CP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TEST_TH4_CP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEST_TH4_CP															
R/W															
0h															

Access Types Legend

Table 4-2486. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH4_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_TH4_CP	R/W	0h	Test CPDMA THost Channel 4 Completion Pointer

4.18.328 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH5_CP_REG Registers

4.18.328.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH5_CP_REG Register (Offset = 34374h) [reset = 0h]

Short Description: Test CPDMA THost Channel 5 CP

Long Description: Test CPDMA THost Channel 5 Completion Pointer

Return to Summary Table

Table 4-2487. Instance Table

Instance Name	Physical Address
CPSW	5283 4374h

Figure 4-1156. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH5_CP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TEST_TH5_CP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEST_TH5_CP															
R/W															
0h															

Access Types Legend

Table 4-2488. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH5_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_TH5_CP	R/W	0h	Test CPDMA THost Channel 5 Completion Pointer

4.18.329 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH6_CP_REG Registers

4.18.329.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH6_CP_REG Register (Offset = 34378h) [reset = 0h]

Short Description: Test CPDMA THost Channel 6 CP

Long Description: Test CPDMA THost Channel 6 Completion Pointer

Return to Summary Table

Table 4-2489. Instance Table

Instance Name	Physical Address
CPSW	5283 4378h

Figure 4-1157. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH6_CP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TEST_TH6_CP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEST_TH6_CP															
R/W															
0h															

Access Types Legend

Table 4-2490. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH6_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_TH6_CP	R/W	0h	Test CPDMA THost Channel 6 Completion Pointer

4.18.330 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH7_CP_REG Registers

4.18.330.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH7_CP_REG Register (Offset = 3437Ch) [reset = 0h]

Short Description: Test CPDMA THost Channel 7 CP

Long Description: Test CPDMA THost Channel 7 Completion Pointer

Return to Summary Table

Table 4-2491. Instance Table

Instance Name	Physical Address
CPSW	5283 437Ch

Figure 4-1158. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH7_CP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TEST_TH7_CP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEST_TH7_CP															
R/W															
0h															

Access Types Legend

Table 4-2492. CPSW_NC_CPSW_NC_CPSW_CPDMA_SRAM_TEST_CPDMA_TH7_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_TH7_CP	R/W	0h	Test CPDMA THost Channel 7 Completion Pointer

4.18.331 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXGOODFRAMES_J Registers

4.18.331.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXGOODFRAMES_J Register (Offset = 3A000h) [reset = 0h]

Short Description: RxGoodFrames

Long Description: Total number of good frames received

Return to Summary Table

Offset = 3a000h + (j * 200h); where j = 0h to 2h

Table 4-2493. Instance Table

Instance Name	Physical Address
CPSW	5283 A000h

Figure 4-1159. CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXGOODFRAMES_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2494. CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXGOODFRAMES_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of good frames received

4.18.332 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXBROADCASTFRAMES_J Registers

4.18.332.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXBROADCASTFRAMES_J Register (Offset = 3A004h) [reset = 0h]

Short Description: RxBroadcastFrames

Long Description: Total number of good broadcast frames received

Return to Summary Table

Offset = 3a004h + (j * 200h); where j = 0h to 2h

Table 4-2495. Instance Table

Instance Name	Physical Address
CPSW	5283 A004h

Figure 4-1160. CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXBROADCASTFRAMES_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2496. CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXBROADCASTFRAMES_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of good broadcast frames received

4.18.333 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXMULTICASTFRAMES_J Registers

4.18.333.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXMULTICASTFRAMES_J Register (Offset = 3A008h) [reset = 0h]

Short Description: RxMulticastFrames

Long Description: Total number of good multicast frames received

Return to Summary Table

Offset = 3a008h + (j * 200h); where j = 0h to 2h

Table 4-2497. Instance Table

Instance Name	Physical Address
CPSW	5283 A008h

Figure 4-1161. CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXMULTICASTFRAMES_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2498. CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXMULTICASTFRAMES_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of good multicast frames received

4.18.334 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXPAUSEFRAMES_J Registers

4.18.334.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXPAUSEFRAMES_J Register (Offset = 3A00Ch) [reset = 0h]

Short Description: RxPauseFrames

Long Description: Total number of pause frames received

Return to Summary Table

Offset = 3a00ch + (j * 200h); where j = 0h to 2h

Table 4-2499. Instance Table

Instance Name	Physical Address
CPSW	5283 A00Ch

Figure 4-1162. CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXPAUSEFRAMES_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2500. CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXPAUSEFRAMES_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of pause frames received

4.18.335 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXCRCERRORS_J Registers

4.18.335.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXCRCERRORS_J Register (Offset = 3A010h) [reset = 0h]

Short Description: RxCRCErrors

Long Description: Total number of CRC errors frames received

Return to Summary Table

Offset = 3a010h + (j * 200h); where j = 0h to 2h

Table 4-2501. Instance Table

Instance Name	Physical Address
CPSW	5283 A010h

Figure 4-1163. CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXCRCERRORS_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2502. CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXCRCERRORS_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of CRC errors frames received

4.18.336 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXALIGNCODEERRORS_J Registers

4.18.336.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXALIGNCODEERRORS_J Register (Offset = 3A014h) [reset = 0h]

Short Description: RxAlignCodeErrors

Long Description: Total number of alignment/code errors received

Return to Summary Table

Offset = 3a014h + (j * 200h); where j = 0h to 2h

Table 4-2503. Instance Table

Instance Name	Physical Address
CPSW	5283 A014h

Figure 4-1164. CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXALIGNCODEERRORS_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2504. CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXALIGNCODEERRORS_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of alignment/code errors received

4.18.337 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXOVERSIZEDFRAMES_J Registers

4.18.337.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXOVERSIZEDFRAMES_J Register (Offset = 3A018h) [reset = 0h]

Short Description: RxOversizedFrames

Long Description: Total number of oversized frames received

Return to Summary Table

Offset = 3a018h + (j * 200h); where j = 0h to 2h

Table 4-2505. Instance Table

Instance Name	Physical Address
CPSW	5283 A018h

Figure 4-1165. CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXOVERSIZEDFRAMES_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2506. CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXOVERSIZEDFRAMES_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of oversized frames received

4.18.338 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXJABBERFRAMES_J Registers

4.18.338.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXJABBERFRAMES_J Register (Offset = 3A01Ch) [reset = 0h]

Short Description: RxJabberFrames

Long Description: Total number of jabber frames received

Return to Summary Table

Offset = 3a01ch + (j * 200h); where j = 0h to 2h

Table 4-2507. Instance Table

Instance Name	Physical Address
CPSW	5283 A01Ch

Figure 4-1166. CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXJABBERFRAMES_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2508. CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXJABBERFRAMES_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of jabber frames received

4.18.339 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXUNDERSIZEDFRAMES_J Registers

4.18.339.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXUNDERSIZEDFRAMES_J Register (Offset = 3A020h) [reset = 0h]

Short Description: RxUndersizedFrames

Long Description: Total number of undersized frames received

Return to Summary Table

Offset = 3a020h + (j * 200h); where j = 0h to 2h

Table 4-2509. Instance Table

Instance Name	Physical Address
CPSW	5283 A020h

Figure 4-1167. CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXUNDERSIZEDFRAMES_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2510. CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXUNDERSIZEDFRAMES_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of undersized frames received

4.18.340 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXFRAGMENTS_J Registers

4.18.340.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXFRAGMENTS_J Register (Offset = 3A024h) [reset = 0h]

Short Description: RxFragments

Long Description: Total number of fragmented frames received

Return to Summary Table

Offset = 3a024h + (j * 200h); where j = 0h to 2h

Table 4-2511. Instance Table

Instance Name	Physical Address
CPSW	5283 A024h

Figure 4-1168. CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXFRAGMENTS_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2512. CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXFRAGMENTS_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of fragmented frames received

4.18.341 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_DROP_J Registers

4.18.341.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_DROP_J Register (Offset = 3A028h) [reset = 0h]

Short Description: ALE_Drop

Long Description: Total number of frames dropped by the ALE

Return to Summary Table

Offset = 3a028h + (j * 200h); where j = 0h to 2h

Table 4-2513. Instance Table

Instance Name	Physical Address
CPSW	5283 A028h

Figure 4-1169. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_DROP_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2514. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_DROP_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of frames dropped by the ALE

4.18.342 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_OVERRUN_DROP_J Registers

4.18.342.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_OVERRUN_DROP_J Register (Offset = 3A02Ch) [reset = 0h]

Short Description: ALE_Overrun_Drop

Long Description: Total number of overrun frames dropped by the ALE

Return to Summary Table

Offset = 3a02ch + (j * 200h); where j = 0h to 2h

Table 4-2515. Instance Table

Instance Name	Physical Address
CPSW	5283 A02Ch

Figure 4-1170. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_OVERRUN_DROP_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2516. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_OVERRUN_DROP_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of overrun frames dropped by the ALE

4.18.343 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXOCTETS_J Registers

4.18.343.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXOCTETS_J Register (Offset = 3A030h) [reset = 0h]

Short Description: RxOctets

Long Description: Total number of received bytes in good frames

Return to Summary Table

Offset = 3a030h + (j * 200h); where j = 0h to 2h

Table 4-2517. Instance Table

Instance Name	Physical Address
CPSW	5283 A030h

Figure 4-1171. CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXOCTETS_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2518. CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXOCTETS_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of received bytes in good frames

4.18.344 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXGOODFRAMES_J Registers

4.18.344.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXGOODFRAMES_J Register (Offset = 3A034h) [reset = 0h]

Short Description: TxGoodFrames

Long Description: Total number of good frames transmitted

Return to Summary Table

Offset = 3a034h + (j * 200h); where j = 0h to 2h

Table 4-2519. Instance Table

Instance Name	Physical Address
CPSW	5283 A034h

Figure 4-1172. CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXGOODFRAMES_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2520. CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXGOODFRAMES_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of good frames transmitted

4.18.345 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXBROADCASTFRAMES_J Registers

4.18.345.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXBROADCASTFRAMES_J Register (Offset = 3A038h) [reset = 0h]

Short Description: TxBroadcastFrames

Long Description: Total number of good broadcast frames transmitted

Return to Summary Table

Offset = 3a038h + (j * 200h); where j = 0h to 2h

Table 4-2521. Instance Table

Instance Name	Physical Address
CPSW	5283 A038h

Figure 4-1173. CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXBROADCASTFRAMES_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2522. CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXBROADCASTFRAMES_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of good broadcast frames transmitted

4.18.346 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXMULTICASTFRAMES_J Registers

4.18.346.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXMULTICASTFRAMES_J Register (Offset = 3A03Ch) [reset = 0h]

Short Description: TxMulticastFrames

Long Description: Total number of good multicast frames transmitted

Return to Summary Table

Offset = 3a03ch + (j * 200h); where j = 0h to 2h

Table 4-2523. Instance Table

Instance Name	Physical Address
CPSW	5283 A03Ch

Figure 4-1174. CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXMULTICASTFRAMES_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2524. CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXMULTICASTFRAMES_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of good multicast frames transmitted

4.18.347 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXPAUSEFRAMES_J Registers

4.18.347.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXPAUSEFRAMES_J Register (Offset = 3A040h) [reset = 0h]

Short Description: TxPauseFrames

Long Description: Total number of pause frames transmitted

Return to Summary Table

Offset = 3a040h + (j * 200h); where j = 0h to 2h

Table 4-2525. Instance Table

Instance Name	Physical Address
CPSW	5283 A040h

Figure 4-1175. CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXPAUSEFRAMES_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2526. CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXPAUSEFRAMES_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of pause frames transmitted

4.18.348 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXDEFERREDFRAMES_J Registers

4.18.348.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXDEFERREDFRAMES_J Register (Offset = 3A044h) [reset = 0h]

Short Description: TxDeferredFrames

Long Description: Total number of deferred frames transmitted

Return to Summary Table

Offset = 3a044h + (j * 200h); where j = 0h to 2h

Table 4-2527. Instance Table

Instance Name	Physical Address
CPSW	5283 A044h

Figure 4-1176. CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXDEFERREDFRAMES_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2528. CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXDEFERREDFRAMES_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of deferred frames transmitted

4.18.349 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXCOLLISIONFRAMES_J Registers

4.18.349.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXCOLLISIONFRAMES_J Register (Offset = 3A048h) [reset = 0h]

Short Description: TxCollisionFrames

Long Description: Total number of transmitted frames experiencing a collision

Return to Summary Table

Offset = 3a048h + (j * 200h); where j = 0h to 2h

Table 4-2529. Instance Table

Instance Name	Physical Address
CPSW	5283 A048h

Figure 4-1177. CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXCOLLISIONFRAMES_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2530. CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXCOLLISIONFRAMES_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of transmitted frames experiencing a collision

4.18.350 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXSINGLECOLLFRAMES_J Registers

4.18.350.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXSINGLECOLLFRAMES_J Register (Offset = 3A04Ch) [reset = 0h]

Short Description: TxSingleCollFrames

Long Description: Total number of transmitted frames experiencing a single collision

Return to Summary Table

Offset = 3a04ch + (j * 200h); where j = 0h to 2h

Table 4-2531. Instance Table

Instance Name	Physical Address
CPSW	5283 A04Ch

Figure 4-1178. CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXSINGLECOLLFRAMES_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2532. CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXSINGLECOLLFRAMES_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of transmitted frames experiencing a single collision

4.18.351 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXMULTCOLLFRAMES_J Registers

4.18.351.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXMULTCOLLFRAMES_J Register (Offset = 3A050h) [reset = 0h]

Short Description: TxMultCollFrames

Long Description: Total number of transmitted frames experiencing multiple collisions

Return to Summary Table

Offset = 3a050h + (j * 200h); where j = 0h to 2h

Table 4-2533. Instance Table

Instance Name	Physical Address
CPSW	5283 A050h

Figure 4-1179. CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXMULTCOLLFRAMES_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2534. CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXMULTCOLLFRAMES_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of transmitted frames experiencing multiple collisions

4.18.352 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXEXCESSIVECOLLISIONS_J Registers

4.18.352.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXEXCESSIVECOLLISIONS_J Register (Offset = 3A054h) [reset = 0h]

Short Description: TxExcessiveCollisions

Long Description: Total number of transmitted frames abandoned due to excessive collisions

Return to Summary Table

Offset = 3a054h + (j * 200h); where j = 0h to 2h

Table 4-2535. Instance Table

Instance Name	Physical Address
CPSW	5283 A054h

Figure 4-1180. CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXEXCESSIVECOLLISIONS_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2536. CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXEXCESSIVECOLLISIONS_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of transmitted frames abandoned due to excessive collisions

4.18.353 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXLATECOLLISIONS_J Registers

4.18.353.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXLATECOLLISIONS_J Register (Offset = 3A058h) [reset = 0h]

Short Description: TxLateCollisions

Long Description: Total number of transmitted frames abandoned due to a late collision

Return to Summary Table

Offset = 3a058h + (j * 200h); where j = 0h to 2h

Table 4-2537. Instance Table

Instance Name	Physical Address
CPSW	5283 A058h

Figure 4-1181. CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXLATECOLLISIONS_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2538. CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXLATECOLLISIONS_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of transmitted frames abandoned due to a late collision

4.18.354 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXIPGERROR_J Registers

4.18.354.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXIPGERROR_J Register (Offset = 3A05Ch) [reset = 0h]

Short Description: RxIPGError

Long Description: Total number of receive inter-packet gap errors (10G only)

Return to Summary Table

Offset = 3a05ch + (j * 200h); where j = 0h to 2h

Table 4-2539. Instance Table

Instance Name	Physical Address
CPSW	5283 A05Ch

Figure 4-1182. CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXIPGERROR_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2540. CPSW_NC_CPSW_NC_CPSW_NC_STAT_RXIPGERROR_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of receive inter-packet gap errors (10G only)

4.18.355 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXCARRIERSENSEERRORS_J Registers

4.18.355.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXCARRIERSENSEERRORS_J Register (Offset = 3A060h) [reset = 0h]

Short Description: TxCarrierSenseErrors

Long Description: Total number of transmitted frames that experienced a carrier loss

Return to Summary Table

Offset = 3a060h + (j * 200h); where j = 0h to 2h

Table 4-2541. Instance Table

Instance Name	Physical Address
CPSW	5283 A060h

Figure 4-1183. CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXCARRIERSENSEERRORS_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2542. CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXCARRIERSENSEERRORS_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of transmitted frames that experienced a carrier loss

4.18.356 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXOCTETS_J Registers

4.18.356.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXOCTETS_J Register (Offset = 3A064h) [reset = 0h]

Short Description: TxOctets

Long Description: Total number of bytes in all good frames transmitted

Return to Summary Table

Offset = 3a064h + (j * 200h); where j = 0h to 2h

Table 4-2543. Instance Table

Instance Name	Physical Address
CPSW	5283 A064h

Figure 4-1184. CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXOCTETS_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2544. CPSW_NC_CPSW_NC_CPSW_NC_STAT_TXOCTETS_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of bytes in all good frames transmitted

4.18.357 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_OCTETFRAMES64_J Registers

4.18.357.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_OCTETFRAMES64_J Register (Offset = 3A068h) [reset = 0h]

Short Description: OctetFrames64

Long Description: Total number of 64-byte frames received and transmitted

Return to Summary Table

Offset = 3a068h + (j * 200h); where j = 0h to 2h

Table 4-2545. Instance Table

Instance Name	Physical Address
CPSW	5283 A068h

Figure 4-1185. CPSW_NC_CPSW_NC_CPSW_NC_STAT_OCTETFRAMES64_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2546. CPSW_NC_CPSW_NC_CPSW_NC_STAT_OCTETFRAMES64_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of 64-byte frames received and transmitted

4.18.358 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_OCTETFRAMES65T127_J Registers

4.18.358.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_OCTETFRAMES65T127_J Register (Offset = 3A06Ch) [reset = 0h]

Short Description: OctetFrames65t127

Long Description: Total number of frames of size 65 to 127 bytes received and transmitted

Return to Summary Table

Offset = 3a06ch + (j * 200h); where j = 0h to 2h

Table 4-2547. Instance Table

Instance Name	Physical Address
CPSW	5283 A06Ch

Figure 4-1186. CPSW_NC_CPSW_NC_CPSW_NC_STAT_OCTETFRAMES65T127_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2548. CPSW_NC_CPSW_NC_CPSW_NC_STAT_OCTETFRAMES65T127_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of frames of size 65 to 127 bytes received and transmitted

4.18.359 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_OCTETFRAMES128T255_J Registers

4.18.359.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_OCTETFRAMES128T255_J Register (Offset = 3A070h) [reset = 0h]

Short Description: OctetFrames128t255

Long Description: Total number of frames of size 128 to 255 bytes received and transmitted

Return to Summary Table

Offset = 3a070h + (j * 200h); where j = 0h to 2h

Table 4-2549. Instance Table

Instance Name	Physical Address
CPSW	5283 A070h

Figure 4-1187. CPSW_NC_CPSW_NC_CPSW_NC_STAT_OCTETFRAMES128T255_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2550. CPSW_NC_CPSW_NC_CPSW_NC_STAT_OCTETFRAMES128T255_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of frames of size 128 to 255 bytes received and transmitted

4.18.360 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_OCTETFRAMES256T511_J Registers

4.18.360.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_OCTETFRAMES256T511_J Register (Offset = 3A074h) [reset = 0h]

Short Description: OctetFrames256t511

Long Description: Total number of frames of size 256 to 511 bytes received and transmitted

Return to Summary Table

Offset = 3a074h + (j * 200h); where j = 0h to 2h

Table 4-2551. Instance Table

Instance Name	Physical Address
CPSW	5283 A074h

Figure 4-1188. CPSW_NC_CPSW_NC_CPSW_NC_STAT_OCTETFRAMES256T511_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2552. CPSW_NC_CPSW_NC_CPSW_NC_STAT_OCTETFRAMES256T511_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of frames of size 256 to 511 bytes received and transmitted

4.18.361 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_OCTETFRAMES512T1023_J Registers

4.18.361.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_OCTETFRAMES512T1023_J Register (Offset = 3A078h) [reset = 0h]

Short Description: OctetFrames512t1023

Long Description: Total number of frames of size 512 to 1023 bytes received and transmitted

Return to Summary Table

Offset = 3a078h + (j * 200h); where j = 0h to 2h

Table 4-2553. Instance Table

Instance Name	Physical Address
CPSW	5283 A078h

Figure 4-1189. CPSW_NC_CPSW_NC_CPSW_NC_STAT_OCTETFRAMES512T1023_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2554. CPSW_NC_CPSW_NC_CPSW_NC_STAT_OCTETFRAMES512T1023_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of frames of size 512 to 1023 bytes received and transmitted

4.18.362 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_OCTETFRAMES1024TUP_J Registers

4.18.362.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_OCTETFRAMES1024TUP_J Register (Offset = 3A07Ch) [reset = 0h]

Short Description: OctetFrames1024tUP

Long Description: Total number of frames of size 1024 to rx_maxlen bytes received and 1024 bytes or greater transmitted

Return to Summary Table

Offset = 3a07ch + (j * 200h); where j = 0h to 2h

Table 4-2555. Instance Table

Instance Name	Physical Address
CPSW	5283 A07Ch

Figure 4-1190. CPSW_NC_CPSW_NC_CPSW_NC_STAT_OCTETFRAMES1024TUP_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2556. CPSW_NC_CPSW_NC_CPSW_NC_STAT_OCTETFRAMES1024TUP_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of frames of size 1024 to rx_maxlen bytes received and 1024 bytes or greater transmitted

4.18.363 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_NETOCTETS_J Registers

4.18.363.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_NETOCTETS_J Register (Offset = 3A080h) [reset = 0h]

Short Description: NetOctets

Long Description: Total number of bytes received and transmitted

Return to Summary Table

Offset = 3a080h + (j * 200h); where j = 0h to 2h

Table 4-2557. Instance Table

Instance Name	Physical Address
CPSW	5283 A080h

Figure 4-1191. CPSW_NC_CPSW_NC_CPSW_NC_STAT_NETOCTETS_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2558. CPSW_NC_CPSW_NC_CPSW_NC_STAT_NETOCTETS_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of bytes received and transmitted

4.18.364 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_RX_BOTTOM_OF_FIFO_DROP_J Registers

4.18.364.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_RX_BOTTOM_OF_FIFO_DROP_J Register (Offset = 3A084h) [reset = 0h]

Short Description: Rx_Bottom_of_FIFO_Drop

Long Description: Receive Bottom of FIFO Drop

Return to Summary Table

Offset = 3a084h + (j * 200h); where j = 0h to 2h

Table 4-2559. Instance Table

Instance Name	Physical Address
CPSW	5283 A084h

Figure 4-1192. CPSW_NC_CPSW_NC_CPSW_NC_STAT_RX_BOTTOM_OF_FIFO_DROP_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2560. CPSW_NC_CPSW_NC_CPSW_NC_STAT_RX_BOTTOM_OF_FIFO_DROP_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Receive Bottom of FIFO Drop

4.18.365 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_PORTMASK_DROP_J Registers

4.18.365.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_PORTMASK_DROP_J Register (Offset = 3A088h) [reset = 0h]

Short Description: Portmask_Drop

Long Description: Total number of dropped frames received due to portmask

Return to Summary Table

Offset = 3a088h + (j * 200h); where j = 0h to 2h

Table 4-2561. Instance Table

Instance Name	Physical Address
CPSW	5283 A088h

Figure 4-1193. CPSW_NC_CPSW_NC_CPSW_NC_STAT_PORTMASK_DROP_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2562. CPSW_NC_CPSW_NC_CPSW_NC_STAT_PORTMASK_DROP_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of dropped frames received due to portmask

4.18.366 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_RX_TOP_OF_FIFO_DROP_J Registers

4.18.366.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_RX_TOP_OF_FIFO_DROP_J Register (Offset = 3A08Ch) [reset = 0h]

Short Description: Rx_Top_of_FIFO_Drop

Long Description: Receive Top of FIFO Drop

Return to Summary Table

Offset = 3a08ch + (j * 200h); where j = 0h to 2h

Table 4-2563. Instance Table

Instance Name	Physical Address
CPSW	5283 A08Ch

Figure 4-1194. CPSW_NC_CPSW_NC_CPSW_NC_STAT_RX_TOP_OF_FIFO_DROP_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2564. CPSW_NC_CPSW_NC_CPSW_NC_STAT_RX_TOP_OF_FIFO_DROP_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Receive Top of FIFO Drop

4.18.367 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_RATE_LIMIT_DROP_J Registers

4.18.367.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_RATE_LIMIT_DROP_J Register (Offset = 3A090h) [reset = 0h]

Short Description: ALE_Rate_Limit_Drop

Long Description: Total number of dropped frames due to ALE Rate Limiting

Return to Summary Table

Offset = 3a090h + (j * 200h); where j = 0h to 2h

Table 4-2565. Instance Table

Instance Name	Physical Address
CPSW	5283 A090h

Figure 4-1195. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_RATE_LIMIT_DROP_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2566. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_RATE_LIMIT_DROP_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of dropped frames due to ALE Rate Limiting

4.18.368 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_VID_INGRESS_DROP_J Registers

4.18.368.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_VID_INGRESS_DROP_J Register (Offset = 3A094h) [reset = 0h]

Short Description: ALE_VID_Ingress_Drop

Long Description: Total number of dropped frames due to ALE VID Ingress

Return to Summary Table

Offset = 3a094h + (j * 200h); where j = 0h to 2h

Table 4-2567. Instance Table

Instance Name	Physical Address
CPSW	5283 A094h

Figure 4-1196. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_VID_INGRESS_DROP_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2568. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_VID_INGRESS_DROP_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of dropped frames due to ALE VID Ingress

4.18.369 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_DA_EQ_SA_DROP_J Registers

4.18.369.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_DA_EQ_SA_DROP_J Register (Offset = 3A098h) [reset = 0h]

Short Description: ALE_DA_EQ_SA_Drop

Long Description: Total number of dropped frames due to DA=SA

Return to Summary Table

Offset = 3a098h + (j * 200h); where j = 0h to 2h

Table 4-2569. Instance Table

Instance Name	Physical Address
CPSW	5283 A098h

Figure 4-1197. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_DA_EQ_SA_DROP_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2570. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_DA_EQ_SA_DROP_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of dropped frames due to DA=SA

4.18.370 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_BLOCK_DROP_J Registers

4.18.370.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_BLOCK_DROP_J Register (Offset = 3A09Ch) [reset = 0h]

Short Description: ALE_Block_Drop

Long Description: Total number of dropped frames due to ALE Block Mode

Return to Summary Table

Offset = 3a09ch + (j * 200h); where j = 0h to 2h

Table 4-2571. Instance Table

Instance Name	Physical Address
CPSW	5283 A09Ch

Figure 4-1198. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_BLOCK_DROP_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2572. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_BLOCK_DROP_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of dropped frames due to ALE Block Mode

4.18.371 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_SECURE_DROP_J Registers

4.18.371.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_SECURE_DROP_J Register (Offset = 3A0A0h) [reset = 0h]

Short Description: ALE_Secure_Drop

Long Description: Total number of dropped frames due to ALE Secure Mode

Return to Summary Table

Offset = 3a0a0h + (j * 200h); where j = 0h to 2h

Table 4-2573. Instance Table

Instance Name	Physical Address
CPSW	5283 A0A0h

Figure 4-1199. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_SECURE_DROP_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2574. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_SECURE_DROP_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of dropped frames due to ALE Secure Mode

4.18.372 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_AUTH_DROP_J Registers

4.18.372.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_AUTH_DROP_J Register (Offset = 3A0A4h) [reset = 0h]

Short Description: ALE_Auth_Drop

Long Description: Total number of dropped frames due to ALE Authentication

Return to Summary Table

Offset = 3a0a4h + (j * 200h); where j = 0h to 2h

Table 4-2575. Instance Table

Instance Name	Physical Address
CPSW	5283 A0A4h

Figure 4-1200. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_AUTH_DROP_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2576. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_AUTH_DROP_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of dropped frames due to ALE Authentication

4.18.373 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_UNKN_UNI_J Registers

4.18.373.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_UNKN_UNI_J Register (Offset = 3A0A8h) [reset = 0h]

Short Description: ALE_Unkn_Uni

Long Description: ALE Receive Unknown Unicast

Return to Summary Table

Offset = 3a0a8h + (j * 200h); where j = 0h to 2h

Table 4-2577. Instance Table

Instance Name	Physical Address
CPSW	5283 A0A8h

Figure 4-1201. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_UNKN_UNI_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2578. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_UNKN_UNI_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Receive Unknown Unicast

4.18.374 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_UNKN_UNI_BCNT_J Registers

4.18.374.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_UNKN_UNI_BCNT_J Register (Offset = 3A0ACh) [reset = 0h]

Short Description: ALE_Unkn_Uni_Bcnt

Long Description: ALE Receive Unknown Unicast Bytecount

Return to Summary Table

Offset = 3a0ach + (j * 200h); where j = 0h to 2h

Table 4-2579. Instance Table

Instance Name	Physical Address
CPSW	5283 A0ACh

Figure 4-1202. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_UNKN_UNI_BCNT_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2580. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_UNKN_UNI_BCNT_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Receive Unknown Unicast Bytecount

4.18.375 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_UNKN_MLT_J Registers

4.18.375.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_UNKN_MLT_J Register (Offset = 3A0B0h) [reset = 0h]

Short Description: ALE_Unkn_Mlt

Long Description: ALE Receive Unknown Multicast

Return to Summary Table

Offset = 3a0b0h + (j * 200h); where j = 0h to 2h

Table 4-2581. Instance Table

Instance Name	Physical Address
CPSW	5283 A0B0h

Figure 4-1203. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_UNKN_MLT_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2582. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_UNKN_MLT_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Receive Unknown Multicast

4.18.376 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_UNKN_MLT_BCNT_J Registers

4.18.376.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_UNKN_MLT_BCNT_J Register (Offset = 3A0B4h) [reset = 0h]

Short Description: ALE_Unkn_Mlt_Bcnt

Long Description: ALE Receive Unknown Multicast Bytecount

Return to Summary Table

Offset = 3a0b4h + (j * 200h); where j = 0h to 2h

Table 4-2583. Instance Table

Instance Name	Physical Address
CPSW	5283 A0B4h

Figure 4-1204. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_UNKN_MLT_BCNT_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2584. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_UNKN_MLT_BCNT_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Receive Unknown Multicast Bytecount

4.18.377 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_UNKN_BRD_J Registers

4.18.377.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_UNKN_BRD_J Register (Offset = 3A0B8h) [reset = 0h]

Short Description: ALE_Unkn_Brd

Long Description: ALE Receive Unknown Broadcast

Return to Summary Table

Offset = 3a0b8h + (j * 200h); where j = 0h to 2h

Table 4-2585. Instance Table

Instance Name	Physical Address
CPSW	5283 A0B8h

Figure 4-1205. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_UNKN_BRD_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2586. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_UNKN_BRD_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Receive Unknown Broadcast

4.18.378 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_UNKN_BRD_BCNT_J Registers

4.18.378.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_UNKN_BRD_BCNT_J Register (Offset = 3A0BCh) [reset = 0h]

Short Description: ALE_Unkn_Brd_Bcnt

Long Description: ALE Receive Unknown Broadcast Bytecount

Return to Summary Table

Offset = 3a0bch + (j * 200h); where j = 0h to 2h

Table 4-2587. Instance Table

Instance Name	Physical Address
CPSW	5283 A0BCh

Figure 4-1206. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_UNKN_BRD_BCNT_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2588. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_UNKN_BRD_BCNT_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Receive Unknown Broadcast Bytecount

4.18.379 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_POL_MATCH_J Registers

4.18.379.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_POL_MATCH_J Register (Offset = 3A0C0h) [reset = 0h]

Short Description: ALE_Pol_Match

Long Description: ALE Policer Matched

Return to Summary Table

Offset = 3a0c0h + (j * 200h); where j = 0h to 2h

Table 4-2589. Instance Table

Instance Name	Physical Address
CPSW	5283 A0C0h

Figure 4-1207. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_POL_MATCH_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2590. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_POL_MATCH_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Policer Matched

4.18.380 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_POL_MATCH_RED_J Registers

4.18.380.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_POL_MATCH_RED_J Register (Offset = 3A0C4h) [reset = 0h]

Short Description: ALE_Pol_Match_Red

Long Description: ALE Policer Matched and Condition Red

Return to Summary Table

Offset = 3a0c4h + (j * 200h); where j = 0h to 2h

Table 4-2591. Instance Table

Instance Name	Physical Address
CPSW	5283 A0C4h

Figure 4-1208. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_POL_MATCH_RED_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2592. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_POL_MATCH_RED_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Policer Matched and Condition Red

4.18.381 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_POL_MATCH_YELLOW_J Registers

4.18.381.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_POL_MATCH_YELLOW_J Register (Offset = 3A0C8h) [reset = 0h]

Short Description: ALE_Pol_Match_Yellow

Long Description: ALE Policer Matched and Condition Yellow

Return to Summary Table

Offset = 3a0c8h + (j * 200h); where j = 0h to 2h

Table 4-2593. Instance Table

Instance Name	Physical Address
CPSW	5283 A0C8h

Figure 4-1209. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_POL_MATCH_YELLOW_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2594. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_POL_MATCH_YELLOW_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Policer Matched and Condition Yellow

4.18.382 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_MULT_SA_DROP_J Registers

4.18.382.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_MULT_SA_DROP_J Register (Offset = 3A0CCh) [reset = 0h]

Short Description: ALE_MULT_SA_DROP

Long Description: ALE Multicast Source Address Drop

Return to Summary Table

Offset = 3a0cch + (j * 200h); where j = 0h to 2h

Table 4-2595. Instance Table

Instance Name	Physical Address
CPSW	5283 A0CCh

Figure 4-1210. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_MULT_SA_DROP_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2596. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_MULT_SA_DROP_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Multicast Source Address drop

4.18.383 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_DUAL_VLAN_DROP_J Registers

4.18.383.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_DUAL_VLAN_DROP_J Register (Offset = 3A0D0h) [reset = 0h]

Short Description: ALE_DUAL_VLAN_DROP

Long Description: ALE Dual VLAN Drop

Return to Summary Table

Offset = 3a0d0h + (j * 200h); where j = 0h to 2h

Table 4-2597. Instance Table

Instance Name	Physical Address
CPSW	5283 A0D0h

Figure 4-1211. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_DUAL_VLAN_DROP_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2598. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_DUAL_VLAN_DROP_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Dual VLAN drop

4.18.384 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_LEN_ERROR_DROP_J Registers

4.18.384.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_LEN_ERROR_DROP_J Register (Offset = 3A0D4h) [reset = 0h]

Short Description: ALE_LEN_ERROR_DROP

Long Description: ALE Length Error Drop

Return to Summary Table

Offset = 3a0d4h + (j * 200h); where j = 0h to 2h

Table 4-2599. Instance Table

Instance Name	Physical Address
CPSW	5283 A0D4h

Figure 4-1212. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_LEN_ERROR_DROP_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2600. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_LEN_ERROR_DROP_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Length Error drop

4.18.385 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_IP_NEXT_HDR_DROP_J Registers

4.18.385.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_IP_NEXT_HDR_DROP_J Register (Offset = 3A0D8h) [reset = 0h]

Short Description: ALE_IP_NEXT_HDR_DROP

Long Description: ALE IP Next Header Drop

Return to Summary Table

Offset = 3a0d8h + (j * 200h); where j = 0h to 2h

Table 4-2601. Instance Table

Instance Name	Physical Address
CPSW	5283 A0D8h

Figure 4-1213. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_IP_NEXT_HDR_DROP_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2602. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_IP_NEXT_HDR_DROP_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Next Header drop

4.18.386 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_IPV4_FRAG_DROP_J Registers

4.18.386.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_IPV4_FRAG_DROP_J Register (Offset = 3A0DCh) [reset = 0h]

Short Description: ALE_IPV4_FRAG_DROP

Long Description: ALE IPV4 Frag Drop

Return to Summary Table

Offset = 3a0dch + (j * 200h); where j = 0h to 2h

Table 4-2603. Instance Table

Instance Name	Physical Address
CPSW	5283 A0DCh

Figure 4-1214. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_IPV4_FRAG_DROP_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0h															

Access Types Legend

Table 4-2604. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ALE_IPV4_FRAG_DROP_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE IPV4 Fragment drop

4.18.387 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_TX_MEMORY_PROTECT_ERROR_J Registers

4.18.387.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_TX_MEMORY_PROTECT_ERROR_J Register (Offset = 3A17Ch) [reset = 0h]

Short Description: Tx_Memory_Protect_Error

Long Description: Transmit Memory Protect CRC Error

Return to Summary Table

Offset = 3a17ch + (j * 200h); where j = 0h to 2h

Table 4-2605. Instance Table

Instance Name	Physical Address
CPSW	5283 A17Ch

Figure 4-1215. CPSW_NC_CPSW_NC_CPSW_NC_STAT_TX_MEMORY_PROTECT_ERROR_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COUNT							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-2606. CPSW_NC_CPSW_NC_CPSW_NC_STAT_TX_MEMORY_PROTECT_ERROR_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	COUNT	R/W	0h	Transmit Memory Protect CRC Error

4.18.388 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ENET_PN_TX_PRI_REG_J_N Registers

4.18.388.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ENET_PN_TX_PRI_REG_J_N Register (Offset = 3A180h) [reset = 0h]

Short Description: enet_pn_tx_pri

Long Description: ENET Port n PRIORITY N Packet Count

Return to Summary Table

Offset = 3a180h + (j * 4h); where j = 0h to 7h

Table 4-2607. Instance Table

Instance Name	Physical Address
CPSW	5283 A180h

Figure 4-1216. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ENET_PN_TX_PRI_REG_J_N Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PN_TX_PRIN															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PN_TX_PRIN															
R/W															
0h															

Access Types Legend

Table 4-2608. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ENET_PN_TX_PRI_REG_J_N Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PN_TX_PRIN	R/W	0h	ENET TX Priority Packet Count

4.18.389 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ENET_PN_TX_PRI_BCNT_REG_J_N Registers

4.18.389.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ENET_PN_TX_PRI_BCNT_REG_J_N Register (Offset = 3A1A0h) [reset = 0h]

Short Description: enet_pn_tx_pri_bcnt

Long Description: ENET Port n PRIORITY N Packet Byte Count

Return to Summary Table

Offset = 3a1a0h + (j * 4h); where j = 0h to 7h

Table 4-2609. Instance Table

Instance Name	Physical Address
CPSW	5283 A1A0h

Figure 4-1217. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ENET_PN_TX_PRI_BCNT_REG_J_N Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PN_TX_PRIN_BCNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PN_TX_PRIN_BCNT															
R/W															
0h															

Access Types Legend

Table 4-2610. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ENET_PN_TX_PRI_BCNT_REG_J_N Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PN_TX_PRIN_BCNT	R/W	0h	ENET Port n PRIORITY N Packet Byte Count

4.18.390 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ENET_PN_TX_PRI_DROP_REG_J_N Registers

4.18.390.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ENET_PN_TX_PRI_DROP_REG_J_N Register (Offset = 3A1C0h) [reset = 0h]

Short Description: enet_pn_tx_pri_drop

Long Description: ENET Port n PRIORITY N Packet Drop Count

Return to Summary Table

Offset = 3a1c0h + (j * 4h); where j = 0h to 7h

Table 4-2611. Instance Table

Instance Name	Physical Address
CPSW	5283 A1C0h

Figure 4-1218. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ENET_PN_TX_PRI_DROP_REG_J_N Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PN_TX_PRIN_DROP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PN_TX_PRIN_DROP															
R/W															
0h															

Access Types Legend

Table 4-2612. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ENET_PN_TX_PRI_DROP_REG_J_N Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PN_TX_PRIN_DROP	R/W	0h	ENET Port n PRIORITY N Packet Drop Count

4.18.391 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ENET_PN_TX_PRI_DROP_BCNT_REG_J_N Registers

4.18.391.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPSW_NC_STAT_ENET_PN_TX_PRI_DROP_BCNT_REG_J_N Register (Offset = 3A1E0h) [reset = 0h]

Short Description: enet_pn_tx_pri_drop_bcnt

Long Description: ENET Port n PRIORITY N Packet Drop Byte Count

Return to Summary Table

Offset = 3a1e0h + (j * 4h); where j = 0h to 7h

Table 4-2613. Instance Table

Instance Name	Physical Address
CPSW	5283 A1E0h

Figure 4-1219. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ENET_PN_TX_PRI_DROP_BCNT_REG_J_N Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PN_TX_PRIN_DROP_BCNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PN_TX_PRIN_DROP_BCNT															
R/W															
0h															

Access Types Legend

Table 4-2614. CPSW_NC_CPSW_NC_CPSW_NC_STAT_ENET_PN_TX_PRI_DROP_BCNT_REG_J_N Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PN_TX_PRIN_DROP_BCNT	R/W	0h	ENET Port n PRIORITY N Packet Drop Byte Count

4.18.392 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_IDVER_REG Registers

4.18.392.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_IDVER_REG Register (Offset = 3D000h) [reset = 4e8a010ch]

Short Description: idver_reg

Long Description: Identification and Version Register

Return to Summary Table

Table 4-2615. Instance Table

Instance Name	Physical Address
CPSW	5283 D000h

Figure 4-1220. CPSW_NC_CPSW_NC_CPTS_IDVER_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TX_IDENT															
R															
4e8ah															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL_VER					MAJOR_VER			MINOR_VER							
R					R			R							
0h					1h			ch							

Access Types Legend

Table 4-2616. CPSW_NC_CPSW_NC_CPTS_IDVER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TX_IDENT	R	4E8Ah	Identification value
15:11	RTL_VER	R	0h	RTL version value
10:8	MAJOR_VER	R	1h	Major version value
7:0	MINOR_VER	R	Ch	Minor version value

4.18.393 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_CONTROL_REG Registers

4.18.393.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_CONTROL_REG Register (Offset = 3D004h) [reset = 4h]

Short Description: control_reg

Long Description: Time Sync Control Register

Return to Summary Table

Table 4-2617. Instance Table

Instance Name	Physical Address
CPSW	5283 D004h

Figure 4-1221. CPSW_NC_CPSW_NC_CPTS_CONTROL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TS_SYNC_SEL				RESERVED										TS_GENF_CLR_EN	TS_RX_NO_EVENT
R/W				NONE										R/W	R/W
0h				0										0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW8_TS_PUSH_EN	HW7_TS_PUSH_EN	HW6_TS_PUSH_EN	HW5_TS_PUSH_EN	HW4_TS_PUSH_EN	HW3_TS_PUSH_EN	HW2_TS_PUSH_EN	HW1_TS_PUSH_EN	TS_PPM_DIR	TS_COMP_TOG	MODE	SEQUENCE_EN	TSTAMP_EN	TS_COMP_POLARITY	INT_TEST	CPTS_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	1h	0h	0h

Access Types Legend

Table 4-2618. CPSW_NC_CPSW_NC_CPTS_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	TS_SYNC_SEL	R/W	0h	TS_SYNC output timestamp counter bit select
27:18	RESERVED	NONE		Reserved
17	TS_GENF_CLR_EN	R/W	0h	Enable for GENF clear when length is zero
16	TS_RX_NO_EVENT	R/W	0h	Receive Produces no Events
15	HW8_TS_PUSH_EN	R/W	0h	Hardware push 8 enable
14	HW7_TS_PUSH_EN	R/W	0h	Hardware push 7 enable
13	HW6_TS_PUSH_EN	R/W	0h	Hardware push 6 enable
12	HW5_TS_PUSH_EN	R/W	0h	Hardware push 5 enable
11	HW4_TS_PUSH_EN	R/W	0h	Hardware push 4 enable
10	HW3_TS_PUSH_EN	R/W	0h	Hardware push 3 enable
9	HW2_TS_PUSH_EN	R/W	0h	Hardware push 2 enable
8	HW1_TS_PUSH_EN	R/W	0h	Hardware push 1 enable
7	TS_PPM_DIR	R/W	0h	Timestamp PPM Direction
6	TS_COMP_TOG	R/W	0h	Timestamp Compare Toggle mode: 0=TS_COMP is in non-toggle mode, 1=TS_COMP is in toggle mode
5	MODE	R/W	0h	Timestamp mode
4	SEQUENCE_EN	R/W	0h	Sequence Enable
3	TSTAMP_EN	R/W	0h	Host Receive Timestamp Enable
2	TS_COMP_POLARITY	R/W	1h	TS_COMP polarity
1	INT_TEST	R/W	0h	Interrupt test

Table 4-2618. CPSW_NC_CPSW_NC_CPTS_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CPTS_EN	R/W	0h	Time sync enable

4.18.394 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_RFTCLK_SEL_REG Registers

4.18.394.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_RFTCLK_SEL_REG Register (Offset = 3D008h) [reset = 0h]

Short Description: rftclk_sel_reg

Long Description: RFTCLK Select Register

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Table 4-2619. Instance Table

Instance Name	Physical Address
CPSW	5283 D008h

Figure 4-1222. CPSW_NC_CPSW_NC_CPTS_RFTCLK_SEL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											RFTCLK_SEL				
NONE											R/W				
0											0h				

Access Types Legend

Table 4-2620. CPSW_NC_CPSW_NC_CPTS_RFTCLK_SEL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	RFTCLK_SEL	R/W	0h	Reference clock select

4.18.395 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_PUSH_REG Registers

4.18.395.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_PUSH_REG Register (Offset = 3D00Ch) [reset = 0h]

Short Description: ts_push_reg

Long Description: Time Stamp Event Push Register

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Table 4-2621. Instance Table

Instance Name	Physical Address
CPSW	5283 D00Ch

Figure 4-1223. CPSW_NC_CPSW_NC_CPTS_TS_PUSH_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															TS_PUSH
NONE															W
0															0h

Access Types Legend

Table 4-2622. CPSW_NC_CPSW_NC_CPTS_TS_PUSH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	TS_PUSH	W	0h	Time stamp event push

4.18.396 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_LOAD_VAL_REG Registers

4.18.396.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_LOAD_VAL_REG Register (Offset = 3D010h) [reset = 0h]

Short Description: ts_load_low_val_reg

Long Description: Time Stamp Load Low Value Register

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Table 4-2623. Instance Table

Instance Name	Physical Address
CPSW	5283 D010h

Figure 4-1224. CPSW_NC_CPSW_NC_CPTS_TS_LOAD_VAL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TS_LOAD_VAL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_LOAD_VAL															
R/W															
0h															

Access Types Legend

Table 4-2624. CPSW_NC_CPSW_NC_CPTS_TS_LOAD_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_LOAD_VAL	R/W	0h	Time stamp load low value

4.18.397 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_LOAD_EN_REG Registers

4.18.397.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_LOAD_EN_REG Register (Offset = 3D014h) [reset = 0h]

Short Description: ts_load_en_reg

Long Description: Time Stamp Load Enable Register

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Table 4-2625. Instance Table

Instance Name	Physical Address
CPSW	5283 D014h

Figure 4-1225. CPSW_NC_CPSW_NC_CPTS_TS_LOAD_EN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															TS_LOAD_EN
NONE															W
0															0h

Access Types Legend

Table 4-2626. CPSW_NC_CPSW_NC_CPTS_TS_LOAD_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	TS_LOAD_EN	W	0h	Time stamp load enable

4.18.398 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_COMP_VAL_REG Registers

4.18.398.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_COMP_VAL_REG Register (Offset = 3D018h) [reset = 0h]

Short Description: ts_comp_low_val_reg

Long Description: Time Stamp Comparison Low Value Register

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Table 4-2627. Instance Table

Instance Name	Physical Address
CPSW	5283 D018h

Figure 4-1226. CPSW_NC_CPSW_NC_CPTS_TS_COMP_VAL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TS_COMP_VAL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_COMP_VAL															
R/W															
0h															

Access Types Legend

Table 4-2628. CPSW_NC_CPSW_NC_CPTS_TS_COMP_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_COMP_VAL	R/W	0h	Time stamp comparison low value

4.18.399 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_COMP_LEN_REG Registers

4.18.399.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_COMP_LEN_REG Register (Offset = 3D01Ch) [reset = 0h]

Short Description: ts_comp_len_reg

Long Description: Time Stamp Comparison Length Register

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Table 4-2629. Instance Table

Instance Name	Physical Address
CPSW	5283 D01Ch

Figure 4-1227. CPSW_NC_CPSW_NC_CPTS_TS_COMP_LEN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TS_COMP_LENGTH															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_COMP_LENGTH															
R/W															
0h															

Access Types Legend

Table 4-2630. CPSW_NC_CPSW_NC_CPTS_TS_COMP_LEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_COMP_LENGTH	R/W	0h	Time stamp comparison length

4.18.400 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_INTSTAT_RAW_REG Registers

4.18.400.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_INTSTAT_RAW_REG Register (Offset = 3D020h) [reset = 0h]

Short Description: intstat_raw_reg

Long Description: Interrupt Status Register Raw

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Table 4-2631. Instance Table

Instance Name	Physical Address
CPSW	5283 D020h

Figure 4-1228. CPSW_NC_CPSW_NC_CPTS_INTSTAT_RAW_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															TS_PEND_RAW
NONE															R/W
0															0h

Access Types Legend

Table 4-2632. CPSW_NC_CPSW_NC_CPTS_INTSTAT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	TS_PEND_RAW	R/W	0h	TS_PEND_RAW int read (before enable)

4.18.401 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_INTSTAT_MASKED_REG Registers

4.18.401.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_INTSTAT_MASKED_REG Register (Offset = 3D024h) [reset = 0h]

Short Description: intstat_masked_reg

Long Description: Interrupt Status Register Masked

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Table 4-2633. Instance Table

Instance Name	Physical Address
CPSW	5283 D024h

Figure 4-1229. CPSW_NC_CPSW_NC_CPTS_INTSTAT_MASKED_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															TS_PEND
NONE															R
0															0h

Access Types Legend

Table 4-2634. CPSW_NC_CPSW_NC_CPTS_INTSTAT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	TS_PEND	R	0h	TS_PEND masked interrupt read (after enable)

4.18.402 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_INT_ENABLE_REG Registers

4.18.402.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_INT_ENABLE_REG Register (Offset = 3D028h) [reset = 0h]

Short Description: int_enable_reg

Long Description: Interrupt Enable Register

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Table 4-2635. Instance Table

Instance Name	Physical Address
CPSW	5283 D028h

Figure 4-1230. CPSW_NC_CPSW_NC_CPTS_INT_ENABLE_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															TS_PEND_EN
NONE															R/W
0															0h

Access Types Legend

Table 4-2636. CPSW_NC_CPSW_NC_CPTS_INT_ENABLE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	TS_PEND_EN	R/W	0h	TS_PEND masked interrupt enable

4.18.403 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_COMP_NUDGE_REG Registers

4.18.403.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_COMP_NUDGE_REG Register (Offset = 3D02Ch) [reset = 0h]

Short Description: ts_comp_nudge_reg

Long Description: Time Stamp Comparison Nudge Register

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Table 4-2637. Instance Table

Instance Name	Physical Address
CPSW	5283 D02Ch

Figure 4-1231. CPSW_NC_CPSW_NC_CPTS_TS_COMP_NUDGE_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								NUDGE							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-2638. CPSW_NC_CPSW_NC_CPTS_TS_COMP_NUDGE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	NUDGE	R/W	0h	This 2s complement number is added to the ts_comp_length value to increase or decrease the TS_COMP length by the nudge amount

4.18.404 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_EVENT_POP_REG Registers

4.18.404.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_EVENT_POP_REG Register (Offset = 3D030h) [reset = 0h]

Short Description: event_pop_reg

Long Description: Event Pop Register

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Table 4-2639. Instance Table

Instance Name	Physical Address
CPSW	5283 D030h

Figure 4-1232. CPSW_NC_CPSW_NC_CPTS_EVENT_POP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															EVENT_POP
NONE															W
0															0h

Access Types Legend

Table 4-2640. CPSW_NC_CPSW_NC_CPTS_EVENT_POP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	EVENT_POP	W	0h	Event pop

4.18.405 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_EVENT_0_REG Registers

4.18.405.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_EVENT_0_REG Register (Offset = 3D034h) [reset = 0h]

Short Description: event_0_reg

Long Description: Event 0 Register

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Table 4-2641. Instance Table

Instance Name	Physical Address
CPSW	5283 D034h

Figure 4-1233. CPSW_NC_CPSW_NC_CPTS_EVENT_0_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TIME_STAMP															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIME_STAMP															
R															
0h															

Access Types Legend

Table 4-2642. CPSW_NC_CPSW_NC_CPTS_EVENT_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TIME_STAMP	R	0h	Time Stamp

4.18.406 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_EVENT_1_REG Registers

4.18.406.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_EVENT_1_REG Register (Offset = 3D038h) [reset = 0h]

Short Description: event_1_reg

Long Description: Event 1 Register

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Table 4-2643. Instance Table

Instance Name	Physical Address
CPSW	5283 D038h

Figure 4-1234. CPSW_NC_CPSW_NC_CPTS_EVENT_1_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		PREMPT_QUEUE	PORT_NUMBER					EVENT_TYPE				MESSAGE_TYPE			
NONE		R	R					R				R			
0		0h	0h					0h				0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEQUENCE_ID															
R															
0h															

Access Types Legend

Table 4-2644. CPSW_NC_CPSW_NC_CPTS_EVENT_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE		Reserved
29	PREMPT_QUEUE	R	0h	Prempt QUEUE
28:24	PORT_NUMBER	R	0h	Port number
23:20	EVENT_TYPE	R	0h	Event type
19:16	MESSAGE_TYPE	R	0h	Message type
15:0	SEQUENCE_ID	R	0h	Sequence ID

4.18.407 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_EVENT_2_REG Registers

4.18.407.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_EVENT_2_REG Register (Offset = 3D03Ch) [reset = 0h]

Short Description: event_2_reg

Long Description: Event 2 Register

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Table 4-2645. Instance Table

Instance Name	Physical Address
CPSW	5283 D03Ch

Figure 4-1235. CPSW_NC_CPSW_NC_CPTS_EVENT_2_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DOMAIN							
NONE								R							
0								0h							

Access Types Legend

Table 4-2646. CPSW_NC_CPSW_NC_CPTS_EVENT_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	DOMAIN	R	0h	Domain

4.18.408 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_EVENT_3_REG Registers

4.18.408.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_EVENT_3_REG Register (Offset = 3D040h) [reset = 0h]

Short Description: event_3_reg

Long Description: Event 3 Register

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Table 4-2647. Instance Table

Instance Name	Physical Address
CPSW	5283 D040h

Figure 4-1236. CPSW_NC_CPSW_NC_CPTS_EVENT_3_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TIME_STAMP															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIME_STAMP															
R															
0h															

Access Types Legend

Table 4-2648. CPSW_NC_CPSW_NC_CPTS_EVENT_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TIME_STAMP	R	0h	Time Stamp

4.18.409 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_LOAD_HIGH_VAL_REG Registers

4.18.409.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_LOAD_HIGH_VAL_REG Register (Offset = 3D044h) [reset = 0h]

Short Description: ts_load_high_val_reg

Long Description: Time Stamp Load High Value Register

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Table 4-2649. Instance Table

Instance Name	Physical Address
CPSW	5283 D044h

Figure 4-1237. CPSW_NC_CPSW_NC_CPTS_TS_LOAD_HIGH_VAL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TS_LOAD_VAL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_LOAD_VAL															
R/W															
0h															

Access Types Legend

Table 4-2650. CPSW_NC_CPSW_NC_CPTS_TS_LOAD_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_LOAD_VAL	R/W	0h	Time stamp load high value

4.18.410 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_COMP_HIGH_VAL_REG Registers

4.18.410.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_COMP_HIGH_VAL_REG Register (Offset = 3D048h) [reset = 0h]

Short Description: ts_comp_high_val_reg

Long Description: Time Stamp Comparison High Value Register

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Table 4-2651. Instance Table

Instance Name	Physical Address
CPSW	5283 D048h

Figure 4-1238. CPSW_NC_CPSW_NC_CPTS_TS_COMP_HIGH_VAL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TS_COMP_HIGH_VAL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_COMP_HIGH_VAL															
R/W															
0h															

Access Types Legend

Table 4-2652. CPSW_NC_CPSW_NC_CPTS_TS_COMP_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_COMP_HIGH_VAL	R/W	0h	Time stamp comparison high value

4.18.411 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_ADD_VAL_REG Registers

4.18.411.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_ADD_VAL_REG Register (Offset = 3D04Ch) [reset = 0h]

Short Description: ts_add_val

Long Description: TS Add Value Register

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Table 4-2653. Instance Table

Instance Name	Physical Address
CPSW	5283 D04Ch

Figure 4-1239. CPSW_NC_CPSW_NC_CPTS_TS_ADD_VAL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ADD_VAL		
NONE													R/W		
0													0h		

Access Types Legend

Table 4-2654. CPSW_NC_CPSW_NC_CPTS_TS_ADD_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	ADD_VAL	R/W	0h	Add Value

4.18.412 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_PPM_LOW_VAL_REG Registers

4.18.412.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_PPM_LOW_VAL_REG Register (Offset = 3D050h) [reset = 0h]

Short Description: ts_ppm_low_val_reg

Long Description: Time Stamp PPM Low Value Register

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Table 4-2655. Instance Table

Instance Name	Physical Address
CPSW	5283 D050h

Figure 4-1240. CPSW_NC_CPSW_NC_CPTS_TS_PPM_LOW_VAL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TS_PPM_LOW_VAL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_PPM_LOW_VAL															
R/W															
0h															

Access Types Legend

Table 4-2656. CPSW_NC_CPSW_NC_CPTS_TS_PPM_LOW_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_PPM_LOW_VAL	R/W	0h	Time stamp PPM Low value

4.18.413 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_PPM_HIGH_VAL_REG Registers

4.18.413.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_PPM_HIGH_VAL_REG Register (Offset = 3D054h) [reset = 0h]

Short Description: ts_ppm_high_val_reg

Long Description: Time Stamp PPM High Value Register

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Table 4-2657. Instance Table

Instance Name	Physical Address
CPSW	5283 D054h

Figure 4-1241. CPSW_NC_CPSW_NC_CPTS_TS_PPM_HIGH_VAL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						TS_PPM_HIGH_VAL									
NONE						R/W									
0						0h									

Access Types Legend

Table 4-2658. CPSW_NC_CPSW_NC_CPTS_TS_PPM_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	TS_PPM_HIGH_VAL	R/W	0h	Time stamp PPM High value

4.18.414 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_NUDGE_VAL_REG Registers

4.18.414.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_NUDGE_VAL_REG Register (Offset = 3D058h) [reset = 0h]

Short Description: ts_nudge_val_reg

Long Description: Time Stamp Nudge Value Register

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Table 4-2659. Instance Table

Instance Name	Physical Address
CPSW	5283 D058h

Figure 4-1242. CPSW_NC_CPSW_NC_CPTS_TS_NUDGE_VAL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TS_NUDGE_VAL							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-2660. CPSW_NC_CPSW_NC_CPTS_TS_NUDGE_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	TS_NUDGE_VAL	R/W	0h	Time stamp Nudge value

4.18.415 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_CONFIG Registers

4.18.415.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_CONFIG Register (Offset = 3D0D0h) [reset = 2002h]

Short Description: ts_config

Long Description: Time Stamp Configuration Read

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Table 4-2661. Instance Table

Instance Name	Physical Address
CPSW	5283 D0D0h

Figure 4-1243. CPSW_NC_CPSW_NC_CPTS_TS_CONFIG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
e8d4a51001															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EVNT_FIFO_DEPTH								NUM_GENF							
R								R							
20h								2h							

Access Types Legend

Table 4-2662. CPSW_NC_CPSW_NC_CPTS_TS_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:8	EVNT_FIFO_DEPTH	R	20h	The Event FIFO Depth
7:0	NUM_GENF	R	2h	The number of CPTS GENF outputs

4.18.416 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ALE_MOD_VER Registers

4.18.416.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ALE_MOD_VER Register (Offset = 3E000h) [reset = 290105h]

Short Description: Module and Version

Long Description: The Module and Version Register identifies the module identifier and revision of the ALE_3g512e module.

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Table 4-2663. Instance Table

Instance Name	Physical Address
CPSW	5283 E000h

Figure 4-1244. CPSW_NC_CPSW_NC_ALE_MOD_VER Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MODULE_ID															
R															
29h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL_VERSION					MAJOR_REVISION			CUSTOM_REVISION		MINOR_REVISION					
R					R			R		R					
0h					1h			0h		5h					

Access Types Legend

Table 4-2664. CPSW_NC_CPSW_NC_ALE_MOD_VER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MODULE_ID	R	29h	ALE_3g512e module ID.
15:11	RTL_VERSION	R	0h	RTL Version.
10:8	MAJOR_REVISION	R	1h	Major Revision.
7:6	CUSTOM_REVISION	R	0h	Custom Revision.
5:0	MINOR_REVISION	R	5h	Minor Revision.

4.18.417 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ALE_ALE_STATUS Registers

4.18.417.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ALE_ALE_STATUS Register (Offset = 3E004h) [reset = 80000400h]

Short Description: ALE Status

Long Description: The ALE status provides information on the ALE configuration and state. The ~iramdepth is used to determine how IPv6 entries are stored in the table. IPv6 entries are stored in two entries where IPv6 Entry hi is designated by the odd slice index and lo is designated by the even slice index. The slice index is above the ram depth like {SlixeIndex,RamIndex}. So for a 64 deep RAM index of 0x005, the Hi portion of the IPv6 entry is located at 0x005|0x040 and the Lo portion is located at 0x005&(~0x040).

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Table 4-2665. Instance Table

Instance Name	Physical Address
CPSW	5283 E004h

Figure 4-1245. CPSW_NC_CPSW_NC_ALE_ALE_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UREGANDREGMSK12	UREGANDREGMSK08	RESERVED													
R	R	NONE													
1h	0h	989680													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POLCNTDIV8								RAMDEPTH128	RAMDEPTH32	RESERVED	KLUENTRIES				
R								R	R	NONE	R				
4h								0h	0h	0	0h				

Access Types Legend

Table 4-2666. CPSW_NC_CPSW_NC_ALE_ALE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	UREGANDREGMSK12	R	1h	When set, the unregistered multicast field is a mask versus an index on 12 bit boundary in the ALE table.
30	UREGANDREGMSK08	R	0h	When set, the unregistered multicast field is a mask versus an index on 8 bit boundary in the ALE table.
29:16	RESERVED	NONE		Reserved
15:8	POLCNTDIV8	R	4h	This is the number of Classifiers the ALE implements divided by 8. A value of 4 indicates 32 policer engines total.
7	RAMDEPTH128	R	0h	The number of ALE entries per slice of the table when this is set it indicates the depth is 128 if both ramdepth128 and ramdepth32 are zero the depth is 64.
6	RAMDEPTH32	R	0h	The number of ALE entries per slice of the table when this is set it indicates the depth is 32 if both ramdepth128 and ramdepth32 are zero the depth is 64.
5	RESERVED	NONE		Reserved
4:0	KLUENTRIES	R	0h	This is the number of table entries total divided by 1024. A value of 1 indicates 1024 table entries. A value of 8 indicates 8192 table entries.

4.18.418 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ALE_ALE_CONTROL Registers

4.18.418.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ALE_ALE_CONTROL Register (Offset = 3E008h) [reset = 0h]

Short Description: ALE Control

Long Description: The ALE Control Register is used to set the ALE modes used for all ports.

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Table 4-2667. Instance Table

Instance Name	Physical Address
CPSW	5283 E008h

Figure 4-1246. CPSW_NC_CPSW_NC_ALE_ALE_CONTROL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ENABLE_ALE	CLEAR_TABLE	AGE_OUT_NOW	RESERVED			MIRROR_DP		UPD_BW_CTRL			RESERVED			MIRROR_TOP	
R/W	R/W	R/W	NONE			R/W		R/W			NONE			R/W	
0h	0h	0h	0			0h		0h			0			0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UPD_STATIC	LRN_HOST_DST	UVLAN_NO_LEARN	MIRROR_MEN	MIRROR_DEN	MIRROR_SEN	RESERVED	EN_HOST_UNI_FLOOD	LEARN_NO_VLANID	ENABLE_VID0_MODE	ENABLE_OUI_DENY	ENABLE_BYPASS	BCAST_MCAST_CTL	ALE_VLAN_AWARE	ENABLE_AUTH_MODE	ENABLE_RATE_LIMIT
R/W	R/W	R/W	R/W	R/W	R/W	NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-2668. CPSW_NC_CPSW_NC_ALE_ALE_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE_ALE	R/W	0h	Enable ALE 0 - Drop all packets 1 - Enable ALE packet processing
30	CLEAR_TABLE	R/W	0h	Clear ALE address table - Setting this bit causes the ALE hardware to write all table bit values to zero. Software must perform a clear table operation as part of the ALE setup/configuration process. Setting this bit causes all ALE accesses to be held up for 64 clocks while the clear is performed. Access to all ALE registers will be blocked (wait states) until the 64 clocks have completed. This bit cannot be read as one because the read is blocked until the clear table is completed at which time this bit is cleared to zero.
29	AGE_OUT_NOW	R/W	0h	Age Out Address Table Now - Setting this bit causes the ALE hardware to remove (free up) any ageable table entry that does not have a set touch bit. This bit is cleared when the age out process has completed. This bit may be read. The age out process takes four times the number of table entries clock cycles (4096 cycles for 1K addresses) best case (no ale packet processing during ageout) and sixty five times the number of table entries clock cycles (66560 cycles for 1K addresses) absolute worst case.
28:26	RESERVED	NONE		Reserved
25:24	MIRROR_DP	R/W	0h	Mirror Destination Port - This field defines the port to which destination traffic destined will be duplicated. That is all traffic that is forwarded to this port will also be mirrored to the ~imirror_top port.

Table 4-2668. CPSW_NC_CPSW_NC_ALE_ALE_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:21	UPD_BW_CTRL	R/W	0h	The ~iupd_bw_ctrl field allows for up to 8 times the rate in which adds, updates, touches, writes, and aging updates can occur. At frequencies of 350Mhz, the table update rate should be at it lowest or 5 Million updates per second. When operating the switch core at frequencies or above, the ~iupd_bw_ctrl can be programmed more aggressive. If the ~iupd_bw_ctrl is set but the frequency of the switch subsystem is below the associated value, ALE will drop packets due to insufficient time to complete lookup under high traffic loads. 0 - 350Mhz, 5M 1 - 359Mhz, 11M 2 - 367Mhz, 16M 3 - 375Mhz, 22M 4 - 384Mhz, 28M 5 - 392Mhz, 34M 6 - 400Mhz, 39M 7 - 409Mhz, 45M
20:18	RESERVED	NONE		Reserved
17:16	MIRROR_TOP	R/W	0h	Mirror To Port - This field defines the destination port for the mirror traffic. If the traffic is received or transmitted on the mirror destination port it will not be duplicated. Traffic defined as mirror traffic only may be dropped by the switch due to congestion.
15	UPD_STATIC	R/W	0h	Update Static Entries - A static Entry is an entry that is not agable. When clear this bit will prevent any static entry (agable bit clear) from being updated due to port change. When set it allows static entries (agable bit clear) to update the source port if required. This bit should normally be '0' for most switch configurations.
14	LRN_HOST_DST	R/W	0h	Learn Host Destination - This field is set to only learn unicast packet source addresses that are destined to the host port. This bit is only valid for 3 port switches and allows the ALE table to only contain addresses the host port is concerned about. This bit is affectively disabled when ~ien_host_uni_flood is set since any unknown unicast is also sent to the host port for extended bridging operations.
13	UVLAN_NO_LEARN	R/W	0h	Unknown VLAN No Learn - This field when set will prevent source addresses of unknown VLAN IDs from being automatically added into the look up table if learning is enabled.
12	MIRROR_MEN	R/W	0h	Mirror Match Entry Enable - This field enables the match mirror option. When this bit is set any traffic whose destination, source, VLAN or OUI matches the ~imirror_midx entry index will have that traffic also sent to the ~imirror_top port.
11	MIRROR_DEN	R/W	0h	Mirror Destination Port Enable - This field enables the destination port mirror option. When this bit is set any traffic destined for the ~imirror_dp port will have its transmit traffic also sent to the ~imirror_top port.
10	MIRROR_SEN	R/W	0h	Mirror Source Port Enable - This field enables the source port mirror option. When this bit is set any port with the ~ipX_mirror_sp set in the ALE Port Control registers set will have its received traffic also sent to the ~imirror_top port.
9	RESERVED	NONE		Reserved
8	EN_HOST_UNI_FLOOD	R/W	0h	Unknown unicast packets flood to host 0 - unknown unicast packets are not sent to the host 1 - unknown unicast packets flood to host port as well as other ports
7	LEARN_NO_VLANID	R/W	0h	Learn No VID - 0 - VID is learned with the source address 1 - VID is not learned with the source address (source address is not tied to VID). Determines the entry type.
6	ENABLE_VID0_MODE	R/W	0h	Enable VLAN ID = 0 Mode 0 - Process the priority tagged packet with VID = PORT_VLAN[11:0]. 1 - Process the priority tagged packet with VID = 0.
5	ENABLE_OUI_DENY	R/W	0h	Enable OUI Deny Mode - When set, any packet with a non-matching OUI source address will be dropped to the host unless the packet destination address matches a supervisory destination address table entry. When cleared, any packet source address matching an OUI address table entry will be dropped to the host unless the destination address matches with a supervisory destination address table entry.
4	ENABLE_BYPASS	R/W	0h	ALE Bypass - When set, packets received on non-host ports are sent to the host. It is expected that packets from the host are directed to the particular port. 0 - no bypass 1 - bypass the ALE

Table 4-2668. CPSW_NC_CPSW_NC_ALE_ALE_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	BCAST_MCAST_CTL	R/W	0h	Rate Limit Transmit mode 0 - Broadcast and multicast rate limit counters are received port based 1 - Broadcast and multicast rate limit counters are transmit port based
2	ALE_VLAN_AWARE	R/W	0h	ALE VLAN Aware - Determines how traffic is forwarded using VLAN rules. 0 - Simple switch rules, packets forwarded to all ports for unknown destinations. 1 - VLAN Aware rules, packets forwarded based on VLAN members
1	ENABLE_AUTH_MODE	R/W	0h	Enable MAC Authorization Mode - Mac authorization mode requires that all table entries be made by the host software. There is no auto learning of addresses in authorization mode and the packet will be dropped if the source address is not found (and the destination address is not a multicast address with the super table entry bit set). 0 - The ALE is not in MAC authorization mode 1 - The ALE is in MAC authorization mode
0	ENABLE_RATE_LIMIT	R/W	0h	Enable Broadcast and Multicast Rate Limit 0 - Broadcast/Multicast rates not limited 1 - Broadcast/Multicast packet reception limited to the port control register rate limit fields.

4.18.419 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ALE_ALE_CTRL2 Registers

4.18.419.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ALE_ALE_CTRL2 Register (Offset = 3E00Ch) [reset = 0h]

Short Description: ALE Control 2

Long Description: The ALE Control 2 Register is used to set the extended features used for all ports.

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Table 4-2669. Instance Table

Instance Name	Physical Address
CPSW	5283 E00Ch

Figure 4-1247. CPSW_NC_CPSW_NC_ALE_ALE_CTRL2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TRK_EN_DST	TRK_EN_SRC	TRK_EN_PRI	RESERVED	TRK_EN_IVLAN	RESERVED	TRK_EN_SIP	TRK_EN_DIP	DROP_BADLEN	NODROP_SRCMCST	DEFNOFRAG	DEFLMTNXTHDR	RESERVED	TRK_BASE		
R/W	R/W	R/W	NONE	R/W	NONE	R/W	R/W	R/W	R/W	R/W	R/W	NONE	R/W		
0h	0h	0h	0	0h	0	0h	0h	0h	0h	0h	0h	0	0h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MULTIHOST	RESERVED							MIRROR_MIDX							
R/W	NONE							R/W							
0h	0							0h							

Access Types Legend

Table 4-2670. CPSW_NC_CPSW_NC_ALE_ALE_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TRK_EN_DST	R/W	0h	Trunk Enable Destination Address - This field enables the destination MAC address to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination.
30	TRK_EN_SRC	R/W	0h	Trunk Enable Source Address - This field enables the source MAC address to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination.
29	TRK_EN_PRI	R/W	0h	Trunk Enable Priority - This field enables the VLAN Priority bits to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination. In the event that DSCP mapping is enabled and there is no VLAN the DSCP priority will be used. For all other non IP frames without VLAN the port default priority is used.
28	RESERVED	NONE		Reserved
27	TRK_EN_IVLAN	R/W	0h	Trunk Enable Inner VLAN - This field enables the inner VLAN ID value (C-VLANID) to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination.
26	RESERVED	NONE		Reserved
25	TRK_EN_SIP	R/W	0h	Trunk Enable Source IP Address - This field enables the source IP address to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination. This feature supports No tag, Priority tagged, VLAN tagged, Q-in-Q double tagging for both IPV6 and IPV4.
24	TRK_EN_DIP	R/W	0h	Trunk Enable Destination IP Address - This field enables the destination IP address to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination. This feature supports No tag, Priority tagged, VLAN tagged, Q-in-Q double tagging for both IPV6 and IPV4.

Table 4-2670. CPSW_NC_CPSW_NC_ALE_ALE_CTRL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	DROP_BADLEN	R/W	0h	Drop Bad Length will drop any packet that the 802.3 length field is larger than the packet. Ethertypes 0-1500 are 802.3 lengths, all others are Ether types.
22	NODROP_SRCMCST	R/W	0h	No Drop Source Multicast will disable the dropping of any source address with the multicast bit set.
21	DEFNOFRAG	R/W	0h	Default No Frag field will cause an IPv4 fragmented packet to be dropped if a VLAN entry is not found.
20	DEFLMTNXTHDR	R/W	0h	Default limit next header field will cause an IPv4 protocol or IPv6 next header packet to be dropped if a VLAN entry is not found and the protocol or next header does not match the ~iALE_NXT_HDR register values.
19	RESERVED	NONE		Reserved
18:16	TRK_BASE	R/W	0h	Trunk Base - This field is the hash formula starting value. Changing this value will cause the packet distribution on trunk ports to be changed. If all the ~itrk_en_dst, ~itrk_en_src, ~itrk_en_pri and ~itrk_en_vlan are '0', this value is used as the distribution index. That is a '0' will select the 1st bit of an 'N' link trunk, a '1' will select the second, etc. Below is the distribution across the trunk links. The first number in the ~iitalic sequence indicates the traffic is sent to the lowest numbered port of a trunk group. For example if you have a 3 port trunk, the hash result 0 will go to the base port (0), hash result 1 will go to the highest port of the trunk group (2), hash result 2 will go to the middle port (1), etc. 1 - ~i00000000 2 - ~i01010101 3 - ~i02102102 4 - ~i03210321
15	MULTIHOST	R/W	0h	The ~multihost allows host traffic to be sent bact to the host if the DA is market for the host port.
14:9	RESERVED	NONE		Reserved
8:0	MIRROR_MIDX	R/W	0h	Mirror Index - This field is the ALE lookup table entry index that when a match occurs will cause this traffic to be mirrored to the ~imirror_top port. That is any VLAN, ONU or address with or withou VLAN can be selected for traffic mirroring.

4.18.420 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ALE_ALE_PRESCALE Registers

4.18.420.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ALE_ALE_PRESCALE Register (Offset = 3E010h) [reset = 0h]

Short Description: ALE Prescale

Long Description: The ALE Prescale Register is used to set the Broadcast and Multicast rate limiting prescaler value.

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Table 4-2671. Instance Table

Instance Name	Physical Address
CPSW	5283 E010h

Figure 4-1248. CPSW_NC_CPSW_NC_ALE_ALE_PRESCALE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												ALE_PRESCALE			
NONE												R/W			
0												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALE_PRESCALE															
R/W															
0h															

Access Types Legend

Table 4-2672. CPSW_NC_CPSW_NC_ALE_ALE_PRESCALE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19:0	ALE_PRESCALE	R/W	0h	ALE Prescale - The input clock is divided by this value for use in the multicast/broadcast rate limiters. The minimum operating value is 0x10. The prescaler is off when the value is zero.

4.18.421 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ALE_ALE_AGING_CTRL Registers

4.18.421.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ALE_ALE_AGING_CTRL Register (Offset = 3E014h) [reset = 0h]

Short Description: ALE Aging Control

Long Description: The ALE Aging Control sets the aging interval which will cause periodic aging to occur. This value specifies the minimum time between aging starts.

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Table 4-2673. Instance Table

Instance Name	Physical Address
CPSW	5283 E014h

Figure 4-1249. CPSW_NC_CPSW_NC_ALE_ALE_AGING_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRESCALE_2_DISABLE	PRESCALE_1_DISABLE	RESERVED						ALE_AGING_TIMER							
R/W	R/W	NONE						R/W							
0h	0h	0						0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALE_AGING_TIMER															
R/W															
0h															

Access Types Legend

Table 4-2674. CPSW_NC_CPSW_NC_ALE_ALE_AGING_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRESCALE_2_DISABLE	R/W	0h	ALE Prescaler 2 Disable - When set will divide the aging interval by 1000. This bit is designed for device verification and should not be used in production software. Combination of PreScale1Disable and PreScale2Disable will divide the aging interval by 1,000,000 for test purposes.
30	PRESCALE_1_DISABLE	R/W	0h	ALE Prescaler 1 Disable - When set will divide the aging interval by 1000. This bit is designed for device verification and should not be used in production software. Combination of PreScale1Disable and PreScale2Disable will divide the aging interval by 1,000,000 for test purposes.
29:24	RESERVED	NONE		Reserved
23:0	ALE_AGING_TIMER	R/W	0h	ALE Aging Timer - This field specifies the number of clock cycles times 1,000,000 between aging operations.

4.18.422 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ALE_ALE_NXT_HDR Registers

4.18.422.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ALE_ALE_NXT_HDR Register (Offset = 3E01Ch) [reset = 0h]

Short Description: ALE Next Header

Long Description: The ALE Next Header is used to limit the IPv6 Next header or IPv4 Protocol values found in the IP header. It is enabled via the ~iLmtNxtHdr bit in the VLAN entry. All four ~iip_nxt_hdr0-3 are compared when enabled, so if only one is required, set them all to the one value to be tested.

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Table 4-2675. Instance Table

Instance Name	Physical Address
CPSW	5283 E01Ch

Figure 4-1250. CPSW_NC_CPSW_NC_ALE_ALE_NXT_HDR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IP_NXT_HDR3								IP_NXT_HDR2							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IP_NXT_HDR1								IP_NXT_HDR0							
R/W								R/W							
0h								0h							

Access Types Legend

Table 4-2676. CPSW_NC_CPSW_NC_ALE_ALE_NXT_HDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	IP_NXT_HDR3	R/W	0h	The ~iip_nxt_hdr3 is the forth protocol or next header compared when enabled.
23:16	IP_NXT_HDR2	R/W	0h	The ~iip_nxt_hdr2 is the third protocol or next header compared when enabled.
15:8	IP_NXT_HDR1	R/W	0h	The ~iip_nxt_hdr1 is the second protocol or next header compared when enabled.
7:0	IP_NXT_HDR0	R/W	0h	The ~iip_nxt_hdr0 is the first protocol or next header compared when enabled.

4.18.423 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ALE_ALE_TBLCTL Registers

4.18.423.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ALE_ALE_TBLCTL Register (Offset = 3E020h) [reset = 0h]

Short Description: ALE Table Control

Long Description: The ALE table control register is used to read or write that ALE table entries. After writing to this register any read or write to any ALE register will be stalled until the read or write operation completes.

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Table 4-2677. Instance Table

Instance Name	Physical Address
CPSW	5283 E020h

Figure 4-1251. CPSW_NC_CPSW_NC_ALE_ALE_TBLCTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TABLEWR	RESERVED														
R/W	NONE														
0h	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TABLEIDX							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-2678. CPSW_NC_CPSW_NC_ALE_ALE_TBLCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TABLEWR	R/W	0h	Table Write - This bit is used to write the table words to the lookup table. 0 - Table Read Operation is performed. The contents of the ~b TABLEIDX entry will be read into the ~b ALE_TBLWx registers 1 - Table write operation is performed. This will take the current contents from the ~b ALE_TBLWx registers and write them to the table at the specified ~b TABLEIDX.
30:9	RESERVED	NONE		Reserved
8:0	TABLEIDX	R/W	0h	The table index is used to determine which lookup table entry is read or written.

4.18.424 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ALE_ALE_TBLW2 Registers

4.18.424.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ALE_ALE_TBLW2 Register (Offset = 3E034h) [reset = 0h]

Short Description: ALE LUT Table word 2

Long Description: The ALE Table Word 2 is the most significant word of an ALE table entry.

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Table 4-2679. Instance Table

Instance Name	Physical Address
CPSW	5283 E034h

Figure 4-1252. CPSW_NC_CPSW_NC_ALE_ALE_TBLW2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									TABLEWRD2						
NONE									R/W						
0									0h						

Access Types Legend

Table 4-2680. CPSW_NC_CPSW_NC_ALE_ALE_TBLW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE		Reserved
6:0	TABLEWRD2	R/W	0h	Table Entry bits [71:64]

4.18.425 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ALE_ALE_TBLW1 Registers

4.18.425.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ALE_ALE_TBLW1 Register (Offset = 3E038h) [reset = 0h]

Short Description: ALE LUT Table word 1

Long Description: The ALE Table Word 1 is the middle word of an ALE table entry.

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Table 4-2681. Instance Table

Instance Name	Physical Address
CPSW	5283 E038h

Figure 4-1253. CPSW_NC_CPSW_NC_ALE_ALE_TBLW1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TABLEWRD1															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TABLEWRD1															
R/W															
0h															

Access Types Legend

Table 4-2682. CPSW_NC_CPSW_NC_ALE_ALE_TBLW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TABLEWRD1	R/W	0h	Table Entry bits [63:32]

4.18.426 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ALE_ALE_TBLW0 Registers

4.18.426.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ALE_ALE_TBLW0 Register (Offset = 3E03Ch) [reset = 0h]

Short Description: ALE LUT Table word 0

Long Description: The ALE Table Word 0 is the least significant word of an ALE table entry.

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Table 4-2683. Instance Table

Instance Name	Physical Address
CPSW	5283 E03Ch

Figure 4-1254. CPSW_NC_CPSW_NC_ALE_ALE_TBLW0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TABLEWRD0															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TABLEWRD0															
R/W															
0h															

Access Types Legend

Table 4-2684. CPSW_NC_CPSW_NC_ALE_ALE_TBLW0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TABLEWRD0	R/W	0h	Table Entry bits [31:0]

4.18.427 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ALE_I0_ALE_PORTCTL0_N Registers

4.18.427.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ALE_I0_ALE_PORTCTL0_N Register (Offset = 3E040h) [reset = 0h]

Short Description: ALE Port Control X

Long Description: The ALE Port Control Register sets the port specific modes of operation.

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Offset = 3e040h + (j * 4h); where j = 0h to 2h

Table 4-2685. Instance Table

Instance Name	Physical Address
CPSW	5283 E040h

Figure 4-1255. CPSW_NC_CPSW_NC_ALE_I0_ALE_PORTCTL0_N Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I0_REG_P0_BCAST_LIMIT								I0_REG_P0_MCAST_LIMIT							
R/W								R/W							
0h								0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I0_REG_P0_DROP_DOUBLE_VLAN	I0_REG_P0_DROP_DUAL_VLAN	I0_REG_P0_MACONLY_CAF	I0_REG_P0_DIS_PAUTHMOD	I0_REG_P0_MACONLY	I0_REG_P0_TRUNKEN	I0_REG_P0_TRUNKNUM		I0_REG_P0_MIRROR_SP	RESERVED	I0_REG_P0_NO_SA_UPDATE	I0_REG_P0_NO_LEARN	I0_REG_P0_VID_INGRESS_CHECK	I0_REG_P0_DROP_UN_TAGGED	I0_REG_P0_PORTSTATE	
R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W	NONE	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h		0h	0	0h	0h	0h	0h	0h	

Access Types Legend

Table 4-2686. CPSW_NC_CPSW_NC_ALE_I0_ALE_PORTCTL0_N Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	I0_REG_P0_BCAST_LIMIT	R/W	0h	Broadcast Packet Rate Limit - Each prescale pulse loads this field into the port broadcast rate limit counter. The port counters are decremented with each packet received or transmitted depending on whether the mode is transmit or receive. If the counters decrement to zero, then further packets are rate limited until the next prescale pulse. Broadcast rate limiting is enabled by a non-zero value in this field.
23:16	I0_REG_P0_MCAST_LIMIT	R/W	0h	Multicast Packet Rate Limit - Each prescale pulse loads this field into the port multicast rate limit counter. The port counters are decremented with each packet received or transmitted depending on whether the mode is transmit or receive. If the counters decrement to zero, then further packets are rate limited until the next prescale pulse. Multicast rate limiting is enabled by a non-zero value in this field.The ~imcast_limit is the number of Multicast packets that will be forwaded per ~iale_prescale time.
15	I0_REG_P0_DROP_DOUBLE_VLAN	R/W	0h	Drop Double VLAN - When set cause any received packet with double VLANs to be dropped. That is if there are two ctag or two stag fields in the packet it will be dropped.
14	I0_REG_P0_DROP_DUAL_VLAN	R/W	0h	Drop Dual VLAN - When set will cause any received packet with dual VLAN stag followed by ctag to be dropped.
13	I0_REG_P0_MACONLY_CAF	R/W	0h	Mac Only Copy All Frames - When set a Mac Only port will transfer all received good frames to the host. When clear a Mac Only port will transfer packets to the host based on ALE destination address lookup operation (which operates more like an Ethernet Mac). A Mac Only port is a port with ~imaconly set.

Table 4-2686. CPSW_NC_CPSW_NC_ALE_I0_ALE_PORTCTL0_N Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	I0_REG_P0_DIS_PAUTH MOD	R/W	0h	Disable Port authorization - When set will allow unknown addresses to arrive on a switch in authorization mode. It is intended for device to device network connection on ports which do not require MACSEC encryption.
11	I0_REG_P0_MACONLY	R/W	0h	MAC Only - When set enables this port be treated like a MAC port for the host. All traffic received is only sent to the host. The host must direct traffic to this port as the lookup engine will not send traffic to the ports with the ~ip0_maconly bit set and the ~ip0_no_learn also set. If ~ip0_maconly bit is set and the ~ip0_no_learn is not set, the host can send non-directed packets that can be sent to the destination of a MacOnly port. It is also possible that The host can broadcast to all ports including MacOnly ports in this mode.
10	I0_REG_P0_TRUNKEN	R/W	0h	Trunk Enable - This field is used to enable a port into a trunk. Any port can be used as a trunk port, any two or more ports with the ~ip0_trunken its set and having the same ~ip0_trunknum will be placed in the same trunk. There is no requirement for trunk ports to be adjacent. If all ports are enabled in the same trunk, no traffic can flow as traffic received within a trunk is never trasnmitted out the same trunk. If only a single port is a member of a trunk, it looks like a normal port with exception of entries in the look up table will be noted as a trunk entry.
9:8	I0_REG_P0_TRUNKNUM	R/W	0h	Trunk Number - This field is used as the trunk number when the ~ip0_trunken is also set. Ports with the same trunk number that have the ~ip0_trunken also set will have traffic distributed within the trunk based on the result of the hash function descrived above.
7	I0_REG_P0_MIRROR_SP	R/W	0h	Mirror Source Port - This field enables the source port mirror option. When this bit is set any traffic received on the port with the reg_p0_mirror_sp bit set will have its received traffic also sent to the ~imirror_top port.
6	RESERVED	NONE		Reserved
5	I0_REG_P0_NO_SA_UP DATE	R/W	0h	No Source Address Update - When set will not update the source addresses for this port.
4	I0_REG_P0_NO_LEARN	R/W	0h	No Learn - When set will not learn the source addresses for this port.
3	I0_REG_P0_VID_INGRE SS_CHECK	R/W	0h	VLAN Ingress Check - When set if a packet received is not a member of the VLAN, the packet will be dropped.
2	I0_REG_P0_DROP_UN_ TAGGED	R/W	0h	If Drop Untagged - When set will drop packets without a VLAN tag.
1:0	I0_REG_P0_PORTSTATE	R/W	0h	Port State - Defins the current port state used for lookup operations. 0 - Disabled 1 - Blocked 2 - Learning 3 - Forwarding

4.18.428 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ALE_ALE_UVLAN_MEMBER Registers

4.18.428.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ALE_ALE_UVLAN_MEMBER Register (Offset = 3E090h) [reset = 0h]

Short Description: ALE Unknown VLAN Member Mask Register

Long Description: The ALE Unknown VLAN Member Mask Register is used to specify the member list for unknown VLAN ID.

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Table 4-2687. Instance Table

Instance Name	Physical Address
CPSW	5283 E090h

Figure 4-1256. CPSW_NC_CPSW_NC_ALE_ALE_UVLAN_MEMBER Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													UVLAN_MEMBER_LIST		
NONE													R/W		
0													0h		

Access Types Legend

Table 4-2688. CPSW_NC_CPSW_NC_ALE_ALE_UVLAN_MEMBER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	UVLAN_MEMBER_LIST	R/W	0h	Unknown VLAN Member List - Each bit represents the port member status for unknown VLANs.

4.18.429 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ALE_ALE_UVLAN_URCAST Registers

4.18.429.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ALE_ALE_UVLAN_URCAST Register (Offset = 3E094h) [reset = 0h]

Short Description: ALE Unknown VLAN Unregistered Multicast Flood Mask Register

Long Description: The ALE Unknown VLAN Unregistered Multicast Flood Mask Register is used to specify which egress ports unregistered multicast addresses egress for the unregistered VLAN ID.

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Table 4-2689. Instance Table

Instance Name	Physical Address
CPSW	5283 E094h

Figure 4-1257. CPSW_NC_CPSW_NC_ALE_ALE_UVLAN_URCAST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													UVLAN_UNREG_MCAST_FLOOD_MASK		
NONE													R/W		
0													0h		

Access Types Legend

Table 4-2690. CPSW_NC_CPSW_NC_ALE_ALE_UVLAN_URCAST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	UVLAN_UNREG_MCAST_FLOOD_MASK	R/W	0h	Unknown VLAN Unregister Multicast Flood Mask - Each bit represents the port to which unregistered multicast are sent for unregistered VLANs.

4.18.430 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ALE_ALE_UVLAN_RMCAST Registers

4.18.430.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ALE_ALE_UVLAN_RMCAST Register (Offset = 3E098h) [reset = 0h]

Short Description: ALE Unknown VLAN Registered Multicast Flood Mask Register

Long Description: The ALE Unknown VLAN Registered Multicast Flood Mask Register is used to specify which egress ports registered multicast addresses egress for the unregistered VLAN ID.

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Table 4-2691. Instance Table

Instance Name	Physical Address
CPSW	5283 E098h

Figure 4-1258. CPSW_NC_CPSW_NC_ALE_ALE_UVLAN_RMCAST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													UVLAN_REG_MCAST_FLOOD_MASK		
NONE													R/W		
0													0h		

Access Types Legend

Table 4-2692. CPSW_NC_CPSW_NC_ALE_ALE_UVLAN_RMCAST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	UVLAN_REG_MCAST_FLOOD_MASK	R/W	0h	Unknown VLAN Register Multicast Flood Mask - Each bit represents the port to which registered multicast are sent for unregistered VLANs. This field is ANDed with the registered multicast mask to determine the destinations for unregistered VLANs.

4.18.431 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ALE_ALE_UVLAN_UNTAG Registers

4.18.431.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ALE_ALE_UVLAN_UNTAG Register (Offset = 3E09Ch) [reset = 0h]

Short Description: ALE Unknown VLAN force Untagged Egress Mask Register

Long Description: The ALE Unknown VLAN force Untagged Egress Mask Register is used to specify which egress ports the VLAN ID will be removed.

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Table 4-2693. Instance Table

Instance Name	Physical Address
CPSW	5283 E09Ch

Figure 4-1259. CPSW_NC_CPSW_NC_ALE_ALE_UVLAN_UNTAG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													UVLAN_FORCE_UNTAGGED_EGRESS		
NONE													R/W		
0													0h		

Access Types Legend

Table 4-2694. CPSW_NC_CPSW_NC_ALE_ALE_UVLAN_UNTAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	UVLAN_FORCE_UNTAGGED_EGRESS	R/W	0h	Unknown VLAN Force Untagged Egress Mask - Each bit represents the port where the VLAN will be removed for unregistered VLANs.

4.18.432 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ALE_ALE_FAST_LUT Registers

4.18.432.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ALE_ALE_FAST_LUT Register (Offset = 3E0B4h) [reset = 0h]

Short Description: ALE Fast LUT Register

Long Description: The Fast LUT registers allows the ports to be placed in Fast LUT mode.

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Table 4-2695. Instance Table

Instance Name	Physical Address
CPSW	5283 E0B4h

Figure 4-1260. CPSW_NC_CPSW_NC_ALE_ALE_FAST_LUT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													FAST_LUT		
NONE													R/W		
0													0h		

Access Types Legend

Table 4-2696. CPSW_NC_CPSW_NC_ALE_ALE_FAST_LUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	FAST_LUT	R/W	0h	The ~Fast_LUT field alows any port to be Fast_LUT mode, which will cause all lookup operations to start based on DA/SA and VLAN only. That is any data beyong the first 32 are not used in the lookup process.

4.18.433 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ALE_ALE_STAT_DIAG Registers

4.18.433.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ALE_ALE_STAT_DIAG Register (Offset = 3E0B8h) [reset = 0h]

Short Description: ALE Statistic Output Diagnostic Register

Long Description: The ALE Statistic Output Diagnostic Register allows the output statistics to diagnose the SW counters. This register is for diagnostice only.

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Table 4-2697. Instance Table

Instance Name	Physical Address
CPSW	5283 E0B8h

Figure 4-1261. CPSW_NC_CPSW_NC_ALE_ALE_STAT_DIAG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PBCAST_DIAG	RESERVED					PORT_DIAG		RESERVED				STAT_DIAG			
R/W	NONE					R/W		NONE				R/W			
0h	0					0h		0				0h			

Access Types Legend

Table 4-2698. CPSW_NC_CPSW_NC_ALE_ALE_STAT_DIAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15	PBCAST_DIAG	R/W	0h	When set and the ~iport_diag is set to zero, will allow all ports to see the same stat diagnostic increment.
14:10	RESERVED	NONE		Reserved
9:8	PORT_DIAG	R/W	0h	The port selected that a received packet will cause the selected error to increment
7:4	RESERVED	NONE		Reserved
3:0	STAT_DIAG	R/W	0h	When non-zero will cause the selected statistic to increment on the next frame received. For the selected Port. 0: Disabled 1: Destination Equal Source Drop Stat will count 2: VLAN Ingress Check Drop Stat will count 3: Source Multicast Drop Stat will count 4: Dual VLAN Drop Stat will count 5: Ether Type length error Drop Stat will count 6: Next Hop Limit Drop Stat will count 7: IPv4 Fragment Drop Stat will count 8: Classifier Hit Stat will count 9: Classifier Red Drop Stat will count 10: Classifier Yellow Drop Stat will count 11: ALE Overflow Drop Stat will count 12: Rate Limit Drop Stat will count 13: Blocked Address Drop Stat will count 14: Secure Address Drop Stat will count 15: Authorization Drop Stat will count.

4.18.434 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ALE_ALE_OAM_LB_CTRL Registers

4.18.434.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ALE_ALE_OAM_LB_CTRL Register (Offset = 3E0BCh) [reset = 0h]

Short Description: ALE OAM Loopback Control

Long Description: The ALE OAM Control allows ports to be put into OAM Loopback, only non-supervisor packet are looped back to the source port.

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Table 4-2699. Instance Table

Instance Name	Physical Address
CPSW	5283 E0BCh

Figure 4-1262. CPSW_NC_CPSW_NC_ALE_ALE_OAM_LB_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													OAM_LB_CTRL		
NONE													R/W		
0													0h		

Access Types Legend

Table 4-2700. CPSW_NC_CPSW_NC_ALE_ALE_OAM_LB_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	OAM_LB_CTRL	R/W	0h	The ~ioam_lb_ctrl allows any port to be put into OAM loopback, that is any packet received will be returned to the same port with an egressop of 0xFF which swaps the source and destination address. BPDUs will still flow through as normal so that OAM can be remotly requested and disabled.

4.18.435 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ALE_EGRESSOP Registers

4.18.435.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ALE_EGRESSOP Register (Offset = 3E0FCh) [reset = 0h]

Short Description: Egress Operation

Long Description: The Egress Operation register allows enabled classifiers with any match like IPSA or IPDA match to use the CPSW Egress Packet Operations Inter VLAN Routing sub functions. If the packet was destined for the host or is destined to any port without any errors, but matches a clasifier that has a programmed egress opcode, it will be forwarded to the destination ports where the destination ports will use the thier egress opcode entry to modify the packet. InterVLAN Routing and mirroring need to be understood, they are orthogonal functions. Care must be taken not to violate VLAN rules as this can redirect packets based on classifier matches.

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Table 4-2701. Instance Table

Instance Name	Physical Address
CPSW	5283 E0FCh

Figure 4-1263. CPSW_NC_CPSW_NC_ALE_EGRESSOP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EGRESS_OP								EGRESS_TRK			TTL_CHECK	RESERVED			
R/W								R/W			R/W	NONE			
0h								0h			0h	0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													DEST_PORTS		
NONE													R/W		
0													0h		

Access Types Legend

Table 4-2702. CPSW_NC_CPSW_NC_ALE_EGRESSOP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	EGRESS_OP	R/W	0h	The Egress Operation defines the operation performed by the CPSW Egress Packet Operations 0: NOP : 1-n: Defines which egress Operation will be performed. This allows Inter VLAN routing to be configured for high bandwidth traffic, reducing CPU load. 0xff: Swap SA and DA of packet, this is intended to allow OAM diagnostics for a link.
23:21	EGRESS_TRK	R/W	0h	The Egress Trunk Index is the calculated trunk index from the SA, DA or VLAN if modified to that InterVLAN routing will work on trunks as well. The DA, SA and VLAN are ignored for trunk generation on InterVLAN Routing so that this field is the index generated from the Egress Op replacements elclusive or'd together into a three bit index.
20	TTL_CHECK	R/W	0h	The TTL Check will cause any packet that fails TTL checks to not be routed to the Inter VLAN Routing sub functions. The packet will be routed to the host it was destined to.
19:3	RESERVED	NONE		Reserved
2:0	DEST_PORTS	R/W	0h	The Destination Ports is a list of the ports the classified packet will be set to. If a destination is a Trunk, all the port bits for that trunck must be set.

4.18.436 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ALE_POLICECFG0 Registers

4.18.436.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ALE_POLICECFG0 Register (Offset = 3E100h) [reset = 0h]

Short Description: Policing Config 0

Long Description: The Policing Config 0 holds the port, frame priority and ONU address index as well as match enables for port, frame priority and ONU address matching.

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Table 4-2703. Instance Table

Instance Name	Physical Address
CPSW	5283 E100h

Figure 4-1264. CPSW_NC_CPSW_NC_ALE_POLICECFG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PORT_MEN	TRUNKID	RESERVED			PORT_NUM		RESERVED					PRI_MEN	PRI_VAL		
R/W	R/W	NONE			R/W		NONE					R/W	R/W		
0h	0h	0			0h		0					0h	0h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ONU_MEN	RESERVED						ONU_INDEX								
R/W	NONE						R/W								
0h	0						0h								

Access Types Legend

Table 4-2704. CPSW_NC_CPSW_NC_ALE_POLICECFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PORT_MEN	R/W	0h	Port Match Enable - Enabled port match for the selected policing/ classifier entry
30	TRUNKID	R/W	0h	Trunk ID - When set indicates the port number is a trunk group.
29:27	RESERVED	NONE		Reserved
26:25	PORT_NUM	R/W	0h	Port Number - Specifies the port address to match for the selected policing/classifier entry
24:20	RESERVED	NONE		Reserved
19	PRI_MEN	R/W	0h	Priority Match Enable - Enables frame priority match for the selected policing/classifier entry
18:16	PRI_VAL	R/W	0h	Priority Value - Specifies the frame priority to match for the selected policing/classifier entry
15	ONU_MEN	R/W	0h	OUI Match Enable - Enables frame ONU address match for the selected policing/classifier entry
14:9	RESERVED	NONE		Reserved
8:0	ONU_INDEX	R/W	0h	OUI Table Entry Index - Specifies the ALE ONU address lookup table index to match for the selected policing/classifier entry

4.18.437 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ALE_POLICECFG1 Registers

4.18.437.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ALE_POLICECFG1 Register (Offset = 3E104h) [reset = 0h]

Short Description: Policing Config 1

Long Description: The Policing Config 1 holds the match enable/match index for the L2 Destination and L2 source addresses

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Table 4-2705. Instance Table

Instance Name	Physical Address
CPSW	5283 E104h

Figure 4-1265. CPSW_NC_CPSW_NC_ALE_POLICECFG1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DST_MEN	RESERVED						DST_INDEX								
R/W	NONE						R/W								
0h	0						0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRC_MEN	RESERVED						SRC_INDEX								
R/W	NONE						R/W								
0h	0						0h								

Access Types Legend

Table 4-2706. CPSW_NC_CPSW_NC_ALE_POLICECFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DST_MEN	R/W	0h	Destination Address Match Enable - Enables frame L2 destination address match for the selected policing/classifier entry
30:25	RESERVED	NONE		Reserved
24:16	DST_INDEX	R/W	0h	Destination Address Table Entry Index - Specifies the ALE L2 destination address lookup table index to match for the selected policing/classifier entry
15	SRC_MEN	R/W	0h	Source Address Match Enable - Enables frame L2 source address match for the selected policing/classifier entry
14:9	RESERVED	NONE		Reserved
8:0	SRC_INDEX	R/W	0h	Source Address Table Entry Index - Specifies the ALE L2 source address lookup table index to match for the selected policing/ classifier entry

4.18.438 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ALE_POLICECFG2 Registers

4.18.438.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ALE_POLICECFG2 Register (Offset = 3E108h) [reset = 0h]

Short Description: Policing Config 2

Long Description: The Policing Config 2 holds the match enable/match index for the Outer VLAN and Inner VLAN addresses

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Table 4-2707. Instance Table

Instance Name	Physical Address
CPSW	5283 E108h

Figure 4-1266. CPSW_NC_CPSW_NC_ALE_POLICECFG2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OVLAN_MEN	RESERVED						OVLAN_INDEX								
R/W	NONE						R/W								
0h	0						0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IVLAN_MEN	RESERVED						IVLAN_INDEX								
R/W	NONE						R/W								
0h	0						0h								

Access Types Legend

Table 4-2708. CPSW_NC_CPSW_NC_ALE_POLICECFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	OVLAN_MEN	R/W	0h	Outer VLAN Match Enable - Enables frame Outer VLAN address match for the selected policing/classifier entry
30:25	RESERVED	NONE		Reserved
24:16	OVLAN_INDEX	R/W	0h	Outer VLAN Table Entry Index - Specifies the ALE Outer VLAN address lookup table index to match for the selected policing/ classifier entry
15	IVLAN_MEN	R/W	0h	Inner VLAN Match Enable - Enables frame Inner VLAN address match for the selected policing/classifier entry
14:9	RESERVED	NONE		Reserved
8:0	IVLAN_INDEX	R/W	0h	Inner VLAN Table Entry Index - Specifies the ALE Inner VLAN address lookup table index to match for the selected policing/ classifier entry

4.18.439 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ALE_POLICECFG3 Registers

4.18.439.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ALE_POLICECFG3 Register (Offset = 3E10Ch) [reset = 0h]

Short Description: Policing Config 3

Long Description: The Policing Config 3 holds the match enable/match index for the Ether Type and IP Source address

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Table 4-2709. Instance Table

Instance Name	Physical Address
CPSW	5283 E10Ch

Figure 4-1267. CPSW_NC_CPSW_NC_ALE_POLICECFG3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ETHERTYPE_MEN	RESERVED						ETHERTYPE_INDEX								
R/W	NONE						R/W								
0h	0						0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IPSRC_MEN	RESERVED						IPSRC_INDEX								
R/W	NONE						R/W								
0h	0						0h								

Access Types Legend

Table 4-2710. CPSW_NC_CPSW_NC_ALE_POLICECFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ETHERTYPE_MEN	R/W	0h	EtherType Match Enable - Enables frame Ether Type match for the selected policing/classifier entry
30:25	RESERVED	NONE		Reserved
24:16	ETHERTYPE_INDEX	R/W	0h	EtherType Table Entry Index - Specifies the ALE Ether Type lookup table index to match for the selected policing/classifier entry
15	IPSRC_MEN	R/W	0h	IP Source Address Match Enable - Enables frame IP Source address match for the selected policing/classifier entry
14:9	RESERVED	NONE		Reserved
8:0	IPSRC_INDEX	R/W	0h	IP Source Address Table Entry Index - Specifies the ALE IP Source address lookup table index to match for the selected policing/classifier entry

4.18.440 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ALE_POLICECFG4 Registers

4.18.440.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ALE_POLICECFG4 Register (Offset = 3E110h) [reset = 0h]

Short Description: Policing Config 4

Long Description: The Policing Config 4 holds the match enable/match index for the IP Destination address

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Table 4-2711. Instance Table

Instance Name	Physical Address
CPSW	5283 E110h

Figure 4-1268. CPSW_NC_CPSW_NC_ALE_POLICECFG4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IPDST_MEN	RESERVED						IPDST_INDEX								
R/W	NONE						R/W								
0h	0						0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
NONE															
0															

Access Types Legend

Table 4-2712. CPSW_NC_CPSW_NC_ALE_POLICECFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IPDST_MEN	R/W	0h	IP Destination Address Match Enable - Enables frame IP Destination address match for the selected policing/classifier entry
30:25	RESERVED	NONE		Reserved
24:16	IPDST_INDEX	R/W	0h	IP Destination Address Table Entry Index - Specifies the ALE IP Destination address lookup table index to match for the selected policing/classifier entry
15:0	RESERVED	NONE		Reserved

4.18.441 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ALE_POLICECFG6 Registers

4.18.441.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ALE_POLICECFG6 Register (Offset = 3E118h) [reset = 0h]

Short Description: Policing Config 6

Long Description: The PIR counter is a 37 bit internal counter where ~ipir_idle_inc_val is added every clock and the frame size << 18 is subtracted at EOF if not RED at LUT time. If the counter is negative the packet will be marked RED, else it can be YELLOW or GREEN based on the CIR counter. If only this counter is used (aka cir_idle_inc_val==0) Packet are marked RED or GREEN based on PIR counter only.

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Table 4-2713. Instance Table

Instance Name	Physical Address
CPSW	5283 E118h

Figure 4-1269. CPSW_NC_CPSW_NC_ALE_POLICECFG6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PIR_IDLE_INC_VAL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PIR_IDLE_INC_VAL															
R/W															
0h															

Access Types Legend

Table 4-2714. CPSW_NC_CPSW_NC_ALE_POLICECFG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PIR_IDLE_INC_VAL	R/W	0h	Peak Information Rate Idle Increment Value - The number added to the PIR counter every clock cycle. If zero the PIR counter is disabled and packets will never be marked or processed as RED.

4.18.442 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ALE_POLICECFG7 Registers

4.18.442.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ALE_POLICECFG7 Register (Offset = 3E11Ch) [reset = 0h]

Short Description: Policing Config 7

Long Description: The CIR counter is a 37 bit internal counter where ~icir_idle_inc_val is added every clock and the frame size << 18 is subtracted at EOF if not RED or YELLOW at LUT time. If the counter is positive the packet will be marked GREEN, else it can be YELLOW or RED based on the PIR counter. If only this counter is used (aka pir_idle_inc_val==0) Packet are marked YELLOW or GREEN based on CIR counter only.

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Table 4-2715. Instance Table

Instance Name	Physical Address
CPSW	5283 E11Ch

Figure 4-1270. CPSW_NC_CPSW_NC_ALE_POLICECFG7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CIR_IDLE_INC_VAL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CIR_IDLE_INC_VAL															
R/W															
0h															

Access Types Legend

Table 4-2716. CPSW_NC_CPSW_NC_ALE_POLICECFG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CIR_IDLE_INC_VAL	R/W	0h	Committed Information Idle Increment Value - The number added to the CIR counter every clock cycle. If zero the CIR counter is disabled and packets will never be marked or processed as YELLOW.

4.18.443 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ALE_POLICETBLCTL Registers

4.18.443.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ALE_POLICETBLCTL Register (Offset = 3E120h) [reset = 0h]

Short Description: Policing Table Control

Long Description: The Policing Table Control is used to read or write the selected policing/classifier entry. The selected policing/classifier entry is only read or written after this register is written based on the value of the ~iwrite_enable bit.

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Table 4-2717. Instance Table

Instance Name	Physical Address
CPSW	5283 E120h

Figure 4-1271. CPSW_NC_CPSW_NC_ALE_POLICETBLCTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WRITE_ENABLE	RESERVED														
R/W	NONE														
0h	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											POL_TBL_IDX				
NONE											R/W				
0											0h				

Access Types Legend

Table 4-2718. CPSW_NC_CPSW_NC_ALE_POLICETBLCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WRITE_ENABLE	R/W	0h	Write Enable - Setting this bit will write the POLICECFG0-7 to the ~ipol_tbl_idx selected policing/classifier entry. Clearing this bit will read the ~ipol_tbl_idx selected policing/classifier entry into the POLICECFG0-7 registers.
30:5	RESERVED	NONE		Reserved
4:0	POL_TBL_IDX	R/W	0h	Policer Entry Index - This field specifies the policing/classifier entry to be read or written. When writing to this field without setting the ~iwrite_enable=1 will cause the selected policing/classifier entry to be loaded into the POLICECFG0-7 registers. When writing to this field with setting the ~iwrite_enable=1 will cause the selected policing/classifier entry to be updated from the POLICECFG0-7 registers.

4.18.444 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ALE_POLICECONTROL Registers

4.18.444.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ALE_POLICECONTROL Register (Offset = 3E124h) [reset = 0h]

Short Description: Policing Control

Long Description: The Control Enables color marking as well as internal ALE packet dropping rules.

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Table 4-2719. Instance Table

Instance Name	Physical Address
CPSW	5283 E124h

Figure 4-1272. CPSW_NC_CPSW_NC_ALE_POLICECONTROL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
POLICING_EN	RESERVED	RED_DROP_EN	YELLOW_DROP_EN	RESERVED	YELLOWTHRESH			POLMCHMODE		PRIORITY_THREAD_EN	MAC_ONLY_DEF_DIS	RESERVED			
R/W	NONE	R/W	R/W	NONE	R/W			R/W		R/W	R/W	NONE			
0h	0	0h	0h	0	0h			0h		0h	0h	0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
NONE															
0															

Access Types Legend

Table 4-2720. CPSW_NC_CPSW_NC_ALE_POLICECONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POLICING_EN	R/W	0h	Policing Enable - Enables the policing to color the packets, this also enables red or yellow drop capabilities.
30	RESERVED	NONE		Reserved
29	RED_DROP_EN	R/W	0h	RED Drop Enable - Enables the ALE to drop the red colored packets.
28	YELLOW_DROP_EN	R/W	0h	WELLOW Drop Enable - Enables the ALE to drop yellow packets based on the ~iyellowthresh value. This field would normally not be used as to let the switch drop packets at a buffer threshold instead. In the event that the switch does not enable buffer threshold dropping, YELLOW packets can be dropped based on this feature.
27	RESERVED	NONE		Reserved
26:24	YELLOWTHRESH	R/W	0h	Yellow Threshold - When set enables a portion of the yellow packets to be dropped based on the ~iyellow_drop_en enable. 0-100% 1=50% 2-33% 3-25% 4=20% 5-17% 6-14% 7-13%
23:22	POLMCHMODE	R/W	0h	Policing Match Mode - This field determines what happens to packets that fail to hit any policing/classifier entry. 0 - No Hit packets are marked GREEN 1 - No Hit packets are marked YELLOW 2 - No Hit packets are marked RED 3 - No Hit packets are marked based on policing/classifier entry=0 state.
21	PRIORITY_THREAD_EN	R/W	0h	Priority Thread Enable - This field determines if priority is OR'd to the default thread when no classifiers hit and the default thread is enabled.
20	MAC_ONLY_DEF_DIS	R/W	0h	MAC Only Default Disable - This field when set disables the default thread on MAC Only Ports. That is the default thread will be {port,priority}. If the traffic matches a classifier with a thread mapping, the classifier thread mapping still occurs.

Table 4-2720. CPSW_NC_CPSW_NC_ALE_POLICECONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	RESERVED	NONE		Reserved

4.18.445 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ALE_POLICETESTCTL Registers

4.18.445.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ALE_POLICETESTCTL Register (Offset = 3E128h) [reset = 0h]

Short Description: Policing Test Control

Long Description: The Policing Test Control enables the ability to determine which policing entry has been hit and whether they reported a red or yellow rate condition.

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Table 4-2721. Instance Table

Instance Name	Physical Address
CPSW	5283 E128h

Figure 4-1273. CPSW_NC_CPSW_NC_ALE_POLICETESTCTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
POL_CLRALL_HIT	POL_CLRALL_REDHIT	POL_CLRALL_YELLOWHIT	POL_CLRSEL_ALL	RESERVED											
R/W	R/W	R/W	R/W	NONE											
0h	0h	0h	0h	0											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											POL_TEST_IDX				
NONE											R/W				
0											0h				

Access Types Legend

Table 4-2722. CPSW_NC_CPSW_NC_ALE_POLICETESTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POL_CLRALL_HIT	R/W	0h	Policer Clear - This bit clears all the policing/classifier hit bits. This bit is self clearing. This can be used to test the fact that a policing/classifier entry has been hit.
30	POL_CLRALL_REDHIT	R/W	0h	Policer Clear RED - This bit clears all the policing/classifier RED hit bits. This bit is self clearing. This can be used to test the fact that a policing/classifier entry has been hit during a RED condition.
29	POL_CLRALL_YELLOWHIT	R/W	0h	Policer Clear YELLOW - This bit clears all the policing/classifier YELLOW hit bits. This bit is self clearing. This can be used to test the fact that a policing/classifier entry has been hit during a YELLOW condition.
28	POL_CLRSEL_ALL	R/W	0h	Police Clear Selected - This bit clears the selected policing/classifier hit, redhit and yellowhit bits. This bit is self clearing.
27:5	RESERVED	NONE		Reserved
4:0	POL_TEST_IDX	R/W	0h	Policer Test Index - This field selects which policing/classifier hit bits will be read or written.

4.18.446 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ALE_POLICEHSTAT Registers

4.18.446.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ALE_POLICEHSTAT Register (Offset = 3E12Ch) [reset = 0h]

Short Description: Policing Hit Status

Long Description: The policing hit status is a read only register that reads the hit bits of the selected policing/classifier.

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Table 4-2723. Instance Table

Instance Name	Physical Address
CPSW	5283 E12Ch

Figure 4-1274. CPSW_NC_CPSW_NC_ALE_POLICEHSTAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
POL_HIT	POL_REDHIT	POL_YELLOWHIT	RESERVED												
R	R	R	NONE												
0h	0h	0h	0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
NONE															
0															

Access Types Legend

Table 4-2724. CPSW_NC_CPSW_NC_ALE_POLICEHSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POL_HIT	R	0h	Policer Hit - This indicates that the selected policing/classifier via the ~ipol_test_idx field has been hit by a packet seen on any port that matches the policing/classifier entry match.
30	POL_REDHIT	R	0h	Policer Hit RED - This indicates that the selected policing/classifier via the ~ipol_test_idx field has been hit during a RED condition by a packet seen on any port that matches the policing/classifier entry match.
29	POL_YELLOWHIT	R	0h	Policer Hit YELLOW - This indicates that the selected policing/classifier via the ~ipol_test_idx field has been hit during a YELLOW condition by a packet seen on any port that matches the policing/classifier entry match.
28:0	RESERVED	NONE		Reserved

4.18.447 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ALE_THREADMAPDEF Registers

4.18.447.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ALE_THREADMAPDEF Register (Offset = 3E134h) [reset = 0h]

Short Description: THREAD Mapping Default Value

Long Description: The THREAD Mapping Default Value register is used to set the default thread ID when no classifier is matched,

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Table 4-2725. Instance Table

Instance Name	Physical Address
CPSW	5283 E134h

Figure 4-1275. CPSW_NC_CPSW_NC_ALE_THREADMAPDEF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEFTHREAD_EN	RESERVED									DEFTHREADVAL					
R/W	NONE									R/W					
0h	0									0h					

Access Types Legend

Table 4-2726. CPSW_NC_CPSW_NC_ALE_THREADMAPDEF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15	DEFTHREAD_EN	R/W	0h	Default Tread Enable - When set the switch will use the ~idefthreadval for the host interface thread ID if no classifier is matched. If clear the switch will generate its own thread ID based on port and priority if there is no classifier match.
14:6	RESERVED	NONE		Reserved
5:0	DEFTHREADVAL	R/W	0h	Default Thread Value - This field specifies the default thread ID value.

4.18.448 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ALE_THREADMAPCTL Registers

4.18.448.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ALE_THREADMAPCTL Register (Offset = 3E138h) [reset = 0h]

Short Description: THREAD Mapping Control

Long Description: The THREAD Mapping Control register allows the highest matched classifier to return a particular thread ID for traffic sent to the host. This allows particular classifier matched traffic to be placed an a particular hosts queue.

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Table 4-2727. Instance Table

Instance Name	Physical Address
CPSW	5283 E138h

Figure 4-1276. CPSW_NC_CPSW_NC_ALE_THREADMAPCTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											CLASSINDEX				
NONE											R/W				
0											0h				

Access Types Legend

Table 4-2728. CPSW_NC_CPSW_NC_ALE_THREADMAPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE		Reserved
4:0	CLASSINDEX	R/W	0h	Classifier Index - This is the classifier index entry that the thread enable and thread value will be read or written by the ~bTHREADMAPVAL register.

4.18.449 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ALE_THREADMAPVAL Registers

4.18.449.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ALE_THREADMAPVAL Register (Offset = 3E13Ch) [reset = 0h]

Short Description: THREAD Mapping Value

Long Description: The THREAD Mapping Value register is used to set the thread ID for a particular classifier entry.

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Table 4-2729. Instance Table

Instance Name	Physical Address
CPSW	5283 E13Ch

Figure 4-1277. CPSW_NC_CPSW_NC_ALE_THREADMAPVAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
THREAD_EN	RESERVED									THREADVAL					
R/W	NONE									R/W					
0h	0									0h					

Access Types Legend

Table 4-2730. CPSW_NC_CPSW_NC_ALE_THREADMAPVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15	THREAD_EN	R/W	0h	Thread Enable - When set the switch will use the ~ithreadval for the selected classifier match. If clear the the thread ID will be determined by the ~bTHREADMAPDEF register settings.
14:6	RESERVED	NONE		Reserved
5:0	THREADVAL	R/W	0h	Thread Value - This field is the thread ID value that is used to map a classifier hit to thread ID for host traffic.

4.18.450 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ECC_REV Registers

4.18.450.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ECC_REV Register (Offset = 3F000h) [reset = 66a03201h]

Short Description: Aggregator Revision Register

Long Description: Revision parameters

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Table 4-2731. Instance Table

Instance Name	Physical Address
CPSW	5283 F000h

Figure 4-1278. CPSW_NC_CPSW_NC_ECC_REV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R		R		R											
1h		2h		6a0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
R					R			R		R					
6h					2h			0h		1h					

Access Types Legend

Table 4-2732. CPSW_NC_CPSW_NC_ECC_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	6h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

4.18.451 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ECC_VECTOR Registers

4.18.451.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ECC_VECTOR Register (Offset = 3F008h) [reset = 0h]

Short Description: ECC Vector Register

Long Description: ECC Vector Register

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Table 4-2733. Instance Table

Instance Name	Physical Address
CPSW	5283 F008h

Figure 4-1279. CPSW_NC_CPSW_NC_ECC_VECTOR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							RD_SVBUS_DONE	RD_SVBUS_ADDRESS							
NONE							R/W1TC	R/W							
0							0h	0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RD_SVBUS	RESERVED				ECC_VECTOR										
R/W1TS	NONE				R/W										
0h	0				0h										

Access Types Legend

Table 4-2734. CPSW_NC_CPSW_NC_ECC_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE		Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE		Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

4.18.452 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ECC_STAT Registers

4.18.452.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ECC_STAT Register (Offset = 3F00Ch) [reset = 14h]

Short Description: Misc Status

Long Description: Misc Status

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Table 4-2735. Instance Table

Instance Name	Physical Address
CPSW	5283 F00Ch

Figure 4-1280. CPSW_NC_CPSW_NC_ECC_STAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
3f2															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					NUM_RAMS										
NONE					R										
3f2					14h										

Access Types Legend

Table 4-2736. CPSW_NC_CPSW_NC_ECC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE		Reserved
10:0	NUM_RAMS	R	14h	Indicates the number of RAMS serviced by the ECC aggregator

4.18.453 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ECC_RESERVED_SVBUS_N Registers

4.18.453.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ECC_RESERVED_SVBUS_N Register (Offset = 3F010h) [reset = 0h]

Short Description: Reserved Area for Serial VBUS Registers

Long Description: Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Offset = 3f010h + (j * 4h); where j = 0h to 7h

Table 4-2737. Instance Table

Instance Name	Physical Address
CPSW	5283 F010h

Figure 4-1281. CPSW_NC_CPSW_NC_ECC_RESERVED_SVBUS_N Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA															
R/W															
0h															

Access Types Legend

Table 4-2738. CPSW_NC_CPSW_NC_ECC_RESERVED_SVBUS_N Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

4.18.454 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ECC_SEC_EOI_REG Registers

4.18.454.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ECC_SEC_EOI_REG Register (Offset = 3F03Ch) [reset = 0h]

Short Description: EOI Register

Long Description: EOI Register

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Table 4-2739. Instance Table

Instance Name	Physical Address
CPSW	5283 F03Ch

Figure 4-1282. CPSW_NC_CPSW_NC_ECC_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															EOI_WR
NONE															R/W1TS
0															0h

Access Types Legend

Table 4-2740. CPSW_NC_CPSW_NC_ECC_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

4.18.455 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ECC_SEC_STATUS_REG0 Registers

4.18.455.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ECC_SEC_STATUS_REG0 Register (Offset = 3F040h) [reset = 0h]

Short Description: Interrupt Status Register 0

Long Description: Interrupt Status Register 0

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Table 4-2741. Instance Table

Instance Name	Physical Address
CPSW	5283 F040h

Figure 4-1283. CPSW_NC_CPSW_NC_ECC_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												RAMECC19_PEND	RAMECC18_PEND	RAMECC17_PEND	RAMECC16_PEND
NONE												R/W1TS	R/W1TS	R/W1TS	R/W1TS
0												0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAMECC15_PEND	RAMECC14_PEND	RAMECC13_PEND	RAMECC12_PEND	RAMECC11_PEND	RAMECC10_PEND	RAMECC9_PEND	RAMECC8_PEND	RAMECC7_PEND	RAMECC6_PEND	RAMECC5_PEND	RAMECC4_PEND	RAMECC3_PEND	RAMECC2_PEND	RAMECC1_PEND	RAMECC0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-2742. CPSW_NC_CPSW_NC_ECC_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19	RAMECC19_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc19_pend
18	RAMECC18_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc18_pend
17	RAMECC17_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc17_pend
16	RAMECC16_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc16_pend
15	RAMECC15_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc15_pend
14	RAMECC14_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc14_pend
13	RAMECC13_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc13_pend
12	RAMECC12_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc12_pend
11	RAMECC11_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc11_pend
10	RAMECC10_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc10_pend
9	RAMECC9_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc9_pend
8	RAMECC8_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc8_pend
7	RAMECC7_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc7_pend
6	RAMECC6_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc6_pend
5	RAMECC5_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc5_pend
4	RAMECC4_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc4_pend
3	RAMECC3_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc3_pend
2	RAMECC2_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc2_pend
1	RAMECC1_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc1_pend

Table 4-2742. CPSW_NC_CPSW_NC_ECC_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RAMECC0_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc0_pend

4.18.456 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ECC_SEC_ENABLE_SET_REG0 Registers

4.18.456.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ECC_SEC_ENABLE_SET_REG0 Register (Offset = 3F080h) [reset = 0h]

Short Description: Interrupt Enable Set Register 0

Long Description: Interrupt Enable Set Register 0

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Table 4-2743. Instance Table

Instance Name	Physical Address
CPSW	5283 F080h

Figure 4-1284. CPSW_NC_CPSW_NC_ECC_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												RAMECC19_ENABLE_SET	RAMECC18_ENABLE_SET	RAMECC17_ENABLE_SET	RAMECC16_ENABLE_SET
NONE												R/W1TS	R/W1TS	R/W1TS	R/W1TS
0												0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAMECC15_ENABLE_SET	RAMECC14_ENABLE_SET	RAMECC13_ENABLE_SET	RAMECC12_ENABLE_SET	RAMECC11_ENABLE_SET	RAMECC10_ENABLE_SET	RAMECC9_ENABLE_SET	RAMECC8_ENABLE_SET	RAMECC7_ENABLE_SET	RAMECC6_ENABLE_SET	RAMECC5_ENABLE_SET	RAMECC4_ENABLE_SET	RAMECC3_ENABLE_SET	RAMECC2_ENABLE_SET	RAMECC1_ENABLE_SET	RAMECC0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-2744. CPSW_NC_CPSW_NC_ECC_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19	RAMECC19_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc19_pend
18	RAMECC18_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc18_pend
17	RAMECC17_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc17_pend
16	RAMECC16_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc16_pend
15	RAMECC15_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc15_pend
14	RAMECC14_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc14_pend
13	RAMECC13_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc13_pend
12	RAMECC12_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc12_pend
11	RAMECC11_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc11_pend
10	RAMECC10_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc10_pend

Table 4-2744. CPSW_NC_CPSW_NC_ECC_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	RAMECC9_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc9_pend
8	RAMECC8_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc8_pend
7	RAMECC7_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc7_pend
6	RAMECC6_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc6_pend
5	RAMECC5_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc5_pend
4	RAMECC4_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc4_pend
3	RAMECC3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc3_pend
2	RAMECC2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc2_pend
1	RAMECC1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc1_pend
0	RAMECC0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc0_pend

4.18.457 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ECC_SEC_ENABLE_CLR_REG0 Registers

4.18.457.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ECC_SEC_ENABLE_CLR_REG0 Register (Offset = 3F0C0h) [reset = 0h]

Short Description: Interrupt Enable Clear Register 0

Long Description: Interrupt Enable Clear Register 0

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Table 4-2745. Instance Table

Instance Name	Physical Address
CPSW	5283 F0C0h

Figure 4-1285. CPSW_NC_CPSW_NC_ECC_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												RAMECC19_ENABLE_CLR	RAMECC18_ENABLE_CLR	RAMECC17_ENABLE_CLR	RAMECC16_ENABLE_CLR
NONE												R/W1TC	R/W1TC	R/W1TC	R/W1TC
0												0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAMECC15_ENABLE_CLR	RAMECC14_ENABLE_CLR	RAMECC13_ENABLE_CLR	RAMECC12_ENABLE_CLR	RAMECC11_ENABLE_CLR	RAMECC10_ENABLE_CLR	RAMECC9_ENABLE_CLR	RAMECC8_ENABLE_CLR	RAMECC7_ENABLE_CLR	RAMECC6_ENABLE_CLR	RAMECC5_ENABLE_CLR	RAMECC4_ENABLE_CLR	RAMECC3_ENABLE_CLR	RAMECC2_ENABLE_CLR	RAMECC1_ENABLE_CLR	RAMECC0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-2746. CPSW_NC_CPSW_NC_ECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19	RAMECC19_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc19_pend
18	RAMECC18_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc18_pend
17	RAMECC17_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc17_pend
16	RAMECC16_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc16_pend
15	RAMECC15_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc15_pend
14	RAMECC14_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc14_pend
13	RAMECC13_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc13_pend
12	RAMECC12_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc12_pend
11	RAMECC11_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc11_pend
10	RAMECC10_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc10_pend

Table 4-2746. CPSW_NC_CPSW_NC_ECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	RAMECC9_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc9_pend
8	RAMECC8_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc8_pend
7	RAMECC7_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc7_pend
6	RAMECC6_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc6_pend
5	RAMECC5_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc5_pend
4	RAMECC4_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc4_pend
3	RAMECC3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc3_pend
2	RAMECC2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc2_pend
1	RAMECC1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc1_pend
0	RAMECC0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc0_pend

4.18.458 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ECC_DED_EOI_REG Registers

4.18.458.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ECC_DED_EOI_REG Register (Offset = 3F13Ch) [reset = 0h]

Short Description: EOI Register

Long Description: EOI Register

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Table 4-2747. Instance Table

Instance Name	Physical Address
CPSW	5283 F13Ch

Figure 4-1286. CPSW_NC_CPSW_NC_ECC_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															EOI_WR
NONE															R/W1TS
0															0h

Access Types Legend

Table 4-2748. CPSW_NC_CPSW_NC_ECC_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

4.18.459 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ECC_DED_STATUS_REG0 Registers

4.18.459.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ECC_DED_STATUS_REG0 Register (Offset = 3F140h) [reset = 0h]

Short Description: Interrupt Status Register 0

Long Description: Interrupt Status Register 0

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Table 4-2749. Instance Table

Instance Name	Physical Address
CPSW	5283 F140h

Figure 4-1287. CPSW_NC_CPSW_NC_ECC_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												RAMECC19_PEND	RAMECC18_PEND	RAMECC17_PEND	RAMECC16_PEND
NONE												R/W1TS	R/W1TS	R/W1TS	R/W1TS
0												0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAMECC15_PEND	RAMECC14_PEND	RAMECC13_PEND	RAMECC12_PEND	RAMECC11_PEND	RAMECC10_PEND	RAMECC9_PEND	RAMECC8_PEND	RAMECC7_PEND	RAMECC6_PEND	RAMECC5_PEND	RAMECC4_PEND	RAMECC3_PEND	RAMECC2_PEND	RAMECC1_PEND	RAMECC0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-2750. CPSW_NC_CPSW_NC_ECC_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19	RAMECC19_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc19_pend
18	RAMECC18_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc18_pend
17	RAMECC17_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc17_pend
16	RAMECC16_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc16_pend
15	RAMECC15_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc15_pend
14	RAMECC14_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc14_pend
13	RAMECC13_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc13_pend
12	RAMECC12_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc12_pend
11	RAMECC11_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc11_pend
10	RAMECC10_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc10_pend
9	RAMECC9_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc9_pend
8	RAMECC8_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc8_pend
7	RAMECC7_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc7_pend
6	RAMECC6_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc6_pend
5	RAMECC5_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc5_pend
4	RAMECC4_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc4_pend
3	RAMECC3_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc3_pend
2	RAMECC2_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc2_pend
1	RAMECC1_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc1_pend

Table 4-2750. CPSW_NC_CPSW_NC_ECC_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RAMECC0_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc0_pend

4.18.460 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ECC_DED_ENABLE_SET_REG0 Registers

4.18.460.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ECC_DED_ENABLE_SET_REG0 Register (Offset = 3F180h) [reset = 0h]

Short Description: Interrupt Enable Set Register 0

Long Description: Interrupt Enable Set Register 0

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Table 4-2751. Instance Table

Instance Name	Physical Address
CPSW	5283 F180h

Figure 4-1288. CPSW_NC_CPSW_NC_ECC_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												RAMECC19_ENABLE_SET	RAMECC18_ENABLE_SET	RAMECC17_ENABLE_SET	RAMECC16_ENABLE_SET
NONE												R/W1TS	R/W1TS	R/W1TS	R/W1TS
0												0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAMECC15_ENABLE_SET	RAMECC14_ENABLE_SET	RAMECC13_ENABLE_SET	RAMECC12_ENABLE_SET	RAMECC11_ENABLE_SET	RAMECC10_ENABLE_SET	RAMECC9_ENABLE_SET	RAMECC8_ENABLE_SET	RAMECC7_ENABLE_SET	RAMECC6_ENABLE_SET	RAMECC5_ENABLE_SET	RAMECC4_ENABLE_SET	RAMECC3_ENABLE_SET	RAMECC2_ENABLE_SET	RAMECC1_ENABLE_SET	RAMECC0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-2752. CPSW_NC_CPSW_NC_ECC_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19	RAMECC19_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc19_pend
18	RAMECC18_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc18_pend
17	RAMECC17_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc17_pend
16	RAMECC16_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc16_pend
15	RAMECC15_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc15_pend
14	RAMECC14_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc14_pend
13	RAMECC13_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc13_pend
12	RAMECC12_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc12_pend
11	RAMECC11_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc11_pend
10	RAMECC10_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc10_pend

Table 4-2752. CPSW_NC_CPSW_NC_ECC_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	RAMECC9_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc9_pend
8	RAMECC8_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc8_pend
7	RAMECC7_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc7_pend
6	RAMECC6_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc6_pend
5	RAMECC5_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc5_pend
4	RAMECC4_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc4_pend
3	RAMECC3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc3_pend
2	RAMECC2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc2_pend
1	RAMECC1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc1_pend
0	RAMECC0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc0_pend

4.18.461 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ECC_DED_ENABLE_CLR_REG0 Registers

4.18.461.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ECC_DED_ENABLE_CLR_REG0 Register (Offset = 3F1C0h) [reset = 0h]

Short Description: Interrupt Enable Clear Register 0

Long Description: Interrupt Enable Clear Register 0

Return to Summary Table

Table 4-2753. Instance Table

Instance Name	Physical Address
CPSW	5283 F1C0h

Figure 4-1289. CPSW_NC_CPSW_NC_ECC_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												RAMECC19_ENABLE_CLR	RAMECC18_ENABLE_CLR	RAMECC17_ENABLE_CLR	RAMECC16_ENABLE_CLR
NONE												R/W1TC	R/W1TC	R/W1TC	R/W1TC
0												0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAMECC15_ENABLE_CLR	RAMECC14_ENABLE_CLR	RAMECC13_ENABLE_CLR	RAMECC12_ENABLE_CLR	RAMECC11_ENABLE_CLR	RAMECC10_ENABLE_CLR	RAMECC9_ENABLE_CLR	RAMECC8_ENABLE_CLR	RAMECC7_ENABLE_CLR	RAMECC6_ENABLE_CLR	RAMECC5_ENABLE_CLR	RAMECC4_ENABLE_CLR	RAMECC3_ENABLE_CLR	RAMECC2_ENABLE_CLR	RAMECC1_ENABLE_CLR	RAMECC0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-2754. CPSW_NC_CPSW_NC_ECC_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE		Reserved
19	RAMECC19_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc19_pend
18	RAMECC18_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc18_pend
17	RAMECC17_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc17_pend
16	RAMECC16_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc16_pend
15	RAMECC15_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc15_pend
14	RAMECC14_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc14_pend
13	RAMECC13_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc13_pend
12	RAMECC12_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc12_pend
11	RAMECC11_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc11_pend
10	RAMECC10_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc10_pend

Table 4-2754. CPSW_NC_CPSW_NC_ECC_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	RAMECC9_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc9_pend
8	RAMECC8_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc8_pend
7	RAMECC7_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc7_pend
6	RAMECC6_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc6_pend
5	RAMECC5_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc5_pend
4	RAMECC4_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc4_pend
3	RAMECC3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc3_pend
2	RAMECC2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc2_pend
1	RAMECC1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc1_pend
0	RAMECC0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc0_pend

4.18.462 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ECC_AGGR_ENABLE_SET Registers

4.18.462.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ECC_AGGR_ENABLE_SET Register (Offset = 3F200h) [reset = 0h]

Short Description: AGGR interrupt enable set Register

Long Description: AGGR interrupt enable set Register

Return to Summary Table

Table 4-2755. Instance Table

Instance Name	Physical Address
CPSW	5283 F200h

Figure 4-1290. CPSW_NC_CPSW_NC_ECC_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														TIMEOUT	PARITY
NONE														R/W1TS	R/W1TS
0														0h	0h

Access Types Legend

Table 4-2756. CPSW_NC_CPSW_NC_ECC_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

4.18.463 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ECC_AGGR_ENABLE_CLR Registers

4.18.463.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ECC_AGGR_ENABLE_CLR Register (Offset = 3F204h) [reset = 0h]

Short Description: AGGR interrupt enable clear Register

Long Description: AGGR interrupt enable clear Register

Return to Summary Table

Table 4-2757. Instance Table

Instance Name	Physical Address
CPSW	5283 F204h

Figure 4-1291. CPSW_NC_CPSW_NC_ECC_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														TIMEOUT	PARITY
NONE														R/W1TC	R/W1TC
0														0h	0h

Access Types Legend

Table 4-2758. CPSW_NC_CPSW_NC_ECC_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

4.18.464 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ECC_AGGR_STATUS_SET Registers

4.18.464.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ECC_AGGR_STATUS_SET Register (Offset = 3F208h) [reset = 0h]

Short Description: AGGR interrupt status set Register

Long Description: AGGR interrupt status set Register

Return to Summary Table

Table 4-2759. Instance Table

Instance Name	Physical Address
CPSW	5283 F208h

Figure 4-1292. CPSW_NC_CPSW_NC_ECC_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												TIMEOUT		PARITY	
NONE												R/WI		R/WI	
0												0h		0h	

Access Types Legend

Table 4-2760. CPSW_NC_CPSW_NC_ECC_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

4.18.465 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ECC_AGGR_STATUS_CLR Registers

4.18.465.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_ECC_AGGR_STATUS_CLR Register (Offset = 3F20Ch) [reset = 0h]

Short Description: AGGR interrupt status clear Register

Long Description: AGGR interrupt status clear Register

Return to Summary Table

Table 4-2761. Instance Table

Instance Name	Physical Address
CPSW	5283 F20Ch

Figure 4-1293. CPSW_NC_CPSW_NC_ECC_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												TIMEOUT		PARITY	
NONE												R/WD		R/WD	
0												0h		0h	

Access Types Legend

Table 4-2762. CPSW_NC_CPSW_NC_ECC_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

4.18.466 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_GENF_COMP_LOW_REG_J Registers

4.18.466.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_GENF_COMP_LOW_REG_J Register (Offset = 3D0E0h) [reset = 0h]

Short Description: comp_low_reg

Long Description: Time Stamp Generate Function Comparison Low Value

Return to Summary Table

Offset = 3d0e0h + (j * 20h); where j = 0h to 1h

Table 4-2763. Instance Table

Instance Name	Physical Address
CPSW	5283 D0E0h

Figure 4-1294. CPSW_NC_CPSW_NC_CPTS_TS_GENF_COMP_LOW_REG_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP_LOW															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP_LOW															
R/W															
0h															

Access Types Legend

Table 4-2764. CPSW_NC_CPSW_NC_CPTS_TS_GENF_COMP_LOW_REG_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP_LOW	R/W	0h	Time Stamp Generate Function Comparison Low Value

4.18.467 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_GENF_COMP_HIGH_REG_J Registers

4.18.467.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_GENF_COMP_HIGH_REG_J Register (Offset = 3D0E4h) [reset = 0h]

Short Description: comp_high_reg

Long Description: Time Stamp Generate Function Comparison high Value

Return to Summary Table

Offset = 3d0e4h + (j * 20h); where j = 0h to 1h

Table 4-2765. Instance Table

Instance Name	Physical Address
CPSW	5283 D0E4h

Figure 4-1295. CPSW_NC_CPSW_NC_CPTS_TS_GENF_COMP_HIGH_REG_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP_HIGH															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP_HIGH															
R/W															
0h															

Access Types Legend

Table 4-2766. CPSW_NC_CPSW_NC_CPTS_TS_GENF_COMP_HIGH_REG_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP_HIGH	R/W	0h	Time Stamp Generate Function Comparison High Value

4.18.468 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_GENF_CONTROL_REG_J Registers

4.18.468.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_GENF_CONTROL_REG_J Register (Offset = 3D0E8h) [reset = 0h]

Short Description: control_reg

Long Description: Time Stamp Generate Function Control

Return to Summary Table

Offset = 3d0e8h + (j * 20h); where j = 0h to 1h

Table 4-2767. Instance Table

Instance Name	Physical Address
CPSW	5283 D0E8h

Figure 4-1296. CPSW_NC_CPSW_NC_CPTS_TS_GENF_CONTROL_REG_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														PPM_DIR	POLARITY_INV
NONE														R/W	R/W
0														0h	0h

Access Types Legend

Table 4-2768. CPSW_NC_CPSW_NC_CPTS_TS_GENF_CONTROL_REG_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1	PPM_DIR	R/W	0h	Time Stamp Generate Function PPM Direction
0	POLARITY_INV	R/W	0h	Time Stamp Generate Function Polarity Invert

4.18.469 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_GENF_LENGTH_REG_J Registers

4.18.469.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_GENF_LENGTH_REG_J Register (Offset = 3D0ECh) [reset = 0h]

Short Description: length_reg

Long Description: Time Stamp Generate Function Length Value

Return to Summary Table

Offset = 3d0ech + (j * 20h); where j = 0h to 1h

Table 4-2769. Instance Table

Instance Name	Physical Address
CPSW	5283 D0ECh

Figure 4-1297. CPSW_NC_CPSW_NC_CPTS_TS_GENF_LENGTH_REG_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LENGTH															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LENGTH															
R/W															
0h															

Access Types Legend

Table 4-2770. CPSW_NC_CPSW_NC_CPTS_TS_GENF_LENGTH_REG_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LENGTH	R/W	0h	Time Stamp Generate Function Length Value

4.18.470 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_GENF_PPM_LOW_REG_J Registers

4.18.470.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_GENF_PPM_LOW_REG_J Register (Offset = 3D0F0h) [reset = 0h]

Short Description: ppm_low_reg

Long Description: Time Stamp Generate Function PPM Low Value

Return to Summary Table

Offset = 3d0f0h + (j * 20h); where j = 0h to 1h

Table 4-2771. Instance Table

Instance Name	Physical Address
CPSW	5283 D0F0h

Figure 4-1298. CPSW_NC_CPSW_NC_CPTS_TS_GENF_PPM_LOW_REG_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PPM_LOW															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPM_LOW															
R/W															
0h															

Access Types Legend

Table 4-2772. CPSW_NC_CPSW_NC_CPTS_TS_GENF_PPM_LOW_REG_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PPM_LOW	R/W	0h	Time Stamp Generate Function PPM Low Value

4.18.471 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_GENF_PPM_HIGH_REG_J Registers

4.18.471.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_GENF_PPM_HIGH_REG_J Register (Offset = 3D0F4h) [reset = 0h]

Short Description: ppm_high_reg

Long Description: Time Stamp Generate Function PPM High Value

Return to Summary Table

Offset = 3d0f4h + (j * 20h); where j = 0h to 1h

Table 4-2773. Instance Table

Instance Name	Physical Address
CPSW	5283 D0F4h

Figure 4-1299. CPSW_NC_CPSW_NC_CPTS_TS_GENF_PPM_HIGH_REG_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PPM_HIGH									
NONE						R/W									
0						0h									

Access Types Legend

Table 4-2774. CPSW_NC_CPSW_NC_CPTS_TS_GENF_PPM_HIGH_REG_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	PPM_HIGH	R/W	0h	Time Stamp Generate Function PPM High Value

4.18.472 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_GENF_NUDGE_REG_J Registers

4.18.472.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_GENF_NUDGE_REG_J Register (Offset = 3D0F8h) [reset = 0h]

Short Description: nudge_reg

Long Description: Time Stamp Generate Function Nudge Value

Return to Summary Table

Offset = 3d0f8h + (j * 20h); where j = 0h to 1h

Table 4-2775. Instance Table

Instance Name	Physical Address
CPSW	5283 D0F8h

Figure 4-1300. CPSW_NC_CPSW_NC_CPTS_TS_GENF_NUDGE_REG_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								NUDGE							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-2776. CPSW_NC_CPSW_NC_CPTS_TS_GENF_NUDGE_REG_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	NUDGE	R/W	0h	Time Stamp Generate Function Nudge Value

4.18.473 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_ESTF_COMP_LOW_REG_J Registers

4.18.473.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_ESTF_COMP_LOW_REG_J Register (Offset = 3D200h) [reset = 0h]

Short Description: comp_low_reg

Long Description: Time Stamp ESTF Generate Function Comparison Low Value

Return to Summary Table

Offset = 3d200h + (j * 20h); where j = 0h to 1h

Table 4-2777. Instance Table

Instance Name	Physical Address
CPSW	5283 D200h

Figure 4-1301. CPSW_NC_CPSW_NC_CPTS_TS_ESTF_COMP_LOW_REG_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP_LOW															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP_LOW															
R/W															
0h															

Access Types Legend

Table 4-2778. CPSW_NC_CPSW_NC_CPTS_TS_ESTF_COMP_LOW_REG_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP_LOW	R/W	0h	Time Stamp ESTF Generate Function Comparison Low Value

4.18.474 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_ESTF_COMP_HIGH_REG_J Registers

4.18.474.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_ESTF_COMP_HIGH_REG_J Register (Offset = 3D204h) [reset = 0h]

Short Description: comp_high_reg

Long Description: Time Stamp ESTF Generate Function Comparison high Value

Return to Summary Table

Offset = 3d204h + (j * 20h); where j = 0h to 1h

Table 4-2779. Instance Table

Instance Name	Physical Address
CPSW	5283 D204h

Figure 4-1302. CPSW_NC_CPSW_NC_CPTS_TS_ESTF_COMP_HIGH_REG_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP_HIGH															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP_HIGH															
R/W															
0h															

Access Types Legend

Table 4-2780. CPSW_NC_CPSW_NC_CPTS_TS_ESTF_COMP_HIGH_REG_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP_HIGH	R/W	0h	Time Stamp ESTF Generate Function Comparison High Value

4.18.475 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_ESTF_CONTROL_REG_J Registers

4.18.475.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_ESTF_CONTROL_REG_J Register (Offset = 3D208h) [reset = 0h]

Short Description: control_reg

Long Description: Time Stamp ESTF Generate Function Control

Return to Summary Table

Offset = 3d208h + (j * 20h); where j = 0h to 1h

Table 4-2781. Instance Table

Instance Name	Physical Address
CPSW	5283 D208h

Figure 4-1303. CPSW_NC_CPSW_NC_CPTS_TS_ESTF_CONTROL_REG_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														PPM_DIR	POLARITY_INV
NONE														R/W	R/W
0														0h	0h

Access Types Legend

Table 4-2782. CPSW_NC_CPSW_NC_CPTS_TS_ESTF_CONTROL_REG_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1	PPM_DIR	R/W	0h	Time Stamp ESTF Generate Function PPM Direction
0	POLARITY_INV	R/W	0h	Time Stamp ESTF Generate Function Polarity Invert

4.18.476 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_ESTF_LENGTH_REG_J Registers

4.18.476.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_ESTF_LENGTH_REG_J Register (Offset = 3D20Ch) [reset = 0h]

Short Description: length_reg

Long Description: Time Stamp ESTF Generate Function Length Value

Return to Summary Table

Offset = 3d20ch + (j * 20h); where j = 0h to 1h

Table 4-2783. Instance Table

Instance Name	Physical Address
CPSW	5283 D20Ch

Figure 4-1304. CPSW_NC_CPSW_NC_CPTS_TS_ESTF_LENGTH_REG_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LENGTH															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LENGTH															
R/W															
0h															

Access Types Legend

Table 4-2784. CPSW_NC_CPSW_NC_CPTS_TS_ESTF_LENGTH_REG_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LENGTH	R/W	0h	Time Stamp ESTF Generate Function Length Value

4.18.477 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_ESTF_PPM_LOW_REG_J Registers

4.18.477.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_ESTF_PPM_LOW_REG_J Register (Offset = 3D210h) [reset = 0h]

Short Description: ppm_low_reg

Long Description: Time Stamp ESTF Generate Function PPM Low Value

Return to Summary Table

Offset = 3d210h + (j * 20h); where j = 0h to 1h

Table 4-2785. Instance Table

Instance Name	Physical Address
CPSW	5283 D210h

Figure 4-1305. CPSW_NC_CPSW_NC_CPTS_TS_ESTF_PPM_LOW_REG_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PPM_LOW															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPM_LOW															
R/W															
0h															

Access Types Legend

Table 4-2786. CPSW_NC_CPSW_NC_CPTS_TS_ESTF_PPM_LOW_REG_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PPM_LOW	R/W	0h	Time Stamp ESTF Generate Function PPM Low Value

4.18.478 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_ESTF_PPM_HIGH_REG_J Registers

4.18.478.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_ESTF_PPM_HIGH_REG_J Register (Offset = 3D214h) [reset = 0h]

Short Description: ppm_high_reg

Long Description: Time Stamp ESTF Generate Function PPM High Value

Return to Summary Table

Offset = 3d214h + (j * 20h); where j = 0h to 1h

Table 4-2787. Instance Table

Instance Name	Physical Address
CPSW	5283 D214h

Figure 4-1306. CPSW_NC_CPSW_NC_CPTS_TS_ESTF_PPM_HIGH_REG_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PPM_HIGH									
NONE						R/W									
0						0h									

Access Types Legend

Table 4-2788. CPSW_NC_CPSW_NC_CPTS_TS_ESTF_PPM_HIGH_REG_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:0	PPM_HIGH	R/W	0h	Time Stamp ESTF Generate Function PPM High Value

4.18.479 CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_ESTF_NUDGE_REG_J Registers

4.18.479.1 CPSW_VBUSP_CPSW_NC_CPSW_NC_CPTS_TS_ESTF_NUDGE_REG_J Register (Offset = 3D218h) [reset = 0h]

Short Description: nudge_reg

Long Description: Time Stamp ESTF Generate Function Nudge Value

Return to Summary Table

Offset = 3d218h + (j * 20h); where j = 0h to 1h

Table 4-2789. Instance Table

Instance Name	Physical Address
CPSW	5283 D218h

Figure 4-1307. CPSW_NC_CPSW_NC_CPTS_TS_ESTF_NUDGE_REG_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								NUDGE							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-2790. CPSW_NC_CPSW_NC_CPTS_TS_ESTF_NUDGE_REG_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	NUDGE	R/W	0h	Time Stamp ESTF Generate Function Nudge Value

4.18.480 Access Table

Table 4-2791. Access Type Codes

Access Type	Code	Description
R	R	Read
R/W	R/W	Read / Write
R/W1TS	R/W1TS	Read/Write 1 To Set
R/W1TC	R/W1TC	Read/Write 1 To Clear
W	W	Write
R/WI	R/WI	Read/Write Increment. A write to this bit field increments the specified register bit field by the amount written.
R/WD	R/WD	Read/Write Decrement. A write to this bit field decrements the specified register bit field by the amount written.

4.19 RTI Registers

Table 4-2792. MEM, MEM Registers, Base Address=0X0000000052180000, Length=256

Offset	Length	Register Name	rti0 Physical Address	rti1 Physical Address	rti2 Physical Address
0h	32	RTIGCTRL	5218 0000h	5218 1000h	5218 2000h
4h	32	RTITBCTRL	5218 0004h	5218 1004h	5218 2004h
8h	32	RTICAPCTRL	5218 0008h	5218 1008h	5218 2008h
Ch	32	RTICOMPCTRL	5218 000Ch	5218 100Ch	5218 200Ch
10h	32	RTIFRC0	5218 0010h	5218 1010h	5218 2010h
14h	32	RTIUC0	5218 0014h	5218 1014h	5218 2014h
18h	32	RTICPUC0	5218 0018h	5218 1018h	5218 2018h
20h	32	RTICAFRC0	5218 0020h	5218 1020h	5218 2020h
24h	32	RTICAUC0	5218 0024h	5218 1024h	5218 2024h
30h	32	RTIFRC1	5218 0030h	5218 1030h	5218 2030h
34h	32	RTIUC1	5218 0034h	5218 1034h	5218 2034h
38h	32	RTICPUC1	5218 0038h	5218 1038h	5218 2038h
40h	32	RTICAFRC1	5218 0040h	5218 1040h	5218 2040h
44h	32	RTICAUC1	5218 0044h	5218 1044h	5218 2044h
50h	32	RTICOMP0	5218 0050h	5218 1050h	5218 2050h
54h	32	RTIUDCP0	5218 0054h	5218 1054h	5218 2054h
58h	32	RTICOMP1	5218 0058h	5218 1058h	5218 2058h
5Ch	32	RTIUDCP1	5218 005Ch	5218 105Ch	5218 205Ch
60h	32	RTICOMP2	5218 0060h	5218 1060h	5218 2060h
64h	32	RTIUDCP2	5218 0064h	5218 1064h	5218 2064h
68h	32	RTICOMP3	5218 0068h	5218 1068h	5218 2068h
6Ch	32	RTIUDCP3	5218 006Ch	5218 106Ch	5218 206Ch
70h	32	RTITBLCOMP	5218 0070h	5218 1070h	5218 2070h
74h	32	RTITBHCOMP	5218 0074h	5218 1074h	5218 2074h
80h	32	RTISETINT	5218 0080h	5218 1080h	5218 2080h
84h	32	RTICLEARINT	5218 0084h	5218 1084h	5218 2084h
88h	32	RTIINTFLAG	5218 0088h	5218 1088h	5218 2088h
90h	32	RTIDWDCTRL	5218 0090h	5218 1090h	5218 2090h
94h	32	RTIDWDPRLD	5218 0094h	5218 1094h	5218 2094h
98h	32	RTIWDSTATUS	5218 0098h	5218 1098h	5218 2098h
9Ch	32	RTIWDKEY	5218 009Ch	5218 109Ch	5218 209Ch
A0h	32	RTIDWDCNTR	5218 00A0h	5218 10A0h	5218 20A0h
A4h	32	RTIWWDRXNCTRL	5218 00A4h	5218 10A4h	5218 20A4h
A8h	32	RTIWWDSIZECTRL	5218 00A8h	5218 10A8h	5218 20A8h
ACh	32	RTIINTCLRENABLE	5218 00ACh	5218 10ACh	5218 20ACh
B0h	32	RTICOMP0CLR	5218 00B0h	5218 10B0h	5218 20B0h
B4h	32	RTICOMP1CLR	5218 00B4h	5218 10B4h	5218 20B4h
B8h	32	RTICOMP2CLR	5218 00B8h	5218 10B8h	5218 20B8h
BCh	32	RTICOMP3CLR	5218 00BCh	5218 10BCh	5218 20BCh

Table 4-2793. MEM, MEM Registers, Base Address=0X0000000052180000, Length=256

Offset	Length	Register Name	rti3 Physical Address
0h	32	RTIGCTRL	5218 3000h
4h	32	RTITBCTRL	5218 3004h
8h	32	RTICAPCTRL	5218 3008h

Table 4-2793. MEM, MEM Registers, Base Address=0X0000000052180000, Length=256 (continued)

Offset	Length	Register Name	rti3 Physical Address
Ch	32	RTICOMPCTRL	5218 300Ch
10h	32	RTIFRC0	5218 3010h
14h	32	RTIUC0	5218 3014h
18h	32	RTICPUC0	5218 3018h
20h	32	RTICAFRC0	5218 3020h
24h	32	RTICAUC0	5218 3024h
30h	32	RTIFRC1	5218 3030h
34h	32	RTIUC1	5218 3034h
38h	32	RTICPUC1	5218 3038h
40h	32	RTICAFRC1	5218 3040h
44h	32	RTICAUC1	5218 3044h
50h	32	RTICOMP0	5218 3050h
54h	32	RTIUDCP0	5218 3054h
58h	32	RTICOMP1	5218 3058h
5Ch	32	RTIUDCP1	5218 305Ch
60h	32	RTICOMP2	5218 3060h
64h	32	RTIUDCP2	5218 3064h
68h	32	RTICOMP3	5218 3068h
6Ch	32	RTIUDCP3	5218 306Ch
70h	32	RTITBLCOMP	5218 3070h
74h	32	RTITBHCOMP	5218 3074h
80h	32	RTISETINT	5218 3080h
84h	32	RTICLEARINT	5218 3084h
88h	32	RTIINTFLAG	5218 3088h
90h	32	RTIDWDCTRL	5218 3090h
94h	32	RTIDWDPRLD	5218 3094h
98h	32	RTIWDSTATUS	5218 3098h
9Ch	32	RTIWDKEY	5218 309Ch
A0h	32	RTIDWDCNTR	5218 30A0h
A4h	32	RTIWWDRXNCTRL	5218 30A4h
A8h	32	RTIWWDSIZECTRL	5218 30A8h
ACh	32	RTIINTCLRENABLE	5218 30ACh
B0h	32	RTICOMP0CLR	5218 30B0h
B4h	32	RTICOMP1CLR	5218 30B4h
B8h	32	RTICOMP2CLR	5218 30B8h
BCh	32	RTICOMP3CLR	5218 30BCh

4.19.1 MEM_RTIGCTRL Registers

4.19.1.1 MEM_RTIGCTRL Register (Offset = 0h) [reset = 0h]

Short Description: Global Control Register s

Long Description: Global Control Register starts / stops the counters

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Table 4-2794. Instance Table

Instance Name	Physical Address
RTI0	5218 0000h
RTI1	5218 1000h
RTI2	5218 2000h
RTI3	5218 3000h

Figure 4-1308. RTIGCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED2												NTUSEL			
R/W												R/W			
0h												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COS	RESERVED1													CNT1EN	CNT0EN
R/W	R/W													R/W	R/W
0h	0h													0h	0h

Access Types Legend

Table 4-2795. RTIGCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED2	R/W	0h	Reserved. Reads return 0 and writes have no effect
19:16	NTUSEL	R/W	0h	NTUSEL: Select NTU signal. These bits determine which NTU input signal is used as external timebase. There are up to four inputs supported with four valid selection combinations. Any invalid selection value written to the NTUSEL bit-field will result in a TIED LOW being used as the NTU signal. The NTU signal will also be TIED LOW in case of a single-bit flip as it will result in an invalid combination of NTUSEL. User and privilege mode [read]: 0000 = NTU0 0101 = NTU1 1010 = NTU2 1111 = NTU3 other = tied to 0 Privilege mode [write]: 0000 = NTU0 0101 = NTU1 1010 = NTU2 1111 = NTU3 other = tied to 0
15	COS	R/W	0h	COS: Continue On Suspend. This bit determines if both counters are stopped when the device goes into debug mode or if they continue counting. User and privilege mode [read]: 0 = counters are stopped while in debug mode 1 = counters are running while in debug mode Privilege mode [write]: 0 = stop counters in debug mode 1 = continue counting in debug mode
14:2	RESERVED1	R/W	0h	Reserved. Reads return 0 and writes have no effect
1	CNT1EN	R/W	0h	CNT1EN: Counter 1 Enable. The CNT1EN bit starts and stops the operation of counter block 1 [UC1 and FRC1]. User and privilege mode [read]: 0 = counters are stopped 1 = counters are running Privilege mode [write]: 0 = stop counters 1 = start counters Gives the absolute 32 bit destination address [physical].

Table 4-2795. RTIGCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CNT0EN	R/W	0h	CNT0EN: Counter 0 Enable.The CNT0EN bit starts and stops the operation of counter block 0 [UC0 and FRC0]. User and privilege mode [read]: 0 = counters are stopped 1 = counters are running Privilege mode [write]: 0 = stop counters 1 = start counters Gives the absolute 32 bits source address [physical].

4.19.2 MEM_RTITBCTRL Registers

4.19.2.1 MEM_RTITBCTRL Register (Offset = 4h) [reset = 0h]

Short Description: Timebase Control selectio

Long Description: Timebase Control selection which source triggers free running counter 0

Return to Summary Table

Table 4-2796. Instance Table

Instance Name	Physical Address
RTI0	5218 0004h
RTI1	5218 1004h
RTI2	5218 2004h
RTI3	5218 3004h

Figure 4-1309. RTITBCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED3															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED3														INC	TBEXT
R/W														R/W	R/W
0h														0h	0h

Access Types Legend

Table 4-2797. RTITBCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED3	R/W	0h	Reserved
1	INC	R/W	0h	INC: Increment Free Running Counter 0. This bit determines wether the Free Running Counter 0 is automatically incremented if a failing clock on the NTUx signal is detected. User and privilege mode [read]: 0 = FRC0 will not be incremented 1 = FRC0 will be incremented Privilege mode [write]: 0 = Do not increment FRC0 on failing external clock 1 = Increment FRC0 on failing external clock
0	TBEXT	R/W	0h	TBEXT: Timebase External. The Timebase External bit selects whether the Free Running Counter 0 is clocked by the internal Up Counter 0 or from the external signal NTUx. Since setting the TBEXT bit to 1 resets Up Counter 0, Free Running Counter 0 will not be incremented in this occurence. The only source which is able to increment Free Running Counter 0 is NTUx. When the Timebase Supervisor circuit detects a missing clockedge, then the TBEXT bit is reset. The selection if the external signal should be used, can only be done by software. User and privilege mode [read]: 0 = UC0 clocks FRC0 1 = NTUx clocks FRC0 Privilege mode [write]: 0 = MUX is switched to internal UC0 clocking scheme 1 = MUX is switched to external NTUx clocking scheme

4.19.3 MEM_RTICAPCTRL Registers

4.19.3.1 MEM_RTICAPCTRL Register (Offset = 8h) [reset = 0h]

Short Description: Capture Control controls

Long Description: Capture Control controls the capture source for the counters

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Table 4-2798. Instance Table

Instance Name	Physical Address
RTI0	5218 0008h
RTI1	5218 1008h
RTI2	5218 2008h
RTI3	5218 3008h

Figure 4-1310. RTICAPCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED4															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED4														CAPCNTR1	CAPCNTR0
R/W														R/W	R/W
0h														0h	0h

Access Types Legend

Table 4-2799. RTICAPCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED4	R/W	0h	Reserved. Reads return 0 and writes have no effect
1	CAPCNTR1	R/W	0h	CAPCNTR1: Capture Counter 1. This bit determines, which external interrupt source triggers a capture event of both UC1 and FRC1. User and privilege mode [read]: 0 = capture event is triggered by Capture Event Source 0 1 = capture event is triggered by Capture Event Source 1 Privilege mode [write]: 0 = enable capture event triggered by Capture Event Source 0 1 = enable capture event triggered by Capture Event Source 1
0	CAPCNTR0	R/W	0h	CAPCNTR0: Capture Counter 0. This bit determines, which external interrupt source triggers a capture event of both UC0 and FRC0. User and privilege mode [read]: 0 = capture event is triggered by Capture Event Source 0 1 = capture event is triggered by Capture Event Source 1 Privilege mode [write]: 0 = enable capture event triggered by Capture Event Source 0 1 = enable capture event triggered by Capture Event Source 1 11 indexed 10 reserved 01 post-increment 00 constant

4.19.4 MEM_RTICOMPCTRL Registers

4.19.4.1 MEM_RTICOMPCTRL Register (Offset = Ch) [reset = 0h]

Short Description: Compare Control controls

Long Description: Compare Control controls the source for the compare registers

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Table 4-2800. Instance Table

Instance Name	Physical Address
RTI0	5218 000Ch
RTI1	5218 100Ch
RTI2	5218 200Ch
RTI3	5218 300Ch

Figure 4-1311. RTICOMPCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED8															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED8			COMP 3SEL	RESERVED7			COMP 2SEL	RESERVED6			COMP 1SEL	RESERVED5			COMP 0SEL
R/W			R/W	R/W			R/W	R/W			R/W	R/W			R/W
0h			0h	0h			0h	0h			0h	0h			0h

Access Types Legend

Table 4-2801. RTICOMPCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED8	R/W	0h	Reserved. Reads return 0 and writes have no effect
12	COMP3SEL	R/W	0h	COMPSEL3: Compare Select 3. This bit determines the counter with which the compare value hold in compare register 3 is compared. User and privilege mode [read]: 0 = value will be compared with FRC 0 1 = value will be compared with FRC 1 Privilege mode [write]: 0 = enable compare with FRC 0 1 = enable compare with FRC 1
11:9	RESERVED7	R/W	0h	Reserved. Reads return 0 and writes have no effect
8	COMP2SEL	R/W	0h	COMPSEL2: Compare Select 2. This bit determines the counter with which the compare value hold in compare register 2 is compared. User and privilege mode [read]: 0 = value will be compared with FRC 0 1 = value will be compared with FRC 1 Privilege mode [write]: 0 = enable compare with FRC 0 1 = enable compare with FRC 1
7:5	RESERVED6	R/W	0h	Reserved. Reads return 0 and writes have no effect
4	COMP1SEL	R/W	0h	COMPSEL1: Compare Select 1. This bit determines the counter with which the compare value hold in compare register 1 is compared. User and privilege mode [read]: 0 = value will be compared with FRC 0 1 = value will be compared with FRC 1 Privilege mode [write]: 0 = enable compare with FRC 0 1 = enable compare with FRC 1
3:1	RESERVED5	R/W	0h	Reserved. Reads return 0 and writes have no effect
0	COMP0SEL	R/W	0h	COMPSEL0: Compare Select 0. This bit determines the counter with which the compare value hold in compare register 0 is compared. User and privilege mode [read]: 0 = value will be compared with FRC 0 1 = value will be compared with FRC 1 Privilege mode [write]: 0 = enable compare with FRC 0 1 = enable compare with FRC 1

4.19.5 MEM_RTIFRC0 Registers

4.19.5.1 MEM_RTIFRC0 Register (Offset = 10h) [reset = 0h]

Short Description: Free Running Counter 0 cu

Long Description: Free Running Counter 0 current value of free running counter 0

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Table 4-2802. Instance Table

Instance Name	Physical Address
RTI0	5218 0010h
RTI1	5218 1010h
RTI2	5218 2010h
RTI3	5218 3010h

Figure 4-1312. RTIFRC0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FRC0															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRC0															
R/W															
0h															

Access Types Legend

Table 4-2803. RTIFRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FRC0	R/W	0h	FRC0: Free Running Counter 0. This registers holds the current value of the Free Running Counter 0 and will be updated continuously. User and privilege mode [read]: current value of the counter Privilege mode [write]: The counter can be preset by writing to this register. The counter increments then from this written value upwards. Note: Presetting counters If counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC0 and RTIFRC0.

4.19.6 MEM_RTIUC0 Registers

4.19.6.1 MEM_RTIUC0 Register (Offset = 14h) [reset = 0h]

Short Description: Up Counter 0 current valu

Long Description: Up Counter 0 current value of prescale counter 0

Return to Summary Table

Table 4-2804. Instance Table

Instance Name	Physical Address
RTI0	5218 0014h
RTI1	5218 1014h
RTI2	5218 2014h
RTI3	5218 3014h

Figure 4-1313. RTIUC0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UC0															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UC0															
R/W															
0h															

Access Types Legend

Table 4-2805. RTIUC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UC0	R/W	0h	UC0: Up Counter 0. This registers holds the current value of the Up Counter 0 and prescales the RTI clock. It will be only updated by a previous read of Free Running Counter 0. This gives effectively a 64 bit read of both counters, without having the problem of a counter being updated between two consecutive reads on Up Counter 0 and Free Running Counter 0. User and privilege mode [read]: value of the counter when the Free Running Counter 0 was read Privilege mode [write]: the counter can be preset by writing to this register. The counter increments then from this written value upwards. Note: Presetting counters If counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC0 and RTIFRC0. Note: Preset value concern If the preset value is bigger than the compare value stored in register RTICPUC0 then it can take a long time until a compare matches, since RTIUC0 has to count up until it overflows.

4.19.7 MEM_RTICPUC0 Registers

4.19.7.1 MEM_RTICPUC0 Register (Offset = 18h) [reset = 0h]

Short Description: Compare Up Counter 0 comp

Long Description: Compare Up Counter 0 compare value compared with prescale counter 0

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Table 4-2806. Instance Table

Instance Name	Physical Address
RTI0	5218 0018h
RTI1	5218 1018h
RTI2	5218 2018h
RTI3	5218 3018h

Figure 4-1314. RTICPUC0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CPUC0															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPUC0															
R/W															
0h															

Access Types Legend

Table 4-2807. RTICPUC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CPUC0	R/W	0h	This registers holds the compare value, which is compared with the Up Counter 0. When the compare matches, Free Running counter 0 is incremented. The Up Counter is set to zero when the counter value matches the CPUC0 value. The value set in this prescales the RTI clock. If CPUC0 = 0: then, frequency = RTICLK/ [2^32] If CPUC0 0: then , frequency = RTICLK/[CPUC0 + 1] User and privilege mode [read]: current compare value Privilege mode [write when TBEXT = 0]: the compare value is updated Privilege mode [write when TBEXT = 1]: the compare value is not changed

4.19.8 MEM_RTICAFRC0 Registers

4.19.8.1 MEM_RTICAFRC0 Register (Offset = 20h) [reset = 0h]

Short Description: Capture Free Running Coun

Long Description: Capture Free Running Counter 0 current value of free running counter 0 on external event

Return to Summary Table

Table 4-2808. Instance Table

Instance Name	Physical Address
RTI0	5218 0020h
RTI1	5218 1020h
RTI2	5218 2020h
RTI3	5218 3020h

Figure 4-1315. RTICAFRC0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CAFRC0															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAFRC0															
R/W															
0h															

Access Types Legend

Table 4-2809. RTICAFRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAFRC0	R/W	0h	CAFRC0: Capture Free Running Counter 0. This registers captures the current value of the Free Running Counter 0 when a event occurs, controlled by the external capture control block. User and privilege mode [read]: value of Free Running Counter 0 on a capture event

4.19.9 MEM_RTICAUC0 Registers

4.19.9.1 MEM_RTICAUC0 Register (Offset = 24h) [reset = 0h]

Short Description: Capture Up Counter 0 curr

Long Description: Capture Up Counter 0 current value of prescale counter 0 on external event

Return to Summary Table

Table 4-2810. Instance Table

Instance Name	Physical Address
RTI0	5218 0024h
RTI1	5218 1024h
RTI2	5218 2024h
RTI3	5218 3024h

Figure 4-1316. RTICAUC0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CAUC0															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAUC0															
R/W															
0h															

Access Types Legend

Table 4-2811. RTICAUC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAUC0	R/W	0h	CAUC0: Capture Up Counter 0. This registers captures the current value of the Up Counter 0 when a event occurs, controlled by the external capture control block. The read sequence has to be the same as with Up Counter 0 and Free Running Counter 0. So the RTICAFRC0 register has to be read first, before the RTICAUC0 register is read. This sequence ensures that the value of the RTICAUC0 register is the corresponding value to the RTICAFRC0 register, even if another capture event happens in between the two reads. User and privilege mode [read]: value of Up Counter 0 on a capture event

4.19.10 MEM_RTIFRC1 Registers

4.19.10.1 MEM_RTIFRC1 Register (Offset = 30h) [reset = 0h]

Short Description: Free Running Counter 1 cu

Long Description: Free Running Counter 1 current value of free running counter 1

Return to Summary Table

Table 4-2812. Instance Table

Instance Name	Physical Address
RTI0	5218 0030h
RTI1	5218 1030h
RTI2	5218 2030h
RTI3	5218 3030h

Figure 4-1317. RTIFRC1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FRC1															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRC1															
R/W															
0h															

Access Types Legend

Table 4-2813. RTIFRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FRC1	R/W	0h	FRC1: Free Running Counter 1. This registers holds the current value of the Free Running Counter 1 and will be updated continuously. User and privilege mode [read]: current value of the counter Privilege mode [write]: The counter can be preset by writing to this register. The counter increments then from this written value upwards. Note: Presetting counters If counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC1 and RTIFRC1.

4.19.11 MEM_RTIUC1 Registers

4.19.11.1 MEM_RTIUC1 Register (Offset = 34h) [reset = 0h]

Short Description: Up Counter 1 current valu

Long Description: Up Counter 1 current value of prescale counter 1

Return to Summary Table

Table 4-2814. Instance Table

Instance Name	Physical Address
RTI0	5218 0034h
RTI1	5218 1034h
RTI2	5218 2034h
RTI3	5218 3034h

Figure 4-1318. RTIUC1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UC1															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UC1															
R/W															
0h															

Access Types Legend

Table 4-2815. RTIUC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UC1	R/W	0h	UC1: Up Counter 1. This registers holds the current value of the Up Counter 1 and prescales the RTI clock. It will be only updated by a previous read of Free Running Counter 1. This gives effectively a 64 bit read of both counters, without having the problem of a counter being updated between two consecutive reads on Up Counter 1 and Free Running Counter 1. User and privilege mode [read]: value of the counter when the Free Running Counter 1 was read Privilege mode [write]: the counter can be preset by writing to this register. The counter increments then from this written value upwards. Note: Presetting counters If counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC1 and RTIFRC1. Note: Preset value concern If the preset value is bigger than the compare value stored in register RTICPUC1 then it can take a long time until a compare matches, since RTIUC1 has to count up until it overflows.

4.19.12 MEM_RTICPUC1 Registers

4.19.12.1 MEM_RTICPUC1 Register (Offset = 38h) [reset = 0h]

Short Description: Compare Up Counter 1 comp

Long Description: Compare Up Counter 1 compare value compared with prescale counter 1

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Table 4-2816. Instance Table

Instance Name	Physical Address
RTI0	5218 0038h
RTI1	5218 1038h
RTI2	5218 2038h
RTI3	5218 3038h

Figure 4-1319. RTICPUC1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CPUC1															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPUC1															
R/W															
0h															

Access Types Legend

Table 4-2817. RTICPUC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CPUC1	R/W	0h	This registers holds the compare value, which is compared with the Up Counter 1. When the compare matches, Free Running Counter 1 is incremented. The Up Counter is set to zero when the counter value matches the CPUC1 value. The value set in this prescales the RTI clock. If CPUC1 = 0: then, frequency = RTICLK/ [2^32] If CPUC1 0: then , frequency = RTICLK/[CPUC1 + 1] User and privilege mode [read]: current compare value Privilege mode [write when TBEXT = 0]: the compare value is updated Privilege mode [write when TBEXT = 1]: the compare value is not changed

4.19.13 MEM_RTICAFRC1 Registers

4.19.13.1 MEM_RTICAFRC1 Register (Offset = 40h) [reset = 0h]

Short Description: Capture Free Running Coun

Long Description: Capture Free Running Counter 1 current value of free running counter 1 on external event

Return to Summary Table

Table 4-2818. Instance Table

Instance Name	Physical Address
RTI0	5218 0040h
RTI1	5218 1040h
RTI2	5218 2040h
RTI3	5218 3040h

Figure 4-1320. RTICAFRC1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CAFRC1															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAFRC1															
R/W															
0h															

Access Types Legend

Table 4-2819. RTICAFRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAFRC1	R/W	0h	CAFRC1: Capture Free Running Counter 1. This registers captures the current value of the Free Running Counter 1 when a event occurs, controlled by the external capture control block. User and privilege mode [read]: value of Free Running Counter 1 on a capture event

4.19.14 MEM_RTICAUC1 Registers

4.19.14.1 MEM_RTICAUC1 Register (Offset = 44h) [reset = 0h]

Short Description: Capture Up Counter 1 curr

Long Description: Capture Up Counter 1 current value of prescale counter 1 on external event

Return to Summary Table

Table 4-2820. Instance Table

Instance Name	Physical Address
RTI0	5218 0044h
RTI1	5218 1044h
RTI2	5218 2044h
RTI3	5218 3044h

Figure 4-1321. RTICAUC1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CAUC1															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAUC1															
R/W															
0h															

Access Types Legend

Table 4-2821. RTICAUC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAUC1	R/W	0h	CAUC1: Capture Up Counter 1. This registers captures the current value of the Up Counter 1 when a event occurs, controlled by the external capture control block. The read sequence has to be the same as with Up Counter 1 and Free Running Counter 1. So the RTICAFRC1 register has to be read first, before the RTICAUC1 register is read. This sequence ensures that the value of the RTICAUC1 register is the corresponding value to the RTICAFRC1 register, even if another capture event happens in between the two reads. User and privilege mode [read]: value of Up Counter 1 on a capture event

4.19.15 MEM_RTICOMP0 Registers

4.19.15.1 MEM_RTICOMP0 Register (Offset = 50h) [reset = 0h]

Short Description: Compare 0 compare value t

Long Description: Compare 0 compare value to be compared with the counters

Return to Summary Table

Table 4-2822. Instance Table

Instance Name	Physical Address
RTI0	5218 0050h
RTI1	5218 1050h
RTI2	5218 2050h
RTI3	5218 3050h

Figure 4-1322. RTICOMP0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP0															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP0															
R/W															
0h															

Access Types Legend

Table 4-2823. RTICOMP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP0	R/W	0h	COMP0: Compare 0. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request. User and privilege mode [read]: current compare value Privilege mode [write]: update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

4.19.16 MEM_RTIUDCP0 Registers

4.19.16.1 MEM_RTIUDCP0 Register (Offset = 54h) [reset = 0h]

Short Description: Update Compare 0 value to

Long Description: Update Compare 0 value to be added to the compare register 0 value on compare match

Return to Summary Table

Table 4-2824. Instance Table

Instance Name	Physical Address
RTI0	5218 0054h
RTI1	5218 1054h
RTI2	5218 2054h
RTI3	5218 3054h

Figure 4-1323. RTIUDCP0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UDCP0															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UDCP0															
R/W															
0h															

Access Types Legend

Table 4-2825. RTIUDCP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UDCP0	R/W	0h	UDCP0: Update Compare 0 Register. This registers holds a value, which is added to the value in the compare 0 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention. User and privilege mode [read]: value to be added to the compare 0 register on the next compare match Privilege mode [write]: new update value

4.19.17 MEM_RTICOMP1 Registers

4.19.17.1 MEM_RTICOMP1 Register (Offset = 58h) [reset = 0h]

Short Description: Compare 1 compare value t

Long Description: Compare 1 compare value to be compared with the counters

Return to Summary Table

Table 4-2826. Instance Table

Instance Name	Physical Address
RTI0	5218 0058h
RTI1	5218 1058h
RTI2	5218 2058h
RTI3	5218 3058h

Figure 4-1324. RTICOMP1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP1															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP1															
R/W															
0h															

Access Types Legend

Table 4-2827. RTICOMP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP1	R/W	0h	COMP1: compare1. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request. User and privilege mode [read]: current compare value Privilege mode [write]: update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

4.19.18 MEM_RTIUDCP1 Registers

4.19.18.1 MEM_RTIUDCP1 Register (Offset = 5Ch) [reset = 0h]

Short Description: Update Compare 1 value to

Long Description: Update Compare 1 value to be added to the compare register 1 value on compare match

Return to Summary Table

Table 4-2828. Instance Table

Instance Name	Physical Address
RTI0	5218 005Ch
RTI1	5218 105Ch
RTI2	5218 205Ch
RTI3	5218 305Ch

Figure 4-1325. RTIUDCP1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UDCP1															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UDCP1															
R/W															
0h															

Access Types Legend

Table 4-2829. RTIUDCP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UDCP1	R/W	0h	UDCP1: Update compare1 Register. This registers holds a value, which is added to the value in the compare1 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention. User and privilege mode [read]: value to be added to the compare1 register on the next compare match Privilege mode [write]: new update value

4.19.19 MEM_RTICOMP2 Registers

4.19.19.1 MEM_RTICOMP2 Register (Offset = 60h) [reset = 0h]

Short Description: Compare 2 compare value t

Long Description: Compare 2 compare value to be compared with the counters

Return to Summary Table

Table 4-2830. Instance Table

Instance Name	Physical Address
RTI0	5218 0060h
RTI1	5218 1060h
RTI2	5218 2060h
RTI3	5218 3060h

Figure 4-1326. RTICOMP2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP2															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP2															
R/W															
0h															

Access Types Legend

Table 4-2831. RTICOMP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP2	R/W	0h	COMP2: compare 2. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request. User and privilege mode [read]: current compare value Privilege mode [write]: update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

4.19.20 MEM_RTIUDCP2 Registers

4.19.20.1 MEM_RTIUDCP2 Register (Offset = 64h) [reset = 0h]

Short Description: Update Compare 2 value to

Long Description: Update Compare 2 value to be added to the compare register 2 value on compare match

Return to Summary Table

Table 4-2832. Instance Table

Instance Name	Physical Address
RTI0	5218 0064h
RTI1	5218 1064h
RTI2	5218 2064h
RTI3	5218 3064h

Figure 4-1327. RTIUDCP2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UDCP2															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UDCP2															
R/W															
0h															

Access Types Legend

Table 4-2833. RTIUDCP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UDCP2	R/W	0h	UDCP2: Update compare 2 Register. This registers holds a value, which is added to the value in the compare 2 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention. User and privilege mode [read]: value to be added to the compare 2 register on the next compare match Privilege mode [write]: new update value

4.19.21 MEM_RTICOMP3 Registers

4.19.21.1 MEM_RTICOMP3 Register (Offset = 68h) [reset = 0h]

Short Description: Compare 3 compare value t

Long Description: Compare 3 compare value to be compared with the counters

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Table 4-2834. Instance Table

Instance Name	Physical Address
RTI0	5218 0068h
RTI1	5218 1068h
RTI2	5218 2068h
RTI3	5218 3068h

Figure 4-1328. RTICOMP3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP3															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP3															
R/W															
0h															

Access Types Legend

Table 4-2835. RTICOMP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP3	R/W	0h	COMP3: compare 3. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request. User and privilege mode [read]: current compare value Privilege mode [write]: update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

4.19.22 MEM_RTIUDCP3 Registers

4.19.22.1 MEM_RTIUDCP3 Register (Offset = 6Ch) [reset = 0h]

Short Description: Update Compare 3 value to

Long Description: Update Compare 3 value to be added to the compare register 3 value on compare match

Return to Summary Table

Table 4-2836. Instance Table

Instance Name	Physical Address
RTI0	5218 006Ch
RTI1	5218 106Ch
RTI2	5218 206Ch
RTI3	5218 306Ch

Figure 4-1329. RTIUDCP3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UDCP3															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UDCP3															
R/W															
0h															

Access Types Legend

Table 4-2837. RTIUDCP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UDCP3	R/W	0h	UDCP3: Update compare 3 Register. This registers holds a value, which is added to the value in the compare 3 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention. User and privilege mode [read]: value to be added to the compare 3 register on the next compare match Privilege mode [write]: new update value

4.19.23 MEM_RTITBLCOMP Registers

4.19.23.1 MEM_RTITBLCOMP Register (Offset = 70h) [reset = 0h]

Short Description: Timebase Low Compare comp

Long Description: Timebase Low Compare compare value to activate edge detection circuit

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Table 4-2838. Instance Table

Instance Name	Physical Address
RTI0	5218 0070h
RTI1	5218 1070h
RTI2	5218 2070h
RTI3	5218 3070h

Figure 4-1330. RTITBLCOMP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TBLCOMP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBLCOMP															
R/W															
0h															

Access Types Legend

Table 4-2839. RTITBLCOMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TBLCOMP	R/W	0h	TBLCOMP: Timebase Low Compare Value. This value determines when the edge detection circuit starts monitoring the NTUx signal. It will be compared with Up Counter 0. User and privilege mode [read]: current compare value Privilege mode [write when TBEXT = 0]: the compare value is updated Privilege mode [write when TBEXT = 1]: the compare value is not changed Note: Reset behavior A reset does not generate a compare match.

4.19.24 MEM_RTITBHCOMP Registers

4.19.24.1 MEM_RTITBHCOMP Register (Offset = 74h) [reset = 0h]

Short Description: Timebase High Compare com

Long Description: Timebase High Compare compare value to deactivate edge detection circuit

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Table 4-2840. Instance Table

Instance Name	Physical Address
RTI0	5218 0074h
RTI1	5218 1074h
RTI2	5218 2074h
RTI3	5218 3074h

Figure 4-1331. RTITBHCOMP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TBHCOMP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBHCOMP															
R/W															
0h															

Access Types Legend

Table 4-2841. RTITBHCOMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TBHCOMP	R/W	0h	TBHCOMP: Timebase High Compare Value. This value determines when the edge detection circuit will stop monitoring the NTUx signal. It will be compared with Up Counter 0. RTITBHCOMP has to be less than RTICPUC0, since RTIUC0 will be reset when RTICPUC0 is reached. Example: The NTUx edge detection circuit should be active +/- 10 RTICLK cycles around RTICPUC0. RTICPUC0 = 0x00000050 RTITBLCOMP = 0x000046 RTITBHCOMP = 0x00000009 User and privilege mode [read]: current compare value Privilege mode [write when TBEXT = 0]: the compare value is updated Privilege mode [write when TBEXT = 1]: the compare value is not changed Note: Reset behavior A reset does not generate a compare match.

4.19.25 MEM_RTISETINT Registers

4.19.25.1 MEM_RTISETINT Register (Offset = 80h) [reset = 0h]

Short Description: Set Interrupt Enable sets

Long Description: Set Interrupt Enable sets interrupt enable bits int RTIINTCTRL without having to do a read-modify-write operation

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Table 4-2842. Instance Table

Instance Name	Physical Address
RTI0	5218 0080h
RTI1	5218 1080h
RTI2	5218 2080h
RTI3	5218 3080h

Figure 4-1332. RTISETINT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED11													SETOVL1INT	SETOVL0INT	SETTBINT
R/W													R/W	R/W	R/W
0h													0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED10				SETDMA3	SETDMA2	SETDMA1	SETDMA0	RESERVED9				SETINT3	SETINT2	SETINT1	SETINT0
R/W				R/W	R/W	R/W	R/W	R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h	0h				0h	0h	0h	0h

Access Types Legend

Table 4-2843. RTISETINT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED11	R/W	0h	Reserved. Reads return 0 and writes have no effect
18	SETOVL1INT	R/W	0h	SETOVL1INT: Set Free Running Counter 1 Overflow Interrupt. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable interrupt
17	SETOVL0INT	R/W	0h	SETOVL0INT: Set Free Running Counter 0 Overflow Interrupt. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable interrupt
16	SETTBINT	R/W	0h	SETTBINT: Set Timebase Interrupt. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable interrupt
15:12	RESERVED10	R/W	0h	Reserved. Reads return 0 and writes have no effect
11	SETDMA3	R/W	0h	SETDMA3: Set Compare DMA Request 3. User and privilege mode [read]: 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable DMA request
10	SETDMA2	R/W	0h	SETDMA2: Set Compare DMA Request 2. User and privilege mode [read]: 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable DMA request

Table 4-2843. RTISETINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	SETDMA1	R/W	0h	SETDMA1: Set Compare DMA Request 1. User and privilege mode [read]: 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable DMA request
8	SETDMA0	R/W	0h	SETDMA0: Set Compare DMA Request 0. User and privilege mode [read]: 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable DMA request
7:4	RESERVED9	R/W	0h	Reserved. Reads return 0 and writes have no effect
3	SETINT3	R/W	0h	SETINT3: Set Compare Interrupt 3. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged
2	SETINT2	R/W	0h	SETINT2: Set Compare Interrupt 2. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable interrupt
1	SETINT1	R/W	0h	SETINT1: Set Compare Interrupt 1. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable interrupt
0	SETINT0	R/W	0h	SETINT0: Set Compare Interrupt 0. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable interrupt

4.19.26 MEM_RTICLEARINT Registers

4.19.26.1 MEM_RTICLEARINT Register (Offset = 84h) [reset = 0h]

Short Description: Clear Interrupt Enable cl

Long Description: Clear Interrupt Enable clears interrupt enable bits int RTIINTCTRL without having to do a read-modify-write operation

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Table 4-2844. Instance Table

Instance Name	Physical Address
RTI0	5218 0084h
RTI1	5218 1084h
RTI2	5218 2084h
RTI3	5218 3084h

Figure 4-1333. RTICLEARINT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED14													CLEAROVL1INT	CLEAROVL0INT	CLEARTBINT
R/W													R/W	R/W	R/W
0h													0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED13				CLEARDMA3	CLEARDMA2	CLEARDMA1	CLEARDMA0	RESERVED12				CLEARINT3	CLEARINT2	CLEARINT1	CLEARINT0
R/W				R/W	R/W	R/W	R/W	R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h	0h				0h	0h	0h	0h

Access Types Legend

Table 4-2845. RTICLEARINT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED14	R/W	0h	Reserved. Reads return 0 and writes have no effect
18	CLEAROVL1INT	R/W	0h	CLEAROVL1INT: CLEAR Free Running Counter 1 Overflow Interrupt. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable interrupt
17	CLEAROVL0INT	R/W	0h	CLEAROVL0INT: CLEAR Free Running Counter 0 Overflow Interrupt. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable interrupt
16	CLEARTBINT	R/W	0h	CLEARTBINT: CLEAR Timebase Interrupt. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable interrupt
15:12	RESERVED13	R/W	0h	Reserved. Reads return 0 and writes have no effect
11	CLEARDMA3	R/W	0h	CLEARDMA3: CLEAR Compare DMA Request 3. User and privilege mode [read]: 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable DMA request
10	CLEARDMA2	R/W	0h	CLEARDMA2: CLEAR Compare DMA Request 2. User and privilege mode [read]: 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable DMA request

Table 4-2845. RTICLEARINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	CLEARDMA1	R/W	0h	CLEARDMA1: CLEAR Compare DMA Request 1. User and privilege mode [read]: 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable DMA request
8	CLEARDMA0	R/W	0h	CLEARDMA0: CLEAR Compare DMA Request 0. User and privilege mode [read]: 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable DMA request
7:4	RESERVED12	R/W	0h	Reserved. Reads return 0 and writes have no effect
3	CLEARINT3	R/W	0h	CLEARINT3: CLEAR Compare Interrupt 3. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable interrupt
2	CLEARINT2	R/W	0h	CLEARINT2: CLEAR Compare Interrupt 2. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable interrupt
1	CLEARINT1	R/W	0h	CLEARINT1: CLEAR Compare Interrupt 1. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable interrupt
0	CLEARINT0	R/W	0h	CLEARINT0: CLEAR Compare Interrupt 0. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable interrupt

4.19.27 MEM_RTIINTFLAG Registers

4.19.27.1 MEM_RTIINTFLAG Register (Offset = 88h) [reset = 0h]

Short Description: Interrupt Flags interrupt

Long Description: Interrupt Flags interrupt pending bits

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Table 4-2846. Instance Table

Instance Name	Physical Address
RTI0	5218 0088h
RTI1	5218 1088h
RTI2	5218 2088h
RTI3	5218 3088h

Figure 4-1334. RTIINTFLAG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED16													OVL1INT	OVL0INT	TBINT
R/W													R/W	R/W	R/W
0h													0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED15												INT3	INT2	INT1	INT0
R/W												R/W	R/W	R/W	R/W
0h												0h	0h	0h	0h

Access Types Legend

Table 4-2847. RTIINTFLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED16	R/W	0h	Reserved. Reads return 0 and writes have no effect
18	OVL1INT	R/W	0h	OVL1INT: Free Running Counter 1 Overflow Interrupt Flag. User and privilege mode [read]: determines if an interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode [write]: 0 = leaves the bit unchanged 1 = set the bit to 0
17	OVL0INT	R/W	0h	OVL0INT: Free Running Counter 0 Overflow Interrupt Flag. User and privilege mode [read]: determines if an interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode [write]: 0 = leaves the bit unchanged 1 = set the bit to 0
16	TBINT	R/W	0h	User and privilege mode [read]: this flag is set when the TBEXT bit is cleared by detection of a missing external clockedge. It will not be set by clearing TBEXT by software. determines if an interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode [write]: 0 = leaves the bit unchanged 1 = set the bit to 0
15:4	RESERVED15	R/W	0h	Reserved. Reads return 0 and writes have no effect
3	INT3	R/W	0h	INT3: Interrupt Flag 3. User and privilege mode [read]: determines if a interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode [write]: 0 = leaves the bit unchanged 1 = set the bit to 0
2	INT2	R/W	0h	INT2: Interrupt Flag 2. User and privilege mode [read]: determines if a interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode [write]: 0 = leaves the bit unchanged 1 = set the bit to 0
1	INT1	R/W	0h	INT1: Interrupt Flag 1. User and privilege mode [read]: determines if a interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode [write]: 0 = leaves the bit unchanged 1 = set the bit to 0

Table 4-2847. RTIINTFLAG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	INT0	R/W	0h	INT0: Interrupt Flag 0. User and privilege mode [read]: determines if a interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode [write]: 0 = leaves the bit unchanged 1 = set the bit to 0

4.19.28 MEM_RTIDWDCTRL Registers

4.19.28.1 MEM_RTIDWDCTRL Register (Offset = 90h) [reset = 0h]

Short Description: Digital Watchdog Control

Long Description: Digital Watchdog Control Enables the Digital Watchdog

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Table 4-2848. Instance Table

Instance Name	Physical Address
RTI0	5218 0090h
RTI1	5218 1090h
RTI2	5218 2090h
RTI3	5218 3090h

Figure 4-1335. RTIDWDCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DWDCTRL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DWDCTRL															
R/W															
0h															

Access Types Legend

Table 4-2849. RTIDWDCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DWDCTRL	R/W	0h	DWDCTRL: Digital Watchdog Control. User and priviledge mode [read]: 0x5312ACED = DWD counter is disabled. This is the default value. 0xA98559DA = DWD counter is enabled Any other value = DWD counter state is unchanged [enabled or disabled] Priviledge mode [write]: 0xA98559DA = DWD counter is enabled Any other value = State of DWD counter is unchanged [stays enabled or disabled] Note: One-Write Functionality of DWDCTRL Register The RTIDWDCTRL register implements a one-write functionality, such that the application cannot write to this registermore than once. Writing the default value will not enable the watchdog as described above. Writing the enable value will start the watchdog counters. A write to RTIDWDCTRL will only be enabled after a system reset again.

4.19.29 MEM_RTIDWDPRLD Registers

4.19.29.1 MEM_RTIDWDPRLD Register (Offset = 94h) [reset = 0h]

Short Description: Digital Watchdog Preload

Long Description: Digital Watchdog Preload sets the experation time of the Digital Watchdog

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Table 4-2850. Instance Table

Instance Name	Physical Address
RTI0	5218 0094h
RTI1	5218 1094h
RTI2	5218 2094h
RTI3	5218 3094h

Figure 4-1336. RTIDWDPRLD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED17															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED17				DWDPRLD											
R/W				R/W											
0h				0h											

Access Types Legend

Table 4-2851. RTIDWDPRLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED17	R/W	0h	Reserved. Reads return 0 and writes have no effect
11:0	DWDPRLD	R/W	0h	DWDPRLD: Digital Watchdog Preload Value. User and priviledge mode [read]: A read from this register in any CPU mode returns the current preload value. Priviledge mode [write]: If the DWD is always enabled after reset is released: The DWD starts counting down from the reset value of the counter, that is, 0x002DFFFF. The application can configure the DWD preload register any time before this down counter expires. When the application services the DWD, the preload register contents are copied left-justified into the DWD down counter and it starts counting down from that value. If the DWD is implemented such that the down counter is enabled by software: The DWD preload register can be configured only when the DWD is disabled. Therefore, the application can only configure the DWD preload register before it enables the DWD down counter. The expiration time of the DWD Down Counter can be determined with following equation: texp = [RTIDWDPRLD+1] x 2 ^ 13 / RTICLK1 where: RTIDWDPRLD = 0...4095

4.19.30 MEM_RTIWDSTATUS Registers

4.19.30.1 MEM_RTIWDSTATUS Register (Offset = 98h) [reset = 0h]

Short Description: Watchdog Status reflects

Long Description: Watchdog Status reflects the status of Analog and Digital Watchdog

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Table 4-2852. Instance Table

Instance Name	Physical Address
RTI0	5218 0098h
RTI1	5218 1098h
RTI2	5218 2098h
RTI3	5218 3098h

Figure 4-1337. RTIWDSTATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED18															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED18										DWWD_ST	ENDTIMEVIOL	STARTTIMEVIOL	KEYST	DWDST	AWDST
R/W										R/W	R/W	R/W	R/W	R/W	R/W
0h										0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-2853. RTIWDSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED18	R/W	0h	Reserved. Reads return 0 and writes have no effect
5	DWWD_ST	R/W	0h	DWWD ST: Windowed Watchdog Status. This bit denotes whether the time-window defined by the windowed watchdog configuration has been violated, or if a wrong key or key sequence was written to service the watchdog. User and priviledge mode [read]: 0 = no time-window violation has occurred. 1 = a time-window violation has occurred. The watchdog will generate either a system reset or a non-maskable interrupt to the CPU in this case. Priviledge mode [write]: 0 = leaves the current value unchanged. 1 = clears the bit to 0. This will also clear all other status flags in the RTIWDSTATUS register except for the AWD ST flag. Clearing of the status flags will deassert the non-maskable interrupt generated due to violation of the DWWD.
4	ENDTIMEVIOL	R/W	0h	END TIME VIOL: Windowed Watchdog End Time Violation Status. This bit denotes whether the end-time defined by the windowed watchdog configuration has been violated. This bit is effectively a copy of the DWD ST status flag. User and priviledge mode [read]: 0 = no end-time window violation has occurred. 1 = the end-time defined by the windowed watchdog configuration has been violated. Priviledge mode [write]: 0 = leaves the current value unchanged. 1 = clears the bit to 0.

Table 4-2853. RTIWDSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	STARTTIMEVIOL	R/W	0h	START TIME VIOL: Windowed Watchdog Start Time Violation Status. This bit denotes whether the start-time defined by the windowed watchdog configuration has been violated. This indicates that the WWD was serviced before the service window was opened. User and priviledge mode [read]: 0 = no start-time window violation has occurred. 1 = the start-time defined by the windowed watchdog configuration has been violated. Priviledge mode [write]: 0 = leaves the current value unchanged. 1 = clears the bit to 0.
2	KEYST	R/W	0h	KEYST: Watchdog KeyStatus. This bit denotes a reset generated by a wrong key or a wrong key-sequence written to the RTIWDKEY register. User and priviledge mode [read]: 0 = no wrong key or key-sequence written 1 = wrong key or key-sequence written to RTIWDKEY register Priviledge mode [write]: 0 = leaves the current value unchanged 1 = clears the bit to 0
1	DWDST	R/W	0h	DWDST: Digital Watchdog Status. This bit is effectively a copy of the END TIME VIOL status flag and is maintained for compatibility reasons. User and priviledge mode [read]: 0 = DWD timeout period not expired 1 = DWD timeout period has expired Priviledge mode [write]: 0 = leaves the current value unchanged 1 = clears the bit to 0
0	AWDST	R/W	0h	AWDST: Analog Watchdog Status. User and priviledge mode [read]: 0 = AWD pin 0 > 1 threshold not exceeded 1 = AWD pin 0 > 1 threshold exceeded Priviledge mode [write]: 0 = leaves the current value unchanged 1 = clears the bit to 0

4.19.31 MEM_RTIWDKEY Registers

4.19.31.1 MEM_RTIWDKEY Register (Offset = 9Ch) [reset = 0h]

Short Description: Watchdog Key correct writ

Long Description: Watchdog Key correct written key values discharge the external capacitor

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Table 4-2854. Instance Table

Instance Name	Physical Address
RTI0	5218 009Ch
RTI1	5218 109Ch
RTI2	5218 209Ch
RTI3	5218 309Ch

Figure 4-1338. RTIWDKEY Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED19															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDKEY															
R/W															
0h															

Access Types Legend

Table 4-2855. RTIWDKEY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED19	R/W	0h	Reserved. Reads return 0 and writes have no effect
15:0	WDKEY	R/W	0h	WDKEY: Watchdog Key. User and privilege mode reads are indeterminate. Privilege mode [write]: A write of 0xE51A followed by 0xA35C in two separate write operations defines the Key Sequence and discharges the watchdog capacitor. This also causes the upper 12 bits of the DWD down counter to be reloaded with the contents of the DWD preload register and the lower 13 bits to become all 1s. Writing any other value causes a digital watchdog reset, as shown in Table 1-3. Note: Register write access time precaution The user has to take into account that the write to the register takes 3 VCLK cycle. This needs to be considered for the AWD/DWD expiration calculation.

4.19.32 MEM_RTIDWDCNTR Registers

4.19.32.1 MEM_RTIDWDCNTR Register (Offset = A0h) [reset = 0h]

Short Description: Digital Watchdog Down Cou

Long Description: Digital Watchdog Down Counter current value of DWD down counter

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Table 4-2856. Instance Table

Instance Name	Physical Address
RTI0	5218 00A0h
RTI1	5218 10A0h
RTI2	5218 20A0h
RTI3	5218 30A0h

Figure 4-1339. RTIDWDCNTR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED20							DWDCNTR								
R/W							R/W								
0h							0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DWDCNTR															
R/W															
0h															

Access Types Legend

Table 4-2857. RTIDWDCNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED20	R/W	0h	Reserved. Reads return 0 and writes have no effect
24:0	DWDCNTR	R/W	0h	DWDCNTR: Digital Watchdog Down Counter. The value of the DWDCNTR after a system reset is 0x002D_FFFF. When the DWD is enabled and the DWD counter starts counting down from this value with an RTICLK1 time base of 3MHz, a watchdog reset will be generated in 1 second. User and privilege mode [read]: Reads return the current counter value. Privilege mode [write]: Writes dont have an effect.

4.19.33 MEM_RTIWWDRXNCTRL Registers

4.19.33.1 MEM_RTIWWDRXNCTRL Register (Offset = A4h) [reset = 0h]

Short Description: Windowed Watchdog Reactio

Long Description: Windowed Watchdog Reaction Control configures the windowed watchdog to either generate a non-maskable interrupt to the CPU or to generate a system reset

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Table 4-2858. Instance Table

Instance Name	Physical Address
RTI0	5218 00A4h
RTI1	5218 10A4h
RTI2	5218 20A4h
RTI3	5218 30A4h

Figure 4-1340. RTIWWDRXNCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED21															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED21												WWDRXN			
R/W												R/W			
0h												0h			

Access Types Legend

Table 4-2859. RTIWWDRXNCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED21	R/W	0h	Reserved. Reads return 0 and writes have no effect
3:0	WWDRXN	R/W	0h	WWDRXN: Digital Windowed Watchdog Reaction. User and privilege mode [read], privileged mode [write]: 0x5 = This is the default value. The windowed watchdog will cause a reset if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all. 0xA = The windowed watchdog will generate a non-maskable interrupt to the CPU if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all. Writing any other value will cause a system reset if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all. Note: Configuration of DWWD Reaction The DWWD reaction can be selected by the application even when the DWWD counter is already enabled. If a change to the WWDRXN is made before the watchdog service window is opened, then the change in the configuration takes effect immediately. If a change to the WWDRXN is made when the watchdog service window is already open, then the change in configuration takes effect only after the watchdog is serviced.

4.19.34 MEM_RTIWWDSIZECTRL Registers

4.19.34.1 MEM_RTIWWDSIZECTRL Register (Offset = A8h) [reset = 0h]

Short Description: Windowed Watchdog Size Co

Long Description: Windowed Watchdog Size Control configures the size of the window for the digital windowed watchdog

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Table 4-2860. Instance Table

Instance Name	Physical Address
RTI0	5218 00A8h
RTI1	5218 10A8h
RTI2	5218 20A8h
RTI3	5218 30A8h

Figure 4-1341. RTIWWDSIZECTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WWDSIZE															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WWDSIZE															
R/W															
0h															

Access Types Legend

Table 4-2861. RTIWWDSIZECTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	WWDSIZE	R/W	0h	WWDSIZE: Digital Windowed Watchdog Window Size. User and privilege mode [read], privileged mode [write]: Value written to WWDSIZE Window Size 0x00000005 100% [Functionality same as the time-out digital watchdog.] 0x00000050 50% 0x00000500 25% 0x00005000 12.5% 0x00050000 6.25% 0x00500000 3.125% Any other value 3.125% Note: Incorrect value being written to watchdog window size control register If an incorerct value is written to the WWDSIZE field, or if a system disturbance causes the WWDSIZE field to have a value other than 0x5, 0x50, 0x500, 0x5000, 0x50000, or 0x500000, then the window size will be configured to be 3.125%. This increases the chances of getting a reset due to the windowed watchdog, which enables the system to handle the cause for the incorrect configuration. Note: Configuration of DWWD Window Size The DWWD window size can be selected by the application even when the DWWD counter is already enabled. If a change to the WWDSIZE is made before the watchdog service window is opened, then the change in the configuration takes effect immediately. If a change to the WWDSIZE is made when the watchdog service window is already open, then

4.19.35 MEM_RTIINTCLRENABLE Registers

4.19.35.1 MEM_RTIINTCLRENABLE Register (Offset = ACh) [reset = 0h]

Short Description: RTI Compare Interrupt Cle

Long Description: RTI Compare Interrupt Clear Enable enable the auto clear functionality for each of the compare interrupts

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Table 4-2862. Instance Table

Instance Name	Physical Address
RTI0	5218 00ACh
RTI1	5218 10ACh
RTI2	5218 20ACh
RTI3	5218 30ACh

Figure 4-1342. RTIINTCLRENABLE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED25				INTCLRENABLE3				RESERVED24				INTCLRENABLE2			
R/W				R/W				R/W				R/W			
0h				0h				0h				0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED23				INTCLRENABLE1				RESERVED22				INTCLRENABLE0			
R/W				R/W				R/W				R/W			
0h				0h				0h				0h			

Access Types Legend

Table 4-2863. RTIINTCLRENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED25	R/W	0h	Reserved. Reads return 0 and writes have no effect
27:24	INTCLRENABLE3	R/W	0h	INTCLRENABLE3. Enables the auto-clear functionality on the compare 3 interrupt. User and Privileged mode [read]: 0x5 = Auto-clear for compare 3 interrupt is disabled. Any other value = Auto-clear for compare 3 interrupt is enabled. Privileged mode [write]: 0x5 = Disables the auto-clear functionality on the compare 3 interrupt. Any other value = Enables the auto-clear functionality on the compare 3 interrupt.
23:20	RESERVED24	R/W	0h	Reserved. Reads return 0 and writes have no effect
19:16	INTCLRENABLE2	R/W	0h	INTCLRENABLE2. Enables the auto-clear functionality on the compare 2 interrupt. User and Privileged mode [read]: 0x5 = Auto-clear for compare 2 interrupt is disabled. Any other value = Auto-clear for compare 2 interrupt is enabled. Privileged mode [write]: 0x5 = Disables the auto-clear functionality on the compare 2 interrupt. Any other value = Enables the auto-clear functionality on the compare 2 interrupt.
15:12	RESERVED23	R/W	0h	Reserved. Reads return 0 and writes have no effect
11:8	INTCLRENABLE1	R/W	0h	INTCLRENABLE1. Enables the auto-clear functionality on the compare 1 interrupt. User and Privileged mode [read]: 0x5 = Auto-clear for compare 1 interrupt is disabled. Any other value = Auto-clear for compare 1 interrupt is enabled. Privileged mode [write]: 0x5 = Disables the auto-clear functionality on the compare 1 interrupt. Any other value = Enables the auto-clear functionality on the compare 1 interrupt.
7:4	RESERVED22	R/W	0h	Reserved. Reads return 0 and writes have no effect

Table 4-2863. RTIINTCLRENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	INTCLRENABLE0	R/W	0h	INTCLRENABLE0. Enables the auto-clear functionality on the compare 0 interrupt. User and Privileged mode [read]: 0x5 = Auto-clear for compare 0 interrupt is disabled. Any other value = Auto-clear for compare 0 interrupt is enabled. Privileged mode [write]: 0x5 = Disables the auto-clear functionality on the compare 0 interrupt. Any other value = Enables the auto-clear functionality on the compare 0 interrupt.

4.19.36 MEM_RTICOMP0CLR Registers

4.19.36.1 MEM_RTICOMP0CLR Register (Offset = B0h) [reset = 0h]

Short Description: Compare 0 Clear compare v

Long Description: Compare 0 Clear compare value to be compared with the counter to clear the compare0 interrupt line

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Table 4-2864. Instance Table

Instance Name	Physical Address
RTI0	5218 00B0h
RTI1	5218 10B0h
RTI2	5218 20B0h
RTI3	5218 30B0h

Figure 4-1343. RTICOMP0CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP0CLR															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP0CLR															
R/W															
0h															

Access Types Legend

Table 4-2865. RTICOMP0CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP0CLR	R/W	0h	COMP0CLR: Compare 0 Clear. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the compare 0 interrupt or DMA request line is cleared. User and privilege mode [read]: current compare value Privilege mode [write]: update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

4.19.37 MEM_RTICOMP1CLR Registers

4.19.37.1 MEM_RTICOMP1CLR Register (Offset = B4h) [reset = 0h]

Short Description: Compare 1 Clear compare v

Long Description: Compare 1 Clear compare value to be compared with the counter to clear the compare1 interrupt line

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Table 4-2866. Instance Table

Instance Name	Physical Address
RTI0	5218 00B4h
RTI1	5218 10B4h
RTI2	5218 20B4h
RTI3	5218 30B4h

Figure 4-1344. RTICOMP1CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP1CLR															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP1CLR															
R/W															
0h															

Access Types Legend

Table 4-2867. RTICOMP1CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP1CLR	R/W	0h	COMP1CLR: Compare 1 Clear. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the Compare 1 interrupt or DMA request line is cleared. User and privilege mode [read]: current compare value Privilege mode [write]: update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

4.19.38 MEM_RTICOMP2CLR Registers

4.19.38.1 MEM_RTICOMP2CLR Register (Offset = B8h) [reset = 0h]

Short Description: Compare 2 Clear compare v

Long Description: Compare 2 Clear compare value to be compared with the counter to clear the compare2 interrupt line

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Table 4-2868. Instance Table

Instance Name	Physical Address
RTI0	5218 00B8h
RTI1	5218 10B8h
RTI2	5218 20B8h
RTI3	5218 30B8h

Figure 4-1345. RTICOMP2CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP2CLR															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP2CLR															
R/W															
0h															

Access Types Legend

Table 4-2869. RTICOMP2CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP2CLR	R/W	0h	COMP2CLR: Compare 2 Clear. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the Compare 2 interrupt or DMA request line is cleared. User and privilege mode [read]: current compare value Privilege mode [write]: update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

4.19.39 MEM_RTICOMP3CLR Registers

4.19.39.1 MEM_RTICOMP3CLR Register (Offset = BCh) [reset = 0h]

Short Description: Compare 3 Clear compare v

Long Description: Compare 3 Clear compare value to be compared with the counter to clear the compare3 interrupt line

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Table 4-2870. Instance Table

Instance Name	Physical Address
RTI0	5218 00BCh
RTI1	5218 10BCh
RTI2	5218 20BCh
RTI3	5218 30BCh

Figure 4-1346. RTICOMP3CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP3CLR															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP3CLR															
R/W															
0h															

Access Types Legend

Table 4-2871. RTICOMP3CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP3CLR	R/W	0h	COMP3CLR: Compare 3 Clear. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the Compare 3 interrupt or DMA request line is cleared. User and privilege mode [read]: current compare value Privilege mode [write]: update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

4.19.40 Access Table

Table 4-2872. Access Type Codes

Access Type	Code	Description
R/W	R/W	Read / Write

4.20 WDT Registers

Note

WDT and RTI both have similar functionality and registers. The Technical Reference Manual combines the WDT and RTI into one chapter, but the Register Addendum separates them into two chapters due to differences in base addresses.

Table 4-2873. MEM, MEM Registers, Base Address=0X0000000052100000, Length=256

Offset	Length	Register Name	WDT0 Physical Address	WDT1 Physical Address	WDT2 Physical Address
0h	32	RTIGCTRL	5210 0000h	5210 1000h	5210 2000h
4h	32	RTITBCTRL	5210 0004h	5210 1004h	5210 2004h
8h	32	RTICAPCTRL	5210 0008h	5210 1008h	5210 2008h
Ch	32	RTICOMPCTRL	5210 000Ch	5210 100Ch	5210 200Ch
10h	32	RTIFRC0	5210 0010h	5210 1010h	5210 2010h
14h	32	RTIUC0	5210 0014h	5210 1014h	5210 2014h
18h	32	RTICPUC0	5210 0018h	5210 1018h	5210 2018h
20h	32	RTICAFRC0	5210 0020h	5210 1020h	5210 2020h
24h	32	RTICAUC0	5210 0024h	5210 1024h	5210 2024h
30h	32	RTIFRC1	5210 0030h	5210 1030h	5210 2030h
34h	32	RTIUC1	5210 0034h	5210 1034h	5210 2034h
38h	32	RTICPUC1	5210 0038h	5210 1038h	5210 2038h
40h	32	RTICAFRC1	5210 0040h	5210 1040h	5210 2040h
44h	32	RTICAUC1	5210 0044h	5210 1044h	5210 2044h
50h	32	RTICOMP0	5210 0050h	5210 1050h	5210 2050h
54h	32	RTIUDCP0	5210 0054h	5210 1054h	5210 2054h
58h	32	RTICOMP1	5210 0058h	5210 1058h	5210 2058h
5Ch	32	RTIUDCP1	5210 005Ch	5210 105Ch	5210 205Ch
60h	32	RTICOMP2	5210 0060h	5210 1060h	5210 2060h
64h	32	RTIUDCP2	5210 0064h	5210 1064h	5210 2064h
68h	32	RTICOMP3	5210 0068h	5210 1068h	5210 2068h
6Ch	32	RTIUDCP3	5210 006Ch	5210 106Ch	5210 206Ch
70h	32	RTITBLCOMP	5210 0070h	5210 1070h	5210 2070h
74h	32	RTITBHCOMP	5210 0074h	5210 1074h	5210 2074h
80h	32	RTISETINT	5210 0080h	5210 1080h	5210 2080h
84h	32	RTICLEARINT	5210 0084h	5210 1084h	5210 2084h
88h	32	RTIINTFLAG	5210 0088h	5210 1088h	5210 2088h
90h	32	RTIDWDCTRL	5210 0090h	5210 1090h	5210 2090h
94h	32	RTIDWDPRLD	5210 0094h	5210 1094h	5210 2094h
98h	32	RTIWDSTATUS	5210 0098h	5210 1098h	5210 2098h
9Ch	32	RTIWDKEY	5210 009Ch	5210 109Ch	5210 209Ch
A0h	32	RTIDWDCNTR	5210 00A0h	5210 10A0h	5210 20A0h
A4h	32	RTIWWDRXNCTRL	5210 00A4h	5210 10A4h	5210 20A4h
A8h	32	RTIWWDSIZECTRL	5210 00A8h	5210 10A8h	5210 20A8h
ACh	32	RTIINTCLRENABLE	5210 00ACh	5210 10ACh	5210 20ACh
B0h	32	RTICOMP0CLR	5210 00B0h	5210 10B0h	5210 20B0h
B4h	32	RTICOMP1CLR	5210 00B4h	5210 10B4h	5210 20B4h
B8h	32	RTICOMP2CLR	5210 00B8h	5210 10B8h	5210 20B8h
BCh	32	RTICOMP3CLR	5210 00BCh	5210 10BCh	5210 20BCh

Table 4-2874. MEM, MEM Registers, Base Address=0X0000000052100000, Length=256

Offset	Length	Register Name	WDT3 Physical Address
0h	32	RTIGCTRL	5210 3000h
4h	32	RTITBCTRL	5210 3004h
8h	32	RTICAPCTRL	5210 3008h
Ch	32	RTICOMPCTRL	5210 300Ch
10h	32	RTIFRC0	5210 3010h
14h	32	RTIUC0	5210 3014h
18h	32	RTICPUC0	5210 3018h
20h	32	RTICAFRC0	5210 3020h
24h	32	RTICAUC0	5210 3024h
30h	32	RTIFRC1	5210 3030h
34h	32	RTIUC1	5210 3034h
38h	32	RTICPUC1	5210 3038h
40h	32	RTICAFRC1	5210 3040h
44h	32	RTICAUC1	5210 3044h
50h	32	RTICOMP0	5210 3050h
54h	32	RTIUDCP0	5210 3054h
58h	32	RTICOMP1	5210 3058h
5Ch	32	RTIUDCP1	5210 305Ch
60h	32	RTICOMP2	5210 3060h
64h	32	RTIUDCP2	5210 3064h
68h	32	RTICOMP3	5210 3068h
6Ch	32	RTIUDCP3	5210 306Ch
70h	32	RTITBLCOMP	5210 3070h
74h	32	RTITBHCOMP	5210 3074h
80h	32	RTISETINT	5210 3080h
84h	32	RTICLEARINT	5210 3084h
88h	32	RTIINTFLAG	5210 3088h
90h	32	RTIDWDCTRL	5210 3090h
94h	32	RTIDWDPRLD	5210 3094h
98h	32	RTIWDSTATUS	5210 3098h
9Ch	32	RTIWDKEY	5210 309Ch
A0h	32	RTIDWDCNTR	5210 30A0h
A4h	32	RTIWWDRXNCTRL	5210 30A4h
A8h	32	RTIWWDSIZECTRL	5210 30A8h
ACh	32	RTIINTCLRENABLE	5210 30ACh
B0h	32	RTICOMP0CLR	5210 30B0h
B4h	32	RTICOMP1CLR	5210 30B4h
B8h	32	RTICOMP2CLR	5210 30B8h
BCh	32	RTICOMP3CLR	5210 30BCh

4.20.1 MEM_RTIGCTRL Registers

4.20.1.1 MEM_RTIGCTRL Register (Offset = 0h) [reset = 0h]

Short Description: Global Control Register s

Long Description: Global Control Register starts / stops the counters

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Table 4-2875. Instance Table

Instance Name	Physical Address
WDT0	5210 0000h
WDT1	5210 1000h
WDT2	5210 2000h
WDT3	5210 3000h

Figure 4-1347. RTIGCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED2												NTUSEL			
R/W												R/W			
0h												0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COS	RESERVED1													CNT1EN	CNT0EN
R/W	R/W													R/W	R/W
0h	0h													0h	0h

Access Types Legend

Table 4-2876. RTIGCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED2	R/W	0h	Reserved. Reads return 0 and writes have no effect
19:16	NTUSEL	R/W	0h	NTUSEL: Select NTU signal. These bits determine which NTU input signal is used as external timebase. There are up to four inputs supported with four valid selection combinations. Any invalid selection value written to the NTUSEL bit-field will result in a TIED LOW being used as the NTU signal. The NTU signal will also be TIED LOW in case of a single-bit flip as it will result in an invalid combination of NTUSEL. User and privilege mode [read]: 0000 = NTU0 0101 = NTU1 1010 = NTU2 1111 = NTU3 other = tied to 0 Privilege mode [write]: 0000 = NTU0 0101 = NTU1 1010 = NTU2 1111 = NTU3 other = tied to 0
15	COS	R/W	0h	COS: Continue On Suspend. This bit determines if both counters are stopped when the device goes into debug mode or if they continue counting. User and privilege mode [read]: 0 = counters are stopped while in debug mode 1 = counters are running while in debug mode Privilege mode [write]: 0 = stop counters in debug mode 1 = continue counting in debug mode
14:2	RESERVED1	R/W	0h	Reserved. Reads return 0 and writes have no effect
1	CNT1EN	R/W	0h	CNT1EN: Counter 1 Enable. The CNT1EN bit starts and stops the operation of counter block 1 [UC1 and FRC1]. User and privilege mode [read]: 0 = counters are stopped 1 = counters are running Privilege mode [write]: 0 = stop counters 1 = start counters Gives the absolute 32 bit destination address [physical].

Table 4-2876. RTIGCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CNT0EN	R/W	0h	CNT0EN: Counter 0 Enable.The CNT0EN bit starts and stops the operation of counter block 0 [UC0 and FRC0]. User and privilege mode [read]: 0 = counters are stopped 1 = counters are running Privilege mode [write]: 0 = stop counters 1 = start counters Gives the absolute 32 bits source address [physical].

4.20.2 MEM_RTITBCTRL Registers

4.20.2.1 MEM_RTITBCTRL Register (Offset = 4h) [reset = 0h]

Short Description: Timebase Control selectio

Long Description: Timebase Control selection which source triggers free running counter 0

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Table 4-2877. Instance Table

Instance Name	Physical Address
WDT0	5210 0004h
WDT1	5210 1004h
WDT2	5210 2004h
WDT3	5210 3004h

Figure 4-1348. RTITBCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED3															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED3														INC	TBEXT
R/W														R/W	R/W
0h														0h	0h

Access Types Legend

Table 4-2878. RTITBCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED3	R/W	0h	Reserved
1	INC	R/W	0h	INC: Increment Free Running Counter 0. This bit determines wether the Free Running Counter 0 is automatically incremented if a failing clock on the NTUx signal is detected. User and privilege mode [read]: 0 = FRC0 will not be incremented 1 = FRC0 will be incremented Privilege mode [write]: 0 = Do not increment FRC0 on failing external clock 1 = Increment FRC0 on failing external clock
0	TBEXT	R/W	0h	TBEXT: Timebase External. The Timebase External bit selects whether the Free Running Counter 0 is clocked by the internal Up Counter 0 or from the external signal NTUx. Since setting the TBEXT bit to 1 resets Up Counter 0, Free Running Counter 0 will not be incremented in this occurence. The only source which is able to increment Free Running Counter 0 is NTUx. When the Timebase Supervisor circuit detects a missing clockedge, then the TBEXT bit is reset. The selection if the external signal should be used, can only be done by software. User and privilege mode [read]: 0 = UC0 clocks FRC0 1 = NTUx clocks FRC0 Privilege mode [write]: 0 = MUX is switched to internal UC0 clocking scheme 1 = MUX is switched to external NTUx clocking scheme

4.20.3 MEM_RTICAPCTRL Registers

4.20.3.1 MEM_RTICAPCTRL Register (Offset = 8h) [reset = 0h]

Short Description: Capture Control controls

Long Description: Capture Control controls the capture source for the counters

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Table 4-2879. Instance Table

Instance Name	Physical Address
WDT0	5210 0008h
WDT1	5210 1008h
WDT2	5210 2008h
WDT3	5210 3008h

Figure 4-1349. RTICAPCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED4															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED4														CAPCNTR1	CAPCNTR0
R/W														R/W	R/W
0h														0h	0h

Access Types Legend

Table 4-2880. RTICAPCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED4	R/W	0h	Reserved. Reads return 0 and writes have no effect
1	CAPCNTR1	R/W	0h	CAPCNTR1: Capture Counter 1. This bit determines, which external interrupt source triggers a capture event of both UC1 and FRC1. User and privilege mode [read]: 0 = capture event is triggered by Capture Event Source 0 1 = capture event is triggered by Capture Event Source 1 Privilege mode [write]: 0 = enable capture event triggered by Capture Event Source 0 1 = enable capture event triggered by Capture Event Source 1
0	CAPCNTR0	R/W	0h	CAPCNTR0: Capture Counter 0. This bit determines, which external interrupt source triggers a capture event of both UC0 and FRC0. User and privilege mode [read]: 0 = capture event is triggered by Capture Event Source 0 1 = capture event is triggered by Capture Event Source 1 Privilege mode [write]: 0 = enable capture event triggered by Capture Event Source 0 1 = enable capture event triggered by Capture Event Source 1 11 indexed 10 reserved 01 post-increment 00 constant

4.20.4 MEM_RTICOMPCTRL Registers

4.20.4.1 MEM_RTICOMPCTRL Register (Offset = Ch) [reset = 0h]

Short Description: Compare Control controls

Long Description: Compare Control controls the source for the compare registers

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Table 4-2881. Instance Table

Instance Name	Physical Address
WDT0	5210 000Ch
WDT1	5210 100Ch
WDT2	5210 200Ch
WDT3	5210 300Ch

Figure 4-1350. RTICOMPCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED8															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED8			COMP 3SEL	RESERVED7			COMP 2SEL	RESERVED6			COMP 1SEL	RESERVED5			COMP 0SEL
R/W			R/W	R/W			R/W	R/W			R/W	R/W			R/W
0h			0h	0h			0h	0h			0h	0h			0h

Access Types Legend

Table 4-2882. RTICOMPCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED8	R/W	0h	Reserved. Reads return 0 and writes have no effect
12	COMP3SEL	R/W	0h	COMPSEL3: Compare Select 3. This bit determines the counter with which the compare value hold in compare register 3 is compared. User and privilege mode [read]: 0 = value will be compared with FRC 0 1 = value will be compared with FRC 1 Privilege mode [write]: 0 = enable compare with FRC 0 1 = enable compare with FRC 1
11:9	RESERVED7	R/W	0h	Reserved. Reads return 0 and writes have no effect
8	COMP2SEL	R/W	0h	COMPSEL2: Compare Select 2. This bit determines the counter with which the compare value hold in compare register 2 is compared. User and privilege mode [read]: 0 = value will be compared with FRC 0 1 = value will be compared with FRC 1 Privilege mode [write]: 0 = enable compare with FRC 0 1 = enable compare with FRC 1
7:5	RESERVED6	R/W	0h	Reserved. Reads return 0 and writes have no effect
4	COMP1SEL	R/W	0h	COMPSEL1: Compare Select 1. This bit determines the counter with which the compare value hold in compare register 1 is compared. User and privilege mode [read]: 0 = value will be compared with FRC 0 1 = value will be compared with FRC 1 Privilege mode [write]: 0 = enable compare with FRC 0 1 = enable compare with FRC 1
3:1	RESERVED5	R/W	0h	Reserved. Reads return 0 and writes have no effect
0	COMP0SEL	R/W	0h	COMPSEL0: Compare Select 0. This bit determines the counter with which the compare value hold in compare register 0 is compared. User and privilege mode [read]: 0 = value will be compared with FRC 0 1 = value will be compared with FRC 1 Privilege mode [write]: 0 = enable compare with FRC 0 1 = enable compare with FRC 1

4.20.5 MEM_RTIFRC0 Registers

4.20.5.1 MEM_RTIFRC0 Register (Offset = 10h) [reset = 0h]

Short Description: Free Running Counter 0 cu

Long Description: Free Running Counter 0 current value of free running counter 0

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Table 4-2883. Instance Table

Instance Name	Physical Address
WDT0	5210 0010h
WDT1	5210 1010h
WDT2	5210 2010h
WDT3	5210 3010h

Figure 4-1351. RTIFRC0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FRC0															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRC0															
R/W															
0h															

Access Types Legend

Table 4-2884. RTIFRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FRC0	R/W	0h	FRC0: Free Running Counter 0. This registers holds the current value of the Free Running Counter 0 and will be updated continuously. User and privilege mode [read]: current value of the counter Privilege mode [write]: The counter can be preset by writing to this register. The counter increments then from this written value upwards. Note: Presetting counters If counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC0 and RTIFRC0.

4.20.6 MEM_RTIUC0 Registers

4.20.6.1 MEM_RTIUC0 Register (Offset = 14h) [reset = 0h]

Short Description: Up Counter 0 current valu

Long Description: Up Counter 0 current value of prescale counter 0

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Table 4-2885. Instance Table

Instance Name	Physical Address
WDT0	5210 0014h
WDT1	5210 1014h
WDT2	5210 2014h
WDT3	5210 3014h

Figure 4-1352. RTIUC0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UC0															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UC0															
R/W															
0h															

Access Types Legend

Table 4-2886. RTIUC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UC0	R/W	0h	UC0: Up Counter 0. This registers holds the current value of the Up Counter 0 and prescales the RTI clock. It will be only updated by a previous read of Free Running Counter 0. This gives effectively a 64 bit read of both counters, without having the problem of a counter being updated between two consecutive reads on Up Counter 0 and Free Running Counter 0. User and privilege mode [read]: value of the counter when the Free Running Counter 0 was read Privilege mode [write]: the counter can be preset by writing to this register. The counter increments then from this written value upwards. Note: Presetting counters If counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC0 and RTIFRC0. Note: Preset value concern If the preset value is bigger than the compare value stored in register RTICPUC0 then it can take a long time until a compare matches, since RTIUC0 has to count up until it overflows.

4.20.7 MEM_RTICPUC0 Registers

4.20.7.1 MEM_RTICPUC0 Register (Offset = 18h) [reset = 0h]

Short Description: Compare Up Counter 0 comp

Long Description: Compare Up Counter 0 compare value compared with prescale counter 0

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Table 4-2887. Instance Table

Instance Name	Physical Address
WDT0	5210 0018h
WDT1	5210 1018h
WDT2	5210 2018h
WDT3	5210 3018h

Figure 4-1353. RTICPUC0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CPUC0															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPUC0															
R/W															
0h															

Access Types Legend

Table 4-2888. RTICPUC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CPUC0	R/W	0h	This registers holds the compare value, which is compared with the Up Counter 0. When the compare matches, Free Running counter 0 is incremented. The Up Counter is set to zero when the counter value matches the CPUC0 value. The value set in this prescales the RTI clock. If CPUC0 = 0: then, frequency = RTICLK/ [2^32] If CPUC0 0: then , frequency = RTICLK/[CPUC0 + 1] User and privilege mode [read]: current compare value Privilege mode [write when TBEXT = 0]: the compare value is updated Privilege mode [write when TBEXT = 1]: the compare value is not changed

4.20.8 MEM_RTICAFRC0 Registers

4.20.8.1 MEM_RTICAFRC0 Register (Offset = 20h) [reset = 0h]

Short Description: Capture Free Running Coun

Long Description: Capture Free Running Counter 0 current value of free running counter 0 on external event

Return to Summary Table

Table 4-2889. Instance Table

Instance Name	Physical Address
WDT0	5210 0020h
WDT1	5210 1020h
WDT2	5210 2020h
WDT3	5210 3020h

Figure 4-1354. RTICAFRC0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CAFRC0															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAFRC0															
R/W															
0h															

Access Types Legend

Table 4-2890. RTICAFRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAFRC0	R/W	0h	CAFRC0: Capture Free Running Counter 0. This registers captures the current value of the Free Running Counter 0 when a event occurs, controlled by the external capture control block. User and privilege mode [read]: value of Free Running Counter 0 on a capture event

4.20.9 MEM_RTICAUC0 Registers

4.20.9.1 MEM_RTICAUC0 Register (Offset = 24h) [reset = 0h]

Short Description: Capture Up Counter 0 curr

Long Description: Capture Up Counter 0 current value of prescale counter 0 on external event

Return to Summary Table

Table 4-2891. Instance Table

Instance Name	Physical Address
WDT0	5210 0024h
WDT1	5210 1024h
WDT2	5210 2024h
WDT3	5210 3024h

Figure 4-1355. RTICAUC0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CAUC0															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAUC0															
R/W															
0h															

Access Types Legend

Table 4-2892. RTICAUC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAUC0	R/W	0h	CAUC0: Capture Up Counter 0. This registers captures the current value of the Up Counter 0 when a event occurs, controlled by the external capture control block. The read sequence has to be the same as with Up Counter 0 and Free Running Counter 0. So the RTICAFRC0 register has to be read first, before the RTICAUC0 register is read. This sequence ensures that the value of the RTICAUC0 register is the corresponding value to the RTICAFRC0 register, even if another capture event happens in between the two reads. User and privilege mode [read]: value of Up Counter 0 on a capture event

4.20.10 MEM_RTIFRC1 Registers

4.20.10.1 MEM_RTIFRC1 Register (Offset = 30h) [reset = 0h]

Short Description: Free Running Counter 1 cu

Long Description: Free Running Counter 1 current value of free running counter 1

Return to Summary Table

Table 4-2893. Instance Table

Instance Name	Physical Address
WDT0	5210 0030h
WDT1	5210 1030h
WDT2	5210 2030h
WDT3	5210 3030h

Figure 4-1356. RTIFRC1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FRC1															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRC1															
R/W															
0h															

Access Types Legend

Table 4-2894. RTIFRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FRC1	R/W	0h	FRC1: Free Running Counter 1. This registers holds the current value of the Free Running Counter 1 and will be updated continuously. User and privilege mode [read]: current value of the counter Privilege mode [write]: The counter can be preset by writing to this register. The counter increments then from this written value upwards. Note: Presetting counters If counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC1 and RTIFRC1.

4.20.11 MEM_RTIUC1 Registers

4.20.11.1 MEM_RTIUC1 Register (Offset = 34h) [reset = 0h]

Short Description: Up Counter 1 current valu

Long Description: Up Counter 1 current value of prescale counter 1

Return to Summary Table

Table 4-2895. Instance Table

Instance Name	Physical Address
WDT0	5210 0034h
WDT1	5210 1034h
WDT2	5210 2034h
WDT3	5210 3034h

Figure 4-1357. RTIUC1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UC1															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UC1															
R/W															
0h															

Access Types Legend

Table 4-2896. RTIUC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UC1	R/W	0h	UC1: Up Counter 1. This registers holds the current value of the Up Counter 1 and prescales the RTI clock. It will be only updated by a previous read of Free Running Counter 1. This gives effectively a 64 bit read of both counters, without having the problem of a counter being updated between two consecutive reads on Up Counter 1 and Free Running Counter 1. User and privilege mode [read]: value of the counter when the Free Running Counter 1 was read Privilege mode [write]: the counter can be preset by writing to this register. The counter increments then from this written value upwards. Note: Presetting counters If counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC1 and RTIFRC1. Note: Preset value concern If the preset value is bigger than the compare value stored in register RTICPUC1 then it can take a long time until a compare matches, since RTIUC1 has to count up until it overflows.

4.20.12 MEM_RTICPUC1 Registers

4.20.12.1 MEM_RTICPUC1 Register (Offset = 38h) [reset = 0h]

Short Description: Compare Up Counter 1 comp

Long Description: Compare Up Counter 1 compare value compared with prescale counter 1

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Table 4-2897. Instance Table

Instance Name	Physical Address
WDT0	5210 0038h
WDT1	5210 1038h
WDT2	5210 2038h
WDT3	5210 3038h

Figure 4-1358. RTICPUC1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CPUC1															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPUC1															
R/W															
0h															

Access Types Legend

Table 4-2898. RTICPUC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CPUC1	R/W	0h	This registers holds the compare value, which is compared with the Up Counter 1. When the compare matches, Free Running Counter 1 is incremented. The Up Counter is set to zero when the counter value matches the CPUC1 value. The value set in this prescales the RTI clock. If CPUC1 = 0: then, frequency = RTICLK/ [2^32] If CPUC1 0: then , frequency = RTICLK/[CPUC1 + 1] User and privilege mode [read]: current compare value Privilege mode [write when TBEXT = 0]: the compare value is updated Privilege mode [write when TBEXT = 1]: the compare value is not changed

4.20.13 MEM_RTICAFRC1 Registers

4.20.13.1 MEM_RTICAFRC1 Register (Offset = 40h) [reset = 0h]

Short Description: Capture Free Running Coun

Long Description: Capture Free Running Counter 1 current value of free running counter 1 on external event

Return to Summary Table

Table 4-2899. Instance Table

Instance Name	Physical Address
WDT0	5210 0040h
WDT1	5210 1040h
WDT2	5210 2040h
WDT3	5210 3040h

Figure 4-1359. RTICAFRC1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CAFRC1															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAFRC1															
R/W															
0h															

Access Types Legend

Table 4-2900. RTICAFRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAFRC1	R/W	0h	CAFRC1: Capture Free Running Counter 1. This registers captures the current value of the Free Running Counter 1 when a event occurs, controlled by the external capture control block. User and privilege mode [read]: value of Free Running Counter 1 on a capture event

4.20.14 MEM_RTICAUC1 Registers

4.20.14.1 MEM_RTICAUC1 Register (Offset = 44h) [reset = 0h]

Short Description: Capture Up Counter 1 curr

Long Description: Capture Up Counter 1 current value of prescale counter 1 on external event

Return to Summary Table

Table 4-2901. Instance Table

Instance Name	Physical Address
WDT0	5210 0044h
WDT1	5210 1044h
WDT2	5210 2044h
WDT3	5210 3044h

Figure 4-1360. RTICAUC1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CAUC1															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAUC1															
R/W															
0h															

Access Types Legend

Table 4-2902. RTICAUC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAUC1	R/W	0h	CAUC1: Capture Up Counter 1. This registers captures the current value of the Up Counter 1 when a event occurs, controlled by the external capture control block. The read sequence has to be the same as with Up Counter 1 and Free Running Counter 1. So the RTICAFRC1 register has to be read first, before the RTICAUC1 register is read. This sequence ensures that the value of the RTICAUC1 register is the corresponding value to the RTICAFRC1 register, even if another capture event happens in between the two reads. User and privilege mode [read]: value of Up Counter 1 on a capture event

4.20.15 MEM_RTICOMP0 Registers

4.20.15.1 MEM_RTICOMP0 Register (Offset = 50h) [reset = 0h]

Short Description: Compare 0 compare value t

Long Description: Compare 0 compare value to be compared with the counters

Return to Summary Table

Table 4-2903. Instance Table

Instance Name	Physical Address
WDT0	5210 0050h
WDT1	5210 1050h
WDT2	5210 2050h
WDT3	5210 3050h

Figure 4-1361. RTICOMP0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP0															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP0															
R/W															
0h															

Access Types Legend

Table 4-2904. RTICOMP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP0	R/W	0h	COMP0: Compare 0. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request. User and privilege mode [read]: current compare value Privilege mode [write]: update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

4.20.16 MEM_RTIUDCP0 Registers

4.20.16.1 MEM_RTIUDCP0 Register (Offset = 54h) [reset = 0h]

Short Description: Update Compare 0 value to

Long Description: Update Compare 0 value to be added to the compare register 0 value on compare match

Return to Summary Table

Table 4-2905. Instance Table

Instance Name	Physical Address
WDT0	5210 0054h
WDT1	5210 1054h
WDT2	5210 2054h
WDT3	5210 3054h

Figure 4-1362. RTIUDCP0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UDCP0															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UDCP0															
R/W															
0h															

Access Types Legend

Table 4-2906. RTIUDCP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UDCP0	R/W	0h	UDCP0: Update Compare 0 Register. This registers holds a value, which is added to the value in the compare 0 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention. User and privilege mode [read]: value to be added to the compare 0 register on the next compare match Privilege mode [write]: new update value

4.20.17 MEM_RTICOMP1 Registers

4.20.17.1 MEM_RTICOMP1 Register (Offset = 58h) [reset = 0h]

Short Description: Compare 1 compare value t

Long Description: Compare 1 compare value to be compared with the counters

Return to Summary Table

Table 4-2907. Instance Table

Instance Name	Physical Address
WDT0	5210 0058h
WDT1	5210 1058h
WDT2	5210 2058h
WDT3	5210 3058h

Figure 4-1363. RTICOMP1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP1															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP1															
R/W															
0h															

Access Types Legend

Table 4-2908. RTICOMP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP1	R/W	0h	COMP1: compare1. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request. User and privilege mode [read]: current compare value Privilege mode [write]: update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

4.20.18 MEM_RTIUDCP1 Registers

4.20.18.1 MEM_RTIUDCP1 Register (Offset = 5Ch) [reset = 0h]

Short Description: Update Compare 1 value to

Long Description: Update Compare 1 value to be added to the compare register 1 value on compare match

Return to Summary Table

Table 4-2909. Instance Table

Instance Name	Physical Address
WDT0	5210 005Ch
WDT1	5210 105Ch
WDT2	5210 205Ch
WDT3	5210 305Ch

Figure 4-1364. RTIUDCP1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UDCP1															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UDCP1															
R/W															
0h															

Access Types Legend

Table 4-2910. RTIUDCP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UDCP1	R/W	0h	UDCP1: Update compare1 Register. This registers holds a value, which is added to the value in the compare1 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention. User and privilege mode [read]: value to be added to the compare1 register on the next compare match Privilege mode [write]: new update value

4.20.19 MEM_RTICOMP2 Registers

4.20.19.1 MEM_RTICOMP2 Register (Offset = 60h) [reset = 0h]

Short Description: Compare 2 compare value t

Long Description: Compare 2 compare value to be compared with the counters

Return to Summary Table

Table 4-2911. Instance Table

Instance Name	Physical Address
WDT0	5210 0060h
WDT1	5210 1060h
WDT2	5210 2060h
WDT3	5210 3060h

Figure 4-1365. RTICOMP2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP2															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP2															
R/W															
0h															

Access Types Legend

Table 4-2912. RTICOMP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP2	R/W	0h	COMP2: compare 2. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request. User and privilege mode [read]: current compare value Privilege mode [write]: update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

4.20.20 MEM_RTIUDCP2 Registers

4.20.20.1 MEM_RTIUDCP2 Register (Offset = 64h) [reset = 0h]

Short Description: Update Compare 2 value to

Long Description: Update Compare 2 value to be added to the compare register 2 value on compare match

Return to Summary Table

Table 4-2913. Instance Table

Instance Name	Physical Address
WDT0	5210 0064h
WDT1	5210 1064h
WDT2	5210 2064h
WDT3	5210 3064h

Figure 4-1366. RTIUDCP2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UDCP2															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UDCP2															
R/W															
0h															

Access Types Legend

Table 4-2914. RTIUDCP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UDCP2	R/W	0h	UDCP2: Update compare 2 Register. This registers holds a value, which is added to the value in the compare 2 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention. User and privilege mode [read]: value to be added to the compare 2 register on the next compare match Privilege mode [write]: new update value

4.20.21 MEM_RTICOMP3 Registers

4.20.21.1 MEM_RTICOMP3 Register (Offset = 68h) [reset = 0h]

Short Description: Compare 3 compare value t

Long Description: Compare 3 compare value to be compared with the counters

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Table 4-2915. Instance Table

Instance Name	Physical Address
WDT0	5210 0068h
WDT1	5210 1068h
WDT2	5210 2068h
WDT3	5210 3068h

Figure 4-1367. RTICOMP3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP3															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP3															
R/W															
0h															

Access Types Legend

Table 4-2916. RTICOMP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP3	R/W	0h	COMP3: compare 3. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request. User and privilege mode [read]: current compare value Privilege mode [write]: update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

4.20.22 MEM_RTIUDCP3 Registers

4.20.22.1 MEM_RTIUDCP3 Register (Offset = 6Ch) [reset = 0h]

Short Description: Update Compare 3 value to

Long Description: Update Compare 3 value to be added to the compare register 3 value on compare match

Return to Summary Table

Table 4-2917. Instance Table

Instance Name	Physical Address
WDT0	5210 006Ch
WDT1	5210 106Ch
WDT2	5210 206Ch
WDT3	5210 306Ch

Figure 4-1368. RTIUDCP3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UDCP3															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UDCP3															
R/W															
0h															

Access Types Legend

Table 4-2918. RTIUDCP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UDCP3	R/W	0h	UDCP3: Update compare 3 Register. This registers holds a value, which is added to the value in the compare 3 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention. User and privilege mode [read]: value to be added to the compare 3 register on the next compare match Privilege mode [write]: new update value

4.20.23 MEM_RTITBLCOMP Registers

4.20.23.1 MEM_RTITBLCOMP Register (Offset = 70h) [reset = 0h]

Short Description: Timebase Low Compare comp

Long Description: Timebase Low Compare compare value to activate edge detection circuit

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Table 4-2919. Instance Table

Instance Name	Physical Address
WDT0	5210 0070h
WDT1	5210 1070h
WDT2	5210 2070h
WDT3	5210 3070h

Figure 4-1369. RTITBLCOMP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TBLCOMP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBLCOMP															
R/W															
0h															

Access Types Legend

Table 4-2920. RTITBLCOMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TBLCOMP	R/W	0h	TBLCOMP: Timebase Low Compare Value. This value determines when the edge detection circuit starts monitoring the NTUx signal. It will be compared with Up Counter 0. User and privilege mode [read]: current compare value Privilege mode [write when TBEXT = 0]: the compare value is updated Privilege mode [write when TBEXT = 1]: the compare value is not changed Note: Reset behavior A reset does not generate a compare match.

4.20.24 MEM_RTITBHCOMP Registers

4.20.24.1 MEM_RTITBHCOMP Register (Offset = 74h) [reset = 0h]

Short Description: Timebase High Compare com

Long Description: Timebase High Compare compare value to deactivate edge detection circuit

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Table 4-2921. Instance Table

Instance Name	Physical Address
WDT0	5210 0074h
WDT1	5210 1074h
WDT2	5210 2074h
WDT3	5210 3074h

Figure 4-1370. RTITBHCOMP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TBHCOMP															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBHCOMP															
R/W															
0h															

Access Types Legend

Table 4-2922. RTITBHCOMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TBHCOMP	R/W	0h	TBHCOMP: Timebase High Compare Value. This value determines when the edge detection circuit will stop monitoring the NTUx signal. It will be compared with Up Counter 0. RTITBHCOMP has to be less than RTICPUC0, since RTIUC0 will be reset when RTICPUC0 is reached. Example: The NTUx edge detection circuit should be active +/- 10 RTICLK cycles around RTICPUC0. RTICPUC0 = 0x00000050 RTITBLCOMP = 0x000046 RTITBHCOMP = 0x00000009 User and privilege mode [read]: current compare value Privilege mode [write when TBEXT = 0]: the compare value is updated Privilege mode [write when TBEXT = 1]: the compare value is not changed Note: Reset behavior A reset does not generate a compare match.

4.20.25 MEM_RTISETINT Registers

4.20.25.1 MEM_RTISETINT Register (Offset = 80h) [reset = 0h]

Short Description: Set Interrupt Enable sets

Long Description: Set Interrupt Enable sets interrupt enable bits int RTIINTCTRL without having to do a read-modify-write operation

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Table 4-2923. Instance Table

Instance Name	Physical Address
WDT0	5210 0080h
WDT1	5210 1080h
WDT2	5210 2080h
WDT3	5210 3080h

Figure 4-1371. RTISETINT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED11													SETOVL1INT	SETOVL0INT	SETTBINT
R/W													R/W	R/W	R/W
0h													0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED10				SETDMA3	SETDMA2	SETDMA1	SETDMA0	RESERVED9				SETINT3	SETINT2	SETINT1	SETINT0
R/W				R/W	R/W	R/W	R/W	R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h	0h				0h	0h	0h	0h

Access Types Legend

Table 4-2924. RTISETINT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED11	R/W	0h	Reserved. Reads return 0 and writes have no effect
18	SETOVL1INT	R/W	0h	SETOVL1INT: Set Free Running Counter 1 Overflow Interrupt. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable interrupt
17	SETOVL0INT	R/W	0h	SETOVL0INT: Set Free Running Counter 0 Overflow Interrupt. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable interrupt
16	SETTBINT	R/W	0h	SETTBINT: Set Timebase Interrupt. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable interrupt
15:12	RESERVED10	R/W	0h	Reserved. Reads return 0 and writes have no effect
11	SETDMA3	R/W	0h	SETDMA3: Set Compare DMA Request 3. User and privilege mode [read]: 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable DMA request
10	SETDMA2	R/W	0h	SETDMA2: Set Compare DMA Request 2. User and privilege mode [read]: 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable DMA request

Table 4-2924. RTISETINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	SETDMA1	R/W	0h	SETDMA1: Set Compare DMA Request 1. User and privilege mode [read]: 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable DMA request
8	SETDMA0	R/W	0h	SETDMA0: Set Compare DMA Request 0. User and privilege mode [read]: 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable DMA request
7:4	RESERVED9	R/W	0h	Reserved. Reads return 0 and writes have no effect
3	SETINT3	R/W	0h	SETINT3: Set Compare Interrupt 3. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged
2	SETINT2	R/W	0h	SETINT2: Set Compare Interrupt 2. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable interrupt
1	SETINT1	R/W	0h	SETINT1: Set Compare Interrupt 1. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable interrupt
0	SETINT0	R/W	0h	SETINT0: Set Compare Interrupt 0. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable interrupt

4.20.26 MEM_RTICLEARINT Registers

4.20.26.1 MEM_RTICLEARINT Register (Offset = 84h) [reset = 0h]

Short Description: Clear Interrupt Enable cl

Long Description: Clear Interrupt Enable clears interrupt enable bits int RTIINTCTRL without having to do a read-modify-write operation

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Table 4-2925. Instance Table

Instance Name	Physical Address
WDT0	5210 0084h
WDT1	5210 1084h
WDT2	5210 2084h
WDT3	5210 3084h

Figure 4-1372. RTICLEARINT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED14													CLEAROVL1INT	CLEAROVL0INT	CLEARTBINT
R/W													R/W	R/W	R/W
0h													0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED13				CLEARDMA3	CLEARDMA2	CLEARDMA1	CLEARDMA0	RESERVED12				CLEARINT3	CLEARINT2	CLEARINT1	CLEARINT0
R/W				R/W	R/W	R/W	R/W	R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h	0h				0h	0h	0h	0h

Access Types Legend

Table 4-2926. RTICLEARINT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED14	R/W	0h	Reserved. Reads return 0 and writes have no effect
18	CLEAROVL1INT	R/W	0h	CLEAROVL1INT: CLEAR Free Running Counter 1 Overflow Interrupt. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable interrupt
17	CLEAROVL0INT	R/W	0h	CLEAROVL0INT: CLEAR Free Running Counter 0 Overflow Interrupt. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable interrupt
16	CLEARTBINT	R/W	0h	CLEARTBINT: CLEAR Timebase Interrupt. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable interrupt
15:12	RESERVED13	R/W	0h	Reserved. Reads return 0 and writes have no effect
11	CLEARDMA3	R/W	0h	CLEARDMA3: CLEAR Compare DMA Request 3. User and privilege mode [read]: 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable DMA request
10	CLEARDMA2	R/W	0h	CLEARDMA2: CLEAR Compare DMA Request 2. User and privilege mode [read]: 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable DMA request

Table 4-2926. RTICLEARINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	CLEARDMA1	R/W	0h	CLEARDMA1: CLEAR Compare DMA Request 1. User and privilege mode [read]: 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable DMA request
8	CLEARDMA0	R/W	0h	CLEARDMA0: CLEAR Compare DMA Request 0. User and privilege mode [read]: 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable DMA request
7:4	RESERVED12	R/W	0h	Reserved. Reads return 0 and writes have no effect
3	CLEARINT3	R/W	0h	CLEARINT3: CLEAR Compare Interrupt 3. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable interrupt
2	CLEARINT2	R/W	0h	CLEARINT2: CLEAR Compare Interrupt 2. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable interrupt
1	CLEARINT1	R/W	0h	CLEARINT1: CLEAR Compare Interrupt 1. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable interrupt
0	CLEARINT0	R/W	0h	CLEARINT0: CLEAR Compare Interrupt 0. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable interrupt

4.20.27 MEM_RTIINTFLAG Registers

4.20.27.1 MEM_RTIINTFLAG Register (Offset = 88h) [reset = 0h]

Short Description: Interrupt Flags interrupt

Long Description: Interrupt Flags interrupt pending bits

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Table 4-2927. Instance Table

Instance Name	Physical Address
WDT0	5210 0088h
WDT1	5210 1088h
WDT2	5210 2088h
WDT3	5210 3088h

Figure 4-1373. RTIINTFLAG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED16													OVL1INT	OVL0INT	TBINT
R/W													R/W	R/W	R/W
0h													0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED15												INT3	INT2	INT1	INT0
R/W												R/W	R/W	R/W	R/W
0h												0h	0h	0h	0h

Access Types Legend

Table 4-2928. RTIINTFLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED16	R/W	0h	Reserved. Reads return 0 and writes have no effect
18	OVL1INT	R/W	0h	OVL1INT: Free Running Counter 1 Overflow Interrupt Flag. User and privilege mode [read]: determines if an interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode [write]: 0 = leaves the bit unchanged 1 = set the bit to 0
17	OVL0INT	R/W	0h	OVL0INT: Free Running Counter 0 Overflow Interrupt Flag. User and privilege mode [read]: determines if an interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode [write]: 0 = leaves the bit unchanged 1 = set the bit to 0
16	TBINT	R/W	0h	User and privilege mode [read]: this flag is set when the TBEXT bit is cleared by detection of a missing external clockedge. It will not be set by clearing TBEXT by software. determines if an interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode [write]: 0 = leaves the bit unchanged 1 = set the bit to 0
15:4	RESERVED15	R/W	0h	Reserved. Reads return 0 and writes have no effect
3	INT3	R/W	0h	INT3: Interrupt Flag 3. User and privilege mode [read]: determines if a interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode [write]: 0 = leaves the bit unchanged 1 = set the bit to 0
2	INT2	R/W	0h	INT2: Interrupt Flag 2. User and privilege mode [read]: determines if a interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode [write]: 0 = leaves the bit unchanged 1 = set the bit to 0
1	INT1	R/W	0h	INT1: Interrupt Flag 1. User and privilege mode [read]: determines if a interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode [write]: 0 = leaves the bit unchanged 1 = set the bit to 0

Table 4-2928. RTIINTFLAG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	INT0	R/W	0h	INT0: Interrupt Flag 0. User and privilege mode [read]: determines if a interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode [write]: 0 = leaves the bit unchanged 1 = set the bit to 0

4.20.28 MEM_RTIDWDCTRL Registers

4.20.28.1 MEM_RTIDWDCTRL Register (Offset = 90h) [reset = 0h]

Short Description: Digital Watchdog Control

Long Description: Digital Watchdog Control Enables the Digital Watchdog

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Table 4-2929. Instance Table

Instance Name	Physical Address
WDT0	5210 0090h
WDT1	5210 1090h
WDT2	5210 2090h
WDT3	5210 3090h

Figure 4-1374. RTIDWDCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DWDCTRL															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DWDCTRL															
R/W															
0h															

Access Types Legend

Table 4-2930. RTIDWDCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DWDCTRL	R/W	0h	DWDCTRL: Digital Watchdog Control. User and priviledge mode [read]: 0x5312ACED = DWD counter is disabled. This is the default value. 0xA98559DA = DWD counter is enabled Any other value = DWD counter state is unchanged [enabled or disabled] Priviledge mode [write]: 0xA98559DA = DWD counter is enabled Any other value = State of DWD counter is unchanged [stays enabled or disabled] Note: One-Write Functionality of DWDCTRL Register The RTIDWDCTRL register implements a one-write functionality, such that the application cannot write to this registermore than once. Writing the default value will not enable the watchdog as described above. Writing the enable value will start the watchdog counters. A write to RTIDWDCTRL will only be enabled after a system reset again.

4.20.29 MEM_RTIDWDPRLD Registers

4.20.29.1 MEM_RTIDWDPRLD Register (Offset = 94h) [reset = 0h]

Short Description: Digital Watchdog Preload

Long Description: Digital Watchdog Preload sets the experation time of the Digital Watchdog

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Table 4-2931. Instance Table

Instance Name	Physical Address
WDT0	5210 0094h
WDT1	5210 1094h
WDT2	5210 2094h
WDT3	5210 3094h

Figure 4-1375. RTIDWDPRLD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED17															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED17				DWDPRLD											
R/W				R/W											
0h				0h											

Access Types Legend

Table 4-2932. RTIDWDPRLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED17	R/W	0h	Reserved. Reads return 0 and writes have no effect
11:0	DWDPRLD	R/W	0h	DWDPRLD: Digital Watchdog Preload Value. User and priviledge mode [read]: A read from this register in any CPU mode returns the current preload value. Priviledge mode [write]: If the DWD is always enabled after reset is released: The DWD starts counting down from the reset value of the counter, that is, 0x002DFFFF. The application can configure the DWD preload register any time before this down counter expires. When the application services the DWD, the preload register contents are copied left-justified into the DWD down counter and it starts counting down from that value. If the DWD is implemented such that the down counter is enabled by software: The DWD preload register can be configured only when the DWD is disabled. Therefore, the application can only configure the DWD preload register before it enables the DWD down counter. The expiration time of the DWD Down Counter can be determined with following equation: texp = [RTIDWDPRLD+1] x 2 ^ 13 / RTICLK1 where: RTIDWDPRLD = 0...4095

4.20.30 MEM_RTIWDSTATUS Registers

4.20.30.1 MEM_RTIWDSTATUS Register (Offset = 98h) [reset = 0h]

Short Description: Watchdog Status reflects

Long Description: Watchdog Status reflects the status of Analog and Digital Watchdog

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Table 4-2933. Instance Table

Instance Name	Physical Address
WDT0	5210 0098h
WDT1	5210 1098h
WDT2	5210 2098h
WDT3	5210 3098h

Figure 4-1376. RTIWDSTATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED18															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED18										DWWD_ST	ENDTIMEVIOL	STARTTIMEVIOL	KEYST	DWDST	AWDST
R/W										R/W	R/W	R/W	R/W	R/W	R/W
0h										0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-2934. RTIWDSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED18	R/W	0h	Reserved. Reads return 0 and writes have no effect
5	DWWD_ST	R/W	0h	DWWD ST: Windowed Watchdog Status. This bit denotes whether the time-window defined by the windowed watchdog configuration has been violated, or if a wrong key or key sequence was written to service the watchdog. User and priviledge mode [read]: 0 = no time-window violation has occurred. 1 = a time-window violation has occurred. The watchdog will generate either a system reset or a non-maskable interrupt to the CPU in this case. Priviledge mode [write]: 0 = leaves the current value unchanged. 1 = clears the bit to 0. This will also clear all other status flags in the RTIWDSTATUS register except for the AWD ST flag. Clearing of the status flags will deassert the non-maskable interrupt generated due to violation of the DWWD.
4	ENDTIMEVIOL	R/W	0h	END TIME VIOL: Windowed Watchdog End Time Violation Status. This bit denotes whether the end-time defined by the windowed watchdog configuration has been violated. This bit is effectively a copy of the DWD ST status flag. User and priviledge mode [read]: 0 = no end-time window violation has occurred. 1 = the end-time defined by the windowed watchdog configuration has been violated. Priviledge mode [write]: 0 = leaves the current value unchanged. 1 = clears the bit to 0.

Table 4-2934. RTIWDSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	STARTTIMEVIOL	R/W	0h	START TIME VIOL: Windowed Watchdog Start Time Violation Status. This bit denotes whether the start-time defined by the windowed watchdog configuration has been violated. This indicates that the WWD was serviced before the service window was opened. User and priviledge mode [read]: 0 = no start-time window violation has occurred. 1 = the start-time defined by the windowed watchdog configuration has been violated. Priviledge mode [write]: 0 = leaves the current value unchanged. 1 = clears the bit to 0.
2	KEYST	R/W	0h	KEYST: Watchdog KeyStatus. This bit denotes a reset generated by a wrong key or a wrong key-sequence written to the RTIWDKEY register. User and priviledge mode [read]: 0 = no wrong key or key-sequence written 1 = wrong key or key-sequence written to RTIWDKEY register Priviledge mode [write]: 0 = leaves the current value unchanged 1 = clears the bit to 0
1	DWDST	R/W	0h	DWDST: Digital Watchdog Status. This bit is effectively a copy of the END TIME VIOL status flag and is maintained for compatibility reasons. User and priviledge mode [read]: 0 = DWD timeout period not expired 1 = DWD timeout period has expired Priviledge mode [write]: 0 = leaves the current value unchanged 1 = clears the bit to 0
0	AWDST	R/W	0h	AWDST: Analog Watchdog Status. User and priviledge mode [read]: 0 = AWD pin 0 > 1 threshold not exceeded 1 = AWD pin 0 > 1 threshold exceeded Priviledge mode [write]: 0 = leaves the current value unchanged 1 = clears the bit to 0

4.20.31 MEM_RTIWDKEY Registers

4.20.31.1 MEM_RTIWDKEY Register (Offset = 9Ch) [reset = 0h]

Short Description: Watchdog Key correct writ

Long Description: Watchdog Key correct written key values discharge the external capacitor

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Table 4-2935. Instance Table

Instance Name	Physical Address
WDT0	5210 009Ch
WDT1	5210 109Ch
WDT2	5210 209Ch
WDT3	5210 309Ch

Figure 4-1377. RTIWDKEY Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED19															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDKEY															
R/W															
0h															

Access Types Legend

Table 4-2936. RTIWDKEY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED19	R/W	0h	Reserved. Reads return 0 and writes have no effect
15:0	WDKEY	R/W	0h	WDKEY: Watchdog Key. User and privilege mode reads are indeterminate. Privilege mode [write]: A write of 0xE51A followed by 0xA35C in two separate write operations defines the Key Sequence and discharges the watchdog capacitor. This also causes the upper 12 bits of the DWD down counter to be reloaded with the contents of the DWD preload register and the lower 13 bits to become all 1s. Writing any other value causes a digital watchdog reset, as shown in Table 1-3. Note: Register write access time precaution The user has to take into account that the write to the register takes 3 VCLK cycle. This needs to be considered for the AWD/DWD expiration calculation.

4.20.32 MEM_RTIDWDCNTR Registers

4.20.32.1 MEM_RTIDWDCNTR Register (Offset = A0h) [reset = 0h]

Short Description: Digital Watchdog Down Cou

Long Description: Digital Watchdog Down Counter current value of DWD down counter

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Table 4-2937. Instance Table

Instance Name	Physical Address
WDT0	5210 00A0h
WDT1	5210 10A0h
WDT2	5210 20A0h
WDT3	5210 30A0h

Figure 4-1378. RTIDWDCNTR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED20							DWDCNTR								
R/W							R/W								
0h							0h								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DWDCNTR															
R/W															
0h															

Access Types Legend

Table 4-2938. RTIDWDCNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED20	R/W	0h	Reserved. Reads return 0 and writes have no effect
24:0	DWDCNTR	R/W	0h	DWDCNTR: Digital Watchdog Down Counter. The value of the DWDCNTR after a system reset is 0x002D_FFFF. When the DWD is enabled and the DWD counter starts counting down from this value with an RTICLK1 time base of 3MHz, a watchdog reset will be generated in 1 second. User and privilege mode [read]: Reads return the current counter value. Privilege mode [write]: Writes dont have an effect.

4.20.33 MEM_RTIWWDRXNCTRL Registers

4.20.33.1 MEM_RTIWWDRXNCTRL Register (Offset = A4h) [reset = 0h]

Short Description: Windowed Watchdog Reactio

Long Description: Windowed Watchdog Reaction Control configures the windowed watchdog to either generate a non-maskable interrupt to the CPU or to generate a system reset

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Table 4-2939. Instance Table

Instance Name	Physical Address
WDT0	5210 00A4h
WDT1	5210 10A4h
WDT2	5210 20A4h
WDT3	5210 30A4h

Figure 4-1379. RTIWWDRXNCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED21															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED21												WWDRXN			
R/W												R/W			
0h												0h			

Access Types Legend

Table 4-2940. RTIWWDRXNCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED21	R/W	0h	Reserved. Reads return 0 and writes have no effect
3:0	WWDRXN	R/W	0h	WWDRXN: Digital Windowed Watchdog Reaction. User and privilege mode [read], privileged mode [write]: 0x5 = This is the default value. The windowed watchdog will cause a reset if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all. 0xA = The windowed watchdog will generate a non-maskable interrupt to the CPU if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all. Writing any other value will cause a system reset if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all. Note: Configuration of DWWD Reaction The DWWD reaction can be selected by the application even when the DWWD counter is already enabled. If a change to the WWDRXN is made before the watchdog service window is opened, then the change in the configuration takes effect immediately. If a change to the WWDRXN is made when the watchdog service window is already open, then the change in configuration takes effect only after the watchdog is serviced.

4.20.34 MEM_RTIWWDSIZECTRL Registers

4.20.34.1 MEM_RTIWWDSIZECTRL Register (Offset = A8h) [reset = 0h]

Short Description: Windowed Watchdog Size Co

Long Description: Windowed Watchdog Size Control configures the size of the window for the digital windowed watchdog

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Table 4-2941. Instance Table

Instance Name	Physical Address
WDT0	5210 00A8h
WDT1	5210 10A8h
WDT2	5210 20A8h
WDT3	5210 30A8h

Figure 4-1380. RTIWWDSIZECTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WWDSIZE															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WWDSIZE															
R/W															
0h															

Access Types Legend

Table 4-2942. RTIWWDSIZECTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	WWDSIZE	R/W	0h	WWDSIZE: Digital Windowed Watchdog Window Size. User and privilege mode [read], privileged mode [write]: Value written to WWDSIZE Window Size 0x00000005 100% [Functionality same as the time-out digital watchdog.] 0x00000050 50% 0x00000500 25% 0x00005000 12.5% 0x00050000 6.25% 0x00500000 3.125% Any other value 3.125% Note: Incorrect value being written to watchdog window size control register If an incorerct value is written to the WWDSIZE field, or if a system disturbance causes the WWDSIZE field to have a value other than 0x5, 0x50, 0x500, 0x5000, 0x50000, or 0x500000, then the window size will be configured to be 3.125%. This increases the chances of getting a reset due to the windowed watchdog, which enables the system to handle the cause for the incorrect configuration. Note: Configuration of DWWD Window Size The DWWD window size can be selected by the application even when the DWWD counter is already enabled. If a change to the WWDSIZE is made before the watchdog service window is opened, then the change in the configuration takes effect immediately. If a change to the WWDSIZE is made when the watchdog service window is already open, then

4.20.35 MEM_RTIINTCLRENABLE Registers

4.20.35.1 MEM_RTIINTCLRENABLE Register (Offset = ACh) [reset = 0h]

Short Description: RTI Compare Interrupt Cle

Long Description: RTI Compare Interrupt Clear Enable enable the auto clear functionality for each of the compare interrupts

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Table 4-2943. Instance Table

Instance Name	Physical Address
WDT0	5210 00ACh
WDT1	5210 10ACh
WDT2	5210 20ACh
WDT3	5210 30ACh

Figure 4-1381. RTIINTCLRENABLE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED25				INTCLRENABLE3				RESERVED24				INTCLRENABLE2			
R/W				R/W				R/W				R/W			
0h				0h				0h				0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED23				INTCLRENABLE1				RESERVED22				INTCLRENABLE0			
R/W				R/W				R/W				R/W			
0h				0h				0h				0h			

Access Types Legend

Table 4-2944. RTIINTCLRENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED25	R/W	0h	Reserved. Reads return 0 and writes have no effect
27:24	INTCLRENABLE3	R/W	0h	INTCLRENABLE3. Enables the auto-clear functionality on the compare 3 interrupt. User and Privileged mode [read]: 0x5 = Auto-clear for compare 3 interrupt is disabled. Any other value = Auto-clear for compare 3 interrupt is enabled. Privileged mode [write]: 0x5 = Disables the auto-clear functionality on the compare 3 interrupt. Any other value = Enables the auto-clear functionality on the compare 3 interrupt.
23:20	RESERVED24	R/W	0h	Reserved. Reads return 0 and writes have no effect
19:16	INTCLRENABLE2	R/W	0h	INTCLRENABLE2. Enables the auto-clear functionality on the compare 2 interrupt. User and Privileged mode [read]: 0x5 = Auto-clear for compare 2 interrupt is disabled. Any other value = Auto-clear for compare 2 interrupt is enabled. Privileged mode [write]: 0x5 = Disables the auto-clear functionality on the compare 2 interrupt. Any other value = Enables the auto-clear functionality on the compare 2 interrupt.
15:12	RESERVED23	R/W	0h	Reserved. Reads return 0 and writes have no effect
11:8	INTCLRENABLE1	R/W	0h	INTCLRENABLE1. Enables the auto-clear functionality on the compare 1 interrupt. User and Privileged mode [read]: 0x5 = Auto-clear for compare 1 interrupt is disabled. Any other value = Auto-clear for compare 1 interrupt is enabled. Privileged mode [write]: 0x5 = Disables the auto-clear functionality on the compare 1 interrupt. Any other value = Enables the auto-clear functionality on the compare 1 interrupt.
7:4	RESERVED22	R/W	0h	Reserved. Reads return 0 and writes have no effect

Table 4-2944. RTIINTCLRENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	INTCLRENABLE0	R/W	0h	INTCLRENABLE0. Enables the auto-clear functionality on the compare 0 interrupt. User and Privileged mode [read]: 0x5 = Auto-clear for compare 0 interrupt is disabled. Any other value = Auto-clear for compare 0 interrupt is enabled. Privileged mode [write]: 0x5 = Disables the auto-clear functionality on the compare 0 interrupt. Any other value = Enables the auto-clear functionality on the compare 0 interrupt.

4.20.36 MEM_RTICOMP0CLR Registers

4.20.36.1 MEM_RTICOMP0CLR Register (Offset = B0h) [reset = 0h]

Short Description: Compare 0 Clear compare v

Long Description: Compare 0 Clear compare value to be compared with the counter to clear the compare0 interrupt line

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Table 4-2945. Instance Table

Instance Name	Physical Address
WDT0	5210 00B0h
WDT1	5210 10B0h
WDT2	5210 20B0h
WDT3	5210 30B0h

Figure 4-1382. RTICOMP0CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP0CLR															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP0CLR															
R/W															
0h															

Access Types Legend

Table 4-2946. RTICOMP0CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP0CLR	R/W	0h	COMP0CLR: Compare 0 Clear. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the compare 0 interrupt or DMA request line is cleared. User and privilege mode [read]: current compare value Privilege mode [write]: update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

4.20.37 MEM_RTICOMP1CLR Registers

4.20.37.1 MEM_RTICOMP1CLR Register (Offset = B4h) [reset = 0h]

Short Description: Compare 1 Clear compare v

Long Description: Compare 1 Clear compare value to be compared with the counter to clear the compare1 interrupt line

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Table 4-2947. Instance Table

Instance Name	Physical Address
WDT0	5210 00B4h
WDT1	5210 10B4h
WDT2	5210 20B4h
WDT3	5210 30B4h

Figure 4-1383. RTICOMP1CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP1CLR															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP1CLR															
R/W															
0h															

Access Types Legend

Table 4-2948. RTICOMP1CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP1CLR	R/W	0h	COMP1CLR: Compare 1 Clear. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the Compare 1 interrupt or DMA request line is cleared. User and privilege mode [read]: current compare value Privilege mode [write]: update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

4.20.38 MEM_RTICOMP2CLR Registers

4.20.38.1 MEM_RTICOMP2CLR Register (Offset = B8h) [reset = 0h]

Short Description: Compare 2 Clear compare v

Long Description: Compare 2 Clear compare value to be compared with the counter to clear the compare2 interrupt line

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Table 4-2949. Instance Table

Instance Name	Physical Address
WDT0	5210 00B8h
WDT1	5210 10B8h
WDT2	5210 20B8h
WDT3	5210 30B8h

Figure 4-1384. RTICOMP2CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP2CLR															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP2CLR															
R/W															
0h															

Access Types Legend

Table 4-2950. RTICOMP2CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP2CLR	R/W	0h	COMP2CLR: Compare 2 Clear. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the Compare 2 interrupt or DMA request line is cleared. User and privilege mode [read]: current compare value Privilege mode [write]: update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

4.20.39 MEM_RTICOMP3CLR Registers

4.20.39.1 MEM_RTICOMP3CLR Register (Offset = BCh) [reset = 0h]

Short Description: Compare 3 Clear compare v

Long Description: Compare 3 Clear compare value to be compared with the counter to clear the compare3 interrupt line

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Table 4-2951. Instance Table

Instance Name	Physical Address
WDT0	5210 00BCh
WDT1	5210 10BCh
WDT2	5210 20BCh
WDT3	5210 30BCh

Figure 4-1385. RTICOMP3CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP3CLR															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP3CLR															
R/W															
0h															

Access Types Legend

Table 4-2952. RTICOMP3CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP3CLR	R/W	0h	COMP3CLR: Compare 3 Clear. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the Compare 3 interrupt or DMA request line is cleared. User and privilege mode [read]: current compare value Privilege mode [write]: update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

4.20.40 Access Table

Table 4-2953. Access Type Codes

Access Type	Code	Description
R/W	R/W	Read / Write

4.21 SPINLOCK Registers

Table 4-2954. , Registers, Base Address=0X0000000050E00000, Length=32768

Offset	Length	Register Name	SPINLOCK0 Physical Address
0h	32	SPINLOCK_REVISION	50E0 0000h
10h	32	SPINLOCK_SYSCONFIG	50E0 0010h
14h	32	SPINLOCK_SYSTATUS	50E0 0014h
800h + Formula	32	SPINLOCK_LOCK_REG_N	50E0 0800h + Formula

4.21.1 SPINLOCK_REVISION Registers

4.21.1.1 REVISION Register (Offset = 0h) [reset = 66fa6900h]

Short Description: Peripheral ID register

Long Description: This is the standard TI peripheral ID register that exists at address 0 in the peripheral space

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Table 4-2955. Instance Table

Instance Name	Physical Address
SPINLOCK0	50E0 0000h

Figure 4-1386. SPINLOCK_REVISION Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		FUNCTION											
R		R		R											
1h		2h		6fah											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL_VER				MAJOR_REV				CUSTOM		MINOR_REV					
R				R				R		R					
dh				1h				0h		0h					

Access Types Legend

Table 4-2956. SPINLOCK_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish which ID numbering scheme is used. Reset Source: core_srst_n
29:28	BU	R	2h	BU identifier Reset Source: core_srst_n
27:16	FUNCTION	R	6FAh	Module family. Reset Source: core_srst_n
15:11	RTL_VER	R	Dh	RTL version. R of X.Y.R.Z Reset Source: core_srst_n
10:8	MAJOR_REV	R	1h	Major revision. X of X.Y.R.Z Reset Source: core_srst_n
7:6	CUSTOM	R	0h	Special version number Reset Source: core_srst_n
5:0	MINOR_REV	R	0h	Minor revision. Y of X.Y.R.Z Reset Source: core_srst_n

4.21.2 SPINLOCK_SYSCONFIG Registers

4.21.2.1 SYSCONFIG Register (Offset = 10h) [reset = 0h]

Short Description: SpinLock top level configuration

Long Description: Provides the SOFTRESET register for backwards compatibility with OMAP Spinlock

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Table 4-2957. Instance Table

Instance Name	Physical Address
SPINLOCK0	50E0 0010h

Figure 4-1387. SPINLOCK_SYSCONFIG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														SOFT_RESET	RESERVED
NONE														R/W	NONE
0														0h	0

Access Types Legend

Table 4-2958. SPINLOCK_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1	SOFT_RESET	R/W	0h	Module Software Reset The bit is automatically reset by the hardware. During reads, it always returns 0 It has the same effect as the hardware reset Writing a 0 has no effect. Writing a 1 will start a soft reset sequence and free all of the locks Reset Source: core_srst_n
0	RESERVED	NONE		Reserved

4.21.3 SPINLOCK_SYSTATUS Registers

4.21.3.1 SYSTATUS Register (Offset = 14h) [reset = 8000000h]

Short Description: SpinLock top level status

Long Description: Provides information about the Spinlock module

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Table 4-2959. Instance Table

Instance Name	Physical Address
SPINLOCK0	50E0 0014h

Figure 4-1388. SPINLOCK_SYSTATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NUM_LOCKS								RESERVED							
R								NONE							
8h								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								IN_USE7	IN_USE6	IN_USE5	IN_USE4	IN_USE3	IN_USE2	IN_USE1	IN_USE0
NONE								R	R	R	R	R	R	R	R
0								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-2960. SPINLOCK_SYSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	NUM_LOCKS	R	8h	Module configuration parameter n, the total number of spinlocks divided by 32. e.g. For 256 spin locks, this will return the number 0x08 Reset Source: core_srst_n
23:8	RESERVED	NONE		Reserved
7	IN_USE7	R	0h	In-Use flag 7 covering lock registers 224 - 255. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 224 - 255 are in the Not Taken state Read 1 : At least one of the lock registers 224 - 255 are in the Taken state Reset Source: core_srst_n
6	IN_USE6	R	0h	In-Use flag 6 covering lock registers 192 - 223. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 192 - 223 are in the Not Taken state Read 1 : At least one of the lock registers 192 - 223 are in the Taken state Reset Source: core_srst_n
5	IN_USE5	R	0h	In-Use flag 5 covering lock registers 160 - 191. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 160 - 191 are in the Not Taken state Read 1 : At least one of the lock registers 160 - 191 are in the Taken state Reset Source: core_srst_n
4	IN_USE4	R	0h	In-Use flag 4 covering lock registers 128 - 159. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 128 - 159 are in the Not Taken state Read 1 : At least one of the lock registers 128 - 159 are in the Taken state Reset Source: core_srst_n
3	IN_USE3	R	0h	In-Use flag 3 covering lock registers 96 - 127. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 96 - 127 are in the Not Taken state Read 1 : At least one of the lock registers 96 - 127 are in the Taken state Reset Source: core_srst_n

Table 4-2960. SPINLOCK_SYSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	IN_USE2	R	0h	In-Use flag 2 covering lock registers 64 - 95. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 64 - 95 are in the Not Taken state Read 1 : At least one of the lock registers 64 - 95 are in the Taken state Reset Source: core_srst_n
1	IN_USE1	R	0h	In-Use flag 1 covering lock registers 32 - 63. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 32 - 63 are in the Not Taken state Read 1 : At least one of the lock registers 32 - 63 are in the Taken state Reset Source: core_srst_n
0	IN_USE0	R	0h	In-Use flag 0 covering lock registers 0 - 31. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 0 - 31 are in the Not Taken state Read 1 : At least one of the lock registers 0 - 31 are in the Taken state Reset Source: core_srst_n

4.21.4 SPINLOCK_LOCK_REG_N Registers

4.21.4.1 LOCK_REG_N Register (Offset = 800h) [reset = 0h]

Short Description: Lock[a] register

Long Description: The Lock[a] register is read and written to perform lock and unlock operations on lock 'a'

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Offset = 800h + (j * 4h); where j = 0h to FFh

Table 4-2961. Instance Table

Instance Name	Physical Address
SPINLOCK0	50E0 0800h

Figure 4-1389. SPINLOCK_LOCK_REG_N Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															TAKEN
NONE															R/W
0															0h

Access Types Legend

Table 4-2962. SPINLOCK_LOCK_REG_N Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE		Reserved
0	TAKEN	R/W	0h	Lock Status Read 0 : Lock was previously free. The reader now has been granted the lock. Read 1 : Lock was previously taken. The reader has not been granted the lock and must retry. Write 0 : Free the lock by setting TAKEN to zero. Write 1 : No effect Reset Source: core_srst_n

4.21.5 Access Table

Table 4-2963. Access Type Codes

Access Type	Code	Description
R	R	Read
R/W	R/W	Read / Write

4.22 MBOX_RAM Registers

Table 4-2964. MEM, MEM Registers, Base Address=0X0000000072000000, Length=16384

Offset	Length	Register Name	MBOX_RAM0 Physical Address
0h	32	START	7200 0000h
3FFCh	32	END	7200 3FFCh

4.22.1 MEM_START Registers

4.22.1.1 MEM_START Register (Offset = 0h) [reset = 0h]

Short Description:

Long Description:

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Table 4-2965. Instance Table

Instance Name	Physical Address
MBOX_RAM0	7200 0000h

Figure 4-1390. START Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START															
R/W															
0h															

Access Types Legend

Table 4-2966. START Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START	R/W	0h	L2 Memory start address Reset Source: Soc_mailbox_RAM_rst_mod_g_rst_n

4.22.2 MEM_END Registers

4.22.2.1 MEM_END Register (Offset = 3FFCh) [reset = 0h]

Short Description:

Long Description:

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Table 4-2967. Instance Table

Instance Name	Physical Address
MBOX_RAM0	7200 3FFCh

Figure 4-1391. END Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END															
R/W															
0h															

Access Types Legend

Table 4-2968. END Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END	R/W	0h	L2 Memory end address Reset Source: Soc_mailbox_RAM_rst_mod_g_rst_n

4.22.3 Access Table

Table 4-2969. Access Type Codes

Access Type	Code	Description
R/W	R/W	Read / Write

4.23 UART Registers

Table 4-2970. , Registers, Base Address=0X0000000052300000, Length=512

Offset	Length	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
0h	32	UART_DLL	5230 0000h	5230 1000h	5230 2000h
0h	32	UART_RHR	5230 0000h	5230 1000h	5230 2000h
0h	32	UART_THR	5230 0000h	5230 1000h	5230 2000h
4h	32	UART_DLH	5230 0004h	5230 1004h	5230 2004h
4h	32	UART_IER_CIR	5230 0004h	5230 1004h	5230 2004h
4h	32	UART_IER_IRDA	5230 0004h	5230 1004h	5230 2004h
4h	32	UART_IER_UART	5230 0004h	5230 1004h	5230 2004h
8h	32	UART_EFR	5230 0008h	5230 1008h	5230 2008h
8h	32	UART_FCR	5230 0008h	5230 1008h	5230 2008h
8h	32	UART_IIR_CIR	5230 0008h	5230 1008h	5230 2008h
8h	32	UART_IIR_IRDA	5230 0008h	5230 1008h	5230 2008h
8h	32	UART_IIR_UART	5230 0008h	5230 1008h	5230 2008h
Ch	32	UART_LCR	5230 000Ch	5230 100Ch	5230 200Ch
10h	32	UART_MCR	5230 0010h	5230 1010h	5230 2010h
10h	32	UART_XON1_ADDR1	5230 0010h	5230 1010h	5230 2010h
14h	32	UART_LSR_CIR	5230 0014h	5230 1014h	5230 2014h
14h	32	UART_LSR_IRDA	5230 0014h	5230 1014h	5230 2014h
14h	32	UART_LSR_UART	5230 0014h	5230 1014h	5230 2014h
14h	32	UART_XON2_ADDR2	5230 0014h	5230 1014h	5230 2014h
18h	32	UART_MSR	5230 0018h	5230 1018h	5230 2018h
18h	32	UART_TCR	5230 0018h	5230 1018h	5230 2018h
18h	32	UART_XOFF1	5230 0018h	5230 1018h	5230 2018h
1Ch	32	UART_SPR	5230 001Ch	5230 101Ch	5230 201Ch
1Ch	32	UART_TLR	5230 001Ch	5230 101Ch	5230 201Ch
1Ch	32	UART_XOFF2	5230 001Ch	5230 101Ch	5230 201Ch
20h	32	UART_MDR1	5230 0020h	5230 1020h	5230 2020h
24h	32	UART_MDR2	5230 0024h	5230 1024h	5230 2024h
28h	32	UART_SFLSR	5230 0028h	5230 1028h	5230 2028h
28h	32	UART_TXFLL	5230 0028h	5230 1028h	5230 2028h
2Ch	32	UART_RESUME	5230 002Ch	5230 102Ch	5230 202Ch
2Ch	32	UART_TXFLH	5230 002Ch	5230 102Ch	5230 202Ch
30h	32	UART_RXFLL	5230 0030h	5230 1030h	5230 2030h
30h	32	UART_SFREGL	5230 0030h	5230 1030h	5230 2030h
34h	32	UART_RXFLH	5230 0034h	5230 1034h	5230 2034h
34h	32	UART_SFREGH	5230 0034h	5230 1034h	5230 2034h
38h	32	UART_BLR	5230 0038h	5230 1038h	5230 2038h
38h	32	UART_UASR	5230 0038h	5230 1038h	5230 2038h
3Ch	32	UART_ACREG	5230 003Ch	5230 103Ch	5230 203Ch
40h	32	UART_SCR	5230 0040h	5230 1040h	5230 2040h
44h	32	UART_SSR	5230 0044h	5230 1044h	5230 2044h
48h	32	UART_EBLR	5230 0048h	5230 1048h	5230 2048h
50h	32	UART_MVR	5230 0050h	5230 1050h	5230 2050h
54h	32	UART_SYSC	5230 0054h	5230 1054h	5230 2054h
58h	32	UART_SYSS	5230 0058h	5230 1058h	5230 2058h

Table 4-2970. , Registers, Base Address=0X0000000052300000, Length=512 (continued)

Offset	Length	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
5Ch	32	UART_WER	5230 005Ch	5230 105Ch	5230 205Ch
60h	32	UART_CFPS	5230 0060h	5230 1060h	5230 2060h
64h	32	UART_RXFIFO_LVL	5230 0064h	5230 1064h	5230 2064h
68h	32	UART_TXFIFO_LVL	5230 0068h	5230 1068h	5230 2068h
6Ch	32	UART_IER2	5230 006Ch	5230 106Ch	5230 206Ch
70h	32	UART_ISR2	5230 0070h	5230 1070h	5230 2070h
74h	32	UART_FREQ_SEL	5230 0074h	5230 1074h	5230 2074h
78h	32	UART_ABAUD_1ST_CHAR	5230 0078h	5230 1078h	5230 2078h
7Ch	32	UART_BAUD_2ND_CHAR	5230 007Ch	5230 107Ch	5230 207Ch
80h	32	UART_MDR3	5230 0080h	5230 1080h	5230 2080h
84h	32	UART_TX_DMA_THRESHOLD	5230 0084h	5230 1084h	5230 2084h
88h	32	UART_MDR4	5230 0088h	5230 1088h	5230 2088h
8Ch	32	UART_EFR2	5230 008Ch	5230 108Ch	5230 208Ch
90h	32	UART_ECR	5230 0090h	5230 1090h	5230 2090h
94h	32	UART_TIMEGUARD	5230 0094h	5230 1094h	5230 2094h
98h	32	UART_TIMEOUTL	5230 0098h	5230 1098h	5230 2098h
9Ch	32	UART_TIMEOUTH	5230 009Ch	5230 109Ch	5230 209Ch
A0h	32	UART_SCCR	5230 00A0h	5230 10A0h	5230 20A0h
A4h	32	UART_ERHR	5230 00A4h	5230 10A4h	5230 20A4h
A4h	32	UART_ETHR	5230 00A4h	5230 10A4h	5230 20A4h
A8h	32	UART_MAR	5230 00A8h	5230 10A8h	5230 20A8h
ACh	32	UART_MMR	5230 00ACh	5230 10ACh	5230 20ACh
B0h	32	UART_MBR	5230 00B0h	5230 10B0h	5230 20B0h

Table 4-2971. , Registers, Base Address=0X0000000052300000, Length=512

Offset	Length	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
0h	32	UART_DLL	5230 3000h	5230 4000h	5230 5000h
0h	32	UART_RHR	5230 3000h	5230 4000h	5230 5000h
0h	32	UART_THR	5230 3000h	5230 4000h	5230 5000h
4h	32	UART_DLH	5230 3004h	5230 4004h	5230 5004h
4h	32	UART_IER_CIR	5230 3004h	5230 4004h	5230 5004h
4h	32	UART_IER_IRDA	5230 3004h	5230 4004h	5230 5004h
4h	32	UART_IER_UART	5230 3004h	5230 4004h	5230 5004h
8h	32	UART_EFR	5230 3008h	5230 4008h	5230 5008h
8h	32	UART_FCR	5230 3008h	5230 4008h	5230 5008h
8h	32	UART_IIR_CIR	5230 3008h	5230 4008h	5230 5008h
8h	32	UART_IIR_IRDA	5230 3008h	5230 4008h	5230 5008h
8h	32	UART_IIR_UART	5230 3008h	5230 4008h	5230 5008h
Ch	32	UART_LCR	5230 300Ch	5230 400Ch	5230 500Ch
10h	32	UART_MCR	5230 3010h	5230 4010h	5230 5010h
10h	32	UART_XON1_ADDR1	5230 3010h	5230 4010h	5230 5010h
14h	32	UART_LSR_CIR	5230 3014h	5230 4014h	5230 5014h
14h	32	UART_LSR_IRDA	5230 3014h	5230 4014h	5230 5014h
14h	32	UART_LSR_UART	5230 3014h	5230 4014h	5230 5014h
14h	32	UART_XON2_ADDR2	5230 3014h	5230 4014h	5230 5014h

Table 4-2971. , Registers, Base Address=0X0000000052300000, Length=512 (continued)

Offset	Length	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
18h	32	UART_MSR	5230 3018h	5230 4018h	5230 5018h
18h	32	UART_TCR	5230 3018h	5230 4018h	5230 5018h
18h	32	UART_XOFF1	5230 3018h	5230 4018h	5230 5018h
1Ch	32	UART_SPR	5230 301Ch	5230 401Ch	5230 501Ch
1Ch	32	UART_TLR	5230 301Ch	5230 401Ch	5230 501Ch
1Ch	32	UART_XOFF2	5230 301Ch	5230 401Ch	5230 501Ch
20h	32	UART_MDR1	5230 3020h	5230 4020h	5230 5020h
24h	32	UART_MDR2	5230 3024h	5230 4024h	5230 5024h
28h	32	UART_SFLSR	5230 3028h	5230 4028h	5230 5028h
28h	32	UART_TXFLL	5230 3028h	5230 4028h	5230 5028h
2Ch	32	UART_RESUME	5230 302Ch	5230 402Ch	5230 502Ch
2Ch	32	UART_TXFLH	5230 302Ch	5230 402Ch	5230 502Ch
30h	32	UART_RXFLL	5230 3030h	5230 4030h	5230 5030h
30h	32	UART_SFREGL	5230 3030h	5230 4030h	5230 5030h
34h	32	UART_RXFLH	5230 3034h	5230 4034h	5230 5034h
34h	32	UART_SFREGH	5230 3034h	5230 4034h	5230 5034h
38h	32	UART_BLR	5230 3038h	5230 4038h	5230 5038h
38h	32	UART_UASR	5230 3038h	5230 4038h	5230 5038h
3Ch	32	UART_ACREG	5230 303Ch	5230 403Ch	5230 503Ch
40h	32	UART_SCR	5230 3040h	5230 4040h	5230 5040h
44h	32	UART_SSR	5230 3044h	5230 4044h	5230 5044h
48h	32	UART_EBLR	5230 3048h	5230 4048h	5230 5048h
50h	32	UART_MVR	5230 3050h	5230 4050h	5230 5050h
54h	32	UART_SYSC	5230 3054h	5230 4054h	5230 5054h
58h	32	UART_SYSS	5230 3058h	5230 4058h	5230 5058h
5Ch	32	UART_WER	5230 305Ch	5230 405Ch	5230 505Ch
60h	32	UART_CFPS	5230 3060h	5230 4060h	5230 5060h
64h	32	UART_RXFIFO_LVL	5230 3064h	5230 4064h	5230 5064h
68h	32	UART_TXFIFO_LVL	5230 3068h	5230 4068h	5230 5068h
6Ch	32	UART_IER2	5230 306Ch	5230 406Ch	5230 506Ch
70h	32	UART_ISR2	5230 3070h	5230 4070h	5230 5070h
74h	32	UART_FREQ_SEL	5230 3074h	5230 4074h	5230 5074h
78h	32	UART_ABAUD_1ST_CHAR	5230 3078h	5230 4078h	5230 5078h
7Ch	32	UART_BAUD_2ND_CHAR	5230 307Ch	5230 407Ch	5230 507Ch
80h	32	UART_MDR3	5230 3080h	5230 4080h	5230 5080h
84h	32	UART_TX_DMA_THRESHOLD	5230 3084h	5230 4084h	5230 5084h
88h	32	UART_MDR4	5230 3088h	5230 4088h	5230 5088h
8Ch	32	UART_EFR2	5230 308Ch	5230 408Ch	5230 508Ch
90h	32	UART_ECR	5230 3090h	5230 4090h	5230 5090h
94h	32	UART_TIMEGUARD	5230 3094h	5230 4094h	5230 5094h
98h	32	UART_TIMEOUTL	5230 3098h	5230 4098h	5230 5098h
9Ch	32	UART_TIMEOUTH	5230 309Ch	5230 409Ch	5230 509Ch
A0h	32	UART_SCCR	5230 30A0h	5230 40A0h	5230 50A0h
A4h	32	UART_ERHR	5230 30A4h	5230 40A4h	5230 50A4h
A4h	32	UART_ETHR	5230 30A4h	5230 40A4h	5230 50A4h
A8h	32	UART_MAR	5230 30A8h	5230 40A8h	5230 50A8h

Table 4-2971. , Registers, Base Address=0X0000000052300000, Length=512 (continued)

Offset	Length	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
ACh	32	UART_MMR	5230 30ACh	5230 40ACh	5230 50ACh
B0h	32	UART_MBR	5230 30B0h	5230 40B0h	5230 50B0h

4.23.1 UART_DLL Registers

4.23.1.1 DLL Register (Offset = 0h) [reset = 0h]

Short Description: Divisor Latches Low Regis

Long Description: Divisor Latches Low Register

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Table 4-2972. Instance Table

Instance Name	Physical Address
UART0	5230 0000h
UART1	5230 1000h
UART2	5230 2000h
UART3	5230 3000h
UART4	5230 4000h
UART5	5230 5000h

Figure 4-1392. UART_DLL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CLOCK_LSB							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-2973. UART_DLL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	CLOCK_LSB	R/W	0h	Used to store the 8-bit LSB divisor value Reset Source: mod_g_arstn

4.23.2 UART_RHR Registers

4.23.2.1 RHR Register (Offset = 0h) [reset = 0h]

Short Description: The receiver section cons

Long Description: The receiver section consists of the receiver holding register (RHR) and the receiver shift register. The RHR is actually a 64-byte FIFO. The receiver shift register receives serial data from RX input. The data is converted to parallel data and moved to the RHR. If the FIFO is disabled location zero of the FIFO is used to store the single data character. Note: If an overflow occurs the data in the RHR is not overwritten.

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Table 4-2974. Instance Table

Instance Name	Physical Address
UART0	5230 0000h
UART1	5230 1000h
UART2	5230 2000h
UART3	5230 3000h
UART4	5230 4000h
UART5	5230 5000h

Figure 4-1393. UART_RHR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RHR							
R								R							
0h								0h							

Access Types Legend

Table 4-2975. UART_RHR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reset Source: mod_g_arstn
7:0	RHR	R	0h	Receive holding register Reset Source: mod_g_arstn

4.23.3 UART_THR Registers

4.23.3.1 THR Register (Offset = 0h) [reset = 0h]

Short Description: The transmitter section c

Long Description: The transmitter section consists of the transmit holding register (THR) and the transmit shift register. The transmit holding register is actually a 64-byte FIFO. The LH writes data to the THR. The data is placed into the transmit shift register where it is shifted out serially on the TX output. If the FIFO is disabled location zero of the FIFO is used to store the data.

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Table 4-2976. Instance Table

Instance Name	Physical Address
UART0	5230 0000h
UART1	5230 1000h
UART2	5230 2000h
UART3	5230 3000h
UART4	5230 4000h
UART5	5230 5000h

Figure 4-1394. UART_THR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								THR							
R								W							
0h								0h							

Access Types Legend

Table 4-2977. UART_THR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reset Source: mod_g_arstn
7:0	THR	W	0h	TRANSMIT HOLDING REGISTER Reset Source: mod_g_arstn

4.23.4 UART_DLH Registers

4.23.4.1 DLH Register (Offset = 4h) [reset = 0h]

Short Description: Divisor Latches High Regi

Long Description: Divisor Latches High Register

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Table 4-2978. Instance Table

Instance Name	Physical Address
UART0	5230 0004h
UART1	5230 1004h
UART2	5230 2004h
UART3	5230 3004h
UART4	5230 4004h
UART5	5230 5004h

Figure 4-1395. UART_DLH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CLOCK_MSB							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-2979. UART_DLH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	CLOCK_MSB	R/W	0h	Used to store the 8-bit MSB divisor value Reset Source: mod_g_arstn

4.23.5 UART_IER_CIR Registers

4.23.5.1 IER_CIR Register (Offset = 4h) [reset = 0h]

Short Description: The interrupt enable regi

Long Description: The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 6 types of interrupt in these modes, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/disabled individually.

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Table 4-2980. Instance Table

Instance Name	Physical Address
UART0	5230 0004h
UART1	5230 1004h
UART2	5230 2004h
UART3	5230 3004h
UART4	5230 4004h
UART5	5230 5004h

Figure 4-1396. UART_IER_CIR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								NOT_USED2		TX_STATUS_IT	NOT_USED1	RX_OVERRUN_IT	RX_STOP_IT	THR_IT	RHR_IT
NONE								R/W		R/W	R/W	R/W	R/W	R/W	R/W
0								0h		0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-2981. UART_IER_CIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:6	NOT_USED2	R/W	0h	Reset Source: mod_g_arstn
5	TX_STATUS_IT	R/W	0h	Reset Source: mod_g_arstn 1 TX_STATUS_IT_Value_1 Enables the TX status interrupt.
4	NOT_USED1	R/W	0h	Reset Source: mod_g_arstn
3	RX_OVERRUN_IT	R/W	0h	Reset Source: mod_g_arstn 1 RX_OVERRUN_IT_Value_ Enables the RX overrun 1 interrupt.
2	RX_STOP_IT	R/W	0h	Reset Source: mod_g_arstn 1 RX_STOP_IT_Value_1 Enables the receive stop interrupt.
1	THR_IT	R/W	0h	Reset Source: mod_g_arstn 1 THR_IT_Value_1 Enables the THR interrupt.
0	RHR_IT	R/W	0h	Reset Source: mod_g_arstn 1 RHR_IT_Value_1 Enables the RHR interrupt.

4.23.6 UART_IER_IRDA Registers

4.23.6.1 IER_IRDA Register (Offset = 4h) [reset = 0h]

Short Description: The interrupt enable regi

Long Description: The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 8 types of interrupt in these modes, received EOF, LSR interrupt, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/disabled individually.

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Table 4-2982. Instance Table

Instance Name	Physical Address
UART0	5230 0004h
UART1	5230 1004h
UART2	5230 2004h
UART3	5230 3004h
UART4	5230 4004h
UART5	5230 5004h

Figure 4-1397. UART_IER_IRDA Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								EOF_IT	LINE_STS_IT	TX_STATUS_IT	STS_FIFO_TRIG_IT	RX_OVERRUN_IT	LAST_RX_BYTE_IT	THR_IT	RHR_IT
NONE								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-2983. UART_IER_IRDA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7	EOF_IT	R/W	0h	Reset Source: mod_g_arstn 1 EOF_IT_Value_1 Enables the received EOF interrupt.
6	LINE_STS_IT	R/W	0h	Reset Source: mod_g_arstn 1 LINE_STS_IT_Value_1 Enables the receiver line status interrupt.
5	TX_STATUS_IT	R/W	0h	Reset Source: mod_g_arstn 1 TX_STATUS_IT_Value_1 Enables the TX status interrupt.
4	STS_FIFO_TRIG_IT	R/W	0h	Reset Source: mod_g_arstn 1 STS_FIFO_TRIG_IT_Val Enables the status FIFO ue_1 trigger level interrupt.
3	RX_OVERRUN_IT	R/W	0h	Reset Source: mod_g_arstn 1 RX_OVERRUN_IT_Value_ Enables the RX overrun 1 interrupt.
2	LAST_RX_BYTE_IT	R/W	0h	Reset Source: mod_g_arstn 1 LAST_RX_BYTE_IT_Valu Enables the last byte of frame e_1 in RX FIFO interrupt.
1	THR_IT	R/W	0h	Reset Source: mod_g_arstn 1 THR_IT_Value_1 Enables the THR interrupt.
0	RHR_IT	R/W	0h	Reset Source: mod_g_arstn 1 RHR_IT_Value_1 Enables the RHR interrupt.

4.23.7 UART_IER_UART Registers

4.23.7.1 IER_UART Register (Offset = 4h) [reset = 0h]

Short Description: The interrupt enable regi

Long Description: The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are seven types of interrupt in this mode: receiver error, RHR interrupt, THR interrupt, XOFF received and CTS*/RTS* change of state from low to high. Each interrupt can be enabled/disabled individually. There is also a sleep mode enable bit.

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Table 4-2984. Instance Table

Instance Name	Physical Address
UART0	5230 0004h
UART1	5230 1004h
UART2	5230 2004h
UART3	5230 3004h
UART4	5230 4004h
UART5	5230 5004h

Figure 4-1398. UART_IER_UART Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CTS_IT	RTS_IT	XOFF_IT	SLEEP_MODE	MODEM_STS_IT	LINE_STS_IT	THR_IT	RHR_IT
R								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-2985. UART_IER_UART Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R		Reset Source: mod_g_arstn
7	CTS_IT	R/W	0h	Reset Source: mod_g_arstn 1 CTS_IT_Value_1 Enables the CTS* interrupt
6	RTS_IT	R/W	0h	Reset Source: mod_g_arstn 1 RTS_IT_Value_1 Enables the RTS* interrupt
5	XOFF_IT	R/W	0h	Reset Source: mod_g_arstn 1 XOFF_IT_Value_1 Enables the XOFF interrupt
4	SLEEP_MODE	R/W	0h	Reset Source: mod_g_arstn 1 SLEEP_MODE_Value_1 Enables sleep mode (stop baud rate clock when the module is inactive)
3	MODEM_STS_IT	R/W	0h	Reset Source: mod_g_arstn 1 MODEM_STS_IT_Value_1 Enables the modem status register interrupt
2	LINE_STS_IT	R/W	0h	Reset Source: mod_g_arstn 1 LINE_STS_IT_u_Value_ Enables the receiver line 1 status interrupt
1	THR_IT	R/W	0h	Reset Source: mod_g_arstn 1 THR_IT_Value_1 Enables the THR interrupt
0	RHR_IT	R/W	0h	Reset Source: mod_g_arstn 1 RHR_IT_Value_1 Enables the RHR interrupt and time out interrupt.

4.23.8 UART_EFR Registers

4.23.8.1 EFR Register (Offset = 8h) [reset = 0h]

Short Description: Enhanced Feature Register

Long Description: Enhanced Feature Register

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Table 4-2986. Instance Table

Instance Name	Physical Address
UART0	5230 0008h
UART1	5230 1008h
UART2	5230 2008h
UART3	5230 3008h
UART4	5230 4008h
UART5	5230 5008h

Figure 4-1399. UART_EFR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								AUTO_CTS_EN	AUTO_RTS_EN	SPECIAL_CHAR_DETECT	ENHANCED_EN	SW_FLOW_CONTROL			
NONE								R/W	R/W	R/W	R/W	R/W			
0								0h	0h	0h	0h	0h			

Access Types Legend

Table 4-2987. UART_EFR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7	AUTO_CTS_EN	R/W	0h	Auto-CTS enable bit. 0: Normal operation. 1: Auto-CTS flow control is enabled i.e. transmission is halted when the CTS* pin is high (inactive). Reset Source: mod_g_arstn
6	AUTO_RTS_EN	R/W	0h	Auto-RTS enable bit. 0: Normal operation. 1: Auto- RTS flow control is enabled i.e. RTS* pin goes high (inactive) when the receiver FIFO HALT trigger level, TCR[3:0], is reached, and goes low (active) when the receiver FIFO RESTORE transmission trigger level is reached. Reset Source: mod_g_arstn
5	SPECIAL_CHAR_DETECT	R/W	0h	0: Normal operation. 1: Special character detect enable. Received data is compared with XOFF2 data. If a match occurs the received data is transferred to RX FIFO and IIR bit 4 is set to 1 to indicate a special character has been detected. Reset Source: mod_g_arstn
4	ENHANCED_EN	R/W	0h	Enhanced functions write enable bit. 0: Disables writing to IER bits 4-7, FCR bits 4-5, and MCR bits 5-7. 1: Enables writing to IER bits 4-7, FCR bits 4-5, and MCR bits 5-7. Reset Source: mod_g_arstn
3:0	SW_FLOW_CONTROL	R/W	0h	Combinations of Software flow control can be selected by programming bit 3 - bit 0. See Software Flow Control Options Reset Source: mod_g_arstn

4.23.9 UART_FCR Registers

4.23.9.1 FCR Register (Offset = 8h) [reset = 0h]

Short Description: Notes: Bits 4 and 5 can

Long Description: Notes: Bits 4 and 5 can only be written to when EFR[4] = 1 Bits 0 to 3 can be changed only when the baud clock is not running (DLL and DLH set to 0) See Table 31 for FCR[5:4] setting restriction when SCR[6]=1 See Table 32 for FCR[7:6] setting restriction when SCR[7]=1

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Table 4-2988. Instance Table

Instance Name	Physical Address
UART0	5230 0008h
UART1	5230 1008h
UART2	5230 2008h
UART3	5230 3008h
UART4	5230 4008h
UART5	5230 5008h

Figure 4-1400. UART_FCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RX_FIFO_TRIG		TX_FIFO_TRIG		DMA_MODE	TX_FIFO_CLEAR	RX_FIFO_CLEAR	FIFO_EN
R								W		W		W	W	W	W
0h								0h		0h		0h	0h	0h	0h

Access Types Legend

Table 4-2989. UART_FCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reset Source: mod_g_arstn
7:6	RX_FIFO_TRIG	W	0h	Sets the trigger level for the RX FIFO: If SCR[7] = 0 and TLR[7:4] = 0000: 00: 8 characters 01: 16 characters 10: 56 characters 11: 60 characters If SCR[7] = 0 and TLR[7:4] != 0000, RX_FIFO_TRIG is not considered. If SCR[7]=1, RX_FIFO_TRIG is 2 LSB of the trigger level [1-63 on 6 bits] with the granularity 1. Reset Source: mod_g_arstn
5:4	TX_FIFO_TRIG	W	0h	Sets the trigger level for the TX FIFO: If SCR[6] = 0 and TLR[3:0] = 0000: 00: 8 spaces 01: 16 spaces 10: 32 spaces 11: 56 spaces If SCR[6] = 0 and TLR[3:0] != 0000, TX_FIFO_TRIG is not considered. If SCR[6]=1, TX_FIFO_TRIG is 2 LSB of the trigger level [1-63 on 6 bits] with the granularity 1 Reset Source: mod_g_arstn
3	DMA_MODE	W	0h	This register is considered if SCR[0] = 0. Reset Source: mod_g_arstn 1 DMA_MODE_Value_1 DMA_MODE 1 (UART_nDMA_REQ[0] in TX, UART_nDMA_REQ[1] in RX)
2	TX_FIFO_CLEAR	W	0h	Reset Source: mod_g_arstn 1 TX_FIFO_CLEAR_Value_ Clears the transmit FIFO and 1 resets its counter logic to zero. Returns to zero after clearing FIFO.
1	RX_FIFO_CLEAR	W	0h	Reset Source: mod_g_arstn 1 RX_FIFO_CLEAR_Value_ Clears the receive FIFO and 1 resets its counter logic to zero. Returns to zero after clearing FIFO.

Table 4-2989. UART_FCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	FIFO_EN	W	0h	Reset Source: mod_g_arstn 1 FIFO_EN_Value_1 : Enables the transmit and receive FIFOs.The transmit and receive holding registers are 64-bytes FIFOs.

4.23.10 UART_IIR_CIR Registers

4.23.10.1 IIR_CIR Register (Offset = 8h) [reset = 0h]

Short Description: The IIR is a read-only re

Long Description: The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.

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Table 4-2990. Instance Table

Instance Name	Physical Address
UART0	5230 0008h
UART1	5230 1008h
UART2	5230 2008h
UART3	5230 3008h
UART4	5230 4008h
UART5	5230 5008h

Figure 4-1401. UART_IIR_CIR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										TX_STATUS_IT	RESERVED	RX_OE_IT	RX_STOP_IT	THR_IT	RHR_IT
NONE										R	NONE	R	R	R	R
0										0h	0	0h	0h	0h	0h

Access Types Legend

Table 4-2991. UART_IIR_CIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE		Reserved
5	TX_STATUS_IT	R	0h	Reset Source: mod_g_arstn 1 TX_STATUS_IT_Value_1 TX status interrupt active
4	RESERVED	NONE		Reserved
3	RX_OE_IT	R	0h	Reset Source: mod_g_arstn 1 RX_OE_IT_Value_1 RX overrun interrupt active
2	RX_STOP_IT	R	0h	Reset Source: mod_g_arstn 1 RX_STOP_IT_Value_1 Receive stop interrupt active
1	THR_IT	R	0h	Reset Source: mod_g_arstn 1 THR_IT_Value_1 THR interrupt active
0	RHR_IT	R	0h	Reset Source: mod_g_arstn 1 RHR_IT_Value_1 RHR interrupt active

4.23.11 UART_IIR_IRDA Registers

4.23.11.1 IIR_IRDA Register (Offset = 8h) [reset = 0h]

Short Description: The IIR is a read-only re

Long Description: The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.

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Table 4-2992. Instance Table

Instance Name	Physical Address
UART0	5230 0008h
UART1	5230 1008h
UART2	5230 2008h
UART3	5230 3008h
UART4	5230 4008h
UART5	5230 5008h

Figure 4-1402. UART_IIR_IRDA Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								EOF_IT	LINE_STS_IT	TX_STATUS_IT	STS_FIFO_IT	RX_OE_IT	RX_FIFO_LAST_BYTE_IT	THR_IT	RHR_IT
NONE								R	R	R	R	R	R	R	R
0								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-2993. UART_IIR_IRDA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7	EOF_IT	R	0h	Reset Source: mod_g_arstn 1 EOF_IT_Value_1 Received EOF interrupt active
6	LINE_STS_IT	R	0h	Reset Source: mod_g_arstn 1 LINE_STS_IT_Value_1 Receiver line status interrupt active
5	TX_STATUS_IT	R	0h	Reset Source: mod_g_arstn 1 TX_STATUS_IT_Value_1 TX status interrupt active
4	STS_FIFO_IT	R	0h	Reset Source: mod_g_arstn 1 STS_FIFO_IT_Value_1 Status FIFO trigger level interrupt active
3	RX_OE_IT	R	0h	Reset Source: mod_g_arstn 1 RX_OE_IT_Value_1 RX overrun interrupt active
2	RX_FIFO_LAST_BYTE_IT	R	0h	Reset Source: mod_g_arstn 1 RX_FIFO_LAST_BYTE_IT Last byte of frame in RX FIFO _Value_1 interrupt active
1	THR_IT	R	0h	Reset Source: mod_g_arstn 1 THR_IT_Value_1 THR interrupt active
0	RHR_IT	R	0h	Reset Source: mod_g_arstn 1 RHR_IT_Value_1 RHR interrupt active

4.23.12 UART_IIR_UART Registers

4.23.12.1 IIR_UART Register (Offset = 8h) [reset = 1h]

Short Description: The IIR is a read-only re

Long Description: The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.

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Table 4-2994. Instance Table

Instance Name	Physical Address
UART0	5230 0008h
UART1	5230 1008h
UART2	5230 2008h
UART3	5230 3008h
UART4	5230 4008h
UART5	5230 5008h

Figure 4-1403. UART_IIR_UART Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								FCR_MIRROR		IT_TYPE					IT_PENDING
R								R		R					R
0h								0h		0h					1h

Access Types Legend

Table 4-2995. UART_IIR_UART Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reset Source: mod_g_arstn
7:6	FCR_MIRROR	R	0h	Mirror the contents of FCR[0] on both bits. Reset Source: mod_g_arstn
5:1	IT_TYPE	R	0h	Reset Source: mod_g_arstn 16 IT_TYPE_Value_10 CTS, RTS, DSR change state from active (low) to inactive (high). Priority=6 8 IT_TYPE_Value_8 Xoff/Special character. Priority=5 6 IT_TYPE_Value_6 Rx timeout. Priority=2 3 IT_TYPE_Value_3 Receiver line status error. Priority=3 2 IT_TYPE_Value_2 RHR interrupt. Priority=2 1 IT_TYPE_Value_1 THR interrupt. Priority=3
0	IT_PENDING	R	1h	Reset Source: mod_g_arstn 1 IT_PENDING_Value_1 No interrupt is pending

4.23.13 UART_LCR Registers

4.23.13.1 LCR Register (Offset = Ch) [reset = 0h]

Short Description: LCR[6:0] define parameter

Long Description: LCR[6:0] define parameters of the transmission and reception. Note: As soon as LCR[6] is set to 1, the TX line is forced to 0 and remains in this state as long as LCR[6] = 1.

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Table 4-2996. Instance Table

Instance Name	Physical Address
UART0	5230 000Ch
UART1	5230 100Ch
UART2	5230 200Ch
UART3	5230 300Ch
UART4	5230 400Ch
UART5	5230 500Ch

Figure 4-1404. UART_LCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								DIV_EN	BREAK_EN	PARITY_TYPE2	PARITY_TYPE1	PARITY_EN	NB_STOP	CHAR_LENGTH	
R								R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h								0h	0h	0h	0h	0h	0h	0h	

Access Types Legend

Table 4-2997. UART_LCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reset Source: mod_g_arstn
7	DIV_EN	R/W	0h	Reset Source: mod_g_arstn 1 DIV_EN_Value_1 Divisor latch enable. Allows to access to DLL, DLH and other registers (refer to the registers mapping)
6	BREAK_EN	R/W	0h	Break control bit. Reset Source: mod_g_arstn 1 BREAK_EN_Value_1 Forces the transmitter output to go low to alert the communication terminal
5	PARITY_TYPE2	R/W	0h	Selects the forced parity format [if LCR[3] = 1]. If LCR[5] = 1 and LCR[4] = 0, the parity bit is forced to 1 in the transmitted and received data. If LCR[5] = 1 and LCR[4] = 1, the parity bit is forced to 0 in the transmitted and received data. Reset Source: mod_g_arstn
4	PARITY_TYPE1	R/W	0h	Reset Source: mod_g_arstn 1 PARITY_TYPE1_Value_1 Even parity is generated (if LCR[3] = 1)
3	PARITY_EN	R/W	0h	Reset Source: mod_g_arstn 1 PARITY_EN_Value_1 A parity bit is generated during transmission and the receiver checks for received parity.
2	NB_STOP	R/W	0h	Specifies the number of stop bits: Reset Source: mod_g_arstn 1 NB_STOP_Value_1 1.5 stop bits (word length = 5) in USART mode. 2 stop bits (word length = 6, 7, 8)

Table 4-2997. UART_LCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	CHAR_LENGTH	R/W	0h	Specifies the word length to be transmitted or received. Reset Source: mod_g_arstn 3 CHAR_LENGTH_Value_3 8 bits 2 CHAR_LENGTH_Value_2 7 bits 1 CHAR_LENGTH_Value_1 6 bits

4.23.14 UART_MCR Registers

4.23.14.1 MCR Register (Offset = 10h) [reset = 0h]

Short Description: MCR[3:0] controls the int

Long Description: MCR[3:0] controls the interface with the modem, data set or peripheral device that is emulating the modem.

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Table 4-2998. Instance Table

Instance Name	Physical Address
UART0	5230 0010h
UART1	5230 1010h
UART2	5230 2010h
UART3	5230 3010h
UART4	5230 4010h
UART5	5230 5010h

Figure 4-1405. UART_MCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RESERVED	TCR_TLR	XON_EN	LOOPBACK_EN	CD_STS_CH	RI_STS_CH	RTS	DTR
R								R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-2999. UART_MCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reset Source: mod_g_arstn
7	RESERVED	R		Reset Source: mod_g_arstn
6	TCR_TLR	R/W	0h	Reset Source: mod_g_arstn 1 TCR_TLR_Value_1 Enables access to the TCR and TLR registers.
5	XON_EN	R/W	0h	Reset Source: mod_g_arstn 1 XON_EN_Value_1 Enable 'XON any' function
4	LOOPBACK_EN	R/W	0h	Reset Source: mod_g_arstn 1 LOOPBACK_EN_Value_1 Enable local loopback mode (internal). In this mode the MCR[3:0] signals are looped back into MSR[7:4]. The transmit output is looped back to the receive input internally
3	CD_STS_CH	R/W	0h	Reset Source: mod_g_arstn 1 CD_STS_CH_Value_1 In loopback forces DCD* input low and IRQ outputs to inactive state.
2	RI_STS_CH	R/W	0h	Reset Source: mod_g_arstn 1 RI_STS_CH_Value_1 In loopback forces RI* input low.
1	RTS	R/W	0h	In loop back controls MSR[4]. If auto-RTS is enabled the RTS* output is controlled by hardware flow control. Reset Source: mod_g_arstn 1 RTS_Value_1 Force RTS* output to active (low).
0	DTR	R/W	0h	Reset Source: mod_g_arstn 1 DTR_Value_1 Force DTR* output to active (low).

4.23.15 UART_XON1_ADDR1 Registers

4.23.15.1 XON1_ADDR1 Register (Offset = 10h) [reset = 0h]

Short Description: XON1/ADDR1 Register

Long Description: XON1/ADDR1 Register

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Table 4-3000. Instance Table

Instance Name	Physical Address
UART0	5230 0010h
UART1	5230 1010h
UART2	5230 2010h
UART3	5230 3010h
UART4	5230 4010h
UART5	5230 5010h

Figure 4-1406. UART_XON1_ADDR1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								XON_WORD1							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-3001. UART_XON1_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	XON_WORD1	R/W	0h	Used to store the 8-bit XON1 character in UART modes and ADDR1 address 1 for IrDA modes. Reset Source: mod_g_arstn

4.23.16 UART_LSR_CIR Registers

4.23.16.1 LSR_CIR Register (Offset = 14h) [reset = 81h]

Short Description:

Long Description:

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Table 4-3002. Instance Table

Instance Name	Physical Address
UART0	5230 0014h
UART1	5230 1014h
UART2	5230 2014h
UART3	5230 3014h
UART4	5230 4014h
UART5	5230 5014h

Figure 4-1407. UART_LSR_CIR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
f4240															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								THR_EMPTY	RESERVED	RX_STOP	RESERVED				RX_FIFO_E
NONE								R	R	R	NONE				R
f4240								1h	0h	0h	0				1h

Access Types Legend

Table 4-3003. UART_LSR_CIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7	THR_EMPTY	R	1h	Reset Source: mod_g_arstn 1 THR_EMPTY_Value_1 Transmit hold register (TX FIFO) is empty. The transmission is not necessarily completed
6	RESERVED	R		Reset Source: mod_g_arstn
5	RX_STOP	R	0h	The RX_STOP is generated based on the value set in the BOF Length register (EBLR). It is cleared on a single read of the LSR register Reset Source: mod_g_arstn 1 RX_STOP_Value_1 Reception is completed
4:1	RESERVED	NONE		Reserved
0	RX_FIFO_E	R	1h	Reset Source: mod_g_arstn 1 RX_FIFO_E_Value_1 At least one data character in the RX FIFO

4.23.17 UART_LSR_IRDA Registers

4.23.17.1 LSR_IRDA Register (Offset = 14h) [reset = 83h]

Short Description:

Long Description:

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Table 4-3004. Instance Table

Instance Name	Physical Address
UART0	5230 0014h
UART1	5230 1014h
UART2	5230 2014h
UART3	5230 3014h
UART4	5230 4014h
UART5	5230 5014h

Figure 4-1408. UART_LSR_IRDA Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
f4241															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								THR_EMPTY	STS_FIFO_FULL	RX_LAST_BYTE	FRAME_TOO_LONG	ABORT	CRC	STS_FIFO_E	RX_FIFO_E
NONE								R	R	R	R	R	R	R	R
f4241								1h	0h	0h	0h	0h	0h	1h	1h

Access Types Legend

Table 4-3005. UART_LSR_IRDA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7	THR_EMPTY	R	1h	Reset Source: mod_g_arstn 1 THR_EMPTY_Value_1 Transmit hold register (TX FIFO) is empty. The transmission is not necessarily completed
6	STS_FIFO_FULL	R	0h	Reset Source: mod_g_arstn 1 STS_FIFO_FULL_Value_ Status FIFO full 1
5	RX_LAST_BYTE	R	0h	Reset Source: mod_g_arstn 1 RX_LAST_BYTE_Value_1 The RX FIFO (RHR) contains the last byte of the frame to be read.This bit is only set when the last byte of a frame is available to be read. It is used to determine the frame boundary. It is cleared on a single read of the LSR register
4	FRAME_TOO_LONG	R	0h	Reset Source: mod_g_arstn 1 FRAME_TOO_LONG_Value Frame-too-long error in the _1 frame at the top of the STATUS FIFO, [next character to be read]. This bit is set to 1 when a frame exceeding the maximum length (set by RXFLH and RXFLL registers) has been received. When this error is detected, current frame reception is terminated. Reception is stopped until the next START flag is detected
3	ABORT	R	0h	Reset Source: mod_g_arstn 1 ABORT_Value_1 Abort pattern is received. SIR & MIR: Abort pattern. FIR: Illegal symbol
2	CRC	R	0h	Reset Source: mod_g_arstn 1 CRC_Value_1 CRC error in the frame at the top of the STATUS FIFO (next character to be read)

Table 4-3005. UART_LSR_IRDA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	STS_FIFO_E	R	1h	Reset Source: mod_g_arstn 1 STS_FIFO_E_Value_1 Status FIFO empty
0	RX_FIFO_E	R	1h	Reset Source: mod_g_arstn 1 RX_FIFO_E_Value_1 At least one data character in the RX FIFO

4.23.18 UART_LSR_UART Registers

4.23.18.1 LSR_UART Register (Offset = 14h) [reset = 60h]

Short Description:

Long Description:

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Table 4-3006. Instance Table

Instance Name	Physical Address
UART0	5230 0014h
UART1	5230 1014h
UART2	5230 2014h
UART3	5230 3014h
UART4	5230 4014h
UART5	5230 5014h

Figure 4-1409. UART_LSR_UART Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RX_FIFO_STS	TX_SR_E	TX_FIFO_E	RX_BI	RX_FE	RX_PE	RX_OE	RX_FIFO_E
R								R	R	R	R	R	R	R	R
0h								0h	1h	1h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-3007. UART_LSR_UART Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reset Source: mod_g_arstn
7	RX_FIFO_STS	R	0h	Reset Source: mod_g_arstn 1 RX_FIFO_STS_Value_1 At least one parity error, framing error or break indication in the RX FIFO. Bit 7 is cleared when no more errors are present in the RX FIFO.
6	TX_SR_E	R	1h	Reset Source: mod_g_arstn 1 TX_SR_E_Value_1 Transmitter hold (TX FIFO) and shift registers are empty
5	TX_FIFO_E	R	1h	Reset Source: mod_g_arstn 1 TX_FIFO_E_Value_1 Transmit hold register (TX FIFO) is empty. The transmission is not necessarily completed.
4	RX_BI	R	0h	Reset Source: mod_g_arstn 1 RX_BI_Value_1 A break was detected while the data being read from the RX FIFO was being received. (i.e. RX input was low for one character + 1 bit time frame).
3	RX_FE	R	0h	Reset Source: mod_g_arstn 1 RX_FE_Value_1 Framing error occurred in data being read from RX FIFO.(received data did not have a valid stop bit)
2	RX_PE	R	0h	Reset Source: mod_g_arstn 1 RX_PE_Value_1 Parity error in data being read from RX FIFO
1	RX_OE	R	0h	Reset Source: mod_g_arstn 1 RX_OE_Value_1 Overrun error has occurred. Set when the character held in the receive shift register is not transferred to the RX FIFO. This case can occurs only when receive FIFO is full.

Table 4-3007. UART_LSR_UART Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RX_FIFO_E	R	0h	Reset Source: mod_g_arstn 1 RX_FIFO_E_Value_1 At least one data character in the RX FIFO

4.23.19 UART_XON2_ADDR2 Registers

4.23.19.1 XON2_ADDR2 Register (Offset = 14h) [reset = 0h]

Short Description: XON2/ADDR2 Register

Long Description: XON2/ADDR2 Register

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Table 4-3008. Instance Table

Instance Name	Physical Address
UART0	5230 0014h
UART1	5230 1014h
UART2	5230 2014h
UART3	5230 3014h
UART4	5230 4014h
UART5	5230 5014h

Figure 4-1410. UART_XON2_ADDR2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								XON_WORD2							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-3009. UART_XON2_ADDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	XON_WORD2	R/W	0h	Used to store the 8-bit XON2 character in UART modes and ADDR2 address 2 for IrDA modes. Reset Source: mod_g_arstn

4.23.20 UART_MSR Registers

4.23.20.1 MSR Register (Offset = 18h) [reset = 0h]

Short Description: This register provides in

Long Description: This register provides information about the current state of the control lines from the modem, data set or peripheral device to the LH. It also indicates when a control input from the modem changes state.

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Table 4-3010. Instance Table

Instance Name	Physical Address
UART0	5230 0018h
UART1	5230 1018h
UART2	5230 2018h
UART3	5230 3018h
UART4	5230 4018h
UART5	5230 5018h

Figure 4-1411. UART_MSR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								NCD_STS	NRI_STS	NDSR_STS	NCTS_STS	DCD_STS	RI_STS	DSR_STS	CTS_STS
R								R	R	R	R	R	R	R	R
0h								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-3011. UART_MSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reset Source: mod_g_arstn
7	NCD_STS	R	0h	This bit is the complement of the DCD* input. In loop-back mode it is equivalent to MCR[3] Reset Source: mod_g_arstn
6	NRI_STS	R	0h	This bit is the complement of the RI* input. In loop-back mode it is equivalent to MCR[2] Reset Source: mod_g_arstn
5	NDSR_STS	R	0h	This bit is the complement of the DSR* input. In loop-back mode, it is equivalent to MCR[0] Reset Source: mod_g_arstn
4	NCTS_STS	R	0h	This bit is the complement of the CTS* input. In loop-back mode it is equivalent to MCR[1] Reset Source: mod_g_arstn
3	DCD_STS	R	0h	Indicates that DCD* input [or MCR[3] in loop back] has changed. Cleared on a read. Reset Source: mod_g_arstn
2	RI_STS	R	0h	Indicates that RI* input [or MCR[2] in loop back] has changed state from low to high. Cleared on a read. Reset Source: mod_g_arstn
1	DSR_STS	R	0h	Reset Source: mod_g_arstn 1 DSR_STS_Value_1 Indicates that DSR* input (or MCR[0] in loop back) has changed state. Cleared on a read
0	CTS_STS	R	0h	Reset Source: mod_g_arstn 1 CTS_STS_Value_1 Indicates that CTS* input (or MCR[1] in loop back) has changed state. Cleared on a read.

4.23.21 UART_TCR Registers

4.23.21.1 TCR Register (Offset = 18h) [reset = fh]

Short Description: Transmission Control Regi

Long Description: Transmission Control Register

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Table 4-3012. Instance Table

Instance Name	Physical Address
UART0	5230 0018h
UART1	5230 1018h
UART2	5230 2018h
UART3	5230 3018h
UART4	5230 4018h
UART5	5230 5018h

Figure 4-1412. UART_TCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
6f															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RX_FIFO_TRIG_START				RX_FIFO_TRIG_HALT			
NONE								R/W				R/W			
6f								0h				fh			

Access Types Legend

Table 4-3013. UART_TCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:4	RX_FIFO_TRIG_START	R/W	0h	RX FIFO trigger level to RESTORE transmission (0 - 60) Reset Source: mod_g_arstn
3:0	RX_FIFO_TRIG_HALT	R/W	Fh	RX FIFO trigger level to HALT transmission (0 - 60) Reset Source: mod_g_arstn

4.23.22 UART_XOFF1 Registers

4.23.22.1 XOFF1 Register (Offset = 18h) [reset = 0h]

Short Description: XOFF1 Register

Long Description: XOFF1 Register

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Table 4-3014. Instance Table

Instance Name	Physical Address
UART0	5230 0018h
UART1	5230 1018h
UART2	5230 2018h
UART3	5230 3018h
UART4	5230 4018h
UART5	5230 5018h

Figure 4-1413. UART_XOFF1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								XOFF_WORD1							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-3015. UART_XOFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	XOFF_WORD1	R/W	0h	Used to store the 8-bit XOFF1 character in used in UART modes. Reset Source: mod_g_arstn

4.23.23 UART_SPR Registers

4.23.23.1 SPR Register (Offset = 1Ch) [reset = 0h]

Short Description: This read/write register

Long Description: This read/write register does not control the module in anyway. It is intended as a scratchpad register to be used by the programmer to hold temporary data.

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Table 4-3016. Instance Table

Instance Name	Physical Address
UART0	5230 001Ch
UART1	5230 101Ch
UART2	5230 201Ch
UART3	5230 301Ch
UART4	5230 401Ch
UART5	5230 501Ch

Figure 4-1414. UART_SPR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								SPR_WORD							
R								R/W							
0h								0h							

Access Types Legend

Table 4-3017. UART_SPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reset Source: mod_g_arstn
7:0	SPR_WORD	R/W	0h	Scratchpad register Reset Source: mod_g_arstn

4.23.24 UART_TLR Registers

4.23.24.1 TLR Register (Offset = 1Ch) [reset = 0h]

Short Description: Trigger Level Register

Long Description: Trigger Level Register

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Table 4-3018. Instance Table

Instance Name	Physical Address
UART0	5230 001Ch
UART1	5230 101Ch
UART2	5230 201Ch
UART3	5230 301Ch
UART4	5230 401Ch
UART5	5230 501Ch

Figure 4-1415. UART_TLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RX_FIFO_TRIG_DMA				TX_FIFO_TRIG_DMA			
NONE								R/W				R/W			
0								0h				0h			

Access Types Legend

Table 4-3019. UART_TLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:4	RX_FIFO_TRIG_DMA	R/W	0h	Receive FIFO trigger level Reset Source: mod_g_arstn
3:0	TX_FIFO_TRIG_DMA	R/W	0h	Transmit FIFO trigger level Reset Source: mod_g_arstn

4.23.25 UART_XOFF2 Registers

4.23.25.1 XOFF2 Register (Offset = 1Ch) [reset = 0h]

Short Description: XOFF2 Register

Long Description: XOFF2 Register

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Table 4-3020. Instance Table

Instance Name	Physical Address
UART0	5230 001Ch
UART1	5230 101Ch
UART2	5230 201Ch
UART3	5230 301Ch
UART4	5230 401Ch
UART5	5230 501Ch

Figure 4-1416. UART_XOFF2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								XOFF_WORD2							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-3021. UART_XOFF2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	XOFF_WORD2	R/W	0h	Used to store the 8-bit XOFF2 character in used in UART modes. Reset Source: mod_g_arstn

4.23.26 UART_MDR1 Registers

4.23.26.1 MDR1 Register (Offset = 20h) [reset = 7h]

Short Description: The mode of operation can

Long Description: The mode of operation can be programmed by writing to MDR1[2:0] and therefore the MDR1 must be programmed on start-up after configuration of the configuration registers (DLL, DLH, LCR). The value of MDR1[2:0] must not be changed again during normal operation. Note: If the module is disabled by setting the MODE_SELECT field to

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Table 4-3022. Instance Table

Instance Name	Physical Address
UART0	5230 0020h
UART1	5230 1020h
UART2	5230 2020h
UART3	5230 3020h
UART4	5230 4020h
UART5	5230 5020h

Figure 4-1417. UART_MDR1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								FRAME_END_MODE	SIP_MODE	SCT	SET_TXIR	IR_SLEEP	MODE_SELECT		
R								R/W	R/W	R/W	R/W	R/W	R/W		
0h								0h	0h	0h	0h	0h	7h		

Access Types Legend

Table 4-3023. UART_MDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reset Source: mod_g_arstn
7	FRAME_END_MODE	R/W	0h	IrDA mode only. Reset Source: mod_g_arstn 1 FRAME_END_MODE_Value Set EOT bit method _1
6	SIP_MODE	R/W	0h	MIR/FIR modes only. Reset Source: mod_g_arstn 1 SIP_MODE_Value_1 Automatic SIP mode: SIP is generated after each transmission.
5	SCT	R/W	0h	Store and control the transmission Reset Source: mod_g_arstn 1 SCT_Value_1 Starts the Infrared transmission with the control of ACREG[2]. Note: before starting any transmission, there must be no reception on going.
4	SET_TXIR	R/W	0h	Used to configure the infrared transceiver. Reset Source: mod_g_arstn 1 SET_TXIR_Value_1 TXIR pin output is forced high (not dependant of MDR2[7] value).
3	IR_SLEEP	R/W	0h	Reset Source: mod_g_arstn 1 IR_SLEEP_Value_1 IrDA/CIR sleep mode enabled

Table 4-3023. UART_MDR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	MODE_SELECT	R/W	7h	Reset Source: mod_g_arstn 7 MODE_SELECT_Value_7 Disable (default state) 6 MODE_SELECT_Value_6 CIR mode 5 MODE_SELECT_Value_5 FIR mode 4 MODE_SELECT_Value_4 MIR mode 3 MODE_SELECT_Value_3 UART 13x mode 2 MODE_SELECT_Value_2 UART 16x auto-baud 1 MODE_SELECT_Value_1 SIR mode

4.23.27 UART_MDR2 Registers

4.23.27.1 MDR2 Register (Offset = 24h) [reset = 0h]

Short Description: IR-IrDA and IR-CIR modes

Long Description: IR-IrDA and IR-CIR modes only. MDR2[0] describes the status of the interrupt in IIR[5]. The IRTX_UNDERRUN bit should be read after an IIR[5] TX_STATUS_IT interrupt has occurred. The bits [2:1] of this register sets the trigger level for the frame status FIFO (8 entries) and must be programmed before the mode is programmed in MDR1[2:0]. Note: The MDR2[6] gives the flexibility to invert the RX pin inside the UART module to ensure that the protocol at the input of the transceiver module has the same polarity at module level. By default, the RX pin is inverted because most of transceiver invert the IR receive pin.

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Table 4-3024. Instance Table

Instance Name	Physical Address
UART0	5230 0024h
UART1	5230 1024h
UART2	5230 2024h
UART3	5230 3024h
UART4	5230 4024h
UART5	5230 5024h

Figure 4-1418. UART_MDR2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								SET_TXIR_ALT	IRRXINVERT	CIR_PULSE_MODE		UART_PULSE	STS_FIFO_TRIG		IRTX_UNDERRUN
R								R/W	R/W	R/W		R/W	R/W		R
0h								0h	0h	0h		0h	0h		0h

Access Types Legend

Table 4-3025. UART_MDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reset Source: mod_g_arstn
7	SET_TXIR_ALT	R/W	0h	Provide alternate functionnality for MDR1[4] [SET_TXIR] Reset Source: mod_g_arstn 1 SET_TXIR_ALT_Value_1 Alternate mode for SET_TXIR
6	IRRXINVERT	R/W	0h	Only for IR mode [IRDA & CIR]Invert RX pin inside the module before the voting or sampling system logic of the infra red block. This will not affect the RX path in UART Modem modes. Reset Source: mod_g_arstn 1 IRRXINVERT_Value_1 No inversion is performed
5:4	CIR_PULSE_MODE	R/W	0h	CIR Pulse modulation definition. It defines high level of the pulse width associated with a digit: Reset Source: mod_g_arstn 3 CIR_PULSE_MODE_Value Pulse width of 6 from 12 _3 cycles 2 CIR_PULSE_MODE_Value Pulse width of 5 from 12 _2 cycles 1 CIR_PULSE_MODE_Value Pulse width of 4 from 12 _1 cycles
3	UART_PULSE	R/W	0h	UART mode only. Used to allow pulse shaping in UART mode. Reset Source: mod_g_arstn 1 UART_PULSE_Value_1 UART mode with a pulse shaping

Table 4-3025. UART_MDR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:1	STS_FIFO_TRIG	R/W	0h	Only for IR-IRDA mode. Frame Status FIFO Threshold select: Reset Source: mod_g_arstn 3 STS_FIFO_TRIG_Value_ 8 entries 3 2 STS_FIFO_TRIG_Value_ 7 entries 2 1 STS_FIFO_TRIG_Value_ 4 entries 1
0	IRTX_UNDERRUN	R	0h	IRDA Transmission status interrupt.When the IIR[5] interrupt occurs, the meaning of the interrupt is : Reset Source: mod_g_arstn 1 IRTX_UNDERRUN_Value_ an underrun has occurred. The 1 last bit of the frame has been transmitted but with an underrun error present. The bit is reset to '0' when the RESUME register is read.

4.23.28 UART_SFLSR Registers

4.23.28.1 SFLSR Register (Offset = 28h) [reset = 0h]

Short Description: IrDA modes only. Reading

Long Description: IrDA modes only. Reading this register effectively reads frame status information from the status FIFO (this register doesn't physically exist). Reading this register will increment the status FIFO read pointer (SFREGL and SFREGH must be read first).

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Table 4-3026. Instance Table

Instance Name	Physical Address
UART0	5230 0028h
UART1	5230 1028h
UART2	5230 2028h
UART3	5230 3028h
UART4	5230 4028h
UART5	5230 5028h

Figure 4-1419. UART_SFLSR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RESERVED5			OE_ERROR	FRAME_TOO_LONG_ERROR	ABORT_DETECT	CRC_ERROR	RESERVED0
R								R			R	R	R	R	R
0h								0h			0h	0h	0h	0h	0h

Access Types Legend

Table 4-3027. UART_SFLSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reset Source: mod_g_arstn
7:5	RESERVED5	R	0h	Reset Source: mod_g_arstn
4	OE_ERROR	R	0h	Reset Source: mod_g_arstn 1 OE_ERROR_Value_1 Overrun error in RX FIFO when frame at top of RX FIFO was received.
3	FRAME_TOO_LONG_ERROR	R	0h	Reset Source: mod_g_arstn 1 FRAME_TOO_LONG_ERROR Frame-length too long error in _Value_1 frame at top of RX FIFO.
2	ABORT_DETECT	R	0h	Reset Source: mod_g_arstn 1 ABORT_DETECT_Value_1 Abort pattern detected in frame at top of RX FIFO
1	CRC_ERROR	R	0h	Reset Source: mod_g_arstn 1 CRC_ERROR_Value_1 CRC error in frame at top of RX FIFO. top of RX FIFO = Next frame to be read from RX FIFO
0	RESERVED0	R	0h	Reset Source: mod_g_arstn

4.23.29 UART_TXFLL Registers

4.23.29.1 TXFLL Register (Offset = 28h) [reset = 0h]

Short Description: IrDA modes only. The reg

Long Description: IrDA modes only. The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.

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Table 4-3028. Instance Table

Instance Name	Physical Address
UART0	5230 0028h
UART1	5230 1028h
UART2	5230 2028h
UART3	5230 3028h
UART4	5230 4028h
UART5	5230 5028h

Figure 4-1420. UART_TXFLL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								TXFLL							
R								W							
0h								0h							

Access Types Legend

Table 4-3029. UART_TXFLL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reset Source: mod_g_arstn
7:0	TXFLL	W	0h	LSB register used to specify the frame length Reset Source: mod_g_arstn

4.23.30 UART_RESUME Registers

4.23.30.1 RESUME Register (Offset = 2Ch) [reset = 0h]

Short Description: IR-IrDA and IR-CIR modes

Long Description: IR-IrDA and IR-CIR modes only. This register is used to clear internal flags, which halt transmission/reception when an underrun/overrun error occurs. Reading this register resumes the halted operation. This register does not physically exist and reads always as 0x00.

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Table 4-3030. Instance Table

Instance Name	Physical Address
UART0	5230 002Ch
UART1	5230 102Ch
UART2	5230 202Ch
UART3	5230 302Ch
UART4	5230 402Ch
UART5	5230 502Ch

Figure 4-1421. UART_RESUME Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RESUME							
R								R							
0h								0h							

Access Types Legend

Table 4-3031. UART_RESUME Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reset Source: mod_g_arstn
7:0	RESUME	R	0h	Dummy read to restart the TX or RX Reset Source: mod_g_arstn

4.23.31 UART_TXFLH Registers

4.23.31.1 TXFLH Register (Offset = 2Ch) [reset = 0h]

Short Description: IrDA modes only. The regi

Long Description: IrDA modes only. The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.

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Table 4-3032. Instance Table

Instance Name	Physical Address
UART0	5230 002Ch
UART1	5230 102Ch
UART2	5230 202Ch
UART3	5230 302Ch
UART4	5230 402Ch
UART5	5230 502Ch

Figure 4-1422. UART_TXFLH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RESERVED			TXFLH				
R								R			W				
0h								0h			0h				

Access Types Legend

Table 4-3033. UART_TXFLH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reset Source: mod_g_arstn
7:5	RESERVED	R		Reset Source: mod_g_arstn
4:0	TXFLH	W	0h	MSB register used to specify the frame length Reset Source: mod_g_arstn

4.23.32 UART_RXFLL Registers

4.23.32.1 RXFLL Register (Offset = 30h) [reset = 0h]

Short Description: IrDA modes only. The reg

Long Description: IrDA modes only. The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).

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Table 4-3034. Instance Table

Instance Name	Physical Address
UART0	5230 0030h
UART1	5230 1030h
UART2	5230 2030h
UART3	5230 3030h
UART4	5230 4030h
UART5	5230 5030h

Figure 4-1423. UART_RXFLL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RXFLL							
R								W							
0h								0h							

Access Types Legend

Table 4-3035. UART_RXFLL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reset Source: mod_g_arstn
7:0	RXFLL	W	0h	LSB register used to specify the frame length in reception Reset Source: mod_g_arstn

4.23.33 UART_SFREGL Registers

4.23.33.1 SFREGL Register (Offset = 30h) [reset = 0h]

Short Description: IrDA modes only. The fra

Long Description: IrDA modes only. The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.

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Table 4-3036. Instance Table

Instance Name	Physical Address
UART0	5230 0030h
UART1	5230 1030h
UART2	5230 2030h
UART3	5230 3030h
UART4	5230 4030h
UART5	5230 5030h

Figure 4-1424. UART_SFREGL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								SFREGL							
R								R							
0h								0h							

Access Types Legend

Table 4-3037. UART_SFREGL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reset Source: mod_g_arstn
7:0	SFREGL	R	0h	LSB part of the frame length Reset Source: mod_g_arstn

4.23.34 UART_RXFLH Registers

4.23.34.1 RXFLH Register (Offset = 34h) [reset = 0h]

Short Description: IrDA modes only. The reg

Long Description: IrDA modes only. The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).

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Table 4-3038. Instance Table

Instance Name	Physical Address
UART0	5230 0034h
UART1	5230 1034h
UART2	5230 2034h
UART3	5230 3034h
UART4	5230 4034h
UART5	5230 5034h

Figure 4-1425. UART_RXFLH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RESERVED				RXFLH			
R								R				W			
0h								0h				0h			

Access Types Legend

Table 4-3039. UART_RXFLH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reset Source: mod_g_arstn
7:4	RESERVED	R		Reset Source: mod_g_arstn
3:0	RXFLH	W	0h	MSB register used to specify the frame length in reception Reset Source: mod_g_arstn

4.23.35 UART_SFREGH Registers

4.23.35.1 SFREGH Register (Offset = 34h) [reset = 0h]

Short Description: IrDA modes only. The fra

Long Description: IrDA modes only. The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.

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Table 4-3040. Instance Table

Instance Name	Physical Address
UART0	5230 0034h
UART1	5230 1034h
UART2	5230 2034h
UART3	5230 3034h
UART4	5230 4034h
UART5	5230 5034h

Figure 4-1426. UART_SFREGH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RESERVED				SFREGH			
R								R				R			
0h								0h				0h			

Access Types Legend

Table 4-3041. UART_SFREGH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reset Source: mod_g_arstn
7:4	RESERVED	R		Reset Source: mod_g_arstn
3:0	SFREGH	R	0h	MSB part of the frame length Reset Source: mod_g_arstn

4.23.36 UART_BLR Registers

4.23.36.1 BLR Register (Offset = 38h) [reset = 40h]

Short Description: IrDA modes only. Note th

Long Description: IrDA modes only. Note that BLR[6] is used to select whether 0xC0 or 0xFF start patterns are to be used, when multiple start flags are required in SIR Mode. If only one start flag is required, this will always be 0xC0. If n start flags are required, then either (n-1) 0xC0 or (n-1) 0xFF flags are sent, followed by a single 0xC0 flag (immediately preceding the first data byte).

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Table 4-3042. Instance Table

Instance Name	Physical Address
UART0	5230 0038h
UART1	5230 1038h
UART2	5230 2038h
UART3	5230 3038h
UART4	5230 4038h
UART5	5230 5038h

Figure 4-1427. UART_BLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								STS_FIFO_RESET	XBOF_TYPE	RESERVED					
R								R/W1TS	R/W	R					
0h								0h	1h	0h					

Access Types Legend

Table 4-3043. UART_BLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reset Source: mod_g_arstn
7	STS_FIFO_RESET	R/W1TS	0h	Status FIFO reset. This bit is self-clearing Reset Source: mod_g_arstn
6	XBOF_TYPE	R/W	1h	SIR xBOF select. Reset Source: mod_g_arstn 1 XBOF_TYPE_Value_1 0xC0
5:0	RESERVED	R		Reset Source: mod_g_arstn

4.23.37 UART_UASR Registers

4.23.37.1 UASR Register (Offset = 38h) [reset = 0h]

Short Description: UART Autobauding Status R

Long Description: UART Autobauding Status Register

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Table 4-3044. Instance Table

Instance Name	Physical Address
UART0	5230 0038h
UART1	5230 1038h
UART2	5230 2038h
UART3	5230 3038h
UART4	5230 4038h
UART5	5230 5038h

Figure 4-1428. UART_UASR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PARITY_TYPE		BIT_BY_CHAR	SPEED				
NONE								R		R	R				
0								0h		0h	0h				

Access Types Legend

Table 4-3045. UART_UASR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:6	PARITY_TYPE	R	0h	00 => No Parity identified. 01 => Parity space. 10 => Even Parity. 11 => Odd Parity Reset Source: mod_g_arstn
5	BIT_BY_CHAR	R	0h	0 => 7 bits character identified. 1 => 8 bits character identified Reset Source: mod_g_arstn
4:0	SPEED	R	0h	Used to report the speed identified. 00000 => No speed identified. 00001 => 115200 bauds. 00010 => 57600 bauds. 00011 => 38400 bauds. 00100 => 28800 bauds. 00101 => 19200 bauds. 00110 => 14400 bauds. 00111 => 9600 bauds. 01000 => 4800 bauds. 01001 => 2400 bauds. 01010 => 1200 bauds Reset Source: mod_g_arstn

4.23.38 UART_ACREG Registers

4.23.38.1 ACREG Register (Offset = 3Ch) [reset = 0h]

Short Description: IR-IrDA and IR-CIR modes

Long Description: IR-IrDA and IR-CIR modes only.

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Table 4-3046. Instance Table

Instance Name	Physical Address
UART0	5230 003Ch
UART1	5230 103Ch
UART2	5230 203Ch
UART3	5230 303Ch
UART4	5230 403Ch
UART5	5230 503Ch

Figure 4-1429. UART_ACREG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								PULSE_TYPE	SD_MOD	DIS_IR_RX	DIS_TX_UNDERRUN	SEND_SIP	SCTX_EN	ABORT_EN	EOT_EN
R								R/W	R/W	R/W	R/W	R/W1TS	R/W1TS	R/W	R/W1TS
0h								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-3047. UART_ACREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reset Source: mod_g_arstn
7	PULSE_TYPE	R/W	0h	SIR pulse width select: Reset Source: mod_g_arstn 1 PULSE_TYPE_Value_1 1.6us
6	SD_MOD	R/W	0h	Primary output used to configure transceivers. Connected to the SD/MODE input pin of IrDA transceivers. Reset Source: mod_g_arstn 1 SD_MOD_Value_1 SD pin is set to low
5	DIS_IR_RX	R/W	0h	Reset Source: mod_g_arstn 1 DIS_IR_RX_Value_1 Disables RX input (permanent state - independent of transmit).
4	DIS_TX_UNDERRUN	R/W	0h	It is recommended to disable TX FIFO underrun capability by masking corresponding underrun interrupt. When disabling underrun by setting ACREG[4]=1, garbage data is sent over TX line. Reset Source: mod_g_arstn 1 DIS_TX_UNDERRUN_Valu Long stop bits can be e_1 transmitted, TX underrun is disabled
3	SEND_SIP	R/W1TS	0h	MIR/FIR Modes only.Send Serial Infrared Interaction Pulse [SIP] If this bit is set during a MIR/FIR transmission, the SIP will be send at the end of it.This bit automatically gets cleared at the end of the SIP transmission. Reset Source: mod_g_arstn 1 SEND_SIP_Value_1 Send SIP pulse.
2	SCTX_EN	R/W1TS	0h	Store and controlled TX start. When MDR1[5] = 1 and the LH writes 1 to this bit the TX state machine starts frame transmission. This bit is self-clearing. Reset Source: mod_g_arstn

Table 4-3047. UART_ACREG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ABORT_EN	R/W	0h	Frame Abort. The LH can intentionally abort transmission of a frame by writing 1 to this bit. Neither the end flag nor the CRC bits are appended to the frame. If transmit FIFO is not empty and MDR1[5]=1, UART IrDA will start a new transfer with data of previous frame as soon as abort frame has been sent. Therefore, TX FIFO must be reset before sending an abort frame. Reset Source: mod_g_arstn
0	EOT_EN	R/W1TS	0h	EOT [end of transmission] bit. The LH writes 1 to this bit just before it writes the last byte to the TX FIFO in set-EOT bit frame closing method. This bit automatically gets cleared when the LH writes to the THR [TX FIFO]. Reset Source: mod_g_arstn

4.23.39 UART_SCR Registers

4.23.39.1 SCR Register (Offset = 40h) [reset = 0h]

Short Description: Note: Bit 4 enables the w

Long Description: Note: Bit 4 enables the wake-up interrupt, but this interrupt is not mapped into the IIR register. Therefore, when an interrupt occurs and there is no interrupt pending in the IIR register, the SSR[1] bit must be checked. To clear the wake-up interrupt, bit SCR[4] must be reset to 0.

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Table 4-3048. Instance Table

Instance Name	Physical Address
UART0	5230 0040h
UART1	5230 1040h
UART2	5230 2040h
UART3	5230 3040h
UART4	5230 4040h
UART5	5230 5040h

Figure 4-1430. UART_SCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RX_TRIG_GRANU1	TX_TRIG_GRANU1	DSR_IT	RX_CTS_DSR_WAKE_UP_ENABLE	TX_EMPTY_CTL_IT	DMA_MODE_2		DMA_MODE_CTL
R								R/W	R/W	R/W	R/W	R/W	R/W		R/W
0h								0h	0h	0h	0h	0h	0h		0h

Access Types Legend

Table 4-3049. UART_SCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reset Source: mod_g_arstn
7	RX_TRIG_GRANU1	R/W	0h	Reset Source: mod_g_arstn 1 RX_TRIG_GRANU1_Value ENABLES THE GRANULARITY OF 1 _1 FOR TRIGGER RX LEVEL.
6	TX_TRIG_GRANU1	R/W	0h	Reset Source: mod_g_arstn 1 TX_TRIG_GRANU1_Value Enables the granularity of 1 _1 for trigger TX level.
5	DSR_IT	R/W	0h	Reset Source: mod_g_arstn 1 DSR_IT_Value_1 ENABLES DSR* INTERRUPT.
4	RX_CTS_DSR_WAKE_UP_ENABLE	R/W	0h	Reset Source: mod_g_arstn 1 RX_CTS_DSR_WAKE_UP_E Waits for a falling edge of NABLE_Value_1 pins RX, CTS* or DSR* to generate an interrupt
3	TX_EMPTY_CTL_IT	R/W	0h	Reset Source: mod_g_arstn 1 TX_EMPTY_CTL_IT_Valu THE THR INTERRUPT IS GENERATED e_1 WHEN TX FIFO AND TX SHIFT REGISTER ARE EMPTY.
2:1	DMA_MODE_2	R/W	0h	Used to specify the DMA mode valid if SCR[0] = 1 Reset Source: mod_g_arstn 3 DMA_MODE_2_Value_3 DMA mode 3 (UART_nDMA_REQ[0] in TX) 2 DMA_MODE_2_Value_2 DMA mode 2 (UART_nDMA_REQ[0] in RX) 1 DMA_MODE_2_Value_1 DMA mode 1 (UART_nDMA_REQ[0] in TX, UART_nDMA_REQ[1] in RX)

Table 4-3049. UART_SCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DMA_MODE_CTL	R/W	0h	Reset Source: mod_g_arstn 1 DMA_MODE_CTL_Value_1 The DMA_MODE is set with SCR[2:1]

4.23.40 UART_SSR Registers

4.23.40.1 SSR Register (Offset = 44h) [reset = 4h]

Short Description: Note: Bit 1 is reset only

Long Description: Note: Bit 1 is reset only when SCR[4] is reset to 0.

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Table 4-3050. Instance Table

Instance Name	Physical Address
UART0	5230 0044h
UART1	5230 1044h
UART2	5230 2044h
UART3	5230 3044h
UART4	5230 4044h
UART5	5230 5044h

Figure 4-1431. UART_SSR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RESERVED					DMA_COUNTER_RST	RX_CTS_DSR_WAKE_UP_STS	TX_FIFO_FULL
R								R					R/W	R	R
0h								0h					1h	0h	0h

Access Types Legend

Table 4-3051. UART_SSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reset Source: mod_g_arstn
7:3	RESERVED	R		Reset Source: mod_g_arstn
2	DMA_COUNTER_RST	R/W	1h	Reset Source: mod_g_arstn 1 DMA_COUNTER_RST_Valu The DMA counter will be reset e_1 if corresponding FIFO is reset (via FCR[1] or FCR[2])
1	RX_CTS_DSR_WAKE_UP_STS	R	0h	Reset Source: mod_g_arstn 1 RX_CTS_DSR_WAKE_UP_S A falling edge occurred on RX, TS_Value_1 CTS* or DSR*
0	TX_FIFO_FULL	R	0h	Reset Source: mod_g_arstn 1 TX_FIFO_FULL_Value_1 TX FIFO is full.

4.23.41 UART_EBLR Registers

4.23.41.1 EBLR Register (Offset = 48h) [reset = 0h]

Short Description: IR-IrDA and IR-CIR modes

Long Description: IR-IrDA and IR-CIR modes only. In IR-IrDA SIR operation, this register specifies the number of BOF + xBOFs to transmit. Value set into this register must take into account the BOF character, therefore to only sent one BOF with no XBOF this register must be set to 1. To send one BOF with N XBOF this register must be set to N+1. Furthermore, the value 0 will send 1 BOF plus 255 XBOF. In IR-IrDA MIR mode, this register specifies the number of additional start flags (MIR protocol mandates a minimum of 2 start flags). In IR-CIR mode, this register specifies the number of consecutive zeros to be received before generating the RX_STOP interrupt (IIR[2]). All the received zeros are stored in the RX FIFO. When the register is set to 0, this feature is de-activated and always in reception state which can be disabled by setting the ACREG[5] to

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Table 4-3052. Instance Table

Instance Name	Physical Address
UART0	5230 0048h
UART1	5230 1048h
UART2	5230 2048h
UART3	5230 3048h
UART4	5230 4048h
UART5	5230 5048h

Figure 4-1432. UART_EBLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								EBLR							
R								R/W							
0h								0h							

Access Types Legend

Table 4-3053. UART_EBLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reset Source: mod_g_arstn
7:0	EBLR	R/W	0h	IR-IRDA mode: This register allows to define up to 176 xBOFs, the maximum required by IrDA specification. IR-CIR mode: This register specifies the number of consecutive zeros to be received before generating the RX_STOP interrupt [IIR[2]]. 0x00: feature disabled. 0x01: generate RX_STOP interrupt after receiving one zero bit. ... 0xFF: generate RX_STOP interrupt after receiving 255 zero bits. Reset Source: mod_g_arstn

4.23.42 UART_MVR Registers

4.23.42.1 MVR Register (Offset = 50h) [reset = 47424e03h]

Short Description: The reset value is fixed

Long Description: The reset value is fixed by hardware and corresponds to the RTL revision of this module. A reset has no effect on the value returned Notes: UART / IRDA SIR only module is revision 1.x (WMU_012_1 specification). UART / IRDA with SIR, MIR and FIR support is revision 2.x (WMU_012_2 specification). UART / IRDA with SIR, MIR and FIR / CIR support is revision 3.x (this specification). For example: MVR = 0x30 => Version 3.0 MVR = 0x38 => Version 3.8

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Table 4-3054. Instance Table

Instance Name	Physical Address
UART0	5230 0050h
UART1	5230 1050h
UART2	5230 2050h
UART3	5230 3050h
UART4	5230 4050h
UART5	5230 5050h

Figure 4-1433. UART_MVR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		RESERVED		FUNC											
R		R		R											
1h		0h		742h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL				MAJOR				CUSTOM		MINOR					
R				R				R		R					
9h				6h				0h		3h					

Access Types Legend

Table 4-3055. UART_MVR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme revision number of module Reset Source: mod_g_arstn
29:28	RESERVED	R		Reset Source: mod_g_arstn
27:16	FUNC	R	742h	Function revision number of module Reset Source: mod_g_arstn
15:11	RTL	R	9h	Rtl revision number of module Reset Source: mod_g_arstn
10:8	MAJOR	R	6h	Major revision number of the module. Reset Source: mod_g_arstn
7:6	CUSTOM	R	0h	Custom revision number of the module. Reset Source: mod_g_arstn
5:0	MINOR	R	3h	Minor revision number of the module. Reset Source: mod_g_arstn

4.23.43 UART_SYSC Registers

4.23.43.1 SYSC Register (Offset = 54h) [reset = 0h]

Short Description: The auto idle bit control

Long Description: The auto idle bit controls a power saving technique to reduce the logic power consumption of the OCP interface. That is to say when the feature is enabled, the clock will be gated off until an OCP command for this device has been detected. When the software reset bit is set high it causes a full device reset.

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Table 4-3056. Instance Table

Instance Name	Physical Address
UART0	5230 0054h
UART1	5230 1054h
UART2	5230 2054h
UART3	5230 3054h
UART4	5230 4054h
UART5	5230 5054h

Figure 4-1434. UART_SYSC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RESERVED			IDLEMODE		ENAWAKEUP	SOFTRESET	AUTOIDLE
R								R			R/W		R/W	W	R/W
0h								0h			0h		0h	0h	0h

Access Types Legend

Table 4-3057. UART_SYSC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reset Source: mod_g_arstn
7:5	RESERVED	R		Reset Source: mod_g_arstn
4:3	IDLEMODE	R/W	0h	POWER MANAGEMENT REQ/ACK CONTROL REF: OCP DESIGN GUIDELINES VERSION 1.1 Reset Source: mod_g_arstn 3 IDLEMODE_Value_3 reserved 2 IDLEMODE_Value_2 Smart idle. Acknowledgement to an idle request is given based in the internal activity of the module. 1 IDLEMODE_Value_1 No-idle. An idle request is never acknowledged.
2	ENAWAKEUP	R/W	0h	WAKE UP FEATURE CONTROL Reset Source: mod_g_arstn 1 ENAWAKEUP_Value_1 Wake up capability is enabled
1	SOFTRESET	W	0h	Software reset. Set this bit to 1 to trigger a module reset. This bit is automatically reset by the hardware. During reads it always returns a 0. Reset Source: mod_g_arstn 1 SOFTRESET_Value_1 The module is reset
0	AUTOIDLE	R/W	0h	Internal OCP clock gating strategy Reset Source: mod_g_arstn 1 AUTOIDLE_Value_1 Automatic OCP clock gating strategy is applied, based on the OCP interface activity

4.23.44 UART_SYSS Registers

4.23.44.1 SYSS Register (Offset = 58h) [reset = 0h]

Short Description:

Long Description:

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Table 4-3058. Instance Table

Instance Name	Physical Address
UART0	5230 0058h
UART1	5230 1058h
UART2	5230 2058h
UART3	5230 3058h
UART4	5230 4058h
UART5	5230 5058h

Figure 4-1435. UART_SYSS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RESERVED							RESET DONE
R								R							R
0h								0h							0h

Access Types Legend

Table 4-3059. UART_SYSS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reset Source: mod_g_arstn
7:1	RESERVED	R		Reset Source: mod_g_arstn
0	RESETDONE	R	0h	Internal Reset Monitoring Reset Source: mod_g_arstn 1 RESETDONE_Value_1 Reset completed

4.23.45 UART_WER Registers

4.23.45.1 WER Register (Offset = 5Ch) [reset = ffh]

Short Description: The UART wakeup enable re

Long Description: The UART wakeup enable register is used to mask and unmask a UART event that would subsequently notify the system. The events are any activity in the logic that could cause an interrupt and/ or an activity that would require the system to wakeup. It should be noted that even if the wakeup is disabled for certain events, if these events are also an interrupt to the UART, then the UART will still register the interrupt as such.

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Table 4-3060. Instance Table

Instance Name	Physical Address
UART0	5230 005Ch
UART1	5230 105Ch
UART2	5230 205Ch
UART3	5230 305Ch
UART4	5230 405Ch
UART5	5230 505Ch

Figure 4-1436. UART_WER Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								EVENT_7_TX_WAKEUP_EN	EVENT_6_RECEIVER_LINE_STATUS_INTERRUPT	EVENT_5_RHR_INTERRUPT	EVENT_4_RX_ACTIVITY	EVENT_3_DCD_CD_ACTIVITY	EVENT_2_RI_ACTIVITY	EVENT_1_DSR_ACTIVITY	EVENT_0_CTS_ACTIVITY
R								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h								1h	1h	1h	1h	1h	1h	1h	1h

Access Types Legend

Table 4-3061. UART_WER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reset Source: mod_g_arstn
7	EVENT_7_TX_WAKEUP_EN	R/W	1h	Reset Source: mod_g_arstn 1 Event_7_TX_WAKEUP_EN EVENT CAN WAKE UP THE SYSTEM: _Value_1 Event can be: THR_IT or TX_DMA request and/or TX_SATUS_IT
6	EVENT_6_RECEIVER_LINE_STATUS_INTERRUPT	R/W	1h	Reset Source: mod_g_arstn 1 Event_6_Receiver_Lin Event can wake up the system e_Status_Interrupt_V alue_1
5	EVENT_5_RHR_INTERRUPT	R/W	1h	Reset Source: mod_g_arstn 1 Event_5_RHR_Interrup Event can wake up the system t_Value_1
4	EVENT_4_RX_ACTIVITY	R/W	1h	Reset Source: mod_g_arstn 1 Event_4_RX_Activity_ Event can wake up the system Value_1
3	EVENT_3_DCD_CD_ACTIVITY	R/W	1h	Reset Source: mod_g_arstn 1 Event_3_DCD_CD_Activ Event can wake up the system ity_Value_1

Table 4-3061. UART_WER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	EVENT_2_RI_ACTIVITY	R/W	1h	Reset Source: mod_g_arstn 1 Event_2_RI_Activity_ Event can wake up the system Value_1
1	EVENT_1_DSR_ACTIVITY	R/W	1h	Reset Source: mod_g_arstn 1 Event_1_DSR_Activity Event can wake up the system _Value_1
0	EVENT_0_CTS_ACTIVITY	R/W	1h	Reset Source: mod_g_arstn 1 Event_0_CTS_activity Event can wake up the system _Value_1

4.23.46 UART_CFPS Registers

4.23.46.1 CFPS Register (Offset = 60h) [reset = 69h]

Short Description: Since the Consumer IR wor

Long Description: Since the Consumer IR works at modulation rates of 30 56.8 KHz, the 48 MHz clock must be pre scaled before the clock can drive the IR logic. This register sets the divisor rate to give a range to accommodate the remote control requirements in BAUD multiples of 12x. The value of the CFPS at reset is 0105 decimal which equates to a 38.1 KHz output from starting conditions. The 48 MHz carrier is prescaled by the CFPS which is then divided by the 12x BAUD multiple.

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Table 4-3062. Instance Table

Instance Name	Physical Address
UART0	5230 0060h
UART1	5230 1060h
UART2	5230 2060h
UART3	5230 3060h
UART4	5230 4060h
UART5	5230 5060h

Figure 4-1437. UART_CFPS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								CFPS							
R								R/W							
0h								69h							

Access Types Legend

Table 4-3063. UART_CFPS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reset Source: mod_g_arstn
7:0	CFPS	R/W	69h	System clock frequency prescaler at [12x multiple]. Examples for CFPS values are given in the table below. Target Freq [KHz] CFPS [decimal] Actual Freq[KHz] 30 133 30.08 32.75 122 32.79 36 111 36.04 36.7 109 36.69 38* 105 38.1 40 100 40 56.8 70 57.14 * configured at reset to this value Note: CFPS = 0 is not supported. Reset Source: mod_g_arstn

4.23.47 UART_RXFIFO_LVL Registers

4.23.47.1 RXFIFO_LVL Register (Offset = 64h) [reset = 0h]

Short Description: Level of the RX FIFO

Long Description: Level of the RX FIFO

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Table 4-3064. Instance Table

Instance Name	Physical Address
UART0	5230 0064h
UART1	5230 1064h
UART2	5230 2064h
UART3	5230 3064h
UART4	5230 4064h
UART5	5230 5064h

Figure 4-1438. UART_RXFIFO_LVL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED24															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED24								RXFIFO_LVL							
R								R							
0h								0h							

Access Types Legend

Table 4-3065. UART_RXFIFO_LVL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED24	R	0h	Reset Source: mod_g_arstn
7:0	RXFIFO_LVL	R	0h	Reset Source: mod_g_arstn

4.23.48 UART_TXFIFO_LVL Registers

4.23.48.1 TXFIFO_LVL Register (Offset = 68h) [reset = 0h]

Short Description: Level of the TX FIFO

Long Description: Level of the TX FIFO

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Table 4-3066. Instance Table

Instance Name	Physical Address
UART0	5230 0068h
UART1	5230 1068h
UART2	5230 2068h
UART3	5230 3068h
UART4	5230 4068h
UART5	5230 5068h

Figure 4-1439. UART_TXFIFO_LVL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED24															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED24								TXFIFO_LVL							
R								R							
0h								0h							

Access Types Legend

Table 4-3067. UART_TXFIFO_LVL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED24	R	0h	Reset Source: mod_g_arstn
7:0	TXFIFO_LVL	R	0h	Reset Source: mod_g_arstn

4.23.49 UART_IER2 Registers

4.23.49.1 IER2 Register (Offset = 6Ch) [reset = 0h]

Short Description: Enables RX/TX FIFOs empty

Long Description: Enables RX/TX FIFOs empty corresponding interrupts.

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Table 4-3068. Instance Table

Instance Name	Physical Address
UART0	5230 006Ch
UART1	5230 106Ch
UART2	5230 206Ch
UART3	5230 306Ch
UART4	5230 406Ch
UART5	5230 506Ch

Figure 4-1440. UART_IER2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED1								RESERVED					RHR_IT_DIS	EN_TXFIFO_EMPTY	EN_RXFIFO_EMPTY
R								R					R/W	R/W	R/W
0h								0h					0h	0h	0h

Access Types Legend

Table 4-3069. UART_IER2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	Reset Source: mod_g_arstn
7:3	RESERVED	R		Reset Source: mod_g_arstn
2	RHR_IT_DIS	R/W	0h	Reset Source: mod_g_arstn 1 RHR_IT_DIS_Value_1 Disables the RHR interrupt.
1	EN_TXFIFO_EMPTY	R/W	0h	Enables[1]/DISABLES[00 EN_TXFIFO_EMPTY interrupt. Reset Source: mod_g_arstn
0	EN_RXFIFO_EMPTY	R/W	0h	Enables[1]/disables[0] EN_RXFIFO_EMPTY interrupt. Reset Source: mod_g_arstn

4.23.50 UART_ISR2 Registers

4.23.50.1 ISR2 Register (Offset = 70h) [reset = 3h]

Short Description: Status of RX/TX FIFOs em

Long Description: Status of RX/TX FIFOs empty corresponding interrupts.

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Table 4-3070. Instance Table

Instance Name	Physical Address
UART0	5230 0070h
UART1	5230 1070h
UART2	5230 2070h
UART3	5230 3070h
UART4	5230 4070h
UART5	5230 5070h

Figure 4-1441. UART_ISR2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED1								RESERVED						TXFIFO_EMPTY_STS	RXFIFO_EMPTY_STS
R								R						R/W1TC	R/W1TC
0h								0h						1h	1h

Access Types Legend

Table 4-3071. UART_ISR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	Reset Source: mod_g_arstn
7:2	RESERVED	R		Reset Source: mod_g_arstn
1	TXFIFO_EMPTY_STS	R/W1TC	1h	TXFIFO interrupt pending Reset Source: mod_g_arstn 1 TXFIFO_EMPTY_STS_Val TXFIFO_EMPTY interrupt ue_1 pending.
0	RXFIFO_EMPTY_STS	R/W1TC	1h	RXFIFO interrupt pending Reset Source: mod_g_arstn 1 RXFIFO_EMPTY_STS_Val RXFIFO_EMPTY interrupt ue_1 pending.

4.23.51 UART_FREQ_SEL Registers

4.23.51.1 FREQ_SEL Register (Offset = 74h) [reset = 1ah]

Short Description: Sample per bit value sele

Long Description: Sample per bit value selector

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Table 4-3072. Instance Table

Instance Name	Physical Address
UART0	5230 0074h
UART1	5230 1074h
UART2	5230 2074h
UART3	5230 3074h
UART4	5230 4074h
UART5	5230 5074h

Figure 4-1442. UART_FREQ_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED2															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED2								FREQ_SEL							
R								R/W							
0h								1ah							

Access Types Legend

Table 4-3073. UART_FREQ_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED2	R	0h	RESERVED Reset Source: mod_g_arstn
7:0	FREQ_SEL	R/W	1Ah	Sets the sample per bit if non default frequency is used. MDR3[1] must be set to 1 after this value is set. Must be equal or higher then 6. Reset Source: mod_g_arstn

4.23.52 UART_ABAUD_1ST_CHAR Registers

4.23.52.1 ABAUD_1ST_CHAR Register (Offset = 78h) [reset = 0h]

Short Description: Unused

Long Description: Unused

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Table 4-3074. Instance Table

Instance Name	Physical Address
UART0	5230 0078h
UART1	5230 1078h
UART2	5230 2078h
UART3	5230 3078h
UART4	5230 4078h
UART5	5230 5078h

Figure 4-1443. UART_ABAUD_1ST_CHAR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R															
0h															

Access Types Legend

Table 4-3075. UART_ABAUD_1ST_CHAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R		Reset Source: mod_g_arstn

4.23.53 UART_BAUD_2ND_CHAR Registers

4.23.53.1 BAUD_2ND_CHAR Register (Offset = 7Ch) [reset = 0h]

Short Description: Unused

Long Description: Unused

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Table 4-3076. Instance Table

Instance Name	Physical Address
UART0	5230 007Ch
UART1	5230 107Ch
UART2	5230 207Ch
UART3	5230 307Ch
UART4	5230 407Ch
UART5	5230 507Ch

Figure 4-1444. UART_BAUD_2ND_CHAR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R															
0h															

Access Types Legend

Table 4-3077. UART_BAUD_2ND_CHAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R		Reset Source: mod_g_arstn

4.23.54 UART_MDR3 Registers

4.23.54.1 MDR3 Register (Offset = 80h) [reset = 0h]

Short Description: Mode definition register

Long Description: Mode definition register 3.

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Table 4-3078. Instance Table

Instance Name	Physical Address
UART0	5230 0080h
UART1	5230 1080h
UART2	5230 2080h
UART3	5230 3080h
UART4	5230 4080h
UART5	5230 5080h

Figure 4-1445. UART_MDR3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED2															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED2								RESERVED1			DIR_EN	DIR_POL	SET_DMA_TX_THRESHOLD	NONDEFAULT_FREQ	DISABLE_CIR_RX_DEMOD
R								R			R/W	R/W	R/W	R/W	R/W
0h								0h			0h	0h	0h	0h	0h

Access Types Legend

Table 4-3079. UART_MDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED2	R	0h	Reset Source: mod_g_arstn
7:5	RESERVED1	R	0h	Reserved Reset Source: mod_g_arstn
4	DIR_EN	R/W	0h	RS-485 External Transceiver Direction Enable Reset Source: mod_g_arstn
3	DIR_POL	R/W	0h	RS-485 External Transceiver Direction Polarity. 0 => TX: RTS=0, RX: RTS=1. 1 => TX: RTS=1, RX: RTS=0 Reset Source: mod_g_arstn
2	SET_DMA_TX_THRESHOLD	R/W	0h	Enable to set different TX DMA threshold then 64-trigger [usage of new register TX_DNA_THRESHOLD] Reset Source: mod_g_arstn
1	NONDEFAULT_FREQ	R/W	0h	Enables[1]/Disables[0] using NONDEFAULT fclk frequencies Reset Source: mod_g_arstn
0	DISABLE_CIR_RX_DEMOD	R/W	0h	Disables[1]/Enables[0] CIR RX demodulation Reset Source: mod_g_arstn 1 DISABLE_CIR_RX_DEMOD Disables CIR RX demodulation _Value_1

4.23.55 UART_TX_DMA_THRESHOLD Registers

4.23.55.1 TX_DMA_THRESHOLD Register (Offset = 84h) [reset = 0h]

Short Description: Use to manually set the T

Long Description: Use to manually set the TX DMA threshold level. MDR3[2] SET_TX_DMA_THRESHOLD must be one and must be value + tx_trigger_level <= 64 (TX FIFO size). If not, 64-tx_trigger_level will be used w/o modifying the value of this register.

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Table 4-3080. Instance Table

Instance Name	Physical Address
UART0	5230 0084h
UART1	5230 1084h
UART2	5230 2084h
UART3	5230 3084h
UART4	5230 4084h
UART5	5230 5084h

Figure 4-1446. UART_TX_DMA_THRESHOLD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED1								RESERVED		TX_DMA_THRESHOLD					
R								R		R/W					
0h								0h		0h					

Access Types Legend

Table 4-3081. UART_TX_DMA_THRESHOLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	RESERVED Reset Source: mod_g_arstn
7:6	RESERVED	R		Reserved Reset Source: mod_g_arstn
5:0	TX_DMA_THRESHOLD	R/W	0h	Use to manually set the TX DMA threshold level. Reset Source: mod_g_arstn

4.23.56 UART_MDR4 Registers

4.23.56.1 MDR4 Register (Offset = 88h) [reset = 0h]

Short Description: Mode definition register

Long Description: Mode definition register 4

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Table 4-3082. Instance Table

Instance Name	Physical Address
UART0	5230 0088h
UART1	5230 1088h
UART2	5230 2088h
UART3	5230 3088h
UART4	5230 4088h
UART5	5230 5088h

Figure 4-1447. UART_MDR4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED1								RESERVED	MODE9	FREQ_SEL_H			MODE		
R								R	R/W	R/W			R/W		
0h								0h	0h	0h			0h		

Access Types Legend

Table 4-3083. UART_MDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	Reset Source: mod_g_arstn
7	RESERVED	R		Reset Source: mod_g_arstn
6	MODE9	R/W	0h	9-bit character length. When '1', overrides character length setting in LCR Reset Source: mod_g_arstn
5:3	FREQ_SEL_H	R/W	0h	Upper 3 bits of FREQ_SEL register for higher division values, as required for example for FI/Di in ISO7816 mode Reset Source: mod_g_arstn
2:0	MODE	R/W	0h	New modes [when set, overrides MDR1 modes] Reset Source: mod_g_arstn 7 Reserved2 reserved 6 Reserved1 reserved 5 ISO7816_1 ISO 7816 mode T=1 4 ISO7816_0 ISO 7816 mode T=0 3 Synch_gen Synchronous mode with generated clock 2 Synch_ext Synchronous mode with external clock 1 Reserved reserved

4.23.57 UART_EFR2 Registers

4.23.57.1 EFR2 Register (Offset = 8Ch) [reset = 0h]

Short Description: Enhanced Features Registe

Long Description: Enhanced Features Register 2

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Table 4-3084. Instance Table

Instance Name	Physical Address
UART0	5230 008Ch
UART1	5230 108Ch
UART2	5230 208Ch
UART3	5230 308Ch
UART4	5230 408Ch
UART5	5230 508Ch

Figure 4-1448. UART_EFR2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED1								BROADCAST	TIMEOUT_BEHAVE	C8	C4	C2	MULTIDROP	RHR_OVERRUN	ENDIAN
R								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-3085. UART_EFR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	Reset Source: mod_g_arstn
7	BROADCAST	R/W	0h	Enables broadcast address matching in multi-drop address match mode Reset Source: mod_g_arstn
6	TIMEOUT_BEHAVE	R/W	0h	Specifies how timeout is measured Reset Source: mod_g_arstn 1 _1 periodic timeout even when no character has been received
5	C8	R/W	0h	Value for ISO 7816 C8 pin for software control Reset Source: mod_g_arstn
4	C4	R/W	0h	Value for ISO 7816 C4 pin for software control Reset Source: mod_g_arstn
3	C2	R/W	0h	Value for ISO 7816 reset pin [software controllable] Reset Source: mod_g_arstn
2	MULTIDROP	R/W	0h	Enables parity Multi-drop mode [overrides LCR[5..3]] when '1' Reset Source: mod_g_arstn
1	RHR_OVERRUN	R/W	0h	RHR Overrun behaviour when buffer full Reset Source: mod_g_arstn 1 Atmel data in RHR is overwritten when buffer full (and FIFO disabled)
0	ENDIAN	R/W	0h	Endianness Reset Source: mod_g_arstn 1 Big_Endian Big Endian (MSB First)

4.23.58 UART_ECR Registers

4.23.58.1 ECR Register (Offset = 90h) [reset = 18h]

Short Description: Enhanced Control register

Long Description: Enhanced Control register

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Table 4-3086. Instance Table

Instance Name	Physical Address
UART0	5230 0090h
UART1	5230 1090h
UART2	5230 2090h
UART3	5230 3090h
UART4	5230 4090h
UART5	5230 5090h

Figure 4-1449. UART_ECR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED1								RESERVED		CLEAR_TX_PE	TX_EN	RX_EN	TX_RST	RX_RST	A_MULTIDROP
R								R		W	R/W	R/W	W	W	W
0h								0h		0h	1h	1h	0h	0h	0h

Access Types Legend

Table 4-3087. UART_ECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	Reset Source: mod_g_arstn
7:6	RESERVED	R		Reset Source: mod_g_arstn
5	CLEAR_TX_PE	W	0h	Write 1 to clear parity error from the Transmitter to allow it to continue to try sending data [ISO7816 transmit only] Reset Source: mod_g_arstn
4	TX_EN	R/W	1h	Enables/Disables the transmitter Reset Source: mod_g_arstn 1 Enabled Transmitter is working
3	RX_EN	R/W	1h	Enables/Disables the receiver Reset Source: mod_g_arstn 1 Enabled Receiver is operating
2	TX_RST	W	0h	Writing '1' resets the transmitter Reset Source: mod_g_arstn
1	RX_RST	W	0h	Writing '1' resets the receiver Reset Source: mod_g_arstn
0	A_MULTIDROP	W	0h	In multi-drop mode, when written with the value '1' causes the next byte written into THR to be transmitted with the parity bit set, signaling an address Reset Source: mod_g_arstn

4.23.59 UART_TIMEGUARD Registers

4.23.59.1 TIMEGUARD Register (Offset = 94h) [reset = 0h]

Short Description: Timeguard

Long Description: Timeguard

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Table 4-3088. Instance Table

Instance Name	Physical Address
UART0	5230 0094h
UART1	5230 1094h
UART2	5230 2094h
UART3	5230 3094h
UART4	5230 4094h
UART5	5230 5094h

Figure 4-1450. UART_TIMEGUARD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TIMEGUARD							
R								R/W							
0h								0h							

Access Types Legend

Table 4-3089. UART_TIMEGUARD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R		Reset Source: mod_g_arstn
7:0	TIMEGUARD	R/W	0h	Specifies the amount of idle baud clocks [transmitter bit period] to insert between transmitted bytes, useful when comunicating with slower devices Reset Source: mod_g_arstn

4.23.60 UART_TIMEOUTL Registers

4.23.60.1 TIMEOUTL Register (Offset = 98h) [reset = 0h]

Short Description: Timeout lower byte

Long Description: Timeout lower byte

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Table 4-3090. Instance Table

Instance Name	Physical Address
UART0	5230 0098h
UART1	5230 1098h
UART2	5230 2098h
UART3	5230 3098h
UART4	5230 4098h
UART5	5230 5098h

Figure 4-1451. UART_TIMEOUTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TIMEOUT_L							
R								R/W							
0h								0h							

Access Types Legend

Table 4-3091. UART_TIMEOUTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R		Reset Source: mod_g_arstn
7:0	TIMEOUT_L	R/W	0h	Custom timeout period in baud clocks, to override the internal value, when different from 0. [Lower byte of the 16 bit value] Reset Source: mod_g_arstn

4.23.61 UART_TIMEOUTH Registers

4.23.61.1 TIMEOUTH Register (Offset = 9Ch) [reset = 0h]

Short Description: Timeout higher byte

Long Description: Timeout higher byte

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Table 4-3092. Instance Table

Instance Name	Physical Address
UART0	5230 009Ch
UART1	5230 109Ch
UART2	5230 209Ch
UART3	5230 309Ch
UART4	5230 409Ch
UART5	5230 509Ch

Figure 4-1452. UART_TIMEOUTH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TIMEOUT_H							
R								R/W							
0h								0h							

Access Types Legend

Table 4-3093. UART_TIMEOUTH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R		Reset Source: mod_g_arstn
7:0	TIMEOUT_H	R/W	0h	Custom timeout period in baud clocks, to override the internal value, when different from 0. [Higher byte of the 16 bit value] Reset Source: mod_g_arstn

4.23.62 UART_SCCR Registers

4.23.62.1 SCCR Register (Offset = A0h) [reset = 7h]

Short Description: Smartcard (ISO7816) mode

Long Description: Smartcard (ISO7816) mode Control Register

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Table 4-3094. Instance Table

Instance Name	Physical Address
UART0	5230 00A0h
UART1	5230 10A0h
UART2	5230 20A0h
UART3	5230 30A0h
UART4	5230 40A0h
UART5	5230 50A0h

Figure 4-1453. UART_SCCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED1								DSNACK	INACK	RESERVED			MAX_ITERATION		
R								R/W	R/W	R			R/W		
0h								0h	0h	0h			7h		

Access Types Legend

Table 4-3095. UART_SCCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	Reset Source: mod_g_arstn
7	DSNACK	R/W	0h	Applies Max_Iteration to receiver aswell - when maximum number of NACKs have been returned, the receiver will accept the data regardless of error. The data will be loaded into the receiver FIFO and PE will be set when reading it. Reset Source: mod_g_arstn
6	INACK	R/W	0h	Inhibit NACK when receiving, even if an error is received. The data will be loaded into the receiver FIFO and PE will be set when reading it. Reset Source: mod_g_arstn
5:3	RESERVED	R		Reset Source: mod_g_arstn
2:0	MAX_ITERATION	R/W	7h	Number of times to repeat transmitted character, if the receiver did not acknowledge. If not acknowledged after the max value is reached, the USART transmitter will set parity error, stop and not continue until it is cleared. Reset Source: mod_g_arstn

4.23.63 UART_ERHR Registers

4.23.63.1 ERHR Register (Offset = A4h) [reset = 0h]

Short Description: Extended Receive Holding

Long Description: Extended Receive Holding Register

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Table 4-3096. Instance Table

Instance Name	Physical Address
UART0	5230 00A4h
UART1	5230 10A4h
UART2	5230 20A4h
UART3	5230 30A4h
UART4	5230 40A4h
UART5	5230 50A4h

Figure 4-1454. UART_ERHR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							ERHR								
R							R								
0h							0h								

Access Types Legend

Table 4-3097. UART_ERHR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	R		Reset Source: mod_g_arstn
8:0	ERHR	R	0h	Extended Receive Holding Register - allows accessing the full 9bit RHR Reset Source: mod_g_arstn

4.23.64 UART_ETHR Registers

4.23.64.1 ETHR Register (Offset = A4h) [reset = 0h]

Short Description: Extended Transmit Holding

Long Description: Extended Transmit Holding Register

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Table 4-3098. Instance Table

Instance Name	Physical Address
UART0	5230 00A4h
UART1	5230 10A4h
UART2	5230 20A4h
UART3	5230 30A4h
UART4	5230 40A4h
UART5	5230 50A4h

Figure 4-1455. UART_ETHR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							ETHR								
R							W								
0h							0h								

Access Types Legend

Table 4-3099. UART_ETHR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	R		Reset Source: mod_g_arstn
8:0	ETHR	W	0h	Extended Transmit Holding Register - allows writing the full 9bit RHR Reset Source: mod_g_arstn

4.23.65 UART_MAR Registers

4.23.65.1 MAR Register (Offset = A8h) [reset = 0h]

Short Description: Multidrop Address Registe

Long Description: Multidrop Address Register

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Table 4-3100. Instance Table

Instance Name	Physical Address
UART0	5230 00A8h
UART1	5230 10A8h
UART2	5230 20A8h
UART3	5230 30A8h
UART4	5230 40A8h
UART5	5230 50A8h

Figure 4-1456. UART_MAR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								ADDRESS							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-3101. UART_MAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	ADDRESS	R/W	0h	Multidrop match address value Reset Source: mod_g_arstn

4.23.66 UART_MMR Registers

4.23.66.1 MMR Register (Offset = ACh) [reset = 0h]

Short Description: Multidrop Mask Register

Long Description: Multidrop Mask Register

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Table 4-3102. Instance Table

Instance Name	Physical Address
UART0	5230 00ACh
UART1	5230 10ACh
UART2	5230 20ACh
UART3	5230 30ACh
UART4	5230 40ACh
UART5	5230 50ACh

Figure 4-1457. UART_MMR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MASK							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-3103. UART_MMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	MASK	R/W	0h	Address match masking value ? writing a 0 to a bit means that the corresponding address bit will be ignored in matching Reset Source: mod_g_arstn

4.23.67 UART_MBR Registers

4.23.67.1 MBR Register (Offset = B0h) [reset = 0h]

Short Description: Multidrop Broadcast Addre

Long Description: Multidrop Broadcast Address Register

Return to Summary Table

Table 4-3104. Instance Table

Instance Name	Physical Address
UART0	5230 00B0h
UART1	5230 10B0h
UART2	5230 20B0h
UART3	5230 30B0h
UART4	5230 40B0h
UART5	5230 50B0h

Figure 4-1458. UART_MBR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								BROADCAST_ADDRESS							
NONE								R/W							
0								0h							

Access Types Legend

Table 4-3105. UART_MBR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE		Reserved
7:0	BROADCAST_ADDRESS	R/W	0h	Broadcast address for address matching Reset Source: mod_g_arstn

4.23.68 Access Table

Table 4-3106. Access Type Codes

Access Type	Code	Description
R/W	R/W	Read / Write
R	R	Read
W	W	Write
R/W1TS	R/W1TS	Read/Write 1 To Set
R/W1TC	R/W1TC	Read/Write 1 To Clear

4.24 MSS_VIM Registers

Table 4-3107. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9

Offset	Length	Register Name	Description	VIM Physical Address
0h	32	MSS_VIM_PID	The Revision Register contains the major and minor revisions for the module.	50F0 0000h
4h	32	MSS_VIM_INFO	The Info Register gives the configuration Inforrmation of this VIM.	50F0 0004h
8h	32	MSS_VIM_PRIIRQ	The Prioritized IRQ Register shows the number of the highest priority pending IRQ.	50F0 0008h
Ch	32	MSS_VIM_PRIFIQ	The Prioritized FIQ Register shows the number of the highest priority pending FIQ.	50F0 000Ch
10h	32	MSS_VIM_IRQGSTS	The IRQ Group Status Register indicates which groups have pending IRQ interrupts.	50F0 0010h
14h	32	MSS_VIM_FIQGSTS	The FIQ Group Status Register indicates which groups have pending FIQ interrupts.	50F0 0014h
18h	32	MSS_VIM_IRQVEC	The IRQ Vector Address Register contains the 32-bit address of the interrupt vector for the current pendind IRQ.	50F0 0018h
1Ch	32	MSS_VIM_FIQVEC	The FIQ Vector Address Register contains the 32-bit address of the interrupt vector for the current pendind FIQ.	50F0 001Ch
20h	32	MSS_VIM_ACTIRQ	The Active IRQ Register shows the number of the currently active IRQ.	50F0 0020h
24h	32	MSS_VIM_ACTFIQ	The Active FIQ Register shows the number of the currently active FIQ.	50F0 0024h
28h	32	MSS_VIM_IRQPRIMSK	The IRQ Priority Mask Register allows all IRQs of a particular priority to be enabled or disabled.	50F0 0028h
2Ch	32	MSS_VIM_FIQPRIMSK	The FIQ Priority Mask Register allows all FIQs of a particular priority to be enabled or disabled.	50F0 002Ch
30h	32	MSS_VIM_DEDVEC	The DED Vector Address contains a default vector address for when an uncorrectable error is detected for an active IRQ or FIQ.	50F0 0030h
400h	32	MSS_VIM_RAW	Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00	50F0 0400h
404h	32	MSS_VIM_STS	Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04	50F0 0404h
408h	32	MSS_VIM_INTR_EN_SET	Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08	50F0 0408h
40Ch	32	MSS_VIM_INTER_EN_CLR	Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C	50F0 040Ch

Table 4-3107. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Register Name	Description	VIM Physical Address
410h	32	MSS_VIM_IRQSTS	Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10	50F0 0410h
414h	32	MSS_VIM_FIQSTS	Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14	50F0 0414h
418h	32	MSS_VIM_INTMAP	Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18	50F0 0418h
41Ch	32	MSS_VIM_INTTYPE	Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C	50F0 041Ch
420h	32	MSS_VIM_RAW_1	Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00	50F0 0420h
424h	32	MSS_VIM_STS_1	Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04	50F0 0424h
428h	32	MSS_VIM_INTR_EN_SET_1	Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08	50F0 0428h
42Ch	32	MSS_VIM_INTER_EN_CLR_1	Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C	50F0 042Ch
430h	32	MSS_VIM_IRQSTS_1	Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10	50F0 0430h
434h	32	MSS_VIM_FIQSTS_1	Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14	50F0 0434h
438h	32	MSS_VIM_INTMAP_1	Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18	50F0 0438h
43Ch	32	MSS_VIM_INTTYPE_1	Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C	50F0 043Ch
440h	32	MSS_VIM_RAW_2	Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00	50F0 0440h
444h	32	MSS_VIM_STS_2	Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04	50F0 0444h
448h	32	MSS_VIM_INTR_EN_SET_2	Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08	50F0 0448h
44Ch	32	MSS_VIM_INTER_EN_CLR_2	Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C	50F0 044Ch
450h	32	MSS_VIM_IRQSTS_2	Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10	50F0 0450h
454h	32	MSS_VIM_FIQSTS_2	Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14	50F0 0454h
458h	32	MSS_VIM_INTMAP_2	Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18	50F0 0458h
45Ch	32	MSS_VIM_INTTYPE_2	Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C	50F0 045Ch

Table 4-3107. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Register Name	Description	VIM Physical Address
460h	32	MSS_VIM_RAW_3	Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00	50F0 0460h
464h	32	MSS_VIM_STS_3	Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04	50F0 0464h
468h	32	MSS_VIM_INTR_EN_SET_3	Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08	50F0 0468h
46Ch	32	MSS_VIM_INTER_EN_CLR_3	Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C	50F0 046Ch
470h	32	MSS_VIM_IRQSTS_3	Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10	50F0 0470h
474h	32	MSS_VIM_FIQSTS_3	Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14	50F0 0474h
478h	32	MSS_VIM_INTMAP_3	Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18	50F0 0478h
47Ch	32	MSS_VIM_INTTYPE_3	Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C	50F0 047Ch
480h	32	MSS_VIM_RAW_4	Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00	50F0 0480h
484h	32	MSS_VIM_STS_4	Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04	50F0 0484h
488h	32	MSS_VIM_INTR_EN_SET_4	Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08	50F0 0488h
48Ch	32	MSS_VIM_INTER_EN_CLR_4	Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C	50F0 048Ch
490h	32	MSS_VIM_IRQSTS_4	Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10	50F0 0490h
494h	32	MSS_VIM_FIQSTS_4	Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14	50F0 0494h
498h	32	MSS_VIM_INTMAP_4	Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18	50F0 0498h
49Ch	32	MSS_VIM_INTTYPE_4	Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C	50F0 049Ch
4A0h	32	MSS_VIM_RAW_5	Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00	50F0 04A0h
4A4h	32	MSS_VIM_STS_5	Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04	50F0 04A4h
4A8h	32	MSS_VIM_INTR_EN_SET_5	Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08	50F0 04A8h
4ACh	32	MSS_VIM_INTER_EN_CLR_5	Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C	50F0 04ACh

Table 4-3107. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Register Name	Description	VIM Physical Address
4B0h	32	MSS_VIM_IRQSTS_5	Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10	50F0 04B0h
4B4h	32	MSS_VIM_FIQSTS_5	Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14	50F0 04B4h
4B8h	32	MSS_VIM_INTMAP_5	Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18	50F0 04B8h
4BCh	32	MSS_VIM_INTTYPE_5	Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C	50F0 04BCh
4C0h	32	MSS_VIM_RAW_6	Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00	50F0 04C0h
4C4h	32	MSS_VIM_STS_6	Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04	50F0 04C4h
4C8h	32	MSS_VIM_INTR_EN_SET_6	Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08	50F0 04C8h
4CCh	32	MSS_VIM_INTER_EN_CLR_6	Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C	50F0 04CCh
4D0h	32	MSS_VIM_IRQSTS_6	Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10	50F0 04D0h
4D4h	32	MSS_VIM_FIQSTS_6	Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14	50F0 04D4h
4D8h	32	MSS_VIM_INTMAP_6	Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18	50F0 04D8h
4DCh	32	MSS_VIM_INTTYPE_6	Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C	50F0 04DCh
4E0h	32	MSS_VIM_RAW_7	Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00	50F0 04E0h
4E4h	32	MSS_VIM_STS_7	Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04	50F0 04E4h
4E8h	32	MSS_VIM_INTR_EN_SET_7	Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08	50F0 04E8h
4ECh	32	MSS_VIM_INTER_EN_CLR_7	Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C	50F0 04ECh
4F0h	32	MSS_VIM_IRQSTS_7	Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10	50F0 04F0h
4F4h	32	MSS_VIM_FIQSTS_7	Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14	50F0 04F4h
4F8h	32	MSS_VIM_INTMAP_7	Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18	50F0 04F8h
4FCh	32	MSS_VIM_INTTYPE_7	Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C	50F0 04FCh

Table 4-3107. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Register Name	Description	VIM Physical Address
1000h	32	MSS_VIM_INTPRIORITY	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h4	50F0 1000h
1004h	32	MSS_VIM_INTPRIORITY_1	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h5	50F0 1004h
1008h	32	MSS_VIM_INTPRIORITY_2	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h6	50F0 1008h
100Ch	32	MSS_VIM_INTPRIORITY_3	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h7	50F0 100Ch
1010h	32	MSS_VIM_INTPRIORITY_4	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h8	50F0 1010h
1014h	32	MSS_VIM_INTPRIORITY_5	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h9	50F0 1014h
1018h	32	MSS_VIM_INTPRIORITY_6	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h10	50F0 1018h
101Ch	32	MSS_VIM_INTPRIORITY_7	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h11	50F0 101Ch
1020h	32	MSS_VIM_INTPRIORITY_8	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h12	50F0 1020h
1024h	32	MSS_VIM_INTPRIORITY_9	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h13	50F0 1024h
1028h	32	MSS_VIM_INTPRIORITY_10	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h14	50F0 1028h
102Ch	32	MSS_VIM_INTPRIORITY_11	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h15	50F0 102Ch
1030h	32	MSS_VIM_INTPRIORITY_12	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h16	50F0 1030h
1034h	32	MSS_VIM_INTPRIORITY_13	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h17	50F0 1034h
1038h	32	MSS_VIM_INTPRIORITY_14	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h18	50F0 1038h
103Ch	32	MSS_VIM_INTPRIORITY_15	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h19	50F0 103Ch
1040h	32	MSS_VIM_INTPRIORITY_16	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h20	50F0 1040h
1044h	32	MSS_VIM_INTPRIORITY_17	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h21	50F0 1044h
1048h	32	MSS_VIM_INTPRIORITY_18	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h22	50F0 1048h

Table 4-3107. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Register Name	Description	VIM Physical Address
104Ch	32	MSS_VIM_INTPRIORITY_19	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h23	50F0 104Ch
1050h	32	MSS_VIM_INTPRIORITY_20	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h24	50F0 1050h
1054h	32	MSS_VIM_INTPRIORITY_21	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h25	50F0 1054h
1058h	32	MSS_VIM_INTPRIORITY_22	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h26	50F0 1058h
105Ch	32	MSS_VIM_INTPRIORITY_23	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h27	50F0 105Ch
1060h	32	MSS_VIM_INTPRIORITY_24	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h28	50F0 1060h
1064h	32	MSS_VIM_INTPRIORITY_25	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h29	50F0 1064h
1068h	32	MSS_VIM_INTPRIORITY_26	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h30	50F0 1068h
106Ch	32	MSS_VIM_INTPRIORITY_27	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h31	50F0 106Ch
1070h	32	MSS_VIM_INTPRIORITY_28	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h32	50F0 1070h
1074h	32	MSS_VIM_INTPRIORITY_29	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h33	50F0 1074h
1078h	32	MSS_VIM_INTPRIORITY_30	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h34	50F0 1078h
107Ch	32	MSS_VIM_INTPRIORITY_31	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h35	50F0 107Ch
1080h	32	MSS_VIM_INTPRIORITY_32	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h36	50F0 1080h
1084h	32	MSS_VIM_INTPRIORITY_33	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h37	50F0 1084h
1088h	32	MSS_VIM_INTPRIORITY_34	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h38	50F0 1088h
108Ch	32	MSS_VIM_INTPRIORITY_35	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h39	50F0 108Ch
1090h	32	MSS_VIM_INTPRIORITY_36	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h40	50F0 1090h
1094h	32	MSS_VIM_INTPRIORITY_37	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h41	50F0 1094h

Table 4-3107. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Register Name	Description	VIM Physical Address
1098h	32	MSS_VIM_INTPRIORITY_38	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h42	50F0 1098h
109Ch	32	MSS_VIM_INTPRIORITY_39	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h43	50F0 109Ch
10A0h	32	MSS_VIM_INTPRIORITY_40	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h44	50F0 10A0h
10A4h	32	MSS_VIM_INTPRIORITY_41	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h45	50F0 10A4h
10A8h	32	MSS_VIM_INTPRIORITY_42	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h46	50F0 10A8h
10ACh	32	MSS_VIM_INTPRIORITY_43	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h47	50F0 10ACh
10B0h	32	MSS_VIM_INTPRIORITY_44	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h48	50F0 10B0h
10B4h	32	MSS_VIM_INTPRIORITY_45	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h49	50F0 10B4h
10B8h	32	MSS_VIM_INTPRIORITY_46	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h50	50F0 10B8h
10BCh	32	MSS_VIM_INTPRIORITY_47	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h51	50F0 10BCh
10C0h	32	MSS_VIM_INTPRIORITY_48	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h52	50F0 10C0h
10C4h	32	MSS_VIM_INTPRIORITY_49	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h53	50F0 10C4h
10C8h	32	MSS_VIM_INTPRIORITY_50	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h54	50F0 10C8h
10CCh	32	MSS_VIM_INTPRIORITY_51	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h55	50F0 10CCh
10D0h	32	MSS_VIM_INTPRIORITY_52	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h56	50F0 10D0h
10D4h	32	MSS_VIM_INTPRIORITY_53	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h57	50F0 10D4h
10D8h	32	MSS_VIM_INTPRIORITY_54	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h58	50F0 10D8h
10DCh	32	MSS_VIM_INTPRIORITY_55	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h59	50F0 10DCh
10E0h	32	MSS_VIM_INTPRIORITY_56	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h60	50F0 10E0h

Table 4-3107. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Register Name	Description	VIM Physical Address
10E4h	32	MSS_VIM_INTPRIORITY_57	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h61	50F0 10E4h
10E8h	32	MSS_VIM_INTPRIORITY_58	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h62	50F0 10E8h
10ECh	32	MSS_VIM_INTPRIORITY_59	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h63	50F0 10ECh
10F0h	32	MSS_VIM_INTPRIORITY_60	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h64	50F0 10F0h
10F4h	32	MSS_VIM_INTPRIORITY_61	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h65	50F0 10F4h
10F8h	32	MSS_VIM_INTPRIORITY_62	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h66	50F0 10F8h
10FCh	32	MSS_VIM_INTPRIORITY_63	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h67	50F0 10FCh
1100h	32	MSS_VIM_INTPRIORITY_64	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h68	50F0 1100h
1104h	32	MSS_VIM_INTPRIORITY_65	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h69	50F0 1104h
1108h	32	MSS_VIM_INTPRIORITY_66	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h70	50F0 1108h
110Ch	32	MSS_VIM_INTPRIORITY_67	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h71	50F0 110Ch
1110h	32	MSS_VIM_INTPRIORITY_68	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h72	50F0 1110h
1114h	32	MSS_VIM_INTPRIORITY_69	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h73	50F0 1114h
1118h	32	MSS_VIM_INTPRIORITY_70	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h74	50F0 1118h
111Ch	32	MSS_VIM_INTPRIORITY_71	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h75	50F0 111Ch
1120h	32	MSS_VIM_INTPRIORITY_72	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h76	50F0 1120h
1124h	32	MSS_VIM_INTPRIORITY_73	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h77	50F0 1124h
1128h	32	MSS_VIM_INTPRIORITY_74	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h78	50F0 1128h
112Ch	32	MSS_VIM_INTPRIORITY_75	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h79	50F0 112Ch

Table 4-3107. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Register Name	Description	VIM Physical Address
1130h	32	MSS_VIM_INTPRIORITY_76	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h80	50F0 1130h
1134h	32	MSS_VIM_INTPRIORITY_77	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h81	50F0 1134h
1138h	32	MSS_VIM_INTPRIORITY_78	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h82	50F0 1138h
113Ch	32	MSS_VIM_INTPRIORITY_79	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h83	50F0 113Ch
1140h	32	MSS_VIM_INTPRIORITY_80	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h84	50F0 1140h
1144h	32	MSS_VIM_INTPRIORITY_81	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h85	50F0 1144h
1148h	32	MSS_VIM_INTPRIORITY_82	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h86	50F0 1148h
114Ch	32	MSS_VIM_INTPRIORITY_83	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h87	50F0 114Ch
1150h	32	MSS_VIM_INTPRIORITY_84	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h88	50F0 1150h
1154h	32	MSS_VIM_INTPRIORITY_85	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h89	50F0 1154h
1158h	32	MSS_VIM_INTPRIORITY_86	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h90	50F0 1158h
115Ch	32	MSS_VIM_INTPRIORITY_87	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h91	50F0 115Ch
1160h	32	MSS_VIM_INTPRIORITY_88	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h92	50F0 1160h
1164h	32	MSS_VIM_INTPRIORITY_89	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h93	50F0 1164h
1168h	32	MSS_VIM_INTPRIORITY_90	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h94	50F0 1168h
116Ch	32	MSS_VIM_INTPRIORITY_91	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h95	50F0 116Ch
1170h	32	MSS_VIM_INTPRIORITY_92	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h96	50F0 1170h
1174h	32	MSS_VIM_INTPRIORITY_93	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h97	50F0 1174h
1178h	32	MSS_VIM_INTPRIORITY_94	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h98	50F0 1178h

Table 4-3107. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Register Name	Description	VIM Physical Address
117Ch	32	MSS_VIM_INTPRIORITY_95	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h99	50F0 117Ch
1180h	32	MSS_VIM_INTPRIORITY_96	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h100	50F0 1180h
1184h	32	MSS_VIM_INTPRIORITY_97	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h101	50F0 1184h
1188h	32	MSS_VIM_INTPRIORITY_98	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h102	50F0 1188h
118Ch	32	MSS_VIM_INTPRIORITY_99	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h103	50F0 118Ch
1190h	32	MSS_VIM_INTPRIORITY_100	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h104	50F0 1190h
1194h	32	MSS_VIM_INTPRIORITY_101	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h105	50F0 1194h
1198h	32	MSS_VIM_INTPRIORITY_102	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h106	50F0 1198h
119Ch	32	MSS_VIM_INTPRIORITY_103	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h107	50F0 119Ch
11A0h	32	MSS_VIM_INTPRIORITY_104	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h108	50F0 11A0h
11A4h	32	MSS_VIM_INTPRIORITY_105	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h109	50F0 11A4h
11A8h	32	MSS_VIM_INTPRIORITY_106	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h110	50F0 11A8h
11ACh	32	MSS_VIM_INTPRIORITY_107	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h111	50F0 11ACh
11B0h	32	MSS_VIM_INTPRIORITY_108	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h112	50F0 11B0h
11B4h	32	MSS_VIM_INTPRIORITY_109	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h113	50F0 11B4h
11B8h	32	MSS_VIM_INTPRIORITY_110	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h114	50F0 11B8h
11BCh	32	MSS_VIM_INTPRIORITY_111	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h115	50F0 11BCh
11C0h	32	MSS_VIM_INTPRIORITY_112	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h116	50F0 11C0h
11C4h	32	MSS_VIM_INTPRIORITY_113	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h117	50F0 11C4h

Table 4-3107. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Register Name	Description	VIM Physical Address
11C8h	32	MSS_VIM_INTPRIORITY_114	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h118	50F0 11C8h
11CCh	32	MSS_VIM_INTPRIORITY_115	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h119	50F0 11CCh
11D0h	32	MSS_VIM_INTPRIORITY_116	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h120	50F0 11D0h
11D4h	32	MSS_VIM_INTPRIORITY_117	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h121	50F0 11D4h
11D8h	32	MSS_VIM_INTPRIORITY_118	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h122	50F0 11D8h
11DCh	32	MSS_VIM_INTPRIORITY_119	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h123	50F0 11DCh
11E0h	32	MSS_VIM_INTPRIORITY_120	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h124	50F0 11E0h
11E4h	32	MSS_VIM_INTPRIORITY_121	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h125	50F0 11E4h
11E8h	32	MSS_VIM_INTPRIORITY_122	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h126	50F0 11E8h
11ECh	32	MSS_VIM_INTPRIORITY_123	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h127	50F0 11ECh
11F0h	32	MSS_VIM_INTPRIORITY_124	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h128	50F0 11F0h
11F4h	32	MSS_VIM_INTPRIORITY_125	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h129	50F0 11F4h
11F8h	32	MSS_VIM_INTPRIORITY_126	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h130	50F0 11F8h
11FCh	32	MSS_VIM_INTPRIORITY_127	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h131	50F0 11FCh
1200h	32	MSS_VIM_INTPRIORITY_128	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h132	50F0 1200h
1204h	32	MSS_VIM_INTPRIORITY_129	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h133	50F0 1204h
1208h	32	MSS_VIM_INTPRIORITY_130	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h134	50F0 1208h
120Ch	32	MSS_VIM_INTPRIORITY_131	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h135	50F0 120Ch
1210h	32	MSS_VIM_INTPRIORITY_132	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h136	50F0 1210h

Table 4-3107. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Register Name	Description	VIM Physical Address
1214h	32	MSS_VIM_INTPRIORITY_133	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h137	50F0 1214h
1218h	32	MSS_VIM_INTPRIORITY_134	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h138	50F0 1218h
121Ch	32	MSS_VIM_INTPRIORITY_135	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h139	50F0 121Ch
1220h	32	MSS_VIM_INTPRIORITY_136	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h140	50F0 1220h
1224h	32	MSS_VIM_INTPRIORITY_137	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h141	50F0 1224h
1228h	32	MSS_VIM_INTPRIORITY_138	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h142	50F0 1228h
122Ch	32	MSS_VIM_INTPRIORITY_139	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h143	50F0 122Ch
1230h	32	MSS_VIM_INTPRIORITY_140	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h144	50F0 1230h
1234h	32	MSS_VIM_INTPRIORITY_141	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h145	50F0 1234h
1238h	32	MSS_VIM_INTPRIORITY_142	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h146	50F0 1238h
123Ch	32	MSS_VIM_INTPRIORITY_143	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h147	50F0 123Ch
1240h	32	MSS_VIM_INTPRIORITY_144	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h148	50F0 1240h
1244h	32	MSS_VIM_INTPRIORITY_145	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h149	50F0 1244h
1248h	32	MSS_VIM_INTPRIORITY_146	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h150	50F0 1248h
124Ch	32	MSS_VIM_INTPRIORITY_147	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h151	50F0 124Ch
1250h	32	MSS_VIM_INTPRIORITY_148	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h152	50F0 1250h
1254h	32	MSS_VIM_INTPRIORITY_149	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h153	50F0 1254h
1258h	32	MSS_VIM_INTPRIORITY_150	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h154	50F0 1258h
125Ch	32	MSS_VIM_INTPRIORITY_151	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h155	50F0 125Ch

Table 4-3107. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Register Name	Description	VIM Physical Address
1260h	32	MSS_VIM_INTPRIORITY_152	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h156	50F0 1260h
1264h	32	MSS_VIM_INTPRIORITY_153	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h157	50F0 1264h
1268h	32	MSS_VIM_INTPRIORITY_154	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h158	50F0 1268h
126Ch	32	MSS_VIM_INTPRIORITY_155	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h159	50F0 126Ch
1270h	32	MSS_VIM_INTPRIORITY_156	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h160	50F0 1270h
1274h	32	MSS_VIM_INTPRIORITY_157	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h161	50F0 1274h
1278h	32	MSS_VIM_INTPRIORITY_158	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h162	50F0 1278h
127Ch	32	MSS_VIM_INTPRIORITY_159	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h163	50F0 127Ch
1280h	32	MSS_VIM_INTPRIORITY_160	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h164	50F0 1280h
1284h	32	MSS_VIM_INTPRIORITY_161	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h165	50F0 1284h
1288h	32	MSS_VIM_INTPRIORITY_162	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h166	50F0 1288h
128Ch	32	MSS_VIM_INTPRIORITY_163	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h167	50F0 128Ch
1290h	32	MSS_VIM_INTPRIORITY_164	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h168	50F0 1290h
1294h	32	MSS_VIM_INTPRIORITY_165	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h169	50F0 1294h
1298h	32	MSS_VIM_INTPRIORITY_166	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h170	50F0 1298h
129Ch	32	MSS_VIM_INTPRIORITY_167	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h171	50F0 129Ch
12A0h	32	MSS_VIM_INTPRIORITY_168	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h172	50F0 12A0h
12A4h	32	MSS_VIM_INTPRIORITY_169	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h173	50F0 12A4h
12A8h	32	MSS_VIM_INTPRIORITY_170	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h174	50F0 12A8h

Table 4-3107. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Register Name	Description	VIM Physical Address
12ACh	32	MSS_VIM_INTPRIORITY_171	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h175	50F0 12ACh
12B0h	32	MSS_VIM_INTPRIORITY_172	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h176	50F0 12B0h
12B4h	32	MSS_VIM_INTPRIORITY_173	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h177	50F0 12B4h
12B8h	32	MSS_VIM_INTPRIORITY_174	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h178	50F0 12B8h
12BCh	32	MSS_VIM_INTPRIORITY_175	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h179	50F0 12BCh
12C0h	32	MSS_VIM_INTPRIORITY_176	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h180	50F0 12C0h
12C4h	32	MSS_VIM_INTPRIORITY_177	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h181	50F0 12C4h
12C8h	32	MSS_VIM_INTPRIORITY_178	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h182	50F0 12C8h
12CCh	32	MSS_VIM_INTPRIORITY_179	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h183	50F0 12CCh
12D0h	32	MSS_VIM_INTPRIORITY_180	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h184	50F0 12D0h
12D4h	32	MSS_VIM_INTPRIORITY_181	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h185	50F0 12D4h
12D8h	32	MSS_VIM_INTPRIORITY_182	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h186	50F0 12D8h
12DCh	32	MSS_VIM_INTPRIORITY_183	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h187	50F0 12DCh
12E0h	32	MSS_VIM_INTPRIORITY_184	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h188	50F0 12E0h
12E4h	32	MSS_VIM_INTPRIORITY_185	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h189	50F0 12E4h
12E8h	32	MSS_VIM_INTPRIORITY_186	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h190	50F0 12E8h
12ECh	32	MSS_VIM_INTPRIORITY_187	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h191	50F0 12ECh
12F0h	32	MSS_VIM_INTPRIORITY_188	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h192	50F0 12F0h
12F4h	32	MSS_VIM_INTPRIORITY_189	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h193	50F0 12F4h

Table 4-3107. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Register Name	Description	VIM Physical Address
12F8h	32	MSS_VIM_INTPRIORITY_190	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h194	50F0 12F8h
12FCh	32	MSS_VIM_INTPRIORITY_191	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h195	50F0 12FCh
1300h	32	MSS_VIM_INTPRIORITY_192	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h196	50F0 1300h
1304h	32	MSS_VIM_INTPRIORITY_193	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h197	50F0 1304h
1308h	32	MSS_VIM_INTPRIORITY_194	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h198	50F0 1308h
130Ch	32	MSS_VIM_INTPRIORITY_195	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h199	50F0 130Ch
1310h	32	MSS_VIM_INTPRIORITY_196	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h200	50F0 1310h
1314h	32	MSS_VIM_INTPRIORITY_197	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h201	50F0 1314h
1318h	32	MSS_VIM_INTPRIORITY_198	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h202	50F0 1318h
131Ch	32	MSS_VIM_INTPRIORITY_199	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h203	50F0 131Ch
1320h	32	MSS_VIM_INTPRIORITY_200	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h204	50F0 1320h
1324h	32	MSS_VIM_INTPRIORITY_201	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h205	50F0 1324h
1328h	32	MSS_VIM_INTPRIORITY_202	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h206	50F0 1328h
132Ch	32	MSS_VIM_INTPRIORITY_203	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h207	50F0 132Ch
1330h	32	MSS_VIM_INTPRIORITY_204	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h208	50F0 1330h
1334h	32	MSS_VIM_INTPRIORITY_205	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h209	50F0 1334h
1338h	32	MSS_VIM_INTPRIORITY_206	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h210	50F0 1338h
133Ch	32	MSS_VIM_INTPRIORITY_207	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h211	50F0 133Ch
1340h	32	MSS_VIM_INTPRIORITY_208	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h212	50F0 1340h

Table 4-3107. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Register Name	Description	VIM Physical Address
1344h	32	MSS_VIM_INTPRIORITY_209	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h213	50F0 1344h
1348h	32	MSS_VIM_INTPRIORITY_210	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h214	50F0 1348h
134Ch	32	MSS_VIM_INTPRIORITY_211	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h215	50F0 134Ch
1350h	32	MSS_VIM_INTPRIORITY_212	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h216	50F0 1350h
1354h	32	MSS_VIM_INTPRIORITY_213	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h217	50F0 1354h
1358h	32	MSS_VIM_INTPRIORITY_214	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h218	50F0 1358h
135Ch	32	MSS_VIM_INTPRIORITY_215	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h219	50F0 135Ch
1360h	32	MSS_VIM_INTPRIORITY_216	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h220	50F0 1360h
1364h	32	MSS_VIM_INTPRIORITY_217	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h221	50F0 1364h
1368h	32	MSS_VIM_INTPRIORITY_218	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h222	50F0 1368h
136Ch	32	MSS_VIM_INTPRIORITY_219	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h223	50F0 136Ch
1370h	32	MSS_VIM_INTPRIORITY_220	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h224	50F0 1370h
1374h	32	MSS_VIM_INTPRIORITY_221	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h225	50F0 1374h
1378h	32	MSS_VIM_INTPRIORITY_222	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h226	50F0 1378h
137Ch	32	MSS_VIM_INTPRIORITY_223	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h227	50F0 137Ch
1380h	32	MSS_VIM_INTPRIORITY_224	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h228	50F0 1380h
1384h	32	MSS_VIM_INTPRIORITY_225	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h229	50F0 1384h
1388h	32	MSS_VIM_INTPRIORITY_226	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h230	50F0 1388h
138Ch	32	MSS_VIM_INTPRIORITY_227	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h231	50F0 138Ch

Table 4-3107. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Register Name	Description	VIM Physical Address
1390h	32	MSS_VIM_INTPRIORITY_228	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h232	50F0 1390h
1394h	32	MSS_VIM_INTPRIORITY_229	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h233	50F0 1394h
1398h	32	MSS_VIM_INTPRIORITY_230	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h234	50F0 1398h
139Ch	32	MSS_VIM_INTPRIORITY_231	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h235	50F0 139Ch
13A0h	32	MSS_VIM_INTPRIORITY_232	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h236	50F0 13A0h
13A4h	32	MSS_VIM_INTPRIORITY_233	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h237	50F0 13A4h
13A8h	32	MSS_VIM_INTPRIORITY_234	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h238	50F0 13A8h
13ACh	32	MSS_VIM_INTPRIORITY_235	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h239	50F0 13ACh
13B0h	32	MSS_VIM_INTPRIORITY_236	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h240	50F0 13B0h
13B4h	32	MSS_VIM_INTPRIORITY_237	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h241	50F0 13B4h
13B8h	32	MSS_VIM_INTPRIORITY_238	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h242	50F0 13B8h
13BCh	32	MSS_VIM_INTPRIORITY_239	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h243	50F0 13BCh
13C0h	32	MSS_VIM_INTPRIORITY_240	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h244	50F0 13C0h
13C4h	32	MSS_VIM_INTPRIORITY_241	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h245	50F0 13C4h
13C8h	32	MSS_VIM_INTPRIORITY_242	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h246	50F0 13C8h
13CCh	32	MSS_VIM_INTPRIORITY_243	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h247	50F0 13CCh
13D0h	32	MSS_VIM_INTPRIORITY_244	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h248	50F0 13D0h
13D4h	32	MSS_VIM_INTPRIORITY_245	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h249	50F0 13D4h
13D8h	32	MSS_VIM_INTPRIORITY_246	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h250	50F0 13D8h

Table 4-3107. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Register Name	Description	VIM Physical Address
13DCh	32	MSS_VIM_INTPRIORITY_247	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h251	50F0 13DCh
13E0h	32	MSS_VIM_INTPRIORITY_248	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h252	50F0 13E0h
13E4h	32	MSS_VIM_INTPRIORITY_249	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h253	50F0 13E4h
13E8h	32	MSS_VIM_INTPRIORITY_250	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h254	50F0 13E8h
13ECh	32	MSS_VIM_INTPRIORITY_251	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h255	50F0 13ECh
13F0h	32	MSS_VIM_INTPRIORITY_252	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h256	50F0 13F0h
13F4h	32	MSS_VIM_INTPRIORITY_253	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h257	50F0 13F4h
13F8h	32	MSS_VIM_INTPRIORITY_254	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h258	50F0 13F8h
13FCh	32	MSS_VIM_INTPRIORITY_255	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h259	50F0 13FCh
2000h	32	MSS_VIM_INTVECTOR	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h4	50F0 2000h
2004h	32	MSS_VIM_INTVECTOR_1	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h5	50F0 2004h
2008h	32	MSS_VIM_INTVECTOR_2	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h6	50F0 2008h
200Ch	32	MSS_VIM_INTVECTOR_3	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h7	50F0 200Ch
2010h	32	MSS_VIM_INTVECTOR_4	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h8	50F0 2010h
2014h	32	MSS_VIM_INTVECTOR_5	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h9	50F0 2014h
2018h	32	MSS_VIM_INTVECTOR_6	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h10	50F0 2018h
201Ch	32	MSS_VIM_INTVECTOR_7	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h11	50F0 201Ch
2020h	32	MSS_VIM_INTVECTOR_8	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h12	50F0 2020h
2024h	32	MSS_VIM_INTVECTOR_9	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h13	50F0 2024h

Table 4-3107. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Register Name	Description	VIM Physical Address
2028h	32	MSS_VIM_INTVECTOR_10	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h14	50F0 2028h
202Ch	32	MSS_VIM_INTVECTOR_11	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h15	50F0 202Ch
2030h	32	MSS_VIM_INTVECTOR_12	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h16	50F0 2030h
2034h	32	MSS_VIM_INTVECTOR_13	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h17	50F0 2034h
2038h	32	MSS_VIM_INTVECTOR_14	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h18	50F0 2038h
203Ch	32	MSS_VIM_INTVECTOR_15	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h19	50F0 203Ch
2040h	32	MSS_VIM_INTVECTOR_16	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h20	50F0 2040h
2044h	32	MSS_VIM_INTVECTOR_17	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h21	50F0 2044h
2048h	32	MSS_VIM_INTVECTOR_18	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h22	50F0 2048h
204Ch	32	MSS_VIM_INTVECTOR_19	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h23	50F0 204Ch
2050h	32	MSS_VIM_INTVECTOR_20	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h24	50F0 2050h
2054h	32	MSS_VIM_INTVECTOR_21	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h25	50F0 2054h
2058h	32	MSS_VIM_INTVECTOR_22	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h26	50F0 2058h
205Ch	32	MSS_VIM_INTVECTOR_23	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h27	50F0 205Ch
2060h	32	MSS_VIM_INTVECTOR_24	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h28	50F0 2060h
2064h	32	MSS_VIM_INTVECTOR_25	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h29	50F0 2064h
2068h	32	MSS_VIM_INTVECTOR_26	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h30	50F0 2068h
206Ch	32	MSS_VIM_INTVECTOR_27	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h31	50F0 206Ch
2070h	32	MSS_VIM_INTVECTOR_28	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h32	50F0 2070h

Table 4-3107. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Register Name	Description	VIM Physical Address
2074h	32	MSS_VIM_INTVECTOR_29	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h33	50F0 2074h
2078h	32	MSS_VIM_INTVECTOR_30	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h34	50F0 2078h
207Ch	32	MSS_VIM_INTVECTOR_31	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h35	50F0 207Ch
2080h	32	MSS_VIM_INTVECTOR_32	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h36	50F0 2080h
2084h	32	MSS_VIM_INTVECTOR_33	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h37	50F0 2084h
2088h	32	MSS_VIM_INTVECTOR_34	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h38	50F0 2088h
208Ch	32	MSS_VIM_INTVECTOR_35	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h39	50F0 208Ch
2090h	32	MSS_VIM_INTVECTOR_36	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h40	50F0 2090h
2094h	32	MSS_VIM_INTVECTOR_37	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h41	50F0 2094h
2098h	32	MSS_VIM_INTVECTOR_38	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h42	50F0 2098h
209Ch	32	MSS_VIM_INTVECTOR_39	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h43	50F0 209Ch
20A0h	32	MSS_VIM_INTVECTOR_40	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h44	50F0 20A0h
20A4h	32	MSS_VIM_INTVECTOR_41	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h45	50F0 20A4h
20A8h	32	MSS_VIM_INTVECTOR_42	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h46	50F0 20A8h
20ACh	32	MSS_VIM_INTVECTOR_43	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h47	50F0 20ACh
20B0h	32	MSS_VIM_INTVECTOR_44	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h48	50F0 20B0h
20B4h	32	MSS_VIM_INTVECTOR_45	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h49	50F0 20B4h
20B8h	32	MSS_VIM_INTVECTOR_46	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h50	50F0 20B8h
20BCh	32	MSS_VIM_INTVECTOR_47	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h51	50F0 20BCh

Table 4-3107. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Register Name	Description	VIM Physical Address
20C0h	32	MSS_VIM_INTVECTOR_48	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h52	50F0 20C0h
20C4h	32	MSS_VIM_INTVECTOR_49	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h53	50F0 20C4h
20C8h	32	MSS_VIM_INTVECTOR_50	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h54	50F0 20C8h
20CCh	32	MSS_VIM_INTVECTOR_51	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h55	50F0 20CCh
20D0h	32	MSS_VIM_INTVECTOR_52	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h56	50F0 20D0h
20D4h	32	MSS_VIM_INTVECTOR_53	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h57	50F0 20D4h
20D8h	32	MSS_VIM_INTVECTOR_54	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h58	50F0 20D8h
20DCh	32	MSS_VIM_INTVECTOR_55	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h59	50F0 20DCh
20E0h	32	MSS_VIM_INTVECTOR_56	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h60	50F0 20E0h
20E4h	32	MSS_VIM_INTVECTOR_57	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h61	50F0 20E4h
20E8h	32	MSS_VIM_INTVECTOR_58	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h62	50F0 20E8h
20ECh	32	MSS_VIM_INTVECTOR_59	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h63	50F0 20ECh
20F0h	32	MSS_VIM_INTVECTOR_60	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h64	50F0 20F0h
20F4h	32	MSS_VIM_INTVECTOR_61	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h65	50F0 20F4h
20F8h	32	MSS_VIM_INTVECTOR_62	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h66	50F0 20F8h
20FCh	32	MSS_VIM_INTVECTOR_63	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h67	50F0 20FCh
2100h	32	MSS_VIM_INTVECTOR_64	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h68	50F0 2100h
2104h	32	MSS_VIM_INTVECTOR_65	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h69	50F0 2104h
2108h	32	MSS_VIM_INTVECTOR_66	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h70	50F0 2108h

Table 4-3107. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Register Name	Description	VIM Physical Address
210Ch	32	MSS_VIM_INTVECTOR_67	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h71	50F0 210Ch
2110h	32	MSS_VIM_INTVECTOR_68	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h72	50F0 2110h
2114h	32	MSS_VIM_INTVECTOR_69	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h73	50F0 2114h
2118h	32	MSS_VIM_INTVECTOR_70	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h74	50F0 2118h
211Ch	32	MSS_VIM_INTVECTOR_71	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h75	50F0 211Ch
2120h	32	MSS_VIM_INTVECTOR_72	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h76	50F0 2120h
2124h	32	MSS_VIM_INTVECTOR_73	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h77	50F0 2124h
2128h	32	MSS_VIM_INTVECTOR_74	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h78	50F0 2128h
212Ch	32	MSS_VIM_INTVECTOR_75	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h79	50F0 212Ch
2130h	32	MSS_VIM_INTVECTOR_76	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h80	50F0 2130h
2134h	32	MSS_VIM_INTVECTOR_77	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h81	50F0 2134h
2138h	32	MSS_VIM_INTVECTOR_78	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h82	50F0 2138h
213Ch	32	MSS_VIM_INTVECTOR_79	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h83	50F0 213Ch
2140h	32	MSS_VIM_INTVECTOR_80	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h84	50F0 2140h
2144h	32	MSS_VIM_INTVECTOR_81	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h85	50F0 2144h
2148h	32	MSS_VIM_INTVECTOR_82	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h86	50F0 2148h
214Ch	32	MSS_VIM_INTVECTOR_83	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h87	50F0 214Ch
2150h	32	MSS_VIM_INTVECTOR_84	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h88	50F0 2150h
2154h	32	MSS_VIM_INTVECTOR_85	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h89	50F0 2154h

Table 4-3107. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Register Name	Description	VIM Physical Address
2158h	32	MSS_VIM_INTVECTOR_86	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h90	50F0 2158h
215Ch	32	MSS_VIM_INTVECTOR_87	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h91	50F0 215Ch
2160h	32	MSS_VIM_INTVECTOR_88	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h92	50F0 2160h
2164h	32	MSS_VIM_INTVECTOR_89	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h93	50F0 2164h
2168h	32	MSS_VIM_INTVECTOR_90	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h94	50F0 2168h
216Ch	32	MSS_VIM_INTVECTOR_91	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h95	50F0 216Ch
2170h	32	MSS_VIM_INTVECTOR_92	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h96	50F0 2170h
2174h	32	MSS_VIM_INTVECTOR_93	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h97	50F0 2174h
2178h	32	MSS_VIM_INTVECTOR_94	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h98	50F0 2178h
217Ch	32	MSS_VIM_INTVECTOR_95	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h99	50F0 217Ch
2180h	32	MSS_VIM_INTVECTOR_96	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h100	50F0 2180h
2184h	32	MSS_VIM_INTVECTOR_97	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h101	50F0 2184h
2188h	32	MSS_VIM_INTVECTOR_98	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h102	50F0 2188h
218Ch	32	MSS_VIM_INTVECTOR_99	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h103	50F0 218Ch
2190h	32	MSS_VIM_INTVECTOR_100	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h104	50F0 2190h
2194h	32	MSS_VIM_INTVECTOR_101	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h105	50F0 2194h
2198h	32	MSS_VIM_INTVECTOR_102	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h106	50F0 2198h
219Ch	32	MSS_VIM_INTVECTOR_103	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h107	50F0 219Ch
21A0h	32	MSS_VIM_INTVECTOR_104	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h108	50F0 21A0h

Table 4-3107. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Register Name	Description	VIM Physical Address
21A4h	32	MSS_VIM_INTVECTOR_105	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h109	50F0 21A4h
21A8h	32	MSS_VIM_INTVECTOR_106	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h110	50F0 21A8h
21ACh	32	MSS_VIM_INTVECTOR_107	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h111	50F0 21ACh
21B0h	32	MSS_VIM_INTVECTOR_108	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h112	50F0 21B0h
21B4h	32	MSS_VIM_INTVECTOR_109	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h113	50F0 21B4h
21B8h	32	MSS_VIM_INTVECTOR_110	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h114	50F0 21B8h
21BCh	32	MSS_VIM_INTVECTOR_111	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h115	50F0 21BCh
21C0h	32	MSS_VIM_INTVECTOR_112	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h116	50F0 21C0h
21C4h	32	MSS_VIM_INTVECTOR_113	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h117	50F0 21C4h
21C8h	32	MSS_VIM_INTVECTOR_114	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h118	50F0 21C8h
21CCh	32	MSS_VIM_INTVECTOR_115	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h119	50F0 21CCh
21D0h	32	MSS_VIM_INTVECTOR_116	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h120	50F0 21D0h
21D4h	32	MSS_VIM_INTVECTOR_117	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h121	50F0 21D4h
21D8h	32	MSS_VIM_INTVECTOR_118	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h122	50F0 21D8h
21DCh	32	MSS_VIM_INTVECTOR_119	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h123	50F0 21DCh
21E0h	32	MSS_VIM_INTVECTOR_120	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h124	50F0 21E0h
21E4h	32	MSS_VIM_INTVECTOR_121	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h125	50F0 21E4h
21E8h	32	MSS_VIM_INTVECTOR_122	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h126	50F0 21E8h
21ECh	32	MSS_VIM_INTVECTOR_123	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h127	50F0 21ECh

Table 4-3107. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Register Name	Description	VIM Physical Address
21F0h	32	MSS_VIM_INTVECTOR_124	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h128	50F0 21F0h
21F4h	32	MSS_VIM_INTVECTOR_125	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h129	50F0 21F4h
21F8h	32	MSS_VIM_INTVECTOR_126	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h130	50F0 21F8h
21FCh	32	MSS_VIM_INTVECTOR_127	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h131	50F0 21FCh
2200h	32	MSS_VIM_INTVECTOR_128	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h132	50F0 2200h
2204h	32	MSS_VIM_INTVECTOR_129	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h133	50F0 2204h
2208h	32	MSS_VIM_INTVECTOR_130	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h134	50F0 2208h
220Ch	32	MSS_VIM_INTVECTOR_131	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h135	50F0 220Ch
2210h	32	MSS_VIM_INTVECTOR_132	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h136	50F0 2210h
2214h	32	MSS_VIM_INTVECTOR_133	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h137	50F0 2214h
2218h	32	MSS_VIM_INTVECTOR_134	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h138	50F0 2218h
221Ch	32	MSS_VIM_INTVECTOR_135	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h139	50F0 221Ch
2220h	32	MSS_VIM_INTVECTOR_136	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h140	50F0 2220h
2224h	32	MSS_VIM_INTVECTOR_137	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h141	50F0 2224h
2228h	32	MSS_VIM_INTVECTOR_138	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h142	50F0 2228h
222Ch	32	MSS_VIM_INTVECTOR_139	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h143	50F0 222Ch
2230h	32	MSS_VIM_INTVECTOR_140	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h144	50F0 2230h
2234h	32	MSS_VIM_INTVECTOR_141	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h145	50F0 2234h
2238h	32	MSS_VIM_INTVECTOR_142	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h146	50F0 2238h

Table 4-3107. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Register Name	Description	VIM Physical Address
223Ch	32	MSS_VIM_INTVECTOR_143	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h147	50F0 223Ch
2240h	32	MSS_VIM_INTVECTOR_144	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h148	50F0 2240h
2244h	32	MSS_VIM_INTVECTOR_145	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h149	50F0 2244h
2248h	32	MSS_VIM_INTVECTOR_146	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h150	50F0 2248h
224Ch	32	MSS_VIM_INTVECTOR_147	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h151	50F0 224Ch
2250h	32	MSS_VIM_INTVECTOR_148	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h152	50F0 2250h
2254h	32	MSS_VIM_INTVECTOR_149	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h153	50F0 2254h
2258h	32	MSS_VIM_INTVECTOR_150	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h154	50F0 2258h
225Ch	32	MSS_VIM_INTVECTOR_151	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h155	50F0 225Ch
2260h	32	MSS_VIM_INTVECTOR_152	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h156	50F0 2260h
2264h	32	MSS_VIM_INTVECTOR_153	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h157	50F0 2264h
2268h	32	MSS_VIM_INTVECTOR_154	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h158	50F0 2268h
226Ch	32	MSS_VIM_INTVECTOR_155	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h159	50F0 226Ch
2270h	32	MSS_VIM_INTVECTOR_156	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h160	50F0 2270h
2274h	32	MSS_VIM_INTVECTOR_157	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h161	50F0 2274h
2278h	32	MSS_VIM_INTVECTOR_158	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h162	50F0 2278h
227Ch	32	MSS_VIM_INTVECTOR_159	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h163	50F0 227Ch
2280h	32	MSS_VIM_INTVECTOR_160	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h164	50F0 2280h
2284h	32	MSS_VIM_INTVECTOR_161	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h165	50F0 2284h

Table 4-3107. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Register Name	Description	VIM Physical Address
2288h	32	MSS_VIM_INTVECTOR_162	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h166	50F0 2288h
228Ch	32	MSS_VIM_INTVECTOR_163	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h167	50F0 228Ch
2290h	32	MSS_VIM_INTVECTOR_164	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h168	50F0 2290h
2294h	32	MSS_VIM_INTVECTOR_165	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h169	50F0 2294h
2298h	32	MSS_VIM_INTVECTOR_166	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h170	50F0 2298h
229Ch	32	MSS_VIM_INTVECTOR_167	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h171	50F0 229Ch
22A0h	32	MSS_VIM_INTVECTOR_168	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h172	50F0 22A0h
22A4h	32	MSS_VIM_INTVECTOR_169	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h173	50F0 22A4h
22A8h	32	MSS_VIM_INTVECTOR_170	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h174	50F0 22A8h
22ACh	32	MSS_VIM_INTVECTOR_171	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h175	50F0 22ACh
22B0h	32	MSS_VIM_INTVECTOR_172	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h176	50F0 22B0h
22B4h	32	MSS_VIM_INTVECTOR_173	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h177	50F0 22B4h
22B8h	32	MSS_VIM_INTVECTOR_174	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h178	50F0 22B8h
22BCh	32	MSS_VIM_INTVECTOR_175	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h179	50F0 22BCh
22C0h	32	MSS_VIM_INTVECTOR_176	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h180	50F0 22C0h
22C4h	32	MSS_VIM_INTVECTOR_177	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h181	50F0 22C4h
22C8h	32	MSS_VIM_INTVECTOR_178	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h182	50F0 22C8h
22CCh	32	MSS_VIM_INTVECTOR_179	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h183	50F0 22CCh
22D0h	32	MSS_VIM_INTVECTOR_180	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h184	50F0 22D0h

Table 4-3107. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Register Name	Description	VIM Physical Address
22D4h	32	MSS_VIM_INTVECTOR_181	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h185	50F0 22D4h
22D8h	32	MSS_VIM_INTVECTOR_182	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h186	50F0 22D8h
22DCh	32	MSS_VIM_INTVECTOR_183	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h187	50F0 22DCh
22E0h	32	MSS_VIM_INTVECTOR_184	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h188	50F0 22E0h
22E4h	32	MSS_VIM_INTVECTOR_185	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h189	50F0 22E4h
22E8h	32	MSS_VIM_INTVECTOR_186	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h190	50F0 22E8h
22ECh	32	MSS_VIM_INTVECTOR_187	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h191	50F0 22ECh
22F0h	32	MSS_VIM_INTVECTOR_188	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h192	50F0 22F0h
22F4h	32	MSS_VIM_INTVECTOR_189	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h193	50F0 22F4h
22F8h	32	MSS_VIM_INTVECTOR_190	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h194	50F0 22F8h
22FCh	32	MSS_VIM_INTVECTOR_191	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h195	50F0 22FCh
2300h	32	MSS_VIM_INTVECTOR_192	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h196	50F0 2300h
2304h	32	MSS_VIM_INTVECTOR_193	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h197	50F0 2304h
2308h	32	MSS_VIM_INTVECTOR_194	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h198	50F0 2308h
230Ch	32	MSS_VIM_INTVECTOR_195	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h199	50F0 230Ch
2310h	32	MSS_VIM_INTVECTOR_196	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h200	50F0 2310h
2314h	32	MSS_VIM_INTVECTOR_197	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h201	50F0 2314h
2318h	32	MSS_VIM_INTVECTOR_198	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h202	50F0 2318h
231Ch	32	MSS_VIM_INTVECTOR_199	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h203	50F0 231Ch

Table 4-3107. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Register Name	Description	VIM Physical Address
2320h	32	MSS_VIM_INTVECTOR_200	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h204	50F0 2320h
2324h	32	MSS_VIM_INTVECTOR_201	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h205	50F0 2324h
2328h	32	MSS_VIM_INTVECTOR_202	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h206	50F0 2328h
232Ch	32	MSS_VIM_INTVECTOR_203	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h207	50F0 232Ch
2330h	32	MSS_VIM_INTVECTOR_204	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h208	50F0 2330h
2334h	32	MSS_VIM_INTVECTOR_205	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h209	50F0 2334h
2338h	32	MSS_VIM_INTVECTOR_206	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h210	50F0 2338h
233Ch	32	MSS_VIM_INTVECTOR_207	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h211	50F0 233Ch
2340h	32	MSS_VIM_INTVECTOR_208	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h212	50F0 2340h
2344h	32	MSS_VIM_INTVECTOR_209	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h213	50F0 2344h
2348h	32	MSS_VIM_INTVECTOR_210	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h214	50F0 2348h
234Ch	32	MSS_VIM_INTVECTOR_211	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h215	50F0 234Ch
2350h	32	MSS_VIM_INTVECTOR_212	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h216	50F0 2350h
2354h	32	MSS_VIM_INTVECTOR_213	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h217	50F0 2354h
2358h	32	MSS_VIM_INTVECTOR_214	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h218	50F0 2358h
235Ch	32	MSS_VIM_INTVECTOR_215	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h219	50F0 235Ch
2360h	32	MSS_VIM_INTVECTOR_216	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h220	50F0 2360h
2364h	32	MSS_VIM_INTVECTOR_217	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h221	50F0 2364h
2368h	32	MSS_VIM_INTVECTOR_218	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h222	50F0 2368h

Table 4-3107. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Register Name	Description	VIM Physical Address
236Ch	32	MSS_VIM_INTVECTOR_219	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h223	50F0 236Ch
2370h	32	MSS_VIM_INTVECTOR_220	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h224	50F0 2370h
2374h	32	MSS_VIM_INTVECTOR_221	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h225	50F0 2374h
2378h	32	MSS_VIM_INTVECTOR_222	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h226	50F0 2378h
237Ch	32	MSS_VIM_INTVECTOR_223	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h227	50F0 237Ch
2380h	32	MSS_VIM_INTVECTOR_224	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h228	50F0 2380h
2384h	32	MSS_VIM_INTVECTOR_225	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h229	50F0 2384h
2388h	32	MSS_VIM_INTVECTOR_226	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h230	50F0 2388h
238Ch	32	MSS_VIM_INTVECTOR_227	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h231	50F0 238Ch
2390h	32	MSS_VIM_INTVECTOR_228	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h232	50F0 2390h
2394h	32	MSS_VIM_INTVECTOR_229	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h233	50F0 2394h
2398h	32	MSS_VIM_INTVECTOR_230	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h234	50F0 2398h
239Ch	32	MSS_VIM_INTVECTOR_231	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h235	50F0 239Ch
23A0h	32	MSS_VIM_INTVECTOR_232	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h236	50F0 23A0h
23A4h	32	MSS_VIM_INTVECTOR_233	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h237	50F0 23A4h
23A8h	32	MSS_VIM_INTVECTOR_234	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h238	50F0 23A8h
23ACh	32	MSS_VIM_INTVECTOR_235	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h239	50F0 23ACh
23B0h	32	MSS_VIM_INTVECTOR_236	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h240	50F0 23B0h
23B4h	32	MSS_VIM_INTVECTOR_237	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h241	50F0 23B4h

Table 4-3107. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Register Name	Description	VIM Physical Address
23B8h	32	MSS_VIM_INTVECTOR_238	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h242	50F0 23B8h
23BCh	32	MSS_VIM_INTVECTOR_239	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h243	50F0 23BCh
23C0h	32	MSS_VIM_INTVECTOR_240	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h244	50F0 23C0h
23C4h	32	MSS_VIM_INTVECTOR_241	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h245	50F0 23C4h
23C8h	32	MSS_VIM_INTVECTOR_242	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h246	50F0 23C8h
23CCh	32	MSS_VIM_INTVECTOR_243	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h247	50F0 23CCh
23D0h	32	MSS_VIM_INTVECTOR_244	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h248	50F0 23D0h
23D4h	32	MSS_VIM_INTVECTOR_245	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h249	50F0 23D4h
23D8h	32	MSS_VIM_INTVECTOR_246	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h250	50F0 23D8h
23DCh	32	MSS_VIM_INTVECTOR_247	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h251	50F0 23DCh
23E0h	32	MSS_VIM_INTVECTOR_248	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h252	50F0 23E0h
23E4h	32	MSS_VIM_INTVECTOR_249	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h253	50F0 23E4h
23E8h	32	MSS_VIM_INTVECTOR_250	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h254	50F0 23E8h
23ECh	32	MSS_VIM_INTVECTOR_251	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h255	50F0 23ECh
23F0h	32	MSS_VIM_INTVECTOR_252	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h256	50F0 23F0h
23F4h	32	MSS_VIM_INTVECTOR_253	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h257	50F0 23F4h
23F8h	32	MSS_VIM_INTVECTOR_254	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h258	50F0 23F8h
23FCh	32	MSS_VIM_INTVECTOR_255	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h259	50F0 23FCh

4.24.1 VIM_MSS_VIM_PID Registers

4.24.1.1 VIM_PID Register (Offset = 0h) [reset = h]

Short Description: The Revision Register contains the major and minor revisions for the module.

Long Description: The Revision Register contains the major and minor revisions for the module.

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Table 4-3108. Instance Table

Instance Name	Physical Address
VIM	50F0 0000h

Figure 4-1459. PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		FUNC											
RO		RO		RO											
1		2		144											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
RO					RO			RO		RO					
0					0			0		1					

Access Types Legend

Table 4-3109. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	PID register scheme
29 - 28	BU	RO	2h	Business Unit: 10 = Processors
27 - 16	FUNC	RO	90h	Module ID
15 - 11	RTL	RO	0h	RTL revision. Will vary depending on release.
10 - 8	MAJOR	RO	0h	Major revision
7 - 6	CUSTOM	RO	0h	Custom
5 - 0	MINOR	RO	1h	Minor revision

4.24.2 VIM_MSS_VIM_INFO Registers

4.24.2.1 VIM_INFO Register (Offset = 4h) [reset = h]

Short Description: The Info Register gives the configuration Inforrmation of this VIM.

Long Description: The Info Register gives the configuration Inforrmation of this VIM.

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Table 4-3110. Instance Table

Instance Name	Physical Address
VIM	50F0 0004h

Figure 4-1460. INFO Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES1					INTERRUPTS										
RO					RO										
0					256										

Access Types Legend

Table 4-3111. INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 11	RES1	RO	0h	RESERVE FIELD
10 - 0	INTERRUPTS	RO	100h	Total number of Interrupts

4.24.3 VIM_MSS_VIM_PRIIRQ Registers

4.24.3.1 VIM_PRIIRQ Register (Offset = 8h) [reset = h]

Short Description: The Prioritized IRQ Register shows the number of the highest priority pending IRQ.

Long Description: The Prioritized IRQ Register shows the number of the highest priority pending IRQ.

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Table 4-3112. Instance Table

Instance Name	Physical Address
VIM	50F0 0008h

Figure 4-1461. PRIIRQ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VALID	RES2											PRI			
RO	RO											RO			
0	0											0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES3						NUM									
RO						RO									
0						0									

Access Types Legend

Table 4-3113. PRIIRQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VALID	RO	0h	Indicates that the num field is valid.
30 - 20	RES2	RO	0h	RESERVE FIELD
19 - 16	PRI	RO	0h	Priority of the highest priority pending IRQ. valid only if the valid flag is set.
15 - 10	RES3	RO	0h	RESERVE FIELD
9 - 0	NUM	RO	0h	Number of the highest priority pending IRQ. valid only if the valid flag is set.

4.24.4 VIM_MSS_VIM_PRIFIQ Registers

4.24.4.1 VIM_PRIFIQ Register (Offset = Ch) [reset = h]

Short Description: The Prioritized FIQ Register shows the number of the highest priority pending FIQ.

Long Description: The Prioritized FIQ Register shows the number of the highest priority pending FIQ.

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Table 4-3114. Instance Table

Instance Name	Physical Address
VIM	50F0 000Ch

Figure 4-1462. PRIFIQ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VALID	RES4											PRI			
RO	RO											RO			
0	0											0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES5						NUM									
RO						RO									
0						0									

Access Types Legend

Table 4-3115. PRIFIQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VALID	RO	0h	Indicates that the num field is valid.
30 - 20	RES4	RO	0h	RESERVE FIELD
19 - 16	PRI	RO	0h	Priority of the highest priority pending FIQ. valid only if the valid flag is set.
15 - 10	RES5	RO	0h	RESERVE FIELD
9 - 0	NUM	RO	0h	Number of the highest priority pending FIQ. valid only if the valid flag is set.

4.24.5 VIM_MSS_VIM_IRQGSTS Registers

4.24.5.1 VIM_IRQGSTS Register (Offset = 10h) [reset = h]

Short Description: The IRQ Group Status Register indicates which groups have pending IRQ interrupts.

Long Description: The IRQ Group Status Register indicates which groups have pending IRQ interrupts.

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Table 4-3116. Instance Table

Instance Name	Physical Address
VIM	50F0 0010h

Figure 4-1463. IRQGSTS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STS															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STS															
RO															
0															

Access Types Legend

Table 4-3117. IRQGSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RO	0h	Indicates that the num field is valid.

4.24.6 VIM_MSS_VIM_FIQGSTS Registers

4.24.6.1 VIM_FIQGSTS Register (Offset = 14h) [reset = h]

Short Description: The FIQ Group Status Register indicates which groups have pending FIQ interrupts.

Long Description: The FIQ Group Status Register indicates which groups have pending FIQ interrupts.

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Table 4-3118. Instance Table

Instance Name	Physical Address
VIM	50F0 0014h

Figure 4-1464. FIQGSTS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STS															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STS															
RO															
0															

Access Types Legend

Table 4-3119. FIQGSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RO	0h	Indicates that the num field is valid.

4.24.7 VIM_MSS_VIM_IRQVEC Registers

4.24.7.1 VIM_IRQVEC Register (Offset = 18h) [reset = h]

Short Description: The IRQ Vector Address Register contains the 32-bit address of the interrupt vector for the current pendind IRQ.

Long Description: The IRQ Vector Address Register contains the 32-bit address of the interrupt vector for the current pendind IRQ.

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Table 4-3120. Instance Table

Instance Name	Physical Address
VIM	50F0 0018h

Figure 4-1465. IRQVEC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES21	
RW														RO	
0														0	

Access Types Legend

Table 4-3121. IRQVEC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	Upper 30 bits of the 32-bit vector address. Only valid if the Prioritized IRQ Register valid flag is true.
1 - 0	RES21	RO	0h	RESERVE FIELD

4.24.8 VIM_MSS_VIM_FIQVEC Registers

4.24.8.1 VIM_FIQVEC Register (Offset = 1Ch) [reset = h]

Short Description: The FIQ Vector Address Register contains the 32-bit address of the interrupt vector for the current pendind FIQ.

Long Description: The FIQ Vector Address Register contains the 32-bit address of the interrupt vector for the current pendind FIQ.

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Table 4-3122. Instance Table

Instance Name	Physical Address
VIM	50F0 001Ch

Figure 4-1466. FIQVEC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES22	
RW														RO	
0														0	

Access Types Legend

Table 4-3123. FIQVEC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	Upper 30 bits of the 32-bit vector address. Only valid if the Prioritized FIQ Register valid flag is true.
1 - 0	RES22	RO	0h	RESERVE FIELD

4.24.9 VIM_MSS_VIM_ACTIRQ Registers

4.24.9.1 VIM_ACTIRQ Register (Offset = 20h) [reset = h]

Short Description: The Active IRQ Register shows the number of the currently active IRQ.

Long Description: The Active IRQ Register shows the number of the currently active IRQ.

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Table 4-3124. Instance Table

Instance Name	Physical Address
VIM	50F0 0020h

Figure 4-1467. ACTIRQ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VALID	RES6											PRI			
RO	RO											RO			
0	0											0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES7						NUM									
RO						RO									
0						0									

Access Types Legend

Table 4-3125. ACTIRQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VALID	RO	0h	Indicates that the num field is valid. Set when the IRQ Vector Address Register is read and cleared whenever the IRQ Vector Address Register is written.
30 - 20	RES6	RO	0h	RESERVE FIELD
19 - 16	PRI	RO	0h	Priority of the highest priority pending IRQ. valid only if the valid flag is set.
15 - 10	RES7	RO	0h	RESERVE FIELD
9 - 0	NUM	RO	0h	Number of the currently active IRQ. Loaded from teh Prioritized IRQ Register whenever the IRQ Vector Address is read. Valid only if the valid flag is set.

4.24.10 VIM_MSS_VIM_ACTFIQ Registers

4.24.10.1 VIM_ACTFIQ Register (Offset = 24h) [reset = h]

Short Description: The Active FIQ Register shows the number of the currently active FIQ.

Long Description: The Active FIQ Register shows the number of the currently active FIQ.

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Table 4-3126. Instance Table

Instance Name	Physical Address
VIM	50F0 0024h

Figure 4-1468. ACTFIQ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VALID	RES8											PRI			
RO	RO											RO			
0	0											0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES9						NUM									
RO						RO									
0						0									

Access Types Legend

Table 4-3127. ACTFIQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VALID	RO	0h	Indicates that the num field is valid. Set when the FIQ Vector Address Register is read and cleared whenever the FIQ Vector Address Register is written.
30 - 20	RES8	RO	0h	RESERVE FIELD
19 - 16	PRI	RO	0h	Priority of the highest priority pending IRQ. valid only if the valid flag is set.
15 - 10	RES9	RO	0h	RESERVE FIELD
9 - 0	NUM	RO	0h	Number of the currently active FIQ. Loaded from teh Prioritized FIQ Register whenever the FIQ Vector Address is read. Valid only if the valid flag is set.

4.24.11 VIM_MSS_VIM_IRQPRIMSK Registers

4.24.11.1 VIM_IRQPRIMSK Register (Offset = 28h) [reset = h]

Short Description: The IRQ Priority Mask Register allows all IRQs of a particular priority to be enabled or disabled.

Long Description: The IRQ Priority Mask Register allows all IRQs of a particular priority to be enabled or disabled.

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Table 4-3128. Instance Table

Instance Name	Physical Address
VIM	50F0 0028h

Figure 4-1469. IRQPRIMSK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSK															
RW															
65535															

Access Types Legend

Table 4-3129. IRQPRIMSK Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RES24	RO	0h	RESERVE FIELD
15 - 0	MSK	RW	FFFFh	Each bit corresponds to the given priority. 1 - IRQs of this priority are enabled. 0 - IRQs of this priority are disabled.

4.24.12 VIM_MSS_VIM_FIQPRIMSK Registers

4.24.12.1 VIM_FIQPRIMSK Register (Offset = 2Ch) [reset = h]

Short Description: The FIQ Priority Mask Register allows all FIQs of a particular priority to be enabled or disabled.

Long Description: The FIQ Priority Mask Register allows all FIQs of a particular priority to be enabled or disabled.

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Table 4-3130. Instance Table

Instance Name	Physical Address
VIM	50F0 002Ch

Figure 4-1470. FIQPRIMSK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSK															
RW															
65535															

Access Types Legend

Table 4-3131. FIQPRIMSK Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RES24	RO	0h	RESERVE FIELD
15 - 0	MSK	RW	FFFFh	Each bit corresponds to the given priority. 1 - FIQs of this priority are enabled. 0 - FIQs of this priority are disabled.

4.24.13 VIM_MSS_VIM_DEDVEC Registers

4.24.13.1 VIM_DEDVEC Register (Offset = 30h) [reset = h]

Short Description: The DED Vector Address contains a default vector address for when an uncorrectable error is detected for an active IRQ or FIQ.

Long Description: The DED Vector Address contains a default vector address for when an uncorrectable error is detected for an active IRQ or FIQ.

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Table 4-3132. Instance Table

Instance Name	Physical Address
VIM	50F0 0030h

Figure 4-1471. DEDVEC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES23	
RW														RO	
0														0	

Access Types Legend

Table 4-3133. DEDVEC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	Upper 30 bits of the 32-bit vector address.
1 - 0	RES23	RO	0h	RESERVE FIELD

4.24.14 VIM_MSS_VIM_RAW Registers

4.24.14.1 VIM_RAW Register (Offset = 400h) [reset = h]

Short Description: Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00

Long Description: Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00

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Table 4-3134. Instance Table

Instance Name	Physical Address
VIM	50F0 0400h

Figure 4-1472. RAW Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STS															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STS															
RW															
0															

Access Types Legend

Table 4-3135. RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RW	0h	This is the raw status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 InactiveRead 1 Active/ PendingWrite 0 No effectWrite 1 Set to Interrupt Raw Status

4.24.15 VIM_MSS_VIM_STS Registers

4.24.15.1 VIM_STS Register (Offset = 404h) [reset = h]

Short Description: Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04

Long Description: Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04

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Table 4-3136. Instance Table

Instance Name	Physical Address
VIM	50F0 0404h

Figure 4-1473. STS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3137. STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Inactive or DisabledRead 1 Active/Pending and EnabledWrite 0 No effectWrite 1 Clear Interrupt Raw Status

4.24.16 VIM_MSS_VIM_INTR_EN_SET Registers

4.24.16.1 VIM_EN_SET Register (Offset = 408h) [reset = h]

Short Description: Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08

Long Description: Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08

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Table 4-3138. Instance Table

Instance Name	Physical Address
VIM	50F0 0408h

Figure 4-1474. INTR_EN_SET Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3139. INTR_EN_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to enable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Set Enable

4.24.17 VIM_MSS_VIM_INTER_EN_CLR Registers

4.24.17.1 VIM_EN_CLR Register (Offset = 40Ch) [reset = h]

Short Description: Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C

Long Description: Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C

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Table 4-3140. Instance Table

Instance Name	Physical Address
VIM	50F0 040Ch

Figure 4-1475. INTER_EN_CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3141. INTER_EN_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to disable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Clear Enable

4.24.18 VIM_MSS_VIM_IRQSTS Registers

4.24.18.1 VIM_IRQSTS Register (Offset = 410h) [reset = h]

Short Description: Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10

Long Description: Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10

Return to Summary Table

Table 4-3142. Instance Table

Instance Name	Physical Address
VIM	50F0 0410h

Figure 4-1476. IRQSTS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3143. IRQSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to IRQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an IRQRead 1 Active/Pending, Enabled, and IRQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if IRQ)

4.24.19 VIM_MSS_VIM_FIQSTS Registers

4.24.19.1 VIM_FIQSTS Register (Offset = 414h) [reset = h]

Short Description: Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14

Long Description: Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14

Return to Summary Table

Table 4-3144. Instance Table

Instance Name	Physical Address
VIM	50F0 0414h

Figure 4-1477. FIQSTS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3145. FIQSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to FIQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an FIQRead 1 Active/Pending, Enabled, and FIQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if FIQ)

4.24.20 VIM_MSS_VIM_INTMAP Registers

4.24.20.1 VIM_INTMAP Register (Offset = 418h) [reset = h]

Short Description: Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18

Long Description: Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18

Return to Summary Table

Table 4-3146. Instance Table

Instance Name	Physical Address
VIM	50F0 0418h

Figure 4-1478. INTMAP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3147. INTMAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to indicate which interrupt the corresponding event influences (if enabled) for event group M. Each bit corresponds to event Q where Q = Mx32+Bit 0 IRQ Interrupt (default)1 FIQ Interrupt

4.24.21 VIM_MSS_VIM_INTTYPE Registers

4.24.21.1 VIM_INTTYPE Register (Offset = 41Ch) [reset = h]

Short Description: Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C

Long Description: Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C

Return to Summary Table

Table 4-3148. Instance Table

Instance Name	Physical Address
VIM	50F0 041Ch

Figure 4-1479. INTTYPE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VAL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL															
RW															
0															

Access Types Legend

Table 4-3149. INTTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	VAL	RW	0h	This field is used to indicate whether the source of an interrupt is a level (default) or a pulse for event group M. This is informational so that an ISR may query this register and know whether it has to clear a pulse event or a level event (see 3.4 Interrupt Handling). The value has no effect on how the VIM hardware functions. The input interrupts are agnostic as to whether they are pulse or level. Each bit corresponds to event Q where Q = Mx32+Bit0 Level (default)1 Pulse

4.24.22 VIM_MSS_VIM_RAW_1 Registers

4.24.22.1 VIM_1 Register (Offset = 420h) [reset = h]

Short Description: Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00

Long Description: Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00

Return to Summary Table

Table 4-3150. Instance Table

Instance Name	Physical Address
VIM	50F0 0420h

Figure 4-1480. RAW_1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STS															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STS															
RW															
0															

Access Types Legend

Table 4-3151. RAW_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RW	0h	This is the raw status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 InactiveRead 1 Active/ PendingWrite 0 No effectWrite 1 Set to Interrupt Raw Status

4.24.23 VIM_MSS_VIM_STS_1 Registers

4.24.23.1 VIM_1 Register (Offset = 424h) [reset = h]

Short Description: Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04

Long Description: Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04

Return to Summary Table

Table 4-3152. Instance Table

Instance Name	Physical Address
VIM	50F0 0424h

Figure 4-1481. STS_1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3153. STS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Inactive or DisabledRead 1 Active/Pending and EnabledWrite 0 No effectWrite 1 Clear Interrupt Raw Status

4.24.24 VIM_MSS_VIM_INTR_EN_SET_1 Registers

4.24.24.1 VIM_EN_SET_1 Register (Offset = 428h) [reset = h]

Short Description: Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08

Long Description: Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08

Return to Summary Table

Table 4-3154. Instance Table

Instance Name	Physical Address
VIM	50F0 0428h

Figure 4-1482. INTR_EN_SET_1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3155. INTR_EN_SET_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to enable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Set Enable

4.24.25 VIM_MSS_VIM_INTER_EN_CLR_1 Registers

4.24.25.1 VIM_EN_CLR_1 Register (Offset = 42Ch) [reset = h]

Short Description: Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C

Long Description: Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C

Return to Summary Table

Table 4-3156. Instance Table

Instance Name	Physical Address
VIM	50F0 042Ch

Figure 4-1483. INTER_EN_CLR_1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3157. INTER_EN_CLR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to disable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Clear Enable

4.24.26 VIM_MSS_VIM_IRQSTS_1 Registers

4.24.26.1 VIM_1 Register (Offset = 430h) [reset = h]

Short Description: Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10

Long Description: Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10

Return to Summary Table

Table 4-3158. Instance Table

Instance Name	Physical Address
VIM	50F0 0430h

Figure 4-1484. IRQSTS_1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3159. IRQSTS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to IRQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an IRQRead 1 Active/Pending, Enabled, and IRQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if IRQ)

4.24.27 VIM_MSS_VIM_FIQSTS_1 Registers

4.24.27.1 VIM_1 Register (Offset = 434h) [reset = h]

Short Description: Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14

Long Description: Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14

Return to Summary Table

Table 4-3160. Instance Table

Instance Name	Physical Address
VIM	50F0 0434h

Figure 4-1485. FIQSTS_1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3161. FIQSTS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to FIQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an FIQRead 1 Active/Pending, Enabled, and FIQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if FIQ)

4.24.28 VIM_MSS_VIM_INTMAP_1 Registers

4.24.28.1 VIM_1 Register (Offset = 438h) [reset = h]

Short Description: Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18

Long Description: Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18

Return to Summary Table

Table 4-3162. Instance Table

Instance Name	Physical Address
VIM	50F0 0438h

Figure 4-1486. INTMAP_1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3163. INTMAP_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to indicate which interrupt the corresponding event influences (if enabled) for event group M. Each bit corresponds to event Q where Q = Mx32+Bit 0 IRQ Interrupt (default)1 FIQ Interrupt

4.24.29 VIM_MSS_VIM_INTTYPE_1 Registers

4.24.29.1 VIM_1 Register (Offset = 43Ch) [reset = h]

Short Description: Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C

Long Description: Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C

Return to Summary Table

Table 4-3164. Instance Table

Instance Name	Physical Address
VIM	50F0 043Ch

Figure 4-1487. INTTYPE_1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VAL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL															
RW															
0															

Access Types Legend

Table 4-3165. INTTYPE_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	VAL	RW	0h	This field is used to indicate whether the source of an interrupt is a level (default) or a pulse for event group M. This is informational so that an ISR may query this register and know whether it has to clear a pulse event or a level event (see 3.4 Interrupt Handling). The value has no effect on how the VIM hardware functions. The input interrupts are agnostic as to whether they are pulse or level. Each bit corresponds to event Q where Q = Mx32+Bit0 Level (default)1 Pulse

4.24.30 VIM_MSS_VIM_RAW_2 Registers

4.24.30.1 VIM_2 Register (Offset = 440h) [reset = h]

Short Description: Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00

Long Description: Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00

Return to Summary Table

Table 4-3166. Instance Table

Instance Name	Physical Address
VIM	50F0 0440h

Figure 4-1488. RAW_2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STS															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STS															
RW															
0															

Access Types Legend

Table 4-3167. RAW_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RW	0h	This is the raw status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 InactiveRead 1 Active/ PendingWrite 0 No effectWrite 1 Set to Interrupt Raw Status

4.24.31 VIM_MSS_VIM_STS_2 Registers

4.24.31.1 VIM_2 Register (Offset = 444h) [reset = h]

Short Description: Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04

Long Description: Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04

Return to Summary Table

Table 4-3168. Instance Table

Instance Name	Physical Address
VIM	50F0 0444h

Figure 4-1489. STS_2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3169. STS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Inactive or DisabledRead 1 Active/Pending and EnabledWrite 0 No effectWrite 1 Clear Interrupt Raw Status

4.24.32 VIM_MSS_VIM_INTR_EN_SET_2 Registers

4.24.32.1 VIM_EN_SET_2 Register (Offset = 448h) [reset = h]

Short Description: Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08

Long Description: Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08

Return to Summary Table

Table 4-3170. Instance Table

Instance Name	Physical Address
VIM	50F0 0448h

Figure 4-1490. INTR_EN_SET_2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3171. INTR_EN_SET_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to enable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Set Enable

4.24.33 VIM_MSS_VIM_INTER_EN_CLR_2 Registers

4.24.33.1 VIM_EN_CLR_2 Register (Offset = 44Ch) [reset = h]

Short Description: Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C

Long Description: Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C

Return to Summary Table

Table 4-3172. Instance Table

Instance Name	Physical Address
VIM	50F0 044Ch

Figure 4-1491. INTER_EN_CLR_2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3173. INTER_EN_CLR_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to disable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Clear Enable

4.24.34 VIM_MSS_VIM_IRQSTS_2 Registers

4.24.34.1 VIM_2 Register (Offset = 450h) [reset = h]

Short Description: Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10

Long Description: Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10

Return to Summary Table

Table 4-3174. Instance Table

Instance Name	Physical Address
VIM	50F0 0450h

Figure 4-1492. IRQSTS_2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3175. IRQSTS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to IRQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an IRQRead 1 Active/Pending, Enabled, and IRQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if IRQ)

4.24.35 VIM_MSS_VIM_FIQSTS_2 Registers

4.24.35.1 VIM_2 Register (Offset = 454h) [reset = h]

Short Description: Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14

Long Description: Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14

Return to Summary Table

Table 4-3176. Instance Table

Instance Name	Physical Address
VIM	50F0 0454h

Figure 4-1493. FIQSTS_2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3177. FIQSTS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to FIQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an FIQRead 1 Active/Pending, Enabled, and FIQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if FIQ)

4.24.36 VIM_MSS_VIM_INTMAP_2 Registers

4.24.36.1 VIM_2 Register (Offset = 458h) [reset = h]

Short Description: Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18

Long Description: Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18

Return to Summary Table

Table 4-3178. Instance Table

Instance Name	Physical Address
VIM	50F0 0458h

Figure 4-1494. INTMAP_2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3179. INTMAP_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to indicate which interrupt the corresponding event influences (if enabled) for event group M. Each bit corresponds to event Q where Q = Mx32+Bit 0 IRQ Interrupt (default)1 FIQ Interrupt

4.24.37 VIM_MSS_VIM_INTTYPE_2 Registers

4.24.37.1 VIM_2 Register (Offset = 45Ch) [reset = h]

Short Description: Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C

Long Description: Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C

Return to Summary Table

Table 4-3180. Instance Table

Instance Name	Physical Address
VIM	50F0 045Ch

Figure 4-1495. INTTYPE_2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VAL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL															
RW															
0															

Access Types Legend

Table 4-3181. INTTYPE_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	VAL	RW	0h	This field is used to indicate whether the source of an interrupt is a level (default) or a pulse for event group M. This is informational so that an ISR may query this register and know whether it has to clear a pulse event or a level event (see 3.4 Interrupt Handling). The value has no effect on how the VIM hardware functions. The input interrupts are agnostic as to whether they are pulse or level. Each bit corresponds to event Q where Q = Mx32+Bit0 Level (default)1 Pulse

4.24.38 VIM_MSS_VIM_RAW_3 Registers

4.24.38.1 VIM_3 Register (Offset = 460h) [reset = h]

Short Description: Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00

Long Description: Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00

Return to Summary Table

Table 4-3182. Instance Table

Instance Name	Physical Address
VIM	50F0 0460h

Figure 4-1496. RAW_3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STS															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STS															
RW															
0															

Access Types Legend

Table 4-3183. RAW_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RW	0h	This is the raw status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 InactiveRead 1 Active/ PendingWrite 0 No effectWrite 1 Set to Interrupt Raw Status

4.24.39 VIM_MSS_VIM_STS_3 Registers

4.24.39.1 VIM_3 Register (Offset = 464h) [reset = h]

Short Description: Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04

Long Description: Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04

Return to Summary Table

Table 4-3184. Instance Table

Instance Name	Physical Address
VIM	50F0 0464h

Figure 4-1497. STS_3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3185. STS_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Inactive or DisabledRead 1 Active/Pending and EnabledWrite 0 No effectWrite 1 Clear Interrupt Raw Status

4.24.40 VIM_MSS_VIM_INTR_EN_SET_3 Registers

4.24.40.1 VIM_EN_SET_3 Register (Offset = 468h) [reset = h]

Short Description: Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08

Long Description: Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08

Return to Summary Table

Table 4-3186. Instance Table

Instance Name	Physical Address
VIM	50F0 0468h

Figure 4-1498. INTR_EN_SET_3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3187. INTR_EN_SET_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to enable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Set Enable

4.24.41 VIM_MSS_VIM_INTER_EN_CLR_3 Registers

4.24.41.1 VIM_EN_CLR_3 Register (Offset = 46Ch) [reset = h]

Short Description: Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C

Long Description: Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C

Return to Summary Table

Table 4-3188. Instance Table

Instance Name	Physical Address
VIM	50F0 046Ch

Figure 4-1499. INTER_EN_CLR_3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3189. INTER_EN_CLR_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to disable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Clear Enable

4.24.42 VIM_MSS_VIM_IRQSTS_3 Registers

4.24.42.1 VIM_3 Register (Offset = 470h) [reset = h]

Short Description: Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10

Long Description: Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10

Return to Summary Table

Table 4-3190. Instance Table

Instance Name	Physical Address
VIM	50F0 0470h

Figure 4-1500. IRQSTS_3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3191. IRQSTS_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to IRQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an IRQRead 1 Active/Pending, Enabled, and IRQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if IRQ)

4.24.43 VIM_MSS_VIM_FIQSTS_3 Registers

4.24.43.1 VIM_3 Register (Offset = 474h) [reset = h]

Short Description: Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14

Long Description: Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14

Return to Summary Table

Table 4-3192. Instance Table

Instance Name	Physical Address
VIM	50F0 0474h

Figure 4-1501. FIQSTS_3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3193. FIQSTS_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to FIQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an FIQRead 1 Active/Pending, Enabled, and FIQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if FIQ)

4.24.44 VIM_MSS_VIM_INTMAP_3 Registers

4.24.44.1 VIM_3 Register (Offset = 478h) [reset = h]

Short Description: Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18

Long Description: Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18

Return to Summary Table

Table 4-3194. Instance Table

Instance Name	Physical Address
VIM	50F0 0478h

Figure 4-1502. INTMAP_3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3195. INTMAP_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to indicate which interrupt the corresponding event influences (if enabled) for event group M. Each bit corresponds to event Q where Q = Mx32+Bit 0 IRQ Interrupt (default)1 FIQ Interrupt

4.24.45 VIM_MSS_VIM_INTTYPE_3 Registers

4.24.45.1 VIM_3 Register (Offset = 47Ch) [reset = h]

Short Description: Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C

Long Description: Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C

Return to Summary Table

Table 4-3196. Instance Table

Instance Name	Physical Address
VIM	50F0 047Ch

Figure 4-1503. INTTYPE_3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VAL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL															
RW															
0															

Access Types Legend

Table 4-3197. INTTYPE_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	VAL	RW	0h	This field is used to indicate whether the source of an interrupt is a level (default) or a pulse for event group M. This is informational so that an ISR may query this register and know whether it has to clear a pulse event or a level event (see 3.4 Interrupt Handling). The value has no effect on how the VIM hardware functions. The input interrupts are agnostic as to whether they are pulse or level. Each bit corresponds to event Q where Q = Mx32+Bit0 Level (default)1 Pulse

4.24.46 VIM_MSS_VIM_RAW_4 Registers

4.24.46.1 VIM_4 Register (Offset = 480h) [reset = h]

Short Description: Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00

Long Description: Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00

Return to Summary Table

Table 4-3198. Instance Table

Instance Name	Physical Address
VIM	50F0 0480h

Figure 4-1504. RAW_4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STS															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STS															
RW															
0															

Access Types Legend

Table 4-3199. RAW_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RW	0h	This is the raw status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 InactiveRead 1 Active/ PendingWrite 0 No effectWrite 1 Set to Interrupt Raw Status

4.24.47 VIM_MSS_VIM_STS_4 Registers

4.24.47.1 VIM_4 Register (Offset = 484h) [reset = h]

Short Description: Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04

Long Description: Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04

Return to Summary Table

Table 4-3200. Instance Table

Instance Name	Physical Address
VIM	50F0 0484h

Figure 4-1505. STS_4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3201. STS_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Inactive or DisabledRead 1 Active/Pending and EnabledWrite 0 No effectWrite 1 Clear Interrupt Raw Status

4.24.48 VIM_MSS_VIM_INTR_EN_SET_4 Registers

4.24.48.1 VIM_EN_SET_4 Register (Offset = 488h) [reset = h]

Short Description: Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08

Long Description: Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08

Return to Summary Table

Table 4-3202. Instance Table

Instance Name	Physical Address
VIM	50F0 0488h

Figure 4-1506. INTR_EN_SET_4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3203. INTR_EN_SET_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to enable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Set Enable

4.24.49 VIM_MSS_VIM_INTER_EN_CLR_4 Registers

4.24.49.1 VIM_EN_CLR_4 Register (Offset = 48Ch) [reset = h]

Short Description: Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C

Long Description: Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C

Return to Summary Table

Table 4-3204. Instance Table

Instance Name	Physical Address
VIM	50F0 048Ch

Figure 4-1507. INTER_EN_CLR_4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3205. INTER_EN_CLR_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to disable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Clear Enable

4.24.50 VIM_MSS_VIM_IRQSTS_4 Registers

4.24.50.1 VIM_4 Register (Offset = 490h) [reset = h]

Short Description: Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10

Long Description: Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10

Return to Summary Table

Table 4-3206. Instance Table

Instance Name	Physical Address
VIM	50F0 0490h

Figure 4-1508. IRQSTS_4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3207. IRQSTS_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to IRQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an IRQRead 1 Active/Pending, Enabled, and IRQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if IRQ)

4.24.51 VIM_MSS_VIM_FIQSTS_4 Registers

4.24.51.1 VIM_4 Register (Offset = 494h) [reset = h]

Short Description: Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14

Long Description: Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14

Return to Summary Table

Table 4-3208. Instance Table

Instance Name	Physical Address
VIM	50F0 0494h

Figure 4-1509. FIQSTS_4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3209. FIQSTS_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to FIQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an FIQRead 1 Active/Pending, Enabled, and FIQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if FIQ)

4.24.52 VIM_MSS_VIM_INTMAP_4 Registers

4.24.52.1 VIM_4 Register (Offset = 498h) [reset = h]

Short Description: Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18

Long Description: Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18

Return to Summary Table

Table 4-3210. Instance Table

Instance Name	Physical Address
VIM	50F0 0498h

Figure 4-1510. INTMAP_4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3211. INTMAP_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to indicate which interrupt the corresponding event influences (if enabled) for event group M. Each bit corresponds to event Q where Q = Mx32+Bit 0 IRQ Interrupt (default)1 FIQ Interrupt

4.24.53 VIM_MSS_VIM_INTTYPE_4 Registers

4.24.53.1 VIM_4 Register (Offset = 49Ch) [reset = h]

Short Description: Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C

Long Description: Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C

Return to Summary Table

Table 4-3212. Instance Table

Instance Name	Physical Address
VIM	50F0 049Ch

Figure 4-1511. INTTYPE_4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VAL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL															
RW															
0															

Access Types Legend

Table 4-3213. INTTYPE_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	VAL	RW	0h	This field is used to indicate whether the source of an interrupt is a level (default) or a pulse for event group M. This is informational so that an ISR may query this register and know whether it has to clear a pulse event or a level event (see 3.4 Interrupt Handling). The value has no effect on how the VIM hardware functions. The input interrupts are agnostic as to whether they are pulse or level. Each bit corresponds to event Q where Q = Mx32+Bit0 Level (default)1 Pulse

4.24.54 VIM_MSS_VIM_RAW_5 Registers

4.24.54.1 VIM_5 Register (Offset = 4A0h) [reset = h]

Short Description: Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00

Long Description: Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00

Return to Summary Table

Table 4-3214. Instance Table

Instance Name	Physical Address
VIM	50F0 04A0h

Figure 4-1512. RAW_5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STS															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STS															
RW															
0															

Access Types Legend

Table 4-3215. RAW_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RW	0h	This is the raw status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 InactiveRead 1 Active/ PendingWrite 0 No effectWrite 1 Set to Interrupt Raw Status

4.24.55 VIM_MSS_VIM_STS_5 Registers

4.24.55.1 VIM_5 Register (Offset = 4A4h) [reset = h]

Short Description: Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04

Long Description: Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04

Return to Summary Table

Table 4-3216. Instance Table

Instance Name	Physical Address
VIM	50F0 04A4h

Figure 4-1513. STS_5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3217. STS_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Inactive or DisabledRead 1 Active/Pending and EnabledWrite 0 No effectWrite 1 Clear Interrupt Raw Status

4.24.56 VIM_MSS_VIM_INTR_EN_SET_5 Registers

4.24.56.1 VIM_EN_SET_5 Register (Offset = 4A8h) [reset = h]

Short Description: Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08

Long Description: Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08

Return to Summary Table

Table 4-3218. Instance Table

Instance Name	Physical Address
VIM	50F0 04A8h

Figure 4-1514. INTR_EN_SET_5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3219. INTR_EN_SET_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to enable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Set Enable

4.24.57 VIM_MSS_VIM_INTER_EN_CLR_5 Registers

4.24.57.1 VIM_EN_CLR_5 Register (Offset = 4ACh) [reset = h]

Short Description: Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C

Long Description: Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C

Return to Summary Table

Table 4-3220. Instance Table

Instance Name	Physical Address
VIM	50F0 04ACh

Figure 4-1515. INTER_EN_CLR_5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3221. INTER_EN_CLR_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to disable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Clear Enable

4.24.58 VIM_MSS_VIM_IRQSTS_5 Registers

4.24.58.1 VIM_5 Register (Offset = 4B0h) [reset = h]

Short Description: Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10

Long Description: Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10

Return to Summary Table

Table 4-3222. Instance Table

Instance Name	Physical Address
VIM	50F0 04B0h

Figure 4-1516. IRQSTS_5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3223. IRQSTS_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to IRQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an IRQRead 1 Active/Pending, Enabled, and IRQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if IRQ)

4.24.59 VIM_MSS_VIM_FIQSTS_5 Registers

4.24.59.1 VIM_5 Register (Offset = 4B4h) [reset = h]

Short Description: Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14

Long Description: Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14

Return to Summary Table

Table 4-3224. Instance Table

Instance Name	Physical Address
VIM	50F0 04B4h

Figure 4-1517. FIQSTS_5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3225. FIQSTS_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to FIQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an FIQRead 1 Active/Pending, Enabled, and FIQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if FIQ)

4.24.60 VIM_MSS_VIM_INTMAP_5 Registers

4.24.60.1 VIM_5 Register (Offset = 4B8h) [reset = h]

Short Description: Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18

Long Description: Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18

Return to Summary Table

Table 4-3226. Instance Table

Instance Name	Physical Address
VIM	50F0 04B8h

Figure 4-1518. INTMAP_5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3227. INTMAP_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to indicate which interrupt the corresponding event influences (if enabled) for event group M. Each bit corresponds to event Q where Q = Mx32+Bit 0 IRQ Interrupt (default)1 FIQ Interrupt

4.24.61 VIM_MSS_VIM_INTTYPE_5 Registers

4.24.61.1 VIM_5 Register (Offset = 4BCh) [reset = h]

Short Description: Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C

Long Description: Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C

Return to Summary Table

Table 4-3228. Instance Table

Instance Name	Physical Address
VIM	50F0 04BCh

Figure 4-1519. INTTYPE_5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VAL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL															
RW															
0															

Access Types Legend

Table 4-3229. INTTYPE_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	VAL	RW	0h	This field is used to indicate whether the source of an interrupt is a level (default) or a pulse for event group M. This is informational so that an ISR may query this register and know whether it has to clear a pulse event or a level event (see 3.4 Interrupt Handling). The value has no effect on how the VIM hardware functions. The input interrupts are agnostic as to whether they are pulse or level. Each bit corresponds to event Q where Q = Mx32+Bit0 Level (default)1 Pulse

4.24.62 VIM_MSS_VIM_RAW_6 Registers

4.24.62.1 VIM_6 Register (Offset = 4C0h) [reset = h]

Short Description: Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00

Long Description: Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00

Return to Summary Table

Table 4-3230. Instance Table

Instance Name	Physical Address
VIM	50F0 04C0h

Figure 4-1520. RAW_6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STS															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STS															
RW															
0															

Access Types Legend

Table 4-3231. RAW_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RW	0h	This is the raw status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 InactiveRead 1 Active/ PendingWrite 0 No effectWrite 1 Set to Interrupt Raw Status

4.24.63 VIM_MSS_VIM_STS_6 Registers

4.24.63.1 VIM_6 Register (Offset = 4C4h) [reset = h]

Short Description: Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04

Long Description: Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04

Return to Summary Table

Table 4-3232. Instance Table

Instance Name	Physical Address
VIM	50F0 04C4h

Figure 4-1521. STS_6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3233. STS_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Inactive or DisabledRead 1 Active/Pending and EnabledWrite 0 No effectWrite 1 Clear Interrupt Raw Status

4.24.64 VIM_MSS_VIM_INTR_EN_SET_6 Registers

4.24.64.1 VIM_EN_SET_6 Register (Offset = 4C8h) [reset = h]

Short Description: Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08

Long Description: Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08

Return to Summary Table

Table 4-3234. Instance Table

Instance Name	Physical Address
VIM	50F0 04C8h

Figure 4-1522. INTR_EN_SET_6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3235. INTR_EN_SET_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to enable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Set Enable

4.24.65 VIM_MSS_VIM_INTER_EN_CLR_6 Registers

4.24.65.1 VIM_EN_CLR_6 Register (Offset = 4CCh) [reset = h]

Short Description: Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C

Long Description: Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C

Return to Summary Table

Table 4-3236. Instance Table

Instance Name	Physical Address
VIM	50F0 04CCh

Figure 4-1523. INTER_EN_CLR_6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3237. INTER_EN_CLR_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to disable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Clear Enable

4.24.66 VIM_MSS_VIM_IRQSTS_6 Registers

4.24.66.1 VIM_6 Register (Offset = 4D0h) [reset = h]

Short Description: Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10

Long Description: Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10

Return to Summary Table

Table 4-3238. Instance Table

Instance Name	Physical Address
VIM	50F0 04D0h

Figure 4-1524. IRQSTS_6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3239. IRQSTS_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to IRQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an IRQRead 1 Active/Pending, Enabled, and IRQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if IRQ)

4.24.67 VIM_MSS_VIM_FIQSTS_6 Registers

4.24.67.1 VIM_6 Register (Offset = 4D4h) [reset = h]

Short Description: Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14

Long Description: Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14

Return to Summary Table

Table 4-3240. Instance Table

Instance Name	Physical Address
VIM	50F0 04D4h

Figure 4-1525. FIQSTS_6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3241. FIQSTS_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to FIQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an FIQRead 1 Active/Pending, Enabled, and FIQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if FIQ)

4.24.68 VIM_MSS_VIM_INTMAP_6 Registers

4.24.68.1 VIM_6 Register (Offset = 4D8h) [reset = h]

Short Description: Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18

Long Description: Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18

Return to Summary Table

Table 4-3242. Instance Table

Instance Name	Physical Address
VIM	50F0 04D8h

Figure 4-1526. INTMAP_6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3243. INTMAP_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to indicate which interrupt the corresponding event influences (if enabled) for event group M. Each bit corresponds to event Q where Q = Mx32+Bit 0 IRQ Interrupt (default)1 FIQ Interrupt

4.24.69 VIM_MSS_VIM_INTTYPE_6 Registers

4.24.69.1 VIM_6 Register (Offset = 4DCh) [reset = h]

Short Description: Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C

Long Description: Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C

Return to Summary Table

Table 4-3244. Instance Table

Instance Name	Physical Address
VIM	50F0 04DCh

Figure 4-1527. INTTYPE_6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VAL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL															
RW															
0															

Access Types Legend

Table 4-3245. INTTYPE_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	VAL	RW	0h	This field is used to indicate whether the source of an interrupt is a level (default) or a pulse for event group M. This is informational so that an ISR may query this register and know whether it has to clear a pulse event or a level event (see 3.4 Interrupt Handling). The value has no effect on how the VIM hardware functions. The input interrupts are agnostic as to whether they are pulse or level. Each bit corresponds to event Q where Q = Mx32+Bit0 Level (default)1 Pulse

4.24.70 VIM_MSS_VIM_RAW_7 Registers

4.24.70.1 VIM_7 Register (Offset = 4E0h) [reset = h]

Short Description: Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00

Long Description: Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00

Return to Summary Table

Table 4-3246. Instance Table

Instance Name	Physical Address
VIM	50F0 04E0h

Figure 4-1528. RAW_7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STS															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STS															
RW															
0															

Access Types Legend

Table 4-3247. RAW_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RW	0h	This is the raw status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 InactiveRead 1 Active/ PendingWrite 0 No effectWrite 1 Set to Interrupt Raw Status

4.24.71 VIM_MSS_VIM_STS_7 Registers

4.24.71.1 VIM_7 Register (Offset = 4E4h) [reset = h]

Short Description: Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04

Long Description: Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04

Return to Summary Table

Table 4-3248. Instance Table

Instance Name	Physical Address
VIM	50F0 04E4h

Figure 4-1529. STS_7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3249. STS_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Inactive or DisabledRead 1 Active/Pending and EnabledWrite 0 No effectWrite 1 Clear Interrupt Raw Status

4.24.72 VIM_MSS_VIM_INTR_EN_SET_7 Registers

4.24.72.1 VIM_EN_SET_7 Register (Offset = 4E8h) [reset = h]

Short Description: Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08

Long Description: Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08

Return to Summary Table

Table 4-3250. Instance Table

Instance Name	Physical Address
VIM	50F0 04E8h

Figure 4-1530. INTR_EN_SET_7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3251. INTR_EN_SET_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to enable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Set Enable

4.24.73 VIM_MSS_VIM_INTER_EN_CLR_7 Registers

4.24.73.1 VIM_EN_CLR_7 Register (Offset = 4ECh) [reset = h]

Short Description: Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C

Long Description: Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C

Return to Summary Table

Table 4-3252. Instance Table

Instance Name	Physical Address
VIM	50F0 04ECh

Figure 4-1531. INTER_EN_CLR_7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3253. INTER_EN_CLR_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to disable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Clear Enable

4.24.74 VIM_MSS_VIM_IRQSTS_7 Registers

4.24.74.1 VIM_7 Register (Offset = 4F0h) [reset = h]

Short Description: Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10

Long Description: Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10

Return to Summary Table

Table 4-3254. Instance Table

Instance Name	Physical Address
VIM	50F0 04F0h

Figure 4-1532. IRQSTS_7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3255. IRQSTS_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to IRQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an IRQRead 1 Active/Pending, Enabled, and IRQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if IRQ)

4.24.75 VIM_MSS_VIM_FIQSTS_7 Registers

4.24.75.1 VIM_7 Register (Offset = 4F4h) [reset = h]

Short Description: Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14

Long Description: Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14

Return to Summary Table

Table 4-3256. Instance Table

Instance Name	Physical Address
VIM	50F0 04F4h

Figure 4-1533. FIQSTS_7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3257. FIQSTS_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to FIQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an FIQRead 1 Active/Pending, Enabled, and FIQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if FIQ)

4.24.76 VIM_MSS_VIM_INTMAP_7 Registers

4.24.76.1 VIM_7 Register (Offset = 4F8h) [reset = h]

Short Description: Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18

Long Description: Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18

Return to Summary Table

Table 4-3258. Instance Table

Instance Name	Physical Address
VIM	50F0 04F8h

Figure 4-1534. INTMAP_7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3259. INTMAP_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to indicate which interrupt the corresponding event influences (if enabled) for event group M. Each bit corresponds to event Q where Q = Mx32+Bit 0 IRQ Interrupt (default)1 FIQ Interrupt

4.24.77 VIM_MSS_VIM_INTTYPE_7 Registers

4.24.77.1 VIM_7 Register (Offset = 4FCh) [reset = h]

Short Description: Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C

Long Description: Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C

Return to Summary Table

Table 4-3260. Instance Table

Instance Name	Physical Address
VIM	50F0 04FCh

Figure 4-1535. INTTYPE_7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VAL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL															
RW															
0															

Access Types Legend

Table 4-3261. INTTYPE_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	VAL	RW	0h	This field is used to indicate whether the source of an interrupt is a level (default) or a pulse for event group M. This is informational so that an ISR may query this register and know whether it has to clear a pulse event or a level event (see 3.4 Interrupt Handling). The value has no effect on how the VIM hardware functions. The input interrupts are agnostic as to whether they are pulse or level. Each bit corresponds to event Q where Q = Mx32+Bit0 Level (default)1 Pulse

4.24.78 VIM_MSS_VIM_INTPRIORITY Registers

4.24.78.1 VIM_INTPRIORITY Register (Offset = 1000h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h4

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h4

Return to Summary Table

Table 4-3262. Instance Table

Instance Name	Physical Address
VIM	50F0 1000h

Figure 4-1536. INTPRIORITY Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3263. INTPRIORITY Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.79 VIM_MSS_VIM_INTPRIORITY_1 Registers

4.24.79.1 VIM_1 Register (Offset = 1004h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h5

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h5

Return to Summary Table

Table 4-3264. Instance Table

Instance Name	Physical Address
VIM	50F0 1004h

Figure 4-1537. INTPRIORITY_1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3265. INTPRIORITY_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.80 VIM_MSS_VIM_INTPRIORITY_2 Registers

4.24.80.1 VIM_2 Register (Offset = 1008h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h6

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h6

Return to Summary Table

Table 4-3266. Instance Table

Instance Name	Physical Address
VIM	50F0 1008h

Figure 4-1538. INTPRIORITY_2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3267. INTPRIORITY_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.81 VIM_MSS_VIM_INTPRIORITY_3 Registers

4.24.81.1 VIM_3 Register (Offset = 100Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h7

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h7

Return to Summary Table

Table 4-3268. Instance Table

Instance Name	Physical Address
VIM	50F0 100Ch

Figure 4-1539. INTPRIORITY_3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3269. INTPRIORITY_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.82 VIM_MSS_VIM_INTPRIORITY_4 Registers

4.24.82.1 VIM_4 Register (Offset = 1010h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h8

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h8

Return to Summary Table

Table 4-3270. Instance Table

Instance Name	Physical Address
VIM	50F0 1010h

Figure 4-1540. INTPRIORITY_4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3271. INTPRIORITY_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.83 VIM_MSS_VIM_INTPRIORITY_5 Registers

4.24.83.1 VIM_5 Register (Offset = 1014h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h9

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h9

Return to Summary Table

Table 4-3272. Instance Table

Instance Name	Physical Address
VIM	50F0 1014h

Figure 4-1541. INTPRIORITY_5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3273. INTPRIORITY_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.84 VIM_MSS_VIM_INTPRIORITY_6 Registers

4.24.84.1 VIM_6 Register (Offset = 1018h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h10

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h10

Return to Summary Table

Table 4-3274. Instance Table

Instance Name	Physical Address
VIM	50F0 1018h

Figure 4-1542. INTPRIORITY_6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3275. INTPRIORITY_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.85 VIM_MSS_VIM_INTPRIORITY_7 Registers

4.24.85.1 VIM_7 Register (Offset = 101Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h11

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h11

Return to Summary Table

Table 4-3276. Instance Table

Instance Name	Physical Address
VIM	50F0 101Ch

Figure 4-1543. INTPRIORITY_7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3277. INTPRIORITY_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.86 VIM_MSS_VIM_INTPRIORITY_8 Registers

4.24.86.1 VIM_8 Register (Offset = 1020h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h12

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h12

Return to Summary Table

Table 4-3278. Instance Table

Instance Name	Physical Address
VIM	50F0 1020h

Figure 4-1544. INTPRIORITY_8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3279. INTPRIORITY_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.87 VIM_MSS_VIM_INTPRIORITY_9 Registers

4.24.87.1 VIM_9 Register (Offset = 1024h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h13

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h13

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Table 4-3280. Instance Table

Instance Name	Physical Address
VIM	50F0 1024h

Figure 4-1545. INTPRIORITY_9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3281. INTPRIORITY_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.88 VIM_MSS_VIM_INTPRIORITY_10 Registers

4.24.88.1 VIM_10 Register (Offset = 1028h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h14

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h14

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Table 4-3282. Instance Table

Instance Name	Physical Address
VIM	50F0 1028h

Figure 4-1546. INTPRIORITY_10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3283. INTPRIORITY_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.89 VIM_MSS_VIM_INTPRIORITY_11 Registers

4.24.89.1 VIM_11 Register (Offset = 102Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h15

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h15

Return to Summary Table

Table 4-3284. Instance Table

Instance Name	Physical Address
VIM	50F0 102Ch

Figure 4-1547. INTPRIORITY_11 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3285. INTPRIORITY_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.90 VIM_MSS_VIM_INTPRIORITY_12 Registers

4.24.90.1 VIM_12 Register (Offset = 1030h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h16

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h16

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Table 4-3286. Instance Table

Instance Name	Physical Address
VIM	50F0 1030h

Figure 4-1548. INTPRIORITY_12 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3287. INTPRIORITY_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.91 VIM_MSS_VIM_INTPRIORITY_13 Registers

4.24.91.1 VIM_13 Register (Offset = 1034h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h17

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h17

Return to Summary Table

Table 4-3288. Instance Table

Instance Name	Physical Address
VIM	50F0 1034h

Figure 4-1549. INTPRIORITY_13 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3289. INTPRIORITY_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.92 VIM_MSS_VIM_INTPRIORITY_14 Registers

4.24.92.1 VIM_14 Register (Offset = 1038h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h18

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h18

Return to Summary Table

Table 4-3290. Instance Table

Instance Name	Physical Address
VIM	50F0 1038h

Figure 4-1550. INTPRIORITY_14 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3291. INTPRIORITY_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.93 VIM_MSS_VIM_INTPRIORITY_15 Registers

4.24.93.1 VIM_15 Register (Offset = 103Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h19

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h19

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Table 4-3292. Instance Table

Instance Name	Physical Address
VIM	50F0 103Ch

Figure 4-1551. INTPRIORITY_15 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3293. INTPRIORITY_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.94 VIM_MSS_VIM_INTPRIORITY_16 Registers

4.24.94.1 VIM_16 Register (Offset = 1040h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h20

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h20

Return to Summary Table

Table 4-3294. Instance Table

Instance Name	Physical Address
VIM	50F0 1040h

Figure 4-1552. INTPRIORITY_16 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3295. INTPRIORITY_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.95 VIM_MSS_VIM_INTPRIORITY_17 Registers

4.24.95.1 VIM_17 Register (Offset = 1044h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h21

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h21

Return to Summary Table

Table 4-3296. Instance Table

Instance Name	Physical Address
VIM	50F0 1044h

Figure 4-1553. INTPRIORITY_17 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3297. INTPRIORITY_17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.96 VIM_MSS_VIM_INTPRIORITY_18 Registers

4.24.96.1 VIM_18 Register (Offset = 1048h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h22

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h22

Return to Summary Table

Table 4-3298. Instance Table

Instance Name	Physical Address
VIM	50F0 1048h

Figure 4-1554. INTPRIORITY_18 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3299. INTPRIORITY_18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.97 VIM_MSS_VIM_INTPRIORITY_19 Registers

4.24.97.1 VIM_19 Register (Offset = 104Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h23

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h23

Return to Summary Table

Table 4-3300. Instance Table

Instance Name	Physical Address
VIM	50F0 104Ch

Figure 4-1555. INTPRIORITY_19 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3301. INTPRIORITY_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.98 VIM_MSS_VIM_INTPRIORITY_20 Registers

4.24.98.1 VIM_20 Register (Offset = 1050h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h24

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h24

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Table 4-3302. Instance Table

Instance Name	Physical Address
VIM	50F0 1050h

Figure 4-1556. INTPRIORITY_20 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3303. INTPRIORITY_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.99 VIM_MSS_VIM_INTPRIORITY_21 Registers

4.24.99.1 VIM_21 Register (Offset = 1054h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h25

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h25

Return to Summary Table

Table 4-3304. Instance Table

Instance Name	Physical Address
VIM	50F0 1054h

Figure 4-1557. INTPRIORITY_21 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3305. INTPRIORITY_21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.100 VIM_MSS_VIM_INTPRIORITY_22 Registers

4.24.100.1 VIM_22 Register (Offset = 1058h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h26

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h26

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Table 4-3306. Instance Table

Instance Name	Physical Address
VIM	50F0 1058h

Figure 4-1558. INTPRIORITY_22 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3307. INTPRIORITY_22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.101 VIM_MSS_VIM_INTPRIORITY_23 Registers

4.24.101.1 VIM_23 Register (Offset = 105Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h27

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h27

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Table 4-3308. Instance Table

Instance Name	Physical Address
VIM	50F0 105Ch

Figure 4-1559. INTPRIORITY_23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3309. INTPRIORITY_23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.102 VIM_MSS_VIM_INTPRIORITY_24 Registers

4.24.102.1 VIM_24 Register (Offset = 1060h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h28

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h28

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Table 4-3310. Instance Table

Instance Name	Physical Address
VIM	50F0 1060h

Figure 4-1560. INTPRIORITY_24 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3311. INTPRIORITY_24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.103 VIM_MSS_VIM_INTPRIORITY_25 Registers

4.24.103.1 VIM_25 Register (Offset = 1064h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h29

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h29

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Table 4-3312. Instance Table

Instance Name	Physical Address
VIM	50F0 1064h

Figure 4-1561. INTPRIORITY_25 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3313. INTPRIORITY_25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.104 VIM_MSS_VIM_INTPRIORITY_26 Registers

4.24.104.1 VIM_26 Register (Offset = 1068h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h30

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h30

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Table 4-3314. Instance Table

Instance Name	Physical Address
VIM	50F0 1068h

Figure 4-1562. INTPRIORITY_26 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3315. INTPRIORITY_26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.105 VIM_MSS_VIM_INTPRIORITY_27 Registers

4.24.105.1 VIM_27 Register (Offset = 106Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h31

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h31

Return to Summary Table

Table 4-3316. Instance Table

Instance Name	Physical Address
VIM	50F0 106Ch

Figure 4-1563. INTPRIORITY_27 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3317. INTPRIORITY_27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.106 VIM_MSS_VIM_INTPRIORITY_28 Registers

4.24.106.1 VIM_28 Register (Offset = 1070h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h32

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h32

Return to Summary Table

Table 4-3318. Instance Table

Instance Name	Physical Address
VIM	50F0 1070h

Figure 4-1564. INTPRIORITY_28 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3319. INTPRIORITY_28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.107 VIM_MSS_VIM_INTPRIORITY_29 Registers

4.24.107.1 VIM_29 Register (Offset = 1074h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h33

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h33

Return to Summary Table

Table 4-3320. Instance Table

Instance Name	Physical Address
VIM	50F0 1074h

Figure 4-1565. INTPRIORITY_29 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3321. INTPRIORITY_29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.108 VIM_MSS_VIM_INTPRIORITY_30 Registers

4.24.108.1 VIM_30 Register (Offset = 1078h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h34

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h34

Return to Summary Table

Table 4-3322. Instance Table

Instance Name	Physical Address
VIM	50F0 1078h

Figure 4-1566. INTPRIORITY_30 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3323. INTPRIORITY_30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.109 VIM_MSS_VIM_INTPRIORITY_31 Registers

4.24.109.1 VIM_31 Register (Offset = 107Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h35

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h35

Return to Summary Table

Table 4-3324. Instance Table

Instance Name	Physical Address
VIM	50F0 107Ch

Figure 4-1567. INTPRIORITY_31 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3325. INTPRIORITY_31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.110 VIM_MSS_VIM_INTPRIORITY_32 Registers

4.24.110.1 VIM_32 Register (Offset = 1080h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h36

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h36

Return to Summary Table

Table 4-3326. Instance Table

Instance Name	Physical Address
VIM	50F0 1080h

Figure 4-1568. INTPRIORITY_32 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3327. INTPRIORITY_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.111 VIM_MSS_VIM_INTPRIORITY_33 Registers

4.24.111.1 VIM_33 Register (Offset = 1084h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h37

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h37

Return to Summary Table

Table 4-3328. Instance Table

Instance Name	Physical Address
VIM	50F0 1084h

Figure 4-1569. INTPRIORITY_33 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3329. INTPRIORITY_33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.112 VIM_MSS_VIM_INTPRIORITY_34 Registers

4.24.112.1 VIM_34 Register (Offset = 1088h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h38

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h38

Return to Summary Table

Table 4-3330. Instance Table

Instance Name	Physical Address
VIM	50F0 1088h

Figure 4-1570. INTPRIORITY_34 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3331. INTPRIORITY_34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.113 VIM_MSS_VIM_INTPRIORITY_35 Registers

4.24.113.1 VIM_35 Register (Offset = 108Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h39

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h39

Return to Summary Table

Table 4-3332. Instance Table

Instance Name	Physical Address
VIM	50F0 108Ch

Figure 4-1571. INTPRIORITY_35 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3333. INTPRIORITY_35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.114 VIM_MSS_VIM_INTPRIORITY_36 Registers

4.24.114.1 VIM_36 Register (Offset = 1090h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h40

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h40

Return to Summary Table

Table 4-3334. Instance Table

Instance Name	Physical Address
VIM	50F0 1090h

Figure 4-1572. INTPRIORITY_36 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3335. INTPRIORITY_36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.115 VIM_MSS_VIM_INTPRIORITY_37 Registers

4.24.115.1 VIM_37 Register (Offset = 1094h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h41

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h41

Return to Summary Table

Table 4-3336. Instance Table

Instance Name	Physical Address
VIM	50F0 1094h

Figure 4-1573. INTPRIORITY_37 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3337. INTPRIORITY_37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.116 VIM_MSS_VIM_INTPRIORITY_38 Registers

4.24.116.1 VIM_38 Register (Offset = 1098h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h42

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h42

Return to Summary Table

Table 4-3338. Instance Table

Instance Name	Physical Address
VIM	50F0 1098h

Figure 4-1574. INTPRIORITY_38 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3339. INTPRIORITY_38 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.117 VIM_MSS_VIM_INTPRIORITY_39 Registers

4.24.117.1 VIM_39 Register (Offset = 109Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h43

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h43

Return to Summary Table

Table 4-3340. Instance Table

Instance Name	Physical Address
VIM	50F0 109Ch

Figure 4-1575. INTPRIORITY_39 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3341. INTPRIORITY_39 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.118 VIM_MSS_VIM_INTPRIORITY_40 Registers

4.24.118.1 VIM_40 Register (Offset = 10A0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h44

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h44

Return to Summary Table

Table 4-3342. Instance Table

Instance Name	Physical Address
VIM	50F0 10A0h

Figure 4-1576. INTPRIORITY_40 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3343. INTPRIORITY_40 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.119 VIM_MSS_VIM_INTPRIORITY_41 Registers

4.24.119.1 VIM_41 Register (Offset = 10A4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h45

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h45

Return to Summary Table

Table 4-3344. Instance Table

Instance Name	Physical Address
VIM	50F0 10A4h

Figure 4-1577. INTPRIORITY_41 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3345. INTPRIORITY_41 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.120 VIM_MSS_VIM_INTPRIORITY_42 Registers

4.24.120.1 VIM_42 Register (Offset = 10A8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h46

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h46

Return to Summary Table

Table 4-3346. Instance Table

Instance Name	Physical Address
VIM	50F0 10A8h

Figure 4-1578. INTPRIORITY_42 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3347. INTPRIORITY_42 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.121 VIM_MSS_VIM_INTPRIORITY_43 Registers

4.24.121.1 VIM_43 Register (Offset = 10ACh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h47

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h47

Return to Summary Table

Table 4-3348. Instance Table

Instance Name	Physical Address
VIM	50F0 10ACh

Figure 4-1579. INTPRIORITY_43 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3349. INTPRIORITY_43 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.122 VIM_MSS_VIM_INTPRIORITY_44 Registers

4.24.122.1 VIM_44 Register (Offset = 10B0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h48

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h48

Return to Summary Table

Table 4-3350. Instance Table

Instance Name	Physical Address
VIM	50F0 10B0h

Figure 4-1580. INTPRIORITY_44 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3351. INTPRIORITY_44 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.123 VIM_MSS_VIM_INTPRIORITY_45 Registers

4.24.123.1 VIM_45 Register (Offset = 10B4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h49

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h49

Return to Summary Table

Table 4-3352. Instance Table

Instance Name	Physical Address
VIM	50F0 10B4h

Figure 4-1581. INTPRIORITY_45 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3353. INTPRIORITY_45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.124 VIM_MSS_VIM_INTPRIORITY_46 Registers

4.24.124.1 VIM_46 Register (Offset = 10B8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h50

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h50

Return to Summary Table

Table 4-3354. Instance Table

Instance Name	Physical Address
VIM	50F0 10B8h

Figure 4-1582. INTPRIORITY_46 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3355. INTPRIORITY_46 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.125 VIM_MSS_VIM_INTPRIORITY_47 Registers

4.24.125.1 VIM_47 Register (Offset = 10BCh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h51

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h51

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Table 4-3356. Instance Table

Instance Name	Physical Address
VIM	50F0 10BCh

Figure 4-1583. INTPRIORITY_47 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3357. INTPRIORITY_47 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.126 VIM_MSS_VIM_INTPRIORITY_48 Registers

4.24.126.1 VIM_48 Register (Offset = 10C0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h52

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h52

Return to Summary Table

Table 4-3358. Instance Table

Instance Name	Physical Address
VIM	50F0 10C0h

Figure 4-1584. INTPRIORITY_48 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3359. INTPRIORITY_48 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.127 VIM_MSS_VIM_INTPRIORITY_49 Registers

4.24.127.1 VIM_49 Register (Offset = 10C4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h53

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h53

Return to Summary Table

Table 4-3360. Instance Table

Instance Name	Physical Address
VIM	50F0 10C4h

Figure 4-1585. INTPRIORITY_49 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3361. INTPRIORITY_49 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.128 VIM_MSS_VIM_INTPRIORITY_50 Registers

4.24.128.1 VIM_50 Register (Offset = 10C8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h54

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h54

Return to Summary Table

Table 4-3362. Instance Table

Instance Name	Physical Address
VIM	50F0 10C8h

Figure 4-1586. INTPRIORITY_50 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3363. INTPRIORITY_50 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.129 VIM_MSS_VIM_INTPRIORITY_51 Registers

4.24.129.1 VIM_51 Register (Offset = 10CCh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h55

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h55

Return to Summary Table

Table 4-3364. Instance Table

Instance Name	Physical Address
VIM	50F0 10CCh

Figure 4-1587. INTPRIORITY_51 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3365. INTPRIORITY_51 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.130 VIM_MSS_VIM_INTPRIORITY_52 Registers

4.24.130.1 VIM_52 Register (Offset = 10D0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h56

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h56

Return to Summary Table

Table 4-3366. Instance Table

Instance Name	Physical Address
VIM	50F0 10D0h

Figure 4-1588. INTPRIORITY_52 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3367. INTPRIORITY_52 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.131 VIM_MSS_VIM_INTPRIORITY_53 Registers

4.24.131.1 VIM_53 Register (Offset = 10D4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h57

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h57

Return to Summary Table

Table 4-3368. Instance Table

Instance Name	Physical Address
VIM	50F0 10D4h

Figure 4-1589. INTPRIORITY_53 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3369. INTPRIORITY_53 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.132 VIM_MSS_VIM_INTPRIORITY_54 Registers

4.24.132.1 VIM_54 Register (Offset = 10D8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h58

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h58

Return to Summary Table

Table 4-3370. Instance Table

Instance Name	Physical Address
VIM	50F0 10D8h

Figure 4-1590. INTPRIORITY_54 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3371. INTPRIORITY_54 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.133 VIM_MSS_VIM_INTPRIORITY_55 Registers

4.24.133.1 VIM_55 Register (Offset = 10DCh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h59

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h59

Return to Summary Table

Table 4-3372. Instance Table

Instance Name	Physical Address
VIM	50F0 10DCh

Figure 4-1591. INTPRIORITY_55 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3373. INTPRIORITY_55 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.134 VIM_MSS_VIM_INTPRIORITY_56 Registers

4.24.134.1 VIM_56 Register (Offset = 10E0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h60

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h60

Return to Summary Table

Table 4-3374. Instance Table

Instance Name	Physical Address
VIM	50F0 10E0h

Figure 4-1592. INTPRIORITY_56 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3375. INTPRIORITY_56 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.135 VIM_MSS_VIM_INTPRIORITY_57 Registers

4.24.135.1 VIM_57 Register (Offset = 10E4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h61

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h61

Return to Summary Table

Table 4-3376. Instance Table

Instance Name	Physical Address
VIM	50F0 10E4h

Figure 4-1593. INTPRIORITY_57 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3377. INTPRIORITY_57 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.136 VIM_MSS_VIM_INTPRIORITY_58 Registers

4.24.136.1 VIM_58 Register (Offset = 10E8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h62

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h62

Return to Summary Table

Table 4-3378. Instance Table

Instance Name	Physical Address
VIM	50F0 10E8h

Figure 4-1594. INTPRIORITY_58 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3379. INTPRIORITY_58 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.137 VIM_MSS_VIM_INTPRIORITY_59 Registers

4.24.137.1 VIM_59 Register (Offset = 10ECh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h63

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h63

Return to Summary Table

Table 4-3380. Instance Table

Instance Name	Physical Address
VIM	50F0 10ECh

Figure 4-1595. INTPRIORITY_59 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3381. INTPRIORITY_59 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.138 VIM_MSS_VIM_INTPRIORITY_60 Registers

4.24.138.1 VIM_60 Register (Offset = 10F0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h64

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h64

Return to Summary Table

Table 4-3382. Instance Table

Instance Name	Physical Address
VIM	50F0 10F0h

Figure 4-1596. INTPRIORITY_60 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3383. INTPRIORITY_60 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.139 VIM_MSS_VIM_INTPRIORITY_61 Registers

4.24.139.1 VIM_61 Register (Offset = 10F4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h65

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h65

Return to Summary Table

Table 4-3384. Instance Table

Instance Name	Physical Address
VIM	50F0 10F4h

Figure 4-1597. INTPRIORITY_61 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3385. INTPRIORITY_61 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.140 VIM_MSS_VIM_INTPRIORITY_62 Registers

4.24.140.1 VIM_62 Register (Offset = 10F8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h66

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h66

Return to Summary Table

Table 4-3386. Instance Table

Instance Name	Physical Address
VIM	50F0 10F8h

Figure 4-1598. INTPRIORITY_62 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3387. INTPRIORITY_62 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.141 VIM_MSS_VIM_INTPRIORITY_63 Registers

4.24.141.1 VIM_63 Register (Offset = 10FCh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h67

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h67

Return to Summary Table

Table 4-3388. Instance Table

Instance Name	Physical Address
VIM	50F0 10FCh

Figure 4-1599. INTPRIORITY_63 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3389. INTPRIORITY_63 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.142 VIM_MSS_VIM_INTPRIORITY_64 Registers

4.24.142.1 VIM_64 Register (Offset = 1100h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h68

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h68

Return to Summary Table

Table 4-3390. Instance Table

Instance Name	Physical Address
VIM	50F0 1100h

Figure 4-1600. INTPRIORITY_64 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3391. INTPRIORITY_64 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.143 VIM_MSS_VIM_INTPRIORITY_65 Registers

4.24.143.1 VIM_65 Register (Offset = 1104h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h69

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h69

Return to Summary Table

Table 4-3392. Instance Table

Instance Name	Physical Address
VIM	50F0 1104h

Figure 4-1601. INTPRIORITY_65 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3393. INTPRIORITY_65 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.144 VIM_MSS_VIM_INTPRIORITY_66 Registers

4.24.144.1 VIM_66 Register (Offset = 1108h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h70

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h70

Return to Summary Table

Table 4-3394. Instance Table

Instance Name	Physical Address
VIM	50F0 1108h

Figure 4-1602. INTPRIORITY_66 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3395. INTPRIORITY_66 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.145 VIM_MSS_VIM_INTPRIORITY_67 Registers

4.24.145.1 VIM_67 Register (Offset = 110Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h71

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h71

Return to Summary Table

Table 4-3396. Instance Table

Instance Name	Physical Address
VIM	50F0 110Ch

Figure 4-1603. INTPRIORITY_67 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3397. INTPRIORITY_67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.146 VIM_MSS_VIM_INTPRIORITY_68 Registers

4.24.146.1 VIM_68 Register (Offset = 1110h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h72

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h72

Return to Summary Table

Table 4-3398. Instance Table

Instance Name	Physical Address
VIM	50F0 1110h

Figure 4-1604. INTPRIORITY_68 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3399. INTPRIORITY_68 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.147 VIM_MSS_VIM_INTPRIORITY_69 Registers

4.24.147.1 VIM_69 Register (Offset = 1114h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h73

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h73

Return to Summary Table

Table 4-3400. Instance Table

Instance Name	Physical Address
VIM	50F0 1114h

Figure 4-1605. INTPRIORITY_69 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3401. INTPRIORITY_69 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.148 VIM_MSS_VIM_INTPRIORITY_70 Registers

4.24.148.1 VIM_70 Register (Offset = 1118h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h74

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h74

Return to Summary Table

Table 4-3402. Instance Table

Instance Name	Physical Address
VIM	50F0 1118h

Figure 4-1606. INTPRIORITY_70 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3403. INTPRIORITY_70 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.149 VIM_MSS_VIM_INTPRIORITY_71 Registers

4.24.149.1 VIM_71 Register (Offset = 111Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h75

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h75

Return to Summary Table

Table 4-3404. Instance Table

Instance Name	Physical Address
VIM	50F0 111Ch

Figure 4-1607. INTPRIORITY_71 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3405. INTPRIORITY_71 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.150 VIM_MSS_VIM_INTPRIORITY_72 Registers

4.24.150.1 VIM_72 Register (Offset = 1120h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h76

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h76

Return to Summary Table

Table 4-3406. Instance Table

Instance Name	Physical Address
VIM	50F0 1120h

Figure 4-1608. INTPRIORITY_72 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3407. INTPRIORITY_72 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.151 VIM_MSS_VIM_INTPRIORITY_73 Registers

4.24.151.1 VIM_73 Register (Offset = 1124h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h77

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h77

Return to Summary Table

Table 4-3408. Instance Table

Instance Name	Physical Address
VIM	50F0 1124h

Figure 4-1609. INTPRIORITY_73 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3409. INTPRIORITY_73 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.152 VIM_MSS_VIM_INTPRIORITY_74 Registers

4.24.152.1 VIM_74 Register (Offset = 1128h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h78

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h78

Return to Summary Table

Table 4-3410. Instance Table

Instance Name	Physical Address
VIM	50F0 1128h

Figure 4-1610. INTPRIORITY_74 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3411. INTPRIORITY_74 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.153 VIM_MSS_VIM_INTPRIORITY_75 Registers

4.24.153.1 VIM_75 Register (Offset = 112Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h79

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h79

Return to Summary Table

Table 4-3412. Instance Table

Instance Name	Physical Address
VIM	50F0 112Ch

Figure 4-1611. INTPRIORITY_75 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3413. INTPRIORITY_75 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.154 VIM_MSS_VIM_INTPRIORITY_76 Registers

4.24.154.1 VIM_76 Register (Offset = 1130h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h80

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h80

Return to Summary Table

Table 4-3414. Instance Table

Instance Name	Physical Address
VIM	50F0 1130h

Figure 4-1612. INTPRIORITY_76 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3415. INTPRIORITY_76 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.155 VIM_MSS_VIM_INTPRIORITY_77 Registers

4.24.155.1 VIM_77 Register (Offset = 1134h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h81

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h81

Return to Summary Table

Table 4-3416. Instance Table

Instance Name	Physical Address
VIM	50F0 1134h

Figure 4-1613. INTPRIORITY_77 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3417. INTPRIORITY_77 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.156 VIM_MSS_VIM_INTPRIORITY_78 Registers

4.24.156.1 VIM_78 Register (Offset = 1138h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h82

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h82

Return to Summary Table

Table 4-3418. Instance Table

Instance Name	Physical Address
VIM	50F0 1138h

Figure 4-1614. INTPRIORITY_78 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3419. INTPRIORITY_78 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.157 VIM_MSS_VIM_INTPRIORITY_79 Registers

4.24.157.1 VIM_79 Register (Offset = 113Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h83

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h83

Return to Summary Table

Table 4-3420. Instance Table

Instance Name	Physical Address
VIM	50F0 113Ch

Figure 4-1615. INTPRIORITY_79 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3421. INTPRIORITY_79 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.158 VIM_MSS_VIM_INTPRIORITY_80 Registers

4.24.158.1 VIM_80 Register (Offset = 1140h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h84

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h84

Return to Summary Table

Table 4-3422. Instance Table

Instance Name	Physical Address
VIM	50F0 1140h

Figure 4-1616. INTPRIORITY_80 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3423. INTPRIORITY_80 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.159 VIM_MSS_VIM_INTPRIORITY_81 Registers

4.24.159.1 VIM_81 Register (Offset = 1144h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h85

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h85

Return to Summary Table

Table 4-3424. Instance Table

Instance Name	Physical Address
VIM	50F0 1144h

Figure 4-1617. INTPRIORITY_81 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3425. INTPRIORITY_81 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.160 VIM_MSS_VIM_INTPRIORITY_82 Registers

4.24.160.1 VIM_82 Register (Offset = 1148h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h86

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h86

Return to Summary Table

Table 4-3426. Instance Table

Instance Name	Physical Address
VIM	50F0 1148h

Figure 4-1618. INTPRIORITY_82 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3427. INTPRIORITY_82 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.161 VIM_MSS_VIM_INTPRIORITY_83 Registers

4.24.161.1 VIM_83 Register (Offset = 114Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h87

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h87

Return to Summary Table

Table 4-3428. Instance Table

Instance Name	Physical Address
VIM	50F0 114Ch

Figure 4-1619. INTPRIORITY_83 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3429. INTPRIORITY_83 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.162 VIM_MSS_VIM_INTPRIORITY_84 Registers

4.24.162.1 VIM_84 Register (Offset = 1150h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h88

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h88

Return to Summary Table

Table 4-3430. Instance Table

Instance Name	Physical Address
VIM	50F0 1150h

Figure 4-1620. INTPRIORITY_84 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3431. INTPRIORITY_84 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.163 VIM_MSS_VIM_INTPRIORITY_85 Registers

4.24.163.1 VIM_85 Register (Offset = 1154h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h89

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h89

Return to Summary Table

Table 4-3432. Instance Table

Instance Name	Physical Address
VIM	50F0 1154h

Figure 4-1621. INTPRIORITY_85 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3433. INTPRIORITY_85 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.164 VIM_MSS_VIM_INTPRIORITY_86 Registers

4.24.164.1 VIM_86 Register (Offset = 1158h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h90

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h90

Return to Summary Table

Table 4-3434. Instance Table

Instance Name	Physical Address
VIM	50F0 1158h

Figure 4-1622. INTPRIORITY_86 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3435. INTPRIORITY_86 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.165 VIM_MSS_VIM_INTPRIORITY_87 Registers

4.24.165.1 VIM_87 Register (Offset = 115Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h91

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h91

Return to Summary Table

Table 4-3436. Instance Table

Instance Name	Physical Address
VIM	50F0 115Ch

Figure 4-1623. INTPRIORITY_87 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3437. INTPRIORITY_87 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.166 VIM_MSS_VIM_INTPRIORITY_88 Registers

4.24.166.1 VIM_88 Register (Offset = 1160h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h92

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h92

Return to Summary Table

Table 4-3438. Instance Table

Instance Name	Physical Address
VIM	50F0 1160h

Figure 4-1624. INTPRIORITY_88 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3439. INTPRIORITY_88 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.167 VIM_MSS_VIM_INTPRIORITY_89 Registers

4.24.167.1 VIM_89 Register (Offset = 1164h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h93

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h93

Return to Summary Table

Table 4-3440. Instance Table

Instance Name	Physical Address
VIM	50F0 1164h

Figure 4-1625. INTPRIORITY_89 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3441. INTPRIORITY_89 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.168 VIM_MSS_VIM_INTPRIORITY_90 Registers

4.24.168.1 VIM_90 Register (Offset = 1168h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h94

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h94

Return to Summary Table

Table 4-3442. Instance Table

Instance Name	Physical Address
VIM	50F0 1168h

Figure 4-1626. INTPRIORITY_90 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3443. INTPRIORITY_90 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.169 VIM_MSS_VIM_INTPRIORITY_91 Registers

4.24.169.1 VIM_91 Register (Offset = 116Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h95

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h95

Return to Summary Table

Table 4-3444. Instance Table

Instance Name	Physical Address
VIM	50F0 116Ch

Figure 4-1627. INTPRIORITY_91 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3445. INTPRIORITY_91 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.170 VIM_MSS_VIM_INTPRIORITY_92 Registers

4.24.170.1 VIM_92 Register (Offset = 1170h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h96

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h96

Return to Summary Table

Table 4-3446. Instance Table

Instance Name	Physical Address
VIM	50F0 1170h

Figure 4-1628. INTPRIORITY_92 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3447. INTPRIORITY_92 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.171 VIM_MSS_VIM_INTPRIORITY_93 Registers

4.24.171.1 VIM_93 Register (Offset = 1174h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h97

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h97

Return to Summary Table

Table 4-3448. Instance Table

Instance Name	Physical Address
VIM	50F0 1174h

Figure 4-1629. INTPRIORITY_93 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3449. INTPRIORITY_93 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.172 VIM_MSS_VIM_INTPRIORITY_94 Registers

4.24.172.1 VIM_94 Register (Offset = 1178h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h98

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h98

Return to Summary Table

Table 4-3450. Instance Table

Instance Name	Physical Address
VIM	50F0 1178h

Figure 4-1630. INTPRIORITY_94 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3451. INTPRIORITY_94 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.173 VIM_MSS_VIM_INTPRIORITY_95 Registers

4.24.173.1 VIM_95 Register (Offset = 117Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h99

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h99

Return to Summary Table

Table 4-3452. Instance Table

Instance Name	Physical Address
VIM	50F0 117Ch

Figure 4-1631. INTPRIORITY_95 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3453. INTPRIORITY_95 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.174 VIM_MSS_VIM_INTPRIORITY_96 Registers

4.24.174.1 VIM_96 Register (Offset = 1180h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h100

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h100

Return to Summary Table

Table 4-3454. Instance Table

Instance Name	Physical Address
VIM	50F0 1180h

Figure 4-1632. INTPRIORITY_96 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3455. INTPRIORITY_96 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.175 VIM_MSS_VIM_INTPRIORITY_97 Registers

4.24.175.1 VIM_97 Register (Offset = 1184h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h101

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h101

Return to Summary Table

Table 4-3456. Instance Table

Instance Name	Physical Address
VIM	50F0 1184h

Figure 4-1633. INTPRIORITY_97 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3457. INTPRIORITY_97 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.176 VIM_MSS_VIM_INTPRIORITY_98 Registers

4.24.176.1 VIM_98 Register (Offset = 1188h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h102

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h102

Return to Summary Table

Table 4-3458. Instance Table

Instance Name	Physical Address
VIM	50F0 1188h

Figure 4-1634. INTPRIORITY_98 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3459. INTPRIORITY_98 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.177 VIM_MSS_VIM_INTPRIORITY_99 Registers

4.24.177.1 VIM_99 Register (Offset = 118Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h103

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h103

Return to Summary Table

Table 4-3460. Instance Table

Instance Name	Physical Address
VIM	50F0 118Ch

Figure 4-1635. INTPRIORITY_99 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3461. INTPRIORITY_99 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.178 VIM_MSS_VIM_INTPRIORITY_100 Registers

4.24.178.1 VIM_100 Register (Offset = 1190h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h104

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h104

Return to Summary Table

Table 4-3462. Instance Table

Instance Name	Physical Address
VIM	50F0 1190h

Figure 4-1636. INTPRIORITY_100 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3463. INTPRIORITY_100 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.179 VIM_MSS_VIM_INTPRIORITY_101 Registers

4.24.179.1 VIM_101 Register (Offset = 1194h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h105

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h105

Return to Summary Table

Table 4-3464. Instance Table

Instance Name	Physical Address
VIM	50F0 1194h

Figure 4-1637. INTPRIORITY_101 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3465. INTPRIORITY_101 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.180 VIM_MSS_VIM_INTPRIORITY_102 Registers

4.24.180.1 VIM_102 Register (Offset = 1198h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h106

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h106

Return to Summary Table

Table 4-3466. Instance Table

Instance Name	Physical Address
VIM	50F0 1198h

Figure 4-1638. INTPRIORITY_102 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3467. INTPRIORITY_102 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.181 VIM_MSS_VIM_INTPRIORITY_103 Registers

4.24.181.1 VIM_103 Register (Offset = 119Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h107

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h107

Return to Summary Table

Table 4-3468. Instance Table

Instance Name	Physical Address
VIM	50F0 119Ch

Figure 4-1639. INTPRIORITY_103 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3469. INTPRIORITY_103 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.182 VIM_MSS_VIM_INTPRIORITY_104 Registers

4.24.182.1 VIM_104 Register (Offset = 11A0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h108

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h108

Return to Summary Table

Table 4-3470. Instance Table

Instance Name	Physical Address
VIM	50F0 11A0h

Figure 4-1640. INTPRIORITY_104 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3471. INTPRIORITY_104 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.183 VIM_MSS_VIM_INTPRIORITY_105 Registers

4.24.183.1 VIM_105 Register (Offset = 11A4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h109

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h109

Return to Summary Table

Table 4-3472. Instance Table

Instance Name	Physical Address
VIM	50F0 11A4h

Figure 4-1641. INTPRIORITY_105 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3473. INTPRIORITY_105 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.184 VIM_MSS_VIM_INTPRIORITY_106 Registers

4.24.184.1 VIM_106 Register (Offset = 11A8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h110

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h110

Return to Summary Table

Table 4-3474. Instance Table

Instance Name	Physical Address
VIM	50F0 11A8h

Figure 4-1642. INTPRIORITY_106 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3475. INTPRIORITY_106 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.185 VIM_MSS_VIM_INTPRIORITY_107 Registers

4.24.185.1 VIM_107 Register (Offset = 11ACh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h111

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h111

Return to Summary Table

Table 4-3476. Instance Table

Instance Name	Physical Address
VIM	50F0 11ACh

Figure 4-1643. INTPRIORITY_107 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3477. INTPRIORITY_107 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.186 VIM_MSS_VIM_INTPRIORITY_108 Registers

4.24.186.1 VIM_108 Register (Offset = 11B0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h112

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h112

Return to Summary Table

Table 4-3478. Instance Table

Instance Name	Physical Address
VIM	50F0 11B0h

Figure 4-1644. INTPRIORITY_108 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3479. INTPRIORITY_108 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.187 VIM_MSS_VIM_INTPRIORITY_109 Registers

4.24.187.1 VIM_109 Register (Offset = 11B4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h113

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h113

Return to Summary Table

Table 4-3480. Instance Table

Instance Name	Physical Address
VIM	50F0 11B4h

Figure 4-1645. INTPRIORITY_109 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3481. INTPRIORITY_109 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.188 VIM_MSS_VIM_INTPRIORITY_110 Registers

4.24.188.1 VIM_110 Register (Offset = 11B8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h114

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h114

Return to Summary Table

Table 4-3482. Instance Table

Instance Name	Physical Address
VIM	50F0 11B8h

Figure 4-1646. INTPRIORITY_110 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3483. INTPRIORITY_110 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.189 VIM_MSS_VIM_INTPRIORITY_111 Registers

4.24.189.1 VIM_111 Register (Offset = 11BCh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h115

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h115

Return to Summary Table

Table 4-3484. Instance Table

Instance Name	Physical Address
VIM	50F0 11BCh

Figure 4-1647. INTPRIORITY_111 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3485. INTPRIORITY_111 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.190 VIM_MSS_VIM_INTPRIORITY_112 Registers

4.24.190.1 VIM_112 Register (Offset = 11C0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h116

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h116

Return to Summary Table

Table 4-3486. Instance Table

Instance Name	Physical Address
VIM	50F0 11C0h

Figure 4-1648. INTPRIORITY_112 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3487. INTPRIORITY_112 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.191 VIM_MSS_VIM_INTPRIORITY_113 Registers

4.24.191.1 VIM_113 Register (Offset = 11C4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h117

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h117

Return to Summary Table

Table 4-3488. Instance Table

Instance Name	Physical Address
VIM	50F0 11C4h

Figure 4-1649. INTPRIORITY_113 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3489. INTPRIORITY_113 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.192 VIM_MSS_VIM_INTPRIORITY_114 Registers

4.24.192.1 VIM_114 Register (Offset = 11C8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h118

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h118

Return to Summary Table

Table 4-3490. Instance Table

Instance Name	Physical Address
VIM	50F0 11C8h

Figure 4-1650. INTPRIORITY_114 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3491. INTPRIORITY_114 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.193 VIM_MSS_VIM_INTPRIORITY_115 Registers

4.24.193.1 VIM_115 Register (Offset = 11CCh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h119

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h119

Return to Summary Table

Table 4-3492. Instance Table

Instance Name	Physical Address
VIM	50F0 11CCh

Figure 4-1651. INTPRIORITY_115 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3493. INTPRIORITY_115 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.194 VIM_MSS_VIM_INTPRIORITY_116 Registers

4.24.194.1 VIM_116 Register (Offset = 11D0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h120

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h120

Return to Summary Table

Table 4-3494. Instance Table

Instance Name	Physical Address
VIM	50F0 11D0h

Figure 4-1652. INTPRIORITY_116 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3495. INTPRIORITY_116 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.195 VIM_MSS_VIM_INTPRIORITY_117 Registers

4.24.195.1 VIM_117 Register (Offset = 11D4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h121

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h121

Return to Summary Table

Table 4-3496. Instance Table

Instance Name	Physical Address
VIM	50F0 11D4h

Figure 4-1653. INTPRIORITY_117 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3497. INTPRIORITY_117 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.196 VIM_MSS_VIM_INTPRIORITY_118 Registers

4.24.196.1 VIM_118 Register (Offset = 11D8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h122

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h122

Return to Summary Table

Table 4-3498. Instance Table

Instance Name	Physical Address
VIM	50F0 11D8h

Figure 4-1654. INTPRIORITY_118 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3499. INTPRIORITY_118 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.197 VIM_MSS_VIM_INTPRIORITY_119 Registers

4.24.197.1 VIM_119 Register (Offset = 11DCh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h123

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h123

Return to Summary Table

Table 4-3500. Instance Table

Instance Name	Physical Address
VIM	50F0 11DCh

Figure 4-1655. INTPRIORITY_119 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3501. INTPRIORITY_119 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.198 VIM_MSS_VIM_INTPRIORITY_120 Registers

4.24.198.1 VIM_120 Register (Offset = 11E0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h124

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h124

Return to Summary Table

Table 4-3502. Instance Table

Instance Name	Physical Address
VIM	50F0 11E0h

Figure 4-1656. INTPRIORITY_120 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3503. INTPRIORITY_120 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.199 VIM_MSS_VIM_INTPRIORITY_121 Registers

4.24.199.1 VIM_121 Register (Offset = 11E4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h125

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h125

Return to Summary Table

Table 4-3504. Instance Table

Instance Name	Physical Address
VIM	50F0 11E4h

Figure 4-1657. INTPRIORITY_121 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3505. INTPRIORITY_121 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.200 VIM_MSS_VIM_INTPRIORITY_122 Registers

4.24.200.1 VIM_122 Register (Offset = 11E8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h126

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h126

Return to Summary Table

Table 4-3506. Instance Table

Instance Name	Physical Address
VIM	50F0 11E8h

Figure 4-1658. INTPRIORITY_122 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3507. INTPRIORITY_122 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.201 VIM_MSS_VIM_INTPRIORITY_123 Registers

4.24.201.1 VIM_123 Register (Offset = 11ECh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h127

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h127

Return to Summary Table

Table 4-3508. Instance Table

Instance Name	Physical Address
VIM	50F0 11ECh

Figure 4-1659. INTPRIORITY_123 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3509. INTPRIORITY_123 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.202 VIM_MSS_VIM_INTPRIORITY_124 Registers

4.24.202.1 VIM_124 Register (Offset = 11F0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h128

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h128

Return to Summary Table

Table 4-3510. Instance Table

Instance Name	Physical Address
VIM	50F0 11F0h

Figure 4-1660. INTPRIORITY_124 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3511. INTPRIORITY_124 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.203 VIM_MSS_VIM_INTPRIORITY_125 Registers

4.24.203.1 VIM_125 Register (Offset = 11F4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h129

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h129

Return to Summary Table

Table 4-3512. Instance Table

Instance Name	Physical Address
VIM	50F0 11F4h

Figure 4-1661. INTPRIORITY_125 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3513. INTPRIORITY_125 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.204 VIM_MSS_VIM_INTPRIORITY_126 Registers

4.24.204.1 VIM_126 Register (Offset = 11F8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h130

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h130

Return to Summary Table

Table 4-3514. Instance Table

Instance Name	Physical Address
VIM	50F0 11F8h

Figure 4-1662. INTPRIORITY_126 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3515. INTPRIORITY_126 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.205 VIM_MSS_VIM_INTPRIORITY_127 Registers

4.24.205.1 VIM_127 Register (Offset = 11FCh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h131

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h131

Return to Summary Table

Table 4-3516. Instance Table

Instance Name	Physical Address
VIM	50F0 11FCh

Figure 4-1663. INTPRIORITY_127 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3517. INTPRIORITY_127 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.206 VIM_MSS_VIM_INTPRIORITY_128 Registers

4.24.206.1 VIM_128 Register (Offset = 1200h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h132

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h132

Return to Summary Table

Table 4-3518. Instance Table

Instance Name	Physical Address
VIM	50F0 1200h

Figure 4-1664. INTPRIORITY_128 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3519. INTPRIORITY_128 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.207 VIM_MSS_VIM_INTPRIORITY_129 Registers

4.24.207.1 VIM_129 Register (Offset = 1204h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h133

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h133

Return to Summary Table

Table 4-3520. Instance Table

Instance Name	Physical Address
VIM	50F0 1204h

Figure 4-1665. INTPRIORITY_129 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3521. INTPRIORITY_129 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.208 VIM_MSS_VIM_INTPRIORITY_130 Registers

4.24.208.1 VIM_130 Register (Offset = 1208h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h134

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h134

Return to Summary Table

Table 4-3522. Instance Table

Instance Name	Physical Address
VIM	50F0 1208h

Figure 4-1666. INTPRIORITY_130 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3523. INTPRIORITY_130 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.209 VIM_MSS_VIM_INTPRIORITY_131 Registers

4.24.209.1 VIM_131 Register (Offset = 120Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h135

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h135

Return to Summary Table

Table 4-3524. Instance Table

Instance Name	Physical Address
VIM	50F0 120Ch

Figure 4-1667. INTPRIORITY_131 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3525. INTPRIORITY_131 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.210 VIM_MSS_VIM_INTPRIORITY_132 Registers

4.24.210.1 VIM_132 Register (Offset = 1210h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h136

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h136

Return to Summary Table

Table 4-3526. Instance Table

Instance Name	Physical Address
VIM	50F0 1210h

Figure 4-1668. INTPRIORITY_132 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3527. INTPRIORITY_132 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.211 VIM_MSS_VIM_INTPRIORITY_133 Registers

4.24.211.1 VIM_133 Register (Offset = 1214h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h137

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h137

Return to Summary Table

Table 4-3528. Instance Table

Instance Name	Physical Address
VIM	50F0 1214h

Figure 4-1669. INTPRIORITY_133 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3529. INTPRIORITY_133 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.212 VIM_MSS_VIM_INTPRIORITY_134 Registers

4.24.212.1 VIM_134 Register (Offset = 1218h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h138

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h138

Return to Summary Table

Table 4-3530. Instance Table

Instance Name	Physical Address
VIM	50F0 1218h

Figure 4-1670. INTPRIORITY_134 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3531. INTPRIORITY_134 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.213 VIM_MSS_VIM_INTPRIORITY_135 Registers

4.24.213.1 VIM_135 Register (Offset = 121Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h139

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h139

Return to Summary Table

Table 4-3532. Instance Table

Instance Name	Physical Address
VIM	50F0 121Ch

Figure 4-1671. INTPRIORITY_135 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3533. INTPRIORITY_135 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.214 VIM_MSS_VIM_INTPRIORITY_136 Registers

4.24.214.1 VIM_136 Register (Offset = 1220h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h140

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h140

Return to Summary Table

Table 4-3534. Instance Table

Instance Name	Physical Address
VIM	50F0 1220h

Figure 4-1672. INTPRIORITY_136 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3535. INTPRIORITY_136 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.215 VIM_MSS_VIM_INTPRIORITY_137 Registers

4.24.215.1 VIM_137 Register (Offset = 1224h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h141

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h141

Return to Summary Table

Table 4-3536. Instance Table

Instance Name	Physical Address
VIM	50F0 1224h

Figure 4-1673. INTPRIORITY_137 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3537. INTPRIORITY_137 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.216 VIM_MSS_VIM_INTPRIORITY_138 Registers

4.24.216.1 VIM_138 Register (Offset = 1228h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h142

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h142

Return to Summary Table

Table 4-3538. Instance Table

Instance Name	Physical Address
VIM	50F0 1228h

Figure 4-1674. INTPRIORITY_138 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3539. INTPRIORITY_138 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.217 VIM_MSS_VIM_INTPRIORITY_139 Registers

4.24.217.1 VIM_139 Register (Offset = 122Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h143

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h143

Return to Summary Table

Table 4-3540. Instance Table

Instance Name	Physical Address
VIM	50F0 122Ch

Figure 4-1675. INTPRIORITY_139 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3541. INTPRIORITY_139 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.218 VIM_MSS_VIM_INTPRIORITY_140 Registers

4.24.218.1 VIM_140 Register (Offset = 1230h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h144

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h144

Return to Summary Table

Table 4-3542. Instance Table

Instance Name	Physical Address
VIM	50F0 1230h

Figure 4-1676. INTPRIORITY_140 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3543. INTPRIORITY_140 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.219 VIM_MSS_VIM_INTPRIORITY_141 Registers

4.24.219.1 VIM_141 Register (Offset = 1234h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h145

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h145

Return to Summary Table

Table 4-3544. Instance Table

Instance Name	Physical Address
VIM	50F0 1234h

Figure 4-1677. INTPRIORITY_141 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3545. INTPRIORITY_141 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.220 VIM_MSS_VIM_INTPRIORITY_142 Registers

4.24.220.1 VIM_142 Register (Offset = 1238h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h146

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h146

Return to Summary Table

Table 4-3546. Instance Table

Instance Name	Physical Address
VIM	50F0 1238h

Figure 4-1678. INTPRIORITY_142 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3547. INTPRIORITY_142 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.221 VIM_MSS_VIM_INTPRIORITY_143 Registers

4.24.221.1 VIM_143 Register (Offset = 123Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h147

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h147

Return to Summary Table

Table 4-3548. Instance Table

Instance Name	Physical Address
VIM	50F0 123Ch

Figure 4-1679. INTPRIORITY_143 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3549. INTPRIORITY_143 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.222 VIM_MSS_VIM_INTPRIORITY_144 Registers

4.24.222.1 VIM_144 Register (Offset = 1240h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h148

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h148

Return to Summary Table

Table 4-3550. Instance Table

Instance Name	Physical Address
VIM	50F0 1240h

Figure 4-1680. INTPRIORITY_144 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3551. INTPRIORITY_144 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.223 VIM_MSS_VIM_INTPRIORITY_145 Registers

4.24.223.1 VIM_145 Register (Offset = 1244h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h149

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h149

Return to Summary Table

Table 4-3552. Instance Table

Instance Name	Physical Address
VIM	50F0 1244h

Figure 4-1681. INTPRIORITY_145 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3553. INTPRIORITY_145 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.224 VIM_MSS_VIM_INTPRIORITY_146 Registers

4.24.224.1 VIM_146 Register (Offset = 1248h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h150

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h150

Return to Summary Table

Table 4-3554. Instance Table

Instance Name	Physical Address
VIM	50F0 1248h

Figure 4-1682. INTPRIORITY_146 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3555. INTPRIORITY_146 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.225 VIM_MSS_VIM_INTPRIORITY_147 Registers

4.24.225.1 VIM_147 Register (Offset = 124Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h151

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h151

Return to Summary Table

Table 4-3556. Instance Table

Instance Name	Physical Address
VIM	50F0 124Ch

Figure 4-1683. INTPRIORITY_147 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3557. INTPRIORITY_147 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.226 VIM_MSS_VIM_INTPRIORITY_148 Registers

4.24.226.1 VIM_148 Register (Offset = 1250h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h152

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h152

Return to Summary Table

Table 4-3558. Instance Table

Instance Name	Physical Address
VIM	50F0 1250h

Figure 4-1684. INTPRIORITY_148 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3559. INTPRIORITY_148 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.227 VIM_MSS_VIM_INTPRIORITY_149 Registers

4.24.227.1 VIM_149 Register (Offset = 1254h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h153

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h153

Return to Summary Table

Table 4-3560. Instance Table

Instance Name	Physical Address
VIM	50F0 1254h

Figure 4-1685. INTPRIORITY_149 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3561. INTPRIORITY_149 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.228 VIM_MSS_VIM_INTPRIORITY_150 Registers

4.24.228.1 VIM_150 Register (Offset = 1258h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h154

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h154

Return to Summary Table

Table 4-3562. Instance Table

Instance Name	Physical Address
VIM	50F0 1258h

Figure 4-1686. INTPRIORITY_150 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3563. INTPRIORITY_150 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.229 VIM_MSS_VIM_INTPRIORITY_151 Registers

4.24.229.1 VIM_151 Register (Offset = 125Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h155

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h155

Return to Summary Table

Table 4-3564. Instance Table

Instance Name	Physical Address
VIM	50F0 125Ch

Figure 4-1687. INTPRIORITY_151 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3565. INTPRIORITY_151 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.230 VIM_MSS_VIM_INTPRIORITY_152 Registers

4.24.230.1 VIM_152 Register (Offset = 1260h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h156

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h156

Return to Summary Table

Table 4-3566. Instance Table

Instance Name	Physical Address
VIM	50F0 1260h

Figure 4-1688. INTPRIORITY_152 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3567. INTPRIORITY_152 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.231 VIM_MSS_VIM_INTPRIORITY_153 Registers

4.24.231.1 VIM_153 Register (Offset = 1264h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h157

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h157

Return to Summary Table

Table 4-3568. Instance Table

Instance Name	Physical Address
VIM	50F0 1264h

Figure 4-1689. INTPRIORITY_153 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3569. INTPRIORITY_153 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.232 VIM_MSS_VIM_INTPRIORITY_154 Registers

4.24.232.1 VIM_154 Register (Offset = 1268h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h158

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h158

Return to Summary Table

Table 4-3570. Instance Table

Instance Name	Physical Address
VIM	50F0 1268h

Figure 4-1690. INTPRIORITY_154 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3571. INTPRIORITY_154 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.233 VIM_MSS_VIM_INTPRIORITY_155 Registers

4.24.233.1 VIM_155 Register (Offset = 126Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h159

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h159

Return to Summary Table

Table 4-3572. Instance Table

Instance Name	Physical Address
VIM	50F0 126Ch

Figure 4-1691. INTPRIORITY_155 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3573. INTPRIORITY_155 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.234 VIM_MSS_VIM_INTPRIORITY_156 Registers

4.24.234.1 VIM_156 Register (Offset = 1270h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h160

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h160

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Table 4-3574. Instance Table

Instance Name	Physical Address
VIM	50F0 1270h

Figure 4-1692. INTPRIORITY_156 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3575. INTPRIORITY_156 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.235 VIM_MSS_VIM_INTPRIORITY_157 Registers

4.24.235.1 VIM_157 Register (Offset = 1274h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h161

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h161

Return to Summary Table

Table 4-3576. Instance Table

Instance Name	Physical Address
VIM	50F0 1274h

Figure 4-1693. INTPRIORITY_157 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3577. INTPRIORITY_157 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.236 VIM_MSS_VIM_INTPRIORITY_158 Registers

4.24.236.1 VIM_158 Register (Offset = 1278h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h162

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h162

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Table 4-3578. Instance Table

Instance Name	Physical Address
VIM	50F0 1278h

Figure 4-1694. INTPRIORITY_158 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3579. INTPRIORITY_158 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.237 VIM_MSS_VIM_INTPRIORITY_159 Registers

4.24.237.1 VIM_159 Register (Offset = 127Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h163

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h163

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Table 4-3580. Instance Table

Instance Name	Physical Address
VIM	50F0 127Ch

Figure 4-1695. INTPRIORITY_159 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3581. INTPRIORITY_159 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.238 VIM_MSS_VIM_INTPRIORITY_160 Registers

4.24.238.1 VIM_160 Register (Offset = 1280h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h164

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h164

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Table 4-3582. Instance Table

Instance Name	Physical Address
VIM	50F0 1280h

Figure 4-1696. INTPRIORITY_160 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3583. INTPRIORITY_160 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.239 VIM_MSS_VIM_INTPRIORITY_161 Registers

4.24.239.1 VIM_161 Register (Offset = 1284h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h165

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h165

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Table 4-3584. Instance Table

Instance Name	Physical Address
VIM	50F0 1284h

Figure 4-1697. INTPRIORITY_161 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3585. INTPRIORITY_161 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.240 VIM_MSS_VIM_INTPRIORITY_162 Registers

4.24.240.1 VIM_162 Register (Offset = 1288h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h166

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h166

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Table 4-3586. Instance Table

Instance Name	Physical Address
VIM	50F0 1288h

Figure 4-1698. INTPRIORITY_162 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3587. INTPRIORITY_162 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.241 VIM_MSS_VIM_INTPRIORITY_163 Registers

4.24.241.1 VIM_163 Register (Offset = 128Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h167

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h167

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Table 4-3588. Instance Table

Instance Name	Physical Address
VIM	50F0 128Ch

Figure 4-1699. INTPRIORITY_163 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3589. INTPRIORITY_163 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.242 VIM_MSS_VIM_INTPRIORITY_164 Registers

4.24.242.1 VIM_164 Register (Offset = 1290h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h168

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h168

Return to Summary Table

Table 4-3590. Instance Table

Instance Name	Physical Address
VIM	50F0 1290h

Figure 4-1700. INTPRIORITY_164 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3591. INTPRIORITY_164 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.243 VIM_MSS_VIM_INTPRIORITY_165 Registers

4.24.243.1 VIM_165 Register (Offset = 1294h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h169

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h169

Return to Summary Table

Table 4-3592. Instance Table

Instance Name	Physical Address
VIM	50F0 1294h

Figure 4-1701. INTPRIORITY_165 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3593. INTPRIORITY_165 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.244 VIM_MSS_VIM_INTPRIORITY_166 Registers

4.24.244.1 VIM_166 Register (Offset = 1298h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h170

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h170

Return to Summary Table

Table 4-3594. Instance Table

Instance Name	Physical Address
VIM	50F0 1298h

Figure 4-1702. INTPRIORITY_166 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3595. INTPRIORITY_166 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.245 VIM_MSS_VIM_INTPRIORITY_167 Registers

4.24.245.1 VIM_167 Register (Offset = 129Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h171

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h171

Return to Summary Table

Table 4-3596. Instance Table

Instance Name	Physical Address
VIM	50F0 129Ch

Figure 4-1703. INTPRIORITY_167 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3597. INTPRIORITY_167 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.246 VIM_MSS_VIM_INTPRIORITY_168 Registers

4.24.246.1 VIM_168 Register (Offset = 12A0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h172

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h172

Return to Summary Table

Table 4-3598. Instance Table

Instance Name	Physical Address
VIM	50F0 12A0h

Figure 4-1704. INTPRIORITY_168 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3599. INTPRIORITY_168 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.247 VIM_MSS_VIM_INTPRIORITY_169 Registers

4.24.247.1 VIM_169 Register (Offset = 12A4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h173

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h173

Return to Summary Table

Table 4-3600. Instance Table

Instance Name	Physical Address
VIM	50F0 12A4h

Figure 4-1705. INTPRIORITY_169 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3601. INTPRIORITY_169 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.248 VIM_MSS_VIM_INTPRIORITY_170 Registers

4.24.248.1 VIM_170 Register (Offset = 12A8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h174

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h174

Return to Summary Table

Table 4-3602. Instance Table

Instance Name	Physical Address
VIM	50F0 12A8h

Figure 4-1706. INTPRIORITY_170 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3603. INTPRIORITY_170 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.249 VIM_MSS_VIM_INTPRIORITY_171 Registers

4.24.249.1 VIM_171 Register (Offset = 12ACh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h175

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h175

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Table 4-3604. Instance Table

Instance Name	Physical Address
VIM	50F0 12ACh

Figure 4-1707. INTPRIORITY_171 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3605. INTPRIORITY_171 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.250 VIM_MSS_VIM_INTPRIORITY_172 Registers

4.24.250.1 VIM_172 Register (Offset = 12B0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h176

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h176

Return to Summary Table

Table 4-3606. Instance Table

Instance Name	Physical Address
VIM	50F0 12B0h

Figure 4-1708. INTPRIORITY_172 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3607. INTPRIORITY_172 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.251 VIM_MSS_VIM_INTPRIORITY_173 Registers

4.24.251.1 VIM_173 Register (Offset = 12B4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h177

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h177

Return to Summary Table

Table 4-3608. Instance Table

Instance Name	Physical Address
VIM	50F0 12B4h

Figure 4-1709. INTPRIORITY_173 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3609. INTPRIORITY_173 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.252 VIM_MSS_VIM_INTPRIORITY_174 Registers

4.24.252.1 VIM_174 Register (Offset = 12B8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h178

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h178

Return to Summary Table

Table 4-3610. Instance Table

Instance Name	Physical Address
VIM	50F0 12B8h

Figure 4-1710. INTPRIORITY_174 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3611. INTPRIORITY_174 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.253 VIM_MSS_VIM_INTPRIORITY_175 Registers

4.24.253.1 VIM_175 Register (Offset = 12BCh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h179

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h179

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Table 4-3612. Instance Table

Instance Name	Physical Address
VIM	50F0 12BCh

Figure 4-1711. INTPRIORITY_175 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3613. INTPRIORITY_175 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.254 VIM_MSS_VIM_INTPRIORITY_176 Registers

4.24.254.1 VIM_176 Register (Offset = 12C0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h180

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h180

Return to Summary Table

Table 4-3614. Instance Table

Instance Name	Physical Address
VIM	50F0 12C0h

Figure 4-1712. INTPRIORITY_176 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3615. INTPRIORITY_176 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.255 VIM_MSS_VIM_INTPRIORITY_177 Registers

4.24.255.1 VIM_177 Register (Offset = 12C4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h181

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h181

Return to Summary Table

Table 4-3616. Instance Table

Instance Name	Physical Address
VIM	50F0 12C4h

Figure 4-1713. INTPRIORITY_177 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3617. INTPRIORITY_177 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.256 VIM_MSS_VIM_INTPRIORITY_178 Registers

4.24.256.1 VIM_178 Register (Offset = 12C8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h182

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h182

Return to Summary Table

Table 4-3618. Instance Table

Instance Name	Physical Address
VIM	50F0 12C8h

Figure 4-1714. INTPRIORITY_178 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3619. INTPRIORITY_178 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.257 VIM_MSS_VIM_INTPRIORITY_179 Registers

4.24.257.1 VIM_179 Register (Offset = 12CCh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h183

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h183

Return to Summary Table

Table 4-3620. Instance Table

Instance Name	Physical Address
VIM	50F0 12CCh

Figure 4-1715. INTPRIORITY_179 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3621. INTPRIORITY_179 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.258 VIM_MSS_VIM_INTPRIORITY_180 Registers

4.24.258.1 VIM_180 Register (Offset = 12D0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h184

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h184

Return to Summary Table

Table 4-3622. Instance Table

Instance Name	Physical Address
VIM	50F0 12D0h

Figure 4-1716. INTPRIORITY_180 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3623. INTPRIORITY_180 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.259 VIM_MSS_VIM_INTPRIORITY_181 Registers

4.24.259.1 VIM_181 Register (Offset = 12D4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h185

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h185

Return to Summary Table

Table 4-3624. Instance Table

Instance Name	Physical Address
VIM	50F0 12D4h

Figure 4-1717. INTPRIORITY_181 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3625. INTPRIORITY_181 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.260 VIM_MSS_VIM_INTPRIORITY_182 Registers

4.24.260.1 VIM_182 Register (Offset = 12D8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h186

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h186

Return to Summary Table

Table 4-3626. Instance Table

Instance Name	Physical Address
VIM	50F0 12D8h

Figure 4-1718. INTPRIORITY_182 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3627. INTPRIORITY_182 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.261 VIM_MSS_VIM_INTPRIORITY_183 Registers

4.24.261.1 VIM_183 Register (Offset = 12DCh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h187

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h187

Return to Summary Table

Table 4-3628. Instance Table

Instance Name	Physical Address
VIM	50F0 12DCh

Figure 4-1719. INTPRIORITY_183 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3629. INTPRIORITY_183 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.262 VIM_MSS_VIM_INTPRIORITY_184 Registers

4.24.262.1 VIM_184 Register (Offset = 12E0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h188

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h188

Return to Summary Table

Table 4-3630. Instance Table

Instance Name	Physical Address
VIM	50F0 12E0h

Figure 4-1720. INTPRIORITY_184 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3631. INTPRIORITY_184 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.263 VIM_MSS_VIM_INTPRIORITY_185 Registers

4.24.263.1 VIM_185 Register (Offset = 12E4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h189

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h189

Return to Summary Table

Table 4-3632. Instance Table

Instance Name	Physical Address
VIM	50F0 12E4h

Figure 4-1721. INTPRIORITY_185 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3633. INTPRIORITY_185 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.264 VIM_MSS_VIM_INTPRIORITY_186 Registers

4.24.264.1 VIM_186 Register (Offset = 12E8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h190

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h190

Return to Summary Table

Table 4-3634. Instance Table

Instance Name	Physical Address
VIM	50F0 12E8h

Figure 4-1722. INTPRIORITY_186 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3635. INTPRIORITY_186 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.265 VIM_MSS_VIM_INTPRIORITY_187 Registers

4.24.265.1 VIM_187 Register (Offset = 12ECh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h191

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h191

Return to Summary Table

Table 4-3636. Instance Table

Instance Name	Physical Address
VIM	50F0 12ECh

Figure 4-1723. INTPRIORITY_187 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3637. INTPRIORITY_187 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.266 VIM_MSS_VIM_INTPRIORITY_188 Registers

4.24.266.1 VIM_188 Register (Offset = 12F0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h192

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h192

Return to Summary Table

Table 4-3638. Instance Table

Instance Name	Physical Address
VIM	50F0 12F0h

Figure 4-1724. INTPRIORITY_188 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3639. INTPRIORITY_188 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.267 VIM_MSS_VIM_INTPRIORITY_189 Registers

4.24.267.1 VIM_189 Register (Offset = 12F4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h193

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h193

Return to Summary Table

Table 4-3640. Instance Table

Instance Name	Physical Address
VIM	50F0 12F4h

Figure 4-1725. INTPRIORITY_189 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3641. INTPRIORITY_189 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.268 VIM_MSS_VIM_INTPRIORITY_190 Registers

4.24.268.1 VIM_190 Register (Offset = 12F8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h194

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h194

Return to Summary Table

Table 4-3642. Instance Table

Instance Name	Physical Address
VIM	50F0 12F8h

Figure 4-1726. INTPRIORITY_190 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3643. INTPRIORITY_190 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.269 VIM_MSS_VIM_INTPRIORITY_191 Registers

4.24.269.1 VIM_191 Register (Offset = 12FCh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h195

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h195

Return to Summary Table

Table 4-3644. Instance Table

Instance Name	Physical Address
VIM	50F0 12FCh

Figure 4-1727. INTPRIORITY_191 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3645. INTPRIORITY_191 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.270 VIM_MSS_VIM_INTPRIORITY_192 Registers

4.24.270.1 VIM_192 Register (Offset = 1300h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h196

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h196

Return to Summary Table

Table 4-3646. Instance Table

Instance Name	Physical Address
VIM	50F0 1300h

Figure 4-1728. INTPRIORITY_192 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3647. INTPRIORITY_192 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.271 VIM_MSS_VIM_INTPRIORITY_193 Registers

4.24.271.1 VIM_193 Register (Offset = 1304h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h197

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h197

Return to Summary Table

Table 4-3648. Instance Table

Instance Name	Physical Address
VIM	50F0 1304h

Figure 4-1729. INTPRIORITY_193 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3649. INTPRIORITY_193 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.272 VIM_MSS_VIM_INTPRIORITY_194 Registers

4.24.272.1 VIM_194 Register (Offset = 1308h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h198

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h198

Return to Summary Table

Table 4-3650. Instance Table

Instance Name	Physical Address
VIM	50F0 1308h

Figure 4-1730. INTPRIORITY_194 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3651. INTPRIORITY_194 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.273 VIM_MSS_VIM_INTPRIORITY_195 Registers

4.24.273.1 VIM_195 Register (Offset = 130Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h199

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h199

Return to Summary Table

Table 4-3652. Instance Table

Instance Name	Physical Address
VIM	50F0 130Ch

Figure 4-1731. INTPRIORITY_195 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3653. INTPRIORITY_195 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.274 VIM_MSS_VIM_INTPRIORITY_196 Registers

4.24.274.1 VIM_196 Register (Offset = 1310h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h200

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h200

Return to Summary Table

Table 4-3654. Instance Table

Instance Name	Physical Address
VIM	50F0 1310h

Figure 4-1732. INTPRIORITY_196 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3655. INTPRIORITY_196 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.275 VIM_MSS_VIM_INTPRIORITY_197 Registers

4.24.275.1 VIM_197 Register (Offset = 1314h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h201

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h201

Return to Summary Table

Table 4-3656. Instance Table

Instance Name	Physical Address
VIM	50F0 1314h

Figure 4-1733. INTPRIORITY_197 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3657. INTPRIORITY_197 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.276 VIM_MSS_VIM_INTPRIORITY_198 Registers

4.24.276.1 VIM_198 Register (Offset = 1318h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h202

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h202

Return to Summary Table

Table 4-3658. Instance Table

Instance Name	Physical Address
VIM	50F0 1318h

Figure 4-1734. INTPRIORITY_198 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3659. INTPRIORITY_198 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.277 VIM_MSS_VIM_INTPRIORITY_199 Registers

4.24.277.1 VIM_199 Register (Offset = 131Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h203

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h203

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Table 4-3660. Instance Table

Instance Name	Physical Address
VIM	50F0 131Ch

Figure 4-1735. INTPRIORITY_199 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3661. INTPRIORITY_199 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.278 VIM_MSS_VIM_INTPRIORITY_200 Registers

4.24.278.1 VIM_200 Register (Offset = 1320h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h204

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h204

Return to Summary Table

Table 4-3662. Instance Table

Instance Name	Physical Address
VIM	50F0 1320h

Figure 4-1736. INTPRIORITY_200 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3663. INTPRIORITY_200 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.279 VIM_MSS_VIM_INTPRIORITY_201 Registers

4.24.279.1 VIM_201 Register (Offset = 1324h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h205

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h205

Return to Summary Table

Table 4-3664. Instance Table

Instance Name	Physical Address
VIM	50F0 1324h

Figure 4-1737. INTPRIORITY_201 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3665. INTPRIORITY_201 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.280 VIM_MSS_VIM_INTPRIORITY_202 Registers

4.24.280.1 VIM_202 Register (Offset = 1328h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h206

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h206

Return to Summary Table

Table 4-3666. Instance Table

Instance Name	Physical Address
VIM	50F0 1328h

Figure 4-1738. INTPRIORITY_202 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3667. INTPRIORITY_202 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.281 VIM_MSS_VIM_INTPRIORITY_203 Registers

4.24.281.1 VIM_203 Register (Offset = 132Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h207

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h207

Return to Summary Table

Table 4-3668. Instance Table

Instance Name	Physical Address
VIM	50F0 132Ch

Figure 4-1739. INTPRIORITY_203 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3669. INTPRIORITY_203 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.282 VIM_MSS_VIM_INTPRIORITY_204 Registers

4.24.282.1 VIM_204 Register (Offset = 1330h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h208

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h208

Return to Summary Table

Table 4-3670. Instance Table

Instance Name	Physical Address
VIM	50F0 1330h

Figure 4-1740. INTPRIORITY_204 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3671. INTPRIORITY_204 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.283 VIM_MSS_VIM_INTPRIORITY_205 Registers

4.24.283.1 VIM_205 Register (Offset = 1334h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h209

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h209

Return to Summary Table

Table 4-3672. Instance Table

Instance Name	Physical Address
VIM	50F0 1334h

Figure 4-1741. INTPRIORITY_205 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3673. INTPRIORITY_205 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.284 VIM_MSS_VIM_INTPRIORITY_206 Registers

4.24.284.1 VIM_206 Register (Offset = 1338h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h210

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h210

Return to Summary Table

Table 4-3674. Instance Table

Instance Name	Physical Address
VIM	50F0 1338h

Figure 4-1742. INTPRIORITY_206 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3675. INTPRIORITY_206 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.285 VIM_MSS_VIM_INTPRIORITY_207 Registers

4.24.285.1 VIM_207 Register (Offset = 133Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h211

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h211

Return to Summary Table

Table 4-3676. Instance Table

Instance Name	Physical Address
VIM	50F0 133Ch

Figure 4-1743. INTPRIORITY_207 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3677. INTPRIORITY_207 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.286 VIM_MSS_VIM_INTPRIORITY_208 Registers

4.24.286.1 VIM_208 Register (Offset = 1340h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h212

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h212

Return to Summary Table

Table 4-3678. Instance Table

Instance Name	Physical Address
VIM	50F0 1340h

Figure 4-1744. INTPRIORITY_208 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3679. INTPRIORITY_208 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.287 VIM_MSS_VIM_INTPRIORITY_209 Registers

4.24.287.1 VIM_209 Register (Offset = 1344h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h213

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h213

Return to Summary Table

Table 4-3680. Instance Table

Instance Name	Physical Address
VIM	50F0 1344h

Figure 4-1745. INTPRIORITY_209 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3681. INTPRIORITY_209 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.288 VIM_MSS_VIM_INTPRIORITY_210 Registers

4.24.288.1 VIM_210 Register (Offset = 1348h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h214

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h214

Return to Summary Table

Table 4-3682. Instance Table

Instance Name	Physical Address
VIM	50F0 1348h

Figure 4-1746. INTPRIORITY_210 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3683. INTPRIORITY_210 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.289 VIM_MSS_VIM_INTPRIORITY_211 Registers

4.24.289.1 VIM_211 Register (Offset = 134Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h215

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h215

Return to Summary Table

Table 4-3684. Instance Table

Instance Name	Physical Address
VIM	50F0 134Ch

Figure 4-1747. INTPRIORITY_211 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3685. INTPRIORITY_211 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.290 VIM_MSS_VIM_INTPRIORITY_212 Registers

4.24.290.1 VIM_212 Register (Offset = 1350h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h216

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h216

Return to Summary Table

Table 4-3686. Instance Table

Instance Name	Physical Address
VIM	50F0 1350h

Figure 4-1748. INTPRIORITY_212 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3687. INTPRIORITY_212 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.291 VIM_MSS_VIM_INTPRIORITY_213 Registers

4.24.291.1 VIM_213 Register (Offset = 1354h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h217

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h217

Return to Summary Table

Table 4-3688. Instance Table

Instance Name	Physical Address
VIM	50F0 1354h

Figure 4-1749. INTPRIORITY_213 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3689. INTPRIORITY_213 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.292 VIM_MSS_VIM_INTPRIORITY_214 Registers

4.24.292.1 VIM_214 Register (Offset = 1358h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h218

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h218

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Table 4-3690. Instance Table

Instance Name	Physical Address
VIM	50F0 1358h

Figure 4-1750. INTPRIORITY_214 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3691. INTPRIORITY_214 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.293 VIM_MSS_VIM_INTPRIORITY_215 Registers

4.24.293.1 VIM_215 Register (Offset = 135Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h219

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h219

Return to Summary Table

Table 4-3692. Instance Table

Instance Name	Physical Address
VIM	50F0 135Ch

Figure 4-1751. INTPRIORITY_215 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3693. INTPRIORITY_215 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.294 VIM_MSS_VIM_INTPRIORITY_216 Registers

4.24.294.1 VIM_216 Register (Offset = 1360h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h220

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h220

Return to Summary Table

Table 4-3694. Instance Table

Instance Name	Physical Address
VIM	50F0 1360h

Figure 4-1752. INTPRIORITY_216 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3695. INTPRIORITY_216 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.295 VIM_MSS_VIM_INTPRIORITY_217 Registers

4.24.295.1 VIM_217 Register (Offset = 1364h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h221

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h221

Return to Summary Table

Table 4-3696. Instance Table

Instance Name	Physical Address
VIM	50F0 1364h

Figure 4-1753. INTPRIORITY_217 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3697. INTPRIORITY_217 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.296 VIM_MSS_VIM_INTPRIORITY_218 Registers

4.24.296.1 VIM_218 Register (Offset = 1368h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h222

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h222

Return to Summary Table

Table 4-3698. Instance Table

Instance Name	Physical Address
VIM	50F0 1368h

Figure 4-1754. INTPRIORITY_218 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3699. INTPRIORITY_218 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.297 VIM_MSS_VIM_INTPRIORITY_219 Registers

4.24.297.1 VIM_219 Register (Offset = 136Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h223

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h223

Return to Summary Table

Table 4-3700. Instance Table

Instance Name	Physical Address
VIM	50F0 136Ch

Figure 4-1755. INTPRIORITY_219 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3701. INTPRIORITY_219 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.298 VIM_MSS_VIM_INTPRIORITY_220 Registers

4.24.298.1 VIM_220 Register (Offset = 1370h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h224

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h224

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Table 4-3702. Instance Table

Instance Name	Physical Address
VIM	50F0 1370h

Figure 4-1756. INTPRIORITY_220 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3703. INTPRIORITY_220 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.299 VIM_MSS_VIM_INTPRIORITY_221 Registers

4.24.299.1 VIM_221 Register (Offset = 1374h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h225

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h225

Return to Summary Table

Table 4-3704. Instance Table

Instance Name	Physical Address
VIM	50F0 1374h

Figure 4-1757. INTPRIORITY_221 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3705. INTPRIORITY_221 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.300 VIM_MSS_VIM_INTPRIORITY_222 Registers

4.24.300.1 VIM_222 Register (Offset = 1378h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h226

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h226

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Table 4-3706. Instance Table

Instance Name	Physical Address
VIM	50F0 1378h

Figure 4-1758. INTPRIORITY_222 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3707. INTPRIORITY_222 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.301 VIM_MSS_VIM_INTPRIORITY_223 Registers

4.24.301.1 VIM_223 Register (Offset = 137Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h227

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h227

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Table 4-3708. Instance Table

Instance Name	Physical Address
VIM	50F0 137Ch

Figure 4-1759. INTPRIORITY_223 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3709. INTPRIORITY_223 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.302 VIM_MSS_VIM_INTPRIORITY_224 Registers

4.24.302.1 VIM_224 Register (Offset = 1380h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h228

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h228

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Table 4-3710. Instance Table

Instance Name	Physical Address
VIM	50F0 1380h

Figure 4-1760. INTPRIORITY_224 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3711. INTPRIORITY_224 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.303 VIM_MSS_VIM_INTPRIORITY_225 Registers

4.24.303.1 VIM_225 Register (Offset = 1384h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h229

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h229

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Table 4-3712. Instance Table

Instance Name	Physical Address
VIM	50F0 1384h

Figure 4-1761. INTPRIORITY_225 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3713. INTPRIORITY_225 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.304 VIM_MSS_VIM_INTPRIORITY_226 Registers

4.24.304.1 VIM_226 Register (Offset = 1388h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h230

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h230

Return to Summary Table

Table 4-3714. Instance Table

Instance Name	Physical Address
VIM	50F0 1388h

Figure 4-1762. INTPRIORITY_226 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3715. INTPRIORITY_226 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.305 VIM_MSS_VIM_INTPRIORITY_227 Registers

4.24.305.1 VIM_227 Register (Offset = 138Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h231

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h231

Return to Summary Table

Table 4-3716. Instance Table

Instance Name	Physical Address
VIM	50F0 138Ch

Figure 4-1763. INTPRIORITY_227 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3717. INTPRIORITY_227 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.306 VIM_MSS_VIM_INTPRIORITY_228 Registers

4.24.306.1 VIM_228 Register (Offset = 1390h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h232

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h232

Return to Summary Table

Table 4-3718. Instance Table

Instance Name	Physical Address
VIM	50F0 1390h

Figure 4-1764. INTPRIORITY_228 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3719. INTPRIORITY_228 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.307 VIM_MSS_VIM_INTPRIORITY_229 Registers

4.24.307.1 VIM_229 Register (Offset = 1394h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h233

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h233

Return to Summary Table

Table 4-3720. Instance Table

Instance Name	Physical Address
VIM	50F0 1394h

Figure 4-1765. INTPRIORITY_229 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3721. INTPRIORITY_229 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.308 VIM_MSS_VIM_INTPRIORITY_230 Registers

4.24.308.1 VIM_230 Register (Offset = 1398h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h234

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h234

Return to Summary Table

Table 4-3722. Instance Table

Instance Name	Physical Address
VIM	50F0 1398h

Figure 4-1766. INTPRIORITY_230 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3723. INTPRIORITY_230 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.309 VIM_MSS_VIM_INTPRIORITY_231 Registers

4.24.309.1 VIM_231 Register (Offset = 139Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h235

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h235

Return to Summary Table

Table 4-3724. Instance Table

Instance Name	Physical Address
VIM	50F0 139Ch

Figure 4-1767. INTPRIORITY_231 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3725. INTPRIORITY_231 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.310 VIM_MSS_VIM_INTPRIORITY_232 Registers

4.24.310.1 VIM_232 Register (Offset = 13A0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h236

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h236

Return to Summary Table

Table 4-3726. Instance Table

Instance Name	Physical Address
VIM	50F0 13A0h

Figure 4-1768. INTPRIORITY_232 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3727. INTPRIORITY_232 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.311 VIM_MSS_VIM_INTPRIORITY_233 Registers

4.24.311.1 VIM_233 Register (Offset = 13A4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h237

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h237

Return to Summary Table

Table 4-3728. Instance Table

Instance Name	Physical Address
VIM	50F0 13A4h

Figure 4-1769. INTPRIORITY_233 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3729. INTPRIORITY_233 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.312 VIM_MSS_VIM_INTPRIORITY_234 Registers

4.24.312.1 VIM_234 Register (Offset = 13A8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h238

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h238

Return to Summary Table

Table 4-3730. Instance Table

Instance Name	Physical Address
VIM	50F0 13A8h

Figure 4-1770. INTPRIORITY_234 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3731. INTPRIORITY_234 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.313 VIM_MSS_VIM_INTPRIORITY_235 Registers

4.24.313.1 VIM_235 Register (Offset = 13ACh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h239

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h239

Return to Summary Table

Table 4-3732. Instance Table

Instance Name	Physical Address
VIM	50F0 13ACh

Figure 4-1771. INTPRIORITY_235 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3733. INTPRIORITY_235 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.314 VIM_MSS_VIM_INTPRIORITY_236 Registers

4.24.314.1 VIM_236 Register (Offset = 13B0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h240

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h240

Return to Summary Table

Table 4-3734. Instance Table

Instance Name	Physical Address
VIM	50F0 13B0h

Figure 4-1772. INTPRIORITY_236 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3735. INTPRIORITY_236 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.315 VIM_MSS_VIM_INTPRIORITY_237 Registers

4.24.315.1 VIM_237 Register (Offset = 13B4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h241

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h241

Return to Summary Table

Table 4-3736. Instance Table

Instance Name	Physical Address
VIM	50F0 13B4h

Figure 4-1773. INTPRIORITY_237 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3737. INTPRIORITY_237 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.316 VIM_MSS_VIM_INTPRIORITY_238 Registers

4.24.316.1 VIM_238 Register (Offset = 13B8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h242

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h242

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Table 4-3738. Instance Table

Instance Name	Physical Address
VIM	50F0 13B8h

Figure 4-1774. INTPRIORITY_238 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3739. INTPRIORITY_238 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.317 VIM_MSS_VIM_INTPRIORITY_239 Registers

4.24.317.1 VIM_239 Register (Offset = 13BCh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h243

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h243

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Table 4-3740. Instance Table

Instance Name	Physical Address
VIM	50F0 13BCh

Figure 4-1775. INTPRIORITY_239 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3741. INTPRIORITY_239 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.318 VIM_MSS_VIM_INTPRIORITY_240 Registers

4.24.318.1 VIM_240 Register (Offset = 13C0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h244

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h244

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Table 4-3742. Instance Table

Instance Name	Physical Address
VIM	50F0 13C0h

Figure 4-1776. INTPRIORITY_240 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3743. INTPRIORITY_240 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.319 VIM_MSS_VIM_INTPRIORITY_241 Registers

4.24.319.1 VIM_241 Register (Offset = 13C4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h245

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h245

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Table 4-3744. Instance Table

Instance Name	Physical Address
VIM	50F0 13C4h

Figure 4-1777. INTPRIORITY_241 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3745. INTPRIORITY_241 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.320 VIM_MSS_VIM_INTPRIORITY_242 Registers

4.24.320.1 VIM_242 Register (Offset = 13C8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h246

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h246

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Table 4-3746. Instance Table

Instance Name	Physical Address
VIM	50F0 13C8h

Figure 4-1778. INTPRIORITY_242 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3747. INTPRIORITY_242 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.321 VIM_MSS_VIM_INTPRIORITY_243 Registers

4.24.321.1 VIM_243 Register (Offset = 13CCh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h247

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h247

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Table 4-3748. Instance Table

Instance Name	Physical Address
VIM	50F0 13CCh

Figure 4-1779. INTPRIORITY_243 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3749. INTPRIORITY_243 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.322 VIM_MSS_VIM_INTPRIORITY_244 Registers

4.24.322.1 VIM_244 Register (Offset = 13D0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h248

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h248

Return to Summary Table

Table 4-3750. Instance Table

Instance Name	Physical Address
VIM	50F0 13D0h

Figure 4-1780. INTPRIORITY_244 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3751. INTPRIORITY_244 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.323 VIM_MSS_VIM_INTPRIORITY_245 Registers

4.24.323.1 VIM_245 Register (Offset = 13D4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h249

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h249

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Table 4-3752. Instance Table

Instance Name	Physical Address
VIM	50F0 13D4h

Figure 4-1781. INTPRIORITY_245 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3753. INTPRIORITY_245 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.324 VIM_MSS_VIM_INTPRIORITY_246 Registers

4.24.324.1 VIM_246 Register (Offset = 13D8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h250

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h250

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Table 4-3754. Instance Table

Instance Name	Physical Address
VIM	50F0 13D8h

Figure 4-1782. INTPRIORITY_246 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3755. INTPRIORITY_246 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.325 VIM_MSS_VIM_INTPRIORITY_247 Registers

4.24.325.1 VIM_247 Register (Offset = 13DCh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h251

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h251

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Table 4-3756. Instance Table

Instance Name	Physical Address
VIM	50F0 13DCh

Figure 4-1783. INTPRIORITY_247 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3757. INTPRIORITY_247 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.326 VIM_MSS_VIM_INTPRIORITY_248 Registers

4.24.326.1 VIM_248 Register (Offset = 13E0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h252

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h252

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Table 4-3758. Instance Table

Instance Name	Physical Address
VIM	50F0 13E0h

Figure 4-1784. INTPRIORITY_248 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3759. INTPRIORITY_248 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.327 VIM_MSS_VIM_INTPRIORITY_249 Registers

4.24.327.1 VIM_249 Register (Offset = 13E4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h253

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h253

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Table 4-3760. Instance Table

Instance Name	Physical Address
VIM	50F0 13E4h

Figure 4-1785. INTPRIORITY_249 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3761. INTPRIORITY_249 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.328 VIM_MSS_VIM_INTPRIORITY_250 Registers

4.24.328.1 VIM_250 Register (Offset = 13E8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h254

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h254

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Table 4-3762. Instance Table

Instance Name	Physical Address
VIM	50F0 13E8h

Figure 4-1786. INTPRIORITY_250 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3763. INTPRIORITY_250 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.329 VIM_MSS_VIM_INTPRIORITY_251 Registers

4.24.329.1 VIM_251 Register (Offset = 13ECh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h255

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h255

Return to Summary Table

Table 4-3764. Instance Table

Instance Name	Physical Address
VIM	50F0 13ECh

Figure 4-1787. INTPRIORITY_251 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3765. INTPRIORITY_251 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.330 VIM_MSS_VIM_INTPRIORITY_252 Registers

4.24.330.1 VIM_252 Register (Offset = 13F0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h256

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h256

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Table 4-3766. Instance Table

Instance Name	Physical Address
VIM	50F0 13F0h

Figure 4-1788. INTPRIORITY_252 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3767. INTPRIORITY_252 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.331 VIM_MSS_VIM_INTPRIORITY_253 Registers

4.24.331.1 VIM_253 Register (Offset = 13F4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h257

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h257

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Table 4-3768. Instance Table

Instance Name	Physical Address
VIM	50F0 13F4h

Figure 4-1789. INTPRIORITY_253 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3769. INTPRIORITY_253 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.332 VIM_MSS_VIM_INTPRIORITY_254 Registers

4.24.332.1 VIM_254 Register (Offset = 13F8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h258

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h258

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Table 4-3770. Instance Table

Instance Name	Physical Address
VIM	50F0 13F8h

Figure 4-1790. INTPRIORITY_254 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3771. INTPRIORITY_254 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.333 VIM_MSS_VIM_INTPRIORITY_255 Registers

4.24.333.1 VIM_255 Register (Offset = 13FCh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h259

Long Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h259

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Table 4-3772. Instance Table

Instance Name	Physical Address
VIM	50F0 13FCh

Figure 4-1791. INTPRIORITY_255 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												15			

Access Types Legend

Table 4-3773. INTPRIORITY_255 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.24.334 VIM_MSS_VIM_INTVECTOR Registers

4.24.334.1 VIM_INTVECTOR Register (Offset = 2000h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h4

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h4

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Table 4-3774. Instance Table

Instance Name	Physical Address
VIM	50F0 2000h

Figure 4-1792. INTVECTOR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3775. INTVECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.335 VIM_MSS_VIM_INTVECTOR_1 Registers

4.24.335.1 VIM_1 Register (Offset = 2004h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h5

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h5

Return to Summary Table

Table 4-3776. Instance Table

Instance Name	Physical Address
VIM	50F0 2004h

Figure 4-1793. INTVECTOR_1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3777. INTVECTOR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.336 VIM_MSS_VIM_INTVECTOR_2 Registers

4.24.336.1 VIM_2 Register (Offset = 2008h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h6

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h6

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Table 4-3778. Instance Table

Instance Name	Physical Address
VIM	50F0 2008h

Figure 4-1794. INTVECTOR_2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3779. INTVECTOR_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.337 VIM_MSS_VIM_INTVECTOR_3 Registers

4.24.337.1 VIM_3 Register (Offset = 200Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h7

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h7

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Table 4-3780. Instance Table

Instance Name	Physical Address
VIM	50F0 200Ch

Figure 4-1795. INTVECTOR_3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3781. INTVECTOR_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.338 VIM_MSS_VIM_INTVECTOR_4 Registers

4.24.338.1 VIM_4 Register (Offset = 2010h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h8

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h8

Return to Summary Table

Table 4-3782. Instance Table

Instance Name	Physical Address
VIM	50F0 2010h

Figure 4-1796. INTVECTOR_4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3783. INTVECTOR_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.339 VIM_MSS_VIM_INTVECTOR_5 Registers

4.24.339.1 VIM_5 Register (Offset = 2014h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h9

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h9

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Table 4-3784. Instance Table

Instance Name	Physical Address
VIM	50F0 2014h

Figure 4-1797. INTVECTOR_5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3785. INTVECTOR_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.340 VIM_MSS_VIM_INTVECTOR_6 Registers

4.24.340.1 VIM_6 Register (Offset = 2018h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h10

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h10

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Table 4-3786. Instance Table

Instance Name	Physical Address
VIM	50F0 2018h

Figure 4-1798. INTVECTOR_6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3787. INTVECTOR_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.341 VIM_MSS_VIM_INTVECTOR_7 Registers

4.24.341.1 VIM_7 Register (Offset = 201Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h11

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h11

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Table 4-3788. Instance Table

Instance Name	Physical Address
VIM	50F0 201Ch

Figure 4-1799. INTVECTOR_7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3789. INTVECTOR_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.342 VIM_MSS_VIM_INTVECTOR_8 Registers

4.24.342.1 VIM_8 Register (Offset = 2020h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h12

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h12

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Table 4-3790. Instance Table

Instance Name	Physical Address
VIM	50F0 2020h

Figure 4-1800. INTVECTOR_8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3791. INTVECTOR_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.343 VIM_MSS_VIM_INTVECTOR_9 Registers

4.24.343.1 VIM_9 Register (Offset = 2024h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h13

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h13

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Table 4-3792. Instance Table

Instance Name	Physical Address
VIM	50F0 2024h

Figure 4-1801. INTVECTOR_9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3793. INTVECTOR_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.344 VIM_MSS_VIM_INTVECTOR_10 Registers

4.24.344.1 VIM_10 Register (Offset = 2028h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h14

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h14

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Table 4-3794. Instance Table

Instance Name	Physical Address
VIM	50F0 2028h

Figure 4-1802. INTVECTOR_10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3795. INTVECTOR_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.345 VIM_MSS_VIM_INTVECTOR_11 Registers

4.24.345.1 VIM_11 Register (Offset = 202Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h15

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h15

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Table 4-3796. Instance Table

Instance Name	Physical Address
VIM	50F0 202Ch

Figure 4-1803. INTVECTOR_11 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3797. INTVECTOR_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.346 VIM_MSS_VIM_INTVECTOR_12 Registers

4.24.346.1 VIM_12 Register (Offset = 2030h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h16

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h16

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Table 4-3798. Instance Table

Instance Name	Physical Address
VIM	50F0 2030h

Figure 4-1804. INTVECTOR_12 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3799. INTVECTOR_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.347 VIM_MSS_VIM_INTVECTOR_13 Registers

4.24.347.1 VIM_13 Register (Offset = 2034h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h17

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h17

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Table 4-3800. Instance Table

Instance Name	Physical Address
VIM	50F0 2034h

Figure 4-1805. INTVECTOR_13 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3801. INTVECTOR_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.348 VIM_MSS_VIM_INTVECTOR_14 Registers

4.24.348.1 VIM_14 Register (Offset = 2038h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h18

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h18

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Table 4-3802. Instance Table

Instance Name	Physical Address
VIM	50F0 2038h

Figure 4-1806. INTVECTOR_14 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3803. INTVECTOR_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.349 VIM_MSS_VIM_INTVECTOR_15 Registers

4.24.349.1 VIM_15 Register (Offset = 203Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h19

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h19

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Table 4-3804. Instance Table

Instance Name	Physical Address
VIM	50F0 203Ch

Figure 4-1807. INTVECTOR_15 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3805. INTVECTOR_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.350 VIM_MSS_VIM_INTVECTOR_16 Registers

4.24.350.1 VIM_16 Register (Offset = 2040h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h20

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h20

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Table 4-3806. Instance Table

Instance Name	Physical Address
VIM	50F0 2040h

Figure 4-1808. INTVECTOR_16 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3807. INTVECTOR_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.351 VIM_MSS_VIM_INTVECTOR_17 Registers

4.24.351.1 VIM_17 Register (Offset = 2044h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h21

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h21

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Table 4-3808. Instance Table

Instance Name	Physical Address
VIM	50F0 2044h

Figure 4-1809. INTVECTOR_17 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3809. INTVECTOR_17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.352 VIM_MSS_VIM_INTVECTOR_18 Registers

4.24.352.1 VIM_18 Register (Offset = 2048h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h22

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h22

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Table 4-3810. Instance Table

Instance Name	Physical Address
VIM	50F0 2048h

Figure 4-1810. INTVECTOR_18 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3811. INTVECTOR_18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.353 VIM_MSS_VIM_INTVECTOR_19 Registers

4.24.353.1 VIM_19 Register (Offset = 204Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h23

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h23

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Table 4-3812. Instance Table

Instance Name	Physical Address
VIM	50F0 204Ch

Figure 4-1811. INTVECTOR_19 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3813. INTVECTOR_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.354 VIM_MSS_VIM_INTVECTOR_20 Registers

4.24.354.1 VIM_20 Register (Offset = 2050h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h24

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h24

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Table 4-3814. Instance Table

Instance Name	Physical Address
VIM	50F0 2050h

Figure 4-1812. INTVECTOR_20 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3815. INTVECTOR_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.355 VIM_MSS_VIM_INTVECTOR_21 Registers

4.24.355.1 VIM_21 Register (Offset = 2054h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h25

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h25

Return to Summary Table

Table 4-3816. Instance Table

Instance Name	Physical Address
VIM	50F0 2054h

Figure 4-1813. INTVECTOR_21 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3817. INTVECTOR_21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.356 VIM_MSS_VIM_INTVECTOR_22 Registers

4.24.356.1 VIM_22 Register (Offset = 2058h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h26

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h26

Return to Summary Table

Table 4-3818. Instance Table

Instance Name	Physical Address
VIM	50F0 2058h

Figure 4-1814. INTVECTOR_22 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3819. INTVECTOR_22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.357 VIM_MSS_VIM_INTVECTOR_23 Registers

4.24.357.1 VIM_23 Register (Offset = 205Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h27

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h27

Return to Summary Table

Table 4-3820. Instance Table

Instance Name	Physical Address
VIM	50F0 205Ch

Figure 4-1815. INTVECTOR_23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3821. INTVECTOR_23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.358 VIM_MSS_VIM_INTVECTOR_24 Registers

4.24.358.1 VIM_24 Register (Offset = 2060h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h28

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h28

Return to Summary Table

Table 4-3822. Instance Table

Instance Name	Physical Address
VIM	50F0 2060h

Figure 4-1816. INTVECTOR_24 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3823. INTVECTOR_24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.359 VIM_MSS_VIM_INTVECTOR_25 Registers

4.24.359.1 VIM_25 Register (Offset = 2064h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h29

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h29

Return to Summary Table

Table 4-3824. Instance Table

Instance Name	Physical Address
VIM	50F0 2064h

Figure 4-1817. INTVECTOR_25 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3825. INTVECTOR_25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.360 VIM_MSS_VIM_INTVECTOR_26 Registers

4.24.360.1 VIM_26 Register (Offset = 2068h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h30

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h30

Return to Summary Table

Table 4-3826. Instance Table

Instance Name	Physical Address
VIM	50F0 2068h

Figure 4-1818. INTVECTOR_26 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3827. INTVECTOR_26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.361 VIM_MSS_VIM_INTVECTOR_27 Registers

4.24.361.1 VIM_27 Register (Offset = 206Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h31

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h31

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Table 4-3828. Instance Table

Instance Name	Physical Address
VIM	50F0 206Ch

Figure 4-1819. INTVECTOR_27 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3829. INTVECTOR_27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.362 VIM_MSS_VIM_INTVECTOR_28 Registers

4.24.362.1 VIM_28 Register (Offset = 2070h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h32

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h32

Return to Summary Table

Table 4-3830. Instance Table

Instance Name	Physical Address
VIM	50F0 2070h

Figure 4-1820. INTVECTOR_28 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3831. INTVECTOR_28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.363 VIM_MSS_VIM_INTVECTOR_29 Registers

4.24.363.1 VIM_29 Register (Offset = 2074h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h33

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h33

Return to Summary Table

Table 4-3832. Instance Table

Instance Name	Physical Address
VIM	50F0 2074h

Figure 4-1821. INTVECTOR_29 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3833. INTVECTOR_29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.364 VIM_MSS_VIM_INTVECTOR_30 Registers

4.24.364.1 VIM_30 Register (Offset = 2078h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h34

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h34

Return to Summary Table

Table 4-3834. Instance Table

Instance Name	Physical Address
VIM	50F0 2078h

Figure 4-1822. INTVECTOR_30 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3835. INTVECTOR_30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.365 VIM_MSS_VIM_INTVECTOR_31 Registers

4.24.365.1 VIM_31 Register (Offset = 207Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h35

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h35

Return to Summary Table

Table 4-3836. Instance Table

Instance Name	Physical Address
VIM	50F0 207Ch

Figure 4-1823. INTVECTOR_31 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3837. INTVECTOR_31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.366 VIM_MSS_VIM_INTVECTOR_32 Registers

4.24.366.1 VIM_32 Register (Offset = 2080h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h36

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h36

Return to Summary Table

Table 4-3838. Instance Table

Instance Name	Physical Address
VIM	50F0 2080h

Figure 4-1824. INTVECTOR_32 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3839. INTVECTOR_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.367 VIM_MSS_VIM_INTVECTOR_33 Registers

4.24.367.1 VIM_33 Register (Offset = 2084h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h37

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h37

Return to Summary Table

Table 4-3840. Instance Table

Instance Name	Physical Address
VIM	50F0 2084h

Figure 4-1825. INTVECTOR_33 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3841. INTVECTOR_33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.368 VIM_MSS_VIM_INTVECTOR_34 Registers

4.24.368.1 VIM_34 Register (Offset = 2088h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h38

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h38

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Table 4-3842. Instance Table

Instance Name	Physical Address
VIM	50F0 2088h

Figure 4-1826. INTVECTOR_34 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3843. INTVECTOR_34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.369 VIM_MSS_VIM_INTVECTOR_35 Registers

4.24.369.1 VIM_35 Register (Offset = 208Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h39

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h39

Return to Summary Table

Table 4-3844. Instance Table

Instance Name	Physical Address
VIM	50F0 208Ch

Figure 4-1827. INTVECTOR_35 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3845. INTVECTOR_35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.370 VIM_MSS_VIM_INTVECTOR_36 Registers

4.24.370.1 VIM_36 Register (Offset = 2090h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h40

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h40

Return to Summary Table

Table 4-3846. Instance Table

Instance Name	Physical Address
VIM	50F0 2090h

Figure 4-1828. INTVECTOR_36 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3847. INTVECTOR_36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.371 VIM_MSS_VIM_INTVECTOR_37 Registers

4.24.371.1 VIM_37 Register (Offset = 2094h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h41

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h41

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Table 4-3848. Instance Table

Instance Name	Physical Address
VIM	50F0 2094h

Figure 4-1829. INTVECTOR_37 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3849. INTVECTOR_37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.372 VIM_MSS_VIM_INTVECTOR_38 Registers

4.24.372.1 VIM_38 Register (Offset = 2098h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h42

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h42

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Table 4-3850. Instance Table

Instance Name	Physical Address
VIM	50F0 2098h

Figure 4-1830. INTVECTOR_38 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3851. INTVECTOR_38 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.373 VIM_MSS_VIM_INTVECTOR_39 Registers

4.24.373.1 VIM_39 Register (Offset = 209Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h43

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h43

Return to Summary Table

Table 4-3852. Instance Table

Instance Name	Physical Address
VIM	50F0 209Ch

Figure 4-1831. INTVECTOR_39 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3853. INTVECTOR_39 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.374 VIM_MSS_VIM_INTVECTOR_40 Registers

4.24.374.1 VIM_40 Register (Offset = 20A0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h44

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h44

Return to Summary Table

Table 4-3854. Instance Table

Instance Name	Physical Address
VIM	50F0 20A0h

Figure 4-1832. INTVECTOR_40 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3855. INTVECTOR_40 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.375 VIM_MSS_VIM_INTVECTOR_41 Registers

4.24.375.1 VIM_41 Register (Offset = 20A4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h45

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h45

Return to Summary Table

Table 4-3856. Instance Table

Instance Name	Physical Address
VIM	50F0 20A4h

Figure 4-1833. INTVECTOR_41 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3857. INTVECTOR_41 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.376 VIM_MSS_VIM_INTVECTOR_42 Registers

4.24.376.1 VIM_42 Register (Offset = 20A8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h46

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h46

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Table 4-3858. Instance Table

Instance Name	Physical Address
VIM	50F0 20A8h

Figure 4-1834. INTVECTOR_42 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3859. INTVECTOR_42 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.377 VIM_MSS_VIM_INTVECTOR_43 Registers

4.24.377.1 VIM_43 Register (Offset = 20ACh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h47

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h47

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Table 4-3860. Instance Table

Instance Name	Physical Address
VIM	50F0 20ACh

Figure 4-1835. INTVECTOR_43 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3861. INTVECTOR_43 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.378 VIM_MSS_VIM_INTVECTOR_44 Registers

4.24.378.1 VIM_44 Register (Offset = 20B0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h48

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h48

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Table 4-3862. Instance Table

Instance Name	Physical Address
VIM	50F0 20B0h

Figure 4-1836. INTVECTOR_44 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3863. INTVECTOR_44 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.379 VIM_MSS_VIM_INTVECTOR_45 Registers

4.24.379.1 VIM_45 Register (Offset = 20B4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h49

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h49

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Table 4-3864. Instance Table

Instance Name	Physical Address
VIM	50F0 20B4h

Figure 4-1837. INTVECTOR_45 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3865. INTVECTOR_45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.380 VIM_MSS_VIM_INTVECTOR_46 Registers

4.24.380.1 VIM_46 Register (Offset = 20B8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h50

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h50

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Table 4-3866. Instance Table

Instance Name	Physical Address
VIM	50F0 20B8h

Figure 4-1838. INTVECTOR_46 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3867. INTVECTOR_46 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.381 VIM_MSS_VIM_INTVECTOR_47 Registers

4.24.381.1 VIM_47 Register (Offset = 20BCh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h51

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h51

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Table 4-3868. Instance Table

Instance Name	Physical Address
VIM	50F0 20BCh

Figure 4-1839. INTVECTOR_47 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3869. INTVECTOR_47 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.382 VIM_MSS_VIM_INTVECTOR_48 Registers

4.24.382.1 VIM_48 Register (Offset = 20C0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h52

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h52

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Table 4-3870. Instance Table

Instance Name	Physical Address
VIM	50F0 20C0h

Figure 4-1840. INTVECTOR_48 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3871. INTVECTOR_48 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.383 VIM_MSS_VIM_INTVECTOR_49 Registers

4.24.383.1 VIM_49 Register (Offset = 20C4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h53

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h53

Return to Summary Table

Table 4-3872. Instance Table

Instance Name	Physical Address
VIM	50F0 20C4h

Figure 4-1841. INTVECTOR_49 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3873. INTVECTOR_49 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.384 VIM_MSS_VIM_INTVECTOR_50 Registers

4.24.384.1 VIM_50 Register (Offset = 20C8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h54

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h54

Return to Summary Table

Table 4-3874. Instance Table

Instance Name	Physical Address
VIM	50F0 20C8h

Figure 4-1842. INTVECTOR_50 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3875. INTVECTOR_50 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.385 VIM_MSS_VIM_INTVECTOR_51 Registers

4.24.385.1 VIM_51 Register (Offset = 20CCh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h55

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h55

Return to Summary Table

Table 4-3876. Instance Table

Instance Name	Physical Address
VIM	50F0 20CCh

Figure 4-1843. INTVECTOR_51 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3877. INTVECTOR_51 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.386 VIM_MSS_VIM_INTVECTOR_52 Registers

4.24.386.1 VIM_52 Register (Offset = 20D0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h56

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h56

Return to Summary Table

Table 4-3878. Instance Table

Instance Name	Physical Address
VIM	50F0 20D0h

Figure 4-1844. INTVECTOR_52 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3879. INTVECTOR_52 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.387 VIM_MSS_VIM_INTVECTOR_53 Registers

4.24.387.1 VIM_53 Register (Offset = 20D4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h57

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h57

Return to Summary Table

Table 4-3880. Instance Table

Instance Name	Physical Address
VIM	50F0 20D4h

Figure 4-1845. INTVECTOR_53 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3881. INTVECTOR_53 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.388 VIM_MSS_VIM_INTVECTOR_54 Registers

4.24.388.1 VIM_54 Register (Offset = 20D8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h58

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h58

Return to Summary Table

Table 4-3882. Instance Table

Instance Name	Physical Address
VIM	50F0 20D8h

Figure 4-1846. INTVECTOR_54 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3883. INTVECTOR_54 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.389 VIM_MSS_VIM_INTVECTOR_55 Registers

4.24.389.1 VIM_55 Register (Offset = 20DCh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h59

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h59

Return to Summary Table

Table 4-3884. Instance Table

Instance Name	Physical Address
VIM	50F0 20DCh

Figure 4-1847. INTVECTOR_55 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3885. INTVECTOR_55 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.390 VIM_MSS_VIM_INTVECTOR_56 Registers

4.24.390.1 VIM_56 Register (Offset = 20E0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h60

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h60

Return to Summary Table

Table 4-3886. Instance Table

Instance Name	Physical Address
VIM	50F0 20E0h

Figure 4-1848. INTVECTOR_56 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3887. INTVECTOR_56 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.391 VIM_MSS_VIM_INTVECTOR_57 Registers

4.24.391.1 VIM_57 Register (Offset = 20E4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h61

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h61

Return to Summary Table

Table 4-3888. Instance Table

Instance Name	Physical Address
VIM	50F0 20E4h

Figure 4-1849. INTVECTOR_57 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3889. INTVECTOR_57 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.392 VIM_MSS_VIM_INTVECTOR_58 Registers

4.24.392.1 VIM_58 Register (Offset = 20E8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h62

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h62

Return to Summary Table

Table 4-3890. Instance Table

Instance Name	Physical Address
VIM	50F0 20E8h

Figure 4-1850. INTVECTOR_58 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3891. INTVECTOR_58 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.393 VIM_MSS_VIM_INTVECTOR_59 Registers

4.24.393.1 VIM_59 Register (Offset = 20ECh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h63

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h63

Return to Summary Table

Table 4-3892. Instance Table

Instance Name	Physical Address
VIM	50F0 20ECh

Figure 4-1851. INTVECTOR_59 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3893. INTVECTOR_59 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.394 VIM_MSS_VIM_INTVECTOR_60 Registers

4.24.394.1 VIM_60 Register (Offset = 20F0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h64

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h64

Return to Summary Table

Table 4-3894. Instance Table

Instance Name	Physical Address
VIM	50F0 20F0h

Figure 4-1852. INTVECTOR_60 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3895. INTVECTOR_60 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.395 VIM_MSS_VIM_INTVECTOR_61 Registers

4.24.395.1 VIM_61 Register (Offset = 20F4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h65

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h65

Return to Summary Table

Table 4-3896. Instance Table

Instance Name	Physical Address
VIM	50F0 20F4h

Figure 4-1853. INTVECTOR_61 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3897. INTVECTOR_61 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.396 VIM_MSS_VIM_INTVECTOR_62 Registers

4.24.396.1 VIM_62 Register (Offset = 20F8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h66

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h66

Return to Summary Table

Table 4-3898. Instance Table

Instance Name	Physical Address
VIM	50F0 20F8h

Figure 4-1854. INTVECTOR_62 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3899. INTVECTOR_62 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.397 VIM_MSS_VIM_INTVECTOR_63 Registers

4.24.397.1 VIM_63 Register (Offset = 20FCh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h67

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h67

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Table 4-3900. Instance Table

Instance Name	Physical Address
VIM	50F0 20FCh

Figure 4-1855. INTVECTOR_63 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3901. INTVECTOR_63 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.398 VIM_MSS_VIM_INTVECTOR_64 Registers

4.24.398.1 VIM_64 Register (Offset = 2100h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h68

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h68

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Table 4-3902. Instance Table

Instance Name	Physical Address
VIM	50F0 2100h

Figure 4-1856. INTVECTOR_64 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3903. INTVECTOR_64 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.399 VIM_MSS_VIM_INTVECTOR_65 Registers

4.24.399.1 VIM_65 Register (Offset = 2104h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h69

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h69

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Table 4-3904. Instance Table

Instance Name	Physical Address
VIM	50F0 2104h

Figure 4-1857. INTVECTOR_65 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3905. INTVECTOR_65 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.400 VIM_MSS_VIM_INTVECTOR_66 Registers

4.24.400.1 VIM_66 Register (Offset = 2108h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h70

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h70

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Table 4-3906. Instance Table

Instance Name	Physical Address
VIM	50F0 2108h

Figure 4-1858. INTVECTOR_66 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3907. INTVECTOR_66 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.401 VIM_MSS_VIM_INTVECTOR_67 Registers

4.24.401.1 VIM_67 Register (Offset = 210Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h71

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h71

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Table 4-3908. Instance Table

Instance Name	Physical Address
VIM	50F0 210Ch

Figure 4-1859. INTVECTOR_67 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3909. INTVECTOR_67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.402 VIM_MSS_VIM_INTVECTOR_68 Registers

4.24.402.1 VIM_68 Register (Offset = 2110h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h72

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h72

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Table 4-3910. Instance Table

Instance Name	Physical Address
VIM	50F0 2110h

Figure 4-1860. INTVECTOR_68 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3911. INTVECTOR_68 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.403 VIM_MSS_VIM_INTVECTOR_69 Registers

4.24.403.1 VIM_69 Register (Offset = 2114h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h73

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h73

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Table 4-3912. Instance Table

Instance Name	Physical Address
VIM	50F0 2114h

Figure 4-1861. INTVECTOR_69 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3913. INTVECTOR_69 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.404 VIM_MSS_VIM_INTVECTOR_70 Registers

4.24.404.1 VIM_70 Register (Offset = 2118h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h74

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h74

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Table 4-3914. Instance Table

Instance Name	Physical Address
VIM	50F0 2118h

Figure 4-1862. INTVECTOR_70 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3915. INTVECTOR_70 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.405 VIM_MSS_VIM_INTVECTOR_71 Registers

4.24.405.1 VIM_71 Register (Offset = 211Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h75

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h75

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Table 4-3916. Instance Table

Instance Name	Physical Address
VIM	50F0 211Ch

Figure 4-1863. INTVECTOR_71 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3917. INTVECTOR_71 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.406 VIM_MSS_VIM_INTVECTOR_72 Registers

4.24.406.1 VIM_72 Register (Offset = 2120h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h76

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h76

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Table 4-3918. Instance Table

Instance Name	Physical Address
VIM	50F0 2120h

Figure 4-1864. INTVECTOR_72 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3919. INTVECTOR_72 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.407 VIM_MSS_VIM_INTVECTOR_73 Registers

4.24.407.1 VIM_73 Register (Offset = 2124h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h77

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h77

Return to Summary Table

Table 4-3920. Instance Table

Instance Name	Physical Address
VIM	50F0 2124h

Figure 4-1865. INTVECTOR_73 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3921. INTVECTOR_73 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.408 VIM_MSS_VIM_INTVECTOR_74 Registers

4.24.408.1 VIM_74 Register (Offset = 2128h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h78

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h78

Return to Summary Table

Table 4-3922. Instance Table

Instance Name	Physical Address
VIM	50F0 2128h

Figure 4-1866. INTVECTOR_74 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3923. INTVECTOR_74 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.409 VIM_MSS_VIM_INTVECTOR_75 Registers

4.24.409.1 VIM_75 Register (Offset = 212Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h79

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h79

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Table 4-3924. Instance Table

Instance Name	Physical Address
VIM	50F0 212Ch

Figure 4-1867. INTVECTOR_75 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3925. INTVECTOR_75 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.410 VIM_MSS_VIM_INTVECTOR_76 Registers

4.24.410.1 VIM_76 Register (Offset = 2130h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h80

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h80

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Table 4-3926. Instance Table

Instance Name	Physical Address
VIM	50F0 2130h

Figure 4-1868. INTVECTOR_76 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3927. INTVECTOR_76 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.411 VIM_MSS_VIM_INTVECTOR_77 Registers

4.24.411.1 VIM_77 Register (Offset = 2134h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h81

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h81

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Table 4-3928. Instance Table

Instance Name	Physical Address
VIM	50F0 2134h

Figure 4-1869. INTVECTOR_77 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3929. INTVECTOR_77 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.412 VIM_MSS_VIM_INTVECTOR_78 Registers

4.24.412.1 VIM_78 Register (Offset = 2138h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h82

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h82

Return to Summary Table

Table 4-3930. Instance Table

Instance Name	Physical Address
VIM	50F0 2138h

Figure 4-1870. INTVECTOR_78 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3931. INTVECTOR_78 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.413 VIM_MSS_VIM_INTVECTOR_79 Registers

4.24.413.1 VIM_79 Register (Offset = 213Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h83

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h83

Return to Summary Table

Table 4-3932. Instance Table

Instance Name	Physical Address
VIM	50F0 213Ch

Figure 4-1871. INTVECTOR_79 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3933. INTVECTOR_79 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.414 VIM_MSS_VIM_INTVECTOR_80 Registers

4.24.414.1 VIM_80 Register (Offset = 2140h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h84

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h84

Return to Summary Table

Table 4-3934. Instance Table

Instance Name	Physical Address
VIM	50F0 2140h

Figure 4-1872. INTVECTOR_80 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3935. INTVECTOR_80 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.415 VIM_MSS_VIM_INTVECTOR_81 Registers

4.24.415.1 VIM_81 Register (Offset = 2144h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h85

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h85

Return to Summary Table

Table 4-3936. Instance Table

Instance Name	Physical Address
VIM	50F0 2144h

Figure 4-1873. INTVECTOR_81 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3937. INTVECTOR_81 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.416 VIM_MSS_VIM_INTVECTOR_82 Registers

4.24.416.1 VIM_82 Register (Offset = 2148h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h86

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h86

Return to Summary Table

Table 4-3938. Instance Table

Instance Name	Physical Address
VIM	50F0 2148h

Figure 4-1874. INTVECTOR_82 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3939. INTVECTOR_82 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.417 VIM_MSS_VIM_INTVECTOR_83 Registers

4.24.417.1 VIM_83 Register (Offset = 214Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h87

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h87

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Table 4-3940. Instance Table

Instance Name	Physical Address
VIM	50F0 214Ch

Figure 4-1875. INTVECTOR_83 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3941. INTVECTOR_83 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.418 VIM_MSS_VIM_INTVECTOR_84 Registers

4.24.418.1 VIM_84 Register (Offset = 2150h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h88

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h88

Return to Summary Table

Table 4-3942. Instance Table

Instance Name	Physical Address
VIM	50F0 2150h

Figure 4-1876. INTVECTOR_84 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3943. INTVECTOR_84 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.419 VIM_MSS_VIM_INTVECTOR_85 Registers

4.24.419.1 VIM_85 Register (Offset = 2154h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h89

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h89

Return to Summary Table

Table 4-3944. Instance Table

Instance Name	Physical Address
VIM	50F0 2154h

Figure 4-1877. INTVECTOR_85 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3945. INTVECTOR_85 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.420 VIM_MSS_VIM_INTVECTOR_86 Registers

4.24.420.1 VIM_86 Register (Offset = 2158h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h90

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h90

Return to Summary Table

Table 4-3946. Instance Table

Instance Name	Physical Address
VIM	50F0 2158h

Figure 4-1878. INTVECTOR_86 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3947. INTVECTOR_86 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.421 VIM_MSS_VIM_INTVECTOR_87 Registers

4.24.421.1 VIM_87 Register (Offset = 215Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h91

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h91

Return to Summary Table

Table 4-3948. Instance Table

Instance Name	Physical Address
VIM	50F0 215Ch

Figure 4-1879. INTVECTOR_87 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3949. INTVECTOR_87 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.422 VIM_MSS_VIM_INTVECTOR_88 Registers

4.24.422.1 VIM_88 Register (Offset = 2160h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h92

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h92

Return to Summary Table

Table 4-3950. Instance Table

Instance Name	Physical Address
VIM	50F0 2160h

Figure 4-1880. INTVECTOR_88 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3951. INTVECTOR_88 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.423 VIM_MSS_VIM_INTVECTOR_89 Registers

4.24.423.1 VIM_89 Register (Offset = 2164h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h93

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h93

Return to Summary Table

Table 4-3952. Instance Table

Instance Name	Physical Address
VIM	50F0 2164h

Figure 4-1881. INTVECTOR_89 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3953. INTVECTOR_89 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.424 VIM_MSS_VIM_INTVECTOR_90 Registers

4.24.424.1 VIM_90 Register (Offset = 2168h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h94

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h94

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Table 4-3954. Instance Table

Instance Name	Physical Address
VIM	50F0 2168h

Figure 4-1882. INTVECTOR_90 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3955. INTVECTOR_90 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.425 VIM_MSS_VIM_INTVECTOR_91 Registers

4.24.425.1 VIM_91 Register (Offset = 216Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h95

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h95

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Table 4-3956. Instance Table

Instance Name	Physical Address
VIM	50F0 216Ch

Figure 4-1883. INTVECTOR_91 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3957. INTVECTOR_91 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.426 VIM_MSS_VIM_INTVECTOR_92 Registers

4.24.426.1 VIM_92 Register (Offset = 2170h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h96

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h96

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Table 4-3958. Instance Table

Instance Name	Physical Address
VIM	50F0 2170h

Figure 4-1884. INTVECTOR_92 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3959. INTVECTOR_92 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.427 VIM_MSS_VIM_INTVECTOR_93 Registers

4.24.427.1 VIM_93 Register (Offset = 2174h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h97

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h97

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Table 4-3960. Instance Table

Instance Name	Physical Address
VIM	50F0 2174h

Figure 4-1885. INTVECTOR_93 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3961. INTVECTOR_93 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.428 VIM_MSS_VIM_INTVECTOR_94 Registers

4.24.428.1 VIM_94 Register (Offset = 2178h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h98

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h98

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Table 4-3962. Instance Table

Instance Name	Physical Address
VIM	50F0 2178h

Figure 4-1886. INTVECTOR_94 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3963. INTVECTOR_94 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.429 VIM_MSS_VIM_INTVECTOR_95 Registers

4.24.429.1 VIM_95 Register (Offset = 217Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h99

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h99

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Table 4-3964. Instance Table

Instance Name	Physical Address
VIM	50F0 217Ch

Figure 4-1887. INTVECTOR_95 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3965. INTVECTOR_95 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.430 VIM_MSS_VIM_INTVECTOR_96 Registers

4.24.430.1 VIM_96 Register (Offset = 2180h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h100

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h100

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Table 4-3966. Instance Table

Instance Name	Physical Address
VIM	50F0 2180h

Figure 4-1888. INTVECTOR_96 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3967. INTVECTOR_96 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.431 VIM_MSS_VIM_INTVECTOR_97 Registers

4.24.431.1 VIM_97 Register (Offset = 2184h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h101

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h101

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Table 4-3968. Instance Table

Instance Name	Physical Address
VIM	50F0 2184h

Figure 4-1889. INTVECTOR_97 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3969. INTVECTOR_97 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.432 VIM_MSS_VIM_INTVECTOR_98 Registers

4.24.432.1 VIM_98 Register (Offset = 2188h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h102

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h102

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Table 4-3970. Instance Table

Instance Name	Physical Address
VIM	50F0 2188h

Figure 4-1890. INTVECTOR_98 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3971. INTVECTOR_98 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.433 VIM_MSS_VIM_INTVECTOR_99 Registers

4.24.433.1 VIM_99 Register (Offset = 218Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h103

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h103

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Table 4-3972. Instance Table

Instance Name	Physical Address
VIM	50F0 218Ch

Figure 4-1891. INTVECTOR_99 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3973. INTVECTOR_99 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.434 VIM_MSS_VIM_INTVECTOR_100 Registers

4.24.434.1 VIM_100 Register (Offset = 2190h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h104

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h104

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Table 4-3974. Instance Table

Instance Name	Physical Address
VIM	50F0 2190h

Figure 4-1892. INTVECTOR_100 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3975. INTVECTOR_100 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.435 VIM_MSS_VIM_INTVECTOR_101 Registers

4.24.435.1 VIM_101 Register (Offset = 2194h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h105

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h105

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Table 4-3976. Instance Table

Instance Name	Physical Address
VIM	50F0 2194h

Figure 4-1893. INTVECTOR_101 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3977. INTVECTOR_101 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.436 VIM_MSS_VIM_INTVECTOR_102 Registers

4.24.436.1 VIM_102 Register (Offset = 2198h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h106

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h106

Return to Summary Table

Table 4-3978. Instance Table

Instance Name	Physical Address
VIM	50F0 2198h

Figure 4-1894. INTVECTOR_102 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3979. INTVECTOR_102 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.437 VIM_MSS_VIM_INTVECTOR_103 Registers

4.24.437.1 VIM_103 Register (Offset = 219Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h107

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h107

Return to Summary Table

Table 4-3980. Instance Table

Instance Name	Physical Address
VIM	50F0 219Ch

Figure 4-1895. INTVECTOR_103 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3981. INTVECTOR_103 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.438 VIM_MSS_VIM_INTVECTOR_104 Registers

4.24.438.1 VIM_104 Register (Offset = 21A0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h108

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h108

Return to Summary Table

Table 4-3982. Instance Table

Instance Name	Physical Address
VIM	50F0 21A0h

Figure 4-1896. INTVECTOR_104 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3983. INTVECTOR_104 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.439 VIM_MSS_VIM_INTVECTOR_105 Registers

4.24.439.1 VIM_105 Register (Offset = 21A4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h109

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h109

Return to Summary Table

Table 4-3984. Instance Table

Instance Name	Physical Address
VIM	50F0 21A4h

Figure 4-1897. INTVECTOR_105 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3985. INTVECTOR_105 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.440 VIM_MSS_VIM_INTVECTOR_106 Registers

4.24.440.1 VIM_106 Register (Offset = 21A8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h110

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h110

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Table 4-3986. Instance Table

Instance Name	Physical Address
VIM	50F0 21A8h

Figure 4-1898. INTVECTOR_106 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3987. INTVECTOR_106 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.441 VIM_MSS_VIM_INTVECTOR_107 Registers

4.24.441.1 VIM_107 Register (Offset = 21ACh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h111

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h111

Return to Summary Table

Table 4-3988. Instance Table

Instance Name	Physical Address
VIM	50F0 21ACh

Figure 4-1899. INTVECTOR_107 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3989. INTVECTOR_107 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.442 VIM_MSS_VIM_INTVECTOR_108 Registers

4.24.442.1 VIM_108 Register (Offset = 21B0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h112

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h112

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Table 4-3990. Instance Table

Instance Name	Physical Address
VIM	50F0 21B0h

Figure 4-1900. INTVECTOR_108 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3991. INTVECTOR_108 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.443 VIM_MSS_VIM_INTVECTOR_109 Registers

4.24.443.1 VIM_109 Register (Offset = 21B4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h113

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h113

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Table 4-3992. Instance Table

Instance Name	Physical Address
VIM	50F0 21B4h

Figure 4-1901. INTVECTOR_109 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3993. INTVECTOR_109 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.444 VIM_MSS_VIM_INTVECTOR_110 Registers

4.24.444.1 VIM_110 Register (Offset = 21B8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h114

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h114

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Table 4-3994. Instance Table

Instance Name	Physical Address
VIM	50F0 21B8h

Figure 4-1902. INTVECTOR_110 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3995. INTVECTOR_110 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.445 VIM_MSS_VIM_INTVECTOR_111 Registers

4.24.445.1 VIM_111 Register (Offset = 21BCh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h115

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h115

Return to Summary Table

Table 4-3996. Instance Table

Instance Name	Physical Address
VIM	50F0 21BCh

Figure 4-1903. INTVECTOR_111 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3997. INTVECTOR_111 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.446 VIM_MSS_VIM_INTVECTOR_112 Registers

4.24.446.1 VIM_112 Register (Offset = 21C0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h116

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h116

Return to Summary Table

Table 4-3998. Instance Table

Instance Name	Physical Address
VIM	50F0 21C0h

Figure 4-1904. INTVECTOR_112 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3999. INTVECTOR_112 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.447 VIM_MSS_VIM_INTVECTOR_113 Registers

4.24.447.1 VIM_113 Register (Offset = 21C4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h117

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h117

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Table 4-4000. Instance Table

Instance Name	Physical Address
VIM	50F0 21C4h

Figure 4-1905. INTVECTOR_113 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4001. INTVECTOR_113 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.448 VIM_MSS_VIM_INTVECTOR_114 Registers

4.24.448.1 VIM_114 Register (Offset = 21C8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h118

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h118

Return to Summary Table

Table 4-4002. Instance Table

Instance Name	Physical Address
VIM	50F0 21C8h

Figure 4-1906. INTVECTOR_114 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4003. INTVECTOR_114 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.449 VIM_MSS_VIM_INTVECTOR_115 Registers

4.24.449.1 VIM_115 Register (Offset = 21CCh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h119

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h119

Return to Summary Table

Table 4-4004. Instance Table

Instance Name	Physical Address
VIM	50F0 21CCh

Figure 4-1907. INTVECTOR_115 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4005. INTVECTOR_115 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.450 VIM_MSS_VIM_INTVECTOR_116 Registers

4.24.450.1 VIM_116 Register (Offset = 21D0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h120

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h120

Return to Summary Table

Table 4-4006. Instance Table

Instance Name	Physical Address
VIM	50F0 21D0h

Figure 4-1908. INTVECTOR_116 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4007. INTVECTOR_116 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.451 VIM_MSS_VIM_INTVECTOR_117 Registers

4.24.451.1 VIM_117 Register (Offset = 21D4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h121

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h121

Return to Summary Table

Table 4-4008. Instance Table

Instance Name	Physical Address
VIM	50F0 21D4h

Figure 4-1909. INTVECTOR_117 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4009. INTVECTOR_117 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.452 VIM_MSS_VIM_INTVECTOR_118 Registers

4.24.452.1 VIM_118 Register (Offset = 21D8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h122

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h122

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Table 4-4010. Instance Table

Instance Name	Physical Address
VIM	50F0 21D8h

Figure 4-1910. INTVECTOR_118 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4011. INTVECTOR_118 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.453 VIM_MSS_VIM_INTVECTOR_119 Registers

4.24.453.1 VIM_119 Register (Offset = 21DCh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h123

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h123

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Table 4-4012. Instance Table

Instance Name	Physical Address
VIM	50F0 21DCh

Figure 4-1911. INTVECTOR_119 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4013. INTVECTOR_119 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.454 VIM_MSS_VIM_INTVECTOR_120 Registers

4.24.454.1 VIM_120 Register (Offset = 21E0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h124

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h124

Return to Summary Table

Table 4-4014. Instance Table

Instance Name	Physical Address
VIM	50F0 21E0h

Figure 4-1912. INTVECTOR_120 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4015. INTVECTOR_120 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.455 VIM_MSS_VIM_INTVECTOR_121 Registers

4.24.455.1 VIM_121 Register (Offset = 21E4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h125

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h125

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Table 4-4016. Instance Table

Instance Name	Physical Address
VIM	50F0 21E4h

Figure 4-1913. INTVECTOR_121 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4017. INTVECTOR_121 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.456 VIM_MSS_VIM_INTVECTOR_122 Registers

4.24.456.1 VIM_122 Register (Offset = 21E8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h126

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h126

Return to Summary Table

Table 4-4018. Instance Table

Instance Name	Physical Address
VIM	50F0 21E8h

Figure 4-1914. INTVECTOR_122 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4019. INTVECTOR_122 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.457 VIM_MSS_VIM_INTVECTOR_123 Registers

4.24.457.1 VIM_123 Register (Offset = 21ECh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h127

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h127

Return to Summary Table

Table 4-4020. Instance Table

Instance Name	Physical Address
VIM	50F0 21ECh

Figure 4-1915. INTVECTOR_123 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4021. INTVECTOR_123 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.458 VIM_MSS_VIM_INTVECTOR_124 Registers

4.24.458.1 VIM_124 Register (Offset = 21F0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h128

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h128

Return to Summary Table

Table 4-4022. Instance Table

Instance Name	Physical Address
VIM	50F0 21F0h

Figure 4-1916. INTVECTOR_124 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4023. INTVECTOR_124 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.459 VIM_MSS_VIM_INTVECTOR_125 Registers

4.24.459.1 VIM_125 Register (Offset = 21F4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h129

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h129

Return to Summary Table

Table 4-4024. Instance Table

Instance Name	Physical Address
VIM	50F0 21F4h

Figure 4-1917. INTVECTOR_125 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4025. INTVECTOR_125 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.460 VIM_MSS_VIM_INTVECTOR_126 Registers

4.24.460.1 VIM_126 Register (Offset = 21F8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h130

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h130

Return to Summary Table

Table 4-4026. Instance Table

Instance Name	Physical Address
VIM	50F0 21F8h

Figure 4-1918. INTVECTOR_126 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4027. INTVECTOR_126 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.461 VIM_MSS_VIM_INTVECTOR_127 Registers

4.24.461.1 VIM_127 Register (Offset = 21FCh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h131

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h131

Return to Summary Table

Table 4-4028. Instance Table

Instance Name	Physical Address
VIM	50F0 21FCh

Figure 4-1919. INTVECTOR_127 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4029. INTVECTOR_127 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.462 VIM_MSS_VIM_INTVECTOR_128 Registers

4.24.462.1 VIM_128 Register (Offset = 2200h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h132

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h132

Return to Summary Table

Table 4-4030. Instance Table

Instance Name	Physical Address
VIM	50F0 2200h

Figure 4-1920. INTVECTOR_128 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4031. INTVECTOR_128 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.463 VIM_MSS_VIM_INTVECTOR_129 Registers

4.24.463.1 VIM_129 Register (Offset = 2204h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h133

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h133

Return to Summary Table

Table 4-4032. Instance Table

Instance Name	Physical Address
VIM	50F0 2204h

Figure 4-1921. INTVECTOR_129 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4033. INTVECTOR_129 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.464 VIM_MSS_VIM_INTVECTOR_130 Registers

4.24.464.1 VIM_130 Register (Offset = 2208h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h134

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h134

Return to Summary Table

Table 4-4034. Instance Table

Instance Name	Physical Address
VIM	50F0 2208h

Figure 4-1922. INTVECTOR_130 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4035. INTVECTOR_130 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.465 VIM_MSS_VIM_INTVECTOR_131 Registers

4.24.465.1 VIM_131 Register (Offset = 220Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h135

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h135

Return to Summary Table

Table 4-4036. Instance Table

Instance Name	Physical Address
VIM	50F0 220Ch

Figure 4-1923. INTVECTOR_131 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4037. INTVECTOR_131 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.466 VIM_MSS_VIM_INTVECTOR_132 Registers

4.24.466.1 VIM_132 Register (Offset = 2210h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h136

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h136

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Table 4-4038. Instance Table

Instance Name	Physical Address
VIM	50F0 2210h

Figure 4-1924. INTVECTOR_132 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4039. INTVECTOR_132 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.467 VIM_MSS_VIM_INTVECTOR_133 Registers

4.24.467.1 VIM_133 Register (Offset = 2214h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h137

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h137

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Table 4-4040. Instance Table

Instance Name	Physical Address
VIM	50F0 2214h

Figure 4-1925. INTVECTOR_133 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4041. INTVECTOR_133 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.468 VIM_MSS_VIM_INTVECTOR_134 Registers

4.24.468.1 VIM_134 Register (Offset = 2218h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h138

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h138

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Table 4-4042. Instance Table

Instance Name	Physical Address
VIM	50F0 2218h

Figure 4-1926. INTVECTOR_134 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4043. INTVECTOR_134 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.469 VIM_MSS_VIM_INTVECTOR_135 Registers

4.24.469.1 VIM_135 Register (Offset = 221Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h139

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h139

Return to Summary Table

Table 4-4044. Instance Table

Instance Name	Physical Address
VIM	50F0 221Ch

Figure 4-1927. INTVECTOR_135 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4045. INTVECTOR_135 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.470 VIM_MSS_VIM_INTVECTOR_136 Registers

4.24.470.1 VIM_136 Register (Offset = 2220h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h140

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h140

Return to Summary Table

Table 4-4046. Instance Table

Instance Name	Physical Address
VIM	50F0 2220h

Figure 4-1928. INTVECTOR_136 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4047. INTVECTOR_136 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.471 VIM_MSS_VIM_INTVECTOR_137 Registers

4.24.471.1 VIM_137 Register (Offset = 2224h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h141

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h141

Return to Summary Table

Table 4-4048. Instance Table

Instance Name	Physical Address
VIM	50F0 2224h

Figure 4-1929. INTVECTOR_137 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4049. INTVECTOR_137 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.472 VIM_MSS_VIM_INTVECTOR_138 Registers

4.24.472.1 VIM_138 Register (Offset = 2228h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h142

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h142

Return to Summary Table

Table 4-4050. Instance Table

Instance Name	Physical Address
VIM	50F0 2228h

Figure 4-1930. INTVECTOR_138 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4051. INTVECTOR_138 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.473 VIM_MSS_VIM_INTVECTOR_139 Registers

4.24.473.1 VIM_139 Register (Offset = 222Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h143

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h143

Return to Summary Table

Table 4-4052. Instance Table

Instance Name	Physical Address
VIM	50F0 222Ch

Figure 4-1931. INTVECTOR_139 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4053. INTVECTOR_139 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.474 VIM_MSS_VIM_INTVECTOR_140 Registers

4.24.474.1 VIM_140 Register (Offset = 2230h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h144

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h144

Return to Summary Table

Table 4-4054. Instance Table

Instance Name	Physical Address
VIM	50F0 2230h

Figure 4-1932. INTVECTOR_140 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4055. INTVECTOR_140 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.475 VIM_MSS_VIM_INTVECTOR_141 Registers

4.24.475.1 VIM_141 Register (Offset = 2234h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h145

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h145

Return to Summary Table

Table 4-4056. Instance Table

Instance Name	Physical Address
VIM	50F0 2234h

Figure 4-1933. INTVECTOR_141 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4057. INTVECTOR_141 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.476 VIM_MSS_VIM_INTVECTOR_142 Registers

4.24.476.1 VIM_142 Register (Offset = 2238h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h146

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h146

Return to Summary Table

Table 4-4058. Instance Table

Instance Name	Physical Address
VIM	50F0 2238h

Figure 4-1934. INTVECTOR_142 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4059. INTVECTOR_142 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.477 VIM_MSS_VIM_INTVECTOR_143 Registers

4.24.477.1 VIM_143 Register (Offset = 223Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h147

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h147

Return to Summary Table

Table 4-4060. Instance Table

Instance Name	Physical Address
VIM	50F0 223Ch

Figure 4-1935. INTVECTOR_143 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4061. INTVECTOR_143 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.478 VIM_MSS_VIM_INTVECTOR_144 Registers

4.24.478.1 VIM_144 Register (Offset = 2240h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h148

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h148

Return to Summary Table

Table 4-4062. Instance Table

Instance Name	Physical Address
VIM	50F0 2240h

Figure 4-1936. INTVECTOR_144 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4063. INTVECTOR_144 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.479 VIM_MSS_VIM_INTVECTOR_145 Registers

4.24.479.1 VIM_145 Register (Offset = 2244h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h149

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h149

Return to Summary Table

Table 4-4064. Instance Table

Instance Name	Physical Address
VIM	50F0 2244h

Figure 4-1937. INTVECTOR_145 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4065. INTVECTOR_145 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.480 VIM_MSS_VIM_INTVECTOR_146 Registers

4.24.480.1 VIM_146 Register (Offset = 2248h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h150

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h150

Return to Summary Table

Table 4-4066. Instance Table

Instance Name	Physical Address
VIM	50F0 2248h

Figure 4-1938. INTVECTOR_146 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4067. INTVECTOR_146 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.481 VIM_MSS_VIM_INTVECTOR_147 Registers

4.24.481.1 VIM_147 Register (Offset = 224Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h151

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h151

Return to Summary Table

Table 4-4068. Instance Table

Instance Name	Physical Address
VIM	50F0 224Ch

Figure 4-1939. INTVECTOR_147 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4069. INTVECTOR_147 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.482 VIM_MSS_VIM_INTVECTOR_148 Registers

4.24.482.1 VIM_148 Register (Offset = 2250h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h152

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h152

Return to Summary Table

Table 4-4070. Instance Table

Instance Name	Physical Address
VIM	50F0 2250h

Figure 4-1940. INTVECTOR_148 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4071. INTVECTOR_148 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.483 VIM_MSS_VIM_INTVECTOR_149 Registers

4.24.483.1 VIM_149 Register (Offset = 2254h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h153

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h153

Return to Summary Table

Table 4-4072. Instance Table

Instance Name	Physical Address
VIM	50F0 2254h

Figure 4-1941. INTVECTOR_149 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4073. INTVECTOR_149 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.484 VIM_MSS_VIM_INTVECTOR_150 Registers

4.24.484.1 VIM_150 Register (Offset = 2258h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h154

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h154

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Table 4-4074. Instance Table

Instance Name	Physical Address
VIM	50F0 2258h

Figure 4-1942. INTVECTOR_150 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4075. INTVECTOR_150 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.485 VIM_MSS_VIM_INTVECTOR_151 Registers

4.24.485.1 VIM_151 Register (Offset = 225Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h155

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h155

Return to Summary Table

Table 4-4076. Instance Table

Instance Name	Physical Address
VIM	50F0 225Ch

Figure 4-1943. INTVECTOR_151 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4077. INTVECTOR_151 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.486 VIM_MSS_VIM_INTVECTOR_152 Registers

4.24.486.1 VIM_152 Register (Offset = 2260h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h156

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h156

Return to Summary Table

Table 4-4078. Instance Table

Instance Name	Physical Address
VIM	50F0 2260h

Figure 4-1944. INTVECTOR_152 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4079. INTVECTOR_152 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.487 VIM_MSS_VIM_INTVECTOR_153 Registers

4.24.487.1 VIM_153 Register (Offset = 2264h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h157

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h157

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Table 4-4080. Instance Table

Instance Name	Physical Address
VIM	50F0 2264h

Figure 4-1945. INTVECTOR_153 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4081. INTVECTOR_153 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.488 VIM_MSS_VIM_INTVECTOR_154 Registers

4.24.488.1 VIM_154 Register (Offset = 2268h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h158

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h158

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Table 4-4082. Instance Table

Instance Name	Physical Address
VIM	50F0 2268h

Figure 4-1946. INTVECTOR_154 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4083. INTVECTOR_154 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.489 VIM_MSS_VIM_INTVECTOR_155 Registers

4.24.489.1 VIM_155 Register (Offset = 226Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h159

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h159

Return to Summary Table

Table 4-4084. Instance Table

Instance Name	Physical Address
VIM	50F0 226Ch

Figure 4-1947. INTVECTOR_155 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4085. INTVECTOR_155 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.490 VIM_MSS_VIM_INTVECTOR_156 Registers

4.24.490.1 VIM_156 Register (Offset = 2270h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h160

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h160

Return to Summary Table

Table 4-4086. Instance Table

Instance Name	Physical Address
VIM	50F0 2270h

Figure 4-1948. INTVECTOR_156 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4087. INTVECTOR_156 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.491 VIM_MSS_VIM_INTVECTOR_157 Registers

4.24.491.1 VIM_157 Register (Offset = 2274h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h161

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h161

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Table 4-4088. Instance Table

Instance Name	Physical Address
VIM	50F0 2274h

Figure 4-1949. INTVECTOR_157 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4089. INTVECTOR_157 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.492 VIM_MSS_VIM_INTVECTOR_158 Registers

4.24.492.1 VIM_158 Register (Offset = 2278h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h162

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h162

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Table 4-4090. Instance Table

Instance Name	Physical Address
VIM	50F0 2278h

Figure 4-1950. INTVECTOR_158 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4091. INTVECTOR_158 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.493 VIM_MSS_VIM_INTVECTOR_159 Registers

4.24.493.1 VIM_159 Register (Offset = 227Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h163

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h163

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Table 4-4092. Instance Table

Instance Name	Physical Address
VIM	50F0 227Ch

Figure 4-1951. INTVECTOR_159 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4093. INTVECTOR_159 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.494 VIM_MSS_VIM_INTVECTOR_160 Registers

4.24.494.1 VIM_160 Register (Offset = 2280h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h164

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h164

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Table 4-4094. Instance Table

Instance Name	Physical Address
VIM	50F0 2280h

Figure 4-1952. INTVECTOR_160 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4095. INTVECTOR_160 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.495 VIM_MSS_VIM_INTVECTOR_161 Registers

4.24.495.1 VIM_161 Register (Offset = 2284h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h165

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h165

Return to Summary Table

Table 4-4096. Instance Table

Instance Name	Physical Address
VIM	50F0 2284h

Figure 4-1953. INTVECTOR_161 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4097. INTVECTOR_161 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.496 VIM_MSS_VIM_INTVECTOR_162 Registers

4.24.496.1 VIM_162 Register (Offset = 2288h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h166

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h166

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Table 4-4098. Instance Table

Instance Name	Physical Address
VIM	50F0 2288h

Figure 4-1954. INTVECTOR_162 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4099. INTVECTOR_162 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.497 VIM_MSS_VIM_INTVECTOR_163 Registers

4.24.497.1 VIM_163 Register (Offset = 228Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h167

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h167

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Table 4-4100. Instance Table

Instance Name	Physical Address
VIM	50F0 228Ch

Figure 4-1955. INTVECTOR_163 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4101. INTVECTOR_163 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.498 VIM_MSS_VIM_INTVECTOR_164 Registers

4.24.498.1 VIM_164 Register (Offset = 2290h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h168

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h168

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Table 4-4102. Instance Table

Instance Name	Physical Address
VIM	50F0 2290h

Figure 4-1956. INTVECTOR_164 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4103. INTVECTOR_164 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.499 VIM_MSS_VIM_INTVECTOR_165 Registers

4.24.499.1 VIM_165 Register (Offset = 2294h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h169

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h169

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Table 4-4104. Instance Table

Instance Name	Physical Address
VIM	50F0 2294h

Figure 4-1957. INTVECTOR_165 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4105. INTVECTOR_165 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.500 VIM_MSS_VIM_INTVECTOR_166 Registers

4.24.500.1 VIM_166 Register (Offset = 2298h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h170

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h170

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Table 4-4106. Instance Table

Instance Name	Physical Address
VIM	50F0 2298h

Figure 4-1958. INTVECTOR_166 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4107. INTVECTOR_166 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.501 VIM_MSS_VIM_INTVECTOR_167 Registers

4.24.501.1 VIM_167 Register (Offset = 229Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h171

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h171

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Table 4-4108. Instance Table

Instance Name	Physical Address
VIM	50F0 229Ch

Figure 4-1959. INTVECTOR_167 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4109. INTVECTOR_167 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.502 VIM_MSS_VIM_INTVECTOR_168 Registers

4.24.502.1 VIM_168 Register (Offset = 22A0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h172

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h172

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Table 4-4110. Instance Table

Instance Name	Physical Address
VIM	50F0 22A0h

Figure 4-1960. INTVECTOR_168 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4111. INTVECTOR_168 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.503 VIM_MSS_VIM_INTVECTOR_169 Registers

4.24.503.1 VIM_169 Register (Offset = 22A4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h173

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h173

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Table 4-4112. Instance Table

Instance Name	Physical Address
VIM	50F0 22A4h

Figure 4-1961. INTVECTOR_169 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4113. INTVECTOR_169 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.504 VIM_MSS_VIM_INTVECTOR_170 Registers

4.24.504.1 VIM_170 Register (Offset = 22A8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h174

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h174

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Table 4-4114. Instance Table

Instance Name	Physical Address
VIM	50F0 22A8h

Figure 4-1962. INTVECTOR_170 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4115. INTVECTOR_170 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.505 VIM_MSS_VIM_INTVECTOR_171 Registers

4.24.505.1 VIM_171 Register (Offset = 22ACh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h175

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h175

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Table 4-4116. Instance Table

Instance Name	Physical Address
VIM	50F0 22ACh

Figure 4-1963. INTVECTOR_171 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4117. INTVECTOR_171 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.506 VIM_MSS_VIM_INTVECTOR_172 Registers

4.24.506.1 VIM_172 Register (Offset = 22B0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h176

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h176

Return to Summary Table

Table 4-4118. Instance Table

Instance Name	Physical Address
VIM	50F0 22B0h

Figure 4-1964. INTVECTOR_172 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4119. INTVECTOR_172 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.507 VIM_MSS_VIM_INTVECTOR_173 Registers

4.24.507.1 VIM_173 Register (Offset = 22B4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h177

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h177

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Table 4-4120. Instance Table

Instance Name	Physical Address
VIM	50F0 22B4h

Figure 4-1965. INTVECTOR_173 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4121. INTVECTOR_173 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.508 VIM_MSS_VIM_INTVECTOR_174 Registers

4.24.508.1 VIM_174 Register (Offset = 22B8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h178

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h178

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Table 4-4122. Instance Table

Instance Name	Physical Address
VIM	50F0 22B8h

Figure 4-1966. INTVECTOR_174 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4123. INTVECTOR_174 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.509 VIM_MSS_VIM_INTVECTOR_175 Registers

4.24.509.1 VIM_175 Register (Offset = 22BCh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h179

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h179

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Table 4-4124. Instance Table

Instance Name	Physical Address
VIM	50F0 22BCh

Figure 4-1967. INTVECTOR_175 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4125. INTVECTOR_175 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.510 VIM_MSS_VIM_INTVECTOR_176 Registers

4.24.510.1 VIM_176 Register (Offset = 22C0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h180

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h180

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Table 4-4126. Instance Table

Instance Name	Physical Address
VIM	50F0 22C0h

Figure 4-1968. INTVECTOR_176 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4127. INTVECTOR_176 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.511 VIM_MSS_VIM_INTVECTOR_177 Registers

4.24.511.1 VIM_177 Register (Offset = 22C4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h181

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h181

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Table 4-4128. Instance Table

Instance Name	Physical Address
VIM	50F0 22C4h

Figure 4-1969. INTVECTOR_177 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4129. INTVECTOR_177 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.512 VIM_MSS_VIM_INTVECTOR_178 Registers

4.24.512.1 VIM_178 Register (Offset = 22C8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h182

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h182

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Table 4-4130. Instance Table

Instance Name	Physical Address
VIM	50F0 22C8h

Figure 4-1970. INTVECTOR_178 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4131. INTVECTOR_178 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.513 VIM_MSS_VIM_INTVECTOR_179 Registers

4.24.513.1 VIM_179 Register (Offset = 22CCh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h183

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h183

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Table 4-4132. Instance Table

Instance Name	Physical Address
VIM	50F0 22CCh

Figure 4-1971. INTVECTOR_179 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4133. INTVECTOR_179 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.514 VIM_MSS_VIM_INTVECTOR_180 Registers

4.24.514.1 VIM_180 Register (Offset = 22D0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h184

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h184

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Table 4-4134. Instance Table

Instance Name	Physical Address
VIM	50F0 22D0h

Figure 4-1972. INTVECTOR_180 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4135. INTVECTOR_180 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.515 VIM_MSS_VIM_INTVECTOR_181 Registers

4.24.515.1 VIM_181 Register (Offset = 22D4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h185

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h185

Return to Summary Table

Table 4-4136. Instance Table

Instance Name	Physical Address
VIM	50F0 22D4h

Figure 4-1973. INTVECTOR_181 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4137. INTVECTOR_181 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.516 VIM_MSS_VIM_INTVECTOR_182 Registers

4.24.516.1 VIM_182 Register (Offset = 22D8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h186

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h186

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Table 4-4138. Instance Table

Instance Name	Physical Address
VIM	50F0 22D8h

Figure 4-1974. INTVECTOR_182 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4139. INTVECTOR_182 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.517 VIM_MSS_VIM_INTVECTOR_183 Registers

4.24.517.1 VIM_183 Register (Offset = 22DCh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h187

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h187

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Table 4-4140. Instance Table

Instance Name	Physical Address
VIM	50F0 22DCh

Figure 4-1975. INTVECTOR_183 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4141. INTVECTOR_183 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.518 VIM_MSS_VIM_INTVECTOR_184 Registers

4.24.518.1 VIM_184 Register (Offset = 22E0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h188

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h188

Return to Summary Table

Table 4-4142. Instance Table

Instance Name	Physical Address
VIM	50F0 22E0h

Figure 4-1976. INTVECTOR_184 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4143. INTVECTOR_184 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.519 VIM_MSS_VIM_INTVECTOR_185 Registers

4.24.519.1 VIM_185 Register (Offset = 22E4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h189

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h189

Return to Summary Table

Table 4-4144. Instance Table

Instance Name	Physical Address
VIM	50F0 22E4h

Figure 4-1977. INTVECTOR_185 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4145. INTVECTOR_185 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.520 VIM_MSS_VIM_INTVECTOR_186 Registers

4.24.520.1 VIM_186 Register (Offset = 22E8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h190

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h190

Return to Summary Table

Table 4-4146. Instance Table

Instance Name	Physical Address
VIM	50F0 22E8h

Figure 4-1978. INTVECTOR_186 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4147. INTVECTOR_186 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.521 VIM_MSS_VIM_INTVECTOR_187 Registers

4.24.521.1 VIM_187 Register (Offset = 22ECh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h191

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h191

Return to Summary Table

Table 4-4148. Instance Table

Instance Name	Physical Address
VIM	50F0 22ECh

Figure 4-1979. INTVECTOR_187 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4149. INTVECTOR_187 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.522 VIM_MSS_VIM_INTVECTOR_188 Registers

4.24.522.1 VIM_188 Register (Offset = 22F0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h192

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h192

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Table 4-4150. Instance Table

Instance Name	Physical Address
VIM	50F0 22F0h

Figure 4-1980. INTVECTOR_188 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4151. INTVECTOR_188 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.523 VIM_MSS_VIM_INTVECTOR_189 Registers

4.24.523.1 VIM_189 Register (Offset = 22F4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h193

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h193

Return to Summary Table

Table 4-4152. Instance Table

Instance Name	Physical Address
VIM	50F0 22F4h

Figure 4-1981. INTVECTOR_189 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4153. INTVECTOR_189 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.524 VIM_MSS_VIM_INTVECTOR_190 Registers

4.24.524.1 VIM_190 Register (Offset = 22F8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h194

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h194

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Table 4-4154. Instance Table

Instance Name	Physical Address
VIM	50F0 22F8h

Figure 4-1982. INTVECTOR_190 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4155. INTVECTOR_190 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.525 VIM_MSS_VIM_INTVECTOR_191 Registers

4.24.525.1 VIM_191 Register (Offset = 22FCh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h195

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h195

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Table 4-4156. Instance Table

Instance Name	Physical Address
VIM	50F0 22FCh

Figure 4-1983. INTVECTOR_191 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4157. INTVECTOR_191 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.526 VIM_MSS_VIM_INTVECTOR_192 Registers

4.24.526.1 VIM_192 Register (Offset = 2300h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h196

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h196

Return to Summary Table

Table 4-4158. Instance Table

Instance Name	Physical Address
VIM	50F0 2300h

Figure 4-1984. INTVECTOR_192 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4159. INTVECTOR_192 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.527 VIM_MSS_VIM_INTVECTOR_193 Registers

4.24.527.1 VIM_193 Register (Offset = 2304h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h197

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h197

Return to Summary Table

Table 4-4160. Instance Table

Instance Name	Physical Address
VIM	50F0 2304h

Figure 4-1985. INTVECTOR_193 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4161. INTVECTOR_193 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.528 VIM_MSS_VIM_INTVECTOR_194 Registers

4.24.528.1 VIM_194 Register (Offset = 2308h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h198

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h198

Return to Summary Table

Table 4-4162. Instance Table

Instance Name	Physical Address
VIM	50F0 2308h

Figure 4-1986. INTVECTOR_194 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4163. INTVECTOR_194 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.529 VIM_MSS_VIM_INTVECTOR_195 Registers

4.24.529.1 VIM_195 Register (Offset = 230Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h199

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h199

Return to Summary Table

Table 4-4164. Instance Table

Instance Name	Physical Address
VIM	50F0 230Ch

Figure 4-1987. INTVECTOR_195 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4165. INTVECTOR_195 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.530 VIM_MSS_VIM_INTVECTOR_196 Registers

4.24.530.1 VIM_196 Register (Offset = 2310h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h200

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h200

Return to Summary Table

Table 4-4166. Instance Table

Instance Name	Physical Address
VIM	50F0 2310h

Figure 4-1988. INTVECTOR_196 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4167. INTVECTOR_196 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.531 VIM_MSS_VIM_INTVECTOR_197 Registers

4.24.531.1 VIM_197 Register (Offset = 2314h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h201

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h201

Return to Summary Table

Table 4-4168. Instance Table

Instance Name	Physical Address
VIM	50F0 2314h

Figure 4-1989. INTVECTOR_197 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4169. INTVECTOR_197 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.532 VIM_MSS_VIM_INTVECTOR_198 Registers

4.24.532.1 VIM_198 Register (Offset = 2318h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h202

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h202

Return to Summary Table

Table 4-4170. Instance Table

Instance Name	Physical Address
VIM	50F0 2318h

Figure 4-1990. INTVECTOR_198 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4171. INTVECTOR_198 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.533 VIM_MSS_VIM_INTVECTOR_199 Registers

4.24.533.1 VIM_199 Register (Offset = 231Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h203

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h203

Return to Summary Table

Table 4-4172. Instance Table

Instance Name	Physical Address
VIM	50F0 231Ch

Figure 4-1991. INTVECTOR_199 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4173. INTVECTOR_199 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.534 VIM_MSS_VIM_INTVECTOR_200 Registers

4.24.534.1 VIM_200 Register (Offset = 2320h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h204

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h204

Return to Summary Table

Table 4-4174. Instance Table

Instance Name	Physical Address
VIM	50F0 2320h

Figure 4-1992. INTVECTOR_200 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4175. INTVECTOR_200 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.535 VIM_MSS_VIM_INTVECTOR_201 Registers

4.24.535.1 VIM_201 Register (Offset = 2324h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h205

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h205

Return to Summary Table

Table 4-4176. Instance Table

Instance Name	Physical Address
VIM	50F0 2324h

Figure 4-1993. INTVECTOR_201 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4177. INTVECTOR_201 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.536 VIM_MSS_VIM_INTVECTOR_202 Registers

4.24.536.1 VIM_202 Register (Offset = 2328h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h206

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h206

Return to Summary Table

Table 4-4178. Instance Table

Instance Name	Physical Address
VIM	50F0 2328h

Figure 4-1994. INTVECTOR_202 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4179. INTVECTOR_202 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.537 VIM_MSS_VIM_INTVECTOR_203 Registers

4.24.537.1 VIM_203 Register (Offset = 232Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h207

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h207

Return to Summary Table

Table 4-4180. Instance Table

Instance Name	Physical Address
VIM	50F0 232Ch

Figure 4-1995. INTVECTOR_203 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4181. INTVECTOR_203 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.538 VIM_MSS_VIM_INTVECTOR_204 Registers

4.24.538.1 VIM_204 Register (Offset = 2330h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h208

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h208

Return to Summary Table

Table 4-4182. Instance Table

Instance Name	Physical Address
VIM	50F0 2330h

Figure 4-1996. INTVECTOR_204 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4183. INTVECTOR_204 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.539 VIM_MSS_VIM_INTVECTOR_205 Registers

4.24.539.1 VIM_205 Register (Offset = 2334h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h209

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h209

Return to Summary Table

Table 4-4184. Instance Table

Instance Name	Physical Address
VIM	50F0 2334h

Figure 4-1997. INTVECTOR_205 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4185. INTVECTOR_205 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.540 VIM_MSS_VIM_INTVECTOR_206 Registers

4.24.540.1 VIM_206 Register (Offset = 2338h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h210

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h210

Return to Summary Table

Table 4-4186. Instance Table

Instance Name	Physical Address
VIM	50F0 2338h

Figure 4-1998. INTVECTOR_206 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4187. INTVECTOR_206 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.541 VIM_MSS_VIM_INTVECTOR_207 Registers

4.24.541.1 VIM_207 Register (Offset = 233Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h211

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h211

Return to Summary Table

Table 4-4188. Instance Table

Instance Name	Physical Address
VIM	50F0 233Ch

Figure 4-1999. INTVECTOR_207 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4189. INTVECTOR_207 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.542 VIM_MSS_VIM_INTVECTOR_208 Registers

4.24.542.1 VIM_208 Register (Offset = 2340h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h212

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h212

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Table 4-4190. Instance Table

Instance Name	Physical Address
VIM	50F0 2340h

Figure 4-2000. INTVECTOR_208 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4191. INTVECTOR_208 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.543 VIM_MSS_VIM_INTVECTOR_209 Registers

4.24.543.1 VIM_209 Register (Offset = 2344h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h213

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h213

Return to Summary Table

Table 4-4192. Instance Table

Instance Name	Physical Address
VIM	50F0 2344h

Figure 4-2001. INTVECTOR_209 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4193. INTVECTOR_209 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.544 VIM_MSS_VIM_INTVECTOR_210 Registers

4.24.544.1 VIM_210 Register (Offset = 2348h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h214

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h214

Return to Summary Table

Table 4-4194. Instance Table

Instance Name	Physical Address
VIM	50F0 2348h

Figure 4-2002. INTVECTOR_210 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4195. INTVECTOR_210 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.545 VIM_MSS_VIM_INTVECTOR_211 Registers

4.24.545.1 VIM_211 Register (Offset = 234Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h215

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h215

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Table 4-4196. Instance Table

Instance Name	Physical Address
VIM	50F0 234Ch

Figure 4-2003. INTVECTOR_211 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4197. INTVECTOR_211 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.546 VIM_MSS_VIM_INTVECTOR_212 Registers

4.24.546.1 VIM_212 Register (Offset = 2350h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h216

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h216

Return to Summary Table

Table 4-4198. Instance Table

Instance Name	Physical Address
VIM	50F0 2350h

Figure 4-2004. INTVECTOR_212 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4199. INTVECTOR_212 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.547 VIM_MSS_VIM_INTVECTOR_213 Registers

4.24.547.1 VIM_213 Register (Offset = 2354h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h217

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h217

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Table 4-4200. Instance Table

Instance Name	Physical Address
VIM	50F0 2354h

Figure 4-2005. INTVECTOR_213 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4201. INTVECTOR_213 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.548 VIM_MSS_VIM_INTVECTOR_214 Registers

4.24.548.1 VIM_214 Register (Offset = 2358h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h218

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h218

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Table 4-4202. Instance Table

Instance Name	Physical Address
VIM	50F0 2358h

Figure 4-2006. INTVECTOR_214 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4203. INTVECTOR_214 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.549 VIM_MSS_VIM_INTVECTOR_215 Registers

4.24.549.1 VIM_215 Register (Offset = 235Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h219

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h219

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Table 4-4204. Instance Table

Instance Name	Physical Address
VIM	50F0 235Ch

Figure 4-2007. INTVECTOR_215 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4205. INTVECTOR_215 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.550 VIM_MSS_VIM_INTVECTOR_216 Registers

4.24.550.1 VIM_216 Register (Offset = 2360h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h220

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h220

Return to Summary Table

Table 4-4206. Instance Table

Instance Name	Physical Address
VIM	50F0 2360h

Figure 4-2008. INTVECTOR_216 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4207. INTVECTOR_216 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.551 VIM_MSS_VIM_INTVECTOR_217 Registers

4.24.551.1 VIM_217 Register (Offset = 2364h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h221

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h221

Return to Summary Table

Table 4-4208. Instance Table

Instance Name	Physical Address
VIM	50F0 2364h

Figure 4-2009. INTVECTOR_217 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4209. INTVECTOR_217 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.552 VIM_MSS_VIM_INTVECTOR_218 Registers

4.24.552.1 VIM_218 Register (Offset = 2368h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h222

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h222

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Table 4-4210. Instance Table

Instance Name	Physical Address
VIM	50F0 2368h

Figure 4-2010. INTVECTOR_218 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4211. INTVECTOR_218 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.553 VIM_MSS_VIM_INTVECTOR_219 Registers

4.24.553.1 VIM_219 Register (Offset = 236Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h223

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h223

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Table 4-4212. Instance Table

Instance Name	Physical Address
VIM	50F0 236Ch

Figure 4-2011. INTVECTOR_219 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4213. INTVECTOR_219 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.554 VIM_MSS_VIM_INTVECTOR_220 Registers

4.24.554.1 VIM_220 Register (Offset = 2370h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h224

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h224

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Table 4-4214. Instance Table

Instance Name	Physical Address
VIM	50F0 2370h

Figure 4-2012. INTVECTOR_220 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4215. INTVECTOR_220 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.555 VIM_MSS_VIM_INTVECTOR_221 Registers

4.24.555.1 VIM_221 Register (Offset = 2374h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h225

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h225

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Table 4-4216. Instance Table

Instance Name	Physical Address
VIM	50F0 2374h

Figure 4-2013. INTVECTOR_221 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4217. INTVECTOR_221 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.556 VIM_MSS_VIM_INTVECTOR_222 Registers

4.24.556.1 VIM_222 Register (Offset = 2378h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h226

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h226

Return to Summary Table

Table 4-4218. Instance Table

Instance Name	Physical Address
VIM	50F0 2378h

Figure 4-2014. INTVECTOR_222 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4219. INTVECTOR_222 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.557 VIM_MSS_VIM_INTVECTOR_223 Registers

4.24.557.1 VIM_223 Register (Offset = 237Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h227

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h227

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Table 4-4220. Instance Table

Instance Name	Physical Address
VIM	50F0 237Ch

Figure 4-2015. INTVECTOR_223 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4221. INTVECTOR_223 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.558 VIM_MSS_VIM_INTVECTOR_224 Registers

4.24.558.1 VIM_224 Register (Offset = 2380h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h228

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h228

Return to Summary Table

Table 4-4222. Instance Table

Instance Name	Physical Address
VIM	50F0 2380h

Figure 4-2016. INTVECTOR_224 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4223. INTVECTOR_224 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.559 VIM_MSS_VIM_INTVECTOR_225 Registers

4.24.559.1 VIM_225 Register (Offset = 2384h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h229

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h229

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Table 4-4224. Instance Table

Instance Name	Physical Address
VIM	50F0 2384h

Figure 4-2017. INTVECTOR_225 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4225. INTVECTOR_225 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.560 VIM_MSS_VIM_INTVECTOR_226 Registers

4.24.560.1 VIM_226 Register (Offset = 2388h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h230

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h230

Return to Summary Table

Table 4-4226. Instance Table

Instance Name	Physical Address
VIM	50F0 2388h

Figure 4-2018. INTVECTOR_226 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4227. INTVECTOR_226 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.561 VIM_MSS_VIM_INTVECTOR_227 Registers

4.24.561.1 VIM_227 Register (Offset = 238Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h231

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h231

Return to Summary Table

Table 4-4228. Instance Table

Instance Name	Physical Address
VIM	50F0 238Ch

Figure 4-2019. INTVECTOR_227 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4229. INTVECTOR_227 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.562 VIM_MSS_VIM_INTVECTOR_228 Registers

4.24.562.1 VIM_228 Register (Offset = 2390h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h232

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h232

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Table 4-4230. Instance Table

Instance Name	Physical Address
VIM	50F0 2390h

Figure 4-2020. INTVECTOR_228 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4231. INTVECTOR_228 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.563 VIM_MSS_VIM_INTVECTOR_229 Registers

4.24.563.1 VIM_229 Register (Offset = 2394h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h233

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h233

Return to Summary Table

Table 4-4232. Instance Table

Instance Name	Physical Address
VIM	50F0 2394h

Figure 4-2021. INTVECTOR_229 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4233. INTVECTOR_229 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.564 VIM_MSS_VIM_INTVECTOR_230 Registers

4.24.564.1 VIM_230 Register (Offset = 2398h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h234

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h234

Return to Summary Table

Table 4-4234. Instance Table

Instance Name	Physical Address
VIM	50F0 2398h

Figure 4-2022. INTVECTOR_230 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4235. INTVECTOR_230 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.565 VIM_MSS_VIM_INTVECTOR_231 Registers

4.24.565.1 VIM_231 Register (Offset = 239Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h235

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h235

Return to Summary Table

Table 4-4236. Instance Table

Instance Name	Physical Address
VIM	50F0 239Ch

Figure 4-2023. INTVECTOR_231 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4237. INTVECTOR_231 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.566 VIM_MSS_VIM_INTVECTOR_232 Registers

4.24.566.1 VIM_232 Register (Offset = 23A0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h236

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h236

Return to Summary Table

Table 4-4238. Instance Table

Instance Name	Physical Address
VIM	50F0 23A0h

Figure 4-2024. INTVECTOR_232 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4239. INTVECTOR_232 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.567 VIM_MSS_VIM_INTVECTOR_233 Registers

4.24.567.1 VIM_233 Register (Offset = 23A4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h237

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h237

Return to Summary Table

Table 4-4240. Instance Table

Instance Name	Physical Address
VIM	50F0 23A4h

Figure 4-2025. INTVECTOR_233 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4241. INTVECTOR_233 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.568 VIM_MSS_VIM_INTVECTOR_234 Registers

4.24.568.1 VIM_234 Register (Offset = 23A8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h238

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h238

Return to Summary Table

Table 4-4242. Instance Table

Instance Name	Physical Address
VIM	50F0 23A8h

Figure 4-2026. INTVECTOR_234 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4243. INTVECTOR_234 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.569 VIM_MSS_VIM_INTVECTOR_235 Registers

4.24.569.1 VIM_235 Register (Offset = 23ACh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h239

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h239

Return to Summary Table

Table 4-4244. Instance Table

Instance Name	Physical Address
VIM	50F0 23ACh

Figure 4-2027. INTVECTOR_235 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4245. INTVECTOR_235 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.570 VIM_MSS_VIM_INTVECTOR_236 Registers

4.24.570.1 VIM_236 Register (Offset = 23B0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h240

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h240

Return to Summary Table

Table 4-4246. Instance Table

Instance Name	Physical Address
VIM	50F0 23B0h

Figure 4-2028. INTVECTOR_236 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4247. INTVECTOR_236 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.571 VIM_MSS_VIM_INTVECTOR_237 Registers

4.24.571.1 VIM_237 Register (Offset = 23B4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h241

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h241

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Table 4-4248. Instance Table

Instance Name	Physical Address
VIM	50F0 23B4h

Figure 4-2029. INTVECTOR_237 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4249. INTVECTOR_237 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.572 VIM_MSS_VIM_INTVECTOR_238 Registers

4.24.572.1 VIM_238 Register (Offset = 23B8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h242

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h242

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Table 4-4250. Instance Table

Instance Name	Physical Address
VIM	50F0 23B8h

Figure 4-2030. INTVECTOR_238 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4251. INTVECTOR_238 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.573 VIM_MSS_VIM_INTVECTOR_239 Registers

4.24.573.1 VIM_239 Register (Offset = 23BCh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h243

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h243

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Table 4-4252. Instance Table

Instance Name	Physical Address
VIM	50F0 23BCh

Figure 4-2031. INTVECTOR_239 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4253. INTVECTOR_239 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.574 VIM_MSS_VIM_INTVECTOR_240 Registers

4.24.574.1 VIM_240 Register (Offset = 23C0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h244

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h244

Return to Summary Table

Table 4-4254. Instance Table

Instance Name	Physical Address
VIM	50F0 23C0h

Figure 4-2032. INTVECTOR_240 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4255. INTVECTOR_240 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.575 VIM_MSS_VIM_INTVECTOR_241 Registers

4.24.575.1 VIM_241 Register (Offset = 23C4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h245

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h245

Return to Summary Table

Table 4-4256. Instance Table

Instance Name	Physical Address
VIM	50F0 23C4h

Figure 4-2033. INTVECTOR_241 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4257. INTVECTOR_241 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.576 VIM_MSS_VIM_INTVECTOR_242 Registers

4.24.576.1 VIM_242 Register (Offset = 23C8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h246

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h246

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Table 4-4258. Instance Table

Instance Name	Physical Address
VIM	50F0 23C8h

Figure 4-2034. INTVECTOR_242 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4259. INTVECTOR_242 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.577 VIM_MSS_VIM_INTVECTOR_243 Registers

4.24.577.1 VIM_243 Register (Offset = 23CCh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h247

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h247

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Table 4-4260. Instance Table

Instance Name	Physical Address
VIM	50F0 23CCh

Figure 4-2035. INTVECTOR_243 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4261. INTVECTOR_243 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.578 VIM_MSS_VIM_INTVECTOR_244 Registers

4.24.578.1 VIM_244 Register (Offset = 23D0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h248

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h248

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Table 4-4262. Instance Table

Instance Name	Physical Address
VIM	50F0 23D0h

Figure 4-2036. INTVECTOR_244 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4263. INTVECTOR_244 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.579 VIM_MSS_VIM_INTVECTOR_245 Registers

4.24.579.1 VIM_245 Register (Offset = 23D4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h249

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h249

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Table 4-4264. Instance Table

Instance Name	Physical Address
VIM	50F0 23D4h

Figure 4-2037. INTVECTOR_245 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4265. INTVECTOR_245 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.580 VIM_MSS_VIM_INTVECTOR_246 Registers

4.24.580.1 VIM_246 Register (Offset = 23D8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h250

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h250

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Table 4-4266. Instance Table

Instance Name	Physical Address
VIM	50F0 23D8h

Figure 4-2038. INTVECTOR_246 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4267. INTVECTOR_246 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.581 VIM_MSS_VIM_INTVECTOR_247 Registers

4.24.581.1 VIM_247 Register (Offset = 23DCh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h251

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h251

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Table 4-4268. Instance Table

Instance Name	Physical Address
VIM	50F0 23DCh

Figure 4-2039. INTVECTOR_247 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4269. INTVECTOR_247 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.582 VIM_MSS_VIM_INTVECTOR_248 Registers

4.24.582.1 VIM_248 Register (Offset = 23E0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h252

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h252

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Table 4-4270. Instance Table

Instance Name	Physical Address
VIM	50F0 23E0h

Figure 4-2040. INTVECTOR_248 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4271. INTVECTOR_248 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.583 VIM_MSS_VIM_INTVECTOR_249 Registers

4.24.583.1 VIM_249 Register (Offset = 23E4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h253

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h253

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Table 4-4272. Instance Table

Instance Name	Physical Address
VIM	50F0 23E4h

Figure 4-2041. INTVECTOR_249 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4273. INTVECTOR_249 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.584 VIM_MSS_VIM_INTVECTOR_250 Registers

4.24.584.1 VIM_250 Register (Offset = 23E8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h254

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h254

Return to Summary Table

Table 4-4274. Instance Table

Instance Name	Physical Address
VIM	50F0 23E8h

Figure 4-2042. INTVECTOR_250 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4275. INTVECTOR_250 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.585 VIM_MSS_VIM_INTVECTOR_251 Registers

4.24.585.1 VIM_251 Register (Offset = 23ECh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h255

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h255

Return to Summary Table

Table 4-4276. Instance Table

Instance Name	Physical Address
VIM	50F0 23ECh

Figure 4-2043. INTVECTOR_251 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4277. INTVECTOR_251 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.586 VIM_MSS_VIM_INTVECTOR_252 Registers

4.24.586.1 VIM_252 Register (Offset = 23F0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h256

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h256

Return to Summary Table

Table 4-4278. Instance Table

Instance Name	Physical Address
VIM	50F0 23F0h

Figure 4-2044. INTVECTOR_252 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4279. INTVECTOR_252 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.587 VIM_MSS_VIM_INTVECTOR_253 Registers

4.24.587.1 VIM_253 Register (Offset = 23F4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h257

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h257

Return to Summary Table

Table 4-4280. Instance Table

Instance Name	Physical Address
VIM	50F0 23F4h

Figure 4-2045. INTVECTOR_253 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4281. INTVECTOR_253 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.588 VIM_MSS_VIM_INTVECTOR_254 Registers

4.24.588.1 VIM_254 Register (Offset = 23F8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h258

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h258

Return to Summary Table

Table 4-4282. Instance Table

Instance Name	Physical Address
VIM	50F0 23F8h

Figure 4-2046. INTVECTOR_254 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4283. INTVECTOR_254 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.589 VIM_MSS_VIM_INTVECTOR_255 Registers

4.24.589.1 VIM_255 Register (Offset = 23FCh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h259

Long Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h259

Return to Summary Table

Table 4-4284. Instance Table

Instance Name	Physical Address
VIM	50F0 23FCh

Figure 4-2047. INTVECTOR_255 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4285. INTVECTOR_255 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.24.590 Access Table

Table 4-4286. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RW	RW	Undefined

4.25 TOP_ESM Registers

Table 4-4287. TOP_ESM Registers Base Address Table

Offset	Length	Acronym	TOP_ESM Physical Address
0h	32	TOP_ESM_PID	52D0 0000h
4h	32	TOP_ESM_INFO	52D0 0004h
8h	8	TOP_ESM_EN	52D0 0008h

Table 4-4287. TOP_ESM Registers Base Address Table (continued)

Offset	Length	Acronym	TOP_ESM Physical Address
Ch	8	TOP_ESM_SFT_RST	52D0 000Ch
10h	8	TOP_ESM_ERR_RAW	52D0 0010h
14h	8	TOP_ESM_ERR_STS	52D0 0014h
18h	8	TOP_ESM_ERR_EN_SET	52D0 0018h
1Ch	8	TOP_ESM_ERR_EN_CLR	52D0 001Ch
20h	32	TOP_ESM_LOW_PRI	52D0 0020h
24h	32	TOP_ESM_HI_PRI	52D0 0024h
28h	32	TOP_ESM_LOW	52D0 0028h
2Ch	32	TOP_ESM_HI	52D0 002Ch
30h	16	TOP_ESM_EOI	52D0 0030h
40h	8	TOP_ESM_PIN_CTRL	52D0 0040h
44h	0	TOP_ESM_PIN_STS	52D0 0044h
48h	24	TOP_ESM_PIN_CNTR	52D0 0048h
4Ch	24	TOP_ESM_PIN_CNTR_PRE	52D0 004Ch
50h	24	TOP_ESM_PWMH_PIN_CNTR	52D0 0050h
54h	24	TOP_ESM_PWMH_PIN_CNTR_PRE	52D0 0054h
58h	24	TOP_ESM_PWML_PIN_CNTR	52D0 0058h
5Ch	24	TOP_ESM_PWML_PIN_CNTR_PRE	52D0 005Ch

4.25.1 TOP_ESM_PID Registers

4.25.1.1 TOP_ESM_PID Register (Offset = 0h) [reset = h]

Short Description: The Revision Register contains the major and minor revisions for the module.

Long Description:

Return to Summary Table

Table 4-4288. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0000h

Access Types Legend

Table 4-4289. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	PID register scheme
29 - 28	BU	RO	2h	Business Unit: 10 = Processors
27 - 16	FUNC	RO	FE0h	Module ID
15 - 11	RTL	RO	9h	RTL revision. Will vary depending on release.
10 - 8	MAJOR	RO	1h	Major revision
7 - 6	CUSTOM	RO	0h	Custom
5 - 0	MINOR	RO	0h	Minor revision

4.25.2 TOP_ESM_INFO Registers

4.25.2.1 TOP_ESM_INFO Register (Offset = 4h) [reset = h]

Short Description: The Info Register gives the configuration Inforrmation of this ESM.

Long Description:

Return to Summary Table

Table 4-4290. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0004h

Access Types Legend

Table 4-4291. INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LAST_RESET	RO	0h	Indicates the Source of the last Reset
	RESERVED	NONE		Reserved
15 - 8	PULSE_GROUPS	RO	1h	Number of Pulse Error Groups
7 - 0	GROUPS	RO	Bh	Total number of Error Groups

4.25.3 TOP_ESM_EN Registers

4.25.3.1 TOP_ESM_EN Register (Offset = 8h) [reset = h]

Short Description: The Global Enable Register has the master interrupt mask

Long Description:

Return to Summary Table

Table 4-4292. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0008h

Access Types Legend

Table 4-4293. EN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	KEY	RW	0h	Global Enable

4.25.4 TOP_ESM_SFT_RST Registers

4.25.4.1 TOP_ESM_SFT_RST Register (Offset = Ch) [reset = h]

Short Description: The Global Soft Reset Register controls the global clear for raw status and enables

Long Description:

Return to Summary Table

Table 4-4294. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 000Ch

Access Types Legend

Table 4-4295. SFT_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	KEY	WO	0h	Global Soft Reset

4.25.5 TOP_ESM_ERR_RAW Registers

4.25.5.1 TOP_ESM_ERR_RAW Register (Offset = 10h) [reset = h]

Short Description: Raw Status/Set Register for Configuration Errors

Long Description:

Return to Summary Table

Table 4-4296. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0010h

Access Types Legend

Table 4-4297. ERR_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	STS	RW	0h	This is the raw status for config errors

4.25.6 TOP_ESM_ERR_STS Registers

4.25.6.1 TOP_ESM_ERR_STS Register (Offset = 14h) [reset = h]

Short Description: Config Error Enable and Clear Register

Long Description:

Return to Summary Table

Table 4-4298. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0014h

Access Types Legend

Table 4-4299. ERR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	MSK	RW	0h	This is the masked status/clear for config errors

4.25.7 TOP_ESM_ERR_EN_SET Registers

4.25.7.1 TOP_ESM_ERR_EN_SET Register (Offset = 18h) [reset = h]

Short Description: Config Error Enable Set Register

Long Description:

Return to Summary Table

Table 4-4300. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0018h

Access Types Legend

Table 4-4301. ERR_EN_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	MSK	RW	0h	This is the mask enable set for config errors

4.25.8 TOP_ESM_ERR_EN_CLR Registers

4.25.8.1 TOP_ESM_ERR_EN_CLR Register (Offset = 1Ch) [reset = h]

Short Description: Config Error Interrupt Enabled Clear register

Long Description:

Return to Summary Table

Table 4-4302. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 001Ch

Access Types Legend

Table 4-4303. ERR_EN_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	MSK	RW	0h	This is the mask enable clear for config errors

4.25.9 TOP_ESM_LOW_PRI Registers

4.25.9.1 TOP_ESM_LOW_PRI Register (Offset = 20h) [reset = h]

Short Description: Shows which is the highest priority outstanding low priority interrupt

Long Description:

Return to Summary Table

Table 4-4304. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0020h

Access Types Legend

Table 4-4305. LOW_PRI Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	PLS	RO	FFFFh	This is the highest priority outstanding low priority pulse interrupt
15 - 0	LVL	RO	FFFFh	This is the highest priority outstanding low priority level interrupt

4.25.10 TOP_ESM_HI_PRI Registers

4.25.10.1 TOP_ESM_HI_PRI Register (Offset = 24h) [reset = h]

Short Description: Shows which is the highest priority outstanding high priority interrupt

Long Description:

Return to Summary Table

Table 4-4306. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0024h

Access Types Legend

Table 4-4307. HI_PRI Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	PLS	RO	FFFFh	This is the highest priority outstanding high priority pulse interrupt
15 - 0	LVL	RO	FFFFh	This is the highest priority outstanding high priority level interrupt

4.25.11 TOP_ESM_LOW Registers

4.25.11.1 TOP_ESM_LOW Register (Offset = 28h) [reset = h]

Short Description: Shows which groups have oustanding low priority interrupts

Long Description:

Return to Summary Table

Table 4-4308. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0028h

Access Types Legend

Table 4-4309. LOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RO	0h	This is the raw status for config errors

4.25.12 TOP_ESM_HI Registers

4.25.12.1 TOP_ESM_HI Register (Offset = 2Ch) [reset = h]

Short Description: Shows which groups have oustanding high priority interrupts

Long Description:

Return to Summary Table

Table 4-4310. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 002Ch

Access Types Legend

Table 4-4311. HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RO	0h	This is the raw status for config errors

4.25.13 TOP_ESM_EOI Registers

4.25.13.1 TOP_ESM_EOI Register (Offset = 30h) [reset = h]

Short Description: End of Interrupt Register

Long Description:

Return to Summary Table

Table 4-4312. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0030h

Access Types Legend

Table 4-4313. EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
10 - 0	KEY	WO	0h	This is the interrupt being serviced

4.25.14 TOP_ESM_PIN_CTRL Registers

4.25.14.1 TOP_ESM_PIN_CTRL Register (Offset = 40h) [reset = h]

Short Description: This register controls the error_pin_n output

Long Description:

Return to Summary Table

Table 4-4314. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0040h

Access Types Legend

Table 4-4315. PIN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 4	PWM_EN	RW	0h	PWM enable
3 - 0	KEY	RW	0h	Pin Control Key

4.25.15 TOP_ESM_PIN_STS Registers

4.25.15.1 TOP_ESM_PIN_STS Register (Offset = 44h) [reset = h]

Short Description: This register reflects the status of the error_pin_n output

Long Description:

Return to Summary Table

Table 4-4316. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0044h

Access Types Legend

Table 4-4317. PIN_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
0	VAL	RO	0h	Value of the error_pin_n

4.25.16 TOP_ESM_PIN_CNTR Registers

4.25.16.1 TOP_ESM_PIN_CNTR Register (Offset = 48h) [reset = h]

Short Description: This register shows the current value of the error pin counter

Long Description:

Return to Summary Table

Table 4-4318. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0048h

Access Types Legend

Table 4-4319. PIN_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	COUNT	RO	0h	Current Counter Value

4.25.17 TOP_ESM_PIN_CNTR_PRE Registers

4.25.17.1 TOP_ESM_PIN_CNTR_PRE Register (Offset = 4Ch) [reset = h]

Short Description: This register contains the value that is loaded in to the Error Counter

Long Description:

Return to Summary Table

Table 4-4320. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 004Ch

Access Types Legend

Table 4-4321. PIN_CNTR_PRE Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	COUNT	RW	0h	Counter Pre-Load Value

4.25.18 TOP_ESM_PWMH_PIN_CNTR Registers

4.25.18.1 TOP_ESM_PWMH_PIN_CNTR Register (Offset = 50h) [reset = h]

Short Description: This register shows the current value of the error pin PWM high counter

Long Description:

Return to Summary Table

Table 4-4322. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0050h

Access Types Legend

Table 4-4323. PWMH_PIN_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	COUNT	RO	0h	Current Counter Value

4.25.19 TOP_ESM_PWMH_PIN_CNTR_PRE Registers

4.25.19.1 TOP_ESM_PWMH_PIN_CNTR_PRE Register (Offset = 54h) [reset = h]

Short Description: This register contains the value that is loaded in to the Error PWM High Counter

Long Description:

Return to Summary Table

Table 4-4324. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0054h

Access Types Legend

Table 4-4325. PWMH_PIN_CNTR_PRE Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	COUNT	RW	0h	Counter Pre-Load Value

4.25.20 TOP_ESM_PWML_PIN_CNTR Registers

4.25.20.1 TOP_ESM_PWML_PIN_CNTR Register (Offset = 58h) [reset = h]

Short Description: This register shows the current value of the error pin PWM low counter

Long Description:

Return to Summary Table

Table 4-4326. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0058h

Access Types Legend

Table 4-4327. PWML_PIN_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	COUNT	RO	0h	Current Counter Value

4.25.21 TOP_ESM_PWML_PIN_CNTR_PRE Registers

4.25.21.1 TOP_ESM_PWML_PIN_CNTR_PRE Register (Offset = 5Ch) [reset = h]

Short Description: This register contains the value that is loaded in to the Error PWM Low Counter

Long Description:

Return to Summary Table

Table 4-4328. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 005Ch

Access Types Legend

Table 4-4329. PWML_PIN_CNTR_PRE Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	COUNT	RW	0h	Counter Pre-Load Value

4.25.22 Access Table

Table 4-4330. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write
WO	WO	Write

4.26 GPMC Registers

Table 4-4331. CFG, CFG Registers, Base Address=0X0000000048400000, Length=1024

Offset	Length	Register Name	GPMC0 Physical Address
18h	32	GPMC_IRQSTATUS	4840 0018h
1Ch	32	GPMC_IRQENABLE	4840 001Ch
40h	32	GPMC_TIMEOUT_CONTROL	4840 0040h
44h	32	GPMC_ERR_ADDRESS	4840 0044h
48h	32	GPMC_ERR_TYPE	4840 0048h
50h	32	GPMC_CONFIG	4840 0050h
54h	32	GPMC_STATUS	4840 0054h
60h + Formula	32	cs_cs_GPMC_CONFIG1_j_j	4840 0060h + Formula
64h + Formula	32	cs_cs_GPMC_CONFIG2_j_j	4840 0064h + Formula
68h + Formula	32	cs_cs_GPMC_CONFIG3_j_j	4840 0068h + Formula
6Ch + Formula	32	cs_cs_GPMC_CONFIG4_j_j	4840 006Ch + Formula
70h + Formula	32	cs_cs_GPMC_CONFIG5_j_j	4840 0070h + Formula
74h + Formula	32	cs_cs_GPMC_CONFIG6_j_j	4840 0074h + Formula
78h + Formula	32	cs_cs_GPMC_CONFIG7_j_j	4840 0078h + Formula
7Ch + Formula	32	cs_cs_GPMC_NAND_COMMAND_j_j	4840 007Ch + Formula
80h + Formula	32	cs_cs_GPMC_NAND_ADDRESS_j_j	4840 0080h + Formula
84h + Formula	32	cs_cs_GPMC_NAND_DATA_j_j	4840 0084h + Formula
1E0h	32	GPMC_PREFETCH_CONFIG1	4840 01E0h
1E4h	32	GPMC_PREFETCH_CONFIG2	4840 01E4h
1ECh	32	GPMC_PREFETCH_CONTROL	4840 01ECh
1F0h	32	GPMC_PREFETCH_STATUS	4840 01F0h
1F4h	32	GPMC_ECC_CONFIG	4840 01F4h
1F8h	32	GPMC_ECC_CONTROL	4840 01F8h
1FCh	32	GPMC_ECC_SIZE_CONFIG	4840 01FCh
200h + Formula	32	GPMC_ECC_RESULT_N	4840 0200h + Formula
240h + Formula	32	csel_csel_GPMC_BCH_RESULT_0_j_j	4840 0240h + Formula
244h + Formula	32	csel_csel_GPMC_BCH_RESULT_1_j_j	4840 0244h + Formula
248h + Formula	32	csel_csel_GPMC_BCH_RESULT_2_j_j	4840 0248h + Formula
24Ch + Formula	32	csel_csel_GPMC_BCH_RESULT_3_j_j	4840 024Ch + Formula
2D0h	32	GPMC_BCH_SWDATA	4840 02D0h
300h + Formula	32	chipsel_chipsel_GPMC_BCH_RESULT_4_j_j	4840 0300h + Formula
304h + Formula	32	chipsel_chipsel_GPMC_BCH_RESULT_5_j_j	4840 0304h + Formula

Table 4-4331. CFG, CFG Registers, Base Address=0X0000000048400000, Length=1024 (continued)

Offset	Length	Register Name	GPMC0 Physical Address
308h + Formula	32	chipsel_chipsel_GPMC_BCH_RESULT_6_j_j	4840 0308h + Formula

4.26.1 CFG_GPMC_REVISION Registers

4.26.1.1 CFG_REVISION Register (Offset = 0h) [reset = 60h]

Short Description: This register contains th

Long Description: This register contains the IP revision code

Return to Summary Table

Table 4-4332. Instance Table

Instance Name	Physical Address
GPMC0	4840 0000h

Figure 4-2048. GPMC_REVISION Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
N/A															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								REV							
N/A								R							
0h								60h							

Access Types Legend

Table 4-4333. GPMC_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	N/A		Reads returns 0 Reset Source: func_mod_g_arst_n
7:0	REV	R	60h	IP revision [7:4] Major revision [3:0] Minor revision Examples: 0x10 for 1.0, 0x21 for 2.1 Reset Source: func_mod_g_arst_n

4.26.2 CFG_GPMC_SYSCONFIG Registers

4.26.2.1 CFG_SYSCONFIG Register (Offset = 10h) [reset = 0h]

Short Description: This register controls th

Long Description: This register controls the various parameters of the OCP interface

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Table 4-4334. Instance Table

Instance Name	Physical Address
GPMC0	4840 0010h

Figure 4-2049. GPMC_SYSCONFIG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
N/A															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											IDLEMODE		RESERVED	RESERVED	AUTOIDLE
N/A											R/W		N/A	R/W	R/W
0h											0h		0h	0h	0h

Access Types Legend

Table 4-4335. GPMC_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	N/A		Write 0's for future compatibility Reads return 0 Reset Source: func_mod_g_arst_n
4:3	IDLEMODE	R/W	0h	Reset Source: func_mod_g_arst_n 3 Reserved reserved do not use 2 SmartIdle Smart-idle. Acknowledgement to an idle request is given based on the internal activity of the module 1 NoIdle No-idle. An idle request is never acknowledged
2	RESERVED	N/A		Write 0 for future compatibility Reads returns 0 Reset Source: func_mod_g_arst_n
1	RESERVED	R/W		This bit must be kept 0 for normal functioning of the IP. Do not set this bit to 1 Reset Source: func_mod_g_arst_n 1 Reset The module is reset
0	AUTOIDLE	R/W	0h	Internal OCP clock gating strategy Reset Source: func_mod_g_arst_n 1 AutoRun Automatic OCP clock gating strategy is applied, based on the OCP interface activity

4.26.3 CFG_GPMC_SYSSTATUS Registers

4.26.3.1 CFG_SYSSTATUS Register (Offset = 14h) [reset = 0h]

Short Description: This register provides st

Long Description: This register provides status information about the module, excluding the interrupt status information

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Table 4-4336. Instance Table

Instance Name	Physical Address
GPMC0	4840 0014h

Figure 4-2050. GPMC_SYSSTATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
N/A															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RESERVED							RESET DONE
N/A								R							R
0h								0h							0h

Access Types Legend

Table 4-4337. GPMC_SYSSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	N/A		Reads returns 0 Reset Source: func_mod_g_arst_n
7:1	RESERVED	R		Reads returns 0 [reserved for OCP-socket status information] Reset Source: func_mod_g_arst_n
0	RESETDONE	R	0h	Internal reset monitoring Reset Source: func_mod_g_arst_n 1 RstDone Reset completed

4.26.4 CFG_GPMC_IRQSTATUS Registers

4.26.4.1 CFG_IRQSTATUS Register (Offset = 18h) [reset = 0h]

Short Description: This interrupt status reg

Long Description: This interrupt status register regroups all the status of the module internal events that can generate an interrupt.

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Table 4-4338. Instance Table

Instance Name	Physical Address
GPMC0	4840 0018h

Figure 4-2051. GPMC_IRQSTATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
N/A															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				WAIT3EDGEDETECTIONSTATUS	WAIT2EDGEDETECTIONSTATUS	WAIT1EDGEDETECTIONSTATUS	WAIT0EDGEDETECTIONSTATUS	RESERVED						TERMINALCOUNTSTATUS	FIFOEVENTSTATUS
N/A				R/W1TC	R/W1TC	R/W1TC	R/W1TC	N/A						R/W1TC	R/W1TC
0h				0h	0h	0h	0h	0h						0h	0h

Access Types Legend

Table 4-4339. GPMC_IRQSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
11	WAIT3EDGEDETECTIONSTATUS	R/W1TC	0h	Status of the Wait3 Edge Detection interrupt Reset Source: func_mod_g_arst_n 1 W3Det1_R Read 1: A transition on WAIT3 input pin has been detected 1 W3Det1_W Write 1: Wait3EdgeDetection status bit is reset
10	WAIT2EDGEDETECTIONSTATUS	R/W1TC	0h	Status of the Wait2 Edge Detection interrupt Reset Source: func_mod_g_arst_n 1 W2Det1_R Read 1: A transition on WAIT2 input pin has been detected 1 W2Det1_W Write 1: Wait2EdgeDetection status bit is reset
9	WAIT1EDGEDETECTIONSTATUS	R/W1TC	0h	Status of the Wait1 Edge Detection interrupt Reset Source: func_mod_g_arst_n 1 W1Det1_R Read 1: A transition on WAIT1 input pin has been detected 1 W1Det1_W Write 1: Wait1EdgeDetection status bit is reset
8	WAIT0EDGEDETECTIONSTATUS	R/W1TC	0h	Status of the Wait0 Edge Detection interrupt Reset Source: func_mod_g_arst_n 1 W0Det1_R Read 1: A transition on WAIT0 input pin has been detected 1 W0Det1_W Write 1: Wait0EdgeDetection status bit is reset
7:2	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
1	TERMINALCOUNTSTATUS	R/W1TC	0h	Status of the TerminalCountEvent interrupt Reset Source: func_mod_g_arst_n 1 TCStat1_R Read 1: Indicates that CountValue is equal to 0 1 TCStat1_W Write 1: TerminalCountEvent status bit is reset

Table 4-4339. GPMC_IRQSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	FIFOEVENTSTATUS	R/W1TC	0h	Status of the FIFOEvent interrupt Reset Source: func_mod_g_arst_n 1 FIFOStat1_R Read 1: Indicates than at least FIFOThreshold bytes are available in prefetch mode and at least FIFOThreshold bytes free places are available in write posting mode. 1 FIFOStat1_W Write 1: FIFOEvent status bit is reset

4.26.5 CFG_GPMC_IRQENABLE Registers

4.26.5.1 CFG_IRQENABLE Register (Offset = 1Ch) [reset = 0h]

Short Description: The interrupt enable regi

Long Description: The interrupt enable register allows to mask/unmask the module internal sources of interrupt, on a event-by-event basis.

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Table 4-4340. Instance Table

Instance Name	Physical Address
GPMC0	4840 001Ch

Figure 4-2052. GPMC_IRQENABLE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
N/A															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				WAIT3EDGEDETECTIONENABLE	WAIT2EDGEDETECTIONENABLE	WAIT1EDGEDETECTIONENABLE	WAIT0EDGEDETECTIONENABLE	RESERVED						TERMINALCOUNTEVENTENABLE	FIFOEVENTENABLE
N/A				R/W	R/W	R/W	R/W	N/A						R/W	R/W
0h				0h	0h	0h	0h	0h						0h	0h

Access Types Legend

Table 4-4341. GPMC_IRQENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
11	WAIT3EDGEDETECTIONENABLE	R/W	0h	Enables the Wait3 Edge Detection interrupt Reset Source: func_mod_g_arst_n 1 W3Enabled Wait3EdgeDetection event generates an interrupt if occurs
10	WAIT2EDGEDETECTIONENABLE	R/W	0h	Enables the Wait2 Edge Detection interrupt Reset Source: func_mod_g_arst_n 1 W2Enabled Wait2EdgeDetection event generates an interrupt if occurs
9	WAIT1EDGEDETECTIONENABLE	R/W	0h	Enables the Wait1 Edge Detection interrupt Reset Source: func_mod_g_arst_n 1 W1Enabled Wait1EdgeDetection event generates an interrupt if occurs
8	WAIT0EDGEDETECTIONENABLE	R/W	0h	Enables the Wait0 Edge Detection interrupt Reset Source: func_mod_g_arst_n 1 W0Enabled Wait0EdgeDetection event generates an interrupt if occurs
7:2	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
1	TERMINALCOUNTEVENTENABLE	R/W	0h	Enables TerminalCountEvent interrupt issuing in pre-fetch or write posting mode Reset Source: func_mod_g_arst_n 1 TCEnabled TerminalCountEvent interrupt is not masked
0	FIFOEVENTENABLE	R/W	0h	Enables the FIFOEvent interrupt Reset Source: func_mod_g_arst_n 1 FIFOEnabled FIFOEvent interrupt is not masked

4.26.6 CFG_GPMC_TIMEOUT_CONTROL Registers

4.26.6.1 CFG_TIMEOUT_CONTROL Register (Offset = 40h) [reset = 1ff0h]

Short Description: The GPMC_TIMEOUT_CONTROL

Long Description: The GPMC_TIMEOUT_CONTROL register allows the user to set the start value of the timeout counter

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Table 4-4342. Instance Table

Instance Name	Physical Address
GPMC0	4840 0040h

Figure 4-2053. GPMC_TIMEOUT_CONTROL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
N/A															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			TIMEOUTSTARTVALUE									RESERVED			TIMEOUTENABLE
N/A			R/W									N/A			R/W
0h			1ffh									0h			0h

Access Types Legend

Table 4-4343. GPMC_TIMEOUT_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
12:4	TIMEOUTSTARTVALUE	R/W	1FFh	Start value of the time-out counter [0x000 corresponds to 0 GPMC.FCLK cycle, 0x001 corresponds to 1 GmpcClk cycle, &, 0x1FF corresponds to 511 GPMC.FCLK cyles.] Reset Source: func_mod_g_arst_n
3:1	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
0	TIMEOUTENABLE	R/W	0h	Enable bit of the TimeOut feature Reset Source: func_mod_g_arst_n 1 TOEnabled TimeOut feature is enabled

4.26.7 CFG_GPMC_ERR_ADDRESS Registers

4.26.7.1 CFG_ERR_ADDRESS Register (Offset = 44h) [reset = 0h]

Short Description: The GPMC_ERR_ADDRESS regi

Long Description: The GPMC_ERR_ADDRESS register stores the address of the illegal access when an error occurs

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Table 4-4344. Instance Table

Instance Name	Physical Address
GPMC0	4840 0044h

Figure 4-2054. GPMC_ERR_ADDRESS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	ILLEGALADD														
N/A	R														
0h	0h														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ILLEGALADD															
R															
0h															

Access Types Legend

Table 4-4345. GPMC_ERR_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
30:0	ILLEGALADD	R	0h	Address of illegal access : A30[0 for memory region, 1 for GPMC register region] and A29-A0[1 GBytes maximum] Reset Source: func_mod_g_arst_n

4.26.8 CFG_GPMC_ERR_TYPE Registers

4.26.8.1 CFG_ERR_TYPE Register (Offset = 48h) [reset = 0h]

Short Description: The GPMC_ERR_TYPE registe

Long Description: The GPMC_ERR_TYPE register stores the type of error when an error occurs

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Table 4-4346. Instance Table

Instance Name	Physical Address
GPMC0	4840 0048h

Figure 4-2055. GPMC_ERR_TYPE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
N/A															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					ILLEGALMCMD			RESERVED			ERRORNOTSUPPADD	ERRORNOTSUPPMCMD	ERRORTIMEOUT	RESERVED	ERRORVALID
N/A					R			N/A			R	R	R	N/A	R/W1TC
0h					0h			0h			0h	0h	0h	0h	0h

Access Types Legend

Table 4-4347. GPMC_ERR_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
10:8	ILLEGALMCMD	R	0h	System Command of the transaction that caused the error Reset Source: func_mod_g_arst_n
7:5	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
4	ERRORNOTSUPPADD	R	0h	Not supported Address error Reset Source: func_mod_g_arst_n 1 Err The error is due to a non supported Address
3	ERRORNOTSUPPMCMD	R	0h	Not supported Command error Reset Source: func_mod_g_arst_n 1 Err The error is due to a non supported Command
2	ERRORTIMEOUT	R	0h	Time-out error Reset Source: func_mod_g_arst_n 1 Err The error is due to a time out
1	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
0	ERRORVALID	R/W1TC	0h	Error validity status - Must be explicitely cleared with a write 1 transaction Reset Source: func_mod_g_arst_n 1 ErrDetect Error detected and logged in the other error fields

4.26.9 CFG_GPMC_CONFIG Registers

4.26.9.1 CFG_CONFIG Register (Offset = 50h) [reset = a00h]

Short Description: The configuration regist

Long Description: The configuration register allows global configuration of the GPMC

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Table 4-4348. Instance Table

Instance Name	Physical Address
GPMC0	4840 0050h

Figure 4-2056. GPMC_CONFIG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
N/A															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				WAIT3PINPOLARITY	WAIT2PINPOLARITY	WAIT1PINPOLARITY	WAIT0PINPOLARITY	RESERVED			WRITEPROTECT	RESERVED		LIMITEDADDRESS	NANDFORCEPOSTEDWRITE
N/A				R/W	R/W	R/W	R/W	N/A			R/W	N/A		R/W	R/W
0h				1h	0h	1h	0h	0h			0h	0h		0h	0h

Access Types Legend

Table 4-4349. GPMC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
11	WAIT3PINPOLARITY	R/W	1h	Selects the polarity of input pin WAIT3 Reset Source: func_mod_g_arst_n 1 W3ActiveH WAIT3 active high
10	WAIT2PINPOLARITY	R/W	0h	Selects the polarity of input pin WAIT2 Reset Source: func_mod_g_arst_n 1 W2ActiveH WAIT2 active high
9	WAIT1PINPOLARITY	R/W	1h	Selects the polarity of input pin WAIT1 Reset Source: func_mod_g_arst_n 1 W1ActiveH WAIT1 active high
8	WAIT0PINPOLARITY	R/W	0h	Selects the polarity of input pin WAIT0 Reset Source: func_mod_g_arst_n 1 W0ActiveH WAIT0 active high
7:5	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
4	WRITEPROTECT	R/W	0h	Controls the WP output pin level Reset Source: func_mod_g_arst_n 1 WPHigh WP output pin is high
3:2	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
1	LIMITEDADDRESS	R/W	0h	Limited Address device support Reset Source: func_mod_g_arst_n 1 Limited A26-A11 are not modified during an external memory access.
0	NANDFORCEPOSTEDWRITE	R/W	0h	Enables the Force Posted Write feature to NAND Cmd/Add/Data location Reset Source: func_mod_g_arst_n 1 ForcePWr Enables Force Posted Write

4.26.10 CFG_GPMC_STATUS Registers

4.26.10.1 CFG_STATUS Register (Offset = 54h) [reset = 1h]

Short Description: The status register prov

Long Description: The status register provides global status bits of the GPMC

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Table 4-4350. Instance Table

Instance Name	Physical Address
GPMC0	4840 0054h

Figure 4-2057. GPMC_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
N/A															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				WAIT3STATUS	WAIT2STATUS	WAIT1STATUS	WAIT0STATUS	RESERVED							EMPTYWRITEBUFFERSTATUS
N/A				R	R	R	R	N/A							R
0h				0h	0h	0h	0h	0h							1h

Access Types Legend

Table 4-4351. GPMC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
11	WAIT3STATUS	R	0h	Is a copy of input pin WAIT3. [Reset value is WAIT3 input pin sampled at IC reset] Reset Source: func_mod_g_arst_n 1 W3ActiveH WAIT3 asserted
10	WAIT2STATUS	R	0h	Is a copy of input pin WAIT2. [Reset value is WAIT2 input pin sampled at IC reset] Reset Source: func_mod_g_arst_n 1 W2ActiveH WAIT2 asserted
9	WAIT1STATUS	R	0h	Is a copy of input pin WAIT1. [Reset value is WAIT1 input pin sampled at IC reset] Reset Source: func_mod_g_arst_n 1 W1ActiveH WAIT1 asserted
8	WAIT0STATUS	R	0h	Is a copy of input pin WAIT0. [Reset value is WAIT0 input pin sampled at IC reset] Reset Source: func_mod_g_arst_n 1 W0ActiveH WAIT0 asserted
7:1	RESERVED	N/A		Write 0's for future compatibility Reads returns 0 Reset Source: func_mod_g_arst_n
0	EMPTYWRITEBUFFERSTATUS	R	1h	Stores the empty status of the write buffer Reset Source: func_mod_g_arst_n 1 b1 Write Buffer is empty

4.26.11 CFG_GPMC_PREFETCH_CONFIG1 Registers

4.26.11.1 CFG_PREFETCH_CONFIG1 Register (Offset = 1E0h) [reset = 4000h]

Short Description: Prefetch engine configura

Long Description: Prefetch engine configuration 1

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Table 4-4352. Instance Table

Instance Name	Physical Address
GPMC0	4840 01E0h

Figure 4-2058. GPMC_PREFETCH_CONFIG1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	CYCLEOPTIMIZATION			ENABLEOPTIMIZEDACCESS	ENGINECSSELECTOR			PFPWENROUNDROBIN	RESERVED			PFPWWEIGHTEDPRIO			
N/A	R/W			R/W	R/W			R/W	N/A			R/W			
0h	0h			0h	0h			0h	0h			0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	FIFOTHRESHOLD							ENABLEENGINE	RESERVED	WAITPINSELECTOR		SYNCHROMODE	DMAMODE	ENDIANISMTYPE	ACCESSMODE
N/A	R/W							R/W	N/A	R/W		R/W	R/W	R/W	R/W
0h	40h							0h	0h	0h		0h	0h	0h	0h

Access Types Legend

Table 4-4353. GPMC_PREFETCH_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
30:28	CYCLEOPTIMIZATION	R/W	0h	Define the number of GPMC.FCLK cycles to be substracted from RdCycleTime, WrCycleTime, AccessTime, CSRdOffTime, CSWrOffTime, ADVRdOffTime, ADVWrOffTime, OEOffTime, WEOffTime [0x0 corresponds to 0 GPMC.FCLK cycle, 0x1 corresponds to 1 GPMC.FCLK cycle, &, 0x7 corresponds to 7 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n
27	ENABLEOPTIMIZEDACCESS	R/W	0h	Enables access cycle optimization Reset Source: func_mod_g_arst_n 1 OptEnabled Access cycle optimization is enabled
26:24	ENGINECSSELECTOR	R/W	0h	Selects the CS where Prefetch Postwrite engine is active [0x0 corresponds toCS0, 0x1 corresponds to CS1, &, 0x7 corresponds to CS7] Reset Source: func_mod_g_arst_n
23	PFPWENROUNDROBIN	R/W	0h	Enables the PFPW RoundRobin arbitration Reset Source: func_mod_g_arst_n 1 RREnabled Prefetch Postwrite engine round robin arbitration is enabled
22:20	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
19:16	PFPWWEIGHTEDPRIO	R/W	0h	When an arbitration occurs between a direct memory access and a PFPW engine access, the direct memory access is always serviced. If the PFPWEnRoundRobin is enabled, 0x0 means : the next access is granted to the PFPW engine, 0x1 means : the two next accesses are granted to the PFPW engine, ..., 0xF means : the 16 next accesses are granted to the PFPW engine. Reset Source: func_mod_g_arst_n

Table 4-4353. GPMC_PREFETCH_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
14:8	FIFOTHRESHOLD	R/W	40h	Selects the maximum number of bytes read from the FIFO or written to the FIFO by the host on a DMA or interrupt request [0x00 corresponds to 0 byte, 0x01 corresponds to 1 byte, &, 0x40 corresponds to 64 bytes] Reset Source: func_mod_g_arst_n
7	ENABLEENGINE	R/W	0h	Enables the Prefetch Postwite engine Reset Source: func_mod_g_arst_n 1 PPEnabled Prefetch Postwrite engine is enabled
6	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
5:4	WAITPINSELECTOR	R/W	0h	Select which wait pin edge detector should start the engine in synchronized mode Reset Source: func_mod_g_arst_n 3 W3 Selects Wait3EdgeDetection 2 W2 Selects Wait2EdgeDetection 1 W1 Selects Wait1EdgeDetection
3	SYNCHROMODE	R/W	0h	Selects when the engine starts the access to CS Reset Source: func_mod_g_arst_n 1 AtStartAndWait Engine starts the access to CS as soon as StartEngine is set AND wait to non wait edge detection on the selected wait pin
2	DMAMODE	R/W	0h	Selects interrupt synchronization or DMA request synchronization Reset Source: func_mod_g_arst_n 1 DMAReqSync DMA request synchronization is enabled.A DMA request protocol is used.
1	ENDIANISMTYPE	R/W	0h	Selects endianism for prefetch data [0x0 for Little Endian and 0x1 for Big Endian] Reset Source: func_mod_g_arst_n
0	ACCESSMODE	R/W	0h	Selects pre-fetch read or write posting accesses Reset Source: func_mod_g_arst_n 1 WritePosting Write posting mode

4.26.12 CFG_GPMC_PREFETCH_CONFIG2 Registers

4.26.12.1 CFG_PREFETCH_CONFIG2 Register (Offset = 1E4h) [reset = 0h]

Short Description: Prefetch engine configura

Long Description: Prefetch engine configuration 2

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Table 4-4354. Instance Table

Instance Name	Physical Address
GPMC0	4840 01E4h

Figure 4-2059. GPMC_PREFETCH_CONFIG2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
N/A															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TRANSFERCOUNT													
N/A		R/W													
0h		0h													

Access Types Legend

Table 4-4355. GPMC_PREFETCH_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
13:0	TRANSFERCOUNT	R/W	0h	Selects the number of bytes to be read or written by the engine to the selected CS [0x0000 corresponds to 0 byte, 0x0001 corresponds to 1 byte, &, 0x2000 corresponds to 8 Kbytes] Reset Source: func_mod_g_arst_n

4.26.13 CFG_GPMC_PREFETCH_CONTROL Registers

4.26.13.1 CFG_PREFETCH_CONTROL Register (Offset = 1ECh) [reset = 0h]

Short Description: Prefetch engine control

Long Description: Prefetch engine control

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Table 4-4356. Instance Table

Instance Name	Physical Address
GPMC0	4840 01ECh

Figure 4-2060. GPMC_PREFETCH_CONTROL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
N/A															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															STARTENGINE
N/A															R/W
0h															0h

Access Types Legend

Table 4-4357. GPMC_PREFETCH_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
0	STARTENGINE	R/W	0h	Resets the FIFO pointer and starts the engine Reset Source: func_mod_g_arst_n 1 Start Write 1 resets the FIFO pointer to 0x0 in prefetch mode and 0x40 in postwrite mode and starts the engine. Read 1: engine is running

4.26.14 CFG_GPMC_PREFETCH_STATUS Registers

4.26.14.1 CFG_PREFETCH_STATUS Register (Offset = 1F0h) [reset = 0h]

Short Description: Prefetch engine status

Long Description: Prefetch engine status

Return to Summary Table

Table 4-4358. Instance Table

Instance Name	Physical Address
GPMC0	4840 01F0h

Figure 4-2061. GPMC_PREFETCH_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	FIFOPOINTER							RESERVED							FIFOTHRESHOLDSTATUS
N/A	R							N/A							R
0h	0h							0h							0h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	COUNTVALUE														
N/A	R														
0h	0h														

Access Types Legend

Table 4-4359. GPMC_PREFETCH_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
30:24	FIFOPOINTER	R	0h	Number of available bytes to be read or number of free empty byte places to be written [0x00 corresponds to 0 byte available to be read or 0 free empty place to be written, &, 0x40 corresponds to 64 bytes available to be read or 64 empty places to be written] Reset Source: func_mod_g_arst_n
23:17	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
16	FIFOTHRESHOLDSTATUS	R	0h	Set when FIFOPointer exceeds FIFOThreshold value Reset Source: func_mod_g_arst_n 1 GreaterThanThres FIFOPointer greater than FIFOThreshold. Writing to this bit has no effect
15:14	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
13:0	COUNTVALUE	R	0h	Number of remaining bytes to be read or to be written by the engine according to the TransferCount value [0x0000 corresponds to 0 byte remaining to be read or to be written, 0x0001 corresponds to 1 byte remaining to be read or to be written, &, 0x2000 corresponds to 8 Kbytes remaining to be read or to be written] Reset Source: func_mod_g_arst_n

4.26.15 CFG_GPMC_ECC_CONFIG Registers

4.26.15.1 CFG_ECC_CONFIG Register (Offset = 1F4h) [reset = 1030h]

Short Description: ECC configuration

Long Description: ECC configuration

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Table 4-4360. Instance Table

Instance Name	Physical Address
GPMC0	4840 01F4h

Figure 4-2062. GPMC_ECC_CONFIG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															ECCALGORITHM
N/A															R/W
0h															0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		ECCBCHTSEL		ECCWRAPMODE				ECC16B	ECCTOPSECTOR			ECCCS			ECCENABLE
N/A		R/W		R/W				R/W	R/W			R/W			R/W
0h		1h		0h				0h	3h			0h			0h

Access Types Legend

Table 4-4361. GPMC_ECC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
16	ECCALGORITHM	R/W	0h	ECC algorithm used 0x0: Hamming code 0x1: BCH code Reset Source: func_mod_g_arst_n
15:14	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
13:12	ECCBCHTSEL	R/W	1h	Error correction capability used for BCH 0x0: up to 4 bits error correction [t = 4] 0x1: up to 8 bits error correction [t=8] 0x2: up to 16 bits error correction [t=16] 0x3: reserved Reset Source: func_mod_g_arst_n
11:8	ECCWRAPMODE	R/W	0h	Spare area organization definition for the BCH algorithm. See the BCH syndrome/parity calculator module functional specification for more details Reset Source: func_mod_g_arst_n
7	ECC16B	R/W	0h	Selects an ECC calculated on 16 columns Reset Source: func_mod_g_arst_n 1 SixteenCol ECC calculated on 16 columns
6:4	ECCTOPSECTOR	R/W	3h	Number of sectors to process with the BCH algorithm 0x0: 1 sector [512kB page] 0x1: 2 sectors ... 0x3: 4 sectors [2kB page] ... 0x7: 8 sectors [4kB page] Reset Source: func_mod_g_arst_n
3:1	ECCCS	R/W	0h	Selects the CS where ECC is computed Reset Source: func_mod_g_arst_n 7 CS7 Chip select 7 6 CS6 Chip select 6 5 CS5 Chip select 5 4 CS4 Chip select 4 3 CS3 Chip select 3 2 CS2 Chip select 2 1 CS1 Chip select 1

Table 4-4361. GPMC_ECC_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ECCENABLE	R/W	0h	Enables the ECC feature Reset Source: func_mod_g_arst_n 1 ECCEnabled ECC enabled

4.26.16 CFG_GPMC_ECC_CONTROL Registers

4.26.16.1 CFG_ECC_CONTROL Register (Offset = 1F8h) [reset = 0h]

Short Description: ECC control

Long Description: ECC control

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Table 4-4362. Instance Table

Instance Name	Physical Address
GPMC0	4840 01F8h

Figure 4-2063. GPMC_ECC_CONTROL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
N/A															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							ECCCLEAR	RESERVED				ECCPOINTER			
N/A							R/W1TC	N/A				R/W			
0h							0h	0h				0h			

Access Types Legend

Table 4-4363. GPMC_ECC_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
8	ECCCLEAR	R/W1TC	0h	Clear all ECC result registers [Reads returns 0 - Writes 1 to this field clear all ECC result registers - Writes 0 are ignored] Reset Source: func_mod_g_arst_n
7:4	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
3:0	ECCPOINTER	R/W	0h	Selects ECC result register [Reads to this field give the dynamic position of the ECC pointer - Writes to this field select the ECC result register where the first ECC computation will be stored]; Other enums: writing other values disables the ECC engine [ECCEnable bit of GPMC_ECC_CONFIG set to 0] Reset Source: func_mod_g_arst_n 9 ECCRes9 ECC result register 9 is selected 8 ECCRes8 ECC result register 8 is selected 7 ECCRes7 ECC result register 7 is selected 6 ECCRes6 ECC result register 6 is selected 5 ECCRes5 ECC result register 5 is selected 4 ECCRes4 ECC result register 4 is selected 3 ECCRes3 ECC result register 3 is selected 2 ECCRes2 ECC result register 2 is selected 1 ECCRes1 ECC result register 1 is selected

4.26.17 CFG_GPMC_ECC_SIZE_CONFIG Registers

4.26.17.1 CFG_ECC_SIZE_CONFIG Register (Offset = 1FCh) [reset = fffff000h]

Short Description: ECC size

Long Description: ECC size

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Table 4-4364. Instance Table

Instance Name	Physical Address
GPMC0	4840 01FCh

Figure 4-2064. GPMC_ECC_SIZE_CONFIG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECCSIZE1										ECCSIZE0					
R/W										R/W					
3ffh										3ffh					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECCSIZE0				RESERVED			ECC9 RESULTSIZE	ECC8 RESULTSIZE	ECC7 RESULTSIZE	ECC6 RESULTSIZE	ECC5 RESULTSIZE	ECC4 RESULTSIZE	ECC3 RESULTSIZE	ECC2 RESULTSIZE	ECC1 RESULTSIZE
R/W				N/A			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
3ffh				0h			0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4365. GPMC_ECC_SIZE_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	ECCSIZE1	R/W	3FFh	Defines ECC size 1 [For Hamming Code: 0x000 corresponds to 2 Bytes, 0x001 corresponds to 4 Bytes, 0x002 corresponds to 6 Bytes, 0x003 corresponds to 8 Bytes, &, 0x0FF corresponds to 512 Bytes. Max supported value is 0x0FF.] [For BCH: 0x000 corresponds to 0 nibbles, 0x001 corresponds to 1 nibble, 0x002 corresponds to 2 nibbles, 0x003 corresponds to 3 nibbles, &, 0x3FF corresponds to 1023 nibbles.] Reset Source: func_mod_g_arst_n
21:12	ECCSIZE0	R/W	3FFh	Defines ECC size 0 [For Hamming Code: 0x000 corresponds to 2 Bytes, 0x001 corresponds to 4 Bytes, 0x002 corresponds to 6 Bytes, 0x003 corresponds to 8 Bytes, &, 0x0FF corresponds to 512 Bytes. Max supported value is 0x0FF.] [For BCH: 0x000 corresponds to 0 nibbles, 0x001 corresponds to 1 nibble, 0x002 corresponds to 2 nibbles, 0x003 corresponds to 3 nibbles, &, 0x3FF corresponds to 1023 nibbles.] Reset Source: func_mod_g_arst_n
11:9	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
8	ECC9RESULTSIZE	R/W	0h	Selects ECC size for ECC 9 result register Reset Source: func_mod_g_arst_n 1 Size1Sel ECCSize1 is selected
7	ECC8RESULTSIZE	R/W	0h	Selects ECC size for ECC 8 result register Reset Source: func_mod_g_arst_n 1 Size1Sel ECCSize1 is selected
6	ECC7RESULTSIZE	R/W	0h	Selects ECC size for ECC 7 result register Reset Source: func_mod_g_arst_n 1 Size1Sel ECCSize1 is selected
5	ECC6RESULTSIZE	R/W	0h	Selects ECC size for ECC 6 result register Reset Source: func_mod_g_arst_n 1 Size1Sel ECCSize1 is selected
4	ECC5RESULTSIZE	R/W	0h	Selects ECC size for ECC 5 result register Reset Source: func_mod_g_arst_n 1 Size1Sel ECCSize1 is selected
3	ECC4RESULTSIZE	R/W	0h	Selects ECC size for ECC 4 result register Reset Source: func_mod_g_arst_n 1 Size1Sel ECCSize1 is selected

Table 4-4365. GPMC_ECC_SIZE_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	ECC3RESULTSIZE	R/W	0h	Selects ECC size for ECC 3 result register Reset Source: func_mod_g_arst_n 1 Size1Sel ECCSize1 is selected
1	ECC2RESULTSIZE	R/W	0h	Selects ECC size for ECC 2 result register Reset Source: func_mod_g_arst_n 1 Size1Sel ECCSize1 is selected
0	ECC1RESULTSIZE	R/W	0h	Selects ECC size for ECC 1 result register Reset Source: func_mod_g_arst_n 1 Size1Sel ECCSize1 is selected

4.26.18 CFG_GPMC_ECC_RESULT_N Registers

4.26.18.1 CFG_ECC_RESULT_N Register (Offset = 200h) [reset = 0h]

Short Description: ECC result register

Long Description: ECC result register

Return to Summary Table

Offset = 200h + (j * 4h); where j = 0h to 8h

Table 4-4366. Instance Table

Instance Name	Physical Address
GPMC0	4840 0200h

Figure 4-2065. GPMC_ECC_RESULT_N Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				P2048O	P1024O	P512O	P256O	P128O	P64O	P32O	P16O	P8O	P4O	P2O	P1O
N/A				R	R	R	R	R	R	R	R	R	R	R	R
0h				0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				P2048E	P1024E	P512E	P256E	P128E	P64E	P32E	P16E	P8E	P4E	P2E	P1E
N/A				R	R	R	R	R	R	R	R	R	R	R	R
0h				0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4367. GPMC_ECC_RESULT_N Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
27	P2048O	R	0h	Odd Row Parity bit 2048, only used for ECC computed on 512 Bytes Reset Source: func_mod_g_arst_n
26	P1024O	R	0h	Odd Row Parity bit 1024 Reset Source: func_mod_g_arst_n
25	P512O	R	0h	Odd Row Parity bit 512 Reset Source: func_mod_g_arst_n
24	P256O	R	0h	Odd Row Parity bit 256 Reset Source: func_mod_g_arst_n
23	P128O	R	0h	Odd Row Parity bit 128 Reset Source: func_mod_g_arst_n
22	P64O	R	0h	Odd Row Parity bit 64 Reset Source: func_mod_g_arst_n
21	P32O	R	0h	Odd Row Parity bit 32 Reset Source: func_mod_g_arst_n
20	P16O	R	0h	Odd Row Parity bit 16 Reset Source: func_mod_g_arst_n
19	P8O	R	0h	Odd Row Parity bit 8 Reset Source: func_mod_g_arst_n
18	P4O	R	0h	Odd Column Parity bit 4 Reset Source: func_mod_g_arst_n
17	P2O	R	0h	Odd Column Parity bit 2 Reset Source: func_mod_g_arst_n
16	P1O	R	0h	Odd Column Parity bit 1 Reset Source: func_mod_g_arst_n
15:12	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
11	P2048E	R	0h	Even Row Parity bit 2048, only used for ECC computed on 512 Bytes Reset Source: func_mod_g_arst_n
10	P1024E	R	0h	Even Row Parity bit 1024 Reset Source: func_mod_g_arst_n
9	P512E	R	0h	Even Row Parity bit 512 Reset Source: func_mod_g_arst_n
8	P256E	R	0h	Even Row Parity bit 256 Reset Source: func_mod_g_arst_n
7	P128E	R	0h	Even Row Parity bit 128 Reset Source: func_mod_g_arst_n

Table 4-4367. GPMC_ECC_RESULT_N Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	P64E	R	0h	Even Row Parity bit 64 Reset Source: func_mod_g_arst_n
5	P32E	R	0h	Even Row Parity bit 32 Reset Source: func_mod_g_arst_n
4	P16E	R	0h	Even Row Parity bit 16 Reset Source: func_mod_g_arst_n
3	P8E	R	0h	Even Row Parity bit 8 Reset Source: func_mod_g_arst_n
2	P4E	R	0h	Even Column Parity bit 4 Reset Source: func_mod_g_arst_n
1	P2E	R	0h	Even Column Parity bit 2 Reset Source: func_mod_g_arst_n
0	P1E	R	0h	Even Column Parity bit 1 Reset Source: func_mod_g_arst_n

4.26.19 CFG_GPMC_BCH_SWDATA Registers

4.26.19.1 CFG_BCH_SWDATA Register (Offset = 2D0h) [reset = 0h]

Short Description: This register is used to

Long Description: This register is used to directly pass data to the BCH ECC calculator without accessing the actual NAND flash interface.

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Table 4-4368. Instance Table

Instance Name	Physical Address
GPMC0	4840 02D0h

Figure 4-2066. GPMC_BCH_SWDATA Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCH_DATA															
W															
0h															

Access Types Legend

Table 4-4369. GPMC_BCH_SWDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R		Reserved Reset Source: func_mod_g_arst_n
15:0	BCH_DATA	W	0h	Data to be included in the BCH calculation. Only bits 0 to 7 are taken into account if the calculator is configured to use 8 bits data [ECC16B = 0] Reset Source: func_mod_g_arst_n

4.26.20 CFG_CS_CS_GPMC_CONFIG1_J_J Registers

4.26.20.1 CFG_CS_GPMC_CONFIG1_J_J Register (Offset = 60h) [reset = 0h]

Short Description: The configuration 1 regi

Long Description: The configuration 1 register sets signal control parameters per chip select

Return to Summary Table

Offset = 60h + (j * 30h); where j = 0h to 7h

Table 4-4370. Instance Table

Instance Name	Physical Address
GPMC0	4840 0060h

Figure 4-2067. CS_CS_GPMC_CONFIG1_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WRAPBURST	READMULTIPLE	READTYPE	WRITEMULTIPLE	WRITETYPE	CLKACTIVATIONTIME		ATTACHEDDEVICEPAGELENGTH		WAITREADMONITORING	WAITWRITEMONITORING	RESERVED	WAITMONITORINGTIME		WAITPINSELECT	
R/W	R/W	R/W	R/W	R/W	R/W		R/W		R/W	R/W	N/A	R/W		R/W	
0h	0h	0h	0h	0h	0h		0h		0h	0h	0h	0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		DEVICESIZE		DEVICETYPE		MUXADDDATA		RESERVED			TIMEPARAGRANULARITY	RESERVED		GPMCFCLKDIVIDER	
N/A		R/W		R/W		R/W		N/A			R/W	N/A		R/W	
0h		0h		0h		0h		0h			0h	0h		0h	

Access Types Legend

Table 4-4371. CS_CS_GPMC_CONFIG1_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WRAPBURST	R/W	0h	Enables the wrapping burst capability. Must be set if the attached device is configured in wrapping burst Reset Source: func_mod_g_arst_n 1 WrapSupp Synchronous wrapping burst supported
30	READMULTIPLE	R/W	0h	Selects the read single or multiple access Reset Source: func_mod_g_arst_n 1 RdMultiple multiple access (burst if synchonous, page if asynchronous)
29	READTYPE	R/W	0h	Selects the read mode operation Reset Source: func_mod_g_arst_n 1 RdSync Read Synchronous
28	WRITEMULTIPLE	R/W	0h	Selects the write single or multiple access Reset Source: func_mod_g_arst_n 1 WrMultiple multiple access (burst if synchonous, considered as single if asynchronous)
27	WRITETYPE	R/W	0h	Selects the write mode operation Reset Source: func_mod_g_arst_n 1 WrSync Write Synchronous
26:25	CLKACTIVATIONTIME	R/W	0h	Output GPMC.CLK activation time Reset Source: func_mod_g_arst_n 3 NotDefined not defined 2 TwoClkB4 First rising edge of GPMC.CLK two GPMC.FCLK cycles after Start Access Time 1 OneClkB4 First rising edge of GPMC.CLK one GPMC.FCLK cycle after Start Access Time
24:23	ATTACHEDDEVICEPAGELENGTH	R/W	0h	Specifies the attached device page [burst] length Reset Source: func_mod_g_arst_n 3 ThirtyTwo 32 Words 2 Sixteen 16 Words 1 Eight 8 Words

Table 4-4371. CS_CS_GPMC_CONFIG1_J_J Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	WAITREADMONITORING	R/W	0h	Selects the Wait monitoring configuration for Read accesses [Reset value is BOOTWAITEN input pin sampled at IC reset] Reset Source: func_mod_g_arst_n 1 Wmonit Wait pin is monitored for read accesses
21	WAITWRITEMONITORING	R/W	0h	Selects the Wait monitoring configuration for Write accesses Reset Source: func_mod_g_arst_n 1 Wmonit Wait pin is monitored for write accesses
20	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
19:18	WAITMONITORINGTIME	R/W	0h	Selects input pin Wait monitoring time Reset Source: func_mod_g_arst_n 3 NotDefined not defined 2 TwoDeviceB4 Wait pin is monitored two GPMC.CLK cycle before valid data 1 OneDeviceB4 Wait pin is monitored one GPMC.CLK cycle before valid data
17:16	WAITPINSELECT	R/W	0h	Selects the input WAIT pin for this chip select [Reset value is BOOTWAITSELECT input pin sampled at IC reset for CS0 and 0 for CS1-7] Reset Source: func_mod_g_arst_n 3 W3 Wait input pin is WAIT3 2 W2 Wait input pin is WAIT2 1 W1 Wait input pin is WAIT1
15:14	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
13:12	DEVICESIZE	R/W	0h	Selects the device size attached [Reset value is BOOTDEVICESIZE input pin sampled at IC reset for CS0 and 01 for CS1-7] Reset Source: func_mod_g_arst_n 3 Res reserved 2 ThirtyTwoBits 32 bit 1 SixteenBits 16 bit
11:10	DEVICETYPE	R/W	0h	Selects the attached device type Reset Source: func_mod_g_arst_n 3 Res2 reserved 2 NANDlike NAND Flash stream mode 1 Res1 reserved
9:8	MUXADDDATA	R/W	0h	Enables the Address and data multiplexed protocol [Reset value is CS0MUXDEVICE input pin sampled at IC reset for CS0 and 0 for CS1-7] Reset Source: func_mod_g_arst_n 3 Reserved Reserved 2 Mux Address and data multiplexed attached device 1 AADMux AAD-Mux protocol device
7:5	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
4	TIMEPARAGRANULARITY	R/W	0h	Signals timing latencies scalar factor [Rd/WRCycleTime, AccessTime, PageBurstAccessTime, CSOnTime, CSRd/WrOffTime, ADVOnTime, ADVRd/WrOffTime, OEOnTime, OEOffTime, WEOnTime, WEOffTime, Cycle2CycleDelay, BusTurnAround, TimeOutStartValue] Reset Source: func_mod_g_arst_n 1 x2 x2 latencies
3:2	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
1:0	GPMCFCLKDIVIDER	R/W	0h	Divides the GPMC.FCLK clock Reset Source: func_mod_g_arst_n 3 DivBy4 GPMC.CLK frequency = GPMC.FCLK frequency /4 2 DivBy3 GPMC.CLK frequency = GPMC.FCLK frequency / 3 1 DivBy2 GPMC.CLK frequency = GPMC.FCLK frequency / 2

4.26.21 CFG_CS_CS_GPMC_CONFIG2_J_J Registers

4.26.21.1 CFG_CS_GPMC_CONFIG2_J_J Register (Offset = 64h) [reset = 101001h]

Short Description: Chip-select signal timing

Long Description: Chip-select signal timing parameter configuration

Return to Summary Table

Offset = 64h + (j * 30h); where j = 0h to 7h

Table 4-4372. Instance Table

Instance Name	Physical Address
GPMC0	4840 0064h

Figure 4-2068. CS_CS_GPMC_CONFIG2_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED											CSWROFFTIME				
N/A											R/W				
0h											10h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CSRDOFFTIME					CSEXTRADELAY	RESERVED		CSONTIME				
N/A			R/W					R/W	N/A		R/W				
0h			10h					0h	0h		1h				

Access Types Legend

Table 4-4373. CS_CS_GPMC_CONFIG2_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	N/A		Write 0's for future compatibility Reads returns 0 Reset Source: func_mod_g_arst_n
20:16	CSWROFFTIME	R/W	10h	CS# de-assertion time from start cycle time for write accesses [0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n
15:13	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
12:8	CSRDOFFTIME	R/W	10h	CS# de-assertion time from start cycle time for read accesses [0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n
7	CSEXTRADELAY	R/W	0h	CS# Add Extra Half GPMC.FCLK cycle Reset Source: func_mod_g_arst_n 1 Delayed CS# Timing control signal is delayed of half GPMC.FCLK clock cycle
6:4	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
3:0	CSONTIME	R/W	1h	CS# assertion time from start cycle time [0x0 corresponds to 0 GPMC.FCLK cycle, 0x1 corresponds to 1 GPMC.FCLK cycle, &, 0xF corresponds to 15 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n

4.26.22 CFG_CS_CS_GPMC_CONFIG3_J_J Registers

4.26.22.1 CFG_CS_GPMC_CONFIG3_J_J Register (Offset = 68h) [reset = 22060514h]

Short Description: ADV# signal timing parame

Long Description: ADV# signal timing parameter configuration

Return to Summary Table

Offset = 68h + (j * 30h); where j = 0h to 7h

Table 4-4374. Instance Table

Instance Name	Physical Address
GPMC0	4840 0068h

Figure 4-2069. CS_CS_GPMC_CONFIG3_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1	ADVAADMUXWROFFTIME			RESERVED_0	ADVAADMUXRDOFFTIME			RESERVED			ADVWROFFTIME				
R	R/W			R	R/W			N/A			R/W				
0h	2h			0h	2h			0h			6h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				ADVRDOFFTIME				ADVEXTRADELAY	ADVAADMUXONTIME			ADVONTIME			
N/A				R/W				R/W	R/W			R/W			
0h				5h				0h	1h			4h			

Access Types Legend

Table 4-4375. CS_CS_GPMC_CONFIG3_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED_1	R	0h	Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
30:28	ADVAADMUXWROFFTIME	R/W	2h	ADV# de-assertion for first address phase when using the AAD-Mux protocol Reset Source: func_mod_g_arst_n
27	RESERVED_0	R	0h	Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
26:24	ADVAADMUXRDOFFTIME	R/W	2h	ADV# assertion for first address phase when using the AAD-Mux protocol Reset Source: func_mod_g_arst_n
23:21	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
20:16	ADVWROFFTIME	R/W	6h	ADV# de-assertion time from start cycle time for write accesses [0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n
15:13	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
12:8	ADVRDOFFTIME	R/W	5h	ADV# de-assertion time from start cycle time for read accesses[0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n
7	ADVEXTRADELAY	R/W	0h	ADV# Add Extra Half GPMC.FCLK cycle Reset Source: func_mod_g_arst_n 1 Delayed ADV# Timing control signal is delayed of half GPMC.FCLK clock cycle
6:4	ADVAADMUXONTIME	R/W	1h	ADV# assertion for first address phase when using the AAD-Mux protocol Reset Source: func_mod_g_arst_n

Table 4-4375. CS_CS_GPMC_CONFIG3_J_J Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ADVONTIME	R/W	4h	ADV# assertion time from start cycle time [0x0 corresponds to 0 GPMC.FCLK cycle, 0x1 corresponds to 1 GPMC.FCLK cycle, &, 0xF corresponds to 15 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n

4.26.23 CFG_CS_CS_GPMC_CONFIG4_J_J Registers

4.26.23.1 CFG_CS_GPMC_CONFIG4_J_J Register (Offset = 6Ch) [reset = 10057016h]

Short Description: WE# and OE# signals timin

Long Description: WE# and OE# signals timing parameter configuration

Return to Summary Table

Offset = 6ch + (j * 30h); where j = 0h to 7h

Table 4-4376. Instance Table

Instance Name	Physical Address
GPMC0	4840 006Ch

Figure 4-2070. CS_CS_GPMC_CONFIG4_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			WEOFFTIME					WEEXTRADELAY	RESERVED			WEONTIME			
R			R/W					R/W	N/A			R/W			
0h			10h					0h	0h			5h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OEAADMUXOFFTIME			OEOFFTIME					OEEXTRADELAY	OEAADMUXONTIME			OEONTIME			
R/W			R/W					R/W	R/W			R/W			
3h			10h					0h	1h			6h			

Access Types Legend

Table 4-4377. CS_CS_GPMC_CONFIG4_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	R		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
28:24	WEOFFTIME	R/W	10h	WE# de-assertion time from start cycle time [0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n
23	WEEXTRADELAY	R/W	0h	WE# Add Extra Half GPMC.FCLK cycle Reset Source: func_mod_g_arst_n 1 Delayed WE# Timing control signal is delayed of half GPMC.FCLK clock cycle
22:20	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
19:16	WEONTIME	R/W	5h	WE# assertion time from start cycle time [0x0 corresponds to 0 GPMC.FCLK cycle, 0x1 corresponds to 1 GPMC.FCLK cycle, &, 0xF corresponds to 15 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n
15:13	OEAADMUXOFFTIME	R/W	3h	OE# de-assertion time for the first address phase in an AAD-Mux access Reset Source: func_mod_g_arst_n
12:8	OEOFFTIME	R/W	10h	OE# de-assertion time from start cycle time [0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n
7	OEEXTRADELAY	R/W	0h	OE# Add Extra Half GPMC.FCLK cycle Reset Source: func_mod_g_arst_n 1 Delayed OE# Timing control signal is delayed of half GPMC.FCLK clock cycle
6:4	OEAADMUXONTIME	R/W	1h	OE# assertion time for the first address phase in an AAD-Mux access Reset Source: func_mod_g_arst_n

Table 4-4377. CS_CS_GPMC_CONFIG4_J_J Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	OEONTIME	R/W	6h	OE# assertion time from start cycle time [0x0 corresponds to 0 GPMC.FCLK cycle, 0x1 corresponds to 1 GPMC.FCLK cycle, &, 0xF corresponds to 15 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n

4.26.24 CFG_CS_CS_GPMC_CONFIG5_J_J Registers

4.26.24.1 CFG_CS_GPMC_CONFIG5_J_J Register (Offset = 70h) [reset = 10f1111h]

Short Description: RdAccessTime and CycleTim

Long Description: RdAccessTime and CycleTime timing parameters configuration

Return to Summary Table

Offset = 70h + (j * 30h); where j = 0h to 7h

Table 4-4378. Instance Table

Instance Name	Physical Address
GPMC0	4840 0070h

Figure 4-2071. CS_CS_GPMC_CONFIG5_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PAGEBURSTACCESSTIME				RESERVED			RDACCESSTIME				
N/A				R/W				N/A			R/W				
0h				1h				0h			fh				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				WRCYCLETIME				RESERVED			RDCYCLETIME				
N/A				R/W				N/A			R/W				
0h				11h				0h			11h				

Access Types Legend

Table 4-4379. CS_CS_GPMC_CONFIG5_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
27:24	PAGEBURSTACCESSTIME	R/W	1h	Delay between successive words in a multiple access [0x0 corresponds to 0 GPMC.FCLK cycle, 0x1 corresponds to 1 GPMC.FCLK cycle, &, 0xF corresponds to 15 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n
23:21	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
20:16	RDACCESSTIME	R/W	Fh	Delay between start cycle time and first data valid [0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n
15:13	RESERVED	N/A		Write 0's for future compatibility Reads returns 0 Reset Source: func_mod_g_arst_n
12:8	WRCYCLETIME	R/W	11h	Total write cycle time [0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n
7:5	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
4:0	RDCYCLETIME	R/W	11h	Total read cycle time [0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n

4.26.25 CFG_CS_CS_GPMC_CONFIG6_J_J Registers

4.26.25.1 CFG_CS_GPMC_CONFIG6_J_J Register (Offset = 74h) [reset = 8f070000h]

Short Description: WrAccessTime, WrDataOnADm

Long Description: WrAccessTime, WrDataOnADmuxBus, Cycle2Cycle and BusTurnAround parameters configuration

Return to Summary Table

Offset = 74h + (j * 30h); where j = 0h to 7h

Table 4-4380. Instance Table

Instance Name	Physical Address
GPMC0	4840 0074h

Figure 4-2072. CS_CS_GPMC_CONFIG6_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	RESERVED			WRACCESSTIME				RESERVED				WRDATAONADMUXBUS			
R/W	N/A			R/W				N/A				R/W			
1h	0h			fh				0h				7h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CYCLE2CYCLEDELAY				CYCLE2CYCLESAMECSEN	CYCLE2CYCLEDIFFCSEN	RESERVED		BUSTURNAROUND			
N/A				R/W				R/W	R/W	N/A		R/W			
0h				0h				0h	0h	0h		0h			

Access Types Legend

Table 4-4381. CS_CS_GPMC_CONFIG6_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W		TI Internal use - Do not modify Reset Source: func_mod_g_arst_n
30:29	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
28:24	WRACCESSTIME	R/W	Fh	Delay from StartAccessTime to the GPMC.FCLK rising edge corresponding the the GPMC.CLK rising edge used by the attached memory for the first data capture [0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n
23:20	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
19:16	WRDATAONADMUXBUS	R/W	7h	Specifies on which GPMC.FCLK rising edge the first data of the synchronous burst write is driven in the add/data mux bus Reset Source: func_mod_g_arst_n
15:12	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
11:8	CYCLE2CYCLEDELAY	R/W	0h	Chip select high pulse delay between two successive accesses [0x0 corresponds to 0 GPMC.FCLK cycle, 0x1 corresponds to 1 GPMC.FCLK cycle, &, 0xF corresponds to 15 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n
7	CYCLE2CYCLESAMECSEN	R/W	0h	Add Cycle2CycleDelay between two successive accesses to the same chip-select [any access type] Reset Source: func_mod_g_arst_n 1 C2CDelay Add Cycle2CycleDelay

Table 4-4381. CS_CS_GPMC_CONFIG6_J_J Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CYCLE2CYCLEDIFFCSEN	R/W	0h	Add Cycle2CycleDelay between two successive accesses to a different chip-select [any access type] Reset Source: func_mod_g_arst_n 1 C2CDelay Add Cycle2CycleDelay
5:4	RESERVED	N/A		Write 0's for future compatibility Reads returns 0 Reset Source: func_mod_g_arst_n
3:0	BUSTURNAROUND	R/W	0h	Bus turn around latency between two successive accesses to the same chip-select [rd to wr] or to a different chip-select [read to read and read to write] [0x0 corresponds to 0 GPMC.FCLK cycle, 0x1 corresponds to 1 GPMC.FCLK cycle, &, 0xF corresponds to 15 GPMC.FCLK cycles] Reset Source: func_mod_g_arst_n

4.26.26 CFG_CS_CS_GPMC_CONFIG7_J_J Registers

4.26.26.1 CFG_CS_GPMC_CONFIG7_J_J Register (Offset = 78h) [reset = f40h]

Short Description: Chip-select address mappi

Long Description: Chip-select address mapping configuration Note: For CS0, the register reset is 0xf40 while for all the other instances CS1-CS7, the reset is 0xf00.

Return to Summary Table

Offset = 78h + (j * 30h); where j = 0h to 7h

Table 4-4382. Instance Table

Instance Name	Physical Address
GPMC0	4840 0078h

Figure 4-2073. CS_CS_GPMC_CONFIG7_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
N/A															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MASKADDRESS				RESERVED	CSVALID	BASEADDRESS					
N/A				R/W				N/A	R/W	R/W					
0h				fh				0h	1h	0h					

Access Types Legend

Table 4-4383. CS_CS_GPMC_CONFIG7_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
11:8	MASKADDRESS	R/W	Fh	Chip-select mask address Reset Source: func_mod_g_arst_n
7	RESERVED	N/A		Write 0's for future compatibility. Read returns 0 Reset Source: func_mod_g_arst_n
6	CSVALID	R/W	1h	Chip-select enable [reset value is 1 for CS0 and 0 for CS1-7] Reset Source: func_mod_g_arst_n 1 CSEnabled Chip-select enabled
5:0	BASEADDRESS	R/W	0h	Chip-select base address Reset Source: func_mod_g_arst_n

4.26.27 CFG_CS_CS_GPMC_NAND_COMMAND_J_J Registers

4.26.27.1 CFG_CS_GPMC_NAND_COMMAND_J_J Register (Offset = 7Ch) [reset = 0h]

Short Description: This Register is not a tr

Long Description: This Register is not a true register, just a address location.

Return to Summary Table

Offset = 7ch + (j * 30h); where j = 0h to 7h

Table 4-4384. Instance Table

Instance Name	Physical Address
GPMC0	4840 007Ch

Figure 4-2074. CS_CS_GPMC_NAND_COMMAND_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPMC_NAND_COMMAND_0															
W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_NAND_COMMAND_0															
W															
0h															

Access Types Legend

Table 4-4385. CS_CS_GPMC_NAND_COMMAND_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	GPMC_NAND_COMMAND_0	W	0h	Reset Source: func_mod_g_arst_n

4.26.28 CFG_CS_CS_GPMC_NAND_ADDRESS_J_J Registers

4.26.28.1 CFG_CS_GPMC_NAND_ADDRESS_J_J Register (Offset = 80h) [reset = 0h]

Short Description: This Register is not a tr

Long Description: This Register is not a true register, just a address location.

Return to Summary Table

Offset = 80h + (j * 30h); where j = 0h to 7h

Table 4-4386. Instance Table

Instance Name	Physical Address
GPMC0	4840 0080h

Figure 4-2075. CS_CS_GPMC_NAND_ADDRESS_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPMC_NAND_ADDRESS_0															
W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_NAND_ADDRESS_0															
W															
0h															

Access Types Legend

Table 4-4387. CS_CS_GPMC_NAND_ADDRESS_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	GPMC_NAND_ADDRESS_0	W	0h	Reset Source: func_mod_g_arst_n

4.26.29 CFG_CS_CS_GPMC_NAND_DATA_J_J Registers

4.26.29.1 CFG_CS_GPMC_NAND_DATA_J_J Register (Offset = 84h) [reset = 0h]

Short Description: This Register is not a tr

Long Description: This Register is not a true register, just a address location.

Return to Summary Table

Offset = 84h + (j * 30h); where j = 0h to 7h

Table 4-4388. Instance Table

Instance Name	Physical Address
GPMC0	4840 0084h

Figure 4-2076. CS_CS_GPMC_NAND_DATA_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPMC_NAND_DATA_0															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_NAND_DATA_0															
R/W															
0h															

Access Types Legend

Table 4-4389. CS_CS_GPMC_NAND_DATA_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	GPMC_NAND_DATA_0	R/W	0h	Reset Source: func_mod_g_arst_n

4.26.30 CFG_CSEL_CSEL_GPMC_BCH_RESULT_0_J_J Registers

4.26.30.1 CFG_CSEL_GPMC_BCH_RESULT_0_J_J Register (Offset = 240h) [reset = 0h]

Short Description: BCH ECC result, bits 0 to

Long Description: BCH ECC result, bits 0 to 31

Return to Summary Table

Offset = 240h + (j * 10h); where j = 0h to 7h

Table 4-4390. Instance Table

Instance Name	Physical Address
GPMC0	4840 0240h

Figure 4-2077. CSEL_CSEL_GPMC_BCH_RESULT_0_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BCH_RESULT_0															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCH_RESULT_0															
R															
0h															

Access Types Legend

Table 4-4391. CSEL_CSEL_GPMC_BCH_RESULT_0_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BCH_RESULT_0	R	0h	BCH ECC result, bits 0 to 31 Reset Source: func_mod_g_arst_n

4.26.31 CFG_CSEL_CSEL_GPMC_BCH_RESULT_1_J_J Registers

4.26.31.1 CFG_CSEL_GPMC_BCH_RESULT_1_J_J Register (Offset = 244h) [reset = 0h]

Short Description: BCH ECC result, bits 32 t

Long Description: BCH ECC result, bits 32 to 63

Return to Summary Table

Offset = 244h + (j * 10h); where j = 0h to 7h

Table 4-4392. Instance Table

Instance Name	Physical Address
GPMC0	4840 0244h

Figure 4-2078. CSEL_CSEL_GPMC_BCH_RESULT_1_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BCH_RESULT_1															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCH_RESULT_1															
R															
0h															

Access Types Legend

Table 4-4393. CSEL_CSEL_GPMC_BCH_RESULT_1_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BCH_RESULT_1	R	0h	BCH ECC result, bits 32 to 63 Reset Source: func_mod_g_arst_n

4.26.32 CFG_CSEL_CSEL_GPMC_BCH_RESULT_2_J_J Registers

4.26.32.1 CFG_CSEL_GPMC_BCH_RESULT_2_J_J Register (Offset = 248h) [reset = 0h]

Short Description: BCH ECC result, bits 64 t

Long Description: BCH ECC result, bits 64 to 95

Return to Summary Table

Offset = 248h + (j * 10h); where j = 0h to 7h

Table 4-4394. Instance Table

Instance Name	Physical Address
GPMC0	4840 0248h

Figure 4-2079. CSEL_CSEL_GPMC_BCH_RESULT_2_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BCH_RESULT_2															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCH_RESULT_2															
R															
0h															

Access Types Legend

Table 4-4395. CSEL_CSEL_GPMC_BCH_RESULT_2_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BCH_RESULT_2	R	0h	BCH ECC result, bits 64 to 95 Reset Source: func_mod_g_arst_n

4.26.33 CFG_CSEL_CSEL_GPMC_BCH_RESULT_3_J_J Registers

4.26.33.1 CFG_CSEL_GPMC_BCH_RESULT_3_J_J Register (Offset = 24Ch) [reset = 0h]

Short Description: BCH ECC result, bits 96 t

Long Description: BCH ECC result, bits 96 to 127

Return to Summary Table

Offset = 24ch + (j * 10h); where j = 0h to 7h

Table 4-4396. Instance Table

Instance Name	Physical Address
GPMC0	4840 024Ch

Figure 4-2080. CSEL_CSEL_GPMC_BCH_RESULT_3_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BCH_RESULT_3															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCH_RESULT_3															
R															
0h															

Access Types Legend

Table 4-4397. CSEL_CSEL_GPMC_BCH_RESULT_3_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BCH_RESULT_3	R	0h	BCH ECC result, bits 96 to 127 Reset Source: func_mod_g_arst_n

4.26.34 CFG_CHIPSEL_CHIPSEL_GPMC_BCH_RESULT_4_J_J Registers

4.26.34.1 CFG_CHIPSEL_GPMC_BCH_RESULT_4_J_J Register (Offset = 300h) [reset = 0h]

Short Description: BCH ECC result, bits 128

Long Description: BCH ECC result, bits 128 to 159

Return to Summary Table

Offset = 300h + (j * 10h); where j = 0h to 7h

Table 4-4398. Instance Table

Instance Name	Physical Address
GPMC0	4840 0300h

Figure 4-2081. CHIPSEL_CHIPSEL_GPMC_BCH_RESULT_4_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BCH_RESULT_4															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCH_RESULT_4															
R															
0h															

Access Types Legend

Table 4-4399. CHIPSEL_CHIPSEL_GPMC_BCH_RESULT_4_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BCH_RESULT_4	R	0h	BCH ECC result, bits 128 to 159 Reset Source: func_mod_g_arst_n

4.26.35 CFG_CHIPSEL_CHIPSEL_GPMC_BCH_RESULT_5_J_J Registers

4.26.35.1 CFG_CHIPSEL_GPMC_BCH_RESULT_5_J_J Register (Offset = 304h) [reset = 0h]

Short Description: BCH ECC result, bits 160

Long Description: BCH ECC result, bits 160 to 191

Return to Summary Table

Offset = 304h + (j * 10h); where j = 0h to 7h

Table 4-4400. Instance Table

Instance Name	Physical Address
GPMC0	4840 0304h

Figure 4-2082. CHIPSEL_CHIPSEL_GPMC_BCH_RESULT_5_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BCH_RESULT_5															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCH_RESULT_5															
R															
0h															

Access Types Legend

Table 4-4401. CHIPSEL_CHIPSEL_GPMC_BCH_RESULT_5_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BCH_RESULT_5	R	0h	BCH ECC result, bits 160 to 191 Reset Source: func_mod_g_arst_n

4.26.36 CFG_CHIPSEL_CHIPSEL_GPMC_BCH_RESULT_6_J_J Registers

4.26.36.1 CFG_CHIPSEL_GPMC_BCH_RESULT_6_J_J Register (Offset = 308h) [reset = 0h]

Short Description: BCH ECC result, bits 192

Long Description: BCH ECC result, bits 192 to 207

Return to Summary Table

Offset = 308h + (j * 10h); where j = 0h to 7h

Table 4-4402. Instance Table

Instance Name	Physical Address
GPMC0	4840 0308h

Figure 4-2083. CHIPSEL_CHIPSEL_GPMC_BCH_RESULT_6_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCH_RESULT_6															
R															
0h															

Access Types Legend

Table 4-4403. CHIPSEL_CHIPSEL_GPMC_BCH_RESULT_6_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R		Reserved Reset Source: func_mod_g_arst_n
15:0	BCH_RESULT_6	R	0h	BCH ECC result, bits 192 to 207 Reset Source: func_mod_g_arst_n

4.26.37 Access Table

Table 4-4404. Access Type Codes

Access Type	Code	Description
N/A	N/A	Undefined
R	R	Read
R/W	R/W	Read / Write
R/W1TC	R/W1TC	Read/Write 1 To Clear
W	W	Write

4.27 ELM Registers

Table 4-4405. , Registers, Base Address=0X00000000527F0000, Length=4096

Offset	Length	Register Name	ELM0 Physical Address
14h	32	ELM_ELM_SYSSTATUS	527F 0014h
18h	32	ELM_ELM_IRQSTATUS	527F 0018h
1Ch	32	ELM_ELM_IRQENABLE	527F 001Ch
20h	32	ELM_ELM_LOCATION_CONFIG	527F 0020h
80h	32	ELM_ELM_PAGE_CTRL	527F 0080h
400h + Formula	32	ELM_poly_poly_ELM_SYNDROME_FRAGMENT_0_j_j	527F 0400h + Formula
404h + Formula	32	ELM_poly_poly_ELM_SYNDROME_FRAGMENT_1_j_j	527F 0404h + Formula
408h + Formula	32	ELM_poly_poly_ELM_SYNDROME_FRAGMENT_2_j_j	527F 0408h + Formula
40Ch + Formula	32	ELM_poly_poly_ELM_SYNDROME_FRAGMENT_3_j_j	527F 040Ch + Formula
410h + Formula	32	ELM_poly_poly_ELM_SYNDROME_FRAGMENT_4_j_j	527F 0410h + Formula
414h + Formula	32	ELM_poly_poly_ELM_SYNDROME_FRAGMENT_5_j_j	527F 0414h + Formula
418h + Formula	32	ELM_poly_poly_ELM_SYNDROME_FRAGMENT_6_j_j	527F 0418h + Formula
800h + Formula	32	ELM_err_loc_err_loc_ELM_LOCATION_STATUS_j_j	527F 0800h + Formula
880h + Formula	32	ELM_err_loc_err_loc_ELM_ERROR_LOCATION_0_j_j	527F 0880h + Formula
884h + Formula	32	ELM_err_loc_err_loc_ELM_ERROR_LOCATION_1_j_j	527F 0884h + Formula
888h + Formula	32	ELM_err_loc_err_loc_ELM_ERROR_LOCATION_2_j_j	527F 0888h + Formula
88Ch + Formula	32	ELM_err_loc_err_loc_ELM_ERROR_LOCATION_3_j_j	527F 088Ch + Formula
890h + Formula	32	ELM_err_loc_err_loc_ELM_ERROR_LOCATION_4_j_j	527F 0890h + Formula
894h + Formula	32	ELM_err_loc_err_loc_ELM_ERROR_LOCATION_5_j_j	527F 0894h + Formula
898h + Formula	32	ELM_err_loc_err_loc_ELM_ERROR_LOCATION_6_j_j	527F 0898h + Formula
89Ch + Formula	32	ELM_err_loc_err_loc_ELM_ERROR_LOCATION_7_j_j	527F 089Ch + Formula
8A0h + Formula	32	ELM_err_loc_err_loc_ELM_ERROR_LOCATION_8_j_j	527F 08A0h + Formula
8A4h + Formula	32	ELM_err_loc_err_loc_ELM_ERROR_LOCATION_9_j_j	527F 08A4h + Formula
8A8h + Formula	32	ELM_err_loc_err_loc_ELM_ERROR_LOCATION_10_j_j	527F 08A8h + Formula
8ACh + Formula	32	ELM_err_loc_err_loc_ELM_ERROR_LOCATION_11_j_j	527F 08ACh + Formula
8B0h + Formula	32	ELM_err_loc_err_loc_ELM_ERROR_LOCATION_12_j_j	527F 08B0h + Formula
8B4h + Formula	32	ELM_err_loc_err_loc_ELM_ERROR_LOCATION_13_j_j	527F 08B4h + Formula
8B8h + Formula	32	ELM_err_loc_err_loc_ELM_ERROR_LOCATION_14_j_j	527F 08B8h + Formula

Table 4-4405. , Registers, Base Address=0X00000000527F0000, Length=4096 (continued)

Offset	Length	Register Name	ELM0 Physical Address
8BCh + Formula	32	ELM_err_loc_err_loc_ELM_ERROR_LOCATION_15_j_j	527F 08BCh + Formula

4.27.1 ELM_ELM_REVISION Registers

4.27.1.1 ELM_REVISION Register (Offset = 0h) [reset = 20h]

Short Description: This register contains th

Long Description: This register contains the IP revision code. (A write to this register has no effect, the same as the reset)

Return to Summary Table

Table 4-4406. Instance Table

Instance Name	Physical Address
ELM0	527F 0000h

Figure 4-2084. ELM_ELM_REVISION Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_0															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_0								REV_NUMBER							
R								R							
0h								20h							

Access Types Legend

Table 4-4407. ELM_ELM_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_0	R	0h	Read returns 0 Reset Source: mod_g_arst_n
7:0	REV_NUMBER	R	20h	IP revision number [RTL] [7:4] Major revision [3:0] Minor revision Reset Source: mod_g_arst_n

4.27.2 ELM_ELM_SYSCONFIG Registers

4.27.2.1 ELM_SYSCONFIG Register (Offset = 10h) [reset = 11h]

Short Description: This register allows cont

Long Description: This register allows controlling various parameters of the OCP interface

Return to Summary Table

Table 4-4408. Instance Table

Instance Name	Physical Address
ELM0	527F 0010h

Figure 4-2085. ELM_ELM_SYSCONFIG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_2															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2							CLOCKACTIVITYOCP	RESERVED_1			SIDLEMODE		RESERVED_0	SOFTRESET	AUTOGATING
R							R/W	R			R/W		R	R/W	R/W
0h							0h	0h			2h		0h	0h	1h

Access Types Legend

Table 4-4409. ELM_ELM_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED_2	R	0h	Reserved Reset Source: mod_g_arst_n
8	CLOCKACTIVITYOCP	R/W	0h	OCP Clock activity when module is in IDLE mode [during wake up mode period] Reset Source: mod_g_arst_n
7:5	RESERVED_1	R	0h	Reserved Reset Source: mod_g_arst_n
4:3	SIDLEMODE	R/W	2h	Slave interface power management [IDLE req/ack control] Reset Source: mod_g_arst_n
2	RESERVED_0	R	0h	Reserved Reset Source: mod_g_arst_n
1	SOFTRESET	R/W	0h	Module Software Reset The bit is automatically reset by the hardware [During reads, it always returns 0] It has same effect as the OCP Hardware reset Reset Source: mod_g_arst_n
0	AUTOGATING	R/W	1h	Internal OCP clock gating strategy [no module visible impact other than saving power] Reset Source: mod_g_arst_n

4.27.3 ELM_ELM_SYSSTATUS Registers

4.27.3.1 ELM_SYSSTATUS Register (Offset = 14h) [reset = 0h]

Short Description: Internal Reset monitoring

Long Description: Internal Reset monitoring (OCP domain) Undefined since: on HW perspective reset state is 0 on SW user perspective when module is accessible is 1

Return to Summary Table

Table 4-4410. Instance Table

Instance Name	Physical Address
ELM0	527F 0014h

Figure 4-2086. ELM_ELM_SYSSTATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_0															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_0															RESETDONE
R															R
0h															0h

Access Types Legend

Table 4-4411. ELM_ELM_SYSSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED_0	R	0h	Reserved Reset Source: mod_g_arst_n
0	RESETDONE	R	0h	Internal Reset monitoring [OCP domain] Undefined since: on HW perspective reset state is 0 on SW user perspective when module is accessible is 1 Reset Source: mod_g_arst_n

4.27.4 ELM_ELM_IRQSTATUS Registers

4.27.4.1 ELM_IRQSTATUS Register (Offset = 18h) [reset = 0h]

Short Description: Interrupt status. This re

Long Description: Interrupt status. This register doubles as a status register for the error location processes.

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Table 4-4412. Instance Table

Instance Name	Physical Address
ELM0	527F 0018h

Figure 4-2087. ELM_ELM_IRQSTATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_0															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_0							PAGE_VALID	LOC_VALID_7	LOC_VALID_6	LOC_VALID_5	LOC_VALID_4	LOC_VALID_3	LOC_VALID_2	LOC_VALID_1	LOC_VALID_0
R							R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h							0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4413. ELM_ELM_IRQSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED_0	R	0h	Reserved Reset Source: mod_g_arst_n
8	PAGE_VALID	R/W1TC	0h	Error location status for a full page, based on the mask definition Read 0x0: error locations invalid for all polynomials enabled in the ECC_INTERRUPT_MASK register Read 0x1: all error locations valid Write 0x0: no effect Write 0x1: clear interrupt Reset Source: mod_g_arst_n
7	LOC_VALID_7	R/W1TC	0h	Error location status for syndrome polynomial 7 Read 0x0: no syndrome processed or process in progress Read 0x1: error location process completed Write 0x0: no effect Write 0x1: clear interrupt Reset Source: mod_g_arst_n
6	LOC_VALID_6	R/W1TC	0h	Error location status for syndrome polynomial 6 Reset Source: mod_g_arst_n
5	LOC_VALID_5	R/W1TC	0h	Error location status for syndrome polynomial 5 Reset Source: mod_g_arst_n
4	LOC_VALID_4	R/W1TC	0h	Error location status for syndrome polynomial 4 Reset Source: mod_g_arst_n
3	LOC_VALID_3	R/W1TC	0h	Error location status for syndrome polynomial 3 Reset Source: mod_g_arst_n
2	LOC_VALID_2	R/W1TC	0h	Error location status for syndrome polynomial 2 Reset Source: mod_g_arst_n
1	LOC_VALID_1	R/W1TC	0h	Error location status for syndrome polynomial 1 Reset Source: mod_g_arst_n
0	LOC_VALID_0	R/W1TC	0h	Error location status for syndrome polynomial 0 Reset Source: mod_g_arst_n

4.27.5 ELM_ELM_IRQENABLE Registers

4.27.5.1 ELM_IRQENABLE Register (Offset = 1Ch) [reset = 0h]

Short Description: Interrupt enable

Long Description: Interrupt enable

Return to Summary Table

Table 4-4414. Instance Table

Instance Name	Physical Address
ELM0	527F 001Ch

Figure 4-2088. ELM_ELM_IRQENABLE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_0															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_0							PAGE_MASK	LOCATION_MASK_7	LOCATION_MASK_6	LOCATION_MASK_5	LOCATION_MASK_4	LOCATION_MASK_3	LOCATION_MASK_2	LOCATION_MASK_1	LOCATION_MASK_0
R							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h							0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4415. ELM_ELM_IRQENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED_0	R	0h	Reserved Reset Source: mod_g_arst_n
8	PAGE_MASK	R/W	0h	Page interrupt mask bit 0: disable interrupt 1: enable interrupt Reset Source: mod_g_arst_n
7	LOCATION_MASK_7	R/W	0h	Error location interrupt mask bit for syndrome polynomial 7 Reset Source: mod_g_arst_n
6	LOCATION_MASK_6	R/W	0h	Error location interrupt mask bit for syndrome polynomial 6 Reset Source: mod_g_arst_n
5	LOCATION_MASK_5	R/W	0h	Error location interrupt mask bit for syndrome polynomial 5 Reset Source: mod_g_arst_n
4	LOCATION_MASK_4	R/W	0h	Error location interrupt mask bit for syndrome polynomial 4 Reset Source: mod_g_arst_n
3	LOCATION_MASK_3	R/W	0h	Error location interrupt mask bit for syndrome polynomial 3 Reset Source: mod_g_arst_n
2	LOCATION_MASK_2	R/W	0h	Error location interrupt mask bit for syndrome polynomial 2 Reset Source: mod_g_arst_n
1	LOCATION_MASK_1	R/W	0h	Error location interrupt mask bit for syndrome polynomial 1 Reset Source: mod_g_arst_n
0	LOCATION_MASK_0	R/W	0h	Error location interrupt mask bit for syndrome polynomial 0 0: disable interrupt 1: enable interrupt Reset Source: mod_g_arst_n

4.27.6 ELM_ELM_LOCATION_CONFIG Registers

4.27.6.1 ELM_LOCATION_CONFIG Register (Offset = 20h) [reset = 0h]

Short Description: ECC algorithm parameters

Long Description: ECC algorithm parameters

Return to Summary Table

Table 4-4416. Instance Table

Instance Name	Physical Address
ELM0	527F 0020h

Figure 4-2089. ELM_ELM_LOCATION_CONFIG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1					ECC_SIZE										
R					R/W										
0h					0h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_0														ECC_BCH_LEVEL	
R														R/W	
0h														0h	

Access Types Legend

Table 4-4417. ELM_ELM_LOCATION_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED_1	R	0h	Reserved Reset Source: mod_g_arst_n
26:16	ECC_SIZE	R/W	0h	Maximum size of the buffers for which the error location engine is used, in number of nibbles [4-bits entities] Reset Source: mod_g_arst_n
15:2	RESERVED_0	R	0h	Reserved Reset Source: mod_g_arst_n
1:0	ECC_BCH_LEVEL	R/W	0h	Error correction level 0x0: 4 bits 0x1: 8 bits 0x2: 16 bits 0x3: reserved Reset Source: mod_g_arst_n

4.27.7 ELM_ELM_PAGE_CTRL Registers

4.27.7.1 ELM_PAGE_CTRL Register (Offset = 80h) [reset = 0h]

Short Description: Page definition

Long Description: Page definition

Return to Summary Table

Table 4-4418. Instance Table

Instance Name	Physical Address
ELM0	527F 0080h

Figure 4-2090. ELM_ELM_PAGE_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_0															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_0								SECTOR_7	SECTOR_6	SECTOR_5	SECTOR_4	SECTOR_3	SECTOR_2	SECTOR_1	SECTOR_0
R								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4419. ELM_ELM_PAGE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_0	R	0h	Reserved Reset Source: mod_g_arst_n
7	SECTOR_7	R/W	0h	Set to 1 if syndrome polynomial 7 is part of the page in page mode Must be 0 in continuous mode Reset Source: mod_g_arst_n
6	SECTOR_6	R/W	0h	Set to 1 if syndrome polynomial 6 is part of the page in page mode Must be 0 in continuous mode Reset Source: mod_g_arst_n
5	SECTOR_5	R/W	0h	Set to 1 if syndrome polynomial 5 is part of the page in page mode Must be 0 in continuous mode Reset Source: mod_g_arst_n
4	SECTOR_4	R/W	0h	Set to 1 if syndrome polynomial 4 is part of the page in page mode Must be 0 in continuous mode Reset Source: mod_g_arst_n
3	SECTOR_3	R/W	0h	Set to 1 if syndrome polynomial 3 is part of the page in page mode Must be 0 in continuous mode Reset Source: mod_g_arst_n
2	SECTOR_2	R/W	0h	Set to 1 if syndrome polynomial 2 is part of the page in page mode Must be 0 in continuous mode Reset Source: mod_g_arst_n
1	SECTOR_1	R/W	0h	Set to 1 if syndrome polynomial 1 is part of the page in page mode Must be 0 in continuous mode Reset Source: mod_g_arst_n
0	SECTOR_0	R/W	0h	Set to 1 if syndrome polynomial 0 is part of the page in page mode Must be 0 in continuous mode Reset Source: mod_g_arst_n

4.27.8 ELM_POLY_POLY_ELM_SYNDROME_FRAGMENT_0_J_J Registers

4.27.8.1 POLY_POLY_ELM_SYNDROME_FRAGMENT_0_J_J Register (Offset = 400h) [reset = 0h]

Short Description: Input syndrome polynomial

Long Description: Input syndrome polynomial bits 0 to 31.

Return to Summary Table

Offset = 400h + (j * 40h); where j = 0h to 7h

Table 4-4420. Instance Table

Instance Name	Physical Address
ELM0	527F 0400h

Figure 4-2091. ELM_POLY_POLY_ELM_SYNDROME_FRAGMENT_0_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SYNDROME_0															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNDROME_0															
R/W															
0h															

Access Types Legend

Table 4-4421. ELM_POLY_POLY_ELM_SYNDROME_FRAGMENT_0_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SYNDROME_0	R/W	0h	Syndrome bits 0 to 31 Reset Source: mod_g_arst_n

4.27.9 ELM_POLY_POLY_ELM_SYNDROME_FRAGMENT_1_J_J Registers

4.27.9.1 POLY_POLY_ELM_SYNDROME_FRAGMENT_1_J_J Register (Offset = 404h) [reset = 0h]

Short Description: Input syndrome polynomial

Long Description: Input syndrome polynomial bits 32 to 63.

Return to Summary Table

Offset = 404h + (j * 40h); where j = 0h to 7h

Table 4-4422. Instance Table

Instance Name	Physical Address
ELM0	527F 0404h

Figure 4-2092. ELM_POLY_POLY_ELM_SYNDROME_FRAGMENT_1_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SYNDROME_1															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNDROME_1															
R/W															
0h															

Access Types Legend

Table 4-4423. ELM_POLY_POLY_ELM_SYNDROME_FRAGMENT_1_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SYNDROME_1	R/W	0h	Syndrome bits 32 to 63 Reset Source: mod_g_arst_n

4.27.10 ELM_POLY_POLY_ELM_SYNDROME_FRAGMENT_2_J_J Registers

4.27.10.1 POLY_POLY_ELM_SYNDROME_FRAGMENT_2_J_J Register (Offset = 408h) [reset = 0h]

Short Description: Input syndrome polynomial

Long Description: Input syndrome polynomial bits 64 to 95.

Return to Summary Table

Offset = 408h + (j * 40h); where j = 0h to 7h

Table 4-4424. Instance Table

Instance Name	Physical Address
ELM0	527F 0408h

Figure 4-2093. ELM_POLY_POLY_ELM_SYNDROME_FRAGMENT_2_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SYNDROME_2															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNDROME_2															
R/W															
0h															

Access Types Legend

Table 4-4425. ELM_POLY_POLY_ELM_SYNDROME_FRAGMENT_2_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SYNDROME_2	R/W	0h	Syndrome bits 64 to 95 Reset Source: mod_g_arst_n

4.27.11 ELM_POLY_POLY_ELM_SYNDROME_FRAGMENT_3_J_J Registers

4.27.11.1 POLY_POLY_ELM_SYNDROME_FRAGMENT_3_J_J Register (Offset = 40Ch) [reset = 0h]

Short Description: Input syndrome polynomial

Long Description: Input syndrome polynomial bits 96 to 127

Return to Summary Table

Offset = 40ch + (j * 40h); where j = 0h to 7h

Table 4-4426. Instance Table

Instance Name	Physical Address
ELM0	527F 040Ch

Figure 4-2094. ELM_POLY_POLY_ELM_SYNDROME_FRAGMENT_3_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SYNDROME_3															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNDROME_3															
R/W															
0h															

Access Types Legend

Table 4-4427. ELM_POLY_POLY_ELM_SYNDROME_FRAGMENT_3_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SYNDROME_3	R/W	0h	Syndrome bits 96 to 127 Reset Source: mod_g_arst_n

4.27.12 ELM_POLY_POLY_ELM_SYNDROME_FRAGMENT_4_J_J Registers

4.27.12.1 POLY_POLY_ELM_SYNDROME_FRAGMENT_4_J_J Register (Offset = 410h) [reset = 0h]

Short Description: Input syndrome polynomial

Long Description: Input syndrome polynomial bits 128 to 159.

Return to Summary Table

Offset = 410h + (j * 40h); where j = 0h to 7h

Table 4-4428. Instance Table

Instance Name	Physical Address
ELM0	527F 0410h

Figure 4-2095. ELM_POLY_POLY_ELM_SYNDROME_FRAGMENT_4_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SYNDROME_4															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNDROME_4															
R/W															
0h															

Access Types Legend

Table 4-4429. ELM_POLY_POLY_ELM_SYNDROME_FRAGMENT_4_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SYNDROME_4	R/W	0h	Syndrome bits 128 to 159 Reset Source: mod_g_arst_n

4.27.13 ELM_POLY_POLY_ELM_SYNDROME_FRAGMENT_5_J_J Registers

4.27.13.1 POLY_POLY_ELM_SYNDROME_FRAGMENT_5_J_J Register (Offset = 414h) [reset = 0h]

Short Description: Input syndrome polynomial

Long Description: Input syndrome polynomial bits 160 to 191.

Return to Summary Table

Offset = 414h + (j * 40h); where j = 0h to 7h

Table 4-4430. Instance Table

Instance Name	Physical Address
ELM0	527F 0414h

Figure 4-2096. ELM_POLY_POLY_ELM_SYNDROME_FRAGMENT_5_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SYNDROME_5															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNDROME_5															
R/W															
0h															

Access Types Legend

Table 4-4431. ELM_POLY_POLY_ELM_SYNDROME_FRAGMENT_5_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SYNDROME_5	R/W	0h	Syndrome bits 160 to 191 Reset Source: mod_g_arst_n

4.27.14 ELM_POLY_POLY_ELM_SYNDROME_FRAGMENT_6_J_J Registers

4.27.14.1 POLY_POLY_ELM_SYNDROME_FRAGMENT_6_J_J Register (Offset = 418h) [reset = 0h]

Short Description: Input syndrome polynomial

Long Description: Input syndrome polynomial bits 192 to 207.

Return to Summary Table

Offset = 418h + (j * 40h); where j = 0h to 7h

Table 4-4432. Instance Table

Instance Name	Physical Address
ELM0	527F 0418h

Figure 4-2097. ELM_POLY_POLY_ELM_SYNDROME_FRAGMENT_6_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															SYNDROME_VALID
R															R/W
0h															0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNDROME_6															
R/W															
0h															

Access Types Legend

Table 4-4433. ELM_POLY_POLY_ELM_SYNDROME_FRAGMENT_6_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	R		Reserved Reset Source: mod_g_arst_n
16	SYNDROME_VALID	R/W	0h	Syndrome valid bit 0x0: this syndrome polynomial should not be processed 0x1: this syndrome polynomial must be processed Reset Source: mod_g_arst_n
15:0	SYNDROME_6	R/W	0h	Syndrome bits 192 to 207 Reset Source: mod_g_arst_n

4.27.15 ELM_ERR_LOC_ERR_LOC_ELM_LOCATION_STATUS_J_J Registers

4.27.15.1 ERR_LOC_ERR_LOC_ELM_LOCATION_STATUS_J_J Register (Offset = 800h) [reset = 0h]

Short Description: Exit status for the syndr

Long Description: Exit status for the syndrome polynomial processing

Return to Summary Table

Offset = 800h + (j * 100h); where j = 0h to 7h

Table 4-4434. Instance Table

Instance Name	Physical Address
ELM0	527F 0800h

Figure 4-2098. ELM_ERR_LOC_ERR_LOC_ELM_LOCATION_STATUS_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_0															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_0							ECC_CORRECTABLE	RESERVED_1			ECC_NB_ERRORS				
R							R	R			R				
0h							0h	0h			0h				

Access Types Legend

Table 4-4435. ELM_ERR_LOC_ERR_LOC_ELM_LOCATION_STATUS_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED_0	R	0h	Reserved Reset Source: mod_g_arst_n
8	ECC_CORRECTABLE	R	0h	Error location process exit status 0x0: ECC error location process failed Number of errors and error locations are invalid 0x1: all errors were successfully located Number of errors and error locations are valid Reset Source: mod_g_arst_n
7:5	RESERVED_1	R	0h	Reserved Reset Source: mod_g_arst_n
4:0	ECC_NB_ERRORS	R	0h	Number of errors detected and located Reset Source: mod_g_arst_n

4.27.16 ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_0_J_J Registers

4.27.16.1 ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_0_J_J Register (Offset = 880h) [reset = 0h]

Short Description: Error location register

Long Description: Error location register

Return to Summary Table

Offset = 880h + (j * 100h); where j = 0h to 7h

Table 4-4436. Instance Table

Instance Name	Physical Address
ELM0	527F 0880h

Figure 4-2099. ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_0_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_0															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_0			ECC_ERROR_LOCATION												
R			R												
0h			0h												

Access Types Legend

Table 4-4437. ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_0_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_0	R	0h	Reserved Reset Source: mod_g_arst_n
12:0	ECC_ERROR_LOCATION	R	0h	Error location bit address Reset Source: mod_g_arst_n

4.27.17 ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_1_J_J Registers

4.27.17.1 ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_1_J_J Register (Offset = 884h) [reset = 0h]

Short Description: Error location register

Long Description: Error location register

Return to Summary Table

Offset = 884h + (j * 100h); where j = 0h to 7h

Table 4-4438. Instance Table

Instance Name	Physical Address
ELM0	527F 0884h

Figure 4-2100. ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_1_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_0															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_0			ECC_ERROR_LOCATION												
R			R												
0h			0h												

Access Types Legend

Table 4-4439. ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_1_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_0	R	0h	Reserved Reset Source: mod_g_arst_n
12:0	ECC_ERROR_LOCATION	R	0h	Error location bit address Reset Source: mod_g_arst_n

4.27.18 ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_2_J_J Registers

4.27.18.1 ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_2_J_J Register (Offset = 888h) [reset = 0h]

Short Description: Error location register

Long Description: Error location register

Return to Summary Table

Offset = 888h + (j * 100h); where j = 0h to 7h

Table 4-4440. Instance Table

Instance Name	Physical Address
ELM0	527F 0888h

Figure 4-2101. ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_2_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_0															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_0			ECC_ERROR_LOCATION												
R			R												
0h			0h												

Access Types Legend

Table 4-4441. ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_2_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_0	R	0h	Reserved Reset Source: mod_g_arst_n
12:0	ECC_ERROR_LOCATION	R	0h	Error location bit address Reset Source: mod_g_arst_n

4.27.19 ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_3_J_J Registers

4.27.19.1 ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_3_J_J Register (Offset = 88Ch) [reset = 0h]

Short Description: Error location register

Long Description: Error location register

Return to Summary Table

Offset = 88ch + (j * 100h); where j = 0h to 7h

Table 4-4442. Instance Table

Instance Name	Physical Address
ELM0	527F 088Ch

Figure 4-2102. ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_3_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_0															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_0			ECC_ERROR_LOCATION												
R			R												
0h			0h												

Access Types Legend

Table 4-4443. ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_3_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_0	R	0h	Reserved Reset Source: mod_g_arst_n
12:0	ECC_ERROR_LOCATION	R	0h	Error location bit address Reset Source: mod_g_arst_n

4.27.20 ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_4_J_J Registers

4.27.20.1 ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_4_J_J Register (Offset = 890h) [reset = 0h]

Short Description: Error location register

Long Description: Error location register

Return to Summary Table

Offset = 890h + (j * 100h); where j = 0h to 7h

Table 4-4444. Instance Table

Instance Name	Physical Address
ELM0	527F 0890h

Figure 4-2103. ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_4_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_0															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_0			ECC_ERROR_LOCATION												
R			R												
0h			0h												

Access Types Legend

Table 4-4445. ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_4_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_0	R	0h	Reserved Reset Source: mod_g_arst_n
12:0	ECC_ERROR_LOCATION	R	0h	Error location bit address Reset Source: mod_g_arst_n

4.27.21 ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_5_J_J Registers

4.27.21.1 ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_5_J_J Register (Offset = 894h) [reset = 0h]

Short Description: Error location register

Long Description: Error location register

Return to Summary Table

Offset = 894h + (j * 100h); where j = 0h to 7h

Table 4-4446. Instance Table

Instance Name	Physical Address
ELM0	527F 0894h

Figure 4-2104. ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_5_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_0															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_0			ECC_ERROR_LOCATION												
R			R												
0h			0h												

Access Types Legend

Table 4-4447. ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_5_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_0	R	0h	Reserved Reset Source: mod_g_arst_n
12:0	ECC_ERROR_LOCATION	R	0h	Error location bit address Reset Source: mod_g_arst_n

4.27.22 ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_6_J_J Registers

4.27.22.1 ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_6_J_J Register (Offset = 898h) [reset = 0h]

Short Description: Error location register

Long Description: Error location register

Return to Summary Table

Offset = 898h + (j * 100h); where j = 0h to 7h

Table 4-4448. Instance Table

Instance Name	Physical Address
ELM0	527F 0898h

Figure 4-2105. ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_6_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_0															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_0			ECC_ERROR_LOCATION												
R			R												
0h			0h												

Access Types Legend

Table 4-4449. ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_6_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_0	R	0h	Reserved Reset Source: mod_g_arst_n
12:0	ECC_ERROR_LOCATION	R	0h	Error location bit address Reset Source: mod_g_arst_n

4.27.23 ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_7_J_J Registers

4.27.23.1 ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_7_J_J Register (Offset = 89Ch) [reset = 0h]

Short Description: Error location register

Long Description: Error location register

Return to Summary Table

Offset = 89ch + (j * 100h); where j = 0h to 7h

Table 4-4450. Instance Table

Instance Name	Physical Address
ELM0	527F 089Ch

Figure 4-2106. ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_7_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_0															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_0			ECC_ERROR_LOCATION												
R			R												
0h			0h												

Access Types Legend

Table 4-4451. ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_7_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_0	R	0h	Reserved Reset Source: mod_g_arst_n
12:0	ECC_ERROR_LOCATION	R	0h	Error location bit address Reset Source: mod_g_arst_n

4.27.24 ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_8_J_J Registers

4.27.24.1 ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_8_J_J Register (Offset = 8A0h) [reset = 0h]

Short Description: Error location register

Long Description: Error location register

Return to Summary Table

Offset = 8a0h + (j * 100h); where j = 0h to 7h

Table 4-4452. Instance Table

Instance Name	Physical Address
ELM0	527F 08A0h

Figure 4-2107. ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_8_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_0															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_0			ECC_ERROR_LOCATION												
R			R												
0h			0h												

Access Types Legend

Table 4-4453. ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_8_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_0	R	0h	Reserved Reset Source: mod_g_arst_n
12:0	ECC_ERROR_LOCATION	R	0h	Error location bit address Reset Source: mod_g_arst_n

4.27.25 ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_9_J_J Registers

4.27.25.1 ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_9_J_J Register (Offset = 8A4h) [reset = 0h]

Short Description: Error location register

Long Description: Error location register

Return to Summary Table

Offset = 8a4h + (j * 100h); where j = 0h to 7h

Table 4-4454. Instance Table

Instance Name	Physical Address
ELM0	527F 08A4h

Figure 4-2108. ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_9_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_0															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_0			ECC_ERROR_LOCATION												
R			R												
0h			0h												

Access Types Legend

Table 4-4455. ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_9_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_0	R	0h	Reserved Reset Source: mod_g_arst_n
12:0	ECC_ERROR_LOCATION	R	0h	Error location bit address Reset Source: mod_g_arst_n

4.27.26 ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_10_J_J Registers

4.27.26.1 ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_10_J_J Register (Offset = 8A8h) [reset = 0h]

Short Description: Error location register

Long Description: Error location register

Return to Summary Table

Offset = 8a8h + (j * 100h); where j = 0h to 7h

Table 4-4456. Instance Table

Instance Name	Physical Address
ELM0	527F 08A8h

Figure 4-2109. ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_10_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_0															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_0			ECC_ERROR_LOCATION												
R			R												
0h			0h												

Access Types Legend

Table 4-4457. ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_10_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_0	R	0h	Reserved Reset Source: mod_g_arst_n
12:0	ECC_ERROR_LOCATION	R	0h	Error location bit address Reset Source: mod_g_arst_n

4.27.27 ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_11_J_J Registers

4.27.27.1 ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_11_J_J Register (Offset = 8ACh) [reset = 0h]

Short Description: Error location register

Long Description: Error location register

Return to Summary Table

Offset = 8ach + (j * 100h); where j = 0h to 7h

Table 4-4458. Instance Table

Instance Name	Physical Address
ELM0	527F 08ACh

Figure 4-2110. ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_11_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_0															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_0			ECC_ERROR_LOCATION												
R			R												
0h			0h												

Access Types Legend

Table 4-4459. ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_11_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_0	R	0h	Reserved Reset Source: mod_g_arst_n
12:0	ECC_ERROR_LOCATION	R	0h	Error location bit address Reset Source: mod_g_arst_n

4.27.28 ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_12_J_J Registers

4.27.28.1 ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_12_J_J Register (Offset = 8B0h) [reset = 0h]

Short Description: Error location register

Long Description: Error location register

Return to Summary Table

Offset = 8b0h + (j * 100h); where j = 0h to 7h

Table 4-4460. Instance Table

Instance Name	Physical Address
ELM0	527F 08B0h

Figure 4-2111. ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_12_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_0															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_0			ECC_ERROR_LOCATION												
R			R												
0h			0h												

Access Types Legend

Table 4-4461. ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_12_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_0	R	0h	Reserved Reset Source: mod_g_arst_n
12:0	ECC_ERROR_LOCATION	R	0h	Error location bit address Reset Source: mod_g_arst_n

4.27.29 ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_13_J_J Registers

4.27.29.1 ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_13_J_J Register (Offset = 8B4h) [reset = 0h]

Short Description: Error location register

Long Description: Error location register

Return to Summary Table

Offset = 8b4h + (j * 100h); where j = 0h to 7h

Table 4-4462. Instance Table

Instance Name	Physical Address
ELM0	527F 08B4h

Figure 4-2112. ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_13_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_0															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_0			ECC_ERROR_LOCATION												
R			R												
0h			0h												

Access Types Legend

Table 4-4463. ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_13_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_0	R	0h	Reserved Reset Source: mod_g_arst_n
12:0	ECC_ERROR_LOCATION	R	0h	Error location bit address Reset Source: mod_g_arst_n

4.27.30 ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_14_J_J Registers

4.27.30.1 ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_14_J_J Register (Offset = 8B8h) [reset = 0h]

Short Description: Error location register

Long Description: Error location register

Return to Summary Table

Offset = 8b8h + (j * 100h); where j = 0h to 7h

Table 4-4464. Instance Table

Instance Name	Physical Address
ELM0	527F 08B8h

Figure 4-2113. ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_14_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_0															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_0			ECC_ERROR_LOCATION												
R			R												
0h			0h												

Access Types Legend

Table 4-4465. ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_14_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_0	R	0h	Reserved Reset Source: mod_g_arst_n
12:0	ECC_ERROR_LOCATION	R	0h	Error location bit address Reset Source: mod_g_arst_n

4.27.31 ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_15_J_J Registers

4.27.31.1 ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_15_J_J Register (Offset = 8BCh) [reset = 0h]

Short Description: Error location register

Long Description: Error location register

Return to Summary Table

Offset = 8bch + (j * 100h); where j = 0h to 7h

Table 4-4466. Instance Table

Instance Name	Physical Address
ELM0	527F 08BCh

Figure 4-2114. ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_15_J_J Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_0															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_0			ECC_ERROR_LOCATION												
R			R												
0h			0h												

Access Types Legend

Table 4-4467. ELM_ERR_LOC_ERR_LOC_ELM_ERROR_LOCATION_15_J_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_0	R	0h	Reserved Reset Source: mod_g_arst_n
12:0	ECC_ERROR_LOCATION	R	0h	Error location bit address Reset Source: mod_g_arst_n

4.27.32 Access Table

Table 4-4468. Access Type Codes

Access Type	Code	Description
R	R	Read
R/W	R/W	Read / Write
R/W1TC	R/W1TC	Read/Write 1 To Clear

4.28 EDMA Registers

Table 4-4469. TPCC, TPCC Registers, Base Address=0X0000000052A00000, Length=32768

Offset	Length	Register Name	edma0 Physical Address
0h	32	PID	52A0 0000h
4h	32	CCCFG	52A0 0004h
200h	32	QCHMAPN	52A0 0200h
240h	32	DMAQNUMN	52A0 0240h
260h	32	QDMAQNUM	52A0 0260h
280h	32	QUETCMAP	52A0 0280h
284h	32	QUEPRI	52A0 0284h
300h	32	EMR	52A0 0300h
304h	32	EMRH	52A0 0304h
308h	32	EMCR	52A0 0308h
30Ch	32	EMCRH	52A0 030Ch
310h	32	QEMR	52A0 0310h
314h	32	QEMCR	52A0 0314h
318h	32	CCERR	52A0 0318h
31Ch	32	CCERRCLR	52A0 031Ch
320h	32	EEVAL	52A0 0320h
340h	32	DRAEM	52A0 0340h
344h	32	DRAEHM	52A0 0344h
380h	32	QRAEN	52A0 0380h
400h	32	QNE0	52A0 0400h
404h	32	QNE1	52A0 0404h
408h	32	QNE2	52A0 0408h
40Ch	32	QNE3	52A0 040Ch
410h	32	QNE4	52A0 0410h
414h	32	QNE5	52A0 0414h
418h	32	QNE6	52A0 0418h
41Ch	32	QNE7	52A0 041Ch
420h	32	QNE8	52A0 0420h
424h	32	QNE9	52A0 0424h
428h	32	QNE10	52A0 0428h
42Ch	32	QNE11	52A0 042Ch
430h	32	QNE12	52A0 0430h
434h	32	QNE13	52A0 0434h
438h	32	QNE14	52A0 0438h
43Ch	32	QNE15	52A0 043Ch
600h	32	QSTATN	52A0 0600h
620h	32	QWMTHRA	52A0 0620h
640h	32	CCSTAT	52A0 0640h
700h	32	AETCTL	52A0 0700h
704h	32	AETSTAT	52A0 0704h
708h	32	AETCMD	52A0 0708h
1000h	32	ER	52A0 1000h
1004h	32	ERH	52A0 1004h
1008h	32	ECR	52A0 1008h
100Ch	32	ECRH	52A0 100Ch

Table 4-4469. TPCC, TPCC Registers, Base Address=0X0000000052A00000, Length=32768 (continued)

Offset	Length	Register Name	edma0 Physical Address
1010h	32	ESR	52A0 1010h
1014h	32	ESRH	52A0 1014h
1018h	32	CER	52A0 1018h
101Ch	32	CERH	52A0 101Ch
1020h	32	EER	52A0 1020h
1024h	32	EERH	52A0 1024h
1028h	32	EECR	52A0 1028h
102Ch	32	EECRH	52A0 102Ch
1030h	32	EESR	52A0 1030h
1034h	32	EESRH	52A0 1034h
1038h	32	SER	52A0 1038h
103Ch	32	SERH	52A0 103Ch
1040h	32	SECR	52A0 1040h
1044h	32	SECRH	52A0 1044h
1050h	32	IER	52A0 1050h
1054h	32	IERH	52A0 1054h
1058h	32	IECR	52A0 1058h
105Ch	32	IECRH	52A0 105Ch
1060h	32	IESR	52A0 1060h
1064h	32	IESRH	52A0 1064h
1068h	32	IPR	52A0 1068h
106Ch	32	IPRH	52A0 106Ch
1070h	32	ICR	52A0 1070h
1074h	32	ICRH	52A0 1074h
1078h	32	IEVAL	52A0 1078h
1080h	32	QER	52A0 1080h
1084h	32	QEER	52A0 1084h
1088h	32	QEECR	52A0 1088h
108Ch	32	QEESR	52A0 108Ch
1090h	32	QSER	52A0 1090h
1094h	32	QSECR	52A0 1094h
2000h	32	ER_RN	52A0 2000h
2004h	32	ERH_RN	52A0 2004h
2008h	32	ECR_RN	52A0 2008h
200Ch	32	ECRH_RN	52A0 200Ch
2010h	32	ESR_RN	52A0 2010h
2014h	32	ESRH_RN	52A0 2014h
2018h	32	CER_RN	52A0 2018h
201Ch	32	CERH_RN	52A0 201Ch
2020h	32	EER_RN	52A0 2020h
2024h	32	EERH_RN	52A0 2024h
2028h	32	EECR_RN	52A0 2028h
202Ch	32	EECRH_RN	52A0 202Ch
2030h	32	EESR_RN	52A0 2030h
2034h	32	EESRH_RN	52A0 2034h
2038h	32	SER_RN	52A0 2038h
203Ch	32	SERH_RN	52A0 203Ch

Table 4-4469. TPCC, TPCC Registers, Base Address=0X0000000052A00000, Length=32768 (continued)

Offset	Length	Register Name	edma0 Physical Address
2040h	32	SECR_RN	52A0 2040h
2044h	32	SECRH_RN	52A0 2044h
2050h	32	IER_RN	52A0 2050h
2054h	32	IERH_RN	52A0 2054h
2058h	32	IECR_RN	52A0 2058h
205Ch	32	IECRH_RN	52A0 205Ch
2060h	32	IESR_RN	52A0 2060h
2064h	32	IESRH_RN	52A0 2064h
2068h	32	IPR_RN	52A0 2068h
206Ch	32	IPRH_RN	52A0 206Ch
2070h	32	ICR_RN	52A0 2070h
2074h	32	ICRH_RN	52A0 2074h
2078h	32	IEVAL_RN	52A0 2078h
2080h	32	QER_RN	52A0 2080h
2084h	32	QEER_RN	52A0 2084h
2088h	32	QEECR_RN	52A0 2088h
208Ch	32	QEESR_RN	52A0 208Ch
2090h	32	QSER_RN	52A0 2090h
2094h	32	QSECR_RN	52A0 2094h
4000h	32	OPT	52A0 4000h
4004h	32	SRC	52A0 4004h
4008h	32	ABCNT	52A0 4008h
400Ch	32	DST	52A0 400Ch
4010h	32	BIDX	52A0 4010h
4014h	32	LNK	52A0 4014h
4018h	32	CIDX	52A0 4018h
401Ch	32	CCNT	52A0 401Ch

Table 4-4470. TPTC, TPTC Registers, Base Address=0X0000000052A60000, Length=4096

Offset	Length	Register Name	edma0 Physical Address	edma1 Physical Address
0h	32	PID	52A6 0000h	52A4 0000h
4h	32	TCCFG	52A6 0004h	52A4 0004h
100h	32	TCSTAT	52A6 0100h	52A4 0100h
104h	32	INTSTAT	52A6 0104h	52A4 0104h
108h	32	INTEN	52A6 0108h	52A4 0108h
10Ch	32	INTCLR	52A6 010Ch	52A4 010Ch
110h	32	INTCMD	52A6 0110h	52A4 0110h
120h	32	ERRSTAT	52A6 0120h	52A4 0120h
124h	32	ERREN	52A6 0124h	52A4 0124h
128h	32	ERRCLR	52A6 0128h	52A4 0128h
12Ch	32	ERRDET	52A6 012Ch	52A4 012Ch
130h	32	ERRCMD	52A6 0130h	52A4 0130h
140h	32	RDRATE	52A6 0140h	52A4 0140h
200h	32	POPT	52A6 0200h	52A4 0200h
204h	32	PSRC	52A6 0204h	52A4 0204h
208h	32	PCNT	52A6 0208h	52A4 0208h

Table 4-4470. TPTC, TPTC Registers, Base Address=0X0000000052A60000, Length=4096 (continued)

Offset	Length	Register Name	edma0 Physical Address	edma1 Physical Address
20Ch	32	PDST	52A6 020Ch	52A4 020Ch
210h	32	PBIDX	52A6 0210h	52A4 0210h
214h	32	PMPPRXY	52A6 0214h	52A4 0214h
240h	32	SAOPT	52A6 0240h	52A4 0240h
244h	32	SASRC	52A6 0244h	52A4 0244h
248h	32	SACNT	52A6 0248h	52A4 0248h
24Ch	32	SADST	52A6 024Ch	52A4 024Ch
250h	32	SABIDX	52A6 0250h	52A4 0250h
254h	32	SAMPPRXY	52A6 0254h	52A4 0254h
258h	32	SACNTRLD	52A6 0258h	52A4 0258h
25Ch	32	SASRCBREF	52A6 025Ch	52A4 025Ch
260h	32	SADSTBREF	52A6 0260h	52A4 0260h
264h	32	SABCNT	52A6 0264h	52A4 0264h
280h	32	DFCNTRLD	52A6 0280h	52A4 0280h
284h	32	DFSRCBREF	52A6 0284h	52A4 0284h
300h	32	DFOPT0	52A6 0300h	52A4 0300h
304h	32	DFSRC0	52A6 0304h	52A4 0304h
308h	32	DFACNT0	52A6 0308h	52A4 0308h
30Ch	32	DFDST0	52A6 030Ch	52A4 030Ch
310h	32	DFBIDX0	52A6 0310h	52A4 0310h
314h	32	DFMPPRXY0	52A6 0314h	52A4 0314h
318h	32	DFBCNT0	52A6 0318h	52A4 0318h
340h	32	DFOPT1	52A6 0340h	52A4 0340h
344h	32	DFSRC1	52A6 0344h	52A4 0344h
348h	32	DFACNT1	52A6 0348h	52A4 0348h
34Ch	32	DFDST1	52A6 034Ch	52A4 034Ch
350h	32	DFBIDX1	52A6 0350h	52A4 0350h
354h	32	DFMPPRXY1	52A6 0354h	52A4 0354h
358h	32	DFBCNT1	52A6 0358h	52A4 0358h

4.28.1 TPCC_PID Registers

4.28.1.1 TPCC_PID Register (Offset = 0h) [reset = 4001ab00h]

Short Description: Peripheral ID Re

Long Description: Peripheral ID Register

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Table 4-4471. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0000h

Figure 4-2115. PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		RES1		FUNC											
R		R		R											
1h		0h		1h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL				MAJOR				CUSTOM		MINOR					
R				R				R		R					
15h				3h				0h		0h					

Access Types Legend

Table 4-4472. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID Scheme: Used to distinguish between old ID scheme and current. Spare bit to encode future schemes EDMA uses 'new scheme' indicated with value of 0x1. Reset Source: edma_rst_mod_g_rst_n
29:28	RES1	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
27:16	FUNC	R	1h	Function indicates a software compatible module family. Reset Source: edma_rst_mod_g_rst_n
15:11	RTL	R	15h	RTL Version Reset Source: edma_rst_mod_g_rst_n
10:8	MAJOR	R	3h	Major Revision Reset Source: edma_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom revision field: Not used on this version of EDMA. Reset Source: edma_rst_mod_g_rst_n
5:0	MINOR	R	0h	Minor Revision Reset Source: edma_rst_mod_g_rst_n

4.28.2 TPCC_CCCFG Registers

4.28.2.1 TPCC_CCCFG Register (Offset = 4h) [reset = 213445h]

Short Description: CC Configuration

Long Description: CC Configuration Register

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Table 4-4473. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0004h

Figure 4-2116. CCCFG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES2						MPEXIST	CHMAPEXIST	RES3		NUMREGN		RES4	NUMTC		
R						R	R	R		R		R	R		
0h						0h	0h	0h		2h		0h	1h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES5	NUMPAENTRY			RES6	NUMINTCH			RES7	NUMQDMACH			RES8	NUMDMACH		
R	R			R	R			R	R			R	R		
0h	3h			0h	4h			0h	4h			0h	5h		

Access Types Legend

Table 4-4474. CCCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RES2	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
25	MPEXIST	R	0h	Memory Protection Existence MPEXIST = 0 : No memory protection. MPEXIST = 1 : Memory Protection logic included. Reset Source: edma_rst_mod_g_rst_n
24	CHMAPEXIST	R	0h	Channel Mapping Existence CHMAPEXIST = 0 : No Channel mapping. CHMAPEXIST = 1 : Channel mapping logic included. Reset Source: edma_rst_mod_g_rst_n
23:22	RES3	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
21:20	NUMREGN	R	2h	Number of MP and Shadow regions Reset Source: edma_rst_mod_g_rst_n
19	RES4	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
18:16	NUMTC	R	1h	Number of Queues/Number of TCs Reset Source: edma_rst_mod_g_rst_n
15	RES5	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
14:12	NUMPAENTRY	R	3h	Number of PaRAM entries Reset Source: edma_rst_mod_g_rst_n
11	RES6	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
10:8	NUMINTCH	R	4h	Number of Interrupt Channels Reset Source: edma_rst_mod_g_rst_n
7	RES7	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
6:4	NUMQDMACH	R	4h	Number of QDMA Channels Reset Source: edma_rst_mod_g_rst_n
3	RES8	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
2:0	NUMDMACH	R	5h	Number of DMA Channels Reset Source: edma_rst_mod_g_rst_n

4.28.3 TPCC_QCHMAPN Registers

4.28.3.1 TPCC_QCHMAPN Register (Offset = 200h) [reset = 0h]

Short Description: QDMA Channel N M

Long Description: QDMA Channel N Mapping Register

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Table 4-4475. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0200h

Figure 4-2117. QCHMAPN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES10															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES10		PAENTRY									TRWORD			RESERVED	
R		R/W									R/W			NONE	
0h		0h									0h			0	

Access Types Legend

Table 4-4476. QCHMAPN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RES10	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
13:5	PAENTRY	R/W	0h	PaRAM Entry number for QDMA Channel N. Reset Source: edma_rst_mod_g_rst_n
4:2	TRWORD	R/W	0h	TRWORD points to the specific trigger word of the PaRAM Entry defined by PAENTRY. A write to the trigger word results in a QDMA Event being recognized. Reset Source: edma_rst_mod_g_rst_n
1:0	RESERVED	NONE		Reserved

4.28.4 TPCC_DMAQNUMN Registers

4.28.4.1 TPCC_DMAQNUMN Register (Offset = 240h) [reset = 0h]

Short Description: DMA Queue Number

Long Description: DMA Queue Number Register n Contains the Event queue number to be used for the corresponding DMA Channel.

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Table 4-4477. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0240h

Figure 4-2118. DMAQNUMN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES11		E7		RES12		E6		RES13		E5		RES14		E4	
R		R/W		R		R/W		R		R/W		R		R/W	
0h		0h		0h		0h		0h		0h		0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES15		E3		RES16		E2		RES17		E1		RES18		E0	
R		R/W		R		R/W		R		R/W		R		R/W	
0h		0h		0h		0h		0h		0h		0h		0h	

Access Types Legend

Table 4-4478. DMAQNUMN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RES11	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
30:28	E7	R/W	0h	DMA Queue Number for event #7 Reset Source: edma_rst_mod_g_rst_n
27	RES12	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
26:24	E6	R/W	0h	DMA Queue Number for event #6 Reset Source: edma_rst_mod_g_rst_n
23	RES13	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
22:20	E5	R/W	0h	DMA Queue Number for event #5 Reset Source: edma_rst_mod_g_rst_n
19	RES14	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
18:16	E4	R/W	0h	DMA Queue Number for event #4 Reset Source: edma_rst_mod_g_rst_n
15	RES15	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
14:12	E3	R/W	0h	DMA Queue Number for event #3 Reset Source: edma_rst_mod_g_rst_n
11	RES16	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
10:8	E2	R/W	0h	DMA Queue Number for event #2 Reset Source: edma_rst_mod_g_rst_n
7	RES17	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
6:4	E1	R/W	0h	DMA Queue Number for event #1 Reset Source: edma_rst_mod_g_rst_n
3	RES18	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
2:0	E0	R/W	0h	DMA Queue Number for event #0 Reset Source: edma_rst_mod_g_rst_n

4.28.5 TPCC_QDMAQNUM Registers

4.28.5.1 TPCC_QDMAQNUM Register (Offset = 260h) [reset = 0h]

Short Description: QDMA Queue Numbe

Long Description: QDMA Queue Number Register Contains the Event queue number to be used for the corresponding QDMA Channel.

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Table 4-4479. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0260h

Figure 4-2119. QDMAQNUM Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19		E7		RES20		E6		RES21		E5		RES22		E4	
R		R/W		R		R/W		R		R/W		R		R/W	
0h		0h		0h		0h		0h		0h		0h		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES23		E3		RES24		E2		RES25		E1		RES26		E0	
R		R/W		R		R/W		R		R/W		R		R/W	
0h		0h		0h		0h		0h		0h		0h		0h	

Access Types Legend

Table 4-4480. QDMAQNUM Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RES19	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
30:28	E7	R/W	0h	QDMA Queue Number for event #7 Reset Source: edma_rst_mod_g_rst_n
27	RES20	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
26:24	E6	R/W	0h	QDMA Queue Number for event #6 Reset Source: edma_rst_mod_g_rst_n
23	RES21	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
22:20	E5	R/W	0h	QDMA Queue Number for event #5 Reset Source: edma_rst_mod_g_rst_n
19	RES22	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
18:16	E4	R/W	0h	QDMA Queue Number for event #4 Reset Source: edma_rst_mod_g_rst_n
15	RES23	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
14:12	E3	R/W	0h	QDMA Queue Number for event #3 Reset Source: edma_rst_mod_g_rst_n
11	RES24	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
10:8	E2	R/W	0h	QDMA Queue Number for event #2 Reset Source: edma_rst_mod_g_rst_n
7	RES25	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
6:4	E1	R/W	0h	QDMA Queue Number for event #1 Reset Source: edma_rst_mod_g_rst_n
3	RES26	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
2:0	E0	R/W	0h	QDMA Queue Number for event #0 Reset Source: edma_rst_mod_g_rst_n

4.28.6 TPCC_QUETCMAP Registers

4.28.6.1 TPCC_QUETCMAP Register (Offset = 280h) [reset = 10h]

Short Description: Queue to TC Mapp

Long Description: Queue to TC Mapping

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Table 4-4481. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0280h

Figure 4-2120. QUETCMAP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES27															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES27									TCNUMQ1			RES28	TCNUMQ0		
R									R/W			R	R/W		
0h									1h			0h	0h		

Access Types Legend

Table 4-4482. QUETCMAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RES27	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
6:4	TCNUMQ1	R/W	1h	TC Number for Queue N: Defines the TC number that Event Queue N TRs are written to. Reset Source: edma_rst_mod_g_rst_n
3	RES28	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
2:0	TCNUMQ0	R/W	0h	TC Number for Queue N: Defines the TC number that Event Queue N TRs are written to. Reset Source: edma_rst_mod_g_rst_n

4.28.7 TPCC_QUEPRI Registers

4.28.7.1 TPCC_QUEPRI Register (Offset = 284h) [reset = 0h]

Short Description: Queue Priority

Long Description: Queue Priority

Return to Summary Table

Table 4-4483. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0284h

Figure 4-2121. QUEPRI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES29															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES29									PRIQ1			RES30	PRIQ0		
R									R/W			R	R/W		
0h									0h			0h	0h		

Access Types Legend

Table 4-4484. QUEPRI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RES29	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
6:4	PRIQ1	R/W	0h	Priority Level for Queue 1 Dictates the priority level used for the OPTIONS field programmation for Qn TRs. Sets the priority used for TC read and write commands. Reset Source: edma_rst_mod_g_rst_n
3	RES30	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
2:0	PRIQ0	R/W	0h	Priority Level for Queue 0 Dictates the priority level used for the OPTIONS field programmation for Qn TRs. Sets the priority used for TC read and write commands. Reset Source: edma_rst_mod_g_rst_n

4.28.8 TPCC_EMR Registers

4.28.8.1 TPCC_EMR Register (Offset = 300h) [reset = 0h]

Short Description: Event Missed Reg

Long Description: Event Missed Register: The Event Missed register is set if 2 events are received without the first event being cleared or if a Null TR is serviced. Chained events (CER) Set Events (ESR) and normal events (ER) are treated individually. If any bit in the EMR register is set (and all errors (including QEMR/CCERR) were previously clear) then an error will be signaled with TPCC error interrupt.

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Table 4-4485. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0300h

Figure 4-2122. EMR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4486. EMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	R	0h	Event Missed #31 Reset Source: edma_rst_mod_g_rst_n
30	E30	R	0h	Event Missed #30 Reset Source: edma_rst_mod_g_rst_n
29	E29	R	0h	Event Missed #29 Reset Source: edma_rst_mod_g_rst_n
28	E28	R	0h	Event Missed #28 Reset Source: edma_rst_mod_g_rst_n
27	E27	R	0h	Event Missed #27 Reset Source: edma_rst_mod_g_rst_n
26	E26	R	0h	Event Missed #26 Reset Source: edma_rst_mod_g_rst_n
25	E25	R	0h	Event Missed #25 Reset Source: edma_rst_mod_g_rst_n
24	E24	R	0h	Event Missed #24 Reset Source: edma_rst_mod_g_rst_n
23	E23	R	0h	Event Missed #23 Reset Source: edma_rst_mod_g_rst_n
22	E22	R	0h	Event Missed #22 Reset Source: edma_rst_mod_g_rst_n
21	E21	R	0h	Event Missed #21 Reset Source: edma_rst_mod_g_rst_n
20	E20	R	0h	Event Missed #20 Reset Source: edma_rst_mod_g_rst_n
19	E19	R	0h	Event Missed #19 Reset Source: edma_rst_mod_g_rst_n
18	E18	R	0h	Event Missed #18 Reset Source: edma_rst_mod_g_rst_n
17	E17	R	0h	Event Missed #17 Reset Source: edma_rst_mod_g_rst_n
16	E16	R	0h	Event Missed #16 Reset Source: edma_rst_mod_g_rst_n
15	E15	R	0h	Event Missed #15 Reset Source: edma_rst_mod_g_rst_n
14	E14	R	0h	Event Missed #14 Reset Source: edma_rst_mod_g_rst_n
13	E13	R	0h	Event Missed #13 Reset Source: edma_rst_mod_g_rst_n
12	E12	R	0h	Event Missed #12 Reset Source: edma_rst_mod_g_rst_n
11	E11	R	0h	Event Missed #11 Reset Source: edma_rst_mod_g_rst_n
10	E10	R	0h	Event Missed #10 Reset Source: edma_rst_mod_g_rst_n

Table 4-4486. EMR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	E9	R	0h	Event Missed #9 Reset Source: edma_rst_mod_g_rst_n
8	E8	R	0h	Event Missed #8 Reset Source: edma_rst_mod_g_rst_n
7	E7	R	0h	Event Missed #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	R	0h	Event Missed #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	R	0h	Event Missed #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	R	0h	Event Missed #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	R	0h	Event Missed #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	R	0h	Event Missed #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	R	0h	Event Missed #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	R	0h	Event Missed #0 Reset Source: edma_rst_mod_g_rst_n

4.28.9 TPCC_EMRH Registers

4.28.9.1 TPCC_EMRH Register (Offset = 304h) [reset = 0h]

Short Description: Event Missed Reg

Long Description: Event Missed Register (High Part): The Event Missed register is set if 2 events are received without the first event being cleared or if a Null TR is serviced. Chained events (CER) Set Events (ESR) and normal events (ER) are treated individually. If any bit in the EMR register is set (and all errors (including QEMR/CCERR) were previously clear) then an error will be signaled with TPCC error interrupt.

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Table 4-4487. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0304h

Figure 4-2123. EMRH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4488. EMRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	R	0h	Event Missed #63 Reset Source: edma_rst_mod_g_rst_n
30	E62	R	0h	Event Missed #62 Reset Source: edma_rst_mod_g_rst_n
29	E61	R	0h	Event Missed #61 Reset Source: edma_rst_mod_g_rst_n
28	E60	R	0h	Event Missed #60 Reset Source: edma_rst_mod_g_rst_n
27	E59	R	0h	Event Missed #59 Reset Source: edma_rst_mod_g_rst_n
26	E58	R	0h	Event Missed #58 Reset Source: edma_rst_mod_g_rst_n
25	E57	R	0h	Event Missed #57 Reset Source: edma_rst_mod_g_rst_n
24	E56	R	0h	Event Missed #56 Reset Source: edma_rst_mod_g_rst_n
23	E55	R	0h	Event Missed #55 Reset Source: edma_rst_mod_g_rst_n
22	E54	R	0h	Event Missed #54 Reset Source: edma_rst_mod_g_rst_n
21	E53	R	0h	Event Missed #53 Reset Source: edma_rst_mod_g_rst_n
20	E52	R	0h	Event Missed #52 Reset Source: edma_rst_mod_g_rst_n
19	E51	R	0h	Event Missed #51 Reset Source: edma_rst_mod_g_rst_n
18	E50	R	0h	Event Missed #50 Reset Source: edma_rst_mod_g_rst_n
17	E49	R	0h	Event Missed #49 Reset Source: edma_rst_mod_g_rst_n
16	E48	R	0h	Event Missed #48 Reset Source: edma_rst_mod_g_rst_n
15	E47	R	0h	Event Missed #47 Reset Source: edma_rst_mod_g_rst_n
14	E46	R	0h	Event Missed #46 Reset Source: edma_rst_mod_g_rst_n
13	E45	R	0h	Event Missed #45 Reset Source: edma_rst_mod_g_rst_n
12	E44	R	0h	Event Missed #44 Reset Source: edma_rst_mod_g_rst_n
11	E43	R	0h	Event Missed #43 Reset Source: edma_rst_mod_g_rst_n
10	E42	R	0h	Event Missed #42 Reset Source: edma_rst_mod_g_rst_n

Table 4-4488. EMRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	E41	R	0h	Event Missed #41 Reset Source: edma_rst_mod_g_rst_n
8	E40	R	0h	Event Missed #40 Reset Source: edma_rst_mod_g_rst_n
7	E39	R	0h	Event Missed #39 Reset Source: edma_rst_mod_g_rst_n
6	E38	R	0h	Event Missed #38 Reset Source: edma_rst_mod_g_rst_n
5	E37	R	0h	Event Missed #37 Reset Source: edma_rst_mod_g_rst_n
4	E36	R	0h	Event Missed #36 Reset Source: edma_rst_mod_g_rst_n
3	E35	R	0h	Event Missed #35 Reset Source: edma_rst_mod_g_rst_n
2	E34	R	0h	Event Missed #34 Reset Source: edma_rst_mod_g_rst_n
1	E33	R	0h	Event Missed #33 Reset Source: edma_rst_mod_g_rst_n
0	E32	R	0h	Event Missed #32 Reset Source: edma_rst_mod_g_rst_n

4.28.10 TPCC_EMCR Registers

4.28.10.1 TPCC_EMCR Register (Offset = 308h) [reset = 0h]

Short Description: Event Missed Cle

Long Description: Event Missed Clear Register: CPU write of '1' to the EMCR.En bit causes the EMR.En bit to be cleared. CPU write of '0' has no effect.. All error bits must be cleared before additional error interrupts will be asserted by CC.

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Table 4-4489. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0308h

Figure 4-2124. EMCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4490. EMCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	W	0h	Event Missed Clear #31 Reset Source: edma_rst_mod_g_rst_n
30	E30	W	0h	Event Missed Clear #30 Reset Source: edma_rst_mod_g_rst_n
29	E29	W	0h	Event Missed Clear #29 Reset Source: edma_rst_mod_g_rst_n
28	E28	W	0h	Event Missed Clear #28 Reset Source: edma_rst_mod_g_rst_n
27	E27	W	0h	Event Missed Clear #27 Reset Source: edma_rst_mod_g_rst_n
26	E26	W	0h	Event Missed Clear #26 Reset Source: edma_rst_mod_g_rst_n
25	E25	W	0h	Event Missed Clear #25 Reset Source: edma_rst_mod_g_rst_n
24	E24	W	0h	Event Missed Clear #24 Reset Source: edma_rst_mod_g_rst_n
23	E23	W	0h	Event Missed Clear #23 Reset Source: edma_rst_mod_g_rst_n
22	E22	W	0h	Event Missed Clear #22 Reset Source: edma_rst_mod_g_rst_n
21	E21	W	0h	Event Missed Clear #21 Reset Source: edma_rst_mod_g_rst_n
20	E20	W	0h	Event Missed Clear #20 Reset Source: edma_rst_mod_g_rst_n
19	E19	W	0h	Event Missed Clear #19 Reset Source: edma_rst_mod_g_rst_n
18	E18	W	0h	Event Missed Clear #18 Reset Source: edma_rst_mod_g_rst_n
17	E17	W	0h	Event Missed Clear #17 Reset Source: edma_rst_mod_g_rst_n
16	E16	W	0h	Event Missed Clear #16 Reset Source: edma_rst_mod_g_rst_n
15	E15	W	0h	Event Missed Clear #15 Reset Source: edma_rst_mod_g_rst_n
14	E14	W	0h	Event Missed Clear #14 Reset Source: edma_rst_mod_g_rst_n
13	E13	W	0h	Event Missed Clear #13 Reset Source: edma_rst_mod_g_rst_n
12	E12	W	0h	Event Missed Clear #12 Reset Source: edma_rst_mod_g_rst_n
11	E11	W	0h	Event Missed Clear #11 Reset Source: edma_rst_mod_g_rst_n
10	E10	W	0h	Event Missed Clear #10 Reset Source: edma_rst_mod_g_rst_n
9	E9	W	0h	Event Missed Clear #9 Reset Source: edma_rst_mod_g_rst_n

Table 4-4490. EMCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	E8	W	0h	Event Missed Clear #8 Reset Source: edma_rst_mod_g_rst_n
7	E7	W	0h	Event Missed Clear #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	W	0h	Event Missed Clear #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	W	0h	Event Missed Clear #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	W	0h	Event Missed Clear #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	W	0h	Event Missed Clear #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	W	0h	Event Missed Clear #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	W	0h	Event Missed Clear #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	W	0h	Event Missed Clear #0 Reset Source: edma_rst_mod_g_rst_n

4.28.11 TPCC_EMCRH Registers

4.28.11.1 TPCC_EMCRH Register (Offset = 30Ch) [reset = 0h]

Short Description: Event Missed Cle

Long Description: Event Missed Clear Register (High Part): CPU write of '1' to the EMCR.En bit causes the EMR.En bit to be cleared. CPU write of '0' has no effect.. All error bits must be cleared before additional error interrupts will be asserted by CC.

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Table 4-4491. Instance Table

Instance Name	Physical Address
EDMA0	52A0 030Ch

Figure 4-2125. EMCRH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4492. EMCRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	W	0h	Event Missed Clear #63 Reset Source: edma_rst_mod_g_rst_n
30	E62	W	0h	Event Missed Clear #62 Reset Source: edma_rst_mod_g_rst_n
29	E61	W	0h	Event Missed Clear #61 Reset Source: edma_rst_mod_g_rst_n
28	E60	W	0h	Event Missed Clear #60 Reset Source: edma_rst_mod_g_rst_n
27	E59	W	0h	Event Missed Clear #59 Reset Source: edma_rst_mod_g_rst_n
26	E58	W	0h	Event Missed Clear #58 Reset Source: edma_rst_mod_g_rst_n
25	E57	W	0h	Event Missed Clear #57 Reset Source: edma_rst_mod_g_rst_n
24	E56	W	0h	Event Missed Clear #56 Reset Source: edma_rst_mod_g_rst_n
23	E55	W	0h	Event Missed Clear #55 Reset Source: edma_rst_mod_g_rst_n
22	E54	W	0h	Event Missed Clear #54 Reset Source: edma_rst_mod_g_rst_n
21	E53	W	0h	Event Missed Clear #53 Reset Source: edma_rst_mod_g_rst_n
20	E52	W	0h	Event Missed Clear #52 Reset Source: edma_rst_mod_g_rst_n
19	E51	W	0h	Event Missed Clear #51 Reset Source: edma_rst_mod_g_rst_n
18	E50	W	0h	Event Missed Clear #50 Reset Source: edma_rst_mod_g_rst_n
17	E49	W	0h	Event Missed Clear #49 Reset Source: edma_rst_mod_g_rst_n
16	E48	W	0h	Event Missed Clear #48 Reset Source: edma_rst_mod_g_rst_n
15	E47	W	0h	Event Missed Clear #47 Reset Source: edma_rst_mod_g_rst_n
14	E46	W	0h	Event Missed Clear #46 Reset Source: edma_rst_mod_g_rst_n
13	E45	W	0h	Event Missed Clear #45 Reset Source: edma_rst_mod_g_rst_n
12	E44	W	0h	Event Missed Clear #44 Reset Source: edma_rst_mod_g_rst_n
11	E43	W	0h	Event Missed Clear #43 Reset Source: edma_rst_mod_g_rst_n
10	E42	W	0h	Event Missed Clear #42 Reset Source: edma_rst_mod_g_rst_n
9	E41	W	0h	Event Missed Clear #41 Reset Source: edma_rst_mod_g_rst_n

Table 4-4492. EMCRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	E40	W	0h	Event Missed Clear #40 Reset Source: edma_rst_mod_g_rst_n
7	E39	W	0h	Event Missed Clear #39 Reset Source: edma_rst_mod_g_rst_n
6	E38	W	0h	Event Missed Clear #38 Reset Source: edma_rst_mod_g_rst_n
5	E37	W	0h	Event Missed Clear #37 Reset Source: edma_rst_mod_g_rst_n
4	E36	W	0h	Event Missed Clear #36 Reset Source: edma_rst_mod_g_rst_n
3	E35	W	0h	Event Missed Clear #35 Reset Source: edma_rst_mod_g_rst_n
2	E34	W	0h	Event Missed Clear #34 Reset Source: edma_rst_mod_g_rst_n
1	E33	W	0h	Event Missed Clear #33 Reset Source: edma_rst_mod_g_rst_n
0	E32	W	0h	Event Missed Clear #32 Reset Source: edma_rst_mod_g_rst_n

4.28.12 TPCC_QEMR Registers

4.28.12.1 TPCC_QEMR Register (Offset = 310h) [reset = 0h]

Short Description: QDMA Event Misse

Long Description: QDMA Event Missed Register: The QDMA Event Missed register is set if 2 QDMA events are detected without the first event being cleared or if a Null TR is serviced.. If any bit in the QEMR register is set (and all errors (including EMR/CCERR) were previously clear) then an error will be signaled with TPCC error interrupt.

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Table 4-4493. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0310h

Figure 4-2126. QEMR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES31															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES31								E7	E6	E5	E4	E3	E2	E1	E0
R								R	R	R	R	R	R	R	R
0h								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4494. QEMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES31	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
7	E7	R	0h	Event Missed #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	R	0h	Event Missed #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	R	0h	Event Missed #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	R	0h	Event Missed #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	R	0h	Event Missed #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	R	0h	Event Missed #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	R	0h	Event Missed #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	R	0h	Event Missed #0 Reset Source: edma_rst_mod_g_rst_n

4.28.13 TPCC_QEMCR Registers

4.28.13.1 TPCC_QEMCR Register (Offset = 314h) [reset = 0h]

Short Description: QDMA Event Misse

Long Description: QDMA Event Missed Clear Register: CPU write of '1' to the QEMCR.En bit causes the QEMR.En bit to be cleared. CPU write of '0' has no effect.. All error bits must be cleared before additional error interrupts will be asserted by CC.

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Table 4-4495. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0314h

Figure 4-2127. QEMCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES32															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES32								E7	E6	E5	E4	E3	E2	E1	E0
R								W	W	W	W	W	W	W	W
0h								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4496. QEMCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES32	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
7	E7	W	0h	Event Missed Clear #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	W	0h	Event Missed Clear #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	W	0h	Event Missed Clear #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	W	0h	Event Missed Clear #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	W	0h	Event Missed Clear #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	W	0h	Event Missed Clear #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	W	0h	Event Missed Clear #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	W	0h	Event Missed Clear #0 Reset Source: edma_rst_mod_g_rst_n

4.28.14 TPCC_CCERR Registers

4.28.14.1 TPCC_CCERR Register (Offset = 318h) [reset = 0h]

Short Description: CC Error Registe

Long Description: CC Error Register

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Table 4-4497. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0318h

Figure 4-2128. CCERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES33															TCERR
R															R
0h															0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES34								QTHRXCD7	QTHRXCD6	QTHRXCD5	QTHRXCD4	QTHRXCD3	QTHRXCD2	QTHRXCD1	QTHRXCD0
R								R	R	R	R	R	R	R	R
0h								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4498. CCERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RES33	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
16	TCERR	R	0h	Transfer Completion Code Error: TCCERR = 0 : Total number of allowed TCCs outstanding has not been reached. TCCERR = 1 : Total number of allowed TCCs has been reached. TCCERR can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set [and all errors were previously clear] then an error will be signaled with TPCC error interrupt. Reset Source: edma_rst_mod_g_rst_n
15:8	RES34	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
7	QTHRXCD7	R	0h	Queue Threshold Error for Q7: QTHRXCD7 = 0 : Watermark/ threshold has not been exceeded. QTHRXCD7 = 1 : Watermark/ threshold has been exceeded. CCERR.QTHRXCD7 can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set [and all errors [including EMR/QEMR] were previously clear] then an error will be signaled with the TPCC error interrupt. Reset Source: edma_rst_mod_g_rst_n
6	QTHRXCD6	R	0h	Queue Threshold Error for Q6: QTHRXCD6 = 0 : Watermark/ threshold has not been exceeded. QTHRXCD6 = 1 : Watermark/ threshold has been exceeded. CCERR.QTHRXCD6 can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set [and all errors [including EMR/QEMR] were previously clear] then an error will be signaled with the TPCC error interrupt. Reset Source: edma_rst_mod_g_rst_n
5	QTHRXCD5	R	0h	Queue Threshold Error for Q5: QTHRXCD5 = 0 : Watermark/ threshold has not been exceeded. QTHRXCD5 = 1 : Watermark/ threshold has been exceeded. CCERR.QTHRXCD5 can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set [and all errors [including EMR/QEMR] were previously clear] then an error will be signaled with the TPCC error interrupt. Reset Source: edma_rst_mod_g_rst_n

Table 4-4498. CCERR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	QTHRXCD4	R	0h	Queue Threshold Error for Q4: QTHRXCD4 = 0 : Watermark/ threshold has not been exceeded. QTHRXCD4 = 1 : Watermark/ threshold has been exceeded. CCERR.QTHRXCD4 can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set [and all errors [including EMR/QEMR] were previously clear] then an error will be signaled with the TPCC error interrupt. Reset Source: edma_rst_mod_g_rst_n
3	QTHRXCD3	R	0h	Queue Threshold Error for Q3: QTHRXCD3 = 0 : Watermark/ threshold has not been exceeded. QTHRXCD3 = 1 : Watermark/ threshold has been exceeded. CCERR.QTHRXCD3 can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set [and all errors [including EMR/QEMR] were previously clear] then an error will be signaled with the TPCC error interrupt. Reset Source: edma_rst_mod_g_rst_n
2	QTHRXCD2	R	0h	Queue Threshold Error for Q2: QTHRXCD2 = 0 : Watermark/ threshold has not been exceeded. QTHRXCD2 = 1 : Watermark/ threshold has been exceeded. CCERR.QTHRXCD2 can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set [and all errors [including EMR/QEMR] were previously clear] then an error will be signaled with the TPCC error interrupt. Reset Source: edma_rst_mod_g_rst_n
1	QTHRXCD1	R	0h	Queue Threshold Error for Q1: QTHRXCD1 = 0 : Watermark/ threshold has not been exceeded. QTHRXCD1 = 1 : Watermark/ threshold has been exceeded. CCERR.QTHRXCD1 can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set [and all errors [including EMR/QEMR] were previously clear] then an error will be signaled with the TPCC error interrupt. Reset Source: edma_rst_mod_g_rst_n
0	QTHRXCD0	R	0h	Queue Threshold Error for Q0: QTHRXCD0 = 0 : Watermark/ threshold has not been exceeded. QTHRXCD0 = 1 : Watermark/ threshold has been exceeded. CCERR.QTHRXCD0 can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set [and all errors [including EMR/QEMR] were previously clear] then an error will be signaled with the TPCC error interrupt. Reset Source: edma_rst_mod_g_rst_n

4.28.15 TPCC_CCERRCLR Registers

4.28.15.1 TPCC_CCERRCLR Register (Offset = 31Ch) [reset = 0h]

Short Description: CC Error Clear R

Long Description: CC Error Clear Register

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Table 4-4499. Instance Table

Instance Name	Physical Address
EDMA0	52A0 031Ch

Figure 4-2129. CCERRCLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES35															TCERR
R															W
0h															0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES36								QTHRXCD7	QTHRXCD6	QTHRXCD5	QTHRXCD4	QTHRXCD3	QTHRXCD2	QTHRXCD1	QTHRXCD0
R								W	W	W	W	W	W	W	W
0h								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4500. CCERRCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RES35	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
16	TCERR	W	0h	Clear Error for CCERR.TCERR: Write of '1' clears the value of CCERR bit N. Writes of '0' have no affect. Reset Source: edma_rst_mod_g_rst_n
15:8	RES36	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
7	QTHRXCD7	W	0h	Clear error for CCERR.QTHRXCD7: Write of '1' clears the values of QSTAT7.WM QSTAT7.THRXCD CCERR.QTHRXCD7 Writes of '0' have no affect. Reset Source: edma_rst_mod_g_rst_n
6	QTHRXCD6	W	0h	Clear error for CCERR.QTHRXCD6: Write of '1' clears the values of QSTAT6.WM QSTAT6.THRXCD CCERR.QTHRXCD6 Writes of '0' have no affect. Reset Source: edma_rst_mod_g_rst_n
5	QTHRXCD5	W	0h	Clear error for CCERR.QTHRXCD5: Write of '1' clears the values of QSTAT5.WM QSTAT5.THRXCD CCERR.QTHRXCD5 Writes of '0' have no affect. Reset Source: edma_rst_mod_g_rst_n
4	QTHRXCD4	W	0h	Clear error for CCERR.QTHRXCD4: Write of '1' clears the values of QSTAT4.WM QSTAT4.THRXCD CCERR.QTHRXCD4 Writes of '0' have no affect. Reset Source: edma_rst_mod_g_rst_n
3	QTHRXCD3	W	0h	Clear error for CCERR.QTHRXCD3: Write of '1' clears the values of QSTAT3.WM QSTAT3.THRXCD CCERR.QTHRXCD3 Writes of '0' have no affect. Reset Source: edma_rst_mod_g_rst_n
2	QTHRXCD2	W	0h	Clear error for CCERR.QTHRXCD2: Write of '1' clears the values of QSTAT2.WM QSTAT2.THRXCD CCERR.QTHRXCD2 Writes of '0' have no affect. Reset Source: edma_rst_mod_g_rst_n
1	QTHRXCD1	W	0h	Clear error for CCERR.QTHRXCD1: Write of '1' clears the values of QSTAT1.WM QSTAT1.THRXCD CCERR.QTHRXCD1 Writes of '0' have no affect. Reset Source: edma_rst_mod_g_rst_n

Table 4-4500. CCERRCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	QTHRXCD0	W	0h	Clear error for CCERR.QTHRXCD0: Write of '1' clears the values of QSTAT0.WM QSTAT0.THRXCD CCERR.QTHRXCD0 Writes of '0' have no affect. Reset Source: edma_rst_mod_g_rst_n

4.28.16 TPCC_EEVAL Registers

4.28.16.1 TPCC_EEVAL Register (Offset = 320h) [reset = 0h]

Short Description: Error Eval Regis

Long Description: Error Eval Register

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Table 4-4501. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0320h

Figure 4-2130. EEVAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES37															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES37														SET	EVAL
R														W	W
0h														0h	0h

Access Types Legend

Table 4-4502. EEVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RES37	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
1	SET	W	0h	Error Interrupt Set: CPU write of '1' to the SET bit causes the TPCC error interrupt to be pulsed regardless of state of EMR/EMRH QEMR or CCERR. CPU write of '0' has no effect. Reset Source: edma_rst_mod_g_rst_n
0	EVAL	W	0h	Error Interrupt Evaluate: CPU write of '1' to the EVAL bit causes the TPCC error interrupt to be pulsed if any errors have not been cleared in the EMR/EMRH QEMR or CCERR registers. CPU write of '0' has no effect. Reset Source: edma_rst_mod_g_rst_n

4.28.17 TPCC_DRAEM Registers

4.28.17.1 TPCC_DRAEM Register (Offset = 340h) [reset = 0h]

Short Description: DMA Region Acces

Long Description: DMA Region Access enable for bit N in Region M: En = 0 : Accesses via Region M address space to Bit N in any DMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any DMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region M interrupt.

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Table 4-4503. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0340h

Figure 4-2131. DRAEM Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4504. DRAEM Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	R/W	0h	DMA Region Access enable for Region M bit #31 Reset Source: edma_rst_mod_g_rst_n
30	E30	R/W	0h	DMA Region Access enable for Region M bit #30 Reset Source: edma_rst_mod_g_rst_n
29	E29	R/W	0h	DMA Region Access enable for Region M bit #29 Reset Source: edma_rst_mod_g_rst_n
28	E28	R/W	0h	DMA Region Access enable for Region M bit #28 Reset Source: edma_rst_mod_g_rst_n
27	E27	R/W	0h	DMA Region Access enable for Region M bit #27 Reset Source: edma_rst_mod_g_rst_n
26	E26	R/W	0h	DMA Region Access enable for Region M bit #26 Reset Source: edma_rst_mod_g_rst_n
25	E25	R/W	0h	DMA Region Access enable for Region M bit #25 Reset Source: edma_rst_mod_g_rst_n
24	E24	R/W	0h	DMA Region Access enable for Region M bit #24 Reset Source: edma_rst_mod_g_rst_n
23	E23	R/W	0h	DMA Region Access enable for Region M bit #23 Reset Source: edma_rst_mod_g_rst_n
22	E22	R/W	0h	DMA Region Access enable for Region M bit #22 Reset Source: edma_rst_mod_g_rst_n
21	E21	R/W	0h	DMA Region Access enable for Region M bit #21 Reset Source: edma_rst_mod_g_rst_n
20	E20	R/W	0h	DMA Region Access enable for Region M bit #20 Reset Source: edma_rst_mod_g_rst_n

Table 4-4504. DRAEM Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	E19	R/W	0h	DMA Region Access enable for Region M bit #19 Reset Source: edma_rst_mod_g_rst_n
18	E18	R/W	0h	DMA Region Access enable for Region M bit #18 Reset Source: edma_rst_mod_g_rst_n
17	E17	R/W	0h	DMA Region Access enable for Region M bit #17 Reset Source: edma_rst_mod_g_rst_n
16	E16	R/W	0h	DMA Region Access enable for Region M bit #16 Reset Source: edma_rst_mod_g_rst_n
15	E15	R/W	0h	DMA Region Access enable for Region M bit #15 Reset Source: edma_rst_mod_g_rst_n
14	E14	R/W	0h	DMA Region Access enable for Region M bit #14 Reset Source: edma_rst_mod_g_rst_n
13	E13	R/W	0h	DMA Region Access enable for Region M bit #13 Reset Source: edma_rst_mod_g_rst_n
12	E12	R/W	0h	DMA Region Access enable for Region M bit #12 Reset Source: edma_rst_mod_g_rst_n
11	E11	R/W	0h	DMA Region Access enable for Region M bit #11 Reset Source: edma_rst_mod_g_rst_n
10	E10	R/W	0h	DMA Region Access enable for Region M bit #10 Reset Source: edma_rst_mod_g_rst_n
9	E9	R/W	0h	DMA Region Access enable for Region M bit #9 Reset Source: edma_rst_mod_g_rst_n
8	E8	R/W	0h	DMA Region Access enable for Region M bit #8 Reset Source: edma_rst_mod_g_rst_n
7	E7	R/W	0h	DMA Region Access enable for Region M bit #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	R/W	0h	DMA Region Access enable for Region M bit #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	R/W	0h	DMA Region Access enable for Region M bit #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	R/W	0h	DMA Region Access enable for Region M bit #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	R/W	0h	DMA Region Access enable for Region M bit #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	R/W	0h	DMA Region Access enable for Region M bit #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	R/W	0h	DMA Region Access enable for Region M bit #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	R/W	0h	DMA Region Access enable for Region M bit #0 Reset Source: edma_rst_mod_g_rst_n

4.28.18 TPCC_DRAEHM Registers

4.28.18.1 TPCC_DRAEHM Register (Offset = 344h) [reset = 0h]

Short Description: DMA Region Acces

Long Description: DMA Region Access enable for bit N in Region M: En = 0 : Accesses via Region M address space to Bit N in any DMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any DMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region M interrupt. En = 0 : Accesses via Region M address space to Bit N in any DMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any DMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region M interrupt.

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Table 4-4505. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0344h

Figure 4-2132. DRAEHM Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4506. DRAEHM Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	R/W	0h	DMA Region Access enable for Region M bit #63 Reset Source: edma_rst_mod_g_rst_n
30	E62	R/W	0h	DMA Region Access enable for Region M bit #62 Reset Source: edma_rst_mod_g_rst_n
29	E61	R/W	0h	DMA Region Access enable for Region M bit #61 Reset Source: edma_rst_mod_g_rst_n
28	E60	R/W	0h	DMA Region Access enable for Region M bit #60 Reset Source: edma_rst_mod_g_rst_n
27	E59	R/W	0h	DMA Region Access enable for Region M bit #59 Reset Source: edma_rst_mod_g_rst_n
26	E58	R/W	0h	DMA Region Access enable for Region M bit #58 Reset Source: edma_rst_mod_g_rst_n
25	E57	R/W	0h	DMA Region Access enable for Region M bit #57 Reset Source: edma_rst_mod_g_rst_n
24	E56	R/W	0h	DMA Region Access enable for Region M bit #56 Reset Source: edma_rst_mod_g_rst_n
23	E55	R/W	0h	DMA Region Access enable for Region M bit #55 Reset Source: edma_rst_mod_g_rst_n

Table 4-4506. DRAEHM Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	E54	R/W	0h	DMA Region Access enable for Region M bit #54 Reset Source: edma_rst_mod_g_rst_n
21	E53	R/W	0h	DMA Region Access enable for Region M bit #53 Reset Source: edma_rst_mod_g_rst_n
20	E52	R/W	0h	DMA Region Access enable for Region M bit #52 Reset Source: edma_rst_mod_g_rst_n
19	E51	R/W	0h	DMA Region Access enable for Region M bit #51 Reset Source: edma_rst_mod_g_rst_n
18	E50	R/W	0h	DMA Region Access enable for Region M bit #50 Reset Source: edma_rst_mod_g_rst_n
17	E49	R/W	0h	DMA Region Access enable for Region M bit #49 Reset Source: edma_rst_mod_g_rst_n
16	E48	R/W	0h	DMA Region Access enable for Region M bit #48 Reset Source: edma_rst_mod_g_rst_n
15	E47	R/W	0h	DMA Region Access enable for Region M bit #47 Reset Source: edma_rst_mod_g_rst_n
14	E46	R/W	0h	DMA Region Access enable for Region M bit #46 Reset Source: edma_rst_mod_g_rst_n
13	E45	R/W	0h	DMA Region Access enable for Region M bit #45 Reset Source: edma_rst_mod_g_rst_n
12	E44	R/W	0h	DMA Region Access enable for Region M bit #44 Reset Source: edma_rst_mod_g_rst_n
11	E43	R/W	0h	DMA Region Access enable for Region M bit #43 Reset Source: edma_rst_mod_g_rst_n
10	E42	R/W	0h	DMA Region Access enable for Region M bit #42 Reset Source: edma_rst_mod_g_rst_n
9	E41	R/W	0h	DMA Region Access enable for Region M bit #41 Reset Source: edma_rst_mod_g_rst_n
8	E40	R/W	0h	DMA Region Access enable for Region M bit #40 Reset Source: edma_rst_mod_g_rst_n
7	E39	R/W	0h	DMA Region Access enable for Region M bit #39 Reset Source: edma_rst_mod_g_rst_n
6	E38	R/W	0h	DMA Region Access enable for Region M bit #38 Reset Source: edma_rst_mod_g_rst_n
5	E37	R/W	0h	DMA Region Access enable for Region M bit #37 Reset Source: edma_rst_mod_g_rst_n
4	E36	R/W	0h	DMA Region Access enable for Region M bit #36 Reset Source: edma_rst_mod_g_rst_n
3	E35	R/W	0h	DMA Region Access enable for Region M bit #35 Reset Source: edma_rst_mod_g_rst_n
2	E34	R/W	0h	DMA Region Access enable for Region M bit #34 Reset Source: edma_rst_mod_g_rst_n
1	E33	R/W	0h	DMA Region Access enable for Region M bit #33 Reset Source: edma_rst_mod_g_rst_n
0	E32	R/W	0h	DMA Region Access enable for Region M bit #32 Reset Source: edma_rst_mod_g_rst_n

4.28.19 TPCC_QRAEN Registers

4.28.19.1 TPCC_QRAEN Register (Offset = 380h) [reset = 0h]

Short Description: QDMA Region Acce

Long Description: QDMA Region Access enable for bit N in Region M: En = 0 : Accesses via Region M address space to Bit N in any QDMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any QDMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region n interrupt.

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Table 4-4507. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0380h

Figure 4-2133. QRAEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES38															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES38								E7	E6	E5	E4	E3	E2	E1	E0
R								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4508. QRAEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES38	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
7	E7	R/W	0h	QDMA Region Access enable for Region M bit #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	R/W	0h	QDMA Region Access enable for Region M bit #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	R/W	0h	QDMA Region Access enable for Region M bit #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	R/W	0h	QDMA Region Access enable for Region M bit #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	R/W	0h	QDMA Region Access enable for Region M bit #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	R/W	0h	QDMA Region Access enable for Region M bit #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	R/W	0h	QDMA Region Access enable for Region M bit #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	R/W	0h	QDMA Region Access enable for Region M bit #0 Reset Source: edma_rst_mod_g_rst_n

4.28.20 TPCC_QNE0 Registers

4.28.20.1 TPCC_QNE0 Register (Offset = 400h) [reset = 0h]

Short Description: Event Queue Entr

Long Description: Event Queue Entry Diagram for Queue n - Entry 0

Return to Summary Table

Table 4-4509. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0400h

Figure 4-2134. QNE0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES39															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES39								ETYPE		ENUM					
R								R		R					
0h								0h		0h					

Access Types Legend

Table 4-4510. QNE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES39	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
7:6	ETYPE	R	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue. Reset Source: edma_rst_mod_g_rst_n
5:0	ENUM	R	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7]. Reset Source: edma_rst_mod_g_rst_n

4.28.21 TPCC_QNE1 Registers

4.28.21.1 TPCC_QNE1 Register (Offset = 404h) [reset = 0h]

Short Description: Event Queue Entr

Long Description: Event Queue Entry Diagram for Queue n - Entry 1

Return to Summary Table

Table 4-4511. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0404h

Figure 4-2135. QNE1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES40															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES40								ETYPE		ENUM					
R								R		R					
0h								0h		0h					

Access Types Legend

Table 4-4512. QNE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES40	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
7:6	ETYPE	R	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue. Reset Source: edma_rst_mod_g_rst_n
5:0	ENUM	R	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7]. Reset Source: edma_rst_mod_g_rst_n

4.28.22 TPCC_QNE2 Registers

4.28.22.1 TPCC_QNE2 Register (Offset = 408h) [reset = 0h]

Short Description: Event Queue Entr

Long Description: Event Queue Entry Diagram for Queue n - Entry 2

Return to Summary Table

Table 4-4513. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0408h

Figure 4-2136. QNE2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES41															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES41								ETYPE		ENUM					
R								R		R					
0h								0h		0h					

Access Types Legend

Table 4-4514. QNE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES41	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
7:6	ETYPE	R	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue. Reset Source: edma_rst_mod_g_rst_n
5:0	ENUM	R	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7]. Reset Source: edma_rst_mod_g_rst_n

4.28.23 TPCC_QNE3 Registers

4.28.23.1 TPCC_QNE3 Register (Offset = 40Ch) [reset = 0h]

Short Description: Event Queue Entr

Long Description: Event Queue Entry Diagram for Queue n - Entry 3

Return to Summary Table

Table 4-4515. Instance Table

Instance Name	Physical Address
EDMA0	52A0 040Ch

Figure 4-2137. QNE3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES42															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES42								ETYPE		ENUM					
R								R		R					
0h								0h		0h					

Access Types Legend

Table 4-4516. QNE3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES42	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
7:6	ETYPE	R	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue. Reset Source: edma_rst_mod_g_rst_n
5:0	ENUM	R	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7]. Reset Source: edma_rst_mod_g_rst_n

4.28.24 TPCC_QNE4 Registers

4.28.24.1 TPCC_QNE4 Register (Offset = 410h) [reset = 0h]

Short Description: Event Queue Entr

Long Description: Event Queue Entry Diagram for Queue n - Entry 4

Return to Summary Table

Table 4-4517. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0410h

Figure 4-2138. QNE4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES43															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES43								ETYPE		ENUM					
R								R		R					
0h								0h		0h					

Access Types Legend

Table 4-4518. QNE4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES43	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
7:6	ETYPE	R	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue. Reset Source: edma_rst_mod_g_rst_n
5:0	ENUM	R	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7]. Reset Source: edma_rst_mod_g_rst_n

4.28.25 TPCC_QNE5 Registers

4.28.25.1 TPCC_QNE5 Register (Offset = 414h) [reset = 0h]

Short Description: Event Queue Entr

Long Description: Event Queue Entry Diagram for Queue n - Entry 5

Return to Summary Table

Table 4-4519. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0414h

Figure 4-2139. QNE5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES44															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES44								ETYPE		ENUM					
R								R		R					
0h								0h		0h					

Access Types Legend

Table 4-4520. QNE5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES44	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
7:6	ETYPE	R	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue. Reset Source: edma_rst_mod_g_rst_n
5:0	ENUM	R	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7]. Reset Source: edma_rst_mod_g_rst_n

4.28.26 TPCC_QNE6 Registers

4.28.26.1 TPCC_QNE6 Register (Offset = 418h) [reset = 0h]

Short Description: Event Queue Entr

Long Description: Event Queue Entry Diagram for Queue n - Entry 6

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Table 4-4521. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0418h

Figure 4-2140. QNE6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES45															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES45								ETYPE		ENUM					
R								R		R					
0h								0h		0h					

Access Types Legend

Table 4-4522. QNE6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES45	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
7:6	ETYPE	R	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue. Reset Source: edma_rst_mod_g_rst_n
5:0	ENUM	R	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7]. Reset Source: edma_rst_mod_g_rst_n

4.28.27 TPCC_QNE7 Registers

4.28.27.1 TPCC_QNE7 Register (Offset = 41Ch) [reset = 0h]

Short Description: Event Queue Entr

Long Description: Event Queue Entry Diagram for Queue n - Entry 7

Return to Summary Table

Table 4-4523. Instance Table

Instance Name	Physical Address
EDMA0	52A0 041Ch

Figure 4-2141. QNE7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES46															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES46								ETYPE		ENUM					
R								R		R					
0h								0h		0h					

Access Types Legend

Table 4-4524. QNE7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES46	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
7:6	ETYPE	R	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue. Reset Source: edma_rst_mod_g_rst_n
5:0	ENUM	R	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7]. Reset Source: edma_rst_mod_g_rst_n

4.28.28 TPCC_QNE8 Registers

4.28.28.1 TPCC_QNE8 Register (Offset = 420h) [reset = 0h]

Short Description: Event Queue Entr

Long Description: Event Queue Entry Diagram for Queue n - Entry 8

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Table 4-4525. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0420h

Figure 4-2142. QNE8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES47															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES47								ETYPE		ENUM					
R								R		R					
0h								0h		0h					

Access Types Legend

Table 4-4526. QNE8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES47	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
7:6	ETYPE	R	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue. Reset Source: edma_rst_mod_g_rst_n
5:0	ENUM	R	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7]. Reset Source: edma_rst_mod_g_rst_n

4.28.29 TPCC_QNE9 Registers

4.28.29.1 TPCC_QNE9 Register (Offset = 424h) [reset = 0h]

Short Description: Event Queue Entr

Long Description: Event Queue Entry Diagram for Queue n - Entry 9

Return to Summary Table

Table 4-4527. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0424h

Figure 4-2143. QNE9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES48															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES48								ETYPE		ENUM					
R								R		R					
0h								0h		0h					

Access Types Legend

Table 4-4528. QNE9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES48	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
7:6	ETYPE	R	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue. Reset Source: edma_rst_mod_g_rst_n
5:0	ENUM	R	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7]. Reset Source: edma_rst_mod_g_rst_n

4.28.30 TPCC_QNE10 Registers

4.28.30.1 TPCC_QNE10 Register (Offset = 428h) [reset = 0h]

Short Description: Event Queue Entr

Long Description: Event Queue Entry Diagram for Queue n - Entry 0

Return to Summary Table

Table 4-4529. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0428h

Figure 4-2144. QNE10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES49															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES49								ETYPE		ENUM					
R								R		R					
0h								0h		0h					

Access Types Legend

Table 4-4530. QNE10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES49	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
7:6	ETYPE	R	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue. Reset Source: edma_rst_mod_g_rst_n
5:0	ENUM	R	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7]. Reset Source: edma_rst_mod_g_rst_n

4.28.31 TPCC_QNE11 Registers

4.28.31.1 TPCC_QNE11 Register (Offset = 42Ch) [reset = 0h]

Short Description: Event Queue Entr

Long Description: Event Queue Entry Diagram for Queue n - Entry 11

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Table 4-4531. Instance Table

Instance Name	Physical Address
EDMA0	52A0 042Ch

Figure 4-2145. QNE11 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES50															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES50								ETYPE		ENUM					
R								R		R					
0h								0h		0h					

Access Types Legend

Table 4-4532. QNE11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES50	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
7:6	ETYPE	R	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue. Reset Source: edma_rst_mod_g_rst_n
5:0	ENUM	R	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7]. Reset Source: edma_rst_mod_g_rst_n

4.28.32 TPCC_QNE12 Registers

4.28.32.1 TPCC_QNE12 Register (Offset = 430h) [reset = 0h]

Short Description: Event Queue Entr

Long Description: Event Queue Entry Diagram for Queue n - Entry 12

Return to Summary Table

Table 4-4533. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0430h

Figure 4-2146. QNE12 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES51															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES51								ETYPE		ENUM					
R								R		R					
0h								0h		0h					

Access Types Legend

Table 4-4534. QNE12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES51	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
7:6	ETYPE	R	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue. Reset Source: edma_rst_mod_g_rst_n
5:0	ENUM	R	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7]. Reset Source: edma_rst_mod_g_rst_n

4.28.33 TPCC_QNE13 Registers

4.28.33.1 TPCC_QNE13 Register (Offset = 434h) [reset = 0h]

Short Description: Event Queue Entr

Long Description: Event Queue Entry Diagram for Queue n - Entry 13

Return to Summary Table

Table 4-4535. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0434h

Figure 4-2147. QNE13 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES52															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES52								ETYPE		ENUM					
R								R		R					
0h								0h		0h					

Access Types Legend

Table 4-4536. QNE13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES52	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
7:6	ETYPE	R	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue. Reset Source: edma_rst_mod_g_rst_n
5:0	ENUM	R	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7]. Reset Source: edma_rst_mod_g_rst_n

4.28.34 TPCC_QNE14 Registers

4.28.34.1 TPCC_QNE14 Register (Offset = 438h) [reset = 0h]

Short Description: Event Queue Entr

Long Description: Event Queue Entry Diagram for Queue n - Entry 14

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Table 4-4537. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0438h

Figure 4-2148. QNE14 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES53															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES53								ETYPE		ENUM					
R								R		R					
0h								0h		0h					

Access Types Legend

Table 4-4538. QNE14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES53	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
7:6	ETYPE	R	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue. Reset Source: edma_rst_mod_g_rst_n
5:0	ENUM	R	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7]. Reset Source: edma_rst_mod_g_rst_n

4.28.35 TPCC_QNE15 Registers

4.28.35.1 TPCC_QNE15 Register (Offset = 43Ch) [reset = 0h]

Short Description: Event Queue Entr

Long Description: Event Queue Entry Diagram for Queue n - Entry 15

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Table 4-4539. Instance Table

Instance Name	Physical Address
EDMA0	52A0 043Ch

Figure 4-2149. QNE15 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES54															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES54								ETYPE		ENUM					
R								R		R					
0h								0h		0h					

Access Types Legend

Table 4-4540. QNE15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES54	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
7:6	ETYPE	R	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue. Reset Source: edma_rst_mod_g_rst_n
5:0	ENUM	R	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7]. Reset Source: edma_rst_mod_g_rst_n

4.28.36 TPCC_QSTATN Registers

4.28.36.1 TPCC_QSTATN Register (Offset = 600h) [reset = 0h]

Short Description: QSTATn Register

Long Description: QSTATn Register Set

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Table 4-4541. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0600h

Figure 4-2150. QSTATN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES55							THRXCD	RES56			WM				
R							R	R			R				
0h							0h	0h			0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES57			NUMVAL					RES58			STRTPTR				
R			R					R			R				
0h			0h					0h			0h				

Access Types Legend

Table 4-4542. QSTATN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RES55	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
24	THRXCD	R	0h	Threshold Exceeded: THRXCD = 0 : Threshold specified by QWMTHR[A B].Qn has not been exceeded. THRXCD = 1 : Threshold specified by QWMTHR[A B].Qn has been exceeded. QSTATn.THRXCD is cleared via CCERR.WMCLRn bit. Reset Source: edma_rst_mod_g_rst_n
23:21	RES56	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
20:16	WM	R	0h	Watermark for Maximum Queue Usage: Watermark tracks the most entries that have been in QueueN since reset or since the last time that the watermark [WM] was cleared. QSTATn.WM is cleared via CCERR.WMCLRn bit. Legal values = 0x0 [empty] to 0x10 [full] Reset Source: edma_rst_mod_g_rst_n
15:13	RES57	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
12:8	NUMVAL	R	0h	Number of Valid Entries in QueueN: Represents the total number of entries residing in the Queue Manager FIFO at a given instant. Always enabled. Legal values = 0x0 [empty] to 0x10 [full] Reset Source: edma_rst_mod_g_rst_n
7:4	RES58	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
3:0	STRTPTR	R	0h	Start Pointer: Represents the offset to the head entry of QueueN in units of entries. Always enabled. Legal values = 0x0 [0th entry] to 0xF [15th entry] Reset Source: edma_rst_mod_g_rst_n

4.28.37 TPCC_QWMTHRA Registers

4.28.37.1 TPCC_QWMTHRA Register (Offset = 620h) [reset = 1010h]

Short Description: Queue Threshold

Long Description: Queue Threshold A for Q[3:0]: CCERR.QTHRXCDn and QSTATn.THRXCD error bit is set when the number of Events in QueueN at an instant in time (visible via QSTATn.NUMVAL) equals or exceeds the value specified by QWMTHRA.Qn. Legal values = 0x0 (ever used?) to 0x10 (ever full?) A value of 0x11 disables threshold errors.

Return to Summary Table

Table 4-4543. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0620h

Figure 4-2151. QWMTHRA Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES59															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES59			Q1					RES60			Q0				
R			R/W					R			R/W				
0h			10h					0h			10h				

Access Types Legend

Table 4-4544. QWMTHRA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RES59	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
12:8	Q1	R/W	10h	Queue Threshold for Q1 value Reset Source: edma_rst_mod_g_rst_n
7:5	RES60	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
4:0	Q0	R/W	10h	Queue Threshold for Q0 value Reset Source: edma_rst_mod_g_rst_n

4.28.38 TPCC_CCSTAT Registers

4.28.38.1 TPCC_CCSTAT Register (Offset = 640h) [reset = 0h]

Short Description: CC Status Regist

Long Description: CC Status Register

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Table 4-4545. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0640h

Figure 4-2152. CCSTAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES61								QUEACTV7	QUEACTV6	QUEACTV5	QUEACTV4	QUEACTV3	QUEACTV2	QUEACTV1	QUEACTV0
R								R	R	R	R	R	R	R	R
0h								0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES62		COMPACTV						RES63			ACTV	RES64	TRACTV	QEVTACTV	EVTACTV
R		R						R			R	R	R	R	R
0h		0h						0h			0h	0h	0h	0h	0h

Access Types Legend

Table 4-4546. CCSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES61	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
23	QUEACTV7	R	0h	Queue 7 Active QUEACTV7 = 0 : No Evts are queued in Q7. QUEACTV7 = 1 : At least one TR is queued in Q7. Reset Source: edma_rst_mod_g_rst_n
22	QUEACTV6	R	0h	Queue 6 Active QUEACTV6 = 0 : No Evts are queued in Q6. QUEACTV6 = 1 : At least one TR is queued in Q6. Reset Source: edma_rst_mod_g_rst_n
21	QUEACTV5	R	0h	Queue 5 Active QUEACTV5 = 0 : No Evts are queued in Q5. QUEACTV5 = 1 : At least one TR is queued in Q5. Reset Source: edma_rst_mod_g_rst_n
20	QUEACTV4	R	0h	Queue 4 Active QUEACTV4 = 0 : No Evts are queued in Q4. QUEACTV4 = 1 : At least one TR is queued in Q4. Reset Source: edma_rst_mod_g_rst_n
19	QUEACTV3	R	0h	Queue 3 Active QUEACTV3 = 0 : No Evts are queued in Q3. QUEACTV3 = 1 : At least one TR is queued in Q3. Reset Source: edma_rst_mod_g_rst_n
18	QUEACTV2	R	0h	Queue 2 Active QUEACTV2 = 0 : No Evts are queued in Q2. QUEACTV2 = 1 : At least one TR is queued in Q2. Reset Source: edma_rst_mod_g_rst_n
17	QUEACTV1	R	0h	Queue 1 Active QUEACTV1 = 0 : No Evts are queued in Q1. QUEACTV1 = 1 : At least one TR is queued in Q1. Reset Source: edma_rst_mod_g_rst_n
16	QUEACTV0	R	0h	Queue 0 Active QUEACTV0 = 0 : No Evts are queued in Q0. QUEACTV0 = 1 : At least one TR is queued in Q0. Reset Source: edma_rst_mod_g_rst_n
15:14	RES62	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n

Table 4-4546. CCSTAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:8	COMPACTV	R	0h	Completion Request Active: Counter that tracks the total number of completion requests submitted to the TC. The counter increments when a TR is submitted with TCINTEN or TCCHEN set to '1'. The counter decrements for every valid completion code received from any of the external TCs. The CC will not service new TRs if COMPACTV count is already at the limit. COMPACTV = 0 : No completion requests outstanding. COMPACTV = 1: Total of '1' completion request outstanding. ... COMPACTV = 63 : Total of 63 completion requests are outstanding. No additional TRs will be submitted until count is less than 63. Reset Source: edma_rst_mod_g_rst_n
7:5	RES63	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
4	ACTV	R	0h	Channel Controller Active: Channel Controller Active is a logical-OR of each of the ACTV signals. The ACTV bit must remain high through the life of a TR. ACTV = 0 : Channel is idle. ACTV = 1 : Channel is busy. Reset Source: edma_rst_mod_g_rst_n
3	RES64	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
2	TRACTV	R	0h	Transfer Request Active: TRACTV = 0 : Transfer Request processing/submission logic is inactive. TRACTV = 1 : Transfer Request processing/submission logic is active. Reset Source: edma_rst_mod_g_rst_n
1	QEVTACTV	R	0h	QDMA Event Active: QEVTACTV = 0 : No enabled QDMA Events are active within the CC. QEVTACTV = 1 : At least one enabled DMA Event [ER & EER ESR CER] is active within the CC. Reset Source: edma_rst_mod_g_rst_n
0	EVTACTV	R	0h	DMA Event Active: EVTACTV = 0 : No enabled DMA Events are active within the CC. EVTACTV = 1 : At least one enabled DMA Event [ER & EER ESR CER] is active within the CC. Reset Source: edma_rst_mod_g_rst_n

4.28.39 TPCC_AETCTL Registers

4.28.39.1 TPCC_AETCTL Register (Offset = 700h) [reset = 0h]

Short Description: Advanced Event T

Long Description: Advanced Event Trigger Control

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Table 4-4547. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0700h

Figure 4-2153. AETCTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EN	RES65														
R/W	R														
0h	0h														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES65		ENDINT						RES66	TYPE	STRTEVT					
R		R/W						R	R/W	R/W					
0h		0h						0h	0h	0h					

Access Types Legend

Table 4-4548. AETCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EN	R/W	0h	AET Enable: EN = 0 : AET event generation is disabled. EN = 1 : AET event generation is enabled. Reset Source: edma_rst_mod_g_rst_n
30:14	RES65	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
13:8	ENDINT	R/W	0h	AET End Interrupt: Dictates the completion interrupt number that will force the tpcc_aet signal to be deasserted [low] Reset Source: edma_rst_mod_g_rst_n
7	RES66	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
6	TYPE	R/W	0h	AET Event Type: TYPE = 0 : Event specified by STARTEVT applies to DMA Events [set by ER ESR or CER] TYPE = 1 : Event specified by STARTEVT applies to QDMA Events Reset Source: edma_rst_mod_g_rst_n
5:0	STRTEVT	R/W	0h	AET Start Event: Dictates the Event Number that will force the tpcc_aet signal to be asserted [high] Reset Source: edma_rst_mod_g_rst_n

4.28.40 TPCC_AETSTAT Registers

4.28.40.1 TPCC_AETSTAT Register (Offset = 704h) [reset = 0h]

Short Description: Advanced Event T

Long Description: Advanced Event Trigger Stat

Return to Summary Table

Table 4-4549. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0704h

Figure 4-2154. AETSTAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES67															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES67															STAT
R															R
0h															0h

Access Types Legend

Table 4-4550. AETSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES67	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
0	STAT	R	0h	AET Status: AETSTAT = 0 : tpcc_aet is currently low. AETSTAT = 1 : tpcc_aet is currently high. Reset Source: edma_rst_mod_g_rst_n

4.28.41 TPCC_AETCMD Registers

4.28.41.1 TPCC_AETCMD Register (Offset = 708h) [reset = 0h]

Short Description: AET Command

Long Description: AET Command

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Table 4-4551. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0708h

Figure 4-2155. AETCMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES68															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES68															CLR
R															W
0h															0h

Access Types Legend

Table 4-4552. AETCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES68	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
0	CLR	W	0h	AET Clear command: CPU write of '1' to the CLR bit causes the tpcc_aet output signal and AETSTAT.STAT register to be cleared. CPU write of '0' has no effect.. Reset Source: edma_rst_mod_g_rst_n

4.28.42 TPCC_ER Registers

4.28.42.1 TPCC_ER Register (Offset = 1000h) [reset = 0h]

Short Description: Event Register:

Long Description: Event Register: If ER.En bit is set and the EER.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ER.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EER.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ER.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EER register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECR pseudo-register.

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Table 4-4553. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1000h

Figure 4-2156. ER Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4554. ER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	R	0h	Event #31 Reset Source: edma_rst_mod_g_rst_n
30	E30	R	0h	Event #30 Reset Source: edma_rst_mod_g_rst_n
29	E29	R	0h	Event #29 Reset Source: edma_rst_mod_g_rst_n
28	E28	R	0h	Event #28 Reset Source: edma_rst_mod_g_rst_n
27	E27	R	0h	Event #27 Reset Source: edma_rst_mod_g_rst_n
26	E26	R	0h	Event #26 Reset Source: edma_rst_mod_g_rst_n
25	E25	R	0h	Event #25 Reset Source: edma_rst_mod_g_rst_n
24	E24	R	0h	Event #24 Reset Source: edma_rst_mod_g_rst_n
23	E23	R	0h	Event #23 Reset Source: edma_rst_mod_g_rst_n
22	E22	R	0h	Event #22 Reset Source: edma_rst_mod_g_rst_n
21	E21	R	0h	Event #21 Reset Source: edma_rst_mod_g_rst_n
20	E20	R	0h	Event #20 Reset Source: edma_rst_mod_g_rst_n
19	E19	R	0h	Event #19 Reset Source: edma_rst_mod_g_rst_n
18	E18	R	0h	Event #18 Reset Source: edma_rst_mod_g_rst_n
17	E17	R	0h	Event #17 Reset Source: edma_rst_mod_g_rst_n
16	E16	R	0h	Event #16 Reset Source: edma_rst_mod_g_rst_n
15	E15	R	0h	Event #15 Reset Source: edma_rst_mod_g_rst_n
14	E14	R	0h	Event #14 Reset Source: edma_rst_mod_g_rst_n
13	E13	R	0h	Event #13 Reset Source: edma_rst_mod_g_rst_n

Table 4-4554. ER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	E12	R	0h	Event #12 Reset Source: edma_rst_mod_g_rst_n
11	E11	R	0h	Event #11 Reset Source: edma_rst_mod_g_rst_n
10	E10	R	0h	Event #10 Reset Source: edma_rst_mod_g_rst_n
9	E9	R	0h	Event #9 Reset Source: edma_rst_mod_g_rst_n
8	E8	R	0h	Event #8 Reset Source: edma_rst_mod_g_rst_n
7	E7	R	0h	Event #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	R	0h	Event #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	R	0h	Event #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	R	0h	Event #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	R	0h	Event #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	R	0h	Event #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	R	0h	Event #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	R	0h	Event #0 Reset Source: edma_rst_mod_g_rst_n

4.28.43 TPCC_ERH Registers

4.28.43.1 TPCC_ERH Register (Offset = 1004h) [reset = 0h]

Short Description: Event Register (

Long Description: Event Register (High Part): If ERH.En bit is set and the EERH.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ERH.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EERH.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ERH.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EERH register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECRH pseudo-register.

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Table 4-4555. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1004h

Figure 4-2157. ERH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4556. ERH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	R	0h	Event #63 Reset Source: edma_rst_mod_g_rst_n
30	E62	R	0h	Event #62 Reset Source: edma_rst_mod_g_rst_n
29	E61	R	0h	Event #61 Reset Source: edma_rst_mod_g_rst_n
28	E60	R	0h	Event #60 Reset Source: edma_rst_mod_g_rst_n
27	E59	R	0h	Event #59 Reset Source: edma_rst_mod_g_rst_n
26	E58	R	0h	Event #58 Reset Source: edma_rst_mod_g_rst_n
25	E57	R	0h	Event #57 Reset Source: edma_rst_mod_g_rst_n
24	E56	R	0h	Event #56 Reset Source: edma_rst_mod_g_rst_n
23	E55	R	0h	Event #55 Reset Source: edma_rst_mod_g_rst_n
22	E54	R	0h	Event #54 Reset Source: edma_rst_mod_g_rst_n
21	E53	R	0h	Event #53 Reset Source: edma_rst_mod_g_rst_n
20	E52	R	0h	Event #52 Reset Source: edma_rst_mod_g_rst_n
19	E51	R	0h	Event #51 Reset Source: edma_rst_mod_g_rst_n
18	E50	R	0h	Event #50 Reset Source: edma_rst_mod_g_rst_n
17	E49	R	0h	Event #49 Reset Source: edma_rst_mod_g_rst_n
16	E48	R	0h	Event #48 Reset Source: edma_rst_mod_g_rst_n
15	E47	R	0h	Event #47 Reset Source: edma_rst_mod_g_rst_n
14	E46	R	0h	Event #46 Reset Source: edma_rst_mod_g_rst_n
13	E45	R	0h	Event #45 Reset Source: edma_rst_mod_g_rst_n

Table 4-4556. ERH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	E44	R	0h	Event #44 Reset Source: edma_rst_mod_g_rst_n
11	E43	R	0h	Event #43 Reset Source: edma_rst_mod_g_rst_n
10	E42	R	0h	Event #42 Reset Source: edma_rst_mod_g_rst_n
9	E41	R	0h	Event #41 Reset Source: edma_rst_mod_g_rst_n
8	E40	R	0h	Event #40 Reset Source: edma_rst_mod_g_rst_n
7	E39	R	0h	Event #39 Reset Source: edma_rst_mod_g_rst_n
6	E38	R	0h	Event #38 Reset Source: edma_rst_mod_g_rst_n
5	E37	R	0h	Event #37 Reset Source: edma_rst_mod_g_rst_n
4	E36	R	0h	Event #36 Reset Source: edma_rst_mod_g_rst_n
3	E35	R	0h	Event #35 Reset Source: edma_rst_mod_g_rst_n
2	E34	R	0h	Event #34 Reset Source: edma_rst_mod_g_rst_n
1	E33	R	0h	Event #33 Reset Source: edma_rst_mod_g_rst_n
0	E32	R	0h	Event #32 Reset Source: edma_rst_mod_g_rst_n

4.28.44 TPCC_ECR Registers

4.28.44.1 TPCC_ECR Register (Offset = 1008h) [reset = 0h]

Short Description: Event Clear Regi

Long Description: Event Clear Register: CPU write of '1' to the ECR.En bit causes the ER.En bit to be cleared. CPU write of '0' has no effect.

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Table 4-4557. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1008h

Figure 4-2158. ECR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4558. ECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	W	0h	Event #31 Reset Source: edma_rst_mod_g_rst_n
30	E30	W	0h	Event #30 Reset Source: edma_rst_mod_g_rst_n
29	E29	W	0h	Event #29 Reset Source: edma_rst_mod_g_rst_n
28	E28	W	0h	Event #28 Reset Source: edma_rst_mod_g_rst_n
27	E27	W	0h	Event #27 Reset Source: edma_rst_mod_g_rst_n
26	E26	W	0h	Event #26 Reset Source: edma_rst_mod_g_rst_n
25	E25	W	0h	Event #25 Reset Source: edma_rst_mod_g_rst_n
24	E24	W	0h	Event #24 Reset Source: edma_rst_mod_g_rst_n
23	E23	W	0h	Event #23 Reset Source: edma_rst_mod_g_rst_n
22	E22	W	0h	Event #22 Reset Source: edma_rst_mod_g_rst_n
21	E21	W	0h	Event #21 Reset Source: edma_rst_mod_g_rst_n
20	E20	W	0h	Event #20 Reset Source: edma_rst_mod_g_rst_n
19	E19	W	0h	Event #19 Reset Source: edma_rst_mod_g_rst_n
18	E18	W	0h	Event #18 Reset Source: edma_rst_mod_g_rst_n
17	E17	W	0h	Event #17 Reset Source: edma_rst_mod_g_rst_n
16	E16	W	0h	Event #16 Reset Source: edma_rst_mod_g_rst_n
15	E15	W	0h	Event #15 Reset Source: edma_rst_mod_g_rst_n
14	E14	W	0h	Event #14 Reset Source: edma_rst_mod_g_rst_n
13	E13	W	0h	Event #13 Reset Source: edma_rst_mod_g_rst_n
12	E12	W	0h	Event #12 Reset Source: edma_rst_mod_g_rst_n
11	E11	W	0h	Event #11 Reset Source: edma_rst_mod_g_rst_n
10	E10	W	0h	Event #10 Reset Source: edma_rst_mod_g_rst_n
9	E9	W	0h	Event #9 Reset Source: edma_rst_mod_g_rst_n
8	E8	W	0h	Event #8 Reset Source: edma_rst_mod_g_rst_n

Table 4-4558. ECR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	E7	W	0h	Event #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	W	0h	Event #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	W	0h	Event #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	W	0h	Event #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	W	0h	Event #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	W	0h	Event #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	W	0h	Event #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	W	0h	Event #0 Reset Source: edma_rst_mod_g_rst_n

4.28.45 TPCC_ECRH Registers

4.28.45.1 TPCC_ECRH Register (Offset = 100Ch) [reset = 0h]

Short Description: Event Clear Regi

Long Description: Event Clear Register (High Part): CPU write of '1' to the ECRH.En bit causes the ERH.En bit to be cleared. CPU write of '0' has no effect.

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Table 4-4559. Instance Table

Instance Name	Physical Address
EDMA0	52A0 100Ch

Figure 4-2159. ECRH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4560. ECRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	W	0h	Event #63 Reset Source: edma_rst_mod_g_rst_n
30	E62	W	0h	Event #62 Reset Source: edma_rst_mod_g_rst_n
29	E61	W	0h	Event #61 Reset Source: edma_rst_mod_g_rst_n
28	E60	W	0h	Event #60 Reset Source: edma_rst_mod_g_rst_n
27	E59	W	0h	Event #59 Reset Source: edma_rst_mod_g_rst_n
26	E58	W	0h	Event #58 Reset Source: edma_rst_mod_g_rst_n
25	E57	W	0h	Event #57 Reset Source: edma_rst_mod_g_rst_n
24	E56	W	0h	Event #56 Reset Source: edma_rst_mod_g_rst_n
23	E55	W	0h	Event #55 Reset Source: edma_rst_mod_g_rst_n
22	E54	W	0h	Event #54 Reset Source: edma_rst_mod_g_rst_n
21	E53	W	0h	Event #53 Reset Source: edma_rst_mod_g_rst_n
20	E52	W	0h	Event #52 Reset Source: edma_rst_mod_g_rst_n
19	E51	W	0h	Event #51 Reset Source: edma_rst_mod_g_rst_n
18	E50	W	0h	Event #50 Reset Source: edma_rst_mod_g_rst_n
17	E49	W	0h	Event #49 Reset Source: edma_rst_mod_g_rst_n
16	E48	W	0h	Event #48 Reset Source: edma_rst_mod_g_rst_n
15	E47	W	0h	Event #47 Reset Source: edma_rst_mod_g_rst_n
14	E46	W	0h	Event #46 Reset Source: edma_rst_mod_g_rst_n
13	E45	W	0h	Event #45 Reset Source: edma_rst_mod_g_rst_n
12	E44	W	0h	Event #44 Reset Source: edma_rst_mod_g_rst_n
11	E43	W	0h	Event #43 Reset Source: edma_rst_mod_g_rst_n
10	E42	W	0h	Event #42 Reset Source: edma_rst_mod_g_rst_n
9	E41	W	0h	Event #41 Reset Source: edma_rst_mod_g_rst_n
8	E40	W	0h	Event #40 Reset Source: edma_rst_mod_g_rst_n

Table 4-4560. ECRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	E39	W	0h	Event #39 Reset Source: edma_rst_mod_g_rst_n
6	E38	W	0h	Event #38 Reset Source: edma_rst_mod_g_rst_n
5	E37	W	0h	Event #37 Reset Source: edma_rst_mod_g_rst_n
4	E36	W	0h	Event #36 Reset Source: edma_rst_mod_g_rst_n
3	E35	W	0h	Event #35 Reset Source: edma_rst_mod_g_rst_n
2	E34	W	0h	Event #34 Reset Source: edma_rst_mod_g_rst_n
1	E33	W	0h	Event #33 Reset Source: edma_rst_mod_g_rst_n
0	E32	W	0h	Event #32 Reset Source: edma_rst_mod_g_rst_n

4.28.46 TPCC_ESR Registers

4.28.46.1 TPCC_ESR Register (Offset = 1010h) [reset = 0h]

Short Description: Event Set Regist

Long Description: Event Set Register: CPU write of '1' to the ESR.En bit causes the ER.En bit to be set. CPU write of '0' has no effect.

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Table 4-4561. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1010h

Figure 4-2160. ESR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4562. ESR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	W	0h	Event #31 Reset Source: edma_rst_mod_g_rst_n
30	E30	W	0h	Event #30 Reset Source: edma_rst_mod_g_rst_n
29	E29	W	0h	Event #29 Reset Source: edma_rst_mod_g_rst_n
28	E28	W	0h	Event #28 Reset Source: edma_rst_mod_g_rst_n
27	E27	W	0h	Event #27 Reset Source: edma_rst_mod_g_rst_n
26	E26	W	0h	Event #26 Reset Source: edma_rst_mod_g_rst_n
25	E25	W	0h	Event #25 Reset Source: edma_rst_mod_g_rst_n
24	E24	W	0h	Event #24 Reset Source: edma_rst_mod_g_rst_n
23	E23	W	0h	Event #23 Reset Source: edma_rst_mod_g_rst_n
22	E22	W	0h	Event #22 Reset Source: edma_rst_mod_g_rst_n
21	E21	W	0h	Event #21 Reset Source: edma_rst_mod_g_rst_n
20	E20	W	0h	Event #20 Reset Source: edma_rst_mod_g_rst_n
19	E19	W	0h	Event #19 Reset Source: edma_rst_mod_g_rst_n
18	E18	W	0h	Event #18 Reset Source: edma_rst_mod_g_rst_n
17	E17	W	0h	Event #17 Reset Source: edma_rst_mod_g_rst_n
16	E16	W	0h	Event #16 Reset Source: edma_rst_mod_g_rst_n
15	E15	W	0h	Event #15 Reset Source: edma_rst_mod_g_rst_n
14	E14	W	0h	Event #14 Reset Source: edma_rst_mod_g_rst_n
13	E13	W	0h	Event #13 Reset Source: edma_rst_mod_g_rst_n
12	E12	W	0h	Event #12 Reset Source: edma_rst_mod_g_rst_n
11	E11	W	0h	Event #11 Reset Source: edma_rst_mod_g_rst_n
10	E10	W	0h	Event #10 Reset Source: edma_rst_mod_g_rst_n
9	E9	W	0h	Event #9 Reset Source: edma_rst_mod_g_rst_n
8	E8	W	0h	Event #8 Reset Source: edma_rst_mod_g_rst_n

Table 4-4562. ESR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	E7	W	0h	Event #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	W	0h	Event #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	W	0h	Event #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	W	0h	Event #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	W	0h	Event #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	W	0h	Event #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	W	0h	Event #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	W	0h	Event #0 Reset Source: edma_rst_mod_g_rst_n

4.28.47 TPCC_ESRH Registers

4.28.47.1 TPCC_ESRH Register (Offset = 1014h) [reset = 0h]

Short Description: Event Set Regist

Long Description: Event Set Register (High Part) CPU write of '1' to the ESRH.En bit causes the ERH.En bit to be set. CPU write of '0' has no effect.

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Table 4-4563. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1014h

Figure 4-2161. ESRH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4564. ESRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	W	0h	Event #63 Reset Source: edma_rst_mod_g_rst_n
30	E62	W	0h	Event #62 Reset Source: edma_rst_mod_g_rst_n
29	E61	W	0h	Event #61 Reset Source: edma_rst_mod_g_rst_n
28	E60	W	0h	Event #60 Reset Source: edma_rst_mod_g_rst_n
27	E59	W	0h	Event #59 Reset Source: edma_rst_mod_g_rst_n
26	E58	W	0h	Event #58 Reset Source: edma_rst_mod_g_rst_n
25	E57	W	0h	Event #57 Reset Source: edma_rst_mod_g_rst_n
24	E56	W	0h	Event #56 Reset Source: edma_rst_mod_g_rst_n
23	E55	W	0h	Event #55 Reset Source: edma_rst_mod_g_rst_n
22	E54	W	0h	Event #54 Reset Source: edma_rst_mod_g_rst_n
21	E53	W	0h	Event #53 Reset Source: edma_rst_mod_g_rst_n
20	E52	W	0h	Event #52 Reset Source: edma_rst_mod_g_rst_n
19	E51	W	0h	Event #51 Reset Source: edma_rst_mod_g_rst_n
18	E50	W	0h	Event #50 Reset Source: edma_rst_mod_g_rst_n
17	E49	W	0h	Event #49 Reset Source: edma_rst_mod_g_rst_n
16	E48	W	0h	Event #48 Reset Source: edma_rst_mod_g_rst_n
15	E47	W	0h	Event #47 Reset Source: edma_rst_mod_g_rst_n
14	E46	W	0h	Event #46 Reset Source: edma_rst_mod_g_rst_n
13	E45	W	0h	Event #45 Reset Source: edma_rst_mod_g_rst_n
12	E44	W	0h	Event #44 Reset Source: edma_rst_mod_g_rst_n
11	E43	W	0h	Event #43 Reset Source: edma_rst_mod_g_rst_n
10	E42	W	0h	Event #42 Reset Source: edma_rst_mod_g_rst_n
9	E41	W	0h	Event #41 Reset Source: edma_rst_mod_g_rst_n
8	E40	W	0h	Event #40 Reset Source: edma_rst_mod_g_rst_n

Table 4-4564. ESRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	E39	W	0h	Event #39 Reset Source: edma_rst_mod_g_rst_n
6	E38	W	0h	Event #38 Reset Source: edma_rst_mod_g_rst_n
5	E37	W	0h	Event #37 Reset Source: edma_rst_mod_g_rst_n
4	E36	W	0h	Event #36 Reset Source: edma_rst_mod_g_rst_n
3	E35	W	0h	Event #35 Reset Source: edma_rst_mod_g_rst_n
2	E34	W	0h	Event #34 Reset Source: edma_rst_mod_g_rst_n
1	E33	W	0h	Event #33 Reset Source: edma_rst_mod_g_rst_n
0	E32	W	0h	Event #32 Reset Source: edma_rst_mod_g_rst_n

4.28.48 TPCC_CER Registers

4.28.48.1 TPCC_CER Register (Offset = 1018h) [reset = 0h]

Short Description: Chained Event Re

Long Description: Chained Event Register: If CER.En bit is set (regardless of state of EER.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CER.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CER.En bit is cleared when the corresponding event is prioritized and serviced. If the CER.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CER.En cannot be set or cleared via software.

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Table 4-4565. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1018h

Figure 4-2162. CER Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4566. CER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	R	0h	Event #31 Reset Source: edma_rst_mod_g_rst_n
30	E30	R	0h	Event #30 Reset Source: edma_rst_mod_g_rst_n
29	E29	R	0h	Event #29 Reset Source: edma_rst_mod_g_rst_n
28	E28	R	0h	Event #28 Reset Source: edma_rst_mod_g_rst_n
27	E27	R	0h	Event #27 Reset Source: edma_rst_mod_g_rst_n
26	E26	R	0h	Event #26 Reset Source: edma_rst_mod_g_rst_n
25	E25	R	0h	Event #25 Reset Source: edma_rst_mod_g_rst_n
24	E24	R	0h	Event #24 Reset Source: edma_rst_mod_g_rst_n
23	E23	R	0h	Event #23 Reset Source: edma_rst_mod_g_rst_n
22	E22	R	0h	Event #22 Reset Source: edma_rst_mod_g_rst_n
21	E21	R	0h	Event #21 Reset Source: edma_rst_mod_g_rst_n
20	E20	R	0h	Event #20 Reset Source: edma_rst_mod_g_rst_n
19	E19	R	0h	Event #19 Reset Source: edma_rst_mod_g_rst_n
18	E18	R	0h	Event #18 Reset Source: edma_rst_mod_g_rst_n
17	E17	R	0h	Event #17 Reset Source: edma_rst_mod_g_rst_n
16	E16	R	0h	Event #16 Reset Source: edma_rst_mod_g_rst_n
15	E15	R	0h	Event #15 Reset Source: edma_rst_mod_g_rst_n
14	E14	R	0h	Event #14 Reset Source: edma_rst_mod_g_rst_n
13	E13	R	0h	Event #13 Reset Source: edma_rst_mod_g_rst_n

Table 4-4566. CER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	E12	R	0h	Event #12 Reset Source: edma_rst_mod_g_rst_n
11	E11	R	0h	Event #11 Reset Source: edma_rst_mod_g_rst_n
10	E10	R	0h	Event #10 Reset Source: edma_rst_mod_g_rst_n
9	E9	R	0h	Event #9 Reset Source: edma_rst_mod_g_rst_n
8	E8	R	0h	Event #8 Reset Source: edma_rst_mod_g_rst_n
7	E7	R	0h	Event #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	R	0h	Event #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	R	0h	Event #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	R	0h	Event #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	R	0h	Event #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	R	0h	Event #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	R	0h	Event #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	R	0h	Event #0 Reset Source: edma_rst_mod_g_rst_n

4.28.49 TPCC_CERH Registers

4.28.49.1 TPCC_CERH Register (Offset = 101Ch) [reset = 0h]

Short Description: Chained Event Re

Long Description: Chained Event Register (High Part): If CERH.En bit is set (regardless of state of EERH.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CERH.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CERH.En bit is cleared when the corresponding event is prioritized and serviced. If the CERH.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CERH.En cannot be set or cleared via software.

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Table 4-4567. Instance Table

Instance Name	Physical Address
EDMA0	52A0 101Ch

Figure 4-2163. CERH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4568. CERH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	R	0h	Event #63 Reset Source: edma_rst_mod_g_rst_n
30	E62	R	0h	Event #62 Reset Source: edma_rst_mod_g_rst_n
29	E61	R	0h	Event #61 Reset Source: edma_rst_mod_g_rst_n
28	E60	R	0h	Event #60 Reset Source: edma_rst_mod_g_rst_n
27	E59	R	0h	Event #59 Reset Source: edma_rst_mod_g_rst_n
26	E58	R	0h	Event #58 Reset Source: edma_rst_mod_g_rst_n
25	E57	R	0h	Event #57 Reset Source: edma_rst_mod_g_rst_n
24	E56	R	0h	Event #56 Reset Source: edma_rst_mod_g_rst_n
23	E55	R	0h	Event #55 Reset Source: edma_rst_mod_g_rst_n
22	E54	R	0h	Event #54 Reset Source: edma_rst_mod_g_rst_n
21	E53	R	0h	Event #53 Reset Source: edma_rst_mod_g_rst_n
20	E52	R	0h	Event #52 Reset Source: edma_rst_mod_g_rst_n
19	E51	R	0h	Event #51 Reset Source: edma_rst_mod_g_rst_n
18	E50	R	0h	Event #50 Reset Source: edma_rst_mod_g_rst_n
17	E49	R	0h	Event #49 Reset Source: edma_rst_mod_g_rst_n
16	E48	R	0h	Event #48 Reset Source: edma_rst_mod_g_rst_n
15	E47	R	0h	Event #47 Reset Source: edma_rst_mod_g_rst_n
14	E46	R	0h	Event #46 Reset Source: edma_rst_mod_g_rst_n
13	E45	R	0h	Event #45 Reset Source: edma_rst_mod_g_rst_n

Table 4-4568. CERH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	E44	R	0h	Event #44 Reset Source: edma_rst_mod_g_rst_n
11	E43	R	0h	Event #43 Reset Source: edma_rst_mod_g_rst_n
10	E42	R	0h	Event #42 Reset Source: edma_rst_mod_g_rst_n
9	E41	R	0h	Event #41 Reset Source: edma_rst_mod_g_rst_n
8	E40	R	0h	Event #40 Reset Source: edma_rst_mod_g_rst_n
7	E39	R	0h	Event #39 Reset Source: edma_rst_mod_g_rst_n
6	E38	R	0h	Event #38 Reset Source: edma_rst_mod_g_rst_n
5	E37	R	0h	Event #37 Reset Source: edma_rst_mod_g_rst_n
4	E36	R	0h	Event #36 Reset Source: edma_rst_mod_g_rst_n
3	E35	R	0h	Event #35 Reset Source: edma_rst_mod_g_rst_n
2	E34	R	0h	Event #34 Reset Source: edma_rst_mod_g_rst_n
1	E33	R	0h	Event #33 Reset Source: edma_rst_mod_g_rst_n
0	E32	R	0h	Event #32 Reset Source: edma_rst_mod_g_rst_n

4.28.50 TPCC_EER Registers

4.28.50.1 TPCC_EER Register (Offset = 1020h) [reset = 0h]

Short Description: Event Enable Reg

Long Description: Event Enable Register: Enables DMA transfers for ER.En pending events. ER.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CER) or Event Set Register (ESR). Note that if a bit is set in ER.En while EER.En is disabled no action is taken. If EER.En is enabled at a later point (and ER.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EER.En is not directly writeable. Events can be enabled via writes to EESR and can be disabled via writes to EECR register. EER.En = 0: ER.En is not enabled to trigger DMA transfers. EER.En = 1: ER.En is enabled to trigger DMA transfers.

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Table 4-4569. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1020h

Figure 4-2164. EER Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4570. EER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	R	0h	Event #31 Reset Source: edma_rst_mod_g_rst_n
30	E30	R	0h	Event #30 Reset Source: edma_rst_mod_g_rst_n
29	E29	R	0h	Event #29 Reset Source: edma_rst_mod_g_rst_n
28	E28	R	0h	Event #28 Reset Source: edma_rst_mod_g_rst_n
27	E27	R	0h	Event #27 Reset Source: edma_rst_mod_g_rst_n
26	E26	R	0h	Event #26 Reset Source: edma_rst_mod_g_rst_n
25	E25	R	0h	Event #25 Reset Source: edma_rst_mod_g_rst_n
24	E24	R	0h	Event #24 Reset Source: edma_rst_mod_g_rst_n
23	E23	R	0h	Event #23 Reset Source: edma_rst_mod_g_rst_n
22	E22	R	0h	Event #22 Reset Source: edma_rst_mod_g_rst_n
21	E21	R	0h	Event #21 Reset Source: edma_rst_mod_g_rst_n
20	E20	R	0h	Event #20 Reset Source: edma_rst_mod_g_rst_n
19	E19	R	0h	Event #19 Reset Source: edma_rst_mod_g_rst_n
18	E18	R	0h	Event #18 Reset Source: edma_rst_mod_g_rst_n
17	E17	R	0h	Event #17 Reset Source: edma_rst_mod_g_rst_n
16	E16	R	0h	Event #16 Reset Source: edma_rst_mod_g_rst_n
15	E15	R	0h	Event #15 Reset Source: edma_rst_mod_g_rst_n
14	E14	R	0h	Event #14 Reset Source: edma_rst_mod_g_rst_n
13	E13	R	0h	Event #13 Reset Source: edma_rst_mod_g_rst_n

Table 4-4570. EER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	E12	R	0h	Event #12 Reset Source: edma_rst_mod_g_rst_n
11	E11	R	0h	Event #11 Reset Source: edma_rst_mod_g_rst_n
10	E10	R	0h	Event #10 Reset Source: edma_rst_mod_g_rst_n
9	E9	R	0h	Event #9 Reset Source: edma_rst_mod_g_rst_n
8	E8	R	0h	Event #8 Reset Source: edma_rst_mod_g_rst_n
7	E7	R	0h	Event #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	R	0h	Event #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	R	0h	Event #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	R	0h	Event #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	R	0h	Event #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	R	0h	Event #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	R	0h	Event #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	R	0h	Event #0 Reset Source: edma_rst_mod_g_rst_n

4.28.51 TPCC_EERH Registers

4.28.51.1 TPCC_EERH Register (Offset = 1024h) [reset = 0h]

Short Description: Event Enable Reg

Long Description: Event Enable Register (High Part): Enables DMA transfers for ERH.En pending events. ERH.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CERH) or Event Set Register (ESRH). Note that if a bit is set in ERH.En while EERH.En is disabled no action is taken. If EERH.En is enabled at a later point (and ERH.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EERH.En is not directly writeable. Events can be enabled via writes to EESRH and can be disabled via writes to EECRH register. EERH.En = 0: ER.En is not enabled to trigger DMA transfers. EERH.En = 1: ER.En is enabled to trigger DMA transfers.

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Table 4-4571. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1024h

Figure 4-2165. EERH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4572. EERH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	R	0h	Event #63 Reset Source: edma_rst_mod_g_rst_n
30	E62	R	0h	Event #62 Reset Source: edma_rst_mod_g_rst_n
29	E61	R	0h	Event #61 Reset Source: edma_rst_mod_g_rst_n
28	E60	R	0h	Event #60 Reset Source: edma_rst_mod_g_rst_n
27	E59	R	0h	Event #59 Reset Source: edma_rst_mod_g_rst_n
26	E58	R	0h	Event #58 Reset Source: edma_rst_mod_g_rst_n
25	E57	R	0h	Event #57 Reset Source: edma_rst_mod_g_rst_n
24	E56	R	0h	Event #56 Reset Source: edma_rst_mod_g_rst_n
23	E55	R	0h	Event #55 Reset Source: edma_rst_mod_g_rst_n
22	E54	R	0h	Event #54 Reset Source: edma_rst_mod_g_rst_n
21	E53	R	0h	Event #53 Reset Source: edma_rst_mod_g_rst_n
20	E52	R	0h	Event #52 Reset Source: edma_rst_mod_g_rst_n
19	E51	R	0h	Event #51 Reset Source: edma_rst_mod_g_rst_n
18	E50	R	0h	Event #50 Reset Source: edma_rst_mod_g_rst_n
17	E49	R	0h	Event #49 Reset Source: edma_rst_mod_g_rst_n
16	E48	R	0h	Event #48 Reset Source: edma_rst_mod_g_rst_n
15	E47	R	0h	Event #47 Reset Source: edma_rst_mod_g_rst_n
14	E46	R	0h	Event #46 Reset Source: edma_rst_mod_g_rst_n
13	E45	R	0h	Event #45 Reset Source: edma_rst_mod_g_rst_n

Table 4-4572. EERH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	E44	R	0h	Event #44 Reset Source: edma_rst_mod_g_rst_n
11	E43	R	0h	Event #43 Reset Source: edma_rst_mod_g_rst_n
10	E42	R	0h	Event #42 Reset Source: edma_rst_mod_g_rst_n
9	E41	R	0h	Event #41 Reset Source: edma_rst_mod_g_rst_n
8	E40	R	0h	Event #40 Reset Source: edma_rst_mod_g_rst_n
7	E39	R	0h	Event #39 Reset Source: edma_rst_mod_g_rst_n
6	E38	R	0h	Event #38 Reset Source: edma_rst_mod_g_rst_n
5	E37	R	0h	Event #37 Reset Source: edma_rst_mod_g_rst_n
4	E36	R	0h	Event #36 Reset Source: edma_rst_mod_g_rst_n
3	E35	R	0h	Event #35 Reset Source: edma_rst_mod_g_rst_n
2	E34	R	0h	Event #34 Reset Source: edma_rst_mod_g_rst_n
1	E33	R	0h	Event #33 Reset Source: edma_rst_mod_g_rst_n
0	E32	R	0h	Event #32 Reset Source: edma_rst_mod_g_rst_n

4.28.52 TPCC_EECR Registers

4.28.52.1 TPCC_EECR Register (Offset = 1028h) [reset = 0h]

Short Description: Event Enable Cle

Long Description: Event Enable Clear Register: CPU write of '1' to the EECR.En bit causes the EER.En bit to be cleared. CPU write of '0' has no effect..

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Table 4-4573. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1028h

Figure 4-2166. EECR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4574. EECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	W	0h	Event #31 Reset Source: edma_rst_mod_g_rst_n
30	E30	W	0h	Event #30 Reset Source: edma_rst_mod_g_rst_n
29	E29	W	0h	Event #29 Reset Source: edma_rst_mod_g_rst_n
28	E28	W	0h	Event #28 Reset Source: edma_rst_mod_g_rst_n
27	E27	W	0h	Event #27 Reset Source: edma_rst_mod_g_rst_n
26	E26	W	0h	Event #26 Reset Source: edma_rst_mod_g_rst_n
25	E25	W	0h	Event #25 Reset Source: edma_rst_mod_g_rst_n
24	E24	W	0h	Event #24 Reset Source: edma_rst_mod_g_rst_n
23	E23	W	0h	Event #23 Reset Source: edma_rst_mod_g_rst_n
22	E22	W	0h	Event #22 Reset Source: edma_rst_mod_g_rst_n
21	E21	W	0h	Event #21 Reset Source: edma_rst_mod_g_rst_n
20	E20	W	0h	Event #20 Reset Source: edma_rst_mod_g_rst_n
19	E19	W	0h	Event #19 Reset Source: edma_rst_mod_g_rst_n
18	E18	W	0h	Event #18 Reset Source: edma_rst_mod_g_rst_n
17	E17	W	0h	Event #17 Reset Source: edma_rst_mod_g_rst_n
16	E16	W	0h	Event #16 Reset Source: edma_rst_mod_g_rst_n
15	E15	W	0h	Event #15 Reset Source: edma_rst_mod_g_rst_n
14	E14	W	0h	Event #14 Reset Source: edma_rst_mod_g_rst_n
13	E13	W	0h	Event #13 Reset Source: edma_rst_mod_g_rst_n
12	E12	W	0h	Event #12 Reset Source: edma_rst_mod_g_rst_n
11	E11	W	0h	Event #11 Reset Source: edma_rst_mod_g_rst_n
10	E10	W	0h	Event #10 Reset Source: edma_rst_mod_g_rst_n
9	E9	W	0h	Event #9 Reset Source: edma_rst_mod_g_rst_n
8	E8	W	0h	Event #8 Reset Source: edma_rst_mod_g_rst_n

Table 4-4574. EECR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	E7	W	0h	Event #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	W	0h	Event #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	W	0h	Event #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	W	0h	Event #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	W	0h	Event #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	W	0h	Event #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	W	0h	Event #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	W	0h	Event #0 Reset Source: edma_rst_mod_g_rst_n

4.28.53 TPCC_EECRH Registers

4.28.53.1 TPCC_EECRH Register (Offset = 102Ch) [reset = 0h]

Short Description: Event Enable Cle

Long Description: Event Enable Clear Register (High Part): CPU write of '1' to the EECRH.En bit causes the EERH.En bit to be cleared. CPU write of '0' has no effect..

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Table 4-4575. Instance Table

Instance Name	Physical Address
EDMA0	52A0 102Ch

Figure 4-2167. EECRH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4576. EECRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	W	0h	Event #63 Reset Source: edma_rst_mod_g_rst_n
30	E62	W	0h	Event #62 Reset Source: edma_rst_mod_g_rst_n
29	E61	W	0h	Event #61 Reset Source: edma_rst_mod_g_rst_n
28	E60	W	0h	Event #60 Reset Source: edma_rst_mod_g_rst_n
27	E59	W	0h	Event #59 Reset Source: edma_rst_mod_g_rst_n
26	E58	W	0h	Event #58 Reset Source: edma_rst_mod_g_rst_n
25	E57	W	0h	Event #57 Reset Source: edma_rst_mod_g_rst_n
24	E56	W	0h	Event #56 Reset Source: edma_rst_mod_g_rst_n
23	E55	W	0h	Event #55 Reset Source: edma_rst_mod_g_rst_n
22	E54	W	0h	Event #54 Reset Source: edma_rst_mod_g_rst_n
21	E53	W	0h	Event #53 Reset Source: edma_rst_mod_g_rst_n
20	E52	W	0h	Event #52 Reset Source: edma_rst_mod_g_rst_n
19	E51	W	0h	Event #51 Reset Source: edma_rst_mod_g_rst_n
18	E50	W	0h	Event #50 Reset Source: edma_rst_mod_g_rst_n
17	E49	W	0h	Event #49 Reset Source: edma_rst_mod_g_rst_n
16	E48	W	0h	Event #48 Reset Source: edma_rst_mod_g_rst_n
15	E47	W	0h	Event #47 Reset Source: edma_rst_mod_g_rst_n
14	E46	W	0h	Event #46 Reset Source: edma_rst_mod_g_rst_n
13	E45	W	0h	Event #45 Reset Source: edma_rst_mod_g_rst_n
12	E44	W	0h	Event #44 Reset Source: edma_rst_mod_g_rst_n
11	E43	W	0h	Event #43 Reset Source: edma_rst_mod_g_rst_n
10	E42	W	0h	Event #42 Reset Source: edma_rst_mod_g_rst_n
9	E41	W	0h	Event #41 Reset Source: edma_rst_mod_g_rst_n
8	E40	W	0h	Event #40 Reset Source: edma_rst_mod_g_rst_n

Table 4-4576. EECRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	E39	W	0h	Event #39 Reset Source: edma_rst_mod_g_rst_n
6	E38	W	0h	Event #38 Reset Source: edma_rst_mod_g_rst_n
5	E37	W	0h	Event #37 Reset Source: edma_rst_mod_g_rst_n
4	E36	W	0h	Event #36 Reset Source: edma_rst_mod_g_rst_n
3	E35	W	0h	Event #35 Reset Source: edma_rst_mod_g_rst_n
2	E34	W	0h	Event #34 Reset Source: edma_rst_mod_g_rst_n
1	E33	W	0h	Event #33 Reset Source: edma_rst_mod_g_rst_n
0	E32	W	0h	Event #32 Reset Source: edma_rst_mod_g_rst_n

4.28.54 TPCC_EESR Registers

4.28.54.1 TPCC_EESR Register (Offset = 1030h) [reset = 0h]

Short Description: Event Enable Set

Long Description: Event Enable Set Register: CPU write of '1' to the EESR.En bit causes the EER.En bit to be set. CPU write of '0' has no effect..

Return to Summary Table

Table 4-4577. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1030h

Figure 4-2168. EESR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4578. EESR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	W	0h	Event #31 Reset Source: edma_rst_mod_g_rst_n
30	E30	W	0h	Event #30 Reset Source: edma_rst_mod_g_rst_n
29	E29	W	0h	Event #29 Reset Source: edma_rst_mod_g_rst_n
28	E28	W	0h	Event #28 Reset Source: edma_rst_mod_g_rst_n
27	E27	W	0h	Event #27 Reset Source: edma_rst_mod_g_rst_n
26	E26	W	0h	Event #26 Reset Source: edma_rst_mod_g_rst_n
25	E25	W	0h	Event #25 Reset Source: edma_rst_mod_g_rst_n
24	E24	W	0h	Event #24 Reset Source: edma_rst_mod_g_rst_n
23	E23	W	0h	Event #23 Reset Source: edma_rst_mod_g_rst_n
22	E22	W	0h	Event #22 Reset Source: edma_rst_mod_g_rst_n
21	E21	W	0h	Event #21 Reset Source: edma_rst_mod_g_rst_n
20	E20	W	0h	Event #20 Reset Source: edma_rst_mod_g_rst_n
19	E19	W	0h	Event #19 Reset Source: edma_rst_mod_g_rst_n
18	E18	W	0h	Event #18 Reset Source: edma_rst_mod_g_rst_n
17	E17	W	0h	Event #17 Reset Source: edma_rst_mod_g_rst_n
16	E16	W	0h	Event #16 Reset Source: edma_rst_mod_g_rst_n
15	E15	W	0h	Event #15 Reset Source: edma_rst_mod_g_rst_n
14	E14	W	0h	Event #14 Reset Source: edma_rst_mod_g_rst_n
13	E13	W	0h	Event #13 Reset Source: edma_rst_mod_g_rst_n
12	E12	W	0h	Event #12 Reset Source: edma_rst_mod_g_rst_n
11	E11	W	0h	Event #11 Reset Source: edma_rst_mod_g_rst_n
10	E10	W	0h	Event #10 Reset Source: edma_rst_mod_g_rst_n
9	E9	W	0h	Event #9 Reset Source: edma_rst_mod_g_rst_n
8	E8	W	0h	Event #8 Reset Source: edma_rst_mod_g_rst_n

Table 4-4578. EESR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	E7	W	0h	Event #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	W	0h	Event #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	W	0h	Event #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	W	0h	Event #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	W	0h	Event #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	W	0h	Event #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	W	0h	Event #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	W	0h	Event #0 Reset Source: edma_rst_mod_g_rst_n

4.28.55 TPCC_EESRH Registers

4.28.55.1 TPCC_EESRH Register (Offset = 1034h) [reset = 0h]

Short Description: Event Enable Set

Long Description: Event Enable Set Register (High Part): CPU write of '1' to the EESRH.En bit causes the EERH.En bit to be set. CPU write of '0' has no effect..

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Table 4-4579. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1034h

Figure 4-2169. EESRH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4580. EESRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	W	0h	Event #63 Reset Source: edma_rst_mod_g_rst_n
30	E62	W	0h	Event #62 Reset Source: edma_rst_mod_g_rst_n
29	E61	W	0h	Event #61 Reset Source: edma_rst_mod_g_rst_n
28	E60	W	0h	Event #60 Reset Source: edma_rst_mod_g_rst_n
27	E59	W	0h	Event #59 Reset Source: edma_rst_mod_g_rst_n
26	E58	W	0h	Event #58 Reset Source: edma_rst_mod_g_rst_n
25	E57	W	0h	Event #57 Reset Source: edma_rst_mod_g_rst_n
24	E56	W	0h	Event #56 Reset Source: edma_rst_mod_g_rst_n
23	E55	W	0h	Event #55 Reset Source: edma_rst_mod_g_rst_n
22	E54	W	0h	Event #54 Reset Source: edma_rst_mod_g_rst_n
21	E53	W	0h	Event #53 Reset Source: edma_rst_mod_g_rst_n
20	E52	W	0h	Event #52 Reset Source: edma_rst_mod_g_rst_n
19	E51	W	0h	Event #51 Reset Source: edma_rst_mod_g_rst_n
18	E50	W	0h	Event #50 Reset Source: edma_rst_mod_g_rst_n
17	E49	W	0h	Event #49 Reset Source: edma_rst_mod_g_rst_n
16	E48	W	0h	Event #48 Reset Source: edma_rst_mod_g_rst_n
15	E47	W	0h	Event #47 Reset Source: edma_rst_mod_g_rst_n
14	E46	W	0h	Event #46 Reset Source: edma_rst_mod_g_rst_n
13	E45	W	0h	Event #45 Reset Source: edma_rst_mod_g_rst_n
12	E44	W	0h	Event #44 Reset Source: edma_rst_mod_g_rst_n
11	E43	W	0h	Event #43 Reset Source: edma_rst_mod_g_rst_n
10	E42	W	0h	Event #42 Reset Source: edma_rst_mod_g_rst_n
9	E41	W	0h	Event #41 Reset Source: edma_rst_mod_g_rst_n
8	E40	W	0h	Event #40 Reset Source: edma_rst_mod_g_rst_n

Table 4-4580. EESRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	E39	W	0h	Event #39 Reset Source: edma_rst_mod_g_rst_n
6	E38	W	0h	Event #38 Reset Source: edma_rst_mod_g_rst_n
5	E37	W	0h	Event #37 Reset Source: edma_rst_mod_g_rst_n
4	E36	W	0h	Event #36 Reset Source: edma_rst_mod_g_rst_n
3	E35	W	0h	Event #35 Reset Source: edma_rst_mod_g_rst_n
2	E34	W	0h	Event #34 Reset Source: edma_rst_mod_g_rst_n
1	E33	W	0h	Event #33 Reset Source: edma_rst_mod_g_rst_n
0	E32	W	0h	Event #32 Reset Source: edma_rst_mod_g_rst_n

4.28.56 TPCC_SER Registers

4.28.56.1 TPCC_SER Register (Offset = 1038h) [reset = 0h]

Short Description: Secondary Event

Long Description: Secondary Event Register: The secondary event register is used along with the Event Register (ER) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

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Table 4-4581. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1038h

Figure 4-2170. SER Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4582. SER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	R	0h	Event #31 Reset Source: edma_rst_mod_g_rst_n
30	E30	R	0h	Event #30 Reset Source: edma_rst_mod_g_rst_n
29	E29	R	0h	Event #29 Reset Source: edma_rst_mod_g_rst_n
28	E28	R	0h	Event #28 Reset Source: edma_rst_mod_g_rst_n
27	E27	R	0h	Event #27 Reset Source: edma_rst_mod_g_rst_n
26	E26	R	0h	Event #26 Reset Source: edma_rst_mod_g_rst_n
25	E25	R	0h	Event #25 Reset Source: edma_rst_mod_g_rst_n
24	E24	R	0h	Event #24 Reset Source: edma_rst_mod_g_rst_n
23	E23	R	0h	Event #23 Reset Source: edma_rst_mod_g_rst_n
22	E22	R	0h	Event #22 Reset Source: edma_rst_mod_g_rst_n
21	E21	R	0h	Event #21 Reset Source: edma_rst_mod_g_rst_n
20	E20	R	0h	Event #20 Reset Source: edma_rst_mod_g_rst_n
19	E19	R	0h	Event #19 Reset Source: edma_rst_mod_g_rst_n
18	E18	R	0h	Event #18 Reset Source: edma_rst_mod_g_rst_n
17	E17	R	0h	Event #17 Reset Source: edma_rst_mod_g_rst_n
16	E16	R	0h	Event #16 Reset Source: edma_rst_mod_g_rst_n
15	E15	R	0h	Event #15 Reset Source: edma_rst_mod_g_rst_n
14	E14	R	0h	Event #14 Reset Source: edma_rst_mod_g_rst_n
13	E13	R	0h	Event #13 Reset Source: edma_rst_mod_g_rst_n
12	E12	R	0h	Event #12 Reset Source: edma_rst_mod_g_rst_n
11	E11	R	0h	Event #11 Reset Source: edma_rst_mod_g_rst_n
10	E10	R	0h	Event #10 Reset Source: edma_rst_mod_g_rst_n
9	E9	R	0h	Event #9 Reset Source: edma_rst_mod_g_rst_n

Table 4-4582. SER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	E8	R	0h	Event #8 Reset Source: edma_rst_mod_g_rst_n
7	E7	R	0h	Event #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	R	0h	Event #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	R	0h	Event #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	R	0h	Event #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	R	0h	Event #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	R	0h	Event #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	R	0h	Event #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	R	0h	Event #0 Reset Source: edma_rst_mod_g_rst_n

4.28.57 TPCC_SERH Registers

4.28.57.1 TPCC_SERH Register (Offset = 103Ch) [reset = 0h]

Short Description: Secondary Event

Long Description: Secondary Event Register (High Part): The secondary event register is used along with the Event Register (ERH) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

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Table 4-4583. Instance Table

Instance Name	Physical Address
EDMA0	52A0 103Ch

Figure 4-2171. SERH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4584. SERH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	R	0h	Event #63 Reset Source: edma_rst_mod_g_rst_n
30	E62	R	0h	Event #62 Reset Source: edma_rst_mod_g_rst_n
29	E61	R	0h	Event #61 Reset Source: edma_rst_mod_g_rst_n
28	E60	R	0h	Event #60 Reset Source: edma_rst_mod_g_rst_n
27	E59	R	0h	Event #59 Reset Source: edma_rst_mod_g_rst_n
26	E58	R	0h	Event #58 Reset Source: edma_rst_mod_g_rst_n
25	E57	R	0h	Event #57 Reset Source: edma_rst_mod_g_rst_n
24	E56	R	0h	Event #56 Reset Source: edma_rst_mod_g_rst_n
23	E55	R	0h	Event #55 Reset Source: edma_rst_mod_g_rst_n
22	E54	R	0h	Event #54 Reset Source: edma_rst_mod_g_rst_n
21	E53	R	0h	Event #53 Reset Source: edma_rst_mod_g_rst_n
20	E52	R	0h	Event #52 Reset Source: edma_rst_mod_g_rst_n
19	E51	R	0h	Event #51 Reset Source: edma_rst_mod_g_rst_n
18	E50	R	0h	Event #50 Reset Source: edma_rst_mod_g_rst_n
17	E49	R	0h	Event #49 Reset Source: edma_rst_mod_g_rst_n
16	E48	R	0h	Event #48 Reset Source: edma_rst_mod_g_rst_n
15	E47	R	0h	Event #47 Reset Source: edma_rst_mod_g_rst_n
14	E46	R	0h	Event #46 Reset Source: edma_rst_mod_g_rst_n
13	E45	R	0h	Event #45 Reset Source: edma_rst_mod_g_rst_n
12	E44	R	0h	Event #44 Reset Source: edma_rst_mod_g_rst_n
11	E43	R	0h	Event #43 Reset Source: edma_rst_mod_g_rst_n
10	E42	R	0h	Event #42 Reset Source: edma_rst_mod_g_rst_n
9	E41	R	0h	Event #41 Reset Source: edma_rst_mod_g_rst_n

Table 4-4584. SERH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	E40	R	0h	Event #40 Reset Source: edma_rst_mod_g_rst_n
7	E39	R	0h	Event #39 Reset Source: edma_rst_mod_g_rst_n
6	E38	R	0h	Event #38 Reset Source: edma_rst_mod_g_rst_n
5	E37	R	0h	Event #37 Reset Source: edma_rst_mod_g_rst_n
4	E36	R	0h	Event #36 Reset Source: edma_rst_mod_g_rst_n
3	E35	R	0h	Event #35 Reset Source: edma_rst_mod_g_rst_n
2	E34	R	0h	Event #34 Reset Source: edma_rst_mod_g_rst_n
1	E33	R	0h	Event #33 Reset Source: edma_rst_mod_g_rst_n
0	E32	R	0h	Event #32 Reset Source: edma_rst_mod_g_rst_n

4.28.58 TPCC_SECR Registers

4.28.58.1 TPCC_SECR Register (Offset = 1040h) [reset = 0h]

Short Description: Secondary Event

Long Description: Secondary Event Clear Register: The secondary event clear register is used to clear the status of the SER registers. CPU write of '1' to the SECR.En bit clears the SER register. CPU write of '0' has no effect.

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Table 4-4585. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1040h

Figure 4-2172. SECR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4586. SECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	W	0h	Event #31 Reset Source: edma_rst_mod_g_rst_n
30	E30	W	0h	Event #30 Reset Source: edma_rst_mod_g_rst_n
29	E29	W	0h	Event #29 Reset Source: edma_rst_mod_g_rst_n
28	E28	W	0h	Event #28 Reset Source: edma_rst_mod_g_rst_n
27	E27	W	0h	Event #27 Reset Source: edma_rst_mod_g_rst_n
26	E26	W	0h	Event #26 Reset Source: edma_rst_mod_g_rst_n
25	E25	W	0h	Event #25 Reset Source: edma_rst_mod_g_rst_n
24	E24	W	0h	Event #24 Reset Source: edma_rst_mod_g_rst_n
23	E23	W	0h	Event #23 Reset Source: edma_rst_mod_g_rst_n
22	E22	W	0h	Event #22 Reset Source: edma_rst_mod_g_rst_n
21	E21	W	0h	Event #21 Reset Source: edma_rst_mod_g_rst_n
20	E20	W	0h	Event #20 Reset Source: edma_rst_mod_g_rst_n
19	E19	W	0h	Event #19 Reset Source: edma_rst_mod_g_rst_n
18	E18	W	0h	Event #18 Reset Source: edma_rst_mod_g_rst_n
17	E17	W	0h	Event #17 Reset Source: edma_rst_mod_g_rst_n
16	E16	W	0h	Event #16 Reset Source: edma_rst_mod_g_rst_n
15	E15	W	0h	Event #15 Reset Source: edma_rst_mod_g_rst_n
14	E14	W	0h	Event #14 Reset Source: edma_rst_mod_g_rst_n
13	E13	W	0h	Event #13 Reset Source: edma_rst_mod_g_rst_n
12	E12	W	0h	Event #12 Reset Source: edma_rst_mod_g_rst_n
11	E11	W	0h	Event #11 Reset Source: edma_rst_mod_g_rst_n
10	E10	W	0h	Event #10 Reset Source: edma_rst_mod_g_rst_n
9	E9	W	0h	Event #9 Reset Source: edma_rst_mod_g_rst_n

Table 4-4586. SECR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	E8	W	0h	Event #8 Reset Source: edma_rst_mod_g_rst_n
7	E7	W	0h	Event #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	W	0h	Event #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	W	0h	Event #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	W	0h	Event #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	W	0h	Event #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	W	0h	Event #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	W	0h	Event #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	W	0h	Event #0 Reset Source: edma_rst_mod_g_rst_n

4.28.59 TPCC_SECRH Registers

4.28.59.1 TPCC_SECRH Register (Offset = 1044h) [reset = 0h]

Short Description: Secondary Event

Long Description: Secondary Event Clear Register (High Part): The secondary event clear register is used to clear the status of the SERH registers. CPU write of '1' to the SECRH.En bit clears the SERH register. CPU write of '0' has no effect.

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Table 4-4587. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1044h

Figure 4-2173. SECRH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4588. SECRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	W	0h	Event #63 Reset Source: edma_rst_mod_g_rst_n
30	E62	W	0h	Event #62 Reset Source: edma_rst_mod_g_rst_n
29	E61	W	0h	Event #61 Reset Source: edma_rst_mod_g_rst_n
28	E60	W	0h	Event #60 Reset Source: edma_rst_mod_g_rst_n
27	E59	W	0h	Event #59 Reset Source: edma_rst_mod_g_rst_n
26	E58	W	0h	Event #58 Reset Source: edma_rst_mod_g_rst_n
25	E57	W	0h	Event #57 Reset Source: edma_rst_mod_g_rst_n
24	E56	W	0h	Event #56 Reset Source: edma_rst_mod_g_rst_n
23	E55	W	0h	Event #55 Reset Source: edma_rst_mod_g_rst_n
22	E54	W	0h	Event #54 Reset Source: edma_rst_mod_g_rst_n
21	E53	W	0h	Event #53 Reset Source: edma_rst_mod_g_rst_n
20	E52	W	0h	Event #52 Reset Source: edma_rst_mod_g_rst_n
19	E51	W	0h	Event #51 Reset Source: edma_rst_mod_g_rst_n
18	E50	W	0h	Event #50 Reset Source: edma_rst_mod_g_rst_n
17	E49	W	0h	Event #49 Reset Source: edma_rst_mod_g_rst_n
16	E48	W	0h	Event #48 Reset Source: edma_rst_mod_g_rst_n
15	E47	W	0h	Event #47 Reset Source: edma_rst_mod_g_rst_n
14	E46	W	0h	Event #46 Reset Source: edma_rst_mod_g_rst_n
13	E45	W	0h	Event #45 Reset Source: edma_rst_mod_g_rst_n
12	E44	W	0h	Event #44 Reset Source: edma_rst_mod_g_rst_n
11	E43	W	0h	Event #43 Reset Source: edma_rst_mod_g_rst_n
10	E42	W	0h	Event #42 Reset Source: edma_rst_mod_g_rst_n
9	E41	W	0h	Event #41 Reset Source: edma_rst_mod_g_rst_n

Table 4-4588. SECRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	E40	W	0h	Event #40 Reset Source: edma_rst_mod_g_rst_n
7	E39	W	0h	Event #39 Reset Source: edma_rst_mod_g_rst_n
6	E38	W	0h	Event #38 Reset Source: edma_rst_mod_g_rst_n
5	E37	W	0h	Event #37 Reset Source: edma_rst_mod_g_rst_n
4	E36	W	0h	Event #36 Reset Source: edma_rst_mod_g_rst_n
3	E35	W	0h	Event #35 Reset Source: edma_rst_mod_g_rst_n
2	E34	W	0h	Event #34 Reset Source: edma_rst_mod_g_rst_n
1	E33	W	0h	Event #33 Reset Source: edma_rst_mod_g_rst_n
0	E32	W	0h	Event #32 Reset Source: edma_rst_mod_g_rst_n

4.28.60 TPCC_IER Registers

4.28.60.1 TPCC_IER Register (Offset = 1050h) [reset = 0h]

Short Description: Int Enable Regis

Long Description: Int Enable Register: IER.In is not directly writeable. Interrupts can be enabled via writes to IESR and can be disabled via writes to IECR register. IER.In = 0: IPR.In is NOT enabled for interrupts. IER.In = 1: IPR.In IS enabled for interrupts.

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Table 4-4589. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1050h

Figure 4-2174. IER Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4590. IER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	R	0h	Interrupt associated with TCC #31 Reset Source: edma_rst_mod_g_rst_n
30	I30	R	0h	Interrupt associated with TCC #30 Reset Source: edma_rst_mod_g_rst_n
29	I29	R	0h	Interrupt associated with TCC #29 Reset Source: edma_rst_mod_g_rst_n
28	I28	R	0h	Interrupt associated with TCC #28 Reset Source: edma_rst_mod_g_rst_n
27	I27	R	0h	Interrupt associated with TCC #27 Reset Source: edma_rst_mod_g_rst_n
26	I26	R	0h	Interrupt associated with TCC #26 Reset Source: edma_rst_mod_g_rst_n
25	I25	R	0h	Interrupt associated with TCC #25 Reset Source: edma_rst_mod_g_rst_n
24	I24	R	0h	Interrupt associated with TCC #24 Reset Source: edma_rst_mod_g_rst_n
23	I23	R	0h	Interrupt associated with TCC #23 Reset Source: edma_rst_mod_g_rst_n
22	I22	R	0h	Interrupt associated with TCC #22 Reset Source: edma_rst_mod_g_rst_n
21	I21	R	0h	Interrupt associated with TCC #21 Reset Source: edma_rst_mod_g_rst_n
20	I20	R	0h	Interrupt associated with TCC #20 Reset Source: edma_rst_mod_g_rst_n
19	I19	R	0h	Interrupt associated with TCC #19 Reset Source: edma_rst_mod_g_rst_n

Table 4-4590. IER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	I18	R	0h	Interrupt associated with TCC #18 Reset Source: edma_rst_mod_g_rst_n
17	I17	R	0h	Interrupt associated with TCC #17 Reset Source: edma_rst_mod_g_rst_n
16	I16	R	0h	Interrupt associated with TCC #16 Reset Source: edma_rst_mod_g_rst_n
15	I15	R	0h	Interrupt associated with TCC #15 Reset Source: edma_rst_mod_g_rst_n
14	I14	R	0h	Interrupt associated with TCC #14 Reset Source: edma_rst_mod_g_rst_n
13	I13	R	0h	Interrupt associated with TCC #13 Reset Source: edma_rst_mod_g_rst_n
12	I12	R	0h	Interrupt associated with TCC #12 Reset Source: edma_rst_mod_g_rst_n
11	I11	R	0h	Interrupt associated with TCC #11 Reset Source: edma_rst_mod_g_rst_n
10	I10	R	0h	Interrupt associated with TCC #10 Reset Source: edma_rst_mod_g_rst_n
9	I9	R	0h	Interrupt associated with TCC #9 Reset Source: edma_rst_mod_g_rst_n
8	I8	R	0h	Interrupt associated with TCC #8 Reset Source: edma_rst_mod_g_rst_n
7	I7	R	0h	Interrupt associated with TCC #7 Reset Source: edma_rst_mod_g_rst_n
6	I6	R	0h	Interrupt associated with TCC #6 Reset Source: edma_rst_mod_g_rst_n
5	I5	R	0h	Interrupt associated with TCC #5 Reset Source: edma_rst_mod_g_rst_n
4	I4	R	0h	Interrupt associated with TCC #4 Reset Source: edma_rst_mod_g_rst_n
3	I3	R	0h	Interrupt associated with TCC #3 Reset Source: edma_rst_mod_g_rst_n
2	I2	R	0h	Interrupt associated with TCC #2 Reset Source: edma_rst_mod_g_rst_n
1	I1	R	0h	Interrupt associated with TCC #1 Reset Source: edma_rst_mod_g_rst_n
0	I0	R	0h	Interrupt associated with TCC #0 Reset Source: edma_rst_mod_g_rst_n

4.28.61 TPCC_IERH Registers

4.28.61.1 TPCC_IERH Register (Offset = 1054h) [reset = 0h]

Short Description: Int Enable Regis

Long Description: Int Enable Register (High Part): IERH.In is not directly writeable. Interrupts can be enabled via writes to IESRH and can be disabled via writes to IECRH register. IERH.In = 0: IPRH.In is NOT enabled for interrupts. IERH.In = 1: IPRH.In IS enabled for interrupts.

Return to Summary Table

Table 4-4591. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1054h

Figure 4-2175. IERH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4592. IERH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	R	0h	Interrupt associated with TCC #63 Reset Source: edma_rst_mod_g_rst_n
30	I62	R	0h	Interrupt associated with TCC #62 Reset Source: edma_rst_mod_g_rst_n
29	I61	R	0h	Interrupt associated with TCC #61 Reset Source: edma_rst_mod_g_rst_n
28	I60	R	0h	Interrupt associated with TCC #60 Reset Source: edma_rst_mod_g_rst_n
27	I59	R	0h	Interrupt associated with TCC #59 Reset Source: edma_rst_mod_g_rst_n
26	I58	R	0h	Interrupt associated with TCC #58 Reset Source: edma_rst_mod_g_rst_n
25	I57	R	0h	Interrupt associated with TCC #57 Reset Source: edma_rst_mod_g_rst_n
24	I56	R	0h	Interrupt associated with TCC #56 Reset Source: edma_rst_mod_g_rst_n
23	I55	R	0h	Interrupt associated with TCC #55 Reset Source: edma_rst_mod_g_rst_n
22	I54	R	0h	Interrupt associated with TCC #54 Reset Source: edma_rst_mod_g_rst_n
21	I53	R	0h	Interrupt associated with TCC #53 Reset Source: edma_rst_mod_g_rst_n
20	I52	R	0h	Interrupt associated with TCC #52 Reset Source: edma_rst_mod_g_rst_n
19	I51	R	0h	Interrupt associated with TCC #51 Reset Source: edma_rst_mod_g_rst_n

Table 4-4592. IERH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	I50	R	0h	Interrupt associated with TCC #50 Reset Source: edma_rst_mod_g_rst_n
17	I49	R	0h	Interrupt associated with TCC #49 Reset Source: edma_rst_mod_g_rst_n
16	I48	R	0h	Interrupt associated with TCC #48 Reset Source: edma_rst_mod_g_rst_n
15	I47	R	0h	Interrupt associated with TCC #47 Reset Source: edma_rst_mod_g_rst_n
14	I46	R	0h	Interrupt associated with TCC #46 Reset Source: edma_rst_mod_g_rst_n
13	I45	R	0h	Interrupt associated with TCC #45 Reset Source: edma_rst_mod_g_rst_n
12	I44	R	0h	Interrupt associated with TCC #44 Reset Source: edma_rst_mod_g_rst_n
11	I43	R	0h	Interrupt associated with TCC #43 Reset Source: edma_rst_mod_g_rst_n
10	I42	R	0h	Interrupt associated with TCC #42 Reset Source: edma_rst_mod_g_rst_n
9	I41	R	0h	Interrupt associated with TCC #41 Reset Source: edma_rst_mod_g_rst_n
8	I40	R	0h	Interrupt associated with TCC #40 Reset Source: edma_rst_mod_g_rst_n
7	I39	R	0h	Interrupt associated with TCC #39 Reset Source: edma_rst_mod_g_rst_n
6	I38	R	0h	Interrupt associated with TCC #38 Reset Source: edma_rst_mod_g_rst_n
5	I37	R	0h	Interrupt associated with TCC #37 Reset Source: edma_rst_mod_g_rst_n
4	I36	R	0h	Interrupt associated with TCC #36 Reset Source: edma_rst_mod_g_rst_n
3	I35	R	0h	Interrupt associated with TCC #35 Reset Source: edma_rst_mod_g_rst_n
2	I34	R	0h	Interrupt associated with TCC #34 Reset Source: edma_rst_mod_g_rst_n
1	I33	R	0h	Interrupt associated with TCC #33 Reset Source: edma_rst_mod_g_rst_n
0	I32	R	0h	Interrupt associated with TCC #32 Reset Source: edma_rst_mod_g_rst_n

4.28.62 TPCC_IECR Registers

4.28.62.1 TPCC_IECR Register (Offset = 1058h) [reset = 0h]

Short Description: Int Enable Clear

Long Description: Int Enable Clear Register: CPU write of '1' to the IECR.In bit causes the IER.In bit to be cleared. CPU write of '0' has no effect..

Return to Summary Table

Table 4-4593. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1058h

Figure 4-2176. IECR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4594. IECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	W	0h	Interrupt associated with TCC #31 Reset Source: edma_rst_mod_g_rst_n
30	I30	W	0h	Interrupt associated with TCC #30 Reset Source: edma_rst_mod_g_rst_n
29	I29	W	0h	Interrupt associated with TCC #29 Reset Source: edma_rst_mod_g_rst_n
28	I28	W	0h	Interrupt associated with TCC #28 Reset Source: edma_rst_mod_g_rst_n
27	I27	W	0h	Interrupt associated with TCC #27 Reset Source: edma_rst_mod_g_rst_n
26	I26	W	0h	Interrupt associated with TCC #26 Reset Source: edma_rst_mod_g_rst_n
25	I25	W	0h	Interrupt associated with TCC #25 Reset Source: edma_rst_mod_g_rst_n
24	I24	W	0h	Interrupt associated with TCC #24 Reset Source: edma_rst_mod_g_rst_n
23	I23	W	0h	Interrupt associated with TCC #23 Reset Source: edma_rst_mod_g_rst_n
22	I22	W	0h	Interrupt associated with TCC #22 Reset Source: edma_rst_mod_g_rst_n
21	I21	W	0h	Interrupt associated with TCC #21 Reset Source: edma_rst_mod_g_rst_n
20	I20	W	0h	Interrupt associated with TCC #20 Reset Source: edma_rst_mod_g_rst_n
19	I19	W	0h	Interrupt associated with TCC #19 Reset Source: edma_rst_mod_g_rst_n
18	I18	W	0h	Interrupt associated with TCC #18 Reset Source: edma_rst_mod_g_rst_n

Table 4-4594. IECR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	I17	W	0h	Interrupt associated with TCC #17 Reset Source: edma_rst_mod_g_rst_n
16	I16	W	0h	Interrupt associated with TCC #16 Reset Source: edma_rst_mod_g_rst_n
15	I15	W	0h	Interrupt associated with TCC #15 Reset Source: edma_rst_mod_g_rst_n
14	I14	W	0h	Interrupt associated with TCC #14 Reset Source: edma_rst_mod_g_rst_n
13	I13	W	0h	Interrupt associated with TCC #13 Reset Source: edma_rst_mod_g_rst_n
12	I12	W	0h	Interrupt associated with TCC #12 Reset Source: edma_rst_mod_g_rst_n
11	I11	W	0h	Interrupt associated with TCC #11 Reset Source: edma_rst_mod_g_rst_n
10	I10	W	0h	Interrupt associated with TCC #10 Reset Source: edma_rst_mod_g_rst_n
9	I9	W	0h	Interrupt associated with TCC #9 Reset Source: edma_rst_mod_g_rst_n
8	I8	W	0h	Interrupt associated with TCC #8 Reset Source: edma_rst_mod_g_rst_n
7	I7	W	0h	Interrupt associated with TCC #7 Reset Source: edma_rst_mod_g_rst_n
6	I6	W	0h	Interrupt associated with TCC #6 Reset Source: edma_rst_mod_g_rst_n
5	I5	W	0h	Interrupt associated with TCC #5 Reset Source: edma_rst_mod_g_rst_n
4	I4	W	0h	Interrupt associated with TCC #4 Reset Source: edma_rst_mod_g_rst_n
3	I3	W	0h	Interrupt associated with TCC #3 Reset Source: edma_rst_mod_g_rst_n
2	I2	W	0h	Interrupt associated with TCC #2 Reset Source: edma_rst_mod_g_rst_n
1	I1	W	0h	Interrupt associated with TCC #1 Reset Source: edma_rst_mod_g_rst_n
0	I0	W	0h	Interrupt associated with TCC #0 Reset Source: edma_rst_mod_g_rst_n

4.28.63 TPCC_IECRH Registers

4.28.63.1 TPCC_IECRH Register (Offset = 105Ch) [reset = 0h]

Short Description: Int Enable Clear

Long Description: Int Enable Clear Register (High Part): CPU write of '1' to the IECRH.In bit causes the IERH.In bit to be cleared. CPU write of '0' has no effect..

Return to Summary Table

Table 4-4595. Instance Table

Instance Name	Physical Address
EDMA0	52A0 105Ch

Figure 4-2177. IECRH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4596. IECRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	W	0h	Interrupt associated with TCC #63 Reset Source: edma_rst_mod_g_rst_n
30	I62	W	0h	Interrupt associated with TCC #62 Reset Source: edma_rst_mod_g_rst_n
29	I61	W	0h	Interrupt associated with TCC #61 Reset Source: edma_rst_mod_g_rst_n
28	I60	W	0h	Interrupt associated with TCC #60 Reset Source: edma_rst_mod_g_rst_n
27	I59	W	0h	Interrupt associated with TCC #59 Reset Source: edma_rst_mod_g_rst_n
26	I58	W	0h	Interrupt associated with TCC #58 Reset Source: edma_rst_mod_g_rst_n
25	I57	W	0h	Interrupt associated with TCC #57 Reset Source: edma_rst_mod_g_rst_n
24	I56	W	0h	Interrupt associated with TCC #56 Reset Source: edma_rst_mod_g_rst_n
23	I55	W	0h	Interrupt associated with TCC #55 Reset Source: edma_rst_mod_g_rst_n
22	I54	W	0h	Interrupt associated with TCC #54 Reset Source: edma_rst_mod_g_rst_n
21	I53	W	0h	Interrupt associated with TCC #53 Reset Source: edma_rst_mod_g_rst_n
20	I52	W	0h	Interrupt associated with TCC #52 Reset Source: edma_rst_mod_g_rst_n
19	I51	W	0h	Interrupt associated with TCC #51 Reset Source: edma_rst_mod_g_rst_n
18	I50	W	0h	Interrupt associated with TCC #50 Reset Source: edma_rst_mod_g_rst_n

Table 4-4596. IECRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	I49	W	0h	Interrupt associated with TCC #49 Reset Source: edma_rst_mod_g_rst_n
16	I48	W	0h	Interrupt associated with TCC #48 Reset Source: edma_rst_mod_g_rst_n
15	I47	W	0h	Interrupt associated with TCC #47 Reset Source: edma_rst_mod_g_rst_n
14	I46	W	0h	Interrupt associated with TCC #46 Reset Source: edma_rst_mod_g_rst_n
13	I45	W	0h	Interrupt associated with TCC #45 Reset Source: edma_rst_mod_g_rst_n
12	I44	W	0h	Interrupt associated with TCC #44 Reset Source: edma_rst_mod_g_rst_n
11	I43	W	0h	Interrupt associated with TCC #43 Reset Source: edma_rst_mod_g_rst_n
10	I42	W	0h	Interrupt associated with TCC #42 Reset Source: edma_rst_mod_g_rst_n
9	I41	W	0h	Interrupt associated with TCC #41 Reset Source: edma_rst_mod_g_rst_n
8	I40	W	0h	Interrupt associated with TCC #40 Reset Source: edma_rst_mod_g_rst_n
7	I39	W	0h	Interrupt associated with TCC #39 Reset Source: edma_rst_mod_g_rst_n
6	I38	W	0h	Interrupt associated with TCC #38 Reset Source: edma_rst_mod_g_rst_n
5	I37	W	0h	Interrupt associated with TCC #37 Reset Source: edma_rst_mod_g_rst_n
4	I36	W	0h	Interrupt associated with TCC #36 Reset Source: edma_rst_mod_g_rst_n
3	I35	W	0h	Interrupt associated with TCC #35 Reset Source: edma_rst_mod_g_rst_n
2	I34	W	0h	Interrupt associated with TCC #34 Reset Source: edma_rst_mod_g_rst_n
1	I33	W	0h	Interrupt associated with TCC #33 Reset Source: edma_rst_mod_g_rst_n
0	I32	W	0h	Interrupt associated with TCC #32 Reset Source: edma_rst_mod_g_rst_n

4.28.64 TPCC_IESR Registers

4.28.64.1 TPCC_IESR Register (Offset = 1060h) [reset = 0h]

Short Description: Int Enable Set R

Long Description: Int Enable Set Register: CPU write of '1' to the IESR.In bit causes the IESR.In bit to be set. CPU write of '0' has no effect..

Return to Summary Table

Table 4-4597. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1060h

Figure 4-2178. IESR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4598. IESR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	W	0h	Interrupt associated with TCC #31 Reset Source: edma_rst_mod_g_rst_n
30	I30	W	0h	Interrupt associated with TCC #30 Reset Source: edma_rst_mod_g_rst_n
29	I29	W	0h	Interrupt associated with TCC #29 Reset Source: edma_rst_mod_g_rst_n
28	I28	W	0h	Interrupt associated with TCC #28 Reset Source: edma_rst_mod_g_rst_n
27	I27	W	0h	Interrupt associated with TCC #27 Reset Source: edma_rst_mod_g_rst_n
26	I26	W	0h	Interrupt associated with TCC #26 Reset Source: edma_rst_mod_g_rst_n
25	I25	W	0h	Interrupt associated with TCC #25 Reset Source: edma_rst_mod_g_rst_n
24	I24	W	0h	Interrupt associated with TCC #24 Reset Source: edma_rst_mod_g_rst_n
23	I23	W	0h	Interrupt associated with TCC #23 Reset Source: edma_rst_mod_g_rst_n
22	I22	W	0h	Interrupt associated with TCC #22 Reset Source: edma_rst_mod_g_rst_n
21	I21	W	0h	Interrupt associated with TCC #21 Reset Source: edma_rst_mod_g_rst_n
20	I20	W	0h	Interrupt associated with TCC #20 Reset Source: edma_rst_mod_g_rst_n
19	I19	W	0h	Interrupt associated with TCC #19 Reset Source: edma_rst_mod_g_rst_n
18	I18	W	0h	Interrupt associated with TCC #18 Reset Source: edma_rst_mod_g_rst_n

Table 4-4598. IESR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	I17	W	0h	Interrupt associated with TCC #17 Reset Source: edma_rst_mod_g_rst_n
16	I16	W	0h	Interrupt associated with TCC #16 Reset Source: edma_rst_mod_g_rst_n
15	I15	W	0h	Interrupt associated with TCC #15 Reset Source: edma_rst_mod_g_rst_n
14	I14	W	0h	Interrupt associated with TCC #14 Reset Source: edma_rst_mod_g_rst_n
13	I13	W	0h	Interrupt associated with TCC #13 Reset Source: edma_rst_mod_g_rst_n
12	I12	W	0h	Interrupt associated with TCC #12 Reset Source: edma_rst_mod_g_rst_n
11	I11	W	0h	Interrupt associated with TCC #11 Reset Source: edma_rst_mod_g_rst_n
10	I10	W	0h	Interrupt associated with TCC #10 Reset Source: edma_rst_mod_g_rst_n
9	I9	W	0h	Interrupt associated with TCC #9 Reset Source: edma_rst_mod_g_rst_n
8	I8	W	0h	Interrupt associated with TCC #8 Reset Source: edma_rst_mod_g_rst_n
7	I7	W	0h	Interrupt associated with TCC #7 Reset Source: edma_rst_mod_g_rst_n
6	I6	W	0h	Interrupt associated with TCC #6 Reset Source: edma_rst_mod_g_rst_n
5	I5	W	0h	Interrupt associated with TCC #5 Reset Source: edma_rst_mod_g_rst_n
4	I4	W	0h	Interrupt associated with TCC #4 Reset Source: edma_rst_mod_g_rst_n
3	I3	W	0h	Interrupt associated with TCC #3 Reset Source: edma_rst_mod_g_rst_n
2	I2	W	0h	Interrupt associated with TCC #2 Reset Source: edma_rst_mod_g_rst_n
1	I1	W	0h	Interrupt associated with TCC #1 Reset Source: edma_rst_mod_g_rst_n
0	I0	W	0h	Interrupt associated with TCC #0 Reset Source: edma_rst_mod_g_rst_n

4.28.65 TPCC_IESRH Registers

4.28.65.1 TPCC_IESRH Register (Offset = 1064h) [reset = 0h]

Short Description: Int Enable Set R

Long Description: Int Enable Set Register (High Part): CPU write of '1' to the IESRH.In bit causes the IESRH.In bit to be set. CPU write of '0' has no effect..

Return to Summary Table

Table 4-4599. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1064h

Figure 4-2179. IESRH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4600. IESRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	W	0h	Interrupt associated with TCC #63 Reset Source: edma_rst_mod_g_rst_n
30	I62	W	0h	Interrupt associated with TCC #62 Reset Source: edma_rst_mod_g_rst_n
29	I61	W	0h	Interrupt associated with TCC #61 Reset Source: edma_rst_mod_g_rst_n
28	I60	W	0h	Interrupt associated with TCC #60 Reset Source: edma_rst_mod_g_rst_n
27	I59	W	0h	Interrupt associated with TCC #59 Reset Source: edma_rst_mod_g_rst_n
26	I58	W	0h	Interrupt associated with TCC #58 Reset Source: edma_rst_mod_g_rst_n
25	I57	W	0h	Interrupt associated with TCC #57 Reset Source: edma_rst_mod_g_rst_n
24	I56	W	0h	Interrupt associated with TCC #56 Reset Source: edma_rst_mod_g_rst_n
23	I55	W	0h	Interrupt associated with TCC #55 Reset Source: edma_rst_mod_g_rst_n
22	I54	W	0h	Interrupt associated with TCC #54 Reset Source: edma_rst_mod_g_rst_n
21	I53	W	0h	Interrupt associated with TCC #53 Reset Source: edma_rst_mod_g_rst_n
20	I52	W	0h	Interrupt associated with TCC #52 Reset Source: edma_rst_mod_g_rst_n
19	I51	W	0h	Interrupt associated with TCC #51 Reset Source: edma_rst_mod_g_rst_n
18	I50	W	0h	Interrupt associated with TCC #50 Reset Source: edma_rst_mod_g_rst_n

Table 4-4600. IESRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	I49	W	0h	Interrupt associated with TCC #49 Reset Source: edma_rst_mod_g_rst_n
16	I48	W	0h	Interrupt associated with TCC #48 Reset Source: edma_rst_mod_g_rst_n
15	I47	W	0h	Interrupt associated with TCC #47 Reset Source: edma_rst_mod_g_rst_n
14	I46	W	0h	Interrupt associated with TCC #46 Reset Source: edma_rst_mod_g_rst_n
13	I45	W	0h	Interrupt associated with TCC #45 Reset Source: edma_rst_mod_g_rst_n
12	I44	W	0h	Interrupt associated with TCC #44 Reset Source: edma_rst_mod_g_rst_n
11	I43	W	0h	Interrupt associated with TCC #43 Reset Source: edma_rst_mod_g_rst_n
10	I42	W	0h	Interrupt associated with TCC #42 Reset Source: edma_rst_mod_g_rst_n
9	I41	W	0h	Interrupt associated with TCC #41 Reset Source: edma_rst_mod_g_rst_n
8	I40	W	0h	Interrupt associated with TCC #40 Reset Source: edma_rst_mod_g_rst_n
7	I39	W	0h	Interrupt associated with TCC #39 Reset Source: edma_rst_mod_g_rst_n
6	I38	W	0h	Interrupt associated with TCC #38 Reset Source: edma_rst_mod_g_rst_n
5	I37	W	0h	Interrupt associated with TCC #37 Reset Source: edma_rst_mod_g_rst_n
4	I36	W	0h	Interrupt associated with TCC #36 Reset Source: edma_rst_mod_g_rst_n
3	I35	W	0h	Interrupt associated with TCC #35 Reset Source: edma_rst_mod_g_rst_n
2	I34	W	0h	Interrupt associated with TCC #34 Reset Source: edma_rst_mod_g_rst_n
1	I33	W	0h	Interrupt associated with TCC #33 Reset Source: edma_rst_mod_g_rst_n
0	I32	W	0h	Interrupt associated with TCC #32 Reset Source: edma_rst_mod_g_rst_n

4.28.66 TPCC_IPR Registers

4.28.66.1 TPCC_IPR Register (Offset = 1068h) [reset = 0h]

Short Description: Interrupt Pendin

Long Description: Interrupt Pending Register: IPR.In bit is set when a interrupt completion code with TCC of N is detected. IPR.In bit is cleared via software by writing a '1' to ICR.In bit.

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Table 4-4601. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1068h

Figure 4-2180. IPR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4602. IPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	R	0h	Interrupt associated with TCC #31 Reset Source: edma_rst_mod_g_rst_n
30	I30	R	0h	Interrupt associated with TCC #30 Reset Source: edma_rst_mod_g_rst_n
29	I29	R	0h	Interrupt associated with TCC #29 Reset Source: edma_rst_mod_g_rst_n
28	I28	R	0h	Interrupt associated with TCC #28 Reset Source: edma_rst_mod_g_rst_n
27	I27	R	0h	Interrupt associated with TCC #27 Reset Source: edma_rst_mod_g_rst_n
26	I26	R	0h	Interrupt associated with TCC #26 Reset Source: edma_rst_mod_g_rst_n
25	I25	R	0h	Interrupt associated with TCC #25 Reset Source: edma_rst_mod_g_rst_n
24	I24	R	0h	Interrupt associated with TCC #24 Reset Source: edma_rst_mod_g_rst_n
23	I23	R	0h	Interrupt associated with TCC #23 Reset Source: edma_rst_mod_g_rst_n
22	I22	R	0h	Interrupt associated with TCC #22 Reset Source: edma_rst_mod_g_rst_n
21	I21	R	0h	Interrupt associated with TCC #21 Reset Source: edma_rst_mod_g_rst_n
20	I20	R	0h	Interrupt associated with TCC #20 Reset Source: edma_rst_mod_g_rst_n
19	I19	R	0h	Interrupt associated with TCC #19 Reset Source: edma_rst_mod_g_rst_n
18	I18	R	0h	Interrupt associated with TCC #18 Reset Source: edma_rst_mod_g_rst_n

Table 4-4602. IPR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	I17	R	0h	Interrupt associated with TCC #17 Reset Source: edma_rst_mod_g_rst_n
16	I16	R	0h	Interrupt associated with TCC #16 Reset Source: edma_rst_mod_g_rst_n
15	I15	R	0h	Interrupt associated with TCC #15 Reset Source: edma_rst_mod_g_rst_n
14	I14	R	0h	Interrupt associated with TCC #14 Reset Source: edma_rst_mod_g_rst_n
13	I13	R	0h	Interrupt associated with TCC #13 Reset Source: edma_rst_mod_g_rst_n
12	I12	R	0h	Interrupt associated with TCC #12 Reset Source: edma_rst_mod_g_rst_n
11	I11	R	0h	Interrupt associated with TCC #11 Reset Source: edma_rst_mod_g_rst_n
10	I10	R	0h	Interrupt associated with TCC #10 Reset Source: edma_rst_mod_g_rst_n
9	I9	R	0h	Interrupt associated with TCC #9 Reset Source: edma_rst_mod_g_rst_n
8	I8	R	0h	Interrupt associated with TCC #8 Reset Source: edma_rst_mod_g_rst_n
7	I7	R	0h	Interrupt associated with TCC #7 Reset Source: edma_rst_mod_g_rst_n
6	I6	R	0h	Interrupt associated with TCC #6 Reset Source: edma_rst_mod_g_rst_n
5	I5	R	0h	Interrupt associated with TCC #5 Reset Source: edma_rst_mod_g_rst_n
4	I4	R	0h	Interrupt associated with TCC #4 Reset Source: edma_rst_mod_g_rst_n
3	I3	R	0h	Interrupt associated with TCC #3 Reset Source: edma_rst_mod_g_rst_n
2	I2	R	0h	Interrupt associated with TCC #2 Reset Source: edma_rst_mod_g_rst_n
1	I1	R	0h	Interrupt associated with TCC #1 Reset Source: edma_rst_mod_g_rst_n
0	I0	R	0h	Interrupt associated with TCC #0 Reset Source: edma_rst_mod_g_rst_n

4.28.67 TPCC_IPRH Registers

4.28.67.1 TPCC_IPRH Register (Offset = 106Ch) [reset = 0h]

Short Description: Interrupt Pendin

Long Description: Interrupt Pending Register (High Part): IPRH.In bit is set when a interrupt completion code with TCC of N is detected. IPRH.In bit is cleared via software by writing a '1' to ICRH.In bit.

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Table 4-4603. Instance Table

Instance Name	Physical Address
EDMA0	52A0 106Ch

Figure 4-2181. IPRH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4604. IPRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	R	0h	Interrupt associated with TCC #63 Reset Source: edma_rst_mod_g_rst_n
30	I62	R	0h	Interrupt associated with TCC #62 Reset Source: edma_rst_mod_g_rst_n
29	I61	R	0h	Interrupt associated with TCC #61 Reset Source: edma_rst_mod_g_rst_n
28	I60	R	0h	Interrupt associated with TCC #60 Reset Source: edma_rst_mod_g_rst_n
27	I59	R	0h	Interrupt associated with TCC #59 Reset Source: edma_rst_mod_g_rst_n
26	I58	R	0h	Interrupt associated with TCC #58 Reset Source: edma_rst_mod_g_rst_n
25	I57	R	0h	Interrupt associated with TCC #57 Reset Source: edma_rst_mod_g_rst_n
24	I56	R	0h	Interrupt associated with TCC #56 Reset Source: edma_rst_mod_g_rst_n
23	I55	R	0h	Interrupt associated with TCC #55 Reset Source: edma_rst_mod_g_rst_n
22	I54	R	0h	Interrupt associated with TCC #54 Reset Source: edma_rst_mod_g_rst_n
21	I53	R	0h	Interrupt associated with TCC #53 Reset Source: edma_rst_mod_g_rst_n
20	I52	R	0h	Interrupt associated with TCC #52 Reset Source: edma_rst_mod_g_rst_n
19	I51	R	0h	Interrupt associated with TCC #51 Reset Source: edma_rst_mod_g_rst_n
18	I50	R	0h	Interrupt associated with TCC #50 Reset Source: edma_rst_mod_g_rst_n

Table 4-4604. IPRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	I49	R	0h	Interrupt associated with TCC #49 Reset Source: edma_rst_mod_g_rst_n
16	I48	R	0h	Interrupt associated with TCC #48 Reset Source: edma_rst_mod_g_rst_n
15	I47	R	0h	Interrupt associated with TCC #47 Reset Source: edma_rst_mod_g_rst_n
14	I46	R	0h	Interrupt associated with TCC #46 Reset Source: edma_rst_mod_g_rst_n
13	I45	R	0h	Interrupt associated with TCC #45 Reset Source: edma_rst_mod_g_rst_n
12	I44	R	0h	Interrupt associated with TCC #44 Reset Source: edma_rst_mod_g_rst_n
11	I43	R	0h	Interrupt associated with TCC #43 Reset Source: edma_rst_mod_g_rst_n
10	I42	R	0h	Interrupt associated with TCC #42 Reset Source: edma_rst_mod_g_rst_n
9	I41	R	0h	Interrupt associated with TCC #41 Reset Source: edma_rst_mod_g_rst_n
8	I40	R	0h	Interrupt associated with TCC #40 Reset Source: edma_rst_mod_g_rst_n
7	I39	R	0h	Interrupt associated with TCC #39 Reset Source: edma_rst_mod_g_rst_n
6	I38	R	0h	Interrupt associated with TCC #38 Reset Source: edma_rst_mod_g_rst_n
5	I37	R	0h	Interrupt associated with TCC #37 Reset Source: edma_rst_mod_g_rst_n
4	I36	R	0h	Interrupt associated with TCC #36 Reset Source: edma_rst_mod_g_rst_n
3	I35	R	0h	Interrupt associated with TCC #35 Reset Source: edma_rst_mod_g_rst_n
2	I34	R	0h	Interrupt associated with TCC #34 Reset Source: edma_rst_mod_g_rst_n
1	I33	R	0h	Interrupt associated with TCC #33 Reset Source: edma_rst_mod_g_rst_n
0	I32	R	0h	Interrupt associated with TCC #32 Reset Source: edma_rst_mod_g_rst_n

4.28.68 TPCC_ICR Registers

4.28.68.1 TPCC_ICR Register (Offset = 1070h) [reset = 0h]

Short Description: Interrupt Clear

Long Description: Interrupt Clear Register: CPU write of '1' to the ICR.In bit causes the IPR.In bit to be cleared. CPU write of '0' has no effect. All IPR.In bits must be cleared before additional interrupts will be asserted by CC.

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Table 4-4605. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1070h

Figure 4-2182. ICR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4606. ICR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	W	0h	Interrupt associated with TCC #31 Reset Source: edma_rst_mod_g_rst_n
30	I30	W	0h	Interrupt associated with TCC #30 Reset Source: edma_rst_mod_g_rst_n
29	I29	W	0h	Interrupt associated with TCC #29 Reset Source: edma_rst_mod_g_rst_n
28	I28	W	0h	Interrupt associated with TCC #28 Reset Source: edma_rst_mod_g_rst_n
27	I27	W	0h	Interrupt associated with TCC #27 Reset Source: edma_rst_mod_g_rst_n
26	I26	W	0h	Interrupt associated with TCC #26 Reset Source: edma_rst_mod_g_rst_n
25	I25	W	0h	Interrupt associated with TCC #25 Reset Source: edma_rst_mod_g_rst_n
24	I24	W	0h	Interrupt associated with TCC #24 Reset Source: edma_rst_mod_g_rst_n
23	I23	W	0h	Interrupt associated with TCC #23 Reset Source: edma_rst_mod_g_rst_n
22	I22	W	0h	Interrupt associated with TCC #22 Reset Source: edma_rst_mod_g_rst_n
21	I21	W	0h	Interrupt associated with TCC #21 Reset Source: edma_rst_mod_g_rst_n
20	I20	W	0h	Interrupt associated with TCC #20 Reset Source: edma_rst_mod_g_rst_n
19	I19	W	0h	Interrupt associated with TCC #19 Reset Source: edma_rst_mod_g_rst_n
18	I18	W	0h	Interrupt associated with TCC #18 Reset Source: edma_rst_mod_g_rst_n

Table 4-4606. ICR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	I17	W	0h	Interrupt associated with TCC #17 Reset Source: edma_rst_mod_g_rst_n
16	I16	W	0h	Interrupt associated with TCC #16 Reset Source: edma_rst_mod_g_rst_n
15	I15	W	0h	Interrupt associated with TCC #15 Reset Source: edma_rst_mod_g_rst_n
14	I14	W	0h	Interrupt associated with TCC #14 Reset Source: edma_rst_mod_g_rst_n
13	I13	W	0h	Interrupt associated with TCC #13 Reset Source: edma_rst_mod_g_rst_n
12	I12	W	0h	Interrupt associated with TCC #12 Reset Source: edma_rst_mod_g_rst_n
11	I11	W	0h	Interrupt associated with TCC #11 Reset Source: edma_rst_mod_g_rst_n
10	I10	W	0h	Interrupt associated with TCC #10 Reset Source: edma_rst_mod_g_rst_n
9	I9	W	0h	Interrupt associated with TCC #9 Reset Source: edma_rst_mod_g_rst_n
8	I8	W	0h	Interrupt associated with TCC #8 Reset Source: edma_rst_mod_g_rst_n
7	I7	W	0h	Interrupt associated with TCC #7 Reset Source: edma_rst_mod_g_rst_n
6	I6	W	0h	Interrupt associated with TCC #6 Reset Source: edma_rst_mod_g_rst_n
5	I5	W	0h	Interrupt associated with TCC #5 Reset Source: edma_rst_mod_g_rst_n
4	I4	W	0h	Interrupt associated with TCC #4 Reset Source: edma_rst_mod_g_rst_n
3	I3	W	0h	Interrupt associated with TCC #3 Reset Source: edma_rst_mod_g_rst_n
2	I2	W	0h	Interrupt associated with TCC #2 Reset Source: edma_rst_mod_g_rst_n
1	I1	W	0h	Interrupt associated with TCC #1 Reset Source: edma_rst_mod_g_rst_n
0	I0	W	0h	Interrupt associated with TCC #0 Reset Source: edma_rst_mod_g_rst_n

4.28.69 TPCC_ICRH Registers

4.28.69.1 TPCC_ICRH Register (Offset = 1074h) [reset = 0h]

Short Description: Interrupt Clear

Long Description: Interrupt Clear Register (High Part): CPU write of '1' to the ICRH.In bit causes the IPRH.In bit to be cleared. CPU write of '0' has no effect. All IPRH.In bits must be cleared before additional interrupts will be asserted by CC.

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Table 4-4607. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1074h

Figure 4-2183. ICRH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4608. ICRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	W	0h	Interrupt associated with TCC #63 Reset Source: edma_rst_mod_g_rst_n
30	I62	W	0h	Interrupt associated with TCC #62 Reset Source: edma_rst_mod_g_rst_n
29	I61	W	0h	Interrupt associated with TCC #61 Reset Source: edma_rst_mod_g_rst_n
28	I60	W	0h	Interrupt associated with TCC #60 Reset Source: edma_rst_mod_g_rst_n
27	I59	W	0h	Interrupt associated with TCC #59 Reset Source: edma_rst_mod_g_rst_n
26	I58	W	0h	Interrupt associated with TCC #58 Reset Source: edma_rst_mod_g_rst_n
25	I57	W	0h	Interrupt associated with TCC #57 Reset Source: edma_rst_mod_g_rst_n
24	I56	W	0h	Interrupt associated with TCC #56 Reset Source: edma_rst_mod_g_rst_n
23	I55	W	0h	Interrupt associated with TCC #55 Reset Source: edma_rst_mod_g_rst_n
22	I54	W	0h	Interrupt associated with TCC #54 Reset Source: edma_rst_mod_g_rst_n
21	I53	W	0h	Interrupt associated with TCC #53 Reset Source: edma_rst_mod_g_rst_n
20	I52	W	0h	Interrupt associated with TCC #52 Reset Source: edma_rst_mod_g_rst_n
19	I51	W	0h	Interrupt associated with TCC #51 Reset Source: edma_rst_mod_g_rst_n

Table 4-4608. ICRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	I50	W	0h	Interrupt associated with TCC #50 Reset Source: edma_rst_mod_g_rst_n
17	I49	W	0h	Interrupt associated with TCC #49 Reset Source: edma_rst_mod_g_rst_n
16	I48	W	0h	Interrupt associated with TCC #48 Reset Source: edma_rst_mod_g_rst_n
15	I47	W	0h	Interrupt associated with TCC #47 Reset Source: edma_rst_mod_g_rst_n
14	I46	W	0h	Interrupt associated with TCC #46 Reset Source: edma_rst_mod_g_rst_n
13	I45	W	0h	Interrupt associated with TCC #45 Reset Source: edma_rst_mod_g_rst_n
12	I44	W	0h	Interrupt associated with TCC #44 Reset Source: edma_rst_mod_g_rst_n
11	I43	W	0h	Interrupt associated with TCC #43 Reset Source: edma_rst_mod_g_rst_n
10	I42	W	0h	Interrupt associated with TCC #42 Reset Source: edma_rst_mod_g_rst_n
9	I41	W	0h	Interrupt associated with TCC #41 Reset Source: edma_rst_mod_g_rst_n
8	I40	W	0h	Interrupt associated with TCC #40 Reset Source: edma_rst_mod_g_rst_n
7	I39	W	0h	Interrupt associated with TCC #39 Reset Source: edma_rst_mod_g_rst_n
6	I38	W	0h	Interrupt associated with TCC #38 Reset Source: edma_rst_mod_g_rst_n
5	I37	W	0h	Interrupt associated with TCC #37 Reset Source: edma_rst_mod_g_rst_n
4	I36	W	0h	Interrupt associated with TCC #36 Reset Source: edma_rst_mod_g_rst_n
3	I35	W	0h	Interrupt associated with TCC #35 Reset Source: edma_rst_mod_g_rst_n
2	I34	W	0h	Interrupt associated with TCC #34 Reset Source: edma_rst_mod_g_rst_n
1	I33	W	0h	Interrupt associated with TCC #33 Reset Source: edma_rst_mod_g_rst_n
0	I32	W	0h	Interrupt associated with TCC #32 Reset Source: edma_rst_mod_g_rst_n

4.28.70 TPCC_IEVAL Registers

4.28.70.1 TPCC_IEVAL Register (Offset = 1078h) [reset = 0h]

Short Description: Interrupt Eval R

Long Description: Interrupt Eval Register

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Table 4-4609. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1078h

Figure 4-2184. IEVAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES69															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES69														SET	EVAL
R														W	W
0h														0h	0h

Access Types Legend

Table 4-4610. IEVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RES69	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
1	SET	W	0h	Interrupt Set: CPU write of '1' to the SETn bit causes the tpcc_intN output signal to be pulsed egardless of state of interrupts enable [IERn] and status [IPRn]. CPU write of '0' has no effect. Reset Source: edma_rst_mod_g_rst_n
0	EVAL	W	0h	Interrupt Evaluate: CPU write of '1' to the EVALn bit causes the tpcc_intN output signal to be pulsed if any enabled interrupts [IERn] are still pending [IPRn]. CPU write of '0' has no effect.. Reset Source: edma_rst_mod_g_rst_n

4.28.71 TPCC_QER Registers

4.28.71.1 TPCC_QER Register (Offset = 1080h) [reset = 0h]

Short Description: QDMA Event Regis

Long Description: QDMA Event Register: If QER.En bit is set then the corresponding QDMA channel is prioritized vs. other qdma events for submission to the TC. QER.En bit is set when a vbus write byte matches the address defined in the QCHMAPn register. QER.En bit is cleared when the corresponding event is prioritized and serviced. QER.En is also cleared when user writes a '1' to the QSECR.En bit. If the QER.En bit is already set and a new QDMA event is detected due to user write to QDMA trigger location and QEER register is set then the corresponding bit in the QDMA Event Missed Register is set.

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Table 4-4611. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1080h

Figure 4-2185. QER Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES70															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES70								E7	E6	E5	E4	E3	E2	E1	E0
R								R	R	R	R	R	R	R	R
0h								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4612. QER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES70	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
7	E7	R	0h	Event #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	R	0h	Event #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	R	0h	Event #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	R	0h	Event #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	R	0h	Event #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	R	0h	Event #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	R	0h	Event #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	R	0h	Event #0 Reset Source: edma_rst_mod_g_rst_n

4.28.72 TPCC_QEER Registers

4.28.72.1 TPCC_QEER Register (Offset = 1084h) [reset = 0h]

Short Description: QDMA Event Enabl

Long Description: QDMA Event Enable Register: Enabled/disabled QDMA address comparator for QDMA Channel N. QEER.En is not directly writeable. QDMA channels can be enabled via writes to QEESR and can be disabled via writes to QEECR register. QEER.En = 1 The corresponding QDMA channel comparator is enabled and Events will be recognized and latched in QER.En. QEER.En = 0 The corresponding QDMA channel comparator is disabled. Events will not be recognized/latched in QER.En.

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Table 4-4613. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1084h

Figure 4-2186. QEER Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES71															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES71								E7	E6	E5	E4	E3	E2	E1	E0
R								R	R	R	R	R	R	R	R
0h								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4614. QEER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES71	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
7	E7	R	0h	Event #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	R	0h	Event #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	R	0h	Event #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	R	0h	Event #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	R	0h	Event #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	R	0h	Event #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	R	0h	Event #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	R	0h	Event #0 Reset Source: edma_rst_mod_g_rst_n

4.28.73 TPCC_QEECR Registers

4.28.73.1 TPCC_QEECR Register (Offset = 1088h) [reset = 0h]

Short Description: QDMA Event Enabl

Long Description: QDMA Event Enable Clear Register: CPU write of '1' to the QEECR.En bit causes the QEER.En bit to be cleared. CPU write of '0' has no effect..

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Table 4-4615. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1088h

Figure 4-2187. QEECR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES72															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES72								E7	E6	E5	E4	E3	E2	E1	E0
R								W	W	W	W	W	W	W	W
0h								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4616. QEECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES72	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
7	E7	W	0h	Event #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	W	0h	Event #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	W	0h	Event #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	W	0h	Event #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	W	0h	Event #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	W	0h	Event #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	W	0h	Event #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	W	0h	Event #0 Reset Source: edma_rst_mod_g_rst_n

4.28.74 TPCC_QEESR Registers

4.28.74.1 TPCC_QEESR Register (Offset = 108Ch) [reset = 0h]

Short Description: QDMA Event Enabl

Long Description: QDMA Event Enable Set Register: CPU write of '1' to the QEESR.En bit causes the QEESR.En bit to be set. CPU write of '0' has no effect..

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Table 4-4617. Instance Table

Instance Name	Physical Address
EDMA0	52A0 108Ch

Figure 4-2188. QEESR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES73															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES73								E7	E6	E5	E4	E3	E2	E1	E0
R								W	W	W	W	W	W	W	W
0h								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4618. QEESR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES73	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
7	E7	W	0h	Event #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	W	0h	Event #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	W	0h	Event #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	W	0h	Event #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	W	0h	Event #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	W	0h	Event #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	W	0h	Event #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	W	0h	Event #0 Reset Source: edma_rst_mod_g_rst_n

4.28.75 TPCC_QSER Registers

4.28.75.1 TPCC_QSER Register (Offset = 1090h) [reset = 0h]

Short Description: QDMA Secondary E

Long Description: QDMA Secondary Event Register: The QDMA secondary event register is used along with the QDMA Event Register (QER) to provide information on the state of a QDMA Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

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Table 4-4619. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1090h

Figure 4-2189. QSER Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES74															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES74								E7	E6	E5	E4	E3	E2	E1	E0
R								R	R	R	R	R	R	R	R
0h								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4620. QSER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES74	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
7	E7	R	0h	Event #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	R	0h	Event #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	R	0h	Event #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	R	0h	Event #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	R	0h	Event #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	R	0h	Event #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	R	0h	Event #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	R	0h	Event #0 Reset Source: edma_rst_mod_g_rst_n

4.28.76 TPCC_QSECR Registers

4.28.76.1 TPCC_QSECR Register (Offset = 1094h) [reset = 0h]

Short Description: QDMA Secondary E

Long Description: QDMA Secondary Event Clear Register: The secondary event clear register is used to clear the status of the QSER and QER register (note that this is slightly different than the SER operation which does not clear the ER.En register). CPU write of '1' to the QSECR.En bit clears the QSER.En and QER.En register fields. CPU write of '0' has no effect..

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Table 4-4621. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1094h

Figure 4-2190. QSECR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES75															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES75								E7	E6	E5	E4	E3	E2	E1	E0
R								W	W	W	W	W	W	W	W
0h								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4622. QSECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES75	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
7	E7	W	0h	Event #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	W	0h	Event #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	W	0h	Event #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	W	0h	Event #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	W	0h	Event #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	W	0h	Event #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	W	0h	Event #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	W	0h	Event #0 Reset Source: edma_rst_mod_g_rst_n

4.28.77 TPCC_ER_RN Registers

4.28.77.1 TPCC_RN Register (Offset = 2000h) [reset = 0h]

Short Description: Event Register:

Long Description: Event Register: If ER.En bit is set and the EER.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ER.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EER.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ER.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EER register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECR pseudo-register.

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Table 4-4623. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2000h

Figure 4-2191. ER_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4624. ER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	R	0h	Event #31 Reset Source: edma_rst_mod_g_rst_n
30	E30	R	0h	Event #30 Reset Source: edma_rst_mod_g_rst_n
29	E29	R	0h	Event #29 Reset Source: edma_rst_mod_g_rst_n
28	E28	R	0h	Event #28 Reset Source: edma_rst_mod_g_rst_n
27	E27	R	0h	Event #27 Reset Source: edma_rst_mod_g_rst_n
26	E26	R	0h	Event #26 Reset Source: edma_rst_mod_g_rst_n
25	E25	R	0h	Event #25 Reset Source: edma_rst_mod_g_rst_n
24	E24	R	0h	Event #24 Reset Source: edma_rst_mod_g_rst_n
23	E23	R	0h	Event #23 Reset Source: edma_rst_mod_g_rst_n
22	E22	R	0h	Event #22 Reset Source: edma_rst_mod_g_rst_n
21	E21	R	0h	Event #21 Reset Source: edma_rst_mod_g_rst_n
20	E20	R	0h	Event #20 Reset Source: edma_rst_mod_g_rst_n
19	E19	R	0h	Event #19 Reset Source: edma_rst_mod_g_rst_n
18	E18	R	0h	Event #18 Reset Source: edma_rst_mod_g_rst_n
17	E17	R	0h	Event #17 Reset Source: edma_rst_mod_g_rst_n
16	E16	R	0h	Event #16 Reset Source: edma_rst_mod_g_rst_n
15	E15	R	0h	Event #15 Reset Source: edma_rst_mod_g_rst_n
14	E14	R	0h	Event #14 Reset Source: edma_rst_mod_g_rst_n
13	E13	R	0h	Event #13 Reset Source: edma_rst_mod_g_rst_n

Table 4-4624. ER_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	E12	R	0h	Event #12 Reset Source: edma_rst_mod_g_rst_n
11	E11	R	0h	Event #11 Reset Source: edma_rst_mod_g_rst_n
10	E10	R	0h	Event #10 Reset Source: edma_rst_mod_g_rst_n
9	E9	R	0h	Event #9 Reset Source: edma_rst_mod_g_rst_n
8	E8	R	0h	Event #8 Reset Source: edma_rst_mod_g_rst_n
7	E7	R	0h	Event #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	R	0h	Event #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	R	0h	Event #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	R	0h	Event #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	R	0h	Event #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	R	0h	Event #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	R	0h	Event #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	R	0h	Event #0 Reset Source: edma_rst_mod_g_rst_n

4.28.78 TPCC_ERH_RN Registers

4.28.78.1 TPCC_RN Register (Offset = 2004h) [reset = 0h]

Short Description: Event Register (

Long Description: Event Register (High Part): If ERH.En bit is set and the EERH.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ERH.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EERH.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ERH.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EERH register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECRH pseudo-register.

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Table 4-4625. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2004h

Figure 4-2192. ERH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4626. ERH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	R	0h	Event #63 Reset Source: edma_rst_mod_g_rst_n
30	E62	R	0h	Event #62 Reset Source: edma_rst_mod_g_rst_n
29	E61	R	0h	Event #61 Reset Source: edma_rst_mod_g_rst_n
28	E60	R	0h	Event #60 Reset Source: edma_rst_mod_g_rst_n
27	E59	R	0h	Event #59 Reset Source: edma_rst_mod_g_rst_n
26	E58	R	0h	Event #58 Reset Source: edma_rst_mod_g_rst_n
25	E57	R	0h	Event #57 Reset Source: edma_rst_mod_g_rst_n
24	E56	R	0h	Event #56 Reset Source: edma_rst_mod_g_rst_n
23	E55	R	0h	Event #55 Reset Source: edma_rst_mod_g_rst_n
22	E54	R	0h	Event #54 Reset Source: edma_rst_mod_g_rst_n
21	E53	R	0h	Event #53 Reset Source: edma_rst_mod_g_rst_n
20	E52	R	0h	Event #52 Reset Source: edma_rst_mod_g_rst_n
19	E51	R	0h	Event #51 Reset Source: edma_rst_mod_g_rst_n
18	E50	R	0h	Event #50 Reset Source: edma_rst_mod_g_rst_n
17	E49	R	0h	Event #49 Reset Source: edma_rst_mod_g_rst_n
16	E48	R	0h	Event #48 Reset Source: edma_rst_mod_g_rst_n
15	E47	R	0h	Event #47 Reset Source: edma_rst_mod_g_rst_n
14	E46	R	0h	Event #46 Reset Source: edma_rst_mod_g_rst_n
13	E45	R	0h	Event #45 Reset Source: edma_rst_mod_g_rst_n

Table 4-4626. ERH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	E44	R	0h	Event #44 Reset Source: edma_rst_mod_g_rst_n
11	E43	R	0h	Event #43 Reset Source: edma_rst_mod_g_rst_n
10	E42	R	0h	Event #42 Reset Source: edma_rst_mod_g_rst_n
9	E41	R	0h	Event #41 Reset Source: edma_rst_mod_g_rst_n
8	E40	R	0h	Event #40 Reset Source: edma_rst_mod_g_rst_n
7	E39	R	0h	Event #39 Reset Source: edma_rst_mod_g_rst_n
6	E38	R	0h	Event #38 Reset Source: edma_rst_mod_g_rst_n
5	E37	R	0h	Event #37 Reset Source: edma_rst_mod_g_rst_n
4	E36	R	0h	Event #36 Reset Source: edma_rst_mod_g_rst_n
3	E35	R	0h	Event #35 Reset Source: edma_rst_mod_g_rst_n
2	E34	R	0h	Event #34 Reset Source: edma_rst_mod_g_rst_n
1	E33	R	0h	Event #33 Reset Source: edma_rst_mod_g_rst_n
0	E32	R	0h	Event #32 Reset Source: edma_rst_mod_g_rst_n

4.28.79 TPCC_ECR_RN Registers

4.28.79.1 TPCC_RN Register (Offset = 2008h) [reset = 0h]

Short Description: Event Clear Regi

Long Description: Event Clear Register: CPU write of '1' to the ECR.En bit causes the ER.En bit to be cleared. CPU write of '0' has no effect.

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Table 4-4627. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2008h

Figure 4-2193. ECR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4628. ECR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	W	0h	Event #31 Reset Source: edma_rst_mod_g_rst_n
30	E30	W	0h	Event #30 Reset Source: edma_rst_mod_g_rst_n
29	E29	W	0h	Event #29 Reset Source: edma_rst_mod_g_rst_n
28	E28	W	0h	Event #28 Reset Source: edma_rst_mod_g_rst_n
27	E27	W	0h	Event #27 Reset Source: edma_rst_mod_g_rst_n
26	E26	W	0h	Event #26 Reset Source: edma_rst_mod_g_rst_n
25	E25	W	0h	Event #25 Reset Source: edma_rst_mod_g_rst_n
24	E24	W	0h	Event #24 Reset Source: edma_rst_mod_g_rst_n
23	E23	W	0h	Event #23 Reset Source: edma_rst_mod_g_rst_n
22	E22	W	0h	Event #22 Reset Source: edma_rst_mod_g_rst_n
21	E21	W	0h	Event #21 Reset Source: edma_rst_mod_g_rst_n
20	E20	W	0h	Event #20 Reset Source: edma_rst_mod_g_rst_n
19	E19	W	0h	Event #19 Reset Source: edma_rst_mod_g_rst_n
18	E18	W	0h	Event #18 Reset Source: edma_rst_mod_g_rst_n
17	E17	W	0h	Event #17 Reset Source: edma_rst_mod_g_rst_n
16	E16	W	0h	Event #16 Reset Source: edma_rst_mod_g_rst_n
15	E15	W	0h	Event #15 Reset Source: edma_rst_mod_g_rst_n
14	E14	W	0h	Event #14 Reset Source: edma_rst_mod_g_rst_n
13	E13	W	0h	Event #13 Reset Source: edma_rst_mod_g_rst_n
12	E12	W	0h	Event #12 Reset Source: edma_rst_mod_g_rst_n
11	E11	W	0h	Event #11 Reset Source: edma_rst_mod_g_rst_n
10	E10	W	0h	Event #10 Reset Source: edma_rst_mod_g_rst_n
9	E9	W	0h	Event #9 Reset Source: edma_rst_mod_g_rst_n
8	E8	W	0h	Event #8 Reset Source: edma_rst_mod_g_rst_n

Table 4-4628. ECR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	E7	W	0h	Event #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	W	0h	Event #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	W	0h	Event #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	W	0h	Event #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	W	0h	Event #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	W	0h	Event #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	W	0h	Event #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	W	0h	Event #0 Reset Source: edma_rst_mod_g_rst_n

4.28.80 TPCC_ECRH_RN Registers

4.28.80.1 TPCC_RN Register (Offset = 200Ch) [reset = 0h]

Short Description: Event Clear Regi

Long Description: Event Clear Register (High Part): CPU write of '1' to the ECRH.En bit causes the ERH.En bit to be cleared. CPU write of '0' has no effect.

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Table 4-4629. Instance Table

Instance Name	Physical Address
EDMA0	52A0 200Ch

Figure 4-2194. ECRH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4630. ECRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	W	0h	Event #63 Reset Source: edma_rst_mod_g_rst_n
30	E62	W	0h	Event #62 Reset Source: edma_rst_mod_g_rst_n
29	E61	W	0h	Event #61 Reset Source: edma_rst_mod_g_rst_n
28	E60	W	0h	Event #60 Reset Source: edma_rst_mod_g_rst_n
27	E59	W	0h	Event #59 Reset Source: edma_rst_mod_g_rst_n
26	E58	W	0h	Event #58 Reset Source: edma_rst_mod_g_rst_n
25	E57	W	0h	Event #57 Reset Source: edma_rst_mod_g_rst_n
24	E56	W	0h	Event #56 Reset Source: edma_rst_mod_g_rst_n
23	E55	W	0h	Event #55 Reset Source: edma_rst_mod_g_rst_n
22	E54	W	0h	Event #54 Reset Source: edma_rst_mod_g_rst_n
21	E53	W	0h	Event #53 Reset Source: edma_rst_mod_g_rst_n
20	E52	W	0h	Event #52 Reset Source: edma_rst_mod_g_rst_n
19	E51	W	0h	Event #51 Reset Source: edma_rst_mod_g_rst_n
18	E50	W	0h	Event #50 Reset Source: edma_rst_mod_g_rst_n
17	E49	W	0h	Event #49 Reset Source: edma_rst_mod_g_rst_n
16	E48	W	0h	Event #48 Reset Source: edma_rst_mod_g_rst_n
15	E47	W	0h	Event #47 Reset Source: edma_rst_mod_g_rst_n
14	E46	W	0h	Event #46 Reset Source: edma_rst_mod_g_rst_n
13	E45	W	0h	Event #45 Reset Source: edma_rst_mod_g_rst_n
12	E44	W	0h	Event #44 Reset Source: edma_rst_mod_g_rst_n
11	E43	W	0h	Event #43 Reset Source: edma_rst_mod_g_rst_n
10	E42	W	0h	Event #42 Reset Source: edma_rst_mod_g_rst_n
9	E41	W	0h	Event #41 Reset Source: edma_rst_mod_g_rst_n
8	E40	W	0h	Event #40 Reset Source: edma_rst_mod_g_rst_n

Table 4-4630. ECRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	E39	W	0h	Event #39 Reset Source: edma_rst_mod_g_rst_n
6	E38	W	0h	Event #38 Reset Source: edma_rst_mod_g_rst_n
5	E37	W	0h	Event #37 Reset Source: edma_rst_mod_g_rst_n
4	E36	W	0h	Event #36 Reset Source: edma_rst_mod_g_rst_n
3	E35	W	0h	Event #35 Reset Source: edma_rst_mod_g_rst_n
2	E34	W	0h	Event #34 Reset Source: edma_rst_mod_g_rst_n
1	E33	W	0h	Event #33 Reset Source: edma_rst_mod_g_rst_n
0	E32	W	0h	Event #32 Reset Source: edma_rst_mod_g_rst_n

4.28.81 TPCC_ESR_RN Registers

4.28.81.1 TPCC_RN Register (Offset = 2010h) [reset = 0h]

Short Description: Event Set Regist

Long Description: Event Set Register: CPU write of '1' to the ESR.En bit causes the ER.En bit to be set. CPU write of '0' has no effect.

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Table 4-4631. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2010h

Figure 4-2195. ESR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4632. ESR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	W	0h	Event #31 Reset Source: edma_rst_mod_g_rst_n
30	E30	W	0h	Event #30 Reset Source: edma_rst_mod_g_rst_n
29	E29	W	0h	Event #29 Reset Source: edma_rst_mod_g_rst_n
28	E28	W	0h	Event #28 Reset Source: edma_rst_mod_g_rst_n
27	E27	W	0h	Event #27 Reset Source: edma_rst_mod_g_rst_n
26	E26	W	0h	Event #26 Reset Source: edma_rst_mod_g_rst_n
25	E25	W	0h	Event #25 Reset Source: edma_rst_mod_g_rst_n
24	E24	W	0h	Event #24 Reset Source: edma_rst_mod_g_rst_n
23	E23	W	0h	Event #23 Reset Source: edma_rst_mod_g_rst_n
22	E22	W	0h	Event #22 Reset Source: edma_rst_mod_g_rst_n
21	E21	W	0h	Event #21 Reset Source: edma_rst_mod_g_rst_n
20	E20	W	0h	Event #20 Reset Source: edma_rst_mod_g_rst_n
19	E19	W	0h	Event #19 Reset Source: edma_rst_mod_g_rst_n
18	E18	W	0h	Event #18 Reset Source: edma_rst_mod_g_rst_n
17	E17	W	0h	Event #17 Reset Source: edma_rst_mod_g_rst_n
16	E16	W	0h	Event #16 Reset Source: edma_rst_mod_g_rst_n
15	E15	W	0h	Event #15 Reset Source: edma_rst_mod_g_rst_n
14	E14	W	0h	Event #14 Reset Source: edma_rst_mod_g_rst_n
13	E13	W	0h	Event #13 Reset Source: edma_rst_mod_g_rst_n
12	E12	W	0h	Event #12 Reset Source: edma_rst_mod_g_rst_n
11	E11	W	0h	Event #11 Reset Source: edma_rst_mod_g_rst_n
10	E10	W	0h	Event #10 Reset Source: edma_rst_mod_g_rst_n
9	E9	W	0h	Event #9 Reset Source: edma_rst_mod_g_rst_n
8	E8	W	0h	Event #8 Reset Source: edma_rst_mod_g_rst_n

Table 4-4632. ESR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	E7	W	0h	Event #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	W	0h	Event #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	W	0h	Event #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	W	0h	Event #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	W	0h	Event #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	W	0h	Event #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	W	0h	Event #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	W	0h	Event #0 Reset Source: edma_rst_mod_g_rst_n

4.28.82 TPCC_ESRH_RN Registers

4.28.82.1 TPCC_RN Register (Offset = 2014h) [reset = 0h]

Short Description: Event Set Regist

Long Description: Event Set Register (High Part) CPU write of '1' to the ESRH.En bit causes the ERH.En bit to be set. CPU write of '0' has no effect.

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Table 4-4633. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2014h

Figure 4-2196. ESRH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4634. ESRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	W	0h	Event #63 Reset Source: edma_rst_mod_g_rst_n
30	E62	W	0h	Event #62 Reset Source: edma_rst_mod_g_rst_n
29	E61	W	0h	Event #61 Reset Source: edma_rst_mod_g_rst_n
28	E60	W	0h	Event #60 Reset Source: edma_rst_mod_g_rst_n
27	E59	W	0h	Event #59 Reset Source: edma_rst_mod_g_rst_n
26	E58	W	0h	Event #58 Reset Source: edma_rst_mod_g_rst_n
25	E57	W	0h	Event #57 Reset Source: edma_rst_mod_g_rst_n
24	E56	W	0h	Event #56 Reset Source: edma_rst_mod_g_rst_n
23	E55	W	0h	Event #55 Reset Source: edma_rst_mod_g_rst_n
22	E54	W	0h	Event #54 Reset Source: edma_rst_mod_g_rst_n
21	E53	W	0h	Event #53 Reset Source: edma_rst_mod_g_rst_n
20	E52	W	0h	Event #52 Reset Source: edma_rst_mod_g_rst_n
19	E51	W	0h	Event #51 Reset Source: edma_rst_mod_g_rst_n
18	E50	W	0h	Event #50 Reset Source: edma_rst_mod_g_rst_n
17	E49	W	0h	Event #49 Reset Source: edma_rst_mod_g_rst_n
16	E48	W	0h	Event #48 Reset Source: edma_rst_mod_g_rst_n
15	E47	W	0h	Event #47 Reset Source: edma_rst_mod_g_rst_n
14	E46	W	0h	Event #46 Reset Source: edma_rst_mod_g_rst_n
13	E45	W	0h	Event #45 Reset Source: edma_rst_mod_g_rst_n
12	E44	W	0h	Event #44 Reset Source: edma_rst_mod_g_rst_n
11	E43	W	0h	Event #43 Reset Source: edma_rst_mod_g_rst_n
10	E42	W	0h	Event #42 Reset Source: edma_rst_mod_g_rst_n
9	E41	W	0h	Event #41 Reset Source: edma_rst_mod_g_rst_n
8	E40	W	0h	Event #40 Reset Source: edma_rst_mod_g_rst_n

Table 4-4634. ESRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	E39	W	0h	Event #39 Reset Source: edma_rst_mod_g_rst_n
6	E38	W	0h	Event #38 Reset Source: edma_rst_mod_g_rst_n
5	E37	W	0h	Event #37 Reset Source: edma_rst_mod_g_rst_n
4	E36	W	0h	Event #36 Reset Source: edma_rst_mod_g_rst_n
3	E35	W	0h	Event #35 Reset Source: edma_rst_mod_g_rst_n
2	E34	W	0h	Event #34 Reset Source: edma_rst_mod_g_rst_n
1	E33	W	0h	Event #33 Reset Source: edma_rst_mod_g_rst_n
0	E32	W	0h	Event #32 Reset Source: edma_rst_mod_g_rst_n

4.28.83 TPCC_CER_RN Registers

4.28.83.1 TPCC_RN Register (Offset = 2018h) [reset = 0h]

Short Description: Chained Event Re

Long Description: Chained Event Register: If CER.En bit is set (regardless of state of EER.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CER.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CER.En bit is cleared when the corresponding event is prioritized and serviced. If the CER.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CER.En cannot be set or cleared via software.

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Table 4-4635. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2018h

Figure 4-2197. CER_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4636. CER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	R	0h	Event #31 Reset Source: edma_rst_mod_g_rst_n
30	E30	R	0h	Event #30 Reset Source: edma_rst_mod_g_rst_n
29	E29	R	0h	Event #29 Reset Source: edma_rst_mod_g_rst_n
28	E28	R	0h	Event #28 Reset Source: edma_rst_mod_g_rst_n
27	E27	R	0h	Event #27 Reset Source: edma_rst_mod_g_rst_n
26	E26	R	0h	Event #26 Reset Source: edma_rst_mod_g_rst_n
25	E25	R	0h	Event #25 Reset Source: edma_rst_mod_g_rst_n
24	E24	R	0h	Event #24 Reset Source: edma_rst_mod_g_rst_n
23	E23	R	0h	Event #23 Reset Source: edma_rst_mod_g_rst_n
22	E22	R	0h	Event #22 Reset Source: edma_rst_mod_g_rst_n
21	E21	R	0h	Event #21 Reset Source: edma_rst_mod_g_rst_n
20	E20	R	0h	Event #20 Reset Source: edma_rst_mod_g_rst_n
19	E19	R	0h	Event #19 Reset Source: edma_rst_mod_g_rst_n
18	E18	R	0h	Event #18 Reset Source: edma_rst_mod_g_rst_n
17	E17	R	0h	Event #17 Reset Source: edma_rst_mod_g_rst_n
16	E16	R	0h	Event #16 Reset Source: edma_rst_mod_g_rst_n
15	E15	R	0h	Event #15 Reset Source: edma_rst_mod_g_rst_n
14	E14	R	0h	Event #14 Reset Source: edma_rst_mod_g_rst_n
13	E13	R	0h	Event #13 Reset Source: edma_rst_mod_g_rst_n

Table 4-4636. CER_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	E12	R	0h	Event #12 Reset Source: edma_rst_mod_g_rst_n
11	E11	R	0h	Event #11 Reset Source: edma_rst_mod_g_rst_n
10	E10	R	0h	Event #10 Reset Source: edma_rst_mod_g_rst_n
9	E9	R	0h	Event #9 Reset Source: edma_rst_mod_g_rst_n
8	E8	R	0h	Event #8 Reset Source: edma_rst_mod_g_rst_n
7	E7	R	0h	Event #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	R	0h	Event #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	R	0h	Event #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	R	0h	Event #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	R	0h	Event #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	R	0h	Event #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	R	0h	Event #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	R	0h	Event #0 Reset Source: edma_rst_mod_g_rst_n

4.28.84 TPCC_CERH_RN Registers

4.28.84.1 TPCC_RN Register (Offset = 201Ch) [reset = 0h]

Short Description: Chained Event Re

Long Description: Chained Event Register (High Part): If CERH.En bit is set (regardless of state of EERH.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CERH.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CERH.En bit is cleared when the corresponding event is prioritized and serviced. If the CERH.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CERH.En cannot be set or cleared via software.

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Table 4-4637. Instance Table

Instance Name	Physical Address
EDMA0	52A0 201Ch

Figure 4-2198. CERH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4638. CERH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	R	0h	Event #63 Reset Source: edma_rst_mod_g_rst_n
30	E62	R	0h	Event #62 Reset Source: edma_rst_mod_g_rst_n
29	E61	R	0h	Event #61 Reset Source: edma_rst_mod_g_rst_n
28	E60	R	0h	Event #60 Reset Source: edma_rst_mod_g_rst_n
27	E59	R	0h	Event #59 Reset Source: edma_rst_mod_g_rst_n
26	E58	R	0h	Event #58 Reset Source: edma_rst_mod_g_rst_n
25	E57	R	0h	Event #57 Reset Source: edma_rst_mod_g_rst_n
24	E56	R	0h	Event #56 Reset Source: edma_rst_mod_g_rst_n
23	E55	R	0h	Event #55 Reset Source: edma_rst_mod_g_rst_n
22	E54	R	0h	Event #54 Reset Source: edma_rst_mod_g_rst_n
21	E53	R	0h	Event #53 Reset Source: edma_rst_mod_g_rst_n
20	E52	R	0h	Event #52 Reset Source: edma_rst_mod_g_rst_n
19	E51	R	0h	Event #51 Reset Source: edma_rst_mod_g_rst_n
18	E50	R	0h	Event #50 Reset Source: edma_rst_mod_g_rst_n
17	E49	R	0h	Event #49 Reset Source: edma_rst_mod_g_rst_n
16	E48	R	0h	Event #48 Reset Source: edma_rst_mod_g_rst_n
15	E47	R	0h	Event #47 Reset Source: edma_rst_mod_g_rst_n
14	E46	R	0h	Event #46 Reset Source: edma_rst_mod_g_rst_n
13	E45	R	0h	Event #45 Reset Source: edma_rst_mod_g_rst_n

Table 4-4638. CERH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	E44	R	0h	Event #44 Reset Source: edma_rst_mod_g_rst_n
11	E43	R	0h	Event #43 Reset Source: edma_rst_mod_g_rst_n
10	E42	R	0h	Event #42 Reset Source: edma_rst_mod_g_rst_n
9	E41	R	0h	Event #41 Reset Source: edma_rst_mod_g_rst_n
8	E40	R	0h	Event #40 Reset Source: edma_rst_mod_g_rst_n
7	E39	R	0h	Event #39 Reset Source: edma_rst_mod_g_rst_n
6	E38	R	0h	Event #38 Reset Source: edma_rst_mod_g_rst_n
5	E37	R	0h	Event #37 Reset Source: edma_rst_mod_g_rst_n
4	E36	R	0h	Event #36 Reset Source: edma_rst_mod_g_rst_n
3	E35	R	0h	Event #35 Reset Source: edma_rst_mod_g_rst_n
2	E34	R	0h	Event #34 Reset Source: edma_rst_mod_g_rst_n
1	E33	R	0h	Event #33 Reset Source: edma_rst_mod_g_rst_n
0	E32	R	0h	Event #32 Reset Source: edma_rst_mod_g_rst_n

4.28.85 TPCC_EER_RN Registers

4.28.85.1 TPCC_RN Register (Offset = 2020h) [reset = 0h]

Short Description: Event Enable Reg

Long Description: Event Enable Register: Enables DMA transfers for ER.En pending events. ER.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CER) or Event Set Register (ESR). Note that if a bit is set in ER.En while EER.En is disabled no action is taken. If EER.En is enabled at a later point (and ER.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EER.En is not directly writeable. Events can be enabled via writes to EESR and can be disabled via writes to EECR register. EER.En = 0: ER.En is not enabled to trigger DMA transfers. EER.En = 1: ER.En is enabled to trigger DMA transfers.

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Table 4-4639. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2020h

Figure 4-2199. EER_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4640. EER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	R	0h	Event #31 Reset Source: edma_rst_mod_g_rst_n
30	E30	R	0h	Event #30 Reset Source: edma_rst_mod_g_rst_n
29	E29	R	0h	Event #29 Reset Source: edma_rst_mod_g_rst_n
28	E28	R	0h	Event #28 Reset Source: edma_rst_mod_g_rst_n
27	E27	R	0h	Event #27 Reset Source: edma_rst_mod_g_rst_n
26	E26	R	0h	Event #26 Reset Source: edma_rst_mod_g_rst_n
25	E25	R	0h	Event #25 Reset Source: edma_rst_mod_g_rst_n
24	E24	R	0h	Event #24 Reset Source: edma_rst_mod_g_rst_n
23	E23	R	0h	Event #23 Reset Source: edma_rst_mod_g_rst_n
22	E22	R	0h	Event #22 Reset Source: edma_rst_mod_g_rst_n
21	E21	R	0h	Event #21 Reset Source: edma_rst_mod_g_rst_n
20	E20	R	0h	Event #20 Reset Source: edma_rst_mod_g_rst_n
19	E19	R	0h	Event #19 Reset Source: edma_rst_mod_g_rst_n
18	E18	R	0h	Event #18 Reset Source: edma_rst_mod_g_rst_n
17	E17	R	0h	Event #17 Reset Source: edma_rst_mod_g_rst_n
16	E16	R	0h	Event #16 Reset Source: edma_rst_mod_g_rst_n
15	E15	R	0h	Event #15 Reset Source: edma_rst_mod_g_rst_n
14	E14	R	0h	Event #14 Reset Source: edma_rst_mod_g_rst_n
13	E13	R	0h	Event #13 Reset Source: edma_rst_mod_g_rst_n

Table 4-4640. EER_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	E12	R	0h	Event #12 Reset Source: edma_rst_mod_g_rst_n
11	E11	R	0h	Event #11 Reset Source: edma_rst_mod_g_rst_n
10	E10	R	0h	Event #10 Reset Source: edma_rst_mod_g_rst_n
9	E9	R	0h	Event #9 Reset Source: edma_rst_mod_g_rst_n
8	E8	R	0h	Event #8 Reset Source: edma_rst_mod_g_rst_n
7	E7	R	0h	Event #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	R	0h	Event #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	R	0h	Event #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	R	0h	Event #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	R	0h	Event #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	R	0h	Event #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	R	0h	Event #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	R	0h	Event #0 Reset Source: edma_rst_mod_g_rst_n

4.28.86 TPCC_EERH_RN Registers

4.28.86.1 TPCC_RN Register (Offset = 2024h) [reset = 0h]

Short Description: Event Enable Reg

Long Description: Event Enable Register (High Part): Enables DMA transfers for ERH.En pending events. ERH.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CERH) or Event Set Register (ESRH). Note that if a bit is set in ERH.En while EERH.En is disabled no action is taken. If EERH.En is enabled at a later point (and ERH.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EERH.En is not directly writeable. Events can be enabled via writes to EESRH and can be disabled via writes to EECRH register. EERH.En = 0: ER.En is not enabled to trigger DMA transfers. EERH.En = 1: ER.En is enabled to trigger DMA transfers.

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Table 4-4641. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2024h

Figure 4-2200. EERH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4642. EERH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	R	0h	Event #63 Reset Source: edma_rst_mod_g_rst_n
30	E62	R	0h	Event #62 Reset Source: edma_rst_mod_g_rst_n
29	E61	R	0h	Event #61 Reset Source: edma_rst_mod_g_rst_n
28	E60	R	0h	Event #60 Reset Source: edma_rst_mod_g_rst_n
27	E59	R	0h	Event #59 Reset Source: edma_rst_mod_g_rst_n
26	E58	R	0h	Event #58 Reset Source: edma_rst_mod_g_rst_n
25	E57	R	0h	Event #57 Reset Source: edma_rst_mod_g_rst_n
24	E56	R	0h	Event #56 Reset Source: edma_rst_mod_g_rst_n
23	E55	R	0h	Event #55 Reset Source: edma_rst_mod_g_rst_n
22	E54	R	0h	Event #54 Reset Source: edma_rst_mod_g_rst_n
21	E53	R	0h	Event #53 Reset Source: edma_rst_mod_g_rst_n
20	E52	R	0h	Event #52 Reset Source: edma_rst_mod_g_rst_n
19	E51	R	0h	Event #51 Reset Source: edma_rst_mod_g_rst_n
18	E50	R	0h	Event #50 Reset Source: edma_rst_mod_g_rst_n
17	E49	R	0h	Event #49 Reset Source: edma_rst_mod_g_rst_n
16	E48	R	0h	Event #48 Reset Source: edma_rst_mod_g_rst_n
15	E47	R	0h	Event #47 Reset Source: edma_rst_mod_g_rst_n
14	E46	R	0h	Event #46 Reset Source: edma_rst_mod_g_rst_n
13	E45	R	0h	Event #45 Reset Source: edma_rst_mod_g_rst_n

Table 4-4642. EERH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	E44	R	0h	Event #44 Reset Source: edma_rst_mod_g_rst_n
11	E43	R	0h	Event #43 Reset Source: edma_rst_mod_g_rst_n
10	E42	R	0h	Event #42 Reset Source: edma_rst_mod_g_rst_n
9	E41	R	0h	Event #41 Reset Source: edma_rst_mod_g_rst_n
8	E40	R	0h	Event #40 Reset Source: edma_rst_mod_g_rst_n
7	E39	R	0h	Event #39 Reset Source: edma_rst_mod_g_rst_n
6	E38	R	0h	Event #38 Reset Source: edma_rst_mod_g_rst_n
5	E37	R	0h	Event #37 Reset Source: edma_rst_mod_g_rst_n
4	E36	R	0h	Event #36 Reset Source: edma_rst_mod_g_rst_n
3	E35	R	0h	Event #35 Reset Source: edma_rst_mod_g_rst_n
2	E34	R	0h	Event #34 Reset Source: edma_rst_mod_g_rst_n
1	E33	R	0h	Event #33 Reset Source: edma_rst_mod_g_rst_n
0	E32	R	0h	Event #32 Reset Source: edma_rst_mod_g_rst_n

4.28.87 TPCC_EECR_RN Registers

4.28.87.1 TPCC_RN Register (Offset = 2028h) [reset = 0h]

Short Description: Event Enable Cle

Long Description: Event Enable Clear Register: CPU write of '1' to the EECR.En bit causes the EER.En bit to be cleared. CPU write of '0' has no effect..

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Table 4-4643. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2028h

Figure 4-2201. EECR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4644. EECR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	W	0h	Event #31 Reset Source: edma_rst_mod_g_rst_n
30	E30	W	0h	Event #30 Reset Source: edma_rst_mod_g_rst_n
29	E29	W	0h	Event #29 Reset Source: edma_rst_mod_g_rst_n
28	E28	W	0h	Event #28 Reset Source: edma_rst_mod_g_rst_n
27	E27	W	0h	Event #27 Reset Source: edma_rst_mod_g_rst_n
26	E26	W	0h	Event #26 Reset Source: edma_rst_mod_g_rst_n
25	E25	W	0h	Event #25 Reset Source: edma_rst_mod_g_rst_n
24	E24	W	0h	Event #24 Reset Source: edma_rst_mod_g_rst_n
23	E23	W	0h	Event #23 Reset Source: edma_rst_mod_g_rst_n
22	E22	W	0h	Event #22 Reset Source: edma_rst_mod_g_rst_n
21	E21	W	0h	Event #21 Reset Source: edma_rst_mod_g_rst_n
20	E20	W	0h	Event #20 Reset Source: edma_rst_mod_g_rst_n
19	E19	W	0h	Event #19 Reset Source: edma_rst_mod_g_rst_n
18	E18	W	0h	Event #18 Reset Source: edma_rst_mod_g_rst_n
17	E17	W	0h	Event #17 Reset Source: edma_rst_mod_g_rst_n
16	E16	W	0h	Event #16 Reset Source: edma_rst_mod_g_rst_n
15	E15	W	0h	Event #15 Reset Source: edma_rst_mod_g_rst_n
14	E14	W	0h	Event #14 Reset Source: edma_rst_mod_g_rst_n
13	E13	W	0h	Event #13 Reset Source: edma_rst_mod_g_rst_n
12	E12	W	0h	Event #12 Reset Source: edma_rst_mod_g_rst_n
11	E11	W	0h	Event #11 Reset Source: edma_rst_mod_g_rst_n
10	E10	W	0h	Event #10 Reset Source: edma_rst_mod_g_rst_n
9	E9	W	0h	Event #9 Reset Source: edma_rst_mod_g_rst_n
8	E8	W	0h	Event #8 Reset Source: edma_rst_mod_g_rst_n

Table 4-4644. EECR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	E7	W	0h	Event #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	W	0h	Event #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	W	0h	Event #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	W	0h	Event #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	W	0h	Event #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	W	0h	Event #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	W	0h	Event #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	W	0h	Event #0 Reset Source: edma_rst_mod_g_rst_n

4.28.88 TPCC_EECRH_RN Registers

4.28.88.1 TPCC_RN Register (Offset = 202Ch) [reset = 0h]

Short Description: Event Enable Cle

Long Description: Event Enable Clear Register (High Part): CPU write of '1' to the EECRH.En bit causes the EERH.En bit to be cleared. CPU write of '0' has no effect..

Return to Summary Table

Table 4-4645. Instance Table

Instance Name	Physical Address
EDMA0	52A0 202Ch

Figure 4-2202. EECRH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4646. EECRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	W	0h	Event #63 Reset Source: edma_rst_mod_g_rst_n
30	E62	W	0h	Event #62 Reset Source: edma_rst_mod_g_rst_n
29	E61	W	0h	Event #61 Reset Source: edma_rst_mod_g_rst_n
28	E60	W	0h	Event #60 Reset Source: edma_rst_mod_g_rst_n
27	E59	W	0h	Event #59 Reset Source: edma_rst_mod_g_rst_n
26	E58	W	0h	Event #58 Reset Source: edma_rst_mod_g_rst_n
25	E57	W	0h	Event #57 Reset Source: edma_rst_mod_g_rst_n
24	E56	W	0h	Event #56 Reset Source: edma_rst_mod_g_rst_n
23	E55	W	0h	Event #55 Reset Source: edma_rst_mod_g_rst_n
22	E54	W	0h	Event #54 Reset Source: edma_rst_mod_g_rst_n
21	E53	W	0h	Event #53 Reset Source: edma_rst_mod_g_rst_n
20	E52	W	0h	Event #52 Reset Source: edma_rst_mod_g_rst_n
19	E51	W	0h	Event #51 Reset Source: edma_rst_mod_g_rst_n
18	E50	W	0h	Event #50 Reset Source: edma_rst_mod_g_rst_n
17	E49	W	0h	Event #49 Reset Source: edma_rst_mod_g_rst_n
16	E48	W	0h	Event #48 Reset Source: edma_rst_mod_g_rst_n
15	E47	W	0h	Event #47 Reset Source: edma_rst_mod_g_rst_n
14	E46	W	0h	Event #46 Reset Source: edma_rst_mod_g_rst_n
13	E45	W	0h	Event #45 Reset Source: edma_rst_mod_g_rst_n
12	E44	W	0h	Event #44 Reset Source: edma_rst_mod_g_rst_n
11	E43	W	0h	Event #43 Reset Source: edma_rst_mod_g_rst_n
10	E42	W	0h	Event #42 Reset Source: edma_rst_mod_g_rst_n
9	E41	W	0h	Event #41 Reset Source: edma_rst_mod_g_rst_n
8	E40	W	0h	Event #40 Reset Source: edma_rst_mod_g_rst_n

Table 4-4646. EECRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	E39	W	0h	Event #39 Reset Source: edma_rst_mod_g_rst_n
6	E38	W	0h	Event #38 Reset Source: edma_rst_mod_g_rst_n
5	E37	W	0h	Event #37 Reset Source: edma_rst_mod_g_rst_n
4	E36	W	0h	Event #36 Reset Source: edma_rst_mod_g_rst_n
3	E35	W	0h	Event #35 Reset Source: edma_rst_mod_g_rst_n
2	E34	W	0h	Event #34 Reset Source: edma_rst_mod_g_rst_n
1	E33	W	0h	Event #33 Reset Source: edma_rst_mod_g_rst_n
0	E32	W	0h	Event #32 Reset Source: edma_rst_mod_g_rst_n

4.28.89 TPCC_EESR_RN Registers

4.28.89.1 TPCC_RN Register (Offset = 2030h) [reset = 0h]

Short Description: Event Enable Set

Long Description: Event Enable Set Register: CPU write of '1' to the EESR.En bit causes the EER.En bit to be set. CPU write of '0' has no effect..

Return to Summary Table

Table 4-4647. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2030h

Figure 4-2203. EESR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4648. EESR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	W	0h	Event #31 Reset Source: edma_rst_mod_g_rst_n
30	E30	W	0h	Event #30 Reset Source: edma_rst_mod_g_rst_n
29	E29	W	0h	Event #29 Reset Source: edma_rst_mod_g_rst_n
28	E28	W	0h	Event #28 Reset Source: edma_rst_mod_g_rst_n
27	E27	W	0h	Event #27 Reset Source: edma_rst_mod_g_rst_n
26	E26	W	0h	Event #26 Reset Source: edma_rst_mod_g_rst_n
25	E25	W	0h	Event #25 Reset Source: edma_rst_mod_g_rst_n
24	E24	W	0h	Event #24 Reset Source: edma_rst_mod_g_rst_n
23	E23	W	0h	Event #23 Reset Source: edma_rst_mod_g_rst_n
22	E22	W	0h	Event #22 Reset Source: edma_rst_mod_g_rst_n
21	E21	W	0h	Event #21 Reset Source: edma_rst_mod_g_rst_n
20	E20	W	0h	Event #20 Reset Source: edma_rst_mod_g_rst_n
19	E19	W	0h	Event #19 Reset Source: edma_rst_mod_g_rst_n
18	E18	W	0h	Event #18 Reset Source: edma_rst_mod_g_rst_n
17	E17	W	0h	Event #17 Reset Source: edma_rst_mod_g_rst_n
16	E16	W	0h	Event #16 Reset Source: edma_rst_mod_g_rst_n
15	E15	W	0h	Event #15 Reset Source: edma_rst_mod_g_rst_n
14	E14	W	0h	Event #14 Reset Source: edma_rst_mod_g_rst_n
13	E13	W	0h	Event #13 Reset Source: edma_rst_mod_g_rst_n
12	E12	W	0h	Event #12 Reset Source: edma_rst_mod_g_rst_n
11	E11	W	0h	Event #11 Reset Source: edma_rst_mod_g_rst_n
10	E10	W	0h	Event #10 Reset Source: edma_rst_mod_g_rst_n
9	E9	W	0h	Event #9 Reset Source: edma_rst_mod_g_rst_n
8	E8	W	0h	Event #8 Reset Source: edma_rst_mod_g_rst_n

Table 4-4648. EESR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	E7	W	0h	Event #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	W	0h	Event #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	W	0h	Event #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	W	0h	Event #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	W	0h	Event #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	W	0h	Event #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	W	0h	Event #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	W	0h	Event #0 Reset Source: edma_rst_mod_g_rst_n

4.28.90 TPCC_EESRH_RN Registers

4.28.90.1 TPCC_RN Register (Offset = 2034h) [reset = 0h]

Short Description: Event Enable Set

Long Description: Event Enable Set Register (High Part): CPU write of '1' to the EESRH.En bit causes the EERH.En bit to be set. CPU write of '0' has no effect..

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Table 4-4649. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2034h

Figure 4-2204. EESRH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4650. EESRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	W	0h	Event #63 Reset Source: edma_rst_mod_g_rst_n
30	E62	W	0h	Event #62 Reset Source: edma_rst_mod_g_rst_n
29	E61	W	0h	Event #61 Reset Source: edma_rst_mod_g_rst_n
28	E60	W	0h	Event #60 Reset Source: edma_rst_mod_g_rst_n
27	E59	W	0h	Event #59 Reset Source: edma_rst_mod_g_rst_n
26	E58	W	0h	Event #58 Reset Source: edma_rst_mod_g_rst_n
25	E57	W	0h	Event #57 Reset Source: edma_rst_mod_g_rst_n
24	E56	W	0h	Event #56 Reset Source: edma_rst_mod_g_rst_n
23	E55	W	0h	Event #55 Reset Source: edma_rst_mod_g_rst_n
22	E54	W	0h	Event #54 Reset Source: edma_rst_mod_g_rst_n
21	E53	W	0h	Event #53 Reset Source: edma_rst_mod_g_rst_n
20	E52	W	0h	Event #52 Reset Source: edma_rst_mod_g_rst_n
19	E51	W	0h	Event #51 Reset Source: edma_rst_mod_g_rst_n
18	E50	W	0h	Event #50 Reset Source: edma_rst_mod_g_rst_n
17	E49	W	0h	Event #49 Reset Source: edma_rst_mod_g_rst_n
16	E48	W	0h	Event #48 Reset Source: edma_rst_mod_g_rst_n
15	E47	W	0h	Event #47 Reset Source: edma_rst_mod_g_rst_n
14	E46	W	0h	Event #46 Reset Source: edma_rst_mod_g_rst_n
13	E45	W	0h	Event #45 Reset Source: edma_rst_mod_g_rst_n
12	E44	W	0h	Event #44 Reset Source: edma_rst_mod_g_rst_n
11	E43	W	0h	Event #43 Reset Source: edma_rst_mod_g_rst_n
10	E42	W	0h	Event #42 Reset Source: edma_rst_mod_g_rst_n
9	E41	W	0h	Event #41 Reset Source: edma_rst_mod_g_rst_n
8	E40	W	0h	Event #40 Reset Source: edma_rst_mod_g_rst_n

Table 4-4650. EESRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	E39	W	0h	Event #39 Reset Source: edma_rst_mod_g_rst_n
6	E38	W	0h	Event #38 Reset Source: edma_rst_mod_g_rst_n
5	E37	W	0h	Event #37 Reset Source: edma_rst_mod_g_rst_n
4	E36	W	0h	Event #36 Reset Source: edma_rst_mod_g_rst_n
3	E35	W	0h	Event #35 Reset Source: edma_rst_mod_g_rst_n
2	E34	W	0h	Event #34 Reset Source: edma_rst_mod_g_rst_n
1	E33	W	0h	Event #33 Reset Source: edma_rst_mod_g_rst_n
0	E32	W	0h	Event #32 Reset Source: edma_rst_mod_g_rst_n

4.28.91 TPCC_SER_RN Registers

4.28.91.1 TPCC_RN Register (Offset = 2038h) [reset = 0h]

Short Description: Secondary Event

Long Description: Secondary Event Register: The secondary event register is used along with the Event Register (ER) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

Return to Summary Table

Table 4-4651. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2038h

Figure 4-2205. SER_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4652. SER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	R	0h	Event #31 Reset Source: edma_rst_mod_g_rst_n
30	E30	R	0h	Event #30 Reset Source: edma_rst_mod_g_rst_n
29	E29	R	0h	Event #29 Reset Source: edma_rst_mod_g_rst_n
28	E28	R	0h	Event #28 Reset Source: edma_rst_mod_g_rst_n
27	E27	R	0h	Event #27 Reset Source: edma_rst_mod_g_rst_n
26	E26	R	0h	Event #26 Reset Source: edma_rst_mod_g_rst_n
25	E25	R	0h	Event #25 Reset Source: edma_rst_mod_g_rst_n
24	E24	R	0h	Event #24 Reset Source: edma_rst_mod_g_rst_n
23	E23	R	0h	Event #23 Reset Source: edma_rst_mod_g_rst_n
22	E22	R	0h	Event #22 Reset Source: edma_rst_mod_g_rst_n
21	E21	R	0h	Event #21 Reset Source: edma_rst_mod_g_rst_n
20	E20	R	0h	Event #20 Reset Source: edma_rst_mod_g_rst_n
19	E19	R	0h	Event #19 Reset Source: edma_rst_mod_g_rst_n
18	E18	R	0h	Event #18 Reset Source: edma_rst_mod_g_rst_n
17	E17	R	0h	Event #17 Reset Source: edma_rst_mod_g_rst_n
16	E16	R	0h	Event #16 Reset Source: edma_rst_mod_g_rst_n
15	E15	R	0h	Event #15 Reset Source: edma_rst_mod_g_rst_n
14	E14	R	0h	Event #14 Reset Source: edma_rst_mod_g_rst_n
13	E13	R	0h	Event #13 Reset Source: edma_rst_mod_g_rst_n
12	E12	R	0h	Event #12 Reset Source: edma_rst_mod_g_rst_n
11	E11	R	0h	Event #11 Reset Source: edma_rst_mod_g_rst_n
10	E10	R	0h	Event #10 Reset Source: edma_rst_mod_g_rst_n
9	E9	R	0h	Event #9 Reset Source: edma_rst_mod_g_rst_n

Table 4-4652. SER_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	E8	R	0h	Event #8 Reset Source: edma_rst_mod_g_rst_n
7	E7	R	0h	Event #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	R	0h	Event #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	R	0h	Event #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	R	0h	Event #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	R	0h	Event #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	R	0h	Event #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	R	0h	Event #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	R	0h	Event #0 Reset Source: edma_rst_mod_g_rst_n

4.28.92 TPCC_SERH_RN Registers

4.28.92.1 TPCC_RN Register (Offset = 203Ch) [reset = 0h]

Short Description: Secondary Event

Long Description: Secondary Event Register (High Part): The secondary event register is used along with the Event Register (ERH) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

Return to Summary Table

Table 4-4653. Instance Table

Instance Name	Physical Address
EDMA0	52A0 203Ch

Figure 4-2206. SERH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4654. SERH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	R	0h	Event #63 Reset Source: edma_rst_mod_g_rst_n
30	E62	R	0h	Event #62 Reset Source: edma_rst_mod_g_rst_n
29	E61	R	0h	Event #61 Reset Source: edma_rst_mod_g_rst_n
28	E60	R	0h	Event #60 Reset Source: edma_rst_mod_g_rst_n
27	E59	R	0h	Event #59 Reset Source: edma_rst_mod_g_rst_n
26	E58	R	0h	Event #58 Reset Source: edma_rst_mod_g_rst_n
25	E57	R	0h	Event #57 Reset Source: edma_rst_mod_g_rst_n
24	E56	R	0h	Event #56 Reset Source: edma_rst_mod_g_rst_n
23	E55	R	0h	Event #55 Reset Source: edma_rst_mod_g_rst_n
22	E54	R	0h	Event #54 Reset Source: edma_rst_mod_g_rst_n
21	E53	R	0h	Event #53 Reset Source: edma_rst_mod_g_rst_n
20	E52	R	0h	Event #52 Reset Source: edma_rst_mod_g_rst_n
19	E51	R	0h	Event #51 Reset Source: edma_rst_mod_g_rst_n
18	E50	R	0h	Event #50 Reset Source: edma_rst_mod_g_rst_n
17	E49	R	0h	Event #49 Reset Source: edma_rst_mod_g_rst_n
16	E48	R	0h	Event #48 Reset Source: edma_rst_mod_g_rst_n
15	E47	R	0h	Event #47 Reset Source: edma_rst_mod_g_rst_n
14	E46	R	0h	Event #46 Reset Source: edma_rst_mod_g_rst_n
13	E45	R	0h	Event #45 Reset Source: edma_rst_mod_g_rst_n
12	E44	R	0h	Event #44 Reset Source: edma_rst_mod_g_rst_n
11	E43	R	0h	Event #43 Reset Source: edma_rst_mod_g_rst_n
10	E42	R	0h	Event #42 Reset Source: edma_rst_mod_g_rst_n
9	E41	R	0h	Event #41 Reset Source: edma_rst_mod_g_rst_n

Table 4-4654. SERH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	E40	R	0h	Event #40 Reset Source: edma_rst_mod_g_rst_n
7	E39	R	0h	Event #39 Reset Source: edma_rst_mod_g_rst_n
6	E38	R	0h	Event #38 Reset Source: edma_rst_mod_g_rst_n
5	E37	R	0h	Event #37 Reset Source: edma_rst_mod_g_rst_n
4	E36	R	0h	Event #36 Reset Source: edma_rst_mod_g_rst_n
3	E35	R	0h	Event #35 Reset Source: edma_rst_mod_g_rst_n
2	E34	R	0h	Event #34 Reset Source: edma_rst_mod_g_rst_n
1	E33	R	0h	Event #33 Reset Source: edma_rst_mod_g_rst_n
0	E32	R	0h	Event #32 Reset Source: edma_rst_mod_g_rst_n

4.28.93 TPCC_SECR_RN Registers

4.28.93.1 TPCC_RN Register (Offset = 2040h) [reset = 0h]

Short Description: Secondary Event

Long Description: Secondary Event Clear Register: The secondary event clear register is used to clear the status of the SER registers. CPU write of '1' to the SECR.En bit clears the SER register. CPU write of '0' has no effect.

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Table 4-4655. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2040h

Figure 4-2207. SECR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4656. SECR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	W	0h	Event #31 Reset Source: edma_rst_mod_g_rst_n
30	E30	W	0h	Event #30 Reset Source: edma_rst_mod_g_rst_n
29	E29	W	0h	Event #29 Reset Source: edma_rst_mod_g_rst_n
28	E28	W	0h	Event #28 Reset Source: edma_rst_mod_g_rst_n
27	E27	W	0h	Event #27 Reset Source: edma_rst_mod_g_rst_n
26	E26	W	0h	Event #26 Reset Source: edma_rst_mod_g_rst_n
25	E25	W	0h	Event #25 Reset Source: edma_rst_mod_g_rst_n
24	E24	W	0h	Event #24 Reset Source: edma_rst_mod_g_rst_n
23	E23	W	0h	Event #23 Reset Source: edma_rst_mod_g_rst_n
22	E22	W	0h	Event #22 Reset Source: edma_rst_mod_g_rst_n
21	E21	W	0h	Event #21 Reset Source: edma_rst_mod_g_rst_n
20	E20	W	0h	Event #20 Reset Source: edma_rst_mod_g_rst_n
19	E19	W	0h	Event #19 Reset Source: edma_rst_mod_g_rst_n
18	E18	W	0h	Event #18 Reset Source: edma_rst_mod_g_rst_n
17	E17	W	0h	Event #17 Reset Source: edma_rst_mod_g_rst_n
16	E16	W	0h	Event #16 Reset Source: edma_rst_mod_g_rst_n
15	E15	W	0h	Event #15 Reset Source: edma_rst_mod_g_rst_n
14	E14	W	0h	Event #14 Reset Source: edma_rst_mod_g_rst_n
13	E13	W	0h	Event #13 Reset Source: edma_rst_mod_g_rst_n
12	E12	W	0h	Event #12 Reset Source: edma_rst_mod_g_rst_n
11	E11	W	0h	Event #11 Reset Source: edma_rst_mod_g_rst_n
10	E10	W	0h	Event #10 Reset Source: edma_rst_mod_g_rst_n
9	E9	W	0h	Event #9 Reset Source: edma_rst_mod_g_rst_n

Table 4-4656. SECR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	E8	W	0h	Event #8 Reset Source: edma_rst_mod_g_rst_n
7	E7	W	0h	Event #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	W	0h	Event #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	W	0h	Event #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	W	0h	Event #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	W	0h	Event #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	W	0h	Event #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	W	0h	Event #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	W	0h	Event #0 Reset Source: edma_rst_mod_g_rst_n

4.28.94 TPCC_SECRH_RN Registers

4.28.94.1 TPCC_RN Register (Offset = 2044h) [reset = 0h]

Short Description: Secondary Event

Long Description: Secondary Event Clear Register (High Part): The secondary event clear register is used to clear the status of the SERH registers. CPU write of '1' to the SECRH.En bit clears the SERH register. CPU write of '0' has no effect.

Return to Summary Table

Table 4-4657. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2044h

Figure 4-2208. SECRH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4658. SECRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	W	0h	Event #63 Reset Source: edma_rst_mod_g_rst_n
30	E62	W	0h	Event #62 Reset Source: edma_rst_mod_g_rst_n
29	E61	W	0h	Event #61 Reset Source: edma_rst_mod_g_rst_n
28	E60	W	0h	Event #60 Reset Source: edma_rst_mod_g_rst_n
27	E59	W	0h	Event #59 Reset Source: edma_rst_mod_g_rst_n
26	E58	W	0h	Event #58 Reset Source: edma_rst_mod_g_rst_n
25	E57	W	0h	Event #57 Reset Source: edma_rst_mod_g_rst_n
24	E56	W	0h	Event #56 Reset Source: edma_rst_mod_g_rst_n
23	E55	W	0h	Event #55 Reset Source: edma_rst_mod_g_rst_n
22	E54	W	0h	Event #54 Reset Source: edma_rst_mod_g_rst_n
21	E53	W	0h	Event #53 Reset Source: edma_rst_mod_g_rst_n
20	E52	W	0h	Event #52 Reset Source: edma_rst_mod_g_rst_n
19	E51	W	0h	Event #51 Reset Source: edma_rst_mod_g_rst_n
18	E50	W	0h	Event #50 Reset Source: edma_rst_mod_g_rst_n
17	E49	W	0h	Event #49 Reset Source: edma_rst_mod_g_rst_n
16	E48	W	0h	Event #48 Reset Source: edma_rst_mod_g_rst_n
15	E47	W	0h	Event #47 Reset Source: edma_rst_mod_g_rst_n
14	E46	W	0h	Event #46 Reset Source: edma_rst_mod_g_rst_n
13	E45	W	0h	Event #45 Reset Source: edma_rst_mod_g_rst_n
12	E44	W	0h	Event #44 Reset Source: edma_rst_mod_g_rst_n
11	E43	W	0h	Event #43 Reset Source: edma_rst_mod_g_rst_n
10	E42	W	0h	Event #42 Reset Source: edma_rst_mod_g_rst_n
9	E41	W	0h	Event #41 Reset Source: edma_rst_mod_g_rst_n

Table 4-4658. SECRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	E40	W	0h	Event #40 Reset Source: edma_rst_mod_g_rst_n
7	E39	W	0h	Event #39 Reset Source: edma_rst_mod_g_rst_n
6	E38	W	0h	Event #38 Reset Source: edma_rst_mod_g_rst_n
5	E37	W	0h	Event #37 Reset Source: edma_rst_mod_g_rst_n
4	E36	W	0h	Event #36 Reset Source: edma_rst_mod_g_rst_n
3	E35	W	0h	Event #35 Reset Source: edma_rst_mod_g_rst_n
2	E34	W	0h	Event #34 Reset Source: edma_rst_mod_g_rst_n
1	E33	W	0h	Event #33 Reset Source: edma_rst_mod_g_rst_n
0	E32	W	0h	Event #32 Reset Source: edma_rst_mod_g_rst_n

4.28.95 TPCC_IER_RN Registers

4.28.95.1 TPCC_RN Register (Offset = 2050h) [reset = 0h]

Short Description: Int Enable Regis

Long Description: Int Enable Register: IER.In is not directly writeable. Interrupts can be enabled via writes to IESR and can be disabled via writes to IECR register. IER.In = 0: IPR.In is NOT enabled for interrupts. IER.In = 1: IPR.In IS enabled for interrupts.

Return to Summary Table

Table 4-4659. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2050h

Figure 4-2209. IER_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4660. IER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	R	0h	Interrupt associated with TCC #31 Reset Source: edma_rst_mod_g_rst_n
30	I30	R	0h	Interrupt associated with TCC #30 Reset Source: edma_rst_mod_g_rst_n
29	I29	R	0h	Interrupt associated with TCC #29 Reset Source: edma_rst_mod_g_rst_n
28	I28	R	0h	Interrupt associated with TCC #28 Reset Source: edma_rst_mod_g_rst_n
27	I27	R	0h	Interrupt associated with TCC #27 Reset Source: edma_rst_mod_g_rst_n
26	I26	R	0h	Interrupt associated with TCC #26 Reset Source: edma_rst_mod_g_rst_n
25	I25	R	0h	Interrupt associated with TCC #25 Reset Source: edma_rst_mod_g_rst_n
24	I24	R	0h	Interrupt associated with TCC #24 Reset Source: edma_rst_mod_g_rst_n
23	I23	R	0h	Interrupt associated with TCC #23 Reset Source: edma_rst_mod_g_rst_n
22	I22	R	0h	Interrupt associated with TCC #22 Reset Source: edma_rst_mod_g_rst_n
21	I21	R	0h	Interrupt associated with TCC #21 Reset Source: edma_rst_mod_g_rst_n
20	I20	R	0h	Interrupt associated with TCC #20 Reset Source: edma_rst_mod_g_rst_n
19	I19	R	0h	Interrupt associated with TCC #19 Reset Source: edma_rst_mod_g_rst_n

Table 4-4660. IER_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	I18	R	0h	Interrupt associated with TCC #18 Reset Source: edma_rst_mod_g_rst_n
17	I17	R	0h	Interrupt associated with TCC #17 Reset Source: edma_rst_mod_g_rst_n
16	I16	R	0h	Interrupt associated with TCC #16 Reset Source: edma_rst_mod_g_rst_n
15	I15	R	0h	Interrupt associated with TCC #15 Reset Source: edma_rst_mod_g_rst_n
14	I14	R	0h	Interrupt associated with TCC #14 Reset Source: edma_rst_mod_g_rst_n
13	I13	R	0h	Interrupt associated with TCC #13 Reset Source: edma_rst_mod_g_rst_n
12	I12	R	0h	Interrupt associated with TCC #12 Reset Source: edma_rst_mod_g_rst_n
11	I11	R	0h	Interrupt associated with TCC #11 Reset Source: edma_rst_mod_g_rst_n
10	I10	R	0h	Interrupt associated with TCC #10 Reset Source: edma_rst_mod_g_rst_n
9	I9	R	0h	Interrupt associated with TCC #9 Reset Source: edma_rst_mod_g_rst_n
8	I8	R	0h	Interrupt associated with TCC #8 Reset Source: edma_rst_mod_g_rst_n
7	I7	R	0h	Interrupt associated with TCC #7 Reset Source: edma_rst_mod_g_rst_n
6	I6	R	0h	Interrupt associated with TCC #6 Reset Source: edma_rst_mod_g_rst_n
5	I5	R	0h	Interrupt associated with TCC #5 Reset Source: edma_rst_mod_g_rst_n
4	I4	R	0h	Interrupt associated with TCC #4 Reset Source: edma_rst_mod_g_rst_n
3	I3	R	0h	Interrupt associated with TCC #3 Reset Source: edma_rst_mod_g_rst_n
2	I2	R	0h	Interrupt associated with TCC #2 Reset Source: edma_rst_mod_g_rst_n
1	I1	R	0h	Interrupt associated with TCC #1 Reset Source: edma_rst_mod_g_rst_n
0	I0	R	0h	Interrupt associated with TCC #0 Reset Source: edma_rst_mod_g_rst_n

4.28.96 TPCC_IERH_RN Registers

4.28.96.1 TPCC_RN Register (Offset = 2054h) [reset = 0h]

Short Description: Int Enable Regis

Long Description: Int Enable Register (High Part): IERH.In is not directly writeable. Interrupts can be enabled via writes to IESRH and can be disabled via writes to IECRH register. IERH.In = 0: IPRH.In is NOT enabled for interrupts. IERH.In = 1: IPRH.In IS enabled for interrupts.

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Table 4-4661. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2054h

Figure 4-2210. IERH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4662. IERH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	R	0h	Interrupt associated with TCC #63 Reset Source: edma_rst_mod_g_rst_n
30	I62	R	0h	Interrupt associated with TCC #62 Reset Source: edma_rst_mod_g_rst_n
29	I61	R	0h	Interrupt associated with TCC #61 Reset Source: edma_rst_mod_g_rst_n
28	I60	R	0h	Interrupt associated with TCC #60 Reset Source: edma_rst_mod_g_rst_n
27	I59	R	0h	Interrupt associated with TCC #59 Reset Source: edma_rst_mod_g_rst_n
26	I58	R	0h	Interrupt associated with TCC #58 Reset Source: edma_rst_mod_g_rst_n
25	I57	R	0h	Interrupt associated with TCC #57 Reset Source: edma_rst_mod_g_rst_n
24	I56	R	0h	Interrupt associated with TCC #56 Reset Source: edma_rst_mod_g_rst_n
23	I55	R	0h	Interrupt associated with TCC #55 Reset Source: edma_rst_mod_g_rst_n
22	I54	R	0h	Interrupt associated with TCC #54 Reset Source: edma_rst_mod_g_rst_n
21	I53	R	0h	Interrupt associated with TCC #53 Reset Source: edma_rst_mod_g_rst_n
20	I52	R	0h	Interrupt associated with TCC #52 Reset Source: edma_rst_mod_g_rst_n
19	I51	R	0h	Interrupt associated with TCC #51 Reset Source: edma_rst_mod_g_rst_n

Table 4-4662. IERH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	I50	R	0h	Interrupt associated with TCC #50 Reset Source: edma_rst_mod_g_rst_n
17	I49	R	0h	Interrupt associated with TCC #49 Reset Source: edma_rst_mod_g_rst_n
16	I48	R	0h	Interrupt associated with TCC #48 Reset Source: edma_rst_mod_g_rst_n
15	I47	R	0h	Interrupt associated with TCC #47 Reset Source: edma_rst_mod_g_rst_n
14	I46	R	0h	Interrupt associated with TCC #46 Reset Source: edma_rst_mod_g_rst_n
13	I45	R	0h	Interrupt associated with TCC #45 Reset Source: edma_rst_mod_g_rst_n
12	I44	R	0h	Interrupt associated with TCC #44 Reset Source: edma_rst_mod_g_rst_n
11	I43	R	0h	Interrupt associated with TCC #43 Reset Source: edma_rst_mod_g_rst_n
10	I42	R	0h	Interrupt associated with TCC #42 Reset Source: edma_rst_mod_g_rst_n
9	I41	R	0h	Interrupt associated with TCC #41 Reset Source: edma_rst_mod_g_rst_n
8	I40	R	0h	Interrupt associated with TCC #40 Reset Source: edma_rst_mod_g_rst_n
7	I39	R	0h	Interrupt associated with TCC #39 Reset Source: edma_rst_mod_g_rst_n
6	I38	R	0h	Interrupt associated with TCC #38 Reset Source: edma_rst_mod_g_rst_n
5	I37	R	0h	Interrupt associated with TCC #37 Reset Source: edma_rst_mod_g_rst_n
4	I36	R	0h	Interrupt associated with TCC #36 Reset Source: edma_rst_mod_g_rst_n
3	I35	R	0h	Interrupt associated with TCC #35 Reset Source: edma_rst_mod_g_rst_n
2	I34	R	0h	Interrupt associated with TCC #34 Reset Source: edma_rst_mod_g_rst_n
1	I33	R	0h	Interrupt associated with TCC #33 Reset Source: edma_rst_mod_g_rst_n
0	I32	R	0h	Interrupt associated with TCC #32 Reset Source: edma_rst_mod_g_rst_n

4.28.97 TPCC_IECR_RN Registers

4.28.97.1 TPCC_RN Register (Offset = 2058h) [reset = 0h]

Short Description: Int Enable Clear

Long Description: Int Enable Clear Register: CPU write of '1' to the IECR.In bit causes the IER.In bit to be cleared. CPU write of '0' has no effect..

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Table 4-4663. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2058h

Figure 4-2211. IECR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4664. IECR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	W	0h	Interrupt associated with TCC #31 Reset Source: edma_rst_mod_g_rst_n
30	I30	W	0h	Interrupt associated with TCC #30 Reset Source: edma_rst_mod_g_rst_n
29	I29	W	0h	Interrupt associated with TCC #29 Reset Source: edma_rst_mod_g_rst_n
28	I28	W	0h	Interrupt associated with TCC #28 Reset Source: edma_rst_mod_g_rst_n
27	I27	W	0h	Interrupt associated with TCC #27 Reset Source: edma_rst_mod_g_rst_n
26	I26	W	0h	Interrupt associated with TCC #26 Reset Source: edma_rst_mod_g_rst_n
25	I25	W	0h	Interrupt associated with TCC #25 Reset Source: edma_rst_mod_g_rst_n
24	I24	W	0h	Interrupt associated with TCC #24 Reset Source: edma_rst_mod_g_rst_n
23	I23	W	0h	Interrupt associated with TCC #23 Reset Source: edma_rst_mod_g_rst_n
22	I22	W	0h	Interrupt associated with TCC #22 Reset Source: edma_rst_mod_g_rst_n
21	I21	W	0h	Interrupt associated with TCC #21 Reset Source: edma_rst_mod_g_rst_n
20	I20	W	0h	Interrupt associated with TCC #20 Reset Source: edma_rst_mod_g_rst_n
19	I19	W	0h	Interrupt associated with TCC #19 Reset Source: edma_rst_mod_g_rst_n
18	I18	W	0h	Interrupt associated with TCC #18 Reset Source: edma_rst_mod_g_rst_n

Table 4-4664. IECR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	I17	W	0h	Interrupt associated with TCC #17 Reset Source: edma_rst_mod_g_rst_n
16	I16	W	0h	Interrupt associated with TCC #16 Reset Source: edma_rst_mod_g_rst_n
15	I15	W	0h	Interrupt associated with TCC #15 Reset Source: edma_rst_mod_g_rst_n
14	I14	W	0h	Interrupt associated with TCC #14 Reset Source: edma_rst_mod_g_rst_n
13	I13	W	0h	Interrupt associated with TCC #13 Reset Source: edma_rst_mod_g_rst_n
12	I12	W	0h	Interrupt associated with TCC #12 Reset Source: edma_rst_mod_g_rst_n
11	I11	W	0h	Interrupt associated with TCC #11 Reset Source: edma_rst_mod_g_rst_n
10	I10	W	0h	Interrupt associated with TCC #10 Reset Source: edma_rst_mod_g_rst_n
9	I9	W	0h	Interrupt associated with TCC #9 Reset Source: edma_rst_mod_g_rst_n
8	I8	W	0h	Interrupt associated with TCC #8 Reset Source: edma_rst_mod_g_rst_n
7	I7	W	0h	Interrupt associated with TCC #7 Reset Source: edma_rst_mod_g_rst_n
6	I6	W	0h	Interrupt associated with TCC #6 Reset Source: edma_rst_mod_g_rst_n
5	I5	W	0h	Interrupt associated with TCC #5 Reset Source: edma_rst_mod_g_rst_n
4	I4	W	0h	Interrupt associated with TCC #4 Reset Source: edma_rst_mod_g_rst_n
3	I3	W	0h	Interrupt associated with TCC #3 Reset Source: edma_rst_mod_g_rst_n
2	I2	W	0h	Interrupt associated with TCC #2 Reset Source: edma_rst_mod_g_rst_n
1	I1	W	0h	Interrupt associated with TCC #1 Reset Source: edma_rst_mod_g_rst_n
0	I0	W	0h	Interrupt associated with TCC #0 Reset Source: edma_rst_mod_g_rst_n

4.28.98 TPCC_IECRH_RN Registers

4.28.98.1 TPCC_RN Register (Offset = 205Ch) [reset = 0h]

Short Description: Int Enable Clear

Long Description: Int Enable Clear Register (High Part): CPU write of '1' to the IECRH.In bit causes the IERH.In bit to be cleared. CPU write of '0' has no effect..

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Table 4-4665. Instance Table

Instance Name	Physical Address
EDMA0	52A0 205Ch

Figure 4-2212. IECRH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4666. IECRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	W	0h	Interrupt associated with TCC #63 Reset Source: edma_rst_mod_g_rst_n
30	I62	W	0h	Interrupt associated with TCC #62 Reset Source: edma_rst_mod_g_rst_n
29	I61	W	0h	Interrupt associated with TCC #61 Reset Source: edma_rst_mod_g_rst_n
28	I60	W	0h	Interrupt associated with TCC #60 Reset Source: edma_rst_mod_g_rst_n
27	I59	W	0h	Interrupt associated with TCC #59 Reset Source: edma_rst_mod_g_rst_n
26	I58	W	0h	Interrupt associated with TCC #58 Reset Source: edma_rst_mod_g_rst_n
25	I57	W	0h	Interrupt associated with TCC #57 Reset Source: edma_rst_mod_g_rst_n
24	I56	W	0h	Interrupt associated with TCC #56 Reset Source: edma_rst_mod_g_rst_n
23	I55	W	0h	Interrupt associated with TCC #55 Reset Source: edma_rst_mod_g_rst_n
22	I54	W	0h	Interrupt associated with TCC #54 Reset Source: edma_rst_mod_g_rst_n
21	I53	W	0h	Interrupt associated with TCC #53 Reset Source: edma_rst_mod_g_rst_n
20	I52	W	0h	Interrupt associated with TCC #52 Reset Source: edma_rst_mod_g_rst_n
19	I51	W	0h	Interrupt associated with TCC #51 Reset Source: edma_rst_mod_g_rst_n
18	I50	W	0h	Interrupt associated with TCC #50 Reset Source: edma_rst_mod_g_rst_n

Table 4-4666. IECRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	I49	W	0h	Interrupt associated with TCC #49 Reset Source: edma_rst_mod_g_rst_n
16	I48	W	0h	Interrupt associated with TCC #48 Reset Source: edma_rst_mod_g_rst_n
15	I47	W	0h	Interrupt associated with TCC #47 Reset Source: edma_rst_mod_g_rst_n
14	I46	W	0h	Interrupt associated with TCC #46 Reset Source: edma_rst_mod_g_rst_n
13	I45	W	0h	Interrupt associated with TCC #45 Reset Source: edma_rst_mod_g_rst_n
12	I44	W	0h	Interrupt associated with TCC #44 Reset Source: edma_rst_mod_g_rst_n
11	I43	W	0h	Interrupt associated with TCC #43 Reset Source: edma_rst_mod_g_rst_n
10	I42	W	0h	Interrupt associated with TCC #42 Reset Source: edma_rst_mod_g_rst_n
9	I41	W	0h	Interrupt associated with TCC #41 Reset Source: edma_rst_mod_g_rst_n
8	I40	W	0h	Interrupt associated with TCC #40 Reset Source: edma_rst_mod_g_rst_n
7	I39	W	0h	Interrupt associated with TCC #39 Reset Source: edma_rst_mod_g_rst_n
6	I38	W	0h	Interrupt associated with TCC #38 Reset Source: edma_rst_mod_g_rst_n
5	I37	W	0h	Interrupt associated with TCC #37 Reset Source: edma_rst_mod_g_rst_n
4	I36	W	0h	Interrupt associated with TCC #36 Reset Source: edma_rst_mod_g_rst_n
3	I35	W	0h	Interrupt associated with TCC #35 Reset Source: edma_rst_mod_g_rst_n
2	I34	W	0h	Interrupt associated with TCC #34 Reset Source: edma_rst_mod_g_rst_n
1	I33	W	0h	Interrupt associated with TCC #33 Reset Source: edma_rst_mod_g_rst_n
0	I32	W	0h	Interrupt associated with TCC #32 Reset Source: edma_rst_mod_g_rst_n

4.28.99 TPCC_IESR_RN Registers

4.28.99.1 TPCC_RN Register (Offset = 2060h) [reset = 0h]

Short Description: Int Enable Set R

Long Description: Int Enable Set Register: CPU write of '1' to the IESR.In bit causes the IESR.In bit to be set. CPU write of '0' has no effect..

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Table 4-4667. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2060h

Figure 4-2213. IESR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4668. IESR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	W	0h	Interrupt associated with TCC #31 Reset Source: edma_rst_mod_g_rst_n
30	I30	W	0h	Interrupt associated with TCC #30 Reset Source: edma_rst_mod_g_rst_n
29	I29	W	0h	Interrupt associated with TCC #29 Reset Source: edma_rst_mod_g_rst_n
28	I28	W	0h	Interrupt associated with TCC #28 Reset Source: edma_rst_mod_g_rst_n
27	I27	W	0h	Interrupt associated with TCC #27 Reset Source: edma_rst_mod_g_rst_n
26	I26	W	0h	Interrupt associated with TCC #26 Reset Source: edma_rst_mod_g_rst_n
25	I25	W	0h	Interrupt associated with TCC #25 Reset Source: edma_rst_mod_g_rst_n
24	I24	W	0h	Interrupt associated with TCC #24 Reset Source: edma_rst_mod_g_rst_n
23	I23	W	0h	Interrupt associated with TCC #23 Reset Source: edma_rst_mod_g_rst_n
22	I22	W	0h	Interrupt associated with TCC #22 Reset Source: edma_rst_mod_g_rst_n
21	I21	W	0h	Interrupt associated with TCC #21 Reset Source: edma_rst_mod_g_rst_n
20	I20	W	0h	Interrupt associated with TCC #20 Reset Source: edma_rst_mod_g_rst_n
19	I19	W	0h	Interrupt associated with TCC #19 Reset Source: edma_rst_mod_g_rst_n
18	I18	W	0h	Interrupt associated with TCC #18 Reset Source: edma_rst_mod_g_rst_n

Table 4-4668. IESR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	I17	W	0h	Interrupt associated with TCC #17 Reset Source: edma_rst_mod_g_rst_n
16	I16	W	0h	Interrupt associated with TCC #16 Reset Source: edma_rst_mod_g_rst_n
15	I15	W	0h	Interrupt associated with TCC #15 Reset Source: edma_rst_mod_g_rst_n
14	I14	W	0h	Interrupt associated with TCC #14 Reset Source: edma_rst_mod_g_rst_n
13	I13	W	0h	Interrupt associated with TCC #13 Reset Source: edma_rst_mod_g_rst_n
12	I12	W	0h	Interrupt associated with TCC #12 Reset Source: edma_rst_mod_g_rst_n
11	I11	W	0h	Interrupt associated with TCC #11 Reset Source: edma_rst_mod_g_rst_n
10	I10	W	0h	Interrupt associated with TCC #10 Reset Source: edma_rst_mod_g_rst_n
9	I9	W	0h	Interrupt associated with TCC #9 Reset Source: edma_rst_mod_g_rst_n
8	I8	W	0h	Interrupt associated with TCC #8 Reset Source: edma_rst_mod_g_rst_n
7	I7	W	0h	Interrupt associated with TCC #7 Reset Source: edma_rst_mod_g_rst_n
6	I6	W	0h	Interrupt associated with TCC #6 Reset Source: edma_rst_mod_g_rst_n
5	I5	W	0h	Interrupt associated with TCC #5 Reset Source: edma_rst_mod_g_rst_n
4	I4	W	0h	Interrupt associated with TCC #4 Reset Source: edma_rst_mod_g_rst_n
3	I3	W	0h	Interrupt associated with TCC #3 Reset Source: edma_rst_mod_g_rst_n
2	I2	W	0h	Interrupt associated with TCC #2 Reset Source: edma_rst_mod_g_rst_n
1	I1	W	0h	Interrupt associated with TCC #1 Reset Source: edma_rst_mod_g_rst_n
0	I0	W	0h	Interrupt associated with TCC #0 Reset Source: edma_rst_mod_g_rst_n

4.28.100 TPCC_IESRH_RN Registers

4.28.100.1 TPCC_RN Register (Offset = 2064h) [reset = 0h]

Short Description: Int Enable Set R

Long Description: Int Enable Set Register (High Part): CPU write of '1' to the IESRH.In bit causes the IESRH.In bit to be set. CPU write of '0' has no effect..

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Table 4-4669. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2064h

Figure 4-2214. IESRH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4670. IESRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	W	0h	Interrupt associated with TCC #63 Reset Source: edma_rst_mod_g_rst_n
30	I62	W	0h	Interrupt associated with TCC #62 Reset Source: edma_rst_mod_g_rst_n
29	I61	W	0h	Interrupt associated with TCC #61 Reset Source: edma_rst_mod_g_rst_n
28	I60	W	0h	Interrupt associated with TCC #60 Reset Source: edma_rst_mod_g_rst_n
27	I59	W	0h	Interrupt associated with TCC #59 Reset Source: edma_rst_mod_g_rst_n
26	I58	W	0h	Interrupt associated with TCC #58 Reset Source: edma_rst_mod_g_rst_n
25	I57	W	0h	Interrupt associated with TCC #57 Reset Source: edma_rst_mod_g_rst_n
24	I56	W	0h	Interrupt associated with TCC #56 Reset Source: edma_rst_mod_g_rst_n
23	I55	W	0h	Interrupt associated with TCC #55 Reset Source: edma_rst_mod_g_rst_n
22	I54	W	0h	Interrupt associated with TCC #54 Reset Source: edma_rst_mod_g_rst_n
21	I53	W	0h	Interrupt associated with TCC #53 Reset Source: edma_rst_mod_g_rst_n
20	I52	W	0h	Interrupt associated with TCC #52 Reset Source: edma_rst_mod_g_rst_n
19	I51	W	0h	Interrupt associated with TCC #51 Reset Source: edma_rst_mod_g_rst_n
18	I50	W	0h	Interrupt associated with TCC #50 Reset Source: edma_rst_mod_g_rst_n

Table 4-4670. IESRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	I49	W	0h	Interrupt associated with TCC #49 Reset Source: edma_rst_mod_g_rst_n
16	I48	W	0h	Interrupt associated with TCC #48 Reset Source: edma_rst_mod_g_rst_n
15	I47	W	0h	Interrupt associated with TCC #47 Reset Source: edma_rst_mod_g_rst_n
14	I46	W	0h	Interrupt associated with TCC #46 Reset Source: edma_rst_mod_g_rst_n
13	I45	W	0h	Interrupt associated with TCC #45 Reset Source: edma_rst_mod_g_rst_n
12	I44	W	0h	Interrupt associated with TCC #44 Reset Source: edma_rst_mod_g_rst_n
11	I43	W	0h	Interrupt associated with TCC #43 Reset Source: edma_rst_mod_g_rst_n
10	I42	W	0h	Interrupt associated with TCC #42 Reset Source: edma_rst_mod_g_rst_n
9	I41	W	0h	Interrupt associated with TCC #41 Reset Source: edma_rst_mod_g_rst_n
8	I40	W	0h	Interrupt associated with TCC #40 Reset Source: edma_rst_mod_g_rst_n
7	I39	W	0h	Interrupt associated with TCC #39 Reset Source: edma_rst_mod_g_rst_n
6	I38	W	0h	Interrupt associated with TCC #38 Reset Source: edma_rst_mod_g_rst_n
5	I37	W	0h	Interrupt associated with TCC #37 Reset Source: edma_rst_mod_g_rst_n
4	I36	W	0h	Interrupt associated with TCC #36 Reset Source: edma_rst_mod_g_rst_n
3	I35	W	0h	Interrupt associated with TCC #35 Reset Source: edma_rst_mod_g_rst_n
2	I34	W	0h	Interrupt associated with TCC #34 Reset Source: edma_rst_mod_g_rst_n
1	I33	W	0h	Interrupt associated with TCC #33 Reset Source: edma_rst_mod_g_rst_n
0	I32	W	0h	Interrupt associated with TCC #32 Reset Source: edma_rst_mod_g_rst_n

4.28.101 TPCC_IPR_RN Registers

4.28.101.1 TPCC_RN Register (Offset = 2068h) [reset = 0h]

Short Description: Interrupt Pendin

Long Description: Interrupt Pending Register: IPR.In bit is set when a interrupt completion code with TCC of N is detected. IPR.In bit is cleared via software by writing a '1' to ICR.In bit.

Return to Summary Table

Table 4-4671. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2068h

Figure 4-2215. IPR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4672. IPR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	R	0h	Interrupt associated with TCC #31 Reset Source: edma_rst_mod_g_rst_n
30	I30	R	0h	Interrupt associated with TCC #30 Reset Source: edma_rst_mod_g_rst_n
29	I29	R	0h	Interrupt associated with TCC #29 Reset Source: edma_rst_mod_g_rst_n
28	I28	R	0h	Interrupt associated with TCC #28 Reset Source: edma_rst_mod_g_rst_n
27	I27	R	0h	Interrupt associated with TCC #27 Reset Source: edma_rst_mod_g_rst_n
26	I26	R	0h	Interrupt associated with TCC #26 Reset Source: edma_rst_mod_g_rst_n
25	I25	R	0h	Interrupt associated with TCC #25 Reset Source: edma_rst_mod_g_rst_n
24	I24	R	0h	Interrupt associated with TCC #24 Reset Source: edma_rst_mod_g_rst_n
23	I23	R	0h	Interrupt associated with TCC #23 Reset Source: edma_rst_mod_g_rst_n
22	I22	R	0h	Interrupt associated with TCC #22 Reset Source: edma_rst_mod_g_rst_n
21	I21	R	0h	Interrupt associated with TCC #21 Reset Source: edma_rst_mod_g_rst_n
20	I20	R	0h	Interrupt associated with TCC #20 Reset Source: edma_rst_mod_g_rst_n
19	I19	R	0h	Interrupt associated with TCC #19 Reset Source: edma_rst_mod_g_rst_n
18	I18	R	0h	Interrupt associated with TCC #18 Reset Source: edma_rst_mod_g_rst_n

Table 4-4672. IPR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	I17	R	0h	Interrupt associated with TCC #17 Reset Source: edma_rst_mod_g_rst_n
16	I16	R	0h	Interrupt associated with TCC #16 Reset Source: edma_rst_mod_g_rst_n
15	I15	R	0h	Interrupt associated with TCC #15 Reset Source: edma_rst_mod_g_rst_n
14	I14	R	0h	Interrupt associated with TCC #14 Reset Source: edma_rst_mod_g_rst_n
13	I13	R	0h	Interrupt associated with TCC #13 Reset Source: edma_rst_mod_g_rst_n
12	I12	R	0h	Interrupt associated with TCC #12 Reset Source: edma_rst_mod_g_rst_n
11	I11	R	0h	Interrupt associated with TCC #11 Reset Source: edma_rst_mod_g_rst_n
10	I10	R	0h	Interrupt associated with TCC #10 Reset Source: edma_rst_mod_g_rst_n
9	I9	R	0h	Interrupt associated with TCC #9 Reset Source: edma_rst_mod_g_rst_n
8	I8	R	0h	Interrupt associated with TCC #8 Reset Source: edma_rst_mod_g_rst_n
7	I7	R	0h	Interrupt associated with TCC #7 Reset Source: edma_rst_mod_g_rst_n
6	I6	R	0h	Interrupt associated with TCC #6 Reset Source: edma_rst_mod_g_rst_n
5	I5	R	0h	Interrupt associated with TCC #5 Reset Source: edma_rst_mod_g_rst_n
4	I4	R	0h	Interrupt associated with TCC #4 Reset Source: edma_rst_mod_g_rst_n
3	I3	R	0h	Interrupt associated with TCC #3 Reset Source: edma_rst_mod_g_rst_n
2	I2	R	0h	Interrupt associated with TCC #2 Reset Source: edma_rst_mod_g_rst_n
1	I1	R	0h	Interrupt associated with TCC #1 Reset Source: edma_rst_mod_g_rst_n
0	I0	R	0h	Interrupt associated with TCC #0 Reset Source: edma_rst_mod_g_rst_n

4.28.102 TPCC_IPRH_RN Registers

4.28.102.1 TPCC_RN Register (Offset = 206Ch) [reset = 0h]

Short Description: Interrupt Pendin

Long Description: Interrupt Pending Register (High Part): IPRH.In bit is set when a interrupt completion code with TCC of N is detected. IPRH.In bit is cleared via software by writing a '1' to ICRH.In bit.

Return to Summary Table

Table 4-4673. Instance Table

Instance Name	Physical Address
EDMA0	52A0 206Ch

Figure 4-2216. IPRH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4674. IPRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	R	0h	Interrupt associated with TCC #63 Reset Source: edma_rst_mod_g_rst_n
30	I62	R	0h	Interrupt associated with TCC #62 Reset Source: edma_rst_mod_g_rst_n
29	I61	R	0h	Interrupt associated with TCC #61 Reset Source: edma_rst_mod_g_rst_n
28	I60	R	0h	Interrupt associated with TCC #60 Reset Source: edma_rst_mod_g_rst_n
27	I59	R	0h	Interrupt associated with TCC #59 Reset Source: edma_rst_mod_g_rst_n
26	I58	R	0h	Interrupt associated with TCC #58 Reset Source: edma_rst_mod_g_rst_n
25	I57	R	0h	Interrupt associated with TCC #57 Reset Source: edma_rst_mod_g_rst_n
24	I56	R	0h	Interrupt associated with TCC #56 Reset Source: edma_rst_mod_g_rst_n
23	I55	R	0h	Interrupt associated with TCC #55 Reset Source: edma_rst_mod_g_rst_n
22	I54	R	0h	Interrupt associated with TCC #54 Reset Source: edma_rst_mod_g_rst_n
21	I53	R	0h	Interrupt associated with TCC #53 Reset Source: edma_rst_mod_g_rst_n
20	I52	R	0h	Interrupt associated with TCC #52 Reset Source: edma_rst_mod_g_rst_n
19	I51	R	0h	Interrupt associated with TCC #51 Reset Source: edma_rst_mod_g_rst_n
18	I50	R	0h	Interrupt associated with TCC #50 Reset Source: edma_rst_mod_g_rst_n

Table 4-4674. IPRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	I49	R	0h	Interrupt associated with TCC #49 Reset Source: edma_rst_mod_g_rst_n
16	I48	R	0h	Interrupt associated with TCC #48 Reset Source: edma_rst_mod_g_rst_n
15	I47	R	0h	Interrupt associated with TCC #47 Reset Source: edma_rst_mod_g_rst_n
14	I46	R	0h	Interrupt associated with TCC #46 Reset Source: edma_rst_mod_g_rst_n
13	I45	R	0h	Interrupt associated with TCC #45 Reset Source: edma_rst_mod_g_rst_n
12	I44	R	0h	Interrupt associated with TCC #44 Reset Source: edma_rst_mod_g_rst_n
11	I43	R	0h	Interrupt associated with TCC #43 Reset Source: edma_rst_mod_g_rst_n
10	I42	R	0h	Interrupt associated with TCC #42 Reset Source: edma_rst_mod_g_rst_n
9	I41	R	0h	Interrupt associated with TCC #41 Reset Source: edma_rst_mod_g_rst_n
8	I40	R	0h	Interrupt associated with TCC #40 Reset Source: edma_rst_mod_g_rst_n
7	I39	R	0h	Interrupt associated with TCC #39 Reset Source: edma_rst_mod_g_rst_n
6	I38	R	0h	Interrupt associated with TCC #38 Reset Source: edma_rst_mod_g_rst_n
5	I37	R	0h	Interrupt associated with TCC #37 Reset Source: edma_rst_mod_g_rst_n
4	I36	R	0h	Interrupt associated with TCC #36 Reset Source: edma_rst_mod_g_rst_n
3	I35	R	0h	Interrupt associated with TCC #35 Reset Source: edma_rst_mod_g_rst_n
2	I34	R	0h	Interrupt associated with TCC #34 Reset Source: edma_rst_mod_g_rst_n
1	I33	R	0h	Interrupt associated with TCC #33 Reset Source: edma_rst_mod_g_rst_n
0	I32	R	0h	Interrupt associated with TCC #32 Reset Source: edma_rst_mod_g_rst_n

4.28.103 TPCC_ICR_RN Registers

4.28.103.1 TPCC_RN Register (Offset = 2070h) [reset = 0h]

Short Description: Interrupt Clear

Long Description: Interrupt Clear Register: CPU write of '1' to the ICR.In bit causes the IPR.In bit to be cleared. CPU write of '0' has no effect. All IPR.In bits must be cleared before additional interrupts will be asserted by CC.

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Table 4-4675. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2070h

Figure 4-2217. ICR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4676. ICR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	W	0h	Interrupt associated with TCC #31 Reset Source: edma_rst_mod_g_rst_n
30	I30	W	0h	Interrupt associated with TCC #30 Reset Source: edma_rst_mod_g_rst_n
29	I29	W	0h	Interrupt associated with TCC #29 Reset Source: edma_rst_mod_g_rst_n
28	I28	W	0h	Interrupt associated with TCC #28 Reset Source: edma_rst_mod_g_rst_n
27	I27	W	0h	Interrupt associated with TCC #27 Reset Source: edma_rst_mod_g_rst_n
26	I26	W	0h	Interrupt associated with TCC #26 Reset Source: edma_rst_mod_g_rst_n
25	I25	W	0h	Interrupt associated with TCC #25 Reset Source: edma_rst_mod_g_rst_n
24	I24	W	0h	Interrupt associated with TCC #24 Reset Source: edma_rst_mod_g_rst_n
23	I23	W	0h	Interrupt associated with TCC #23 Reset Source: edma_rst_mod_g_rst_n
22	I22	W	0h	Interrupt associated with TCC #22 Reset Source: edma_rst_mod_g_rst_n
21	I21	W	0h	Interrupt associated with TCC #21 Reset Source: edma_rst_mod_g_rst_n
20	I20	W	0h	Interrupt associated with TCC #20 Reset Source: edma_rst_mod_g_rst_n
19	I19	W	0h	Interrupt associated with TCC #19 Reset Source: edma_rst_mod_g_rst_n
18	I18	W	0h	Interrupt associated with TCC #18 Reset Source: edma_rst_mod_g_rst_n

Table 4-4676. ICR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	I17	W	0h	Interrupt associated with TCC #17 Reset Source: edma_rst_mod_g_rst_n
16	I16	W	0h	Interrupt associated with TCC #16 Reset Source: edma_rst_mod_g_rst_n
15	I15	W	0h	Interrupt associated with TCC #15 Reset Source: edma_rst_mod_g_rst_n
14	I14	W	0h	Interrupt associated with TCC #14 Reset Source: edma_rst_mod_g_rst_n
13	I13	W	0h	Interrupt associated with TCC #13 Reset Source: edma_rst_mod_g_rst_n
12	I12	W	0h	Interrupt associated with TCC #12 Reset Source: edma_rst_mod_g_rst_n
11	I11	W	0h	Interrupt associated with TCC #11 Reset Source: edma_rst_mod_g_rst_n
10	I10	W	0h	Interrupt associated with TCC #10 Reset Source: edma_rst_mod_g_rst_n
9	I9	W	0h	Interrupt associated with TCC #9 Reset Source: edma_rst_mod_g_rst_n
8	I8	W	0h	Interrupt associated with TCC #8 Reset Source: edma_rst_mod_g_rst_n
7	I7	W	0h	Interrupt associated with TCC #7 Reset Source: edma_rst_mod_g_rst_n
6	I6	W	0h	Interrupt associated with TCC #6 Reset Source: edma_rst_mod_g_rst_n
5	I5	W	0h	Interrupt associated with TCC #5 Reset Source: edma_rst_mod_g_rst_n
4	I4	W	0h	Interrupt associated with TCC #4 Reset Source: edma_rst_mod_g_rst_n
3	I3	W	0h	Interrupt associated with TCC #3 Reset Source: edma_rst_mod_g_rst_n
2	I2	W	0h	Interrupt associated with TCC #2 Reset Source: edma_rst_mod_g_rst_n
1	I1	W	0h	Interrupt associated with TCC #1 Reset Source: edma_rst_mod_g_rst_n
0	I0	W	0h	Interrupt associated with TCC #0 Reset Source: edma_rst_mod_g_rst_n

4.28.104 TPCC_ICRH_RN Registers

4.28.104.1 TPCC_RN Register (Offset = 2074h) [reset = 0h]

Short Description: Interrupt Clear

Long Description: Interrupt Clear Register (High Part): CPU write of '1' to the ICRH.In bit causes the IPRH.In bit to be cleared. CPU write of '0' has no effect. All IPRH.In bits must be cleared before additional interrupts will be asserted by CC.

Return to Summary Table

Table 4-4677. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2074h

Figure 4-2218. ICRH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4678. ICRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	W	0h	Interrupt associated with TCC #63 Reset Source: edma_rst_mod_g_rst_n
30	I62	W	0h	Interrupt associated with TCC #62 Reset Source: edma_rst_mod_g_rst_n
29	I61	W	0h	Interrupt associated with TCC #61 Reset Source: edma_rst_mod_g_rst_n
28	I60	W	0h	Interrupt associated with TCC #60 Reset Source: edma_rst_mod_g_rst_n
27	I59	W	0h	Interrupt associated with TCC #59 Reset Source: edma_rst_mod_g_rst_n
26	I58	W	0h	Interrupt associated with TCC #58 Reset Source: edma_rst_mod_g_rst_n
25	I57	W	0h	Interrupt associated with TCC #57 Reset Source: edma_rst_mod_g_rst_n
24	I56	W	0h	Interrupt associated with TCC #56 Reset Source: edma_rst_mod_g_rst_n
23	I55	W	0h	Interrupt associated with TCC #55 Reset Source: edma_rst_mod_g_rst_n
22	I54	W	0h	Interrupt associated with TCC #54 Reset Source: edma_rst_mod_g_rst_n
21	I53	W	0h	Interrupt associated with TCC #53 Reset Source: edma_rst_mod_g_rst_n
20	I52	W	0h	Interrupt associated with TCC #52 Reset Source: edma_rst_mod_g_rst_n
19	I51	W	0h	Interrupt associated with TCC #51 Reset Source: edma_rst_mod_g_rst_n

Table 4-4678. ICRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	I50	W	0h	Interrupt associated with TCC #50 Reset Source: edma_rst_mod_g_rst_n
17	I49	W	0h	Interrupt associated with TCC #49 Reset Source: edma_rst_mod_g_rst_n
16	I48	W	0h	Interrupt associated with TCC #48 Reset Source: edma_rst_mod_g_rst_n
15	I47	W	0h	Interrupt associated with TCC #47 Reset Source: edma_rst_mod_g_rst_n
14	I46	W	0h	Interrupt associated with TCC #46 Reset Source: edma_rst_mod_g_rst_n
13	I45	W	0h	Interrupt associated with TCC #45 Reset Source: edma_rst_mod_g_rst_n
12	I44	W	0h	Interrupt associated with TCC #44 Reset Source: edma_rst_mod_g_rst_n
11	I43	W	0h	Interrupt associated with TCC #43 Reset Source: edma_rst_mod_g_rst_n
10	I42	W	0h	Interrupt associated with TCC #42 Reset Source: edma_rst_mod_g_rst_n
9	I41	W	0h	Interrupt associated with TCC #41 Reset Source: edma_rst_mod_g_rst_n
8	I40	W	0h	Interrupt associated with TCC #40 Reset Source: edma_rst_mod_g_rst_n
7	I39	W	0h	Interrupt associated with TCC #39 Reset Source: edma_rst_mod_g_rst_n
6	I38	W	0h	Interrupt associated with TCC #38 Reset Source: edma_rst_mod_g_rst_n
5	I37	W	0h	Interrupt associated with TCC #37 Reset Source: edma_rst_mod_g_rst_n
4	I36	W	0h	Interrupt associated with TCC #36 Reset Source: edma_rst_mod_g_rst_n
3	I35	W	0h	Interrupt associated with TCC #35 Reset Source: edma_rst_mod_g_rst_n
2	I34	W	0h	Interrupt associated with TCC #34 Reset Source: edma_rst_mod_g_rst_n
1	I33	W	0h	Interrupt associated with TCC #33 Reset Source: edma_rst_mod_g_rst_n
0	I32	W	0h	Interrupt associated with TCC #32 Reset Source: edma_rst_mod_g_rst_n

4.28.105 TPCC_IEVAL_RN Registers

4.28.105.1 TPCC_RN Register (Offset = 2078h) [reset = 0h]

Short Description: Interrupt Eval R

Long Description: Interrupt Eval Register

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Table 4-4679. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2078h

Figure 4-2219. IEVAL_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES76															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES76														SET	EVAL
R														W	W
0h														0h	0h

Access Types Legend

Table 4-4680. IEVAL_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RES76	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
1	SET	W	0h	Interrupt Set: CPU write of '1' to the SETn bit causes the tpcc_intN output signal to be pulsed egardless of state of interrupts enable [IERn] and status [IPRn]. CPU write of '0' has no effect. Reset Source: edma_rst_mod_g_rst_n
0	EVAL	W	0h	Interrupt Evaluate: CPU write of '1' to the EVALn bit causes the tpcc_intN output signal to be pulsed if any enabled interrupts [IERn] are still pending [IPRn]. CPU write of '0' has no effect.. Reset Source: edma_rst_mod_g_rst_n

4.28.106 TPCC_QER_RN Registers

4.28.106.1 TPCC_RN Register (Offset = 2080h) [reset = 0h]

Short Description: QDMA Event Regis

Long Description: QDMA Event Register: If QER.En bit is set then the corresponding QDMA channel is prioritized vs. other qdma events for submission to the TC. QER.En bit is set when a vbus write byte matches the address defined in the QCHMAPn register. QER.En bit is cleared when the corresponding event is prioritized and serviced. QER.En is also cleared when user writes a '1' to the QSECR.En bit. If the QER.En bit is already set and a new QDMA event is detected due to user write to QDMA trigger location and QEER register is set then the corresponding bit in the QDMA Event Missed Register is set.

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Table 4-4681. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2080h

Figure 4-2220. QER_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES77															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES77								E7	E6	E5	E4	E3	E2	E1	E0
R								R	R	R	R	R	R	R	R
0h								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4682. QER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES77	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
7	E7	R	0h	Event #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	R	0h	Event #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	R	0h	Event #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	R	0h	Event #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	R	0h	Event #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	R	0h	Event #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	R	0h	Event #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	R	0h	Event #0 Reset Source: edma_rst_mod_g_rst_n

4.28.107 TPCC_QEER_RN Registers

4.28.107.1 TPCC_RN Register (Offset = 2084h) [reset = 0h]

Short Description: QDMA Event Enabl

Long Description: QDMA Event Enable Register: Enabled/disabled QDMA address comparator for QDMA Channel N. QEER.En is not directly writeable. QDMA channels can be enabled via writes to QEESR and can be disabled via writes to QEECR register. QEER.En = 1 The corresponding QDMA channel comparator is enabled and Events will be recognized and latched in QER.En. QEER.En = 0 The corresponding QDMA channel comparator is disabled. Events will not be recognized/latched in QER.En.

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Table 4-4683. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2084h

Figure 4-2221. QEER_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES78															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES78								E7	E6	E5	E4	E3	E2	E1	E0
R								R	R	R	R	R	R	R	R
0h								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4684. QEER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES78	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
7	E7	R	0h	Event #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	R	0h	Event #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	R	0h	Event #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	R	0h	Event #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	R	0h	Event #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	R	0h	Event #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	R	0h	Event #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	R	0h	Event #0 Reset Source: edma_rst_mod_g_rst_n

4.28.108 TPCC_QEECR_RN Registers

4.28.108.1 TPCC_RN Register (Offset = 2088h) [reset = 0h]

Short Description: QDMA Event Enabl

Long Description: QDMA Event Enable Clear Register: CPU write of '1' to the QEECR.En bit causes the QEER.En bit to be cleared. CPU write of '0' has no effect..

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Table 4-4685. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2088h

Figure 4-2222. QEECR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES79															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES79								E7	E6	E5	E4	E3	E2	E1	E0
R								W	W	W	W	W	W	W	W
0h								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4686. QEECR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES79	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
7	E7	W	0h	Event #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	W	0h	Event #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	W	0h	Event #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	W	0h	Event #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	W	0h	Event #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	W	0h	Event #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	W	0h	Event #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	W	0h	Event #0 Reset Source: edma_rst_mod_g_rst_n

4.28.109 TPCC_QEESR_RN Registers

4.28.109.1 TPCC_RN Register (Offset = 208Ch) [reset = 0h]

Short Description: QDMA Event Enabl

Long Description: QDMA Event Enable Set Register: CPU write of '1' to the QEESR.En bit causes the QEESR.En bit to be set. CPU write of '0' has no effect..

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Table 4-4687. Instance Table

Instance Name	Physical Address
EDMA0	52A0 208Ch

Figure 4-2223. QEESR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES80															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES80								E7	E6	E5	E4	E3	E2	E1	E0
R								W	W	W	W	W	W	W	W
0h								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4688. QEESR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES80	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
7	E7	W	0h	Event #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	W	0h	Event #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	W	0h	Event #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	W	0h	Event #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	W	0h	Event #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	W	0h	Event #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	W	0h	Event #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	W	0h	Event #0 Reset Source: edma_rst_mod_g_rst_n

4.28.110 TPCC_QSER_RN Registers

4.28.110.1 TPCC_RN Register (Offset = 2090h) [reset = 0h]

Short Description: QDMA Secondary E

Long Description: QDMA Secondary Event Register: The QDMA secondary event register is used along with the QDMA Event Register (QER) to provide information on the state of a QDMA Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

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Table 4-4689. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2090h

Figure 4-2224. QSER_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES81															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES81								E7	E6	E5	E4	E3	E2	E1	E0
R								R	R	R	R	R	R	R	R
0h								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4690. QSER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES81	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
7	E7	R	0h	Event #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	R	0h	Event #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	R	0h	Event #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	R	0h	Event #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	R	0h	Event #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	R	0h	Event #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	R	0h	Event #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	R	0h	Event #0 Reset Source: edma_rst_mod_g_rst_n

4.28.111 TPCC_QSECR_RN Registers

4.28.111.1 TPCC_RN Register (Offset = 2094h) [reset = 0h]

Short Description: QDMA Secondary E

Long Description: QDMA Secondary Event Clear Register: The secondary event clear register is used to clear the status of the QSER and QER register (note that this is slightly different than the SER operation which does not clear the ER.En register). CPU write of '1' to the QSECR.En bit clears the QSER.En and QER.En register fields. CPU write of '0' has no effect..

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Table 4-4691. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2094h

Figure 4-2225. QSECR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES82															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES82								E7	E6	E5	E4	E3	E2	E1	E0
R								W	W	W	W	W	W	W	W
0h								0h	0h	0h	0h	0h	0h	0h	0h

Access Types Legend

Table 4-4692. QSECR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES82	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
7	E7	W	0h	Event #7 Reset Source: edma_rst_mod_g_rst_n
6	E6	W	0h	Event #6 Reset Source: edma_rst_mod_g_rst_n
5	E5	W	0h	Event #5 Reset Source: edma_rst_mod_g_rst_n
4	E4	W	0h	Event #4 Reset Source: edma_rst_mod_g_rst_n
3	E3	W	0h	Event #3 Reset Source: edma_rst_mod_g_rst_n
2	E2	W	0h	Event #2 Reset Source: edma_rst_mod_g_rst_n
1	E1	W	0h	Event #1 Reset Source: edma_rst_mod_g_rst_n
0	E0	W	0h	Event #0 Reset Source: edma_rst_mod_g_rst_n

4.28.112 TPCC_OPT Registers

4.28.112.1 TPCC_OPT Register (Offset = 4000h) [reset = 0h]

Short Description: Options Parame

Long Description: Options Parameter

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Table 4-4693. Instance Table

Instance Name	Physical Address
EDMA0	52A0 4000h

Figure 4-2226. OPT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRIV	RES83			PRIVID				ITCCHEN	TCCHEN	ITCINTEN	TCINTEN	WIMODE	RES84	TCC	
R	R			R				R/W	R/W	R/W	R/W	R/W	R	R/W	
0h	0h			0h				0h	0h	0h	0h	0h	0h	0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCC				TCCMODE	FWID			RES85				STATIC	SYNCDIM	DAM	SAM
R/W				R/W	R/W			R				R/W	R/W	R/W	R/W
0h				0h	0h			0h				0h	0h	0h	0h

Access Types Legend

Table 4-4694. OPT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRIV	R	0h	Privilege level: privilege level [supervisor vs. user] for the host/cpu/dma that programmed this PaRAM Entry. Value is set with the vbus priv value when any part of the PaRAM Entry is written. Not writeable via vbus wdata bus. Is readable via VBus rdata bus. PRIV = 0 : User level privilege PRIV = 1 : Supervisor level privilege Reset Source: edma_rst_mod_g_rst_n
30:28	RES83	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
27:24	PRIVID	R	0h	Privilege ID: Privilege ID for the external host/cpu/dma that programmed this PaRAM Entry. This value is set with the vbus privid value when any part of the PaRAM Entry is written. Not writeable via vbus wdata bus. Is readable via VBus rdata bus. Reset Source: edma_rst_mod_g_rst_n
23	ITCCHEN	R/W	0h	Intermediate transfer completion chaining enable: 0: Intermediate transfer complete chaining is disabled. 1: Intermediate transfer complete chaining is enabled. Reset Source: edma_rst_mod_g_rst_n
22	TCCHEN	R/W	0h	Transfer complete chaining enable: 0: Transfer complete chaining is disabled. 1: Transfer complete chaining is enabled. Reset Source: edma_rst_mod_g_rst_n
21	ITCINTEN	R/W	0h	Intermediate transfer completion interrupt enable: 0: Intermediate transfer complete interrupt is disabled. 1: Intermediate transfer complete interrupt is enabled [corresponding IER[TCC] bit must be set to 1 to generate interrupt] Reset Source: edma_rst_mod_g_rst_n
20	TCINTEN	R/W	0h	Transfer complete interrupt enable: 0: Transfer complete interrupt is disabled. 1: Transfer complete interrupt is enabled [corresponding IER[TCC] bit must be set to 1 to generate interrupt] Reset Source: edma_rst_mod_g_rst_n

Table 4-4694. OPT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	WIMODE	R/W	0h	Backward compatibility mode: 0: Normal operation 1 : WI Backwards Compatibility mode forces BCNT to be adjusted by '1' upon TR submission [0 means 1 1 means 2 ...] and forces ACNT to be treated as a word-count [left shifted by 2 by hardware to create byte cnt for TR submission] Reset Source: edma_rst_mod_g_rst_n
18	RES84	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
17:12	TCC	R/W	0h	Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER [bit CER[TCC]] for chaining or in IER [bit IER[TCC]] for interrupts. Reset Source: edma_rst_mod_g_rst_n
11	TCCMODE	R/W	0h	Transfer complete code mode: Indicates the point at which a transfer is considered completed. Applies to both chaining and interrupt. 0: Normal Completion A transfer is considered completed after the transfer parameters are returned to the CC from the TC [which was returned from the peripheral]. 1: Early Completion A transfer is considered completed after the CC submits a TR to the TC. CC generates completion code internally . Reset Source: edma_rst_mod_g_rst_n
10:8	FWID	R/W	0h	FIFO width: Applies if either SAM or DAM is set to FIFO mode. Pass-thru to TC. Reset Source: edma_rst_mod_g_rst_n
7:4	RES85	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
3	STATIC	R/W	0h	Static Entry: 0: Entry is updated as normal 1: Entry is static Count and Address updates are not updated after TRP is submitted. Linking is not performed. Reset Source: edma_rst_mod_g_rst_n
2	SYNCDIM	R/W	0h	Transfer Synchronization Dimension: 0: A-Sync Each event triggers the transfer of ACNT elements. 1: AB-Sync Each event triggers the transfer of BCNT arrays of ACNT elements Reset Source: edma_rst_mod_g_rst_n
1	DAM	R/W	0h	Destination Address Mode: Destination Address Mode within an array. Pass-thru to TC. 0: INCR Dst addressing within an array increments. Dst is not a FIFO. 1: FIFO Dst addressing within an array wraps around upon reaching FIFO width. Reset Source: edma_rst_mod_g_rst_n
0	SAM	R/W	0h	Source Address Mode: Source Address Mode within an array. Pass-thru to TC. 0: INCR Src addressing within an array increments. Source is not a FIFO. 1: FIFO Src addressing within an array wraps around upon reaching FIFO width. Reset Source: edma_rst_mod_g_rst_n

4.28.113 TPCC_SRC Registers

4.28.113.1 TPCC_SRC Register (Offset = 4004h) [reset = 0h]

Short Description: Source Address

Long Description: Source Address

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Table 4-4695. Instance Table

Instance Name	Physical Address
EDMA0	52A0 4004h

Figure 4-2227. SRC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SRC															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRC															
R/W															
0h															

Access Types Legend

Table 4-4696. SRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SRC	R/W	0h	Source Address: The 32-bit source address parameters specify the starting byte address of the source . If SAM is set to FIFO mode then the user should program the Source address to be aligned to the value specified by the OPT.FWID field. No errors are recognized here but TC will assert error if this is not true. Reset Source: edma_rst_mod_g_rst_n

4.28.114 TPCC_ABCNT Registers

4.28.114.1 TPCC_ABCNT Register (Offset = 4008h) [reset = 0h]

Short Description: A and B byte cou

Long Description: A and B byte count

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Table 4-4697. Instance Table

Instance Name	Physical Address
EDMA0	52A0 4008h

Figure 4-2228. ABCNT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BCNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACNT															
R/W															
0h															

Access Types Legend

Table 4-4698. ABCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	BCNT	R/W	0h	BCNT : Count for 2nd Dimension: BCNT is a 16-bit unsigned value that specifies the number of arrays of length ACNT. For normal operation valid values for BCNT can be anywhere between 1 and 65535. Therefore the maximum number of arrays in a frame is 65535 [64K-1 arrays]. BCNT=1 means 1 array in the frame and BCNT=0 means 0 arrays in the frame. In normal mode a BCNT of '0' is considered as either a Null or Dummy transfer. A Dummy or Null transfer will generate a Completion code depending on the settings of the completion bit fields of the OPT field. If the OPT.WIMODE bit is set then the programmed BCNT value will be incremented by '1' before submission to TC. I.e. 0 means 1 1 means 2 2 means 3 ... Reset Source: edma_rst_mod_g_rst_n
15:0	ACNT	R/W	0h	ACNT : number of bytes in 1st dimension: ACNT represents the number of bytes within the first dimension of a transfer. ACNT is a 16-bit unsigned value with valid values between 0 and 65535. Therefore the maximum number of bytes in an array is 65535 bytes [64K-1 bytes]. ACNT must be greater than or equal to '1' for a TR to be submitted to TC. An ACNT of '0' is considered as either a null or dummy transfer. A Dummy or Null transfer will generate a Completion code depending on the settings of the completion bit fields of the OPT field. If the OPT.WIMODE bit is set then the ACNT field represents a word count. The CC must internally multiply by 4 to translate the word count to a byte count prior to submission to the TC. The 2 MSBs of the 16-bit ACNT are reserved and should always be written as 'b00 by the user. If user writes a value other than 0 it will still be treated as 0 since the multiply-by-4 operation [to translate between a word count and a byte count] will drop the 2 msbits. For dummy and null transfer definition the ACNT definition will disregard the 2 msbits. I.e. a programmed ACNT value of 0x8000 in WI-mode will be treated as 0 byte transfer resulting in null or dummy operation dependent on the state of BCNT and CCNT. Reset Source: edma_rst_mod_g_rst_n

4.28.115 TPCC_DST Registers

4.28.115.1 TPCC_DST Register (Offset = 400Ch) [reset = 0h]

Short Description: Destination Addr

Long Description: Destination Address

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Table 4-4699. Instance Table

Instance Name	Physical Address
EDMA0	52A0 400Ch

Figure 4-2229. DST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DST															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DST															
R/W															
0h															

Access Types Legend

Table 4-4700. DST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DST	R/W	0h	Destination Address: The 32-bit destination address parameters specify the starting byte address of the destination. If DAM is set to FIFO mode then the user should program the Destination address to be aligned to the value specified by the OPT.FWID field. No errors are recognized here but TC will assert error if this is not true. Reset Source: edma_rst_mod_g_rst_n

4.28.116 TPCC_BIDX Registers

4.28.116.1 TPCC_BIDX Register (Offset = 4010h) [reset = 0h]

Short Description: Register descrip

Long Description: Register description is not available

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Table 4-4701. Instance Table

Instance Name	Physical Address
EDMA0	52A0 4010h

Figure 4-2230. BIDX Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DBIDX															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SBIDX															
R/W															
0h															

Access Types Legend

Table 4-4702. BIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DBIDX	R/W	0h	Destination 2nd Dimension Index: DBIDX is a 16-bit signed value [2's complement] used for destination address modification in between each array in the 2nd dimension. It is a signed value between -32768 and 32767. It provides a byte address offset from the beginning of the destination array to the beginning of the next destination array within the current frame. It applies to both A-Sync and AB-Sync transfers. Reset Source: edma_rst_mod_g_rst_n
15:0	SBIDX	R/W	0h	Source 2nd Dimension Index: SBIDX is a 16-bit signed value [2's complement] used for source address modification in between each array in the 2nd dimension. It is a signed value between -32768 and 32767. It provides a byte address offset from the beginning of the source array to the beginning of the next source array. It applies to both A-sync and AB-sync transfers. Reset Source: edma_rst_mod_g_rst_n

4.28.117 TPCC_LNK Registers

4.28.117.1 TPCC_LNK Register (Offset = 4014h) [reset = 0h]

Short Description: Link and Reload

Long Description: Link and Reload parameters

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Table 4-4703. Instance Table

Instance Name	Physical Address
EDMA0	52A0 4014h

Figure 4-2231. LNK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BCNTRLD															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LINK															
R/W															
0h															

Access Types Legend

Table 4-4704. LNK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	BCNTRLD	R/W	0h	BCNT Reload: BCNTRLD is a 16-bit unsigned value used to reload the BCNT field once the last array in the 2nd dimension is transferred. This field is only used for A-Sync'ed transfers. In this case the CC decrements the BCNT value by one on each TR submission. When BCNT [conceptually] reaches zero then the CC decrements CCNT and uses the BCNTRLD value to reinitialize the BCNT value. For AB-synchronized transfers the CC submits the BCNT in the TR and therefore the TC is responsible to keep track of BCNT not thus BCNTRLD is a don't care field. Reset Source: edma_rst_mod_g_rst_n

Table 4-4704. LNK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:0	LINK	R/W	0h	Link Address: The CC provides a mechanism to reload the current PaRAM Entry upon its natural termination [i.e. after count fields are decremented to '0'] with a new PaRAM Entry. This is called 'linking'. The 16-bit parameter LINK specifies the byte address offset in the PaRAM from which the CC loads/reloads the next PaRAM entry in the link. The CC should disregard the value in the upper 2 bits of the LINK field as well as the lower 5-bits of the LINK field. The upper two bits are ignored such that the user can program either the 'literal' byte address of the LINK parameter or the 'PaRAM base-relative' address of the link field. Therefore if the user uses the literal address with a range from 0x4000 to 0x7FFF it will be treated as a PaRAM-base-relative value of 0x0000 to 0x3FFF. The lower-5 bits are ignored and treated as 'b00000 thereby guaranteeing that all Link pointers point to a 32-byte aligned PaRAM entry. In the latter case [5-lsbs] behavior is undefined for the user [i.e. don't have to test it]. In the former case [2 msbs] user should be able to take advantage of this feature [i.e. do have to test it]. If a Link Update is requested to a PaRAM address that is beyond the actual range of implemented PaRAM then the Link will be treated as a Null Linkand all 0s plus 0xFFFF will be written to the current entry location. A LINK value of 0xFFFF is referred to as a NULL link which should cause the CC to write 0x0 to all entries of the current PaRAM Entry except for the LINK field which is set to 0xFFFF. The Priv/Privid/Secure state is overwritten to 0x0 when linking. MSBs and LSBS should not be masked when comparing against the 0xFFFF value. I.e. a value of 0x3FFE is a non-NULL PaRAM link field. Reset Source: edma_rst_mod_g_rst_n

4.28.118 TPCC_CIDX Registers

4.28.118.1 TPCC_CIDX Register (Offset = 4018h) [reset = 0h]

Short Description: Register descrip

Long Description: Register description is not available

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Table 4-4705. Instance Table

Instance Name	Physical Address
EDMA0	52A0 4018h

Figure 4-2232. CIDX Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DCIDX															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCIDX															
R/W															
0h															

Access Types Legend

Table 4-4706. CIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DCIDX	R/W	0h	Destination Frame Index: DCIDX is a 16-bit signed value [2's complement] used for destination address modification for the 3rd dimension. It is a signed value between -32768 and 32767. It provides a byte address offset from the beginning of the current array [pointed to by DST address] to the beginning of the first destination array in the next frame. It applies to both A-sync and AB-sync transfers. Note that when DCIDX is applied the current array in an A-sync transfer is the last array in the frame while the current array in a ABsync transfer is the first array in the frame. Reset Source: edma_rst_mod_g_rst_n
15:0	SCIDX	R/W	0h	Source Frame Index: SCIDX is a 16-bit signed value [2's complement] used for source address modification for the 3rd dimension. It is a signed value between -32768 and 32767. It provides a byte address offset from the beginning of the current array [pointed to by SRC address] to the beginning of the first source array in the next frame. It applies to both A-sync and AB-sync transfers. Note that when SCIDX is applied the current array in an A-sync transfer is the last array in the frame while the current array in a AB-sync transfer is the first array in the frame. Reset Source: edma_rst_mod_g_rst_n

4.28.119 TPCC_CCNT Registers

4.28.119.1 TPCC_CCNT Register (Offset = 401Ch) [reset = 0h]

Short Description: C byte count

Long Description: C byte count

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Table 4-4707. Instance Table

Instance Name	Physical Address
EDMA0	52A0 401Ch

Figure 4-2233. CCNT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES86															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCNT															
R/W															
0h															

Access Types Legend

Table 4-4708. CCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES86	R	0h	RESERVE FIELD Reset Source: edma_rst_mod_g_rst_n
15:0	CCNT	R/W	0h	CCNT : Count for 3rd Dimension: CCNT is a 16-bit unsigned value that specifies the number of frames in a block. Valid values for CCNT can be anywhere between 1 and 65535. Therefore the maximum number of frames in a block is 65535 [64K-1 frames]. CCNT of '1' means '1' frame in the block and CCNT of '0' means '0' frames in the block. A CCNT value of '0' is considered as either a null or dummy transfer. A Dummy or Null transfer will generate a Completion code depending on the settings of the completion bit fields of the OPT field. WIMODE has no affect on CCNT operation. Reset Source: edma_rst_mod_g_rst_n

4.28.120 TPTC_PID Registers

4.28.120.1 TPTC_PID Register (Offset = 0h) [reset = 40000b01h]

Short Description: Peripheral ID Register

Long Description: Peripheral ID Register

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Table 4-4709. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0000h
EDMA1	52A4 0000h

Figure 4-2234. PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		RESERVED		FUNC											
R		NONE		R											
1h		0		0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
R					R			R		R					
1h					3h			0h		1h					

Access Types Legend

Table 4-4710. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID Scheme: Used to distinguish between old ID scheme and current. Spare bit to encode future schemes EDMA uses 'new scheme' indicated with value of 0x1. Reset Source: edma_rst_mod_g_rst_n
29:28	RESERVED	NONE		Reserved
27:16	FUNC	R	0h	Function indicates a software compatible module family. Reset Source: edma_rst_mod_g_rst_n
15:11	RTL	R	1h	RTL Version Reset Source: edma_rst_mod_g_rst_n
10:8	MAJOR	R	3h	Major Revision Reset Source: edma_rst_mod_g_rst_n
7:6	CUSTOM	R	0h	Custom revision field: Not used on this version of EDMA. Reset Source: edma_rst_mod_g_rst_n
5:0	MINOR	R	1h	Minor Revision Reset Source: edma_rst_mod_g_rst_n

4.28.121 TPTC_TCCFG Registers

4.28.121.1 TPTC_TCCFG Register (Offset = 4h) [reset = 224h]

Short Description: TC Configuration Registe

Long Description: TC Configuration Register

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Table 4-4711. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0004h
EDMA1	52A4 0004h

Figure 4-2235. TCCFG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
5f6081a															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						DREGDEPTH		RESERVED		BUSWIDTH		RESERVED	FIFOSIZE		
NONE						R		NONE		R		NONE	R		
5f6081a						2h		0		2h		0	4h		

Access Types Legend

Table 4-4712. TCCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9:8	DREGDEPTH	R	2h	Dst Register FIFO Depth Parameterization Reset Source: edma_rst_mod_g_rst_n
7:6	RESERVED	NONE		Reserved
5:4	BUSWIDTH	R	2h	Bus Width Parameterization Reset Source: edma_rst_mod_g_rst_n
3	RESERVED	NONE		Reserved
2:0	FIFOSIZE	R	4h	Fifo Size Parameterization Reset Source: edma_rst_mod_g_rst_n

4.28.122 TPTC_TCSTAT Registers

4.28.122.1 TPTC_TCSTAT Register (Offset = 100h) [reset = 100h]

Short Description: TC Status Register

Long Description: TC Status Register

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Table 4-4713. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0100h
EDMA1	52A4 0100h

Figure 4-2236. TCSTAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
989680															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		DFSTRTPTR		RESERVED			ACTV	RESERVED	DSTACTV			RESERVED	WSACTV	SRCACTV	PROGBUSY
NONE		R		NONE			R	NONE	R			NONE	R	R	R
989680		0h		0			1h	0	0h			0	0h	0h	0h

Access Types Legend

Table 4-4714. TCSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE		Reserved
13:12	DFSTRTPTR	R	0h	Dst FIFO Start Pointer Represents the offset to the head entry of Dst Register FIFO in units of entries. Legal values = 0x0 to 0x3 Reset Source: edma_rst_mod_g_rst_n
11:9	RESERVED	NONE		Reserved
8	ACTV	R	1h	Channel Active Channel Active is a logical-OR of each of the BUSY/ACTV signals. The ACTV bit must remain high through the life of a TR. ACTV = 0 : Channel is idle. ACTV = 1 : Channel is busy. Reset Source: edma_rst_mod_g_rst_n
7	RESERVED	NONE		Reserved
6:4	DSTACTV	R	0h	Destination Active State Specifies the number of TRs that are resident in the Dst Register FIFO at a given instant. Legal values are constrained by the DSTREGDEPTH parameter. Reset Source: edma_rst_mod_g_rst_n
3	RESERVED	NONE		Reserved
2	WSACTV	R	0h	Write Status Active WSACTV = 0 : Write status is not pending. Write status has been received for all previously issued write commands. WSACTV = 1 : Write Status is pending. Write status has not been received for all previously issued write commands. Reset Source: edma_rst_mod_g_rst_n
1	SRCACTV	R	0h	Source Active State SRCACTV = 0 : Source Active set is idle. Any TR written to Prog Set will immediately transition to Source Active set as long as the Dst FIFO Set is not full [DSTFULL == 1]. SRCACTV = 1 : Source Active set is busy either performing read transfers or waiting to perform read transfers for current Transfer Request. Reset Source: edma_rst_mod_g_rst_n

Table 4-4714. TCSTAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PROGBUSY	R	0h	Program Register Set Busy PROGBUSY = 0 : Prog set idle and is available for programming. PROGBUSY = 1 : Prog set busy. User should poll for PROGBUSY equal to '0' prior to re-programming the Program Register set. Reset Source: edma_rst_mod_g_rst_n

4.28.123 TPTC_INTSTAT Registers

4.28.123.1 TPTC_INTSTAT Register (Offset = 104h) [reset = 0h]

Short Description: Interrupt Status Registe

Long Description: Interrupt Status Register

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Table 4-4715. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0104h
EDMA1	52A4 0104h

Figure 4-2237. INTSTAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														TRDONE	PROGEMPTY
NONE														R	R
0														0h	0h

Access Types Legend

Table 4-4716. INTSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1	TRDONE	R	0h	TR Done Event Status: TRDONE = 0 : Condition not detected. TRDONE = 1 : Set when TC has completed a Transfer Request. TRDONE should be set when the write status is returned for the final write of a TR. Cleared when user writes '1' to INTCLR.TRDONE register bit. Reset Source: edma_rst_mod_g_rst_n
0	PROGEMPTY	R	0h	Program Set Empty Event Status: PROGEMPTY = 0 : Condition not detected. PROGEMPTY = 1 : Set when Program Register set transitions to empty state. Cleared when user writes '1' to INTCLR.PROGEMPTY register bit. Reset Source: edma_rst_mod_g_rst_n

4.28.124 TPTC_INTEN Registers

4.28.124.1 TPTC_INTEN Register (Offset = 108h) [reset = 0h]

Short Description: Interrupt Enable Registe

Long Description: Interrupt Enable Register

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Table 4-4717. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0108h
EDMA1	52A4 0108h

Figure 4-2238. INTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														TRDONE	PROGEMPTY
NONE														R/W	R/W
0														0h	0h

Access Types Legend

Table 4-4718. INTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1	TRDONE	R/W	0h	TR Done Event Enable: INTEN.TRDONE = 0 : TRDONE Event is disabled. INTEN.TRDONE = 1 : TRDONE Event is enabled and contributes to interrupt generation Reset Source: edma_rst_mod_g_rst_n
0	PROGEMPTY	R/W	0h	Program Set Empty Event Enable: INTEN.PROGEMPTY = 0 : PROGEMPTY Event is disabled. INTEN.PROGEMPTY = 1 : PROGEMPTY Event is enabled and contributes to interrupt generation Reset Source: edma_rst_mod_g_rst_n

4.28.125 TPTC_INTCLR Registers

4.28.125.1 TPTC_INTCLR Register (Offset = 10Ch) [reset = 0h]

Short Description: Interrupt Clear Register

Long Description: Interrupt Clear Register

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Table 4-4719. Instance Table

Instance Name	Physical Address
EDMA0	52A6 010Ch
EDMA1	52A4 010Ch

Figure 4-2239. INTCLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														TRDONE	PROGEMPTY
NONE														W	W
0														0h	0h

Access Types Legend

Table 4-4720. INTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1	TRDONE	W	0h	TR Done Event Clear: INTCLR.TRDONE = 0 : Writes of '0' have no effect. INTCLR.TRDONE = 1 : Write of '1' clears INTSTAT.TRDONE bit Reset Source: edma_rst_mod_g_rst_n
0	PROGEMPTY	W	0h	Program Set Empty Event Clear: INTCLR.PROGEMPTY = 0 : Writes of '0' have no effect. INTCLR.PROGEMPTY = 1 : Write of '1' clears INTSTAT.PROGEMPTY bit Reset Source: edma_rst_mod_g_rst_n

4.28.126 TPTC_INTCMD Registers

4.28.126.1 TPTC_INTCMD Register (Offset = 110h) [reset = 0h]

Short Description: Interrupt Command Regist

Long Description: Interrupt Command Register

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Table 4-4721. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0110h
EDMA1	52A4 0110h

Figure 4-2240. INTCMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														SET	EVAL
NONE														W	W
0														0h	0h

Access Types Legend

Table 4-4722. INTCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1	SET	W	0h	Set TPTC interrupt: Write of '1' to SET causes TPTC interrupt to be pulsed unconditionally. Writes of '0' have no affect. Reset Source: edma_rst_mod_g_rst_n
0	EVAL	W	0h	Evaluate state of TPTC interrupt Write of '1' to EVAL causes TPTC interrupt to be pulsed if any of the INTSTAT bits are set to '1'. Writes of '0' have no affect. Reset Source: edma_rst_mod_g_rst_n

4.28.127 TPTC_ERRSTAT Registers

4.28.127.1 TPTC_ERRSTAT Register (Offset = 120h) [reset = 0h]

Short Description: Error Status Register

Long Description: Error Status Register

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Table 4-4723. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0120h
EDMA1	52A4 0120h

Figure 4-2241. ERRSTAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												MMRAERR	TRERR	RESERVED	BUSERR
NONE												R	R	NONE	R
0												0h	0h	0	0h

Access Types Legend

Table 4-4724. ERRSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	MMRAERR	R	0h	MMR Address Error: MMRAERR = 0 : Condition not detected. MMRAERR = 1 : User attempted to read or write to invalid address configuration memory map. [Is only be set for non-emulation accesses]. No additional error information is recorded. Reset Source: edma_rst_mod_g_rst_n
2	TRERR	R	0h	TR Error: TR detected that violates FIFO Mode transfer [SAM or DAM is '1'] alignment rules or has ACNT or BCNT == 0. No additional error information is recorded. Reset Source: edma_rst_mod_g_rst_n
1	RESERVED	NONE		Reserved
0	BUSERR	R	0h	Bus Error Event: BUSERR = 0: Condition not detected. BUSERR = 1: TC has detected an error code on the write response bus or read response bus. Error information is stored in Error Details Register [ERRDET]. Reset Source: edma_rst_mod_g_rst_n

4.28.128 TPTC_ERREN Registers

4.28.128.1 TPTC_ERREN Register (Offset = 124h) [reset = 0h]

Short Description: Error Enable Register

Long Description: Error Enable Register

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Table 4-4725. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0124h
EDMA1	52A4 0124h

Figure 4-2242. ERREN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												MMRAERR	TRERR	RESERVED	BUSERR
NONE												R/W	R/W	NONE	R/W
0												0h	0h	0	0h

Access Types Legend

Table 4-4726. ERREN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	MMRAERR	R/W	0h	Interrupt enable for ERRSTAT.MMRAERR: ERREN.MMRAERR = 0 : BUSERR is disabled. ERREN.MMRAERR = 1 : MMRAERR is enabled and contributes to the TPTC error interrupt generation. Reset Source: edma_rst_mod_g_rst_n
2	TRERR	R/W	0h	Interrupt enable for ERRSTAT.TRERR: ERREN.TRERR = 0 : BUSERR is disabled. ERREN.TRERR = 1 : TRERR is enabled and contributes to the TPTC error interrupt generation. Reset Source: edma_rst_mod_g_rst_n
1	RESERVED	NONE		Reserved
0	BUSERR	R/W	0h	Interrupt enable for ERRSTAT.BUSERR: ERREN.BUSERR = 0 : BUSERR is disabled. ERREN.BUSERR = 1 : BUSERR is enabled and contributes to the TPTC error interrupt generation. Reset Source: edma_rst_mod_g_rst_n

4.28.129 TPTC_ERRCLR Registers

4.28.129.1 TPTC_ERRCLR Register (Offset = 128h) [reset = 0h]

Short Description: Error Clear Register

Long Description: Error Clear Register

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Table 4-4727. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0128h
EDMA1	52A4 0128h

Figure 4-2243. ERRCLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												MMRAERR	TRERR	RESERVED	BUSERR
NONE												W	W	NONE	W
0												0h	0h	0	0h

Access Types Legend

Table 4-4728. ERRCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE		Reserved
3	MMRAERR	W	0h	Interrupt clear for ERRSTAT.MMRAERR: ERRCLR.MMRAERR = 0 : Writes of '0' have no effect. ERRCLR.MMRAERR = 1 : Write of '1' clears ERRSTAT.MMRAERR bit. Write of '1' to ERRCLR.MMRAERR does not clear the ERRDET register. Reset Source: edma_rst_mod_g_rst_n
2	TRERR	W	0h	Interrupt clear for ERRSTAT.TRERR: ERRCLR.TRERR = 0 : Writes of '0' have no effect. ERRCLR.TRERR = 1 : Write of '1' clears ERRSTAT.TRERR bit. Write of '1' to ERRCLR.TRERR does not clear the ERRDET register. Reset Source: edma_rst_mod_g_rst_n
1	RESERVED	NONE		Reserved
0	BUSERR	W	0h	Interrupt clear for ERRSTAT.BUSERR: ERRCLR.BUSERR = 0 : Writes of '0' have no effect. ERRCLR.BUSERR = 1 : Write of '1' clears ERRSTAT.BUSERR bit. Write of '1' to ERRCLR.BUSERR clears the ERRDET register. Reset Source: edma_rst_mod_g_rst_n

4.28.130 TPTC_ERRDET Registers

4.28.130.1 TPTC_ERRDET Register (Offset = 12Ch) [reset = 0h]

Short Description: Error Details Register

Long Description: Error Details Register

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Table 4-4729. Instance Table

Instance Name	Physical Address
EDMA0	52A6 012Ch
EDMA1	52A4 012Ch

Figure 4-2244. ERRDET Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														TCCHEN	TCINTEN
NONE														R	R
0														0h	0h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TCC						RESERVED				STAT			
NONE		R						NONE				R			
0		0h						0				0h			

Access Types Legend

Table 4-4730. ERRDET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE		Reserved
17	TCCHEN	R	0h	Contains the OPT.TCCHEN value programmed by the user for the Read or Write transaction that resulted in an error. Reset Source: edma_rst_mod_g_rst_n
16	TCINTEN	R	0h	Contains the OPT.TCINTEN value programmed by the user for the Read or Write transaction that resulted in an error. Reset Source: edma_rst_mod_g_rst_n
15:14	RESERVED	NONE		Reserved
13:8	TCC	R	0h	Transfer Complete Code: Contains the OPT.TCC value programmed by the user for the Read or Write transaction that resulted in an error. Reset Source: edma_rst_mod_g_rst_n
7:4	RESERVED	NONE		Reserved
3:0	STAT	R	0h	Transaction Status: Stores the non-zero status/error code that was detected on the read status or write status bus. MS-bit effectively serves as the read vs. write error code. If read status and write status are returned on the same cycle then the TC chooses non-zero version. If both are non-zero then write status is treated as higher priority. Encoding of errors matches the CBA spec. Reset Source: edma_rst_mod_g_rst_n

4.28.131 TPTC_ERRCMD Registers

4.28.131.1 TPTC_ERRCMD Register (Offset = 130h) [reset = 0h]

Short Description: Error Command Register

Long Description: Error Command Register

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Table 4-4731. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0130h
EDMA1	52A4 0130h

Figure 4-2245. ERRCMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														SET	EVAL
NONE														W	W
0														0h	0h

Access Types Legend

Table 4-4732. ERRCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE		Reserved
1	SET	W	0h	Set TPTC error interrupt: Write of '1' to SET causes TPTC error interrupt to be pulsed unconditionally. Writes of '0' have no affect. Reset Source: edma_rst_mod_g_rst_n
0	EVAL	W	0h	Evaluate state of TPTC error interrupt Write of '1' to EVAL causes TPTC error interrupt to be pulsed if any of the ERRSTAT bits are set to '1'. Writes of '0' have no affect. Reset Source: edma_rst_mod_g_rst_n

4.28.132 TPTC_RDRATE Registers

4.28.132.1 TPTC_RDRATE Register (Offset = 140h) [reset = 0h]

Short Description: Read Rate Register

Long Description: Read Rate Register

Return to Summary Table

Table 4-4733. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0140h
EDMA1	52A4 0140h

Figure 4-2246. RDRATE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													RDRATE		
NONE													R/W		
0													0h		

Access Types Legend

Table 4-4734. RDRATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE		Reserved
2:0	RDRATE	R/W	0h	Read Rate Control: Controls the number of cycles between read commands. This is a global setting that applies to all TRs for this TC. Reset Source: edma_rst_mod_g_rst_n

4.28.133 TPTC_POPT Registers

4.28.133.1 TPTC_POPT Register (Offset = 200h) [reset = 0h]

Short Description: Prog Set Options

Long Description: Prog Set Options

Return to Summary Table

Table 4-4735. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0200h
EDMA1	52A4 0200h

Figure 4-2247. POPT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		DBG_ID		RESERVED					TCCHEN	RESERVED	TCINTEN	RESERVED		TCC	
NONE		R/W		NONE					R/W	NONE	R/W	NONE		R/W	
0		0h		0					0h	0	0h	0		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCC				RESERVED	FWID			RESERVED	PRI			RESERVED		DAM	SAM
R/W				NONE	R/W			NONE	R/W			NONE		R/W	R/W
0h				0	0h			0	0h			0		0h	0h

Access Types Legend

Table 4-4736. POPT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE		Reserved
29:28	DBG_ID	R/W	0h	Debug ID Value driven on the read [tptc_r_dbg_channel_id] and write [tptc_w_dbg_channel_id] command bus. Used at system level for trace/profiling of user selected transfers in systems that include this feature. Reset Source: edma_rst_mod_g_rst_n
27:23	RESERVED	NONE		Reserved
22	TCCHEN	R/W	0h	Transfer complete chaining enable: 0: Transfer complete chaining is disabled. 1: Transfer complete chaining is enabled. Reset Source: edma_rst_mod_g_rst_n
21	RESERVED	NONE		Reserved
20	TCINTEN	R/W	0h	Transfer complete interrupt enable: 0: Transfer complete interrupt is disabled. 1: Transfer complete interrupt is enabled. Reset Source: edma_rst_mod_g_rst_n
19:18	RESERVED	NONE		Reserved
17:12	TCC	R/W	0h	Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER or IPR of the TPCC module. Reset Source: edma_rst_mod_g_rst_n
11	RESERVED	NONE		Reserved
10:8	FWID	R/W	0h	FIFO width control: Applies if either SAM or DAM is set to FIFO mode. Reset Source: edma_rst_mod_g_rst_n
7	RESERVED	NONE		Reserved
6:4	PRI	R/W	0h	Transfer Priority: 0: Priority 0 - Highest priority 1: Priority 1 ... 7: Priority 7 - Lowest priority Reset Source: edma_rst_mod_g_rst_n
3:2	RESERVED	NONE		Reserved

Table 4-4736. POPT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DAM	R/W	0h	Destination Address Mode within an array: 0: INCR Dst addressing within an array increments. 1: FIFO Dst addressing within an array wraps around upon reaching FIFO width. Reset Source: edma_rst_mod_g_rst_n
0	SAM	R/W	0h	Source Address Mode within an array: 0: INCR Src addressing within an array increments. 1: FIFO Src addressing within an array wraps around upon reaching FIFO width. Reset Source: edma_rst_mod_g_rst_n

4.28.134 TPTC_PSRC Registers

4.28.134.1 TPTC_PSRC Register (Offset = 204h) [reset = 0h]

Short Description: Prog Set Src Address

Long Description: Prog Set Src Address

Return to Summary Table

Table 4-4737. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0204h
EDMA1	52A4 0204h

Figure 4-2248. PSRC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SADDR															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SADDR															
R/W															
0h															

Access Types Legend

Table 4-4738. PSRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SADDR	R/W	0h	Source address for Program Register Set Reset Source: edma_rst_mod_g_rst_n

4.28.135 TPTC_PCNT Registers

4.28.135.1 TPTC_PCNT Register (Offset = 208h) [reset = 0h]

Short Description: Prog Set Count

Long Description: Prog Set Count

Return to Summary Table

Table 4-4739. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0208h
EDMA1	52A4 0208h

Figure 4-2249. PCNT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BCNT															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACNT															
R/W															
0h															

Access Types Legend

Table 4-4740. PCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	BCNT	R/W	0h	B-Dimension count. Number of arrays to be transferred where each array is ACNT in length. Reset Source: edma_rst_mod_g_rst_n
15:0	ACNT	R/W	0h	A-Dimension count. Number of bytes to be transferred in first dimension. Reset Source: edma_rst_mod_g_rst_n

4.28.136 TPTC_PDST Registers

4.28.136.1 TPTC_PDST Register (Offset = 20Ch) [reset = 0h]

Short Description: Prog Set Dst Address

Long Description: Prog Set Dst Address

Return to Summary Table

Table 4-4741. Instance Table

Instance Name	Physical Address
EDMA0	52A6 020Ch
EDMA1	52A4 020Ch

Figure 4-2250. PDST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DADDR															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DADDR															
R/W															
0h															

Access Types Legend

Table 4-4742. PDST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DADDR	R/W	0h	Destination address for Program Register Set Reset Source: edma_rst_mod_g_rst_n

4.28.137 TPTC_PBIDX Registers

4.28.137.1 TPTC_PBIDX Register (Offset = 210h) [reset = 0h]

Short Description: Prog Set B-Dim Idx

Long Description: Prog Set B-Dim Idx

Return to Summary Table

Table 4-4743. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0210h
EDMA1	52A4 0210h

Figure 4-2251. PBIDX Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DBIDX															
R/W															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SBIDX															
R/W															
0h															

Access Types Legend

Table 4-4744. PBIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DBIDX	R/W	0h	Dest B-Idx for Program Register Set: B-Idx offset between Destination arrays: Represents the offset in bytes between the starting address of each destination array [recall that there are BCNT arrays of ACNT elements]. DBIDX is always used regardless of whether DAM is Increment or FIFO mode. Reset Source: edma_rst_mod_g_rst_n
15:0	SBIDX	R/W	0h	Source B-Idx for Program Register Set: B-Idx offset between Source arrays: Represents the offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT elements]. SBIDX is always used regardless of whether SAM is Increment or FIFO mode. Reset Source: edma_rst_mod_g_rst_n

4.28.138 TPTC_PMPPRXY Registers

4.28.138.1 TPTC_PMPPRXY Register (Offset = 214h) [reset = 0h]

Short Description: Prog Set Mem Protect Pro

Long Description: Prog Set Mem Protect Proxy

Return to Summary Table

Table 4-4745. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0214h
EDMA1	52A4 0214h

Figure 4-2252. PMPPRXY Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						SECURE	PRIV	RESERVED				PRIVID			
NONE						R	R	NONE				R			
0						0h	0h	0				0h			

Access Types Legend

Table 4-4746. PMPPRXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9	SECURE	R	0h	Secure Level: Deprecated, always read as 0. Reset Source: edma_rst_mod_g_rst_n
8	PRIV	R	0h	Privilege Level: PRIV = 0 : User level privilege PRIV = 1 : Supervisor level privilege PMPPRXY.PRIV is always updated with the value from the configuration bus privilege field on any/every write to Program Set BIDX Register [trigger register]. The PRIV value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the PRIV of the external host that sets up the DMA transaction. Reset Source: edma_rst_mod_g_rst_n
7:4	RESERVED	NONE		Reserved
3:0	PRIVID	R	0h	Privilege ID: PMPPRXY.PRIVID is always updated with the value from configuration bus privilege ID field on any/every write to Program Set BIDX Register [trigger register]. The PRIVID value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the privid of the external host that sets up the DMA transaction. Reset Source: edma_rst_mod_g_rst_n

4.28.139 TPTC_SAOPT Registers

4.28.139.1 TPTC_SAOPT Register (Offset = 240h) [reset = 0h]

Short Description: Src Actv Set Options

Long Description: Src Actv Set Options

Return to Summary Table

Table 4-4747. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0240h
EDMA1	52A4 0240h

Figure 4-2253. SAOPT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		DBG_ID		RESERVED					TCCHEN	RESERVED	TCINTEN	RESERVED		TCC	
NONE		R		NONE					R	NONE	R	NONE		R	
0		0h		0					0h	0	0h	0		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCC				RESERVED	FWID			RESERVED	PRI			RESERVED		DAM	SAM
R				NONE	R			NONE	R			NONE		R	R
0h				0	0h			0	0h			0		0h	0h

Access Types Legend

Table 4-4748. SAOPT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE		Reserved
29:28	DBG_ID	R	0h	Debug ID Value driven on the read [tptc_r_dbg_channel_id] and write [tptc_w_dbg_channel_id] command bus. Used at system level for trace/profiling of user selected transfers in systems that include this feature. Reset Source: edma_rst_mod_g_rst_n
27:23	RESERVED	NONE		Reserved
22	TCCHEN	R	0h	Transfer complete chaining enable: 0: Transfer complete chaining is disabled. 1: Transfer complete chaining is enabled. Reset Source: edma_rst_mod_g_rst_n
21	RESERVED	NONE		Reserved
20	TCINTEN	R	0h	Transfer complete interrupt enable: 0: Transfer complete interrupt is disabled. 1: Transfer complete interrupt is enabled. Reset Source: edma_rst_mod_g_rst_n
19:18	RESERVED	NONE		Reserved
17:12	TCC	R	0h	Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER or IPR of the TPCC module. Reset Source: edma_rst_mod_g_rst_n
11	RESERVED	NONE		Reserved
10:8	FWID	R	0h	FIFO width control: Applies if either SAM or DAM is set to FIFO mode. Reset Source: edma_rst_mod_g_rst_n
7	RESERVED	NONE		Reserved
6:4	PRI	R	0h	Transfer Priority: 0: Priority 0 - Highest priority 1: Priority 1 ... 7: Priority 7 - Lowest priority Reset Source: edma_rst_mod_g_rst_n
3:2	RESERVED	NONE		Reserved

Table 4-4748. SAOPT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DAM	R	0h	Destination Address Mode within an array: 0: INCR Dst addressing within an array increments. 1: FIFO Dst addressing within an array wraps around upon reaching FIFO width. Reset Source: edma_rst_mod_g_rst_n
0	SAM	R	0h	Source Address Mode within an array: 0: INCR Src addressing within an array increments. 1: FIFO Src addressing within an array wraps around upon reaching FIFO width. Reset Source: edma_rst_mod_g_rst_n

4.28.140 TPTC_SASRC Registers

4.28.140.1 TPTC_SASRC Register (Offset = 244h) [reset = 0h]

Short Description: Src Actv Set Src Address

Long Description: Src Actv Set Src Address

Return to Summary Table

Table 4-4749. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0244h
EDMA1	52A4 0244h

Figure 4-2254. SASRC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SADDR															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SADDR															
R															
0h															

Access Types Legend

Table 4-4750. SASRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SADDR	R	0h	Source address for Source Active Register Set Reset Source: edma_rst_mod_g_rst_n

4.28.141 TPTC_SACNT Registers

4.28.141.1 TPTC_SACNT Register (Offset = 248h) [reset = 0h]

Short Description: Src Actv Set A-Count

Long Description: Src Actv Set A-Count

Return to Summary Table

Table 4-4751. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0248h
EDMA1	52A4 0248h

Figure 4-2255. SACNT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED									ACNT						
NONE									R						
0									0h						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACNT															
R															
0h															

Access Types Legend

Table 4-4752. SACNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE		Reserved
22:0	ACNT	R	0h	A-Dimension count. Number of bytes to be transferred in first dimension. Reset Source: edma_rst_mod_g_rst_n

4.28.142 TPTC_SADST Registers

4.28.142.1 TPTC_SADST Register (Offset = 24Ch) [reset = 0h]

Short Description: Src Actv Set Dst Address

Long Description: Src Actv Set Dst Address

Return to Summary Table

Table 4-4753. Instance Table

Instance Name	Physical Address
EDMA0	52A6 024Ch
EDMA1	52A4 024Ch

Figure 4-2256. SADST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DADDR															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DADDR															
R															
0h															

Access Types Legend

Table 4-4754. SADST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DADDR	R	0h	Destination address for Source Active Register Set Reset Source: edma_rst_mod_g_rst_n

4.28.143 TPTC_SABIDX Registers

4.28.143.1 TPTC_SABIDX Register (Offset = 250h) [reset = 0h]

Short Description: Src Actv Set B-Dim Idx

Long Description: Src Actv Set B-Dim Idx

Return to Summary Table

Table 4-4755. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0250h
EDMA1	52A4 0250h

Figure 4-2257. SABIDX Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DBIDX															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SBIDX															
R															
0h															

Access Types Legend

Table 4-4756. SABIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DBIDX	R	0h	Dest B-Idx for Source Active Register Set: B-Idx offset between Destination arrays: Represents the offset in bytes between the starting address of each destination array [recall that there are BCNT arrays of ACNT elements]. DBIDX is always used regardless of whether DAM is Increment or FIFO mode. Reset Source: edma_rst_mod_g_rst_n
15:0	SBIDX	R	0h	Source B-Idx for Source Active Register Set: B-Idx offset between Source arrays: Represents the offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT elements]. SBIDX is always used regardless of whether SAM is Increment or FIFO mode. Reset Source: edma_rst_mod_g_rst_n

4.28.144 TPTC_SAMPPRXY Registers

4.28.144.1 TPTC_SAMPPRXY Register (Offset = 254h) [reset = 0h]

Short Description: Src Actv Set Mem Protect

Long Description: Src Actv Set Mem Protect Proxy

Return to Summary Table

Table 4-4757. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0254h
EDMA1	52A4 0254h

Figure 4-2258. SAMPPRXY Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						SECURE	PRIV	RESERVED				PRIVID			
NONE						R	R	NONE				R			
0						0h	0h	0				0h			

Access Types Legend

Table 4-4758. SAMPPRXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9	SECURE	R	0h	Secure Level: Deprecated, always read as 0. Reset Source: edma_rst_mod_g_rst_n
8	PRIV	R	0h	Privilege Level: PRIV = 0 : User level privilege PRIV = 1 : Supervisor level privilege PMPPRXY.PRIV is always updated with the value from the configuration bus privilege field on any/every write to Program Set BIDX Register [trigger register]. The PRIV value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the PRIV of the external host that sets up the DMA transaction. Reset Source: edma_rst_mod_g_rst_n
7:4	RESERVED	NONE		Reserved
3:0	PRIVID	R	0h	Privilege ID: PMPPRXY.PRIVID is always updated with the value from configuration bus privilege ID field on any/every write to Program Set BIDX Register [trigger register]. The PRIVID value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the privid of the external host that sets up the DMA transaction. Reset Source: edma_rst_mod_g_rst_n

4.28.145 TPTC_SACNTRLD Registers

4.28.145.1 TPTC_SACNTRLD Register (Offset = 258h) [reset = 0h]

Short Description: Src Actv Set Cnt Reload

Long Description: Src Actv Set Cnt Reload

Return to Summary Table

Table 4-4759. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0258h
EDMA1	52A4 0258h

Figure 4-2259. SACNTRLD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACNTRLD															
R															
0h															

Access Types Legend

Table 4-4760. SACNTRLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	ACNTRLD	R	0h	A-Cnt Reload value for Source Active Register set. Value copied from PCNT.ACNT: Represents the originally programmed value of ACNT. The Reload value is used to reinitialize ACNT after each array is serviced [i.e. ACNT decrements to 0]. by the Src offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT bytes] Reset Source: edma_rst_mod_g_rst_n

4.28.146 TPTC_SASRCBREF Registers

4.28.146.1 TPTC_SASRCBREF Register (Offset = 25Ch) [reset = 0h]

Short Description: Src Actv Set Src Addr B-

Long Description: Src Actv Set Src Addr B-Reference

Return to Summary Table

Table 4-4761. Instance Table

Instance Name	Physical Address
EDMA0	52A6 025Ch
EDMA1	52A4 025Ch

Figure 4-2260. SASRCBREF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SADDRBREF															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SADDRBREF															
R															
0h															

Access Types Legend

Table 4-4762. SASRCBREF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SADDRBREF	R	0h	Source address reference for Source Active Register Set: Represents the starting address for the array currently being read. The next array's starting address is calculated as the 'reference address' plus the 'source b-idx' value. Reset Source: edma_rst_mod_g_rst_n

4.28.147 TPTC_SADSTBREF Registers

4.28.147.1 TPTC_SADSTBREF Register (Offset = 260h) [reset = 0h]

Short Description: Src Actv Set Dst Addr B-

Long Description: Src Actv Set Dst Addr B-Reference

Return to Summary Table

Table 4-4763. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0260h
EDMA1	52A4 0260h

Figure 4-2261. SADSTBREF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DADDRBREF															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DADDRBREF															
R															
0h															

Access Types Legend

Table 4-4764. SADSTBREF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DADDRBREF	R	0h	Dst address reference is not applicable for Src Active Register Set. Reads return 0x0. Reset Source: edma_rst_mod_g_rst_n

4.28.148 TPTC_SABCNT Registers

4.28.148.1 TPTC_SABCNT Register (Offset = 264h) [reset = 0h]

Short Description: Src Actv Set B-Count

Long Description: Src Actv Set B-Count

Return to Summary Table

Table 4-4765. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0264h
EDMA1	52A4 0264h

Figure 4-2262. SABCNT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCNT															
R															
0h															

Access Types Legend

Table 4-4766. SABCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	BCNT	R	0h	B-Dimension count: Number of arrays to be transferred where each array is ACNT in length. Count Remaining for Src Active Register Set. Represents the amount of data remaining to be read. Initial value is copied from PCNT. TC decrements ACNT and BCNT as necessary after each read command is issued. Final value should be 0 when TR is complete. Reset Source: edma_rst_mod_g_rst_n

4.28.149 TPTC_DFCNTRLD Registers

4.28.149.1 TPTC_DFCNTRLD Register (Offset = 280h) [reset = 0h]

Short Description: Dst FIFO Set Cnt Reload

Long Description: Dst FIFO Set Cnt Reload

Return to Summary Table

Table 4-4767. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0280h
EDMA1	52A4 0280h

Figure 4-2263. DFCNTRLD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACNTRLD															
R															
0h															

Access Types Legend

Table 4-4768. DFCNTRLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	ACNTRLD	R	0h	A-Cnt Reload value for Destination FIFO Register set. Value copied from PCNT.ACNT: Represents the originally programmed value of ACNT. The Reload value is used to reinitialize ACNT after each array is serviced [i.e. ACNT decrements to 0]. by the Src offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT bytes] Reset Source: edma_rst_mod_g_rst_n

4.28.150 TPTC_DFSRCBREF Registers

4.28.150.1 TPTC_DFSRCBREF Register (Offset = 284h) [reset = 0h]

Short Description: Dst FIFO Set Src Addr B-

Long Description: Dst FIFO Set Src Addr B-Reference

Return to Summary Table

Table 4-4769. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0284h
EDMA1	52A4 0284h

Figure 4-2264. DFSRCBREF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SADDRBREF															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SADDRBREF															
R															
0h															

Access Types Legend

Table 4-4770. DFSRCBREF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SADDRBREF	R	0h	Source address reference for Destination FIFO Register Set: Represents the starting address for the array currently being read. The next array's starting address is calculated as the 'reference address' plus the 'source b-idx' value. Reset Source: edma_rst_mod_g_rst_n

4.28.151 TPTC_DFOPT0 Registers

4.28.151.1 TPTC_DFOPT0 Register (Offset = 300h) [reset = 0h]

Short Description: Dst FIFO Set Options

Long Description: Dst FIFO Set Options

Return to Summary Table

Table 4-4771. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0300h
EDMA1	52A4 0300h

Figure 4-2265. DFOPT0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		DBG_ID		RESERVED					TCCHEN	RESERVED	TCINTEN	RESERVED		TCC	
NONE		R		NONE					R	NONE	R	NONE		R	
0		0h		0					0h	0	0h	0		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCC				RESERVED	FWID			RESERVED	PRI			RESERVED		DAM	SAM
R				NONE	R			NONE	R			NONE		R	R
0h				0	0h			0	0h			0		0h	0h

Access Types Legend

Table 4-4772. DFOPT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE		Reserved
29:28	DBG_ID	R	0h	Debug ID Value driven on the read [tptc_r_dbg_channel_id] and write [tptc_w_dbg_channel_id] command bus. Used at system level for trace/profiling of user selected transfers in systems that include this feature. Reset Source: edma_rst_mod_g_rst_n
27:23	RESERVED	NONE		Reserved
22	TCCHEN	R	0h	Transfer complete chaining enable: 0: Transfer complete chaining is disabled. 1: Transfer complete chaining is enabled. Reset Source: edma_rst_mod_g_rst_n
21	RESERVED	NONE		Reserved
20	TCINTEN	R	0h	Transfer complete interrupt enable: 0: Transfer complete interrupt is disabled. 1: Transfer complete interrupt is enabled. Reset Source: edma_rst_mod_g_rst_n
19:18	RESERVED	NONE		Reserved
17:12	TCC	R	0h	Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER or IPR of the TPCC module. Reset Source: edma_rst_mod_g_rst_n
11	RESERVED	NONE		Reserved
10:8	FWID	R	0h	FIFO width control: Applies if either SAM or DAM is set to FIFO mode. Reset Source: edma_rst_mod_g_rst_n
7	RESERVED	NONE		Reserved
6:4	PRI	R	0h	Transfer Priority: 0: Priority 0 - Highest priority 1: Priority 1 ... 7: Priority 7 - Lowest priority Reset Source: edma_rst_mod_g_rst_n
3:2	RESERVED	NONE		Reserved

Table 4-4772. DFOPT0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DAM	R	0h	Destination Address Mode within an array: 0: INCR Dst addressing within an array increments. 1: FIFO Dst addressing within an array wraps around upon reaching FIFO width. Reset Source: edma_rst_mod_g_rst_n
0	SAM	R	0h	Source Address Mode within an array: 0: INCR Src addressing within an array increments. 1: FIFO Src addressing within an array wraps around upon reaching FIFO width. Reset Source: edma_rst_mod_g_rst_n

4.28.152 TPTC_DFSRC0 Registers

4.28.152.1 TPTC_DFSRC0 Register (Offset = 304h) [reset = 0h]

Short Description: Dst FIFO Set Src Address

Long Description: Dst FIFO Set Src Address

Return to Summary Table

Table 4-4773. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0304h
EDMA1	52A4 0304h

Figure 4-2266. DFSRC0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SADDR															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SADDR															
R															
0h															

Access Types Legend

Table 4-4774. DFSRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SADDR	R	0h	Source address is not applicable for Dst FIFO Register Set: Reads return 0x0. Reset Source: edma_rst_mod_g_rst_n

4.28.153 TPTC_DFACNT0 Registers

4.28.153.1 TPTC_DFACNT0 Register (Offset = 308h) [reset = 0h]

Short Description: Dst FIFO Set A-Count

Long Description: Dst FIFO Set A-Count

Return to Summary Table

Table 4-4775. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0308h
EDMA1	52A4 0308h

Figure 4-2267. DFACNT0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED									ACNT						
NONE									R						
0									0h						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACNT															
R															
0h															

Access Types Legend

Table 4-4776. DFACNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE		Reserved
22:0	ACNT	R	0h	A-Dimension count. Number of bytes to be transferred infirst dimension. Reset Source: edma_rst_mod_g_rst_n

4.28.154 TPTC_DFDST0 Registers

4.28.154.1 TPTC_DFDST0 Register (Offset = 30Ch) [reset = 0h]

Short Description: Dst FIFO Set Dst Address

Long Description: Dst FIFO Set Dst Address

Return to Summary Table

Table 4-4777. Instance Table

Instance Name	Physical Address
EDMA0	52A6 030Ch
EDMA1	52A4 030Ch

Figure 4-2268. DFDST0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DADDR															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DADDR															
R															
0h															

Access Types Legend

Table 4-4778. DFDST0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DADDR	R	0h	Destination address for Dst FIFO Register Set: Initial value is copied from PDST.DADDR. TC updates value according to destination addressing mode [OPT.SAM] and/or dest index value [BIDX.DBIDX] after each write command is issued. When a TR is complete the final value should be the address of the last write command issued. Reset Source: edma_rst_mod_g_rst_n

4.28.155 TPTC_DFBIDX0 Registers

4.28.155.1 TPTC_DFBIDX0 Register (Offset = 310h) [reset = 0h]

Short Description: Dst FIFO Set B-Dim Idx

Long Description: Dst FIFO Set B-Dim Idx

Return to Summary Table

Table 4-4779. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0310h
EDMA1	52A4 0310h

Figure 4-2269. DFBIDX0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DBIDX															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SBIDX															
R															
0h															

Access Types Legend

Table 4-4780. DFBIDX0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DBIDX	R	0h	Dest B-Idx for Dest FIFO Register Set. Value copied from PBIDX: B-Idx offset between Destination arrays: Represents the offset in bytes between the starting address of each destination array [recall that there are BCNT arrays of ACNT elements]. DBIDX is always used regardless of whether DAM is Increment or FIFO mode. Reset Source: edma_rst_mod_g_rst_n
15:0	SBIDX	R	0h	Src B-Idx for Dest FIFO Register Set. Value copied from PBIDX: B-Idx offset between Source arrays: Represents the offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT elements]. SBIDX is always used regardless of whether SAM is Increment or FIFO mode. Reset Source: edma_rst_mod_g_rst_n

4.28.156 TPTC_DFMPPRXY0 Registers

4.28.156.1 TPTC_DFMPPRXY0 Register (Offset = 314h) [reset = 0h]

Short Description: Dst FIFO Set Mem Protect

Long Description: Dst FIFO Set Mem Protect Proxy

Return to Summary Table

Table 4-4781. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0314h
EDMA1	52A4 0314h

Figure 4-2270. DFMPPRXY0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						SECURE	PRIV	RESERVED				PRIVID			
NONE						R	R	NONE				R			
0						0h	0h	0				0h			

Access Types Legend

Table 4-4782. DFMPPRXY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9	SECURE	R	0h	Secure Level: Deprecated, always read as 0. Reset Source: edma_rst_mod_g_rst_n
8	PRIV	R	0h	Privilege Level: PRIV = 0 : User level privilege PRIV = 1 : Supervisor level privilege PMPPRXY.PRIV is always updated with the value from the configuration bus privilege field on any/every write to Program Set BIDX Register [trigger register]. The PRIV value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the PRIV of the external host that sets up the DMA transaction. Reset Source: edma_rst_mod_g_rst_n
7:4	RESERVED	NONE		Reserved
3:0	PRIVID	R	0h	Privilege ID: PMPPRXY.PRIVID is always updated with the value from configuration bus privilege ID field on any/every write to Program Set BIDX Register [trigger register]. The PRIVID value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the privid of the external host that sets up the DMA transaction. Reset Source: edma_rst_mod_g_rst_n

4.28.157 TPTC_DFBCNT0 Registers

4.28.157.1 TPTC_DFBCNT0 Register (Offset = 318h) [reset = 0h]

Short Description: Dst FIFO Set B-Count

Long Description: Dst FIFO Set B-Count

Return to Summary Table

Table 4-4783. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0318h
EDMA1	52A4 0318h

Figure 4-2271. DFBCNT0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCNT															
R															
0h															

Access Types Legend

Table 4-4784. DFBCNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	BCNT	R	0h	B-Count Remaining for Dst Register Set: Number of arrays to be transferred where each array is ACNT in length. Represents the amount of data remaining to be written. Initial value is copied from PCNT. TC decrements ACNT and BCNT as necessary after each write dataphase is issued. Final value should be 0 when TR is complete. Reset Source: edma_rst_mod_g_rst_n

4.28.158 TPTC_DFOPT1 Registers

4.28.158.1 TPTC_DFOPT1 Register (Offset = 340h) [reset = 0h]

Short Description: Dst FIFO Set Options

Long Description: Dst FIFO Set Options

Return to Summary Table

Table 4-4785. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0340h
EDMA1	52A4 0340h

Figure 4-2272. DFOPT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		DBG_ID		RESERVED					TCCHEN	RESERVED	TCINTEN	RESERVED		TCC	
NONE		R		NONE					R	NONE	R	NONE		R	
0		0h		0					0h	0	0h	0		0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCC				RESERVED	FWID			RESERVED	PRI			RESERVED		DAM	SAM
R				NONE	R			NONE	R			NONE		R	R
0h				0	0h			0	0h			0		0h	0h

Access Types Legend

Table 4-4786. DFOPT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE		Reserved
29:28	DBG_ID	R	0h	Debug ID Value driven on the read [tptc_r_dbg_channel_id] and write [tptc_w_dbg_channel_id] command bus. Used at system level for trace/profiling of user selected transfers in systems that include this feature. Reset Source: edma_rst_mod_g_rst_n
27:23	RESERVED	NONE		Reserved
22	TCCHEN	R	0h	Transfer complete chaining enable: 0: Transfer complete chaining is disabled. 1: Transfer complete chaining is enabled. Reset Source: edma_rst_mod_g_rst_n
21	RESERVED	NONE		Reserved
20	TCINTEN	R	0h	Transfer complete interrupt enable: 0: Transfer complete interrupt is disabled. 1: Transfer complete interrupt is enabled. Reset Source: edma_rst_mod_g_rst_n
19:18	RESERVED	NONE		Reserved
17:12	TCC	R	0h	Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER or IPR of the TPCC module. Reset Source: edma_rst_mod_g_rst_n
11	RESERVED	NONE		Reserved
10:8	FWID	R	0h	FIFO width control: Applies if either SAM or DAM is set to FIFO mode. Reset Source: edma_rst_mod_g_rst_n
7	RESERVED	NONE		Reserved
6:4	PRI	R	0h	Transfer Priority: 0: Priority 0 - Highest priority 1: Priority 1 ... 7: Priority 7 - Lowest priority Reset Source: edma_rst_mod_g_rst_n
3:2	RESERVED	NONE		Reserved

Table 4-4786. DFOPT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DAM	R	0h	Destination Address Mode within an array: 0: INCR Dst addressing within an array increments. 1: FIFO Dst addressing within an array wraps around upon reaching FIFO width. Reset Source: edma_rst_mod_g_rst_n
0	SAM	R	0h	Source Address Mode within an array: 0: INCR Src addressing within an array increments. 1: FIFO Src addressing within an array wraps around upon reaching FIFO width. Reset Source: edma_rst_mod_g_rst_n

4.28.159 TPTC_DFSRC1 Registers

4.28.159.1 TPTC_DFSRC1 Register (Offset = 344h) [reset = 0h]

Short Description: Dst FIFO Set Src Address

Long Description: Dst FIFO Set Src Address

Return to Summary Table

Table 4-4787. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0344h
EDMA1	52A4 0344h

Figure 4-2273. DFSRC1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SADDR															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SADDR															
R															
0h															

Access Types Legend

Table 4-4788. DFSRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SADDR	R	0h	Source address is not applicable for Dst FIFO Register Set: Reads return 0x0. Reset Source: edma_rst_mod_g_rst_n

4.28.160 TPTC_DFACNT1 Registers

4.28.160.1 TPTC_DFACNT1 Register (Offset = 348h) [reset = 0h]

Short Description: Dst FIFO Set A-Count

Long Description: Dst FIFO Set A-Count

Return to Summary Table

Table 4-4789. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0348h
EDMA1	52A4 0348h

Figure 4-2274. DFACNT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED									ACNT						
NONE									R						
0									0h						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACNT															
R															
0h															

Access Types Legend

Table 4-4790. DFACNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE		Reserved
22:0	ACNT	R	0h	A-Dimension count. Number of bytes to be transferred infirst dimension. Reset Source: edma_rst_mod_g_rst_n

4.28.161 TPTC_DFDST1 Registers

4.28.161.1 TPTC_DFDST1 Register (Offset = 34Ch) [reset = 0h]

Short Description: Dst FIFO Set Dst Address

Long Description: Dst FIFO Set Dst Address

Return to Summary Table

Table 4-4791. Instance Table

Instance Name	Physical Address
EDMA0	52A6 034Ch
EDMA1	52A4 034Ch

Figure 4-2275. DFDST1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DADDR															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DADDR															
R															
0h															

Access Types Legend

Table 4-4792. DFDST1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DADDR	R	0h	Destination address for Dst FIFO Register Set: Initial value is copied from PDST.DADDR. TC updates value according to destination addressing mode [OPT.SAM] and/or dest index value [BIDX.DBIDX] after each write command is issued. When a TR is complete the final value should be the address of the last write command issued. Reset Source: edma_rst_mod_g_rst_n

4.28.162 TPTC_DFBIDX1 Registers

4.28.162.1 TPTC_DFBIDX1 Register (Offset = 350h) [reset = 0h]

Short Description: Dst FIFO Set B-Dim Idx

Long Description: Dst FIFO Set B-Dim Idx

Return to Summary Table

Table 4-4793. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0350h
EDMA1	52A4 0350h

Figure 4-2276. DFBIDX1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DBIDX															
R															
0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SBIDX															
R															
0h															

Access Types Legend

Table 4-4794. DFBIDX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DBIDX	R	0h	Dest B-Idx for Dest FIFO Register Set. Value copied from PBIDX: B-Idx offset between Destination arrays: Represents the offset in bytes between the starting address of each destination array [recall that there are BCNT arrays of ACNT elements]. DBIDX is always used regardless of whether DAM is Increment or FIFO mode. Reset Source: edma_rst_mod_g_rst_n
15:0	SBIDX	R	0h	Src B-Idx for Dest FIFO Register Set. Value copied from PBIDX: B-Idx offset between Source arrays: Represents the offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT elements]. SBIDX is always used regardless of whether SAM is Increment or FIFO mode. Reset Source: edma_rst_mod_g_rst_n

4.28.163 TPTC_DFMPPRXY1 Registers

4.28.163.1 TPTC_DFMPPRXY1 Register (Offset = 354h) [reset = 0h]

Short Description: Dst FIFO Set Mem Protect

Long Description: Dst FIFO Set Mem Protect Proxy

Return to Summary Table

Table 4-4795. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0354h
EDMA1	52A4 0354h

Figure 4-2277. DFMPPRXY1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						SECURE	PRIV	RESERVED				PRIVID			
NONE						R	R	NONE				R			
0						0h	0h	0				0h			

Access Types Legend

Table 4-4796. DFMPPRXY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE		Reserved
9	SECURE	R	0h	Secure Level: Deprecated, always read as 0. Reset Source: edma_rst_mod_g_rst_n
8	PRIV	R	0h	Privilege Level: PRIV = 0 : User level privilege PRIV = 1 : Supervisor level privilege PMPPRXY.PRIV is always updated with the value from the configuration bus privilege field on any/every write to Program Set BIDX Register [trigger register]. The PRIV value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the PRIV of the external host that sets up the DMA transaction. Reset Source: edma_rst_mod_g_rst_n
7:4	RESERVED	NONE		Reserved
3:0	PRIVID	R	0h	Privilege ID: PMPPRXY.PRIVID is always updated with the value from configuration bus privilege ID field on any/every write to Program Set BIDX Register [trigger register]. The PRIVID value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the privid of the external host that sets up the DMA transaction. Reset Source: edma_rst_mod_g_rst_n

4.28.164 TPTC_DFBCNT1 Registers

4.28.164.1 TPTC_DFBCNT1 Register (Offset = 358h) [reset = 0h]

Short Description: Dst FIFO Set B-Count

Long Description: Dst FIFO Set B-Count

Return to Summary Table

Table 4-4797. Instance Table

Instance Name	Physical Address
EDMA0	52A6 0358h
EDMA1	52A4 0358h

Figure 4-2278. DFBCNT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCNT															
R															
0h															

Access Types Legend

Table 4-4798. DFBCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE		Reserved
15:0	BCNT	R	0h	B-Count Remaining for Dst Register Set: Number of arrays to be transferred where each array is ACNT in length. Represents the amount of data remaining to be written. Initial value is copied from PCNT. TC decrements ACNT and BCNT as necessary after each write dataphase is issued. Final value should be 0 when TR is complete. Reset Source: edma_rst_mod_g_rst_n

4.28.165 Access Table

Table 4-4799. Access Type Codes

Access Type	Code	Description
R	R	Read
R/W	R/W	Read / Write
W	W	Write

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from December 15, 2022 to December 15, 2023 (from Revision C (December 2022) to Revision D (December 2023)) **Page**

- AM263x TRM refinement - remove mention of CTRLMMR, change to sub-topic of Control Overview, add note below table....19

Changes from October 1, 2022 to December 15, 2022 (from Revision B (October 2022) to Revision C (December 2022)) **Page**

- Including AM263x collateral links.... 5
- Updated PRU-ICSS Data RAM2 End Address from 0x0000 FFFF to 0x0001 FFFF.... 17
- Updated table vertical alignment. Updated descriptive text to prevent confusion.... 19
- Lock/Kick protection register unlock values added....19
- Adding note regarding CONTROLSS 16-bit register access requirements....1287
- Updated for ADC_RESULT_REGS instance count....1391

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