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1 Introduction

Note

The J721E hardware includes the PRU peripheral, that has been deprecated by TI and is not supported in TI software. This document highlights its features for posterity, and to enable its use in scenarios that do not require or expect TI support.

2 PRU_ICSSG Overview

The Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU_ICSSG) consists of:

- Two 32-bit load/store RISC CPU cores — Programmable Real-Time Units (PRU0 and PRU1)
- Two auxiliary 32-bit load/store RISC CPU cores — Auxiliary Programmable Real-Time Units (RTU_PRU0 and RTU_PRU1)
- Two 32-bit load/store RISC CPU cores — Transmit Programmable Real-Time Units (TX_PRU0 and TX_PRU1)
- Data RAMs per PRU core
- Instruction RAMs per PRU, per RTU_PRU and per TX_PRU cores
- Shared RAM
- Peripheral modules: UART0, ECAP0, PWM, IEP0 and IEP1
- Interrupt controller (INTC) and Task Manager per core

The programmable nature of the PRU cores, along with their access to pins, events and all device resources, provides flexibility in implementing fast real-time responses, specialized data handling operations, custom peripheral interfaces, and in offloading tasks from the other processor cores of the device.

The PRU cores are programmed with a small, deterministic instruction set. Each PRU can operate independently or in coordination with each other and can also work in coordination with the device-level host CPU. This interaction between processors is determined by the nature of the firmware loaded into the PRU's instruction memory.

[Table 2-1](#) shows the PRU_ICSSG systems allocation within device domains.

Table 2-1. PRU_ICSSG Allocation within Device Domains

Module Instance	Domain		
	WKUP	MCU	MAIN
PRU_ICSSG0	-	-	✓
PRU_ICSSG1	-	-	✓

[PRU_ICSSG Overview](#) shows an overview of the PRU_ICSSG subsystem.



The PRU ICSSG subsystem includes the following main features:

- 6 J721E Programmable Real-Time Unit (PRU)

- Task Manager (Preemption support)
- XFR2TR, for accelerating the internal memory copy of worklist from TRs (Transfer Requests)
- Broadside (32 Byte) connection to MII_G_RTn (where n = 1 or 2), Filter Data Base (FDB), IPC SPAD Memory, Scratchpad Memory (SPAD), SPINLOCK, XFR2VBUS, PRUm and TX_PRUm (where m = 0 or 1)
- Two Transmit Real-Time Transfer Units (TX_PRU0 and TX_PRU1), each with:
 - 6KB program memory with ECC
 - 2KB Broadside (BS) RAM
 - MAC (Multiplier with optional Accumulation)
 - CRC16/CRC32 Hardware accelerator
 - Byte Swap, for Little/Big Endian conversion
 - Task Manager (Preemption support)
 - Broadside (32 Byte) connection to the TX L2 FIFO of MII_G_RTn port (where n = 1 or 2), TX_PRU Scratchpad Memory (SPAD), SPINLOCK, XFR2VBUS, PRUm and RTU_PRUm (where m= 0 or 1)
- Scratchpad Memory (SPAD) with 8 banks of 30 × 32-bit registers:
 - 3 banks for the PRU0 and PRU1 cores
 - 3 banks for the RTU_PRU0 and RTU_PRU1 cores
 - 2 banks for the TX_PRU0 and TX_PRU1 cores
- 64 KB Shared general purpose memory RAM with ECC (Data RAM2), shared between PRU0 and PRU1
- Two 8 KB (shared) Data Memories with ECC (Data RAM0 and Data RAM1)
- 64-bit VBUSM Controller Port:
 - Optional address translation for all transactions to External Host
- 16 Software Events generated by 2 PRUs
- Two Real-Time Ethernet ports (MII_G_RT1 and MII_G_RT2) configurable to connect to each PRUn (where n = 0 or 1) to support multiple industrial communication protocols.
 - Each of the Ethernet ports can be configured as MII/RGMII/SGMII ports
 - **NOTE: SGMII mode is supported only for PRU_ICSSG1 instance**
 - RX Classifier per port
- Two Industrial Ethernet Peripheral's (IEP0/IEP1) to manage/generate Industrial Ethernet functions such as time stamping.
 - Each of the Industrial Ethernet 64-bit timers support 10 capture and 16 compare events along with slow and fast compensation.
 - Supports up to 4 sets of 3-phased motor control with 12 primary and 12 complimentary programmable PWM outputs.
 - Up to 9 safety events with optional external trip IO per PWM set with hardware glitch filter.
- One MDIO port to control external Ethernet PHY
- One Enhanced Capture Module (ECAP0)
- 16550-compatible UART with a dedicated 192-MHz clock to support 12-Mbps PROFIBUS
- Interrupt Controller (INTC)
 - Up to 64 internal events, generated by modules, internal to the PRU_ICSSG
 - Up to 96 external events, generated by the system
 - Supports up to 20 interrupt channels
 - Generation of 20 Host interrupts:
 - 2 Host interrupts to PRU0, PRU1, TX_PRU0 and TX_PRU1
 - 2 Host interrupts to RTU_PRU0 and RTU_PRU1
 - 8 Host interrupts, exported from the PRU_ICSSG for signaling the Arm interrupt controllers (pulse and level provided)
 - 8 Host Interrupts for the Task Managers
 - Each system event can be enabled and disabled
 - Each host event can be enabled and disabled
 - Hardware prioritization of events
- One 32-bit VBUSP target port for memory mapped register and internal memories access
- Flexible power management support
- Integrated 32-bit Interconnect

2.2 Not Supported Features

The following PRU_ICSSG features are not supported:

- Only 4 of the IEP0 (and none of the IEP1) Ethernet Digital Data Input/Output's of each PRU_ICSSG are pinned out
- UART Modem interface (DTR, DSR, and RI) is not supported
- The following features are not supported for PRU_ICSSG0 and PRU_ICSSG1:
 - 12 Enhanced General-Purpose Inputs (pr<0/1>_pru0_r31_in[31:20]) are not pinned out
 - 12 Enhanced General-Purpose Outputs (pr<0/1>_pru0_r31_out[31:20]) are not pinned out
 - SGMII mode is not supported on PRU_ICSSG0

3 PRU_ICSSG Environment

The PRU_ICSSG[1-0] modules are hereinafter referred to as PRU_ICSSG module

This section describes the PRU_ICSSG external connections (environment).

3.1 PRU_ICSSG Internal Pinmux

The PRU_ICSSG0 and PRU_ICSSG1 external interface signals are described in and [Figure 3-2](#), [Figure 3-3](#), respectively. The PRU_ICSSG has a large number of available I/O signals. Most of these are multiplexed with other functional signals at the device level.

The PRU_ICSSG0 and PRU_ICSSG1 also support an internal wrapper multiplexing that expands the device top-level multiplexing. This wrapper multiplexing is controlled by the GPCFGx_REG register (where x = 0 or 1) in the PRU_ICSSG CFG register space and allows MII_RT, 3 channel Peripheral Interface (with EnDAT capabilities), and Sigma Delta functionality to be muxed with the PRU GPI/O device signals, as shown in [Figure 3-1](#). The PRU_ICSSG wrapper multiplexing is described with the device-level signals in . Note that the device top-level muxing has higher priority over the internal PRU_ICSSG muxing.

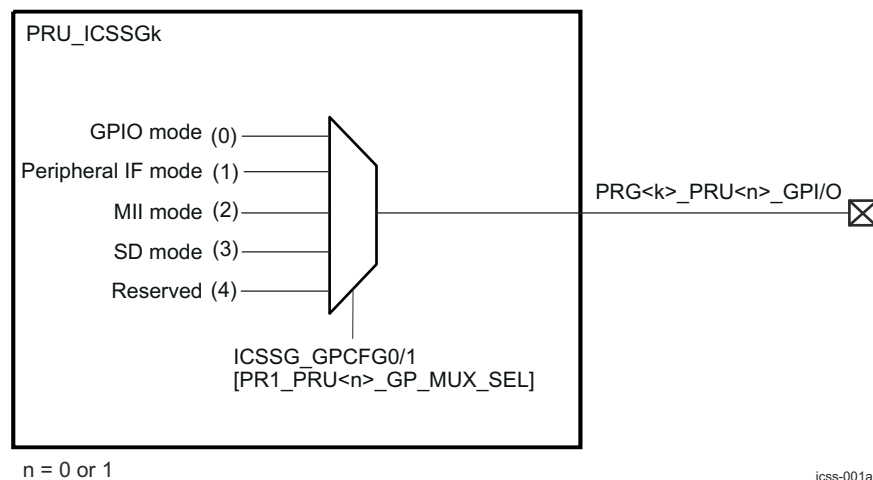


Figure 3-1. PRU_ICSSG Internal Wrapper Multiplexing

Note

Additionally to PRU_ICSSG wrapper multiplexing the device I/O logic maps the PRU_ICSSG signals to the different device pins by programming in the Control Module (CTRL_MMR0). For more information, refer to the [#unique_11referenceTitle](#) *Pad Configuration Registers* in the [#unique_12referenceTitle](#), *CTRL_MMR0 Registers*.

The below [Figure 3-2](#) illustrates the PRU_ICSSG0 I/O interface signals.

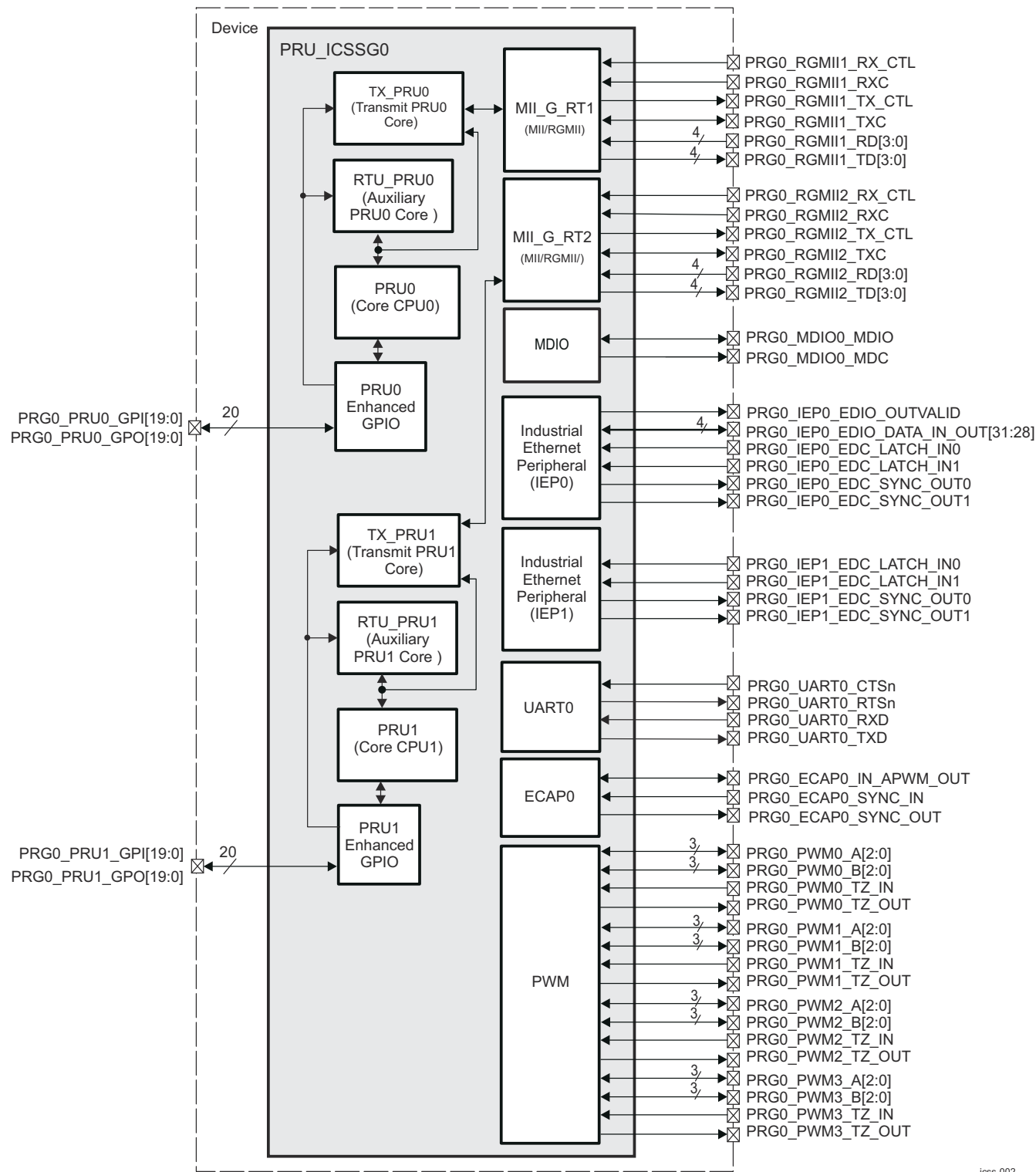


Figure 3-2. PRU_ICSSG0 External Interface I/Os

The [Figure 3-3](#) illustrates the PRU_ICSSG1 I/O interface signals.

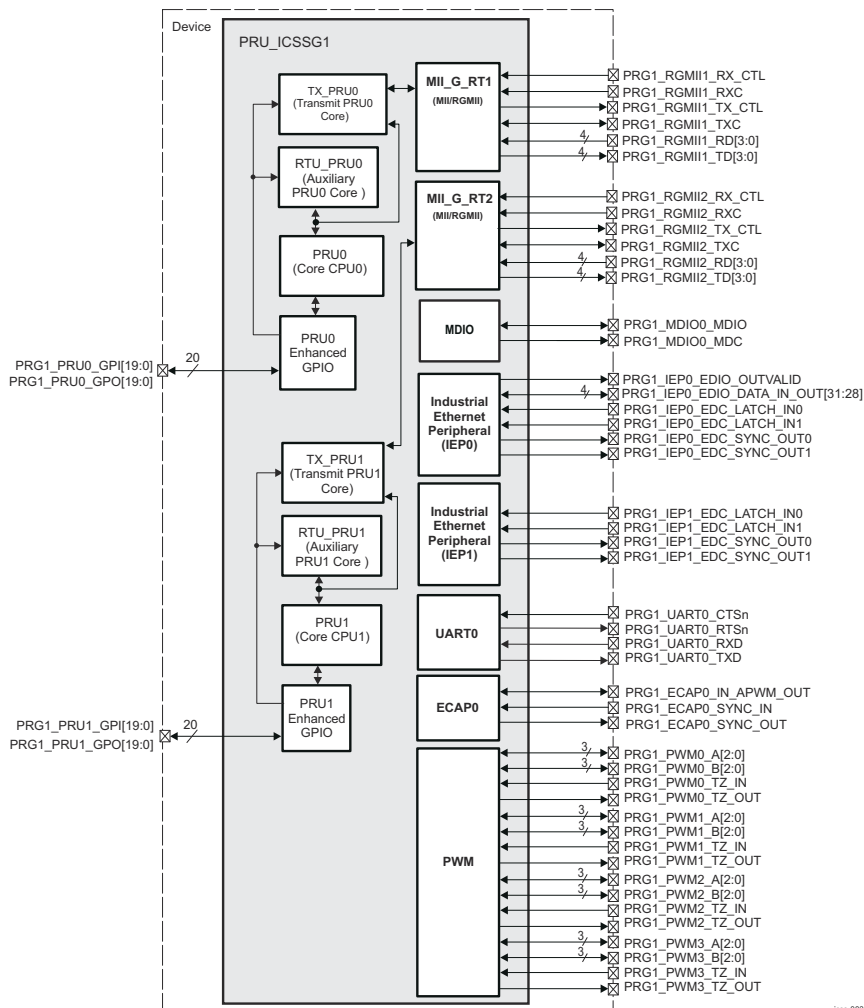


Figure 3-3. PRU_ICSSG1 External Interface I/Os

Note

PRGn_PWMm_A[2:0] = PRGn_PWMm_[2:0]_POS and PRGn_PWMm_B[2:0] = PRGn_PWMm_[2:0]_NEG.

Table 3-1 describes the PRU_ICSSG0 I/O signals.

Table 3-1. PRU_ICSSG0 I/O Signals

Device Level Signal	Alternate Function via Internal Multiplexing				I/O ⁽¹⁾	Description	Pin Reset ⁽²⁾
	ICSSG_GPCFG0_REG[29-26] PR1_PRU0_GP_MUX_SEL=						
PRU0 GP Signals	0h - GPIO mode (default)	1h - PERIF mode	2h - MII mode	3h - SD mode			
PRG0_PRU0_GPO0	pr0_pru0_pru_r30_out[0]	pr0_pru0_perif0_clk			O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO1	pr0_pru0_pru_r30_out[1]	pr0_pru0_perif0_out			O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO2	pr0_pru0_pru_r30_out[2]	pr0_pru0_perif0_out_en			O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO3	pr0_pru0_pru_r30_out[3]	pr0_pru0_perif1_clk			O	PRU0 R30 Outputs	0

Table 3-1. PRU_ICSSG0 I/O Signals (continued)

Device Level Signal	Alternate Function via Internal Multiplexing			I/O ⁽¹⁾	Description	Pin Reset ⁽²⁾
PRG0_PRU0_GPO4	pr0_pru0_pru_r30_o ut[4]	pr0_pru0_perif1_o ut		O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO5	pr0_pru0_pru_r30_o ut[5]	pr0_pru0_perif1_o ut_en		O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO6	pr0_pru0_pru_r30_o ut[6]	pr0_pru0_perif2_cl k		O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO7	pr0_pru0_pru_r30_o ut[7]	pr0_pru0_perif2_o ut		O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO8	pr0_pru0_pru_r30_o ut[8]	pr0_pru0_perif2_o ut_en		O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO9	pr0_pru0_pru_r30_o ut[9]			O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO10	pr0_pru0_pru_r30_o ut[10]			O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO11	pr0_pru0_pru_r30_o ut[11]	pr0_mii1_txd[0]		O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO12	pr0_pru0_pru_r30_o ut[12]	pr0_mii1_txd[1]		O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO13	pr0_pru0_pru_r30_o ut[13]	pr0_mii1_txd[2]		O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO14	pr0_pru0_pru_r30_o ut[14]	pr0_mii1_txd[3]		O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO15	pr0_pru0_pru_r30_o ut[15]	pr0_mii1_txen		O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO16	pr0_pru0_pru_r30_o ut[16]			O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO17	pr0_pru0_pru_r30_o ut[17]			O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO18	pr0_pru0_pru_r30_o ut[18]			O	PRU0 R30 Outputs	0
PRG0_PRU0_GPO19	pr0_pru0_pru_r30_o ut[19]			O	PRU0 R30 Outputs	0
PRG0_PRU0_GPI0	pr0_pru0_pru_r31_in[0]	pr0_mii0_rxd[0]	pr0_pru0_sd0_clk	I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI1	pr0_pru0_pru_r31_in[1]	pr0_mii0_rxd[1]	pr0_pru0_sd0_d	I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI2	pr0_pru0_pru_r31_in[2]	pr0_mii0_rxd[2]	pr0_pru0_sd1_clk	I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI3	pr0_pru0_pru_r31_in[3]	pr0_mii0_rxd[3]	pr0_pru0_sd1_d	I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI4	pr0_pru0_pru_r31_in[4]	pr0_mii0_rxdv	pr0_pru0_sd2_clk	I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI5	pr0_pru0_pru_r31_in[5]	pr0_mii0_rxer	pr0_pru0_sd2_d	I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI6	pr0_pru0_pru_r31_in[6]	pr0_mii_mr0_clk	pr0_pru0_sd3_clk	I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI7	pr0_pru0_pru_r31_in[7]		pr0_pru0_sd3_d	I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI8	pr0_pru0_pru_r31_in[8]	pr0_mii0_rxlink	pr0_pru0_sd4_clk	I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI9	pr0_pru0_pru_r31_in[9]	pr0_pru0_perif0_in pr0_mii0_col	pr0_pru0_sd4_d	I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI10	pr0_pru0_pru_r31_in[10]	pr0_pru0_perif1_in pr0_mii0_crs	pr0_pru0_sd5_clk	I	PRU0 R31 Inputs	HiZ

Table 3-1. PRU_ICSSG0 I/O Signals (continued)

Device Level Signal	Alternate Function via Internal Multiplexing			I/O ⁽¹⁾	Description	Pin Reset ⁽²⁾
PRG0_PRU0_GPI11	pr0_pru0_pru_r31_in[11]	pr0_pru0_perif2_in	pr0_pru0_sd5_d	I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI12	pr0_pru0_pru_r31_in[12]		pr0_pru0_sd6_clk	I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI13	pr0_pru0_pru_r31_in[13]		pr0_pru0_sd6_d	I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI14	pr0_pru0_pru_r31_in[14]		pr0_pru0_sd7_clk	I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI15	pr0_pru0_pru_r31_in[15]		pr0_pru0_sd7_d	I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI16	pr0_pru0_pru_r31_in[16]	pr0_mii_mt1_clk	pr0_pru0_sd8_clk	I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI17	pr0_pru0_pru_r31_in[17]		pr0_pru0_sd8_d	I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI18	pr0_pru0_pru_r31_in[18]			I	PRU0 R31 Inputs	HiZ
PRG0_PRU0_GPI19	pr0_pru0_pru_r31_in[19]			I	PRU0 R31 Inputs	HiZ
PRU1 GP Signals ICSSG_GPCFG1_REG[29-26] PR1_PRU1_GP_MUX_SEL=						
	0h - GPIO mode (default)	1h - PERIF mode	2h - MII mode	3h - SD mode		
PRG0_PRU1_GPO0	pr0_pru1_pru_r30_out[0]	pr0_pru1_perif0_clk			O PRU1 R30 Outputs	0
PRG0_PRU1_GPO1	pr0_pru1_pru_r30_out[1]	pr0_pru1_perif0_out			O PRU1 R30 Outputs	0
PRG0_PRU1_GPO2	pr0_pru1_pru_r30_out[2]	pr0_pru1_perif0_out_en			O PRU1 R30 Outputs	0
PRG0_PRU1_GPO3	pr0_pru1_pru_r30_out[3]	pr0_pru1_perif1_clk			O PRU1 R30 Outputs	0
PRG0_PRU1_GPO4	pr0_pru1_pru_r30_out[4]	pr0_pru1_perif1_out			O PRU1 R30 Outputs	0
PRG0_PRU1_GPO5	pr0_pru1_pru_r30_out[5]	pr0_pru1_perif1_out_en			O PRU1 R30 Outputs	0
PRG0_PRU1_GPO6	pr0_pru1_pru_r30_out[6]	pr0_pru1_perif2_clk			O PRU1 R30 Outputs	0
PRG0_PRU1_GPO7	pr0_pru1_pru_r30_out[7]	pr0_pru1_perif2_out			O PRU1 R30 Outputs	0
PRG0_PRU1_GPO8	pr0_pru1_pru_r30_out[8]	pr0_pru1_perif2_out_en			O PRU1 R30 Outputs	0
PRG0_PRU1_GPO9	pr0_pru1_pru_r30_out[9]				O PRU1 R30 Outputs	0
PRG0_PRU1_GPO10	pr0_pru1_pru_r30_out[10]				O PRU1 R30 Outputs	0
PRG0_PRU1_GPO11	pr0_pru1_pru_r30_out[11]		pr0_mii0_txd[0]		O PRU1 R30 Outputs	0
PRG0_PRU1_GPO12	pr0_pru1_pru_r30_out[12]		pr0_mii0_txd[1]		O PRU1 R30 Outputs	0
PRG0_PRU1_GPO13	pr0_pru1_pru_r30_out[13]		pr0_mii0_txd[2]		O PRU1 R30 Outputs	0
PRG0_PRU1_GPO14	pr0_pru1_pru_r30_out[14]		pr0_mii0_txd[3]		O PRU1 R30 Outputs	0
PRG0_PRU1_GPO15	pr0_pru1_pru_r30_out[15]		pr0_mii0_txen		O PRU1 R30 Outputs	0

Table 3-1. PRU_ICSSG0 I/O Signals (continued)

Table 6-17 PRU1_R30000 I/O Signals (continued)				I/O ⁽¹⁾	Description	Pin Reset ⁽²⁾	
Device Level Signal	Alternate Function via Internal Multiplexing						
PRG0_PRU1_GPO16	pr0_pru1_pru_r30_out[16]			O	PRU1 R30 Outputs	0	
PRG0_PRU1_GPO17	pr0_pru1_pru_r30_out[17]			O	PRU1 R30 Outputs	0	
PRG0_PRU1_GPO18	pr0_pru1_pru_r30_out[18]			O	PRU1 R30 Outputs	0	
PRG0_PRU1_GPO19	pr0_pru1_pru_r30_out[19]			O	PRU1 R30 Outputs	0	
PRG0_PRU1_GPI0	pr0_pru1_pru_r31_in[0]	pr0_mii1_rxd[0]	pr0_pru1_sd0_clk	I	PRU1 R31 Inputs	HiZ	
PRG0_PRU1_GPI1	pr0_pru1_pru_r31_in[1]	pr0_mii1_rxd[1]	pr0_pru1_sd0_d	I	PRU1 R31 Inputs	HiZ	
PRG0_PRU1_GPI2	pr0_pru1_pru_r31_in[2]	pr0_mii1_rxd[2]	pr0_pru1_sd1_clk	I	PRU1 R31 Inputs	HiZ	
PRG0_PRU1_GPI3	pr0_pru1_pru_r31_in[3]	pr0_mii1_rxd[3]	pr0_pru1_sd1_d	I	PRU1 R31 Inputs	HiZ	
PRG0_PRU1_GPI4	pr0_pru1_pru_r31_in[4]	pr0_mii1_rxdv	pr0_pru1_sd2_clk	I	PRU1 R31 Inputs	HiZ	
PRG0_PRU1_GPI5	pr0_pru1_pru_r31_in[5]	pr0_mii1_rxer	pr0_pru1_sd2_d	I	PRU1 R31 Inputs	HiZ	
PRG0_PRU1_GPI6	pr0_pru1_pru_r31_in[6]	pr0_mii_mr1_clk	pr0_pru1_sd3_clk	I	PRU1 R31 Inputs	HiZ	
PRG0_PRU1_GPI7	pr0_pru1_pru_r31_in[7]		pr0_pru1_sd3_d	I	PRU1 R31 Inputs	HiZ	
PRG0_PRU1_GPI8	pr0_pru1_pru_r31_in[8]	pr0_mii1_rxlink	pr0_pru1_sd4_clk	I	PRU1 R31 Inputs	HiZ	
PRG0_PRU1_GPI9	pr0_pru1_pru_r31_in[9]	pr0_pru1_perif0_in	pr0_mii1_col	pr0_pru1_sd4_d	I	PRU1 R31 Inputs	HiZ
PRG0_PRU1_GPI10	pr0_pru1_pru_r31_in[10]	pr0_pru1_perif1_in	pr0_mii1_crs	pr0_pru1_sd5_clk	I	PRU1 R31 Inputs	HiZ
PRG0_PRU1_GPI11	pr0_pru1_pru_r31_in[11]	pr0_pru1_perif2_in		pr0_pru1_sd5_d	I	PRU1 R31 Inputs	HiZ
PRG0_PRU1_GPI12	pr0_pru1_pru_r31_in[12]			pr0_pru1_sd6_clk	I	PRU1 R31 Inputs	HiZ
PRG0_PRU1_GPI13	pr0_pru1_pru_r31_in[13]			pr0_pru1_sd6_d	I	PRU1 R31 Inputs	HiZ
PRG0_PRU1_GPI14	pr0_pru1_pru_r31_in[14]			pr0_pru1_sd7_clk	I	PRU1 R31 Inputs	HiZ
PRG0_PRU1_GPI15	pr0_pru1_pru_r31_in[15]			pr0_pru1_sd7_d	I	PRU1 R31 Inputs	HiZ
PRG0_PRU1_GPI16	pr0_pru1_pru_r31_in[16]	pr0_pru1_pru_r31_in[16]	pr0_mii_mt0_clk	pr0_pru1_sd8_clk	I	PRU1 R31 Inputs	HiZ
PRG0_PRU1_GPI17	pr0_pru1_pru_r31_in[17]			pr0_pru0_sd8_d	I	PRU1 R31 Inputs	HiZ
PRG0_PRU1_GPI18	pr0_pru1_pru_r31_in[18]			I	PRU1 R31 Inputs	HiZ	
PRG0_PRU1_GPI19	pr0_pru1_pru_r31_in[19]			I	PRU1 R31 Inputs	HiZ	
MII_G_RT1 (RGMII mode)							
PRG0_RGMII1_RX_CTL				I	RGMII1 Receive Control	-	

Table 3-1. PRU_ICSSG0 I/O Signals (continued)

Device Level Signal	Alternate Function via Internal Multiplexing	I/O ⁽¹⁾	Description	Pin Reset ⁽²⁾
PRG0_RGMII1_RXC		I	RGMII1 Receive Clock	-
PRG0_RGMII1_TX_CTL		O	RGMII1 Transmit Control	-
PRG0_RGMII1_TXC		I/O	RGMII1 Transmit Clock	-
PRG0_RGMII1_RD[3:0]		I	RGMII1 Receive Data	-
PRG0_RGMII1_TD[3:0]		O	RGMII1 Transmit Data	-
MII_G_RT2 (RGMII mode)				
PRG0_RGMII2_RX_CTL		I	RGMII2 Receive Control	-
PRG0_RGMII2_RXC		I	RGMII2 Receive Clock	-
PRG0_RGMII2_TX_CTL		O	RGMII2 Transmit Control	-
PRG0_RGMII2_TXC		I/O	RGMII2 Transmit Clock	-
PRG0_RGMII2_RD[3:0]		I	RGMII2 Receive Data	-
PRG0_RGMII2_TD[3:0]		O	RGMII2 Transmit Data	-
MDIO MDIO				
PRG0_MDIO0_MDC	pr0_mdio_mdclk	O	MDIO Clock	0
PRG0_MDIO0_MDIO	pr0_mdio_data	I/O	MDIO Data	HiZ
Industrial Ethernet (IEP0) Industrial Ethernet				
PRG0_IEP0_EDIO_OUTVALID	pr0_iep0_edio_outval_id	O	IEP0 Digital I/O Output Valid	0
PRG0_IEP0_EDIO_DATA_IN_OUT[31:28]	pr0_iep0_edio_data_in_out[31:28]	I/O	IEP0 Digital I/Os Data In/Out	HiZ
PRG0_IEP0_EDC_SYNC_OUT0	pr0_iep0_edc_sync_out0	O	IEP0 Distributed Clock Sync Out	0
PRG0_IEP0_EDC_SYNC_OUT1	pr0_iep0_edc_sync_out1	O	IEP0 Distributed Clock Sync Out	0
PRG0_IEP0_EDC_LATCH_IN0	pr0_iep0_edc_latch_in0	I	IEP0 Distributed Clock Latch In	HiZ
PRG0_IEP0_EDC_LATCH_IN1	pr0_iep0_edc_latch_in1	I	IEP0 Distributed Clock Latch In	HiZ
Industrial Ethernet (IEP1) Industrial Ethernet				
PRG0_IEP1_EDC_SYNC_OUT0	pr0_iep1_edc_sync_out0	O	IEP1 Distributed Clock Sync Out	0

Table 3-1. PRU_ICSSG0 I/O Signals (continued)

Device Level Signal	Alternate Function via Internal Multiplexing	I/O ⁽¹⁾	Description	Pin Reset ⁽²⁾
PRG0_IEP1_EDC_S YNC_OUT1	pr0_iep1_edc_sync_ out1	O	IEP1 Distributed Clock Sync Out	0
PRG0_IEP1_EDC_L ATCH_IN0	pr0_iep1_edc_latch_i n0	I	IEP1 Distributed Clock Latch In	HiZ
PRG0_IEP1_EDC_L ATCH_IN1	pr0_iep1_edc_latch_i n1	I	IEP1 Distributed Clock Latch In	HiZ
UART0				
PRG0_UART0_CTSn	pr0_uart0_cts_n	I	UART0 Clear to Send	HiZ
PRG0_UART0_RTSn	pr0_uart0_rts_n	O	UART0 Request to Send	1
PRG0_UART0_RXD	pr0_uart0_rxd	I	UART0 Receive Data	HiZ
PRG0_UART0_TXD	pr0_uart0_txd	O	UART0 Transmit Data	1
ECAP0				
PRG0_ECAP0_IN_A PWM_OUT	pr0_ecap0_ecap_cap in_apwm_o	I/O	Enhanced capture (ECAP0) input or Auxiliary PWM out	HiZ
PRG0_ECAP0_SYN C_IN	pr0_ecap0_ecap_syn cin	I	Enhanced capture (ECAP0) Sync In	0
PRG0_ECAP0_SYN C_OUT	pr0_ecap0_ecap_syn cout	O	Enhanced capture (ECAP0) Sync Out	0
PWM				
PRG0_PWM0_A[2:0] (3)	pr0_pwm_pwm0_[2:0] _pos	I/O	PWM Set 0 Positive In/Out	-
PRG0_PWM0_B[2:0] (3)	pr0_pwm_pwm0_[2:0] _neg	I/O	PWM Set 0 Negative In/Out	-
PRG0_PWM0_TZ_IN	pr0_pwm_pwm0_trip _in	I	PWM Set 0 Tripzone Input	-
PRG0_PWM0_TZ_O UT	pr0_pwm_pwm0_trip _out	O	PWM Set 0 Tripzone Output	-
PRG0_PWM1_A[2:0] (3)	pr0_pwm_pwm1_[2:0] _pos	I/O	PWM Set 1 Positive In/Out	-
PRG0_PWM1_B[2:0] (3)	pr0_pwm_pwm1_[2:0] _neg	I/O	PWM Set 1 Negative In/Out	-
PRG0_PWM1_TZ_IN	pr0_pwm_pwm1_trip _in	I	PWM Set 1 Tripzone Input	-
PRG0_PWM1_TZ_O UT	pr0_pwm_pwm1_trip _out	O	PWM Set 1 Tripzone Output	-
PRG0_PWM2_A[2:0] (3)	pr0_pwm_pwm2_[2:0] _pos	I/O	PWM Set 2 Positive In/Out	-
PRG0_PWM2_B[2:0] (3)	pr0_pwm_pwm2_[2:0] _neg	I/O	PWM Set 2 Negative In/Out	-

Table 3-1. PRU_ICSSG0 I/O Signals (continued)

Device Level Signal	Alternate Function via Internal Multiplexing	I/O ⁽¹⁾	Description	Pin Reset ⁽²⁾
PRG0_PWM2_TZ_IN	pr0_pwm_pwm2_trip_in	I	PWM Set 2 Tripzone Input	-
PRG0_PWM2_TZ_O UT	pr0_pwm_pwm2_trip_out	O	PWM Set 2 Tripzone Output	-
PRG0_PWM3_A[2:0] (3)	pr0_pwm_pwm3_[2:0] _pos	I/O	PWM Set 3 Positive In/Out	-
PRG0_PWM3_B[2:0] (3)	pr0_pwm_pwm3_[2:0] _neg	I/O	PWM Set 3 Negative In/Out	-
PRG0_PWM3_TZ_IN	pr0_pwm_pwm3_trip_in	I	PWM Set 3 Tripzone Input	-
PRG0_PWM3_TZ_O UT	pr0_pwm_pwm3_trip_out	O	PWM Set 3 Tripzone Output	-

(1) I = Input; O = Output

(2) HiZ = High Impedance

(3) NPRGn_PWMm_A[2:0] = PRGn_PWMm_[2:0]_POS and PRGn_PWMm_B[2:0] = PRGn_PWMm_[2:0]_NEG

Table 3-2 describes the PRU_ICSSG1 I/O signals.

Table 3-2. PRU_ICSSG1 I/O Signals

Device Level Signal	Alternate Function via Internal Wrapper Multiplexing				I/O ⁽¹⁾	Description	Pin Reset ⁽²⁾
	ICSSG_GPCFG0_REG[29-26] PR1_PRU0_GP_MUX_SEL=						
PRU0 GP Signals	0h - GPIO mode (default)	1h - PERIF mode	2h - MII mode	3h - SD mode			
PRG1_PRU0_GPO0	pr1_pru0_pru_r30_out[0]	pr1_pru0_perif0_clk			O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO1	pr1_pru0_pru_r30_out[1]	pr1_pru0_perif0_out			O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO2	pr1_pru0_pru_r30_out[2]	pr1_pru0_perif0_out_en			O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO3	pr1_pru0_pru_r30_out[3]	pr1_pru0_perif1_clk			O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO4	pr1_pru0_pru_r30_out[4]	pr1_pru0_perif1_out			O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO5	pr1_pru0_pru_r30_out[5]	pr1_pru0_perif1_out_en			O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO6	pr1_pru0_pru_r30_out[6]	pr1_pru0_perif2_clk			O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO7	pr1_pru0_pru_r30_out[7]	pr1_pru0_perif2_out			O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO8	pr1_pru0_pru_r30_out[8]	pr1_pru0_perif2_out_en			O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO9	pr1_pru0_pru_r30_out[9]				O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO10	pr1_pru0_pru_r30_out[10]				O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO11	pr1_pru0_pru_r30_out[11]		pr1_mii1_txd[0]		O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO12	pr1_pru0_pru_r30_out[12]		pr1_mii1_txd[1]		O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO13	pr1_pru0_pru_r30_out[13]		pr1_mii1_txd[2]		O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO14	pr1_pru0_pru_r30_out[14]		pr1_mii1_txd[3]		O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO15	pr1_pru0_pru_r30_out[15]		pr1_mii1_txen		O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO16	pr1_pru0_pru_r30_out[16]				O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO17	pr1_pru0_pru_r30_out[17]				O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO18	pr1_pru0_pru_r30_out[18]				O	PRU0 R30 Outputs	0
PRG1_PRU0_GPO19	pr1_pru0_pru_r30_out[19]				O	PRU0 R30 Outputs	0
PRG1_PRU0_GPIO0	pr1_pru0_pru_r31_in[0]		pr1_mii0_rxd[0]	pr1_pru0_sd0_clk	I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPIO1	pr1_pru0_pru_r31_in[1]		pr1_mii0_rxd[1]	pr1_pru0_sd0_d	I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPIO2	pr1_pru0_pru_r31_in[2]		pr1_mii0_rxd[2]	pr1_pru0_sd1_clk	I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPIO3	pr1_pru0_pru_r31_in[3]		pr1_mii0_rxd[3]	pr1_pru0_sd1_d	I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPIO4	pr1_pru0_pru_r31_in[4]		pr1_mii0_rxdv	pr1_pru0_sd2_clk	I	PRU0 R31 Inputs	HiZ

Table 3-2. PRU_ICSSG1 I/O Signals (continued)

Device Level Signal	Alternate Function via Internal Wrapper Multiplexing				I/O ⁽¹⁾	Description	Pin Reset ⁽²⁾
PRG1_PRU0_GPI5	pr1_pru0_pru_r31_in[5]	pr1_mii0_rxer	pr1_pru0_sd2_d		I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPI6	pr1_pru0_pru_r31_in[6]	pr1_mii_mr0_clk	pr1_pru0_sd3_clk		I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPI7	pr1_pru0_pru_r31_in[7]		pr1_pru0_sd3_d		I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPI8	pr1_pru0_pru_r31_in[8]	pr1_mii0_rxlk	pr1_pru0_sd4_clk		I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPI9	pr1_pru0_pru_r31_in[9]	pr1_pru0_perif0_in	pr1_mii0_col	pr1_pru0_sd4_d	I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPI10	pr1_pru0_pru_r31_in[10]	pr1_pru0_perif1_in	pr1_mii0_crs	pr1_pru0_sd5_clk	I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPI11	pr1_pru0_pru_r31_in[11]	pr1_pru0_perif2_in		pr1_pru0_sd5_d	I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPI12	pr1_pru0_pru_r31_in[12]			pr1_pru0_sd6_clk	I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPI13	pr1_pru0_pru_r31_in[13]			pr1_pru0_sd6_d	I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPI14	pr1_pru0_pru_r31_in[14]			pr1_pru0_sd7_clk	I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPI15	pr1_pru0_pru_r31_in[15]			pr1_pru0_sd7_d	I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPI16	pr1_pru0_pru_r31_in[16]	pr1_mii_mt1_clk		pr1_pru0_sd8_clk	I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPI17	pr1_pru0_pru_r31_in[17]			pr1_pru0_sd8_d	I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPI18	pr1_pru0_pru_r31_in[18]				I	PRU0 R31 Inputs	HiZ
PRG1_PRU0_GPI19	pr1_pru0_pru_r31_in[19]				I	PRU0 R31 Inputs	HiZ
PRU1 GP Signals		ICSSG_GPCFG1_REG[29-26] PR1_PRU1_GP_MUX_SEL=					
	0h - GPIO mode (default)	1h - PERIF mode	2h - MII mode	3h - SD mode			
PRG1_PRU1_GPO0	pr1_pru1_pru_r30_out[0]	pr1_pru1_perif0_clk			O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO1	pr1_pru1_pru_r30_out[1]	pr1_pru1_perif0_out			O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO2	pr1_pru1_pru_r30_out[2]	pr1_pru1_perif0_out_en			O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO3	pr1_pru1_pru_r30_out[3]	pr1_pru1_perif1_clk			O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO4	pr1_pru1_pru_r30_out[4]	pr1_pru1_perif1_out			O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO5	pr1_pru1_pru_r30_out[5]	pr1_pru1_perif1_out_en			O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO6	pr1_pru1_pru_r30_out[6]	pr1_pru1_perif2_clk			O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO7	pr1_pru1_pru_r30_out[7]	pr1_pru1_perif2_out			O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO8	pr1_pru1_pru_r30_out[8]	pr1_pru1_perif2_out_en			O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO9	pr1_pru1_pru_r30_out[9]				O	PRU1 R30 Outputs	0

Table 3-2. PRU_ICSSG1 I/O Signals (continued)

Device Level Signal	Alternate Function via Internal Wrapper Multiplexing			I/O ⁽¹⁾	Description	Pin Reset ⁽²⁾
PRG1_PRU1_GPO1_0	pr1_pru1_pru_r30_o ut[10]			O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO1_1	pr1_pru1_pru_r30_o ut[11]	pr1_mii0_txd[0]		O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO1_2	pr1_pru1_pru_r30_o ut[12]	pr1_mii0_txd[1]		O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO1_3	pr1_pru1_pru_r30_o ut[13]	pr1_mii0_txd[2]		O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO1_4	pr1_pru1_pru_r30_o ut[14]	pr1_mii0_txd[3]		O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO1_5	pr1_pru1_pru_r30_o ut[15]	pr1_mii0_txen		O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO1_6	pr1_pru1_pru_r30_o ut[16]			O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO1_7	pr1_pru1_pru_r30_o ut[17]			O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO1_8	pr1_pru1_pru_r30_o ut[18]			O	PRU1 R30 Outputs	0
PRG1_PRU1_GPO1_9	pr1_pru1_pru_r30_o ut[19]			O	PRU1 R30 Outputs	0
PRG1_PRU1_GPI0	pr1_pru1_pru_r31_in[0]	pr1_mii1_rxd[0]	pr1_pru1_sd0_clk	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI1	pr1_pru1_pru_r31_in[1]	pr1_mii1_rxd[1]	pr1_pru1_sd0_d	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI2	pr1_pru1_pru_r31_in[2]	pr1_mii1_rxd[2]	pr1_pru1_sd1_clk	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI3	pr1_pru1_pru_r31_in[3]	pr1_mii1_rxd[3]	pr1_pru1_sd1_d	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI4	pr1_pru1_pru_r31_in[4]	pr1_mii1_rxdv	pr1_pru1_sd2_clk	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI5	pr1_pru1_pru_r31_in[5]	pr1_mii1_rxer	pr1_pru1_sd2_d	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI6	pr1_pru1_pru_r31_in[6]	pr1_mii_mr1_clk	pr1_pru1_sd3_clk	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI7	pr1_pru1_pru_r31_in[7]		pr1_pru1_sd3_d	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI8	pr1_pru1_pru_r31_in[8]	pr1_mii1_rxlk	pr1_pru1_sd4_clk	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI9	pr1_pru1_pru_r31_in[9]	pr1_pru1_perif0_in pr1_mii1_col	pr1_pru1_sd4_d	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI10	pr1_pru1_pru_r31_in[10]	pr1_pru1_perif1_in pr1_mii1_crs	pr1_pru1_sd5_clk	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI11	pr1_pru1_pru_r31_in[11]	pr1_pru1_perif2_in	pr1_pru1_sd5_d	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI12	pr1_pru1_pru_r31_in[12]		pr1_pru1_sd6_clk	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI13	pr1_pru1_pru_r31_in[13]		pr1_pru1_sd6_d	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI14	pr1_pru1_pru_r31_in[14]		pr1_pru1_sd7_clk	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI15	pr1_pru1_pru_r31_in[15]		pr1_pru1_sd7_d	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI16	pr1_pru1_pru_r31_in[16]	pr1_pru1_pru_r31 pr1_mii_mt0_clk	pr1_pru1_sd8_clk	I	PRU1 R31 Inputs	HiZ

Table 3-2. PRU_ICSSG1 I/O Signals (continued)

Device Level Signal	Alternate Function via Internal Wrapper Multiplexing	I/O ⁽¹⁾	Description	Pin Reset ⁽²⁾
PRG1_PRU1_GPI17	pr1_pru1_pru_r31_in[17]			
	pr1_pru0_sd8_d	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI18	pr1_pru1_pru_r31_in[18]	I	PRU1 R31 Inputs	HiZ
PRG1_PRU1_GPI19	pr1_pru1_pru_r31_in[19]	I	PRU1 R31 Inputs	HiZ
MII_G_RT1 (RGMII mode)				
PRG1_RGMII1_RX_CTL		I	RGMII1 Receive Control	-
PRG1_RGMII1_RXC		I	RGMII1 Receive Clock	-
PRG1_RGMII1_TX_CTL		O	RGMII1 Transmit Control	-
PRG1_RGMII1_TXC		I/O	RGMII1 Transmit Clock	-
PRG1_RGMII1_RD[3:0]		I	RGMII1 Receive Data	-
PRG1_RGMII1_TD[3:0]		O	RGMII1 Transmit Data	-
MII_G_RT2 (RGMII mode)				
PRG1_RGMII2_RX_CTL		I	RGMII2 Receive Control	-
PRG1_RGMII2_RXC		I	RGMII2 Receive Clock	-
PRG1_RGMII2_TX_CTL		O	RGMII2 Transmit Control	-
PRG1_RGMII2_TXC		I/O	RGMII2 Transmit Clock	-
PRG1_RGMII2_RD[3:0]		I	RGMII2 Receive Data	-
PRG1_RGMII2_TD[3:0]		O	RGMII2 Transmit Data	-
MII_G_RT1 (SGMII mode)				
SERDES1_RX0_P SERDES2_RX0_P	PRG1_SGMII0_RXP 0	I	Receive differential lane 0 for SGMII via Serdes1 or Serdes2	-
SERDES1_RX0_N SERDES2_RX0_N	PRG1_SGMII0_RXN 0	I		-
SERDES1_TX0_P SERDES2_TX0_P	PRG1_SGMII0_TXP 0	O	Transmit differential lane 0 for SGMII via Serdes1 or Serdes2	-
SERDES1_TX0_N SERDES2_TX0_N	PRG1_SGMII0_TXN 0	O		-
MII_G_RT2 (SGMII mode)				

Table 3-2. PRU_ICSSG1 I/O Signals (continued)

Device Level Signal	Alternate Function via Internal Wrapper Multiplexing	I/O ⁽¹⁾	Description	Pin Reset ⁽²⁾
SERDES1_RX1_P SERDES2_RX1_P	PRG1_SGMII1_RXN 0	I	Receive differential lane 1 for SGMII via Serdes1 or Serdes2	-
SERDES1_RX1_N SERDES2_RX1_N	PRG1_SGMII1_RXP 0	I		-
SERDES1_TX1_P SERDES2_TX1_P	PRG1_SGMII1_TXN 0	O	Transmit differential lane 1 for SGMII via Serdes1 or Serdes2	-
SERDES1_TX1_N SERDES2_TX1_N	PRG1_SGMII1_TXP 0	O		-
MDIO	MDIO			
PRG1_MDIO0_MDC	pr1_mdio_mdclk	O	MDIO Clock	0
PRG1_MDIO0_MDIO	pr1_mdio_data	I/O	MDIO Data	HiZ
Industrial Ethernet (IEP0)	Industrial Ethernet			
PRG1_IEP0_EDIO_OUTVALID	pr1_iep0_edio_outval_id	O	IEP0 Digital I/O Output Valid	0
PRG1_IEP0_EDIO_DATA_IN_OUT[31:28]	pr1_iep0_edio_data_in_out[31:28]	I/O	IEP0 Digital I/Os Data In/Out	HiZ
PRG1_IEP0_EDC_SYNC_OUT0	pr1_iep0_edc_sync_out0	O	IEP0 Distributed Clock Sync Out	0
PRG1_IEP0_EDC_SYNC_OUT1	pr1_iep0_edc_sync_out1	O	IEP0 Distributed Clock Sync Out	0
PRG1_IEP0_EDC_LATCH_IN0	pr1_iep0_edc_latch_in0	I	IEP0 Distributed Clock Latch In	HiZ
PRG1_IEP0_EDC_LATCH_IN1	pr1_iep0_edc_latch_in1	I	IEP0 Distributed Clock Latch In	HiZ
Industrial Ethernet (IEP1)	Industrial Ethernet			
PRG1_IEP1_EDC_SYNC_OUT0	pr1_iep1_edc_sync_out0	O	IEP1 Distributed Clock Sync Out	0
PRG1_IEP1_EDC_SYNC_OUT1	pr1_iep1_edc_sync_out1	O	IEP1 Distributed Clock Sync Out	0
PRG1_IEP1_EDC_LATCH_IN0	pr1_iep1_edc_latch_in0	I	IEP1 Distributed Clock Latch In	HiZ
PRG1_IEP1_EDC_LATCH_IN1	pr1_iep1_edc_latch_in1	I	IEP1 Distributed Clock Latch In	HiZ
UART0	UART0			
PRG1_UART0_CTSn	pr1_uart0_cts_n	I	UART0 Clear to Send	HiZ
PRG1_UART0_RTSn	pr1_uart0_rts_n	O	UART0 Request to Send	1
PRG1_UART0_RXD	pr1_uart0_rxd	I	UART0 Receive Data	HiZ
PRG1_UART0_TXD	pr1_uart0_txd	O	UART0 Transmit Data	1

Table 3-2. PRU_ICSSG1 I/O Signals (continued)

Device Level Signal	Alternate Function via Internal Wrapper Multiplexing	I/O ⁽¹⁾	Description	Pin Reset ⁽²⁾
ECAP0				
PRG1_ECAP0_IN_A PWM_OUT	pr1_ecap0_ecap_cap in_apwm_o	I/O	Enhanced capture (ECAP0) input or Auxiliary PWM out	HiZ
PRG1_ECAP0_SYN C_IN	pr1_ecap0_ecap_syn cin	I	Enhanced capture (ECAP0) Sync In	0
PRG1_ECAP0_SYN C_OUT	pr1_ecap0_ecap_syn cout	O	Enhanced capture (ECAP0) Sync Out	0
PWM				
PRG1_PWM0_A[2:0] (3)	pr1_pwm_pwm0_[2:0] _pos	I/O	PWM Set 0 Positive In/Out	-
PRG1_PWM0_B[2:0] (3)	pr1_pwm_pwm0_[2:0] _neg	I/O	PWM Set 0 Negative In/Out	-
PRG1_PWM0_TZ_IN	pr1_pwm_pwm0_trip _in	I	PWM Set 0 Tripzone Input	-
PRG1_PWM0_TZ_O UT	pr1_pwm_pwm0_trip _out	O	PWM Set 0 Tripzone Output	-
PRG1_PWM1_A[2:0] (3)	pr1_pwm_pwm1_[2:0] _pos	I/O	PWM Set 1 Positive In/Out	-
PRG1_PWM1_B[2:0] (3)	pr1_pwm_pwm1_[2:0] _neg	I/O	PWM Set 1 Negative In/Out	-
PRG1_PWM1_TZ_IN	pr1_pwm_pwm1_trip _in	I	PWM Set 1 Tripzone Input	-
PRG1_PWM1_TZ_O UT	pr1_pwm_pwm1_trip _out	O	PWM Set 1 Tripzone Output	-
PRG1_PWM2_A[2:0] (3)	pr1_pwm_pwm2_[2:0] _pos	I/O	PWM Set 2 Positive In/Out	-
PRG1_PWM2_B[2:0] (3)	pr1_pwm_pwm2_[2:0] _neg	I/O	PWM Set 2 Negative In/Out	-
PRG1_PWM2_TZ_IN	pr1_pwm_pwm2_trip _in	I	PWM Set 2 Tripzone Input	-
PRG1_PWM2_TZ_O UT	pr1_pwm_pwm2_trip _out	O	PWM Set 2 Tripzone Output	-
PRG1_PWM3_A[2:0] (3)	pr1_pwm_pwm3_[2:0] _pos	I/O	PWM Set 3 Positive In/Out	-
PRG1_PWM3_B[2:0] (3)	pr1_pwm_pwm3_[2:0] _neg	I/O	PWM Set 3 Negative In/Out	-
PRG1_PWM3_TZ_IN	pr1_pwm_pwm3_trip _in	I	PWM Set 3 Tripzone Input	-
PRG1_PWM3_TZ_O UT	pr1_pwm_pwm3_trip _out	O	PWM Set 3 Tripzone Output	-

(1) I = Input; O = Output

(2) HiZ = High Impedance

(3) PRGn_PWMm_A[2:0] = PRGn_PWMm_[2:0]_POS and PRGn_PWMm_B[2:0] = PRGn_PWMm_[2:0]_NEG

3.2 PRU_ICSSG Fast GPIO pins

Each PRU_ICSSG PRU processor implements fast general purpose outputs (GPO) through its R30 register and fast general purpose inputs (GPI) through its R31 register. The device multiplexes all GPI signals and their corresponding GPO signals onto the same device pin using different device multiplexing modes. In some applications it may be necessary for the PRU to switch between GPO and GPI operation in a fast (or at least a deterministic) manner. This is not possible using SoC level pin muxing since each pin being switched requires a write to a separate pin configuration register located in Control Module (CTRL_MMR0).

In order to address the fast switching issue, special I/O pin connectivity for the PRU_ICSSG GPO/GPI pins is implemented. This feature makes use of the IEP EDIO signal controls to provide input/output switching using a single SoC level pin multiplexing mode.

The IEP EDIO interface has 32 data input (DATA_IN) and 32 data output (DATA_OUT) signals. It also has a set of 32 corresponding data output enable (DATA_OUT_EN) signals to be used as (active low) output driver enables to allow each DATA_OUT/DATA_IN to be implemented as a bidirectional pin. On this device, only 4 of the IEP0 EDIO (and none of the IEP1 EDIO) I/Os of each PRU_ICSSG module are pinned out (PRG[2:0]_IEP0_EDIO_DATA_IN_OUT[31:28]). This leaves a majority of the DATA_OUT_EN signals unused. The device allows these unused output enables to be optionally re-purposed for use as GPO enables. This allows each ICSSG GP pin to function as either a GPO or as a GPI when the I/O pin is configured for the GPO muxmode.

A set of SoC level registers (CTRLMMR_ICSSG[2:0]_CTRL[2:0]) are used to determine the behavior of each GPO mode pin. When a register's [19:0]GPM_BIDI bit field is set to 0h (default value), the corresponding GPO pin operates only as an output when the GPO multiplexing mode is selected and is driven with the R30 bit value. The corresponding GPI signal (ICSSG GPI<n> input, where n = 0 to 19) is driven low. When a register's [19:0]GPM_BIDI bit field is set to 1h, the corresponding IEP_DIGIO_DATA_OUT_EN_REG[31:0] DATA_OUT_EN bit field is used to control the GPO output buffer. If [31:0] DATA_OUT_EN bit field is set to 0h the output is driven and the pin acts as a GPO. If [31:0] DATA_OUT_EN bit field is set to 1h the output is disabled and the pin acts as a GPI.

Figure 3-4 shows the PRU_ICSSGm GPO/GPI pin connectivity. The PRU[1:0]_GPM[19:0] output signals are propagated to the PRG[2:0]_PRU[1:0]_GPO[19:0] pins using Muxmode 0 function and the PRU[1:0]_GPN[19:0] input signals are propagated to the PRG[2:0]_PRU[1:0]_GPI[19:0] pins using Muxmode 1 function. Any GPO (Muxmode 0 function) can be made bidirectional by setting the corresponding bit field [19:0]GPM_BIDI in CTRLMMR_ICSSG[2:0]_CTRL[2:0] register.

Figure 3-4. PRU_ICSSG GPO/GPI pin Connectivity

4 PRU_ICSSG Integration

The PRU_ICSSG0 and PRU_ICSSG1 subsystems integration in the device is shown in [Figure 4-1](#) and [Figure 4-2](#).

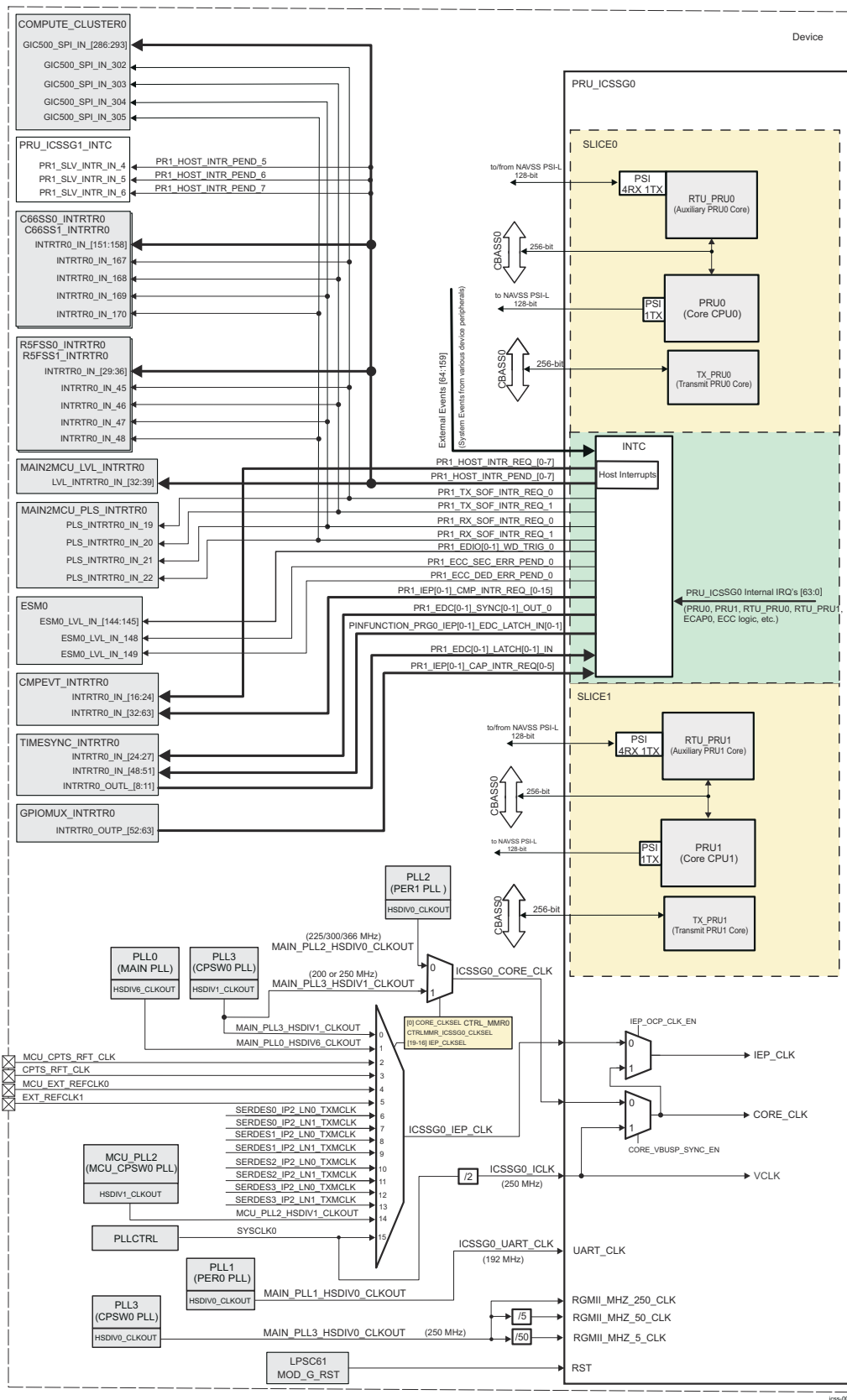


Figure 4-1. PRU_ICSSG0 Integration

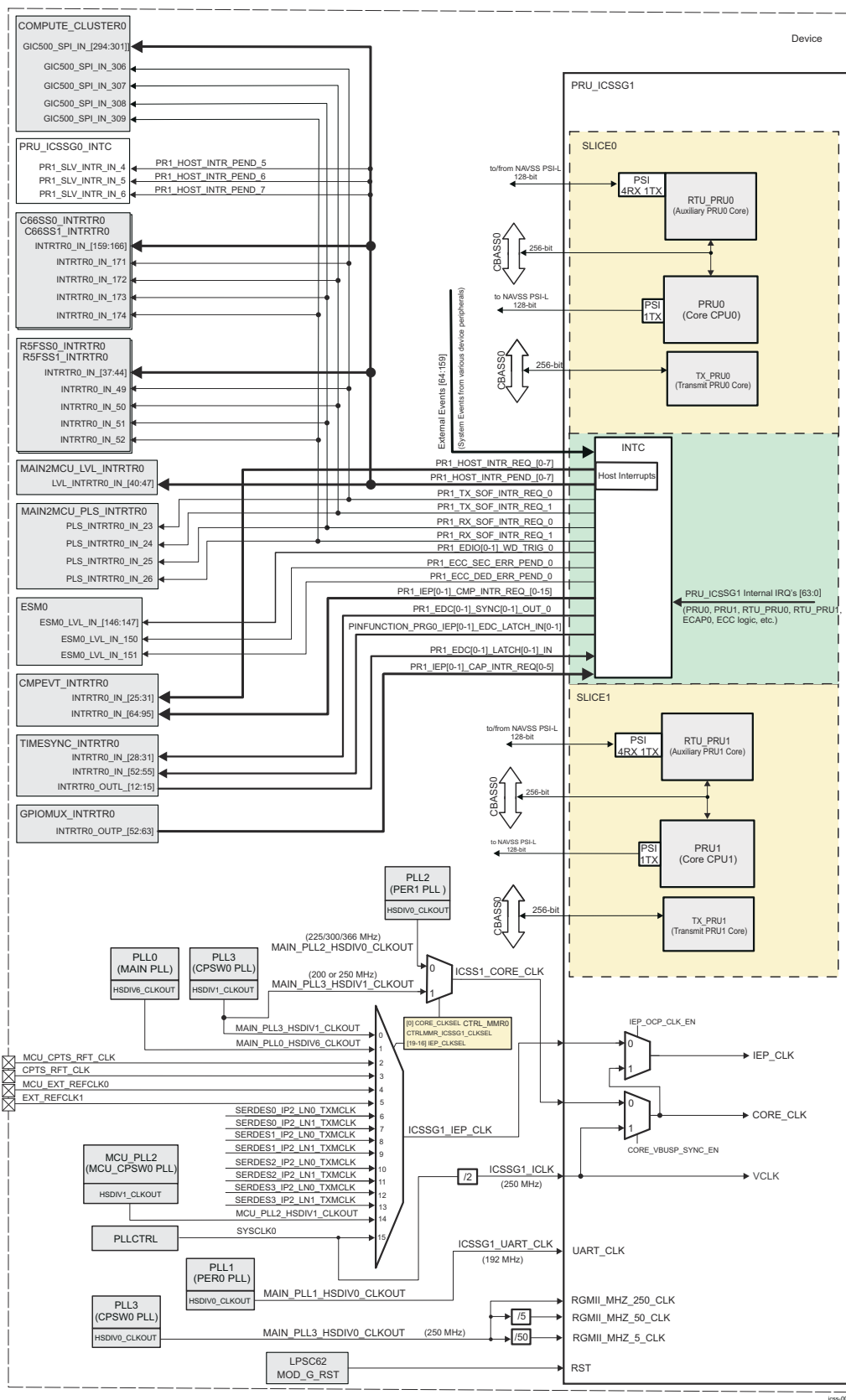


Figure 4-2. PRU_ICSSG1 Integration

The PRU_ICSSG0 and PRU_ICSSG1 integration in the device features:

- PD6 and PD7 power domains instantiation
- One master port for each Slice (shared between PRU0/RTU_PRU0 and PRU1/RTU_PRU1 core initiators) on the device CBASS0 interconnect
- One slave (configuration) port on the CBASS0 interconnect for device hosts (Compute cluster: dual Arm Cortex-A72) to access various memories and registers of PRU_ICSSG
- 20 output interrupt events from local interrupt controllers — INTC:
 - 2 events to each PRU and TX_PRU core (events 0 and 1)
 - 2 events (event 10 and 11) are connected to both auxiliary cores (RTU_PRU0 and RTU_PRU1)
 - 8 events (ICSSG_n_HOST_INTi, where n = 0 or 1 and i = 0 to 7), exported from PRU_ICSSGn (where n = 0 or 1) internal INTC's and mapped to the device interrupt controllers
 - 8 events (event 12 through 19) mapped to each of the 6 Task Managers
- A local software gating of clocks to several modules within PRU subsystem (local clock management protocol), as follows:
 - IEP0 and IEP1
 - ECAP0
 - UART0
 - INTC
 - SLICE0
 - SLICE1
- 7 input clocks obtained from device PLL0 (MAIN PLL), MCU_PLL2 (MCU_CPSW PLL), PLLCTRL, PLL1 (PER0 PLL), PLL2 (PER1 PLL) and PLL3 (CPSW0 PLL) :
 - a ICSSGn_CORE_CLK (where n = 0 or 1) core clock
 - a ICSSGn_IEP_CLK functional clock
 - a ICSSGn_ICLK interface clock
 - a ICSSGn_UART_CLK clock
 - a RGMII_MHZ_250_CLK reference clock
 - a RGMII_MHZ_50_CLK reference clock
 - a RGMII_MHZ_5_CLK reference clock
- 7 input clocks obtained from device PLL0 (MAIN PLL), PLL1 (PER0 PLL), PLL2 (PER1 PLL) and PLLCTRL :
 - a ICSSGn_CORE_CLK (where n = 0 or 1) core clock
 - a ICSSGn_IEP_CLK functional clock
 - a ICSSGn_ICLK interface clock
 - a ICSSGn_UART_CLK clock
 - a RGMII_MHZ_250_CLK reference clock
 - a RGMII_MHZ_50_CLK reference clock
 - a RGMII_MHZ_5_CLK reference clock
- Two input clocks: RGMII0_RXC_I and RGMII1_RXC_I and 2 output clocks: RGMII0_TXC_O and RGMII1_TXC_O, passed as external clocks on device I/Os
- One MDIO_MDCLK, passed as external clock on device I/Os

Table 4-1 through Table 4-3 summarize the integration of PRU_ICSSG0 and PRU_ICSSG1 modules in the device.

Table 4-1. PRU_ICSSG Integration Attributes

Module Instance	Attributes			
	Power Sleep Controller	Power Domain	Module Domain	Interconnect
PRU_ICSSG0	PSC0	PD3	LPSC61	CBASS0
PRU_ICSSG1	PSC0	PD3	LPSC62	CBASS0

Table 4-2. PRU_ICSSG Clocks and Resets

Clocks

Table 4-2. PRU_ICSSG Clocks and Resets (continued)

Module Instance	Module Clock Input	Source Clock Signal	Source	Description
PRU_ICSSG 0	ICSSG0_CORE_CLK	MAIN_PLL2_HSDIV0_CLK OUT	HSDIV0 of PLL2 (PER1 PLL)	PRU_ICSSG0 Core clock. Selected through [0] CORE_CLKSEL.
		MAIN_PLL3_HSDIV1_CLK OUT	HSDIV1 of PLL3 (CPSW0 PLL)	
	ICSSG0_IEP_CLK	MAIN_PLL3_HSDIV1_CLK OUT	HSDIV1 of PLL3 (CPSW0 PLL)	PRU_ICSSG0 Industrial Ethernet Peripheral functional clock. Selected through [19-16] IEP_CLKSEL.
		MAIN_PLL0_HSDIV6_CLK OUT	HSDIV6 of PLL0 (MAIN PLL)	
		MCU_CPTS_RFT_CLK	MCU_CPTS_RFT_CLK pin	
		CPTS_RFT_CLK	CPTS_RFT_CLK pin	
		MCU_EXT_REFCLK0	MCU_EXT_REFCLK0 pin	
		EXT_REFCLK1	EXT_REFCLK1 pin	
		SERDES0_IP2_LN0_TXMC LK	SERDES0, Lane 0, PCIe0	
		SERDES0_IP2_LN1_TXMC LK	SERDES0, Lane 1, PCIe0	
		SERDES1_IP2_LN0_TXMC LK	SERDES1, Lane 0, PCIe1	
		SERDES1_IP2_LN1_TXMC LK	SERDES1, Lane 1, PCIe1	
		SERDES2_IP2_LN0_TXMC LK	SERDES2, Lane 0, PCIe2	
		SERDES2_IP2_LN1_TXMC LK	SERDES2, Lane 1, PCIe2	
		SERDES3_IP2_LN0_TXMC LK	SERDES3, Lane 0, PCIe3	
		SERDES3_IP2_LN1_TXMC LK	SERDES3, Lane 1, PCIe3	
		MCU_PLL2_HSDIV1_CLKO UT	HSDIV1 of MCU_PLL2 (MCU_CPSW0 PLL)	
		SYSCLK0	PLLCTRL	
	ICSSG0_ICLK	SYSCLK0/2	PLLCTRL	PRU_ICSSG0 Interface clock. Clocks both VBUSP slave and VBUSM master ports.
	ICSSG0_UART_CLK	MAIN_PLL1_HSDIV0_CLK OUT	HSDIV0 of PLL1 (PER0 PLL)	PRU_ICSSG0 UART0 functional clock.
	RGMII_MHZ_250_CLK	MAIN_PLL3_HSDIV0_CLK OUT	HSDIV0 of PLL3 (CPSW0 PLL)	RGMII 250MHz reference clock
	RGMII_MHZ_50_CLK	MAIN_PLL3_HSDIV0_CLK OUT/5	HSDIV0 of PLL3 (CPSW0 PLL)	RGMII 50MHz reference clock
	RGMII_MHZ_5_CLK	MAIN_PLL3_HSDIV0_CLK OUT/50	HSDIV0 of PLL3 (CPSW0 PLL)	RGMII 5MHz reference clock
PRU_ICSSG 1	ICSSG1_CORE_CLK	MAIN_PLL2_HSDIV0_CLK OUT	HSDIV0 of PLL2 (PER1 PLL)	PRU_ICSSG1 Core clock. Selected through [0] CORE_CLKSEL.
		MAIN_PLL3_HSDIV1_CLK OUT	HSDIV1 of PLL3 (CPSW0 PLL)	

Table 4-2. PRU_ICSSG Clocks and Resets (continued)

ICSSG1_IEP_CLK	MAIN_PLL3_HSDIV1_CLK OUT	HSDIV1 of PLL3 (CPSW0 PLL)	PRU_ICSSG1 Industrial Ethernet Peripheral functional clock. Selected through [19-16] IEP_CLKSEL.
	MAIN_PLL0_HSDIV6_CLK OUT	HSDIV6 of PLL0 (MAIN PLL)	
	MCU_CPTS_RFT_CLK	MCU_CPTS_RFT_CLK pin	
	CPTS_RFT_CLK	CPTS_RFT_CLK pin	
	MCU_EXT_REFCLK0	MCU_EXT_REFCLK0 pin	
	EXT_REFCLK1	EXT_REFCLK1 pin	
	SERDES0_IP2_LN0_TXMC LK	SERDES0, Lane 0, PCIe0 LK	
	SERDES0_IP2_LN1_TXMC LK	SERDES0, Lane 1, PCIe0 LK	
	SERDES1_IP2_LN0_TXMC LK	SERDES1, Lane 0, PCIe1 LK	
	SERDES1_IP2_LN1_TXMC LK	SERDES1, Lane 1, PCIe1 LK	
	SERDES2_IP2_LN0_TXMC LK	SERDES2, Lane 0, PCIe2 LK	
	SERDES2_IP2_LN1_TXMC LK	SERDES2, Lane 1, PCIe2 LK	
	SERDES3_IP2_LN0_TXMC LK	SERDES3, Lane 0, PCIe3 LK	
	SERDES3_IP2_LN1_TXMC LK	SERDES3, Lane 1, PCIe3 LK	
	MCU_PLL2_HSDIV1_CLKO UT	HSDIV1 of MCU_PLL2 (MCU_CPSW0 PLL)	
ICSSG1_ICLK	SYSCLK0	PLLCTRL	PRU_ICSSG1 Interface clock. Clocks both VBUSP slave and VBUSM master ports.
	SYSCLK0/2	PLLCTRL	
ICSSG1_UART_CLK	MAIN_PLL1_HSDIV0_CLK OUT	HSDIV0 of PLL1 (PER0 PLL)	PRU_ICSSG1 UART0 functional clock.
RGMII_MHZ_250_CLK	MAIN_PLL3_HSDIV0_CLK OUT	HSDIV0 of PLL3 (CPSW0 PLL)	RGMII 250MHz reference clock
RGMII_MHZ_50_CLK	MAIN_PLL3_HSDIV0_CLK OUT/5	HSDIV0 of PLL3 (CPSW0 PLL)	RGMII 50MHz reference clock
RGMII_MHZ_5_CLK	MAIN_PLL3_HSDIV0_CLK OUT/50	HSDIV0 of PLL3 (CPSW0 PLL)	RGMII 5MHz reference clock
LN0_REFCLK	IP4_LN0_REFCLK	SERDES1 or SERDES2 Clock Outputs	PRU_ICSSG1 SGMII1#GUID-F9E1185C-3385-4B48-8731-0E562B30AC61/T6101203-1 reference clocks. Selected through [28] SGMII_SERDES_SEL.
LN0_TXFCLK	IP4_LN0_TXFCLK	SERDES1 or SERDES2 Clock Outputs	
LN0_TXMCLK	IP4_LN0_TXMCLK	SERDES1 or SERDES2 Clock Outputs	
LN0_RXFCLK	IP4_LN0_RXFCLK	SERDES1 or SERDES2 Clock Outputs	
LN0_RXCLK	IP4_LN0_RXCLK	SERDES1 or SERDES2 Clock Outputs	
LN0_TXCLK	IP4_LN0_TXCLK	SERDES1 or SERDES2 Clock Outputs	

Table 4-2. PRU_ICSSG Clocks and Resets (continued)

LN1_REFCLK	IP4_LN1_REFCLK	SERDES1 or SERDES2 Clock Outputs	PRU_ICSSG1 SGMII2#GUID- F9E1185C-3385-4B48-8731-0E562B30AC61/T6101203-1 reference clocks. Selected through Demultiplexer and controlled by [28] SGMII_SERDES_SEL.
LN1_TXFCLK	IP4_LN1_TXFCLK	SERDES1 or SERDES2 Clock Outputs	
LN1_TXMCLK	IP4_LN1_TXMCLK	SERDES1 or SERDES2 Clock Outputs	
LN1_RXFCLK	IP4_LN1_RXFCLK	SERDES1 or SERDES2 Clock Outputs	
LN1_RXCLK	IP4_LN1_RXCLK	SERDES1 or SERDES2 Clock Outputs	
LN1_TXCLK	IP4_LN1_TXCLK	SERDES1 or SERDES2 Clock Outputs	

Resets				
Module Instance	Module Reset Input	Source Reset Signal	Source	Description
PRU_ICSSG0	ICSSG0_RST	MOD_G_RST	LPSC61	Module Reset
PRU_ICSSG1	ICSSG1_RST	MOD_G_RST	LPSC62	Module Reset

- SGMII is supported only for PRU_ICSSG1 instance.

Table 4-3. PRU_ICSSG Hardware Requests

Interrupt Requests					
Module Instance	Module Interrupt Signal	Destination Interrupt Input	Destination	Description	Type
PRU_ICSSG0	PRU_ICSSG0_PR1_HOST_I NTR_PEND_0	GIC500_SPI_IN_286	COMPUTE_CLUSTER0	Host interrupt 0	Level
		C66SS0_INTRTR0_IN_151	C66SS0_INTRTR0		
		C66SS1_INTRTR0_IN_151	C66SS1_INTRTR0		
		R5FSS0_INTRTR0_IN_29	R5FSS0_INTRTR0		
		R5FSS1_INTRTR0_IN_29	R5FSS1_INTRTR0		
		MAIN2MCU_LVL_INTRTR0_I N_32	MAIN2MCU_LVL_INTRTR0		
PRU_ICSSG0	PRU_ICSSG0_PR1_HOST_I NTR_PEND_1	GIC500_SPI_IN_287	COMPUTE_CLUSTER0	Host interrupt 1	Level
		C66SS0_INTRTR0_IN_152	C66SS0_INTRTR0		
		C66SS1_INTRTR0_IN_152	C66SS1_INTRTR0		
		R5FSS0_INTRTR0_IN_30	R5FSS0_INTRTR0		
		R5FSS1_INTRTR0_IN_30	R5FSS1_INTRTR0		
		MAIN2MCU_LVL_INTRTR0_I N_33	MAIN2MCU_LVL_INTRTR0		
PRU_ICSSG0	PRU_ICSSG0_PR1_HOST_I NTR_PEND_2	GIC500_SPI_IN_288	COMPUTE_CLUSTER0	Host interrupt 2	Level
		C66SS0_INTRTR0_IN_153	C66SS0_INTRTR0		
		C66SS1_INTRTR0_IN_153	C66SS1_INTRTR0		
		R5FSS0_INTRTR0_IN_31	R5FSS0_INTRTR0		
		R5FSS1_INTRTR0_IN_31	R5FSS1_INTRTR0		
		MAIN2MCU_LVL_INTRTR0_I N_34	MAIN2MCU_LVL_INTRTR0		
PRU_ICSSG0	PRU_ICSSG0_PR1_HOST_I NTR_PEND_3	GIC500_SPI_IN_289	COMPUTE_CLUSTER0	Host interrupt 3	Level
		C66SS0_INTRTR0_IN_154	C66SS0_INTRTR0		
		C66SS1_INTRTR0_IN_154	C66SS1_INTRTR0		
		R5FSS0_INTRTR0_IN_32	R5FSS0_INTRTR0		

Table 4-3. PRU_ICSSG Hardware Requests (continued)

	R5FSS1_INTRTR0_IN_32	R5FSS1_INTRTR0		
	MAIN2MCU_LVL_INTRTR0_I N_35	MAIN2MCU_LVL_INTR TR0		
PRU_ICSSG0_PR1_HOST_I NTR_PEND_4	GIC500_SPI_IN_290	COMPUTE_CLUSTER	Host interrupt 4	Level 0
	C66SS0_INTRTR0_IN_155	C66SS0_INTRTR0		
	C66SS1_INTRTR0_IN_155	C66SS1_INTRTR0		
	R5FSS0_INTRTR0_IN_33	R5FSS0_INTRTR0		
	R5FSS1_INTRTR0_IN_33	R5FSS1_INTRTR0		
	MAIN2MCU_LVL_INTRTR0_I N_36	MAIN2MCU_LVL_INTR TR0		
PRU_ICSSG0_PR1_HOST_I NTR_PEND_5	GIC500_SPI_IN_291	COMPUTE_CLUSTER	Host interrupt 5	Level 0
	PRU_ICSSG1_PR1_SLV_INT R_IN_4	PRU_ICSSG1_INTC		
	C66SS0_INTRTR0_IN_156	C66SS0_INTRTR0		
	C66SS1_INTRTR0_IN_156	C66SS1_INTRTR0		
	R5FSS0_INTRTR0_IN_34	R5FSS0_INTRTR0		
	R5FSS1_INTRTR0_IN_34	R5FSS1_INTRTR0		
	MAIN2MCU_LVL_INTRTR0_I N_37	MAIN2MCU_LVL_INTR TR0		
PRU_ICSSG0_PR1_HOST_I NTR_PEND_6	GIC500_SPI_IN_292	COMPUTE_CLUSTER	Host interrupt 6	Level 0
	PRU_ICSSG1_PR1_SLV_INT R_IN_5	PRU_ICSSG1_INTC		
	C66SS0_INTRTR0_IN_157	C66SS0_INTRTR0		
	C66SS1_INTRTR0_IN_157	C66SS1_INTRTR0		
	R5FSS0_INTRTR0_IN_35	R5FSS0_INTRTR0		
	R5FSS1_INTRTR0_IN_35	R5FSS1_INTRTR0		
	MAIN2MCU_LVL_INTRTR0_I N_38	MAIN2MCU_LVL_INTR TR0		
PRU_ICSSG0_PR1_HOST_I NTR_PEND_7	GIC500_SPI_IN_293	COMPUTE_CLUSTER	Host interrupt 7	Level 0
	PRU_ICSSG1_PR1_SLV_INT R_IN_6	PRU_ICSSG1_INTC		
	C66SS0_INTRTR0_IN_158	C66SS0_INTRTR0		
	C66SS1_INTRTR0_IN_158	C66SS1_INTRTR0		
	R5FSS0_INTRTR0_IN_36	R5FSS0_INTRTR0		
	R5FSS1_INTRTR0_IN_36	R5FSS1_INTRTR0		
	MAIN2MCU_LVL_INTRTR0_I N_39	MAIN2MCU_LVL_INTR TR0		
PRU_ICSSG0_PR1_TX_SOF _INTR_REQ_0	GIC500_SPI_IN_302	COMPUTE_CLUSTER	Transmit SOF 0 interrupt	Pulse 0
	C66SS0_INTRTR0_IN_167	C66SS0_INTRTR0		
	C66SS1_INTRTR0_IN_167	C66SS1_INTRTR0		
	R5FSS0_INTRTR0_IN_45	R5FSS0_INTRTR0		
	R5FSS1_INTRTR0_IN_45	R5FSS1_INTRTR0		
	MAIN2MCU_PLS_INTRTR0_I N_19	MAIN2MCU_INTRTR_ PLS		
PRU_ICSSG0_PR1_TX_SOF _INTR_REQ_1	GIC500_SPI_IN_303	COMPUTE_CLUSTER	Transmit SOF 1 interrupt	Pulse 0
	C66SS0_INTRTR0_IN_168	C66SS0_INTRTR0		
	C66SS1_INTRTR0_IN_168	C66SS1_INTRTR0		

Table 4-3. PRU_ICSSG Hardware Requests (continued)

		R5FSS0_INTRTR0_IN_46	R5FSS0_INTRTR0		
		R5FSS1_INTRTR0_IN_46	R5FSS1_INTRTR0		
		MAIN2MCU_PLS_INTRTR0_I N_20	MAIN2MCU_PLS_INT RTR0		
PRU_ICSSG0_PR1_RX_SOF _INTR_REQ_0		GIC500_SPI_IN_304	COMPUTE_CLUSTER 0	PRU_ICSSG0 receive SOF 0 interrupt	Pulse
		C66SS0_INTRTR0_IN_169	C66SS0_INTRTR0		
		C66SS1_INTRTR0_IN_169	C66SS1_INTRTR0		
		R5FSS0_INTRTR0_IN_47	R5FSS0_INTRTR0		
		R5FSS1_INTRTR0_IN_47	R5FSS1_INTRTR0		
		MAIN2MCU_PLS_INTRTR0_I N_21	MAIN2MCU_PLS_INT RTR0		
PRU_ICSSG0_PR1_RX_SOF _INTR_REQ_1		GIC500_SPI_IN_305	COMPUTE_CLUSTER 0	PRU_ICSSG0 receive SOF 1 interrupt	Pulse
		C66SS0_INTRTR0_IN_170	C66SS0_INTRTR0		
		C66SS1_INTRTR0_IN_170	C66SS1_INTRTR0		
		R5FSS0_INTRTR0_IN_48	R5FSS0_INTRTR0		
		R5FSS1_INTRTR0_IN_48	R5FSS1_INTRTR0		
		MAIN2MCU_PLS_INTRTR0_I N_22	MAIN2MCU_PLS_INT RTR0		
PRU_ICSSG0_PR1_EDIO0_ WD_TRIG_0		ESM0_LVL_IN_144	ESM0	EDIO0 watchdog trigger interrupt	Level
PRU_ICSSG0_PR1_EDIO1_ WD_TRIG_0		ESM0_LVL_IN_145	ESM0	EDIO1 watchdog trigger interrupt	Level
PRU_ICSSG0_PR1_ECC_SE C_ERR_PEND_0		ESM0_LVL_IN_148	ESM0	SEC ECC error interrupt	Level
PRU_ICSSG0_PR1_ECC_DE D_ERR_PEND_0		ESM0_LVL_IN_149	ESM0	DED ECC error interrupt	Level
PRU_ICSSG1 PRU_ICSSG1_PR1_HOST_I NTR_PEND_0		GIC500_SPI_IN_294	COMPUTE_CLUSTER 0	Host interrupt 0	Level
		C66SS0_INTRTR0_IN_159	C66SS0_INTRTR0		
		C66SS1_INTRTR0_IN_159	C66SS1_INTRTR0		
		R5FSS0_INTRTR0_IN_37	R5FSS0_INTRTR0		
		R5FSS1_INTRTR0_IN_37	R5FSS1_INTRTR0		
		MAIN2MCU_LVL_INTRTR0_I N_40	MAIN2MCU_LVL_INTR TR0		
PRU_ICSSG1_PR1_HOST_I NTR_PEND_1		GIC500_SPI_IN_295	COMPUTE_CLUSTER 0	Host interrupt 1	Level
		C66SS0_INTRTR0_IN_160	C66SS0_INTRTR0		
		C66SS1_INTRTR0_IN_160	C66SS1_INTRTR0		
		R5FSS0_INTRTR0_IN_38	R5FSS0_INTRTR0		
		R5FSS1_INTRTR0_IN_38	R5FSS1_INTRTR0		
		MAIN2MCU_LVL_INTRTR0_I N_41	MAIN2MCU_LVL_INTR TR0		
PRU_ICSSG1_PR1_HOST_I NTR_PEND_2		GIC500_SPI_IN_296	COMPUTE_CLUSTER 0	Host interrupt 2	Level
		C66SS0_INTRTR0_IN_161	C66SS0_INTRTR0		
		C66SS1_INTRTR0_IN_161	C66SS1_INTRTR0		
		R5FSS0_INTRTR0_IN_39	R5FSS0_INTRTR0		
		R5FSS1_INTRTR0_IN_39	R5FSS1_INTRTR0		
		MAIN2MCU_LVL_INTRTR0_I N_42	MAIN2MCU_LVL_INTR TR0		

Table 4-3. PRU_ICSSG Hardware Requests (continued)

PRU_ICSSG1_PR1_HOST_I NTR_PEND_3	GIC500_SPI_IN_297	COMPUTE_CLUSTER	Host interrupt 3	Level
	C66SS0_INTRTR0_IN_162	C66SS0_INTRTR0		
	C66SS1_INTRTR0_IN_162	C66SS1_INTRTR0		
	R5FSS0_INTRTR0_IN_40	R5FSS0_INTRTR0		
	R5FSS1_INTRTR0_IN_40	R5FSS1_INTRTR0		
	MAIN2MCU_LVL_INTRTR0_I N_43	MAIN2MCU_LVL_INTR TR0		
PRU_ICSSG1_PR1_HOST_I NTR_PEND_4	GIC500_SPI_IN_298	COMPUTE_CLUSTER	Host interrupt 4	Level
	C66SS0_INTRTR0_IN_163	C66SS0_INTRTR0		
	C66SS1_INTRTR0_IN_163	C66SS1_INTRTR0		
	R5FSS0_INTRTR0_IN_41	R5FSS0_INTRTR0		
	R5FSS1_INTRTR0_IN_41	R5FSS1_INTRTR0		
	MAIN2MCU_LVL_INTRTR0_I N_44	MAIN2MCU_LVL_INTR TR0		
PRU_ICSSG1_PR1_HOST_I NTR_PEND_5	GIC500_SPI_IN_299	COMPUTE_CLUSTER	Host interrupt 5	Level
	PRU_ICSSG0_PR1_SLV_INT R_IN_4	PRU_ICSSG0_INTC		
	C66SS0_INTRTR0_IN_164	C66SS0_INTRTR0		
	C66SS1_INTRTR0_IN_164	C66SS1_INTRTR0		
	R5FSS0_INTRTR0_IN_42	R5FSS0_INTRTR0		
	R5FSS1_INTRTR0_IN_42	R5FSS1_INTRTR0		
PRU_ICSSG1_PR1_HOST_I NTR_PEND_6	GIC500_SPI_IN_300	COMPUTE_CLUSTER	Host interrupt 6	Level
	PRU_ICSSG0_PR1_SLV_INT R_IN_5	PRU_ICSSG0_INTC		
	C66SS0_INTRTR0_IN_165	C66SS0_INTRTR0		
	C66SS1_INTRTR0_IN_165	C66SS1_INTRTR0		
	R5FSS0_INTRTR0_IN_43	R5FSS0_INTRTR0		
	R5FSS1_INTRTR0_IN_43	R5FSS1_INTRTR0		
PRU_ICSSG1_PR1_HOST_I NTR_PEND_7	GIC500_SPI_IN_301	COMPUTE_CLUSTER	Host interrupt 7	Level
	PRU_ICSSG0_PR1_SLV_INT R_IN_6	PRU_ICSSG0_INTC		
	C66SS0_INTRTR0_IN_166	C66SS0_INTRTR0		
	C66SS1_INTRTR0_IN_166	C66SS1_INTRTR0		
	R5FSS0_INTRTR0_IN_44	R5FSS0_INTRTR0		
	R5FSS1_INTRTR0_IN_44	R5FSS1_INTRTR0		
PRU_ICSSG1_PR1_TX_SOF _INTR_REQ_0	MAIN2MCU_LVL_INTRTR0_I N_47	MAIN2MCU_LVL_INTR TR0		
	GIC500_SPI_IN_306	COMPUTE_CLUSTER	Transmit SOF 0 interrupt	Pulse
	C66SS0_INTRTR0_IN_171	C66SS0_INTRTR0		
	C66SS1_INTRTR0_IN_171	C66SS1_INTRTR0		
	R5FSS0_INTRTR0_IN_49	R5FSS0_INTRTR0		
	R5FSS1_INTRTR0_IN_49	R5FSS1_INTRTR0		

Table 4-3. PRU_ICSSG Hardware Requests (continued)

	MAIN2MCU_PLS_INTRTR0_I N_23	MAIN2MCU_INTRTR_ PLS		
PRU_ICSSG1_PR1_TX_SOF _INTR_REQ_1	GIC500_SPI_IN_307	COMPUTE_CLUSTER 0	Transmit SOF 1 interrupt	Pulse
	C66SS0_INTRTR0_IN_172	C66SS0_INTRTR0		
	C66SS1_INTRTR0_IN_172	C66SS1_INTRTR0		
	R5FSS0_INTRTR0_IN_50	R5FSS0_INTRTR0		
	R5FSS1_INTRTR0_IN_50	R5FSS1_INTRTR0		
	MAIN2MCU_PLS_INTRTR0_I N_24	MAIN2MCU_INTRTR_ PLS		
PRU_ICSSG1_PR1_RX_SOF _INTR_REQ_0	GIC500_SPI_IN_308	COMPUTE_CLUSTER 0	Transmit SOF 0 interrupt	Pulse
	C66SS0_INTRTR0_IN_173	C66SS0_INTRTR0		
	C66SS1_INTRTR0_IN_173	C66SS1_INTRTR0		
	R5FSS0_INTRTR0_IN_51	R5FSS0_INTRTR0		
	R5FSS1_INTRTR0_IN_51	R5FSS1_INTRTR0		
	MAIN2MCU_PLS_INTRTR0_I N_25	MAIN2MCU_INTRTR_ PLS		
PRU_ICSSG1_PR1_RX_SOF _INTR_REQ_1	GIC500_SPI_IN_309	COMPUTE_CLUSTER 0	Transmit SOF 1 interrupt	Pulse
	C66SS0_INTRTR0_IN_174	C66SS0_INTRTR0		
	C66SS1_INTRTR0_IN_174	C66SS1_INTRTR0		
	R5FSS0_INTRTR0_IN_52	R5FSS0_INTRTR0		
	R5FSS1_INTRTR0_IN_52	R5FSS1_INTRTR0		
	MAIN2MCU_PLS_INTRTR0_I N_26	MAIN2MCU_INTRTR_ PLS		
PRU_ICSSG1_PR1_EDIO0_ WD_TRIG_0	ESM0_LVL_IN_146	ESM0	EDIO0 watchdog trigger interrupt	Level
PRU_ICSSG1_PR1_EDIO1_ WD_TRIG_0	ESM0_LVL_IN_147	ESM0	EDIO1 watchdog trigger interrupt	Level
PRU_ICSSG1_PR1_ECC_SE C_ERR_PEND_0	ESM0_LVL_IN_150	ESM0	SEC ECC error interrupt	Level
PRU_ICSSG1_PR1_ECC_DE D_ERR_PEND_0	ESM0_LVL_IN_151	ESM0	PRU_ICSSG1 DED ECC error interrupt	Level

Compare Event Outputs					
Module Instance	Module Event	Destination Event Input	Destination	Description	Type
PRU_ICSSG0	PRU_ICSSG0_PR1_HOST_I NTR_REQ_0	CMPEVENT_INTRTR0_IN_1 6	CMPEVT_INTRTR0	Host interrupt request 0	Pulse
	PRU_ICSSG0_PR1_HOST_I NTR_REQ_1	CMPEVENT_INTRTR0_IN_1 7	CMPEVT_INTRTR0	Host interrupt request 1	Pulse
	PRU_ICSSG0_PR1_HOST_I NTR_REQ_2	CMPEVENT_INTRTR0_IN_1 8	CMPEVT_INTRTR0	Host interrupt request 2	Pulse
	PRU_ICSSG0_PR1_HOST_I NTR_REQ_3	CMPEVENT_INTRTR0_IN_1 9	CMPEVT_INTRTR0	Host interrupt request 3	Pulse
	PRU_ICSSG0_PR1_HOST_I NTR_REQ_4	CMPEVENT_INTRTR0_IN_2 0	CMPEVT_INTRTR0	Host interrupt request 4	Pulse
	PRU_ICSSG0_PR1_HOST_I NTR_REQ_5	CMPEVENT_INTRTR0_IN_2 1	CMPEVT_INTRTR0	Host interrupt request 5	Pulse
	PRU_ICSSG0_PR1_HOST_I NTR_REQ_6	CMPEVENT_INTRTR0_IN_2 2	CMPEVT_INTRTR0	Host interrupt request 6	Pulse
	PRU_ICSSG0_PR1_HOST_I NTR_REQ_7	CMPEVENT_INTRTR0_IN_2 3	CMPEVT_INTRTR0	Host interrupt request 7	Pulse
	PRU_ICSSG0_PR1_IEP0_C MP_INTR_REQ_0	CMPEVENT_INTRTR0_IN_3 2	CMPEVT_INTRTR0	IEP0 Compare timer 0 interrupt	Pulse

Table 4-3. PRU_ICSSG Hardware Requests (continued)

PRU_ICSSG0_PR1_IEP0_C MP_INTR_REQ_1	CMPEVENT_INTRTR0_IN_3 3	CMPEVT_INTRTR0	IEP0 Compare timer 1 interrupt	Pulse
PRU_ICSSG0_PR1_IEP0_C MP_INTR_REQ_2	CMPEVENT_INTRTR0_IN_3 4	CMPEVT_INTRTR0	IEP0 Compare timer 2 interrupt	Pulse
PRU_ICSSG0_PR1_IEP0_C MP_INTR_REQ_3	CMPEVENT_INTRTR0_IN_3 5	CMPEVT_INTRTR0	IEP0 Compare timer 3 interrupt	Pulse
PRU_ICSSG0_PR1_IEP0_C MP_INTR_REQ_4	CMPEVENT_INTRTR0_IN_3 6	CMPEVT_INTRTR0	IEP0 Compare timer 4 interrupt	Pulse
PRU_ICSSG0_PR1_IEP0_C MP_INTR_REQ_5	CMPEVENT_INTRTR0_IN_3 7	CMPEVT_INTRTR0	IEP0 Compare timer 5 interrupt	Pulse
PRU_ICSSG0_PR1_IEP0_C MP_INTR_REQ_6	CMPEVENT_INTRTR0_IN_3 8	CMPEVT_INTRTR0	IEP0 Compare timer 6 interrupt	Pulse
PRU_ICSSG0_PR1_IEP0_C MP_INTR_REQ_7	CMPEVENT_INTRTR0_IN_3 9	CMPEVT_INTRTR0	IEP0 Compare timer 7 interrupt	Pulse
PRU_ICSSG0_PR1_IEP0_C MP_INTR_REQ_8	CMPEVENT_INTRTR0_IN_4 0	CMPEVT_INTRTR0	IEP0 Compare timer 8 interrupt	Pulse
PRU_ICSSG0_PR1_IEP0_C MP_INTR_REQ_9	CMPEVENT_INTRTR0_IN_4 1	CMPEVT_INTRTR0	IEP0 Compare timer 9 interrupt	Pulse
PRU_ICSSG0_PR1_IEP0_C MP_INTR_REQ_10	CMPEVENT_INTRTR0_IN_4 2	CMPEVT_INTRTR0	IEP0 Compare timer 10 interrupt	Pulse
PRU_ICSSG0_PR1_IEP0_C MP_INTR_REQ_11	CMPEVENT_INTRTR0_IN_4 3	CMPEVT_INTRTR0	IEP0 Compare timer 11 interrupt	Pulse
PRU_ICSSG0_PR1_IEP0_C MP_INTR_REQ_12	CMPEVENT_INTRTR0_IN_4 4	CMPEVT_INTRTR0	IEP0 Compare timer 12 interrupt	Pulse
PRU_ICSSG0_PR1_IEP0_C MP_INTR_REQ_13	CMPEVENT_INTRTR0_IN_4 5	CMPEVT_INTRTR0	IEP0 Compare timer 13 interrupt	Pulse
PRU_ICSSG0_PR1_IEP0_C MP_INTR_REQ_14	CMPEVENT_INTRTR0_IN_4 6	CMPEVT_INTRTR0	IEP0 Compare timer 14 interrupt	Pulse
PRU_ICSSG0_PR1_IEP0_C MP_INTR_REQ_15	CMPEVENT_INTRTR0_IN_4 7	CMPEVT_INTRTR0	IEP0 Compare timer 15 interrupt	Pulse
PRU_ICSSG0_PR1_IEP1_C MP_INTR_REQ_0	CMPEVENT_INTRTR0_IN_4 8	CMPEVT_INTRTR0	IEP1 Compare timer 0 interrupt	Pulse
PRU_ICSSG0_PR1_IEP1_C MP_INTR_REQ_1	CMPEVENT_INTRTR0_IN_4 9	CMPEVT_INTRTR0	IEP1 Compare timer 1 interrupt	Pulse
PRU_ICSSG0_PR1_IEP1_C MP_INTR_REQ_2	CMPEVENT_INTRTR0_IN_5 0	CMPEVT_INTRTR0	IEP1 Compare timer 2 interrupt	Pulse
PRU_ICSSG0_PR1_IEP1_C MP_INTR_REQ_3	CMPEVENT_INTRTR0_IN_5 1	CMPEVT_INTRTR0	IEP1 Compare timer 3 interrupt	Pulse
PRU_ICSSG0_PR1_IEP1_C MP_INTR_REQ_4	CMPEVENT_INTRTR0_IN_5 2	CMPEVT_INTRTR0	IEP1 Compare timer 4 interrupt	Pulse
PRU_ICSSG0_PR1_IEP1_C MP_INTR_REQ_5	CMPEVENT_INTRTR0_IN_5 3	CMPEVT_INTRTR0	IEP1 Compare timer 5 interrupt	Pulse
PRU_ICSSG0_PR1_IEP1_C MP_INTR_REQ_6	CMPEVENT_INTRTR0_IN_5 4	CMPEVT_INTRTR0	IEP1 Compare timer 6 interrupt	Pulse
PRU_ICSSG0_PR1_IEP1_C MP_INTR_REQ_7	CMPEVENT_INTRTR0_IN_5 5	CMPEVT_INTRTR0	IEP1 Compare timer 7 interrupt	Pulse
PRU_ICSSG0_PR1_IEP1_C MP_INTR_REQ_8	CMPEVENT_INTRTR0_IN_5 6	CMPEVT_INTRTR0	IEP1 Compare timer 8 interrupt	Pulse
PRU_ICSSG0_PR1_IEP1_C MP_INTR_REQ_9	CMPEVENT_INTRTR0_IN_5 7	CMPEVT_INTRTR0	IEP1 Compare timer 9 interrupt	Pulse
PRU_ICSSG0_PR1_IEP1_C MP_INTR_REQ_10	CMPEVENT_INTRTR0_IN_5 8	CMPEVT_INTRTR0	IEP1 Compare timer 10 interrupt	Pulse
PRU_ICSSG0_PR1_IEP1_C MP_INTR_REQ_11	CMPEVENT_INTRTR0_IN_5 9	CMPEVT_INTRTR0	IEP1 Compare timer 11 interrupt	Pulse
PRU_ICSSG0_PR1_IEP1_C MP_INTR_REQ_12	CMPEVENT_INTRTR0_IN_6 0	CMPEVT_INTRTR0	IEP1 Compare timer 12 interrupt	Pulse

Table 4-3. PRU_ICSSG Hardware Requests (continued)

	PRU_ICSSG0_PR1_IEP1_C MP_INTR_REQ_13	CMPEVENT_INTRTR0_IN_6 1	CMPEVT_INTRTR0	IEP1 Compare timer 13 interrupt	Pulse
	PRU_ICSSG0_PR1_IEP1_C MP_INTR_REQ_14	CMPEVENT_INTRTR0_IN_6 2	CMPEVT_INTRTR0	IEP1 Compare timer 14 interrupt	Pulse
	PRU_ICSSG0_PR1_IEP1_C MP_INTR_REQ_15	CMPEVENT_INTRTR0_IN_6 3	CMPEVT_INTRTR0	IEP1 Compare timer 15 interrupt	Pulse
PRU_ICSSG1	PRU_ICSSG1_PR1_HOST_I NTR_REQ_0	CMPEVENT_INTRTR0_IN_2 4	CMPEVT_INTRTR0	Host interrupt request 0	Pulse
	PRU_ICSSG1_PR1_HOST_I NTR_REQ_1	CMPEVENT_INTRTR0_IN_2 5	CMPEVT_INTRTR0	Host interrupt request 1	Pulse
	PRU_ICSSG1_PR1_HOST_I NTR_REQ_2	CMPEVENT_INTRTR0_IN_2 6	CMPEVT_INTRTR0	Host interrupt request 2	Pulse
	PRU_ICSSG1_PR1_HOST_I NTR_REQ_3	CMPEVENT_INTRTR0_IN_2 7	CMPEVT_INTRTR0	Host interrupt request 3	Pulse
	PRU_ICSSG1_PR1_HOST_I NTR_REQ_4	CMPEVENT_INTRTR0_IN_2 8	CMPEVT_INTRTR0	Host interrupt request 4	Pulse
	PRU_ICSSG1_PR1_HOST_I NTR_REQ_5	CMPEVENT_INTRTR0_IN_2 9	CMPEVT_INTRTR0	Host interrupt request 5	Pulse
	PRU_ICSSG1_PR1_HOST_I NTR_REQ_6	CMPEVENT_INTRTR0_IN_3 0	CMPEVT_INTRTR0	Host interrupt request 6	Pulse
	PRU_ICSSG1_PR1_HOST_I NTR_REQ_7	CMPEVENT_INTRTR0_IN_3 1	CMPEVT_INTRTR0	Host interrupt request 7	Pulse
	PRU_ICSSG1_PR1_IEP0_C MP_INTR_REQ_0	CMPEVENT_INTRTR0_IN_6 4	CMPEVT_INTRTR0	IEP0 Compare timer 0 interrupt	Pulse
	PRU_ICSSG1_PR1_IEP0_C MP_INTR_REQ_1	CMPEVENT_INTRTR0_IN_6 5	CMPEVT_INTRTR0	IEP0 Compare timer 1 interrupt	Pulse
	PRU_ICSSG1_PR1_IEP0_C MP_INTR_REQ_2	CMPEVENT_INTRTR0_IN_6 6	CMPEVT_INTRTR0	IEP0 Compare timer 2 interrupt	Pulse
	PRU_ICSSG1_PR1_IEP0_C MP_INTR_REQ_3	CMPEVENT_INTRTR0_IN_6 7	CMPEVT_INTRTR0	IEP0 Compare timer 3 interrupt	Pulse
	PRU_ICSSG1_PR1_IEP0_C MP_INTR_REQ_4	CMPEVENT_INTRTR0_IN_6 8	CMPEVT_INTRTR0	IEP0 Compare timer 4 interrupt	Pulse
	PRU_ICSSG1_PR1_IEP0_C MP_INTR_REQ_5	CMPEVENT_INTRTR0_IN_6 9	CMPEVT_INTRTR0	IEP0 Compare timer 5 interrupt	Pulse
	PRU_ICSSG1_PR1_IEP0_C MP_INTR_REQ_6	CMPEVENT_INTRTR0_IN_7 0	CMPEVT_INTRTR0	IEP0 Compare timer 6 interrupt	Pulse
	PRU_ICSSG1_PR1_IEP0_C MP_INTR_REQ_7	CMPEVENT_INTRTR0_IN_7 1	CMPEVT_INTRTR0	IEP0 Compare timer 7 interrupt	Pulse
	PRU_ICSSG1_PR1_IEP0_C MP_INTR_REQ_8	CMPEVENT_INTRTR0_IN_7 2	CMPEVT_INTRTR0	IEP0 Compare timer 8 interrupt	Pulse
	PRU_ICSSG1_PR1_IEP0_C MP_INTR_REQ_9	CMPEVENT_INTRTR0_IN_7 3	CMPEVT_INTRTR0	IEP0 Compare timer 9 interrupt	Pulse
	PRU_ICSSG1_PR1_IEP0_C MP_INTR_REQ_10	CMPEVENT_INTRTR0_IN_7 4	CMPEVT_INTRTR0	IEP0 Compare timer 10 interrupt	Pulse
	PRU_ICSSG1_PR1_IEP0_C MP_INTR_REQ_11	CMPEVENT_INTRTR0_IN_7 5	CMPEVT_INTRTR0	IEP0 Compare timer 11 interrupt	Pulse
	PRU_ICSSG1_PR1_IEP0_C MP_INTR_REQ_12	CMPEVENT_INTRTR0_IN_7 6	CMPEVT_INTRTR0	IEP0 Compare timer 12 interrupt	Pulse
	PRU_ICSSG1_PR1_IEP0_C MP_INTR_REQ_13	CMPEVENT_INTRTR0_IN_7 7	CMPEVT_INTRTR0	IEP0 Compare timer 13 interrupt	Pulse
	PRU_ICSSG1_PR1_IEP0_C MP_INTR_REQ_14	CMPEVENT_INTRTR0_IN_7 8	CMPEVT_INTRTR0	IEP0 Compare timer 14 interrupt	Pulse
	PRU_ICSSG1_PR1_IEP0_C MP_INTR_REQ_15	CMPEVENT_INTRTR0_IN_7 9	CMPEVT_INTRTR0	IEP0 Compare timer 15 interrupt	Pulse
	PRU_ICSSG1_PR1_IEP1_C MP_INTR_REQ_0	CMPEVENT_INTRTR0_IN_8 0	CMPEVT_INTRTR0	IEP1 Compare timer 0 interrupt	Pulse

Table 4-3. PRU_ICSSG Hardware Requests (continued)

PRU_ICSSG1_PR1_IEP1_C MP_INTR_REQ_1	CMPEVENT_INTRTR0_IN_8 1	CMPEVT_INTRTR0	IEP1 Compare timer 1 interrupt	Pulse
PRU_ICSSG1_PR1_IEP1_C MP_INTR_REQ_2	CMPEVENT_INTRTR0_IN_8 2	CMPEVT_INTRTR0	IEP1 Compare timer 2 interrupt	Pulse
PRU_ICSSG1_PR1_IEP1_C MP_INTR_REQ_3	CMPEVENT_INTRTR0_IN_8 3	CMPEVT_INTRTR0	IEP1 Compare timer 3 interrupt	Pulse
PRU_ICSSG1_PR1_IEP1_C MP_INTR_REQ_4	CMPEVENT_INTRTR0_IN_8 4	CMPEVT_INTRTR0	IEP1 Compare timer 4 interrupt	Pulse
PRU_ICSSG1_PR1_IEP1_C MP_INTR_REQ_5	CMPEVENT_INTRTR0_IN_8 5	CMPEVT_INTRTR0	IEP1 Compare timer 5 interrupt	Pulse
PRU_ICSSG1_PR1_IEP1_C MP_INTR_REQ_6	CMPEVENT_INTRTR0_IN_8 6	CMPEVT_INTRTR0	IEP1 Compare timer 6 interrupt	Pulse
PRU_ICSSG1_PR1_IEP1_C MP_INTR_REQ_7	CMPEVENT_INTRTR0_IN_8 7	CMPEVT_INTRTR0	IEP1 Compare timer 7 interrupt	Pulse
PRU_ICSSG1_PR1_IEP1_C MP_INTR_REQ_8	CMPEVENT_INTRTR0_IN_8 8	CMPEVT_INTRTR0	IEP1 Compare timer 8 interrupt	Pulse
PRU_ICSSG1_PR1_IEP1_C MP_INTR_REQ_9	CMPEVENT_INTRTR0_IN_8 9	CMPEVT_INTRTR0	IEP1 Compare timer 9 interrupt	Pulse
PRU_ICSSG1_PR1_IEP1_C MP_INTR_REQ_10	CMPEVENT_INTRTR0_IN_9 0	CMPEVT_INTRTR0	IEP1 Compare timer 10 interrupt	Pulse
PRU_ICSSG1_PR1_IEP1_C MP_INTR_REQ_11	CMPEVENT_INTRTR0_IN_9 1	CMPEVT_INTRTR0	IEP1 Compare timer 11 interrupt	Pulse
PRU_ICSSG1_PR1_IEP1_C MP_INTR_REQ_12	CMPEVENT_INTRTR0_IN_9 2	CMPEVT_INTRTR0	IEP1 Compare timer 12 interrupt	Pulse
PRU_ICSSG1_PR1_IEP1_C MP_INTR_REQ_13	CMPEVENT_INTRTR0_IN_9 3	CMPEVT_INTRTR0	IEP1 Compare timer 13 interrupt	Pulse
PRU_ICSSG1_PR1_IEP1_C MP_INTR_REQ_14	CMPEVENT_INTRTR0_IN_9 4	CMPEVT_INTRTR0	IEP1 Compare timer 14 interrupt	Pulse
PRU_ICSSG1_PR1_IEP1_C MP_INTR_REQ_15	CMPEVENT_INTRTR0_IN_9 5	CMPEVT_INTRTR0	IEP1 Compare timer 15 interrupt	Pulse

Capture Event Inputs					
Module Instance	Module Sync Input	Sync Source Signal	Source	Description	Type
PRU_ICSSG0	PRU_ICSSG0_PR1_IEP0_C AP_INTR_REQ0	GPIOMUX_INTRTR0_OUTP_ 52	GPIOMUX_INTRTR0	IEP0 Capture event 0	Pulse
	PRU_ICSSG0_PR1_IEP0_C AP_INTR_REQ1	GPIOMUX_INTRTR0_OUTP_ 53	GPIOMUX_INTRTR0	IEP0 Capture event 1	Pulse
	PRU_ICSSG0_PR1_IEP0_C AP_INTR_REQ2	GPIOMUX_INTRTR0_OUTP_ 54	GPIOMUX_INTRTR0	IEP0 Capture event 2	Pulse
	PRU_ICSSG0_PR1_IEP0_C AP_INTR_REQ3	GPIOMUX_INTRTR0_OUTP_ 55	GPIOMUX_INTRTR0	IEP0 Capture event 3	Pulse
	PRU_ICSSG0_PR1_IEP0_C AP_INTR_REQ4	GPIOMUX_INTRTR0_OUTP_ 56	GPIOMUX_INTRTR0	IEP0 Capture event 4	Pulse
	PRU_ICSSG0_PR1_IEP0_C AP_INTR_REQ5	GPIOMUX_INTRTR0_OUTP_ 57	GPIOMUX_INTRTR0	IEP0 Capture event 5	Pulse
	PRU_ICSSG0_PR1_IEP1_C AP_INTR_REQ0	GPIOMUX_INTRTR0_OUTP_ 58	GPIOMUX_INTRTR0	IEP1 Capture event 0	Pulse
	PRU_ICSSG0_PR1_IEP1_C AP_INTR_REQ1	GPIOMUX_INTRTR0_OUTP_ 59	GPIOMUX_INTRTR0	IEP1 Capture event 1	Pulse
	PRU_ICSSG0_PR1_IEP1_C AP_INTR_REQ2	GPIOMUX_INTRTR0_OUTP_ 60	GPIOMUX_INTRTR0	IEP1 Capture event 2	Pulse
	PRU_ICSSG0_PR1_IEP1_C AP_INTR_REQ3	GPIOMUX_INTRTR0_OUTP_ 61	GPIOMUX_INTRTR0	IEP1 Capture event 3	Pulse
	PRU_ICSSG0_PR1_IEP1_C AP_INTR_REQ4	GPIOMUX_INTRTR0_OUTP_ 62	GPIOMUX_INTRTR0	IEP1 Capture event 4	Pulse
	PRU_ICSSG0_PR1_IEP1_C AP_INTR_REQ5	GPIOMUX_INTRTR0_OUTP_ 63	GPIOMUX_INTRTR0	IEP1 Capture event 5	Pulse

Table 4-3. PRU_ICSSG Hardware Requests (continued)

PRU_ICSSG1	PRU_ICSSG1_PR1_IEP0_C AP_INTR_REQ0	GPIOMUX_INTRTR0_OUTP_ 52	GPIOMUX_INTRTR0	IEP0 Capture event 0	Pulse
	PRU_ICSSG1_PR1_IEP0_C AP_INTR_REQ1	GPIOMUX_INTRTR0_OUTP_ 53	GPIOMUX_INTRTR0	IEP0 Capture event 1	Pulse
	PRU_ICSSG1_PR1_IEP0_C AP_INTR_REQ2	GPIOMUX_INTRTR0_OUTP_ 54	GPIOMUX_INTRTR0	IEP0 Capture event 2	Pulse
	PRU_ICSSG1_PR1_IEP0_C AP_INTR_REQ3	GPIOMUX_INTRTR0_OUTP_ 55	GPIOMUX_INTRTR0	IEP0 Capture event 3	Pulse
	PRU_ICSSG1_PR1_IEP0_C AP_INTR_REQ4	GPIOMUX_INTRTR0_OUTP_ 56	GPIOMUX_INTRTR0	IEP0 Capture event 4	Pulse
	PRU_ICSSG1_PR1_IEP0_C AP_INTR_REQ5	GPIOMUX_INTRTR0_OUTP_ 57	GPIOMUX_INTRTR0	IEP0 Capture event 5	Pulse
	PRU_ICSSG1_PR1_IEP1_C AP_INTR_REQ0	GPIOMUX_INTRTR0_OUTP_ 58	GPIOMUX_INTRTR0	IEP1 Capture event 0	Pulse
	PRU_ICSSG1_PR1_IEP1_C AP_INTR_REQ1	GPIOMUX_INTRTR0_OUTP_ 59	GPIOMUX_INTRTR0	IEP1 Capture event 1	Pulse
	PRU_ICSSG1_PR1_IEP1_C AP_INTR_REQ2	GPIOMUX_INTRTR0_OUTP_ 60	GPIOMUX_INTRTR0	IEP1 Capture event 2	Pulse
	PRU_ICSSG1_PR1_IEP1_C AP_INTR_REQ3	GPIOMUX_INTRTR0_OUTP_ 61	GPIOMUX_INTRTR0	IEP1 Capture event 3	Pulse
	PRU_ICSSG1_PR1_IEP1_C AP_INTR_REQ4	GPIOMUX_INTRTR0_OUTP_ 62	GPIOMUX_INTRTR0	IEP1 Capture event 4	Pulse
	PRU_ICSSG1_PR1_IEP1_C AP_INTR_REQ5	GPIOMUX_INTRTR0_OUTP_ 63	GPIOMUX_INTRTR0	IEP1 Capture event 5	Pulse

Time Sync Event Inputs					
Module Instance	Module Sync Input	Sync Source Signal	Source	Description	Type
PRU_ICSSG0	PRU_ICSSG0_PR1_EDC0_L ATCH0_IN	TIMESYNC_INTRTR0_OUTL_ 8	TIMESYNC_INTRTR0	Selectable time sync event 8	Level
	PRU_ICSSG0_PR1_EDC0_L ATCH1_IN	TIMESYNC_INTRTR0_OUTL_ 9	TIMESYNC_INTRTR0	Selectable time sync event 9	Level
	PRU_ICSSG0_PR1_EDC1_L ATCH0_IN	TIMESYNC_INTRTR0_OUTL_ 10	TIMESYNC_INTRTR0	Selectable time sync event 10	Level
	PRU_ICSSG0_PR1_EDC1_L ATCH1_IN	TIMESYNC_INTRTR0_OUTL_ 11	TIMESYNC_INTRTR0	Selectable time sync event 11	Level
PRU_ICSSG1	PRU_ICSSG1_PR1_EDC0_L ATCH0_IN	TIMESYNC_INTRTR0_OUTL_ 12	TIMESYNC_INTRTR0	Selectable time sync event 12	Level
	PRU_ICSSG1_PR1_EDC0_L ATCH1_IN	TIMESYNC_INTRTR0_OUTL_ 13	TIMESYNC_INTRTR0	Selectable time sync event 13	Level
	PRU_ICSSG1_PR1_EDC1_L ATCH0_IN	TIMESYNC_INTRTR0_OUTL_ 14	TIMESYNC_INTRTR0	Selectable time sync event 14	Level
	PRU_ICSSG1_PR1_EDC1_L ATCH1_IN	TIMESYNC_INTRTR0_OUTL_ 15	TIMESYNC_INTRTR0	Selectable time sync event 15	Level

Time Sync Event Outputs					
Module Instance	Module Sync Output	Destination Sync Input	Destination	Description	Type
PRU_ICSSG0	PRU_ICSSG0_PR1_EDC0_S YNC0_OUT_0	TIMESYNC_INTRTR0_IN_24	TIMESYNC_INTRTR0	IEP0 sync event 0	Pulse
	PRU_ICSSG0_PR1_EDC0_S YNC1_OUT_0	TIMESYNC_INTRTR0_IN_25	TIMESYNC_INTRTR0	IEP0 sync event 1	Pulse
	PRU_ICSSG0_PR1_EDC1_S YNC0_OUT_0	TIMESYNC_INTRTR0_IN_26	TIMESYNC_INTRTR0	IEP1 sync event 0	Pulse
	PRU_ICSSG0_PR1_EDC1_S YNC1_OUT_0	TIMESYNC_INTRTR0_IN_27	TIMESYNC_INTRTR0	IEP1 sync event 1	Pulse
	PINFUNCTION_PRG0_IEP0_ EDC_LATCH_IN0IN_PRG0_I EP0_EDC_LATCH_IN0_0	TIMESYNC_INTRTR0_IN_48	TIMESYNC_INTRTR0	EDC0 Latch 0 input event (I/O pin)	Pulse

Table 4-3. PRU_ICSSG Hardware Requests (continued)

	PINFUNCTION_PRG0_IEP0_	TIMESYNC_INTRTR0_IN_49	TIMESYNC_INTRTR0	EDC0 Latch 1 input event (I/O pin)	Pulse
	EDC_LATCH_IN1IN_PRG0_I				
	EP0_EDC_LATCH_IN1_0				
	PINFUNCTION_PRG0_IEP1_	TIMESYNC_INTRTR0_IN_50	TIMESYNC_INTRTR0	EDC1 Latch 0 input event (I/O pin)	Pulse
	EDC_LATCH_IN0IN_PRG0_I				
	EP1_EDC_LATCH_IN0_0				
	PINFUNCTION_PRG0_IEP1_	TIMESYNC_INTRTR0_IN_51	TIMESYNC_INTRTR0	EDC1 Latch 1 input event (I/O pin)	Pulse
	EDC_LATCH_IN1IN_PRG0_I				
	EP1_EDC_LATCH_IN1_0				
PRU_ICSSG1	PRU_ICSSG1_PR1_EDC0_S	TIMESYNC_INTRTR0_IN_28	TIMESYNC_INTRTR0	IEP0 sync event 0	Pulse
	YNC0_OUT_0				
	PRU_ICSSG1_PR1_EDC0_S	TIMESYNC_INTRTR0_IN_29	TIMESYNC_INTRTR0	IEP0 sync event 1	Pulse
	YNC1_OUT_0				
	PRU_ICSSG1_PR1_EDC1_S	TIMESYNC_INTRTR0_IN_30	TIMESYNC_INTRTR0	IEP1 sync event 0	Pulse
	YNC0_OUT_0				
	PRU_ICSSG1_PR1_EDC1_S	TIMESYNC_INTRTR0_IN_31	TIMESYNC_INTRTR0	IEP1 sync event 1	Pulse
	YNC1_OUT_0				
	PINFUNCTION_PRG1_IEP0_	TIMESYNC_INTRTR0_IN_52	TIMESYNC_INTRTR0	EDC0 Latch 0 input event (I/O pin)	Pulse
	EDC_LATCH_IN0IN_PRG1_I				
	EP0_EDC_LATCH_IN0_0				
	PINFUNCTION_PRG1_IEP0_	TIMESYNC_INTRTR0_IN_53	TIMESYNC_INTRTR0	EDC0 Latch 1 input event (I/O pin)	Pulse
	EDC_LATCH_IN1IN_PRG1_I				
	EP0_EDC_LATCH_IN1_0				
	PINFUNCTION_PRG1_IEP1_	TIMESYNC_INTRTR0_IN_54	TIMESYNC_INTRTR0	EDC1 Latch 0 input event (I/O pin)	Pulse
	EDC_LATCH_IN0IN_PRG1_I				
	EP1_EDC_LATCH_IN0_0				
	PINFUNCTION_PRG1_IEP1_	TIMESYNC_INTRTR0_IN_55	TIMESYNC_INTRTR0	EDC1 Latch 1 input event (I/O pin)	Pulse
	EDC_LATCH_IN1IN_PRG1_I				
	EP1_EDC_LATCH_IN1_0				

Note

For more information about interrupts, see [Section 8, Local Interrupt Controller](#).

For more information on the interconnects, see [#unique_19referenceTitle, System Interconnect](#).

For more information on the power, reset and clock management, see the corresponding sections within [#unique_20referenceTitle, Device Configuration](#).

For more information on the device interrupt controllers, see [#unique_21referenceTitle, Interrupt Controllers](#).

For more information on the time sync and compare events routers, see [#unique_22referenceTitle, Time Sync and Compare Events](#).

5 PRU_ICSSG Top Level Resources Functional Description

This section provides functional description of the device integrated PRU Subsystems modules.

The PRUn/RTU_PRUn (where n = 0 or 1) cores within each PRU_ICSSG have access to all resources on the SoC through the VBUSM Interface Controller port, and the external host processors can access the PRU_ICSSG resources through the VBUSP Interface Target port. The use of XFR2VBUS allows BroadSide 32Bytes of data transfer to/from SoC CBASS0 Interconnect at 256-bit bursts using the VBUSM Controller port. The 32-bit Internal CBASS Interconnect bus will be the primary interconnect between all components internal to the PRU_ICSSG. There are two equally symmetrical halves in each PRU_ICSSG known as SLICE0 and SLICE1. Each slice will share several resources while capable of working independently of each other. There are two sets of XFR2VBUS for each Slice. The XFR2VBUS hardware accelerator is shared between PRU0 and RTU_PRU0 for SLICE0 and the same configuration is valid for SLICE1. The TX_PRU0 and TX_PRU1 cores have also attached XFR2VBUS hardware accelerators. PRUs also has the ability to submit 32-bit bursts transitions, but this will require RAT configuration.

Each of the Slices contains one RAT (Region based Address Translation) module. For example, the RAT module in SLICE0 is shared between RTU_PRU0, PRU0 and TX_PRU0 cores and the same configuration is valid for SLICE1. The RAT module is used to translate 32-bit address of the PRU core to 48-bit physical address.

The PRU cores within the subsystems also have access to all resources on the SoC through the External CBASS0 Interconnect. A subsystem local Interrupt Controller — INTC handles system input events and posts events back to the device-level host CPUs.

Each slice has intergrated one Transmit PRUn core (TX_PRUn, where n = 0 or 1). This RISC cores are used to control the TX L2 FIFO if enabled.

[Figure 5-1](#) shows an overview of the PRU_ICSSG Functional Block Diagram.

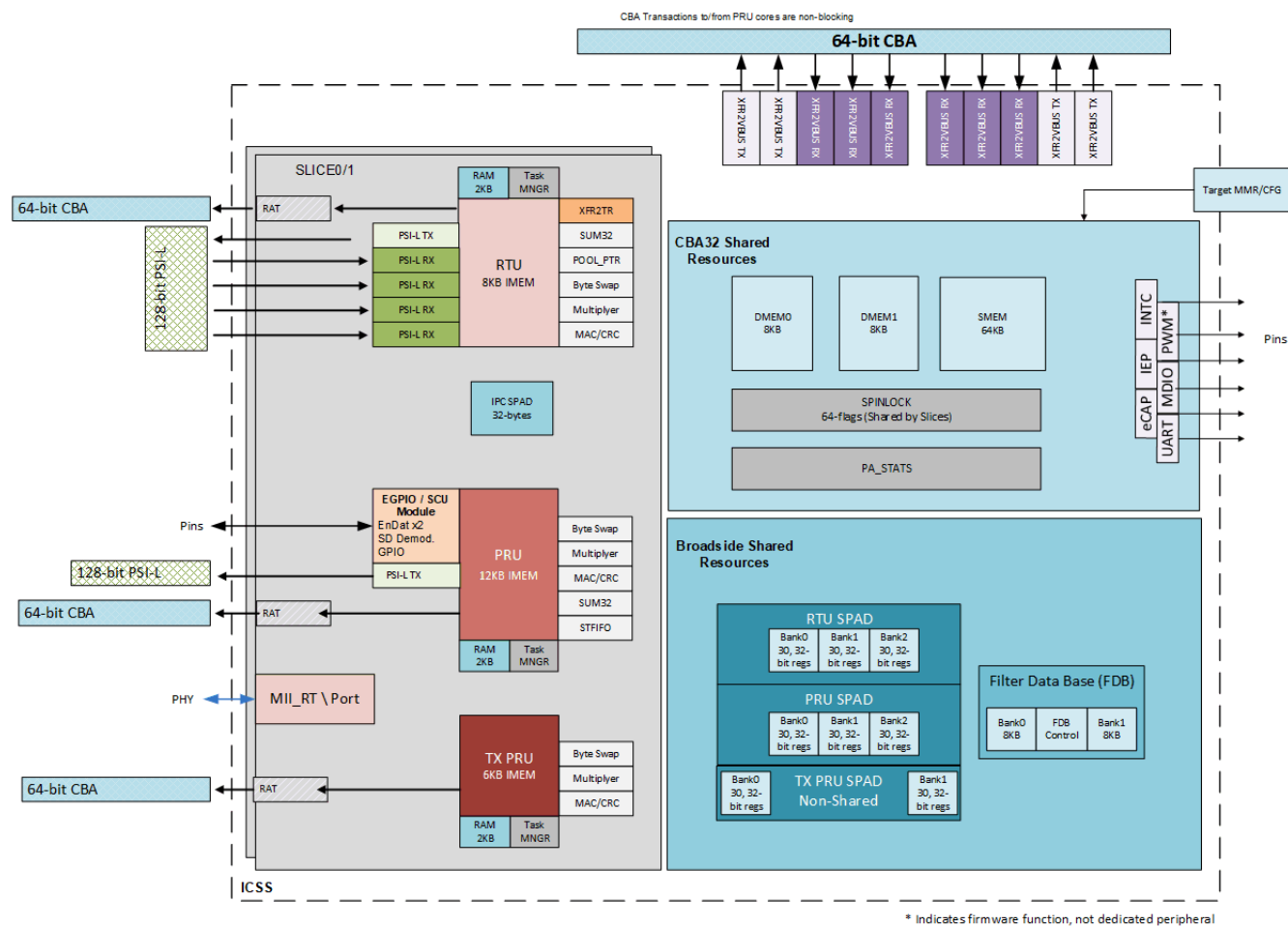


Figure 5-1. PRU_ICSSG Functional Block Diagram

Table 5-1 summarizes the mapping between hardware modules and PRU0/1, RTU_PRU0/1 or TX_PRU0/1 cores.

Table 5-1. Hardware Module Broadside ID Mapping

Hardware Module	Broadside ID	
MPY/MAC	00	6 copies: TX_PRU1/0 + RTU_PRU1/0 + PRU1/0
CRC16/32	01	6 copies: TX_PRU1/0 + RTU_PRU1/0 + PRU1/0 Note: TX_PRU1/0 do not have CRC FIFO
STITCH_FIFO64	08	2 copies: PRU1/0
QUEUE_PTR	09	2 copies: RTU_PRU1/0
SUM32	RTU_PRU MAP: 38 for SUM32 + RAM 39 for SUM32 ONLY PRU MAP: 49 for SUM32 + RAM 47 for SUM32 ONLY 02 for results	4 copies: 1 for each RTU_PRU1/0 1 for each PRU1/0
SPAD Bank0	10	1 copy: shared between PRU1/0 1 copy: shared between RTU_PRU1/0 2 copies: 1 for each TX_PRU1/0
SPAD Bank1	11	1 copy: shared between PRU1/0 1 copy: shared between RTU_PRU1/0

Table 5-1. Hardware Module Broadside ID Mapping (continued)

Hardware Module	Broadside ID	
SPAD Bank2	12	1 copy: shared between PRU1/0 1 copy: shared between RTU_PRU1/0
IPC SPAD	15	2 copies: 1 per slice
RX L2	20/21	2 copies: PRU1/0
RX Classifier	22	2 copies: 1 per slice (RTU_PRU0/PRU0 + RTU_PRU1/PRU1)
RX first 24 Bytes and 16 Bytes of TSN/pre	35	2 copies: RTU_PRU1/0
RX last 12 Bytes	15 RTU_PRU1/0 15 PRU1/0	4 copies: RTU_PRU1/0 PRU1/0 Mapped to upper PRU_RTU_SPAD IPC
FDB 16KB: 2 Banks of 8KB	30-35	1 copy: shared between PRU1/0 and RTU_PRU1/0
FDB results	32/33/34	1 copy: shared between RTU_PRU1/0 and PRU1/0
BS RAM	BS RAM only mode: 30 BS RAM + SUM32 snoop mode: 38	2 copies: RTU_PRU1/0
BS RAM	BS RAM only mode: 48 BS RAM + SUM32 snoop mode: 49	2 copies: PRU1/0 2 copies: TX_PRU1/0
TX L2	40	2 copies: PRU1/0 OR attached/own to TX_PRU1/0 (if register set to enable)
XFR2PSI	0x50/0x51/0x52/0x53	4 copies: RTU_PRU1/0 + PRU1/0
XFR2PSI Share	0x58 RTU_PRU1/0 Only 0x59 RTU_PRU1/0 Only	2 copies of special XFR2PSI which is attached to PRU1/0 The RTU_PRU1/0 can access it using 0x58/0x59 if MII_G_RT_ICSS_G_CFG[9] RTU_PRU_PSI_SHARE_EN bit is set
XFR2VBUSP	0x60 for RD_ID0 0x61 for RD_ID1 0x62 for WD_ID0 0x63 for WD_ID1 0x64 for TX_PRU1/0 RD	2 copies shared of RX per SLICE 2 copies shared of TX per SLICE 1 copy dedicated RX for TX_PRU only per SLICE
XFR2SHORT_DMA	0x70/71/72	2 copies: RTU_PRU1/0
XFR2SPIN	0x90	1 copy per PRU_ICSSG system
BSWAP	0xA0 for Byte Order Swap 0xA1 for 4_8 mode 0xA2 for 4_16 mode	6 copies: TX_PRU1/0 + RTU_PRU1/0 + PRU1/0
QUEUE_EMPTY	0xF0	Share XIN only all 6 PRU cores

5.1 PRU_ICSSG Reset Management

The device supports warm reset isolation (Hard/Soft Reset, Watchdog Reset) on PRU_ICSSG0 and PRU_ICSSG1.

For more details on the PRU_ICSSG Resets Isolation, see also the *ICSS Reset Isolation*.

5.2 PRU_ICSSG Power and Clock Management

The PRU_ICSSG supports two levels of clock gating. First level gates all clocks inside the PRU_ICSSG when requested by the PSC (Power Sleep Controller). The second level allows user software to enable/disable clocks in the clock gating register [ICSSG_CGR_REG](#) to some internal modules, as follows:

- IEP
- ECAP0
- UART0
- INTC

The appropriate configuration registers block controls its local module set inside PRU_ICSSG.

Note

PRU_ICSSG supports different clock speeds for CORE_CLK and IEP_CLK. Please refer to [Section 4, PRU_ICSSG Integration](#), for details.

5.2.1 PRU_ICSSG CORE Clock Generation

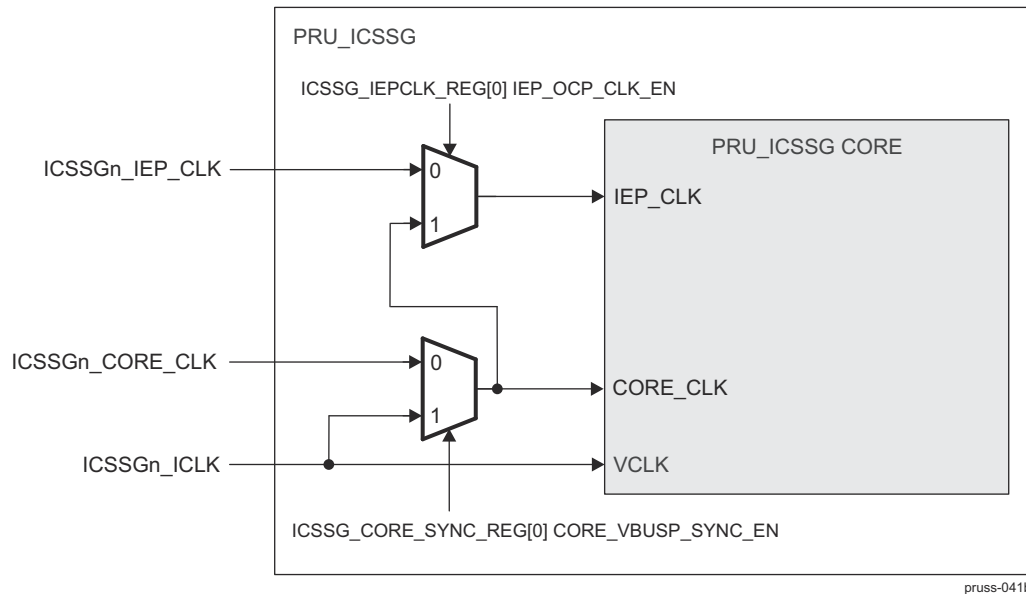


Figure 5-2. PRU_ICSSG CORE Clock Diagram

The CORE block uses two multiplexers to allow software to select one of three source clocks (ICSSGn_CORE_CLK, ICSSGn_ICLK or ICSSGn_IEP_CLK) for the final clock source of the CORE block. The user needs to configure [ICSSG_CORE_SYNC_REG\[0\] CORE_VBUSP_SYNC_EN](#) bit and [ICSSG_IEPCLK_REG\[0\] IEP_OCP_CLK_EN](#) bit to 1 if CORE_CLK and IEP_CLK respectively needs to be synchronous to ICLK (250 MHz).

5.2.2 PRU_ICSSG Idle State

The below lists the clock management settings applicable at PRU_ICSSG subsystem level (first level of local power management).

A transition from an ACTIVE/Normal state to an IDLE state is performed as per the sequence:

1. The host processor requests that the PRU firmware goes into IDLE state and waits for acknowledgement.
2. The host issues Clock Stop Request for each module in [ICSSG_CGR_REG](#) register with gateable clocks defined at second power management level (see [Section 5.2](#))
3. The PRU_ICSSG acknowledges IDLE Request and send Clock Stop Acknowledge to the host processor.
4. The PSC can de-assert PWR_CLK_EN
5. The main clocks can get turned off

A transition from an IDLE state to an ACTIVE/ Normal state is performed as per the sequence:

1. Turn on the main external clocks
2. The PSC can assert PWR_CLK_EN
3. The host will need to de-assert Clock Stop Request for each module, defined in [ICSSG_CGR_REG](#) register,

4. The PRU_ICSSG firmware need to de-assert Clock Stop Acknowledge for each module defined in [ICSSG_CGR_REG](#) register and then wait for the Clock Stop Acknowledge de-assert
5. The PRU_ICSSG firmware will de-assert Clock Stop Acknowledge

5.2.3 PRU_ICSSG Protect

Write protect block allows software to enable safety protection to prevent corruption of key configuration and debug registers and the Instruction memories (IRAM's) of all six PRU cores (PRU0/PRU1, RTU_PRU0/RTU_PRU1 and TX_PRU0/TX_PRU1). Write protection is also supported for Data RAM0 and Data RAM1.

This is achieved by blocking the byte enables during a write transaction if enabled. When enabled, it will prevent any unwanted write transaction to these elements. To Enable/Disable this feature, software will first need to unlock the write access to this block through the [PROT_UNLOCK_KEY](#) register then configure the protection through [PROT_CFG](#) register and relock.

5.2.4 Module Clock Configurations at PRU_ICSSG Top Level

IEP functional clock source selection: The clock source selection to the IEP module is done in register CTRLMMR_ICSSGn_CLKSEL[19-16] IEP_CLKSEL (where n = 0 or 1) in the CTRL_MMRO location. For more information on these PRU_ICSSG level input clocks, refer to the [Section 4](#).

Enhanced GPIO clock divider settings: In certain sample/shift clock settings of the PRU0 and PRU1 EGPIOs (when enabled in serial mode) two cascaded fractional dividers are done in the PR1_ICSSG_CFG top level configuration registers [ICSSG_GPCFG0_REG](#) and [ICSSG_GPCFG1_REG](#). In addition, EGPIo clock active edge selection control can be exerted via the bit PRU0_GPI_CLK_MODE for PRU0 EGPIo and PRU1_GPI_CLK_MODE for the PRU1 EGPIo.

- For the serial PRU0's EGPOs:
 - [ICSSG_GPCFG0_REG](#)[24-20] PRU0_GPO_DIV1
 - [ICSSG_GPCFG0_REG](#)[19-15] PRU0_GPO_DIV0
- For the serial PRU0's EGPIs:
 - [ICSSG_GPCFG0_REG](#)[12-8] PRU0_GPI_DIV1
 - [ICSSG_GPCFG0_REG](#)[7-3] PRU0_GPI_DIV0
- For the serial PRU1's EGPOs:
 - [ICSSG_GPCFG1_REG](#)[24-20] PRU1_GPO_DIV1
 - [ICSSG_GPCFG1_REG](#)[19-15] PRU1_GPO_DIV0
- For the serial PRU1's EGPIs:
 - [ICSSG_GPCFG1_REG](#)[12-8] PRU1_GPI_DIV1
 - [ICSSG_GPCFG1_REG](#)[7-3] PRU1_GPI_DIV0

5.3 Other PRU_ICSSG Module Functional Registers at Subsystem Level

Enhanced GPIO. The other functional mode setting for PRUs EGPIOs at PRU_ICSSG top registers level are:

- [ICSSG_GPCFG0_REG](#) / [ICSSG_GPCFG1_REG](#)[14] PRU0_GPO_MODE (PRU0 or PRU1) — to select between direct or serial EGPO output mode of operation.
- [ICSSG_GPCFG0_REG](#) / [ICSSG_GPCFG1_REG](#)[25] PRU0_GPO_SH_SEL (PRU0 or PRU1) — to select between the EGPO shadow registers 0 and 1 used for output shifting. For more details, refer to the [Section 6.2.2.3.4, Enhanced General-Purpose Module Outputs \(R30\)](#).
- [ICSSG_GPCFG0_REG](#) / [ICSSG_GPCFG1_REG](#)[1-0] PRU0_GPI_MODE (PRU0 or PRU1) — selects the EGPI input mode of operation (selects between "direct input", "parallel capture", "28-bit shift" or "MII_RT" modes).
- [ICSSG_GPCFG0_REG](#) / [ICSSG_GPCFG1_REG](#)[13] PRU0_GPI_SB (PRU0 or PRU1) — start bit event status for 28-bit EGPI input shift mode. For more details, refer to the [Section 6.2.2.3, Enhanced General-Purpose Module Inputs \(R31\)](#).

PRUs scratchpad (SPAD) memory priority and configuration related bits are located in the [ICSSG_SPP_REG](#) register.

5.4 PRU_ICSSG Memory Maps

The PRU_ICSSG comprises various distinct addressable regions that are mapped to both a local and global memory map. The local memory maps are maps with respect to the PRU point of view. The global memory maps are maps with respect to the Host point of view, but can also be accessed by the PRU_ICSSG. Each PRU_ICSSG can also access the memories within the other PRU_ICSSG subsystem without going through an external port, thanks to PRU_ICSSG VBUSP expansion port.

5.4.1 PRU_ICSSG Local Memory Map

The PRU_ICSSG memory map is documented in [Table 5-2](#) (Instruction Space) and in [Table 5-3](#) (Data Space). Note that these two memory maps are implemented inside the PRU_ICSSG and are local to the components of the PRU_ICSSG.

5.4.1.1 PRU_ICSSG Local Instruction Memory Map

Each PRU (PRU0 and PRU1) has a dedicated 12KB of Instruction Memory (12KB for PRU_ICSSG0 and 12KB for PRU_ICSSG1) which needs to be initialized by an external to PRU_ICSSG Host processor before a PRU core executes any instructions.

Each RTU_PRU (Auxiliary PRU Cores: RTU_PRU0 and RTU_PRU1) has also a dedicated 8KB of Instruction Memory (8KB for PRU_ICSSG0 and 8KB for PRU_ICSSG1).

Each TX_PRU (Transmit PRU Cores: TX_PRU0 and TX_PRU1) has also a dedicated 6KB of Instruction Memory (6KB for PRU_ICSSG0 and 6KB for PRU_ICSSG1).

CAUTION

The PRU_ICSSG0 PRU0/1_IRAM regions are ONLY accessible from controllers, external to the PRU_ICSSG (like Arm) when the PRU0/PRU1 is NOT running. The access is via PRU_ICSSG target port on the device CBASS0 interconnect.

Table 5-2. PRU_ICSSG Local Instruction Memory Map

Start Address	PRU0/RTU_PRU0 TX_PRU0	PRU1/RTU_PRU1/TX_PRU1
0000 0000h	12 KB IRAM/8 KB IRAM/6 KB IRAM	12 KB IRAM/8 KB IRAM/6 KB IRAM

5.4.1.2 PRU_ICSSG Local Data Memory Map

The local data memory map in [Table 5-3](#) allows each PRU core to access the PRU_ICSSG addressable regions (both its own subsystem and the other subsystem) and the external host's memory map.

Table 5-3. PRU_ICSSG Local Data Memory Map

Start Address	PRU0/ RTU_PRU0/ TX_PRU0	PRU1/ RTU_PRU1/ TX_PRU1
0000 0000h	PRU_ICSSG1 Data 8 KB RAM0	PRU_ICSSG1 Data 8 KB RAM1
0000 2000h	PRU_ICSSG1 Data 8 KB RAM1 ⁽¹⁾	PRU_ICSSG1 Data 8 KB RAM0 ⁽¹⁾
0000 4000h	Reserved	Reserved
0000 6000h	Reserved	Reserved
0000 8000h	RAT_SLICE0	RAT_SLICE0
0000 9000h	RAT_SLICE1	RAT_SLICE1
0001 0000h	Data 64 KB RAM2 (Shared RAM)	Data 64 KB RAM2 (Shared RAM)
0002 0000h	PRU_ICSSG1 INTC	PRU_ICSSG1 INTC
0002 2000h	PRU0 Control	PRU0 Control
0002 3000h	RTU_PRU0 Control	RTU_PRU0 Control
0002 3400h	Reserved	Reserved
0002 3800h	RTU_PRU1 Control	RTU_PRU1 Control
0002 3C00h	Reserved	Reserved
0002 4000h	PRU1 Control	PRU1 Control
0002 4400h	Reserved	Reserved

Table 5-3. PRU_ICSSG Local Data Memory Map (continued)

Start Address	PRU0/ RTU_PRU0/ TX_PRU0	PRU1/ RTU_PRU1/ TX_PRU1
0002 4800h	Reserved	Reserved
0002 4C00h	PROTECT	PROTECT
0002 5000h	TX_PRU0 Control	TX_PRU0 Control
0002 5800h	TX_PRU1 Control	TX_PRU1 Control
0002 6000h	PRU_ICSSG1 CFG	PRU_ICSSG1 CFG
0002 7000h	PA_STATS_QRAM	PA_STATS_QRAM
0002 8000h	PRU_ICSSG1 UART0	PRU_ICSSG1 UART0
0002 A000h	TM_CFG_PRU0 (Task Manager)	TM_CFG_PRU0 (Task Manager)
0002 A100h	TM_CFG_RTU0 (Task Manager)	TM_CFG_RTU0 (Task Manager)
0002 A200h	TM_CFG_PRU1 (Task Manager)	TM_CFG_PRU1 (Task Manager)
0002 A300h	TM_CFG_RTU1 (Task Manager)	TM_CFG_RTU1 (Task Manager)
0002 A400h	TM_CFG_TX_PRU0 (Task Manager)	TM_CFG_TX_PRU0 (Task Manager)
0002 A500h	TM_CFG_TX_PRU1 (Task Manager)	TM_CFG_TX_PRU1 (Task Manager)
0002 C000h	PA_STATS_CRAM	PA_STATS_CRAM
0002 E000h	IEP0	IEP0
0002 F000h	IEP1	IEP1
0003 0000h	ECAP0	ECAP0
0003 2000h	MII_RT_CFG	MII_RT_CFG
0003 2100h	SGMII0_CFG	SGMII0_CFG
0003 2200h	SGMII1_CFG	SGMII1_CFG
0003 2400h	MII_MDIO	MII_MDIO
0003 3000h	ICSS_G_CFG	ICSS_G_CFG
0003 4000h	Reserved	Reserved
0003 7000h	Reserved	Reserved
0003 8000h	Reserved	Reserved
0003 B000h	Reserved	Reserved
0003 C000h	PA_STATS_CFG	PA_STATS_CFG
0004 0000h	Reserved	Reserved
0008 0000h	Reserved	Reserved

(1) Direct access from PRU0 to Data RAM 1 and PRU1 to Data RAM 0.

5.4.2 PRU_ICSSG Global Memory Map

The global view of the PRU_ICSSG internal memories and control ports is shown in [Table 5-4](#). The offset addresses of each region are implemented inside the PRU_ICSSG but the global device memory mapping places the PRU_ICSSG target port in the address range shown in the external PRU_ICSSG Host top-level memory map.

The global memory map is with respect to the Host point of view (that is, device Arm), but it can also be accessed by the PRU_ICSSG itself. Note that PRU0 and PRU1 can use either the local or global addresses to access their internal memories, but using the local addresses provides access time several cycles faster than using the global addresses. This is because when accessing via the global address the access has to be routed through the CBASS0 switch fabric outside PRU_ICSSG and back in through the PRU_ICSSG target port.

Each of the PRU cores can access the rest of the device memory (including memory mapped peripheral and configuration registers) using the global memory space addresses.

Table 5-4. PRU_ICSSG Global Memory Map

Offset Address	PRU_ICSSG Target
0000 0000h	Data 8 KB RAM0
0000 2000h	Data 8 KB RAM1

Table 5-4. PRU_ICSSG Global Memory Map (continued)

Offset Address	PRU_ICSSG Target
0000 4000h	RTU_PRU0 8 KB IRAM
0000 6000h	RTU_PRU1 8 KB IRAM
0000 8000h	RAT_SLICE0
0000 9000h	RAT_SLICE1
0000 A000h	TX_PRU0 6 KB IRAM
0000 C000h	TX_PRU1 6 KB IRAM
0001 0000h	Data 64 KB RAM2 (shared)
0002 0000h	PRU_ICSSG INTC
0002 2000h	PRU0 Control
0002 2400h	PRU0 Debug
0002 3000h	RTU_PRU0 Control
0002 3400h	RTU_PRU0 Debug
0002 3800h	RTU_PRU1 Control
0002 3C00h	RTU_PRU1 Debug
0002 4000h	PRU1 Control
0002 4400h	PRU1 Debug
0002 4C00h	PROTECT
0002 5000h	TX_PRU0 Control
0002 5400h	TX_PRU0 Debug
0002 5800h	TX_PRU1 Control
0002 5C00h	TX_PRU1 Debug
0002 6000h	PRU_ICSSG CFG
0002 7000h	PA_STATS_QRAM
0002 8000h	PRU_ICSSG UART0
0002 A000h	TM_CFG_PRU0 (Task Manager)
0002 A100h	TM_CFG_RTU0 (Task Manager)
0002 A200h	TM_CFG_PRU1 (Task Manager)
0002 A300h	TM_CFG_RTU1 (Task Manager)
0002 A400h	TM_CFG_TX_PRU0 (Task Manager)
0002 A500h	TM_CFG_TX_PRU1 (Task Manager)
0002 C000h	PA_STATS_CRAM
0002 E000h	IEP0
0002 F000h	IEP1
0003 0000h	ECAP0
0003 2000h	MII_RT_CFG
0003 2100h	SGMII0_CFG
0003 2200h	SGMII1_CFG
0003 2400h	MII_MDIO
0003 3000h	MII_G_RT_CFG
0003 4000h	PRU0 12 KB IRAM
0003 8000h	PRU1 12 KB IRAM
0003 C000h	PA_STATS_CFG
0004 0000h	Reserved

6 PRU_ICSSG PRU Cores

This section describes the functionality of the two Programmable Real-time Unit (PRU) processors (PRU0 and PRU1), RTU_PRU0/ RTU_PRU1 and TX_PRU0/ TX_PRU1 integrated in each of the device PRU_ICSSG.

6.1 PRU Cores Overview

The PRU is a processor optimized for performing embedded tasks that require manipulation of packed memory mapped data structures, handling of system events that have tight real-time constraints and interfacing with systems external to the SoC. The PRU is both very small and very efficient at handling such tasks.

The major attributes of the PRU are shown in [Table 6-1](#).

Table 6-1. PRU Features

Attribute	Value
IO Architecture	Load/Store
Data Flow Architecture	Register to Register
<i>Core Level Bus Architecture</i>	
Type	4-Bus Harvard (1 Instruction, 3 Data)
Instruction I/F	32-Bit Modified VBUSP Controller
Memory I/F 0	32-Bit VBUSP Controller
Memory I/F 1	32-Bit VBUSP Controller
<i>Execution Model</i>	
Issue Type	Scalar
Pipelining	None (Purposefully)
Ordering	In Order
ALU Type	Unsigned Integer
<i>Registers</i>	
General Purpose (GP)	30 (R1 – R30)
External Status	0 (R31)
GP/Indexing	0 (R0)
Addressability in Instruction	Bit, Byte (8-bit), Half-word (16-bit), Word (32-bit), Pointer
<i>Addressing Modes</i>	
Load Immediate	16-bit Immediate
Load/Store – Memory	Register Base + Register Offset
	Register Base + 8-bit Immediate Offset
	Register Base with auto increment/decrement
	Constant Table Base + Register Offset
	Constant Table Base + 8-bit Immediate Offset
	Constant Table Base with auto increment/decrement
Data Path Width	32-bit
Instruction Width	32-bit
Accessibility to Internal PRU Structures	Provides 32-bit VBUSP target with three regions: • Instruction RAM • Control/Status registers • Debug access to internal registers (R0-R31) and constant table

The processor is based on a four-bus architecture which allows instructions to be fetched and executed concurrently with data transfers. In addition, an input is provided in order to allow external status information to be reflected in the internal processor status register. [Figure 6-1](#) shows a block diagram of the processing element and the associated instruction RAM/ROM that contains the code that is to be executed.

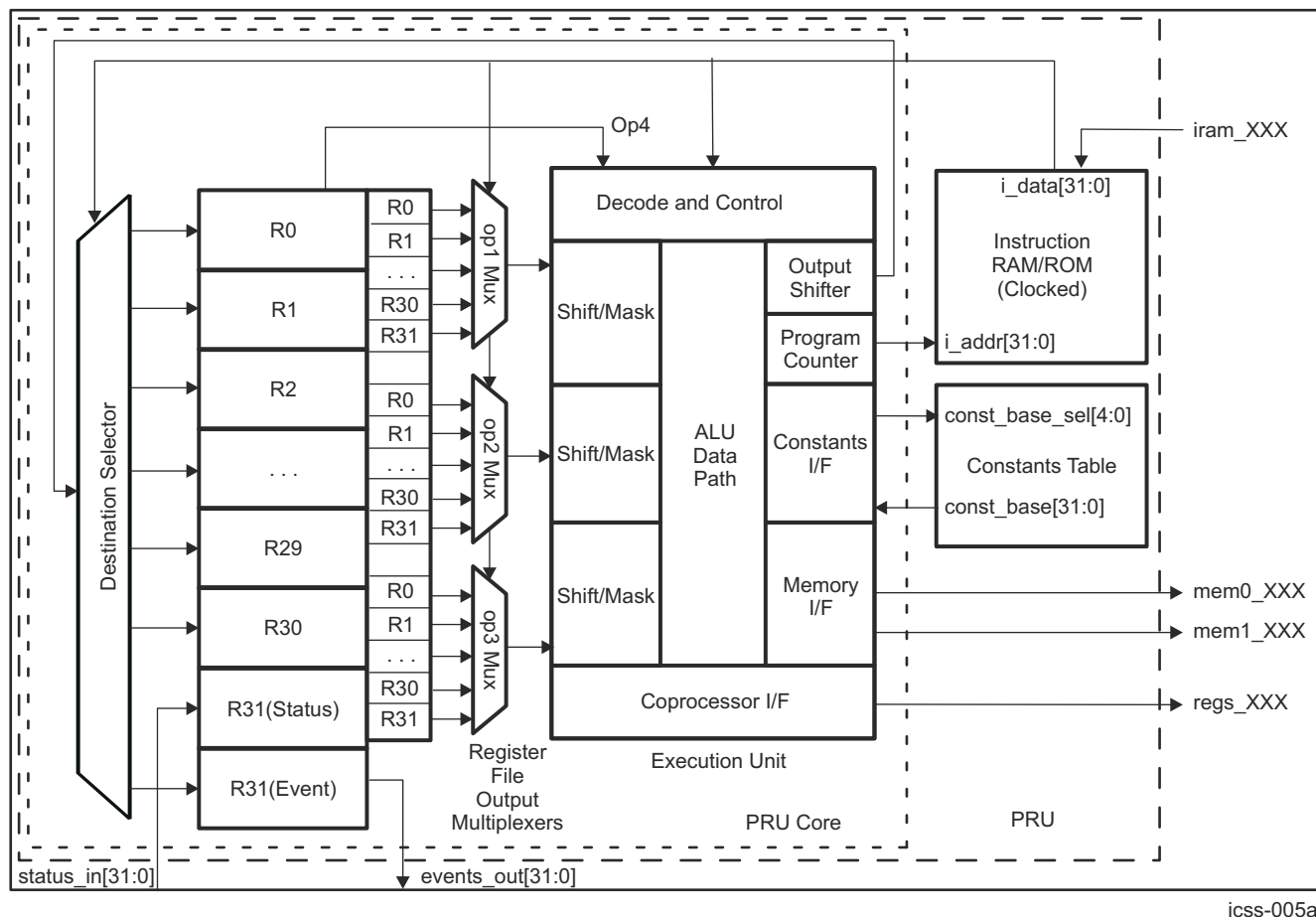


Figure 6-1. PRU Block Diagram

6.2 PRU Cores Functional Description

This section describes the PRU cores supported functionality by describing the constant table, module interface and enhanced GPIOs.

6.2.1 PRUs Constant Table

The PRU Constants Table is a structure of hard-coded memory addresses for commonly used peripherals and memories. The constants table is used for more efficiently load/store data to these commonly accessed addresses by:

- Eliminating the PRU instruction that pre-loads a hard-coded address into the internal register file.
- Maximizing the usage of the PRU register file for embedded processing applications by moving many of the commonly used constant or deterministically calculated base addresses from the internal register file to an external table.

Table 6-2. PRU0/1 Constant Table

Entry No.	Region Pointed To	Value [31:0]
0	PRU_ICSSG INTC (local)	0002_0000h
1	PRU_ICSSG IEP1 (local)	0002_F000h
2	PRU_ICSSG IEP1_0x100 (local)	0002_F100h
3	PRU_ICSSG ECAP0 (local)	0003_0000h
4	PRU_ICSSG CFG (local)	0002_6000h
5	PRU_ICSSG CFG_0x100 (local)	0002_6100h
6	PRU_ICSSG INTC_0x200 (local)	0002_0200h
7	PRU_ICSSG UART0 (local)	0002_8000h
8	PRU_ICSSG IEP0_0x100 (local)	0002_E100h

Table 6-2. PRU0/1 Constant Table (continued)

Entry No.	Region Pointed To	Value [31:0]
9	PRU_ICSSG0 CFG (local)	0003_3000h
10	TM_CFG_PRU0 (Local Task Manager)	0002_A000h PRU0
	TM_CFG_RTU0 (Local Task Manager)	0002_A100h RTU_PRU0
	TM_CFG_PRU1 (Local Task Manager)	0002_A200h PRU1
	TM_CFG_RTU1 (Local Task Manager)	0002_A300h RTU_PRU1
11	PRU_ICSSG PRU0 Control (local)	0002_2000h PRU0
	PRU_ICSSG RTU_PRU0 Control (local)	0002_3000h RTU_PRU0
	PRU_ICSSG RTU_PRU1 Control (local)	0002_3800h RTU_PRU1
	PRU_ICSSG PRU1 Control (local)	0002_4000h PRU1
12	PRU_ICSSG PA_STATS_QRAM (local)	0002 7000h
13	PRU_ICSSG PA_STATS_CRAM (local)	0002 C000h
14	Reserved	0002 4800h
15	Reserved	6000_0000h
16	Reserved	7000_0000h
17	Reserved	8000_0000h
18	Reserved	9000_0000h
19	Reserved	A000_0000h
20	Reserved	B000_0000h
21	MDIO (local)	0003_2400h
22	RAT SLICE0 (local)	0000_8000h PRU0/RTU_PRU0
	RAT SLICE1 (local)	0000_9000h PRU1/RTU_PRU1
23	Reserved	C000_0000h
24	PRU_ICSSG PRU0/PRU1 Data RAM (local)	0000_0n00h, n = c24_blk_index[3:0]
25	PRU_ICSSG PRU1/PRU0 Data RAM (local)	0000_2n00h, n = c25_blk_index[3:0]
26	PRU_ICSSG IEP (local)	0002_En00h, n = c26_blk_index[3:0]
27	PRU_ICSSG MII_RT/SGMII0_CFG/SGMII1_CFG (local)	0003_2n00h, n = c27_blk_index[3:0]
28	PRU_ICSSG Shared RAM (local)	00nn_nn00h, nnnn = c28_pointer[15:0]
29	Reserved	0Dnn_nn00h, nnnn = c29_pointer[15:0]
30	Reserved	0Enn_nn00h, nnnn = c30_pointer[15:0]
31	Reserved	0Fnn_nn00h, nnnn = c31_pointer[15:0]

Note

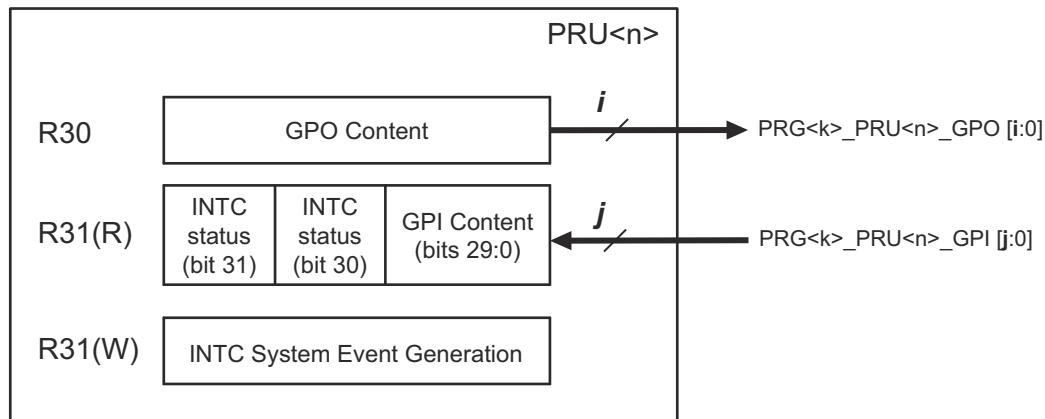
The addresses in constants entries 24–31 are partially programmable. Their programmable bit field (for example, c24_blk_index[3:0]) is programmable through the PRU CTRL register space. As a general rule, the PRU should configure this field before using the partially programmable constant entries.

6.2.2 PRU Module Interface

The PRU module interface consists of the PRU internal registers 30 and 31 (R30 and R31). [Figure 6-2](#) shows the PRU module interface and the functionality of R30 and R31. The register R31 serves as an interface with the dedicated PRU general purpose input (GPI) pins and PRU_ICSSG INTC. Reading R31 returns status information from the GPI pins and PRU_ICSSG INTC via the PRU Real Time Status Interface. Writing to R31 generates PRU system events via the PRU Event Interface. The register R30 serves as an interface with the dedicated PRU general purpose output (GPO) pins.

Note

The below sections cover different functional modes of the PRU_n cores, (where n=0,1), enhanced GPIO (EGPIO) interface. The register bits which control EGPIO functionalities are part of the (PRU_ICSSG CFG) space. For descriptions of these EGPIO register bitfield controls, refer to the [Section 5.3](#).



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Figure 6-2. PRU Module Interface

6.2.2.1 Real-Time Status Interface Mapping (R31): Interrupt Events Input

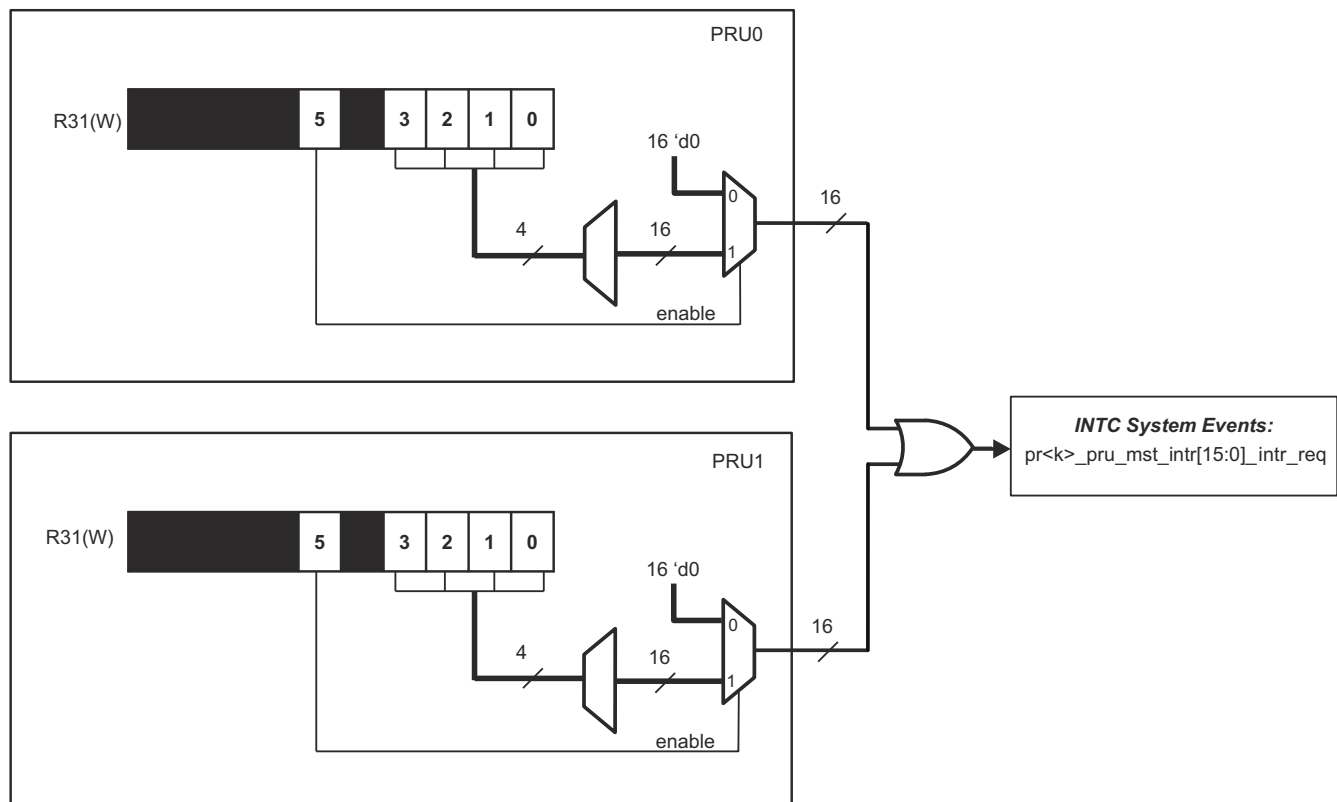
The PRU Real Time Status Interface directly feeds information into register 31 (R31) of the PRU's internal register file. The firmware on the PRU uses the status information to make decisions during execution. The status interface is comprised of signals from different modules inside of the PRU_ICSSG which require some level of interaction with the PRU. More details on the Host interrupts imported into bit 30 and 31 of register R31 of both the PRUs is provided in the [Section 8, PRU_ICSSG Local Interrupt Controller](#).

Table 6-3. Real-Time Status Interface Mapping (R31) Field Descriptions

Bit	Field	Description
31	pru_intr_in[1]	PRU Host Interrupt 1 from local PRU_ICSSG INTC
30	pru_intr_in[0]	PRU Host Interrupt 0 from local PRU_ICSSG INTC
29-0	pru<n>_r31_status[29:0]	Status inputs from primary input via Enhanced GPI port

6.2.2.2 Event Interface Mapping (R31): PRU System Events

This PRU Event Interface directly feeds pulsed event information out of the PRU's internal ALU. These events are exported out of the PRU_ICSSG and need to be connected to the system interrupt controller at the SoC level. The event interface can be used by the firmware to create software interrupts from the PRU to the Host processor.



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Figure 6-3. Event Interface Mapping (R31)

Table 6-4. Event Interface Mapping (R31) Field Descriptions

Bit	Field	Description
31-6	Reserved	
5	pru<n>_r31_vec_valid	Valid strobe for vector output
4	Reserved	
3-0	pru<n>_r31_vec[3:0]	Vector output

Simultaneously writing a '1' to pru<n>_r31_vec_valid (R31 bit 5) and a channel number from 0 to 15 to pru<n>_r31_vec[3:0] (R31 bits 3-0) creates a pulse on the output of the corresponding pr<k>_pru_mst_intr[x]_intr_req INTC system event. For example, writing '100000' will generate a pulse on prk_pru_mst_intr[0]_intr_req, writing '100001' will generate a pulse on prk_pru_mst_intr[1]_intr_req, and so on to where writing '101111' will generate a pulse on prk_pru_mst_intr[15]_intr_req and writing '0xxxxx' will not generate any system event pulses. The output values from both PRU cores in a subsystem are ORed together.

The output channels 0-15 are connected to the INTC system events 16-31, respectively. This allows the PRU to assert one of the system events 16-31 by writing to its own R31 register. The system event is used to either post a completion event to one of the host CPUs (Arm) or to signal the other PRU. The host to be signaled is determined by the system interrupt to interrupt channel mapping (programmable). The 16 events are named as prk_pru_mst_intr<15:0>_intr_req. See the [Section 8.3, PRU_ICSSG Interrupt Requests Mapping](#), in the section, *PRU_ICSSG Local Interrupt Controller*, for more details.

6.2.2.3 General-Purpose Inputs (R31): Enhanced PRU GP Module

The PRU_ICSSG implements an enhanced General Purpose Input/Output (GPIO) module with SCU that supports the following general-purpose input modes: direct input, 16-bit parallel capture, 28-bit serial shift in, and MII_RT. Register R31 serves as an interface with the general-purpose inputs. [Table 6-5](#) describes the input modes in detail.

Note

Each PRU core can only be configured for one GPI mode at a time. Each mode uses the same R31 signals and internal register bits for different purposes. A summary is found in [Table 6-6](#).

Note

The [ICSSG_GPCFG0_REG](#) register, bitfield [29:26] PR1_PRU0_GP_MUX_SEL (PRU0 or PRU1) in the PRU_ICSSG CFG register space needs to be set to 0h for GP mode. For a given PRU core, the following IO modes are mutually exclusive: GP mode, Sigma Delta mode, and 3 channel Peripheral I/F mode.

Table 6-5. PRU R31 (GPI) Modes

Mode	Function	Configuration
Direct input	GPI[19:0] feeds directly into the PRU R31	Default state
16-bit parallel capture	DATAIN[0:15] is captured by the posedge or negedge of CLOCKIN	- Enabled by ICSSG_GPCFG0_REG register (PRU0 or PRU1) - CLOCKIN edge selected by ICSSG_GPCFG0_REG register
28-bit shift in	DATAIN is sampled and shifted into a 28-bit shift register. - Shift Counter (Cnt_16) feature is mapped to pru<n>_r31_status[28]. - SB (Start Bit detection) feature is mapped to pru<n>_r31_status[29]	- Enabled and disabled by ICSSG_GPECFG0_REG register (PRU0 or PRU1) - Cnt_16 is self clearing and is connected to the PRU INTC - Start Bit (SB) is cleared by ICSSG_GPECFG0_REG register - Start Bit value (0h or 1h) selected by ICSSG_GPECFG0_REG register
MII_RT	mii_rt_r31_status [29:0] internally driven by the MII_RT module	Enabled by ICSSG_GPCFG0_REG [1-0] PRU0_GPI_MODE register (value: 3h), where n = 0 or 1

Table 6-6. PRU GPI Signals and Configurations

Pad Names at Device Level ⁽¹⁾	GPI Modes		
	Direct input	Parallel Capture	28-Bit Shift in
PRG<k>_PRU<n>_GPI0	GPI0	DATAIN0	DATAIN
PRG<k>_PRU<n>_GPI1	GPI1	DATAIN1	
PRG<k>_PRU<n>_GPI2	GPI2	DATAIN2	
PRG<k>_PRU<n>_GPI3	GPI3	DATAIN3	
PRG<k>_PRU<n>_GPI4	GPI4	DATAIN4	
PRG<k>_PRU<n>_GPI5	GPI5	DATAIN5	
PRG<k>_PRU<n>_GPI6	GPI6	DATAIN6	
PRG<k>_PRU<n>_GPI7	GPI7	DATAIN7	
PRG<k>_PRU<n>_GPI8	GPI8	DATAIN8	
PRG<k>_PRU<n>_GPI9	GPI9	DATAIN9	
PRG<k>_PRU<n>_GPI10	GPI10	DATAIN10	
PRG<k>_PRU<n>_GPI11	GPI11	DATAIN11	
PRG<k>_PRU<n>_GPI12	GPI12	DATAIN12	
PRG<k>_PRU<n>_GPI13	GPI13	DATAIN13	
PRG<k>_PRU<n>_GPI14	GPI14	DATAIN14	
PRG<k>_PRU<n>_GPI15	GPI15	DATAIN15	
PRG<k>_PRU<n>_GPI16	GPI16	CLOCKIN	
PRG<k>_PRU<n>_GPI17	GPI17		

Table 6-6. PRU GPI Signals and Configurations (continued)

Pad Names at Device Level ⁽¹⁾	GPI Modes		
	Direct input	Parallel Capture	28-Bit Shift in
PRG<k>_PRU<n>_GPI18	GPI18		
PRG<k>_PRU<n>_GPI19	GPI19		

(1) These pins are also used for Sigma Delta or Peripheral I/F mode.

6.2.2.3.1 PRU EGPIs Direct Input

The pru<n>_r31_status[0:19] bits of the internal PRU register file are mapped to device-level, general purpose input pins (PRU0_GPI[0:19]). In GPI Direct Input mode, PRU0_GPI[0:19] feeds directly to pru<n>_r31_status[0:19].

Each PRU of the PRU_ICSSG has a separate mapping to device input signals - PRGn_PRU0_GPI[19:0] for the PRU0 core and PRGn_PRU1_GPI[19:0] for the PRU1 core. There are 80 general purpose inputs in total. For more details, refer also to the [Section 3](#). See the device's system reference guide or datasheet for device specific pin mapping.

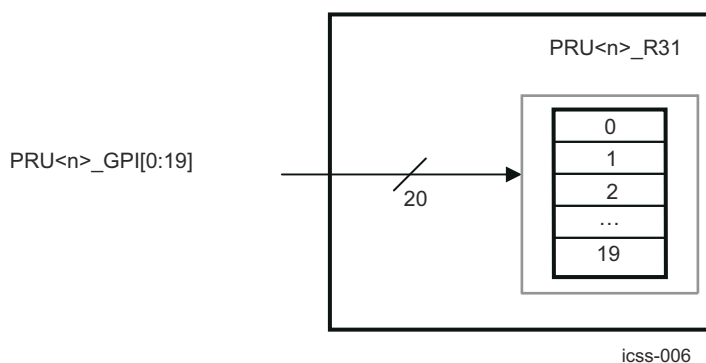


Figure 6-4. PRU R31 (EGPI) Direct Input Mode Block Diagram

6.2.2.3.2 PRU EGPIs 16-Bit Parallel Capture

The pru<n>_r31_status[0:15] and pru<n>_r31_status[16] bits of the internal PRU register file mapped to device-level, general purpose input pins (PRU0_DATAIN [0:15] and PRU0_CLOCKIN, respectively). PRU0_CLOCKIN is designated for an external strobe clock, and is used to capture PRU0_DATAIN [0:15].

The PRU<n>_DATAIN can be captured either by the positive or the negative edge of PRU<n>_CLOCK, programmable through the PRU_ICSSG CFG register space. If the clocking is configured through the PRU_ICSSG CFG register to be positive, then it will equal PRU<n>_CLOCK; however, if the clocking is configured to be negative, then it will equal PRU<n>_CLOCK inverted.

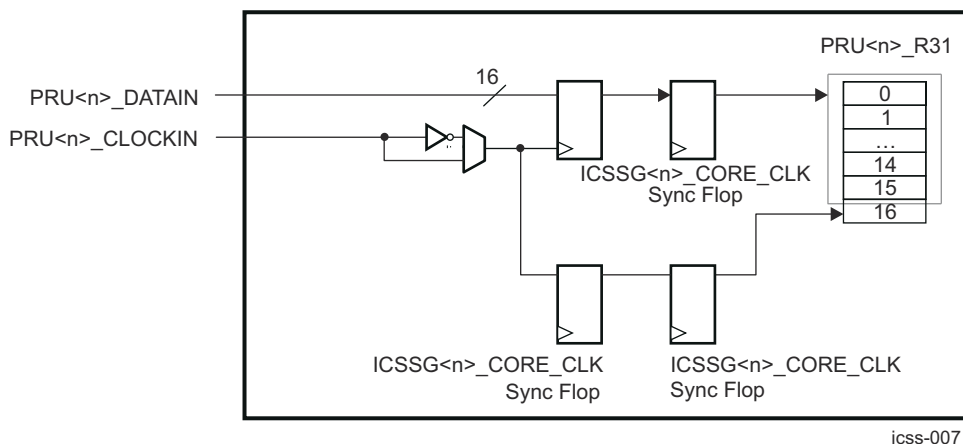


Figure 6-5. PRU R31 (EGPI) 16-Bit Parallel Capture Mode Block Diagram

6.2.2.3.3 PRU EGPIs 28-Bit Shift In

In 28-bit shift in mode, the device-level, general-purpose input pin PRU<n>_DATAIN is sampled and shifted into a 28-bit shift register on an internal clock pulse. The register fills in LSB order (from bit 0 to 27) and then overflows into a bit bucket. The 28-bit register is mapped to pru<n>_r31_status[0:27] and can be cleared in software through the [ICSSG_GPCFG0_REG\[13\]](#) PRU0_GPI_SB register (PRU0 or PRU1).

Note that by default, the PRU will continually capture and shift the DATAIN input when the GPI mode has been set. However, clearing the [ICSSG_GPECFG0_REG\[1\]](#) PRU0_GPI_SHIFT_EN bit will freeze the shift operation.

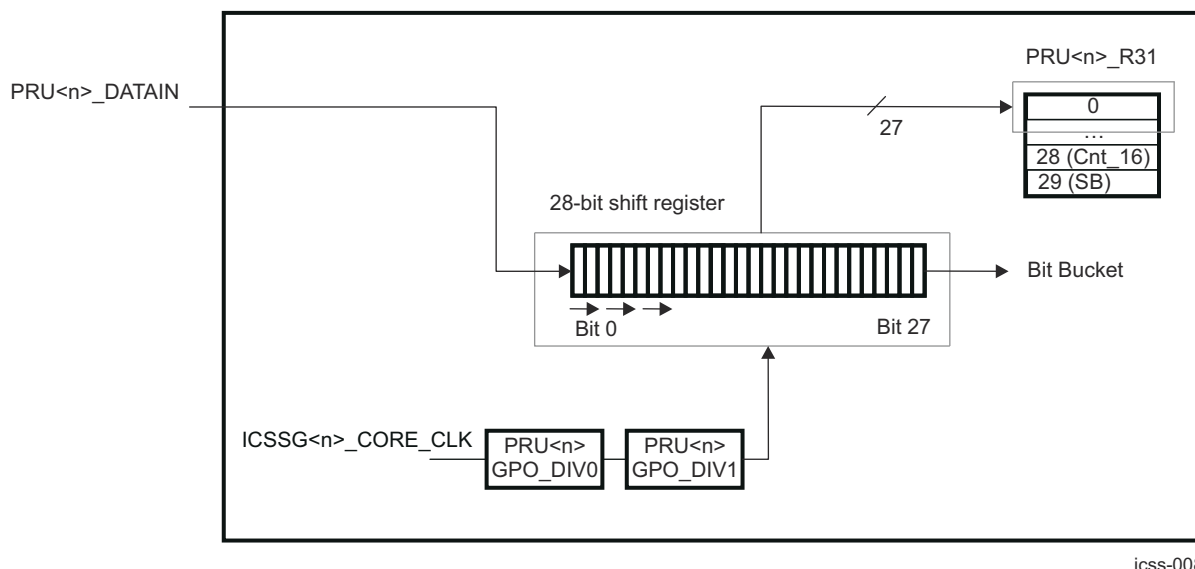
The shift rate is controlled by the effective divisor of two cascaded dividers applied to the ICSSG<n>_CORE_CLK clock (150MHz/ 200MHz/ 225MHz). These cascaded dividers can each be configured through the PRU_ICSSG CFG register space to a value of {1, 1.5, ..., 16}. [Table 6-7](#) shows sample effective clock values and the divisor values that can be used to generate these clocks.

Table 6-7. PRU EGPIs Effective Clock Values

Generated clock	PRU0_GPI_DIV0	PRU0_GPI_DIV1
8-MHz	12.5 (17h)	2 (02h)
10-MHz	10 (12h)	2 (02h)
16-MHz	16 (1Eh)	1 (00h)
20-MHz	10 (12h)	1 (00h)

The 28-bit shift mode also supports the following features:

- SB (Start Bit detection) is mapped to pru<n>_r31_status[29] and is set when the first 1 (default) or 0 is captured on PRU<n>_DATAIN. The Start Bit value (1 or 0) is configured through the [ICSSG_GPECFG0_REG\[0\]](#) PRU0_GPI_SB_P bit (PRU0 or PRU1). The SB flag in pru<n>_r31_status[29] is cleared in software through the PRU_ICSSG CFG register space.
- Cnt_16 (Shift Counter) is mapped to pru<n>_r31_status[28] and is set on every 16 shift clock samples after the Start Bit has been received. CNT_16 is self clearing and is connected to the local PRU_ICSSG INTC. See the [Section 8 PRU_ICSSG Local Interrupt Controller](#) for more details.
- The [ICSSG_GPECFG0_REG\[1\]](#) PRU0_GPI_SHIFT_EN bit can stop or freeze the current shift operation and disable the search for a new Start Bit, if an SB event has not occurred.



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Figure 6-6. PRU R31 (EGPI) 28-Bit Shift Mode

6.2.2.3.3.1 PRU EGPI Programming Model

Follow this steps to configure the PRU EGPI in 28-bit shift input mode:

1. Clear [ICSSG_GPECFG0_REG\[1\]](#) PRU0_GPI_SHIFT_EN bit (PRU0 or PRU1)
2. Clear/Set [ICSSG_GPECFG0_REG\[0\]](#) PRU0_GPI_SB_P bit (PRU0 or PRU1)

3. Clear Start Bit by writing 1h to [ICSSG_GPCFG0_REG](#)[13] PRU0_GPI_SB bit
4. Program the dividers through:
[ICSSG_GPCFG0_REG](#)[24-20] PRU0_GPO_DIV1 bit (PRU0 or PRU1)
[ICSSG_GPCFG0_REG](#)[19-15] PRU0_GPO_DIV0 bit (PRU0 or PRU1)
5. Enable Shift Input Mode by writing to [ICSSG_GPECFG0_REG](#)[1] PRU0_GPI_SHIFT_EN bit

6.2.2.3.4 General-Purpose Outputs (R30): Enhanced PRU GP Module

The PRU_ICSSG implements an enhanced General Purpose Input/Output (GPIO) module that supports two general-purpose output modes: direct output and shift out.

[Table 6-8](#) describes these modes in detail.

Note

Each PRU core can only be configured for one GPO mode at a time. Each mode uses the same R30 signals and internal register bits for different purposes. A summary is found in [Table 6-8](#).

Note

The [ICSSG_GPCFG0_REG](#) register, bitfield [29-26] PR1_PRU0_GP_MUX_SEL (PRU0 or PRU1) in the PRU_ICSSG CFG register space needs to be set to 0h for GP mode. For a given PRU core, the following IO modes are mutually exclusive: GP mode, Sigma Delta mode, and 3 channel Peripheral I/F mode.

Table 6-8. PRU R30 (EGPO) Output Mode

Mode	Function	Configuration
Direct output	pru<n>_r30[19:0] feeds directly to GPO[19:0]	Default state
Shift out	- pru<n>_r30[0] is shifted out on DATAOUT on every rising edge of pru<n>_r30[1] (CLOCKOUT). - LOAD_GPO_SH0 (Load Shadow Register 0) is mapped to pru<n>_r30[29]. - LOAD_GPO_SH1 (Load Shadow Register 1) is mapped to pru<n>_r30[30]. - ENABLE_SHIFT is mapped to pru<n>_r30[31].	Enabled by ICSSG_GPCFG0_REG register (PRU0 or PRU1) Free Running Clock or Fixed Clock Count Mode selected by ICSSG_GPECFG0_REG register.

Table 6-9. GPO Mode Descriptions

Pad Names at Device Level ⁽¹⁾	GPO Modes	
	Direct output	Shift out
PRG<k>_PRU<n>_GPO0	GPO0	DATAOUT
PRG<k>_PRU<n>_GPO1	GPO1	CLOCKOUT
PRG<k>_PRU<n>_GPO2	GPO2	
PRG<k>_PRU<n>_GPO3	GPO3	
PRG<k>_PRU<n>_GPO4	GPO4	
PRG<k>_PRU<n>_GPO5	GPO5	
PRG<k>_PRU<n>_GPO6	GPO6	
PRG<k>_PRU<n>_GPO7	GPO7	
PRG<k>_PRU<n>_GPO8	GPO8	
PRG<k>_PRU<n>_GPO9	GPO9	
PRG<k>_PRU<n>_GPO10	GPO10	
PRG<k>_PRU<n>_GPO11	GPO11	
PRG<k>_PRU<n>_GPO12	GPO12	
PRG<k>_PRU<n>_GPO13	GPO13	
PRG<k>_PRU<n>_GPO14	GPO14	
PRG<k>_PRU<n>_GPO15	GPO15	

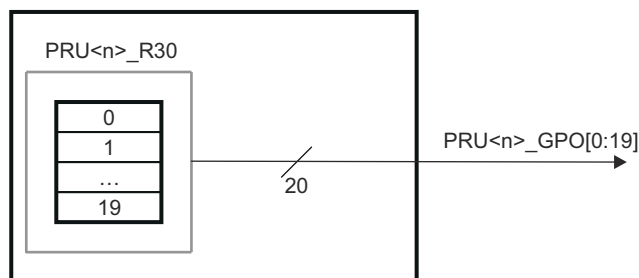
Table 6-9. GPO Mode Descriptions (continued)

Pad Names at Device Level ⁽¹⁾	GPO Modes	
	Direct output	Shift out
PRG<k>_PRU<n>_GPO16	GPO16	
PRG<k>_PRU<n>_GPO17	GPO17	
PRG<k>_PRU<n>_GPO18	GPO18	
PRG<k>_PRU<n>_GPO19	GPO19	

(1) These pins are also used for Sigma Delta or Peripheral I/F mode.

6.2.2.3.4.1 PRU EGPOs Direct Output

The PRU0_r30 [19:0] bits of the internal PRU register files are mapped to device-level, general-purpose output pins (PRU0_GPO[0:19]). In GPO Direct Output mode, PRU0_r30[0:19] feed directly to PRU0_GPO[0:19]. Each PRU of the PRU_ICSSG has a separate mapping to pins, so that there are 40 total general-purpose outputs from the PRU_ICSSG. See the device's system reference guide or datasheet for device-specific pin mapping.



icss-009

Figure 6-7. PRU R30 (EGPO) Direct Output Mode Block Diagram

Note

R30 is not initialized after reset. To avoid unintended output signals, R30 should be initialized before pinmux configuration of PRU signals.

6.2.2.3.4.2

Note

R30 is not initialized after reset. To avoid unintended output signals, R30 should be initialized before pinmux configuration of PRU signals.

6.2.2.3.4.3 PRU EGPO Shift Out

In shift out mode, data is shifted out of PRU0_r30[0] (PRU0_DATAOUT) on every rising edge of PRU0_r30[1] (PRU0_CLOCK). The shift rate is controlled by the effective divisor of two cascaded dividers applied to the ICSSG<n>_CORE_CLK clock (150MHz/ 200MHz/ 225MHz). These cascaded dividers can each be configured through the PRU_ICSSG CFG register space to a value of {1, 1.5, ..., 16}. Table 6-10 shows sample effective clock values and the divisor values that can be used to generate these clocks. Note that shift out mode supports two clocking submodes - Free Running Clock Mode (default) and Fixed Clock Count Mode. The clocking submode is selected through ICSSG_GPECFG0_REG[5] PRU0_GPO_SHIFT_CLK_FREE. In Free Running Clock Mode, PRU0_CLOCKOUT is a free running clock that starts when the PRU GPO mode is set to shift out mode.

Table 6-10. Effective Clock Values

Generated Clock	PRU0_GPO_DIV0	PRU0_GPO_DIV1
8 MHz	12.5 (17h)	2 (02h)
10 MHz	10 (12h)	2 (02h)
16 MHz	16 (1Eh)	1 (00h)

Table 6-10. Effective Clock Values (continued)

Generated Clock	PRU0_GPO_DIV0	PRU0_GPO_DIV1
20 MHz	10 (12h)	1 (00h)

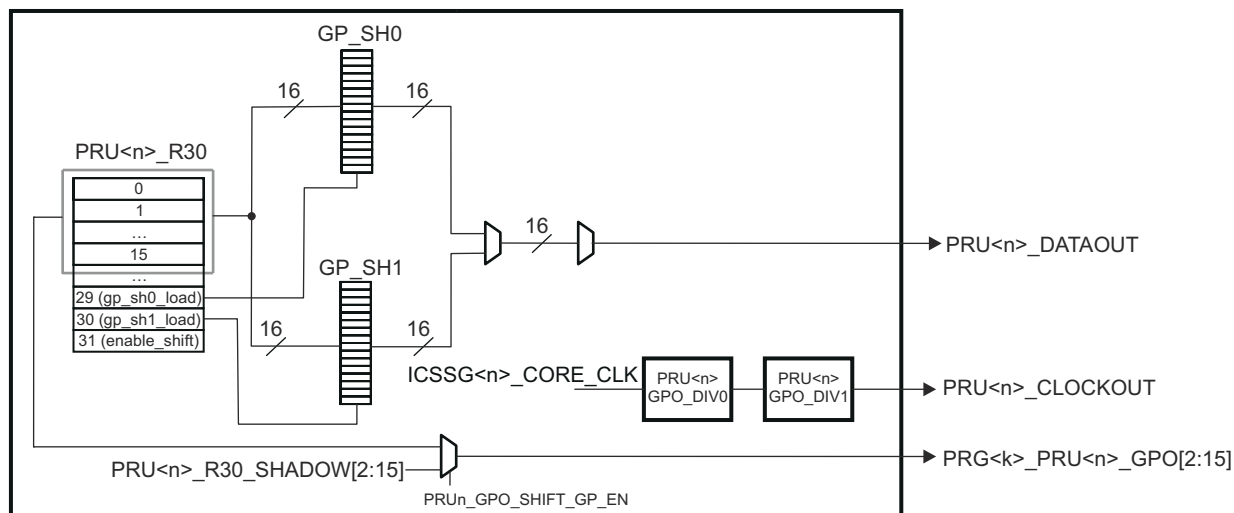
Shift out mode uses two 16-bit shadow registers (GPO_SH0 and GPO_SH1) to support ping-pong buffers. Each shadow register has independent load controls programmable through PRU0_r30[29:30] (PRU0_LOAD_GPO_SH[0:1]). While PRU0_LOAD_GPO_SH[0:1] is set, the contents of PRU<n>_R30[0:15] are loaded into GPO_SH0 and GPO_SH1 shadow registers.

The data shift will start from the LSB or MSB of GPO_SH0 when PRU<n>_R30[31] (PRU0_ENABLE_SHIFT) is set. The LSB or MSB setting is configurable through ICSSG_GPECFG0_REG[4] PRU0_GPO_SHIFT_SWAP. Note that if no new data is loaded into GPO_SH0/GPO_SH1 after shift operation, the shift operation will continue looping and shifting out the pre-loaded data.

For Free Running Clock Mode, the shift operation will continue until PRU0_ENABLE_SHIFT is cleared. When PRU0_ENABLE_SHIFT is cleared, the shift operation will finish shifting out the current shadow register, stop, and then reset.

For Fixed Clock Count Mode, the number of data bits to be shifted out is defined by ICSSG_GPECFG0_REG[15-8] PRU0_GPO_SHIFT_CNT. PRU<n>_CLOCKOUT will stop either high or low with the last data bit. The last data bit will remain persistent. However, the clock stop state is configurable through ICSSG_GPECFG0_REG[16] PRU0_GPO_SHIFT_CLK_HIGH.

The source of PRG<k>_PRU<n>_GPO[2:15] is configurable by ICSSG_GPECFG0_REG[6] PRU0_GPO_SHIFT_GP_EN. By default, if any device-level pins mapped to PRU<n>_R30[2-15] are configured for the PRG<k>_PRU<n>_GPO[2:15] pinmux mode, then these pins will reflect the shadow register value written to PRU<n>_R30. Any pin configured for a different pinmux setting will not reflect the shadow register value written to PRU<n>_R30. However, setting ICSSG_GPECFG0_REG[6] PRU0_GPO_SHIFT_GP_EN = 1h allows PRU<n>_R30[2:15] to be controlled by PRU<n>_R30_SHADOW[2-15], which is updated by PRU<n>_R30[2:15] when PRU<n>_R30[28] = 1h.



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Figure 6-8. PRU R30 (GPO) Shift Out Mode Block Diagram

6.2.2.3.4.3.1 PRU EGPO Programming Model

After the PRU is intilized, the software should only enable Shift Out Mode configuration per intilization.

Follow these steps to use the GPO shift out mode:

Step 1: Initialization

1. Load 16-bits of data into GPO_SH0 shadow register:

- GPO_SH0 = R30[29] ([ICSSG_GPECFG0_REG\[4\]](#) PRU0_GPO_SHIFT_SWAP (or CFG1, PRU1); R30[0-15] : R30[15-0]) : GPO_SH0)
- 2. Load 16-bits of data into GPO_SH1 shadow register:
 - GPO_SH1 = R30[30] ([ICSSG_GPECFG0_REG\[4\]](#) PRU0_GPO_SHIFT_SWAP (or CFG1, PRU1); R30[0-15] : R30[15-0]) : GPO_SH1)

Continuous Mode (Free running clock mode) ([ICSSG_GPECFG0_REG\[5\]](#) PRU0_GPO_SHIFT_CLK_FREE = 1h):

1. R30[31] = 1h (enable shift)
2. Start Loop
3. Poll [ICSSG_GPCFG0_REG\[25\]](#) PRU0_GPO_SH1_SEL (or CFG1, PRU1)
 - If [ICSSG_GPCFG0_REG\[25\]](#) PRU0_GPO_SH1_SEL = 1h
 - Load new 16-bits of data into GPO_SH0 shadow register
4. Poll [ICSSG_GPCFG0_REG\[25\]](#) PRU0_GPO_SH1_SEL (or CFG1, PRU1)
 - If [ICSSG_GPCFG0_REG\[25\]](#) PRU0_GPO_SH1_SEL = 0h
 - Load new 16-bits of data into GPO_SH1 shadow register
5. If more data, loop to 2. Start Loop
6. If no more data, exit
7. R30[31] = 0h (enable shift)

Follow these steps to use the GPO Fixed Packet Length mode:

Fixed Packet Length Mode: ([ICSSG_GPECFG0_REG\[5\]](#) PRU0_GPO_SHIFT_CLK_FREE = 0h):

To enable this mode, the software should prepare the precondition to get the PRU<n>_CLOCKOUT and PRU<n>_DATAOUT in the correct defined state.

Precondition:

1. Clear [ICSSG_GPCFG0_REG\[14\]](#) PRU0_GPO_MODE
2. Configure the Shift Out dividers
3. Clear [ICSSG_GPECFG0_REG\[5\]](#) PRU0_GPO_SHIFT_CLK_FREE (PRU0 or PRU1)
4. Write [ICSSG_GPECFG0_REG\[16\]](#) PRU0_GPO_SHIFT_CLK_HIGH = 1h if Stop high or PRU0_GPO_SHIFT_CLK_HIGH = 0h if Stop low
5. Configure [ICSSG_GPECFG0_REG\[15-8\]](#) PRU0_GPO_SHIFT_CNT to 8h, in order to shift out 8-bits for precondition
6. Load data into GPO_SH0, load FFh (want one at end) or 0h (want zero at end)
7. Set R30[31] = 1h (enable shift)
8. Wait for [ICSSG_GPECFG0_REG\[17\]](#) PRU0_GPO_SHIFT_CLK_DONE = 1h (PRU0 or PRU1)
9. Clear R30[31] = 0h (enable shift)

After the precondition is executed, PRU<n>_CLOCKOUT and PRU<n>_DATAOUT are in the correct state, then the user can configure [ICSSG_GPCFG0_REG\[14\]](#) PRU0_GPO_MODE = 1h (Serial Mode).

After this operation is completed then the software controls the length of the packet along with the number of clock cycles in addition to the idle state of the clock.

[ICSSG_GPECFG0_REG\[15-8\]](#) PRU0_GPO_SHIFT_CNT bit field defines the number of bits shifted out.

- When it is configured to stop low ([ICSSG_GPECFG0_REG\[16\]](#) PRU0_GPO_SHIFT_CLK_HIGH = 0h), this equals the number of rising edge clocks minus one seen on shift clock (ICSSG<n>_CORE_CLK).
- When it is configured to stop high ([ICSSG_GPECFG0_REG\[16\]](#) PRU0_GPO_SHIFT_CLK_HIGH = 1h), this equals the number of rising edge clocks minus one seen on shift clock (ICSSG<n>_CORE_CLK).

This enables the software to fully control the state of shift data (PRU<n>_DATAOUT) for the first edge event. For stop low (PRU0_GPO_SHIFT_CLK_HIGH = 0h), the first edge event is rising edge, the first bit of new data is shifted 1 full clock cycle before the first rising edge seen on the shift clock (ICSSG<n>_CORE_CLK). For stop high (PRU0_GPO_SHIFT_CLK_HIGH = 1h), the first edge event is falling edge, the first bit of new data is shifted 1/2 full clock cycle before the first falling edge seen on shift clock (ICSSG<n>_CORE_CLK).

Send Data

1. Load Data into GPO_SH0/ GPO_SH1

2. Configure the [ICSSG_GPECFG0_REG](#)[15-8] PRU0_GPO_SHIFT_CNT to Nh (where N is the number of bits to be shifted out)
3. Set R30[31] = 1h (enable shift)

Active Data Loop:

1. Monitor when a shadow register has finished shifting out data and can be loaded with new data:
 - (a) Poll PRU0_GPO_SH1_SEL bit in the [ICSSG_GPCFG0_REG](#) register (PRU0 or PRU1)
 - (b) Load new 16-bits of data into GPO_SH0 if PRU0_GPO_SH1_SEL = 1h
 - (c) Exit loop if PRU0_GPO_SHIFT_CLK_DONE = 1h
2. If more data needs to be send, loop to Active Data Loop:
 - (a) Poll PRU0_GPO_SH1_SEL bit of the [ICSSG_GPCFG0_REG](#) register (PRU0 or PRU1)
 - (b) Load new 16-bits of data into GPO_SH1 if PRU0_GPO_SH1_SEL = 0h
 - (c) Jump to Active Data loop if PRU0_GPO_SHIFT_CLK_DONE = 0h
 - (d) Exit loop if PRU0_GPO_SHIFT_CLK_DONE = 1h

Exit:

1. Write 1h to PRU0_GPO_SHIFT_CLK_DONE bit to clear.
2. Clear R30[31] = 0h (enable shift)
3. If more data packets need to be send go to Send Data
4. If no more data, exit loop

Note: Idle time between packets must be greater than 4 clock cycles.

Note

Until the shift operation is disabled, the shift loop will continue looping and shifting out the pre-loaded data if no new data has been loaded into GPO_SH0/1.

6.2.2.3.4.3.2

Follow these steps to use the GPO shift out mode:

Step 1: Initialization

1. Load 16-bits of data into GPO_SH0 shadow register:
 - GPO_SH0 = R30[29] ([ICSSG_GPECFG0_REG](#)[4] PRU0_GPO_SHIFT_SWAP (or CFG1, PRU1); R30[0-15] : R30[15-0]) : GPO_SH0)
2. Load 16-bits of data into GPO_SH1 shadow register:
 - GPO_SH1 = R30[30] ([ICSSG_GPECFG0_REG](#)[4] PRU0_GPO_SHIFT_SWAP (or CFG1, PRU1); R30[0-15] : R30[15-0]) : GPO_SH1)

Continous Mode (Free running clock mode) ([ICSSG_GPECFG0_REG](#)[5] PRU0_GPO_SHIFT_CLK_FREE = 1h):

1. R30[31] = 1h (enable shift)
2. Start Loop
3. Poll [ICSSG_GPCFG0_REG](#)[25] PRU0_GPO_SH1_SEL (or CFG1, PRU1)
 - If [ICSSG_GPCFG0_REG](#)[25] PRU0_GPO_SH1_SEL = 1h
 - Load new 16-bits of data into GPO_SH0 shadow register
4. Poll [ICSSG_GPCFG0_REG](#)[25] PRU0_GPO_SH1_SEL (or CFG1, PRU1)
 - If [ICSSG_GPCFG0_REG](#)[25] PRU0_GPO_SH1_SEL = 0h
 - Load new 16-bits of data into GPO_SH1 shadow register
5. If more data, loop to 2. Start Loop
6. If no more data, exit
7. R30[31] = 0h (enable shift)

Follow these steps to use the GPO Fixed Packet Length mode:

Fixed Packet Length Mode: ([ICSSG_GPECFG0_REG](#)[5] PRU0_GPO_SHIFT_CLK_FREE = 0h):

To enable this mode, the software should prepare the precondition to get the PRU<n>_CLOCKOUT and PRU<n>_DATAOUT in the correct defined state.

Precondition:

1. Clear [ICSSG_GPCFG0_REG](#)[14] PRU0_GPO_MODE
2. Configure the Shift Out dividers
3. Clear [ICSSG_GPECFG0_REG](#)[5] PRU0_GPO_SHIFT_CLK_FREE (PRU0 or PRU1)
4. Write [ICSSG_GPECFG0_REG](#)[16] PRU0_GPO_SHIFT_CLK_HIGH = 1h if Stop high or PRU0_GPO_SHIFT_CLK_HIGH = 0h if Stop low
5. Configure [ICSSG_GPECFG0_REG](#)[15-8] PRU0_GPO_SHIFT_CNT to 8h, in order to shift out 8-bits for precondition
6. Load data into GPO_SH0, load FFh (want one at end) or 0h (want zero at end)
7. Set R30[31] = 1h (enable shift)
8. Wait for [ICSSG_GPECFG0_REG](#)[17] PRU0_GPO_SHIFT_CLK_DONE = 1h (PRU0 or PRU1)
9. Clear R30[31] = 0h (enable shift)

After the precondition is executed, PRU<n>_CLOCKOUT and PRU<n>_DATAOUT are in the correct state, then the user can configure [ICSSG_GPCFG0_REG](#)[14] PRU0_GPO_MODE = 1h (Serial Mode).

After this operation is completed then the software controls the length of the packet along with the number of clock cycles in addition to the idle state of the clock.

[ICSSG_GPECFG0_REG](#)[15-8] PRU0_GPO_SHIFT_CNT bit field defines the number of bits shifted out.

- When it is configured to stop low ([ICSSG_GPECFG0_REG](#)[16] PRU0_GPO_SHIFT_CLK_HIGH = 0h), this equals the number of rising edge clocks minus one seen on shift clock (ICSSG<n>_CORE_CLK).
- When it is configured to stop high ([ICSSG_GPECFG0_REG](#)[16] PRU0_GPO_SHIFT_CLK_HIGH = 1h), this equals the number of rising edge clocks minus one seen on shift clock (ICSSG<n>_CORE_CLK).

This enables the software to fully control the state of shift data (PRU<n>_DATAOUT) for the first edge event. For stop low (PRU0_GPO_SHIFT_CLK_HIGH = 0h), the first edge event is rising edge, the first bit of new data is shifted 1 full clock cycle before the first rising edge seen on the shift clock (ICSSG<n>_CORE_CLK). For stop high (PRU0_GPO_SHIFT_CLK_HIGH = 1h), the first edge event is falling edge, the first bit of new data is shifted 1/2 full clock cycle before the first falling edge seen on shift clock (ICSSG<n>_CORE_CLK).

Send Data

1. Load Data into GPO_SH0/ GPO_SH1
2. Configure the [ICSSG_GPECFG0_REG](#)[15-8] PRU0_GPO_SHIFT_CNT to Nh (where N is the number of bits to be shifted out)
3. Set R30[31] = 1h (enable shift)

Active Data Loop:

1. Monitor when a shadow register has finished shifting out data and can be loaded with new data:
 - (a) Poll PRU0_GPO_SH1_SEL bit in the [ICSSG_GPCFG0_REG](#) register (PRU0 or PRU1)
 - (b) Load new 16-bits of data into GPO_SH0 if PRU0_GPO_SH1_SEL = 1h
 - (c) Exit loop if PRU0_GPO_SHIFT_CLK_DONE = 1h
2. If more data needs to be send, loop to Active Data Loop:
 - (a) Poll PRU0_GPO_SH1_SEL bit of the [ICSSG_GPCFG0_REG](#) register (PRU0 or PRU1)
 - (b) Load new 16-bits of data into GPO_SH1 if PRU0_GPO_SH1_SEL = 0h
 - (c) Jump to Active Data loop if PRU0_GPO_SHIFT_CLK_DONE = 0h
 - (d) Exit loop if PRU0_GPO_SHIFT_CLK_DONE = 1h

Exit:

1. Write 1h to PRU0_GPO_SHIFT_CLK_DONE bit to clear.
2. Clear R30[31] = 0h (enable shift)
3. If more data packets need to be send go to Send Data
4. If no more data, exit loop

Note: Idle time between packets must be greater than 4 clock cycles.

Note

Until the shift operation is disabled, the shift loop will continue looping and shifting out the pre-loaded data if no new data has been loaded into GPO_SH0/1.

6.2.2.3.5 Sigma Delta (SD) Decimation Filtering

Sigma-delta Sinc filtering is achieved by the combination of PRU hardware and firmware. PRU hardware provides hardware integrators that do the accumulation part of Sinc filtering, while the differentiation part is done in firmware.

The integrator serves to count the number of 1's per clock event. Each channel has three cascaded counters, which are the accumulators for the Sinc3 filter. Each counter is 28 bits, giving a maximum count of 268,435,456. Each channel has a free running rollover clock counter. This sample counter updates the count value on the effective clock event for that channel. Each channel also contains a programmable counter compare block, and the compare register has a size of 8 bits. However, the minimum value is 4 and maximum value is 256 due to the 28-bit accumulator. Once sample counter compare value is reached, the shadow register copy is updated and the shadow register copy flag is set.

Features of the integrators in PRUs SD Demodulator:

- Up to 9 channels concurrent counting
- Software can read all 3 stages accumulators
- Flexible clock source configuration for each channel; option of independent clock source for each channel or one clock source for three channels
- Programmable, 8-bit sample counter compare register; used to set the OSR of Sinc filter
- Three 28-bit cascaded counters per channel for accumulation, only Sinc3 and Sinc2 modes supported
- Common channel enable (all channels are active or none are active)
- Fast 1 and 0 min/max count sliding programmable window for each of the 9 channels

6.2.2.3.5.1 Sigma Delta Block Diagram and Signals

The Sigma Delta's I/Os are multiplexed with the PRU GPI/GPO signals, as shown in [Table 6-11](#).

Note: The PR<k>_PRU<n>_GP_MUX_SEL bitfield in the [ICSSG_GPCFG0_REG](#) register (where k = 0 or 1 and n = 0 or 1) must be set to 3h for configure the GPI/GPO signals for SD mode.

Table 6-11. PRU GPI Signals and Configurations for Sigma Delta

Signal Names at Device Level ⁽¹⁾	Sigma Delta (SD) Mode	Function
PRG<k>_PRU<n>_GPI0	SD0_CLK	SD demodulator clock channel 0
PRG<k>_PRU<n>_GPI1	SD0_D	SD demodulator data channel 0
PRG<k>_PRU<n>_GPI2	SD1_CLK	SD demodulator clock channel 1
PRG<k>_PRU<n>_GPI3	SD1_D	SD demodulator data channel 1
PRG<k>_PRU<n>_GPI4	SD2_CLK	SD demodulator clock channel 2
PRG<k>_PRU<n>_GPI5	SD2_D	SD demodulator data channel 2
PRG<k>_PRU<n>_GPI6	SD3_CLK	SD demodulator clock channel 3
PRG<k>_PRU<n>_GPI7	SD3_D	SD demodulator data channel 3
PRG<k>_PRU<n>_GPI8	SD4_CLK	SD demodulator clock channel 4
PRG<k>_PRU<n>_GPI9	SD4_D	SD demodulator data channel 4
PRG<k>_PRU<n>_GPI10	SD5_CLK	SD demodulator clock channel 5
PRG<k>_PRU<n>_GPI11	SD5_D	SD demodulator data channel 5

Table 6-11. PRU GPI Signals and Configurations for Sigma Delta (continued)

Signal Names at Device Level ⁽¹⁾	Sigma Delta (SD) Mode	Function
PRG<k>_PRU<n>_GPI12	SD6_CLK	SD demodulator clock channel 6
PRG<k>_PRU<n>_GPI13	SD6_D	SD demodulator data channel 6
PRG<k>_PRU<n>_GPI14	SD7_CLK	SD demodulator clock channel 7
PRG<k>_PRU<n>_GPI15	SD7_D	SD demodulator data channel 7
PRG<k>_PRU<n>_GPI16	SD8_CLK	SD demodulator clock channel 8
PRG<k>_PRU<n>_GPI17	SD8_D	SD demodulator data channel 8
PRG<k>_PRU<n>_GPI18	-	
PRG<k>_PRU<n>_GPI19	-	

(1) Note: These signals are shared with the GP and Peripheral I/Fs. To configure for Sigma Delta, [ICSSG_GPCFG0_REG\[29-26\]](#) PR1_PRU0_GP_MUX_SEL (where k = 0 or 1 and n = 0 or 1) needs to be set to 3h for SD mode.

The PRG<k>_PRU0_GPI1 signal (muxed with SD0_D) can be used as SD_CLKOUT when PRU_ICSSG generates clock. This is a trade-off as PRU application will lose one SD channel. SD_CLKOUT needs to go through a clock generator chip if driving multiple sigma delta modulators and also be looped back into PRU_ICSSG as SD_CLKIN, typically pru_gpi16.

Note: To output the SD clock on PR<k>_PRU0_GPO1, this device requires that the PRU core be configured for both SD and shift out mode ([ICSSG_GPCFG0_REG\[29-26\]](#) PR1_PRU0_GP_MUX_SEL = 3h and [ICSSG_GPCFG0_REG\[14\]](#) PRU<n>_GPO_MODE = 1h). Be sure to configure the shift out mode's clock divisors before enabling shift out mode ([ICSSG_GPCFG0_REG\[14\]](#) PRU<n>_GPO_MODE = 1h). Additionally, the PRU_ICSSG0, PRU0 SD clock is routed to both PR0_PRU0_GPO1 and PR0_PRU1_GPO1. [Figure 6-9](#) shows a block diagram of the Sigma Delta implementation. Full description of the PRU R30 and R31 registers are shown in [Table 6-13](#) and [Table 6-14](#).

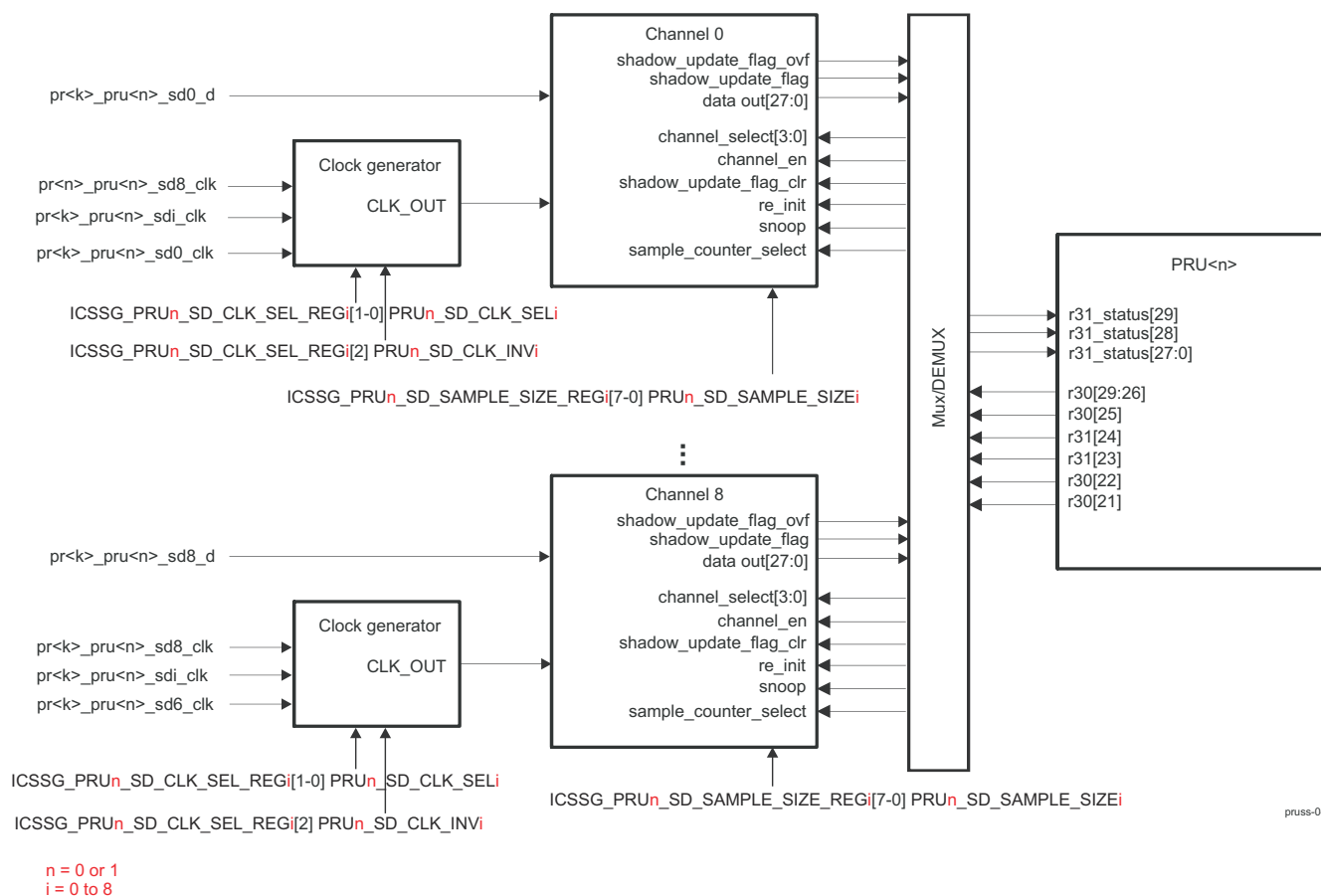


Figure 6-9. Sigma Delta Block Diagram

Note: Each channel can independently be configured to use one of three external clock sources. [Table 6-12](#) shows the clock source options, selectable through ICSSG_PRU0_SD_CLK_SEL_REGi[1-0] PRU0_SD_CLK_SELi (where n = 0 or 1 and i = 0 to 8).

Table 6-12. Sigma Delta External Clock Sources

PRU0_SD_CLK_SELi value	Clock Source
0	pr<k>_pru<n>_sd8_clk
1	pr<k>_pru<n>_sd<i>_clk
2	pr<k>_pru<n>_sd0_clk for sd0, sd1, and sd2; pr<k>_pru<n>_sd3_clk for sd3, sd4, and sd5; pr<k>_pru<n>_sd6_clk for sd6, sd7, and sd8

6.2.2.3.5.2 PRU R30 / R31 Interface

The PRU uses the R30 and R31 registers to interface with the Sigma Delta interface. [Table 6-13](#) and [Table 6-14](#) shows the R31 and R30 interface for the Sigma Delta mode. Note that only the parameters and data for one channel can be viewed at a time. The channel to be viewed is determined by the r30[29-26] (channel_select).

Table 6-13. Sigma Delta PRU Registers: R31

Bits	Field Name	Description
31-30	Reserved	
29	shadow_update_flag_ovf	Shadow update flag overflow, set when over sample count equals over sample size and shadow_update_flag is still set. Set bit R31[24] to clear the flag.
28	shadow_update_flag	Shadow update flag, set when over sample count equals over sample size and shadow_update_flag is still set. Set bit R31[24] to clear the flag.
27-0	data_out[27-0]/ shadow_update_flag_clr (R31[24]) / re_init (R31[23])	data_out[27] (read): most-significant bit of sample data shadow_update_flag_clr (write): re_init (write): Set to reset all counters, flags, and shadow copy. Updates over_sample_size based on the current ICSSG_PRU0_SD_SAMPLE_SIZE_REGi[7-0] register (where n = 0 or 1 and i = 0 to 8) on the selected channel. shadow_update_flag_clr (write): Set to clear shadow_update_flag and shadow_update_flag_ovf (if set).

Table 6-14. Sigma Delta PRU Registers: R30

Bits	Field Name	Description
31-30	Reserved	
29-26	channel_select[3-0]	Channel select ⁽¹⁾ 0h: Channel 0 ... 8h: Channel 8 9h: Reserved ... Fh: Reserved
25	channel_en	Global Channel enable (effects all 9 channels). 0h: All channels disabled. Counters/flags are cleared. 1h: All channels enabled.
24-23	Reserved	
22	snoop	Enable snoop (i.e. fetch data) on the selected channel. 0h: acc1/acc2/acc3 shadow copy 1h: current acc1/acc2/acc3
21	sample_counter_select	Read sample counter. 0h: Not selected 1h: Sample count selected
20-0	Reserved	

(1) If ICSSG_PRU0_SD_CFG_REG[8] SHARE_EN = 1, SD channels are shared between RTU, PRU, and TX_PRU, 3 channels per CPU.

The PRU_ICSSG CFG register space has additional registers for controlling the SD demodulator module:

- ICSSG_PRU0_SD_CLK_SEL_REGi[5-4] PRU0_SD_ACC_SELi (where n = 0 or 1, i = 0 to 8) - Selects accumulator 1, 2 or 3 as source (acc1/acc2/acc3).

- #### 6.2.2.3.5.3 Sigma Delta Description

The block diagram illustrates the PRUn SD block architecture. It features two primary inputs: **SD_IN** and **CLK_OUT**. **SD_IN** is connected to a **Capture** block and a **Sync Flop**. **CLK_OUT** is connected to a **Sync Flop**. The data path begins with **data_in**, which passes through a **Sync Flop** and then into the **acc1** accumulator. The **acc1** accumulator calculates $acc1 = acc1 + data\_in$. Its 28-bit output is fed into the **acc2** accumulator, which calculates $acc2 = acc2 + acc1$. The 28-bit output of **acc2** is then fed into the **acc3** accumulator, which calculates $acc3 = acc3 + acc2$. The 28-bit output of **acc3** is connected to a multiplexer. The other input to this multiplexer is **ICSSG_PRUn_SD_CLK_SEL_REGI[5-4]**. The output of the multiplexer is connected to a **shadow** register. The output of the **shadow** register is connected to another multiplexer. The other input to this multiplexer is **ICSSG_PRUn_SD_SAMPLE_SIZE_REGI[7-0]** (labeled as **PRUn_SD_SAMPLE_SIZEI**). The output of this multiplexer is connected to a **sample_count** block. The output of the **sample_count** block is connected to a **shadow** register. The output of this **shadow** register is connected to a final multiplexer. The other input to this multiplexer is **r30[21] (sample_counter_select)**. The output of the final multiplexer is **r31[27-0] (data_out)**.

The diagram illustrates the internal structure of the PRUn_SD block. It features a data path that begins with SD_IN and CLK_OUT inputs. SD_IN is captured and then passes through a Sync Flop. CLK_OUT is also passed through a Sync Flop. The data path includes three accumulators (acc1, acc2, acc3) and a sample_count block. The output is a 28-bit data_out (r31[27:0]) selected from a shadow register. The diagram also shows control signals like fast_detect, ICSSG_PRUn_SD_CLK_SEL_REG[5:4], and PRUn_SD_ACC_SEL[1].

```
acc1 = acc1 + data_in
acc2 = acc2 + acc1
acc3 = acc3 + acc2
sample count = sample count + 1
```


Each accumulator will rollover at 0xFF_FFFF. For example if acc2 = 0x10 and acc3 = 0xFF_FFFF, then acc3 will update to 0x00_0000F on the next clock event. Sample counter will rollover when it equals the defined sample size (ICSSG_PRU0_SD_SAMPLE_SIZE_REGi[7-0] PRU0_SD_SAMPLE_SIZEi).

Note that while the channels are not enabled, no operations are performed and all flags and counters are cleared. If a new sample size is to be loaded, the PRU firmware should assert re_init (r31[23]), and all stored count values are cleared to 0.

Fast detect block is used to detect fast changes in the amount of ones, presented in a programmable sliding window of 4 to 32 bits. The sliding window is controlled by ICSSG_PRU0_SD_SAMPLE_SIZE_REGi[10-8] PRU0_FD_WINDOW_SIZE_i bit field.

Fast detect must be enabled through the ICSSG_PRU0_SD_SAMPLE_SIZE_REGi[23] PRU0_FD_EN_i register before SD is enabled. It will start the compare after the first 32 sample clocks. Fast detect block will remain active until a re_init (r31[23]) is asserted.

The Sigma Delta interface has two status flags:

- Shadow update flag (r31[28])
- Shadow update flag overflow (r31[29])

When sample_counter equals the defined sample size (ICSSG_PRU0_SD_SAMPLE_SIZE_REGi[7-0] PRU0_SD_SAMPLE_SIZEi), then the acc1/acc2/acc3 shadow register copy will be updated, the shadow_update_flag (r31[28]) will be set, and sample_counter will rollover to 0. The PRU firmware can clear this flag by writing '1' to shadow_update_flag_clr (r31[28]). If sample_count equals the defined sample size and the shadow_update_flag is still set, then shadow_update_flag_ovf (r31[29]) will be set. Similarly, the PRU firmware can clear this flag by writing '1' to shadow_update_flag_ovf_clr (r31[29]). Note that the clear operation for both flags has a higher priority than the set event.

The PRU firmware can monitor the acc2/acc3 and sample_counter values through data_out[27-0] (r31[27-0]). [Table 6-15](#) shows the configuration options for data_out[27-0].

Table 6-15. Data_out[27-0] Configuration Options

snoop (r30[22])	sample_counter_select (r30[21])	data_out (r31[27-0])
0	0	Reads acc1/acc2/acc3 shadow register copy. See Figure 6-10 Sigma Delta Hardware Integrators Block Diagram (snoop = 0).
1	0	Reads acc1/acc2/acc3 directly. See Figure 6-11 Sigma Delta Hardware Integrators Block Diagram (snoop = 1).
0	1	Reads sample_counter shadow register copy. See Figure 6-10 Sigma Delta Hardware Integrators Block Diagram (snoop = 0).
1	1	Reads sample_counter directly. See Figure 6-11 Sigma Delta Hardware Integrators Block Diagram (snoop = 1).

6.2.2.3.5.4 Sigma Delta Basic Programming Example

The following programming example assumes that the PRU is configured for Sigma Delta Mode (ICSSG_GPCFG0_REG[29-26] PR1_PRU<n>_GP_MUX_SEL = 3h).

1. Configure clock sources, accumulator source, and sample size:
 - a. ICSSG_PRU0_SD_CLK_SEL_REGi[1-0] PRU0_SD_CLK_SELi (where n = 0 or 1, i = 0 to 8) for clock source
 - b. ICSSG_PRU0_SD_CLK_SEL_REGi[2] PRU0_SD_CLK_INVi (where n = 0 or 1, i = 0 to 8) for clock polarity
 - c. ICSSG_PRU0_SD_CLK_SEL_REGi[5-4] PRU0_SD_ACC_SELi (where n = 0 or 1, i = 0 to 8) - for accumulator source (acc1/acc2/acc3)
 - d. ICSSG_PRU0_SD_SAMPLE_SIZE_REGISTERi[7-0] PRU0_SD_SAMPLE_SIZE for sample size
2. Reinitialize all channels whose sample size was configured
 - a. Select channel by writing to channel_select (r30[29-26])
 - b. Delay at least 1 PRU cycle before executing re_int in step 2c.

- c. Reinitialize selected channel by writing to re_init (r31[23])
 - d. Repeat steps 2a & 2b for all configured channels
3. Enable all channels by writing '1' to channel_en (r30[25])
4. Select channel by writing to channel_select (r30[29-26])
 - a. Poll shadow_update_flag (r31[28]) to detect when acc1/acc2/acc3 shadow register copy data is ready to be read
 - b. Delay at least 1 PRU cycle before polling shadow_update_flag in Step 4c.
 - c. Read data_out[27-0] (r31[27-0])
 - d. Clear shadow_update_flag by writing '1' to r31[24]
5. Repeat step 4 for new channel

6.2.2.3.6 Three Channel Peripheral Interface

The 3 channel Peripheral Interface supports functionality for operations utilizing the EnDat 2.2 and BiSS protocols.

This module supports the following features:

- 3 channels with baud range from 100 kHz to 16 MHz
- ICSSGn_UART_CLK (default) or ICSSGn_ICLK controller clock is an input to independent div16fr clock dividers to produce a 1X clock (PERIF<m>_CLK) and oversampling clock
- Half-duplex (TX and RX are not supported concurrently)
- TX FIFO size of 32 bits
- RX FIFO size of 4 bits
- Configurable shift size/oversampling on RX
- Optional RX frame size auto shut off
- Programmable HW delay 1 (wire delay, controlling when the clock signal is first driven low) and delay 2 (tst delay, controlling when the clock signal is first driven high) on TX operation
- Optional programmable TX termination
- Individual TX channel start trigger (tx_channel_go) or simultaneous TX start trigger for all channels (tx_global_go)
- Flexible HW assisted clock output generation to allow free running, stop high and stop low (after last RX data), or stop high (after last TX data) operation with optional software clock override feature
- Optional SW direct snoop of data input
- RX Start Bit of '1' or '0'

6.2.2.3.6.1 Peripheral Interface Block Diagram and Signal Configuration

The Peripheral Interface's I/Os are multiplexed with the PRU GPI/GPO signals, as shown in [Table 6-16](#). The PR1_PRU<n>_GP_MUX_SEL bitfield in the [ICSSG_GPCFG0_REG](#) register (PRU0 or PRU1) must be set to 1h for configure the GPI/GPO signals for Peripheral I/F mode.

Table 6-16. PRU GPI/GPO Signals and Configurations for Peripheral I/F⁽¹⁾

Pad Names at Device Level ^{(2) (3)}	Peripheral I/F Mode (ICSSG_GPCFG0_REG [29-26] PR1_PRU0_GP_MUX_SEL = 1h)
PRG<k>_PRU<n>_GPI0	
PRG<k>_PRU<n>_GPI1	
PRG<k>_PRU<n>_GPI2	
PRG<k>_PRU<n>_GPI3	
PRG<k>_PRU<n>_GPI4	
PRG<k>_PRU<n>_GPI5	
PRG<k>_PRU<n>_GPI6	
PRG<k>_PRU<n>_GPI7	
PRG<k>_PRU<n>_GPI8	
PRG<k>_PRU<n>_GPI9	PERIF0_IN
PRG<k>_PRU<n>_GPI10	PERIF1_IN
PRG<k>_PRU<n>_GPI11	PERIF2_IN
PRG<k>_PRU<n>_GPI12	

Table 6-16. PRU GPI/GPO Signals and Configurations for Peripheral I/F⁽¹⁾
(continued)

Pad Names at Device Level ^{(2) (3)}	Peripheral I/F Mode (ICSSG_GPCFG0_REG[29-26] PR1_PRU0_GP_MUX_SEL = 1h)
PRG<k>_PRU<n>_GPI13	
PRG<k>_PRU<n>_GPI14	
PRG<k>_PRU<n>_GPI15	
PRG<k>_PRU<n>_GPI16	
PRG<k>_PRU<n>_GPI17	
PRG<k>_PRU<n>_GPI18	
PRG<k>_PRU<n>_GPI19	
PRG<k>_PRU<n>_GPO0	PERIF0_CLK
PRG<k>_PRU<n>_GPO1	PERIF0_OUT
PRG<k>_PRU<n>_GPO2	PERIF0_OUT_EN
PRG<k>_PRU<n>_GPO3	PERIF1_CLK
PRG<k>_PRU<n>_GPO4	PERIF1_OUT
PRG<k>_PRU<n>_GPO5	PERIF1_OUT_EN
PRG<k>_PRU<n>_GPO6	PERIF2_CLK
PRG<k>_PRU<n>_GPO7	PERIF2_OUT
PRG<k>_PRU<n>_GPO8	PERIF2_OUT_EN
PRG<k>_PRU<n>_GPO9	
PRG<k>_PRU<n>_GPO10	
PRG<k>_PRU<n>_GPO11	
PRG<k>_PRU<n>_GPO12	
PRG<k>_PRU<n>_GPO13	
PRG<k>_PRU<n>_GPO14	
PRG<k>_PRU<n>_GPO15	
PRG<k>_PRU<n>_GPO16	
PRG<k>_PRU<n>_GPO17	
PRG<k>_PRU<n>_GPO18	
PRG<k>_PRU<n>_GPO19	

- (1) Usage of the Peripheral Interface signals are not restricted to only ENDAT interfaces.
(2) Note: These signals are shared with the GP, MII and Sigma Delta modes. To configure for Peripheral I/F, ICSSG_GPCFG0_REG[29-26] PR1_PRU0_GP_MUX_SEL needs to be set to 1h.
(3) Some devices may not pin out all 29 bits of R31 and all 32 bits of R30. For which pins are available on this device, see [Section 3 PRU_ICSSG Environment](#). See the device-specific Datasheet for device pin mapping.

A block diagram for the Peripheral I/F is included in [Figure 6-12](#). As shown, each channel is composed of four I/Os:

- PERIF<m>_IN - RX input data
- PERIF<m>_CLK - Clock (CLK_OUT) generated by the 1x (or TX) clock. The default value is 1.
- PERIF<m>_OUT - TX output data. The default value is 0.
- PERIF<m>_OUT_EN - TX enable output (1 = TX mode, 0 = RX mode). The default value is 0. Note: This signal is auto controlled by hardware.

Figure 6-12. Peripheral I/F Block Diagram

6.2.2.3.6.2 PRU R30 and R31 Interface

The PRU uses the R30 and R31 registers to interface with the Peripheral I/F. [Table 6-17](#) shows the R31 and R30 interface for the Peripheral I/F RX mode, and [Table 6-18](#) shows the comparable interface for the TX mode.

Table 6-17. Peripheral I/F RX

Register	Bits	Field name	Description
R31	31-30	Reserved	PRU Host Interrupts 1/0 from local INTC
	29	ovf2	Overflow Flag for Channel 2. Write 1 to clear.
	28	ovf1	Overflow Flag for Channel 1. Write 1 to clear.
	27	ovf0	Overflow Flag for Channel 0. Write 1 to clear.
	26	val2	Valid Flag for Channel 2. Write 1 to clear.
	25	val1	Valid Flag for Channel 1. Write 1 to clear.
	24	val0	Valid Flag for Channel 0. Write 1 to clear.
	23-16	rx_data_out2	Oversampled Data Output for Channel 2. Note: These bits are shared with the TX Interface. When TX_FIFO has stopped transmission, RX data will be selected.
	15-8	rx_data_out1	Oversampled Data Output for Channel 1. Note: These bits are shared with the TX Interface. When TX_FIFO has stopped transmission, RX data will be selected.
	7:0	rx_data_out0	Oversampled Data Output for Channel 0. Note: These bits are shared with the TX Interface. When TX_FIFO has stopped transmission, RX data will be selected.
R30	31-27	Reserved	
	26	rx_en2	RX Enable for Channel 2. 0h: Channel not enabled, all counters/flags will get reset 1h: Channel is enabled
	25	rx_en1	RX Enable for Channel 1. 0h: Channel not enabled, all counters/flags will get reset 1h: Channel is enabled
	24	rx_en0	RX Enable for Channel 0. 0h: Channel not enabled, all counters/flags will get reset 1h: Channel is enabled
	23-0	Reserved	

Table 6-18. Peripheral I/F TX

Register	Bits	Field name	Description
R31	31-30	Reserved	
	29-22	Reserved	
	21	tx_global_reinit_active/ busy2	Tx_global_reinit action has some latency do to clocking. This status shows if action is completed. 1h: Active 0h: Done For non reinit case, this bit states that last bit is on tx wire. It does not mean the clock is off. 1h: Last bit is not done 0h: Last bit on tx wire Note that by using rx auto arm feature, the observation is lost at rx enable. This can be used to determine when to enable rx during non-auto arm case.
	20	tx_global_go	TX global start of all channels. Note: FIFO must not be empty. If empty, transmit will not start.
	19	tx_global_reinit	Reinit all channels into default mode. This clears all flags and state machines for all channels. Note: Sequence should be assert tx_global_reinit then de-assert rx_en. This will ensure TX and RX are in reset/default state. User must assert this after the frame has been sent and TX is not busy.
	18	tx_channel_go	TX start the channel transmit (selected by tx_ch_sel). Note: FIFO must not be empty.
	17	unr2	Under Run Flag for Channel 2. This flag is only set when the tx_frame_count is nonzero and FIFO is empty at time to send data.
	16	ovr2	Over Run Flag for Channel 2
	15-14	Reserved	

Table 6-18. Peripheral I/F TX (continued)

Register	Bits	Field name	Description
	13	tx_global_reinit_active/ busy1	Tx_global_reinit action has some latency do to clocking. This status shows if action is completed. 1h: Active 0h: Done For non reinit case, this bit states that last bit is on tx wire. It does not mean the clock is off. 1h: Last bit is not done 0h: Last bit on tx wire Note that by using rx auto arm feature, the observation is lost at rx enable. This can be used to determine when to enable rx during non-auto arm case.
	12-10	tx_fifo_sts1	TX FIFO occupancy status for Channel 1. 0 :0 Empty 1h: 1 word 2h: 2 words 3h: 3 words 4h: Full 5h-7h: Reserved
	9	unr1	Under Run Flag for Channel 1. This flag is only set when the tx_frame_count is nonzero and FIFO is empty at time to send data.
	8	ovr1	Over Run Flag for Channel 1
	7-6	Reserved	
	5	tx_global_reinit_active/ busy0	Tx_global_reinit action has some latency do to clocking. This status shows if action is completed. 1h: Active 0h: Done For non reinit case, this bit states that last bit is on tx wire. It does not mean the clock is off. 1h: Last bit is not done 0h: Last bit on tx wire Note that by using rx auto arm feature, the observation is lost at rx enable. This can be used to determine when to enable rx during non-auto arm case.
	4-2	tx_fifo_sts0	TX FIFO occupancy status for Channel 0. 0h: Empty 1h: 1 word 2h: 2 words 3h: 3 words 4h: Full 5h-7h: Reserved
	1	unr0	Under Run Flag for Channel 0. This flag is only set when the tx_frame_count is nonzero and FIFO is empty at time to send data.
	0	ovr0	Over Run Flag for Channel 0
	31-21	Reserved	
R30	20-19	clk_mode	CLK_OUT mode. 0h: Free-running/stop-low. Clock will remain free-running until the receive module has received the number of bits indicated in rx_frame_counter and then the clock will stop low. 1h: Free-running/stop-high (default). Clock will remain free-running until the receive module has received the number of bits indicated in rx_frame_counter and then the clock will stop high. Note: This is the default/reset state, and a hardware reset or reinit will return clk_mode to this state. Note: The initial state of the clock will be high, but the clock will not start until TX GO event. 2h: Free-run. NOTE: You must do a reinit to get out of this clock mode then you can update clk_mode to a different mode. Also if you do multiple TX GO, the 2nd go should have tst_delay and wire_delay zero since the clock is free running after the first go. 3h: Stop high after transmit. Clock will run until the last TX bit is sent and stops high.
	18	Reserved	
	17-16	tx_ch_sel	TX channel select. 0h: Channel 0 1h: Channel 1 2h: Channel 2 3h: Reserved
	15-9	Reserved	

Table 6-18. Peripheral I/F TX (continued)

Register	Bits	Field name	Description
	7-0	tx_data	TX data for FIFO. Notes: FIFO transmits MSB first and is 32-bits deep. TX_FIFO_SWAP_BITS bit in the PRU_ICSSG_CFG register space can be used to flip the load order of bits. The FIFO has 2 modes of operation: 1. Preload and Go. This should be done for EnDAT and frames less than 32-bits. 2. Continuous mode. This should be done for frames bigger than 32-bits. In continuous mode, software needs to keep up with the line rate and ensure that the FIFO is never empty. When the FIFO is at 2 byte level, software needs to load the next 2 bytes. If software waits till the end of the empty state, it is possible to get the TX into a bad state. The FIFO state can be recovered via re-init.

Note

The PRU_ICSSG_CFG register space has additional registers for controlling the Peripheral I/F module.

6.2.2.3.6.3 Clock Generation

6.2.2.3.6.3.1 Configuration

The Peripheral I/F module has two source clock options, ICSSGn_UART_CLK (default) and ICSSGn_ICLK. There are two independent clock dividers (div16) for the 1x and oversampling (OS) clocks, and each clock divider is configurable by two cascading dividers:

- [31-16] PRU0_ED_TX_DIV_FACTOR and [15] PRU0_ED_TX_DIV_FACTOR_FRAC for the 1x clock
- [31-16] PRU0_ED_RX_DIV_FACTOR and [15] PRU0_ED_RX_DIV_FACTOR_FRAC for the OS clock

The 1x clock is output on the PERIF<m>_CLK signal. In TX mode, the output data is read from the TX FIFO at this 1x clock rate. The default value of this clock is high and the start and stop conditions for this clock are described in [Section 6.2.2.3.6.3.2 Clock Output Start Conditions](#) and [Section 6.2.2.3.6.3.3 Stop Conditions](#).

In RX mode, the input data is sampled at the OS clock rate. Note: The OS clock rate divided by the 1x clock rate must equal [2-0] PRU0_ED_RX_SAMPLE_SIZE.

Example clock rates and divisor values relative to the 192-MHz ICSSGn_UART_CLK source are shown in [Table 6-19](#).

Table 6-19. Clock Rate Examples for 192-MHz PRUSSn_UART_GFCLK Clock Source

TX_DIV_FACTOR	1x Clock	RX_DIV_FACTOR	RX_DIV_FACTOR_FRAC	OS Clock	Oversample Factor
12	16 MHz	1	1.5	128 MHz	8x
16	12 MHz	2	1	96 MHz	8x
24	8 MHz	3	1	64 MHz	8x
32	6 MHz	4	1	48 MHz	8x
48	4 MHz	6	1	32 MHz	8x
96	2 MHz	12	1	16 MHz	8x
192	1 MHz	24	1	8 MHz	8x

6.2.2.3.6.3.2 Clock Output Start Conditions

This section describes the configurable start conditions for the PERIF<m>_CLK. The software can completely control via ICSSG_PRU0_ED_CHm_CFG0_REG when bit [29] PRU0_ED_CLK_OUT_OVR_ENm = 1h (where n = 0 or 1 and m = 0 to 2). By default however, the PRU hardware will control the clocks as described in the following sections.

6.2.2.3.6.3.2.1 TX Mode (RX_EN = 0)

In TX mode, the PERIF<m>_CLK begins after the firmware loads the TX FIFO and sets either r30[20] (tx_global_go) or r30[17-16] (tx_channel_go) to 1h. After the “go” bit is set, the delay1 (wire delay) compensation counter for each channel begins. After delay1 is complete, PERIF<m>_CLK is driven low and then the delay2 (tst) counter begins. After the delay2 counter expires, the PERIF<m>_CLK starts running (first low and then

high). Therefore, first rising edge of PERIF<m>_CLK (measured from the go bit) = delay1 (tx wire delay) + delay2 (tst_counter delay) + half of the 1x clock frequency (since the clock starts low).

Figure 6-13 shows the start condition for TX mode. As shown in the figure, the default value of clock is high. The PRU_ICSSG_CFG register space has additional registers for controlling the TX start timing delay values:

- Delay 1: ICSSG_PRU0_ED_CHm_CFG0_REG[10-0] PRU0_ED_TX_WDLYm (where n = 0 or 1 and m = 0 to 2)
- Delay 2: ICSSG_PRU0_ED_CHm_CFG1_REG[15-0] PRU0_ED_TST_DELAY_COUNTERm (where n = 0 or 1 and m = 0 to 2)

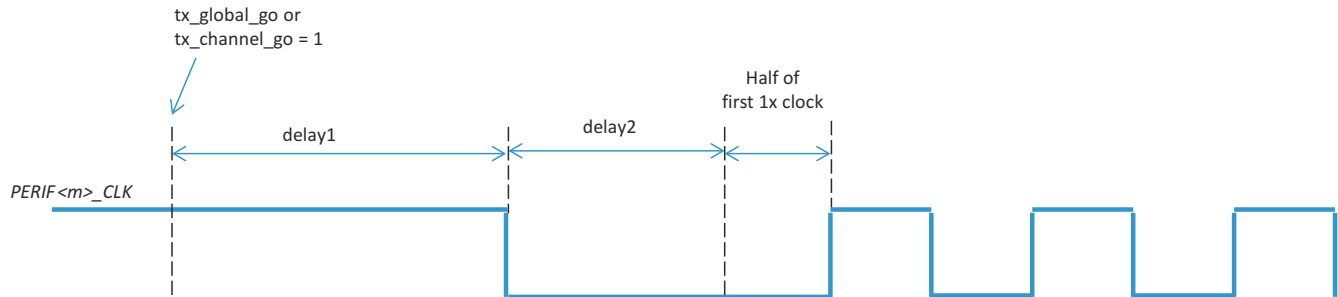


Figure 6-13. TX Mode Start Condition

6.2.2.3.6.3.2.2 RX Mode (RX_EN = 1)

In RX mode, the PERIF<m>_CLK will start running whenever the RX_EN is set. Note that the PRU firmware in this mode is responsible for any delay conditions.

The hardware can also auto-enable RX mode at the end of a TX transaction. The ICSSG_PRU0_ED_CHm_CFG1_REG[31-16] PRU0_ED_RX_EN_COUNTERm (where n = 0 or 1 and m = 0 to 2) is used to program a delay between the last TX bit sent and when the RX_EN is set.

6.2.2.3.6.3.3 Stop Conditions

The r30[20-19] (clk_mode[1:0]) value determines the stop condition for PERIF<m>_CLK. There are 4 options available:

clk_mode_value	Description
0	Stop low on last RX frame
1	Stop high on last RX frame
2	Run continuously
3	Stop high on last TX bit

The last RX frame is configured by ICSSG_PRU0_ED_CHm_CFG0_REG[27-16] PRU0_ED_RX_FRAME_SIZE_m, and the last TX bit is configured by ICSSG_PRU0_ED_CHm_CFG0_REG[15-11] PRU0_ED_TX_FRAME_SIZE_m (where n = 0 or 1 and m = 0 to 2). Each stop condition is shown in Figure 6-14 through Figure 6-17.

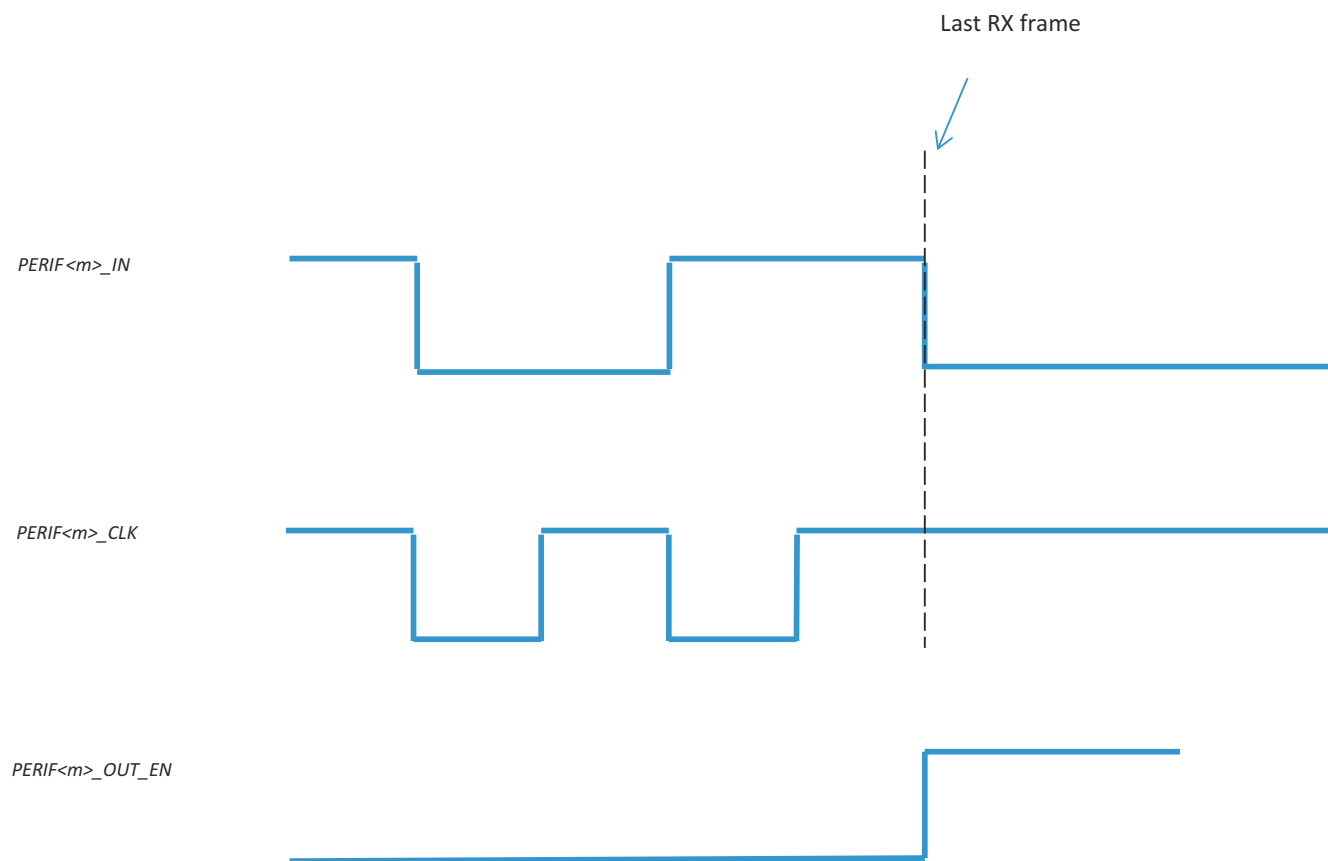


Figure 6-14. $PERIF<m>_{CLK}$ Stop High on Last RX Frame

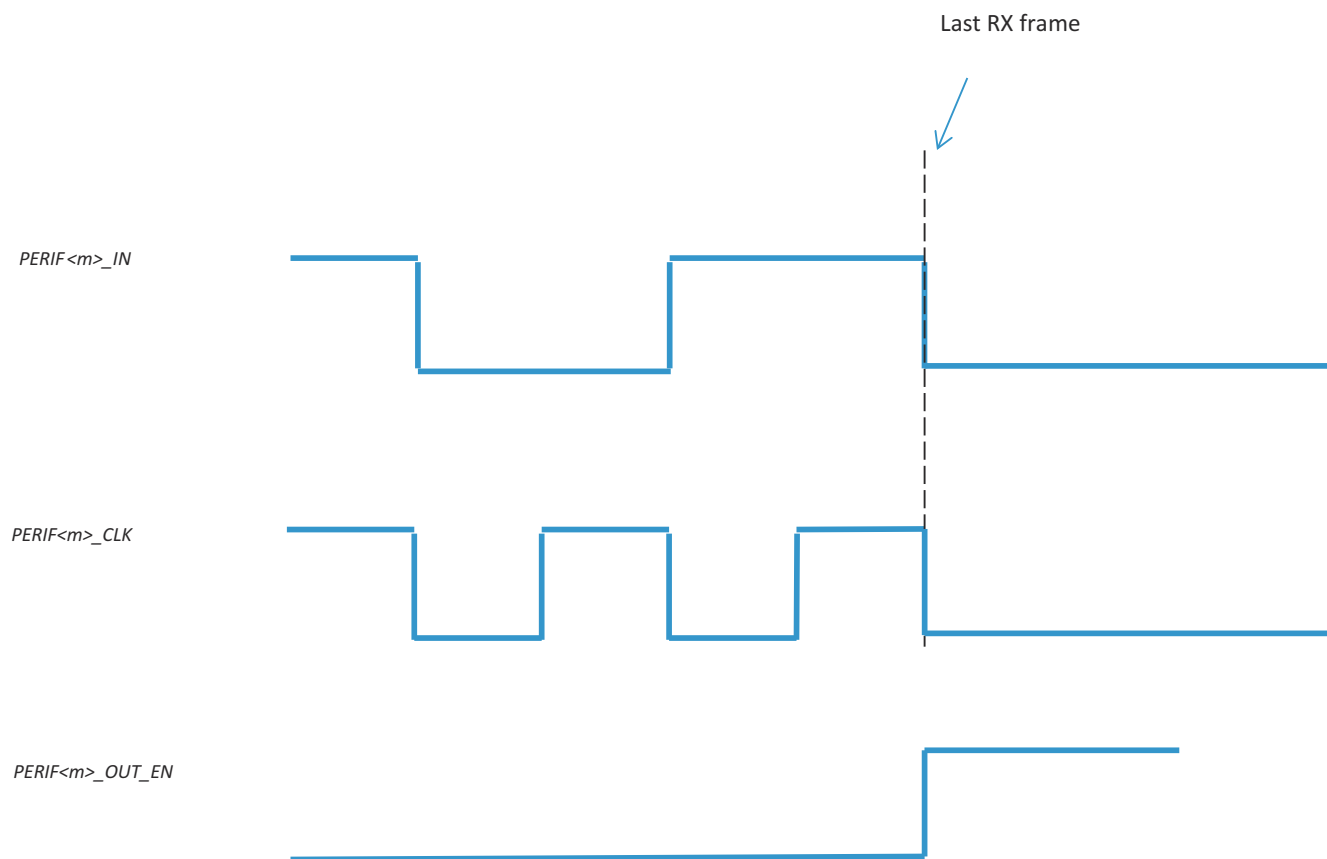


Figure 6-15. PERIF<m>_CLK Stop Low on Last RX Frame

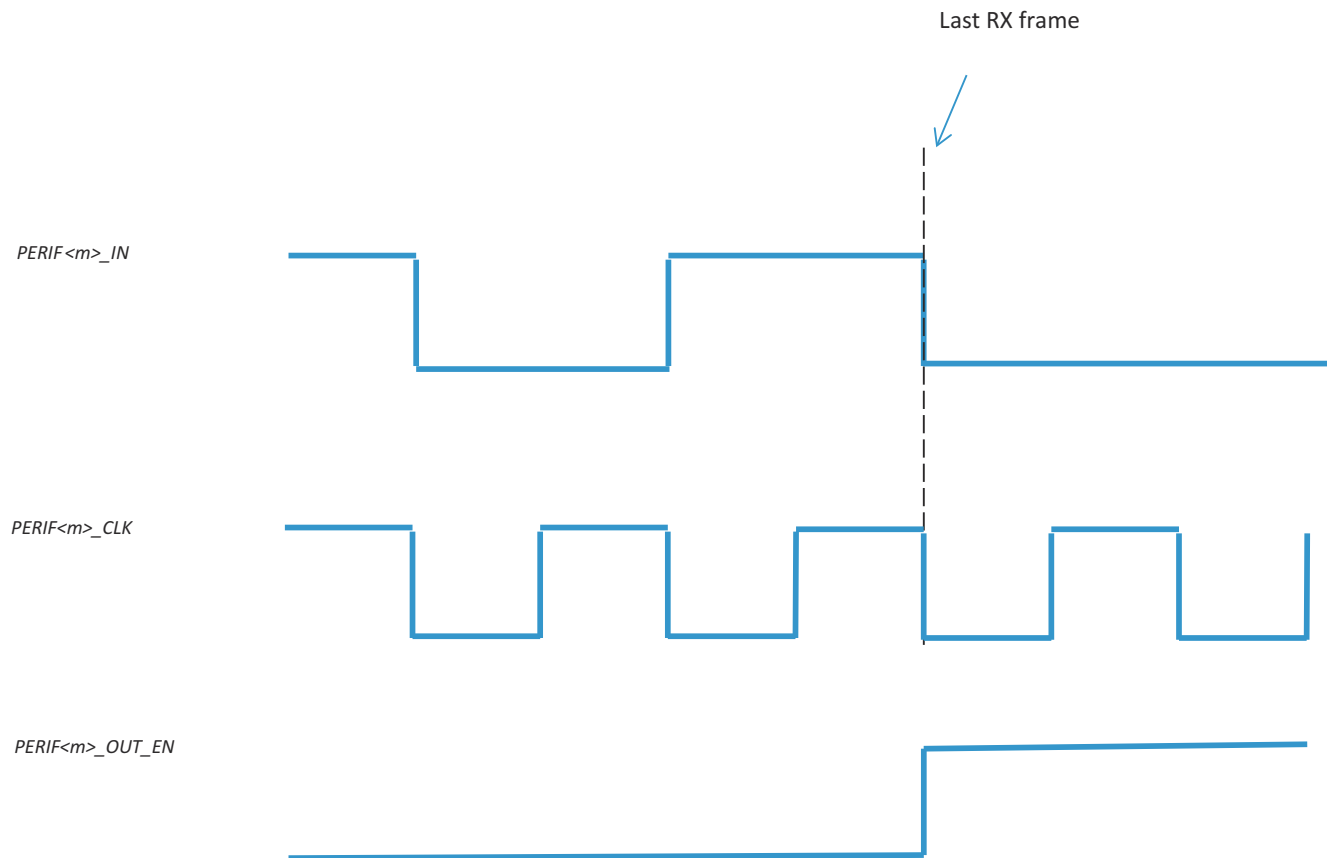


Figure 6-16. PERIF<m>_CLK Run Continuously

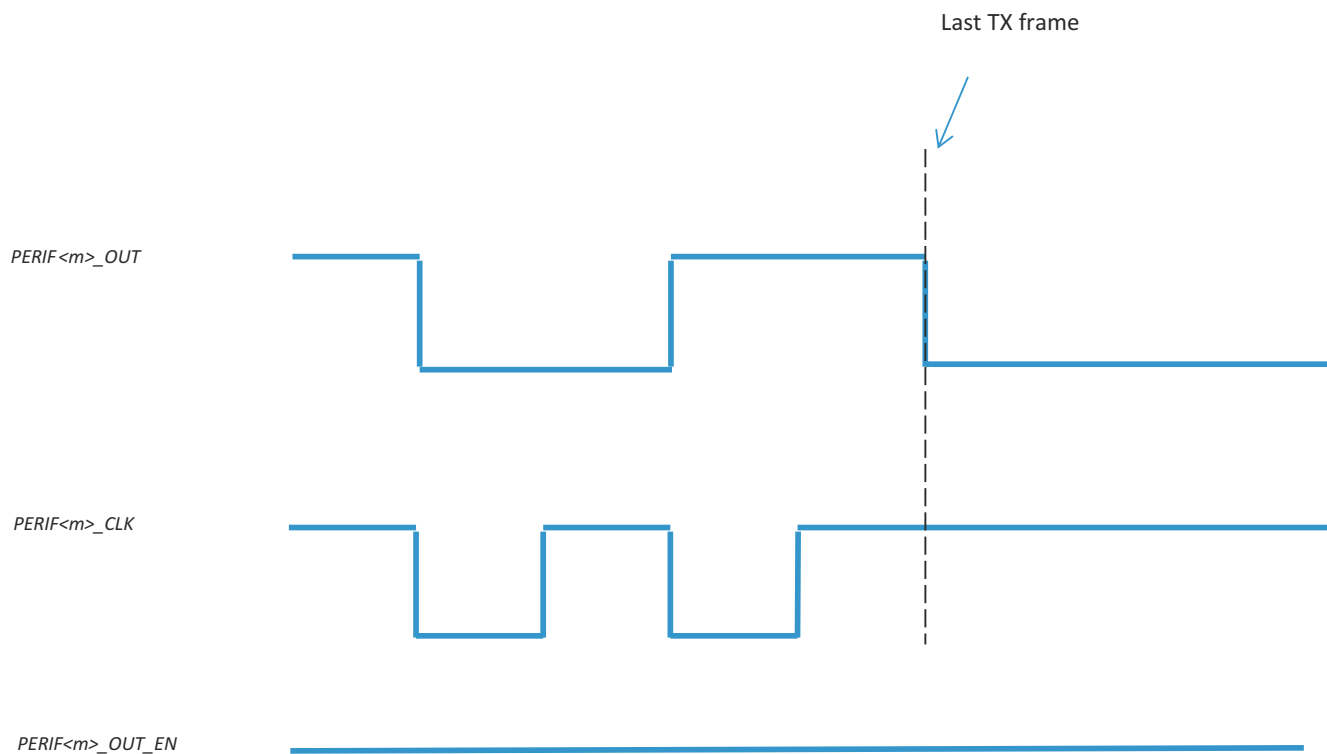


Figure 6-17. PERIF<m>_CLK Stop High on Last TX Bit

6.2.2.3.6.4 Three Peripheral Mode Basic Programming Model

The following programming models assume that the PRU is configured for 3 Peripheral Mode (ICSSG_GPCFG0_REG[29-26] PR1_PRU0_GP_MUX_SEL = 1h).

6.2.2.3.6.4.1 Clock Generation

Follow these steps to configure Peripheral I/F clocks using the HW control of the clock:

1. Select TX and RX clock sources:
 - a. ICSSG_PRU0_ED_TX_CFG_REG[4] PRU0_ED_TX_CLK_SEL for the TX clock source
 - b. ICSSG_PRU0_ED_RX_CFG_REG[4] PRU0_ED_RX_CLK_SEL for the RX clock source
2. Configure the 1x (TX) clock frequency:
 - a. Write Division Factor to ICSSG_PRU0_ED_TX_CFG_REG[31-16] PRU0_ED_TX_DIV_FACTOR
 - b. Write Fraction division factor to ICSSG_PRU0_ED_TX_CFG_REGISTER[15] PRU0_ED_TX_DIV_FACTOR_FRAC
3. Configure the oversampling (RX) frequency and oversample size:
 - a. Write Division Factor to ICSSG_PRU0_ED_RX_CFG_REG[31-16] PRU0_ED_RX_DIV_FACTOR
 - b. Write Fraction division factor to ICSSG_PRU0_ED_RX_CFG_REG[15] PRU0_ED_RX_DIV_FACTOR_FRAC
 - c. Write RX oversample size to ICSSG_PRU0_ED_RX_CFG_REG[2-0] PRU0_ED_RX_SAMPLE_SIZE
4. Select the clk_mode to configure how the PERIF<m>_CLK signal ends after TX/RX:
 - a. Write to r30[20-19] (clk_mode). Note: The clk_mode setting can also be changed per transaction.
5. Configure the wire, tst, and rx_en_counter delay values:
 - a. ICSSG_PRU0_ED_CHm_CFG0_REG[10-0] PRU0_ED_TX_WDLYm for wire delay (where n = 0 or 1 and m = 0 to 2)
 - b. ICSSG_PRU0_ED_CHm_CFG1_REG[15-0] PRU0_ED_TST_DELAY_COUNTERm for tst delay (where n = 0 or 1 and m = 0 to 2)
 - c. ICSSG_PRU0_ED_CHm_CFG1_REG[31-16] PRU0_ED_RX_EN_COUNTER for auto-delay between TX and RX (where n = 0 or 1 and m = 0 to 2)

6.2.2.3.6.4.2 TX - Single Shot

Follow these steps to configure the Peripheral I/F channel(s) for a single shot transmission:

1. (Optional) Configure TX FIFO for MSB (default) or LSB:
 - a. ICSSG_PRU0_ED_CHm_CFG0_REG[31] PRU0_ED_TX_FIFO_SWAP_BITSm (where n = 0 or 1 and m = 0 to 2)
2. Pre-load TX FIFO:
 - a. Select TX channel by writing the desired channel number to R30[17-16] (tx_ch_sel)
 - b. Write 1-4 bytes of data to r30[7-0] (tx_data). At each r30[7-0] write, data will be pushed into the FIFO.
 - c. Repeat Steps 2a and 2b for all desired channels.
3. Configure TX frame size if less than 4 full bytes loaded into FIFO:
 - a. ICSSG_PRU0_ED_CHm_CFG0_REG[15-11] PRU0_ED_TX_FRAME_SIZEEm (where n = 0 or 1 and m = 0 to 2)
4. Push TX FIFO data to PERIF<m>_OUT (see Section 6.2.2.3.6.3.2 for the PERIF<m>_CLK and PERIF<m>_OUT start time relationship);
 - a. To start TX on all channels, set r31[20] = 1 (tx_global_go).
 - b. To start TX on individual channel:
 - i. Select TX channel by writing the desired channel number to R30[17-16] (tx_ch_sel)
 - ii. Set R31[18] = 1 (tx_channel_go)
5. If ICSSG_PRU0_ED_CHm_CFG1_REG[31-16] PRU0_ED_RX_EN_COUNTERm > 0 (where n = 0 or 1 and m = 0 to 2), then the channel will automatically switch into RX mode. See Section 6.2.2.3.6.4.4 for an example of how to program and configure RX content.
6. If ICSSG_PRU0_ED_CHm_CFG1_REG[31-16] PRU0_ED_RX_EN_COUNTERm = 0, poll either r31[21, 13, or 5] (tx_global_reinit_active/busy[2,1,0]) or ICSSG_PRU0_ED_TX_CFG_REG[7, 6, or 5] PRU0_ED_BUSY_m (where m = 0 to 2, indicates channel number) for when TX is complete

Note

The PERIF<m>_CLK Peripheral I/F requires that PERIF<m>_CLK be in a high state at the beginning of a new transaction. If the clock ended the single shot transmission in low state, then the clock needs to be reset before sending more data. The steps to reset PERIF<m>_CLK are:

1. Set R31[19] = 1 (tx_global_reinit) to reset clock high
2. Wait until PRU0_ED_BUSY_m bit is cleared
3. Re-configure R30[20-19] (clk_mode), since reinit will reset the clk_mode to "Free-running/stop-high" mode

6.2.2.3.6.4.3 TX - Continuous FIFO Loading

Follow these steps to configure the Peripheral I/F channel(s) for a continuous loading transmission:

1. (Optional) Configure TX FIFO for MSB (default) or LSB:
 - a. ICSSG_PRU0_ED_CHm_CFG0_REG[31] PRU0_ED_TX_FIFO_SWAP_BITSm
2. Pre-load TX FIFO:
 - a. Select TX channel by writing the desired channel number to r30[17-16] (tx_ch_sel)
 - b. Write 1-4 bytes of data to r30[7-0] (tx_data). At each r30[7-0] write, data will be pushed into the FIFO.
 - c. Repeat Steps 2a and 2b for all desired channels.
3. Configure TX frame size to continuously transmit the TX FIFO until empty:
 - a. Set ICSSG_PRU0_ED_CHm_CFG0_REG[15-11] PRU0_ED_TX_FRAME_SIZE_m = 0h
4. Push TX FIFO data to PERIF<m>_OUT (see [Section 6.2.2.3.6.3.2](#) for the PERIF<m>_CLK and PERIF<m>_OUT start time relationship):
 - a. To start TX on all channels, set r31[20] = 1 (tx_global_go).
 - b. To start TX on individual channel:
 - i. Select TX channel by writing the desired channel number to r30[17-16] (tx_ch_sel)
 - ii. Set r31[18] = 1 (tx_channel_go)
5. Monitor line rate and reload FIFO:
 - a. Polling r31[xx, 12-10, 4-2] (tx_fifo_sts<m>)
 - b. When FIFO level is at 2 bytes, load next 2 bytes of data (see Step 2). Do not let the FIFO get close to 0. Once the FIFO runs empty, the hardware will assume the PRU has reached end of the last transmit. Any new writes to the FIFO will NOT be sent until the software sends another tx_channel_go bit. Note: There are also underrun and overrun error flags that can be monitored.
6. To end TX operation, do not send any new data to FIFO.
 - a. If ICSSG_PRU0_ED_CHm_CFG1_REG[31-16] PRU0_ED_RX_EN_COUNTER_m > 0 (where n = 0 or 1 and m = 0 to 2), then the channel will automatically switch into RX mode. See [Section 6.2.2.3.6.4.4](#) for an example of how to program and configure RX content.
 - b. If ICSSG_PRU0_ED_CHm_CFG1_REG[31-16] PRU0_ED_RX_EN_COUNTER_m = 0, poll either r31[21, 13, or 5] (tx_global_reinit_active/busy[2,1,0]) or ICSSG_PRU0_ED_TX_CFG_REG[7, 6, or 5] PRU0_ED_BUSY_m (where m = 0 to 2, indicates channel number) for when TX is complete

Note

The PERIF<m>_CLK Peripheral I/F requires that PERIF<m>_CLK be in a high state at the beginning of a new transaction. If the clock ended the continuous loading transmission in low state, then the clock needs to be reset before sending more data. The steps to reset PERIF<m>_CLK are:

1. Set R31[19] = 1 (tx_global_reinit) to reset clock high
2. Wait until PRU0_ED_BUSY_m is cleared
3. Re-configure R30[20-19] (clk_mode), since reinit will reset the clk_mode to "Free-running/stop-high" mode

6.2.2.3.6.4.4 RX - Auto Arm or Non-Auto Arm

Follow these steps to configure the Peripheral I/F channel(s) to receive data:

1. Configure RX and frame size:

- a. ICSSG_PRU0_ED_CHm_CFG0_REG[27-16] PRU0_ED_RX_FRAME_SIZE_m (where n = 0 or 1 and m = 0 to 2)
2. Configure start bit polarity:
 - a. ICSSG_PRU0_ED_RX_CFG_REG[3] RX_SB_POL (PRU0 or PRU1)
 - b. For the non-auto arm use case, set r30[26, 25, 24] = 1 (rx_en<m>)
 - c. For the auto arm use case, rx_en<m> will be automatically enabled at the end of a TX operation when ICSSG_PRU0_ED_CHm_CFG1_REG[31-16] PRU0_ED_RX_EN_COUNTER_m > 0 (where n = 0 or 1 and m = 0 to 2)
3. RX FIFO will start filling on the first start bit (PERIF<m>_IN = 1). The data will be captured on the positive edge of the PERIF<m>_CLK and shifted into the LSB position of the 8-bit shadow register.
4. Poll for r31[26, 25, 24] (val<m>) assertion. The valid flag will be asserted when n bits of data (determined by ICSSG_PRU0_ED_RX_CFG_REG[2-0] PRU0_ED_RX_SAMPLE_SIZE) have been collected.
5. Fetch data by reading r31[23-16, 15-8, 7-0] (rx_data_out<m>). The data will remain constant for one data frame, and PRU must read data and clear valid flag within this time. Otherwise, an overflow will occur – r31[29, 28, 27] (ovf<m>) = 1 - indicating that val<m> has been continuously asserted for longer than one data frame.
6. The clock will be stopped based on the r30[20-19] (clk_mode) configured before the start of the RX operation.
7. Clear r30[26, 25, 24] (rx_en<m>) to disable RX mode. All counters and flags will be reset.

6.3 PRU_ICSSG RAM Index Allocation

The PRU_ICSSG module includes integrated ECC Aggregator module to test ECC functionality.

Table 6-20 shows the mapping of the RAM IDs to the ECC RAMs serviced by the ECC Aggregator.

Table 6-20. Mapping of the RAM IDs to the ECC RAMs

RAM Index	ECC RAM Prefix	Description
0	pr<k>_dram0	Data RAM0 (8KB)
1	pr<k>_dram1	Data RAM1 (8KB)
2	pr<k>_pru0_iram	PRU0 Instruction Memory (12KB)
3	pr<k>_pru1_iram	PRU1 Instruction Memory (12KB)
4	pr<k>_ram	Shared Data RAM2 (64KB)
5	pr<k>_rtu0_iram	RTU0 Instruction Memory (8KB)
6	pr<k>_rtu1_iram	RTU1 Instruction Memory (8KB)
7	pr<k>_tx_pru0_iram	TX_PRU0 Instruction Memory (6KB)
8	pr<k>_tx_pru1_iram	TX_PRU1 Instruction Memory (6KB)

7 PRU_ICSSG Broadside Accelerators

7.1 PRU_ICSSG Broadside Accelerators Overview

The PRU_ICSSG supports a broadside interface, which uses the XFR (XIN, XOUT, or XCHG) instruction to transfer the contents of PRUn, RTU_PRUn or TX_PRUn (where n = 0 or 1) registers to or from accelerators. This interface enables up to 31 registers (R0-R30, or 124 bytes) to be transferred in a single instruction. This section details the various accelerators that are available to the PRUn and/or RTU_PRUn and TX_PRUn through the broadside interface.

Each of those functions have a unique XIN ID to determine which operation will occur. For more information see [Table 5-1](#).

7.2 PRU_ICSSG Data Processing Accelerators Functional

7.2.1 PRU Multiplier with Accumulation (MPY/MAC)

This section describes the MAC (multiplier with accumulation) module integrated to PRU0/PRU1 cores, RTU_PRU0/RTU_PRU1 auxiliary cores and TX_PRU0/TX_PRU1 cores of PRU_ICSSGn (or CFG1, PRU1).

Each of the six PRU cores (PRU0/PRU1, RTU_PRU0/RTU_PRU1 auxiliary cores and TX_PRU0/TX_PRU1 transmit cores) has a designated unsigned multiplier with accumulation (MPY/MAC). The MAC supports two modes of operation: Multiply Only and Multiply and Accumulate.

The MAC is directly connected with the PRU internal registers R25-R29 and uses the broadside load/store PRU interface and XFR instructions to both control and mode of the MAC and import the multiplication results into the PRU.

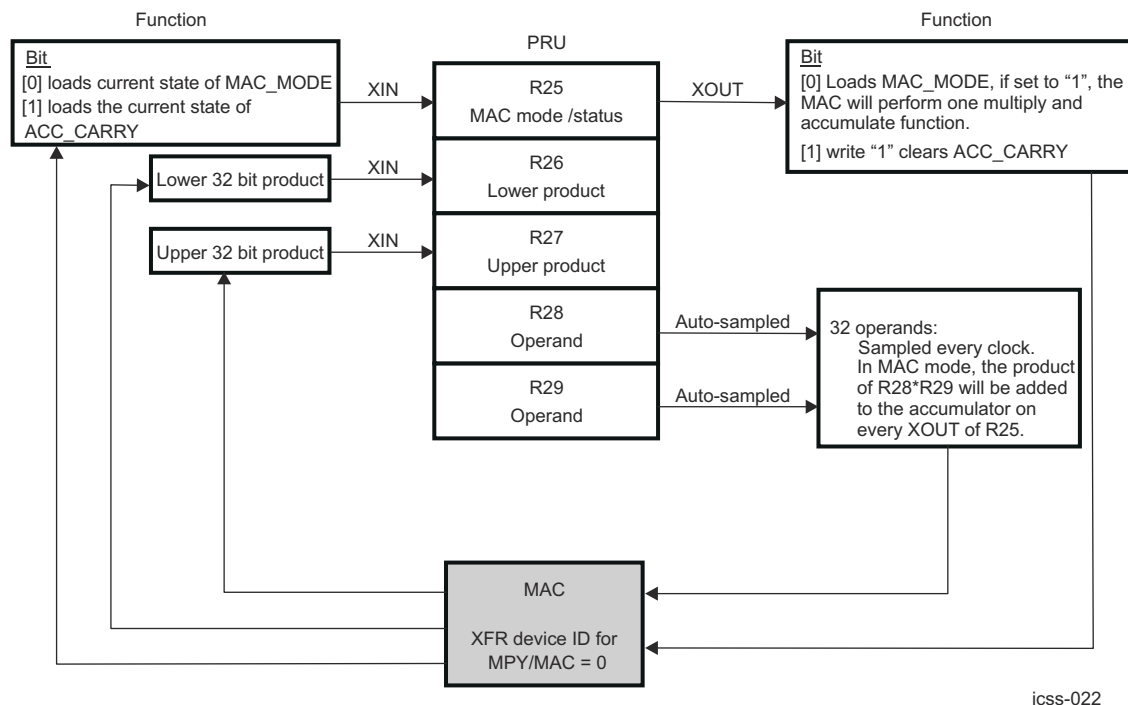
The PRU MPY/MAC features are:

- Configurable Multiply Only and Multiply and Accumulate functionality via PRU register R25
- 32-bit operands with direct connection to PRU registers R28 and R29
- 64-bit result (with carry flag) with direct connection to PRU registers R26 and R27
- One clock cycle per operation
- PRU broadside interface and XFR instructions (XIN, XOUT) allow for importing multiplication results and initiating accumulate function

7.2.1.1 PRU MAC Operations

7.2.1.1.1 PRU versus MAC Interface

The MAC directly connects with the PRU internal registers R25-R29 through use of the PRU broadside interface and XFR instructions. [Figure 7-1](#) shows the functionality of each register.



icss-022

Figure 7-1. Integration of the PRU and MPY/MAC

The XFR instructions (XIN and XOUT) are used to load/store register contents between the PRU core and the MAC. These instructions define the start, size, direction of the operation, and device ID. The device ID number corresponding to the MPY/MAC is shown in [Table 7-1](#).

Table 7-1. MPY/MAC XFR ID

Device ID	Function
0	Selects MPY/MAC

The PRU register R25 is mapped to the MAC_CTRL_STATUS register ([Table 7-2](#)). The MAC's current status (MAC_MODE and ACC_CARRY states) is loaded into R25 using the XIN command on R25. The PRU sets the MAC's mode and clears the ACC_CARRY using the XOUT command on R25.

Table 7-2. MAC_CTRL_STATUS Register (R25) Field Descriptions

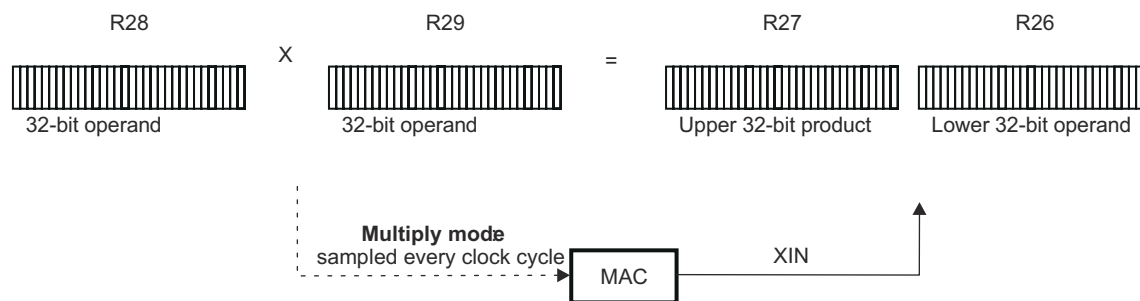
Bit	Field	Description
7-2	RESERVED	Reserved
1	ACC_CARRY	Write 1 to clear. It is sticky. It is set 0 cycles after the event. 0h: 64-bit accumulator carry has not occurred 1h: 64-bit accumulator carry occurred
0	MAC_MODE	0h: Accumulation mode disabled and accumulator is cleared 1h: Accumulation mode enabled

The two 32-bit operands for the multiplication are loaded into R28 and R29. These registers have a direction connection with the MAC. Therefore, XOUT is not required to load the MAC. In multiply mode, the MAC samples these registers every clock cycle. In multiply and accumulate mode, the MAC samples these registers every XOUT R25[7-0] transaction when MAC_MODE = 1.

The product from the MAC is linked to R26 (lower 32 bits) and R27 (upper 32 bits). The product is loaded into register R26 and R27 using XIN.

7.2.1.1.2 Multiply only mode(default state), MAC_MODE = 0

The [Figure 7-2](#) summarizes the MAC operation in "Multiply-only" mode, in which the MAC multiplies the contents of R28 and R29 on every clock cycle.



icss-023

Figure 7-2. MAC Multiply-only Mode- Functional Diagram

7.2.1.1.2.1 Programming PRU MAC in "Multiply-ONLY" mode

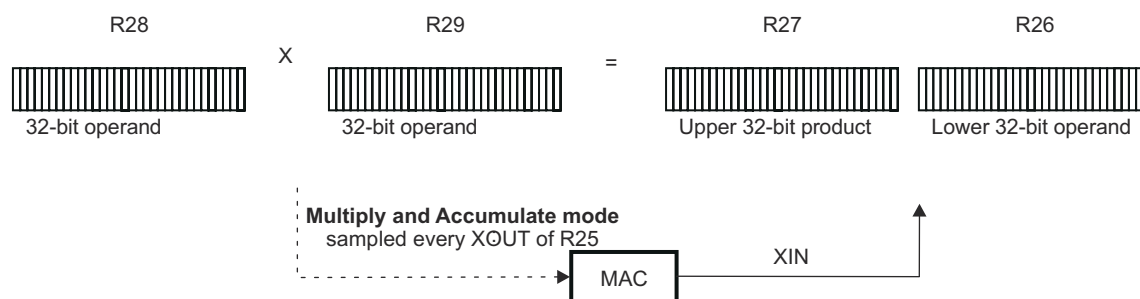
The following steps are performed by the PRU firmware for multiply-only mode:

1. 1. Enable multiply only MAC_MODE.
 - a. (a) Clear R25[0] for multiply only mode.
 - b. (b) Store MAC_MODE to MAC using XOUT instruction with the following parameters:
 - Device ID = 0
 - Base register = R25
 - Size = 1
2. 2. Load operands into R28 and R29.
3. 3. Delay at least 1 PRU cycle before executing XIN in step 4.
4. 4. Load product into PRU using XIN instruction on R26, R27.

Repeat steps 2 and 4 for each new operand.

7.2.1.1.3 Multiply and Accumulate Mode, MAC_MODE = 1

The [Figure 7-3](#) summarizes the MAC operation in "Multiply and Accumulate" mode. On every XOUT R25_REG[7-0] transaction, the MAC multiplies the contents of R28 and R29, adds the product to its accumulated result, and sets ACC_CARRY if an accumulation overflow occurs.



icss-024

Figure 7-3. MAC Multiply and Accumulate Mode Functional Diagram

7.2.1.1.3.1 Programming PRU MAC in Multiply and Accumulate Mode

The following steps are performed by the PRU firmware for multiply and accumulate mode:

1. Enable multiply and accumulate MAC_MODE.
 - (a) Set R25[1-0] = 1 for accumulate mode.
 - (b) Store MAC_MODE to MAC using XOUT instruction with the following parameters:

- Device ID = 0
 - Base register = R25
 - Size = 1
2. Clear accumulator and carry flag.
 - (a) Set R25[1-0] = 2 to clear carry flag (R25[1]=1) and clear accumulator (R25[0]=0).
 - (b) Store accumulator to MAC using XOUT instruction on R25.
 3. Load operands into R28 and R29.
 4. Multiply and accumulate, XOUT R25[1-0] = 1
- Repeat step 4 for each multiply and accumulate using same operands.
- Repeat step 3 and 4 for each multiply and accumulate for new operands.
5. Load the accumulated product into R26, R27, and the ACC_CARRY status into R25 using the XIN instruction.
- 1.

Note

Steps one and two are required to set the accumulator mode and clear the accumulator and carry flag.

7.2.2 PRU CRC16/32 Module

Each of the PRU0/PRU1 cores, RTU_PRU0/RTU_PRU1 auxiliary cores and TX_PRU0/TX_PRU1 transmit cores have a designated CRC16/32 module.

In general, CRC adds error detection capability to communication systems. The CRC encoder appends redundant bits (or CRC bits) to the systematic data message. During reception of the data message, the received data is also encoded with the same CRC encoder. The 2 sets of CRC bits are compared together. If they match, there were no transmission errors; and if they don't match, a transmission error has been detected.

CRC16/32 supports the following features:

- Supports CRC32:
 - $x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^8+x^7+x^5+x^4+x^2+x+1$
- Supports CRC16:
 - $x^{16}+x^{15}+x^2+1$
- Supports CRC16 - CCITT:
 - $x^{16}+x^{12}+x^5+1$
- PRU broadside interface and XFR instructions (XIN, XOUT) allow for importing CRC results and executing accumulate function

7.2.2.1 PRU and CRC16/32 Interface

The CRC16/32 module directly connects with the PRU internal registers R25-R29 through use of the PRU broadside interface and XFR instructions. [Table 7-3](#) shows the functionality of each register.

The XFR instructions (XIN/XOUT/XCHG) are used to load/store register contents between the PRU core and the CRC16/32 module. These instructions define the start, size, direction of the operation, and device ID. The XFR device ID number corresponding to the CRC16/32 module is 1.

Table 7-3. CRC Register to PRU Port Mapping

CRC Register	R/W	Description	PRU Mapping
CRC_CFG	W	Always write all 4 bytes. bit [0] CRC32_ENABLE: 0: CRC16 mode is selected. Hardware will auto-set init state of CRC_SEED to 0000_0000h. However, for CRC16-CCITT software will need to write the init state of FFFF_FFFFh to CRC_SEED. Note: The CRC16 result value is only 16-bits. 1: CRC32 mode is selected. Hardware will auto-set init state of CRC_SEED will be FFFF_FFFFh. bit [1] CRC_32B_NOT_EMPTY: 0: CRC 32Byte buffer is empty 1: CRC 32Byte buffer is not empty bit [2] CRC16_MOD_ENABLE: 0: CRC16 ($x^{16}+x^{15}+x^2+1$) 1: CRC16-CCITT ($x^{16}+x^{12}+x^5+1$) - Note: CRC32_ENABLE field must = 0.	R25
CRC_DATA_8_BFLIP	R	8-bit flip of CRC_DATA. CRC_DATA_8_BFLIP has the same byte order as CRC_DATA[31-0], but each byte has all bits flipped. CRC_DATA_32_FLIP[7-0] = CRC_DATA[0-7] CRC_DATA_32_FLIP[15-8] = CRC_DATA[8-15] CRC_DATA_32_FLIP[23-16] = CRC_DATA[16-23] CRC_DATA_32_FLIP[31-24] = CRC_DATA[24-31] For CRC16, only CRC_DATA_8_BFLIP[15-0] are valid. No auto reset on CRC_DATA_8_BFLIP read.	R27
CRC_SEED	W	CRC SEED value. Hardware will auto-initialize the CRC_SEED value to 0000_0000h for CRC16 and FFFF_FFFFh for CRC32. Software only needs to initialize CRC_SEED if a different default value is required. For CRC16-CCITT, software needs to update initial CRC_SEED value to FFFF_FFFFh. Always write 4 bytes. Note: Reading the CRC_DATA register will reset the CRC value to the CRC_SEED state.	R28

Table 7-3. CRC Register to PRU Port Mapping (continued)

CRC Register	R/W	Description	PRU Mapping
CRC_DATA_32_BFLIP	R	Full 32-bit flip of CRC_DATA CRC_DATA_32_BFLIP[0] = CRC_DATA[31] ... CRC_DATA_32_BFLIP[31] = CRC_DATA[0] For CRC16, only CRC_DATA_32_BFLIP[31-16] are valid. No auto reset on CRC_DATA_32_BFLIP read.	R28
CRC_DATA	RW	For Write, must use a fixed width throughout the session. The CRC module supports lower 8-bit, or lower 16-bit, or full 32-bit data widths. For Read, LSB or CRC_DATA[0] is first bit on the wire. For Read, reset the CRC_DATA back to CRC_SEED state. Note: Firmware must add 1 to 2 NOPs after the last XOUT to the XIN. For CRC16, only CRC_DATA[15-0] is valid.	R29

7.2.2.2 CRC Programming Model

The following steps are performed by the PRU firmware to use the CRC module:

Step1: Configuration (optional)

- Configure CRC type:
For CRC32 operation, set CRC32_ENABLE using XOUT instruction with the following parameters:
 - Device ID = 1
 - Base register = R25
 - Size = 1
- Update CRC_SEED, if required using XOUT with the following parameters:
 - Device ID = 1
 - Base register = R28
 - Size = 1 to 4

Step 2:

- Load new CRC data into R29
- Push CRC data to the CRC16/32 module using XOUT with the following parameters:
 - Device ID = 1
 - Base register = R29
 - Size = 1 to 4
- 1 or 2 NOPS
- Load the accumulated CRC result into the PRU using the XIN instruction with the following parameters:
 - Device ID = 1
 - Base register = R29
 - Size = 4

Repeat Step 2, numbers 1 and 2 for each new CRC data.

Note

When a session starts, the PRU firmware must use the same write data width throughout the session.

7.2.2.3 PRU and CRC16/32 Interface (R9:R2)

The PRU_ICSSG system implements a new wide 32-Bytes data path. The firmware can perform one XOUT of 32-Bytes, the hardware will feed the CRC16/32 4-Bytes at a time. This will take 20 clock cycles for CRC16 and 12 clock cycles for CRC32 for a 32-Bytes XOUT.

Table 7-4. PRU Register to XFR Mapping

PRU Register	XFR ID	Domain/Function	Description
R9:R2 Data	1	Data	XOUT Only 1-Byte to 32-Bytes in size LSB packed and no gaps, for example: 32-Bytes push R9:R2

Table 7-4. PRU Register to XFR Mapping (continued)

PRU Register	XFR ID	Domain/Function	Description
			16-Bytes push R5:R2
			4-Bytes push R2
			7-Bytes push R3(b2.b0):R2
			1-Bytes push R2(b0)

7.2.3 PRU_ICSSG Scratch Pad Memory

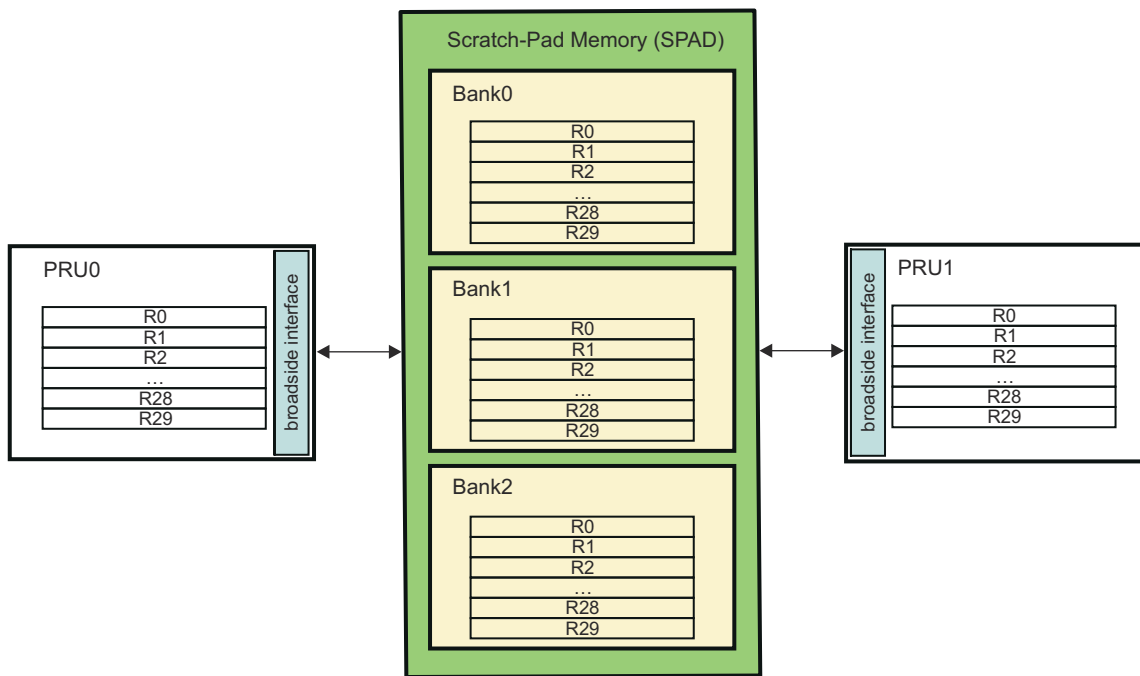
The PRU_ICSSG supports a scratch pad with up to four independent banks accessible by the PRU cores and two independent banks accessible by the RTU_PRU cores. The TX_PRU cores have a separate scratch pad memory with two independent banks. The PRU, RTU_PRU and TX_PRU cores interact with the scratch pad through broadside load/store PRU interface and XFR instructions. The scratch pad can be used as a temporary place holder for the register contents of the PRU, RTU_PRU or TX_PRU cores.

7.2.3.1 PRU0/1 Scratch Pad Overview

The PRU_ICSSG scratch pad supports the following features:

- PRU0 and PRU1 cores have three Scratch Pad banks of 30, 32-bit registers (R29 to R0)
- RTU_PRU0 and RTU_PRU1 auxiliary cores have three Scratch Pad banks of 30, 32-bit registers (R29 to R0)
- TX_PRU0 transmit core has one Scratch Pad bank of 30, 32-bit registers (R29 to R0)
- TX_PRU1 transmit core has one Scratch Pad bank of 30, 32-bit registers (R29 to R0)
- Flexible load/store options:
 - Load/store one byte of R<n> or load/store (R29 to R0) to Bank0, Bank1, Bank2 or Bank3
 - User-defined start byte and length of the transfer
 - Length of transfer ranges from one byte of a register to the entire register content (R29 to R0)
 - Simultaneous transaction supported between PRU0 <-> Bank<n> and PRU1 <-> Bank<m>
- XFR (XIN/XOUT/XCHG) instructions operate in one clock cycle
- Optional XIN/XOUT shift functionality allows remapping of registers (R<n> -> R<m>) during load store operation

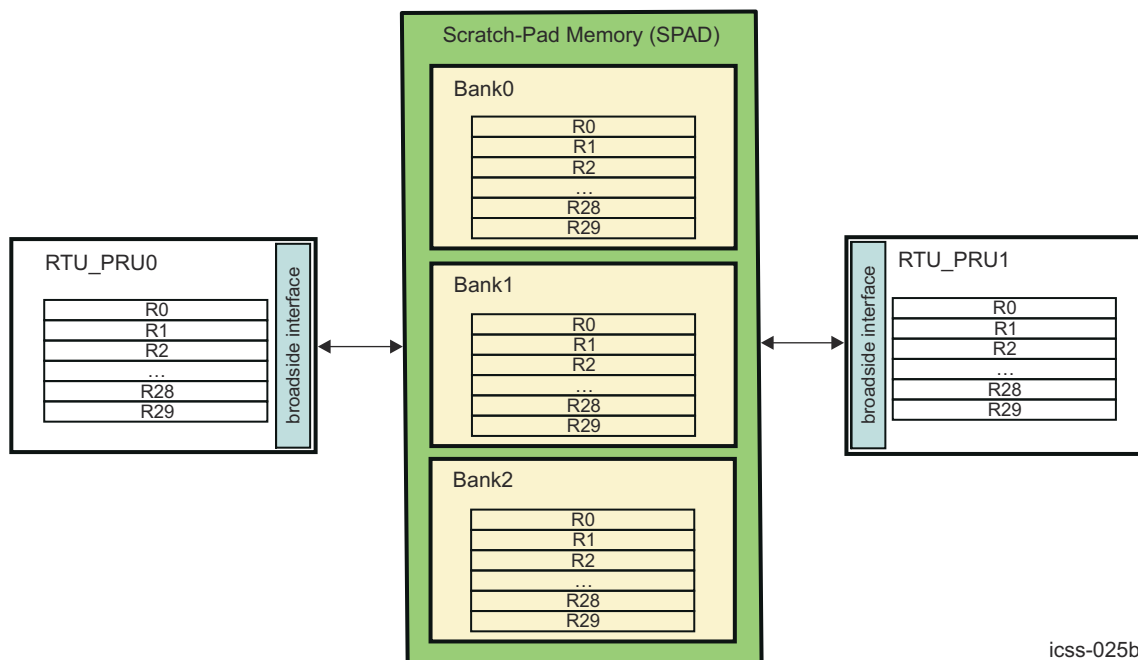
Figure 7-4 shows a simplified model of the Scratch Pad and PRU cores integration.



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Figure 7-4. Scratch Pad and PRU Integration

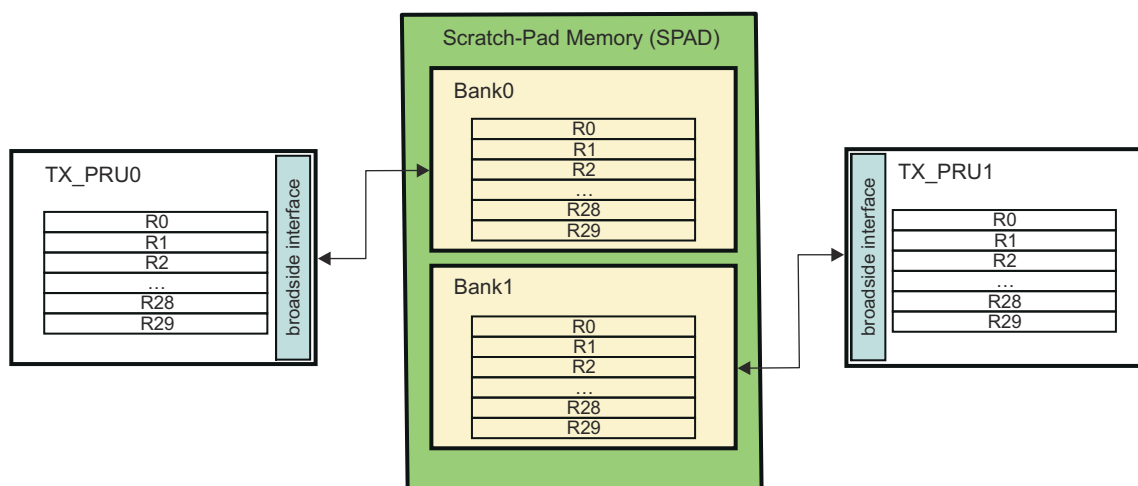
Figure 7-5 shows a simplified model of the Scratch Pad and RTU_PRU cores integration.



icss-025b

Figure 7-5. Scratch Pad and RTU_PRU Integration

Figure 7-6 shows a simplified model of the Scratch Pad and TX_PRU cores integration.



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Figure 7-6. Scratch Pad and TX_PRU Integration

7.2.3.2 PRU0 /1 Scratch Pad Operations

XFR instructions are used to load/store register contents between the PRU cores and the scratch pad banks. These instructions define the start, size, direction of the operation, and device ID. The device ID corresponds to the external source or destination (either a scratch pad bank or the other PRU core). The device ID numbers are shown in [Table 7-5](#).

Table 7-5. Scratch Pad XFR ID

Device ID	Function/Operation
10	Selects Bank0
11	Selects Bank1
12	Selects Bank2

A collision occurs when two XOUT commands simultaneously access the same asset or device ID. [Table 7-6](#) shows the priority assigned to each operation when a collision occurs.

Table 7-6. Scratch Pad XFR Collision and Stall Conditions

Operation	Collision and Stall Handling
PRU<n> XOUT (->) bank[j]	If both PRU cores access the same bank simultaneously, PRU0 is given priority. PRU1 will temporarily stall until the PRU0 operation completes.
RTU_PRU<n> XOUT (->) bank[j]	If both RTU_PRU cores access the same bank simultaneously, RTU_PRU0 is given priority. RTU_PRU1 will temporarily stall until the RTU_PRU0 operation completes.

7.2.3.2.1 Optional XIN/XOUT Shift

The optional XIN/XOUT shift functionality allows register contents to be remapped or shifted within the destination's register space. For example, the contents of PRU0 R6-R8 could be remapped to Bank1 R10-12.

The shift feature is enabled or disabled through the PRU subsystem level register [ICSSG_SPP_REG](#)[1] XFR_SHIFT_EN bit. When enabled, R0[4-0] (internal to the PRU) defines the number of 32-bit registers in which content is shifted in the scratch pad bank. Note that scratch pad banks do not have registers R30 or R31.

7.2.3.2.2 Scratch Pad Operations Examples

The following PRU firmware examples demonstrate the shift functionality. Note: These assume the XFR_SHIFT_EN bit of the [ICSSG_SPP_REG](#) register of the PRU_ICSSG CFG register space has been set.

XOUT Shift By 4 Registers

Store R4:R7 to R8:R11 in Bank0:

- Load 4 into R0.b0
- XOUT using the following parameters:
 - Device ID = 10
 - Base register = R4
 - Size = 16

XOUT Shift By 9 Registers, With Wrap Around

Store R25:R29 to R4:R9 in Bank1:

- Load 9 into R0.b0
- XOUT using the following parameters:
 - Device ID = 11
 - Base register = R25
 - Size = 20

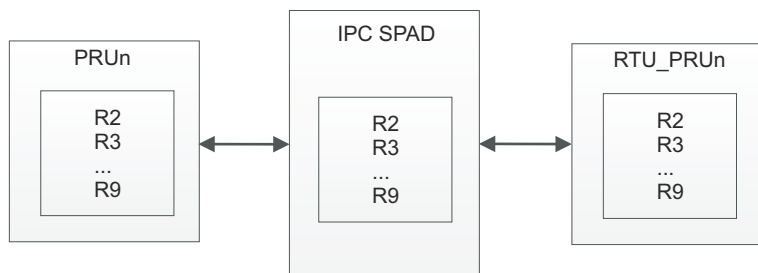
XIN Shift By 10 Registers

Load R14:R16 from Bank2 to R4:R6:

- Load 10 into R0.b0
- XIN using the following parameters:
 - Device ID = 12
 - Base register = R4
 - Size = 12

7.2.4 PRU_ICSSG IPC Scratch Pad Memory

The IPC module is a 32 Byte wide Scratch Pad that connects together PRUn and RTU_PRUn (where n = 0 or 1) cores within a Slice. [Figure 7-7](#) represents the mapping between IPC Scratch Pad (IPC SPAD), PRUn and RTU_PRUn cores..



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Figure 7-7. Integration of the PRU and IPC Scratch Pad

The firmware needs to define which bytes are owned by each of the PRUn/RTU_PRUn cores. There is no hardware arbitration.

Table 7-7. IPC Scratch Pad XFR ID

Register	Device ID	Domain/ Function	Description
R9:R2 Data	15	IPC[255:0]	32 byte wide register bank

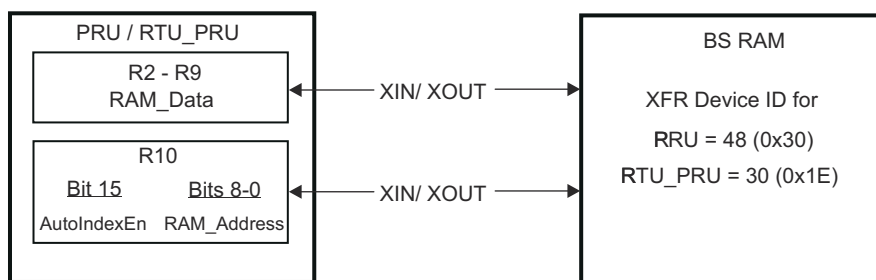
7.2.5 PRU_ICSSG Broadside (BS) RAM

Each PRU core (PRU0 or PRU1) has a dedicated 2KB Broadside (BS) RAM, which is attached to the core. Each of the auxiliary RTU_PRU cores (RTU_PRU0 or RTU_PRU1) have a dedicated 2KB Broadside (BS) RAM. Each of the auxiliary TX_PRU cores (TX_PRU0 or TX_PRU1) have a dedicated 2KB Broadside (BS) RAM.

The BS RAM directly connects with the PRU internal register R2-R10 through use of the PRU broadside interface and XFR instructions. Figure 7-8 shows the functionality of each register.

There are two modes of operation for the PRU to interact with the BS RAM:

1. BS RAM only (shown in Figure 7-8)
2. BS RAM + SUM32 snoop (described in Section 7.2.6)



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Figure 7-8. Integration of the PRU and BS RAM

The XFR instructions (XIN and XOUT) are used to load/store register contents between the PRU/ RTU_PRU core and the BS RAM. These instructions define the start, size, direction of the operation, and device ID. The device ID number corresponding to the BS RAM is shown in Table 7-8.

Table 7-8. BS RAM XFR ID

	Device ID	Function
BS RAM only mode	48 (30h)	PRU
The following IDs can be used to read/write the following registers to the BS RAM:	48 (30h)	TX_PRU
• RAM Data (R2:R9)		
• AutoIndexEn and BS_RAM_Address (R10)	30 (1Eh)	RTU_PRU
Note that R10 must be treated as a 2 byte write.		
BS RAM + SUM32 snoop mode	49 (31h)	PRU
The following IDs can be used to write (only) the following registers to the BS RAM and SUM32 module.		
This mode requires a 32 Byte write.	38 (26h)	RTU_PRU
• RAM Data (R2:R9)		
R12:R10	48 (30h)	PRU
Last 12 Bytes of RX	30 (1Eh)	RTU_PRU

A description of the PRU register R10's functionality is shown in Table 7-9. Note that the firmware must do a 2 byte write of R10[15:0] when transmitting the content of this register to the BS RAM.

Table 7-9. Register (R10) Field Descriptions

Bit	Field	Description
15	AutoIndexEn	RAM Auto Increment the Index Enable 0h: Disable Auto Increment 1h: Enable Auto Increment When enabled, each PRU or RTU_PRU core's write or read to the BS RAM will cause the RAM_Address to increment by 1. Note: Each increment of the RAM_Address is the equivalent of 32 Bytes. The next read or write address will always be 32 Bytes later, regardless of the read or write data size. Rollovers of RAM_Address are not supported. Firmware must reset RAM_Address to zero. This mode must be set before RAM Data transaction.
8-0	RAM_Address	Index for PRU core Read/Write access of the RAM. Index is direct mapping to the 16KB RAM. Note: Max width is 256-bits or 32Bytes. 0h: 1st 32 Bytes 1h: 2nd 32 Bytes Note: For reading data, can be executed XOUT RAM_Address, XIN RAM_Data

7.2.5.1 Programming the BS RAM

The following steps are performed by the PRU firmware to write to the BS RAM:

1. Configure RAM_Address and AutoIndexEn
 - a. Load RAM_Address and AutoIndexEn into R10
 - b. Store RAM_Address and AutoIndexEn to BS RAM using XOUT instruction with the following parameters:
 - Device ID = 30h (PRU) or 1Eh (RTU_PRU)
 - Base register = R10
 - Size = 2
2. Write Data to BS RAM
 - a. Load Data to be written into R2-R9
 - b. Store Data to BS RAM using XOUT instruction with the following parameters:
 - Device ID = See [Table 7-8](#), ID depends on mode.
 - Base register = Register with start of data (R2-R10)
 - Size = Data size (number of bytes)
3. If AutoIndexEn = 1h, repeat Step 2 to write additional data.
4. If AutoIndexEn = 0h,
 - a. Load new address into R10
 - b. Repeat Step 1b
 - c. Repeat Step 2

The following steps are performed by the PRU firmware to read to the BS RAM:

1. Configure RAM_Address and AutoIndexEn
 - a. Load RAM_Address and AutoIndexEn into R10
 - b. Store RAM_Address and AutoIndexEn to BS RAM using XOUT instruction with the following parameters:
 - Device ID = 30h (PRU) or 1Eh (RTU_PRU)
 - Base register = R10
 - Size = 2
2. Read Data from BS RAM
 - a. Load Data to be written into R2-R9
 - b. Load Data to PRU/ RTU_PRU BS RAM using XIN instruction with the following parameters:
 - Device ID = See [Table 7-8](#), ID depends on mode.

- Base register = Register destination for start of data (R2-R10)
 - Size = Data size (number of bytes)
3. If AutoIndexEn = 1h, repeat Step 2 to read additional data.
 4. If AutoIndexEn = 0,
 - a. Load new address into R10
 - b. Repeat Step 1b
 - c. Repeat Step 2

7.2.6 PRU_ICSSG SUM32 Hardware Accelerator

The SUM32 module is a simple hardware accelerator which is used to help generate UDP checksum (User Datagram Protocol) for data integrity. The operation takes 2 clock cycles, read pipe is another 1 clock cycle. The operation is pipelined. The PRUn or RTU_PRUn core (where n = 0 or 1) will not see any hardware backpressure for back to back XOUT 32 Byte operations. The PRU or RTU_PRU core can see up to 2 cycle stall if there is no time between the last XOUT and the XIN to get the SUM value. The FW must insure you have 3 NOPs or 3 clock cycle delay between the last XOUT to the XIN to get the correct SUM value. The XIN operation self clears the SUM.

Figure 7-9 shows the SUM32 module integration. Each PRUn core (where n = 0 or 1) has a dedicated SUM32 module, used to snoop or continuously monitor the Broadside (BS) RAM and facilitate software to detect a UDP Checksum error. There are also two SUM32 modules attached to each auxiliary PRU core (RTU_PRU0 and RTU_PRU1).

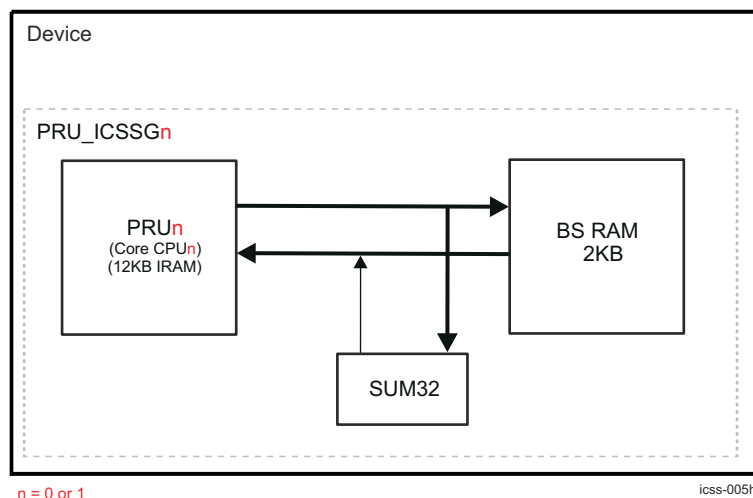


Figure 7-9. SUM32 Integration

Note that there are two modes of operation for the PRU to interact with the SUM32:

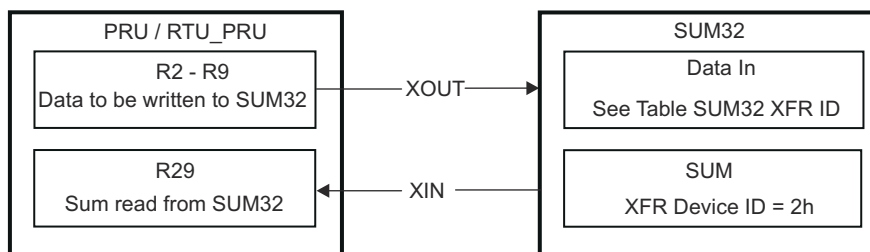
1. BS RAM + SUM32 snoop
2. SUM32 only

The Device ID for each mode is shown in Table 7-10. An XOUT with the BS RAM + XOUT SUM32 snoop Device ID will write the data to the Broadside (BS) RAM and the SUM32 at the same time. An XOUT with the SUM32 only Device ID will write the data only to SUM32. An XIN with either mode's Device ID will read the SUM32 value.

Table 7-10. SUM32 XFR ID

Mode	Device ID	PRU/ PRU_RTU core
XOUT (write) data to SUM32		
BS RAM + SUM32 snoop	49 (31h)	PRU
	38 (26h)	RTU_PRU
SUM32 only	47 (2Fh)	PRU
	39 (27h)	RTU_PRU
XIN (read) sum result		
	02 (2h)	Both PRU & RTU_PRU

The SUM32 directly connects with the PRU internal register R2-R10 and R29 through use of the PRU broadside interface and XFR instructions. Figure 7-10 and Table 7-11 shows the functionality of each register.



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Figure 7-10. Integration of the PRU and SUM32 (Register View)

Table 7-11. Register (R2-R9, R29) Descriptions

Register	Function	Description
R2 – R9	Data	Write only. Always write 32 Bytes for SUM32 XFR IDs.
R29	Sum	Read only. Always read 4 Bytes. This will get the current 32-bit SUM value. The read event will self-clear the SUM.

7.2.7 PRU_ICSSG Byte Swap (BSWAP)

The Byte Swap (BSWAP) module enables any of the internal PRU registers (R0 to R29) to swap byte order in 1 clock cycle via XIN function.

This module supports three functions:

1. Byte Order Swap function, flipping the byte order within a given register
2. 4_8 function, swapping the contents of R2-R5 <-> R6-R9
3. 4_16 function, swapping the contents of R2-R5 <-> R14-R17 and R6-R9 <-> R10-R13

Each of those functions have a unique XIN ID to determine which operation will occur, as shown in [Table 7-12](#).

Table 7-12. BSWAP XFR ID

Device ID ⁽¹⁾	Function	Access
160 (A0h)	Byte Order Swap	XIN
161 (A1h)	4_8	XIN
162 (A2h)	4_16	XIN

(1) Note: All PRU and RTU cores (PRU0, PRU1, RTU_PRU0, and RTU_PRU1 cores) have the same XFR ID mapping.

Note

The following sections use the syntax “Rn.bm.” This syntax is used to represent a byte field within the internal PRU register, Rn. For example, b0 represents “byte 0” (or bits 0-7) and b3 represents “byte 3” (or bits 24- 31) of a given register.

7.2.7.1 Byte Order Swap Function

The PRU core internal registers (R0 to R29) byte order will get flipped within each register. This is used by firmware to convert Little-Endian to Big-Endian or Big-Endian to Little-Endian. As shown in [Table 7-12](#), this function corresponds to the XFR Device ID of A0h.

Within each Rn register after XIN instruction execution, the following will happen.

- Rn.b3 = Rn.b0
- Rn.b2 = Rn.b1
- Rn.b1 = Rn.b2
- Rn.b0 = Rn.b3

Example 1: XIN start of R2.b0 and 8 Bytes in length:

- R2.b3 = R2.b0
- R2.b2 = R2.b1
- R2.b1 = R2.b2
- R2.b0 = R2.b3
- R3.b3 = R3.b0
- R3.b2 = R3.b1
- R3.b1 = R3.b2
- R3.b0 = R3.b3

Example 2: XIN start of R2.b0 and 1 Byte in length:

- R2.b0 = R2.b3

Example 3: XIN start of R2.b0 and 2 bytes in length:

- R2.b0 = R2.b3
- R2.b1 = R2.b2

7.2.7.2 4_8 Function

The 4_8 function swaps the contents of R2-R5 <-> R6-R9. This function operates on the XIN instruction and must start at R2.b0 and cannot exceed R9. As shown in [Table 7-12](#), this function corresponds to the XFR Device ID of A1h.

After XIN instruction execution, the following will happen.

- R2 = R6
- R3 = R7
- R4 = R8
- R5 = R9
- R6 = R2
- R7 = R3
- R8 = R4
- R9 = R5

7.2.7.3 4_16 Function

The 4_16 function swaps the contents of R2-R5 <-> R14-R17 and R6-R9 <-> R10-R13. This function operates on the XIN instruction and must start at R2.b0 and cannot exceed R17. As shown in [Table 7-12](#), this function corresponds to the XFR Device ID of A2h.

After XIN instruction execution, the following will happen.

- R2 = R14
- R3 = R15
- R4 = R16
- R5 = R17
- R6 = R10
- R7 = R11
- R8 = R12
- R9 = R13
- R10 = R6
- R11 = R7
- R12 = R8
- R13 = R9
- R14 = R2
- R15 = R3
- R16 = R4
- R17 = R5

7.2.8 PRU_ICSSG Task Manager

The PRU_ICSSG system integrates 6 Task Managers used for efficient switching between tasks.

There is one dedicated task manager for each PRU, RTU and TX_PRU core (PRU0/ PRU1, RTU_PRU0/ RTU_PRU1 and TX_PRU0/ TX_PRU1 cores), which are described in the subsequent sections. Each task manager works independently from the others.

Figure 7-11 shows a block diagram of the Task Manager modules and the associated PRU0/ PRU1 (Core CPU0 and CPU1), RTU_PRU0/RTU_PRU1 (Aux CPU0 and Aux CPU1) cores and TX_PRU0/ TX_PRU1 (Transmit CPU0 and CPU1) cores.

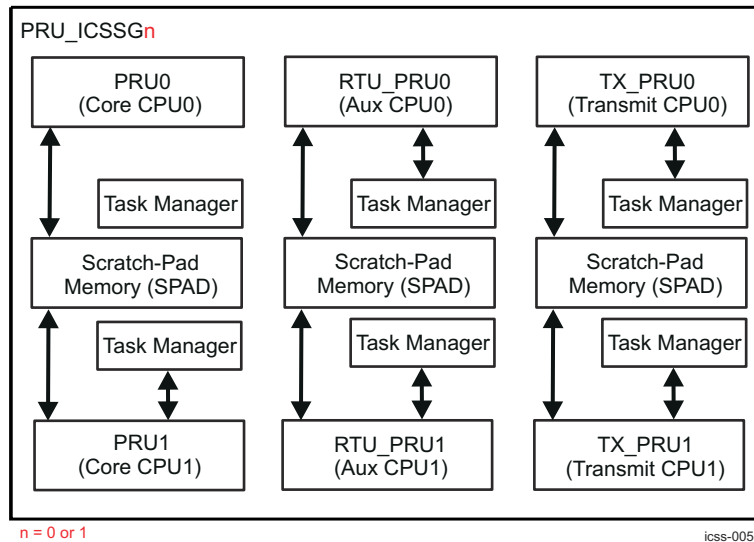


Figure 7-11. Task Manager Block Diagram

The Task Manager has two modes of operation:

- General purpose mode
- RX_TX mode

7.2.8.1 Task Manager General Purpose Mode

The General purpose mode is used to improve the firmware efficiency and performance. This feature enables software to get preempted to do another higher priority task.

It achieves this by preempting the current execution with a new hardware feature inside the PRU that causes the PRU to execute the XCHG instruction. The Task Manager will issue this hardware preemption and respond to the XCHG instruction by saving off the current program counter and ALU flags and providing a new program counter (PC) to start a new task. See section [Section 7.2.8.1.2](#) for more details about hardware context switching. When the firmware completes this new task, it will terminate this task by issuing a XIN instruction. When the Task Manager sees this execution of the XIN instruction, it will return the state of the PRU from the last saved off task.

The General Purpose mode is enabled by the ICSSG_GLOBAL_CFG[1-0] TASKS_MGR_MODE register and is responsible for:

- Saving off the program counter (PC) and flags when switching a task
- Providing a new program counter for a new task
- Restoring the original program counter when the firmware yields

The General Purpose Task manager supports the following features:

- Software can enable/disable hardware preemption
- Allows up to 2 suspended tasks (Task0 and Task1) and 1 active task

7.2.8.1.1 Tasks and Sub-tasks

The General Purpose mode supports 3 tasks - Task0 (default, or background, task), Task1, and Task2. [Figure 7-12](#) shows the basic state machine associated with these tasks.

Task2 has highest priority, Task1 has middle priority, and Task0 has lowest priority. As such, a Task2 event always preempts Task1 or Task0, if either is active. A Task1 event always preempts Task0, if active. To exit out of the current state or task, software must issue a “software completion of task” using XIN and a device ID of 252.

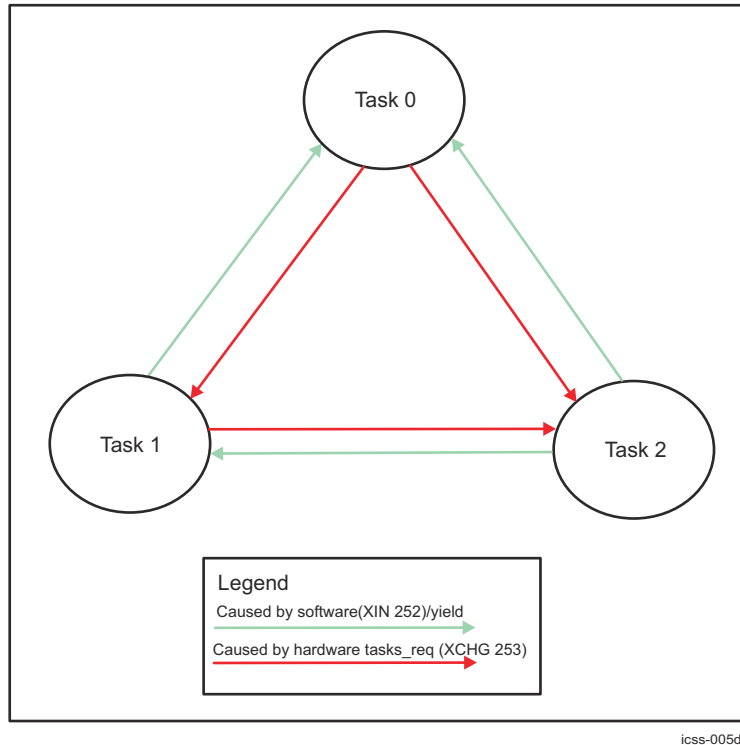


Figure 7-12. High Level Finite State Machine

Task2 and Task1 support up to five sub-tasks (S0-S4), which are enabled or disabled in the ICSSG_GLOBAL_CFG register. [Figure 7-13](#) and [Figure 7-14](#) show the state machines for entering into these sub-tasks, and the priority of these sub-tasks are as follows:

- Task2 sub-tasks order of priority is: T2_S0 (highest priority) -> T2_S1 -> T2_S2 -> T2_S3 -> T2_S4 (lowest priority).
- Task1 sub-tasks order of priority is: T1_S1 (highest priority) -> T1_S2 -> T1_S3 -> T1_S4 -> T1_S0 (lowest priority).

Note that the subtasks can only be preempted by a higher priority task. However, they cannot be preempted by another subtask within the same task. For example, T1_S4 can be preempted by T2_S3. However, T1_S4 cannot be preempted by T1_S3.

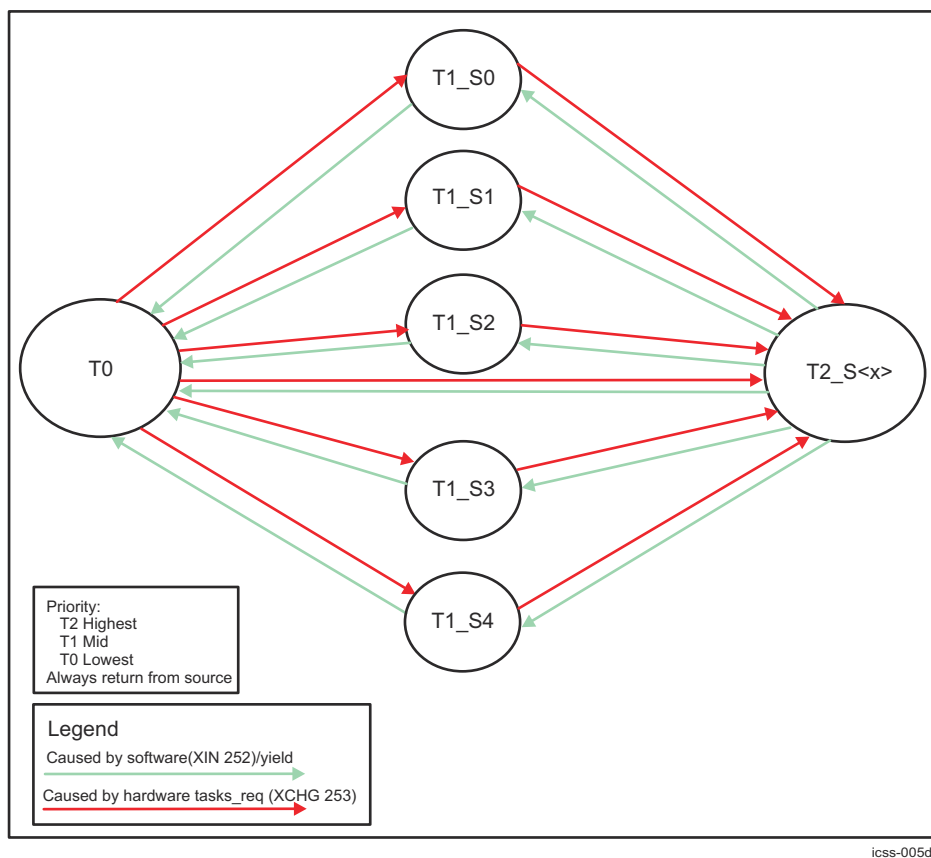


Figure 7-13. Task 1 Finite State Machine

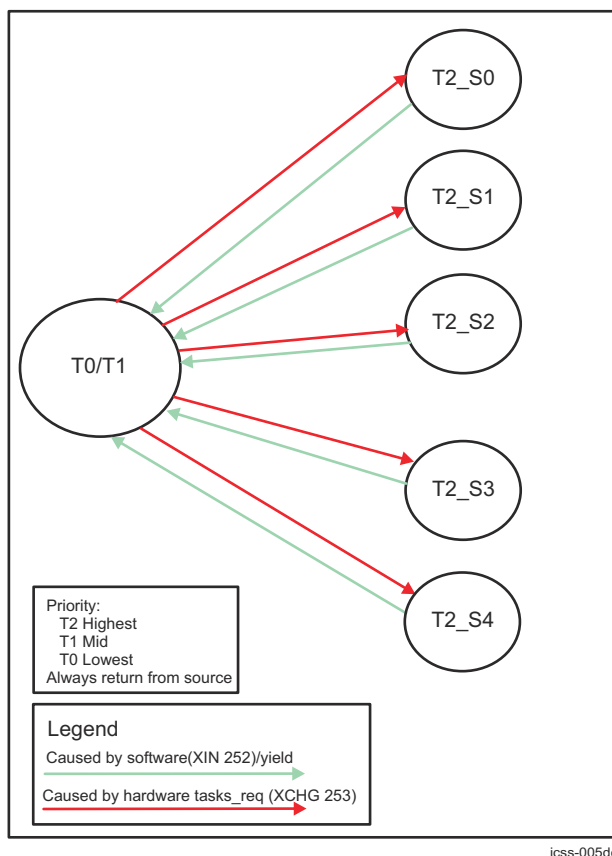


Figure 7-14. Task 2 Finite State Machine

In general purpose mode, the source event for each sub-task is ICSSG_TS1_GEN_CFG1/ ICSSG_TS1_GEN_CFG2 and ICSSG_TS2_GEN_CFG1/ ICSSG_TS2_GEN_CFG2 registers defines the source of the event which will trigger the Task1 and Task2 sub-tasks.

Table 7-13 shows the mapping.

Note

All source events should be cleared before any update to the mapping.

Table 7-13. Task to Event Mapping

ICSSG_TS1_GEN_CFG1/ ICSSG_TS1_GEN_CFG2 and ICSSG_TS2_GEN_CFG1/ ICSSG_TS2_GEN_CFG2	Source Event
0	RX_SOF
1	RX_BK1
2	RX_BK2
3	RX_BKN
4	RX_EOF
5	1h
6	TX_L1_L2_WM
7	TX_L2_EMPTY & TX_L2_EOF_PEND
8	TX_UNDER_RX_OVER_ERR
9	PR1_MDIO_LINKINT[0] (from MDIO)
10	PR1_MDIO_LINKINT[1] (from MDIO)
11	PR1_EDC0_SYNC0_OUT
12	PR1_EDC0_SYNC1_OUT

Table 7-13. Task to Event Mapping (continued)

ICSSG_TS1_GEN_CFG1/ ICSSG_TS1_GEN_CFG2 and ICSSG_TS2_GEN_CFG1/ ICSSG_TS2_GEN_CFG2	Source Event
13	PR1_EDC1_SYNC0_OUT
14	PR1_EDC1_SYNC1_OUT
15	1h
31-16	IEP0_CMP[15:0]
37-32	IEP0_CAPR[5:0]
39-38	IEP0_CAPRF[1:0]
55-40	IEP1_CMP[15:0]
61-56	IEP1_CAPR[5:0]
63-62	IEP1_CAPRF[1:0]
127-64	SPINLOCK_FEED_REQ[63:0] ⁽¹⁾
135-128	INTC_HOST_OUT[7:0]
143-136	INTC_HOST_TASKMGR_REQ[7:0]
145-144	RTU_PDSP_INTR_IN[1:0] ⁽²⁾
147-146	PR1_PDSP_INTR_IN[1:0]
148	xfr_vbus_rd_data_rx0_req (data rdy)
149	xfr_vbus_rd_data_rx1_req (data rdy)
150	xfr_vbus_rd_data_rx2_req (data rdy)
151	(tx_l2_empty & (tx_l1_occ[6:0] == (tx_wm_lvl + 7'b1))) (tx_l2_empty & (tx_l1_occ[6:0] < (tx_wm_lvl + 7'b1)) & tx_l1_eof_pend)
255-148	Reserved

(1) SPINLOCK_FEED_REQ[63:0] is from the spinlock module. It will assert for 1 clock cycle when the clock goes from a 1 to 0, or freed.

(2) PDSP in source event names is equivalent to the PRU processor names.

7.2.8.1.2 Task Manager Hardware Context Switching

When switching between tasks, the Task Manager only saves and restores the program counter (PC) and flags, as shown in [Figure 7-15](#). The firmware is responsible for saving and restoring any Rn internal registers that it will override during a task. The SPAD, Data RAM, or Shared RAM (Data RAM2) can be used to store the Rn register value.

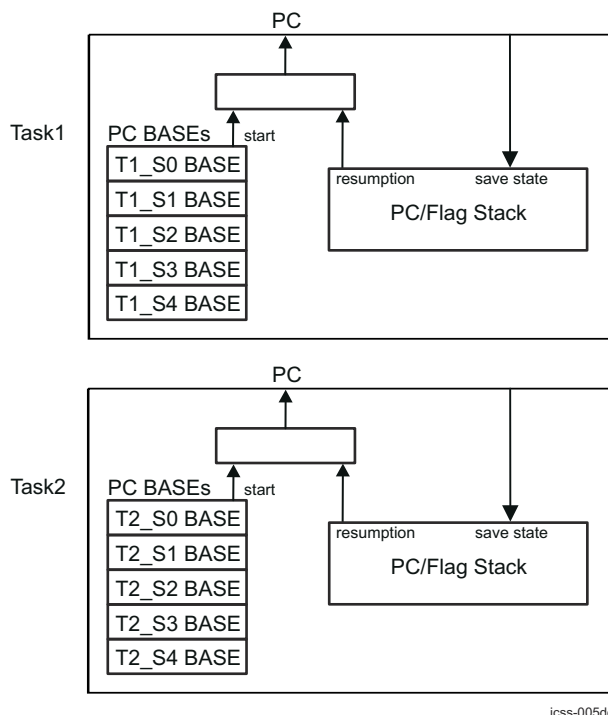


Figure 7-15. Hardware Context Switching Block Diagram

7.2.8.1.3 Task Manager Programming Guide

Figure 7-16 shows the basic programming steps within a given task or sub-task.

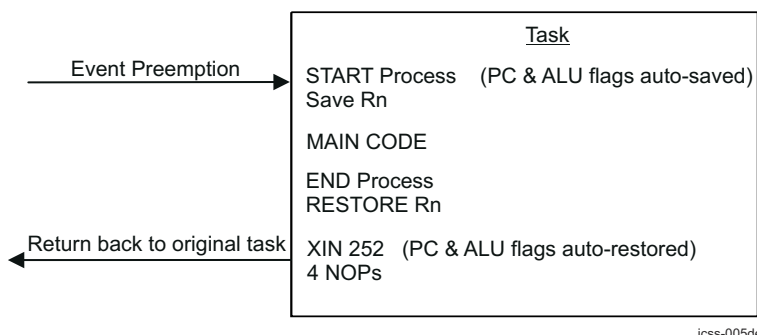


Figure 7-16. Task Programming

Note

The SAVE and RESTORE process can be preempted. It will resume at the next instruction after the higher priority task yields. To avoid preemption, the ICSSG_GLOBAL_CFG[TSm_ENn] bitfield (where m = 1 or 2 and n = 0 to 4) can be used to disable (and re-enable) preemption.

7.2.8.2 Task Manager RX_TX Mode

The RX_TX mode can be used for Ethernet use cases to improve the firmware efficiency and performance. This mode is enabled by the ICSSG_GLOBAL_CFG[1-0] TASKS_MGR_MODE register. In general, the RX_TX mode is similar to the General Purpose mode. Therefore, this section only covers the differences between General Purpose mode and RX_TX mode.

The RX_TX Task manager is responsible for:

- Preempting a lower priority task and providing a new program counter (PC)
- Storing the current program counter (PC) and flags
- Restoring the saved program counter (PC) and flags when the firmware yields

- Tracking the state of background, RX and TX states

7.2.8.2.1 RX_TX Task Manager Features

Task Manager features:

- Software can enable/disable RX or TX preemption or both
- Software can observe the state of task manager
- Software can read the time spent in the 3 domains
- Allows up to 2 suspended tasks (Background and RX) and 1 active task

7.2.8.2.2 Tasks and Sub-tasks

Unlike the General Purpose mode, the Task1 and Task2 sub-states in RX_TX mode have pre-defined source events, listed in [Table 7-14](#).

Table 7-14. Task to Event Mapping

Sub-tasks	Source Event
Task1	
T1_S0	RX_SOF
T1_S1	Programmable size threshold, ranging from 1 Byte to 32 Bytes (ICSSG_RX_CFG[4-0] BK1_SIZE)
T1_S2	Programmable size threshold, ranging from 1 Byte to 32 Bytes (ICSSG_RX_CFG[9-5] BK2_SIZE)
T1_S3	Every 32 Bytes (ICSSG_RX_CFG[14-10] BKN_SIZE)
T1_S4	RX_EOF
Task2	
T2_S0	TX Enable based on IEP CMP SOF and TX Express Type is true
T2_S1	TX Enable based on IEP CMP SOF and TX Express Type is false
T2_S2	TX L2 FIFO WATER MARK event
T2_S3	TX_EOF
T2_S4	RX_TX_ERROR (either RX_L1_UNDERRUN or TX_L1_OVERRUN)

Note

The sub-task priorities are the same as General Purpose mode. For Task1, T1_S1 (highest priority) -> T1_S2 -> T1_S3 -> T1_S4 -> T1_S0 (lowest priority). T1_S0 is the lowest priority to prevent a RX_SOF starting before RX_EOF starts in the case RX_EOF is late. For Task2, T2_S0 (highest priority) -> T2_S1 -> T2_S2 -> T2_S3 -> T2_S4 (lowest priority).

The size threshold is a hardware dependency that must be met in order to switch to a given state. The size is based on the number of bytes that got pushed into the RX L2 FIFO. For example, assume T1_S1 and T1_S2 are both set to 16 Bytes. The task manager will issue a hardware preemption for T1_S1 after the first 16 Bytes got pushed into the RX L2 FIFO. The task manager will issue a hardware preemption for T1_S2 after the second 16 Bytes got pushed into the RX L2 FIFO. The task manager will issue a hardware preemption for T1_S3 after another 32 Bytes got pushed into the RX L2 FIFO. Note the task manager will continue to issue a new hardware preemption for T1_S3 for each new 32 Bytes block of data until a T1_S4 event occurs.

7.2.9 PRU_ICSSG Spinlock

Each PRU_ICSSG subsystems includes Spinlock controller/target interfaces to allow fast signaling and resource sharing within and between PRU_ICSSG subsystems.

Supported Features:

- 64 ownership flags (shared by SLICE0 and SLICE1 within an PRU_ICSSG subsystem) with support of 14 initiators, including:
 - 6 Internal PRU cores:
 - PRU0/1, RTU_PRU0/1 and TX_PRU0/1 cores
 - 2 clock cycle response of Spinlock status
 - 2 External Host register access:
 - Each with a separate address space ([ICSSG_SPIN_LOCK0](#) and [ICSSG_SPIN_LOCK1](#))
 - Enables 2 controllers: Host and DMA
 - 6 External PRU cores:
 - One External PRU_ICSSG with 6 PRU cores
 - With flexible external pipeline for SoC timing closer
 - Allows the sharing of flags across PRU_ICSSG systems
 - 4 to 6 clock cycle response
- Fixed arbitration
- Flag selection through [ICSSG_SPIN_LOCK0/1\[13-8\]](#) MMR_OWN_REQ_VECTOR_0/1 bit field:
 - PRU, RTU_PRU and TX_PRU cores use R1.b0 register, which is snooped or continually monitored by the Spinlock. XOUT of this register is not required. XIN of R1.b0 causes arbitration action.
 - Each Host uses one 32-bit addressable space
 - Vector write (through [ICSSG_SPIN_LOCK0/1\[13-8\]](#) MMR_OWN_REQ_VECTOR_0/1) or status read (through [ICSSG_SPIN_LOCK0/1\[0\]](#) MMR_OWN_REQ_STATUS_0/1) will cause arbitration action

7.2.9.1 PRU0/1 and RTU_PRU0/1 Spinlock Interface

Note: All PRU and RTU cores (PRU0, PRU1, RTU_PRU0, and RTU_PRU1 cores) have the same mapping.

Table 7-15. PRU registers to Spinlock Mapping

PRU Register	BS ID	Access	Type	HW port	Description
Internal/External					
R1.b0[5-0]	NA	NA Always exported	Flag selection	own_req_vector[5:0] input	Defines which flag to arbitrate
Internal					
R1.b3[0]	INT_SPIN_ID 0x90	XIN	Flag status and arbitration	own_req select control input own_req_status status output	own_req input will assert during this XIN transaction. This assertion will cause an arbitration event. The result of this arbitration is returned to R1.b3[0] via own_req_status 0h: not owned/lost 1h: owned/won
R1.b0	INT_SPIN_ID 0x90	XOUT	Flag clear	own_req_clr control input	own_req_clr input will assert during the XOUT R1.b3 transaction. This assertion will clear the flag selected by R1.b0/own_req_vector
External0					
R1.b3[0]	EXT_SPIN_ID0 0x91	XOUT	Flag status and arbitration		own_req input will assert during this XOUT transaction. This assertion will cause an arbitration event. The result of this arbitration is returned to R1.b3[0] via own_req_status: 0h: not owned/lost 1h: owned/won NOTE: Firmware must have 8 NOP before XIN after XOUT.

Table 7-15. PRU registers to Spinlock Mapping (continued)

PRU Register	BS ID	Access	Type	HW port	Description
R1.b3[0]	EXT_SPIN_ID0 0x91	XIN	Flag status and arbitration	own_req_status status output	own_req input will assert during this XIN transaction. This assertion will cause an arbitration event. The result of this arbitration is returned to R1.b3[0] via own_req_status: 0h: not owned/lost 1h: owned/won
R1.b0	EXT_SPIN_ID0 0x91	XOUT	Flag clear	own_req_clr control input	own_req_clr input will assert during the XOUT R1.b1 transaction. This assertion will clear the flag selected by R1.b0/own_req_vector
External1					
R1.b3[0]	EXT_SPIN_ID1 0x92	XOUT	Flag status and arbitration		own_req input will assert during this XOUT transaction. This assertion will cause an arbitration event. The result of this arbitration is returned to R1.b3[0] via own_req_status: 0h: not owned/lost 1h: owned/won NOTE: Firmware must have 8 NOP before XIN after XOUT.
R1.b3[0]	EXT_SPIN_ID1 0x92	XIN	Flag status and arbitration	own_req select control input own_req_status status output	own_req input will assert during this XIN transaction. This assertion will cause an arbitration event. The result of this arbitration is returned to R1.b3[0] via own_req_status: 0h: not owned/lost 1h: owned/won NOTE: Firmware must have 8 NOP before XIN after XOUT.
R1.b0	EXT_SPIN_ID1 0x92	XOUT	Flag clear	own_req_clr control input	own_req_clr input will assert during the XOUT R1.b1 transaction. This assertion will clear the flag selected by R1.b0/own_req_vector

7.2.10 PRU_ICSSG Filter Data Base (FDB)

The Filter Data Base (FDB) block performs hardware lookup and provides the port mapping to firmware. It operates on ingress of the 2 RX physical ports and 1 RX host port.

The Filtering Database (FDB) is used to help ensure efficient usage of a Bridged LAN's resources by only forwarding received frames to those LAN segments on which they need to be. To this end, the FDB aggregates information used to make filtering and forwarding decisions for received MAC frames. The information may be statically or dynamically configured via control plane protocols, or dynamically learned based on observed traffic. Conceptually, the FDB is queried upon reception of each potentially forwarded frame, and the FDB provides the Forwarding Process with a set of potential transmission ports.

FDB Supported Features:

- Optional VLAN -> FID hardware Lookup Table (LUT)
 - Configurable SMEM base address for VLAN to FID mapping
- Optional HSR_SEQ support when VLAN is disabled
- 256-bit 16KB broadside FDB hardware Lookup Table (LUT)
 - Configurable hash with index size (64, 128, 256, 512, 1024, 2048)
 - Configurable bucket sizes (2, 4, 8)
 - Auto hardware start/lookup for RX Port 0/RX Port 1
 - Software start/lookup for RX Host Port
 - General purpose mode, 16Byte compare operation in 1 clock cycle
 - Either PRU core (PRU0/ PRU1) can access the FDB block, but only one needs to own it; spinlock is required for XOUT
- The FDB block supports 3 modes of operation:
 - Generic broadside RAM (256-bit). Each PRU has its own address index.
 - FDB LUT mode:
 - Both PRU cores can access the Lookup Table (LUT)
 - General purpose mode, 16Byte compare (Always active)
- 2 physical banks of RAM, and each bank has 8KB memory size
 - One of the RAM's can operate in FDB LUT mode and the other in Generic broadside RAM/16Byte compare mode

Not Supported Features:

- Bucket size of 1

Figure 7-17 shows a high-level view of the FDB module.

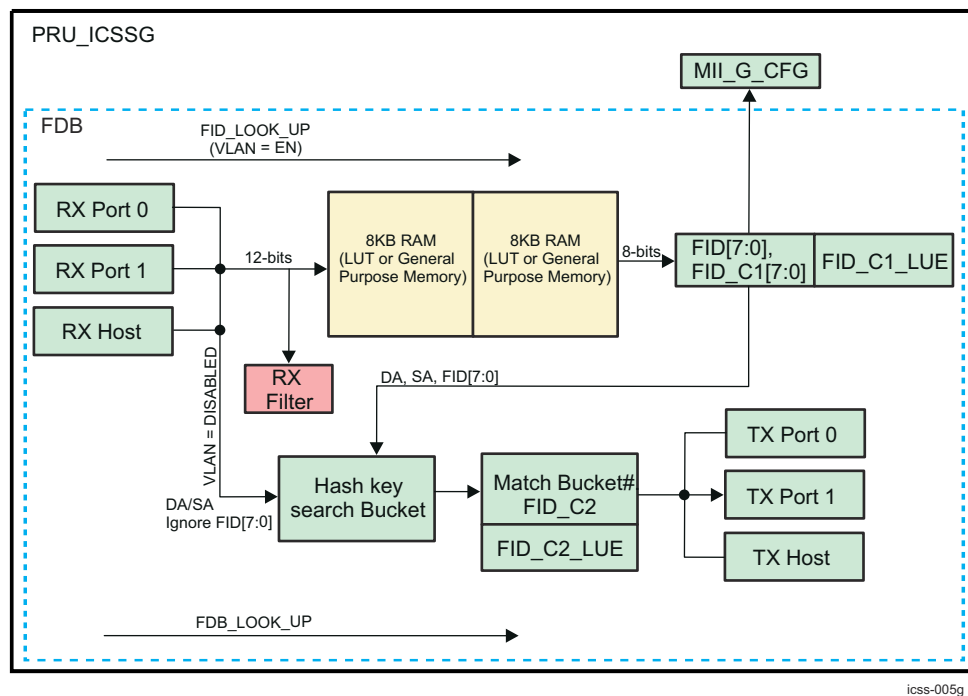


Figure 7-17. PRU_ICSSG FDB Block Diagram

PRU0 or PRU1 cores only can access the FDB RAM's. RTU_PRU0 or RTU_PRU1 auxiliary cores only gets the result of FDB lookup to its broadside access.

7.2.10.1 FDB Modes of operation

Each RAM bank of the FDB module supports 2 modes of operation:

- FDB LUT mode
- Generic broadside RAM (256-bit wide) and General purpose compare mode (16Byte compare)

The FDB block consist of 2 physical banks of RAM, each of 8KB size. The PRU core will always have the ability to read/write the broadside RAM in FDB LUT mode. If FDB LUT mode is disabled then 8KB of the broadside RAM will operate in Generic mode and General purpose compare mode. Table 7-16 shows the valid mode configurations for each FDB physical bank.

Table 7-16. Valid configurations of modes

Config1	FDB Bank0: FDB LUT mode enabled FDB Bank1: FDB LUT mode enabled	The FDB LUT uses the full 16KB memory for the operation. PRU core will write to the RAM entry to learn if the packet miss
Config2	FDB Bank0: FDB LUT mode enabled FDB Bank1: FDB LUT mode disabled	The FDB LUT uses the first bank only (Bank0), or 8KB of memory The second memory bank (Bank1) is disabled for LUT operation. Bank1 is used for general purpose compare mode.
Config3	FDB Bank0: FDB LUT mode disabled FDB Bank1: FDB LUT mode disabled	Bank0 and Bank1 are 16KB RAM and it is used in general purpose compare mode. No FDB LUT events.

Note

In all configurations only one of the PRU cores (PRU0 or PRU1) can access the FDB RAM. It is not legal to have PRU0 access at the same time when PRU1 core access the FDB RAM. This is valid for all modes of operation.

7.2.10.1.1 FDB LUT: Hardware operation (HSR Disabled: MII_G_RT_FDB_GEN_CFG2[5] FDB_HSR_EN = 0h)

The software needs to configure the FDB mode of operation.

If VLAN is enabled through [MII_G_RT_FDB_GEN_CFG2\[6\]](#) FDB_VLAN_EN bit, then first hardware LUT is to translate VLAN_ID[11-0] to FID[7-0] by calling the FID_LOOK_UP process. If VLAN is disabled, then first hardware LUT is to FDB_LOOK_UP.

7.2.10.1.2 FDB LUT: Hardware operation (HSR Enabled: MII_G_RT_FDB_GEN_CFG2[5] FDB_HSR_EN = 1h)

The user needs to configure the FDB mode of operation and set FDB_GEN_CFG2[5] FDB_HSR_EN = 1h bit.

Note

DA Lookup does not support HSR_SEQ. Only SA Lookup supports HSR_SEQ compare.

7.2.10.1.3 8KB/16KB Generic broadside RAM mode of operation

When FDB0/FDB1 LUT mode is disabled, then Generic 8KB/16KB broadside RAM mode is enabled. Both memory banks (Bank0 and Bank1) are used in this mode of operation. Either PRU core (PRU0 or PRU1) can access Bank0 or Bank1 via the FDB_Data/FDB_Address. RTU_PRU0 and RTU_PRU1 auxiliary cores only have access to the results of the lookup. The auxiliary cores (RTU_PRU0 and RTU_PRU1) can not write or read to the FDB memory banks.

7.2.10.1.3.1 Broadside (BS) Mapping

Table 7-17. Broadside (BS) Mapping

Register	XFR ID	Desc	Notes
R9:R2 (32 Bytes)	30/0x1E, PRUx	FDB_Data	No access restriction. 1 Byte upto 32 Byte access
R5:R2 (16 Bytes)	31/0x1F, PRUx	General Pattern	No access restriction. 1 Byte upto 16 Byte access
R10	30/0x1E, PRUx	AutoIndexEn, FDB_Address	Must do 2 byte R10[15:0]. Write Address rollover not supported
R12:R10	32/0x20, PRUx, RTUx	Port0_Result	No access restriction
R12:R10	33/0x21, PRUx, RTUx	Port1_Result	No access restriction
R12:R10	34/0x22, PRUx, RTUx	Host_Result	No access restriction
R10	35/0x23, PRUx	General_Results	No access restriction

Table 7-18. Broadside (BS) FDB_Data mapping with shift of zero

Local	Item
R2	FDB0_0
R3	FDB0_1
R4	FDB1_0
R5	FDB1_1

FDB Structure - HSR Disabled:

([MII_G_RT_FDB_GEN_CFG2\[5\]](#) FDB_HSR_EN = 0h)

FDB = {FDB_1, FDB_0}

FDB_0 = {DA_SA3, DA_SA2, DA_SA1, DA_SA0}

FDB_1 = {FID_C2, FID, DA_SA5, DA_SA4}

FDB Structure - HSR Enabled:

([MII_G_RT_FDB_GEN_CFG2\[5\]](#) FDB_HSR_EN = 1h)

FDB = {FDB_1, FDB_0}

FDB_0 = {DA_SA3, DA_SA2, DA_SA1, DA_SA0}

FDB_1 = {HSR_SEQ, DA_SA5, DA_SA4}

Note

Only SA Lookup supports HSR_SEQ compare.

Table 7-19. FDB Indexing

FDB RAM Address	Content	Bucket Size 2#	Bucket Size 4#	Bucket Size 8#
0	FDB3, FDB2, FDB1, FDB0	1,0	0	0
1	FDB7, FDB6, FDB5, FDB4	3,2	1	0
2	FDB11, FDB10, FDB9, FDB8	5,4	2	1
3	FDB15, FDB14, FDB13, FDB12	7,6	3	1

Table 7-20. FDB Index Configuration

Location	Name	Access Type	Reset State	Description
R10[8-0]	FDB_Address	R/W	9h	FID Index for PRU Read/Write access of the FDB. Index is direct mapping to the 16KB FDB RAM. Note: Width is 256-bits or 32Bytes 0h: 1st 32 Bytes 1h = 2nd 32 Bytes In general purpose mode, the compare always occurs R10[8] determines the Bank 0h: FDB0 (Bank0) 1h: FDB1 (Bank1)
R10[15]	AutoIndexEn	R/W	1h	FID Auto Increment the Index Enable. 0h: Disable Auto Increment 1h: Enable Auto Increment Each PRU Write or Read to the FDB Array will cause the FDB_Address by 1 Note: 1Byte write or a 32Byte will do the auto increment of 1 In general purpose mode, the compare always occurs after each access Note: Address rollover is not supported

Table 7-21. Port<1/0>_Result and Host

Location	Name	Access Type	Reset State	Description
R10[7-0]	FID	R	-	FID from the last VLAN_ID lookup Sticky /Persistence
R10[15-8]	FID_C1	R	-	FID_C1 from the last VLAN_ID lookup Sticky /Persistence. Valid when FID_C1_LUE is SET.
R10[23-16]	DA_FID_C2	R	-	Valid only for HSR Disabled (MII_G_RT_FDB_GEN_CFG2[5] FDB_HSR_EN = 0h) FID_C2 from the last DA FDB lookup Sticky /Persistence. Valid when DA_FID_C2_LUE is SET.
R10[31-24]	SA_FID_C2	R	-	Valid only for HSR Disabled (MII_G_RT_FDB_GEN_CFG2[5] FDB_HSR_EN = 0h) FID_C2 from the last SA FDB lookup Sticky /Persistence. Valid when SA_FID_C2_LUE is SET.
R11[8-0]	DA_FDB_Address	R	-	Address of the HIT Sticky /Persistence. Valid when DA_FID_C2_LUE. Always valid even if a SA match was not found. Used for learning. Always the physical address of the FDB RAM.
R11[9]	RESERVED	R	-	Reserved
R11[10]	DA_FDB_Offset	R	-	Offset only valid for bucket size 2. Used to determine start of the bucket.
R11[11]	RESERVED	R	-	Reserved
R11[14-12]	DA_Bucket#	R	-	Returns the Bucket# 0h: (#1) 3h: (#4) ... 7h: (#8) Valid when DA_FID_C2_LUE & DA_FDB_MATCH
R11[15]	RESERVED	R	-	Reserved
R11[24-16]	SA_FDB_Address	R	-	Address of the HIT Sticky /Persistence. Valid when SA_FID_C2_LUE. Always valid even if a SA match was not found. Used for learning. Always the physical address of the FDB RAM.

Table 7-21. Port<1/0>_Result and Host (continued)

Location	Name	Access Type	Reset State	Description
R11[25]	RESERVED	R	-	Reserved
R11[26]	SA_FDB_Offset	R	-	Offset only valid for bucket size 2. Used determine start of the bucket.
R11[27]	RESERVED	R	-	Reserved
R11[30-28]	SA_Bucket#	R	-	Returns the Bucket# 0h: (#1) 3h: (#4) ... 7h: (#8) Valid when SA_FID_C2_LUE & SA_FDB_MATCH
R12[0]	FID_C1_LUE	R	-	FID C1 LookUpEnd CLR ON SOF OR HOST MMR WRT SET ON After FID lookup, FID is valid and FID_C1 is valid
R12[1]	DA_FID_C2_LUE	R	-	FID C2 LookUpEnd CLR ON Port<1/> SOF OR HOST MMR WRT SET ON After DA FDB lookup and DA, FID & FID_MASK Match. After the first Match it will stop
R12[3]	SA_FID_C2_LUE	R	-	FID C2 LookUpEnd CLR ON Port<0/1> SOF OR HOST MMR WRT SET ON After SA FDB lookup completed
R12[4]	SA_FDB_MATCH	R	-	CLR ON Port<0/1> SOF OR HOST MMR WRT SET ON After SA FDB lookup and SA, FID & FID_MASK Match. After the first Match it will stop

Table 7-22. General Purpose Result

Location	Name	Access Type	Reset State	Description
R10[0]	MATCH	R	-	Default Read Mode of FDB RAM Set, when After XOUT of new Pattern or new Address must wait for 2 clock cycles. Before you can XIN MATCH value By default, below is the compare function XOUT of new pattern(optional). XOUT of new FDB Address(optional). Wait 2 clock cycles. GeneralPattern[gp_size:0] == FDB_RAM.Q[gp_size:0] Write Mode Set when XOUT of write data to the FDB RAM matches the GeneralPattern XOUT of new pattern(optional) XOUT of new FDB Address(optional) XOUT to new data to FDB RAM DATA to compare Wait 2 clock cycles. Before you can XIN MATCH value GeneralPattern[gp_size:0] == FDB_RAM.D[gp_size:0] gp_size is defined in FDB_GEN_CFG2 register. FDB_GEN_MODE_BYTE_EN bit field defines the FDB general mode byte compare size: from 1 Byte upto 16 Bytes The compare function is always active

Table 7-22. General Purpose Result (continued)

Location	Name	Access Type	Reset State	Description
R10[1]	DONE	R	-	CLR ON Any update on GeneralPattern SET ON After the compare has completed. Note: A new compare operation will occur on: Any update on GeneralPattern Any update on FDB_Address Any Write/Read of FDB_Data

7.2.10.1.4 FDB General purpose compare mode operation

When FDB0/FDB1 LUT is disabled, then General purpose compare mode of operation is enabled for that Bank through registers: [MII_G_RT_FDB_GEN_CFG2](#)[7] FDB_GEN_MODE_EN_BK0 (for Bank0) and [8] FDB_GEN_MODE_EN_BK1 (for Bank1).

Compare flow:

- XOUT GeneralPattern
- XOUT FDB_Address
- Delay 2 clock cycles
- XIN General_Results

Another method to perform the compare is:

- XOUT GeneralPattern
- XOUT FDB_Address, enable AutoIndex
- Delay 2 clock cycles
- XIN General_Results for Index
- XIN FDB_DATA (this advances the FDB Address)
- Delay 2 clock cycles
- XIN General_Results for Index + 1

7.3 PRU_ICSSG Data Movement Accelerators Functional

7.3.1 PRU_ICSSG XFR2VBUS Hardware Accelerator

RTU_PRU core can write and read data packets to and from port queues, located in the MSMC SRAM into PRU/RTU_PRU core registers via XFR2VBUS hardware accelerator. Each of the PRU_ICSSG Slices has implemented two sets of TX/RX XFR2VBUS hardware accelerators.

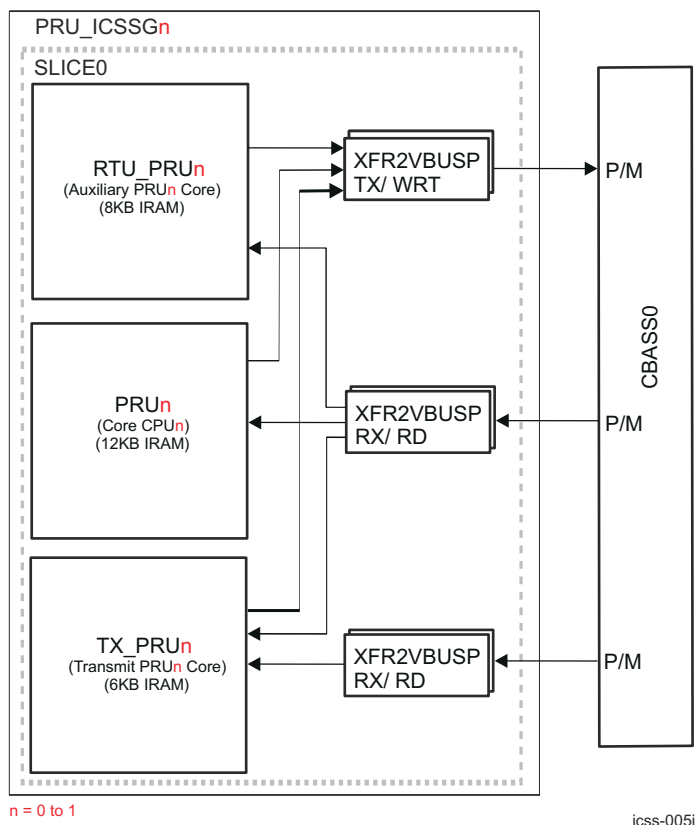


Figure 7-18. XFR2VBUS Hardware Accelerator

Supported features:

- 2 x XFR2VBUS RX threads
- 2 x XFR2VBUS TX threads
- 2 x XFR2VBUS RX only threads, attached to TX_PRU0 and TX_PRU1 Transmit cores

XFR2VBUS RX buffer features:

- 1 x 64 Byte deep RX/Read buffer
 - 4 Byte, 32 Byte, or 64 Byte read size per RD (read) command
 - Optional automatic read command with incrementing address on pop of read data
 - 32 Byte optimization mode available

XFR2VBUS TX buffer features:

- 1 x 64 Byte deep TX/Write buffer
 - 1 Byte up to 64 Byte write size per WRT (write) command

The ownership of commands and data is flexible. The XFR2VBUS accelerator is shared between RTU_PRU and PRU cores. Either RTU_PRU or PRU cores can own command or data. Status is available to both cores.

Note: The ownership should be preplanned and static per use model.

The XFR2VBUS is a simple hardware accelerator which is used to get the lowest read round trip latency from MSMC and to decouple the latency seen by the PRU. Each XFR2VBUS instance is connected to the CBASS0.

The PRU_ICSSG system has a total of 4 XFR2VBUS TX/RX hardware accelerators and 2 extra XFR2VBUS RX only, attached to each of the TX_PRU cores.

The hardware has no protect nor arbitration between the 2 controllers, so it is the firmware responsibility to insure there is only one owner/access to a common address.

7.3.1.1 Blocking Conditions

The only blocking condition is caused when the VBUSM command/data FIFO is full. It is required that the external bandwidth is very high. All egress commands and data should get sent without head of line blocking. Based on arbitration some delay is possible.

7.3.1.2 Read Operation with Auto Disabled

The XFR2VBUS supports 1 command in its command FIFO, 1 XOUT to define the address and size (4 Byte, 32 Byte, 64 Byte, aligned). This will cause the VBUSP read command to be issued. Only 1 read command can be in flight. The read address defines the offset of the 64 Byte of read data. The read size defines the size of the transfer, 4 Byte, 32 Byte, 64 Byte, aligned Offset + size must be aligned to 32 Byte width of the bus. 1 XIN, the software can see the status of command FIFO and read data FIFO.

Note: XIN of the read data will fully pop the data, independent of XIN size.

7.3.1.3 Read Operation with Auto Enabled

The same features as Auto Disabled are valid with the following exceptions:

64 Byte mode:

- Address needs to be MOD 0x40/64 Byte aligned
- Size needs to be 64 Byte
- 1 XOUT to define the start address, which needs to be MOD 0x40/64 Byte aligned
- The XFR2VBUS will issue 1 new command every time this is 64 Bytes available in the read data FIFO
- 1 XIN of read data will cause a new command to be issued since, 64 Bytes are available
- To stop the issuing new read commands, disable auto mode

32 Byte mode:

- Size needs to be 32 Byte
- 1 XOUT to define the start address, which needs to be MOD 0x20/32 Byte aligned
- The XFR2VBUS will issue 1 new command every time this is 32 Bytes available in the read data FIFO
- 1 XIN of read data will cause a new command to be issued since, 32 Bytes are available
- To stop the issuing of new read command, disable auto mode

Note: XIN of the read data will fully pop the data, independent of XIN size.

7.3.1.4 Write Operation with Auto Disabled

The XFR2VBUS supports 1 command in the command FIFO.

- 1 XOUT to define the address, data and size (on the fly). 1 Byte, 4 Byte, 32 Byte, 64 Byte and must be aligned.
- Only 1 write command can be in flight since this is VBUSP
- 1 XIN the software can see the status of write command FIFO and write data FIFO

7.3.1.5 RTU_PRU/ PRU to XFR2VBUS Interface

WR_ID0 = 0x62

WR_ID1 = 0x63

Table 7-23. Write Commands

PRU Register	BS ID	Access Type	Register	Notes
64 Byte Mode (Implied if R17.b3 enable is true)				
R17-R2	WR_ID0/1	XOUT	WR_DATA	Write Data Only 1 XOUT is allowed per transfer including the address/data Must be atomic XOUT R19-R2

Table 7-23. Write Commands (continued)

PRU Register	BS ID	Access Type	Register	Notes
R19-R18	WR_ID0/1	XOUT	WR_ADDR	Write address 48-bits 2 options: Write the full 48-bits with one XOUT or Write the lower 32-bits with one XOUT Note, the one XOUT can set the address and data at the same time, but in this case data needs to be the full 64 bytes. The address can be the full 48-bits or just the lower 32-bits of the address, it will use the current state of the upper 16-bits. Address must be aligned
32 Byte Mode (Implied if R17.b3 enable is false)				
R9-R2	WR_ID0/1	XOUT	WR_DATA	Write Data Size restrictions 1 byte 4 bytes aligned with address, no holes 32 bytes aligned with address, no holes Only 1 XOUT is allowed per transfer including the address/data Only 1 byte and 4 bytes allow not aligned access if MII_G_RT_ICSS_G_CFG[2] RX_L2_G_EN is set.
R11-R10	WR_ID0/1	XOUT	WR_ADDR	Write address 48-bits 2 options: Write the full 48-bits with one XOUT or Write the lower 32-bits with one XOUT Note, the one XOUT can set the address and data at the same time, but in this case data needs to be the full 32 bytes. The address can be the full 48-bits or just the lower 32-bits of the address, it will use the current state of the upper 16-bits.
ALL modes				
R20[0]	WR_ID0/1	XIN	WR_BUSY	Write Busy Status 0h: Idle 1h: Active (WR CMD FIFO LEVEL !=0) or (WR DATA FIFO LEVEL !=0)

RD_ID0 = 0x60

RD_ID1 = 0x61

Table 7-24. Read Commands

PRU Register	BS ID	Access Type	Register	Notes
R17-R2	RD_ID1/0	XIN	RD_DATA	Read Data

Table 7-24. Read Commands (continued)

PRU Register	BS ID	Access Type	Register	Notes
R18[0]	RD_ID1/0	XOUT	RD_AUTO	Read Auto Mode If 0 -> 1, must write RD_ADDR If 1 -> 0, must not write RD_ADDR, must drain RD_DATA/RD_CMD If 0 -> 0, must write RD_ADDR When set, every RD_DATA pop will cause a new read command and read address to increment by 0x20 for the next read command if size is set to 32 Bytes 0x40 for the next read command if size is set to 64 Bytes In this case, user must set the address to be ether mod 0x20 or 0x40. 4 Byte mode is not supported.
R18[2-1]	RD_ID1/0	XOUT	RD_SIZE	Read Size 0h: 4 Bytes 1h: Reserved 2h: 32 Bytes 3h: 64 Bytes
R18[0]	RD_ID1/0	XIN	RD_BUSY	Read Busy Status 0h: Idle 1h: Active (RD CMD FIFO LEVEL !=0) or (RD DATA FIFO LEVEL !=0)
R18[1]	RD_ID1/0	XIN	RD_CMD_FL	Read command FIFO Level 0h: Empty 1h: Occupied Note: It only pop the read command FIFO after the read data has arrived
R18[2]	RD_ID1/0	XIN	RD_DATA_FL	Read data FIFO Level 0h: Empty 1h: Occupied 32 byte or 64 byte Note: In 64 byte mode, the user must wait for RD_MST_REQ = 0h before reading the FIFO.
R18[3]	RD_ID1/0	XIN	RD_MST_REQ	RD MST RED 0h = Last data has been latched 1h = Last data is still in flight Note: In Auto mode, the user must insure that this bit is 0h and wait an additional NOP before user disables Auto mode to prevent a race condition.
R20:R19	RD_ID1/0	XOUT	RD_ADDR	Read address 48-bits 0x20 for the next read command if size is set to 32 Bytes 0x40 for the next read command if size is set to 64 Bytes The address can be the full 48-bits or just the lower 32-bits of the address, it will use the current state of the upper 16-bits

7.3.1.6 XFR2VBUS Programming Model

Write:

- Wait WR_BUSY = 0h
- One XOUT 64 Byte data and (6 Byte address or 4 Byte address) at the same time OR
- One XOUT 32 Byte data and (6 Byte address or 4 Byte address) at the same time OR
- XOUT (6 Byte address or 4 Byte address) and then XOUT 64 Byte data OR

- XOUT (6 Byte address or 4 Byte address) then XOUT 32 Byte/ 8 Byte/ 4 Byte/ 1 Byte data

Read:

- Wait RD_BUSY = 0h
- XOUT R18 (configure RD_AUTO/ RD_SIZE); R19 (RD_ADDR)
- Wait WR_BUSY = 0h OR RD_DATA_FL = 1h
- XIN RD_DATA (Repeat if RD_AUTO is enabled and need new RD_DATA, must always check RD_DATA_FL before XIN RD_DATA)

7.3.2 PRU_ICSSG XFRDMA Functional Operation

The XFRDMA block performs a translation between an XFR bus and PSI-L busses that PRU core uses for packet traffic. This allows the PRU core to directly receive and transmit packets on PSI-L, using the wide busses that PSI-L and XFR provide.

Main supported features:

- Performs a translation between XFR and PSI busses for a PRU
- Supports a configurable number of PSI-L threads, up to 32.
- Supports a configurable data width, 64, 128, or 256 bits

7.3.2.1 XFRDMA: XFR Bus

The XFRDMA block has an XFR bus with a configured data width that matches the PSI-L data width with an extra 4 Bytes for the sideband signals and fields. The XID to the XFRDMA block is used to select the PSI-L thread to access. For example XFRDMA block XID 1 is for the first thread, and XID N is for the N-th thread. The XFRDMA block will allow interleaving between PSI-L threads.

7.3.2.1.1 XFRDMA: XFR Status

The XFRDMA block uses XID 0 to read status of the PSI-L bus. An XIN to XFRDMA XID 0 returns the following data:

- Rx_ready can be used to check when there is receive data ready on a PSI-L thread.
- Tx_ready can be used to check if the XFRDMA block is able to transmit the data to that PSI-L thread without stalling.

These bits are also available as outputs that can be used for PRU core status inputs.

[Table 7-25](#) shows the device XFR status.

Table 7-25. XFR STATUS

Word	Bit	Signal	Description
0	31-0	rx_ready[3:0]	RX data ready, one bit per PSI-L thread
1	31-0	tx_ready[3:0]	Ready for TX data, one bit per PSI-L thread

7.3.2.1.2 XFRDMA: XFR Bus XOUT

The XFRDMA block will take XOUT data and translate into a transmit PSI-L packet. The first word of XFR data determines the sideband and fields for transmit and must always be present. The remaining bytes are the transmit data. The XFRDMA block assumes the contained data is correctly formatted. The XFRDMA block also assumes the data type is in the correct order, such as info words, then control, then payload, then status.

Table 7-26. XOUT STATUS

Word	Bit	Field	Description
0	0	tx_sop	Transmit has PSI-L sop signal.
0	1	tx_eop	Transmit has PSI-L eop signal.
0	2	tx_sol	Transmit has PSI-L sol signal.
0	3	tx_eol	Transmit has PSI-L eol signal.
0	4	tx_lastw	Transmit has PSI-L lastw signal, meaning that is no more data for this data_type.
0	5	tx_drop	Transmit has PSI-L drop signal.
0	11-8	tx_pkt_error[3:0]	Transmit has PSI-L pkt_error signal.
0	23-16	tx_data_type[7:0]	Transmit has PSI-L data_type signal.

Table 7-26. XOUT STATUS (continued)

Word	Bit	Field	Description
0	31-24	tx_xcnt[7:0]	Transmit byte count for XOUT, or for certain data types it is the worden[7:0] field.
1-N	31-0	tx_data	Transmit PSI-L data.

7.3.2.1.3 XFRDMA: XFR Bus XOUXFRDMA Functional Operation T Alignment

The XFRDMA block will correct for misaligned data. For a new data type value, the XFRDMA will shift the entire XFR data from the first enabled byte to the most significant byte on the PSI-L bus using big endian ordering. For continued data type values, the XFRDMA will pack the enabled bytes to the previous data until a full PSI-L line is formed and can be sent. The remaining data will start a new PSI-L line. Any leftover data when an EOP is written will be sent immediately in the next EOP data phase on the PSI-L. It is required that the XOUT have contiguous byte enables, as the XFRDMA will not account for any gaps. The XFRDMA block will update the xcnt locally for additional data, but it cannot update for data types that use the worden field, so that should be correct from the initial XOUT that started the data type.

7.3.2.1.4 XFRDMA: XFR Bus XIN

The XFRDMA block will take PSI-L packet receive data and translate it into XIN data. The first word of XFR data determines the sideband and fields for receive and must always be present. These fields also indicate how many bytes were valid, which could be 0 if there is no data present. If the PSI-L data does not fill the enabled bytes on the XFR, the remaining bytes are returned as 0s. The XFRDMA block will return all the PSI-L data in the same order as it was received. Receive data for different data_types will be returned on successive XINs and are not merged.

Table 7-27. XIN STATUS

Word	Bit	Field	Description
0	0	rx_sop	Receive has PSI-L sop signal.
0	1	rx_eop	Receive has PSI-L eop signal.
0	2	rx_sol	Receive has PSI-L sol signal.
0	3	rx_eol	Receive has PSI-L eol signal.
0	4	rx_lastw	Receive has PSI-L lastw signal, meaning that is no more data for this data_type.
0	5	rx_drop	Receive has PSI-L drop signal.
0	11-8	rx_pkt_error[3-0]	Receive has PSI-L pkt_error signal.
0	23-16	rx_data_type[7-0]	Receive has PSI-L data_type signal.
0	31-24	rx_xcnt[7-0]	Receive byte count for XIN, or for certain data types it is the worden[7:0] field.
1-N	31-0	rx_data	Receive PSI-L data.

7.3.2.1.4.1 XFRDMA: XFR Bus XIN Alignment

The source and the target entities advertise their availability to transfer data on a set of threads and the arbiter then selects one of the threads to transfer data on next. The arbiter outputs the thread ID that has been selected for transfer to both the source and target along with a request strobe to transfer data. Data is transferred in next cycle following the cycle in which the arbiter asserts the request strobe.

The XFRDMA block will correct for misaligned data. The next set of PSI-L data will be presented on the first enabled byte on the XFR bus using big endian ordering, and only the enabled number of bytes will be returned on the XFR bus. It is required that the XIN have contiguous byte enables, as the XFRDMA will not account for any gaps. The rx_xcnt will represent the valid bytes returned, and if the line is not complete then it will be 0. For data_types that use the worden signal the rx_xcnt will be the worden for the read data. The XFRDMA does not correct aligned in these worden types, so they should only be read in words.

7.3.2.2 XFRDMA: PSI-L Bus

The XFRDMA block has a pair of PSI-L busses, one for transmit and one for receive. They are using the configured data width and number of threads. The transmit PSI-L is driven by the XOUT data, while the receive PSI-L will feed the XIN data and status. When there is a transmit word ready, the XFRDMA block will assert the thread_mready for that thread. The PSI-L arbiter will determine when a thread can transmit and only then will the XFRDMA actually transmit data. The XFRDMA block will assert the thread_sready to accept receive data

when the buffer for that thread is able to accept another data phase. Again, the PSI-L arbiter will determine when a thread will receive data and only then will the buffer store the received data. Any PSI-L sideband signals are transmitted with the data phase, or received with the data phase.

The packet streaming interface (PSI) is used to transfer words of packet data and control information between two peer entities in the system via arbiter.

Figure 7-19 shows a block diagram of the PRU_ICSSG PSI topology.

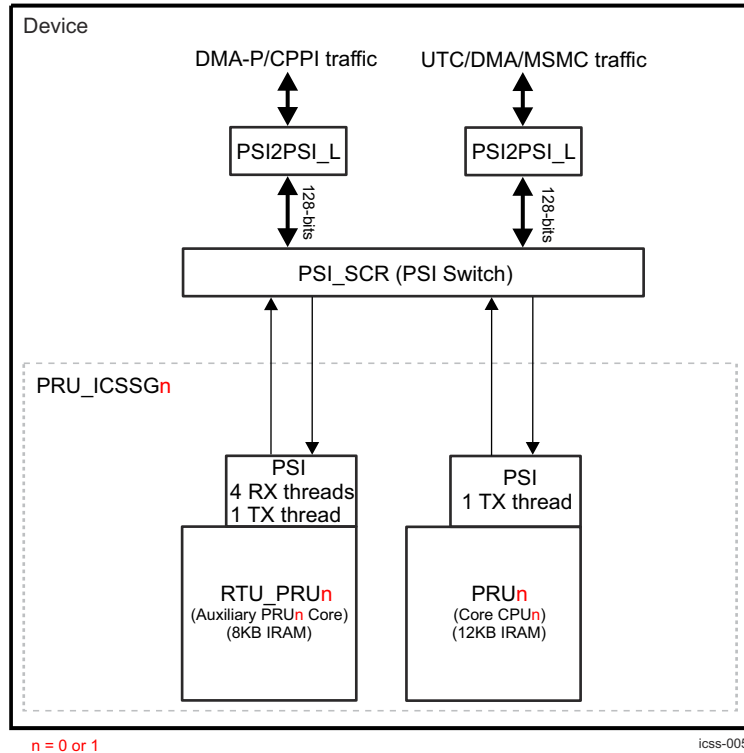


Figure 7-19. PRU_ICSSG PSI Topology

7.3.2.2.1 PRU XFRPSI Mapping

Table 7-28. PRU XFRPSI Mapping

RTU_PRUx/PRUx	xfrpsi_wgt	Note
R5:R1	[159:0] xfr_psi_wdata	R1 is metadata R2 is start of data
R5:R1	[159:0] xfr_psi_rdata	R1 is metadata R2 is start of data
bs_addr[7:4] = 4'h5	xfr_psi_req	Chip Select Decode
bs_addr[3:0]	xfr_psi_addr[3:0]	Direct Connect

7.3.2.3 XFRDMA: Temporary FIFOs

The XFRDMA block has two temporary FIFOs that store the data during the translation, one for transmit and one for receive. Each FIFO has a configurable number of data phases of storage per configured thread. Each FIFO can be accessed independently, and by both the XFR and PSI-L in the same cycle to maintain full bandwidth. For transmit the FIFO holds and packs the XOUT data until it can be sent on the PSI-L bus. For receive the FIFO holds the PSI-L data until it can be unpacked to the XIN data. A transmit FIFO that has a full data phase available or has reached the end of data for that data type is ready to transmit on the PSI-L bus. A receive FIFO that has a full data phase available or has reached the end of data for that data type is ready to receive on an XIN.

7.3.2.3.1 XFRDMA: FIFO Stalls

An XOUT to a transmit FIFO that does not have at least one empty line will result in a stall. Only when the PSI-L transmits some data for that thread, the stall will be released. An XIN to an receive FIFO that does not have a set of data will return blank data of all 0s, and the rx_bytes field will be set to 0. To avoid any transmit stalls, the associated status signal should be checked before sending the XOUT. Every XIN should check the rx_bytes field to determine the number of valid bytes, or the associated status signal should be checked to guarantee a full line of data.

7.3.3 PRU_ICSSG XFR2TR Ring Accelerator

XFR2TR ring is used for accelerating the internal memory copy of worklist from Transfer Requests (TR).

One XFR2TR ring is attached to each of the RTU_PRU cores. XFR2TR creates a Send list by doing a local memory copy of fixed (preconfigured) TR receive list to the Send list. This is accomplished by XOUT commands to define which predefined TRs to add to the list. In this case preconfigured list and Send list are stored in PRU_ICSSG shared RAM (Data RAM2).

Supported features:

- Upto 4KB of source Transfer Requests (TRs)
- 1 ring, with wrap around support along with observation of write pointer and reset write pointer
- Programmable TR size (8Bytes/ 64Bytes) and TR base for source TR queue
- Programmable TR size (8Bytes/ 64Bytes) and ring base for destination ring
- 8-level deep FIFO for TR IDs, upto 8 IDs per XOUT

Not supported features:

- External memory for TRs or Ring
- Hardware Door Bell (firmware will accomplish the Door Bell)
- Hardware Ring completion (managed by firmware)

Table 7-29. RTU_PRU to XFR2TR Ring Interface

RTU_PRU Register	BS ID	Access Type	Register	Notes
R6[17-0]	0x70	XOUT	tr_msrc_base[17-0] Needs to be mode 0x4	Controller TR list Base Address
R7[0]	0x70	XOUT	tr_size 0h: 8 Bytes 1h: 64 Bytes	Size of the TR element
R6[17-0]	0x71	XOUT	tr_rsrc_base[17-0] Needs to be mode 0x40 or 0x08 Size of TR element	Ring TR list Base Address
R7[0]	0x71	XOUT	Reserved	Reserved
R7[1]	0x71	XOUT	tr_rscr_reset	This reset the ring pointer
R7[19-8]	0x71	XOUT	tr_rsrc_nums 0 = 1 TR 4095 = 4096 TRs	The number of the TRs in the ring. This defines the Ring size, which defines the wrap around. Note: It must be larger than maximum submitted TRs. For example, XOUT of 8 TRs then, tr_rsrc_nums >= 7(8)
R7[0]	0x71	XIN	tr_rsrc_busy 0h: Not Busy 1x: Busy	The busy status. It will be busy until the FIFO is empty AND the last write completed /data has landed.
R7[11-8]	0x71	XIN	tr_rscr_fifo_occ 0h: empty 1h: 1 ID 2h: 2 IDs	The number of elements in the submit FIFO.
R8[17-0]	0x71	XIN	tr_rsrc_wrt_ptr	This is the current Write pointer

Table 7-29. RTU_PRU to XFR2TR Ring Interface (continued)

RTU_PRU Register	BS ID	Access Type	Register	Notes
R5:R2	0x72	XOUT	R2[11-0] = ID0[11-0] R2[27-16] = ID1[11-0] R3[11-0] = ID2[11-0] R3[27-16] = ID3[11-0] R4[11-0] = ID4[11-0] R4[27-16] = ID5[11-0] R5[11-0] = ID6[11-0] R5[27-16] = ID7[11-0]	Submit of TRs 1 to 8 IDs per XOUT Left packed ID0 ID1:0 No holes or offsets

7.3.3.1 XFR2TR Programming Model

This section covers the low-level programming model of the XFR2TR ring accelerator.

Typical usage model.

Initial:

- Set number of Transfer Requests (TRs)
- Set TR size
- Set source and destination address

Set A: N = 240, Size = 128B

- Loop N times, make sure that N is bigger ring size
- Push 8 TRs
- Wait for busy

New set, start fresh.

Hit reset.

Set B: N = 140, Size = 80B

- Loop N times, and make sure that N is bigger ring size
- Push 8 TRs
- Wait for busy

New set, start fresh.

Hit reset.

Set C: N = 440, Size = 120B

- Loop N times, and make sure that N is bigger ring size
- Push 8 TRs
- Wait for busy

Typical Ring size will be 100B, 120B, 250B, 512B, just defines when to wrap.

Source table linear table of 2^{12}

Source IDs, linear table

Address value

- 0<0>
- 1<1>
- 2<2>
- 3<3>
- 4<4>
- 5<5>

XOUT 0,1,2,6,3

RD Address value WR Address value

- 3<3> -> 0<3>
- 6<6> -> 1<6>

- 2<2> -> 2<2>
- 1<1> -> 3<1>
- 0<0> -> 4<0>

XOUT 20,4,7,0,1,2

RD Address value WR Address value

- 2<2> -> 5<2>
- 1<1> -> 6<1>
- 0<0> -> 7<0>
- 7<7> -> 8<7>
- 4<4> -> 9<4>
- 20<20> -> 10<20>

RD Address value WR Address value

- 2<2> -> 0<2>
- 1<1> -> 1<1>
- 0<0> -> 2<0>
- 7<7> -> 3<7>
- 4<4> -> 4<4>
- 20<20> -> 5<20>

8 PRU_ICSSG Local INTC

The PRU_ICSSG interrupt controller (INTC) maps interrupts coming from different parts of the device (mapped to PRU_ICSSGn, where n = 0 or 1) to a reduced set of PRU_ICSSG interrupt channels.

The interrupt controller has the following features:

- Capturing up to 160 Events (inputs):
 - Upper 96 are external events
 - Lower 64 are internal events
- Supports up to 20 output interrupt channels.
- Generation of 20 Host Interrupts
 - 2 Host Interrupts shared between the PRUs (PRU0 and PRU1) and TX_PRUs (TX_PRU0 and TX_PRU1).
 - 2 Host Interrupts for the RTU PRUs (RTU_PRU0 and RTU_PRU1).
 - 8 Host Interrupts exported from the PRU_ICSSG internal INTC for signaling the device level interrupt controllers (pulse and level provided).
 - 8 Host Interrupts (event 12 through 19) for the Task Managers.
- Each event can be enabled and disabled.
- Each host event can be enabled and disabled.
- Hardware prioritization of events.

8.1 PRU_ICSSG Interrupt Controller Functional Description

The PRU_ICSSG INTC supports up to 160 interrupts from different peripherals (including 64 internal interrupts from PRU_ICSSG located interrupt sources). The INTC maps these events to 20 channels inside the INTC (see [Figure 8-1](#)). Interrupts from these 20 channels are further mapped to 20 Host Interrupts.

- Any of the 160 internal interrupts can be mapped to any of the 20 channels.
- Multiple interrupts can be mapped to a single channel.
- An interrupt should not be mapped to more than one channel.
- Any of the 20 channels can be mapped to any of the 20 host interrupts. It is recommended to map channel “x” to host interrupt “x”, where x is from 0 to 19.
- A channel should not be mapped to more than one host interrupt
- For channels mapping to the same host interrupt, lower number channels have higher priority.
- For interrupts on same channel, priority is determined by the hardware interrupt number. The lower the interrupt number, the higher the priority.
- Host Interrupt 0 is connected to bit 30 in register 31 (R31) of PRU0 and PRU1 in parallel.
- Host Interrupt 1 is connected to bit 31 in register 31 (R31) for PRU0 and PRU1 in parallel.
- Host Interrupts 2 through 9 exported from PRU_ICSSG and mapped to device level interrupt controllers.
- Host Interrupt 10 is connected to bit 30 in register 31 (R31) to both RTU_PRU0 and RTU_PRU1 in parallel.
- Host Interrupt 11 is connected to bit 31 in register 31 (R31) to both RTU_PRU0 and RTU_PRU1 in parallel.
- Host Interrupts 12 through 19 are connected to each of the 6 Task Managers.

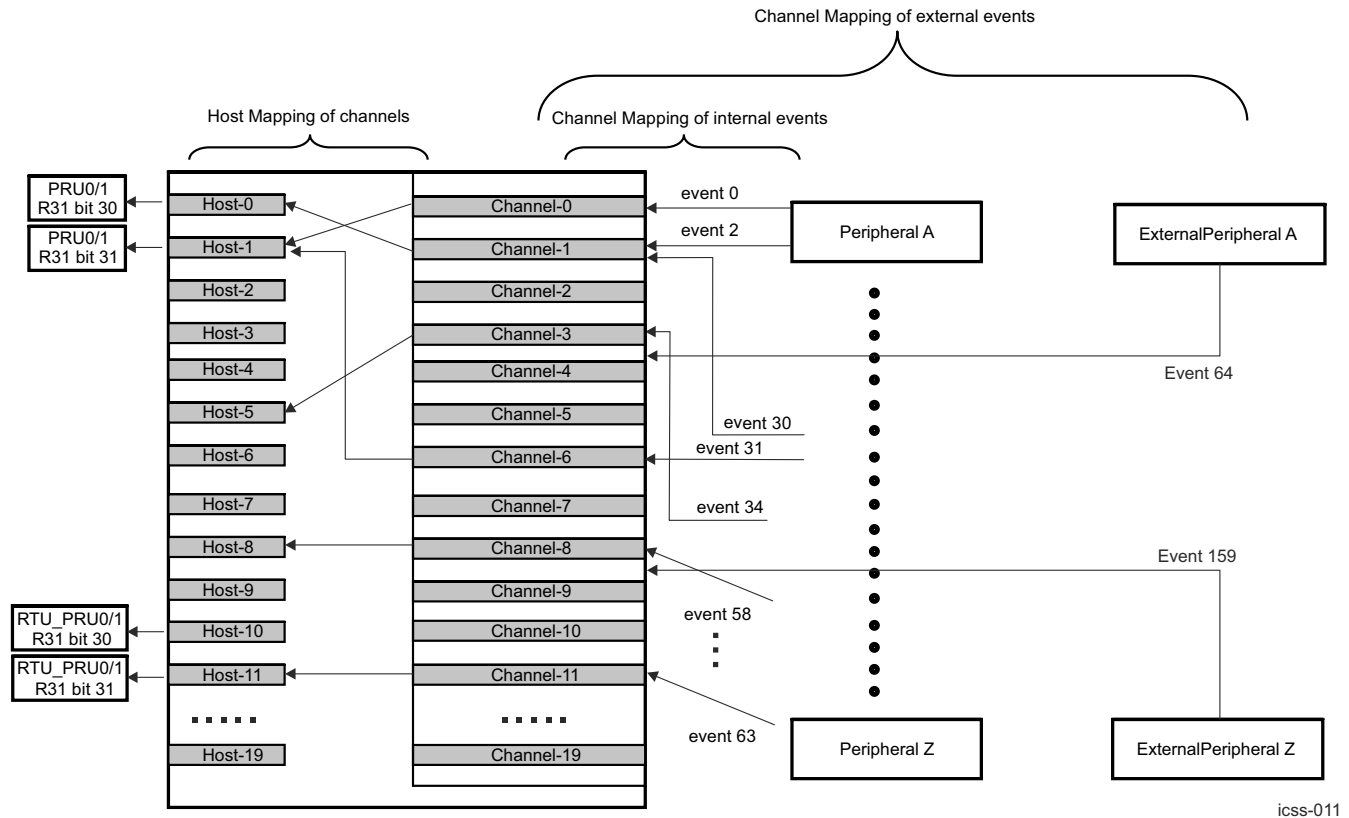


Figure 8-1. PRU_ICSSG Interrupt Controller Block Diagram

8.1.1 PRU_ICSSG Interrupt Controller Events

All 160 PRU_ICSSG system events are interrupt inputs. System events 64 through 159 are external and are generated from different peripherals. System events 0 through 63 are internal and are generated from internal for PRU_ICSSG sources.

8.1.2 PRU_ICSSG Interrupt Controller System Events Flow

The ICSS_INTC module controls the event mapping to the host interrupt interface. Events are generated by the device peripherals or PRUs. The INTC receives the internal interrupts and maps them to internal channels. The channels are used to group interrupts together and to prioritize them. These channels are then mapped onto the host interrupts. Interrupts from the system side are active high in polarity.

The INTC encompasses many functions to process the system interrupts and prepare them for the host interface. These functions are: processing, enabling, status, channel mapping, prioritization, and host interfacing. Figure 8-2 illustrates the flow of interrupts through the functions to the host. The following subsections describe each part of the flow.

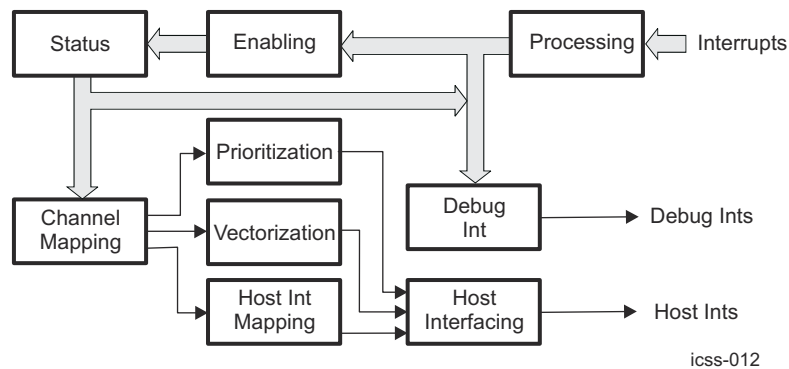


Figure 8-2. Flow of System Interrupts to Host

8.1.2.1 PRU_ICSSG Interrupt Processing

This block does following tasks:

- Synchronization of slower and asynchronous interrupts
- Conversion of polarity to active high
- Conversion of interrupt type to pulse interrupts

After the processing block, all interrupts will be active high pulses.

8.1.2.1.1 PRU_ICSSG Interrupt Enabling

The next stage of INTC is to enable interrupts based on programmed settings. The following sequence has to be followed to enable interrupts:

- Enable required interrupts: System interrupts that are required to get propagated to host are to be enabled individually by writing to [9-0] ENABLE_SET_INDEX bit field in the interrupt enable indexed set register ([ICSS_INTC_ENABLE_SET_INDEX_REG](#)). The interrupt to enable is the index value written. This sets the Enable Register bit of the given index.
- Enable required host interrupts: By writing 1h to the appropriate bit of the [9-0] HINT_ENABLE_SET_INDEX bit field in the host interrupt enable indexed set register ([ICSS_INTC_HINT_ENABLE_SET_INDEX_REG](#)), enable the required host interrupts. The host interrupt to enable is the index value written. This enables the host interrupt output or triggers the output again if that host interrupt is already enabled.
- Enable all host interrupts: By setting the [0] ENABLE_HINT_ANY bit in the global enable register ([ICSS_INTC_GLOBAL_ENABLE_HINT_REG](#)) to 1h, all host interrupts will be enabled. Individual host interrupts are still enabled or disabled from their individual enables and are not overridden by the global enable.

8.1.2.2 PRU_ICSSG Interrupt Status Checking

The next stage is to capture which interrupts are pending. There are two kinds of pending status: raw status and enabled status. Raw status is the pending status of the interrupt without regards to the enable bit for the interrupt. Enabled status is the pending status of the interrupts with the enable bits active. When the enable bit is inactive, the enabled status will always be inactive. The enabled status of interrupts is captured in interrupt status enabled/clear registers ([ICSS_INTC_ENABLE_CLR_REG0](#) to [ICSS_INTC_ENABLE_CLR_REG4](#)).

Status of interrupt 'N' is indicated by the N-th bit of [ICSS_INTC_ENABLE_CLR_REG0](#) to [ICSS_INTC_ENABLE_CLR_REG4](#). Since there are 160 interrupts, five 32-bit registers are used to capture the enabled status of interrupts. The pending status reflects whether the interrupt occurred since the last time the status register bit was cleared. Each bit in the status register can be individually cleared.

8.1.2.3 PRU_ICSSG Interrupt Channel Mapping

The INTC has 20 internal channels to which enabled interrupts can be mapped. Channel 0 has highest priority and channel 19 has the lowest priority. Channels are used to group the interrupts into a smaller number of priorities that can be given to a host interface with a very small number of interrupt inputs.

When multiple interrupts are mapped to the same channel their interrupts are ORed together so that when either is active the output is active. The channel map registers ([ICSS_INTC_CH_MAP_REGi](#), where i=0 to 39) define the channel for each interrupt. There is one register per 4 interrupts; therefore, there are 40 channel map registers for a of 160 interrupts. The channel for each interrupt can be set using these registers.

8.1.2.3.1 PRU_ICSSG Host Interrupt Mapping

The hosts can be the local PRU processors (PRU0 and PRU1) as well as device processors located outside PRU_ICSSG such as MPU Cortex-A72, etc. The 20 channels from the INTC can be mapped to any of the 20 Host interrupts. The Host map registers ([ICSS_INTC_HINT_MAP_REG0](#) to [ICSS_INTC_HINT_MAP_REG4](#)) define the channel for each interrupt. There is one register per 4 channels; therefore, there are 5 host map registers for 20 channels. When multiple channels are mapped to the same host interrupt, then prioritization is done to select which interrupt is in the highest-priority channel and which should be sent first to the host.

8.1.2.3.2 PRU_ICSSG Interrupt Prioritization

The next stage of the INTC is prioritization. Since multiple interrupts can feed into a single channel and multiple channels can feed into a single host interrupt, it is necessary to read the status of all interrupts to determine the

highest priority interrupt that is pending. The INTC provides hardware to perform this prioritization with a given scheme so that software does not have to do this. There are two levels of prioritizations:

- The first level of prioritization is between the active channels for a host interrupt. Channel 0 has the highest priority and channel 9 has the lowest. So the first level of prioritization picks the lowest numbered active channel.
- The second level of prioritization is between the active interrupts for the prioritized channel. The interrupt in position 0 has the highest priority and interrupt 159 has the lowest priority. So the second level of prioritization picks the lowest position active interrupt.

This is the final prioritized interrupt for the host interrupt and is stored in the global prioritized interrupt register ([ICSS_INTC_GLB_PRI_INTR_REG](#)). The highest priority pending interrupt with respect to each host interrupts can be obtained using the host interrupt prioritized interrupt registers ([ICSS_INTC_PRI_HINT_REGj](#) where j = 0 to 19).

8.1.2.4 PRU_ICSSG Interrupt Nesting

The INTC can also perform a nesting function in its prioritization. Nesting is a method of disabling certain interrupts (usually lower-priority interrupts) when an interrupt is taken so that only those desired interrupts can trigger to the host while it is servicing the current interrupt. The typical usage is to nest on the current interrupt and disable all interrupts of the same or lower priority (or channel). Then the host will only be interrupted from a higher priority interrupt.

The nesting is done in one of three methods:

1. Nesting for all host interrupts, based on channel priority: When an interrupt is taken, the nesting level is set to its channel priority. From then, that channel priority and all lower priority channels will be disabled from generating host interrupts and only higher priority channels are allowed. When the interrupt is completely serviced, the nesting level is returned to its original value. When there is no interrupt being serviced, there are no channels disabled due to nesting. The global nesting level register ([ICSS_INTC_GLB_NEST_LEVEL_REG](#)) allows the checking and setting of the global nesting level across all host interrupts. The nesting level is the channel (and all of lower priority channels) that are nested out because of a current interrupt.
2. Nesting for individual host interrupts, based on channel priority: Always nest based on channel priority for each host interrupt individually. When an interrupt is taken on a host interrupt, then, the nesting level is set to its channel priority for just that host interrupt, and other host interrupts do not have their nesting affected. Then for that host interrupt, equal or lower priority channels will not interrupt the host but may on other host interrupts if programmed. When the interrupt is completely serviced the nesting level for the host interrupt is returned to its original value. The host interrupt nesting level registers ([ICSS_INTC_NEST_LEVEL_REGj](#) where j = 0 to 19) display and control the nesting level for each host interrupt. The nesting level controls which channel and lower priority channels are nested. There is one register per host interrupt.
3. Software manually performs the nesting of interrupts. When an interrupt is taken, the software will disable all the host interrupts, manually update the enables for any or all the interrupts, and then re-enables all the host interrupts. This now allows only the interrupts that are still enabled to trigger to the host. When the interrupt is completely serviced the software must reverse the changes to re-enable the nested out interrupts. This method requires the most software interaction but gives the most flexibility if simple channel based nesting mechanisms are not adequate.

8.1.2.5 PRU_ICSSG Interrupt Status Clearing

After servicing the interrupt (after execution of the ISR), interrupt status is to be cleared. If a interrupt status is not cleared, then another host interrupt may not be triggered or another host interrupt may be triggered incorrectly. It is also essential to clear all interrupts before the PRU is halted as the PRU does not power down unless all the interrupt status are cleared. For clearing the status of an interrupt, whose interrupt number is N, write a 1h to the Nth bit position in the interrupt status enabled/clear registers ([ICSS_INTC_ENABLE_CLR_REG0](#) to [ICSS_INTC_ENABLE_CLR_REG4](#)). Interrupt N can also be cleared by writing the value N into the interrupt status indexed clear register ([ICSS_INTC_STATUS_CLR_INDEX_REG](#)).

8.1.3 PRU_ICSSG Interrupt Disabling

At any time, if any interrupt is not to be propagated to the host, then that interrupt should be disabled. For disabling an interrupt whose interrupt number is N, write a 1h to the Nth bit in the interrupt enable clear registers

([ICSS_INTC_ENABLE_CLR_REG0](#) to [ICSS_INTC_ENABLE_CLR_REG4](#)). Interrupt N can also be disabled by writing the value N in the interrupt enable clear index register ([ICSS_INTC_ENABLE_CLR_INDEX_REG](#)).

8.2 PRU_ICSSG Interrupt Controller Basic Programming Model

Follow these steps to configure the interrupt controller.

1. Set polarity and type of event through the Interrupt Polarity Registers ([ICSS_INTC_POLARITY_REG0](#) to [ICSS_INTC_POLARITY_REG4](#)) and the Interrupt Type Registers ([ICSS_INTC_TYPE_REG0](#) to [ICSS_INTC_TYPE_REG4](#)). Polarity of all interrupts is always high. Type of all interrupts is always pulse (after the processing block).
2. Map event to INTC channel through [ICSS_INTC_CH_MAP_REGi](#) (where i=0 to 39) channel mapping registers.
3. Map channel to host interrupt through [ICSS_INTC_HINT_MAP_REG0](#) to [ICSS_INTC_HINT_MAP_REG4](#) registers. Recommended channel “x” to be mapped to host interrupt “x”.
4. Clear interrupt by writing 1h to [ICSS_INTC_ENABLE_CLR_REG0](#) to [ICSS_INTC_ENABLE_CLR_REG4](#) registers.
5. Enable host interrupt by writing index value to [ICSS_INTC_HINT_ENABLE_SET_INDEX_REG](#) register.
6. Enable interrupt nesting if desired.
7. Globally enable all interrupts through register [ICSS_INTC_GLOBAL_ENABLE_HINT_REG\[0\]](#) [ENABLE_HINT_ANY](#) bit.

8.3 PRU_ICSSG Interrupt Requests Mapping

The PRU_ICSSGn Interrupt Controller (where n = 0 or 1) lines 0 through 63 are mapped to internal events which are generated by PRU_ICSSG integrated modules. [Table 8-1](#) shows mapping of the different PRU_ICSSG internally sourced IRQ events to PRU_ICSSG0 INTC and PRU_ICSSG1 INTC interrupt lines 0 through 63.

Table 8-1. PRU_ICSSG0 and PRU_ICSSG1 Internal Interrupts

Event Number	PRU_ICSSG Internal Interrupt Signal	Source
PRU_ICSSG0 INTC		
63	Any sd_fd_zero/one_max/min(of 72)	
62	pr0_iep1_sync0_uint_intr_pend	PRU_ICSSG0 IEP1
61	pr0_iep1_sync1_uint_intr_pend	PRU_ICSSG0 IEP1
60	pr0_iep1_latch0_uint_intr_pend	PRU_ICSSG0 IEP1
59	pr0_iep1_latch1_uint_intr_pend	PRU_ICSSG0 IEP1
58	pr0_iep1_pdi_wd_exp_pend	PRU_ICSSG0 IEP1
57	pr0_iep1_pd_wd_exp_pend	PRU_ICSSG0 IEP1
56	pr0_iep1_any_cmp_cap_pend	PRU_ICSSG0 IEP1
55	pr0_mii1_col and pr0_mii1_txen (external)if rgmii_col_crs_en MMR is set then in RGMII mode rgmii1_col will be mapped	
54	PRU1_RX_EOF	
53	MDIO_MII_LINK[1]	
52	PORT1_TX_OVERFLOW	
51	PORT1_TX_UNDERFLOW	
50	PRU1_RX_OVERFLOW	
49	PRU1_RX_NIBBLE_ODD	
48	PRU1_RX_CRC	
47	PRU1_RX_SOF	
46	PRU1_RX_SFD	
45	PRU1_RX_ERR32	
44	PRU1_RX_ERR	
43	pr0_mii0_col and pr0_mii0_txen (external)if rgmii_col_crs_en MMR is set then in RGMII mode rgmii0_col will be mapped	
42	PRU0_RX_EOF	
41	MDIO_MII_LINK[0]	
40	PORT0_TX_OVERFLOW	
39	PORT0_TX_UNDERFLOW	
38	PRU0_RX_OVERFLOW	
37	PRU0_RX_NIBBLE_ODD	
36	PRU0_RX_CRC	
35	PRU0_RX_SOF	
34	PRU0_RX_SFD	
33	PRU0_RX_ERR32	PRU_ICSSG0 PRU0
32	PRU0_RX_ERR	PRU_ICSSG0 PRU0
31	pr0_pru_mst_intr[15]_intr_req	PRU_ICSSG0 PRU0, PRU_ICSSG0 PRU1
30	pr0_pru_mst_intr[14]_intr_req	PRU_ICSSG0 PRU0, PRU_ICSSG0 PRU1
29	pr0_pru_mst_intr[13]_intr_req	PRU_ICSSG0 PRU0, PRU_ICSSG0 PRU1
28	pr0_pru_mst_intr[12]_intr_req	PRU_ICSSG0 PRU0, PRU_ICSSG0 PRU1
27	pr0_pru_mst_intr[11]_intr_req	PRU_ICSSG0 PRU0, PRU_ICSSG0 PRU1
26	pr0_pru_mst_intr[10]_intr_req	PRU_ICSSG0 PRU0, PRU_ICSSG0 PRU1

Table 8-1. PRU_ICSSG0 and PRU_ICSSG1 Internal Interrupts (continued)

Event Number	PRU_ICSSG Internal Interrupt Signal	Source
25	pr0_pru_mst_intr[9]_intr_req	PRU_ICSSG0 PRU0, PRU_ICSSG0 PRU1
24	pr0_pru_mst_intr[8]_intr_req	PRU_ICSSG0 PRU0, PRU_ICSSG0 PRU1
23	pr0_pru_mst_intr[7]_intr_req	PRU_ICSSG0 PRU0, PRU_ICSSG0 PRU1
22	pr0_pru_mst_intr[6]_intr_req	PRU_ICSSG0 PRU0, PRU_ICSSG0 PRU1
21	pr0_pru_mst_intr[5]_intr_req	PRU_ICSSG0 PRU0, PRU_ICSSG0 PRU1
20	pr0_pru_mst_intr[4]_intr_req	PRU_ICSSG0 PRU0, PRU_ICSSG0 PRU1
19	pr0_pru_mst_intr[3]_intr_req	PRU_ICSSG0 PRU0, PRU_ICSSG0 PRU1
18	pr0_pru_mst_intr[2]_intr_req	PRU_ICSSG0 PRU0, PRU_ICSSG0 PRU1
17	pr0_pru_mst_intr[1]_intr_req	PRU_ICSSG0 PRU0, PRU_ICSSG0 PRU1
16	pr0_pru_mst_intr[0]_intr_req	PRU_ICSSG0 PRU0, PRU_ICSSG0 PRU1
15	pr0_ecap_intr_req	PRU_ICSSG0 ECAP0
14	pr0_sync0_out_pend	PRU_ICSSG0 IEP0
13	pr0_sync1_out_pend	PRU_ICSSG0 IEP0
12	pr0_latch0_in (input to PRU_ICSSG0)	PRU_ICSSG0 IEP0
11	pr0_latch1_in (input to PRU_ICSSG0)	PRU_ICSSG0 IEP0
10	pr0_pdi_wd_exp_pend	PRU_ICSSG0 IEP0
9	pr0_pd_wd_exp_pend	PRU_ICSSG0 IEP0
8	pr0_digio_event_req	PRU_ICSSG0 IEP0
7	pr0_iep_tim_cap_cmp_pend	PRU_ICSSG0 IEP0
6	pr0_uart0_uint_intr_req	PRU_ICSSG0 UART0
5	pr0_uart0_utxevt_intr_req	PRU_ICSSG0 UART0
4	pr0_uart0_urxevt_intr_req	PRU_ICSSG0 UART0
3	pr0_xfr_timeout	PRU_ICSSG0 Scratch Pad
2	pr0_pru1_r31_status_cnt16	PRU_ICSSG0 PRU1 (Shift Capture)
1	pr0_pru0_r31_status_cnt16	PRU_ICSSG0 PRU0 (Shift Capture)
0	pr0_ecc_err_intr	PRU_ICSSG0 ECC Logic
PRU_ICSSG1 INTC		
63	Any sd_fd_zero/one_max/min(of 72)	
62	pr1_iep1_sync0_uint_intr_pend	PRU_ICSSG1 IEP1
61	pr1_iep1_sync1_uint_intr_pend	PRU_ICSSG1 IEP1
60	pr1_iep1_latch0_uint_intr_pend	PRU_ICSSG1 IEP1
59	pr1_iep1_latch1_uint_intr_pend	PRU_ICSSG1 IEP1
58	pr1_iep1_pdi_wd_exp_pend	PRU_ICSSG1 IEP1
57	pr1_iep1_pd_wd_exp_pend	PRU_ICSSG1 IEP1
56	pr1_iep1_any_cmp_cap_pend	PRU_ICSSG1 IEP1
55	pr1_mii1_col and pr1_mii1_txen (external)if rgmii_col_crs_en MMR is set then in RGMII mode rgmii1_col will be mapped	
54	PRU1_RX_EOF	
53	MDIO_MII_LINK[1]	
52	PORT1_TX_OVERFLOW	
51	PORT1_TX_UNDERFLOW	
50	PRU1_RX_OVERFLOW	
49	PRU1_RX_NIBBLE_ODD	
48	PRU1_RX_CRC	
47	PRU1_RX_SOF	
46	PRU1_RX_SFD	

Table 8-1. PRU_ICSSG0 and PRU_ICSSG1 Internal Interrupts (continued)

Event Number	PRU_ICSSG Internal Interrupt Signal	Source
45	PRU1_RX_ERR32	
44	PRU1_RX_ERR	
43	pr1_mii0_col and pr1_mii0_txen (external)if rgmii_col_crs_en MMR is set then in RGMII mode rgmii0_col will be mapped	
42	PRU0_RX_EOF	
41	MDIO_MII_LINK[0]	
40	PORT0_TX_OVERFLOW	
39	PORT0_TX_UNDERFLOW	
38	PRU0_RX_OVERFLOW	
37	PRU0_RX_NIBBLE_ODD	
36	PRU0_RX_CRC	
35	PRU0_RX_SOF	
34	PRU0_RX_SFD	
33	PRU0_RX_ERR32	PRU_ICSSG1 PRU0
32	PRU0_RX_ERR	PRU_ICSSG1 PRU0
31	pr1_pru_mst_intr[15]_intr_req	PRU_ICSSG1 PRU0, PRU_ICSSG1 PRU1
30	pr1_pru_mst_intr[14]_intr_req	PRU_ICSSG1 PRU0, PRU_ICSSG1 PRU1
29	pr1_pru_mst_intr[13]_intr_req	PRU_ICSSG1 PRU0, PRU_ICSSG1 PRU1
28	pr1_pru_mst_intr[12]_intr_req	PRU_ICSSG1 PRU0, PRU_ICSSG1 PRU1
27	pr1_pru_mst_intr[11]_intr_req	PRU_ICSSG1 PRU0, PRU_ICSSG1 PRU1
26	pr1_pru_mst_intr[10]_intr_req	PRU_ICSSG1 PRU0, PRU_ICSSG1 PRU1
25	pr1_pru_mst_intr[9]_intr_req	PRU_ICSSG1 PRU0, PRU_ICSSG1 PRU1
24	pr1_pru_mst_intr[8]_intr_req	PRU_ICSSG1 PRU0, PRU_ICSSG1 PRU1
23	pr1_pru_mst_intr[7]_intr_req	PRU_ICSSG1 PRU0, PRU_ICSSG1 PRU1
22	pr1_pru_mst_intr[6]_intr_req	PRU_ICSSG1 PRU0, PRU_ICSSG1 PRU1
21	pr1_pru_mst_intr[5]_intr_req	PRU_ICSSG1 PRU0, PRU_ICSSG1 PRU1
20	pr1_pru_mst_intr[4]_intr_req	PRU_ICSSG1 PRU0, PRU_ICSSG1 PRU1
19	pr1_pru_mst_intr[3]_intr_req	PRU_ICSSG1 PRU0, PRU_ICSSG1 PRU1
18	pr1_pru_mst_intr[2]_intr_req	PRU_ICSSG1 PRU0, PRU_ICSSG1 PRU1
17	pr1_pru_mst_intr[1]_intr_req	PRU_ICSSG1 PRU0, PRU_ICSSG1 PRU1
16	pr1_pru_mst_intr[0]_intr_req	PRU_ICSSG1 PRU0, PRU_ICSSG1 PRU1
15	pr1_ecap_intr_req	PRU_ICSSG1 ECAP0
14	pr1_sync0_out_pend	PRU_ICSSG1 IEP0
13	pr1_sync1_out_pend	PRU_ICSSG1 IEP0
12	pr1_latch0_in (input to PRU_ICSSG1)	PRU_ICSSG1 IEP0
11	pr1_latch1_in (input to PRU_ICSSG1)	PRU_ICSSG1 IEP0
10	pr1_pdi_wd_exp_pend	PRU_ICSSG1 IEP0
9	pr1_pd_wd_exp_pend	PRU_ICSSG1 IEP0
8	pr1_digio_event_req	PRU_ICSSG1 IEP0
7	pr1_iep_tim_cap_cmp_pend	PRU_ICSSG1 IEP0
6	pr1_uart0_uint_intr_req	PRU_ICSSG1 UART0
5	pr1_uart0_utxevt_intr_req	PRU_ICSSG1 UART0
4	pr1_uart0_urxevt_intr_req	PRU_ICSSG1 UART0
3	pr1_xfr_timeout	PRU_ICSSG1 Scratch Pad
2	pr1_pru1_r31_status_cnt16	PRU_ICSSG1 PRU1 (Shift Capture)
1	pr1_pru0_r31_status_cnt16	PRU_ICSSG1 PRU0 (Shift Capture)

Table 8-1. PRU_ICSSG0 and PRU_ICSSG1 Internal Interrupts (continued)

Event Number	PRU_ICSSG Internal Interrupt Signal	Source
0	pr1_ecc_err_intr	PRU_ICSSG1 ECC Logic

The IRQ input lines 64 through 159 receive interrupts which come from various device peripherals located outside PRU_ICSSG system. They are delivered on the PRU_ICSSG Interrupt Controller inputs (64 through 159).

9 PRU_ICSSG UART Module

This section describes an Universal Asynchronous Receive and Transmit (UART) module integrated into each of the PRU_ICSSG subsystems, named respectively - PRU_ICSSG0_UART0 and PRU_ICSSG1_UART0. Hereinafter the module will be referred as PRU_ICSSG UART0.

9.1 PRU_ICSSG UART Overview

The PRU_ICSSG UART0 peripheral is based on the industry standard TL16C550 asynchronous communications element, which in turn is a functional upgrade of the TL16C450. The information in this chapter assumes that user is familiar with these standards.

Functionally similar to the TL16C450 on power up (single character or TL16C450 mode), the PRU_ICSSG UART0 can be placed in an alternate FIFO (TL16C550) mode. This relieves the CPU of excessive software overhead by buffering received and transmitted characters. The receiver and transmitter FIFOs store up to 16 bytes including three additional bits of error status per byte for the receiver FIFO.

The PRU_ICSSG UART0 performs serial-to-parallel conversions on data received from a peripheral device and parallel-to-serial conversion on data received from the CPU. The CPU can read the PRU_ICSSG UART0 status at any time. The PRU_ICSSG UART0 includes control capability and a processor interrupt system that can be tailored to minimize software management of the communications link.

The PRU_ICSSG UART0 includes a programmable baud generator capable of dividing the PRU_ICSSG UART0 input clock by divisors from 1 to 65535 and producing a 16× reference clock or a 13× reference clock for the internal transmitter and receiver logic.

9.2 PRU_ICSSG UART Environment

This section describes the PRU_ICSSG UART0 module interface to the device environment.

9.2.1 PRU_ICSSG UART Pin Multiplexing

Pin multiplexing is controlled using a combination of hardware configuration at device reset and software programmable register settings. For more information on the PRU_ICSSG UART0 pin multiplexing, refer to the [#unique_160referenceTitle](#), *Pad Configuration Registers* in the chapter, *CTRL_MMR0*.

9.2.2 PRU_ICSSG UART Signal Descriptions

The PRU_ICSSG UART0 utilize a minimal number of signal connections to interface with external devices. The PRU_ICSSG UART0 signal descriptions are described in [Table 9-1](#).

Table 9-1. PRUSS_UART0 Signal Descriptions

Signal Name	Signal Type	Function
UART0_TXD	Output	Serial data transmit
UART0_RXD	Input	Serial data receive
UART0_CTS	Input	Clear-to-Send handshaking signal
UART0_RTS	Output	Request-to-Send handshaking signal

9.2.3 PRU_ICSSG UART Protocol Description and Data Format

9.2.3.1 PRU_ICSSG UART Transmission Protocol

The PRU_ICSSG UART0 transmitter section includes a transmitter hold register (THR), memory mapped in the register [UART_RBR_TBR](#)[17-8] TBR_DATA bitfield and a transmitter shift register (TSR), which is NOT memory mapped. When the PRU_ICSSG UART0 is in the FIFO mode, THR is a 16-byte FIFO. Transmitter section control is a function of the PRU_ICSSG UART0 line control register [UART_LCTR](#). Based on the settings chosen in this register, the PRU_ICSSG UART0 transmitter sends the following to the receiving device:

- 1 START bit
- 5, 6, 7, or 8 data bits
- 1 PARITY bit (optional)
- 1, 1.5, or 2 STOP bits

THR receives data from the internal data bus, and when TSR (transmitter shift register) is ready, the PRU_ICSSG UART0 moves the data from THR to TSR. The PRU_ICSSG UART0 serializes the data in TSR and transmits the data on the UART0_TXD pin.

In the non-FIFO mode, if THR is empty and the Transmitter Holding Register Empty interrupt (THRE) is enabled in the interrupt enable register ([UART_INT_EN\[1\] ETBEI](#)), an interrupt is generated. This interrupt is cleared when a character is loaded into THR or the interrupt identification register [UART_INT_FIFO](#) bitfield [3-1] IIR_INTID is read. In the FIFO mode, the interrupt is generated when the transmitter FIFO is empty, and it is cleared when at least one byte is loaded into the FIFO or [UART_INT_FIFO\[3-1\] IIR_INTID](#) bitfield is read.

9.2.3.2 PRU_ICSSG UART Reception Protocol

The PRU_ICSSG UART0 receiver section includes a receiver shift register (RSR), that is not memory mapped, and a receiver buffer register (RBR), memory mapped as the register [UART_RBR_TBR\[7-0\] RBR_DATA](#) bitfield. When the PRU_ICSSG UART0 is in the FIFO mode, RBR is a 16-byte FIFO. Receiver section control is a function of the PRU_ICSSG UART0 line control register - [UART_LCTR](#). Based on the settings chosen in this register, the PRU_ICSSG UART0 receiver accepts the following from the transmitting device:

- 1 START bit
- 5, 6, 7, or 8 data bits
- 1 PARITY bit (optional)
- 1 STOP bit (any other STOP bits transferred with the above data are not detected)

RSR receives the data bits from the UART0_RXD pin. Then RSR concatenates the data bits and moves the resulting value into RBR (or the receiver FIFO), accessible in the [RBR_TBR\[7-0\] RBR_DATA](#) register bitfield. The PRU_ICSSG UART0 also stores three bits of error status information next to each received character, to record a parity error, framing error, or break.

In the non-FIFO mode, when a character is placed in RBR and the receiver data available interrupt is enabled in the interrupt enable register - [UART_INT_EN\[0\] ERBI](#), an interrupt is generated. This interrupt is cleared when the character is read from RBR. In the FIFO mode, the interrupt is generated when the FIFO is filled to the trigger level selected in the FIFO control MSB part of the register [UART_INT_FIFO](#), and it is cleared when the FIFO contents drop below the trigger level.

9.2.3.3 PRU_ICSSG UART Data Format

The PRU_ICSSG UART0 transmits in the following format:

1 START bit + data bits (5, 6, 7, 8) + 1 PARITY bit (optional) + STOP bit (1, 1.5, 2)

It transmits 1 START bit; 5, 6, 7, or 8 data bits, depending on the data width selection; 1 PARITY bit, if parity is selected; and 1, 1.5, or 2 STOP bits, depending on the STOP bit selection.

The PRU_ICSSG UART0 receives in the following format:

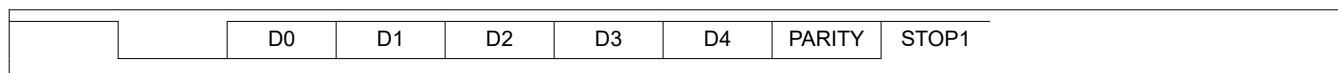
1 START bit + data bits (5, 6, 7, 8) + 1 PARITY bit (optional) + 1 STOP bit

It receives 1 START bit; 5, 6, 7, or 8 data bits, depending on the data width selection; 1 PARITY bit, if parity is selected; and 1 STOP bit.

The protocol formats are shown in [Figure 9-1](#).

Figure 9-1. PRU_ICSSG UART Protocol Formats

Transmit/Receive for 5-bit data, parity Enable, 1 STOP bit



Transmit/Receive for 6-bit data, parity Enable, 1 STOP bit



Transmit/Receive for 7-bit data, parity Enable, 1 STOP bit

		D0	D1	D2	D3	D4	D5	D6	PARITY	STOP1

Transmit/Receive for 8-bit data, parity Enable, 1 STOP bit

		D0	D1	D2	D3	D4	D5	D6	D7	PARITY	STOP1

9.2.3.3.1 Frame Formatting

Character length is specified using the [UART_LCTR\[0\]](#) WLS0 and [UART_LCTR\[1\]](#) WLS1 bits (see [Table 9-3](#)).

The number of stop-bits is specified using the [UART_LCTR\[2\]](#) STB bit (see [Table 9-3](#)).

The parity bit is programmed using the [UART_LCTR\[5\]](#) SP, [UART_LCTR\[4\]](#) EPS, and [UART_LCTR\[3\]](#) PEN bits (see [Table 9-2](#)).

Table 9-2. Relationship Between SP, EPS, and PEN Bits in LCTR

SP Bit	EPS Bit	PEN Bit	Parity Option
x	x	0	Parity disabled: No PARITY bit is transmitted or checked.
0	0	1	Odd parity selected: Odd number of logic 1s.
0	1	1	Even parity selected: Even number of logic 1s.
1	0	1	Stick parity selected with PARITY bit transmitted and checked as set.
1	1	1	Stick parity selected with PARITY bit transmitted and checked as cleared.

Table 9-3. Number of STOP Bits Generated

STB Bit	WLS Bit	Word Length Selected with WLS Bits	Number of STOP Bits Generated	Baud Clock (BCLK) Cycles
0	x	Any word length	1	16
1	0h	5 bits	1.5	24
1	1h	6 bits	2	32
1	2h	7 bits	2	32
1	3h	8 bits	2	32

9.2.4 PRU_ICSSG UART Clock Generation and Control

The PRU_ICSSG UART0 bit clock is derived from an input clock to the PRU_ICSSG UART0. See the device-specific Datasheet to check the maximum data rate supported by the PRU_ICSSG UART0.

[Figure 9-2](#) is a conceptual clock generation diagram for the PRU_ICSSG UART0. The processor clock generator receives a signal from an external clock source and produces a PRU_ICSSG UART0 input clock with a programmed frequency. The PRU_ICSSG UART0 contains a programmable baud generator that takes an input clock and divides it by a divisor in the range between 1 and $(2^{16} - 1)$ to produce a baud clock (BCLK). The frequency of BCLK is sixteen times ($16\times$) the baud rate (each received or transmitted bit lasts 16 BCLK cycles) or thirteen times ($13\times$) the baud rate (each received or transmitted bit lasts 13 BCLK cycles). When the PRU_ICSSG UART0 is receiving, the bit is sampled in the 8th BCLK cycle for $16\times$ over sampling mode and on the 6th BCLK cycle for $13\times$ over-sampling mode. The $16\times$ or $13\times$ reference clock is selected by configuring the mode definition register: [UART_MODE\[0\]](#) OSM_SEL bit. The formula to calculate the divisor is:

$$\text{Divisor} = \frac{\text{UART input clock frequency}}{\text{Desired baud rate} \times 16} \quad [\text{MODE.OSM\_SEL} = 0\text{h}]$$

icss-13

$$\text{Divisor} = \frac{\text{UART input clock frequency}}{\text{Desired baud rate} \times 13} \quad [\text{MODE.OSM\_SEL} = 1\text{h}]$$

icss-14

Two 8-bit register fields:

- [UART_DIVMSB\[7-0\]](#) DLH
- [UART_DIVLSB\[7-0\]](#) DLL,

called divisor latches, hold this 16-bit divisor. DLH holds the most significant bits of the divisor, and DLL holds the least significant bits of the divisor. For information about these register fields, see the PRU_ICSSG UART0 register descriptions in the *PRU_UART_UART0 Registers*. These divisor latches must be loaded during initialization of the PRU_ICSSG UART0 in order to ensure desired operation of the baud generator. Writing to the divisor latches results in two wait states being inserted during the write access while the baud generator is loaded with the new value.

Figure 9-3 summarizes the relationship between the transferred data bit, BCLK, and the PRU_ICSSG UART0 input clock. Note that the timing relationship depicted in Figure 9-3 shows that each bit lasts for 16 BCLK cycles. This is in case of 16x over-sampling mode. For 13x over-sampling mode each bit lasts for 13 BCLK cycles.

Example baud rates and divisor values relative to a 150 MHz PRU_ICSSG UART0 input clock and 16x over-sampling mode are shown in Table 9-4.

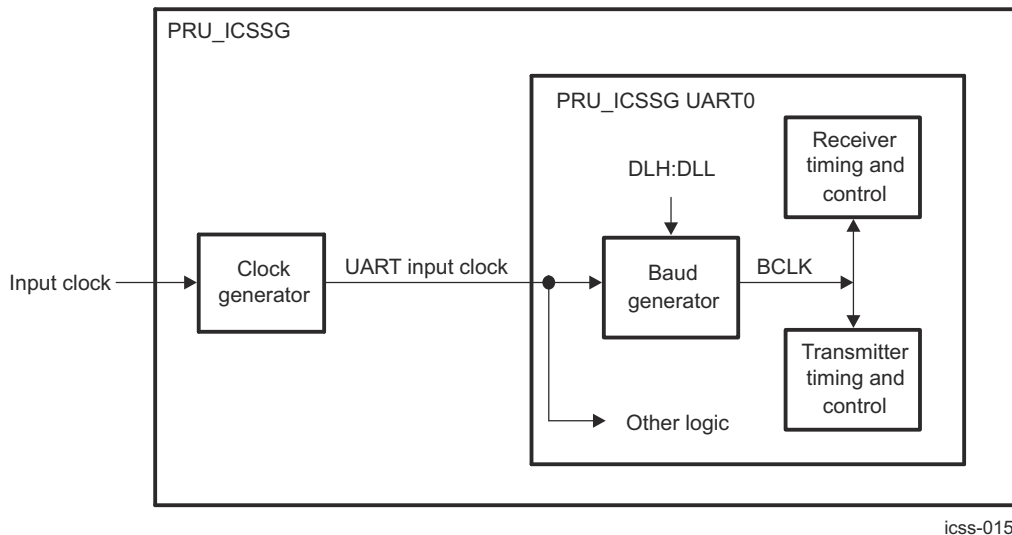


Figure 9-2. PRU_ICSSG UART Clock Generation Diagram

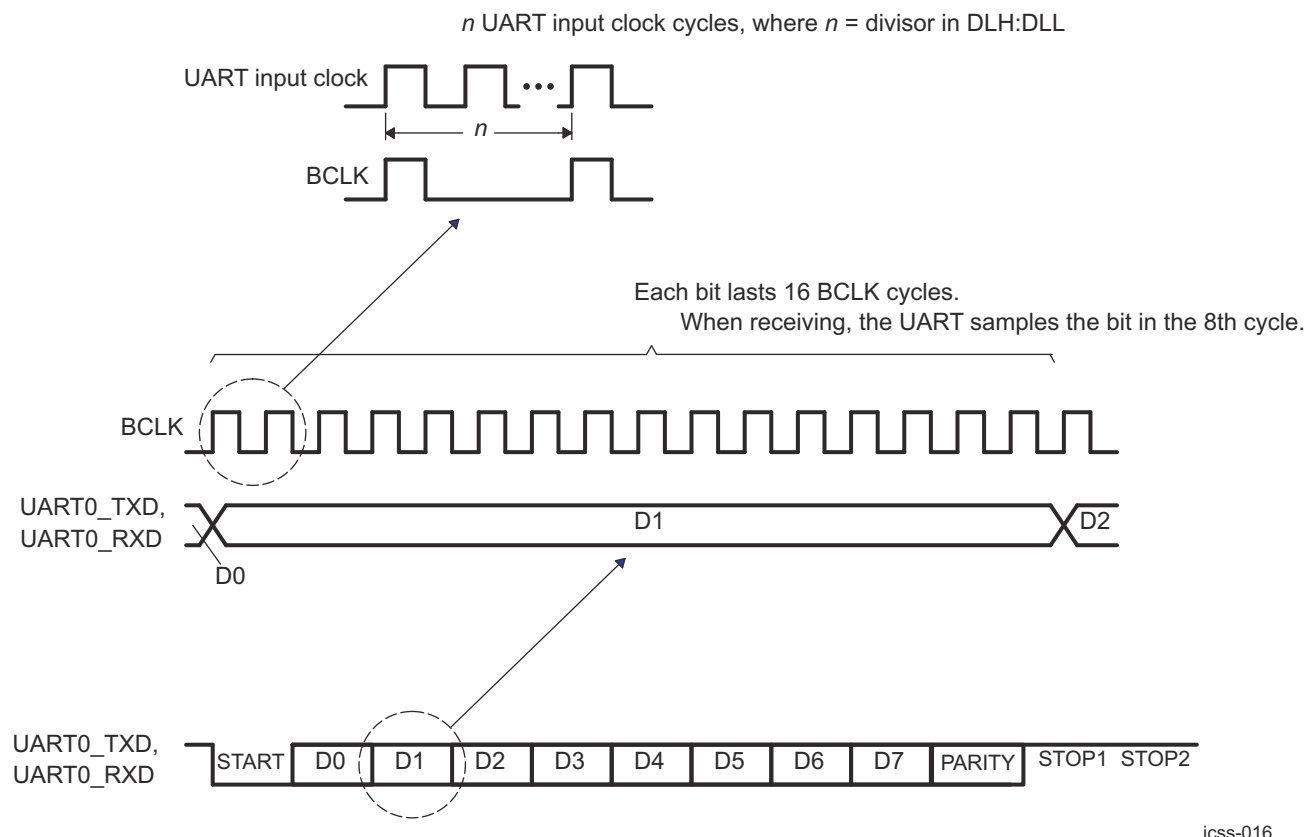


Figure 9-3. Relationships Between PRU_ICSSG UART Data Bit, BCLK, and Input Clock

Table 9-4. Baud Rate Examples for 192-MHZ PRU_ICSSG UART Input Clock and 16× Over-sampling Mode

Baud Rate	Divisor Value	Actual Baud Rate	Error (%)
2400	5000	2400	0.00
4800	2500	4800	0.00
9600	1250	9600	0.00
19200	625	19200	0.00
38400	313	38338.658	-0.16
56000	214	56074.766	0.13
115200	104	115384.6	0.16
128000	94	127659.574	-0.27
3000000	4	3000000	0.00
6000000	2	3000000	0.00
12000000	1	12000000	12000000

Table 9-5. Baud Rate Examples for 192-MHZ PRU_ICSSG UART Input Clock and 13× Over-sampling Mode

Baud Rate	Divisor Value	Actual Baud Rate	Error (%)
2400	6154	2399.940	-0.0025
4800	3077	4799.880	-0.0025
9600	1538	9602.881	0.03
19200	769	19205.762	0.03
38400	385	38361.638	-0.10
56000	264	55944.056	-0.10
115200	128	115384.6	0.16
128000	115	128428.094	0.33

9.3.1 PRU_ICSSG UART Functional Block Diagram

A functional block diagram of the PRU ICSSG UART0

A functional block diagram of the PRU_ICSSG UART0 is shown in [Figure 9-4](#).



NOTE: The value *n* indicates the applicable UART where there are multiple instances. For the PRU_ICSSG, there is only one instance and all UART signals should reflect this (e.g., UART0_TXD instead of UART*n*_TXD).

Figure 9-4. PRU_ICSSG UART Block Diagram

9.3.2 PRU_ICSSG UART Reset Considerations

9.3.2.1 PRU_ICSSG UART Software Reset Considerations

Two bits in the power and emulation management register - [UART_PWR](#), control resetting the parts of the PRU_ICSSG UART0:

- The bit [14]UTRST controls resetting the transmitter only. If bit [14]UTRST = 1h, the transmitter is enabled and active;
if bit [14]UTRST = 0h, the transmitter is disabled and in reset state.
- The bit [13]URRST controls resetting the receiver only. If [13]URRST = 1h, the receiver is enabled and active;
if bit [13]URRST = 0h, the receiver is disabled and in reset state.

In each case, putting the receiver and/or transmitter in reset will reset the state machine of the affected portion but will not affect the PRU_ICSSG UART0 registers.

9.3.2.2 PRU_ICSSG UART Hardware Reset Considerations

When the processor RESET pin is asserted, the entire processor is reset and is held in the reset state until the RESET pin is released. As part of a device reset, the PRU_ICSSG UART0 state machine is reset and the PRU_ICSSG UART0 registers are forced to their default states. The default states of the registers are shown in .

9.3.3 PRU_ICSSG UART Power Management

The PRU_ICSSG UART0 peripheral can be placed in reduced-power modes to conserve power during periods of low activity. The power management of the PRU_ICSSG UART0 peripheral and other PRU_ICSSG peripherals is controlled by the device Power Sleep Controller (PSC). The PSC acts as a controller for power management for all of the peripherals on the device. For more details on the power management procedures using the PSC, refer to the [#unique_175referenceTitle](#), *Power Management*.

9.3.4 PRU_ICSSG UART Interrupt Support

9.3.4.1 PRU_ICSSG UART Interrupt Events and Requests

The PRU_ICSSG UART0 generates the interrupt requests described in [Table 9-6](#). All requests are multiplexed through an arbiter to a single PRU_ICSSG UART0 interrupt request to the CPU, as shown in [Figure 9-5](#). Each of the interrupt requests has an enable bit in the interrupt enable register (IER) - [UART_INT_EN](#) and is recorded in [3-1]IIR_INTID bitfield of [UART_INT_FIFO](#) register.

If an interrupt occurs and the corresponding enable bit is set to 1h, the interrupt request is recorded in corresponding [UART_INT_FIFO](#)[3-1] IIR_INTID bitfield and is forwarded to the CPU. If an interrupt occurs and the corresponding enable bit is cleared to 0h, the interrupt request is blocked. The interrupt request is neither recorded in [UART_INT_FIFO](#)[3-1] IIR_INTID, nor forwarded to the CPU.

9.3.4.2 PRU_ICSSG UART Interrupt Multiplexing

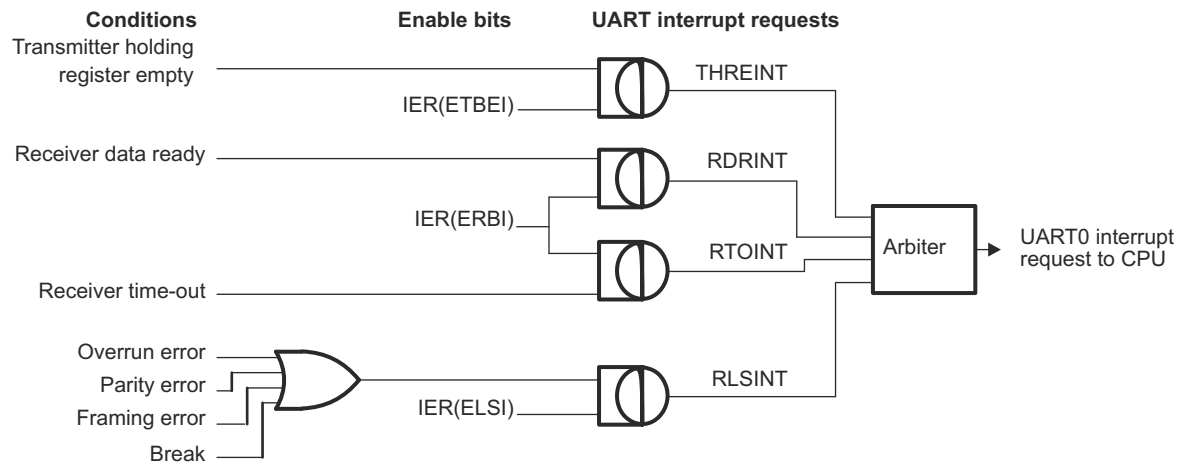
The PRU_ICSSG UART0 have dedicated interrupt signals to the CPU and the interrupts are not multiplexed with any other interrupt source.

Table 9-6. PRU_ICSSG UART Interrupt Requests Descriptions

PRU_ICSSG UART0 Interrupt Request	Interrupt Source	Comment
THREINT	THR-empty condition: The transmitter holding register (THR) or the transmitter FIFO is empty. All of the data has been copied from THR, (i.e. UART_RBR_TBR [7-0] RBR_DATA) to the transmitter shift register (TSR).	If THREINT is enabled in UART_INT_EN register by setting the [1]ETBEI bit, it is recorded in [3-1]IIR_INTID bitfield. As an alternative to using THREINT, the CPU can poll the THRE bit in the line status register UART_LSR1 .
RDAINT	Receive data available in non-FIFO mode or trigger level reached in the FIFO mode.	If RDAINT is enabled in UART_INT_EN register, by setting the [0]ERBI bit, it is recorded in INTID bitfield. As an alternative to using RDAINT, the CPU can poll the [0]DR bit in the line status register UART_LSR1 . In the FIFO mode, this is not a functionally equivalent alternative because the [0]DR bit does not respond to the FIFO trigger level. The [0]DR bit only indicates the presence or absence of unread characters.

Table 9-6. PRU_ICSSG UART Interrupt Requests Descriptions (continued)

PRU_ICSSG UART0 Interrupt Request	Interrupt Source	Comment
RTOINT	Receiver time-out condition (in the FIFO mode only): No characters have been removed from or input to the receiver FIFO during the last four character times (see Table 9-8), and there is at least one character in the receiver FIFO during this time.	The receiver time-out interrupt prevents the PRU_ICSSG UART0 from waiting indefinitely, in the case when the receiver FIFO level is below the trigger level and thus does not generate a receiver data-ready interrupt. If RTOINT is enabled in UART_INT_EN register, by setting the [0]ERBI bit, it is recorded in UART_INT_FIFO[3-1] IIR_INTID bitfield. There is no status bit to reflect the occurrence of a time-out condition.
RLSINT	Receiver line status condition: An overrun error, parity error, framing error, or break has occurred.	If RLSINT is enabled in INT_EN register, by setting the [2]ELSI bit, it is recorded in UART_INT_FIFO[3-1] IIR_INTID bitfield. As an alternative to using RLSINT, the CPU can poll the following bits in the line status register UART_LSR1 : overrun error indicator (bit [1]OE), parity error indicator (bit [2]PE), framing error indicator ([3]FE), and break indicator ([4]BI).



icss-018

Figure 9-5. PRU_ICSSG UART Interrupt Request Enable Paths

9.3.5

Table 9-7. Interrupt Identification and Interrupt Clearing Information

Priority Level	IIR Bits				Interrupt Type	Interrupt Source	Event That Clears Interrupt
	3	2	1	0			
None	0	0	0	1	None	None	None
1	0	1	1	0	Receiver line status	Overrun error, parity error, framing error, or break is detected.	For an overrun error, reading the line status register UART_LSR1 , clears the interrupt. For a parity error, framing error, or break, the interrupt is cleared only after all the erroneous data have been read.
2	0	1	0	0	Receiver data-ready	Non-FIFO mode: Receiver data is ready.	Non-FIFO mode: The receiver buffer register (RBR) is read.
						FIFO mode: Trigger level reached. If four character times pass with no access of the FIFO, the interrupt is asserted again.	FIFO mode: The FIFO drops below the trigger level. ⁽¹⁾
2	1	1	0	0	Receiver time-out	FIFO mode only: No characters have been removed from or input to the receiver FIFO during the last four character times and there is at least one character in the receiver FIFO during this time.	One of the following events: - A character is read from the receiver FIFO ⁽¹⁾ - A new character arrives in the receiver FIFO - The [13]URRST bit in the power and emulation management register (UART_PWR) is loaded with 0h.
3	0	0	1	0	Transmitter holding register empty	Non-FIFO mode: Transmitter holding register (THR) is empty.	A character is written to the transmitter holding register (UART_RBR_TBR) or the interrupt identification register (UART_INT_FIFO) is read.
						FIFO mode: Transmitter FIFO is empty.	

(1) In the FIFO mode, the receiver data-ready interrupt or receiver time-out interrupt is cleared by the CPU or by the DMA controller, whichever reads from the receiver FIFO first.

9.3.6 PRU_ICSSG UART DMA Event Support

In the FIFO mode, the PRU_ICSSG UART0 generates the following two DMA events:

- Receive event (URXEVT):** The trigger level for the receiver FIFO (1, 4, 8, or 14 characters) is set with the FIFO control [UART_INT_FIFO](#)[7-6] IIR_FIFOEN bitfield. Every time the trigger level is reached or a receiver time-out occurs, the PRU_ICSSG UART0 sends a receive event to the DMA controller. In response, the DMA controller reads the data from the receiver FIFO by way of the receiver buffer register [UART_RBR_TBR](#)[7-0] RBR_DATA. Note that the receive event is not asserted if the data at the top of the receiver FIFO is erroneous even if the trigger level has been reached.
- Transmit event (UTXEVT):** When the transmitter FIFO is empty (when the last byte in the transmitter FIFO has been copied to the transmitter shift register), the PRU_ICSSG UART0 sends an UTXEVT signal to the DMA controller. In response, the DMA controller refills the transmitter FIFO by way of the transmitter holding register (THR) - [UART_RBR_TBR](#)[7-0] RBR_DATA. The UTXEVT signal is also sent to the DMA controller when the PRU_ICSSG UART0 is taken out of reset using the [14]UTRST bit in the power and emulation management register ([UART_PWR](#)).

Activity in DMA channels can be synchronized to these events. In the non-FIFO mode, the PRU_ICSSG UART0 generates no DMA events. Any DMA channel synchronized to either of these events must be enabled at the time the PRU_ICSSG UART0 event is generated. Otherwise, the DMA channel will miss the event and, unless the PRU_ICSSG UART0 generates a new event, no data transfer will occur.

9.3.7 PRU_ICSSG UART Operations

9.3.7.1 PRU_ICSSG UART FIFO Modes

The following two modes can be used for servicing the receiver and transmitter FIFOs:

- FIFO interrupt mode. The FIFO is enabled and the associated interrupts are enabled. Interrupts are sent to the CPU to indicate when specific events occur.
- FIFO poll mode. The FIFO is enabled but the associated interrupts are disabled. The CPU polls status bits to detect specific events.

Because the receiver FIFO and the transmitter FIFO are controlled separately, either one or both can be placed into the interrupt mode or the poll mode.

9.3.7.1.1 PRU_ICSSG UART FIFO Interrupt Mode

When the receiver FIFO is enabled in the FIFO control register (FCR), mapped in the MSB part of the register [UART_INT_FIFO](#), and the receiver interrupts are enabled in the interrupt enable register [UART_INT_EN](#), the interrupt mode is selected for the receiver FIFO. The following are important points about the receiver interrupts:

- The receiver data-ready interrupt is issued to the CPU when the FIFO has reached the trigger level that is programmed in FCR. It is cleared when the CPU or the DMA controller reads enough characters from the FIFO such that the FIFO drops below its programmed trigger level.
- The receiver line status interrupt is generated in response to an overrun error, a parity error, a framing error, or a break. This interrupt has higher priority than the receiver data-ready interrupt. For details, see [Section 9.3.4](#).
- The data-ready ([0]DR) bit in the line status register - [UART_LSR1](#), indicates the presence or absence of characters in the receiver FIFO. The [0]DR bit is set when a character is transferred from the receiver shift register (RSR) to the empty receiver FIFO. The [0]DR bit remains set until the FIFO is empty again.
- A receiver time-out interrupt occurs if all of the following conditions exist:
 - At least one character is in the FIFO,
 - The most recent character was received more than four continuous character times ago. A character time is the time allotted for 1 START bit, n data bits, 1 PARITY bit, and 1 STOP bit, where n depends on the word length selected with the WLS0 and WLS1 bits of the line control register [UART_LCTR](#). See [Table 9-8](#).
 - The most recent read of the FIFO has occurred more than four continuous character times before.
- Character times are calculated by using the baud rate.
- When a receiver time-out interrupt has occurred, it is cleared and the time-out timer is cleared when the CPU or the EDMA controller reads one character from the receiver FIFO. The interrupt is also cleared if a new character is received in the FIFO or if the URRST bit is cleared in the power and emulation management register - PWM.
- If a receiver time-out interrupt has not occurred, the time-out timer is cleared after a new character is received or after the CPU or EDMA reads the receiver FIFO.

When the transmitter FIFO is enabled in [UART_INT_FIFO\[0\] IIR_IPEND](#) bit and the transmitter holding register empty (THRE) interrupt is enabled in [UART_INT_EN\[1\] ETBEI](#) bit, the interrupt mode is selected for the transmitter FIFO. The THRE interrupt occurs when the transmitter FIFO is empty. It is cleared when the transmitter hold register (THR) [UART_RBR_TBR\[7-0\] RBR_DATA](#) bitfield is loaded (1 to 16 characters may be written to the transmitter FIFO while servicing this interrupt) or the [3-1]IIR_INTID bitfield is read in the interrupt identification register [UART_INT_FIFO](#).

Table 9-8. Character Time for Word Lengths

Word Length (n)	Character Time	Four Character Times
5	Time for 8 bits	Time for 32 bits
6	Time for 9 bits	Time for 36 bits
7	Time for 10 bits	Time for 40 bits
8	Time for 11 bits	Time for 44 bits

9.3.7.1.2 PRU_ICSSG UART FIFO Poll Mode

When the receiver FIFO is enabled in the FIFO control register (via setting the [UART_INT_FIFO\[0\] IIR_IPEND](#) to 1h) and the receiver interrupts are disabled in the interrupt enable register ([UART_INT_EN](#)), the poll mode is selected for the receiver FIFO. Similarly, when the transmitter FIFO is enabled via setting the same bit ([UART_INT_FIFO\[0\] IIR_IPEND](#) to 1h) and the transmitter interrupts are disabled, the transmitted FIFO is in the poll mode. In the poll mode, the CPU detects events by checking bits in the line status register - [UART_LSR1](#):

- The [UART_LSR1\[7\] RXFIFOE](#) bit indicates whether there are any errors in the receiver FIFO.
- The [UART_LSR1\[6\] TEMT](#) bit indicates that both the transmitter holding register (THR) and the transmitter shift register (TSR) are empty.
- The [UART_LSR1\[5\] THRE](#) bit indicates when THR (mapped in the [UART_RBR_TBR\[7-0\] RBR_DATA](#) bitfield) is empty.
- The following line status register - [UART_LSR1](#) bits specify which error or errors have occurred:
 - [UART_LSR1\[4\] BI](#) - Break Interrupt

- [UART_LSR1\[3\]](#) FE – Framing Error
- [UART_LSR1\[2\]](#) PE – Parity Error
- [UART_LSR1\[1\]](#) OE – Overrun Error
- The [UART_LSR1\[0\]](#) DR (data-ready) bit is set as long as there is at least one byte in the receiver FIFO.

Also, in the FIFO poll mode:

- The interrupt identification ([3-1] IIR_INTID) bit field in register [UART_INT_FIFO](#) are not affected by any events because the interrupts are disabled.
- The PRU_ICSSG UART0 does not indicate when the receiver FIFO trigger level is reached or when a receiver time-out occurs.

9.3.7.2 PRU_ICSSG UART Autoflow Control

The PRU_ICSSG UART0 can employ autoflow control by connecting the [UART0_CTS](#) and [UART0_RTS](#) signals. The [UART0_CTS](#) input must be active before the transmitter FIFO can transmit data. The [UART0_RTS](#) becomes active when the receiver needs more data and notifies the sending device. When [UART0_RTS](#) is connected to [UART0_CTS](#), data transmission does not occur unless the receiver FIFO has space for the data. Therefore, when two UARTs are connected as shown in [Figure 9-6](#) with autoflow enabled ([UART_MCTR\[5\]](#) AFE = 1h), overrun errors are eliminated.

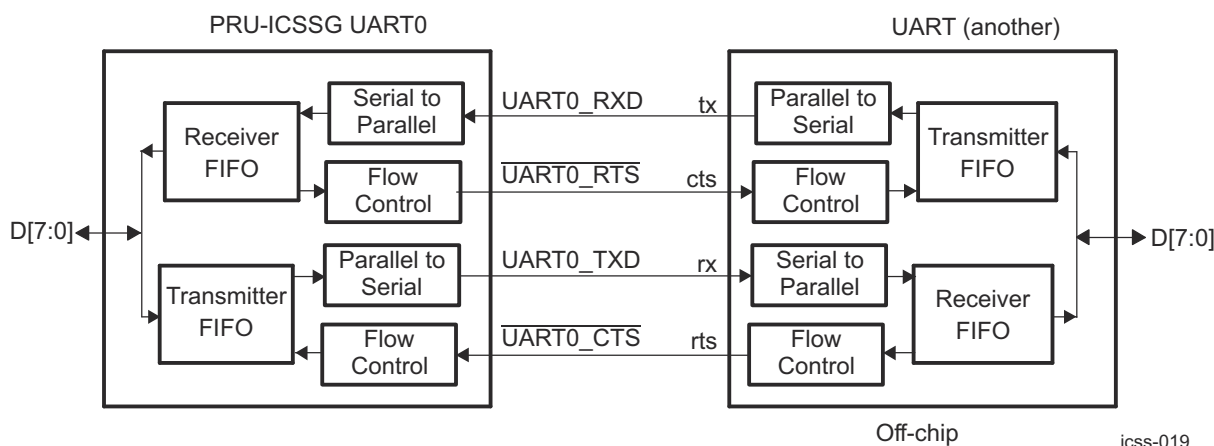
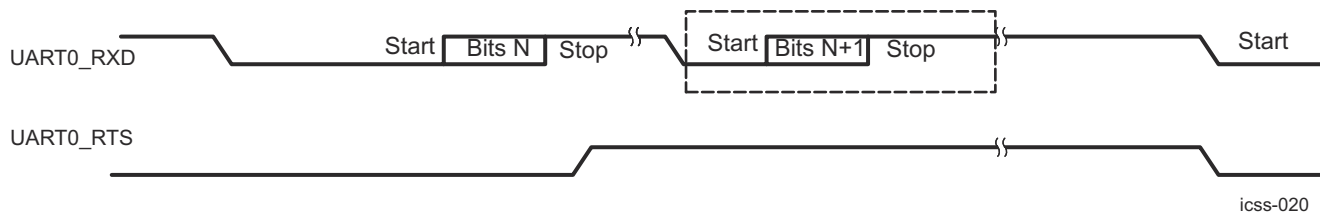


Figure 9-6. UART Interface Using Autoflow Diagram

9.3.7.2.1 PRU_ICSSG UART Signal [UART0_RTS](#) Behavior

[UART0_RTS](#) data flow control originates in the receiver block (see [Figure 9-4](#)). When the receiver FIFO level reaches a trigger level of 1, 4, 8, or 14 (see [Figure 9-7](#)), [UART0_RTS](#) is deasserted. The sending UART may send an additional byte after the trigger level is reached (assuming the sending UART has another byte to send), because it may not recognize the deassertion of [UART0_RTS](#) until after it has begun sending the additional byte. For trigger level 1, 4, and 8, [UART0_RTS](#) is automatically reasserted once the receiver FIFO is emptied. For trigger level 14, [UART0_RTS](#) is automatically reasserted once the receiver FIFO drops below the trigger level.

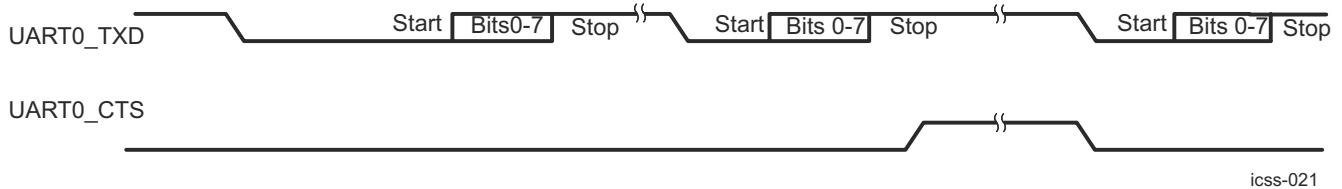


- N = Receiver FIFO trigger level.
- The two blocks in dashed lines cover the case where an additional byte is sent.

Figure 9-7. Autoflow Functional Timing Waveforms for [UART0_RTS](#)

9.3.7.2.2 PRU_ICSSG UART Signal $\overline{\text{UART0\_CTS}}$ Behavior

The transmitter checks $\overline{\text{UART0\_CTS}}$ before sending the next data byte. If $\overline{\text{UART0\_CTS}}$ is active, the transmitter sends the next byte. To stop the transmitter from sending the following byte, $\overline{\text{UART0\_CTS}}$ must be released before the middle of the last STOP bit that is currently being sent (see Figure 9-8). When flow control is enabled, $\overline{\text{UART0\_CTS}}$ level changes do not trigger interrupts because the device automatically controls its own transmitter. Without autoflow control, the transmitter sends any data present in the transmitter FIFO and a receiver overrun error may result.



- A. When $\overline{\text{UART0\_CTS}}$ is active (low), the transmitter keeps sending serial data out.
- B. When $\overline{\text{UART0\_CTS}}$ goes high before the middle of the last STOP bit of the current byte, the transmitter finishes sending the current byte but it does not send the next byte.
- C. When $\overline{\text{UART0\_CTS}}$ goes from high to low, the transmitter begins sending data again.

Figure 9-8. Autoflow Functional Timing Waveforms for $\overline{\text{UART0\_CTS}}$

9.3.7.3 PRU_ICSSG UART Loopback Control

The PRU_ICSSG UART0 can be placed in the diagnostic mode using the [4]LOOP bit in the modem control register - **UART_MCTR**, which internally connects the PRU_ICSSG UART0 output back to the PRU_ICSSG UART0's input. In this mode, the transmit and receive data paths, the transmitter and receiver interrupts, and the modem control interrupts can be verified without connecting to another UART.

9.3.8 PRU_ICSSG UART Emulation Considerations

The [0]FREE bit in the power and emulation management register (**UART_PWR**) determines how the PRU_ICSSG UART0 responds to an emulation suspend event such as an emulator halt or breakpoint. If bit **UART_PWR[0] FREE** = 0h and a transmission is in progress, the PRU_ICSSG UART0 halts after completing the one-word transmission; if bit **UART_PWR[0] FREE** = 0h and a transmission is not in progress, the PRU_ICSSG UART0 halts immediately. If **UART_PWR[0] FREE** = 1h, the PRU_ICSSG UART0 does not halt and continues operating normally.

Note also that most emulator accesses are transparent to PRU_ICSSG UART0 operation. Emulator read operations do not affect any register contents, status bits, or operating states, with the exception of the interrupt identification register (**UART_INT_FIFO**). Emulator writes, however, may affect register contents and may affect PRU_ICSSG UART0 operation, depending on what register is accessed and what value is written.

The PRU_ICSSG UART0 registers can be read from or written to during emulation suspend events, even if the PRU_ICSSG activity has stopped.

9.3.9 PRU_ICSSG UART Exception Processing

9.3.9.1 PRU_ICSSG UART Divisor Latch Not Programmed

Since the processor reset signal has no effect on the divisor latch, the divisor latch will have an unknown value after power up. If the divisor latch is not programmed after power up, the baud clock (BCLK) will not operate and will instead be set to a constant logic 1 state.

The divisor latch values should always be reinitialized following a processor reset.

9.3.9.2 Changing Operating Mode During Busy Serial Communication of PRU_ICSSG UART

Since the serial link characteristics are based on how the control registers are programmed, the PRU_ICSSG UART0 module will expect the control registers to be static while it is busy engaging in a serial communication. Therefore, changing the control registers while the module is still busy communicating with another serial device will most likely cause an error condition and should be avoided.

10 PRU_ICSSG ECAP Module

10.1 PRU_ICSSG ECAP Functional Description

A single instance of an Enhanced Capture event module (ECAP0) is integrated in each device PRU_ICSSG0 and PRU_ICSSG1 subsystem.

For more details on the PRU_ICSSG0 and PRU_ICSSG1 ECAP0 I/O signals available at device level, refer to the [Section 3, PRU_ICSSG Environment](#).

For PRU_ICSSG0 and PRU_ICSSG1 ECAP0 integration details and functionalities, controlled at PRU_ICSSG top level (functional clock control, etc.), refer to the [Section 4, PRU_ICSSG Integration](#) and the [Section 5, PRU-ICSS Top Level Resources Functional Description](#).

Note

The PRU_ICSSG0 and PRU_ICSSG1 ECAP0 "SYNC In" hardware event synchronization input and "SYNC Out" hardware synchronization output are implemented in the device PRU_ICSSG0 and PRU_ICSSG1 respectively. However, a software-forced synchronization via bit [ECAP_ECCTL2_ECCTL1\[24\]](#) SWSYNC, can be used as an alternative, provided that [ECAP_ECCTL2_ECCTL1\[21\]](#) SYNCI_EN bit is set to 1h.

For full description of the PRU_ICSSG0, PRU_ICSSG1 and PRU_ICSSG2 ECAP0 modules and functionalities, refer to the [#unique_196referenceTitle](#), *Enhanced Capture (eCAP) Module*.

11 PRU_ICSSG PWM Module

Each of the PRU_ICSSG modules integrates one Pulse Width Modulation module (PWM). The PWM module uses IEP0 and IEP1 compare events to produce the PWM outputs.

11.1 PRU_ICSSG PWM Supported Features

PRU_ICSSG PWM module supports the following features:

- Supports up to 4 sets of 3 phased motor control with 12 primary and 12 complimentary programmable PWM outputs
- Very flexible Real Time options
 - Up to 9 events with optional external trip IO per PWM set with hardware glitch filter and programmable mask through ICSSG_PWMn[16-8] PWM0_TRIP_MASK (where n = 0 to 2)
 - Hardware compares from IO loopback with hardware glitch filter
 - Supports Sigma Delta (SD) fast detect circuit
- Very flexible PWM output behavior, configurable through state configuration registers: PWMn_0 to PWMn_2 (where n = 0 to 2):
 - Programmable Initial State
 - Programmable Trip State
 - Programmable Active State
- Hardware glitch filters can debounce a glitch from 1 to 255 ICSSG_CORE_CLK counts

Figure 11-1 and Figure 11-2 shows block diagrams of the PRU_ICSSG PWM.

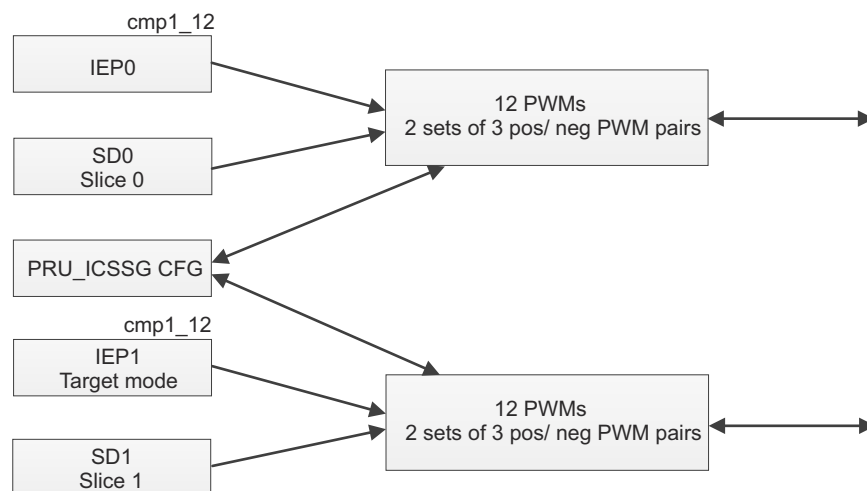


Figure 11-1. PRU_ICSSG PWM Block Diagram

Note

PRGn_PWMm_A[2:0] = PRGn_PWMm_[2:0]_POS and PRGn_PWMm_B[2:0] = PRGn_PWMm_[2:0]_NEG.

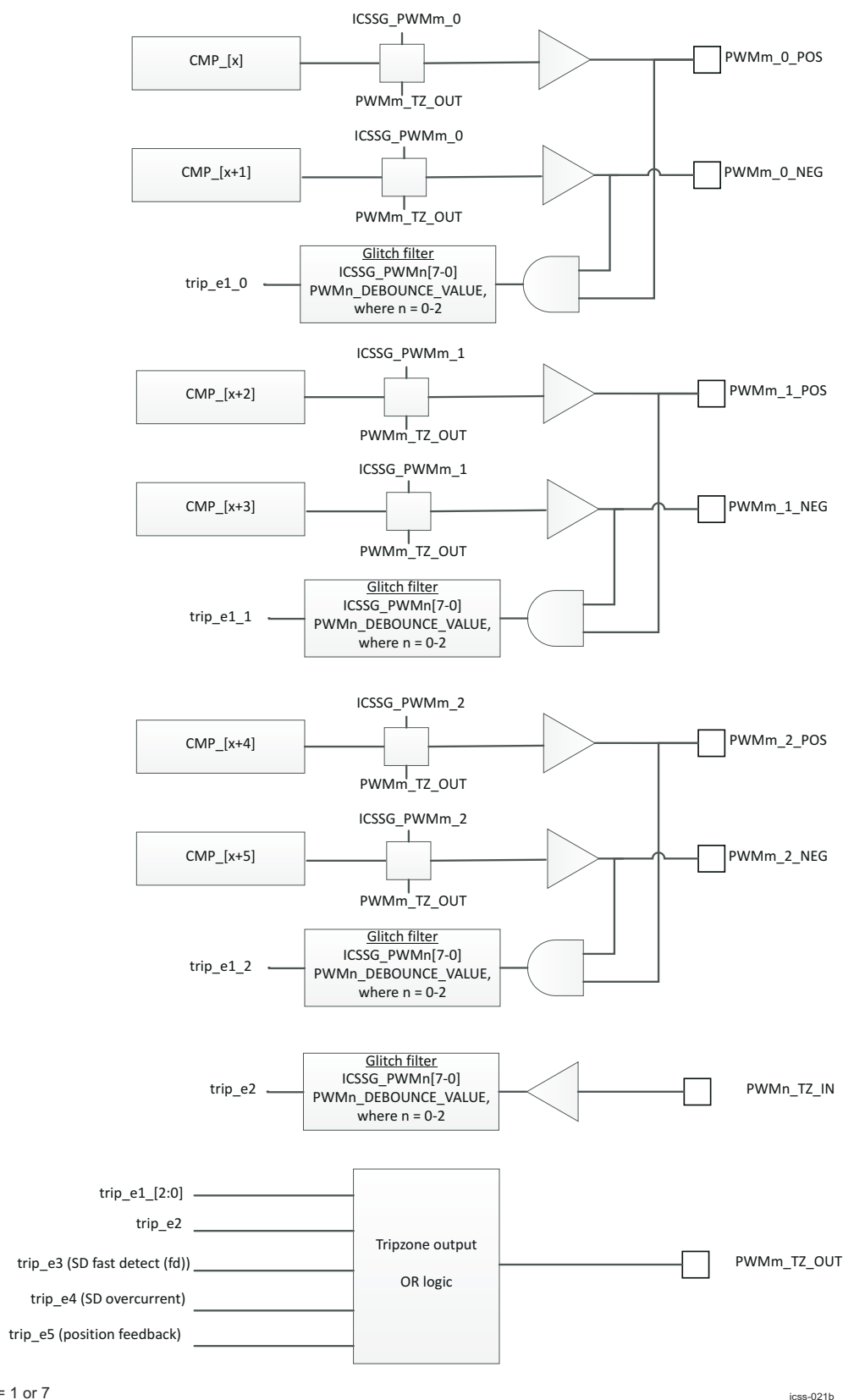


Figure 11-2. PRU_ICSSG PWM I/O Block Diagram

11.2 PRU_ICSSG PWM States Overview

The PWM module has three states (initial, active, and trip), which are shared between PRGn_PWMm_[2:0]_POS and PRGn_PWMm_[2:0]_NEG pins (where n = 0 to 2 and m = 0 to 3). The output value for each pin, however, is unique and is defined in the ICSSG CFG registers. Figure 11-3 shows the PWM module states.

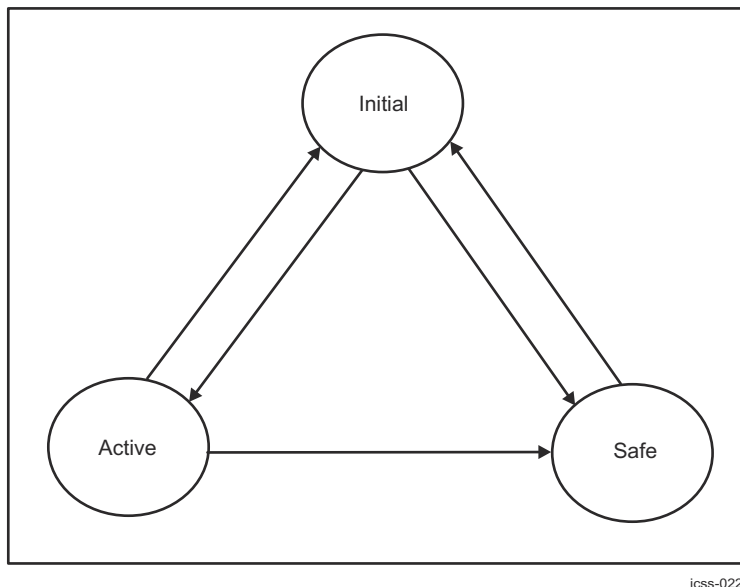


Figure 11-3. Three State Diagram

Each state supports different entry events. Table 11-1 shows a summary of the different entry options.

Table 11-1. Summary of Entry Events

State	Entry Event
Initial	- Hardware reset event - Trip reset event, ICSSG_PWMm[18] PWMm_TRIP_RESET (where m = 0 to 3) - IEP0.CMP0
Active	CMPx event associated with the PWMm set (where m = 0 to 3), as shown in Table 11-3
Trip	PRGn_PWM_m_TRIP_OUT (where n = 0 to 2 and m = 0 to 3) event of that PWMm set

Table 11-2. State Transition Mapping

Current State	Next State	Event causing transition
X	Initial	Hardware reset event
Trip	Initial	Trip reset event or IEP0.CMP0 (if enabled)
Active	Initial	Trip reset event or IEP0.CMP0 (if enabled)
Initial	Active	First CMPx event associated with the PWMm set
X	Safe	PRGn_PWM_m_TRIP_OUT (where n = 0 to 2 and m = 0 to 3) event

Table 11-3. PWM to IEP CMP Mapping

PWM	IEP CMP
PWM0_0_POS	IEP0 CMP1
PWM0_0_NEG	IEP0 CMP2
PWM0_1_POS	IEP0 CMP3
PWM0_1_NEG	IEP0 CMP4
PWM0_2_POS	IEP0 CMP5
PWM0_2_NEG	IEP0 CMP6

Table 11-3. PWM to IEP CMP Mapping (continued)

PWM	IEP CMP
PWM1_0_POS	IEP0 CMP7
PWM1_0_NEG	IEP0 CMP8
PWM1_1_POS	IEP0 CMP9
PWM1_1_NEG	IEP0 CMP10
PWM1_2_POS	IEP0 CMP11
PWM1_2_NEG	IEP0 CMP12
PWM2_0_POS	IEP1 CMP1
PWM2_0_NEG	IEP1 CMP2
PWM2_1_POS	IEP1 CMP3
PWM2_1_NEG	IEP1 CMP4
PWM2_2_POS	IEP1 CMP5
PWM2_2_NEG	IEP1 CMP6
PWM3_0_POS	IEP1 CMP7
PWM3_0_NEG	IEP1 CMP8
PWM3_1_POS	IEP1 CMP9
PWM3_1_NEG	IEP1 CMP10
PWM3_2_POS	IEP1 CMP11
PWM3_2_NEG	IEP1 CMP12

11.3 PRU_ICSSG PWM Trip State Logic

The trip logic is common for each set of PRGn_PWMm_[2:0]_POS and PRGn_PWMm_[2:0]_NEG pins (where n = 0 to 2 and m = 0 to 3). This logic is responsible for monitoring the “error” inputs and producing a PRGn_PWM_m_TRIP_OUT event, which is used to trip the I/O into a predefined trip state.

The I/O will remain in this trip state until the CMP0 event (if enabled) or trip software reset occurs. After clearing of these events (through [ICSSG_PWM0](#)[17] PWM0_TRIP_CMP0_EN bit or [18] PWMm_TRIP_RESET, where m = 0 to 3), then the I/Os will be in the initial state until the first IEP0/1_CMP_INTR_PEND_P[15:0] event occurs that corresponds to a particular PRGn_PWMm_[2:0]_POS or PRGn_PWMm_[2:0]_NEG set of pins. The first compare event occurrence corresponding to that PWMm set will cause all I/Os of that PWMm set to go into an active state. Subsequent compare events will cause the I/Os to toggle.

Note

The SoC pad is in default tristate and the internal weak pull-down resistor is enabled. Before PRU_ICSSG PWM to be exported, the software needs to execute initialization sequence along with the IEP0 and IEP1.

The following registers are used to configure the trip signals:

- [ICSSG_PWM0](#)
- [ICSSG_PWM1](#)
- [ICSSG_PWM2](#)
- [ICSSG_PWM3](#)

11.4 PRU_ICSSG PWM Glitch Filter

The glitch filter is a block which is used to reject pulses smaller than width, defined in the [ICSSG_PWM0](#)[7-0] PWMm_DEBOUNCE_VALUE. For example, if bit field [7-0] PWM0_DEBOUNCE_VALUE is set to 10h, a pulse which is less than 16 x ICSSG_CORE_CLK clock cycles will be filtered.

12 PRU_ICSSG MII_G_RT Module

12.1 PRU_ICSSG MII_G_RT Introduction

The Real-time Media Independent Interface (MII_G_RT) provides a programmable I/O interface for the PRUs to access and control up to two MII ports. The MII_G_RT module can also be configured to push and pull data independent of the PRU cores.

Note

In order to guarantee the MII_G_RT I/O timing values published in the device data sheet, the PRU_ICSSG ICSSGn_CORE_CLK (where n = 0 or 1) core clock must be configured for 200 MHz, 225 MHz or 250 MHz and the TX_CLK_DELAYn (where n = 0 or 1) bit field in the [MII_RT_TXCFG0/1](#) register must be set to 0h (default value).

12.1.1 PRU_ICSSG MII_G_RT Features

The PRU_ICSSG MII_G_RT module supports:

- Two MII ports
 - Each MII port has:
 - 32-Bytes RX L1 FIFO
 - 64-Bytes RX L2 FIFO (two memory banks: Bank0 = 32-Bytes and Bank1 = 32-Bytes)
 - 40-Bytes TX L1 FIFO one per port
 - 64-Bytes TX L2 FIFO one per port
 - Rate decoupling on TX L1 FIFO
 - Configurable pre-amble removal on RX L1 FIFO and insertion on TX L1 FIFO
 - Sync frame delimiter detection
 - Configurable TX L1 FIFO trigger (10 bits with 40 ns ticks)
- MII port multiplexer per direction to support line/ring structure
 - Link detection through RX_ERR
- Cyclic redundancy check (CRC)
 - CRC32 generation on TX path
 - CRC32 checker on RX path

12.1.2 Unsupported Features

The PRU_ICSSG MII_G_RT module does not support:

- Auto padding in TX L1 FIFO
- Dynamic TX multiplexer switching during packet handling:
 - Can allow one PRU to handle both MII interfaces and a second PRU to manage the host and switch functions.

12.1.3 PRU_ICSSG MII_G_RT Block Diagram

[Figure 12-1](#) shows the MII_G_RT in context of the PRU_ICSSG.

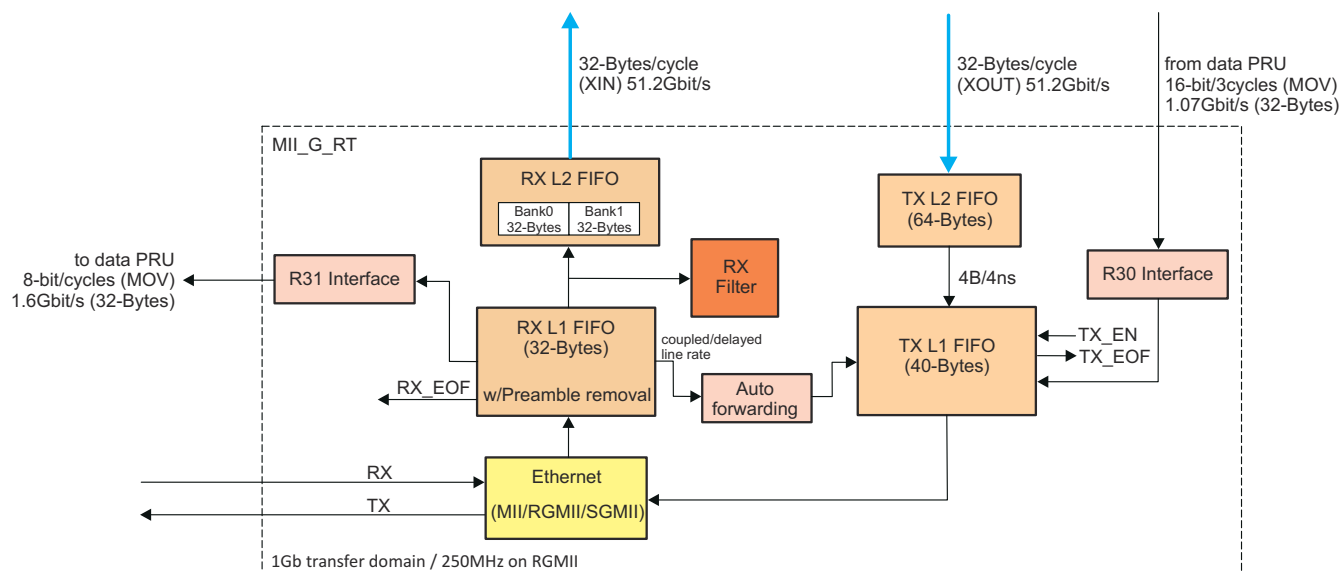


Figure 12-1. PRU_ICSSG MII_G_RT Block Diagram

12.2 MII_G_RT Functional Description

12.2.1 MII_G_RT Data Path Configuration

The MII_G_RT module supports three basic data path configurations. These configurations are compared in [Table 12-1](#) and described in the following sections.

Table 12-1. MII_G_RT Data Path Configuration Comparison

Configuration	PRU Dependency	Data Servicing	Port-to-Port Latency
Auto-forward	Snoop only	One word in flight	Low
8- or 16-bit processing with on-the-fly modifications (RX L1)	Yes	One word or byte in flight	Low
32-byte double buffer or ping-pong processing (RX L2)	Yes	Multi-words in flight	Medium (application-dependent)

12.2.1.1 Auto-forward with Optional PRU Snoop

Data is automatically forwarded from the MII RX port to the MII TX port without manipulations, as shown in [Figure 12-2](#). This configuration does not depend on the PRU core. However, it does support an option for PRU to snoop or monitor the received data through the RX L2, shown in [Figure 12-3](#). The PRU does not access data and status bits through R31, and it does not modify and push data.



Figure 12-2. Auto-forward

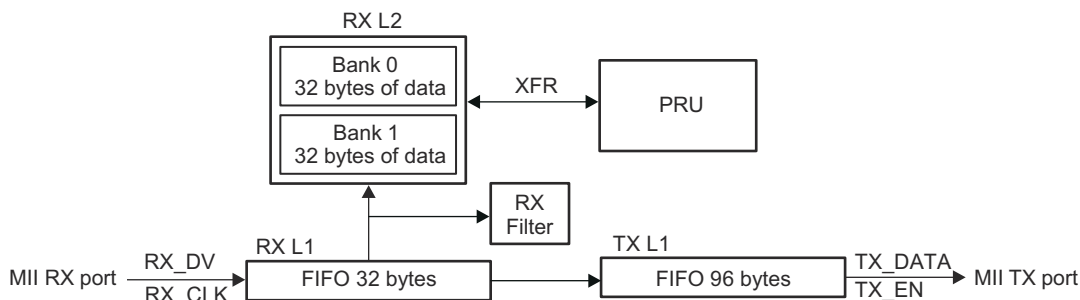


Figure 12-3. Auto-forward with PRU Snoop

12.2.1.2 8- or 16-bit Processing with On-the-Fly Modifications

This configuration services one byte or word in flight and has low latency. The PRU has the option to manipulate the received word and control popping data from the RX L1 FIFO and pushing it on the TX L1 FIFO.

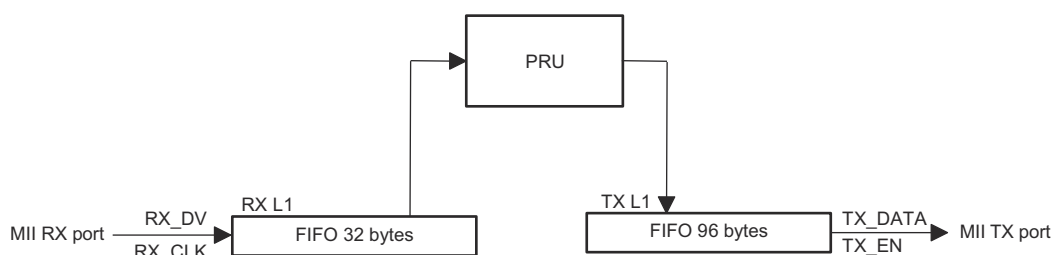


Figure 12-4. 8- or 16-bit Processing with On-the-Fly Modifications

12.2.1.3 32-byte Double Buffer or Ping-Pong Processing

This configuration supports high bandwidth, high efficiency transactions. Often implementations using this mode permit relaxed servicing requirements allowing the PRU to manipulate the received data before transmitting.

Data received in this configuration is passed into the RX L2 buffer. The PRU reads multiple bytes of data from one of the RX L2 banks through the high bandwidth broadside interface and XFR instructions. The PRU can then store or manipulate data before pushing it to the TX L1 FIFO for transmission on the MII TX port.

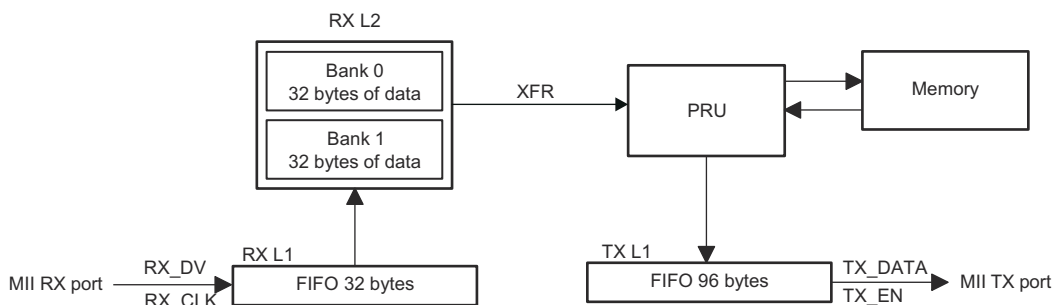


Figure 12-5. 32-byte Double Buffer or Ping-Pong Processing

12.2.2 MII_G_RT Definition and Terms

12.2.2.1 MII_G_RT Data Frame Structure

The data received and transmitted over MII conforms with the frame structure shown in [Table 7-16](#).

Table 12-2. MII_G_RT Frame Structure

Inter-frame	Preamble	Start of Frame Delimiter (SFD)	Data	Cyclic Redundancy Check (CRC)

The data following the SFD is formatted in a 4-bit nibble structure. [Figure 12-6](#) illustrates the nibble order. The MSB arriving first is on the LSB side of a nibble. When receiving data, the MII_G_RT receive logic will wait for the next nibble to arrive before constructing a byte and delivering to the PRU.

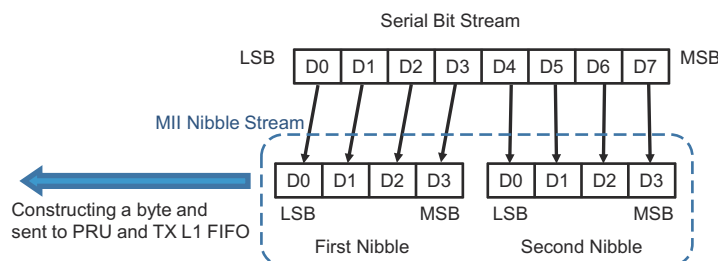


Figure 12-6. Data Nibble Structure

12.2.2.2 PRU R30 and R31

The PRU registers R30 and R31 are used to receive, transmit, and control the data for the PRU. As shown in [Figure 12-7](#), the R31 is used to access data in the RX L1 FIFO, the R30 is used to transmit data from the PRU, and the R31 output is used to control the flow of receive and transmit. For more details about these registers, see the following sections.

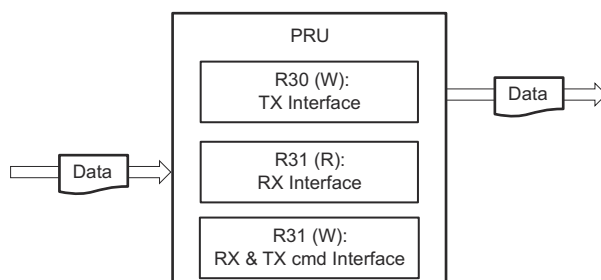


Figure 12-7. PRU R30, R31 Operations

12.2.2.3 RX and TX L1 FIFO Data Movement

To advance the next data byte seen by R31, the PRU must pop the data from the RX L1 FIFO. Likewise, the PRU can push the data from R30 to the TX L1 FIFO. These operations are illustrated in [Figure 12-8](#).

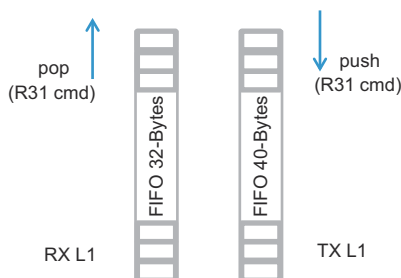


Figure 12-8. Reading and Writing FIFO Data

12.2.2.4 Receive CRC Computation

For the incoming data, the MII_G_RT calculates CRC32 and then compares against the value provided in the incoming frame. If there is a mismatch, the MII_G_RT signals ERROR_CRC to the PRU. If a previous node or Ethernet device appended an error nibble, the CRC calculation of received packet will be wrong because the longer frame and the frame length will end at a 4-bit boundary instead of the usual 8-bit boundary. When RX_DV goes inactive on the 4-bit boundary, the interface will assert DATA_RDY and BYTE_RDY flag with the ERROR_NIBBLE. The error event is also mapped into the PRU_ICSSG INTC.

12.2.2.5 Transmit CRC Computation

For the outgoing data, the MII_G_RT calculates the CRC32 value and inserts it into outgoing packets. The CRC value computed on each MII transmit path is also available in memory map registers that can be read by the PRU and used primarily for debug and diagnostic purposes. The CRC is inserted into the outgoing packet based on the commands received through the R31 register of the PRU. The CRC will be inserted into the TX L1 FIFO, and there must be enough room to store the CRC value in the FIFO or else the FIFO will overflow. As [Table 12-3](#) shows, the CRC programming model supports three sequences that provide more flexibility. Note: "cmdR31" indicates write to the mentioned bits of the R31 command interface.

Table 12-3. TX CRC Programming Models

Option 1	Step 1: cmdR31 [TX_CRC_HIGH + TX_CRC_LOW + TX_EOF]
Option 2	Note: Only valid when TX L2 is disabled. Step 1: cmdR31 [TX_CRC_HIGH] Step 2: wait > 6 clocks (PRU cycles) Step 3: cmdR31 [TX_CRC_LOW + TX_EOF]
Option 3	Note: Only valid when TX L2 is disabled. Step 1: cmdR31 [TX_CRC_HIGH] Step 2: wait > 6 clocks (PRU cycles) Step 3: read TX_CRC0[31-0] TX_CRC0 and TX_CRC1[31-0] TX_CRC1 Step 4: modify CRC[15-0] Step 5: cmdR31 [TX_PUSH16 + TX_EOF + TX_ERROR_NIBBLE]

12.2.2.6 Transmit CRC Computation for fragmented frames

Fragmented frames have a special CRC32. Each fragment CRC32 is based on the previous fragmentations, so a running total. In addition TX_CRC_HIGH is inverted for all fragments except the last fragment. The final fragmentation has a normal CRC which is based on the full frame.

12.2.3 RX MII Interface

The RX MII interface is composed of multiple components that perform various tasks - latch received data, start of frame detection, start frame delimiter detection, CRC calculation and error detection, enhanced link detection through RX error detection and interface to PRU register R31.

[Table 12-4](#) includes more details about the internal signals and output of these components

12.2.3.1 RX MII Receive Data Latch

The receive data from the MII interface is stored in the receive data FIFO which is 32 bytes. The PRU can access this data through the register R31. Depending on the configuration settings, the data can be latched on reception of one or two bytes. In each scheme, the configured number of nibbles is assembled before being copied into the PRU registers. [Figure 12-9](#) shows the inputs and outputs of the data latch logic block.

The receiver logic in MII_RT can be programmed through the MII_RT [MII_RT_RXCFG0](#) and MII_RT [MII_RT_RXCFG1](#) registers to remove or retain the preamble + SFD from incoming frames.

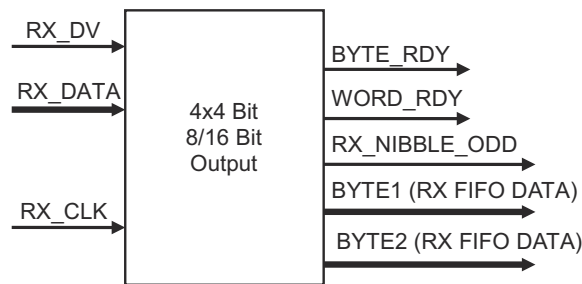


Figure 12-9. RX Data Latch

12.2.3.2 RX MII Start of Frame Detection

The start of frame detection logic tracks the frame boundaries and signals the beginning of a frame to other components of the PRU_ICSSG. This logic detects two events:

- Start of Frame (SOF) event that occurs when Receive Data Valid MII signal is sampled high.
- Start of Frame Delimiter (SFD) event is seen on MII Receive Data bus.

These event triggers can be used to add timestamp to the frames. The notification for these events is available through R31 as well as through INTC which is integrated in the PRU_ICSSG. Figure 12-10 shows the inputs and outputs of the start of frame detection logic block.

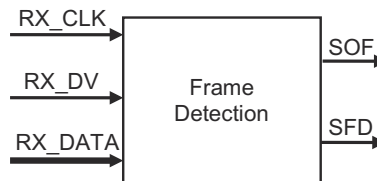


Figure 12-10. RX MII Start of Frame Detection

12.2.3.3 CRC Error Detection

For each incoming frame, the CRC is calculated by the MII_G_RT and compared against the CRC included in the frame. When the two values do not match, a CRC error is flagged. The ERROR_CRC indication is available in the register interface (PRU R31 Receive Interface) as well as in the FIFO interface (RX L2 Status Interface). It is also provided to the INTC which is integrated in the PRU_ICSSG. Figure 12-11 shows the inputs and outputs of CRC error detection logic block.

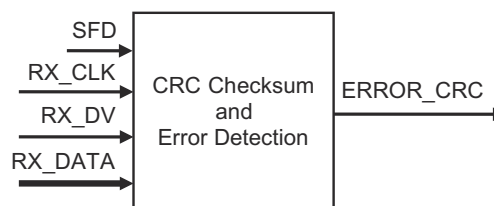


Figure 12-11. CRC Error Detection

12.2.3.4 RX Error Detection and Action

The RX error detection logic tracks the receive error signaled by the physical layer and informs the PRU_ICSSG INTC whenever an error is detected. Figure 12-12 shows the inputs and outputs of the RX error detection logic block. Note the following dependencies:

- RX_ERR signal is only sampled when RX_DV is asserted.
- All nibbles are discarded post RX_ERR event, including the nibble which had RX_ERR asserted. This state will remain until EOF occurs.
- Due to this fact, RX L1 FIFO and RX L2 FIFO will never receive any data with RX_ERR or post RX_ERR during that frame.

Note

RX error detection logic is supported only for MII mode and this feature is not supported for RGMII and SGMII modes of operation.

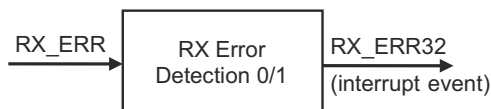
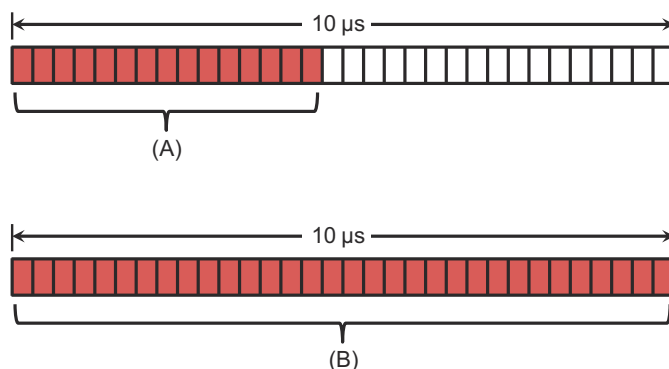


Figure 12-12. RX Error Detection

Note

Note for SGMII and RGMII modes, RX_ERR is sampled after SFD and during the payload if one occurs then it can be detected by R31 and/or INTC same as MII. The MII RX_ERR counter counts for every MII nibble.

This submodule also keeps track of a running count of receive error events within a 10 μ s error detection window, as shown in Figure 12-13. The INTC is notified when 32 or more events have occurred in a 10 μ s error detection window. The error detection window is not a sliding window but a non-overlapping window with no specific initialization time with respect to incoming traffic. The timer starts its 10 μ s counts immediately after de-assertion of reset to the MII_G_RT module.



- A. There are fewer than 32 consecutive error events in the 10 μ s window. The detection module will not forward to the interrupt controller (INTC).
- B. There are more or equal to 32 error events in the 10 μ s window. The detection module will notify the interrupt controller (INTC).

Figure 12-13. Error Detection Window with Running Counter

12.2.3.5 RX Data Path Options to PRU

There are two data path options for delivering received data to the PRU, described further in the subsequent sections:

1. RX MII port $\rightarrow$ RX L1 FIFO $\rightarrow$ PRU (one word in flight)
2. RX MII port $\rightarrow$ RX L1 FIFO $\rightarrow$ RX L2 buffer $\rightarrow$ PRU (multi-word in flight)

Once the PRU has received RX data, the PRU can both manipulate received data or send data to the TX MII Interface.

12.2.3.6 RX MII Port $\rightarrow$ RX L1 FIFO $\rightarrow$ PRU

The RX L1 FIFO to PRU interface is depicted in Figure 12-14. In this mode, the data received from the MII interface is fed into the 32-byte RX L1 FIFO. The first data byte into the FIFO is automatically available in R31 of the PRU. Therefore, the PRU firmware can directly operate on this data without having to read it in a separate instruction. This allows the PRU to access receive data with low latency.

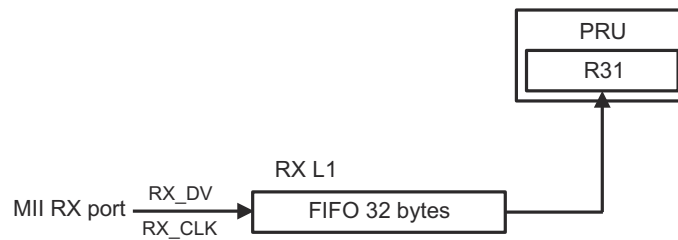


Figure 12-14. RX L1 to PRU Interface

When the new data is received, the PRU is provided with up to two bytes at a time in the R31 register, as shown in Figure 12-15. Once the PRU processes the incoming data, it instructs the MII_G_RT by writing to the R31 command interface bits to pop one or two bytes of data from the 32-byte RX FIFO. The pop operation causes current contents of R31 to be refreshed with new data from the incoming packet. Each time the data is popped, the status bits change to indicate so. If the pop is completed and there is no new data, the status bits immediately change to indicate no new data.

Note: The current R31 content, including data, will be lost after issuing the pop operation. If this information needs to be accessed later, the PRU should store the existing R31 content before popping new data.

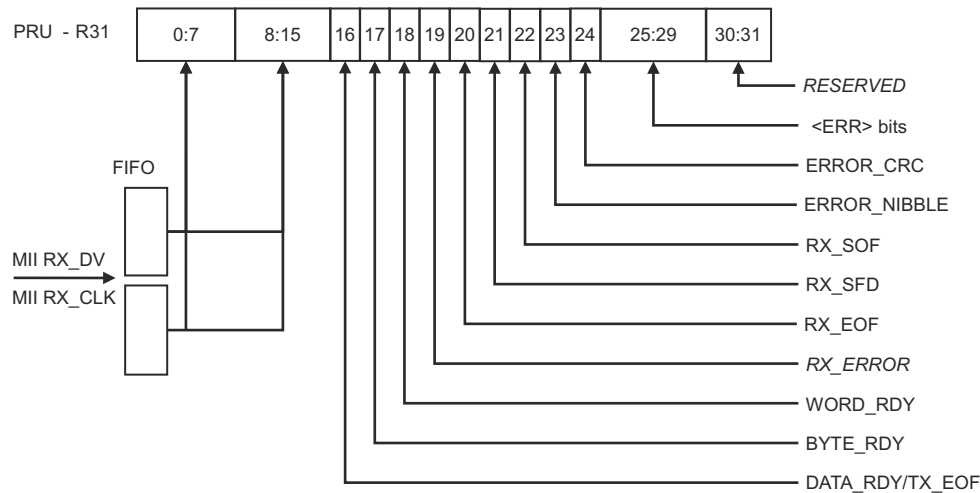


Figure 12-15. MII RX Data to PRU R31 (R) and RX FIFO

Table 12-4 describes the receive interface data and status contents provided by the R31 register. These contents are available when R31 is read. To configure this register, the PRU GPI mode should be set for MII_G_RT mode in the CFG register space. Note the following:

1. If the data from receive path is not read in time, it could cause an overflow event because the data is still continuously provided to the 32-byte receive FIFO. Due to the receive FIFO overflow, the data gets automatically discarded to avoid lack of space in the FIFO. At the same time, an interrupt is raised to the INTC through a system event (PRU<n>_RX_OVERFLOW). To detect an overflow condition, the PRU should poll for this system event condition and a RX RESET command through the R31 command interface is required to clear out from this condition. Note that the received Ethernet frame is corrupted and should not be used for further processing as bytes have been dropped due to the overflow condition. A FIFO reset is recommended.
2. The receive data in the R31 register is available following synchronization to the PRU clock domain. So, there is a finite delay (120 ns) when data is available from MII interface and it is accessible to the PRU.
3. The receive FIFO also has the capability to be reset through software. When reset, all contents of receive FIFO are purged and it may result in the current frame not being received as expected. When a frame is being received and the PRU resets the RX FIFO, the remaining frame is not placed into the RX FIFO. However, any new frame arriving on the receive MII port will be stored in the FIFO.

Table 12-4. PRU R31: Receive Interface Data and Status (Read Mode)

Bits	Field Name	Description
31-30	RESERVED	In case of register interface, these bits are provided to PRU by other modules in PRU_ICSSG. From the MII_G_RT module point of view, these bits are always zero.
29	RX_MIN_FRM_CNT_ERR	RX_MIN_FRM_CNT_ERR is set to 1 when the count of total bytes of incoming frame is less than the value defined by RX_MIN_FRM_CNT. RX_MIN_FRM_CNT_ERR is cleared by RX_ERROR_CLR. Cleared by RX_ERROR_CLR or RX_L2_DONE. Note, during backpressure the status will not get updated by a new packet in L1 FIFO. The flag is valid for the current packet in L2 FIFO.
28	RX_MAX_FRM_CNT_ERR	RX_MAX_FRM_CNT_ERR is set to 1 when the count of total bytes of incoming frame is more than the value defined by RX_MAX_FRM_CNT_ERR. RX_MAX_FRM_CNT_ERR is cleared by RX_ERROR_CLR. Cleared by RX_ERROR_CLR or RX_L2_DONE. Note, during backpressure the status will not get updated by a new packet in L1 FIFO. The flag is valid for the current packet in L2 FIFO.
27	RX_EOF_ERROR	RX_EOF_ERROR is set to 1 when an RX_EOF event or RX_ERROR event occurs. RX_EOF_ERROR is cleared by RX_EOF_CLR and/or RX_ERROR_CLR.
26	RX_MAX_PRE_CNT_ERR	RX_MAX_PRE_CNT_ERR is set to 1 when the number of nibbles equaling 0x5 before SFD event (0xD5) is more than the value defined by PRUSS_MII_RT_RX_PCNT0/1 [RX_MAX_PCNT]. RX_MAX_PRE_CNT_ERR is cleared by RX_ERROR_CLR.
25	RX_ERR	RX_ERR is set to 1 when pr1_mii0/1_rxr is asserted while pr1_mii0/1_rxdv bit is set. RX_ERR is cleared by RX_ERROR_CLR.
24	ERROR_CRC	ERROR_CRC indicates that the frame has a CRC mismatch. This bit is valid when the RX_EOF bit is set. It should be noted that ERROR_CRC bit is ready in early status, which means it is calculated before data is available in RXL1 FIFO. ERROR_CRC is cleared by RX_ERROR_CLR. Cleared by RX_ERROR_CLR or RX_L2_DONE. Note, during backpressure the status will not get updated by a new packet in L1 FIFO. The flag is valid for the current packet in L2 FIFO.
23	ERROR_NIBBLE	ERROR_NIBBLE indicates that the frame ended in odd nibble. It should be considered valid only when the RX_EOF bit and pr1_mii0/1_rxdv are set. Nibble counter is enabled post SFD event. It should be noted that ERROR_NIBBLE bit is ready in early status, which means it is calculated before data is available in RXL1 FIFO. ERROR_NIBBLE is cleared by RX_ERROR_CLR.
22	RX_SOF	RX_SOF transitions from low to high when the frame data starts to arrive and pr1_mii0/1_rxdv is asserted. Note: There will be a small sync delay of 0ns – 5ns. The recommended time to clear this bit via RX_SOF_CLR is at the end of frame (EOF). It should be noted that RX_SOF bit is ready in early status, which means it is calculated before data is available in RXL1 FIFO.
21	RX_SFD	RX_SFD transitions from low to high when the SFD sequence (0xD5) post RX_SOF is observed on the receive MII data. The recommended time to clear this bit via RX_SFD_CLR is at the end of frame (EOF). It should be noted that RX_SFD bit is ready in early status, which means it is calculated before data is available in RXL1 FIFO.
20	RX_EOF	RX_EOF indicates that the frame has ended and pr1_mii0/1_rxdv is de-asserted. It also validates the CRC match bit. Note: There will be a small sync delay of 0ns – 5ns. It should be noted that RX_EOF bit is ready in early status, which means it is calculated before data is available in RXL1 FIFO. Note: Also if RX_L2_EOF_SCLR_DIS is set, then this flag will remain asserted when RX_L2 is enabled until RX_EOF_CLR. Cleared by RX_ERROR_CLR or RX_L2_DONE. Note, during backpressure the status will not get updated by a new packet in L1 FIFO. The flag is valid for the current packet in L2 FIFO.

Table 12-4. PRU R31: Receive Interface Data and Status (Read Mode) (continued)

Bits	Field Name	Description
19	RX_ERROR	RX_ERROR indicates one or more of the following errors occurred: - RX_MAX/MIN_FRM_CNT_ERR - RX_MAX/MIN_PRE_CNT_ERR - RX_ERR RX_ERROR is cleared by RX_ERROR_CLR.
18	WORD_RDY	WORD_RDY indicates that all four nibbles in R31 have valid data. There is a 2 clock cycle latency from the command RX_POP16 to WORD_RDY update. Therefore, firmware needs to insure it does not read WORD_RDY until 2 clock cycles after RX_POP16.
17	BYTE_RDY	BYTE_RDY indicates that the lower two nibbles in R31 have valid data. There is a 2 clock cycle latency from the command RX_POP8 to BYTE_RDY update. Therefore, PRU firmware needs to insure it does not read BYTE_RDY until 2 clock cycles after RX_POP8.
16	DATA_RDY/ TX_EOF	When RX_DATA_RDY_MODE_DIS = 0: DATA_RDY indicates there is valid data in R31 ready to be read. This bit goes to zero when the PRU does a POP8/16 and there is no new data left in the receive MII port. This bit is high if there is more receive data for PRU to read. There is a 2 clock cycle latency from the command RX_POP16/8 to WORD_RDY/BYTE_RDY update. Therefore, PRU firmware needs to insure it does not read BYTE_RDY/WORD_RDY until 2 clock cycles after RX_POP16/8. When RX_DATA_RDY_MODE_DIS = 1: TX_EOF indicates an TX_EOF event (i.e. a 1 --> 0 transition on TX_EN) has occurred. This bit will clear when TX_RESET is set or when new data is first loaded. PRU firmware can wait until TX_EOF = 1, then start a new TX Frame by immediately loading new data.
15-8	BYTE1	Data Byte 1. This data is available such that it is safe to read by the PRU when the DATA_RDY/BYTE_RDY/WORD_RDY bits are asserted.
7-0	BYTE0	Data Byte 0. This data is available such that it is safe to read by the PRU when the DATA_RDY/BYTE_RDY/WORD_RDY bits are asserted.

12.2.3.7 RX MII Port → RX L1 FIFO → RX L2 Buffer → PRU

The RX L2 is an optional high performance buffer between the RX L1 FIFO and the PRU. [Figure 12-16](#) illustrates the receive data path using RX L2 buffer. This data path is characterized by multi-word in flight transactions.

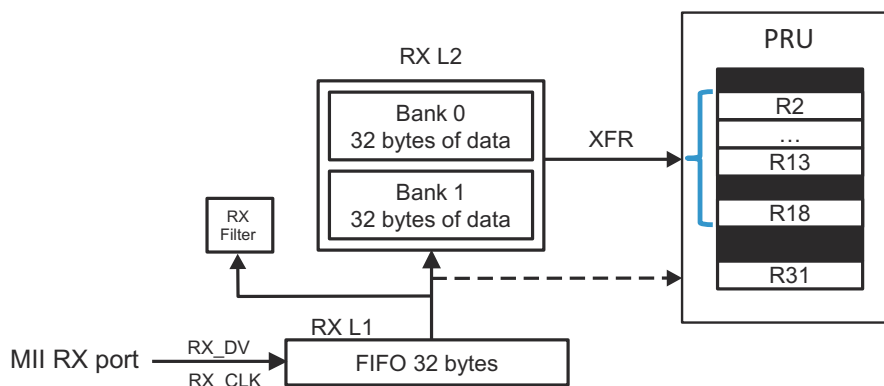


Figure 12-16. RX L2 to PRU Interface

The 64-byte RX L2 buffer is divided into two 32 byte banks, or ping/pong buffers. When the RX L2 is enabled, the incoming data from the MII RX port will transmit first to the 32 byte RX L1 FIFO. RX L1 pushes data into RX L2, starting when the first byte is ready until the final EOF marker. The RX L2 buffer will apply backpressure to the RX L1 FIFO after RX_L2_EOF event occur and until RX_L2_DONE event. Therefore, it is the PRU firmware's responsibility to fetch the data in RX L2 before it is overwritten by the cyclic buffer. The RX L1 will remain near empty, with only one byte (nibble) stored.

Each RX L2 bank holds up to 32 bytes of data, and every four nibbles (or 16 bits) of data has a corresponding 8-bit status. The data and status information are stored in packed arrays. In each bank, R2 to R9 contains the data packed array and R10 to R13 contains the status packed array. Figure 12-17 shows the relationship of the data registers and status registers. The RX L2 status registers record status information about the received data, such as ERROR_CRC, RX_ERROR, STATUS_RDY, etc. The RX L2 status register details are described in Table 12-5. Note: RX_RESET clears all Data and Status elements and resets R18.

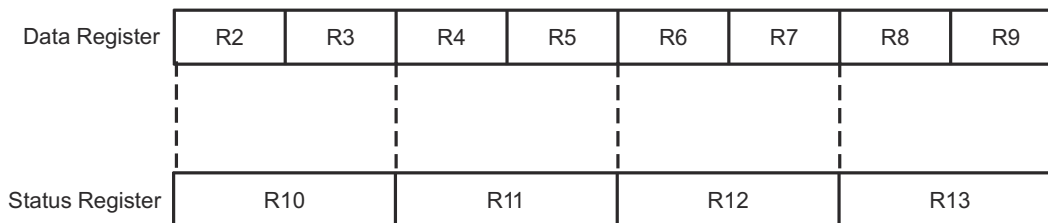


Figure 12-17. Data and Status Register Dependency

12.2.3.7.1 RX L2 Status in mode 0, none IET mode (when ICSS_G_CFG[2] RX_L2_G_EN= 0h)

Table 12-5. RX L2 Status in mode 0

Bit	Field Name	Description
7	ERROR_CRC	ERROR_CRC indicates that the frame has a CRC mismatch. This bit is valid when the RX_EOF bit is set. It should be noted that ERROR_CRC bit is ready in early status, which means it is calculated before data is available in RX L1 FIFO. ERROR_CRC will only be set for one entry, self clear on next entry.
6	ERROR_NIBBLE	ERROR_NIBBLE indicates that the frame ended in odd nibble. It should be considered valid only when the RX_EOF bit and pr1_mii0/1_rxdv are set. Nibble counter is enabled post SFD event. It should be noted that ERROR_NIBBLE bit is ready in early status, which means it is calculated before data is available in RX L1 FIFO. ERROR_NIBBLE will only be set for one entry, self clear on next entry.
5	RX_SOF	RX_SOF transitions from low to high when the frame data starts to arrive and pr1_mii0/1_rxdv is asserted. Note: There will be a small sync delay of 0ns – 5ns. It should be noted that RX_SOF bit is ready in early status, which means it is calculated before data is available in RX L1 FIFO. RX_SOF will only be set for one entry, self clear on next entry.
4	RX_SFD	RX_SFD transitions from low to high when the SFD sequence (0xD5) post RX_SOF is observed on the receive MII data. It should be noted that RX_SFD bit is ready in early status, which means it is calculated before data is available in RX + L1 FIFO. RX_SOF will only be set for one entry, self clear on next entry.
3	RX_EOF	RX_EOF indicates that the frame has ended and pr1_mii0/1_rxdv is de-asserted. It also validates the CRC match bit. Note: There will be a small sync delay of 0ns – 5ns. It should be noted that RX_EOF bit is ready in early status, which means it is calculated before data is available in RX L1 FIFO. If RX_L2_EOF_SCLR_DIS = 1, then RX_EOF will remain set until RX_EOF_CLR event. Otherwise, RX_ERROR is self-clearing on next entry.
2	RX_ERROR	RX_ERROR indicates one or more of the following errors occurred: • RX_MAX/MIN_FRM_CNT_ERR • RX_MAX/MIN_PRE_CNT_ERR • RX_ERR RX_ERROR is cleared by RX_ERROR_CLR.
1	STATUS_RDY	STATUS_RDY is set when RX_EOF or write pointer advanced by 2. This is a simple method for software to determine if RX_EOF event has occurred or new data is available. If RX_EOF is not set, all status bits are static.
0	RX_ERR	RX_ERR is set to 1 when pr1_mii0/1_rxer is asserted while pr1_mii0/1_rxdv bit is set. It will get set for first pr1_mii0/1_rxer event and self clear on SOF for the next FRAME.

12.2.3.7.2

Bank 0 and Bank 1 are used as ping/pong buffers. RX L2 supports the reading of a write pointer in R18 that allows software to determine which bank has active write transactions, as well as the specific write address within packed data arrays.

The PRU interacts with the RX L2 buffer using the high performance XFR read instructions and broadside interface. [Table 12-6](#) shows the device XFR ID numbers for each bank.

Table 12-6. RX L2 XFR ID

Device ID	Function	Description
20	Selects RX L2 Bank0	R2:R9 Data packed array R10:R13 Status packed array mode 0
21	Selects RX L2 Bank1	R2:R9 Data packed array R10:R13 Status packed array mode 0
20/21	Byte pointer of current write	R18[5-0] Pointer indicating location of current write in data packed array. 0 = Bank0.R2.Byte0 (default and reset value) 1 = Bank0.R2.Byte1 2 = Bank0.R2.Byte2 3 = Bank0.R2.Byte3 4 = Bank0.R3.Byte0 ... 63=Bank1.R9.Byte3

12.2.3.7.3 RX L2 Status for IET Type 1/Type 2 (when MII_G_RT_ICSS_G_CFG[2] RX_L2_G_EN = 1h)

Table 12-7. RX L2 XFR ID

Device ID	Function	Description
20	Selects RX L2 Bank0	R2:R9 Data packed array
21	Selects RX L2 Bank1	R2:R9 Data packed array
20/21	Meta Data	R10:R13 Meta Data
20/21	Byte pointer of current write	R18[5-0] Pointer indicating location of current write in data packed array. 0 = Bank0.R2.Byte0 (default and reset value) 1 = Bank0.R2.Byte1 2 = Bank0.R2.Byte2 3 = Bank0.R2.Byte3 4 = Bank0.R3.Byte0 ... 63=Bank1.R9.Byte3

Table 12-8. RX L2 IET mode Type 1/Type 2 (when MII_G_RT_ICSS_G_CFG[2] RX_L2_G_EN = 1h)

Rn	Field Name	Description
R10.b0	SMD	It will place the first byte to this location on first match of D5h or MII_G_RT_PREEMPT_CFG[15-8] EXP_SMD (default value: D5h) or MII_G_RT_SMDT1S_CFG [7-0] SMDT1S_0 MII_G_RT_SMDT1S_CFG [15-8] SMDT1S_1 MII_G_RT_SMDT1S_CFG [23-16] SMDT1S_2 MII_G_RT_SMDT1S_CFG [31-24] SMDT1S_3 MII_G_RT_SMDT1C_CFG [7-0] SMDT1C_0 MII_G_RT_SMDT1C_CFG [15-8] SMDT1C_1 MII_G_RT_SMDT1C_CFG [23-16] SMDT1C_2 MII_G_RT_SMDT1C_CFG [31-24] SMDT1C_3 MII_G_RT_PREEMPT_CFG[23-16] SMD_V or MII_G_RT_PREEMPT_CFG[[31-24] SMD_R The above is valid after RX_SOF and after the data write pointer advance or on RX_BLK1 event is asserted. It will get cleared when RX_L2_DONE event occurs.
R10.b1	FRAG_CNT	Fragment Count Byte Encoded FRAG_CNT will get cleared when RX_L2_DONE event occurs Only valid when SMD = SMDT1-Cx
R10.b2	SMD_Cx Next	This will always be the corresponding SMD_Cx which matches the last active SMD_Sx SMD_C0 when SMD = SMD_S0 SMD_C1 when SMD = SMD_S1 SMD_C2 when SMD = SMD_S2 SMD_C3 when SMD = SMD_S3 Only valid when SMD_Sx_PRESENT is asserted
R10.b3	FRAG_CNT Next	This will always be the next possible FRAG_CNT FRAG_CNT1 when FRAG_CNT = FRAG_CNT0 FRAG_CNT2 when FRAG_CNT = FRAG_CNT1 FRAG_CNT3 when FRAG_CNT = FRAG_CNT2 FRAG_CNT0 when FRAG_CNT = FRAG_CNT3 Only valid when SMD = SMDT1-Cx
R11.b0[0]	MCRC_PRESENT	It will get set when MCRC is matched. This is valid after RX_EOF. It will get cleared when RX_L2_DONE event occurs.
R11.b0[1]	SMD_Sx_PRESENT	It will set if SMD matches one of SMDT1S[3:0] patterns: MII_G_RT_SMDT1S_CFG [7-0] SMDT1S_0 MII_G_RT_SMDT1S_CFG [15-8] SMDT1S_1 MII_G_RT_SMDT1S_CFG [23-16] SMDT1S_2 MII_G_RT_SMDT1S_CFG [31-24] SMDT1S_3 It will get cleared when RX_L2_DONE event occurs.
R11.b0[2]	SMD_Cx_PRESENT	It will set if SMD matches one of SMDT1C[3:0] patterns: MII_G_RT_SMDT1C_CFG [7-0] SMDT1C_0 MII_G_RT_SMDT1C_CFG [15-8] SMDT1C_1 MII_G_RT_SMDT1C_CFG [23-16] SMDT1C_2 MII_G_RT_SMDT1C_CFG [31-24] SMDT1C_3 It will get cleared when RX_L2_DONE event occurs.
R12.b0	0x55 Byte0	Should be 0x55, but not required It will get cleared when RX_L2_DONE event occurs.
R12.b1	0x55 Byte1	Should be 0x55, but not required It will get cleared when RX_L2_DONE event occurs.
R12.b2	0x55 Byte2	Should be 0x55, but not required It will get cleared when RX_L2_DONE event occurs.
R12.b3	0x55 Byte3	Should be 0x55, but not required It will get cleared when RX_L2_DONE event occurs.
R13.b0	0x55 Byte4	Should be 0x55, but not required It will get cleared when RX_L2_DONE event occurs.
R13.b1	0x55 Byte5	Should be 0x55, but not required It will get cleared when RX_L2_DONE event occurs.

**Table 12-8. RX L2 IET mode Type 1/Type 2 (when MII_G_RT_ICSS_G_CFG[2] RX_L2_G_EN = 1h)
(continued)**

Rn	Field Name	Description
R13.b2	0x55/ SMDTx-Cx Byte6	Should be 0x55/SMDTx-Cx, but not required It will get cleared when RX_L2_DONE event occurs.
R13.b3	SMD/FRAG_CNTx Byte7	Should be SMD/FRAG_CNTx, but not required It will get cleared when RX_L2_DONE event occurs.

12.2.3.7.4

XFR read transactions are passive and have no effect on any status or other states in RX L2. The firmware can also read R18 to determine which Bank has active write transactions and the location of the transaction. With this information, the firmware can read multiple times the stable preserved data. Note: When RX L1 data is written to RX L2, the next status byte gets cleared at the same time the current status byte gets updated. The rest of the status buffer is persistent. When software is accessing any register of the ping/ pong buffer, software needs to issue an XFER read transaction to fetch the latest/current state of the ping/pong buffer. The PRU registers will not reflect the current snapshot of L2 unless an XFER is issued by software.

12.2.3.7.5 Broadside Stitch FIFO

A simple 2 deep by 32 Byte Wide broadside FIFO is attached to ID = 08 to enable the firmware to efficiently pack fragments into aligned data words.

Table 12-9. RX L2 XFR ID

Device ID	Function	Description
08	64 Bytes XOUT 1 Byte to 32 Bytes, LSB justify XIN 32 Bytes. Note: FIFO has less than 32 Bytes, it will only return the valid data LSB justified	R2:R9 Data packed array
08	It will subtract 4 bytes from the current wr_ptr	R10[0] Control
08	It will reset the rd and wr ptrs	R10[1] Reset

12.2.3.7.6 MII_G_RT RX Classifier

The RX Classifier block generates set of 16 class signals one set for each PRUn/RTU_PRUn core. It is composed of 3 subblocks:

1. RX L2 Filter block
2. RX Traffic Class Selector block
3. RX Rate Counter block

The software must configure MII_G_RT_RX_CLASS_CFG1_PRU0/1 to define the logic for the final class term. Each class is a function of filter flags which can get ORed or ANDed along with optional inversion. Each class has a set of registers (MII_G_RT_RX_CLASSm_AND_EN_PRUn, where m = 0 to 15 and n = 0 or 1) which determines if class is based on ORed or ANDed logic along with which of the 32 filters are part of the equation.

The final gate determine which of the terms will get factored to produce rx_class[15:0]. Each of the rx_class[15:0] can have different terms. It is fully programmable. Note: This logic will track fragmented frames based on the first segment of that frame. Only filters which will become valid on the intial fragmentation can get used for Traffic Class Selector, shown on [Figure 12-18](#)

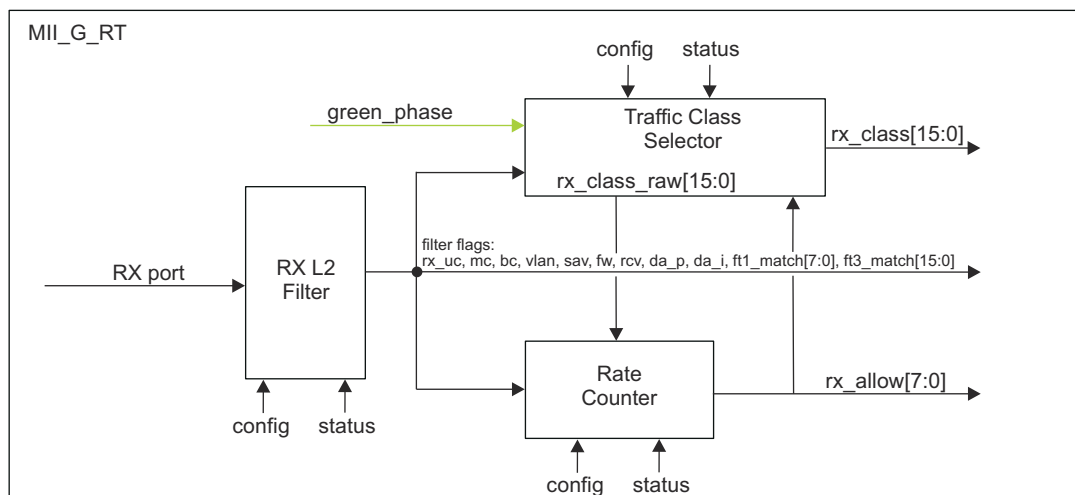


Figure 12-18. MII_G_RT RX Classifier

12.2.3.7.6.1 RX Rate Counter Block

The RX Rate Counter contains 8 independent rate monitors which determines if the rate of traffic of a given class exceeds the threshold set by MII_G_RT_RX_RATE_CFGm_PRUn[31-0] RX_RATE_CIR_IDLEm registers (where m = 0 to 7 and n = 0 or 1).

Each rate monitor has implemented PIR (Peak Information Rate) counter. The PIR counter in each monitor is a 37-bit internal counter where the monitor MII_G_RT_RX_RATE_CFGm_PRUn[31-0] RX_RATE_CIR_IDLEm is added on every clock and the frame size bytes less than 18 is subtracted at End Of Frame (EOF). If the count is negative at lookup time, the packet will be marked RED, else it can be GREEN.

12.2.3.7.6.2 RX Rate Hit Mapping

Each of the 8 RX Rate monitors can monitor 1 of the 0..48 possible data traffic types.

Table 12-10 defines the RX Rate Hit Mapping.

Table 12-10. RX Rate Hit Mapping

Bit Configuration	rx_rate_hit (n= 0 to 7)	Source
0	rx_rate_hit<n>	ft1_match0
1	rx_rate_hit<n>	ft1_match1
2	rx_rate_hit<n>	ft1_match2
3	rx_rate_hit<n>	ft1_match3
4	rx_rate_hit<n>	ft1_match4
5	rx_rate_hit<n>	ft1_match5
6	rx_rate_hit<n>	ft1_match6
7	rx_rate_hit<n>	ft1_match7
8	rx_rate_hit<n>	ft3_match0
9	rx_rate_hit<n>	ft3_match1
10	rx_rate_hit<n>	ft3_match2
11	rx_rate_hit<n>	ft3_match3
12	rx_rate_hit<n>	ft3_match4
13	rx_rate_hit<n>	ft3_match5
14	rx_rate_hit<n>	ft3_match6
15	rx_rate_hit<n>	ft3_match7
16	rx_rate_hit<n>	ft3_match8
17	rx_rate_hit<n>	ft3_match9
18	rx_rate_hit<n>	ft3_match10

Table 12-10. RX Rate Hit Mapping (continued)

Bit Configuration	rx_rate_hit (n= 0 to 7)	Source
19	rx_rate_hit<n>	ft3_match11
20	rx_rate_hit<n>	ft3_match12
21	rx_rate_hit<n>	ft3_match13
22	rx_rate_hit<n>	ft3_match14
23	rx_rate_hit<n>	ft3_match15
24	rx_rate_hit<n>	ft_rx_uc
25	rx_rate_hit<n>	ft_rx_mc
26	rx_rate_hit<n>	ft_rx_bc
27	rx_rate_hit<n>	ft_rx_sav
28	rx_rate_hit<n>	ft_rx_fw
29	rx_rate_hit<n>	ft_rx_rcv
30	rx_rate_hit<n>	ft_rx_vlan
31	rx_rate_hit<n>	ft_rx_da_p
32	rx_rate_hit<n>	ft_rx_da_i
33	rx_rate_hit<n>	rx_class_raw0
34	rx_rate_hit<n>	rx_class_raw1
35	rx_rate_hit<n>	rx_class_raw2
36	rx_rate_hit<n>	rx_class_raw3
37	rx_rate_hit<n>	rx_class_raw4
38	rx_rate_hit<n>	rx_class_raw5
39	rx_rate_hit<n>	rx_class_raw6
40	rx_rate_hit<n>	rx_class_raw7
41	rx_rate_hit<n>	rx_class_raw8
42	rx_rate_hit<n>	rx_class_raw9
43	rx_rate_hit<n>	rx_class_raw10
44	rx_rate_hit<n>	rx_class_raw11
45	rx_rate_hit<n>	rx_class_raw12
46	rx_rate_hit<n>	rx_class_raw13
47	rx_rate_hit<n>	rx_class_raw14
48	rx_rate_hit<n>	rx_class_raw15

To select which traffic type to be monitored register MII_G_RT_RX_STAT_CLASSm_HIT_PRUn[31-0] RX_STAT_CLASSm_PRUn (where m = 0 to 15 and n = 0 or 1) has to configured. If this class is a hit and at the EOF then the counter will get subtracted based on the packet size.

12.2.3.7.6.3 Traffic Class Selector Block

This logic block does simple logic reduction which operates on:

1. The green phase signal
2. All of the filter outputs along with basic filter flags
3. The outputs from the Rate Counter

The Traffic Class Selector module produces 2 sets of outputs:

- rx_class[15:0] - goes to broadside for observation
- rx_class_raw[15:0] - goes to the Rate Counter

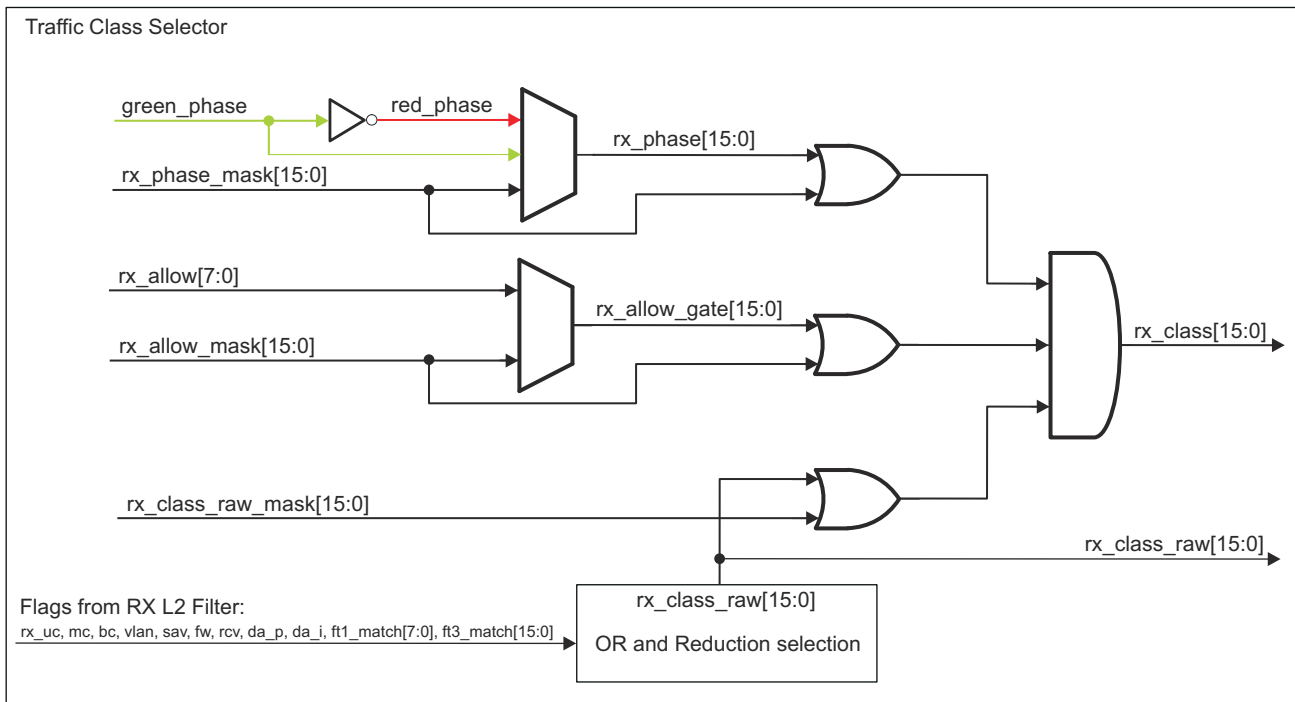


Figure 12-19. Traffic Class Selector

The logic reduction is controlled by a set of registers which controls the type of reduction and the selection of the inputs.

Table 12-11 defines the mapping and the reduction options.

Table 12-11. Traffic Class Data Mapping

rx_class_data	Source
rx_class_data[31]	ft_rx_sav
rx_class_data[30]	ft_rx_mc
rx_class_data[29]	ft_rx_bc
rx_class_data[28]	ft_rx_fw
rx_class_data[27]	ft_rx_rcv
rx_class_data[26]	ft_rx_vlan
rx_class_data[25]	ft_rx_da_p
rx_class_data[24]	ft_rx_da_i
rx_class_data[23:16]	ft1_match[7:0]
rx_class_data[15:8]	ft3_match[15:8]
rx_class_data[7:0]	ft3_match[7:0]

In order to select the source mapping, i.e. which filter flag hit the rate logic, 1 of 8 RATE sources has to be configured through the following registers: MII_G_RT_RX_RATE_SRC_SEL0_PRU0 or MII_G_RT_RX_RATE_SRC_SEL1_PRU0 (for PRU0 core) and MII_G_RT_RX_RATE_SRC_SEL0_PRU1 or MII_G_RT_RX_RATE_SRC_SEL1_PRU1 (for PRU1 core). Note that only 1 of RX Rate classes can be asserted per frame.

12.2.3.7.6.4 PRU_ICSSG RX L2 Filter Block

There are 8 MAC filter instances implemented in the PRU_ICSSG system. Each of the MAC filters (RX L2 Filter - Type 1) has the following specific features, as is shown in Figure 12-20:

- 8 unique set of DA (Destination Address), 6 Bytes used to compare to DA, 6 Bytes mask, optional compare mode (equal, greater than, less than). These 6 Bytes reside in MAC_PRU0_0 and MAC_PRU0_1 registers (for PRU0 core) and in MAC_PRU1_0 and MAC_PRU1_1 registers (for PRU1 core).

- 1 common MAC_PORT0/1, 6 Bytes used to compare to SA (Source Address)
- 1 common MAC Host Interface, 6 Bytes used to compare to SA (Source Address). These 6 Bytes reside in MII_G_RT_MAC_INTERFACE_0[31-0] MAC_INF_0 and MII_G_RT_MAC_INTERFACE_1[15-0] MAC_INF_1 registers.
- Optional RX filter restart

16 Content filter instances (RX L2 Filter - Type 3). Each of the Content filters has the following specific features, as is shown also in [Figure 12-21](#):

- 4 Byte Tag + 8 Byte content compare, 4+8 Byte mask, length, compare range
- Auto VLAN tag detection/shift
- IPV6 filter needs 2 content filters, each of a unique start

8 x ingress rate limiters.

- Global status 2 rate limiter map, 256 bps steps, up to 16 bit window.
- Maximum Packet size is 10,000 bytes. It is software responsibility to insure that the packet size does not go beyond.

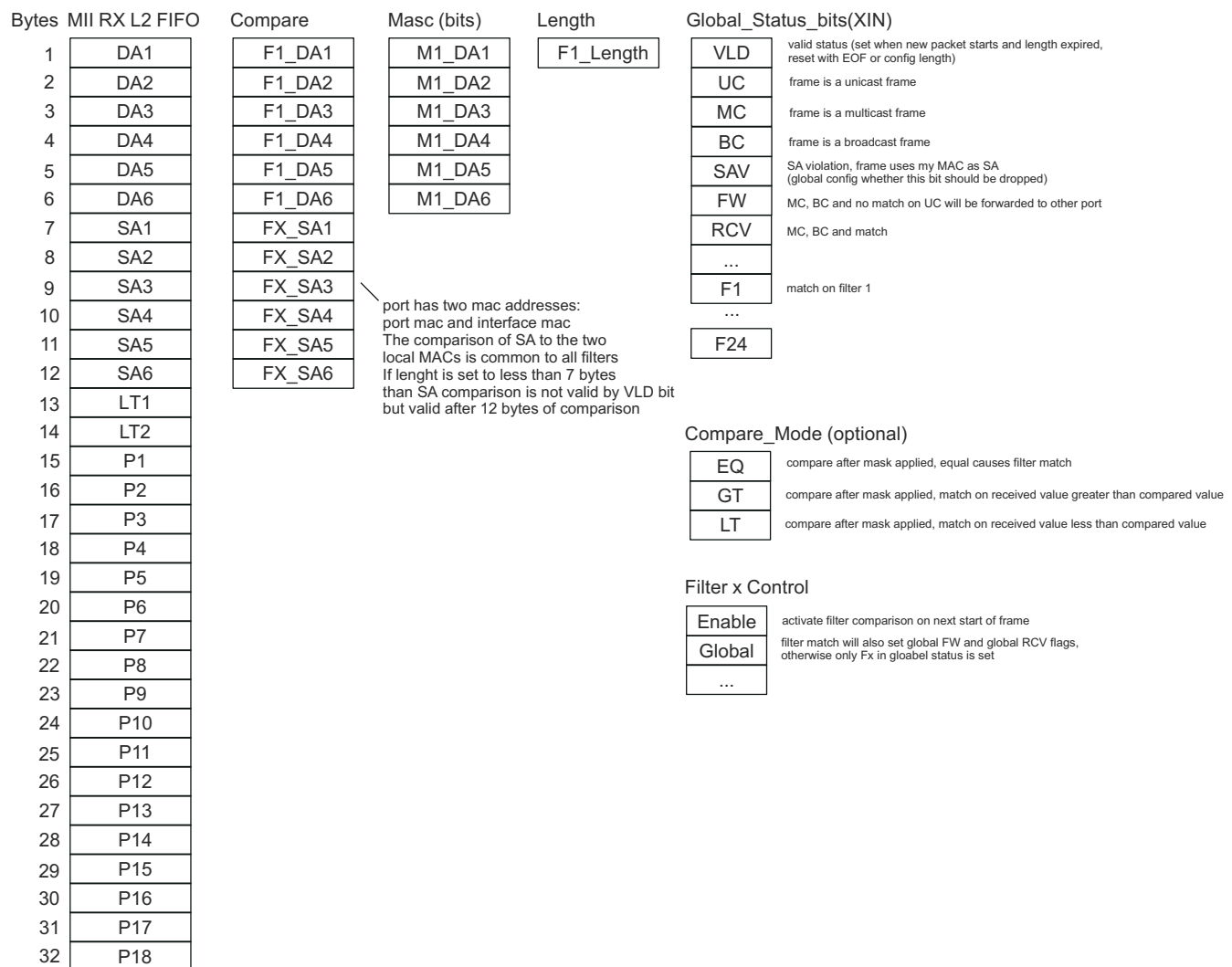


Figure 12-20. PRU_ICSSG RX L2 Filter -Type 1 (MAC Filter)

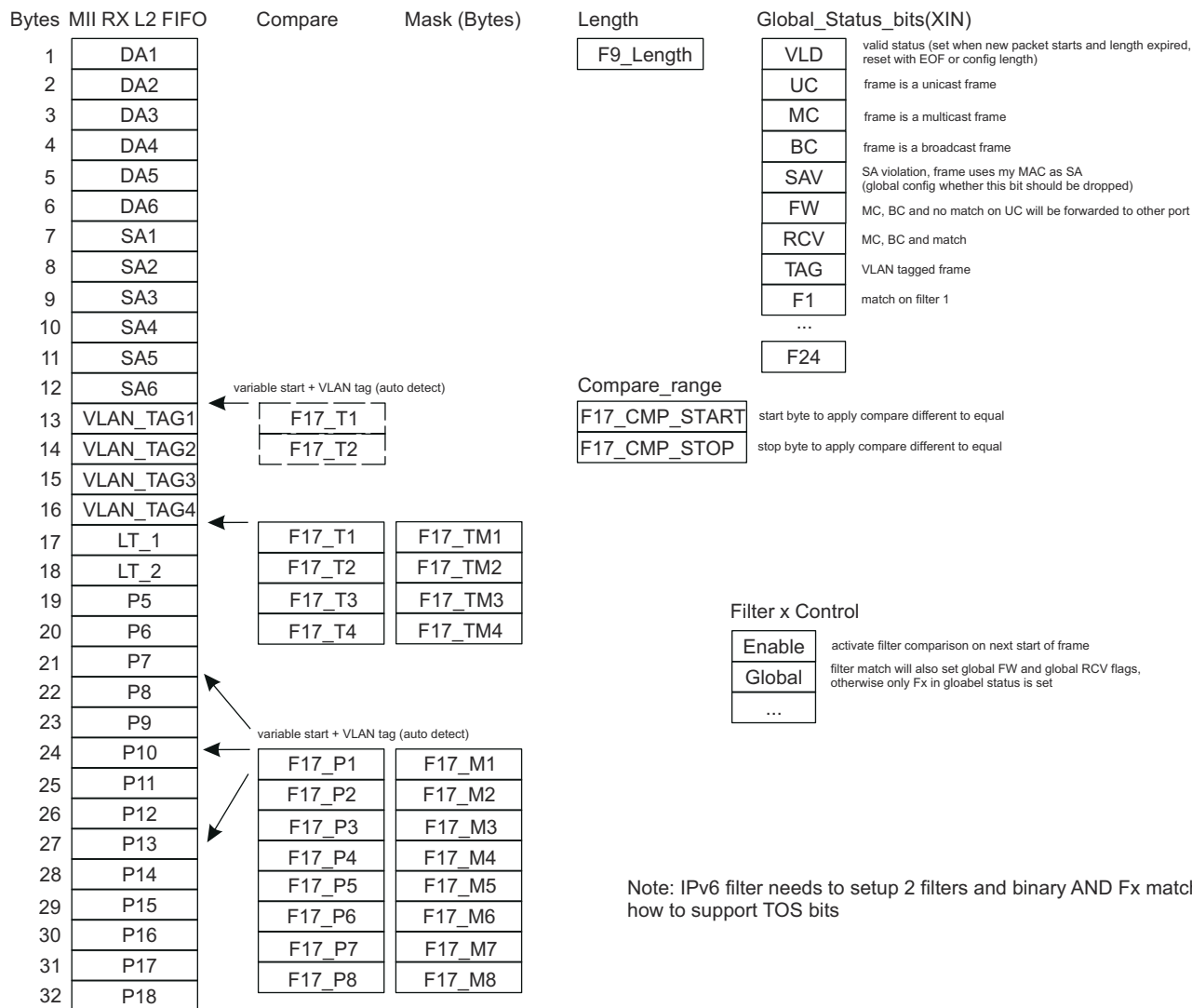


Figure 12-21. PRU_ICSSG RX L2 Filter - Type 3 (Content Filter)

12.2.3.7.6.4.1 PRU_ICSSG RX L2 Filter Operation

The RX L2 filter operates on the data packet when the data packet is pushed into RX L2 FIFO. The RX L2 FIFO will need to be enabled. The filters will work with either enable or disable of the RX L2 features through [MII_G_RT_ICSS_G_CFG\[2\] RX_L2_G_EN](#) bit.

Note

Note that MII mode can operate with or without [MII_G_RT_ICSS_G_CFG\[2\] RX_L2_G_EN](#) bit to be enabled. For RGMII and SGMII modes must have [MII_G_RT_ICSS_G_CFG\[2\] RX_L2_G_EN](#) bit enabled.

The status of the flags is available in Broadside Map of RTU_PRU and PRU along with the poke mode if enabled. The flags are cleared on RX_L2_DONE event or a software update of MII_G_RT_FT3_m_START_PRU[n][14-0] FT3_START bitfield (where m = 0 to 15 and n = 0 or 1). Note that these filters have no state information/context for pre-empted frames or frgements. All data packets are handled the same way, Byte 1 is Byte 1.

[Table 12-12](#) defines the mapping between PRU or RTU_PRU internal core registers and RX filter status flags

Note

Note that both PRU and RTU_PRU cores get the same mapping.

The data is always stored in the RX L2 FIFO before the flag is set, i.e. the flag can be delayed.

Table 12-12. MII_G_RT RX Classifier Broadside Mapping

BS ID	BS R	Bit	Name	Type	Reset	Description
22	R10	14-0	FT_RX_PTR	R	0h	This shows the current byte that the filters are working on. The value remains persistent until a new packet starts. For example 0,1,2,3,...63,63,63,63,63,0,1,2,3...78
22	R11	8	FT_RX_UC	R	0h	Unicast frame defined by DA1[0]. Set on DA[0] = 0h. Clear on RX_L2_DONE event.
22	R11	9	FT_RX_MC	R	0h	Multicast frame defined by DA1[0]. Set on DA[0] = 1h. Clear on RX_L2_DONE event.
22	R11	10	FT_RX_BC	R	0h	Broadcast frame defined by DA6:DA1. Set on DA = FFFF_FFFF_FFFFh. Clear on RX_L2_DONE event.
22	R11	11	FT_RX_SAV	R	0h	Source Address Violation defined by SA and MAC. Set on when SA = MAC_I or MAC_PRU0 or MAC_PRU1. Clear on RX_L2_DONE event.
22	R11	12	FT_RX_FW	R	0h	Forward frame. Set on MC or BC or DA_I Clear on RX_L2_DONE event.
22	R11	13	FT_RX_RCV	R	0h	Receive frame. Set on MC or BC or DA_I Clear on RX_L2_DONE event.
22	R11	14	FT_RX_VLAN	R	0h	VLAN frame. Set when Byte 14 and Byte 13 (16-bit field) == 0x8100 Clear on RX_L2_DONE event.

Table 12-12. MII_G_RT RX Classifier Broadside Mapping (continued)

BS ID	BS R	Bit	Name	Type	Reset	Description
22	R11	15	FT_RX_DA_P	R	0h	Destination Address Match. Set on when DA = MAC_PRUn (where n is the index number of attached PRU core). Clear on RX_L2_DONE event.
22	R11	16	FT_RX_DA_I	R	0h	Destination Address Match. Set on when DA = MAC_I. Clear on RX_L2_DONE event.
22	R11	31	RX_L2_DONE	W	0h	RX L2 Done. Write 1h self-clearing. This will reset all flags and all RX L2 Filters. It can only get a set after the last byte gets posted to RX L2 or RX L2 EOF event. Once set, it will enable data from RX L1 FIFO to be filled into RX L2 FIFO. IF Packet less than 64B you also need to issue RX_RESET.
22	R12	0	FT1_VLD	R	0h	Valid Status of RX L2 Filter -Type 1 (MAC Filter). Set after MII_G_RT_FT1_START_LEN_PRU0/1[19-16] FT1_LEN (this bitfield defines the total numbers of Bytes, Filter 1 will check before Valid bit is set) with TBD additional latency. Clear on RX_L2_DONE event. Clear on MII_G_RT_FT1_START_LEN_PRU0/1[14-0] FT1_START update.
22	R12	15-8	FT1_MATCH	R	0h	RX L2 Filter (Type 1) Match Vector Status. 0h: No Match 1h: Match Clear on RX_L2_DONE event. Clear on MII_G_RT_FT1_START_LEN_PRU0/1[14-0] FT1_START update.
22	R13	7-0	FT3_VLD[7-0]	R	0h	Valid Status of RX L2 Filter-Type 3 (Content Filter). Clear on RX_L2_DONE event. Clear on MII_G_RT_FT3_m_START_PRU0/1[14-0] FT3_START update (where m = 0 to 15).
22	R13	15-8	FT3_MATCH[7-0]	R	0h	RX L2 Filter (Type 3) Match Vector Status. 0h: No Match 1h: Match Clear on RX_L2_DONE event. Clear on MII_G_RT_FT3_m_START_PRU0/1[14-0] FT3_START update (where m = 0 to 15).
22	R14	7-0	FT3_VLD[15-8]	R	0h	Valid Status of RX L2 Filter-Type 3 (Content Filter). Clear on RX_L2_DONE event. Clear on MII_G_RT_FT3_m_START_PRU0/1[14-0] FT3_START update (where m = 0 to 15).
22	R14	15-8	FT3_MATCH[15-8]	R	0h	RX L2 Filter (Type 3) Match Vector Status. 0h: No Match 1h: Match Clear on RX_L2_DONE event. Clear on MII_G_RT_FT3_m_START_PRU0/1[14-0] FT3_START update (where m = 0 to 15).
22	R15	9-0	SA_HASH	R	0h	SA Hash Value. Hash of SA6:SA1

Table 12-12. MII_G_RT RX Classifier Broadside Mapping (continued)

BS ID	BS R	Bit	Name	Type	Reset	Description
22	R15	16	SA_HASH_VLD	R	0h	SA Hash Valid. Set when SA Hash is completed.. Clear on RX_L2_DONE event.
22	R16	10-0	CONN_HASH	R	0h	Connection Hash Value. Hash CONN4:CONN1
22	R16	16	CONN_HASH_VLD	R	0h	Connection Hash Valid. Set when Connection Hash is completed. Note: controlled by MII_G_RT_CONN_HASH_PRU0/1[9-0] CONN_HASH_SEED Clear on RX_L2_DONE event.
22	R17	0	RX_RATE_STATUS0	R	0h	RX Rate Status0. 0h: Green 1h: Red
22	R17	1	RX_RATE_STATUS1	R	0h	RX Rate Status1. 0h: Green 1h: Red
22	R17	2	RX_RATE_STATUS2	R	0h	RX Rate Status2. 0h: Green 1h: Red
22	R17	3	RX_RATE_STATUS3	R	0h	RX Rate Status3. 0h: Green 1h: Red
22	R17	4	RX_RATE_STATUS4	R	0h	RX Rate Status4. 0h: Green 1h: Red
22	R17	5	RX_RATE_STATUS5	R	0h	RX Rate Status5. 0h: Green 1h: Red
22	R17	6	RX_RATE_STATUS6	R	0h	RX Rate Status6. 0h: Green 1h: Red
22	R17	7	RX_RATE_STATUS7	R	0h	RX Rate Status7. 0h: Green 1h: Red
22	R17	23-8	RX_CLASS[15-0]	R	0h	RX Class Status.

12.2.3.7.6.4.2 PRU_ICSSG RX L2 Filter - Type 1 (MAC Filter) Operation

Rules:

- RX L2 Filter (Type 1) attributes can only get updated when the filter is not active
- All 8 × RX L2 Filters (Type 1) will always start at the same time (default is 1st Byte)

Operation:

- RX L2 Filter (Type 1) will have 8 compare functions active concurrently
- RX L2 Filter (Type 1) will start on Byte 1 of the RX Frame by default
- MII_G_RT_FT1_START_LEN_PRU0/1[14-0] FT1_START bitfield (where n = 0 or 1) can be used by software to restart or delay the activation of the Type 1 filter.
- MII_G_RT_FT_RX_PTR_PRU0/1[31-0] FT_RX_PTR_PRUn bitfield (where n = 0 or 1) can be used by software to determine the current byte the filter is working on.

Example for initial setup of RX filter (Type 1):

- Write 1h to MII_G_RT_FT1_START_LEN_PRU0/1[14-0] FT1_START bitfield
- Write 1h to MII_G_RT_FT_RX_PTR_PRU0/1[31-0] FT_RX_PTR_PRUn bitfield (where n = 0 or 1)
- After 22 Bytes, then MII_G_RT_FT_RX_PTR_PRU0/1[31-0] FT_RX_PTR_PRUn = 22 (where n = 0 or 1). The software can then set MII_G_RT_FT1_START_LEN_PRU0/1[14-0] FT1_START = 36 (this action will clear all Type1 filter status bits)
- When MII_G_RT_FT_RX_PTR_PRU0/1[31-0] FT_RX_PTR_PRUn = 36 (where n = 0 or 1), the RX filter Type 1 will start again on Byte 36

12.2.3.7.6.4.3 PRU_ICSSG RX L2 Filter - Type 3 (Content Filter) Operation

Rules:

- RX L2 Filter (Type 3) attributes can only get updated when the filter is not active.
- RX L2 Filter (Type 3) must start on Byte 13 or later

Note: The MII_G_RT_FT3_0_START_PRUn[14-0] FT3_START bit field of “0” contains 1st Byte after preamble

Operation:

- RX L2 Filter (Type 3) will have 16 compare functions active concurrently
- This RX L2 Filter (Type 3) has no dependencies or interaction with RX L2 Filter Type1
- Each of the 16 RX L2 filters (Type 3) have unique start values. See registers MII_G_RT_FT3_0_START_PRU0/1 to MII_G_RT_FT3_15_START_PRU0/1.

RX L2 Filter (Type 3) can start operation on Byte 13 or Byte 17:

- The RX L2 Filter (Type 3) can start operation on Byte 13, if Byte 14 and Byte 13 (16-bit field) are different than value of 0x8100 (this is Tag Protocol Identifier (TPID) IEEE 802.1Q-tagged frame)
- The RX L2 Filter (Type 3) can start operation on Byte 17, if Byte 14 and Byte 13 (16-bit field) are equal to value of 0x8100 in order to identify the frame as IEEE 802.1Q-tagged frame (this is Tag Protocol Identifier (TPID) IEEE 802.1Q-tagged frame)

12.2.3.7.6.4.4 PRU_ICSSG RX L2 Filter - Type 3 (Content Filter) Auto Restart operation

The RX L2 Filter (type 3) have an optional auto offset adjust and continue the next comparison if not match has been found. It will continue to do this until the first hit is found. This mode is enabled when one or more bits is set in MII_G_RT_FT3_m_CFG_PRUn[31-16] FT3_m_TRIG_OR_EN (where m = 0 to 15 and n = 0 or 1). This function only works on RX L2 Filter (type 3) pattern compare function, which is 64-bit compare function.

Rules:

- Only EQ function is allowed and It uses the following configuration registers:
- MII_G_RT_FT3_m_CFG_PRUn[14-0] FT3_m_IJMP_OFFSET_PRUn (where m = 0 to 15 and n = 0 or 1) - relative byte offset jump used after first trigger hit
- MII_G_RT_FT3_m_CFG_PRUn[30-16] FT3_m_NJMP_OFFSET_PRUn (where m = 0 to 15 and n = 0 or 1) - relative byte offset jump used after the first auto compare function and beyond
- MII_G_RT_FT3_m_CFG_PRUn[31-16] FT3_m_TRIG_OR_EN (where m = 0 to 15 and n = 0 or 1) - Simple OR select to determine which FT3 match will cause the first initial jump and auto compare sequence to get enabled. Software can not enable same FT3 to cause its own trigger.
- MII_G_RT_FT3_m_LEN_PRUn[8-0] FT3_m_LEN_START_BIT_PRUn (where m = 0 to 15 and n = 0 or 1) - relative bit offset from the HIT byte location upto 512 bit offset
- MII_G_RT_FT3_m_LEN_PRUn[19-16] FT3_m_LEN_SIZE_BIT_PRUn (where m = 0 to 15 and n = 0 or 1) - used to determine where to end the extraction to determine the on the fly length byte offset

12.2.3.7.6.4.5 RX SA Hash

SA6:SA1 is hashed using the below polynomial providing a 10-bit value:

$$x^{10} + x^7 + x^2 + 1$$

This value can be read through MII_G_RT_SA_HASH_PRU0/1[9-0] SA_HASH_SEED registers.

By default the initial value of MII_G_RT_SA_HASH_PRU0/1[9-0] SA_HASH_SEED bitfield is set to 0h unless software updates it. Given a fixed set of addresses, changing the seed can drastically change the distribution of the result. Given random inputs, the distribution would be random as well.

12.2.3.7.6.4.6 RX Connection Hash

4 Bytes of the packet (P(n+3):Pn) are hashed using the below polynomial providing a 10-bit value.

$$x^{10} + x^7 + x^2 + 1$$

This 10-bit value can be read through MII_G_RT_CONN_HASH_PRU0/1[9-0] CONN_HASH_SEED registers.

By default the initial value of MII_G_RT_CONN_HASH_PRU0/1[9-0] CONN_HASH_SEED bitfield is set to 0h unless software updates it. Given a fixed set of addresses, changing the seed can drastically change the distribution of the result. Given random inputs, the distribution would be random as well.

12.2.4 PRU_ICSSG TX MII Interface

The PRU core directly drives the MII transmit interface via its R30 internal register. The contents of R30 register and RX Data from receive interface are taken and fed into a transmit FIFO (TX L2 FIFO - 64 Bytes).

Data to be transmitted is loaded into the TX L1 FIFO. The transmit FIFO (TX L1) stores up to 40 Bytes of transmit data. Note that this includes the preamble bytes. From the transmit FIFO (TX L1), the data is sent to the MII TX port of the PHY by the MII_RT transmit logic.

The transmit FIFO also has the capability to be reset through software (TX_RESET). When reset, all contents of transmit FIFO are purged and this may result in a frame not getting transmitted as expected, if the transmission is already ongoing. Any new data written in the transmit FIFO results in a new frame being composed and transmitted. An overflow event will require a TX_RESET to recover from this condition.

There are four dependencies that must be true for TX_EN to assert:

1. TX L1 FIFO not empty
2. Interpacket gap (IPG) timer expiration
3. RX_DV to TX_EN timer expiration
4. TX_EN compare timer expiration

The transmit interface also provides an underflow error signal in case there was no data loaded when TX_EN triggered. The transmit underflow signal is mapped to the INTC in PRU_ICSSG. The current FIFO fill level cannot be accessed by PRU firmware. The firmware can issue an R31 command via R31 bit 29 (TX_EOF) to indicate that the last byte has been written into the TX FIFO.

12.2.4.1 TX Data Path Options to TX L1 FIFO

There are two data path options for delivering data to the TX L1 FIFO and transmit port, described further in the subsequent sections:

1. PRU → TX L1 FIFO → TX MII port
2. RX L1 FIFO → TX L1 FIFO → TX MII port

12.2.4.1.1 PRU → TX L1 FIFO → TX MII Port

The PRU can be used to feed data into the TX L1 FIFO using the R30 and R31 registers, shown in [Figure 12-22](#). The PRU has the option to write up two or four bytes of R30 and then pushes the data into the TX L1 FIFO by writing to the R31 command interface.

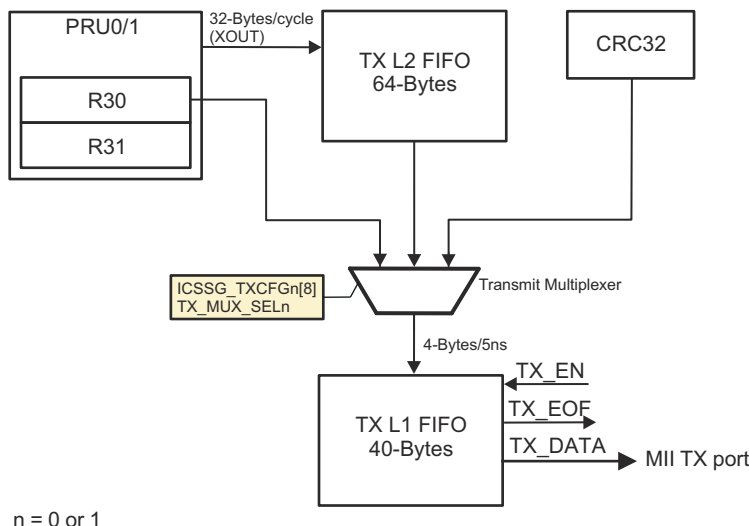


Figure 12-22. PRU to TX L1 FIFO Interface

12.2.4.1.1.1 TX L2 FIFO Features

- 64-Bytes deep TX L2 FIFO which feeds data into a 40-Bytes deep TX L1 FIFO
- Maximum of 64-Bytes Broad Side load, minimum of 1-Byte Broad Side load, R2.b0(start)
- Note:** [MII_RT_TXCFG0/1\[3\] TX_BYTE_SWAPn bit \(where n = 0 or 1\)](#) is not supported for TX L2 FIFO.
- FIFO level status available through [MII_RT_TX_FIFO_LEVEL0\[7-0\] TX_FIFO_LEVEL0](#) and [MII_RT_TX_FIFO_LEVEL1\[7-0\] TX_FIFO_LEVEL1](#) registers
- 2 FIFO threshold events: 32-Bytes (available and empty) or 64-Bytes (available)
- Total bytes sent for a current/last frame is available for software
- New frame can start after TX L2 FIFO is empty, but before TX L1 FIFO is empty from an old frame
 - Note: Only supported for RGMII and SGMII modes of operation**
 - New frame can start after 5 or more core clock cycles after it is drained, this is required to finish the CRC for the first frame

12.2.4.1.1.2

Table 12-13. TX L2 XFR Mapping

Device ID	Function	Description
40	Data	R17:R2 Data, XOUT Only 1-Byte to 64-Bytes in size LSB packed and no gaps, for example 64-Bytes push R17:R2 32-Bytes push R9:R2 16-Bytes push R5:R2 4-Bytes push R2 7-Bytes push R3(b2.b0):R2 1-Bytes push R2(b0) Can do back to back
40	Control	Control of TX L2 FIFO
40	Status	Status of TX L2 FIFO

Table 12-14. TX L2 Control

BS ID	BS R	Bit	Name	Type	Reset	Description
40	R18	1-0	TAG insertion mode	WO	0h	Sets the TAG mode for next frame or current frame. It will have a one time action per frame. After action, software must rearm for a new action 1 cmd per packet. MII_RT_TXCFG0/1[1] TX_AUTO_PREAMBLEn bit (where n = 0 or 1) must be set to 1h. Note: This bit is self cleared.

Table 12-14. TX L2 Control (continued)

BS ID	BS R	Bit	Name	Type	Reset	Description
40	R18	2	VLAN removal	WO	0h	If set, it will remove 4-Bytes of VLAN. This is only valid when TX L2 FIFO is enabled through ICSS_G_CFG[1] TX_L2_ENABLE bit (value 1h) and MII_RT_TXCFG0/1[1] TX_AUTO_PREAMBLE_n = 1h (where n = 0 or 1) then Byte13, Byte14, Byte15, Byte16 will get removed. Note: Byte1 is the first byte which is pushed by PRU core. Note that the first 2 bytes of the VLAN must match the value in MII_G_RT_TX_VLAN_TYPE_TAG_PORT0/1[15-0] TX_VLAN_TYPE_TAG bit field (reset state is 81h). If not, the 4-Bytes will NOT get removed. A RXVLANRemoval flag will get set if the action occurred Allow all combos of TAG + VLAN IN. Note: This will be defined in a matrix. Note: This bit is self cleared.
40	R18	4	EXP_FRAME	WO	0h	Must be set for all EXP_FRAME. We have 3 types of frames: - Implicit EXP_FRAME not set PRE_FRAME - Not set SMD == 0xd5 EXP_FRAME (use a SMD_EXP) - EXP_FRAME set PRE_FRAME not set. PRE_FRAME (use MII_G_RT_SMDT1S_CFG .SMDT1S_n for initial and MII_G_RT_SMDT1C_CFG .SMDT1C_n + MII_G_RT_FRAG_CNT_CFG .FRAG_CNT_n for non initial) EXP_FRAME set PRE_FRAME not set. Note: This bit is self cleared on EOF.
40	R18	6	RESERVED	R	0h	Reserved
40	R18	7	EOF_MCRC_REQ	WO		Set this bit before TX L1 FIFO is empty to generate a MCRC vs CRC. Note: This bit is self cleared on EOF.
40	R18	11-8	RESERVED	R	0h	Reserved

Table 12-15. TX L2 Status

BS ID	BS R	Bit	Name	Type	Reset	Description
40	R19	11-0	TXL2ByteSentCount	R	0h	This bit field defines the number of bytes transmitted to TX L1 FIFO. The count will remain persistent until the next frame starts. This will get used to determine the number of bytes which got transmitted after a Preemption event. This includes all data pushed by the PRU core, which did get transmitted. It does not include the CRC.
40	R19	12	RESERVED	R	0h	Reserved
40	R19	13	RXVLAN Removal	R/W1C	0h	This bit will be set when VLAN removal occurred. VLAN removal will only occur if TPID value is equal to the value in MII_G_RT_TX_VLAN_TYPE_TAG_PORT0/1[15-0] TX_VLAN_TYPE_TAG bit field (reset state is 81h). Software can clear sticky used for debug.
40	R19	14	RESERVED	R	0h	Reserved
40	R19	15	RESERVED	R	0h	Reserved
40	R19	22-16	TXL2Occ	R	0h	This bit field defines the current number of bytes in TX L2 FIFO. 0h: 0 bytes, or empty FIFO buffer 1h: 1 byte ... 64h = 64 bytes, or full FIFO buffer

Table 12-16. TX L2 TAG Modes

TAG Mode	At	What to Push/Add to the Frame
0	None	Nothing
1	Push TAG1	Byte 13 = VLAN_PORT<1/0>[7-0] Byte 14 = VLAN_PORT<1/0>[15-8] Byte 15 = VLAN_PORT<1/0>[23-16] Byte 16 = VLAN_PORT<1/0>[31-24] Used for Host. Host -> PRU_ICSSG -> add VLAN TAG -> Port SFD offset issues
2	Push TAG2	Byte 13 = HTAG_PORT<1/0>[7-0] Byte 14 = HTAG_PORT<1/0>[15-8] Byte 15 = HTAG_PORT<1/0>[23-16] Byte 16 = HTAG_PORT<1/0>[31-24] Byte 17 = SEQ_PORT<1/0>[7-0] Byte 18 = SEQ_PORT<1/0>[15-8]
3	Push TAG3	Byte 13 = VLAN_PORT<1/0>[7-0] Byte 14 = VLAN_PORT<1/0>[15-8] Byte 15 = VLAN_PORT<1/0>[23-16] Byte 16 = VLAN_PORT<1/0>[31-24] Byte 17 = HTAG_PORT<1/0>[7-0] Byte 18 = HTAG_PORT<1/0>[15-8] Byte 19 = HTAG_PORT<1/0>[23-16] Byte 20 = HTAG_PORT<1/0>[31-24] Byte 21 = SEQ_PORT<1/0>[7-0] Byte 22 = SEQ_PORT<1/0>[15-8]

12.2.4.1.1.3 TX Insertion

There are 3 TAG Insertion modes that software can select. Note that the mode must be selected before the first byte is pushed into the TX FIFO. The values, pushed into the TX FIFO are defined in the MII_RT_TX_FIFO_LEVEL0/1[7-0] TX_FIFO_LEVELn registers (where n = 0 or 1).

Table 12-17. TX VLAN_TAG Cases

Case	RM VLAN	ADD VLAN	ADD HSR	In packet	Out packet
1	1	0	0	If pkt[B13:B14] == vlan_type_id	B16, B15, B14, B13 will be removed. If packet is less than 64-Bytes, 0s will get added before the CRC.
2	1	0	0	If pkt[B13:B14] != vlan_type_id	No effect.
3	0	1	0	X	VLAN_TAG added 4-Bytes. Start B13.
4	0	0	1	X	HSR_TAG added 6-Bytes. Start B13.
5	0	1	1	X	VLAN+TAG and HSR_TAG added 10-Bytes. Start B13.
6	1	1	0	If pkt[B13:B14] == vlan_type_id	B16, B15, B14, B13 will be replaced with VLAN_TAG.
7	1	1	0	If pkt[B13:B14] != vlan_type_id	No effect.
8	1	1	1	If pkt[B13:B14] == vlan_type_id	B16, B15, B14, B13 will be replaced with VLAN_TAG. Then HSR_TAG will be added.
9	1	1	1	If pkt[B13:B14] != vlan_type_id	No effect.
10	1	0	1	If pkt[B13:B14] = vlan_type_id	B16, B15, B14, B13 will be removed and HSR_TAG added 6-Bytes. Start B13.
11	1	0	1	If pkt[B13:B14] != vlan_type_id	HSR_TAG added 6-Bytes. Start B13

12.2.4.1.1.4 TX Preemption

Case 1) Preemptible frame which got fragmented.

1. Idle -> preemptible frame when:
 - PRE_FRAME is set before first data push
2. preemptible -> frag when
 - EOF_MCRC_REQ is set after the last data is pushed into TX L2 FIFO and before TX L1 FIFO is empty
3. frag -> frag when
 - PRE_FRAME is set before first data push and EOF_MCRC_REQ is set after the last data is pushed into TX L2 FIFO and before TX L1 FIFO is empty
4. frag -> lfrag when:
 - PRE_FRAME is set before first data push and TX_EOF_REQ set after the last data is pushed into TX L2 FIFO and before TX L1 FIFO is empty
5. lfrag -> Idle when CRC is pushed into TX L1 FIFO

Case 2) Preemptible frame which did not get fragmented.

1. Idle -> preemptible frame when:
 - PRE_FRAME is set before first data push
2. preemptible -> Idle when
 - TX_EOF_REQ is set before TX L1 FIFO is empty

Note: Express frames can and will occur between the fragments.

Rules:

- Preemptible must get set before the first data is pushed into TX L2 FIFO
- EOF_MCRC_REQ is set after the last data is pushed into TX L2 FIFO and before TX L1 FIFO is empty
- TX_EOF_REQ can only get asserted on the last frag or preemptible frame which did not get fragmented. It can not get asserted in none last fragments.

Note: TX_EOF_REQ can not get asserted when EOF_MCRC_REQ is asserted.

12.2.4.1.1.4.1 TX Preemption Programming Model

Start a new frame.

1. Wait until R31.TX_EOF event
2. Load data into TX L2 FIFO until the full frame is completed
3. Issue a R30.TX_EOF + TX_CRC_HIGH + TX_CRC_LOW

Figure 12-23 shows the R30 transmit interface. The lower 16 bits of the R30 (or FIFO transmit word) contain transmit data nibbles. When [MII_RT_TXCFG0/1\[11\] TX_32_MODE_ENn](#) = 0h - default value (where n = 0 or 1), then the upper 16 bits contain mask information. Alternatively, when [MII_RT_TXCFG0/1\[11\] TX_32_MODE_ENn](#) = 1h (where n = 0 or 1), then the upper 16 bits contain transmit data nibbles. The operation to be performed on the transmit interface is controlled by PRU writes to the R31 command interface. [Table 12-18](#) describes the supported configurations for 8, 16, and 32 bit TX push operations.

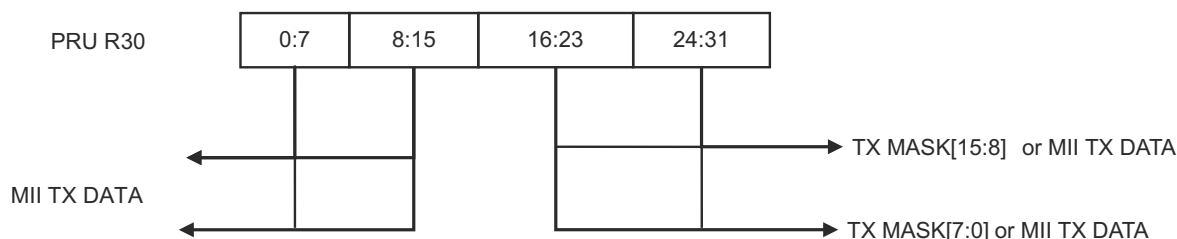


Figure 12-23. PRU to TX MII Interface

Table 12-18. TX Push

R31[25] TX_PUSH16/32	R31[24] TX_PUSH8/32	Supported R30 bits	TX_32_MODE_EN	TX_BYTE_SWAP	TX Push Action
0	1	X	0	X	8 bits of TXDATA (R30[7-0]) pushed post TX mask
1	0	X	0	X	16 bits of TXDATA (R30[15-0]) pushed post TX mask
1	1	X	0	X	Illegal
X	X	0x000000FF	1	0	8 bits of TXDATA (R30[7-0]) pushed
X	X	0x0000FFFF	1	0	16 bits of TXDATA (R30[15-0]) pushed
X	X	0xFFFFFFFF	1	X	32 bits of TXDATA (R30[31-0]) pushed
X	X	All other - reserved	1	X	Reserved

Using [MII_RT_TXCFG0/1\[11\]](#) TX_32_MODE_ENn = 0h and the TX mask, the PRU can send a mix of R30 and RX L1 FIFO data to the TX L1 FIFO. Note the TX mask is only available when the PRU is fed one word or byte at a time by the RX L1 FIFO. It is not applicable when the RX L2 buffer is enabled. To disable TX mask, set TXMASK to 0xFFFF.

As shown in [Figure 12-24](#), the PRU drives the MII transmit interface through its R30 register. The contents of R30 and RX data from the receive interface (RX L1 FIFO) are taken and fed into a 40-Bytes transmit FIFO (TX L1 FIFO).

If [MII_RT_TXCFG0/1\[11\]](#) TX_32_MODE_ENn = 0h (where n = 0 or 1), then before transmission, a mask is applied to the data portion of the R30 register. By using the mask, the PRU firmware can control whether received data from the RX L1 FIFO is sent to transmit, R30 data is sent to transmit, or a mix of the two is sent. The Boolean equation that is used by MII_RT to compose TX data is:

$$\text{TXDATA}[7/15:0] = (\text{R30}[7/15:0] \& \text{MASK}[7/15:0]) \mid (\text{RXDATA}[7/15:0] \& \sim\text{MASK}[7/15:0])$$

As shown in the equation, a mask of FFh will lead to the R30[7:0] being transmitted in an 8-bit transmit operation. A mask of 0h will lead to receive data being sent out in a 16-bit transmit operation.

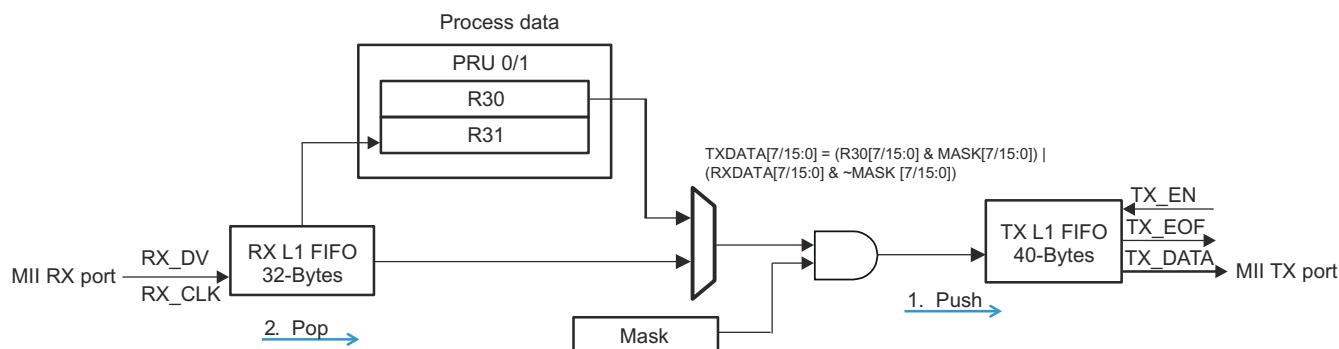


Figure 12-24. TX Mask Mode ([MII_RT_TXCFG0/1\[TX_32_MODE_ENn\]](#) = 0h)

12.2.4.1.2 RX L1 FIFO → TX L1 FIFO (Direct Connection) → TX MII Port

When [MII_RT_TXCFG0/1\[9\]](#) PRE_TX_AUTO_SEQUENCEEn is set to 1h (where n = 0 or 1), the data frame is passed from the RX L1 FIFO to TX L1 FIFO without any interaction of the PRU. This mode of operations is shown in [Figure 12-25](#). The RX L1 FIFO will push data into TX L1 FIFO as long as it is enabled and not full.

There is no PRU dependency in this mode and no option for the PRU to perform any operation to the TX L1 FIFO. RX_RESET clears all data and status elements.

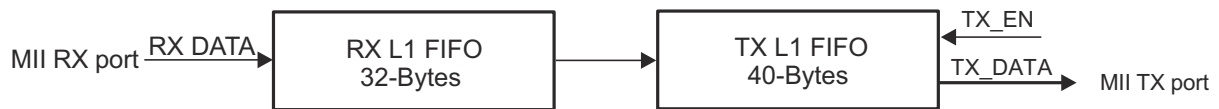


Figure 12-25. RX L1 to TX L1 Interface

For ESC protocols, software should enable [6]RX_AUTO_FWD_PRE0/1 and [4]RX_L2_EN0/1 bits in [MII_RT_RXCFG0/1](#) registers.

For non ESC protocols, software can enable [MII_RT_TXCFG0/1\[1\]](#) TX_AUTO_PREAMBLEn and [MII_RT_RXCFG0/1\[2\]](#) RX_CUT_PREAMBLEn bit (where n = 0 or 1) to insure full preamble is generated for each TX frame.

The PRU core can read the passing through frame by polling the standard R31 register. In Direct mode, the PRU R31 Command is ignored and disabled, except for TX_RESET and RX_RESET.

The following are the legal configurations supported for Direct Connection:

- Configuration 1:
 - PORT1.RX -> PRU1 (snoop only)
 - PORT1.RX -> PORT0.TX
- Configuration 2:
 - PORT0.RX -> PRU0 (snoop only)
 - PORT0.RX -> PORT1.TX
- Configuration 3:
 - PORT1.RX -> PORT1.TX
- Configuration 4:
 - PORT0.RX -> PORT0.TX

12.2.5 PRU R31 Command Interface

The PRU uses writes to R31[31-16] to control the reception and transmission of packets in direct and register mode. [Table 12-19](#) lists the available commands. Each bit in the table is a single clock pulse output from the PRU. When more than one action is to be performed in the same instant, the PRU firmware must set those command bits in one instruction.

Table 12-19. PRU R31: Command Interface (Write Mode)

Bit	Command	Description
31	TX_CRC_ERR	TX_CRC_ERR command when set will add 0xA5 byte to the TX L1 FIFO if the current FCS is valid. This bit can only be set with the TX_EOF command and optionally with the TX_ERROR_NIBBLE command. It cannot get set with any other commands, and the PRU firmware must wait > 2 clocks from the last command. Note: For proper operations auto-forward preamble must be enabled.
30	TX_RESET	TX_RESET command is used to reset the transmit FIFO and clear all its contents. This is required to recover from a TX FIFO overrun.
29	TX_EOF	TX_EOF command is used to indicate that the data loaded is considered last for the current frame
28	TX_ERROR_NIBBLE	TX_ERROR_NIBBLE command is used to insert an error nibble. This makes the frame invalid. Also, it will add 0x0 after the 32-bit CRC.
27	TX_CRC_HIGH	TX_CRC_HIGH command ends the CRC calculations and pushes CRC[31-16] to append to the outgoing frame in the TX L1 FIFO. Note: TX_CRC0/1 will become valid after 6 clock cycles.
26	TX_CRC_LOW	TX_CRC_LOW command pushes CRC[15-0] to append to the outgoing frame in the TX L1 FIFO.
25	TX_PUSH16	TX_PUSH16 command pushes R30[15-0] when MII_RT_TXCFG0/1[11] TX_32_MODE_ENn = 0h (where n = 0 or 1). See Table 12-18 , TX Push for more details. Note: There are no restrictions on concurrent PUSH/POP nor R30 requirements to maintain data. Back to back PUSH is supported.

Table 12-19. PRU R31: Command Interface (Write Mode) (continued)

Bit	Command	Description
24	TX_PUSH8	TX_PUSH8 command pushes R30[7-0] when MII_RT_TXCFG0/1[11] TX_32_MODE_ENn = 0h (where n = 0 or 1). See Table 12-18, TX Push for more details. Note: There are no restrictions on concurrent PUSH/POP nor R30 requirements to maintain data. Back to back PUSH is supported.
23	RX_ERROR_CLR	RX_ERROR_CLR command is used to clear RX_ERROR indicator bit by writing 1h.
22	RX_EOF_CLR	RX_EOF_CLR command is used to clear RX_EOF status indicator bit by writing 1h.
21	RX_SFD_CLR	RX_SFD_CLR command is used to clear RX_SFD indicator bit by writing 1h.
20	RX_SOF_CLR	RX_SOF_CLR command is used to clear RX_SOF indicator bit by writing 1h.
19	Reserved	Reserved
18	RX_RESET	RX_RESET is used to reset the receive FIFO and clear all contents. This is required to recover from a RX FIFO overrun, if software does not want to undrain. The typical use case is assertion after RX_EOF. If asserted during an active frame, the following actions will occur: 1. Terminate the current frame 2. Block/terminate all new data 3. Flush/clear all FIFO elements 4. Cause RX state machine into an idle state 5. Cause EOF event 6. Cause minimum frame error, if you abort before minimum size reached
17	RX_POP16	RX_POP16 command advances the receive traffic by two bytes. This is only required when you are using R31 to read the data. After R31[15-0] is ready to read by PRU, it will set 1h to WORD_RDY, and the next new data will be allowed to advance. RX_POP16 to WORD_RDY update has 2 clock cycles latency. Firmware needs to insure it does not read WORD_RDY/BYTE_RDY until 2 clock cycles after RX_POP16.
16	RX_POP8	RX_POP8 command advances the receive traffic by one bytes. This is only required when you are using R31 to read the data. After R31[7-0] is ready to read by PRU, it will set 1h to BYTE_RDY, and the next new data will be allowed to advance. RX_POP8 to BYTE_RDY update has 2 clock cycles latency. Firmware needs to insure it does not read WORD_RDY/BYTE_RDY until 2 clock cycles after RX_POP8.

12.2.6 Other Configuration Options

12.2.6.1 Nibble and Byte Order

The PRU core is little endian. To support big endian, the MII_G_RT supports optional nibble swapping on both the RX and TX side.

On the receive side, the order of the two data bytes in RX R31 and the RX L2 buffer are configurable through the RX_BYTE_SWAP0/1 bit in the [MII_RT_RXCFG0/1](#) registers, as shown in [Table 12-20](#). Note: The Nibble0 is the first nibble received.

Table 12-20. RX Nibble and Byte Order

Configuration	Order
MII_RT_RXCFG0/1[5] RX_BYTE_SWAPn = 0h (default), where n = 0 or 1	R31[15-8] / RXL2[15-8] = Byte1{Nibble3, Nibble2} R31[7-0] / RXL2[7-0] = Byte0{Nibble1, Nibble0}
MII_RT_RXCFG0/1[5] RX_BYTE_SWAPn = 1h, where n = 0 or 1	R31[15-8] / RXL2[15-8] = Byte0{Nibble1, Nibble0} R31[7-0] / RXL2[7-0] = Byte1{Nibble3, Nibble2}

On the transmit side, the order of the two data bytes and mask bytes in TX R30 are configurable through the TX_BYTE_SWAP0/1 bit in the [MII_RT_TXCFG0/1](#) registers, as shown in [Table 12-21](#). Note the Nibble0 is the first nibble transmitted.

Table 12-21. TX Nibble and Byte Order

Configuration	Order
MII_RT_TXCFG0/1[3] TX_BYTE_SWAPn = 0h (default), where n = 0 or 1	If MII_RT_TXCFG0/1[11] TX_32_MODE_ENn = 0h, where n = 0 or 1 R30[15-8] = Byte1{Nibble3, Nibble2} R30[7-0] = Byte0{Nibble1, Nibble0} R30[31-24] = TX_MASK[15-8] R30[23-16] = TX_MASK[7-0] If MII_RT_TXCFG0/1[11] TX_32_MODE_ENn = 1h, R30[31-24] = Byte3{Nibble7, Nibble6} R30[23-16] = Byte2{Nibble5, Nibble4} R30[15-8] = Byte1{Nibble3, Nibble2} R30[7-0] = Byte0{Nibble1, Nibble0}
MII_RT_TXCFG0/1[3] TX_BYTE_SWAPn = 1h, where n = 0 or 1	If MII_RT_TXCFG0/1[11] TX_32_MODE_EN = 0h, R30[15-8] = Byte0{Nibble1, Nibble0} R30[7-0] = Byte1{Nibble3, Nibble2} R30[31-24] = TX_MASK[7-0] R30[23-16] = TX_MASK[15-8] If MII_RT_TXCFG0/1[11] TX_32_MODE_EN = 1h, Only 32-bit push is supported. R30[31-24] = Byte0{Nibble1, Nibble0} R30[23-16] = Byte1{Nibble3, Nibble2} R30[15-8] = Byte2{Nibble5, Nibble4} R30[7-0] = Byte3{Nibble7, Nibble6}

12.2.6.2 MII_G_RT Preamble Source

The MII_G_RT module has the option to preserve and forward a received preamble in the TX data stream, use a preamble provided by the PRU, or auto-generate a preamble. These configurations are highlighted in [Table 12-22](#).

Table 12-22. Preamble Configuration Options

RX_CUT_PREAMBLE	Determines whether RX preamble is passed to the RX L1/L2 FIFO
RX_AUTO_FWD_PRE	Determines whether RX preamble is automatically passed to TX L1 FIFO
TX_AUTO_PREAMBLE	TX interface logic auto-generates and appends preamble to TX data stream with the first push of data into the TX L1 FIFO. Note that enabling this option does fill the TX FIFO with the preamble length, hence software has to consider this to not overrun the TX FIFO.

12.2.6.3 PRU and MII Port Multiplexer

The MII_G_RT module supports configurable PRU core to MII TXn / RXn port mapping. By default, PRU0 is mapped to TX1 and RX0 and PRU1 is mapped to TX0 and RX1. However, the system supports the flexibility to map any PRU core to any TX and RX port. For example, the input to PRU0 can be either RX_MII0 or RX_MII1. Similarly, the input to TX_MII0 can be either PRU0 or PRU1.

12.2.6.3.1 Receive Multiplexer

A multiplexer is provided to allow selecting either of the two MII interfaces (RX_MII0 or RX_MII1) for the receive data that is sent to PRU. [Figure 12-26](#) shows a simple diagram of PRU receive multiplexer.

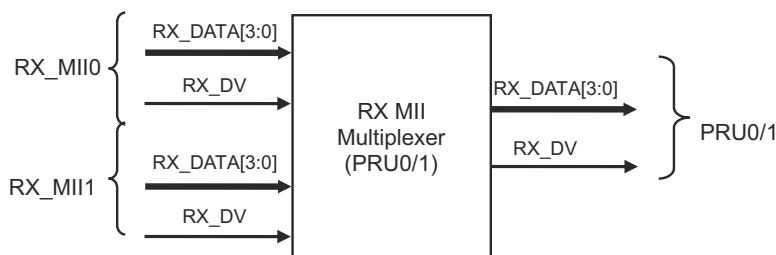


Figure 12-26. MII Receive Multiplexer

There are two receive multiplexer instances to enable selection of RX MII path for each PRU. The select lines of the RX multiplexers are driven from the PRU_ICSSG programmable registers ([MII_RT_RXCFG0/1\[3\]](#) RX_MUX_SEL_n, where n = 0 or 1).

12.2.6.3.2 Transmit Multiplexer

On the MII transmit ports, there is a multiplexer for each MII transmit port that enables selection of either the transmit data from the PRUs or from the RX MII interface of the other MII interface. [Figure 12-27](#) shows a simple diagram of PRU transmit multiplexer.

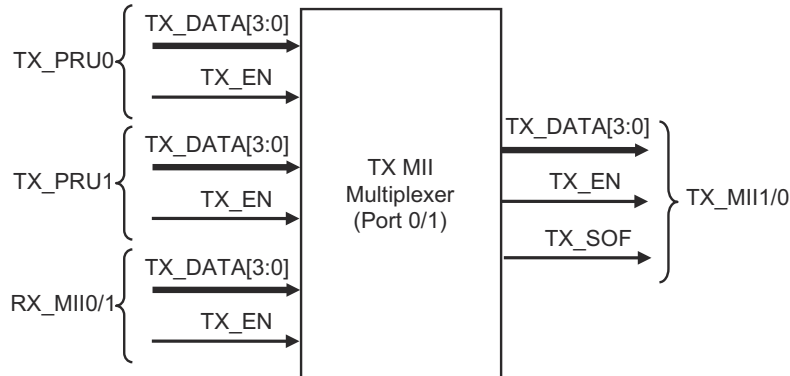


Figure 12-27. MII Transmit Multiplexer

The transmit multiplexers enable the PRU_ICSSG to either operate in a bypass mode where the PRU is not involved in processing MII traffic or use of one of the PRU cores for transmitting data into the MII interface. There are two instances of the TX MII multiplexer and the select lines for each TX multiplexer are provided by the PRU_ICSSG programmable registers ([MII_RT_TXCFG0/1\[8\]](#) TX_MUX_SEL_n, where n = 0 or 1). The select lines are common between register and FIFO interface. It is expected that the select lines will not change during the course of a frame so that can avoid data exchange error.

12.2.6.4 RX L2 Scratch Pad

When the RX L2 is disabled ([MII_RT_RXCFG0/1\[4\]](#) RX_L2_EN_n = 0h, where n = 0 or 1), the RX L2 banks can be used as a generic scratch pad. In scratch pad mode, RX L2 Bank0 and RX L2 Bank1 operate like simple read/write memory mapped registers. All XFR size and start operations are supported. RX_RESET has no effect in this mode. This mode is shown in [Figure 12-28](#).

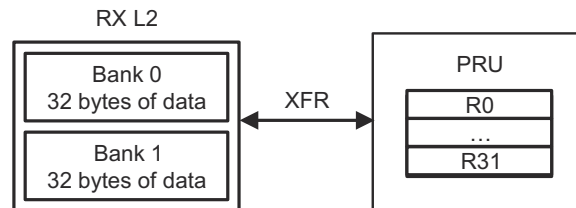


Figure 12-28. Scratch Pad Mode

12.3 SGMII Mode Of Operation

MIIG_RT implements the SGMII block. This block is used to convert GMII into SGMII signals after WIZ interface. The SGMII mode can be enabled through SGMII_ICSS_G_CFG[16] SGMII_MODE bit (=1).

Figure 12-29 shows top level block diagram of the CPSGMII module

Note

Software must configure the SerDes WIZ before it enables SGMII mode, this will insure CPSGMII logic is held in reset until the SerDes WIZ comes on-line. Software must add additional delay (~ 100 ns) after the last WIZ config before SGMII is enabled to remove any race condition.

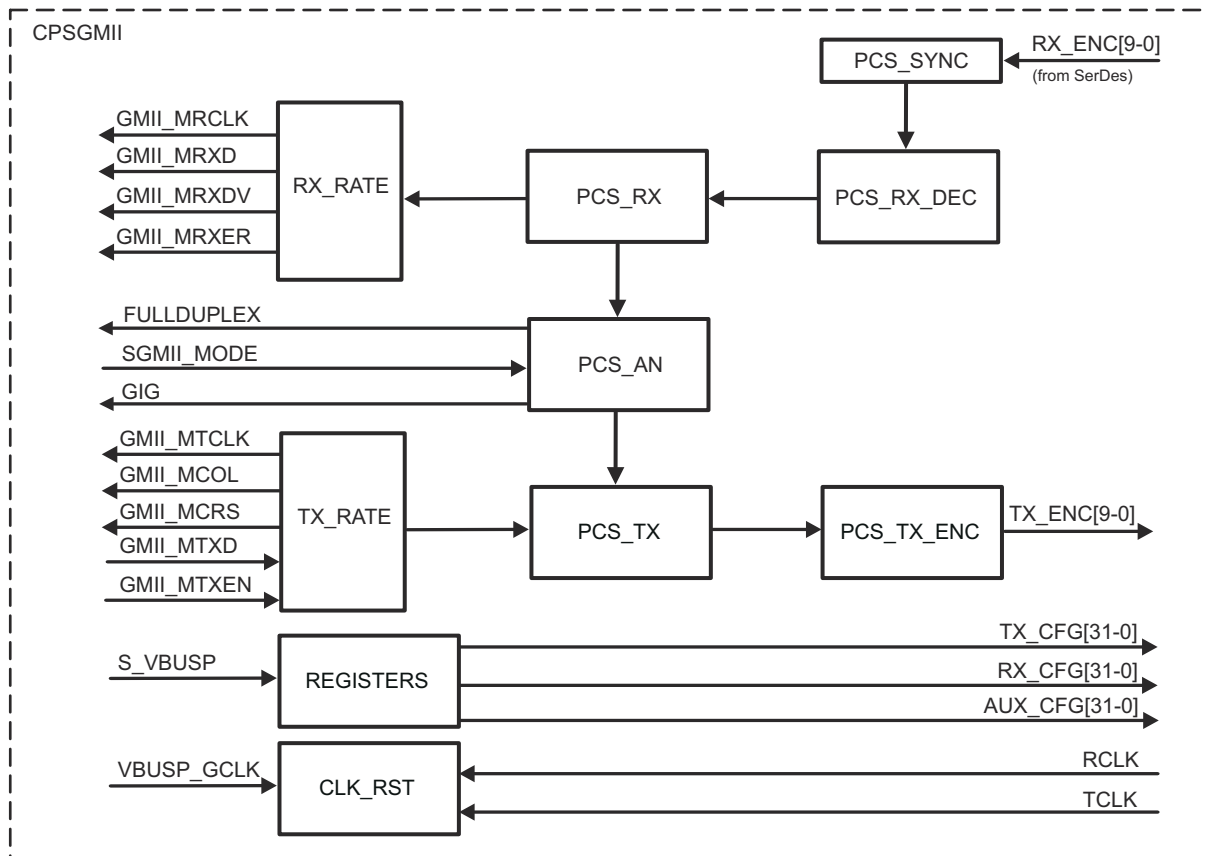


Figure 12-29. CPSGMII Top Level Block Diagram

CPSGMII Features:

- Supports SGMII interface to CPGMAC GMII interface
- 8B/10B Encoding and Decoding
- Compatible with Serial GMII Specification version 1.8
- SGMII mode or Fiber mode is pin selectable
- SGMII mode supports SGMII auto-negotiation (with 1.6ms link timer)
- Fiber mode supports 802.3z clause 37 auto-negotiation (with 10ms link timer)
- SGMII mode supports direct CPSGMII to CPSGMII connection (master/slave configurable via register) with auto-negotiation or with forced link
- CBA 3.1 compliant slave interface
- SGMII support:
 - SerDes datacom variant
 - Requires AC coupling of CML I/O's to interface to LVDS levels
 - 4-pin SGMII implementation (differential data) with clock recovery (transmit clock not included)
 - SerDes configuration programmable through CPSGMII VBUSP slave interface

- SerDes supports power down

12.3.1 CPSGMII Receive Interface

The CPSGMII receive (Rx) interface converts the encoded receive input (RX_ENC[9-0]) from the SerDes into the required CPGMAC GMII signals.

12.3.2 CPSGMII Transmit Interface

The CPSGMII transmit (Tx) interface converts the CPGMAC GMII input data in to the required encoded transmit outputs (TX_ENC[9-0]). The CPGMAC does not source the transmit error signal. Any transmit frame from the CPGMAC with an error (i.e. Underrun) will be indicated as an error by an error CRC. Transmit error is assumed to be 0h at all times and is not input to the CPSGMII module.

Note: In 10/100-Mbit mode, the GMII_MTXD(7:0) data bus uses only the lower nibble.

Any packet in transmission from the CPGMAC while the link signal is deasserted will be ignored. Only packets that begin after the rising edge of link signal will be transferred.

12.3.3 CPSGMII Loopback

The loopback bit ([4]LOOPBACK) in the SGMII [SGMII_CONTROL_REG](#) enables the loopback mode. When loopback is asserted, transmit interface is internally connected to receive interface. This is digital loopback (before the SerDes) from the CPSGMII transmit to the CPSGMII receive. The [1]RT_SOFT_RESET bit in the [SGMII_SOFT_RESET_REG](#) register is used to reset the transmit and receive logic when switching to and from loopback mode. The sequence for entering or exiting the loopback mode is shown below:

1. Clear to 0 the [0] MR_AN_ENABLE bit in the SGMII [SGMII_CONTROL_REG](#) register
2. Write 1 to the [1] RT_SOFT_RESET bit in the [SGMII_SOFT_RESET_REG](#) register
3. Write 1 to the [4] LOOPBACK bit in the SGMII [SGMII_CONTROL_REG](#) register
4. Write 0 to the [1] RT_SOFT_RESET bit in the [SGMII_SOFT_RESET_REG](#) register

12.3.4 CPSGMII Mode - CPGMAC to PHY

Figure 12-30 below shows the SGMII mode of operation.

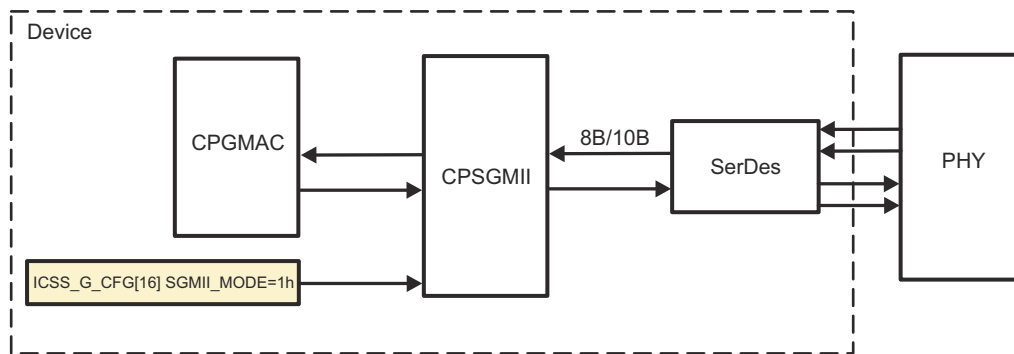


Figure 12-30. CPGMAC to PHY Block Diagram

The following sequence shows the CPSGMII setup for SGMII mode of operation:

1. Setup the CPSGMII and enable auto-negotiation:
 - [SGMII_MR_ADV_ABILITY_REG](#)[15-0] MR_ADV_ABILITY = 1h (MAC to PHY configuration register)
 - [SGMII_CONTROL_REG](#)[0] MR_AN_ENABLE = 1h (enable auto-negotiation, slave mode)
2. Poll the [SGMII_STATUS_REG](#)[1] AN_ERROR bit to determine when auto-negotiation is complete without error. The [1]AN_ERROR bit in the [SGMII_STATUS_REG](#) will be set to 1h if the mode was commanded to be half-duplex Gigabit.
3. Setup the CPGMAC as shown in the CPGMAC specification. The EXT_EN bit in the [SGMII_MAC_CONTROL](#) register must be set to 1h to allow the speed and duplexity to be set by the signals from the CPSGMII.

12.3.5 Fiber Mode - CPGMAC to PHY

Figure 12-31 below shows the Fiber mode of operation.

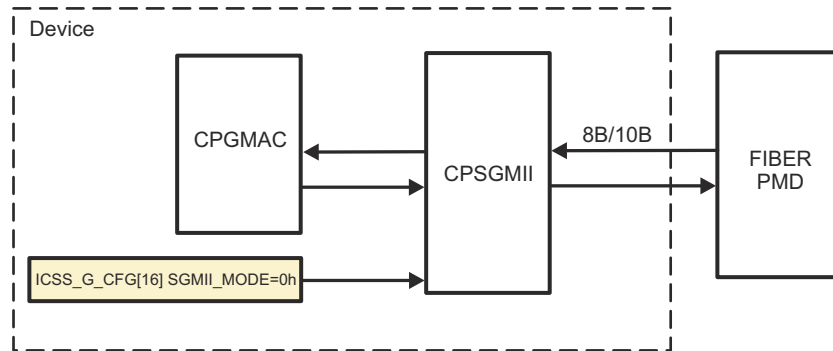


Figure 12-31. CPGMAC to PHY (Fiber mode) Block Diagram

The following sequence shows the CPSGMII setup for Fiber mode of operation:

1. Setup the CPSGMII and enable auto-negotiation:
 - [SGMII_MR_ADV_ABILITY_REG\[15-0\]](#) MR_ADV_ABILITY = 20h (Advertise full duplex only)
 - [SGMII_CONTROL_REG\[0\]](#) MR_AN_ENABLE = 1h (enable auto-negotiation, slave mode)
2. Poll the [SGMII_STATUS_REG\[1\]](#) AN_ERROR bit to determine when auto-negotiation is complete without error. The [1]AN_ERROR bit in the [SGMII_STATUS_REG](#) will be set to 1h if full duplex cannot be negotiated. Software is responsible for reading the [SGMII_MR_LP_ADV_ABILITY_REG](#) register to determine the remote fault encoding and the pause encoding as detailed in IEEE Std. 802.3 clause 37.
3. Setup the CPGMAC as shown in the CPGMAC specification. The EXT_EN bit in the SGMII_MAC_CONTROL register can be set to 1h to allow the speed and duplexity to be set by the signals from the CPSGMII. Otherwise, Fiber mode of operation should be full duplex Gigabit.

12.3.6 SGMII Mode - CPGMAC to CPGMAC (with auto-negotiation)

Figure 12-32 below shows the direct SGMII CPGMAC to CPGMAC mode of operation.

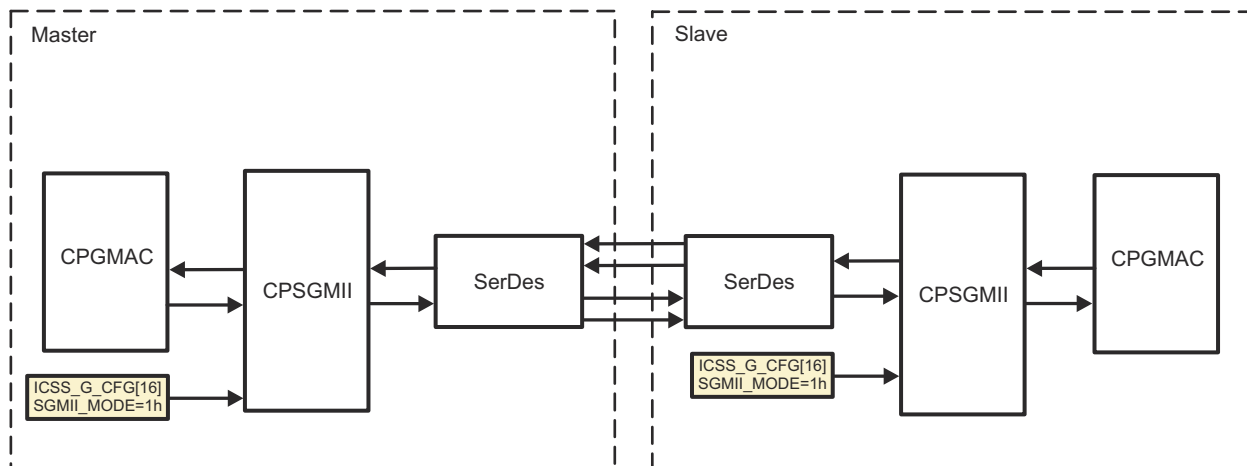


Figure 12-32. CPGMAC to CPGMAC (with auto-negotiation) Block Diagram

The following sequence shows the master CPSGMII setup for this mode of operation:

1. Setup the CPSGMII and enable auto-negotiation:
 - [SGMII_MR_ADV_ABILITY_REG\[15-0\]](#) MR_ADV_ABILITY = 9801h (Advertise full duplex only)
 - [SGMII_CONTROL_REG\[0\]](#) MR_AN_ENABLE = 21h (enable auto-negotiation and master mode)
2. Poll the [SGMII_STATUS_REG\[1\]](#) AN_ERROR bit to determine when auto-negotiation is complete.
3. Setup the CPGMAC as shown in the CPGMAC specification. The EXT_EN bit in the SGMII_MAC_CONTROL register can be set to 1h to allow the speed and duplexity to be set by the signals from the CPSGMII.

The following sequence shows the slave CPSGMII setup for this mode of operation:

1. Setup the CPSGMII and enable auto-negotiation:
 - [SGMII_MR_ADV_ABILITY_REG](#)[15-0] MR_ADV_ABILITY = 1h (MAC to PHY configuration register)
 - [SGMII_CONTROL_REG](#)[0] MR_AN_ENABLE = 1h (enable auto-negotiation and slave mode)
2. Poll the [SGMII_STATUS_REG](#)[1] AN_ERROR bit to determine when auto-negotiation is complete without error. The [1]AN_ERROR bit in the [SGMII_STATUS_REG](#) will be set to 1h if the mode was commanded to be half-duplex Gigabit.
3. Setup the CPGMAC as shown in the CPGMAC specification. The EXT_EN bit in the SGMII_MAC_CONTROL register can be set to 1h to allow the speed and duplexity to be set by the signals from the CPSGMII.

12.3.7 SGMII Mode - CPGMAC to CPGMAC (generic MAC) with forced link

Figure 12-33 below shows the direct SGMII CPGMAC to CPGMAC mode of operation.

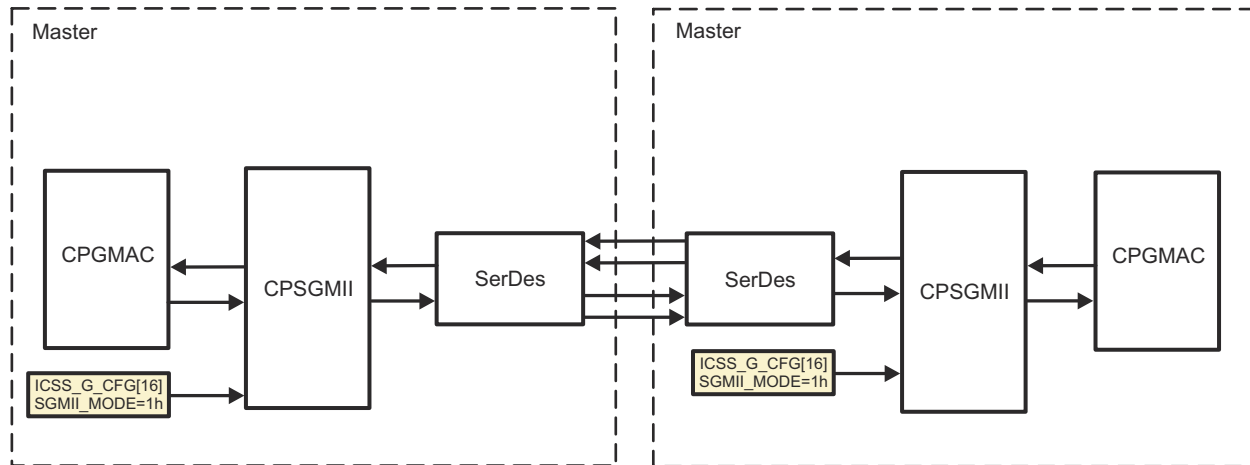


Figure 12-33. CPGMAC to CPGMAC (with forced link) Block Diagram

The following sequence shows the master CPSGMII setup for this mode of operation:

1. Setup the CPSGMII:
 - [SGMII_MR_ADV_ABILITY_REG](#)[15-0] MR_ADV_ABILITY = 9801h (Full duplex GIG (could be 9401h for 100Mbit))
 - [SGMII_CONTROL_REG](#)[0] MR_AN_ENABLE = 20h (master mode (no auto-negotiation enable))
2. Poll the [SGMII_STATUS_REG](#)[1] AN_ERROR bit to determine when link is asserted (the link is up).
3. Setup the CPGMAC as shown in the CPGMAC specification. The EXT_EN bit in the SGMII_MAC_CONTROL register can be set to 1h to allow the speed and duplexity to be set by the signals from the CPSGMII.

12.4 PRU_ICSSG PA_STATS Module

The statistics engine module (PA_STATS) is used to accelerate the task of incrementing and collecting statistics of traffic inside Packet Accelerator subsystem.

Figure 12-34 shows an overview of the PA_STATS module.

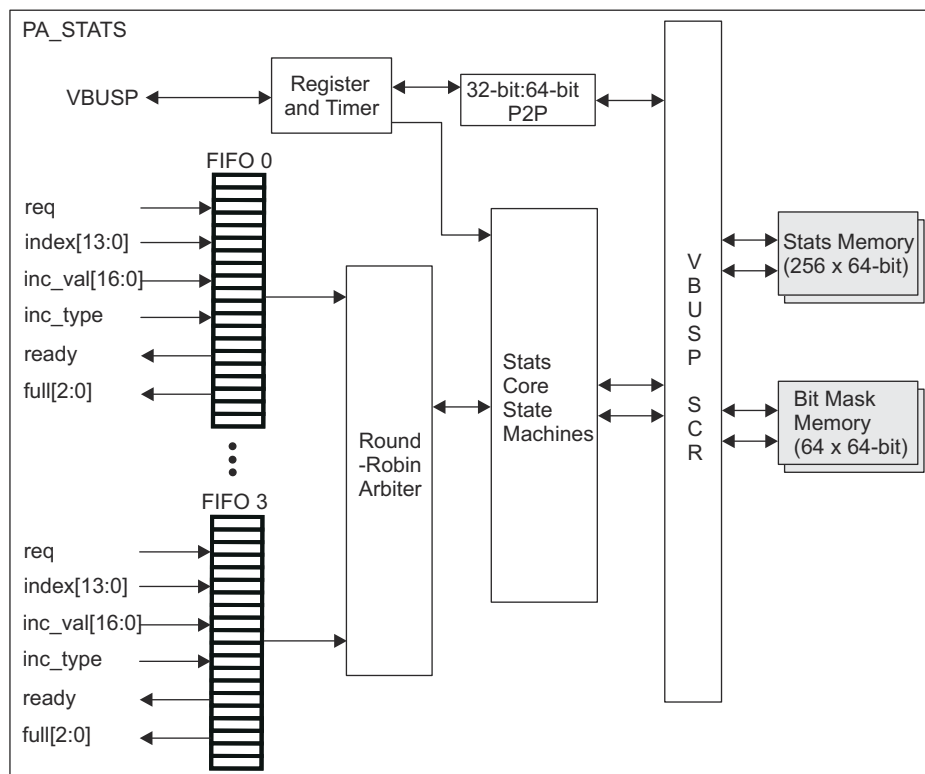


Figure 12-34. PRU_ICSSG PA_STATS Module Overview

The statistics engine has 4 PRU statistics ports, which allow 4 PRU cores or other modules to write statistics commands to the engine simultaneously. In order to allow the engine to accept multiple commands, each port has a 8 entry command FIFO, allowing for up to 8 statistics commands to be written per port before a command could be dropped due to lack of storage. Each PRU in the PA (Packet Accelerator) flow exports byte strobes for both R0 and R31 registers to the statistics engine, however, only a write to R31 register will trigger statistics operation. That trigger is the assertion of request for 1 cycle and at the same clock request is asserted index, inc_val and inc_type must be valid.

The below [Table 12-23](#) shows statistic input ports.

Table 12-23. Statistic Input Ports

Statistic Input Ports			
Bit Field	PRU Registers	Bits	Definition
req	R31[15]	1	Asserted for 1 cycle for each stat increment.
inc_type	R31[14]	1	0h: indicates that the statistic should increment by 1. 1h: indicates that the statistic should increment by the 'inc_val' field.
index	R31[13:0]	14	Indicates which statistic in the memory will be incremented. Acceptable input range for this implementation is 1 ... FFFh.
inc_val	R0[16:0]	17	Indicates the increment value if inc_type is 1. If inc_type is 0 this field is ignored.

The statistics engine outputs three status bits per statistics port, as shown in [Table 12-24](#)

Table 12-24. Statistics Port Status

Statistic Input Ports			
Bit Field	PRU Registers	Bits	Definition
2	R31[2]	1	Set when at least 8 entries in the statistics port FIFO are free.
1	R31[1]	1	Set when at least 4 entries in the statistics port FIFO are free.
0	R31[0]	1	Set when at least 1 entry in the statistics port FIFO is free.

The 'ready' output port is provided for future compatibility.

12.4.1 Statistics Page

The statistics counters are implemented in 2KB memory which can hold a maximum of 512 32-bit counters. These counters can be made into 64-bit counters by specifying the number of 64-bit counters in the Counter Allocation Register (address offset 8h). The default register configuration is 256 64-bit counters and 512 32-bit counters. The 64-bit counters are all placed before the 32-bit counters. The index for 64-bit counters is always an even number and starts from 0. For example if Counter Allocation Register (address offset 8h) is configured to be 5, then statistics at index 0, 2, 4, 6 and 8 are 64-bit stats; index 10,11,12,13,...,511 are all 32-bit stats. All counters are cleared to "0" upon hardware reset or software reset ([31-0] TRIGGER).

To allow both sending of statistics packet to the host and stats update happen simultaneously, the module has a second statistics page and the engine can ping-pong between them. The 'Active' label in Figure 12-35 indicates which page is currently processing new stat bumps. The ping-pong approach allows the engine to get snapshot of the active page and send them based on certain events (timer expiration, an input packet with 'send update' command), while the other page resumes processing of new increments. In Figure 12-35 page A is initially the active page, and page B is the page that will become the active page when the engine goes into output phase.

After the output phase, there is a 'merging' between the two pages to ensure the new active page reflects the latest stats count and the bit masks. This process occurs as a background task and runs at slow interval (every 8 cycles) to minimize bandwidth impact. After the merging process is complete, the state machine resets the applied bit mask to all 1s and reset the counters in the non-active page to all 0s (reset phase). The engine then goes back to a steady state in which new bumps are handled in the active page and the stats in the non-active page are all zero.

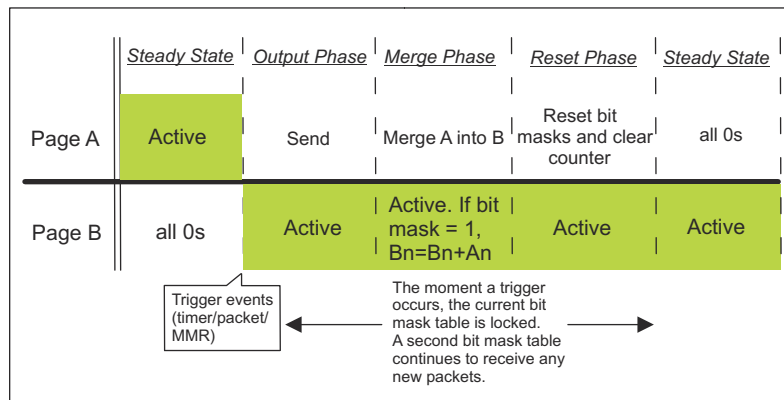


Figure 12-35. Merging between Two Pages

12.4.2 Statistics Collection Modes

There are two ways to collect the statistics: packet based and manual read to the register space. The most efficient and effective way of the getting the stats are by using packet. The advantage is that software has a global pointer that is always pointed to the 'stats page'. When software receives a new packet with the latest stats, software keeps these stats where the CPPI DMA places them and change the global pointer to point to the new 'stats page'. This way software benefits from having "free" stats delivery, and although the stats engine only sends to one host, the host can easily forward the statistics packet to other cores in multi-cores system.

12.4.2.1 Manual Read Mode

Host can issue read on specific counter and the read data comes from the active page. This is especially useful for debug purpose, or when the timer is disabled and the host manually reads the stats. The bit mask table has no effect on the counter on manual read. There are two register addresses for every statistics counter. One address is used for query mode (read and not clear), and another is used for collect mode (read and clear). Note that issuing two 32-bit reads through the 32-bit configuration bus for reading a 64-bit stat can be unreliable, because there may be latency between the two reads and a stat bump can occur in between. This may be unavoidable for Arm cores, but for cores that can issue burst read, such as DSPs, the statistics engine will ensure that reads on 64-bit counter value is treated as atomic operation. However, the module does not support read burst on multiple counters using collect (read and clear) mode.

When reading a 64-bit counter in collect mode through the 32-bit configuration bus, each 32-bit portion of the counter is cleared immediately after the read.

12.4.3 Clock Stop

To initiate clock stop procedure, CLKSTOP_REQ input needs to be asserted and stays asserted until the statistics engine acknowledges the clock stop request, which indicates that it is safe to turn off the clock (CLKSTOP_ACK output is 1). After CLKSTOP_REQ is asserted, no additional packet or configuration access should be sent to the stats engine. Stats engine will ensure that all pending stats bumps requests have been processed (all FIFOs are empty), before issuing CLKSTOP_ACK. In addition, to prevent timer interrupt, the timer is paused when CLKSTOP_REQ = 1.

13 PRU_ICSSG MII MDIO Module

This section describes the PRU_ICSSGn (where n = 0 or 1) integrated MII management interface (MII_MDIO module).

13.1 PRU_ICSSG MII MDIO Overview

The following features are supported:

- Clause 22 and Clause 45.
- Up to 32 PHY addresses.
- Two user access registers to control and monitor up to two PHYs simultaneously.
- Target interface for configuration and control (MII RT MDIO CFG)
- Each PHY can be individually enabled to be polled.
- The inter-poll gap between PHY polls can be changed.
- State Change Mode of operation to monitor up to 32 PHYs simultaneously.
- Manual control by software for GPIO operations.

The PRU_ICSSG MII MDIO management I/F module implements the *802.3 serial management interface* to interrogate and control two Ethernet PHYs simultaneously using a shared two-wire bus. [Figure 13-1](#) shows a device with two MACs, each connected to an Ethernet PHY, being managed by the MII interface module using a shared bus.

The [Figure 13-1](#) gives an overview of the MII MDIO management interface.

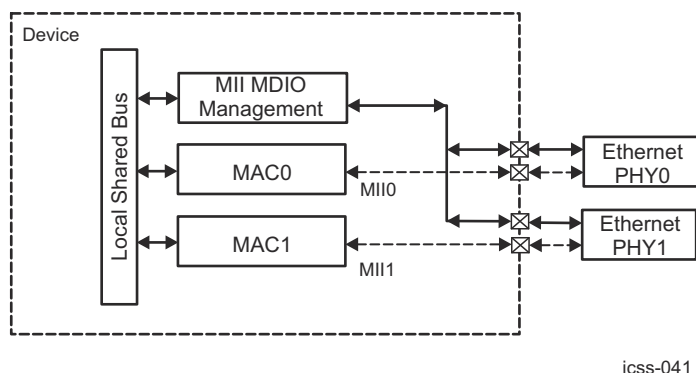


Figure 13-1. Device PRU_ICSSG MII MDIO Management Interface Overview

13.2 PRU_ICSSG MII MDIO Functional Description

The MII Management interface incorporates:

- *MDIO Registers* - The MDIO register block provides a VBUSP 3.0 compliant target interface to the MDIO module. Host interaction with this module is facilitated through the registers in this block.
- *Control and Schedule* - The control and register logic in the MDIO module contain the state machine and scheduling logic which control the wire side operation.
- *MDIO Interface* - The MDIO interface block provides the serial interface to the MDIO interface.

The MDIO logic is fully synchronous to the PRU_ICSSG local shared bus clock.

13.2.1 MDIO Clause 22 Frame Formats

The below [Table 13-1](#) shows the read and write format of the Clause 22 Management interface frames.

Table 13-1. MDIO Clause 22 Frame Formats

Preamble	Start Delimiter	Operation Code	PHY Address	Register Address	Turnaround	Data
MDIO Clause 22 Read Frame Format						
FFFFFFFFh	01	10	AAAAA	RRRRR	Z0	DDDD.DDDD.DDD D.DDDD
MDIO Clause 22 Write Frame Format						

Table 13-1. MDIO Clause 22 Frame Formats (continued)

Preamble	Start Delimiter	Operation Code	PHY Address	Register Address	Turnaround	Data
FFFFFFFFh	01	01	AAAAA	RRRRR	10	DDDD.DDDD.DDD D.DDDD

The default or idle state of the two wire serial interface is a logic one. All tri-state drivers should be disabled and the PHY's pull-up resistor will pull the MDIO line to a logic one. Prior to initiating any other transaction, the station management entity shall send a preamble sequence of 32 contiguous logic one bits on the MDIO line with 32 corresponding cycles on MDCLK to provide the PHY with a pattern that it can use to establish synchronization. A PHY shall observe a sequence of 32 contiguous logic one bits on MDIO with 32 corresponding MDCLK cycles before it responds to any other transaction.

Preamble

The start of a frame is indicated by a preamble, which consists of a sequence of 32 contiguous bits all of which are a "1". This sequence provides the Ethernet PHY a pattern to use to establish synchronization.

Start Delimiter

The preamble is followed by the start delimiter which is indicated by a "01" pattern. The pattern assures transitions from the default logic one state to zero and back to one.

Operation Code

The operation code for a read is "10", while the operation code for a write is a "01".

Ethernet PHY Address

The PHY address is 5 bits allowing 32 unique values. The first bit transmitted is the MSB of the PHY address.

Register Address

The Register address is 5 bits allowing 32 registers to be addressed within each PHY.

Turnaround

An idle bit time during which no device actively drives the MDIO signal shall be inserted between the *Register Address* field and the *Data* field of a read frame in order to avoid contention. During a read frame, the PHY shall drive a zero bit onto MDIO for the first bit time following the idle bit and preceding the Data field. During a write frame, this field shall consist of a one bit followed by a zero bit.

Data

The Data field is 16 bits. The first bit transmitted and received is the MSB of the data word.

13.2.1.1 PRU-ICSSG MDIO Control and Interface Signals

The [Table 13-2](#) shows the PRU_ICSSGn (where n = 0 to 2) MII MDIO signals and their availability at the device boundary.

Table 13-2. PRU_ICSSG MII MDIO Control and Interface Signals

MDIO Control Signals			
Pin Name	Type	Available as device I/O	Function
MDIO_LINKINT[1:0]	O	N.A.	Serial interface link change interrupt. Indicates a change in the state of the PHY link.
MDIO_USERINT[1:0]	O	N.A.	Serial interface user command event complete interrupt.
MDIO Interface Signals			
Pin Name	Type	Available as device I/O	Function
MDIO_I	I	device bidirectional pr0_mdio_data , and pr1_mdio_mdclk pin in input mode	Serial data input
MDIO_O	O	device bidirectional pr0_mdio_data and pr1_mdio_mdclk pin in output mode	Serial data output
MDIO_OE_N	O	N.A.	Serial data output enable. Asserted "0" when data output is valid

Table 13-2. PRU_ICSSG MII MDIO Control and Interface Signals (continued)

MDIO Control Signals			
MDCLK_O	O	device output - pr0_mdio_mdclk pr1_mdio_mdclk	Serial clock output
MLINK_I[1:0]	I	N.A.	Optional link status inputs from PHY. Each input is connected to a single PHY. Unused inputs are tied '0'.

13.2.2 MDIO Clause 45 Frame Formats

The below [Table 13-3](#) shows the address frame format. [Table 13-4](#) shows read, and write format of the supported Clause 45 frames. Post-increment accesses are not supported.

Table 13-3. MDIO Clause 45 Address Frame Formats

Pre-amble	Start Delimiter	Operation Code	PHY Address	MMD Number	Turnaround	Address
MDIO Clause 45 Address Frame Format						
FFFFFFFFh	00	00	AAAAA	RRRRR	10	AAAA.AAAA.AAA A.AAAA

Table 13-4. MDIO Clause 45 Frame Formats

Pre-amble	Start Delimiter	Operation Code	PHY Address	MMD Number	Turnaround	Data
MDIO Clause 45 Read Frame Format						
FFFFFFFFh	00	11	AAAAA	RRRRR	Z0	DDDD.DDDD.DD DD.DDDD
MDIO Clause 45 Write Frame Format						
FFFFFFFFh	00	01	AAAAA	RRRRR	10	DDDD.DDDD.DD DD.DDDD

The default or idle state of the two wire serial interface is a logic one. All tri-state drivers should be disabled and the PHY's pull-up resistor should pull the MDIO line to a logic one. Prior to initiating any other transaction, the station management entity shall send a preamble sequence of 32 contiguous logic one bits on the MDIO line with 32 corresponding cycles on MDCLK to provide the PHY with a pattern that it can use to establish synchronization. A PHY shall observe a sequence of 32 contiguous logic one bits on MDIO with 32 corresponding MDCLK cycles before it responds to any other transaction. The [MDIO_USER_ADDR0_REG](#)/[MDIO_USER_ADDR1_REG](#) registers must be written before a read or write operation is performed to set the address used in the operation. Each read or write operation has a preceeding address frame.

Preamble

The start of a frame is indicated by a preamble, which consists of a sequence of 32 contiguous bits all of which are a "1". This sequence provides the PHY a pattern to use to establish synchronization. The preamble is required in clause 45 operation.

Start Delimiter

The preamble is followed by the start delimiter which is indicated by a "00" pattern.

Operation Code

The operation code for address is "00". The operation code for a read is "11", while the operation code for a write is a "01".

Ethernet PHY Address

The PHY address is 5 bits allowing 32 unique values. The first bit transmitted is the MSB of the PHY address.

MMD Number

The MMD number is 5 bits allowing 32 unique values. The first bit transmitted is the MSB.

Turnaround

An idle bit time during which no device actively drives the MDIO signal shall be inserted between the **MMD Number** field and the **Data** field of a read frame in order to avoid contention. During a read frame, the PHY shall

drive a zero bit onto MDIO for the first bit time following the idle bit and preceding the Data field. During a write frame, this field shall consist of a one bit followed by a zero bit.

Address

The address field is 16-bits on address operations. The first bit transmitted is the MSB of the address word. Each read/write operation initiated has an automatic address operation initiated first that uses the [MDIO_USER_ADDR0_REG\[15-0\]](#) USER_ADDR0 or [MDIO_USER_ADDR1_REG\[15-0\]](#) USER_ADDR1 register values as the 16-bit address.

Data

The Data field is 16 bits on read and write operations. The first bit transmitted and received is the MSB of the data word.

13.2.3 PRU_ICSSG MII MDIO Interactions

The MDIO module will remain idle until enabled by setting the [30] ENABLE bit in the MDIO [MDIO_CONTROL_REG](#) register. The MDIO will then continuously poll the link status from within the Generic Status Register of all possible 32 PHY addresses in turn recording the results in the MDIO [MDIO_LINK_REG](#) register. Individual PHY's can be enabled or disabled for polling through the associated bit in the MDIO [MDIO_POLL_EN_REG](#) register. The MDIO [MDIO_LINK_REG](#) and [MDIO_ALIVE_REG](#) register bit values are updated on the poll of each PHY. In *Normal Mode*, the link status of two of the 32 possible PHY addresses can also be determined using the MLINK pin inputs. The bit [7] LINKSEL in the MDIO [MDIO_USER_PHY_SEL_REG_0/1](#) register determines the status input that is used. A change in the link status of the two PHYs being monitored will set the appropriate bit ([1-0] LINKINTRAW) in the MDIO [MDIO_LINK_INT_RAW_REG](#) register and the [MDIO_LINK_INT_MASKED_REG\[1-0\]](#) LINKINTMASKED register, if enabled by the [6] LINKINT_ENABLE bit in the MDIO [MDIO_USER_PHY_SEL_REG_0/1](#) register. In *State Change Mode*, a change in any PHY status will be indicated on the [MDIO_LINK_INT_RAW_REG\[0\]](#) LINKINTRAW interrupt if enabled.

The MDIO [MDIO_ALIVE_REG](#) register is updated by the MDIO module if the PHY acknowledged the read of the generic status register. In addition, any PHY register read transactions initiated by the host also cause the MDIO [MDIO_ALIVE_REG](#) register to be updated.

At any time, the host can define a transaction for the MDIO module to undertake using the [15-0] DATA, [20-16] PHYADR, [25-21] REGADR, and [30] WRITE fields in a [MDIO_USER_ACCESS_REG_0/1](#) register. When the host sets the [31] GO bit in this register, the MDIO interface module will begin the transaction without any further intervention from the host. Upon completion, the MDIO will clear the [31] GO bit and set the [1-0] USERINTRAW bit field in the [MDIO_USER_INT_RAW_REG](#) register corresponding to the [MDIO_USER_ACCESS_REG_0/1](#) register being used. The corresponding bit in the [MDIO_USER_INT_MASKED_REG](#) register may also be set depending on the mask setting in the [MDIO_USER_INT_MASK_SET_REG](#) and [MDIO_USER_INT_MASK_CLEAR_REG](#) registers. A round-robin arbitration scheme is used to schedule transactions which may be queued by the host in different [MDIO_USER_ACCESS_REG_0/1](#) registers. The host should check the status of the [31] GO bit in the [MDIO_USER_ACCESS_REG_0/1](#) register before initiating a new transaction to ensure that the previous transaction has completed. The host can use the [29] ACK bit in the [MDIO_USER_ACCESS_REG_0/1](#) register to determine the status of a read transaction.

Software may use the MDIO module to set up the auto-negotiation parameters of each PHY attached to a MAC port, retrieve the negotiation results, and set up the MAC Control register in the corresponding MAC.

13.2.4 PRU_ICSSG MII MDIO Interrupts

13.2.4.1 Normal Mode ([30]STATECHANGEMODE = 0h)

The MDIO will assert the MDIO_LINKINT signals if there is a change in the link state of the Ethernet PHY corresponding to the address in the [4-0] PHYADR_MON field of the MDIO [MDIO_USER_PHY_SEL_REG_j](#) (where j = 0 or 1) registers and the corresponding [6] LINKINT_ENABLE bit is set. The MDIO_LINKINT event is also captured in the MDIO [MDIO_LINK_INT_MASKED_REG](#) register. MDIO_LINKINT[0] and MDIO_LINKINT[1] correspond to the MDIO [MDIO_USER_PHY_SEL_REG_0](#) and [MDIO_USER_PHY_SEL_REG_1](#) registers, respectively.

When the [31] GO bit in the [MDIO_USER_ACCESS_REG_j](#) (where j = 0 or 1) registers transitions from '1' to '0', indicating the completion of a user access, and the corresponding [1-0] USERINTMASKSET field in the [MDIO_USER_INT_MASK_SET_REG](#) register is set, the MDIO_USERINT signal is asserted '1'. The MDIO_USERINT event is also captured in the [MDIO_USER_INT_MASKED_REG](#) register. MDIO_USERINT[0] and MDIO_USERINT[1] correspond to the MDIO_USER_ACCESS_REG_0 and MDIO_USER_ACCESS_REG_1 registers, respectively.

13.2.4.2 State Change Mode ([30]STATECHANGEMODE = 1h)

In *State Change Mode*, the MDIO will assert MDIO_LINKINT[0] when any bit in the MDIO [MDIO_ALIVE_REG](#) or MDIO [MDIO_LINK_REG](#) registers changes due to MDIO operations. The MDIO_LINKINT event is also captured in the MDIO [MDIO_LINK_INT_MASKED_REG](#) register. MDIO_LINKINT[1] output and the MDIO [MDIO_USER_PHY_SEL_REG_j](#) (where j = 0 or 1) registers are unused in *State Change Mode*.

13.2.5 Manual Mode

Manual Mode allows software to directly control the serial clock output (MDCLK_O), the serial data output enable (MDIO_OE_N), and the serial data output (MDIO_O). The serial data input can also be read (MDIO_I). This mode is enabled when the [31] MANUALMODE bit is set in the MDIO [MDIO_POLL_REG](#) register. *Manual Mode* is intended to be used by software for slow speed general purpose IO operations and not for MDIO PHY operations.

13.3 PRU_ICSSG MII MDIO Receive/Transmit Frame Host Software Interface

To facilitate transmission and reception of serial management frames, the host has to perform the following operations:

- Configure the [20] PREAMBLE and [15-0] CLKDIV fields in the MDIO [MDIO_CONTROL_REG](#) register.
- Enable the MDIO module by setting the [30] ENABLE bit in the MDIO [MDIO_CONTROL_REG](#) register. If Byte access is being used, the [30] ENABLE bit should be written last.
- The MDIO [MDIO_ALIVE_REG](#) register can be read after a delay to determine which Ethernet PHYs responded.
- Set up the appropriate PHY addresses in the MDIO [MDIO_USER_PHY_SEL_REG_j](#)[4-0] PHYADR_MON bits.
- Set up the appropriate [6] LINKINT_ENABLE bit in the MDIO [MDIO_USER_PHY_SEL_REG_j](#) registers.
- Set up the appropriate [7] LINKSEL bits in the MDIO [MDIO_USER_PHY_SEL_REG_j](#) registers.
- Set up the appropriate [1-0] USERINTMASKEDSET field in the MDIO [MDIO_USER_INT_MASK_SET_REG](#) register.
- To write to an Ethernet PHY register the host should first check to ensure that the [31] GO bit in a MDIO [MDIO_USER_ACCESS_REG_j](#) registers is cleared. The [31] GO, [30] WRITE, [25-21] REGADR, [20-16] PHYADR and data fields in that MDIO [MDIO_USER_ACCESS_REG_j](#) registers can then be updated to the appropriate value. If byte access is being used, the [31] GO bit should be written last. The write operation to the PHY will be scheduled and completed by the module. Completion of the write operation can be determined by examining the [31] GO bit in the MDIO [MDIO_USER_ACCESS_REG_j](#) registers. It also results in a transition on the appropriate MDIO_INT signal and the corresponding bit in the MDIO [MDIO_USER_INT_MASKED_REG](#) register based on the setting of the MDIO [MDIO_USER_INT_MASK_SET_REG](#) register.
- To read from an Ethernet PHY register the host should first check to ensure that the [31] GO bit in a MDIO [MDIO_USER_ACCESS_REG_j](#) registers is cleared. The [31] GO, [25-21] REGADR, and [20-16] PHYADR fields in that MDIO [MDIO_USER_ACCESS_REG_j](#) registers can then be updated to the appropriate value. The read data value will be available in the [15-0] DATA field of the MDIO [MDIO_USER_ACCESS_REG_j](#) registers after the module completes the read operation on the serial bus. The completion of the read operation can be determined by examining the [31] GO and [29] ACK bits in the MDIO [MDIO_USER_ACCESS_REG_j](#) registers. It also results in a transition on the appropriate MDIO_INT signal and the corresponding bit in the MDIO [MDIO_USER_INT_MASKED_REG](#) register based on the setting of the MDIO [MDIO_USER_INT_MASK_SET_REG](#) register.
- The module de-asserts the MDIO_USERINT signal when the host writes to the appropriate [1-0] USERINTMASKED bit field in the MDIO [MDIO_USER_INT_MASKED_REG](#) register or the [1-0] USERINTRAW bit field in the MDIO [MDIO_USER_INT_RAW_REG](#) register.

- The host can poll the MDIO [MDIO_LINK_REG](#) register periodically or use the MDIO_LINKINT signals to determine the state of the serial interface to a particular Ethernet PHY.
- The module de-asserts the MDIO_LINKINT when the host writes to the appropriate [1-0] LINKINTRAW bit field in the MDIO_MDIO LINK_INT_RAW_REG register or the [1-0] LINKINTMASKED bit field in the MDIO_MDIO LINK_INT_MASKED_REG register.

Table 13-5. Summary of the PRU_ICSSG MII MDIO Functional Registers

Address Offset	Register Mnemonic	Register Name	Register Purpose
00h	MDIOVer	MDIO_MDIO_VERSION_REG	Module version register
04h	MDIOControl	MDIO_CONTROL_REG	Module control register
08h	MDIOAlive	MDIO_ALIVE_REG	Ethernet PHY acknowledge status register
0Ch	MDIOLink	MDIO_LINK_REG	Ethernet PHY link status register
10h	MDIOLinkIntRaw	MDIO_LINK_INT_RAW_REG	Link status change interrupt register (raw value)
14h	MDIOLinkIntMasked	MDIO_LINK_INT_MASKED_REG	Link status change interrupt register (masked value)
18h	MDIOLinkIntMaskSet	MDIO_LINK_INT_MASK_SET_REG	Link status change interrupt mask set register
1Ch	MDIOLinkIntMaskClr	MDIO_LINK_INT_MASK_CLEAR_REG	Link status change interrupt mask clear register
20h	MDIOUserIntRaw	MDIO_USER_INT_RAW_REG	User command complete interrupt register (raw value)
24h	MDIOUserIntMasked	MDIO_USER_INT_MASKED_REG	User command complete interrupt register (masked value)
28h	MDIOUserIntMaskSet	MDIO_USER_INT_MASK_SET_REG	User interrupt mask set register
2Ch	MDIOUserIntMaskClr	MDIO_USER_INT_MASK_CLEAR_REG	User interrupt mask clear register
30h	MDIOManual_IF	MDIO_MANUAL_IF_REG	Manual interface register
34h	MDIOPoll_IPG	MDIO_POLL_REG	Poll and IPG register
38h	MDIOPoll_En	MDIO_POLL_EN_REG	Poll Enable register
3Ch	MDIOClause	MDIO_CLAUS45_REG	Clause 22 or 45 enable register
40h	MDIOUser_Addr0	MDIO_USER_ADDR0_REG	User Address register 0
44h	MDIOUser_Addr1	MDIO_USER_ADDR1_REG	User Address register 1
48h – 7Ch	Reserved	-	Reserved
80h	MDIOUserAccess0	MDIO_USER_ACCESS_REG_0	User access register 0
84h	MDIOUserPhySel0	MDIO_USER_PHY_SEL_REG_0	User PHY select register 0
88h	MDIOUserAccess1	MDIO_USER_ACCESS_REG_1	User access register 1
8Ch	MDIOUserPhySel1	MDIO_USER_PHY_SEL_REG_1	User PHY select register 1
90h – FFh	Reserved	-	Reserved

CAUTION

When software enables the clock (at PRU_ICSSG level) to the IEP module clock input via setting bit [ICSSG_IEPCLK_REG\[0\] IEP_OCP_CLK_EN](#) to 1h in the PRUSS_CFG space, there must be NO in-flight transactions to the IEP block.

CAUTION

Switching from ICSSGn_IEP_CLK (the IEP specific functional clock source) to the ICSSGn_CORE_CLK source is supported ONLY in software. Switching back from ICSSGn_CORE_CLK to ICSSGn_IEP_CLK is ONLY supported via assertion of a hardware reset to the PRU_ICSSG.

14.2.2 PRU_ICSSG IEP Timer

The IEP timer is a simple 64-bit timer. This timer is intended for use by industrial ethernet functions but can also be leveraged as a generic timer in other applications.

14.2.2.1 PRU_ICSSG IEP Timer Features

The IEP timer supports the following features:

- One controller 64-bit count-up counter with an overflow status bit.
 - Runs on ICSSG_IEP_CLK or ICSSG_ICLK clock.
 - Write 1h to clear status.
 - Supports a programmable increment value from 1 to 16 (default 5).
 - An optional compensation method allows the increment value to apply compensation increment value from 1 to 16 count up to 2²⁴ ICSSG_IEP_CLK events with additional slow compensation mode.
- 10× 64-bit capture registers:
 - 8 capture inputs, with optional synchronous or asynchronous mode:
 - 6× rise capture registers: [ICSSG_IEP_CAPRi_REG0/ IEP_CAPRi_REG1](#) (where i=0 to 5)
 - 2× rise and fall capture registers: [IEP_CAPR6_REG0/ IEP_CAPR6_REG1](#) and [IEP_CAPR7_REG0/ IEP_CAPR7_REG1](#), each combined with a fall capture - [IEP_CAPF6_REG0/ IEP_CAPF6_REG1](#) and [IEP_CAPF7_REG0/ IEP_CAPF7_REG1](#), respectively
 - One global event (any capture event) output for interrupt
- 16× 64-bit compare registers: [IEP_CMPj_REG0/ IEP_CMPj_REG1](#) (where j = 0 to 15) and [IEP_CMP_STATUS_REG\[15-0\] CMP_STATUS](#)
 - 16 status bits, write 1h to clear
 - 16 individual event outputs
 - One global event output for interrupt generation triggered by any compare event
- 32 outputs, one high-level and one high-pulse for each compare hit event
- [IEP_CMP_CFG_REG\[0\] CMP0_RST_CNT_EN](#), if enabled, will reset the controller counter on the next ICSSG_IEP_CLK/ ICSSG_ICLK cycle
- [EHRPWM0_SYNCO/ EHRPWM3_SYNCO](#), if enabled, will reset the controller counter on the next ICSSG_IEP_CLK/ ICSSG_ICLK cycle
- Controller counter reset-state is programmable
- Optional 32-bit shadow mode of operation, which can be configured through [IEP_CMP_CFG_REG\[17\] SHADOW_EN](#) bit

14.2.3 32-Bit Shadow Mode

The IEP module can be configured in 32-bit shadow mode when [IEP_CMP_CFG_REG\[17\] SHADOW_EN](#) bit is set to 1h (default value is 0h, e.g. 64-bit mode of operation is enabled). In this mode, the controller counter will be in 32-bit mode of operation. This enables the shadow copy functionality of the compare registers.

Rules of operation:

1. Switching the state of the controller counter from 32-bit Shadow mode to 64-bit mode of operation, the counter should be disabled and bit [IEP_CMP_CFG_REG\[17\] SHADOW_EN](#) should be cleared to 0h (default value).

2. A new compare update ([IEP_CMP_CFG_REG\[16-1\] CMP_EN = 1h](#) - enables CMP[0:15] event, where [0]CMP_EN maps to CMP0) should be set 4 cycle counts before the next rollover or reset of the counter and to insure the correct shadow copy to active update is correct.

Sequence of operation:

1. Disable counter through [IEP_GLOBAL_CFG_REG\[0\] CNT_ENABLE = 0h](#) (default value).
2. Clear controller counter through [IEP_CMP_CFG_REG\[17\] SHADOW_EN = 0h](#) (64-bit mode of operation)
3. Enable 32-bit Shadow mode through [IEP_CMP_CFG_REG\[17\] SHADOW_EN](#) bit (value: 1h)
4. Program IEP_CMPm_REGn (where m = 0 to 15 and n = 0 to 1); use the upper 32-bits ([IEP_CMP0_REG1\[31-0\] CMP0_1](#)) of the 64-bit CMP
 - a. The lower 32-bits are the active compare value ([IEP_CMPm_REG0\[31-0\] CMPm_0](#), where m = 0 to 15), software can only read this bits
 - b. The upper 32-bits are the shadow copy ([IEP_CMPm_REG1\[31-0\] CMPm_1](#), where m = 0 to 15), software can write and read this bits
5. Enable counter through [IEP_GLOBAL_CFG_REG\[0\] CNT_ENABLE = 1h](#)

After the counter is enabled, then software can load a new set of CMP[0:15] without affecting the current active values of ([IEP_CMPm_REG0\[31-0\] CMPm_0](#), where m = 0 to 15). Only when the counter is reset to 32-bit Shadow mode ([IEP_CMP_CFG_REG\[17\] SHADOW_EN = 1h](#)), it will load the shadow copy of [IEP_CMPm_REG1\[31-0\] CMPm_1](#) into local copy.

Shadow compare value ([IEP_CMPm_REG1\[31-0\] CMPm_1](#)) is loaded into active register [IEP_CMPm_REG0\[31-0\] CMPm_0](#) when the controller counter is configured in 32-bit Shadow mode. If [IEP_CMP_CFG_REG\[0\] CMP0_RST_CNT_EN](#) bit is enabled (value 1h) to reset the counter, the next reset event will be defined by the last CMP0 update.

14.2.4 PRU_ICSSG IEP Timer Basic Programming Sequence

Follow these basic steps to configure the IEP Timer.

Counter maintains/function:

1. Once enabled, the counter will count every ICSSG_IEP_CLK cycle, default rate of 200 MHz.
2. It is a free running counter with a sticky over flag status bit.
3. The counter over flow flag ([IEP_GLOBAL_STATUS_REG\[0\] CNT_OVF](#)) will get set when the counter switches/rollover from 0xFFFF_FFFF to 0x0000_0000.
4. The counter will continue to count up. The software will need to read/clear the counter over flow flag and increment the MSB in software variable.

Compare function:

1. Initialize timer to known state (default values)
 - Disable counter ([IEP_GLOBAL_CFG_REG\[0\] CNT_ENABLE = 0](#))
 - Reset Count Register ([IEP_COUNT_REG0, IEP_COUNT_REG1](#)) by writing FFFFFFFFh to clear
 - Clear overflow status register ([IEP_GLOBAL_STATUS_REG\[0\] CNT_OVF = 1](#))
 - Clear compare status ([IEP_CMP_STATUS_REG\[15-0\] CMP_STATUS](#)) by writing FFFFFFFFh to clear
2. Set compare values [IEP_CMPj_REG0, IEP_CMPj_REG1](#) (where j = 0 to 15)
3. Enable compare events ([IEP_CMP_CFG_REG\[16-1\] CMP_EN = 1](#))
4. Set increment value ([IEP_GLOBAL_CFG_REG\[7-4\] DEFAULT_INC](#))
5. Set compensation value ([IEP_COMPEN_REG\[22-0\] COMPEN_CNT](#))
6. Enable counter ([IEP_GLOBAL_CFG_REG\[0\] CNT_ENABLE = 1](#))

Capture function:

1. Update/Enable the counter if required
2. Program the enable the desired capture event
3. Wait for global capture event
4. Read/Clear the capture status to determine which capture event occurred
5. Read the capture count

14.2.5 Industrial Ethernet Mapping

Some of the capture inputs and compare registers are mapped to specific industrial Ethernet functions in hardware, shown in [Table 14-1](#). All capture inputs are mapped to industrial Ethernet functions, and these inputs

are not available for any other application. The CMP1 and CMP2 compare registers also function as the start time triggers for SYNC0 and SYNC1, respectively.

Table 14-1. IEP Timer Mode Mapping

Capture Input	IEP Line/Function
IEP_CAPR0_REG0/ IEP_CAPR0_REG1, rise only	If EXT_CAP_EN[0] = 0h (Internal source is selected)/ PRU0_RX_SOF If EXT_CAP_EN[0] = 1h (External source is selected)/ ICSSG_n_IEP0_CAP_INTR_REQ0 ⁽¹⁾ ICSSG_n_IEP1_CAP_INTR_REQ0
IEP_CAPR1_REG0/ IEP_CAPR1_REG1, rise only	If EXT_CAP_EN[1] = 0h (Internal source is selected)/ PRU0_RX_SFD If EXT_CAP_EN[1] = 1h (External source is selected)/ ICSSG_n_IEP0_CAP_INTR_REQ1 ICSSG_n_IEP1_CAP_INTR_REQ1
IEP_CAPR2_REG0/ IEP_CAPR2_REG1, rise only	If EXT_CAP_EN[2] = 0h (Internal source is selected)/ PRU1_RX_SOF If EXT_CAP_EN[2] = 1h (External source is selected)/ ICSSG_n_IEP0_CAP_INTR_REQ2 ICSSG_n_IEP1_CAP_INTR_REQ2
IEP_CAPR3_REG0/ IEP_CAPR3_REG1, rise only	If EXT_CAP_EN[3] = 0h (Internal source is selected)/ PRU1_RX_SFD If EXT_CAP_EN[3] = 1h (External source is selected)/ ICSSG_n_IEP0_CAP_INTR_REQ3 ICSSG_n_IEP1_CAP_INTR_REQ3
IEP_CAPR4_REG0/ IEP_CAPR4_REG1, rise only	If EXT_CAP_EN[4] = 0h (Internal source is selected)/ PORT0_TX_SOF; For MII mode uses loopback for lower jitter 40ns versus 4ns. If EXT_CAP_EN[4] = 1h (External source is selected)/ ICSSG_n_IEP0_CAP_INTR_REQ4 ICSSG_n_IEP1_CAP_INTR_REQ4
IEP_CAPR5_REG0/ IEP_CAPR5_REG1, rise only	If EXT_CAP_EN[5] = 0h (Internal source is selected)/ PORT1_TX_SOF For MII mode uses loopback for lower jitter 40ns versus 4ns. If EXT_CAP_EN[5] = 1h (External source is selected)/ ICSSG_n_IEP0_CAP_INTR_REQ5 ICSSG_n_IEP1_CAP_INTR_REQ5
IEP_CAPR6_REG0/ IEP_CAPR6_REG1 - rise and IEP_CAPF6_REG0/ IEP_CAPF6_REG1 - fall	PRGn_IEP0_EDC_LATCH_IN0 (IO inputs at SoC level) PRGn_IEP1_EDC_LATCH_IN0
IEP_CAPR7_REG0/ IEP_CAPR7_REG1 - rise and IEP_CAPF7_REG0/ IEP_CAPF7_REG1 - fall	PRGn_IEP0_EDC_LATCH_IN1 (IO inputs at SoC level) PRGn_IEP1_EDC_LATCH_IN1
IEP_CMP1_REG0/ IEP_CMP1_REG1	For SYNC0 trigger of start time
IEP_CMP2_REG0/ IEP_CMP2_REG1	For SYNC1 trigger of start time; only valid in the SYNC2 independent mode
IEP_CMP3_REG0/ IEP_CMP3_REG1	For MII TX0 start trigger, if MII register MII_RT_TXCFG0/1[2] TX_EN_MODEn is enabled (where n = 0 or 1). Note: MII_CFG defines which IEP is the source (IEP0 or IEP1).
IEP_CMP4_REG0/ IEP_CMP4_REG1	For MII TX1 start trigger, if MII register MII_RT_TXCFG0/1[2] TX_EN_MODEn is enabled (where n = 0 or 1). Note: MII_CFG defines which IEP is the source (IEP0 or IEP1).

(1) n = 0 to 1

14.2.6 PRU_ICSSG IEP Sync0/Sync1 Module

The industrial ethernet sync block supports the generation of two synchronization signals: SYNC0 and SYNC1. SYNC0 and SYNC1 can be directly mapped to output signals (pr<k>_iep<n>_edc_sync_out0 and pr<k>_iep<n>_edc_sync_out1) for external devices to use. They can also be used for internal synchronization within the PRU_ICSSG. These signals are also mapped as system events and can therefore be mapped to the Arm core's Host interrupts.

14.2.6.1 PRU_ICSSG IEP Sync0/Sync1 Features

The industrial ethernet sync block supports the following features:

- Two synchronize generation signals (SYNC0, SYNC1)
 - Activation time synchronized with IEP Timer
- [IEP_CMP1_REG0/ IEP_CMP1_REG1](#) triggers SYNC0 activation time
- [IEP_CMP2_REG0/ IEP_CMP2_REG1](#) triggers SYNC1 activation time (only valid in the SYNC2 independent mode)
 - Pulse width defined by registers or acknowledge mode (remain asserted until software acknowledged)
 - Cyclic or single-shot operation
 - Option to enable or disable sync generation
- Programmable number of clock cycles between the start of SYNC0 to the start of SYNC1

14.2.6.2 PRU_ICSSG IEP Sync0/Sync1 Generation Modes

There are four modes of operation for the sync signals: cyclic mode, single shot mode, cyclic with acknowledge mode, and single shot with acknowledge mode. [Figure 14-2](#) shows examples of these modes. The start time is set by the [IEP_SYNC_START_REG\[31-0\]](#) SYNC_START bit field. The cycle time is configured by the [IEP_SYNC0_PERIOD_REG\[31-0\]](#) SYNC0_PERIOD bit field. The pulse length is defined by [IEP_SYNC_PWIDTH_REG\[31-0\]](#) SYNC_HPW bit field.

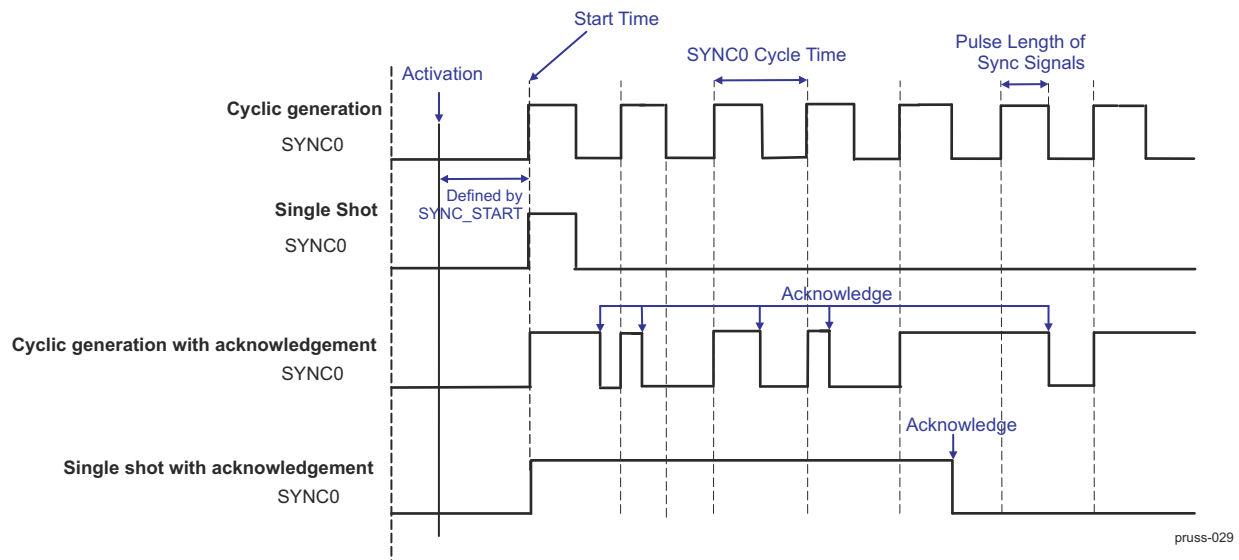
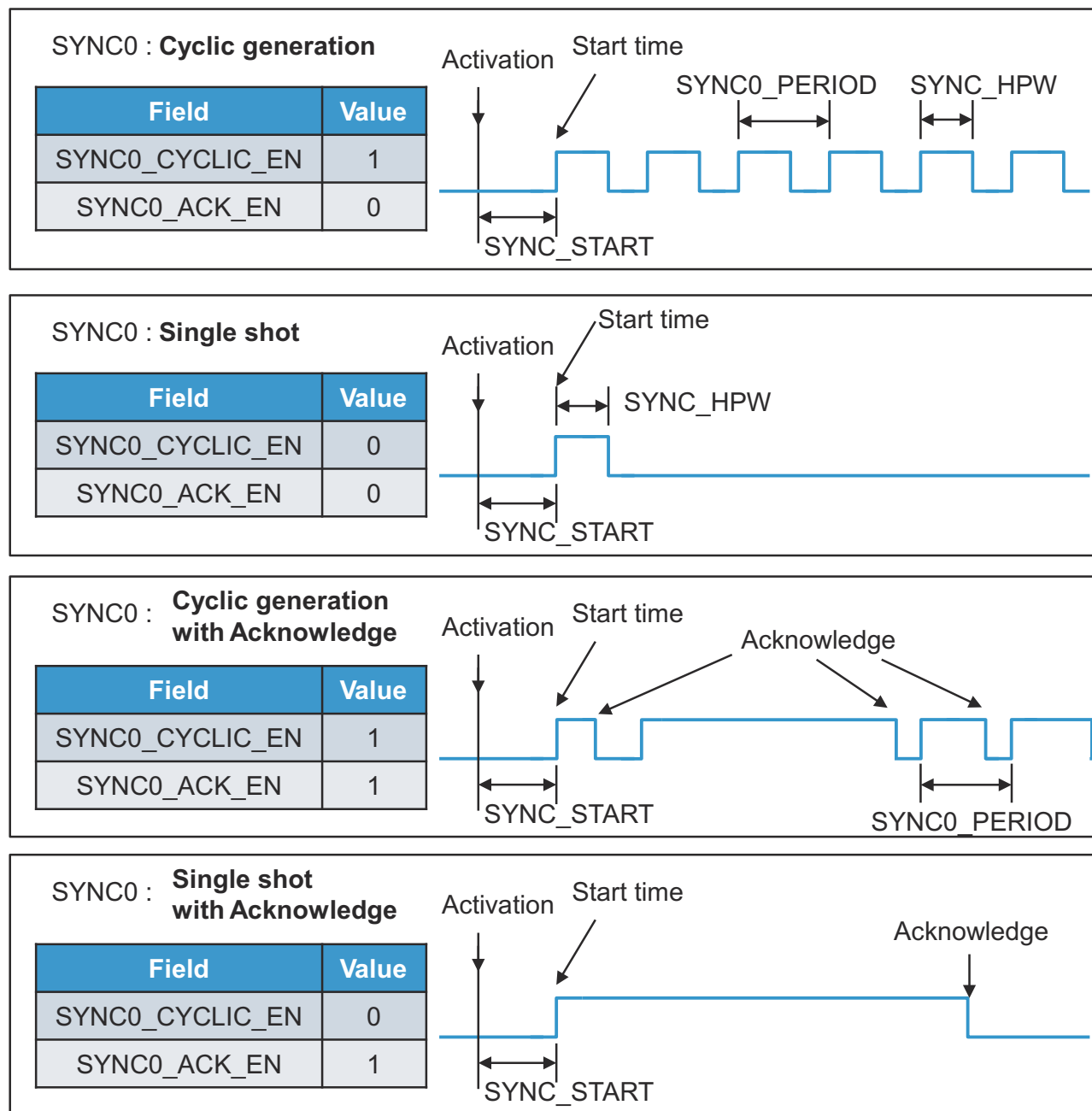


Figure 14-2. PRU_ICSSG IEP SYNC0 Signal Generation Modes

In SYNC1 dependent mode ([IEP_SYNC_CTRL_REG\[8\]](#) SYNC1_IND_EN = 0h), SYNC1 depends on SYNC0 and the start time of the SYNC1 can be defined by the [IEP_SYNC1_DELAY_REG](#) register. [Figure 14-3](#) shows different examples when changing the value in the [IEP_SYNC1_DELAY_REG](#) register. Note: If the SYNC1 delay time is 0, SYNC1 reflects SYNC0. Cyclic generation cannot be used for network time synchronized applications because only the CMP1/CMP2 hit occurs in the compensated time domain.



pruss-031

Figure 14-3. Examples of the Dependent Mode of SYNC1

14.2.7 PRU_ICSSG IEP WatchDog

In industrial ethernet applications, the watchdog timer (WD) is used to monitor process data communication and to turn off the outputs of the digital input/output (DIGIO) functional block after a set time. The WD will thereby protect the system from errors or faults by timeout or expiration. The expiration is used to initiate corrective action in order to keep the system in a safe state and restore normal operation based on configuration. Therefore, if the system is stable, the watchdog timer should be regularly reset or cleared to avoid timeout or expiration.

The IEP watchdog timer supports the following features:

- One 16-bit pre-divider for generating a WD clock (default 100μs) based on ICSSGn_IEP_CLK input
- Two 16-bit Watchdog Timers:
 - PDI_WD for Sync Managers WD, used in conjunction with digital input/output (DIGIO)

- PD_WD for data link layer user WD, used in conjunction with data link layer or application layer interface actions

Note

For more details on the PRU_ICSSG Industrial Ethernet Watchdog timer, refer also to the Watchdog timer register descriptions covered in the [Section 15.9, PRU_ICSSG IEP0 Registers](#) and [PRU_ICSSG IEP1 Registers](#).

14.2.8 PRU_ICSSG IEP DIGIO

The IEP digital I/O (DIGIO) block provides dedicated I/Os for industrial ethernet protocols. The digital inputs can be sampled when specific events occur or continuously as a raw input. Likewise, driving the digital outputs can be triggered by specific events or controlled by software. The timing, delay cycle clocks, data sources, and data valid of the digital input and outputs are controlled by the [IEP_DIGIO_CTRL_REG](#) and [IEP_DIGIO_EXP_REG](#) registers. Additionally, the IEP DIGIO block can be used as generic I/Os in other applications.

14.2.8.1 PRU_ICSSG IEP DIGIO Features

The IEP digital I/O supports the following features:

- Digital data output:
 - 4 channels (PRG<k>_IEP0_EDIO_DATA_IN_OUT[31:28])
 - Five event options for driving output data output:
 - End of frame event (PRU0/1_RX_EOF)
 - SYNC0 events
 - SYNC1 events
 - Watchdog trigger
 - Software enable
- Digital data out enable (optional tri-state control)
- Digital data input:
 - 4 channels (PRG<k>_IEP0_EDIO_DATA_IN_OUT[31:28])
 - [IEP_DIGIO_DATA_IN_RAW_REG](#) supports direct sampling of PRG<k>_IEP0_EDIO_DATA_IN_OUT[31:28]
 - [IEP_DIGIO_DATA_IN_REG](#) supports four event options to trigger sampling of PRG<k>_IEP0_EDIO_DATA_IN_OUT[31:28]:
 - Start of frame event in start of frame (SOF) mode
 - pr<k>_iep<n>_edc_latch_in<0/1> event
 - SYNC0 events: pr<k>_iep<n>_edc_sync_out0
 - SYNC1 events: pr<k>_iep<n>_edc_sync_out1

14.2.8.2

The industrial digital I/Os supported by the PRU_ICSSG IEP peripheral are described in the [Table 14-2:](#)

Table 14-2. PRU_ICSSG IEP Digital IOs

Direction	Port	Mapped to Device I/Os	Notes
output	PRG<k>_IEP0_EDIO_DATA_IN_OUT[0:31]	PRG0_IEP0_EDIO_DATA_IN_OUT[31:28] PRG1_IEP0_EDIO_DATA_IN_OUT[31:28]	Only PRG<k>_IEP0_EDIO_DATA_IN_OUT[31:28] are exported to device pins as a bidirectional.
output	PRG<k>_EDIO_DATA_OUT_EN[0:31]	No	Optional tri-state control for DATA_OUT
output	PRG<k>_IEP0_EDIO_OUTVALID	PRG0_IEP0_EDIO_OUTVALID PRG1_IEP0_EDIO_OUTVALID	Will pulse even same data
output	PRG<k>_EDIO_SOF	No	PRU<0/1>_RX_SOF defined by IEP_DIGIO_EXP_REG[12] SOF_SEL
input	PRG<k>_EDIO_OE_EXT	No	
output	PRG<k>_EDIO_WD_TRIG	No	Just export of IEP_WD_STATUS_REG[0] PD_WD_STAT

Table 14-2. PRU_ICSSG IEP Digital IOs (continued)

Direction	Port	Mapped to Device I/Os	Notes
output	PRG<k>_EDIO_DATA_ENA	No	Reserved. Driven low.
input	PRG<k>_IEP<n>_EDC_LATCH_IN0	PRG0_IEP<n>_EDC_LATCH_IN0 PRG1_IEP<n>_EDC_LATCH_IN0	
input	PRG<k>_IEP<n>_EDC_LATCH_IN1	PRG0_IEP<n>_EDC_LATCH_IN1 PRG1_IEP<n>_EDC_LATCH_IN1	
output	PRG<k>_IEP<n>_EDC_SYNC_OUT0	PRG0_IEP<n>_EDC_SYNC_OUT0 PRG1_IEP<n>_EDC_SYNC_OUT0	
output	PRG<k>_IEP<n>_EDC_SYNC_OUT1	PRG0_IEP<n>_EDC_SYNC_OUT1 PRG1_IEP<n>_EDC_SYNC_OUT1	

14.2.8.3 PRU_ICSSG IEP DIGIO Block Diagrams

Figure 14-4 shows the signals and registers for capturing the DIGIO data in. Note that bit field [5-4]IN_MODE in the [IEP_DIGIO_CTRL_REG](#) register must be set to 1h for data to be latched on the external PRG<k>_IEP<n>_EDC_LATCH_IN0 signal. In PRU0/1_RX_SOF mode, the delay time of capturing PRG<k>_IEP0_EDIO_DATA_IN_OUT[31:28] is programmable through the [11-8]SOF_DLY bit of the [IEP_DIGIO_EXP_REG](#) register.

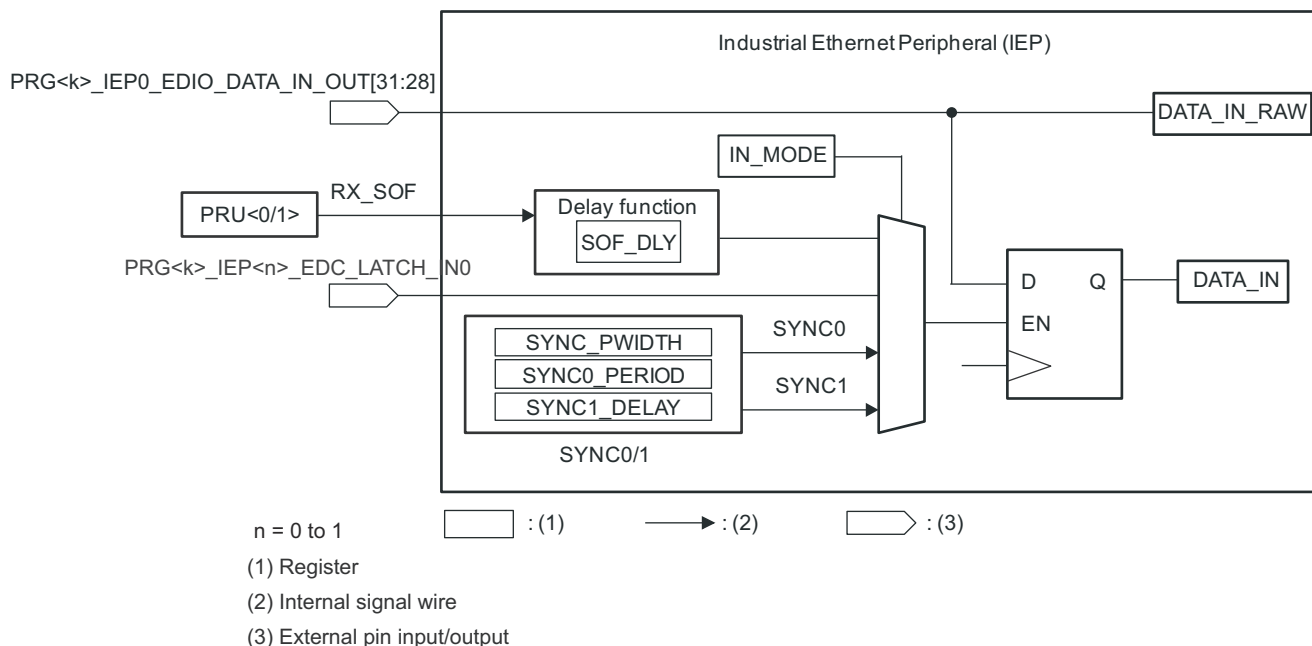


Figure 14-4. IEP DIGIO Data In

Figure 14-5 shows the signals and registers for driving the DIGIO data out.

The PRG<k>_IEP0_EDIO_DATA_IN_OUT[31:28] is immediately forced to zero when [IEP_DIGIO_CTRL_REG](#)[1] OUTVALID_MODE = 1h, pr1_edio_oe_ext = 1h, and pd_wd_exp = 1h, or the next update hardware post pd_wd_exp. Delay assertion of PRG<k>_IEP0_EDIO_OUTVALID from PRG<k>_IEP0_EDIO_DATA_IN_OUT[31:28] update events are controlled by software through [IEP_DIGIO_EXP_REG](#)[2] SW_OUTVALID.

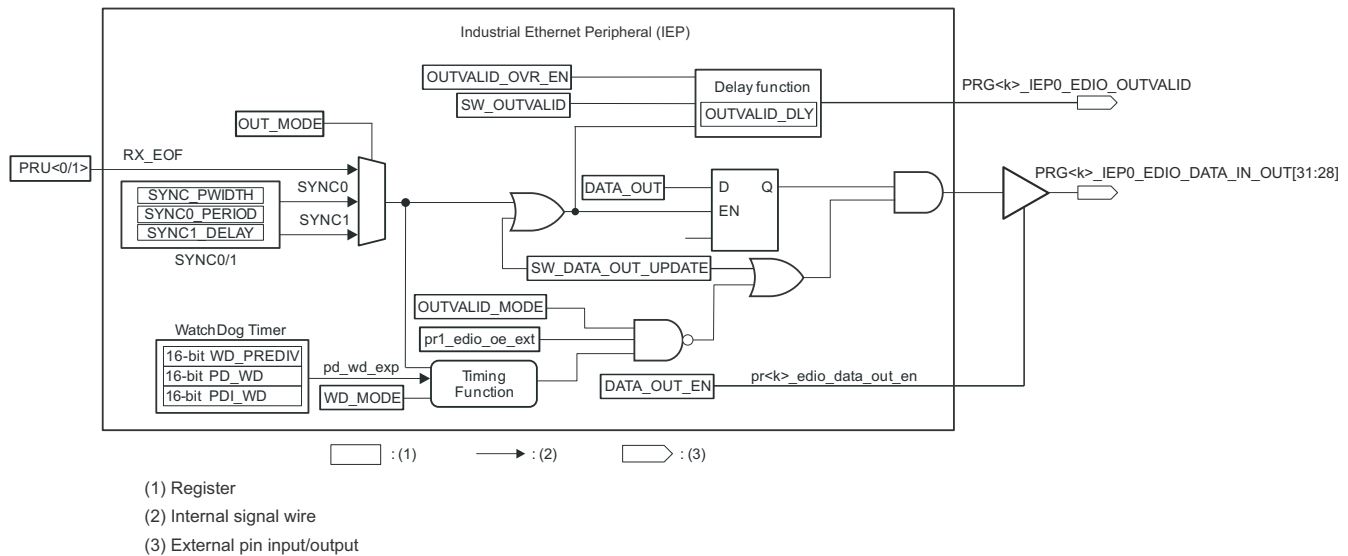


Figure 14-5. IEP DIGIO Data Out

14.2.8.4 PRU_ICSSG IEP Basic Programming Model

Follow these steps to configure and read the DIGIO Data Input:

1. Read [IEP_DIGIO_DATA_IN_RAW_REG](#) for raw input data

or

1. Enable sampling of PRG<k>_IEP0_EDIO_DATA_IN_OUT[31:28] by setting [IEP_DIGIO_CTRL_REG](#)[5-4] IN_MODE = 1h.
2. Read [IEP_DIGIO_DATA_IN_REG](#) for data sampled upon PRG<k>_IEP<n>_EDC_LATCH_IN0 posedge

Follow these steps to configure and write to the DIGIO Data Output:

1. Pre-configure DIGIO by setting [IEP_DIGIO_EXP_REG](#)[1] OUTVALID_OVR_EN and [IEP_DIGIO_EXP_REG](#)[0] SW_DATA_OUT_UP
2. Write to [IEP_DIGIO_DATA_OUT_REG](#) to configure output data.
3. To HiZ output, set corresponding [IEP_DIGIO_DATA_OUT_EN_REG](#)[31-0] DATA_OUT_EN bits to 1h (clear to 0h to drive value stored in [IEP_DIGIO_DATA_OUT_REG](#)).

15 PRU_ICSSG Registers

15.1 PRU_ICSSG PRU_CTRL, RTU_PRU_CTRL, and TX_PRU_CTRL Registers

Table 15-2 through Table 15-4 lists the memory-mapped control registers for the PRU_ICSSG PRU0/PRU1, RTU_PRU0/RTU_PRU1 and TX_PRU0/TX_PRU1 cores. All register offset addresses not listed in Table 15-2 through Table 15-4 should be considered as reserved locations and the register contents should not be modified.

Note

PDSP in instance names is equivalent to the PRU processor.

Table 15-1. PRU_CTRL Instances

Instance	Base Address
PRU_ICSSG0_PR1_PDSP0_IRAM	0B02 2000h
PRU_ICSSG0_PR1_PDSP1_IRAM	0B02 4000h
PRU_ICSSG1_PR1_PDSP0_IRAM	0B12 2000h
PRU_ICSSG1_PR1_PDSP1_IRAM	0B12 4000h
PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM	0B02 3000h
PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM	0B02 3800h
PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM	0B12 3000h
PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM	0B12 3800h
PRU_ICSSG0_PR1_TX_PDSP0_IRAM	0B02 5000h
PRU_ICSSG0_PR1_TX_PDSP1_IRAM	0B02 5800h
PRU_ICSSG1_PR1_TX_PDSP0_IRAM	0B12 5000h
PRU_ICSSG1_PR1_TX_PDSP1_IRAM	0B12 5800h

Table 15-2. PRU_CTRL Registers

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_PDSP0_IRAM Physical Address	PRU_ICSSG0_PR1_PDSP1_IRAM Physical Address	PRU_ICSSG1_PR1_PDSP0_IRAM Physical Address	PRU_ICSSG1_PR1_PDSP1_IRAM Physical Address
0h	ICSSG_PRU_CONTROL	Control Register	0B02 2000h	0B02 4000h	0B12 2000h	0B12 4000h
4h	ICSSG_PRU_STATUS	Status Register	0B02 2004h	0B02 4004h	0B12 2004h	0B12 4004h
8h	ICSSG_PRU_WAKEUP_EN	Wakeup Enable Register	0B02 2008h	0B02 4008h	0B12 2008h	0B12 4008h
Ch	ICSSG_PRU_CYCLE	Cycle Count	0B02 200Ch	0B02 400Ch	0B12 200Ch	0B12 400Ch
10h	ICSSG_PRU_STALL	Stall Count	0B02 2010h	0B02 4010h	0B12 2010h	0B12 4010h
20h	ICSSG_PRU_CTBIRO	Constant Table Block Index Register 0	0B02 2020h	0B02 4020h	0B12 2020h	0B12 4020h
24h	ICSSG_PRU_CTBIRO1	Constant Table Block Index Register 1	0B02 2024h	0B02 4024h	0B12 2024h	0B12 4024h
28h	ICSSG_PRU_CTPPRO	Constant Table Programmable Pointer Register 0	0B02 2028h	0B02 4028h	0B12 2028h	0B12 4028h
2Ch	ICSSG_PRU_CTPPRO1	Constant Table Programmable Pointer Register 1	0B02 202Ch	0B02 402Ch	0B12 202Ch	0B12 402Ch

Table 15-3. PRU_CTRL Registers 2

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_RTU0_P_R1_RTU0_IRAM Physical Address	PRU_ICSSG0_PR1_RTU1_P_R1_RTU1_IRAM Physical Address	PRU_ICSSG1_PR1_RTU0_P_R1_RTU0_IRAM Physical Address	PRU_ICSSG1_PR1_RTU1_P_R1_RTU1_IRAM Physical Address
0h	ICSSG_PRU_CONTROL	Control Register	0B02 3000h	0B02 3800h	0B12 3000h	0B12 3800h
4h	ICSSG_PRU_STATUS	Status Register	0B02 3004h	0B02 3804h	0B12 3004h	0B12 3804h
8h	ICSSG_PRU_WAKEUP_EN	Wakeup Enable Register	0B02 3008h	0B02 3808h	0B12 3008h	0B12 3808h
Ch	ICSSG_PRU_CYCLE	Cycle Count	0B02 300Ch	0B02 380Ch	0B12 300Ch	0B12 380Ch
10h	ICSSG_PRU_STALL	Stall Count	0B02 3010h	0B02 3810h	0B12 3010h	0B12 3810h

Table 15-3. PRU_CTRL Registers 2 (continued)

Offset	Acronym	Register Name	PRU_ICSSG0_ PR1_RTU0_P R1_RTU0_IRA M Physical Address	PRU_ICSSG0_ PR1_RTU1_P R1_RTU1_IRA M Physical Address	PRU_ICSSG1_ PR1_RTU0_P R1_RTU0_IRA M Physical Address	PRU_ICSSG1_ PR1_RTU1_P R1_RTU1_IRA M Physical Address
20h	ICSSG_PRU_CTBIRO	Constant Table Block Index Register 0	0B02 3020h	0B02 3820h	0B12 3020h	0B12 3820h
24h	ICSSG_PRU_CTBIRO1	Constant Table Block Index Register 1	0B02 3024h	0B02 3824h	0B12 3024h	0B12 3824h
28h	ICSSG_PRU_CTPPRO	Constant Table Programmable Pointer Register 0	0B02 3028h	0B02 3828h	0B12 3028h	0B12 3828h
2Ch	ICSSG_PRU_CTPPRO1	Constant Table Programmable Pointer Register 1	0B02 302Ch	0B02 382Ch	0B12 302Ch	0B12 382Ch

Table 15-4. PRU_CTRL Registers 4

Offset	Acronym	Register Name	PRU_ICSSG0_ PR1_TX_PDS P0_IRAM Physical Address	PRU_ICSSG0_ PR1_TX_PDSP P1_IRAM Physical Address	PRU_ICSSG1_ PR1_TX_PDS P0_IRAM Physical Address	PRU_ICSSG1_ PR1_TX_PDS P1_IRAM Physical Address
0h	ICSSG_PRU_CONTROL	Control Register	0B02 5000h	0B02 5800h	0B12 5000h	0B12 5800h
4h	ICSSG_PRU_STATUS	Status Register	0B02 5004h	0B02 5804h	0B12 5004h	0B12 5804h
8h	ICSSG_PRU_WAKEUP_EN	Wakeup Enable Register	0B02 5008h	0B02 5808h	0B12 5008h	0B12 5808h
Ch	ICSSG_PRU_CYCLE	Cycle Count	0B02 500Ch	0B02 580Ch	0B12 500Ch	0B12 580Ch
10h	ICSSG_PRU_STALL	Stall Count	0B02 5010h	0B02 5810h	0B12 5010h	0B12 5810h
20h	ICSSG_PRU_CTBIRO	Constant Table Block Index Register 0	0B02 5020h	0B02 5820h	0B12 5020h	0B12 5820h
24h	ICSSG_PRU_CTBIRO1	Constant Table Block Index Register 1	0B02 5024h	0B02 5824h	0B12 5024h	0B12 5824h
28h	ICSSG_PRU_CTPPRO	Constant Table Programmable Pointer Register 0	0B02 5028h	0B02 5828h	0B12 5028h	0B12 5828h
2Ch	ICSSG_PRU_CTPPRO1	Constant Table Programmable Pointer Register 1	0B02 502Ch	0B02 582Ch	0B12 502Ch	0B12 582Ch

15.1.1 ICSSG_PRU_CONTROL Register (Offset = 0h) [reset = 1h]

PRU_CONTROL is shown in [Figure 15-1](#) and described in [Table 15-6](#).

PRU Control Register.

Table 15-5. ICSSG_PRU_CONTROL Instances

Instance	Physical Address
PRU_ICSSG0_PR1_PDSP0_IRAM	0B02 2000h
PRU_ICSSG0_PR1_PDSP1_IRAM	0B02 4000h
PRU_ICSSG1_PR1_PDSP0_IRAM	0B12 2000h
PRU_ICSSG1_PR1_PDSP1_IRAM	0B12 4000h
PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM	0B02 3000h
PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM	0B02 3800h
PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM	0B12 3000h
PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM	0B12 3800h
PRU_ICSSG0_PR1_TX_PDSP0_IRAM	0B02 5000h
PRU_ICSSG0_PR1_TX_PDSP1_IRAM	0B02 5800h
PRU_ICSSG1_PR1_TX_PDSP0_IRAM	0B12 5000h
PRU_ICSSG1_PR1_TX_PDSP1_IRAM	0B12 5800h

Figure 15-1. ICSSG_PRU_CONTROL Register

31	30	29	28	27	26	25	24
PCOUNTER_RST_VAL							
R/W-0h							
23	22	21	20	19	18	17	16
PCOUNTER_RST_VAL							
R/W-0h							
15	14	13	12	11	10	9	8
RUNSTATE		TS_ENABLE	RESERVED				SINGLE_STEP
R-0h	R-0h		R-0h				R/W-0h
7	6	5	4	3	2	1	0
RESERVED				COUNTER_ENABLE	SLEEPING	ENABLE	SOFT_RST_N
R-0h				R/W-0h	R/W-0h	R/W-0h	R-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-6. ICSSG_PRU_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PCOUNTER_RST_VAL	R/W	0h	Program Counter Reset Value: This field controls the address where the PRU will start executing code from after it is taken out of reset.
15	RUNSTATE	R	0h	Run State: This bit indicates whether the PRU is currently executing an instruction or is halted. 0h = PRU is halted and host has access to the instruction RAM and debug registers regions. 1h = PRU is currently running and the host is locked out of the instruction RAM and debug registers regions. This bit is used by an external debug agent to know when the PRU has actually halted when waiting for a HALT instruction to execute, a single step to finish, or any other time when the [1]ENABLE has been cleared.

Table 15-6. ICSSG_PRU_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	TS_ENABLE	R	0h	Task Swapping Enable: This bit indicates the current state of the internal task swapping enable flag. When this bit is clear, the PRU will ignore requests which are presented on the Task Swap Request interface. When this bit is set, the PRU will gracefully complete any multi-cycle instruction and will then issue an XCHG instruction using the 22 LSBs as provided on the task swap request interface.
12-9	RESERVED	R	0h	Reserved
8	SINGLE_STEP	R/W	0h	Single Step Enable: This bit controls whether or not the PRU will only execute a single instruction when enabled. 0h = PRU will free run when enabled. 1h = PRU will execute a single instruction and then the [1]ENABLE bit will be cleared. Note that this bit does not actually enable the PRU, it only sets the policy for how much code will be run after the PRU is enabled. The [1]ENABLE bit must be explicitly asserted. It is expressly legal to initialize both the [8]SINGLE_STEP and [1]ENABLE bits simultaneously. (Two independent writes are not required to cause the stated functionality).
7-5	RESERVED	R	0h	Reserved
3	COUNTER_ENABLE	R/W	0h	PRU Cycle Counter Enable: Enables PRU cycle counters. 0h = Counters not enabled. 1h = Counters enabled.
2	SLEEPING	R/W	0h	PRU Sleep Indicator: This bit indicates whether or not the PRU is currently asleep. 0h = PRU is not asleep. 1h = PRU is asleep. If this bit is written to a 0h, the PRU will be forced to power up from sleep mode.
1	ENABLE	R/W	0h	Processor Enable: This bit controls whether or not the PRU is allowed to fetch new instructions. 0h = PRU is disabled. 1h = PRU is enabled. If this bit is de-asserted while the PRU is currently running and has completed the initial cycle of a multi-cycle instruction (LBxO, SBxO, SCAN, etc.), the current instruction will be allowed to complete before the PRU pauses execution. Otherwise, the PRU will halt immediately. Because of the unpredictability timing sensitivity of the instruction execution loop, this bit is not a reliable indication of whether or not the PRU is currently running. The [15]RUNSTATE bit should be consulted for an absolute indication of the run state of the core. When the PRU is halted, its internal state remains coherent therefore this bit can be reasserted without issuing a software reset and the PRU will resume processing exactly where it left off in the instruction stream.
0	SOFT_RST_N	R/W	1h	Soft Reset: When this bit is cleared, the PRU will be reset. This bit is set back to 1h on the next cycle after it has been cleared.

Table 15-7. Register Call Summary for ICSSG_PRU_CONTROL

PRU_ICSSG_PRU_CTRL, RTU_PRU_CTRL, and TX_PRU_CTRL Registers

- [ICSSG_PRU_CYCLE Register](#) (Offset = Ch) [reset = 0h]: [\[0\]](#) [\[1\]](#)
- [ICSSG_PRU_STALL Register](#) (Offset = 10h) [reset = 0h]: [\[0\]](#)

15.1.2 ICSSG_PRU_STATUS Register (Offset = 4h) [reset = 0h]

PRU_STATUS is shown in [Figure 15-2](#) and described in [Table 15-9](#).

PRU Status Register.

Table 15-8. ICSSG_PRU_STATUS Instances

Instance	Physical Address
PRU_ICSSG0_PR1_PDSP0_IRAM	0B02 2004h
PRU_ICSSG0_PR1_PDSP1_IRAM	0B02 4004h
PRU_ICSSG1_PR1_PDSP0_IRAM	0B12 2004h
PRU_ICSSG1_PR1_PDSP1_IRAM	0B12 4004h
PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM	0B02 3004h
PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM	0B02 3804h
PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM	0B12 3004h
PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM	0B12 3804h
PRU_ICSSG0_PR1_TX_PDSP0_IRAM	0B02 5004h
PRU_ICSSG0_PR1_TX_PDSP1_IRAM	0B02 5804h
PRU_ICSSG1_PR1_TX_PDSP0_IRAM	0B12 5004h
PRU_ICSSG1_PR1_TX_PDSP1_IRAM	0B12 5804h

Figure 15-2. ICSSG_PRU_STATUS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PCOUNTER															
R-0h																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 15-9. ICSSG_PRU_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	PCOUNTER	R	0h	Program Counter: This field is a registered (1 cycle delayed) reflection of the PRU program counter. Note that the PC is an instruction address where each instruction is a 32 bit word. This is not a byte address and to compute the byte address, multiply the PC by 4 (For example: PC of 2 = byte address of 8h, or PC of 8 = byte address of 20h).

15.1.3 ICSSG_PRU_WAKEUP_EN Register (Offset = 8h) [reset = 0h]

PRU_WAKEUP_EN is shown in [Figure 15-3](#) and described in [Table 15-11](#).

PRU Wakeup Enable Register.

Table 15-10. ICSSG_PRU_WAKEUP_EN Instances

Instance	Physical Address
PRU_ICSSG0_PR1_PDSP0_IRAM	0B02 2008h
PRU_ICSSG0_PR1_PDSP1_IRAM	0B02 4008h
PRU_ICSSG1_PR1_PDSP0_IRAM	0B12 2008h
PRU_ICSSG1_PR1_PDSP1_IRAM	0B12 4008h
PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM	0B02 3008h
PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM	0B02 3808h
PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM	0B12 3008h
PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM	0B12 3808h
PRU_ICSSG0_PR1_TX_PDSP0_IRAM	0B02 5008h
PRU_ICSSG0_PR1_TX_PDSP1_IRAM	0B02 5808h
PRU_ICSSG1_PR1_TX_PDSP0_IRAM	0B12 5008h
PRU_ICSSG1_PR1_TX_PDSP1_IRAM	0B12 5808h

Figure 15-3. ICSSG_PRU_WAKEUP_EN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BITWISE_ENABLES																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-11. ICSSG_PRU_WAKEUP_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BITWISE_ENABLES	R/W	0h	Wakeup Enables: This field is ANDed with the incoming R31 status inputs (whose bit positions were specified in the stmap parameter) to produce a vector which is unary ORed to produce the status_wakeup source for the core. Setting any bit in this vector will allow the corresponding status input to wake up the core when it is asserted high. The PRU should set this enable vector prior to executing a SLP (sleep) instruction to ensure that the desired sources can wake up the core.

15.1.4 ICSSG_PRU_CYCLE Register (Offset = Ch) [reset = 0h]

PRU_CYCLE is shown in [Figure 15-4](#) and described in [Table 15-13](#).

PRU Cycle Count. This register counts the number of cycles for which the PRU has been enabled.

Table 15-12. ICSSG_PRU_CYCLE Instances

Instance	Physical Address
PRU_ICSSG0_PR1_PDSP0_IRAM	0B02 200Ch
PRU_ICSSG0_PR1_PDSP1_IRAM	0B02 400Ch
PRU_ICSSG1_PR1_PDSP0_IRAM	0B12 200Ch
PRU_ICSSG1_PR1_PDSP1_IRAM	0B12 400Ch
PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM	0B02 300Ch
PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM	0B02 380Ch
PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM	0B12 300Ch
PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM	0B12 380Ch
PRU_ICSSG0_PR1_TX_PDSP0_IRAM	0B02 500Ch
PRU_ICSSG0_PR1_TX_PDSP1_IRAM	0B02 580Ch
PRU_ICSSG1_PR1_TX_PDSP0_IRAM	0B12 500Ch
PRU_ICSSG1_PR1_TX_PDSP1_IRAM	0B12 580Ch

Figure 15-4. ICSSG_PRU_CYCLE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CYCLECOUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-13. ICSSG_PRU_CYCLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CYCLECOUNT	R/W	0h	This value is incremented by 1 for every cycle during which the PRU is enabled and the counter is enabled (both bits [1]ENABLE and [3]COUNTER_ENABLE set in the ICSSG_PRU_CONTROL register). Counting halts while the PRU is disabled or counter is disabled, and resumes when re-enabled. Counter clears the [3]COUNTER_ENABLE bit in the ICSSG_PRU_CONTROL register when the count reaches FFFFFFFFh. (Count does not wrap). The register can be read at any time. The register can be cleared when the counter or PRU is disabled. Clearing this register also clears the PRU Stall Count Register (ICSSG_PRU_STALL).

Table 15-14. Register Call Summary for ICSSG_PRU_CYCLE

PRU_ICSSG_PRU_CTRL, RTU_PRU_CTRL, and TX_PRU_CTRL Registers

- [ICSSG_PRU_STALL](#) Register (Offset = 10h) [reset = 0h]: [0] [1]

15.1.5 ICSSG_PRU_STALL Register (Offset = 10h) [reset = 0h]

PRU_STALL is shown in [Figure 15-5](#) and described in [Table 15-16](#).

PRU Stall Count Register. This register counts the number of cycles for which the PRU has been enabled, but unable to fetch a new instruction. It is linked to the Cycle Count Register ([ICSSG_PRU_CYCLE](#), offset: 0Ch) such that this register reflects the stall cycles measured over the same cycles as counted by the cycle count register. Thus the value of this register is always less than or equal to cycle count.

Table 15-15. ICSSG_PRU_STALL Instances

Instance	Physical Address
PRU_ICSSG0_PR1_PDSP0_IRAM	0B02 2010h
PRU_ICSSG0_PR1_PDSP1_IRAM	0B02 4010h
PRU_ICSSG1_PR1_PDSP0_IRAM	0B12 2010h
PRU_ICSSG1_PR1_PDSP1_IRAM	0B12 4010h
PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM	0B02 3010h
PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM	0B02 3810h
PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM	0B12 3010h
PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM	0B12 3810h
PRU_ICSSG0_PR1_TX_PDSP0_IRAM	0B02 5010h
PRU_ICSSG0_PR1_TX_PDSP1_IRAM	0B02 5810h
PRU_ICSSG1_PR1_TX_PDSP0_IRAM	0B12 5010h
PRU_ICSSG1_PR1_TX_PDSP1_IRAM	0B12 5810h

Figure 15-5. ICSSG_PRU_STALL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STALLCOUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-16. ICSSG_PRU_STALL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	STALLCOUNT	R	0h	This value is incremented by 1 for every cycle during which the PRU is enabled and the counter is enabled (both bits [1]ENABLE and [3]COUNTER_ENABLE set in the ICSSG_PRU_CONTROL register), and the PRU was unable to fetch a new instruction for any reason. Counting halts while the PRU is disabled or the counter is disabled, and resumes when re-enabled. The register can be read at any time. The register is cleared when PRU Cycle Count Register (ICSSG_PRU_CYCLE) is cleared.

Table 15-17. Register Call Summary for ICSSG_PRU_STALL

PRU_ICSSG_PRU_CTRL, RTU_PRU_CTRL, and TX_PRU_CTRL Registers

- [ICSSG_PRU_CYCLE](#) Register (Offset = Ch) [reset = 0h]: [0]

15.1.6 ICSSG_PRU_CTBIRO Register (Offset = 20h) [reset = 0h]

PRU_CTBIRO is shown in [Figure 15-6](#) and described in [Table 15-19](#).

Constant Table Block Index Register 0. This register is used to set the block indices which are used to modify entries 24 and 25 in the PRU Constant Table. This register can be written by the PRU whenever it needs to change to a new base pointer for a block in the State Scratchpad RAM. This function is useful since the PRU is often processing multiple processing threads which require it to change contexts. The PRU can use this register to avoid requiring excessive amounts of code for repetitive context switching.

Table 15-18. ICSSG_PRU_CTBIRO Instances

Instance	Physical Address
PRU_ICSSG0_PR1_PDSP0_IRAM	0B02 2020h
PRU_ICSSG0_PR1_PDSP1_IRAM	0B02 4020h
PRU_ICSSG1_PR1_PDSP0_IRAM	0B12 2020h
PRU_ICSSG1_PR1_PDSP1_IRAM	0B12 4020h
PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM	0B02 3020h
PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM	0B02 3820h
PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM	0B12 3020h
PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM	0B12 3820h
PRU_ICSSG0_PR1_TX_PDSP0_IRAM	0B02 5020h
PRU_ICSSG0_PR1_TX_PDSP1_IRAM	0B02 5820h
PRU_ICSSG1_PR1_TX_PDSP0_IRAM	0B12 5020h
PRU_ICSSG1_PR1_TX_PDSP1_IRAM	0B12 5820h

Figure 15-6. ICSSG_PRU_CTBIRO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								C25_BLK_INDEX							
R-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								C24_BLK_INDEX							
R-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-19. ICSSG_PRU_CTBIRO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	C25_BLK_INDEX	R/W	0h	PRU Constant Entry 25 Block Index: This field sets the value that will appear in bits 15:8 of entry 25 in the PRU Constant Table. This field while always present is only used if the creg_cnt configuration value is less than 26.
15-8	RESERVED	R	0h	Reserved
7-0	C24_BLK_INDEX	R/W	0h	PRU Constant Entry 24 Block Index: This field sets the value that will appear in bits 15:8 of entry 24 in the PRU Constant Table. This field while always present is only used if the creg_cnt configuration value is less than 25.

15.1.7 ICSSG_PRU_CTIR1 Register (Offset = 24h) [reset = 0h]

PRU_CTIR1 is shown in [Figure 15-7](#) and described in [Table 15-21](#).

Constant Table Block Index Register 1. This register is used to set the block indices which are used to modify entries 26 and 27 in the PRU Constant Table. This register can be written by the PRU whenever it needs to change to a new base pointer for a block in the State Scratchpad RAM. This function is useful since the PRU is often processing multiple processing threads which require it to change contexts. The PRU can use this register to avoid requiring excessive amounts of code for repetitive context switching.

Table 15-20. ICSSG_PRU_CTIR1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_PDSP0_IRAM	0B02 2024h
PRU_ICSSG0_PR1_PDSP1_IRAM	0B02 4024h
PRU_ICSSG1_PR1_PDSP0_IRAM	0B12 2024h
PRU_ICSSG1_PR1_PDSP1_IRAM	0B12 4024h
PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM	0B02 3024h
PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM	0B02 3824h
PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM	0B12 3024h
PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM	0B12 3824h
PRU_ICSSG0_PR1_TX_PDSP0_IRAM	0B02 5024h
PRU_ICSSG0_PR1_TX_PDSP1_IRAM	0B02 5824h
PRU_ICSSG1_PR1_TX_PDSP0_IRAM	0B12 5024h
PRU_ICSSG1_PR1_TX_PDSP1_IRAM	0B12 5824h

Figure 15-7. ICSSG_PRU_CTIR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								C27_BLK_INDEX							
R-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								C26_BLK_INDEX							
R-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-21. ICSSG_PRU_CTIR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	C27_BLK_INDEX	R/W	0h	PRU Constant Entry 27 Block Index: This field sets the value that will appear in bits 15:8 of entry 27 in the PRU Constant Table. This field while always present is only used if the creg_cnt configuration value is less than 28.
15-8	RESERVED	R	0h	Reserved
7-0	C26_BLK_INDEX	R/W	0h	PRU Constant Entry 26 Block Index: This field sets the value that will appear in bits 15:8 of entry 26 in the PRU Constant Table. This field while always present is only used if the creg_cnt configuration value is less than 27.

15.1.8 ICSSG_PRU_CTPPR0 Register (Offset = 28h) [reset = 0h]

PRU_CTPPR0 is shown in [Figure 15-8](#) and described in [Table 15-23](#).

Constant Table Programmable Pointer Register 0. This register allows the PRU to set up the 256-byte page index for entries 28 and 29 in the PRU Constant Table which serve as general purpose pointers which can be configured to point to any locations inside the session router address map. This register is useful when the PRU needs to frequently access certain structures inside the session router address space whose locations are not hard coded such as tables in scratchpad memory.

Table 15-22. ICSSG_PRU_CTPPR0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_PDSP0_IRAM	0B02 2028h
PRU_ICSSG0_PR1_PDSP1_IRAM	0B02 4028h
PRU_ICSSG1_PR1_PDSP0_IRAM	0B12 2028h
PRU_ICSSG1_PR1_PDSP1_IRAM	0B12 4028h
PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM	0B02 3028h
PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM	0B02 3828h
PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM	0B12 3028h
PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM	0B12 3828h
PRU_ICSSG0_PR1_TX_PDSP0_IRAM	0B02 5028h
PRU_ICSSG0_PR1_TX_PDSP1_IRAM	0B02 5828h
PRU_ICSSG1_PR1_TX_PDSP0_IRAM	0B12 5028h
PRU_ICSSG1_PR1_TX_PDSP1_IRAM	0B12 5828h

Figure 15-8. ICSSG_PRU_CTPPR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C29_POINTER																C28_POINTER															
R/W-0h																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-23. ICSSG_PRU_CTPPR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	C29_POINTER	R/W	0h	PRU Constant Entry 29 Pointer: This field sets the value that will appear in bits [23-8] of entry 29 in the PRU Constant Table. This field while always present is only used if the creg_cnt configuration value is less than 30.
15-0	C28_POINTER	R/W	0h	PRU Constant Entry 28 Pointer: This field sets the value that will appear in bits [23-8] of entry 28 in the PRU Constant Table. This field while always present is only used if the creg_cnt configuration value is less than 29.

15.1.9 ICSSG_PRU_CTPPR1 Register (Offset = 2Ch) [reset = 0h]

PRU_CTPPR1 is shown in [Figure 15-9](#) and described in [Table 15-25](#).

Constant Table Programmable Pointer Register 1. This register functions the same as the PRU Constant Table Programmable Pointer Register 0 but allows the PRU to control entries 30 and 31 in the PRU Constant Table.

Table 15-24. ICSSG_PRU_CTPPR1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_PDSP0_IRAM	0B02 202Ch
PRU_ICSSG0_PR1_PDSP1_IRAM	0B02 402Ch
PRU_ICSSG1_PR1_PDSP0_IRAM	0B12 202Ch
PRU_ICSSG1_PR1_PDSP1_IRAM	0B12 402Ch
PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM	0B02 302Ch
PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM	0B02 382Ch
PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM	0B12 302Ch
PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM	0B12 382Ch
PRU_ICSSG0_PR1_TX_PDSP0_IRAM	0B02 502Ch
PRU_ICSSG0_PR1_TX_PDSP1_IRAM	0B02 582Ch
PRU_ICSSG1_PR1_TX_PDSP0_IRAM	0B12 502Ch
PRU_ICSSG1_PR1_TX_PDSP1_IRAM	0B12 582Ch

Figure 15-9. ICSSG_PRU_CTPPR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C31_POINTER																C30_POINTER															
R/W-0h																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-25. ICSSG_PRU_CTPPR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	C31_POINTER	R/W	0h	PRU Constant Entry 31 Pointer: This field sets the value that will appear in bits [23-8] of entry 31 in the PRU Constant Table. This field while always present is only used if the creg_cnt configuration value is less than 32.
15-0	C30_POINTER	R/W	0h	PRU Constant Entry 30 Pointer: This field sets the value that will appear in bits [23-8] of entry 30 in the PRU Constant Table. This field while always present is only used if the creg_cnt configuration value is less than 31.

15.2 PRU_ICSSG PRU_DEBUG, RTU_PRU_DEBUG, and TX_PRU_DEBUG Registers

Table 15-27 through Table 15-29 lists the memory-mapped registers for the PRU_ICSSG PRU_DEBUG, RTU_PRU_DEBUG and TX_PRU_DEBUG. All register offset addresses not listed in Table 15-27 through Table 15-29 should be considered as reserved locations and the register contents should not be modified.

Note

PDSP in instance names is equivalent to the PRU processor names.

Table 15-26. PRU_DEBUG Instances

Instance	Base Address
PRU_ICSSG0_PR1_PDSP0_IRAM_DEBUG	0B02 2400h
PRU_ICSSG0_PR1_PDSP1_IRAM_DEBUG	0B02 4400h
PRU_ICSSG1_PR1_PDSP0_IRAM_DEBUG	0B12 2400h
PRU_ICSSG1_PR1_PDSP1_IRAM_DEBUG	0B12 4400h
PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM_DEBUG	0B02 3400h
PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM_DEBUG	0B02 3C00h
PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM_DEBUG	0B12 3400h
PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM_DEBUG	0B12 3C00h
PRU_ICSSG0_PR1_TX_PDSP0_IRAM_DEBUG	0B02 5400h
PRU_ICSSG0_PR1_TX_PDSP1_IRAM_DEBUG	0B02 5C00h
PRU_ICSSG1_PR1_TX_PDSP0_IRAM_DEBUG	0B12 5400h
PRU_ICSSG1_PR1_TX_PDSP1_IRAM_DEBUG	0B12 5C00h

Table 15-27. PRU_DEBUG Registers

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_PDSP0_IRAM_DEBUG Physical Address	PRU_ICSSG0_PR1_PDSP1_IRAM_DEBUG Physical Address	PRU_ICSSG1_PR1_PDSP0_IRAM_DEBUG Physical Address	PRU_ICSSG1_PR1_PDSP1_IRAM_DEBUG Physical Address
0h + formula	ICSSG_DBG_GPREG_y	DEBUG PRU General Purpose Registers 0 to 31	0B02 2400h + formula	0B02 4400h + formula	0B12 2400h + formula	0B12 4400h + formula
80h + formula	ICSSG_DBG_CT_REG_y	DEBUG PRU Constant Table Entry Registers 0 to 31	0B02 2480h + formula	0B02 4480h + formula	0B12 2480h + formula	0B12 4480h + formula

Table 15-28. PRU_DEBUG Registers 2

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM_DEBUG Physical Address	PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM_DEBUG Physical Address	PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM_DEBUG Physical Address	PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM_DEBUG Physical Address
0h + formula	ICSSG_DBG_GPREG_y	DEBUG PRU General Purpose Registers 0 to 31	0B02 3400h + formula	0B02 3C00h + formula	0B12 3400h + formula	0B12 3C00h + formula
80h + formula	ICSSG_DBG_CT_REG_y	DEBUG PRU Constant Table Entry Registers 0 to 31	0B02 3480h + formula	0B02 3C80h + formula	0B12 3480h + formula	0B12 3C80h + formula

Table 15-29. PRU_DEBUG Registers 3

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_TX_PDSP0_IRAM_DEBUG Physical Address	PRU_ICSSG0_PR1_TX_PDSP1_IRAM_DEBUG Physical Address	PRU_ICSSG1_PR1_TX_PDSP0_IRAM_DEBUG Physical Address	PRU_ICSSG1_PR1_TX_PDSP1_IRAM_DEBUG Physical Address
0h + formula	ICSSG_DBG_GPREG_y	DEBUG PRU General Purpose Registers 0 to 31	0B02 5400h + formula	0B02 5C00h + formula	0B12 5400h + formula	0B12 5C00h + formula

Table 15-29. PRU_DEBUG Registers 3 (continued)

Offset	Acronym	Register Name	PRU_ICSSG0 _PR1_TX_PD SP0_IRAM_D EBUG Physical Address	PRU_ICSSG0 _PR1_TX_PD SP1_IRAM_D EBUG Physical Address	PRU_ICSSG1 _PR1_TX_PD SP0_IRAM_D EBUG Physical Address	PRU_ICSSG1 _PR1_TX_PD SP1_IRAM_D EBUG Physical Address
80h + formula	ICSSG_DBG_CT_REG_y	DEBUG PRU Constant Table Entry Registers 0 to 31	0B02 5480h + formula	0B02 5C80h + formula	0B12 5480h + formula	0B12 5C80h + formula

15.2.1 ICSSG_DBG_GPREG_y Register (Offset = 0h + formula) [reset = 0h]

ICSSG_DBG_GPREG_y is shown in [Figure 15-10](#) and described in [Table 15-31](#).

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DEBUG PRU General Purpose Registers 0 to 31. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Offset = 0h + (y * 4); where y = 0 to 31

Table 15-30. ICSSG_DBG_GPREG_y Instances

Instance	Physical Address
PRU_ICSSG0_PR1_PDSP0_IRAM_DEBUG	0B02 2400h + formula
PRU_ICSSG0_PR1_PDSP1_IRAM_DEBUG	0B02 4400h + formula
PRU_ICSSG1_PR1_PDSP0_IRAM_DEBUG	0B12 2400h + formula
PRU_ICSSG1_PR1_PDSP1_IRAM_DEBUG	0B12 4400h + formula
PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM_DEBUG	0B02 3400h + formula
PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM_DEBUG	0B02 3C00h + formula
PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM_DEBUG	0B12 3400h + formula
PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM_DEBUG	0B12 3C00h + formula
PRU_ICSSG0_PR1_TX_PDSP0_IRAM_DEBUG	0B02 5400h + formula
PRU_ICSSG0_PR1_TX_PDSP1_IRAM_DEBUG	0B02 5C00h + formula
PRU_ICSSG1_PR1_TX_PDSP0_IRAM_DEBUG	0B12 5400h + formula
PRU_ICSSG1_PR1_TX_PDSP1_IRAM_DEBUG	0B12 5C00h + formula

Figure 15-10. ICSSG_DBG_GPREG_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REGy																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 15-31. ICSSG_DBG_GPREG_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REGy	R/W	0h	PRU Internal GP Register y: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal register file.

15.2.2 ICSSG_DBG_CT_REG_y Register (Offset = 80h + formula) [reset = 0h]

ICSSG_DBG_CT_REG_y is shown in Figure 15-11 and described in Table 15-33.

Return to [Summary Table](#).

DEBUG PRU Constant Table Entry Registers 0 to 31. This register allows an external agent to debug/or configure the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Offset = 80h + (y * 4); where y = 0 to 31

Table 15-32. ICSSG_DBG_CT_REG_y Instances

Instance	Physical Address
PRU_ICSSG0_PR1_PDSP0_IRAM_DEBUG	0B02 2480h + formula
PRU_ICSSG0_PR1_PDSP1_IRAM_DEBUG	0B02 4480h + formula
PRU_ICSSG1_PR1_PDSP0_IRAM_DEBUG	0B12 2480h + formula
PRU_ICSSG1_PR1_PDSP1_IRAM_DEBUG	0B12 4480h + formula
PRU_ICSSG0_PR1_RTU0_PR1_RTU0_IRAM_DEBUG	0B02 3480h + formula
PRU_ICSSG0_PR1_RTU1_PR1_RTU1_IRAM_DEBUG	0B02 3C80h + formula
PRU_ICSSG1_PR1_RTU0_PR1_RTU0_IRAM_DEBUG	0B12 3480h + formula
PRU_ICSSG1_PR1_RTU1_PR1_RTU1_IRAM_DEBUG	0B12 3C80h + formula
PRU_ICSSG0_PR1_TX_PDSP0_IRAM_DEBUG	0B02 5480h + formula
PRU_ICSSG0_PR1_TX_PDSP1_IRAM_DEBUG	0B02 5C80h + formula
PRU_ICSSG1_PR1_TX_PDSP0_IRAM_DEBUG	0B12 5480h + formula
PRU_ICSSG1_PR1_TX_PDSP1_IRAM_DEBUG	0B12 5C80h + formula

Figure 15-11. ICSSG_DBG_CT_REG_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REGy																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -n = value after reset

Table 15-33. ICSSG_DBG_CT_REG_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REGy	R/W	0h	PRU Internal Constants Table Entry y (where y = 0 to 31): Reading this field directly inspects the corresponding entry in the PRU internal constants table. Note: For each register y where y is less than the creg_cnt configuration parameter, the PRU internal Constants Table Entry Register will be writable and these registers are to be used to set the value for these constants. As for reads, the PRU must be disabled in order to access these registers.

Table 15-34. Register Call Summary for ICSSG_DBG_CT_REG_y

ICSSG_DBG_GPREG_y Register (Offset = 0h + formula) [reset = 0h]

- [ICSSG_DBG_CT_REG_y Register \(Offset = 80h + formula\) \[reset = 0h\]: \[0\]](#)

Table 15-35. Register Call Summary for ICSSG_DBG_GPREG_y

PRU_ICSSG PRU_DEBUG, RTU_PRU_DEBUG, and TX_PRU_DEBUG Registers

- [ICSSG_DBG_GPREG_y Register \(Offset = 0h + formula\) \[reset = 0h\]: \[0\]](#)

15.3 PRU_ICSSG_ECC_AGGR Registers

Table 15-37 lists the memory-mapped registers for the PRU_ICSSG_ECC_AGGR registers. All register offset addresses not listed in Table 15-37 should be considered as reserved locations and the register contents should not be modified.

Table 15-36. PRU_ICSSG_ECC_AGGR Instances

Instance	Base Address
PRU_ICSSG0_ECC_AGGR	0BF0 0000h
PRU_ICSSG1_ECC_AGGR	0BF0 1000h

Table 15-37. PRU_ICSSG_ECC_AGGR Registers

Offset	Acronym	Register Name	PRU_ICSSG0_ECC_AGGR Physical Address	PRU_ICSSG1_ECC_AGGR Physical Address
0h	ICSSG_REV	Aggregator Revision Register	0BF0 0000h	0BF0 1000h
8h	ICSSG_VECTOR	ECC Vector Register	0BF0 0008h	0BF0 1008h
Ch	ICSSG_STAT	Misc Status	0BF0 000Ch	0BF0 100Ch
3Ch	ICSSG_SEC_EOI_REG	EOI Register	0BF0 003Ch	0BF0 103Ch
40h	ICSSG_SEC_STATUS_REG0	Interrupt Status Register 0	0BF0 0040h	0BF0 1040h
80h	ICSSG_SEC_ENABLE_SET_REG0	Interrupt Enable Set Register 0	0BF0 0080h	0BF0 1080h
C0h	ICSSG_SEC_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	0BF0 00C0h	0BF0 10C0h
13Ch	ICSSG_DED_EOI_REG	EOI Register	0BF0 013Ch	0BF0 113Ch
140h	ICSSG_DED_STATUS_REG0	Interrupt Status Register 0	0BF0 0140h	0BF0 1140h
180h	ICSSG_DED_ENABLE_SET_REG0	Interrupt Enable Set Register 0	0BF0 0180h	0BF0 1180h
1C0h	ICSSG_DED_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	0BF0 01C0h	0BF0 11C0h
200h	ICSSG_AGGR_ENABLE_SET	AGGR Interrupt Enable Set Register	0BF0 0200h	0BF0 1200h
204h	ICSSG_AGGR_ENABLE_CLR	AGGR Interrupt Enable Clear Register	0BF0 0204h	0BF0 1204h
208h	ICSSG_AGGR_STATUS_SET	AGGR Interrupt Status Set Register	0BF0 0208h	0BF0 1208h
20Ch	ICSSG_AGGR_STATUS_CLR	AGGR Interrupt Status Clear Register	0BF0 020Ch	0BF0 120Ch

15.3.1 ICSSG_REV Register (Offset = 0h) [reset = 66A0E200h]

ICSSG_REV is shown in Figure 15-12 and described in Table 15-39.

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Revision parameters

Table 15-38. ICSSG_REV Instances

Instance	Physical Address
PRU_ICSSG0_ECC_AGGR	0BF0 0000h
PRU_ICSSG1_ECC_AGGR	0BF0 1000h

Figure 15-12. ICSSG_REV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R-1h		R-2h		R-6A0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
R-1Ch					R-2h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 15-39. ICSSG_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	bu
27-16	MODULE_ID	R	6A0h	Module ID
15-11	REVRTL	R	1Ch	RTL version
10-8	REVMAJ	R	2h	Major version
7-6	CUSTOM	R	0h	Custom version
5-0	REVMIN	R	0h	Minor version

Table 15-40. Register Call Summary for ICSSG_REV

PRU_ICSSG_ECC_AGGR Registers

- [PRU_ICSSG_ECC_AGGR Registers: \[0\]](#)
- [ICSSG_REV Register \(Offset = 0h\) \[reset = 66A0E200h\]: \[0\]](#)

15.3.2 ICSSG_VECTOR Register (Offset = 8h) [reset = X]

ICSSG_VECTOR is shown in Figure 15-13 and described in Table 15-42.

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ECC Vector Register

Table 15-41. ICSSG_VECTOR Instances

Instance	Physical Address
PRU_ICSSG0_ECC_AGGR	0BF0 0008h
PRU_ICSSG1_ECC_AGGR	0BF0 1008h

Figure 15-13. ICSSG_VECTOR Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
R/W-X							R/W1C-0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W-0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1S-0h	R/W-X				R/W-0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W-0h							

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 15-42. ICSSG_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	RD_SVBUS_DONE	R/W1C	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23-16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1S	0h	Write 1 to trigger a read on the serial VBUS
14-11	RESERVED	R/W	X	
10-0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

Table 15-43. Register Call Summary for ICSSG_VECTOR

PRU_ICSSG_ECC_AGGR Registers

- [ICSSG_VECTOR Register \(Offset = 8h\) \[reset = X\]: \[0\]](#)
- [PRU_ICSSG_ECC_AGGR Registers: \[0\]](#)

15.3.3 ICSSG_STAT Register (Offset = Ch) [reset = X]

ICSSG_STAT is shown in [Figure 15-14](#) and described in [Table 15-45](#).

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Misc Status

Table 15-44. ICSSG_STAT Instances

Instance	Physical Address
PRU_ICSSG0_ECC_AGGR	0BF0 000Ch
PRU_ICSSG1_ECC_AGGR	0BF0 100Ch

Figure 15-14. ICSSG_STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												NUM_RAMs																			
R-X												R-9h																			

LEGEND: R = Read Only; -n = value after reset

Table 15-45. ICSSG_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	X	
10-0	NUM_RAMs	R	9h	Indicates the number of RAMs serviced by the ECC aggregator

Table 15-46. Register Call Summary for ICSSG_STAT

PRU_ICSSG_ECC_AGGR Registers

- [ICSSG_STAT Register \(Offset = Ch\) \[reset = X\]: \[0\]](#)
- [PRU_ICSSG_ECC_AGGR Registers: \[0\]](#)

15.3.4 ICSSG_SEC_EOI_REG Register (Offset = 3Ch) [reset = X]

ICSSG_SEC_EOI_REG is shown in Figure 15-15 and described in Table 15-48.

Return to [Summary Table](#).

EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 15-47. ICSSG_SEC_EOI_REG Instances

Instance	Physical Address
PRU_ICSSG0_ECC_AGGR	0BF0 003Ch
PRU_ICSSG1_ECC_AGGR	0BF0 103Ch

Figure 15-15. ICSSG_SEC_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 15-48. ICSSG_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EOI_WR	R/W1S	0h	EOI Register

Table 15-49. Register Call Summary for ICSSG_SEC_EOI_REG

PRU_ICSSG_ECC_AGGR Registers

- [ICSSG_SEC_EOI_REG Register \(Offset = 3Ch\) \[reset = X\]: \[0\]](#)
- [PRU_ICSSG_ECC_AGGR Registers: \[0\]](#)

15.3.5 ICSSG_SEC_STATUS_REG0 Register (Offset = 40h) [reset = X]

ICSSG_SEC_STATUS_REG0 is shown in [Figure 15-16](#) and described in [Table 15-51](#).

[Return to Summary Table.](#)

Interrupt Status Register 0

Table 15-50. ICSSG_SEC_STATUS_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_ECC_AGGR	0BF0 0040h
PRU_ICSSG1_ECC_AGGR	0BF0 1040h

Figure 15-16. ICSSG_SEC_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							PR1_PDSP_TX1_IRAM_PEND
R/W-X							R/W1S-0h
7	6	5	4	3	2	1	0
PR1_PDSP_TX0_IRAM_PEND	PR1_RTU1_IRAM_ECC_PEND	PR1_RTU0_IRAM_ECC_PEND	PR1_RAM_PEND	PR1_PDSP1_IRAM_PEND	PR1_PDSP0_IRAM_PEND	PR1_DRAM1_PEND	PR1_DRAM0_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 15-51. ICSSG_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	PR1_PDSP_TX1_IRAM_PEND	R/W1S	0h	Interrupt Pending Status for pr1_pdsp_tx1_iram_pend
7	PR1_PDSP_TX0_IRAM_PEND	R/W1S	0h	Interrupt Pending Status for pr1_pdsp_tx0_iram_pend
6	PR1_RTU1_IRAM_ECC_PEND	R/W1S	0h	Interrupt Pending Status for pr1_rtu1_iram_ecc_pend
5	PR1_RTU0_IRAM_ECC_PEND	R/W1S	0h	Interrupt Pending Status for pr1_rtu0_iram_ecc_pend
4	PR1_RAM_PEND	R/W1S	0h	Interrupt Pending Status for pr1_ram_pend
3	PR1_PDSP1_IRAM_PEND	R/W1S	0h	Interrupt Pending Status for pr1_pdsp1_iram_pend
2	PR1_PDSP0_IRAM_PEND	R/W1S	0h	Interrupt Pending Status for pr1_pdsp0_iram_pend
1	PR1_DRAM1_PEND	R/W1S	0h	Interrupt Pending Status for pr1_dram1_pend
0	PR1_DRAM0_PEND	R/W1S	0h	Interrupt Pending Status for pr1_dram0_pend

Table 15-52. Register Call Summary for ICSSG_SEC_STATUS_REG0

PRU_ICSSG_ECC_AGGR Registers

- [ICSSG_SEC_STATUS_REG0 Register \(Offset = 40h\) \[reset = X\]: \[0\]](#)
- [PRU_ICSSG_ECC_AGGR Registers: \[0\]](#)

15.3.6 ICSSG_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = X]

ICSSG_SEC_ENABLE_SET_REG0 is shown in Figure 15-17 and described in Table 15-54.

Return to [Summary Table](#).

Interrupt Enable Set Register 0

**Table 15-53. ICSSG_SEC_ENABLE_SET_REG0
Instances**

Instance	Physical Address
PRU_ICSSG0_ECC_AGGR	0BF0 0080h
PRU_ICSSG1_ECC_AGGR	0BF0 1080h

Figure 15-17. ICSSG_SEC_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							PR1_PDSP_TX 1_IRAM_ENAB LE_SET
R/W-X							R/W1S-0h
7	6	5	4	3	2	1	0
PR1_PDSP_TX 0_IRAM_ENAB LE_SET	PR1_RTU1_IR AM_ECC_ENA BLE_SET	PR1_RTU0_IR AM_ECC_ENA BLE_SET	PR1_RAM_EN ABLE_SET	PR1_PDSP1_I RAM_ENABLE _SET	PR1_PDSP0_I RAM_ENABLE _SET	PR1_DRAM1_E NABLE_SET	PR1_DRAM0_E NABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 15-54. ICSSG_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	PR1_PDSP_TX1_IRAM_E NABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pr1_pdsp_tx1_iram_pend
7	PR1_PDSP_TX0_IRAM_E NABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pr1_pdsp_tx0_iram_pend
6	PR1_RTU1_IRAM_ECC_ ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pr1_rtu1_iram_ecc_pend
5	PR1_RTU0_IRAM_ECC_ ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pr1_rtu0_iram_ecc_pend
4	PR1_RAM_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pr1_ram_pend
3	PR1_PDSP1_IRAM_ENA BLE_SET	R/W1S	0h	Interrupt Enable Set Register for pr1_pdsp1_iram_pend
2	PR1_PDSP0_IRAM_ENA BLE_SET	R/W1S	0h	Interrupt Enable Set Register for pr1_pdsp0_iram_pend
1	PR1_DRAM1_ENABLE_S ET	R/W1S	0h	Interrupt Enable Set Register for pr1_dram1_pend
0	PR1_DRAM0_ENABLE_S ET	R/W1S	0h	Interrupt Enable Set Register for pr1_dram0_pend

Table 15-55. Register Call Summary for ICSSG_SEC_ENABLE_SET_REG0

PRU_ICSSG_ECC_AGGR Registers

- [PRU_ICSSG_ECC_AGGR Registers](#): [0]
- [ICSSG_SEC_ENABLE_SET_REG0 Register \(Offset = 80h\) \[reset = X\]: \[0\]](#)

15.3.7 ICSSG_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = X]

ICSSG_SEC_ENABLE_CLR_REG0 is shown in Figure 15-18 and described in Table 15-57.

Return to [Summary Table](#).

Interrupt Enable Clear Register 0

**Table 15-56. ICSSG_SEC_ENABLE_CLR_REG0
Instances**

Instance	Physical Address
PRU_ICSSG0_ECC_AGGR	0BF0 00C0h
PRU_ICSSG1_ECC_AGGR	0BF0 10C0h

Figure 15-18. ICSSG_SEC_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							PR1_PDSP_TX 1_IRAM_ENAB LE_CLR
R/W-X							R/W1C-0h
7	6	5	4	3	2	1	0
PR1_PDSP_TX 0_IRAM_ENAB LE_CLR	PR1_RTU1_IR AM_ECC_ENA BLE_CLR	PR1_RTU0_IR AM_ECC_ENA BLE_CLR	PR1_RAM_EN ABLE_CLR	PR1_PDSP1_I RAM_ENABLE _CLR	PR1_PDSP0_I RAM_ENABLE _CLR	PR1_DRAM1_E NABLE_CLR	PR1_DRAM0_E NABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 15-57. ICSSG_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	PR1_PDSP_TX1_IRAM_E NABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pr1_pdsp_tx1_iram_pend
7	PR1_PDSP_TX0_IRAM_E NABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pr1_pdsp_tx0_iram_pend
6	PR1_RTU1_IRAM_ECC_ ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pr1_rtu1_iram_ecc_pend
5	PR1_RTU0_IRAM_ECC_ ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pr1_rtu0_iram_ecc_pend
4	PR1_RAM_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pr1_ram_pend
3	PR1_PDSP1_IRAM_ENA BLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pr1_pdsp1_iram_pend
2	PR1_PDSP0_IRAM_ENA BLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pr1_pdsp0_iram_pend
1	PR1_DRAM1_ENABLE_C LR	R/W1C	0h	Interrupt Enable Clear Register for pr1_dram1_pend
0	PR1_DRAM0_ENABLE_C LR	R/W1C	0h	Interrupt Enable Clear Register for pr1_dram0_pend

Table 15-58. Register Call Summary for ICSSG_SEC_ENABLE_CLR_REG0

PRU_ICSSG_ECC_AGGR Registers

- [ICSSG_SEC_ENABLE_CLR_REG0 Register \(Offset = C0h\) \[reset = X\]: \[0\]](#)
- [PRU_ICSSG_ECC_AGGR Registers: \[0\]](#)

15.3.8 ICSSG_DED_EOI_REG Register (Offset = 13Ch) [reset = X]

ICSSG_DED_EOI_REG is shown in [Figure 15-19](#) and described in [Table 15-60](#).

Return to [Summary Table](#).

EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 15-59. ICSSG_DED_EOI_REG Instances

Instance	Physical Address
PRU_ICSSG0_ECC_AGGR	0BF0 013Ch
PRU_ICSSG1_ECC_AGGR	0BF0 113Ch

Figure 15-19. ICSSG_DED_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 15-60. ICSSG_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EOI_WR	R/W1S	0h	EOI Register

Table 15-61. Register Call Summary for ICSSG_DED_EOI_REG

PRU_ICSSG_ECC_AGGR Registers

- [ICSSG_DED_EOI_REG Register \(Offset = 13Ch\) \[reset = X\]: \[0\]](#)
- [PRU_ICSSG_ECC_AGGR Registers: \[0\]](#)

15.3.9 ICSSG_DED_STATUS_REG0 Register (Offset = 140h) [reset = X]

ICSSG_DED_STATUS_REG0 is shown in Figure 15-20 and described in Table 15-63.

Return to [Summary Table](#).

Interrupt Status Register 0

Table 15-62. ICSSG_DED_STATUS_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_ECC_AGGR	0BF0 0140h
PRU_ICSSG1_ECC_AGGR	0BF0 1140h

Figure 15-20. ICSSG_DED_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							PR1_PDSP_TX1_IRAM_PEND
R/W-X							R/W1S-0h
7	6	5	4	3	2	1	0
PR1_PDSP_TX0_IRAM_PEND	PR1_RTU1_IRAM_ECC_PEND	PR1_RTU0_IRAM_ECC_PEND	PR1_RAM_PEND	PR1_PDSP1_IRAM_PEND	PR1_PDSP0_IRAM_PEND	PR1_DRAM1_PEND	PR1_DRAM0_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 15-63. ICSSG_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	PR1_PDSP_TX1_IRAM_PEND	R/W1S	0h	Interrupt Pending Status for pr1_pdsp_tx1_iram_pend
7	PR1_PDSP_TX0_IRAM_PEND	R/W1S	0h	Interrupt Pending Status for pr1_pdsp_tx0_iram_pend
6	PR1_RTU1_IRAM_ECC_PEND	R/W1S	0h	Interrupt Pending Status for pr1_rtu1_iram_ecc_pend
5	PR1_RTU0_IRAM_ECC_PEND	R/W1S	0h	Interrupt Pending Status for pr1_rtu0_iram_ecc_pend
4	PR1_RAM_PEND	R/W1S	0h	Interrupt Pending Status for pr1_ram_pend
3	PR1_PDSP1_IRAM_PEND	R/W1S	0h	Interrupt Pending Status for pr1_pdsp1_iram_pend
2	PR1_PDSP0_IRAM_PEND	R/W1S	0h	Interrupt Pending Status for pr1_pdsp0_iram_pend
1	PR1_DRAM1_PEND	R/W1S	0h	Interrupt Pending Status for pr1_dram1_pend
0	PR1_DRAM0_PEND	R/W1S	0h	Interrupt Pending Status for pr1_dram0_pend

Table 15-64. Register Call Summary for ICSSG_DED_STATUS_REG0

PRU_ICSSG_ECC_AGGR Registers

- [ICSSG_DED_STATUS_REG0 Register \(Offset = 140h\) \[reset = X\]: \[0\]](#)
- [PRU_ICSSG_ECC_AGGR Registers: \[0\]](#)

15.3.10 ICSSG_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = X]

ICSSG_DED_ENABLE_SET_REG0 is shown in Figure 15-21 and described in Table 15-66.

Return to [Summary Table](#).

Interrupt Enable Set Register 0

Table 15-65. ICSSG_DED_ENABLE_SET_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_ECC_AGGR	0BF0 0180h
PRU_ICSSG1_ECC_AGGR	0BF0 1180h

Figure 15-21. ICSSG_DED_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							PR1_PDSP_TX1_IRAM_ENABLE_SET
R/W-X							R/W1S-0h
7	6	5	4	3	2	1	0
PR1_PDSP_TX0_IRAM_ENABLE_SET	PR1_RTU1_IRAM_ECC_ENABLE_SET	PR1_RTU0_IRAM_ECC_ENABLE_SET	PR1_RAM_ENABLE_SET	PR1_PDSP1_IRAM_ENABLE_SET	PR1_PDSP0_IRAM_ENABLE_SET	PR1_DRAM1_ENABLE_SET	PR1_DRAM0_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 15-66. ICSSG_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	PR1_PDSP_TX1_IRAM_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pr1_pdsp_tx1_iram_pend
7	PR1_PDSP_TX0_IRAM_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pr1_pdsp_tx0_iram_pend
6	PR1_RTU1_IRAM_ECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pr1_rtu1_iram_ecc_pend
5	PR1_RTU0_IRAM_ECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pr1_rtu0_iram_ecc_pend
4	PR1_RAM_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pr1_ram_pend
3	PR1_PDSP1_IRAM_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pr1_pdsp1_iram_pend
2	PR1_PDSP0_IRAM_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pr1_pdsp0_iram_pend
1	PR1_DRAM1_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pr1_dram1_pend
0	PR1_DRAM0_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pr1_dram0_pend

Table 15-67. Register Call Summary for ICSSG_DED_ENABLE_SET_REG0

PRU_ICSSG_ECC_AGGR Registers

- [PRU_ICSSG_ECC_AGGR Registers: \[0\]](#)
- [ICSSG_DED_ENABLE_SET_REG0 Register \(Offset = 180h\) \[reset = X\]: \[0\]](#)

15.3.11 ICSSG_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = X]

ICSSG_DED_ENABLE_CLR_REG0 is shown in Figure 15-22 and described in Table 15-69.

Return to [Summary Table](#).

Interrupt Enable Clear Register 0

Table 15-68. ICSSG_DED_ENABLE_CLR_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_ECC_AGGR	0BF0 01C0h
PRU_ICSSG1_ECC_AGGR	0BF0 11C0h

Figure 15-22. ICSSG_DED_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							PR1_PDSP_TX1_IRAM_ENABLE_CLR
R/W-X							R/W1C-0h
7	6	5	4	3	2	1	0
PR1_PDSP_TX0_IRAM_ENABLE_CLR	PR1_RTU1_IRAM_ECC_ENABLE_CLR	PR1_RTU0_IRAM_ECC_ENABLE_CLR	PR1_RAM_ENABLE_CLR	PR1_PDSP1_IRAM_ENABLE_CLR	PR1_PDSP0_IRAM_ENABLE_CLR	PR1_DRAM1_ENABLE_CLR	PR1_DRAM0_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 15-69. ICSSG_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	PR1_PDSP_TX1_IRAM_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pr1_pdsp_tx1_iram_pending
7	PR1_PDSP_TX0_IRAM_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pr1_pdsp_tx0_iram_pending
6	PR1_RTU1_IRAM_ECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pr1_rtu1_iram_ecc_pending
5	PR1_RTU0_IRAM_ECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pr1_rtu0_iram_ecc_pending
4	PR1_RAM_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pr1_ram_pending
3	PR1_PDSP1_IRAM_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pr1_pdsp1_iram_pending
2	PR1_PDSP0_IRAM_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pr1_pdsp0_iram_pending
1	PR1_DRAM1_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pr1_dram1_pending
0	PR1_DRAM0_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pr1_dram0_pending

Table 15-70. Register Call Summary for ICSSG_DED_ENABLE_CLR_REG0

PRU_ICSSG_ECC_AGGR Registers

- [ICSSG_DED_ENABLE_CLR_REG0 Register \(Offset = 1C0h\) \[reset = X\]: \[0\]](#)
- [PRU_ICSSG_ECC_AGGR Registers: \[0\]](#)

15.3.12 ICSSG_AGGR_ENABLE_SET Register (Offset = 200h) [reset = X]

ICSSG_AGGR_ENABLE_SET is shown in Figure 15-23 and described in Table 15-72.

Return to [Summary Table](#).

AGGR interrupt enable set Register

Table 15-71. ICSSG_AGGR_ENABLE_SET Instances

Instance	Physical Address
PRU_ICSSG0_ECC_AGGR	0BF0 0200h
PRU_ICSSG1_ECC_AGGR	0BF0 1200h

Figure 15-23. ICSSG_AGGR_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R/W-X						R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 15-72. ICSSG_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	TIMEOUT	R/W1S	0h	interrupt enable set for SVBUS timeout errors
0	PARITY	R/W1S	0h	interrupt enable set for parity errors

Table 15-73. Register Call Summary for ICSSG_AGGR_ENABLE_SET

PRU_ICSSG_ECC_AGGR Registers

- [ICSSG_AGGR_ENABLE_SET Register \(Offset = 200h\) \[reset = X\]: \[0\]](#)
- [PRU_ICSSG_ECC_AGGR Registers: \[0\]](#)

15.3.13 ICSSG_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = X]

ICSSG_AGGR_ENABLE_CLR is shown in Figure 15-24 and described in Table 15-75.

Return to [Summary Table](#).

AGGR interrupt enable clear Register

Table 15-74. ICSSG_AGGR_ENABLE_CLR Instances

Instance	Physical Address
PRU_ICSSG0_ECC_AGGR	0BF0 0204h
PRU_ICSSG1_ECC_AGGR	0BF0 1204h

Figure 15-24. ICSSG_AGGR_ENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R/W-X						R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 15-75. ICSSG_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	TIMEOUT	R/W1C	0h	interrupt enable clear for SVBUS timeout errors
0	PARITY	R/W1C	0h	interrupt enable clear for parity errors

Table 15-76. Register Call Summary for ICSSG_AGGR_ENABLE_CLR

PRU_ICSSG_ECC_AGGR Registers

- [ICSSG_AGGR_ENABLE_CLR Register \(Offset = 204h\) \[reset = X\]: \[0\]](#)
- [PRU_ICSSG_ECC_AGGR Registers: \[0\]](#)

15.3.14 ICSSG_AGGR_STATUS_SET Register (Offset = 208h) [reset = X]

ICSSG_AGGR_STATUS_SET is shown in [Figure 15-25](#) and described in [Table 15-78](#).

Return to [Summary Table](#).

AGGR interrupt status set Register

Table 15-77. ICSSG_AGGR_STATUS_SET Instances

Instance	Physical Address
PRU_ICSSG0_ECC_AGGR	0BF0 0208h
PRU_ICSSG1_ECC_AGGR	0BF0 1208h

Figure 15-25. ICSSG_AGGR_STATUS_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R/W-X				R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-78. ICSSG_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-2	TIMEOUT	R/W	0h	interrupt status set for SVBUS timeout errors
1-0	PARITY	R/W	0h	interrupt status set for parity errors

Table 15-79. Register Call Summary for ICSSG_AGGR_STATUS_SET

PRU_ICSSG_ECC_AGGR Registers

- [ICSSG_AGGR_STATUS_SET Register \(Offset = 208h\) \[reset = X\]: \[0\]](#)
- [PRU_ICSSG_ECC_AGGR Registers: \[0\]](#)

15.3.15 ICSSG_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = X]

ICSSG_AGGR_STATUS_CLR is shown in Figure 15-26 and described in Table 15-81.

Return to [Summary Table](#).

AGGR interrupt status clear Register

Table 15-80. ICSSG_AGGR_STATUS_CLR Instances

Instance	Physical Address
PRU_ICSSG0_ECC_AGGR	0BF0 020Ch
PRU_ICSSG1_ECC_AGGR	0BF0 120Ch

Figure 15-26. ICSSG_AGGR_STATUS_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R/W-X				R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-81. ICSSG_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-2	TIMEOUT	R/W	0h	interrupt status clear for SVBUS timeout errors
1-0	PARITY	R/W	0h	interrupt status clear for parity errors

Table 15-82. Register Call Summary for ICSSG_AGGR_STATUS_CLR

PRU_ICSSG_ECC_AGGR Registers

- [ICSSG_AGGR_STATUS_CLR Register \(Offset = 20Ch\) \[reset = X\]: \[0\]](#)
- [PRU_ICSSG_ECC_AGGR Registers: \[0\]](#)

15.4 PRU_ICSSG_DDRAM Registers

Table 15-84 lists the memory-mapped registers for the PRU_ICSSG_DDRAM0 registers. All register offset addresses not listed in Table 15-84 should be considered as reserved locations and the register contents should not be modified.

Table 15-83. PRU_ICSSG_DDRAM Instances

Instance	Base Address
PRU_ICSSG0_DRAM0_SLV_RAM	0B00 0000h
PRU_ICSSG1_DRAM0_SLV_RAM	0B10 0000h
PRU_ICSSG0_DRAM1_SLV_RAM	0B00 2000h
PRU_ICSSG1_DRAM1_SLV_RAM	0B10 2000h

Table 15-84. PRU_ICSSG_DDRAM Registers

Offset	Acronym	Register Name	PRU_ICSSG0_DRAM0_SLV_RAM Physical Address	PRU_ICSSG1_DRAM0_SLV_RAM Physical Address
0h + formula	ICSSG_DRAM_REG_y	RAM memory word	0B00 0000h + formula	0B10 0000h + formula

Table 15-85. PRU_ICSSG_DDRAM Registers 2

Offset	Acronym	Register Name	PRU_ICSSG0_DRAM1_SLV_RAM Physical Address	PRU_ICSSG1_DRAM1_SLV_RAM Physical Address
0h + formula	ICSSG_DRAM_REG_y	RAM memory word	0B00 2000h + formula	0B10 2000h + formula

15.4.1 ICSSG_DRAM_REG_y Register (Offset = 0h + formula) [reset = 0h]

ICSSG_DRAM_REG_y is shown in [Figure 15-27](#) and described in [Table 15-87](#).

Return to [Summary Table](#).

The RAM memory words provide memory mapped random access data storage.

Offset = 0h + (y * 4h); where y = 0h to 7FFh

Table 15-86. ICSSG_DRAM_REG_y Instances

Instance	Physical Address
PRU_ICSSG0_DRAM0_SLV_RAM	0B00 0000h + formula
PRU_ICSSG0_DRAM1_SLV_RAM	0B00 2000h + formula
PRU_ICSSG1_DRAM0_SLV_RAM	0B10 0000h + formula
PRU_ICSSG1_DRAM1_SLV_RAM	0B10 2000h + formula

Figure 15-27. ICSSG_DRAM_REG_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BYTE3								BYTE2								BYTE1								BYTE0							
R/W-0h								R/W-0h								R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-87. ICSSG_DRAM_REG_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	BYTE3	R/W	0h	This is the MSB (Most Significant Byte)
23-16	BYTE2	R/W	0h	This is the UMB (Upper Middle Byte)
15-8	BYTE1	R/W	0h	This is the LMB (Lower Middle Byte)
7-0	BYTE0	R/W	0h	This is the LSB (Least Significant Byte)

Table 15-88. Register Call Summary for ICSSG_DRAM_REG_y

PRU_ICSSG_DDRAM Registers

- [ICSSG_DRAM_REG_y Register \(Offset = 0h + formula\) \[reset = 0h\]: \[0\]](#)

15.5 PRU_ICSSG_CFG Registers

Table 15-90 lists the memory-mapped registers for the PRU_ICSSG_CFG registers. All register offset addresses not listed in Table 15-90 should be considered as reserved locations and the register contents should not be modified.

Table 15-89. PRU_ICSSG_CFG Instances

Instance	Base Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6000h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6000h

Table 15-90. PRU_ICSSG_CFG Registers

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_CFG_SLV Physical Address	PRU_ICSSG1_PR1_CFG_SLV Physical Address
0h	ICSSG_PID_REG	PID Register	0B02 6000h	0B12 6000h
4h	ICSSG_HWDIS_REG	HW Disable Register	0B02 6004h	0B12 6004h
8h	ICSSG_GPCFG0_REG	GP Configuration 0 Register	0B02 6008h	0B12 6008h
Ch	ICSSG_GPCFG1_REG	GP Configuration 1 Register	0B02 600Ch	0B12 600Ch
10h	ICSSG_CGR_REG	Clock Gating Register	0B02 6010h	0B12 6010h
14h	ICSSG_GPECFG0_REG	GP Enc Configuration 0 Register	0B02 6014h	0B12 6014h
18h	ICSSG_GPECFG1_REG	GP Enc Configuration 1 Register	0B02 6018h	0B12 6018h
2Ch	ICSSG_MII_RT_REG	MII_RT Event Enable Register	0B02 602Ch	0B12 602Ch
30h	ICSSG_IEPCLK_REG	IEP Configuration Register	0B02 6030h	0B12 6030h
34h	ICSSG_SPP_REG	Scratchpad Priority and Shift Register	0B02 6034h	0B12 6034h
3Ch	ICSSG_CORE_SYNC_REG	CoreSync Configuration Register	0B02 603Ch	0B12 603Ch
40h	ICSSG_SA_MX_REG	SA Mux Selection Register	0B02 6040h	0B12 6040h
48h	ICSSG_PRU0_SD_CLK_SEL_REG0	PRU0 FD, ACC and Clock Selection Register 0	0B02 6048h	0B12 6048h
4Ch	ICSSG_PRU0_SD_SAMPLE_SIZE_REG0	PRU0 FD and Over Sample Size Register 0	0B02 604Ch	0B12 604Ch
50h	ICSSG_PRU0_SD_CLK_SEL_REG1	PRU0 FD, ACC and Clock Selection Register 1	0B02 6050h	0B12 6050h
54h	ICSSG_PRU0_SD_SAMPLE_SIZE_REG1	PRU0 FD and Over Sample Size Register 1	0B02 6054h	0B12 6054h
58h	ICSSG_PRU0_SD_CLK_SEL_REG2	PRU0 FD, ACC and Clock Selection Register 2	0B02 6058h	0B12 6058h
5Ch	ICSSG_PRU0_SD_SAMPLE_SIZE_REG2	PRU0 FD and Over Sample Size Register 2	0B02 605Ch	0B12 605Ch
60h	ICSSG_PRU0_SD_CLK_SEL_REG3	PRU0 FD, ACC and Clock Selection Register 3	0B02 6060h	0B12 6060h
64h	ICSSG_PRU0_SD_SAMPLE_SIZE_REG3	PRU0 FD and Over Sample Size Register 3	0B02 6064h	0B12 6064h
68h	ICSSG_PRU0_SD_CLK_SEL_REG4	PRU0 FD, ACC and Clock Selection Register 4	0B02 6068h	0B12 6068h
6Ch	ICSSG_PRU0_SD_SAMPLE_SIZE_REG4	PRU0 FD and Over Sample Size Register 4	0B02 606Ch	0B12 606Ch
70h	ICSSG_PRU0_SD_CLK_SEL_REG5	PRU0 FD, ACC and Clock Selection Register 5	0B02 6070h	0B12 6070h
74h	ICSSG_PRU0_SD_SAMPLE_SIZE_REG5	PRU0 FD and Over Sample Size Register 5	0B02 6074h	0B12 6074h
78h	ICSSG_PRU0_SD_CLK_SEL_REG6	PRU0 FD, ACC and Clock Selection Register 6	0B02 6078h	0B12 6078h

Table 15-90. PRU_ICSSG_CFG Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_CFG_SLV Physical Address	PRU_ICSSG1_PR1_CFG_SLV Physical Address
7Ch	ICSSG_PRU0_SD_SAMPLE_SIZE_REG6	PRU0 FD and Over Sample Size Register 6	0B02 607Ch	0B12 607Ch
80h	ICSSG_PRU0_SD_CLK_SEL_REG7	PRU0 FD, ACC and Clock Selection Register 7	0B02 6080h	0B12 6080h
84h	ICSSG_PRU0_SD_SAMPLE_SIZE_REG7	PRU0 FD and Over Sample Size Register 7	0B02 6084h	0B12 6084h
88h	ICSSG_PRU0_SD_CLK_SEL_REG8	PRU0 FD, ACC and Clock Selection Register 8	0B02 6088h	0B12 6088h
8Ch	ICSSG_PRU0_SD_SAMPLE_SIZE_REG8	PRU0 FD and Over Sample Size Register 8	0B02 608Ch	0B12 608Ch
94h	ICSSG_PRU1_SD_CLK_SEL_REG0	PRU1 FD, ACC and Clock Selection Register 0	0B02 6094h	0B12 6094h
98h	ICSSG_PRU1_SD_SAMPLE_SIZE_REG0	PRU1 FD and Over Sample Size Register 0	0B02 6098h	0B12 6098h
9Ch	ICSSG_PRU1_SD_CLK_SEL_REG1	PRU1 FD, ACC and Clock Selection Register 1	0B02 609Ch	0B12 609Ch
A0h	ICSSG_PRU1_SD_SAMPLE_SIZE_REG1	PRU1 FD and Over Sample Size Register 1	0B02 60A0h	0B12 60A0h
A4h	ICSSG_PRU1_SD_CLK_SEL_REG2	PRU1 FD, ACC and Clock Selection Register 2	0B02 60A4h	0B12 60A4h
A8h	ICSSG_PRU1_SD_SAMPLE_SIZE_REG2	PRU1 FD and Over Sample Size Register 2	0B02 60A8h	0B12 60A8h
ACh	ICSSG_PRU1_SD_CLK_SEL_REG3	PRU1 FD, ACC and Clock Selection Register 3	0B02 60ACh	0B12 60ACh
B0h	ICSSG_PRU1_SD_SAMPLE_SIZE_REG3	PRU1 FD and Over Sample Size Register 3	0B02 60B0h	0B12 60B0h
B4h	ICSSG_PRU1_SD_CLK_SEL_REG4	PRU1 FD, ACC and Clock Selection Register 4	0B02 60B4h	0B12 60B4h
B8h	ICSSG_PRU1_SD_SAMPLE_SIZE_REG4	PRU1 FD and Over Sample Size Register 4	0B02 60B8h	0B12 60B8h
BCh	ICSSG_PRU1_SD_CLK_SEL_REG5	PRU1 FD, ACC and Clock Selection Register 5	0B02 60BCh	0B12 60BCh
C0h	ICSSG_PRU1_SD_SAMPLE_SIZE_REG5	PRU1 FD and Over Sample Size Register 5	0B02 60C0h	0B12 60C0h
C4h	ICSSG_PRU1_SD_CLK_SEL_REG6	PRU1 FD, ACC and Clock Selection Register 6	0B02 60C4h	0B12 60C4h
C8h	ICSSG_PRU1_SD_SAMPLE_SIZE_REG6	PRU1 FD and Over Sample Size Register 6	0B02 60C8h	0B12 60C8h
CCh	ICSSG_PRU1_SD_CLK_SEL_REG7	PRU1 FD, ACC and Clock Selection Register 7	0B02 60CCh	0B12 60CCh
D0h	ICSSG_PRU1_SD_SAMPLE_SIZE_REG7	PRU1 FD and Over Sample Size Register 7	0B02 60D0h	0B12 60D0h
D4h	ICSSG_PRU1_SD_CLK_SEL_REG8	PRU1 FD, ACC and Clock Selection Register 8	0B02 60D4h	0B12 60D4h
D8h	ICSSG_PRU1_SD_SAMPLE_SIZE_REG8	PRU1 FD and Over Sample Size Register 8	0B02 60D8h	0B12 60D8h
E0h	ICSSG_PRU0_ED_RX_CFG_REG	PRU0 ED Receive Global Configuration Register	0B02 60E0h	0B12 60E0h
E4h	ICSSG_PRU0_ED_TX_CFG_REG	PRU0 ED Transmit Global Configuration Register	0B02 60E4h	0B12 60E4h
E8h	ICSSG_PRU0_ED_CH0_CFG0_REG	PRU0 ED Channel 0 Configuration 0 Register	0B02 60E8h	0B12 60E8h
ECh	ICSSG_PRU0_ED_CH0_CFG1_REG	PRU0 ED Channel 0 Configuration 1 Register	0B02 60ECh	0B12 60ECh

Table 15-90. PRU_ICSSG_CFG Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_CFG_SLV Physical Address	PRU_ICSSG1_PR1_CFG_SLV Physical Address
F0h	ICSSG_PRU0_ED_CH1_CFG0_REG	PRU0 ED Channel 1 Configuration 0 Register	0B02 60F0h	0B12 60F0h
F4h	ICSSG_PRU0_ED_CH1_CFG1_REG	PRU0 ED Channel 1 Configuration 1 Register	0B02 60F4h	0B12 60F4h
F8h	ICSSG_PRU0_ED_CH2_CFG0_REG	PRU0 ED Channel 2 Configuration 0 Register	0B02 60F8h	0B12 60F8h
FCh	ICSSG_PRU0_ED_CH2_CFG1_REG	PRU0 ED Channel 2 Configuration 1 Register	0B02 60FCh	0B12 60FCh
100h	ICSSG_PRU1_ED_RX_CFG_REG	PRU1 ED Receive Global Configuration Register	0B02 6100h	0B12 6100h
104h	ICSSG_PRU1_ED_TX_CFG_REG	PRU1 ED Transmit Global Configuration Register	0B02 6104h	0B12 6104h
108h	ICSSG_PRU1_ED_CH0_CFG0_REG	PRU1 ED Channel 0 Configuration 0 Register	0B02 6108h	0B12 6108h
10Ch	ICSSG_PRU1_ED_CH0_CFG1_REG	PRU1 ED Channel 0 Configuration 1 Register	0B02 610Ch	0B12 610Ch
110h	ICSSG_PRU1_ED_CH1_CFG0_REG	PRU1 ED Channel 1 Configuration 0 Register	0B02 6110h	0B12 6110h
114h	ICSSG_PRU1_ED_CH1_CFG1_REG	PRU1 ED Channel 1 Configuration 1 Register	0B02 6114h	0B12 6114h
118h	ICSSG_PRU1_ED_CH2_CFG0_REG	PRU1 ED Channel 2 Configuration 0 Register	0B02 6118h	0B12 6118h
11Ch	ICSSG_PRU1_ED_CH2_CFG1_REG	PRU1 ED Channel 2 Configuration 1 Register	0B02 611Ch	0B12 611Ch
124h	ICSSG_RTU0_POKE_EN0_REG	RTU0 Poke Enable 0 Register	0B02 6124h	0B12 6124h
12Ch	ICSSG_RTU1_POKE_EN0_REG	RTU1 Poke Enable 0 Register	0B02 612Ch	0B12 612Ch
130h	ICSSG_PWM0	PWM0 Trip Configuration Register	0B02 6130h	0B12 6130h
134h	ICSSG_PWM1	PWM1 Trip Configuration Register	0B02 6134h	0B12 6134h
138h	ICSSG_PWM2	PWM2 Trip Configuration Register	0B02 6138h	0B12 6138h
13Ch	ICSSG_PWM3	PWM3 Trip Configuration Register	0B02 613Ch	0B12 613Ch
140h	ICSSG_PWM0_0	PWM0 State Configuration 0 Register	0B02 6140h	0B12 6140h
144h	ICSSG_PWM0_1	PWM0 State Configuration 1 Register	0B02 6144h	0B12 6144h
148h	ICSSG_PWM0_2	PWM0 State Configuration 2 Register	0B02 6148h	0B12 6148h
14Ch	ICSSG_PWM1_0	PWM1 State Configuration 0 Register	0B02 614Ch	0B12 614Ch
150h	ICSSG_PWM1_1	PWM1 State Configuration 1 Register	0B02 6150h	0B12 6150h
154h	ICSSG_PWM1_2	PWM1 State Configuration 2 Register	0B02 6154h	0B12 6154h
158h	ICSSG_PWM2_0	PWM2 State Configuration 0 Register	0B02 6158h	0B12 6158h
15Ch	ICSSG_PWM2_1	PWM2 State Configuration 1 Register	0B02 615Ch	0B12 615Ch
160h	ICSSG_PWM2_2	PWM2 State Configuration 2 Register	0B02 6160h	0B12 6160h
164h	ICSSG_PWM3_0	PWM3 State Configuration 0 Register	0B02 6164h	0B12 6164h
168h	ICSSG_PWM3_1	PWM3 State Configuration 1 Register	0B02 6168h	0B12 6168h

Table 15-90. PRU_ICSSG_CFG Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_CFG_SLV Physical Address	PRU_ICSSG1_PR1_CFG_SLV Physical Address
16Ch	ICSSG_PWM3_2	PWM3 State Configuration 2 Register	0B02 616Ch	0B12 616Ch
170h	ICSSG_SPIN_LOCK0	Spin Lock 0 Register	0B02 6170h	0B12 6170h
174h	ICSSG_SPIN_LOCK1	Spin Lock 1 Register	0B02 6174h	0B12 6174h
178h	ICSSG_PA_STAT_PDSP_CFG0	PA STATS PDSP0 Vector 0 Register	0B02 6178h	0B12 6178h
17Ch	ICSSG_PA_STAT_PDSP_STAT0	PA STATS PDSP0 Status 0 Register	0B02 617Ch	0B12 617Ch
180h	ICSSG_PA_STAT_PDSP_CFG1	PA STATS PDSP0 Vector 1 Register	0B02 6180h	0B12 6180h
184h	ICSSG_PA_STAT_PDSP_STAT1	PA STATS PDSP0 Status 1 Register	0B02 6184h	0B12 6184h
188h	ICSSG_PA_STAT_PDSP_CFG2	PA STATS PDSP0 Vector 2 Register	0B02 6188h	0B12 6188h
18Ch	ICSSG_PA_STAT_PDSP_STAT2	PA STATS PDSP0 Status 2 Register	0B02 618Ch	0B12 618Ch
190h	ICSSG_PA_STAT_PDSP_CFG3	PA STATS PDSP0 Vector 3 Register	0B02 6190h	0B12 6190h
194h	ICSSG_PA_STAT_PDSP_STAT3	PA STATS PDSP0 Status 3 Register	0B02 6194h	0B12 6194h

15.5.1 ICSSG_PID_REG Register (Offset = 0h) [reset = Xh]

ICSSG_PID_REG is shown in [Figure 15-28](#) and described in [Table 15-92](#).

Return to [Summary Table](#).

PID Register.

Table 15-91. ICSSG_PID_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6000h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6000h

Figure 15-28. ICSSG_PID_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MODID															
6B00h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL				REVMJ				CUSTOM				REVMIN			
R-X				R-1h				R-0h				R-X			

LEGEND: R = Read Only; -n = value after reset

Table 15-92. ICSSG_PID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	6B00h	Module ID field. ICSS_G.
15-11	REVRTL	R	0h	RTL revision. 19H in this device.
10-8	REVMJ	R	1h	Major
7-6	CUSTOM	R	0h	Custom
5-0	REVMIN	R	3h	Minor. 0H in this device.

Table 15-93. Register Call Summary for ICSSG_PID_REG

PRU_ICSSG_CFG Registers

- [ICSSG_PID_REG Register \(Offset = 0h\) \[reset = 6B00C900h\]: \[0\]](#)

15.5.2 ICSSG_HWDIS_REG Register (Offset = 4h) [reset = X]

ICSSG_HWDIS_REG is shown in [Figure 15-29](#) and described in [Table 15-95](#).

Return to [Summary Table](#).

HW Disable Register

Table 15-94. ICSSG_HWDIS_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6004h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6004h

Figure 15-29. ICSSG_HWDIS_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								HWDIS							
R-X																								R-X							

LEGEND: R = Read Only; -n = value after reset

Table 15-95. ICSSG_HWDIS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	X	
7-0	HWDIS	R	X	Read the state of the efuse bits which drive pr1_hw_disable[7:0]

Table 15-96. Register Call Summary for ICSSG_HWDIS_REG

PRU_ICSSG_CFG Registers

- [ICSSG_HWDIS_REG Register \(Offset = 4h\) \[reset = X\]: \[0\]](#)

15.5.3 ICSSG_GPCFG0_REG Register (Offset = 8h) [reset = X]

ICSSG_GPCFG0_REG is shown in [Figure 15-30](#) and described in [Table 15-98](#).

Return to [Summary Table](#).

GP Configuration 0 Register

Table 15-97. ICSSG_GPCFG0_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6008h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6008h

Figure 15-30. ICSSG_GPCFG0_REG Register

31	30	29	28	27	26	25	24
RESERVED		PR1_PRU0_GP_MUX_SEL				PRU0_GPO_SH1_SEL	PRU0_GPO_DIV1
R/W-X		R/W-0h				R-0h	R/W-0h
23	22	21	20	19	18	17	16
PRU0_GPO_DIV1				PRU0_GPO_DIV0			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
PRU0_GPO_DIV0	PRU0_GPO_MODE	PRU0_GPI_SB	PRU0_GPI_DIV1				
R/W-0h	R/W-0h	R/W1C-0h	R/W-0h				
7	6	5	4	3	2	1	0
PRU0_GPI_DIV0				PRU0_GPI_CLK_MODE		PRU0_GPI_MODE	
R/W-0h				R/W-0h		R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to clear Bit; -n = value after reset

Table 15-98. ICSSG_GPCFG0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-26	PR1_PRU0_GP_MUX_SEL	R/W	0h	Controls the icss_wrap mux sel 0h = GP selected 1h = EnDAT mode 2h = MII mode 3h = SD mode
25	PRU0_GPO_SH1_SEL	R	0h	This defines which shadow register is currently getting used for GPO shifting. 0h = gpo_sh0 is selected 1h = gpo_sh1 is selected
24-20	PRU0_GPO_DIV1	R/W	0h	Divisor value , divide by PRU0_GPO_DIV1 + 1 0h = div 1.0 1h = div 1.5 2h = div 2.0 .. 1Eh = div 16.0 1Fh = reserved

Table 15-98. ICSSG_GPCFG0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-15	PRU0_GPO_DIV0	R/W	0h	Divisor value , divide by PRU0_GPO_DIV0 + 1 0h = div 1.0 1h = div 1.5 2h = div 2.0 .. 1Eh = div 16.0 1Fh = reserved
14	PRU0_GPO_MODE	R/W	0h	0h = Parallel output mode 1h = Serial output mode, pru<n>_r30[31] enables shift pru<n>r30[0] is shift data out pru<n>r30[1] is shift clock
13	PRU0_GPI_SB	R/W1C	0h	PRU0_GPI_SB set when first capture on 1 on r31_status[0] r31_status[29] == PRU0_GPI_SB Read 1 Start Bit event occurred Read 0 Start Bit event has not occurred Write 1 Will clear PRU0_GPI_SB, 28 bit shift register, and shift counter Write 0 No Effect
12-8	PRU0_GPI_DIV1	R/W	0h	Divisor value , divide by PRU0_GPI_DIV1 + 1 0h = div 1.0 1h = div 1.5 2h = div 2.0 .. 1Eh = div 16.0 1Fh = reserved
7-3	PRU0_GPI_DIV0	R/W	0h	Divisor value , divide by PRU0_GPI_DIV0 + 1 0h = div 1.0 1h = div 1.5 2h = div 2.0 .. 1Eh = div 16.0 1Fh = reserved
2	PRU0_GPI_CLK_MODE	R/W	0h	Parallel 16-bit capture mode clock edge 0h = Use the positive edge of pru<n>_r31_status[16] 1h = Use the negative edge of pru<n>_r31_status[16]
1-0	PRU0_GPI_MODE	R/W	0h	0h = Direct connect of pru<n>_r31_status[29:0] 1h = Parallel 16-bit capture mode. pru<n>_r31_status [15:0] is captured using pru<n>_r31_status [16] 2h = 29-bit shift. pru<n>_r31_status[0] -> r31_status[0] -> r31_status[1] -> r_status[28] -> bit bucket 3h = mii_rt mode. Selects mii_rt pru0 bus

Table 15-99. Register Call Summary for ICSSG_GPCFG0_REG

PRU_ICSSG_CFG Registers
ICSSG_GPCFG0_REG Register (Offset = 8h) [reset = X]: [0]
PRU_ICSSG Top Level Resources Functional Description
Module Clock Configurations at PRU_ICSSG Top Level: [0] [1] [2] [3] [4]
PRU_ICSSG PRU Cores
General-Purpose Inputs (R31): Enhanced PRU GP Module: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [18] [20] [21] [22] [23] [24] [25] [26] [27] [28]

Table 15-99. Register Call Summary for ICSSG_GPCFG0_REG (continued)

PRU_ICSSG Environment

- [PRU_ICSSG Internal Pinmux: \[0\] \[1\]](#)

15.5.4 ICSSG_GPCFG1_REG Register (Offset = Ch) [reset = X]

ICSSG_GPCFG1_REG is shown in [Figure 15-31](#) and described in [Table 15-101](#).

Return to [Summary Table](#).

GP Configuration 1 Register

Table 15-100. ICSSG_GPCFG1_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 600Ch
PRU_ICSSG1_PR1_CFG_SLV	0B12 600Ch

Figure 15-31. ICSSG_GPCFG1_REG Register

31	30	29	28	27	26	25	24
RESERVED		PR1_PRU1_GP_MUX_SEL				PRU1_GPO_SH1_SEL	PRU1_GPO_DIV1
R/W-X		R/W-0h				R-0h	R/W-0h
23	22	21	20	19	18	17	16
PRU1_GPO_DIV1				PRU1_GPO_DIV0			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
PRU1_GPO_DIV0	PRU1_GPO_MODE	PRU1_GPI_SB	PRU1_GPI_DIV1				
R/W-0h	R/W-0h	R/W1C-0h	R/W-0h				
7	6	5	4	3	2	1	0
PRU1_GPI_DIV0				PRU1_GPI_CLK_MODE	PRU1_GPI_MODE		
R/W-0h				R/W-0h	R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to clear Bit; -n = value after reset

Table 15-101. ICSSG_GPCFG1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-26	PR1_PRU1_GP_MUX_SEL	R/W	0h	Controls the icss_wrap mux sel 0h = GP selected 1h = EnDAT mode 2h = MII mode 3h = SD mode
25	PRU1_GPO_SH1_SEL	R	0h	This defines which shadow register is currently getting used for GPO shifting. 0h = gpo_sh0 is selected 1h = gpo_sh1 is selected
24-20	PRU1_GPO_DIV1	R/W	0h	Divisor value , divide by PRU1_GPO_DIV1 + 1 0h = div 1.0 1h = div 1.5 2h = div 2.0 .. 1Eh = div 16.0 1Fh = reserved

Table 15-101. ICSSG_GPCFG1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-15	PRU1_GPO_DIV0	R/W	0h	Divisor value , divide by PRU1_GPO_DIV0 + 1 0h = div 1.0 1h = div 1.5 2h = div 2.0 .. 1Eh = div 16.0 1Fh = reserved
14	PRU1_GPO_MODE	R/W	0h	0hh = Parallel output mode 0x1h = Serial output mode, pru<n>_r30[31] enables shift pru<n>_r30[0] is shift data out pru<n>_r30[1] is shift clock
13	PRU1_GPI_SB	R/W1C	0h	PRU1_GPI_SB set when first capture on 1 on r31_status[0] r31_status[29] == PRU1_GPI_SB Read 1 Start Bit event occurred Read 0 Start Bit event has not occurred Write 1 Will clear PRU1_GPI_SB, 28 bit shift register, and shift counter Write 0 No Effect
12-8	PRU1_GPI_DIV1	R/W	0h	Divisor value , divide by PRU1_GPI_DIV1 + 1 0h = div 1.0 1h = div 1.5 2h = div 2.0 .. 1Eh = div 16.0 1Fh = reserved
7-3	PRU1_GPI_DIV0	R/W	0h	Divisor value , divide by PRU1_GPI_DIV0 + 1 0h = div 1.0 1h = div 1.5 2h = div 2.0 .. 1Eh = div 16.0 1Fh = reserved
2	PRU1_GPI_CLK_MODE	R/W	0h	Parallel 16-bit capture mode clock edge 0h = Use the positive edge of pru<n>_r31_status[16] 0x1h = Use the negative edge of pru<n>_r31_status[16]
1-0	PRU1_GPI_MODE	R/W	0h	0h = Direct connect of pru<n>_r31_status[29:0] 1h = Parallel 16-bit capture mode. pru<n>_r31_status [15:0] is captured using pru<n>_r31_status [16] 2h = 29-bit shift. pru<n>_r31_status[0] -> r31_status[0]->r31_status[1]...-> r_status[28] -> bit bucket 3h = mii_rt mode. Selects mii_rt pru1 bus

Table 15-102. Register Call Summary for ICSSG_GPCFG1_REG

PRU_ICSSG_CFG Registers
ICSSG_GPCFG1_REG Register (Offset = Ch) [reset = X]: [0]
PRU_ICSSG Top Level Resources Functional Description
Module Clock Configurations at PRU_ICSSG Top Level: [0] [1] [2] [3] [4]
PRU_ICSSG Environment
PRU_ICSSG Internal Pinmux: [0] [1]

15.5.5 ICSSG_CGR_REG Register (Offset = 10h) [reset = X]

ICSSG_CGR_REG is shown in [Figure 15-32](#) and described in [Table 15-104](#).

Return to [Summary Table](#).

Clock Gating Register

Table 15-103. ICSSG_CGR_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6010h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6010h

Figure 15-32. ICSSG_CGR_REG Register

31	30	29	28	27	26	25	24
ICSS_STOP_A CK	ICSS_STOP_R EQ	ICSS_PWR_ID LE	RESERVED				
R/W-1h	R-0h	R/W-1h	R/W-X				
23	22	21	20	19	18	17	16
RESERVED						IEP_CLK_EN	IEP_CLK_STO P_ACK
R/W-X						R/W-1h	R-0h
15	14	13	12	11	10	9	8
IEP_CLK_STO P_REQ	ECAP_CLK_EN	ECAP_CLK_ST OP_ACK	ECAP_CLK_ST OP_REQ	UART_CLK_EN	UART_CLK_ST OP_ACK	UART_CLK_ST OP_REQ	INTC_CLK_EN
R/W-0h	R/W-1h	R-0h	R/W-0h	R/W-1h	R-0h	R/W-0h	R/W-1h
7	6	5	4	3	2	1	0
INTC_CLK_ST OP_ACK	INTC_CLK_ST OP_REQ	RESERVED					
R-0h	R/W-0h	R/W-X					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-104. ICSSG_CGR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ICSS_STOP_ACK	R/W	1h	ICSS 0h = Not Ready to Gate Clock 1h = Ready to Gate Clock
30	ICSS_STOP_REQ	R	0h	ICSS 0h = No Gate Clock Request 1h = Gate Clock Request
29	ICSS_PWR_IDLE	R/W	1h	ICSS 0h = Not Idle 1h = Idle
28-18	RESERVED	R/W	X	
17	IEP_CLK_EN	R/W	1h	IEP 0h = Disable Clock 1h = Enable Clock
16	IEP_CLK_STOP_ACK	R	0h	IEP 0h = Not Ready to Gate Clock 1h = Ready to Gate Clock
15	IEP_CLK_STOP_REQ	R/W	0h	IEP 0h = do not request to stop clock 1h = request to stop clock

Table 15-104. ICSSG_CGR_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	ECAP_CLK_EN	R/W	1h	ECAP 0h = Disable Clock 1h = Enable Clock
13	ECAP_CLK_STOP_ACK	R	0h	ECAP 0h = Not Ready to Gate Clock 1h = Ready to Gate Clock
12	ECAP_CLK_STOP_REQ	R/W	0h	ECAP 0h = do not request to stop clock 1h = request to stop clock
11	UART_CLK_EN	R/W	1h	UART 0h = Disable Clock 1h = Enable Clock
10	UART_CLK_STOP_ACK	R	0h	UART 0h = Not Ready to Gate Clock 1h = Ready to Gate Clock
9	UART_CLK_STOP_REQ	R/W	0h	UART 0h = do not request to stop clock 1h = request to stop clock
8	INTC_CLK_EN	R/W	1h	INTC 0h = Disable Clock 1h = Enable Clock
7	INTC_CLK_STOP_ACK	R	0h	INTC 0h = Not Ready to Gate Clock 1h = Ready to Gate Clock
6	INTC_CLK_STOP_REQ	R/W	0h	INTC 0h = do not request to stop clock 1h = request to stop clock
5-0	RESERVED	R/W	X	

Table 15-105. Register Call Summary for ICSSG_CGR_REG

PRU_ICSSG_CFG Registers
ICSSG_CGR_REG Register (Offset = 10h) [reset = X]: [0]
PRU_ICSSG Top Level Resources Functional Description
PRU_ICSSG Power and Clock Management: [0] PRU_ICSSG Idle State: [0] [1] [2]

15.5.6 ICSSG_GPECFG0_REG Register (Offset = 14h) [reset = X]

ICSSG_GPECFG0_REG is shown in Figure 15-33 and described in Table 15-107.

Return to [Summary Table](#).

GP Enc Configuration 0 Register

Table 15-106. ICSSG_GPECFG0_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6014h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6014h

Figure 15-33. ICSSG_GPECFG0_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						PRU0_GPO_S HIFT_CLK_DO NE	PRU0_GPO_S HIFT_CLK_HI G
R/W-X						R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
PRU0_GPO_SHIFT_CNT							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED	PRU0_GPO_S HIFT_GP_EN	PRU0_GPO_S HIFT_CLK_FR EE	PRU0_GPO_S HIFT_SWAP	RESERVED		PRU0_GPI_SHI FT_EN	PRU0_GPI_SB _P
R/W-X	R/W-0h	R/W-1h	R/W-0h	R/W-X		R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-107. ICSSG_GPECFG0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17	PRU0_GPO_SHIFT_CLK_DONE	R/W	0h	Shift Clock Done is active when PRU0_GPO_SHIFT_CNT is none zero 0h = Shift Bit Count has not expired 1h = Set when Shift Bit Count has expired Write 1 to clear. This is only valid when PRU0/1_GPO_SHIFT_CLK_FREE is not set
16	PRU0_GPO_SHIFT_CLK_HIGH	R/W	0h	Shift Clock Stop High 0h = Stop Low, if Stop is enabled 1h = Stop High, if Stop is enabled This is only active when PRU0/1_GPO_SHIFT_CLK_FREE is not set Also, you must define PRU0/1_GPO_SHIFT_CNT Note: Software can only update once during initial configuration

Table 15-107. ICSSG_GPECFG0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-8	PRU0_GPO_SHIFT_CNT	R/W	0h	Shift Bit Count 0h – 0x3h = Reserved PRU0_GPO_SHIFT_CNT determine how many bits to shift out. After the count is reached it will stop shifting , the last bit will remain persistent. 0x4h = shift 4 bits 0x5h = shift 5 bits 0xff = shift 255 bits This is only active when PRU0/1_GPO_SHIFT_CLK_FREE is not set Note: first new shift data is before the first clock edge. Due to this fact, the number of shift_clk is one minus PRU0/1_GPO_SHIFT_CNT
7	RESERVED	R/W	X	
6	PRU0_GPO_SHIFT_GP_EN	R/W	0h	Enable pru<n>r30[15:2] control during shift out mode 0h = direction connection pru<n>r30[15:2] is controlled by r30[15:2] 1h = shadow connection pru<n>r30[15:2] is controlled by r30_shadow[15:2] Note: r30_shadow[15:2] is updated by r30[15:2] when r30[28] is high
5	PRU0_GPO_SHIFT_CLK_FREE	R/W	1h	Free Running Clock Mode This controls the behavior of the Shift Clock Out 0h = Shift Clock Out only active when bits are shifted out Default state of Shift Clock Out is low before and after shift (Shift is enabled only when shift_enable is TRUE and PRU0_GPO_SHIFT_CNT has not expired 1h = Shift Clock Out Free running The clock will start and remain active independent of shifting out new data When shift_enable is de-asserted and shift data out is completed, data out will go low
4	PRU0_GPO_SHIFT_SWAP	R/W	0h	0h = No Swap The shadow copy gets loaded with R30[15:0] 1h = Swap The shadow copy gets loaded with R30[0:15]
3-2	RESERVED	R/W	X	
1	PRU0_GPI_SHIFT_EN	R/W	1h	GPI Shift In Enable 0h = disable This will freeze the current shift in process This will also disable the looking for a SB if SB event has not occurred 1h = enable
0	PRU0_GPI_SB_P	R/W	1h	GPI Shift In Start Bit Polarity 0h = Active Low SB is set on the first “0” seen 1h = Active High SB is set on the first “1” seen

Table 15-108. Register Call Summary for ICSSG_GPECFG0_REG

PRU_ICSSG_CFG Registers

- [ICSSG_GPECFG0_REG Register \(Offset = 14h\) \[reset = X\]: \[0\]](#)

Table 15-108. Register Call Summary for ICSSG_GPECFG0_REG (continued)

PRU_ICSSG PRU Cores

- [General-Purpose Inputs \(R31\): Enhanced PRU GP Module: \[0\] \[1\] \[2\] \[3\] \[4\] \[5\] \[6\] \[7\] \[8\] \[9\] \[10\] \[11\] \[12\] \[13\] \[14\] \[15\]](#)

15.5.7 ICSSG_GPECFG1_REG Register (Offset = 18h) [reset = X]

ICSSG_GPECFG1_REG is shown in Figure 15-34 and described in Table 15-110.

Return to [Summary Table](#).

GP Enc Configuration 1 Register

Table 15-109. ICSSG_GPECFG1_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6018h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6018h

Figure 15-34. ICSSG_GPECFG1_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						PRU1_GPO_S HIFT_CLK_DO NE	PRU1_GPO_S HIFT_CLK_HI G
R/W-X						R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
PRU1_GPO_SHIFT_CNT							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED	PRU1_GPO_S HIFT_GP_EN	PRU1_GPO_S HIFT_CLK_FR EE	PRU1_GPO_S HIFT_SWAP	RESERVED		PRU1_GPI_SHI FT_EN	PRU1_GPI_SB _P
R/W-X	R/W-0h	R/W-1h	R/W-0h	R/W-X		R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-110. ICSSG_GPECFG1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17	PRU1_GPO_SHIFT_CLK_DONE	R/W	0h	Shift Clock Done is active when PRU1_GPO_SHIFT_CNT is none zero 0h = Shift Bit Count has not expired 1h = Set when Shift Bit Count has expired Write 1 to clear This is only valid when PRU0/1_GPO_SHIFT_CLK_FREE is not set
16	PRU1_GPO_SHIFT_CLK_HIGH	R/W	0h	Shift Clock Stop High 0h = Stop Low, if Stop is enabled 1h = Stop High, if Stop is enabled This is only valid when PRU0/1_GPO_SHIFT_CLK_FREE is not set Also, you must define PRU0/1_GPO_SHIFT_CNT Note: Software can only update once during initial configuration

Table 15-110. ICSSG_GPECFG1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-8	PRU1_GPO_SHIFT_CNT	R/W	0h	Shift Bit Count 0h – 3h = Reserved PRU1_GPO_SHIFT_CNT determine how many bits to shift out. After the count is reached it will stop shifting , the last bit will remain presistant. 4h = shift 4 bits 5h = shift 5 bits ffh = shift 255 bits This is only active when PRU0/1_GPO_SHIFT_CLK_FREE is not set Note: first new shift data is before the first clock edge Do to this fact, the number of shift_clk is one minus PRU0/1_GPO_SHIFT_CNT
7	RESERVED	R/W	X	
6	PRU1_GPO_SHIFT_GP_EN	R/W	0h	Enable pru<n>r30[15:2] control during shift out mode 0h = direction connection pru<n>r30[15:2] is controlled by r30[15:2] 1h = shadow connection pru<n>r30[15:2] is controlled by r30_shadow[15:2] Note: r30_shadow[15:2] is updated by r30[15:2] when r30[28] is high
5	PRU1_GPO_SHIFT_CLK_FREE	R/W	1h	Free Running Clock Mode This controls the behavior of the Shift Clock Out 0h = Shift Clock Out only active when bits are shifted out Default state of Shift Clock Out is low before and after shift 1h = Shift Clock Out Free running The clock will start and remain active independent of shifting out new data
4	PRU1_GPO_SHIFT_SWAP	R/W	0h	0h = No Swap The shadow copy gets loaded with R30[15:0] 1h = Swap The shadow copy gets loaded with R30[0:15]
3-2	RESERVED	R/W	X	
1	PRU1_GPI_SHIFT_EN	R/W	1h	GPI Shift In Enable 0h = disable This will freeze the current shift in process This will also disable the looking for a SB if SB event has not occurred 1h = enable
0	PRU1_GPI_SB_P	R/W	1h	GPI Shift In Start Bit Polarity 0h = Active Low SB is set on the first “0” seen 1h = Active High SB is set on the first “1” seen

Table 15-111. Register Call Summary for ICSSG_GPECFG1_REG

PRU_ICSSG_CFG Registers

- [ICSSG_GPECFG1_REG Register \(Offset = 18h\) \[reset = X\]: \[0\]](#)

15.5.8 ICSSG_MII_RT_REG Register (Offset = 2Ch) [reset = X]

ICSSG_MII_RT_REG is shown in [Figure 15-35](#) and described in [Table 15-113](#).

Return to [Summary Table](#).

MII_RT Event Enable Register

Table 15-112. ICSSG_MII_RT_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 602Ch
PRU_ICSSG1_PR1_CFG_SLV	0B12 602Ch

Figure 15-35. ICSSG_MII_RT_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							MII_RT_EVENT_EN
R/W-X							R/W-1h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-113. ICSSG_MII_RT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	MII_RT_EVENT_EN	R/W	1h	Enables the MII_RT Events to the INTC 0h = disabled Use external events 1h = enabled Use MII_RT events

Table 15-114. Register Call Summary for ICSSG_MII_RT_REG

PRU_ICSSG_CFG Registers
• ICSSG_MII_RT_REG Register (Offset = 2Ch) [reset = X]: [0]
PRU_ICSSG Top Level Resources Functional Description

15.5.9 ICSSG_IEPCLK_REG Register (Offset = 30h) [reset = X]

ICSSG_IEPCLK_REG is shown in [Figure 15-36](#) and described in [Table 15-116](#).

Return to [Summary Table](#).

IEP Configuration Register

Table 15-115. ICSSG_IEPCLK_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6030h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6030h

Figure 15-36. ICSSG_IEPCLK_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						IEP1_SLV_EN	IEP_OCP_CLK_EN
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-116. ICSSG_IEPCLK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	IEP1_SLV_EN	R/W	0h	IEP1 Controller Counter Target enable 0h = disabled 1h = enabled When Enabled IEP1 counter[63:0] is from IEP0 during 64-bit mode IEP1 counter[31:0] is from IEP0 during 32-bit mode
0	IEP_OCP_CLK_EN	R/W	0h	Defines the source of the IEP CLK 0h = iep_clk is the source Async Mode 1h = ICSSGn_CORE_CLK is the source Sync Mode When this is selected the async IEP bridge is bypassed No transaction active when this bit get SET It can only get CLR by a HW reset Note: This means all PRU-ICSSG IOs which use internal IEP clock can use ether internal core clock or external IEP clock.

Table 15-117. Register Call Summary for ICSSG_IEPCLK_REG

PRU_ICSSG_CFG Registers

- [ICSSG_IEPCLK_REG Register \(Offset = 30h\) \[reset = X\]: \[0\]](#)

Table 15-117. Register Call Summary for ICSSG_IEPCLK_REG (continued)

PRU_ICSSG Top Level Resources Functional Description
PRU_ICSSG CORE Clock Generation: [0]
PRU_ICSSG IEP
PRU_ICSSG IEP Clock Generation: [0] [1] PRU_ICSSG IEP Functional Description: [0]

15.5.10 ICSSG_SPP_REG Register (Offset = 34h) [reset = X]

ICSSG_SPP_REG is shown in Figure 15-37 and described in Table 15-119.

Return to [Summary Table](#).

Scratchpad Priority and Shift Register

Table 15-118. ICSSG_SPP_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6034h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6034h

Figure 15-37. ICSSG_SPP_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				RTU_XFR_SHI FT_EN	XFR_BYTE_SH IFT_EN	XFR_SHIFT_E N	PRU1_PAD_HP _EN
R/W-X				R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-119. ICSSG_SPP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3	RTU_XFR_SHIFT_EN	R/W	0h	Shift enable using R0[4:0] to define the number of 32-bit offset for XIN and XOUT operations. 0h = disabled 1h = enabled When enabled, R0[4:0] (internal to RTU) defines the number of 32-bits the XIN and XOUT operation to the scratch pad bank. R0[4:0] = 2 XIN/XOUT of R4 will read/write bank<n>.R6 Wrap is supported R0[4:0] = 4 XIN/XOUT of R18:29 will read/write bank<n>.R22:R3
2	XFR_BYTE_SHIFT_EN	R/W	0h	Shift enable using R0[6:0] to define the number of 8-bit offset for XIN and XOUT operations. 0h = disabled 1h = enabled When enabled, R0[6:0] (internal to PRU/RTU) defines the number of 8-bits the XIN and XOUT operation to the scratch pad bank.

Table 15-119. ICSSG_SPP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	XFR_SHIFT_EN	R/W	0h	Shift enable using R0[4:0] to define the number of 32-bit offset for XIN and XOUT operations. 0h = disabled 1h = enabled When enabled, R0[4:0] (internal to PRU) defines the number of 32-bits the XIN and XOUT operation to the scratch pad bank. R0[4:0] = 2 XIN/XOUT of R4 will read/write bank<n>.R6 Wrap is supported R0[4:0] = 4 XIN/XOUT of R18:29 will read/write bank<n>.R22:R3
0	PRU1_PAD_HP_EN	R/W	0h	Reserved

Table 15-120. Register Call Summary for ICSSG_SPP_REG

PRU_ICSSG_CFG Registers
ICSSG_SPP_REG Register (Offset = 34h) [reset = X]: [0]
PRU_ICSSG Broadside Accelerators
PRU0 /1 Scratch Pad Operations: [0] [1]
PRU_ICSSG Top Level Resources Functional Description
Other PRU_ICSSG Module Functional Registers at Subsystem Level: [0]

15.5.11 ICSSG_CORE_SYNC_REG Register (Offset = 3Ch) [reset = X]

ICSSG_CORE_SYNC_REG is shown in [Figure 15-38](#) and described in [Table 15-122](#).

Return to [Summary Table](#).

CoreSync Configuration Register.

Table 15-121. ICSSG_CORE_SYNC_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 603Ch
PRU_ICSSG1_PR1_CFG_SLV	0B12 603Ch

Figure 15-38. ICSSG_CORE_SYNC_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							CORE_VBUSB_SYNC_EN
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-122. ICSSG_CORE_SYNC_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	CORE_VBUSB_SYNC_EN	R/W	0h	Defines the source of the internal CORE CLK 0h = ICSSGn_CORE_CLK is the source Async Mode 1h = ICSSGn_ICLK is the source (Sync Mode) When this is selected the async vbusp controller bridge is bypassed No transaction active when this bit get SET It can only get CLR by a HW reset The user should enable to get the lowest latency and high speed, since ICSSGn_ICLK should be at 250 MHz Note: This means all PRU_ICSSG IOs which use internal core clock (CORE_CLK) can use ether external core clock or external ICSSGn_ICLK.

Table 15-123. Register Call Summary for ICSSG_CORE_SYNC_REG

PRU_ICSSG_CFG Registers
ICSSG_CORE_SYNC_REG Register (Offset = 3Ch) [reset = X]: [0]
PRU_ICSSG Top Level Resources Functional Description
PRU_ICSSG CORE Clock Generation: [0]

15.5.12 ICSSG_SA_MX_REG Register (Offset = 40h) [reset = X]

ICSSG_SA_MX_REG is shown in Figure 15-39 and described in Table 15-125.

Return to [Summary Table](#).

SA Mux Selection Register.

Table 15-124. ICSSG_SA_MX_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6040h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6040h

Figure 15-39. ICSSG_SA_MX_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED				PWM3_REMAP_EN		PWM0_REMAP_EN	
R/W-X				R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
SA_MUX_SEL							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-125. ICSSG_SA_MX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	X	
16-12	RESERVED	R	X	
11-10	PWM3_REMAP_EN	R/W	0h	If enabled, ICSSG Host interrupt 7 (PRU_ICSSGn_PR1_HOST_INTR_REQ_7) now controls pwm3_sync_in Only PRU_ICSSG0 controls the remap 0h = pwm_in_pwm3_sync_in_intc_h7 = pwm3_sync_in(no remap) 1h = pwm_in_pwm3_sync_in_intc_h7 = pr0_host_intr7_intr_pend (PRU_ICSSG0) 2h = pwm_in_pwm3_sync_in_intc_h7 = pr1_host_intr7_intr_pend (PRU_ICSSG1) 3h = Reserved
9-8	PWM0_REMAP_EN	R/W	0h	If enabled, ICSSG Host interrupt 6 (PRU_ICSSGn_PR1_HOST_INTR_REQ_6) now controls pwm0_sync_in Only PRU_ICSSG0 controls the remap 0h = pwm_in_pwm0_sync_in_intc_h6 = pwm_in_pwm0_sync_in (no remap) 1h = pwm_in_pwm0_sync_in_intc_h6 = pr0_host_intr6_intr_pend (PRU_ICSSG0) 2h = pwm_in_pwm0_sync_in_intc_h6 = pr1_host_intr6_intr_pend (PRU_ICSSG1) 3h = Reserved

Table 15-125. ICSSG_SA_MX_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	Reserved
6-0	RESERVED	R/W	0h	Reserved

Table 15-126. Register Call Summary for ICSSG_SA_MX_REG

PRU_ICSSG_CFG Registers

- [ICSSG_SA_MX_REG Register \(Offset = 40h\) \[reset = X\]: \[0\]](#)

15.5.13 ICSSG_PRU0_SD_CLK_SEL_REG0 Register (Offset = 48h) [reset = X]

ICSSG_PRU0_SD_CLK_SEL_REG0 is shown in [Figure 15-40](#) and described in [Table 15-128](#).

Return to [Summary Table](#).

PRU0 FD, ACC and Clock Selection Register 0.

**Table 15-127. ICSSG_PRU0_SD_CLK_SEL_REG0
Instances**

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6048h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6048h

Figure 15-40. ICSSG_PRU0_SD_CLK_SEL_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED	PRU0_FD_ZERO_MAX_0	PRU0_FD_ZERO_MAX_LIMIT_0				PRU0_FD_ZERO_MIN_0	
R/W-X	R/W-0h	R/W-0h				R/W-0h	
15	14	13	12	11	10	9	8
PRU0_FD_ZERO_MIN_LIMIT_0					RESERVED		
R/W-0h					R/W-X		
7	6	5	4	3	2	1	0
RESERVED		PRU0_SD_ACC_SEL0		RESERVED	PRU0_SD_CLK_INV0	PRU0_SD_CLK_SEL0	
R/W-X		R/W-0h		R/W-X	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-128. ICSSG_PRU0_SD_CLK_SEL_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU0_FD_ZERO_MAX_0	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ZERO_MAX_LIMIT_0	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU0_FD_ZERO_MIN_0	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-128. ICSSG_PRU0_SD_CLK_SEL_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU0_FD_ZERO_MIN_LI MIT_0	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU0_SD_ACC_SEL0	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU0_SD_CLK_INV0	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU0_SD_CLK_SEL0	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1h = pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

Table 15-129. Register Call Summary for ICSSG_PRU0_SD_CLK_SEL_REG0

PRU_ICSSG_CFG Registers

- [ICSSG_PRU0_SD_CLK_SEL_REG0 Register \(Offset = 48h\) \[reset = X\]: \[0\]](#)

15.5.14 ICSSG_PRU0_SD_SAMPLE_SIZE_REG0 Register (Offset = 4Ch) [reset = X]

ICSSG_PRU0_SD_SAMPLE_SIZE_REG0 is shown in [Figure 15-41](#) and described in [Table 15-131](#).

Return to [Summary Table](#).

PRU0 FD and Over Sample Size Register 0.

Table 15-130.
ICSSG_PRU0_SD_SAMPLE_SIZE_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 604Ch
PRU_ICSSG1_PR1_CFG_SLV	0B12 604Ch

Figure 15-41. ICSSG_PRU0_SD_SAMPLE_SIZE_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRU0_FD_EN_0	PRU0_FD_ON_E_MAX_0	PRU0_FD_ONE_MAX_LIMIT_0				PRU0_FD_ON_E_MIN_0	
R/W-0h	R/W-0h	R/W-0h				R/W-0h	
15	14	13	12	11	10	9	8
PRU0_FD_ONE_MIN_LIMIT_0				PRU0_FD_WINDOW_SIZE_0			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
PRU0_SD_SAMPLE_SIZE0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-131. ICSSG_PRU0_SD_SAMPLE_SIZE_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU0_FD_EN_0	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU0_FD_ONE_MAX_0	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ONE_MAX_LIMIT_0	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU0_FD_ONE_MIN_0	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-131. ICSSG_PRU0_SD_SAMPLE_SIZE_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU0_FD_ONE_MIN_LIMIT_0	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU0_FD_WINDOW_SIZE_0	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU0_SD_SAMPLE_SIZE_0	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) Note: the 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3hh, then the third clock after first 1 is detected, the VAL will get set.

Table 15-132. Register Call Summary for ICSSG_PRU0_SD_SAMPLE_SIZE_REG0

PRU_ICSSG_CFG Registers

- [ICSSG_PRU0_SD_SAMPLE_SIZE_REG0 Register \(Offset = 4Ch\) \[reset = X\]: \[0\]](#)

15.5.15 ICSSG_PRU0_SD_CLK_SEL_REG1 Register (Offset = 50h) [reset = X]

ICSSG_PRU0_SD_CLK_SEL_REG1 is shown in [Figure 15-42](#) and described in [Table 15-134](#).

Return to [Summary Table](#).

PRU0 FD, ACC and Clock Selection Register 1.

**Table 15-133. ICSSG_PRU0_SD_CLK_SEL_REG1
Instances**

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6050h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6050h

Figure 15-42. ICSSG_PRU0_SD_CLK_SEL_REG1 Register

31		30		29		28		27		26		25		24	
RESERVED															
R/W-X															
23		22		21		20		19		18		17		16	
RESERVED		PRU0_FD_ZERO_MAX_1		PRU0_FD_ZERO_MAX_LIMIT_1										PRU0_FD_ZERO_MIN_1	
R/W-X		R/W-0h		R/W-0h										R/W-0h	
15		14		13		12		11		10		9		8	
PRU0_FD_ZERO_MIN_LIMIT_1										RESERVED					
R/W-0h										R/W-X					
7		6		5		4		3		2		1		0	
RESERVED				PRU0_SD_ACC_SEL1				RESERVED		PRU0_SD_CLK_INV1		PRU0_SD_CLK_SEL1			
R/W-X				R/W-0h				R/W-X		R/W-0h		R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-134. ICSSG_PRU0_SD_CLK_SEL_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU0_FD_ZERO_MAX_1	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ZERO_MAX_LIMIT_1	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU0_FD_ZERO_MIN_1	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-134. ICSSG_PRU0_SD_CLK_SEL_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU0_FD_ZERO_MIN_LI MIT_1	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU0_SD_ACC_SEL1	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU0_SD_CLK_INV1	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU0_SD_CLK_SEL1	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1h = pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

Table 15-135. Register Call Summary for ICSSG_PRU0_SD_CLK_SEL_REG1

PRU_ICSSG_CFG Registers

- [ICSSG_PRU0_SD_CLK_SEL_REG1 Register \(Offset = 50h\) \[reset = X\]: \[0\]](#)

15.5.16 ICSSG_PRU0_SD_SAMPLE_SIZE_REG1 Register (Offset = 54h) [reset = X]

ICSSG_PRU0_SD_SAMPLE_SIZE_REG1 is shown in Figure 15-43 and described in Table 15-137.

Return to [Summary Table](#).

PRU0 FD and Over Sample Size Register 1.

Table 15-136.
ICSSG_PRU0_SD_SAMPLE_SIZE_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6054h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6054h

Figure 15-43. ICSSG_PRU0_SD_SAMPLE_SIZE_REG1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRU0_FD_EN_1	PRU0_FD_ON_E_MAX_1	PRU0_FD_ONE_MAX_LIMIT_1				PRU0_FD_ON_E_MIN_1	
R/W-0h	R/W-0h	R/W-0h				R/W-0h	
15	14	13	12	11	10	9	8
PRU0_FD_ONE_MIN_LIMIT_1				PRU0_FD_WINDOW_SIZE_1			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
PRU0_SD_SAMPLE_SIZE1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-137. ICSSG_PRU0_SD_SAMPLE_SIZE_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU0_FD_EN_1	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU0_FD_ONE_MAX_1	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ONE_MAX_LI MIT_1	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU0_FD_ONE_MIN_1	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-137. ICSSG_PRU0_SD_SAMPLE_SIZE_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU0_FD_ONE_MIN_LIMIT_1	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU0_FD_WINDOW_SIZE_1	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU0_SD_SAMPLE_SIZE_1	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) Note: the 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3h, then the third clock after first 1 is detected, the VAL will get set.

Table 15-138. Register Call Summary for ICSSG_PRU0_SD_SAMPLE_SIZE_REG1

PRU_ICSSG_CFG Registers

- [ICSSG_PRU0_SD_SAMPLE_SIZE_REG1 Register \(Offset = 54h\) \[reset = X\]: \[0\]](#)

15.5.17 ICSSG_PRU0_SD_CLK_SEL_REG2 Register (Offset = 58h) [reset = X]

ICSSG_PRU0_SD_CLK_SEL_REG2 is shown in [Figure 15-44](#) and described in [Table 15-140](#).

Return to [Summary Table](#).

PRU0 FD, ACC and Clock Selection Register 2

**Table 15-139. ICSSG_PRU0_SD_CLK_SEL_REG2
Instances**

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6058h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6058h

Figure 15-44. ICSSG_PRU0_SD_CLK_SEL_REG2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED	PRU0_FD_ZERO_MAX_2	PRU0_FD_ZERO_MAX_LIMIT_2				PRU0_FD_ZERO_MIN_2	
R/W-X	R/W-0h	R/W-0h				R/W-0h	
15	14	13	12	11	10	9	8
PRU0_FD_ZERO_MIN_LIMIT_2					RESERVED		
R/W-0h					R/W-X		
7	6	5	4	3	2	1	0
RESERVED		PRU0_SD_ACC_SEL2		RESERVED	PRU0_SD_CLK_INV2	PRU0_SD_CLK_SEL2	
R/W-X		R/W-0h		R/W-X	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-140. ICSSG_PRU0_SD_CLK_SEL_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU0_FD_ZERO_MAX_2	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ZERO_MAX_LIMIT_2	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU0_FD_ZERO_MIN_2	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-140. ICSSG_PRU0_SD_CLK_SEL_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU0_FD_ZERO_MIN_LI MIT_2	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU0_SD_ACC_SEL2	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU0_SD_CLK_INV2	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU0_SD_CLK_SEL2	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1= pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

Table 15-141. Register Call Summary for ICSSG_PRU0_SD_CLK_SEL_REG2

PRU_ICSSG_CFG Registers

- [ICSSG_PRU0_SD_CLK_SEL_REG2 Register \(Offset = 58h\) \[reset = X\]: \[0\]](#)

15.5.18 ICSSG_PRU0_SD_SAMPLE_SIZE_REG2 Register (Offset = 5Ch) [reset = X]

ICSSG_PRU0_SD_SAMPLE_SIZE_REG2 is shown in Figure 15-45 and described in Table 15-143.

Return to [Summary Table](#).

PRU0 FD and Over Sample Size Register 2.

Table 15-142.
ICSSG_PRU0_SD_SAMPLE_SIZE_REG2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 605Ch
PRU_ICSSG1_PR1_CFG_SLV	0B12 605Ch

Figure 15-45. ICSSG_PRU0_SD_SAMPLE_SIZE_REG2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRU0_FD_EN_2	PRU0_FD_ON_E_MAX_2	PRU0_FD_ONE_MAX_LIMIT_2				PRU0_FD_ON_E_MIN_2	
R/W-0h	R/W-0h	R/W-0h				R/W-0h	
15	14	13	12	11	10	9	8
PRU0_FD_ONE_MIN_LIMIT_2				PRU0_FD_WINDOW_SIZE_2			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
PRU0_SD_SAMPLE_SIZE2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-143. ICSSG_PRU0_SD_SAMPLE_SIZE_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU0_FD_EN_2	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU0_FD_ONE_MAX_2	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ONE_MAX_LI MIT_2	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU0_FD_ONE_MIN_2	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-143. ICSSG_PRU0_SD_SAMPLE_SIZE_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU0_FD_ONE_MIN_LIMIT_2	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU0_FD_WINDOW_SIZE_2	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU0_SD_SAMPLE_SIZE_E2	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) Note: the 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3h, then the third clock after first 1 is detected, the VAL will get set.

Table 15-144. Register Call Summary for ICSSG_PRU0_SD_SAMPLE_SIZE_REG2

PRU_ICSSG_CFG Registers

- [ICSSG_PRU0_SD_SAMPLE_SIZE_REG2 Register \(Offset = 5Ch\) \[reset = X\]: \[0\]](#)

15.5.19 ICSSG_PRU0_SD_CLK_SEL_REG3 Register (Offset = 60h) [reset = X]

ICSSG_PRU0_SD_CLK_SEL_REG3 is shown in [Figure 15-46](#) and described in [Table 15-146](#).

Return to [Summary Table](#).

PRU0 FD, ACC and Clock Selection Register 3.

**Table 15-145. ICSSG_PRU0_SD_CLK_SEL_REG3
Instances**

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6060h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6060h

Figure 15-46. ICSSG_PRU0_SD_CLK_SEL_REG3 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED	PRU0_FD_ZERO_MAX_3	PRU0_FD_ZERO_MAX_LIMIT_3					PRU0_FD_ZERO_MIN_3
R/W-X	R/W-0h	R/W-0h				R/W-0h	
15	14	13	12	11	10	9	8
PRU0_FD_ZERO_MIN_LIMIT_3					RESERVED		
R/W-0h				R/W-X			
7	6	5	4	3	2	1	0
RESERVED		PRU0_SD_ACC_SEL3		RESERVED	PRU0_SD_CLK_INV3	PRU0_SD_CLK_SEL3	
R/W-X		R/W-0h		R/W-X	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-146. ICSSG_PRU0_SD_CLK_SEL_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU0_FD_ZERO_MAX_3	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ZERO_MAX_LIMIT_3	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU0_FD_ZERO_MIN_3	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-146. ICSSG_PRU0_SD_CLK_SEL_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU0_FD_ZERO_MIN_LI MIT_3	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU0_SD_ACC_SEL3	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU0_SD_CLK_INV3	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU0_SD_CLK_SEL3	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1h = pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

Table 15-147. Register Call Summary for ICSSG_PRU0_SD_CLK_SEL_REG3

PRU_ICSSG_CFG Registers

- [ICSSG_PRU0_SD_CLK_SEL_REG3 Register \(Offset = 60h\) \[reset = X\]: \[0\]](#)

15.5.20 ICSSG_PRU0_SD_SAMPLE_SIZE_REG3 Register (Offset = 64h) [reset = X]

ICSSG_PRU0_SD_SAMPLE_SIZE_REG3 is shown in [Figure 15-47](#) and described in [Table 15-149](#).

Return to [Summary Table](#).

PRU0 FD and Over Sample Size Register 3.

Table 15-148.
ICSSG_PRU0_SD_SAMPLE_SIZE_REG3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6064h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6064h

Figure 15-47. ICSSG_PRU0_SD_SAMPLE_SIZE_REG3 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRU0_FD_EN_3	PRU0_FD_ON_E_MAX_3	PRU0_FD_ONE_MAX_LIMIT_3				PRU0_FD_ON_E_MIN_3	
R/W-0h	R/W-0h	R/W-0h				R/W-0h	
15	14	13	12	11	10	9	8
PRU0_FD_ONE_MIN_LIMIT_3				PRU0_FD_WINDOW_SIZE_3			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
PRU0_SD_SAMPLE_SIZE3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-149. ICSSG_PRU0_SD_SAMPLE_SIZE_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU0_FD_EN_3	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU0_FD_ONE_MAX_3	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ONE_MAX_LIMIT_3	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU0_FD_ONE_MIN_3	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-149. ICSSG_PRU0_SD_SAMPLE_SIZE_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU0_FD_ONE_MIN_LIMIT_3	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU0_FD_WINDOW_SIZE_3	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU0_SD_SAMPLE_SIZE_3	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) Note: the 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3h, then the third clock after first 1 is detected, the VAL will get set.

Table 15-150. Register Call Summary for ICSSG_PRU0_SD_SAMPLE_SIZE_REG3

PRU_ICSSG_CFG Registers

- [ICSSG_PRU0_SD_SAMPLE_SIZE_REG3 Register \(Offset = 64h\) \[reset = X\]: \[0\]](#)

15.5.21 ICSSG_PRU0_SD_CLK_SEL_REG4 Register (Offset = 68h) [reset = X]

ICSSG_PRU0_SD_CLK_SEL_REG4 is shown in [Figure 15-48](#) and described in [Table 15-152](#).

Return to [Summary Table](#).

PRU0 FD, ACC and Clock Selection Register 4.

Table 15-151. ICSSG_PRU0_SD_CLK_SEL_REG4 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6068h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6068h

Figure 15-48. ICSSG_PRU0_SD_CLK_SEL_REG4 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED	PRU0_FD_ZERO_MAX_4	PRU0_FD_ZERO_MAX_LIMIT_4				PRU0_FD_ZERO_MIN_4	
R/W-X	R/W-0h	R/W-0h				R/W-0h	
15	14	13	12	11	10	9	8
PRU0_FD_ZERO_MIN_LIMIT_4					RESERVED		
R/W-0h					R/W-X		
7	6	5	4	3	2	1	0
RESERVED		PRU0_SD_ACC_SEL4		RESERVED	PRU0_SD_CLK_INV4	PRU0_SD_CLK_SEL4	
R/W-X		R/W-0h		R/W-X	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-152. ICSSG_PRU0_SD_CLK_SEL_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU0_FD_ZERO_MAX_4	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ZERO_MAX_LIMIT_4	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU0_FD_ZERO_MIN_4	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-152. ICSSG_PRU0_SD_CLK_SEL_REG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU0_FD_ZERO_MIN_LI MIT_4	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU0_SD_ACC_SEL4	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU0_SD_CLK_INV4	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU0_SD_CLK_SEL4	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1h = pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

Table 15-153. Register Call Summary for ICSSG_PRU0_SD_CLK_SEL_REG4

PRU_ICSSG_CFG Registers

- [ICSSG_PRU0_SD_CLK_SEL_REG4 Register \(Offset = 68h\) \[reset = X\]: \[0\]](#)

15.5.22 ICSSG_PRU0_SD_SAMPLE_SIZE_REG4 Register (Offset = 6Ch) [reset = X]

ICSSG_PRU0_SD_SAMPLE_SIZE_REG4 is shown in Figure 15-49 and described in Table 15-155.

Return to [Summary Table](#).

PRU0 FD and Over Sample Size Register 4.

Table 15-154.
ICSSG_PRU0_SD_SAMPLE_SIZE_REG4 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 606Ch
PRU_ICSSG1_PR1_CFG_SLV	0B12 606Ch

Figure 15-49. ICSSG_PRU0_SD_SAMPLE_SIZE_REG4 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRU0_FD_EN_4	PRU0_FD_ON_E_MAX_4	PRU0_FD_ONE_MAX_LIMIT_4				PRU0_FD_ON_E_MIN_4	
R/W-0h	R/W-0h	R/W-0h				R/W-0h	
15	14	13	12	11	10	9	8
PRU0_FD_ONE_MIN_LIMIT_4				PRU0_FD_WINDOW_SIZE_4			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
PRU0_SD_SAMPLE_SIZE4							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-155. ICSSG_PRU0_SD_SAMPLE_SIZE_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU0_FD_EN_4	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU0_FD_ONE_MAX_4	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ONE_MAX_LIMIT_4	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU0_FD_ONE_MIN_4	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-155. ICSSG_PRU0_SD_SAMPLE_SIZE_REG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU0_FD_ONE_MIN_LIM IT_4	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU0_FD_WINDOW_SIZ E_4	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU0_SD_SAMPLE_SIZ E4	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3h, then the third clock after first 1 is detected, the VAL will get set.

Table 15-156. Register Call Summary for ICSSG_PRU0_SD_SAMPLE_SIZE_REG4

PRU_ICSSG_CFG Registers

- [ICSSG_PRU0_SD_SAMPLE_SIZE_REG4 Register \(Offset = 6Ch\) \[reset = X\]: \[0\]](#)

15.5.23 ICSSG_PRU0_SD_CLK_SEL_REG5 Register (Offset = 70h) [reset = X]

ICSSG_PRU0_SD_CLK_SEL_REG5 is shown in [Figure 15-50](#) and described in [Table 15-158](#).

Return to [Summary Table](#).

PRU0 FD, ACC and Clock Selection Register 5.

**Table 15-157. ICSSG_PRU0_SD_CLK_SEL_REG5
Instances**

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6070h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6070h

Figure 15-50. ICSSG_PRU0_SD_CLK_SEL_REG5 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED	PRU0_FD_ZERO_MAX_5	PRU0_FD_ZERO_MAX_LIMIT_5				PRU0_FD_ZERO_MIN_5	
R/W-X	R/W-0h	R/W-0h				R/W-0h	
15	14	13	12	11	10	9	8
PRU0_FD_ZERO_MIN_LIMIT_5					RESERVED		
R/W-0h					R/W-X		
7	6	5	4	3	2	1	0
RESERVED		PRU0_SD_ACC_SEL5		RESERVED	PRU0_SD_CLK_INV5	PRU0_SD_CLK_SEL5	
R/W-X		R/W-0h		R/W-X	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-158. ICSSG_PRU0_SD_CLK_SEL_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU0_FD_ZERO_MAX_5	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ZERO_MAX_LIMIT_5	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU0_FD_ZERO_MIN_5	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-158. ICSSG_PRU0_SD_CLK_SEL_REG5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU0_FD_ZERO_MIN_LI MIT_5	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU0_SD_ACC_SEL5	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU0_SD_CLK_INV5	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU0_SD_CLK_SEL5	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1h = pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

Table 15-159. Register Call Summary for ICSSG_PRU0_SD_CLK_SEL_REG5

PRU_ICSSG_CFG Registers

- [ICSSG_PRU0_SD_CLK_SEL_REG5 Register \(Offset = 70h\) \[reset = X\]: \[0\]](#)

15.5.24 ICSSG_PRU0_SD_SAMPLE_SIZE_REG5 Register (Offset = 74h) [reset = X]

ICSSG_PRU0_SD_SAMPLE_SIZE_REG5 is shown in Figure 15-51 and described in Table 15-161.

Return to [Summary Table](#).

PRU0 FD and Over Sample Size Register 5.

Table 15-160.
ICSSG_PRU0_SD_SAMPLE_SIZE_REG5 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6074h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6074h

Figure 15-51. ICSSG_PRU0_SD_SAMPLE_SIZE_REG5 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRU0_FD_EN_5	PRU0_FD_ON_E_MAX_5	PRU0_FD_ONE_MAX_LIMIT_5				PRU0_FD_ON_E_MIN_5	
R/W-0h	R/W-0h	R/W-0h				R/W-0h	
15	14	13	12	11	10	9	8
PRU0_FD_ONE_MIN_LIMIT_5				PRU0_FD_WINDOW_SIZE_5			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
PRU0_SD_SAMPLE_SIZE5							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-161. ICSSG_PRU0_SD_SAMPLE_SIZE_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU0_FD_EN_5	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU0_FD_ONE_MAX_5	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ONE_MAX_LIMIT_5	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU0_FD_ONE_MIN_5	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-161. ICSSG_PRU0_SD_SAMPLE_SIZE_REG5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU0_FD_ONE_MIN_LIM IT_5	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU0_FD_WINDOW_SIZ E_5	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU0_SD_SAMPLE_SIZ E5	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3h, then the third clock after first 1 is detected, the VAL will get set.

Table 15-162. Register Call Summary for ICSSG_PRU0_SD_SAMPLE_SIZE_REG5

PRU_ICSSG_CFG Registers

- [ICSSG_PRU0_SD_SAMPLE_SIZE_REG5 Register \(Offset = 74h\) \[reset = X\]: \[0\]](#)

15.5.25 ICSSG_PRU0_SD_CLK_SEL_REG6 Register (Offset = 78h) [reset = X]

ICSSG_PRU0_SD_CLK_SEL_REG6 is shown in [Figure 15-52](#) and described in [Table 15-164](#).

Return to [Summary Table](#).

PRU0 FD, ACC and Clock Selection Register 6.

**Table 15-163. ICSSG_PRU0_SD_CLK_SEL_REG6
Instances**

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6078h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6078h

Figure 15-52. ICSSG_PRU0_SD_CLK_SEL_REG6 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED	PRU0_FD_ZERO_MAX_6	PRU0_FD_ZERO_MAX_LIMIT_6				PRU0_FD_ZERO_MIN_6	
R/W-X	R/W-0h	R/W-0h				R/W-0h	
15	14	13	12	11	10	9	8
PRU0_FD_ZERO_MIN_LIMIT_6					RESERVED		
R/W-0h					R/W-X		
7	6	5	4	3	2	1	0
RESERVED		PRU0_SD_ACC_SEL6		RESERVED	PRU0_SD_CLK_INV6	PRU0_SD_CLK_SEL6	
R/W-X		R/W-0h		R/W-X	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-164. ICSSG_PRU0_SD_CLK_SEL_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU0_FD_ZERO_MAX_6	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ZERO_MAX_LIMIT_6	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU0_FD_ZERO_MIN_6	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-164. ICSSG_PRU0_SD_CLK_SEL_REG6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU0_FD_ZERO_MIN_LI MIT_6	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU0_SD_ACC_SEL6	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU0_SD_CLK_INV6	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU0_SD_CLK_SEL6	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1h = pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

Table 15-165. Register Call Summary for ICSSG_PRU0_SD_CLK_SEL_REG6

PRU_ICSSG_CFG Registers

- [ICSSG_PRU0_SD_CLK_SEL_REG6 Register \(Offset = 78h\) \[reset = X\]: \[0\]](#)

15.5.26 ICSSG_PRU0_SD_SAMPLE_SIZE_REG6 Register (Offset = 7Ch) [reset = X]

ICSSG_PRU0_SD_SAMPLE_SIZE_REG6 is shown in Figure 15-53 and described in Table 15-167.

Return to [Summary Table](#).

PRU0 FD and Over Sample Size Register 6.

Table 15-166.
ICSSG_PRU0_SD_SAMPLE_SIZE_REG6 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 607Ch
PRU_ICSSG1_PR1_CFG_SLV	0B12 607Ch

Figure 15-53. ICSSG_PRU0_SD_SAMPLE_SIZE_REG6 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRU0_FD_EN_6	PRU0_FD_ON_E_MAX_6	PRU0_FD_ONE_MAX_LIMIT_6				PRU0_FD_ON_E_MIN_6	
R/W-0h	R/W-0h	R/W-0h				R/W-0h	
15	14	13	12	11	10	9	8
PRU0_FD_ONE_MIN_LIMIT_6				PRU0_FD_WINDOW_SIZE_6			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
PRU0_SD_SAMPLE_SIZE6							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-167. ICSSG_PRU0_SD_SAMPLE_SIZE_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU0_FD_EN_6	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU0_FD_ONE_MAX_6	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ONE_MAX_LIMIT_6	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU0_FD_ONE_MIN_6	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-167. ICSSG_PRU0_SD_SAMPLE_SIZE_REG6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU0_FD_ONE_MIN_LIMIT_6	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU0_FD_WINDOW_SIZE_6	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU0_SD_SAMPLE_SIZE_6	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3h, then the third clock after first 1 is detected, the VAL will get set.

Table 15-168. Register Call Summary for ICSSG_PRU0_SD_SAMPLE_SIZE_REG6

PRU_ICSSG_CFG Registers

- [ICSSG_PRU0_SD_SAMPLE_SIZE_REG6 Register \(Offset = 7Ch\) \[reset = X\]: \[0\]](#)

15.5.27 ICSSG_PRU0_SD_CLK_SEL_REG7 Register (Offset = 80h) [reset = X]

ICSSG_PRU0_SD_CLK_SEL_REG7 is shown in [Figure 15-54](#) and described in [Table 15-170](#).

Return to [Summary Table](#).

PRU0 FD, ACC and Clock Selection Register 7.

**Table 15-169. ICSSG_PRU0_SD_CLK_SEL_REG7
Instances**

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6080h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6080h

Figure 15-54. ICSSG_PRU0_SD_CLK_SEL_REG7 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED	PRU0_FD_ZERO_MAX_7	PRU0_FD_ZERO_MAX_LIMIT_7				PRU0_FD_ZERO_MIN_7	
R/W-X	R/W-0h	R/W-0h				R/W-0h	
15	14	13	12	11	10	9	8
PRU0_FD_ZERO_MIN_LIMIT_7					RESERVED		
R/W-0h					R/W-X		
7	6	5	4	3	2	1	0
RESERVED		PRU0_SD_ACC_SEL7		RESERVED	PRU0_SD_CLK_INV7	PRU0_SD_CLK_SEL7	
R/W-X		R/W-0h		R/W-X	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-170. ICSSG_PRU0_SD_CLK_SEL_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU0_FD_ZERO_MAX_7	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ZERO_MAX_LIMIT_7	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU0_FD_ZERO_MIN_7	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-170. ICSSG_PRU0_SD_CLK_SEL_REG7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU0_FD_ZERO_MIN_LI MIT_7	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU0_SD_ACC_SEL7	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU0_SD_CLK_INV7	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU0_SD_CLK_SEL7	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1h = pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

Table 15-171. Register Call Summary for ICSSG_PRU0_SD_CLK_SEL_REG7

PRU_ICSSG_CFG Registers

- [ICSSG_PRU0_SD_CLK_SEL_REG7 Register \(Offset = 80h\) \[reset = X\]: \[0\]](#)

15.5.28 ICSSG_PRU0_SD_SAMPLE_SIZE_REG7 Register (Offset = 84h) [reset = X]

ICSSG_PRU0_SD_SAMPLE_SIZE_REG7 is shown in Figure 15-55 and described in Table 15-173.

Return to [Summary Table](#).

PRU0 FD and Over Sample Size Register 7.

Table 15-172.
ICSSG_PRU0_SD_SAMPLE_SIZE_REG7 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6084h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6084h

Figure 15-55. ICSSG_PRU0_SD_SAMPLE_SIZE_REG7 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRU0_FD_EN_7	PRU0_FD_ON_E_MAX_7	PRU0_FD_ONE_MAX_LIMIT_7				PRU0_FD_ON_E_MIN_7	
R/W-0h	R/W-0h	R/W-0h				R/W-0h	
15	14	13	12	11	10	9	8
PRU0_FD_ONE_MIN_LIMIT_7				PRU0_FD_WINDOW_SIZE_7			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
PRU0_SD_SAMPLE_SIZE7							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-173. ICSSG_PRU0_SD_SAMPLE_SIZE_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU0_FD_EN_7	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU0_FD_ONE_MAX_7	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ONE_MAX_LIMIT_7	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU0_FD_ONE_MIN_7	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-173. ICSSG_PRU0_SD_SAMPLE_SIZE_REG7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU0_FD_ONE_MIN_LIM IT_7	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU0_FD_WINDOW_SIZ E_7	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU0_SD_SAMPLE_SIZ E7	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3h, then the third clock after first 1 is detected, the VAL will get set.

Table 15-174. Register Call Summary for ICSSG_PRU0_SD_SAMPLE_SIZE_REG7

PRU_ICSSG_CFG Registers

- [ICSSG_PRU0_SD_SAMPLE_SIZE_REG7 Register \(Offset = 84h\) \[reset = X\]: \[0\]](#)

15.5.29 ICSSG_PRU0_SD_CLK_SEL_REG8 Register (Offset = 88h) [reset = X]

ICSSG_PRU0_SD_CLK_SEL_REG8 is shown in [Figure 15-56](#) and described in [Table 15-176](#).

Return to [Summary Table](#).

PRU0 FD, ACC and Clock Selection Register 8.

**Table 15-175. ICSSG_PRU0_SD_CLK_SEL_REG8
Instances**

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6088h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6088h

Figure 15-56. ICSSG_PRU0_SD_CLK_SEL_REG8 Register

31		30		29		28		27		26		25		24	
RESERVED															
R/W-X															
23		22		21		20		19		18		17		16	
RESERVED		PRU0_FD_ZERO_MAX_8		PRU0_FD_ZERO_MAX_LIMIT_8										PRU0_FD_ZERO_MIN_8	
R/W-X		R/W-0h		R/W-0h										R/W-0h	
15		14		13		12		11		10		9		8	
PRU0_FD_ZERO_MIN_LIMIT_8										RESERVED					
R/W-0h										R/W-X					
7		6		5		4		3		2		1		0	
RESERVED				PRU0_SD_ACC_SEL8				RESERVED		PRU0_SD_CLK_INV8		PRU0_SD_CLK_SEL8			
R/W-X				R/W-0h				R/W-X		R/W-0h		R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-176. ICSSG_PRU0_SD_CLK_SEL_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU0_FD_ZERO_MAX_8	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ZERO_MAX_LIMIT_8	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU0_FD_ZERO_MIN_8	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-176. ICSSG_PRU0_SD_CLK_SEL_REG8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU0_FD_ZERO_MIN_LI MIT_8	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU0_SD_ACC_SEL8	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU0_SD_CLK_INV8	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU0_SD_CLK_SEL8	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1h = pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

Table 15-177. Register Call Summary for ICSSG_PRU0_SD_CLK_SEL_REG8

PRU_ICSSG_CFG Registers

- [ICSSG_PRU0_SD_CLK_SEL_REG8 Register \(Offset = 88h\) \[reset = X\]: \[0\]](#)

15.5.30 ICSSG_PRU0_SD_SAMPLE_SIZE_REG8 Register (Offset = 8Ch) [reset = X]

ICSSG_PRU0_SD_SAMPLE_SIZE_REG8 is shown in [Figure 15-57](#) and described in [Table 15-179](#).

Return to [Summary Table](#).

PRU0 FD and Over Sample Size Register 8.

Table 15-178.
ICSSG_PRU0_SD_SAMPLE_SIZE_REG8 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 608Ch
PRU_ICSSG1_PR1_CFG_SLV	0B12 608Ch

Figure 15-57. ICSSG_PRU0_SD_SAMPLE_SIZE_REG8 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRU0_FD_EN_8	PRU0_FD_ON_E_MAX_8	PRU0_FD_ONE_MAX_LIMIT_8				PRU0_FD_ON_E_MIN_8	
R/W-0h	R/W-0h	R/W-0h				R/W-0h	
15	14	13	12	11	10	9	8
PRU0_FD_ONE_MIN_LIMIT_8				PRU0_FD_WINDOW_SIZE_8			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
PRU0_SD_SAMPLE_SIZE8							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-179. ICSSG_PRU0_SD_SAMPLE_SIZE_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU0_FD_EN_8	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU0_FD_ONE_MAX_8	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU0_FD_ONE_MAX_LIMIT_8	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU0_FD_ONE_MIN_8	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-179. ICSSG_PRU0_SD_SAMPLE_SIZE_REG8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU0_FD_ONE_MIN_LIM IT_8	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU0_FD_WINDOW_SIZ E_8	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU0_SD_SAMPLE_SIZ E8	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3h, then the third clock after first 1 is detected, the VAL will get set.

Table 15-180. Register Call Summary for ICSSG_PRU0_SD_SAMPLE_SIZE_REG8

PRU_ICSSG_CFG Registers

- [ICSSG_PRU0_SD_SAMPLE_SIZE_REG8 Register \(Offset = 8Ch\) \[reset = X\]: \[0\]](#)

15.5.31 ICSSG_PRU1_SD_CLK_SEL_REG0 Register (Offset = 94h) [reset = X]

ICSSG_PRU1_SD_CLK_SEL_REG0 is shown in [Figure 15-58](#) and described in [Table 15-182](#).

Return to [Summary Table](#).

PRU1 FD, ACC and Clock Selection Register 0

Table 15-181. ICSSG_PRU1_SD_CLK_SEL_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6094h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6094h

Figure 15-58. ICSSG_PRU1_SD_CLK_SEL_REG0 Register

31		30		29		28		27		26		25		24	
RESERVED															
R/W-X															
23		22		21		20		19		18		17		16	
RESERVED		PRU1_FD_ZERO_MAX_0		PRU1_FD_ZERO_MAX_LIMIT_0										PRU1_FD_ZERO_MIN_0	
R/W-X		R/W-0h		R/W-0h								R/W-0h			
15		14		13		12		11		10		9		8	
PRU1_FD_ZERO_MIN_LIMIT_0										RESERVED					
R/W-0h										R/W-X					
7		6		5		4		3		2		1		0	
RESERVED				PRU1_SD_ACC_SEL0				RESERVED		PRU1_SD_CLK_INV0		PRU1_SD_CLK_SEL0			
R/W-X				R/W-0h				R/W-X		R/W-0h		R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-182. ICSSG_PRU1_SD_CLK_SEL_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU1_FD_ZERO_MAX_0	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ZERO_MAX_LIMIT_0	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU1_FD_ZERO_MIN_0	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-182. ICSSG_PRU1_SD_CLK_SEL_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU1_FD_ZERO_MIN_LI MIT_0	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU1_SD_ACC_SEL0	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU1_SD_CLK_INV0	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU1_SD_CLK_SEL0	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1h = pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

Table 15-183. Register Call Summary for ICSSG_PRU1_SD_CLK_SEL_REG0

PRU_ICSSG_CFG Registers

- [ICSSG_PRU1_SD_CLK_SEL_REG0 Register \(Offset = 94h\) \[reset = X\]: \[0\]](#)

15.5.32 ICSSG_PRU1_SD_SAMPLE_SIZE_REG0 Register (Offset = 98h) [reset = X]

ICSSG_PRU1_SD_SAMPLE_SIZE_REG0 is shown in Figure 15-59 and described in Table 15-185.

Return to [Summary Table](#).

PRU1 FD and Over Sample Size Register 0.

Table 15-184.
ICSSG_PRU1_SD_SAMPLE_SIZE_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6098h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6098h

Figure 15-59. ICSSG_PRU1_SD_SAMPLE_SIZE_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRU1_FD_EN_0	PRU1_FD_ON_E_MAX_0	PRU1_FD_ONE_MAX_LIMIT_0				PRU1_FD_ON_E_MIN_0	
R/W-0h	R/W-0h	R/W-0h				R/W-0h	
15	14	13	12	11	10	9	8
PRU1_FD_ONE_MIN_LIMIT_0				PRU1_FD_WINDOW_SIZE_0			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
PRU1_SD_SAMPLE_SIZE0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-185. ICSSG_PRU1_SD_SAMPLE_SIZE_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU1_FD_EN_0	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU1_FD_ONE_MAX_0	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ONE_MAX_LIMIT_0	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU1_FD_ONE_MIN_0	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-185. ICSSG_PRU1_SD_SAMPLE_SIZE_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU1_FD_ONE_MIN_LIM IT_0	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU1_FD_WINDOW_SIZ E_0	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU1_SD_SAMPLE_SIZ E0	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3h, then the third clock after first 1 is detected, the VAL will get set.

Table 15-186. Register Call Summary for ICSSG_PRU1_SD_SAMPLE_SIZE_REG0

PRU_ICSSG_CFG Registers

- [ICSSG_PRU1_SD_SAMPLE_SIZE_REG0 Register \(Offset = 98h\) \[reset = X\]: \[0\]](#)

15.5.33 ICSSG_PRU1_SD_CLK_SEL_REG1 Register (Offset = 9Ch) [reset = X]

ICSSG_PRU1_SD_CLK_SEL_REG1 is shown in [Figure 15-60](#) and described in [Table 15-188](#).

Return to [Summary Table](#).

PRU1 FD, ACC and Clock Selection Register 1.

**Table 15-187. ICSSG_PRU1_SD_CLK_SEL_REG1
Instances**

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 609Ch
PRU_ICSSG1_PR1_CFG_SLV	0B12 609Ch

Figure 15-60. ICSSG_PRU1_SD_CLK_SEL_REG1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED	PRU1_FD_ZERO_MAX_1	PRU1_FD_ZERO_MAX_LIMIT_1				PRU1_FD_ZERO_MIN_1	
R/W-X	R/W-0h	R/W-0h				R/W-0h	
15	14	13	12	11	10	9	8
PRU1_FD_ZERO_MIN_LIMIT_1					RESERVED		
R/W-0h					R/W-X		
7	6	5	4	3	2	1	0
RESERVED		PRU1_SD_ACC_SEL1		RESERVED	PRU1_SD_CLK_INV1	PRU1_SD_CLK_SEL1	
R/W-X		R/W-0h		R/W-X	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-188. ICSSG_PRU1_SD_CLK_SEL_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU1_FD_ZERO_MAX_1	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ZERO_MAX_LIMIT_1	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1 = 2 .. 1Fh = 32
16	PRU1_FD_ZERO_MIN_1	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-188. ICSSG_PRU1_SD_CLK_SEL_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU1_FD_ZERO_MIN_LI MIT_1	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU1_SD_ACC_SEL1	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU1_SD_CLK_INV1	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU1_SD_CLK_SEL1	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1h = pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

Table 15-189. Register Call Summary for ICSSG_PRU1_SD_CLK_SEL_REG1

PRU_ICSSG_CFG Registers

- [ICSSG_PRU1_SD_CLK_SEL_REG1 Register \(Offset = 9Ch\) \[reset = X\]: \[0\]](#)

15.5.34 ICSSG_PRU1_SD_SAMPLE_SIZE_REG1 Register (Offset = A0h) [reset = X]

ICSSG_PRU1_SD_SAMPLE_SIZE_REG1 is shown in Figure 15-61 and described in Table 15-191.

Return to [Summary Table](#).

PRU1 FD and Over Sample Size Register 1.

Table 15-190.
ICSSG_PRU1_SD_SAMPLE_SIZE_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 60A0h
PRU_ICSSG1_PR1_CFG_SLV	0B12 60A0h

Figure 15-61. ICSSG_PRU1_SD_SAMPLE_SIZE_REG1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRU1_FD_EN_1	PRU1_FD_ON_E_MAX_1	PRU1_FD_ONE_MAX_LIMIT_1				PRU1_FD_ON_E_MIN_1	
R/W-0h	R/W-0h	R/W-0h				R/W-0h	
15	14	13	12	11	10	9	8
PRU1_FD_ONE_MIN_LIMIT_1				PRU1_FD_WINDOW_SIZE_1			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
PRU1_SD_SAMPLE_SIZE1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-191. ICSSG_PRU1_SD_SAMPLE_SIZE_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU1_FD_EN_1	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU1_FD_ONE_MAX_1	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ONE_MAX_LI MIT_1	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU1_FD_ONE_MIN_1	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-191. ICSSG_PRU1_SD_SAMPLE_SIZE_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU1_FD_ONE_MIN_LIM IT_1	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU1_FD_WINDOW_SIZ E_1	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU1_SD_SAMPLE_SIZ E1	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3h, then the third clock after first 1 is detected, the VAL will get set.

Table 15-192. Register Call Summary for ICSSG_PRU1_SD_SAMPLE_SIZE_REG1

PRU_ICSSG_CFG Registers

- [ICSSG_PRU1_SD_SAMPLE_SIZE_REG1 Register \(Offset = A0h\) \[reset = X\]: \[0\]](#)

15.5.35 ICSSG_PRU1_SD_CLK_SEL_REG2 Register (Offset = A4h) [reset = X]

ICSSG_PRU1_SD_CLK_SEL_REG2 is shown in [Figure 15-62](#) and described in [Table 15-194](#).

Return to [Summary Table](#).

PRU1 FD, ACC and Clock Selection Register 2.

**Table 15-193. ICSSG_PRU1_SD_CLK_SEL_REG2
Instances**

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 60A4h
PRU_ICSSG1_PR1_CFG_SLV	0B12 60A4h

Figure 15-62. ICSSG_PRU1_SD_CLK_SEL_REG2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED	PRU1_FD_ZERO_MAX_2	PRU1_FD_ZERO_MAX_LIMIT_2				PRU1_FD_ZERO_MIN_2	
R/W-X	R/W-0h	R/W-0h				R/W-0h	
15	14	13	12	11	10	9	8
PRU1_FD_ZERO_MIN_LIMIT_2					RESERVED		
R/W-0h					R/W-X		
7	6	5	4	3	2	1	0
RESERVED		PRU1_SD_ACC_SEL2		RESERVED	PRU1_SD_CLK_INV2	PRU1_SD_CLK_SEL2	
R/W-X		R/W-0h		R/W-X	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-194. ICSSG_PRU1_SD_CLK_SEL_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU1_FD_ZERO_MAX_2	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ZERO_MAX_LIMIT_2	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU1_FD_ZERO_MIN_2	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-194. ICSSG_PRU1_SD_CLK_SEL_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU1_FD_ZERO_MIN_LI MIT_2	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU1_SD_ACC_SEL2	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU1_SD_CLK_INV2	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU1_SD_CLK_SEL2	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1h = pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

Table 15-195. Register Call Summary for ICSSG_PRU1_SD_CLK_SEL_REG2

PRU_ICSSG_CFG Registers

- [ICSSG_PRU1_SD_CLK_SEL_REG2 Register \(Offset = A4h\) \[reset = X\]: \[0\]](#)

15.5.36 ICSSG_PRU1_SD_SAMPLE_SIZE_REG2 Register (Offset = A8h) [reset = X]

ICSSG_PRU1_SD_SAMPLE_SIZE_REG2 is shown in [Figure 15-63](#) and described in [Table 15-197](#).

Return to [Summary Table](#).

PRU1 FD and Over Sample Size Register 2.

Table 15-196.
ICSSG_PRU1_SD_SAMPLE_SIZE_REG2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 60A8h
PRU_ICSSG1_PR1_CFG_SLV	0B12 60A8h

Figure 15-63. ICSSG_PRU1_SD_SAMPLE_SIZE_REG2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRU1_FD_EN_2	PRU1_FD_ON_E_MAX_2	PRU1_FD_ONE_MAX_LIMIT_2				PRU1_FD_ON_E_MIN_2	
R/W-0h	R/W-0h	R/W-0h				R/W-0h	
15	14	13	12	11	10	9	8
PRU1_FD_ONE_MIN_LIMIT_2				PRU1_FD_WINDOW_SIZE_2			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
PRU1_SD_SAMPLE_SIZE2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-197. ICSSG_PRU1_SD_SAMPLE_SIZE_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU1_FD_EN_2	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU1_FD_ONE_MAX_2	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ONE_MAX_LI MIT_2	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU1_FD_ONE_MIN_2	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-197. ICSSG_PRU1_SD_SAMPLE_SIZE_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU1_FD_ONE_MIN_LIM IT_2	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU1_FD_WINDOW_SIZ E_2	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU1_SD_SAMPLE_SIZ E2	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3h, then the third clock after first 1 is detected, the VAL will get set.

Table 15-198. Register Call Summary for ICSSG_PRU1_SD_SAMPLE_SIZE_REG2

PRU_ICSSG_CFG Registers

- [ICSSG_PRU1_SD_SAMPLE_SIZE_REG2 Register \(Offset = A8h\) \[reset = X\]: \[0\]](#)

15.5.37 ICSSG_PRU1_SD_CLK_SEL_REG3 Register (Offset = ACh) [reset = X]

ICSSG_PRU1_SD_CLK_SEL_REG3 is shown in [Figure 15-64](#) and described in [Table 15-200](#).

Return to [Summary Table](#).

PRU1 FD, ACC and Clock Selection Register 3.

**Table 15-199. ICSSG_PRU1_SD_CLK_SEL_REG3
Instances**

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 60ACh
PRU_ICSSG1_PR1_CFG_SLV	0B12 60ACh

Figure 15-64. ICSSG_PRU1_SD_CLK_SEL_REG3 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED	PRU1_FD_ZERO_MAX_3	PRU1_FD_ZERO_MAX_LIMIT_3				PRU1_FD_ZERO_MIN_3	
R/W-X	R/W-0h	R/W-0h				R/W-0h	
15	14	13	12	11	10	9	8
PRU1_FD_ZERO_MIN_LIMIT_3					RESERVED		
R/W-0h					R/W-X		
7	6	5	4	3	2	1	0
RESERVED		PRU1_SD_ACC_SEL3		RESERVED	PRU1_SD_CLK_INV3	PRU1_SD_CLK_SEL3	
R/W-X		R/W-0h		R/W-X	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-200. ICSSG_PRU1_SD_CLK_SEL_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU1_FD_ZERO_MAX_3	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ZERO_MAX_LIMIT_3	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU1_FD_ZERO_MIN_3	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-200. ICSSG_PRU1_SD_CLK_SEL_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU1_FD_ZERO_MIN_LI MIT_3	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU1_SD_ACC_SEL3	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU1_SD_CLK_INV3	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU1_SD_CLK_SEL3	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1h = pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

Table 15-201. Register Call Summary for ICSSG_PRU1_SD_CLK_SEL_REG3

PRU_ICSSG_CFG Registers

- [ICSSG_PRU1_SD_CLK_SEL_REG3 Register \(Offset = ACh\) \[reset = X\]: \[0\]](#)

15.5.38 ICSSG_PRU1_SD_SAMPLE_SIZE_REG3 Register (Offset = B0h) [reset = X]

ICSSG_PRU1_SD_SAMPLE_SIZE_REG3 is shown in [Figure 15-65](#) and described in [Table 15-203](#).

Return to [Summary Table](#).

PRU1 FD and Over Sample Size Register 3.

Table 15-202.
ICSSG_PRU1_SD_SAMPLE_SIZE_REG3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 60B0h
PRU_ICSSG1_PR1_CFG_SLV	0B12 60B0h

Figure 15-65. ICSSG_PRU1_SD_SAMPLE_SIZE_REG3 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRU1_FD_EN_3	PRU1_FD_ON_E_MAX_3	PRU1_FD_ONE_MAX_LIMIT_3				PRU1_FD_ON_E_MIN_3	
R/W-0h	R/W-0h	R/W-0h				R/W-0h	
15	14	13	12	11	10	9	8
PRU1_FD_ONE_MIN_LIMIT_3				PRU1_FD_WINDOW_SIZE_3			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
PRU1_SD_SAMPLE_SIZE3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-203. ICSSG_PRU1_SD_SAMPLE_SIZE_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU1_FD_EN_3	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU1_FD_ONE_MAX_3	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ONE_MAX_LIMIT_3	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU1_FD_ONE_MIN_3	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-203. ICSSG_PRU1_SD_SAMPLE_SIZE_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU1_FD_ONE_MIN_LIM IT_3	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU1_FD_WINDOW_SIZ E_3	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU1_SD_SAMPLE_SIZ E3	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3h, then the third clock after first 1 is detected, the VAL will get set.

Table 15-204. Register Call Summary for ICSSG_PRU1_SD_SAMPLE_SIZE_REG3

PRU_ICSSG_CFG Registers

- [ICSSG_PRU1_SD_SAMPLE_SIZE_REG3 Register \(Offset = B0h\) \[reset = X\]: \[0\]](#)

15.5.39 ICSSG_PRU1_SD_CLK_SEL_REG4 Register (Offset = B4h) [reset = X]

ICSSG_PRU1_SD_CLK_SEL_REG4 is shown in [Figure 15-66](#) and described in [Table 15-206](#).

Return to [Summary Table](#).

PRU1 FD, ACC and Clock Selection Register 4.

Table 15-205. ICSSG_PRU1_SD_CLK_SEL_REG4 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 60B4h
PRU_ICSSG1_PR1_CFG_SLV	0B12 60B4h

Figure 15-66. ICSSG_PRU1_SD_CLK_SEL_REG4 Register

31		30		29		28		27		26		25		24	
RESERVED															
R/W-X															
23		22		21		20		19		18		17		16	
RESERVED		PRU1_FD_ZERO_MAX_4		PRU1_FD_ZERO_MAX_LIMIT_4										PRU1_FD_ZERO_MIN_4	
R/W-X		R/W-0h		R/W-0h										R/W-0h	
15		14		13		12		11		10		9		8	
PRU1_FD_ZERO_MIN_LIMIT_4										RESERVED					
R/W-0h										R/W-X					
7		6		5		4		3		2		1		0	
RESERVED				PRU1_SD_ACC_SEL4				RESERVED		PRU1_SD_CLK_INV4		PRU1_SD_CLK_SEL4			
R/W-X				R/W-0h				R/W-X		R/W-0h		R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-206. ICSSG_PRU1_SD_CLK_SEL_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU1_FD_ZERO_MAX_4	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ZERO_MAX_LIMIT_4	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU1_FD_ZERO_MIN_4	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-206. ICSSG_PRU1_SD_CLK_SEL_REG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU1_FD_ZERO_MIN_LI MIT_4	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU1_SD_ACC_SEL4	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU1_SD_CLK_INV4	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU1_SD_CLK_SEL4	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1h = pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

Table 15-207. Register Call Summary for ICSSG_PRU1_SD_CLK_SEL_REG4

PRU_ICSSG_CFG Registers

- [ICSSG_PRU1_SD_CLK_SEL_REG4 Register \(Offset = B4h\) \[reset = X\]: \[0\]](#)

15.5.40 ICSSG_PRU1_SD_SAMPLE_SIZE_REG4 Register (Offset = B8h) [reset = X]

ICSSG_PRU1_SD_SAMPLE_SIZE_REG4 is shown in [Figure 15-67](#) and described in [Table 15-209](#).

Return to [Summary Table](#).

PRU1 FD and Over Sample Size Register 4.

Table 15-208.
ICSSG_PRU1_SD_SAMPLE_SIZE_REG4 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 60B8h
PRU_ICSSG1_PR1_CFG_SLV	0B12 60B8h

Figure 15-67. ICSSG_PRU1_SD_SAMPLE_SIZE_REG4 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRU1_FD_EN_4	PRU1_FD_ON_E_MAX_4	PRU1_FD_ONE_MAX_LIMIT_4				PRU1_FD_ON_E_MIN_4	
R/W-0h	R/W-0h	R/W-0h				R/W-0h	
15	14	13	12	11	10	9	8
PRU1_FD_ONE_MIN_LIMIT_4				PRU1_FD_WINDOW_SIZE_4			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
PRU1_SD_SAMPLE_SIZE4							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-209. ICSSG_PRU1_SD_SAMPLE_SIZE_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU1_FD_EN_4	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU1_FD_ONE_MAX_4	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ONE_MAX_LIMIT_4	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU1_FD_ONE_MIN_4	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-209. ICSSG_PRU1_SD_SAMPLE_SIZE_REG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU1_FD_ONE_MIN_LIMIT_4	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU1_FD_WINDOW_SIZE_4	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU1_SD_SAMPLE_SIZE_4	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3h, then the third clock after first 1 is detected, the VAL will get set.

Table 15-210. Register Call Summary for ICSSG_PRU1_SD_SAMPLE_SIZE_REG4

PRU_ICSSG_CFG Registers

- [ICSSG_PRU1_SD_SAMPLE_SIZE_REG4 Register \(Offset = B8h\) \[reset = X\]: \[0\]](#)

15.5.41 ICSSG_PRU1_SD_CLK_SEL_REG5 Register (Offset = BCh) [reset = X]

ICSSG_PRU1_SD_CLK_SEL_REG5 is shown in [Figure 15-68](#) and described in [Table 15-212](#).

Return to [Summary Table](#).

PRU1 FD, ACC and Clock Selection Register 5

**Table 15-211. ICSSG_PRU1_SD_CLK_SEL_REG5
Instances**

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 60BCh
PRU_ICSSG1_PR1_CFG_SLV	0B12 60BCh

Figure 15-68. ICSSG_PRU1_SD_CLK_SEL_REG5 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED	PRU1_FD_ZERO_MAX_5	PRU1_FD_ZERO_MAX_LIMIT_5				PRU1_FD_ZERO_MIN_5	
R/W-X	R/W-0h	R/W-0h				R/W-0h	
15	14	13	12	11	10	9	8
PRU1_FD_ZERO_MIN_LIMIT_5					RESERVED		
R/W-0h					R/W-X		
7	6	5	4	3	2	1	0
RESERVED		PRU1_SD_ACC_SEL5		RESERVED	PRU1_SD_CLK_INV5	PRU1_SD_CLK_SEL5	
R/W-X		R/W-0h		R/W-X	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-212. ICSSG_PRU1_SD_CLK_SEL_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU1_FD_ZERO_MAX_5	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ZERO_MAX_LIMIT_5	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU1_FD_ZERO_MIN_5	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-212. ICSSG_PRU1_SD_CLK_SEL_REG5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU1_FD_ZERO_MIN_LI MIT_5	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU1_SD_ACC_SEL5	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU1_SD_CLK_INV5	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU1_SD_CLK_SEL5	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1h = pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

Table 15-213. Register Call Summary for ICSSG_PRU1_SD_CLK_SEL_REG5

PRU_ICSSG_CFG Registers

- [ICSSG_PRU1_SD_CLK_SEL_REG5 Register \(Offset = BCh\) \[reset = X\]: \[0\]](#)

15.5.42 ICSSG_PRU1_SD_SAMPLE_SIZE_REG5 Register (Offset = C0h) [reset = X]

ICSSG_PRU1_SD_SAMPLE_SIZE_REG5 is shown in [Figure 15-69](#) and described in [Table 15-215](#).

Return to [Summary Table](#).

PRU1 FD and Over Sample Size Register 5

Table 15-214.
ICSSG_PRU1_SD_SAMPLE_SIZE_REG5 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 60C0h
PRU_ICSSG1_PR1_CFG_SLV	0B12 60C0h

Figure 15-69. ICSSG_PRU1_SD_SAMPLE_SIZE_REG5 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRU1_FD_EN_5	PRU1_FD_ON_E_MAX_5	PRU1_FD_ONE_MAX_LIMIT_5				PRU1_FD_ON_E_MIN_5	
R/W-0h	R/W-0h	R/W-0h				R/W-0h	
15	14	13	12	11	10	9	8
PRU1_FD_ONE_MIN_LIMIT_5				PRU1_FD_WINDOW_SIZE_5			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
PRU1_SD_SAMPLE_SIZE5							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-215. ICSSG_PRU1_SD_SAMPLE_SIZE_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU1_FD_EN_5	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU1_FD_ONE_MAX_5	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ONE_MAX_LIMIT_5	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU1_FD_ONE_MIN_5	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-215. ICSSG_PRU1_SD_SAMPLE_SIZE_REG5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU1_FD_ONE_MIN_LIM IT_5	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU1_FD_WINDOW_SIZ E_5	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU1_SD_SAMPLE_SIZ E5	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3h, then the third clock after first 1 is detected, the VAL will get set.

Table 15-216. Register Call Summary for ICSSG_PRU1_SD_SAMPLE_SIZE_REG5

PRU_ICSSG_CFG Registers

- [ICSSG_PRU1_SD_SAMPLE_SIZE_REG5 Register \(Offset = C0h\) \[reset = X\]: \[0\]](#)

15.5.43 ICSSG_PRU1_SD_CLK_SEL_REG6 Register (Offset = C4h) [reset = X]

ICSSG_PRU1_SD_CLK_SEL_REG6 is shown in [Figure 15-70](#) and described in [Table 15-218](#).

Return to [Summary Table](#).

PRU1 FD, ACC and Clock Selection Register 6

**Table 15-217. ICSSG_PRU1_SD_CLK_SEL_REG6
Instances**

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 60C4h
PRU_ICSSG1_PR1_CFG_SLV	0B12 60C4h

Figure 15-70. ICSSG_PRU1_SD_CLK_SEL_REG6 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED	PRU1_FD_ZERO_MAX_6	PRU1_FD_ZERO_MAX_LIMIT_6				PRU1_FD_ZERO_MIN_6	
R/W-X	R/W-0h	R/W-0h				R/W-0h	
15	14	13	12	11	10	9	8
PRU1_FD_ZERO_MIN_LIMIT_6					RESERVED		
R/W-0h					R/W-X		
7	6	5	4	3	2	1	0
RESERVED		PRU1_SD_ACC_SEL6		RESERVED	PRU1_SD_CLK_INV6	PRU1_SD_CLK_SEL6	
R/W-X		R/W-0h		R/W-X	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-218. ICSSG_PRU1_SD_CLK_SEL_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU1_FD_ZERO_MAX_6	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ZERO_MAX_LIMIT_6	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU1_FD_ZERO_MIN_6	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-218. ICSSG_PRU1_SD_CLK_SEL_REG6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU1_FD_ZERO_MIN_LI MIT_6	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU1_SD_ACC_SEL6	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU1_SD_CLK_INV6	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU1_SD_CLK_SEL6	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1h = pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

Table 15-219. Register Call Summary for ICSSG_PRU1_SD_CLK_SEL_REG6

PRU_ICSSG_CFG Registers

- [ICSSG_PRU1_SD_CLK_SEL_REG6 Register \(Offset = C4h\) \[reset = X\]: \[0\]](#)

15.5.44 ICSSG_PRU1_SD_SAMPLE_SIZE_REG6 Register (Offset = C8h) [reset = X]

ICSSG_PRU1_SD_SAMPLE_SIZE_REG6 is shown in Figure 15-71 and described in Table 15-221.

Return to [Summary Table](#).

PRU1 FD and Over Sample Size Register 6

Table 15-220.
ICSSG_PRU1_SD_SAMPLE_SIZE_REG6 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 60C8h
PRU_ICSSG1_PR1_CFG_SLV	0B12 60C8h

Figure 15-71. ICSSG_PRU1_SD_SAMPLE_SIZE_REG6 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRU1_FD_EN_6	PRU1_FD_ON_E_MAX_6	PRU1_FD_ONE_MAX_LIMIT_6				PRU1_FD_ON_E_MIN_6	
R/W-0h	R/W-0h	R/W-0h				R/W-0h	
15	14	13	12	11	10	9	8
PRU1_FD_ONE_MIN_LIMIT_6				PRU1_FD_WINDOW_SIZE_6			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
PRU1_SD_SAMPLE_SIZE6							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-221. ICSSG_PRU1_SD_SAMPLE_SIZE_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU1_FD_EN_6	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU1_FD_ONE_MAX_6	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ONE_MAX_LIMIT_6	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU1_FD_ONE_MIN_6	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-221. ICSSG_PRU1_SD_SAMPLE_SIZE_REG6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU1_FD_ONE_MIN_LIM IT_6	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU1_FD_WINDOW_SIZ E_6	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU1_SD_SAMPLE_SIZ E6	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3h, then the third clock after first 1 is detected, the VAL will get set.

Table 15-222. Register Call Summary for ICSSG_PRU1_SD_SAMPLE_SIZE_REG6

PRU_ICSSG_CFG Registers

- [ICSSG_PRU1_SD_SAMPLE_SIZE_REG6 Register \(Offset = C8h\) \[reset = X\]: \[0\]](#)

15.5.45 ICSSG_PRU1_SD_CLK_SEL_REG7 Register (Offset = CCh) [reset = X]

ICSSG_PRU1_SD_CLK_SEL_REG7 is shown in [Figure 15-72](#) and described in [Table 15-224](#).

Return to [Summary Table](#).

PRU1 FD, ACC and Clock Selection Register 7

**Table 15-223. ICSSG_PRU1_SD_CLK_SEL_REG7
Instances**

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 60CCh
PRU_ICSSG1_PR1_CFG_SLV	0B12 60CCh

Figure 15-72. ICSSG_PRU1_SD_CLK_SEL_REG7 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED	PRU1_FD_ZERO_MAX_7	PRU1_FD_ZERO_MAX_LIMIT_7					PRU1_FD_ZERO_MIN_7
R/W-X	R/W-0h	R/W-0h					R/W-0h
15	14	13	12	11	10	9	8
PRU1_FD_ZERO_MIN_LIMIT_7					RESERVED		
R/W-0h					R/W-X		
7	6	5	4	3	2	1	0
RESERVED		PRU1_SD_ACC_SEL7		RESERVED	PRU1_SD_CLK_INV7	PRU1_SD_CLK_SEL7	
R/W-X		R/W-0h		R/W-X	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-224. ICSSG_PRU1_SD_CLK_SEL_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU1_FD_ZERO_MAX_7	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ZERO_MAX_LIMIT_7	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU1_FD_ZERO_MIN_7	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-224. ICSSG_PRU1_SD_CLK_SEL_REG7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU1_FD_ZERO_MIN_LI MIT_7	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU1_SD_ACC_SEL7	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU1_SD_CLK_INV7	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU1_SD_CLK_SEL7	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1h = pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

Table 15-225. Register Call Summary for ICSSG_PRU1_SD_CLK_SEL_REG7

PRU_ICSSG_CFG Registers

- [ICSSG_PRU1_SD_CLK_SEL_REG7 Register \(Offset = CCh\) \[reset = X\]: \[0\]](#)

15.5.46 ICSSG_PRU1_SD_SAMPLE_SIZE_REG7 Register (Offset = D0h) [reset = X]

ICSSG_PRU1_SD_SAMPLE_SIZE_REG7 is shown in Figure 15-73 and described in Table 15-227.

Return to [Summary Table](#).

PRU1 FD and Over Sample Size Register 7

Table 15-226.
ICSSG_PRU1_SD_SAMPLE_SIZE_REG7 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 60D0h
PRU_ICSSG1_PR1_CFG_SLV	0B12 60D0h

Figure 15-73. ICSSG_PRU1_SD_SAMPLE_SIZE_REG7 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRU1_FD_EN_7	PRU1_FD_ON_E_MAX_7	PRU1_FD_ONE_MAX_LIMIT_7				PRU1_FD_ON_E_MIN_7	
R/W-0h	R/W-0h	R/W-0h				R/W-0h	
15	14	13	12	11	10	9	8
PRU1_FD_ONE_MIN_LIMIT_7				PRU1_FD_WINDOW_SIZE_7			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
PRU1_SD_SAMPLE_SIZE7							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-227. ICSSG_PRU1_SD_SAMPLE_SIZE_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU1_FD_EN_7	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU1_FD_ONE_MAX_7	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ONE_MAX_LIMIT_7	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU1_FD_ONE_MIN_7	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-227. ICSSG_PRU1_SD_SAMPLE_SIZE_REG7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU1_FD_ONE_MIN_LIM IT_7	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU1_FD_WINDOW_SIZ E_7	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU1_SD_SAMPLE_SIZ E7	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3h, then the third clock after first 1 is detected, the VAL will get set.

Table 15-228. Register Call Summary for ICSSG_PRU1_SD_SAMPLE_SIZE_REG7

PRU_ICSSG_CFG Registers

- [ICSSG_PRU1_SD_SAMPLE_SIZE_REG7 Register \(Offset = D0h\) \[reset = X\]: \[0\]](#)

15.5.47 ICSSG_PRU1_SD_CLK_SEL_REG8 Register (Offset = D4h) [reset = X]

ICSSG_PRU1_SD_CLK_SEL_REG8 is shown in [Figure 15-74](#) and described in [Table 15-230](#).

Return to [Summary Table](#).

PRU1 FD, ACC and Clock Selection Register 8

**Table 15-229. ICSSG_PRU1_SD_CLK_SEL_REG8
Instances**

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 60D4h
PRU_ICSSG1_PR1_CFG_SLV	0B12 60D4h

Figure 15-74. ICSSG_PRU1_SD_CLK_SEL_REG8 Register

31		30		29		28		27		26		25		24	
RESERVED															
R/W-X															
23		22		21		20		19		18		17		16	
RESERVED		PRU1_FD_ZERO_MAX_8		PRU1_FD_ZERO_MAX_LIMIT_8										PRU1_FD_ZERO_MIN_8	
R/W-X		R/W-0h		R/W-0h										R/W-0h	
15		14		13		12		11		10		9		8	
PRU1_FD_ZERO_MIN_LIMIT_8										RESERVED					
R/W-0h										R/W-X					
7		6		5		4		3		2		1		0	
RESERVED				PRU1_SD_ACC_SEL8				RESERVED		PRU1_SD_CLK_INV8		PRU1_SD_CLK_SEL8			
R/W-X				R/W-0h				R/W-X		R/W-0h		R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-230. ICSSG_PRU1_SD_CLK_SEL_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	PRU1_FD_ZERO_MAX_8	R/W	0h	Fast Detect Zero Count Max Threshold Hit The number of zeros in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ZERO_MAX_LIMIT_8	R/W	0h	Fast Detect Zero Count Max Threshold More than or Equal will assert fd_max_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU1_FD_ZERO_MIN_8	R/W	0h	Fast Detect Zero Count Min Threshold Hit The number of zeros in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-230. ICSSG_PRU1_SD_CLK_SEL_REG8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU1_FD_ZERO_MIN_LI MIT_8	R/W	0h	Fast Detect Zero Count Min Threshold Less than or Equal will assert fd_min_zero_hit 0h = 1 1h = 2 .. 1Fh = 32
10-6	RESERVED	R/W	X	
5-4	PRU1_SD_ACC_SEL8	R/W	0h	0h = acc3 is selected 1h = acc2 is selected 2h = acc1 is selected
3	RESERVED	R/W	X	
2	PRU1_SD_CLK_INV8	R/W	0h	Optional clock inversion post clock selection multiplexer 0h = No inversion 1h = Inversion
1-0	PRU1_SD_CLK_SEL8	R/W	0h	Selects the clock source 0h = pr1_pru<n>_pru_r31_in[16] Primary Input 1h = pr1_pru<n>_sd<m>_clk Primary Input 2h = pr1_pru<n>_sd0_clk Primary Input For sd0,sd1, and sd2 pr1_pru<n>_sd3_clk Primary Input For sd3,sd4, and sd5 pr1_pru<n>_sd6_clk Primary Input For sd6,sd7, and sd8 3h = Reserved

Table 15-231. Register Call Summary for ICSSG_PRU1_SD_CLK_SEL_REG8

PRU_ICSSG_CFG Registers

- [ICSSG_PRU1_SD_CLK_SEL_REG8 Register \(Offset = D4h\) \[reset = X\]: \[0\]](#)

15.5.48 ICSSG_PRU1_SD_SAMPLE_SIZE_REG8 Register (Offset = D8h) [reset = X]

ICSSG_PRU1_SD_SAMPLE_SIZE_REG8 is shown in Figure 15-75 and described in Table 15-233.

Return to [Summary Table](#).

PRU1 FD and Over Sample Size Register 8

Table 15-232.
ICSSG_PRU1_SD_SAMPLE_SIZE_REG8 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 60D8h
PRU_ICSSG1_PR1_CFG_SLV	0B12 60D8h

Figure 15-75. ICSSG_PRU1_SD_SAMPLE_SIZE_REG8 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRU1_FD_EN_8	PRU1_FD_ON_E_MAX_8	PRU1_FD_ONE_MAX_LIMIT_8				PRU1_FD_ON_E_MIN_8	
R/W-0h	R/W-0h	R/W-0h				R/W-0h	
15	14	13	12	11	10	9	8
PRU1_FD_ONE_MIN_LIMIT_8				PRU1_FD_WINDOW_SIZE_8			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
PRU1_SD_SAMPLE_SIZE8							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-233. ICSSG_PRU1_SD_SAMPLE_SIZE_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	PRU1_FD_EN_8	R/W	0h	Fast Detect One Enable 0h = Disable The events will not assert 1h = Enabled The events can assert, the monitor/shift is active
22	PRU1_FD_ONE_MAX_8	R/W	0h	Fast Detect One Count Max Threshold Hit The number of ones in the sliding window is greater than or equal to threshold Write 1 to clear
21-17	PRU1_FD_ONE_MAX_LIMIT_8	R/W	0h	Fast Detect One Count Max Threshold Less than or Equal will assert fd_max_one_hit 0h = 1 1h = 2 .. 1Fh = 32
16	PRU1_FD_ONE_MIN_8	R/W	0h	Fast Detect One Count Min Threshold Hit The number of ones in the sliding window is less than or equal to threshold Write 1 to clear

Table 15-233. ICSSG_PRU1_SD_SAMPLE_SIZE_REG8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	PRU1_FD_ONE_MIN_LIM IT_8	R/W	0h	Fast Detect One Count Min Threshold Less than or Equal will assert fd_min_one_hit 0h = 1 1h = 2 .. 1Fh = 32
10-8	PRU1_FD_WINDOW_SIZ E_8	R/W	0h	Fast Detect Window Size The number of contiguous samples to monitor A 32-bit shift register is used for the monitor This defines the mask size of the count logic 0h = 4 1h = 8 .. 7h = 32
7-0	PRU1_SD_SAMPLE_SIZ E8	R/W	0h	Over Sample Rate Sample size; how many samples to take before shadow register updated and flag set. The effect count is (sample_size + 1) 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 Nh = Over Sample of N + 1 Note: SB detection uses OVER_SAMPLE_SIZE to determine when to set first VAL flag after first 1 is sampled. It will be set after Over Sample Rate count For example, if OSR is set to 3h, then the third clock after first 1 is detected, the VAL will get set.

Table 15-234. Register Call Summary for ICSSG_PRU1_SD_SAMPLE_SIZE_REG8

PRU_ICSSG_CFG Registers

- [ICSSG_PRU1_SD_SAMPLE_SIZE_REG8 Register \(Offset = D8h\) \[reset = X\]: \[0\]](#)

15.5.49 ICSSG_PRU0_ED_RX_CFG_REG Register (Offset = E0h) [reset = X]

ICSSG_PRU0_ED_RX_CFG_REG is shown in Figure 15-76 and described in Table 15-236.

Return to [Summary Table](#).

PRU0 ED Receive Global Configuration Register

Table 15-235. ICSSG_PRU0_ED_RX_CFG_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 60E0h
PRU_ICSSG1_PR1_CFG_SLV	0B12 60E0h

Figure 15-76. ICSSG_PRU0_ED_RX_CFG_REG Register

31	30	29	28	27	26	25	24
PRU0_ED_RX_DIV_FACTOR							
R/W-0h							
23	22	21	20	19	18	17	16
PRU0_ED_RX_DIV_FACTOR							
R/W-0h							
15	14	13	12	11	10	9	8
PRU0_ED_RX_DIV_FACTOR_FRAC	RESERVED						
R/W-0h	R/W-X						
7	6	5	4	3	2	1	0
RESERVED			PRU0_ED_RX_CLK_SEL	PRU0_ED_RX_SB_POL	PRU0_ED_RX_SAMPLE_SIZE		
R/W-X			R/W-0h	R/W-1h	R/W-7h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-236. ICSSG_PRU0_ED_RX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PRU0_ED_RX_DIV_FACTOR OR	R/W	0h	Div factor for divh16 0h = div 1 1h = div 2 Nh = div (N+1) This divh16 is post divfrac, the effective rate will be Effective rate is 1.5 X main div if frac enabled Effective rate is 1.0 X main div if frac disabled For example , divh16 set to 3h Div by 6 if frac enabled Div by 4 if frac enabled For example , divh16 set to 4 Div by 7.5 if frac enabled Div by 5 if frac enabled
15	PRU0_ED_RX_DIV_FACTOR_FRAC	R/W	0h	Enable Fractional division before the divh16 0h = div 1 1h = div 1.5
14-5	RESERVED	R/W	X	
4	PRU0_ED_RX_CLK_SEL	R/W	0h	Selects the clock source for the divh16fr 0 =192 MHz, the uart_clk 1h = 200 MHz, the ICSSGn_CORE_CLK

Table 15-236. ICSSG_PRU0_ED_RX_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PRU0_ED_RX_SB_POL	R/W	1h	Defines the polarity of the RX Start Bit 0h = 0 1h = 1 Reset/default state
2-0	PRU0_ED_RX_SAMPLE_SIZE	R/W	7h	Over Sample size This defines the number of samples before the shadow copy gets updated and the VAL flag gets set The effect count is (sample_size + 1) 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 6 = Over Sample of 7 7 = Over Sample of 8 Note: the Over Sample Clock rate divided by the 1x Clock rate must equal the Over Sample size.

Table 15-237. Register Call Summary for ICSSG_PRU0_ED_RX_CFG_REG

PRU_ICSSG_CFG Registers
ICSSG_PRU0_ED_RX_CFG_REG Register (Offset = E0h) [reset = X]: [0]
PRU_ICSSG PRU Cores
General-Purpose Inputs (R31): Enhanced PRU GP Module: [0] [1] [2] [3] [4]

15.5.50 ICSSG_PRU0_ED_TX_CFG_REG Register (Offset = E4h) [reset = X]

ICSSG_PRU0_ED_TX_CFG_REG is shown in Figure 15-77 and described in Table 15-239.

Return to [Summary Table](#).

PRU0 ED Transmit Global Configuration Register

Table 15-238. ICSSG_PRU0_ED_TX_CFG_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 60E4h
PRU_ICSSG1_PR1_CFG_SLV	0B12 60E4h

Figure 15-77. ICSSG_PRU0_ED_TX_CFG_REG Register

31	30	29	28	27	26	25	24
PRU0_ED_TX_DIV_FACTOR							
R/W-0h							
23	22	21	20	19	18	17	16
PRU0_ED_TX_DIV_FACTOR							
R/W-0h							
15	14	13	12	11	10	9	8
PRU0_ED_TX_DIV_FACTOR_FRAC	RESERVED				PRU0_ENDAT2_CLK_SYNC	PRU0_ENDAT1_CLK_SYNC	PRU0_ENDAT0_CLK_SYNC
R/W-0h	R/W-X				R-1h	R-1h	R-1h
7	6	5	4	3	2	1	0
PRU0_ED_BUS_Y_2	PRU0_ED_BUS_Y_1	PRU0_ED_BUS_Y_0	PRU0_ED_TX_CLK_SEL	RESERVED			
R-0h	R-0h	R-0h	R/W-0h	R/W-X			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-239. ICSSG_PRU0_ED_TX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PRU0_ED_TX_DIV_FACTOR	R/W	0h	Div factor for divh16 0h = div 1 1h = div 2 Nh = div (N+1) This divh16 is post divfrac, the effective rate will be Effective rate is 1.5 X main div if frac enabled Effective rate is 1.0 X main div if frac disabled For example , divh16 set to 3h Div by 6 if frac enabled Div by 4 if frac enabled For example , divh16 set to 4 Div by 7.5 if frac enabled Div by 5 if frac enabled
15	PRU0_ED_TX_DIV_FACTOR_FRAC	R/W	0h	Enable Fractional division before the divh16 0h = div 1 1h = div 1.5
14-11	RESERVED	R/W	X	
10	PRU0_ENDAT2_CLK_SYNC	R	1h	Observation of pru<n>_endat2_clk pin state

Table 15-239. ICSSG_PRU0_ED_TX_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	PRU0_ENDAT1_CLK_SY NC	R	1h	Observation of pru<n>_endat1_clk pin state
8	PRU0_ENDAT0_CLK_SY NC	R	1h	Observation of pru<n>_endat0_clk pin state
7	PRU0_ED_BUSY_2	R	0h	Determines when you can assert tx go for channel 2 0h = Not busy ready to go 1h = Busy not ready to go Can be used to determine when it issue a new TX frame
6	PRU0_ED_BUSY_1	R	0h	Determines when you can assert tx go for channel 1 0h = Not busy ready to go 1h = Busy not ready to go Can be used to determine when it issue a new TX frame
5	PRU0_ED_BUSY_0	R	0h	Determines when you can assert tx go for channel 0 0h = Not busy ready to go 1h = Busy not ready to go Can be used to determine when it issue a new TX frame
4	PRU0_ED_TX_CLK_SEL	R/W	0h	Selects the clock source for the divh16fr 0h = 192 MHz, the uart_clk 1h = 200 MHz, the ICSSGn_CORE_CLK
3-0	RESERVED	R/W	X	

Table 15-240. Register Call Summary for ICSSG_PRU0_ED_TX_CFG_REG

PRU_ICSSG_CFG Registers

- [ICSSG_PRU0_ED_TX_CFG_REG Register \(Offset = E4h\) \[reset = X\]: \[0\]](#)

PRU_ICSSG PRU Cores

- [General-Purpose Inputs \(R31\): Enhanced PRU GP Module: \[0\] \[1\] \[2\] \[3\]](#)

15.5.51 ICSSG_PRU0_ED_CH0_CFG0_REG Register (Offset = E8h) [reset = 0h]

ICSSG_PRU0_ED_CH0_CFG0_REG is shown in Figure 15-78 and described in Table 15-242.

Return to [Summary Table](#).

PRU0 ED Channel 0 Configuration 0 Register

Table 15-241. ICSSG_PRU0_ED_CH0_CFG0_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 60E8h
PRU_ICSSG1_PR1_CFG_SLV	0B12 60E8h

Figure 15-78. ICSSG_PRU0_ED_CH0_CFG0_REG Register

31	30	29	28	27	26	25	24
PRU0_ED_TX_FIFO_SWAP_BITS0	PRU0_ED_SW_CLK_OUT0	PRU0_ED_CLK_OUT_OVR_EN0	PRU0_ED_RX_SNOOP0	PRU0_ED_RX_FRAME_SIZE0			
R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h			
23	22	21	20	19	18	17	16
PRU0_ED_RX_FRAME_SIZE0							
R/W-0h							
15	14	13	12	11	10	9	8
PRU0_ED_TX_FRAME_SIZE0					PRU0_ED_TX_WDLY0		
R/W-0h					R/W-0h		
7	6	5	4	3	2	1	0
PRU0_ED_TX_WDLY0							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-242. ICSSG_PRU0_ED_CH0_CFG0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRU0_ED_TX_FIFO_SWAP_BITS0	R/W	0h	This enables the swapping of the bits when they are loaded into the TX FIFO. 0h = no swap [7:0] -> [7:0] 1h = swap [7:0] -> [0:7]
30	PRU0_ED_SW_CLK_OUT0	R/W	0h	This controls the state of pru<n>_endat<m>_clk when endat_clk_out_override_en is set
29	PRU0_ED_CLK_OUT_OVR_EN0	R/W	0h	When set, this gives the software the ability to have direct control of pru<n>_endat<m>_clk. CAREFUL consideration to not override clock during free running mode of this will cause clock duty cycle violation.
28	PRU0_ED_RX_SNOOP0	R	0h	Direct Read of pru<n>_endat<m>_in state

Table 15-242. ICSSG_PRU0_ED_CH0_CFG0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27-16	PRU0_ED_RX_FRAME_SIZE0	R/W	0h	RX frame size, after SB is detected 0h = Special case for TX only phase, ignores SB, in this case tx_clk out will stop after last TX 1h = tx_clk out will stop after 1 X Over Sample 8 = tx_clk out will stop after 8 X Over Sample 9 = tx_clk out will stop after 9 X Over Sample . . 4095 tx_clk out will stop after 2047 X Over Sample Note: X Over Sample means the number of VAL events 1 VAL per Over Sample event When the TX CLOCK MODE is either 00 or 01, when this rx frame size is reached the tx controller clock out will remain high or low RULE: The software should not de-assert rx_en before rx_frame_size expires
15-11	PRU0_ED_TX_FRAME_SIZE0	R/W	0h	TX frame size 0h = disabled, the FIFO will transmit until empty then stop 1h = TX FIFO will transmit 1 bits then stop 2h = TX FIFO will transmit 2 bits then stop 8 = TX FIFO will transmit 8 bits then stop 9 = TX FIFO will transmit 9 bits then stop . . 31h = TX FIFO will transmit 31 bits then stop Note: when TX stop. Then endat<n>_out_en will de-assert
10-0	PRU0_ED_TX_WDLY0	R/W	0h	EnDAT TX wire delay using 200 MHz steps (CORE clock). Software should program a number divisible by 5. (Hw) 0h = no delay 5h = 5 ns delay Ah = 10 ns delay Fh = 15 ns delay 7FDh = 2.045 us delay This is used during TX state when CLK_OUT goes from high to low, this transmission can be compensated Hardware will keep count of clocks and add 5 each time. Note: the first rising edge of EnDAT CLK from a TX GO event is ED_TX_WDLY + ED_TST_DELAY_COUNTER + ½ EnDAT CLK period +/- 15 ns

Table 15-243. Register Call Summary for ICSSG_PRU0_ED_CH0_CFG0_REG

PRU_ICSSG_CFG Registers

- [ICSSG_PRU0_ED_CH0_CFG0_REG Register \(Offset = E8h\) \[reset = 0h\]: \[0\]](#)

15.5.52 ICSSG_PRU0_ED_CH0_CFG1_REG Register (Offset = ECh) [reset = 0h]

ICSSG_PRU0_ED_CH0_CFG1_REG is shown in Figure 15-79 and described in Table 15-245.

Return to [Summary Table](#).

PRU0 ED Channel 0 Configuration 1 Register

Table 15-244. ICSSG_PRU0_ED_CH0_CFG1_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 60ECh
PRU_ICSSG1_PR1_CFG_SLV	0B12 60ECh

Figure 15-79. ICSSG_PRU0_ED_CH0_CFG1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRU0_ED_RX_EN_COUNTER0															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRU0_ED_TST_DELAY_COUNTER0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-245. ICSSG_PRU0_ED_CH0_CFG1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PRU0_ED_RX_EN_COUNTER0	R/W	0h	This counter will start counting after the last TX bit is sent and when it expires the HW will automatically arm the receiver (rx_en = 1). Program to 0 if hardware support is not required. Counts in CORE cycles. Software should program value in increments of 5 (hardware will count by 5 s) For example 30, will be 6 ICSSGn_CORE_CLK cycles All channels must be use this feature if enabled. The HW does not allow support of some channels with auto enable and others manual enable. They can have different values , but all must be 0h or all none 0h
15-0	PRU0_ED_TST_DELAY_COUNTER0	R/W	0h	This counter will start after the tx_wire_delay has been met. After this counter expires the 1st transmit clock will be driven high. Counts in CORE cycles. Software programs value divisible by 5, and hardware will count by 5. For example 30, will be 6 ICSSGn_CORE_CLK cycles Note: the first rising edge of EnDAT CLK from a TX GO event is ED_TX_WDLY + ED_TST_DELAY_COUNTER + ½ EnDAT CLK period +/- 15 ns

Table 15-246. Register Call Summary for ICSSG_PRU0_ED_CH0_CFG1_REG

PRU_ICSSG_CFG Registers

- [ICSSG_PRU0_ED_CH0_CFG1_REG Register \(Offset = ECh\) \[reset = 0h\]: \[0\]](#)

15.5.53 ICSSG_PRU0_ED_CH1_CFG0_REG Register (Offset = F0h) [reset = 0h]

ICSSG_PRU0_ED_CH1_CFG0_REG is shown in Figure 15-80 and described in Table 15-248.

Return to [Summary Table](#).

PRU0 ED Channel 1 Configuration 0 Register

Table 15-247. ICSSG_PRU0_ED_CH1_CFG0_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 60F0h
PRU_ICSSG1_PR1_CFG_SLV	0B12 60F0h

Figure 15-80. ICSSG_PRU0_ED_CH1_CFG0_REG Register

31	30	29	28	27	26	25	24
PRU0_ED_TX_FIFO_SWAP_BITS1	PRU0_ED_SW_CLK_OUT1	PRU0_ED_CLK_OUT_OVERRIDE_EN1	PRU0_ED_RX_SNOOP1	PRU0_ED_RX_FRAME_SIZE1			
R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h			
23	22	21	20	19	18	17	16
PRU0_ED_RX_FRAME_SIZE1							
R/W-0h							
15	14	13	12	11	10	9	8
PRU0_ED_TX_FRAME_SIZE1					PRU0_ED_TX_WDLY1		
R/W-0h					R/W-0h		
7	6	5	4	3	2	1	0
PRU0_ED_TX_WDLY1							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-248. ICSSG_PRU0_ED_CH1_CFG0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRU0_ED_TX_FIFO_SWAP_BITS1	R/W	0h	This enables the swapping of the bits when they are loaded into the TX FIFO. 0h = no swap [7:0] -> [7:0] 1h = swap [7:0] -> [0:7]
30	PRU0_ED_SW_CLK_OUT1	R/W	0h	This controls the state of pru<n>_endat<m>_clk when endat_clk_out_override_en is set
29	PRU0_ED_CLK_OUT_OVERRIDE_EN1	R/W	0h	When set, this gives the software the ability to have direct control of pru<n>_endat<m>_clk. CAREFUL consideration to not override clock during free running mode of this will cause clock duty cycle violation.
28	PRU0_ED_RX_SNOOP1	R	0h	Direct Read of pru<n>_endat<m>_in state

Table 15-248. ICSSG_PRU0_ED_CH1_CFG0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27-16	PRU0_ED_RX_FRAME_SIZE1	R/W	0h	RX frame size, after SB is detected 0 = Special case for TX only phase, ignores SB, in this case tx_clk out will stop after last TX 1 = tx_clk out will stop after 1 X Over Sample 8 = tx_clk out will stop after 8 X Over Sample 9 = tx_clk out will stop after 9 X Over Sample . . 4095 tx_clk out will stop after 2047 X Over Sample Note: X Over Sample means the number of VAL events 1 VAL per Over Sample event When the TX CLOCK MODE is either 00 or 01, when this rx frame size is reached the tx controller clock out will remain high or low RULE: The software should not de-assert rx_en before rx_frame_size expires
15-11	PRU0_ED_TX_FRAME_SIZE1	R/W	0h	TX frame size 0h = disabled, the FIFO will transmit until empty then stop 1h = TX FIFO will transmit 1 bits then stop 2h = TX FIFO will transmit 2 bits then stop 8h = TX FIFO will transmit 8 bits then stop 9h = TX FIFO will transmit 9 bits then stop . . 31h = TX FIFO will transmit 31 bits then stop Note: when TX stop. Then endat<n>_out_en will de-assert
10-0	PRU0_ED_TX_WDLY1	R/W	0h	EnDAT TX wire delay using 200 MHz steps (CORE clock). Software should program a number divisible by 5. (Hw) 0h = no delay 5h = 5 ns delay Ah = 10 ns delay Fh = 15 ns delay 7FDh = 2.045 us delay This is used during TX state when CLK_OUT goes from high to low, this transmission can be compensated Hardware will keep count of clocks and add 5 each time. Note: the first rising edge of EnDAT CLK from a TX GO event is ED_TX_WDLY + ED_TST_DELAY_COUNTER + ½ EnDAT CLK period +/- 15 ns

Table 15-249. Register Call Summary for ICSSG_PRU0_ED_CH1_CFG0_REG

PRU_ICSSG_CFG Registers

- [ICSSG_PRU0_ED_CH1_CFG0_REG Register \(Offset = F0h\) \[reset = 0h\]: \[0\]](#)

15.5.54 ICSSG_PRU0_ED_CH1_CFG1_REG Register (Offset = F4h) [reset = 0h]

ICSSG_PRU0_ED_CH1_CFG1_REG is shown in Figure 15-81 and described in Table 15-251.

Return to [Summary Table](#).

PRU0 ED Channel 1 Configuration 1 Register

Table 15-250. ICSSG_PRU0_ED_CH1_CFG1_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 60F4h
PRU_ICSSG1_PR1_CFG_SLV	0B12 60F4h

Figure 15-81. ICSSG_PRU0_ED_CH1_CFG1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRU0_ED_RX_EN_COUNTER1															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRU0_ED_TST_DELAY_COUNTER1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-251. ICSSG_PRU0_ED_CH1_CFG1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PRU0_ED_RX_EN_COUNTER1	R/W	0h	This counter will start counting after the last TX bit is sent and when it expires the HW will automatically arm the receiver (rx_en = 1). Program to 0 if hardware support is not required. Counts in CORE cycles. Software should program value in increments of 5 (hardware will count by 5 s) For example 30, will be 6 ICSSGn_CORE_CLK cycles All channels must be use this feature if enabled. The HW does not allow support of some channels with auto enable and others manual enable. They can have different values , but all must be 0h or all none 0h
15-0	PRU0_ED_TST_DELAY_COUNTER1	R/W	0h	This counter will start after the tx_wire_delay has been met. After this counter expires the 1st transmit clock will be driven high. Counts in CORE cycles. Software programs value divisible by 5, and hardware will count by 5. For example 30, will be 6 ICSSGn_CORE_CLK cycles Note: the first rising edge of EnDAT CLK from a TX GO event is ED_TX_WDLY + ED_TST_DELAY_COUNTER + ½ EnDAT CLK period +/- 15 ns

Table 15-252. Register Call Summary for ICSSG_PRU0_ED_CH1_CFG1_REG

PRU_ICSSG_CFG Registers

- [ICSSG_PRU0_ED_CH1_CFG1_REG Register \(Offset = F4h\) \[reset = 0h\]: \[0\]](#)

15.5.55 ICSSG_PRU0_ED_CH2_CFG0_REG Register (Offset = F8h) [reset = 0h]

ICSSG_PRU0_ED_CH2_CFG0_REG is shown in Figure 15-82 and described in Table 15-254.

Return to [Summary Table](#).

PRU0 ED Channel 2 Configuration 0 Register

Table 15-253. ICSSG_PRU0_ED_CH2_CFG0_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 60F8h
PRU_ICSSG1_PR1_CFG_SLV	0B12 60F8h

Figure 15-82. ICSSG_PRU0_ED_CH2_CFG0_REG Register

31	30	29	28	27	26	25	24
PRU0_ED_TX_FIFO_SWAP_BITS2	PRU0_ED_SW_CLK_OUT2	PRU0_ED_CLK_OUT_OVERRIDE_N2	PRU0_ED_RX_SNOOP2	PRU0_ED_RX_FRAME_SIZE2			
R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h			
23	22	21	20	19	18	17	16
PRU0_ED_RX_FRAME_SIZE2							
R/W-0h							
15	14	13	12	11	10	9	8
PRU0_ED_TX_FRAME_SIZE2					PRU0_ED_TX_WDLY2		
R/W-0h					R/W-0h		
7	6	5	4	3	2	1	0
PRU0_ED_TX_WDLY2							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-254. ICSSG_PRU0_ED_CH2_CFG0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRU0_ED_TX_FIFO_SWAP_BITS2	R/W	0h	This enables the swapping of the bits when they are loaded into the TX FIFO. 0h = no swap [7:0] -> [7:0] 1h = swap [7:0] -> [0:7]
30	PRU0_ED_SW_CLK_OUT2	R/W	0h	This controls the state of pru<n>_endat<m>_clk when endat_clk_out_override_en is set
29	PRU0_ED_CLK_OUT_OVERRIDE_EN2	R/W	0h	When set, this gives the software the ability to have direct control of pru<n>_endat<m>_clk. CAREFUL consideration to not override clock during free running mode of this will cause clock duty cycle violation.
28	PRU0_ED_RX_SNOOP2	R	0h	Direct Read of pru<n>_endat<m>_in state

Table 15-254. ICSSG_PRU0_ED_CH2_CFG0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27-16	PRU0_ED_RX_FRAME_SIZE2	R/W	0h	RX frame size, after SB is detected 0 = Special case for TX only phase, ignores SB, in this case tx_clk out will stop after last TX 1 = tx_clk out will stop after 1 X Over Sample 8 = tx_clk out will stop after 8 X Over Sample 9 = tx_clk out will stop after 9 X Over Sample . . 4095 tx_clk out will stop after 2047 X Over Sample Note: X Over Sample means the number of VAL events 1 VAL per Over Sample event When the TX CLOCK MODE is either 00 or 01, when this rx frame size is reached the tx controller clock out will remain high or low RULE: The software should not de-assert rx_en before rx_frame_size expires
15-11	PRU0_ED_TX_FRAME_SIZE2	R/W	0h	TX frame size 0h = disabled, the FIFO will transmit until empty then stop 1h = TX FIFO will transmit 1 bits then stop 2h = TX FIFO will transmit 2 bits then stop 8h = TX FIFO will transmit 8 bits then stop 9h = TX FIFO will transmit 9 bits then stop . . 31h = TX FIFO will transmit 31 bits then stop Note: when TX stop. Then endat<n>_out_en will de-assert
10-0	PRU0_ED_TX_WDLY2	R/W	0h	EnDAT TX wire delay using 200 MHz steps (CORE clock). Software should program a number divisible by 5. (Hw) 0h = no delay 5h = 5 ns delay Ah = 10 ns delay Fh = 15 ns delay 7FDh = 2.045 us delay This is used during TX state when CLK_OUT goes from high to low, this transmission can be compensated Hardware will keep count of clocks and add 5 each time. Note: the first rising edge of EnDAT CLK from a TX GO event is ED_TX_WDLY + ED_TST_DELAY_COUNTER + ½ EnDAT CLK period +/- 15 ns

Table 15-255. Register Call Summary for ICSSG_PRU0_ED_CH2_CFG0_REG

PRU_ICSSG_CFG Registers

- [ICSSG_PRU0_ED_CH2_CFG0_REG Register \(Offset = F8h\) \[reset = 0h\]: \[0\]](#)

15.5.56 ICSSG_PRU0_ED_CH2_CFG1_REG Register (Offset = FCh) [reset = 0h]

ICSSG_PRU0_ED_CH2_CFG1_REG is shown in Figure 15-83 and described in Table 15-257.

Return to [Summary Table](#).

PRU0 ED Channel 2 Configuration 1 Register

Table 15-256. ICSSG_PRU0_ED_CH2_CFG1_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 60FCh
PRU_ICSSG1_PR1_CFG_SLV	0B12 60FCh

Figure 15-83. ICSSG_PRU0_ED_CH2_CFG1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRU0_ED_RX_EN_COUNTER2															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRU0_ED_TST_DELAY_COUNTER2															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-257. ICSSG_PRU0_ED_CH2_CFG1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PRU0_ED_RX_EN_COUNTER2	R/W	0h	This counter will start counting after the last TX bit is sent and when it expires the HW will automatically arm the receiver (rx_en = 1). Program to 0 if hardware support is not required. Counts in CORE cycles. Software should program value in increments of 5 (hardware will count by 5s) For example 30, will be 6 ICSSGn_CORE_CLK cycles All channels must be use this feature if enabled. The HW does not allow support of some channels with auto enable and others manual enable. They can have different values , but all must be 0h or all none 0h
15-0	PRU0_ED_TST_DELAY_COUNTER2	R/W	0h	This counter will start after the tx_wire_delay has been met. After this counter expires the 1st transmit clock will be driven high. Counts in CORE cycles. Software programs value divisible by 5, and hardware will count by 5. For example 30, will be 6 ICSSGn_CORE_CLK cycles Note: the first rising edge of EnDAT CLK from a TX GO event is ED_TX_WDLY + ED_TST_DELAY_COUNTER + ½ EnDAT CLK period +/- 15 ns

Table 15-258. Register Call Summary for ICSSG_PRU0_ED_CH2_CFG1_REG

PRU_ICSSG_CFG Registers

- [ICSSG_PRU0_ED_CH2_CFG1_REG Register \(Offset = FCh\) \[reset = 0h\]: \[0\]](#)

15.5.57 ICSSG_PRU1_ED_RX_CFG_REG Register (Offset = 100h) [reset = X]

ICSSG_PRU1_ED_RX_CFG_REG is shown in Figure 15-84 and described in Table 15-260.

Return to [Summary Table](#).

PRU1 ED Receive Global Configuration Register.

Table 15-259. ICSSG_PRU1_ED_RX_CFG_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6100h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6100h

Figure 15-84. ICSSG_PRU1_ED_RX_CFG_REG Register

31	30	29	28	27	26	25	24
PRU1_ED_RX_DIV_FACTOR							
R/W-0h							
23	22	21	20	19	18	17	16
PRU1_ED_RX_DIV_FACTOR							
R/W-0h							
15	14	13	12	11	10	9	8
PRU1_ED_RX_DIV_FACTOR_FRAC	RESERVED						
R/W-0h	R/W-X						
7	6	5	4	3	2	1	0
RESERVED			PRU1_ED_RX_CLK_SEL	PRU1_ED_RX_SB_POL	PRU1_ED_RX_SAMPLE_SIZE		
R/W-X			R/W-0h	R/W-1h	R/W-7h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-260. ICSSG_PRU1_ED_RX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PRU1_ED_RX_DIV_FACTOR OR	R/W	0h	div factor for divh16 0h = div 1 1h = div 2 Nh = div (N+1) This divh16 is post divfrac, the effective rate will be Effective rate is 1.5 X main div if frac enabled Effective rate is 1.0 X main div if frac disabled For example , divh16 set to 3h Div by 6 if frac enabled Div by 4 if frac enabled For example , divh16 set to 4 Div by 7.5 if frac enabled Div by 5 if frac enabled
15	PRU1_ED_RX_DIV_FACTOR_FRAC	R/W	0h	Enable Fractional division before the divh16 0h = div 1 1h = div 1.5
14-5	RESERVED	R/W	X	
4	PRU1_ED_RX_CLK_SEL	R/W	0h	Selects the clock source for the divh16fr 0h = 192 MHz, the uart_clk 1h = 200 MHz, the ICSSGn_CORE_CLK

Table 15-260. ICSSG_PRU1_ED_RX_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PRU1_ED_RX_SB_POL	R/W	1h	Defines the polarity of the RX Start Bit 0h = 0 1h = 1 Reset/default state
2-0	PRU1_ED_RX_SAMPLE_SIZE	R/W	7h	Over Sample size This defines the number of samples before the shadow copy gets updated and the VAL flag gets set The effect count is (sample_size + 1) 0h = Reserved 1h = Reserved 2h = Reserved 3h = Over Sample of 4 4h = Over Sample of 5 5h = Over Sample of 6 6h = Over Sample of 7 7h = Over Sample of 8 Note: the Over Sample Clock rate divided by the 1x Clock rate must equal the Over Sample size.

Table 15-261. Register Call Summary for ICSSG_PRU1_ED_RX_CFG_REG

PRU_ICSSG_CFG Registers

- [ICSSG_PRU1_ED_RX_CFG_REG Register \(Offset = 100h\) \[reset = X\]: \[0\]](#)

15.5.58 ICSSG_PRU1_ED_TX_CFG_REG Register (Offset = 104h) [reset = X]

ICSSG_PRU1_ED_TX_CFG_REG is shown in Figure 15-85 and described in Table 15-263.

Return to [Summary Table](#).

PRU1 ED Transmit Global Configuration Register.

Table 15-262. ICSSG_PRU1_ED_TX_CFG_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6104h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6104h

Figure 15-85. ICSSG_PRU1_ED_TX_CFG_REG Register

31	30	29	28	27	26	25	24
PRU0_ED_TX_DIV_FACTOR							
R/W-0h							
23	22	21	20	19	18	17	16
PRU0_ED_TX_DIV_FACTOR							
R/W-0h							
15	14	13	12	11	10	9	8
PRU0_ED_TX_DIV_FACTOR_FRAC	RESERVED				PRU0_ENDAT2_CLK_SYNC	PRU0_ENDAT1_CLK_SYNC	PRU0_ENDAT0_CLK_SYNC
R/W-0h	R/W-X				R-1h	R-1h	R-1h
7	6	5	4	3	2	1	0
PRU0_ED_BUS_Y_2	PRU0_ED_BUS_Y_1	PRU0_ED_BUS_Y_0	PRU0_ED_TX_CLK_SEL	RESERVED			
R-0h	R-0h	R-0h	R/W-0h	R/W-X			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-263. ICSSG_PRU1_ED_TX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PRU0_ED_TX_DIV_FACTOR	R/W	0h	Div factor for divh16 0h = div 1 1h = div 2 Nh = div (N+1) This divh16 is post divfrac, the effective rate will be Effective rate is 1.5 X main div if frac enabled Effective rate is 1.0 X main div if frac disabled For example , divh16 set to 3h Div by 6 if frac enabled Div by 4 if frac enabled For example , divh16 set to 4 Div by 7.5 if frac enabled Div by 5 if frac enabled
15	PRU0_ED_TX_DIV_FACTOR_FRAC	R/W	0h	Enable Fractional division before the divh16 0h = div 1 1h = div 1.5
14-11	RESERVED	R/W	X	
10	PRU0_ENDAT2_CLK_SYNC	R	1h	Observation of pru<n>_endat2_clk pin state

Table 15-263. ICSSG_PRU1_ED_TX_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	PRU0_ENDAT1_CLK_SY NC	R	1h	Observation of pru<n>_endat1_clk pin state
8	PRU0_ENDAT0_CLK_SY NC	R	1h	Observation of pru<n>_endat0_clk pin state
7	PRU0_ED_BUSY_2	R	0h	Determines when you can assert tx go for channel 2 0h = Not busy ready to go 1h = Busy not ready to go Can be used to determine when it issue a new TX frame
6	PRU0_ED_BUSY_1	R	0h	Determines when you can assert tx go for channel 1 0h = Not busy ready to go 1h = Busy not ready to go Can be used to determine when it issue a new TX frame
5	PRU0_ED_BUSY_0	R	0h	Determines when you can assert tx go for channel 0 0h = Not busy ready to go 1h = Busy not ready to go Can be used to determine when it issue a new TX frame
4	PRU0_ED_TX_CLK_SEL	R/W	0h	Selects the clock source for the divh16fr 0h = 192 MHz, the uart_clk 1h = 200 MHz, the ICSSGn_CORE_CLK
3-0	RESERVED	R/W	X	

Table 15-264. Register Call Summary for ICSSG_PRU1_ED_TX_CFG_REG

PRU_ICSSG_CFG Registers

- [ICSSG_PRU1_ED_TX_CFG_REG Register \(Offset = 104h\) \[reset = X\]: \[0\]](#)

15.5.59 ICSSG_PRU1_ED_CH0_CFG0_REG Register (Offset = 108h) [reset = 0h]

ICSSG_PRU1_ED_CH0_CFG0_REG is shown in Figure 15-86 and described in Table 15-266.

Return to [Summary Table](#).

PRU1 ED Channel 0 Configuration 0 Register.

Table 15-265. ICSSG_PRU1_ED_CH0_CFG0_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6108h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6108h

Figure 15-86. ICSSG_PRU1_ED_CH0_CFG0_REG Register

31	30	29	28	27	26	25	24
PRU1_ED_TX_FIFO_SWAP_BITS0	PRU1_ED_SW_CLK_OUT0	PRU1_ED_CLK_OUT_OVERRIDE_EN0	PRU1_ED_RX_SNOOP0	PRU1_ED_RX_FRAME_SIZE0			
R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h			
23	22	21	20	19	18	17	16
PRU1_ED_RX_FRAME_SIZE0							
R/W-0h							
15	14	13	12	11	10	9	8
PRU1_ED_TX_FRAME_SIZE0					PRU1_ED_TX_WDLY0		
R/W-0h					R/W-0h		
7	6	5	4	3	2	1	0
PRU1_ED_TX_WDLY0							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-266. ICSSG_PRU1_ED_CH0_CFG0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRU1_ED_TX_FIFO_SWAP_BITS0	R/W	0h	This enables the swapping of the bits when they are loaded into the TX FIFO. 0h = no swap [7:0] -> [7:0] 1h = swap [7:0] -> [0:7]
30	PRU1_ED_SW_CLK_OUT0	R/W	0h	This controls the state of pru<n>_endat<m>_clk when endat_clk_out_override_en is set
29	PRU1_ED_CLK_OUT_OVERRIDE_EN0	R/W	0h	When set, this gives the software the ability to have direct control of pru<n>_endat<m>_clk. CAREFUL consideration to not override clock during free running mode of this will cause clock duty cycle violation.
28	PRU1_ED_RX_SNOOP0	R	0h	Direct Read of pru<n>_endat<m>_in state

Table 15-266. ICSSG_PRU1_ED_CH0_CFG0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27-16	PRU1_ED_RX_FRAME_SIZE0	R/W	0h	RX frame size, after SB is detected 0h = Special case for TX only phase, ignores SB, in this case tx_clk out will stop after last TX 1h = tx_clk out will stop after 1 X Over Sample 8 = tx_clk out will stop after 8 X Over Sample 9 = tx_clk out will stop after 9 X Over Sample . . 4095 tx_clk out will stop after 4095 X Over Sample Note: X Over Sample means the number of VAL events 1 VAL per Over Sample event When the TX CLOCK MODE is either 00 or 01, when this rx frame size is reached the tx controller clock out will remain high or low RULE: The software should not de-assert rx_en before rx_frame_size expires
15-11	PRU1_ED_TX_FRAME_SIZE0	R/W	0h	TX frame size 0h = disabled, the FIFO will transmit until empty then stop 1h = TX FIFO will transmit 1 bits then stop 2h = TX FIFO will transmit 2 bits then stop 8 = TX FIFO will transmit 8 bits then stop 9 = TX FIFO will transmit 9 bits then stop . . 31h = TX FIFO will transmit 31 bits then stop Note: when TX stop. Then endat<n>_out_en will de-assert
10-0	PRU1_ED_TX_WDLY0	R/W	0h	EnDAT TX wire delay using 200 MHz steps (CORE clock). Software should program a number divisible by 5. (Hw) 0h = no delay 5h = 5 ns delay Ah = 10 ns delay Fh = 15 ns delay 7FDh = 2.045 us delay This is used during TX state when CLK_OUT goes from high to low, this transmission can be compensated Hardware will keep count of clocks and add 5 each time. Note: the first rising edge of EnDAT CLK from a TX GO event is ED_TX_WDLY + ED_TST_DELAY_COUNTER + ½ EnDAT CLK period +/- 15 ns

Table 15-267. Register Call Summary for ICSSG_PRU1_ED_CH0_CFG0_REG

PRU_ICSSG_CFG Registers

- [ICSSG_PRU1_ED_CH0_CFG0_REG Register \(Offset = 108h\) \[reset = 0h\]: \[0\]](#)

15.5.60 ICSSG_PRU1_ED_CH0_CFG1_REG Register (Offset = 10Ch) [reset = 0h]

ICSSG_PRU1_ED_CH0_CFG1_REG is shown in Figure 15-87 and described in Table 15-269.

Return to [Summary Table](#).

PRU1 ED Channel 0 Configuration 1 Register.

Table 15-268. ICSSG_PRU1_ED_CH0_CFG1_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 610Ch
PRU_ICSSG1_PR1_CFG_SLV	0B12 610Ch

Figure 15-87. ICSSG_PRU1_ED_CH0_CFG1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRU1_ED_RX_EN_COUNTER0															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRU1_ED_TST_DELAY_COUNTER0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-269. ICSSG_PRU1_ED_CH0_CFG1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PRU1_ED_RX_EN_COUNTER0	R/W	0h	This counter will start counting after the last TX bit is sent and when it expires the HW will automatically arm the receiver (rx_en = 1). Program to 0h if hardware support is not required. Counts in CORE cycles. Software should program value in increments of 5 (hardware will count by 5 s) For example 30, will be 6 ICSSGn_CORE_CLK cycles All channels must use this feature if enabled. The HW does not allow support of some channels with auto enable and others manual enable. They can have different values , but all must be 0h or all none 0h
15-0	PRU1_ED_TST_DELAY_COUNTER0	R/W	0h	This counter will start after the tx_wire_delay has been met. After this counter expires the 1st transmit clock will be driven high. Counts in CORE cycles. Software programs value divisible by 5, and hardware will count by 5. For example 30, will be 6 ICSSGn_CORE_CLK cycles Note: the first rising edge of EnDAT CLK from a TX GO event is ED_TX_WDLY + ED_TST_DELAY_COUNTER + ½ EnDAT CLK period +/- 15 ns

Table 15-270. Register Call Summary for ICSSG_PRU1_ED_CH0_CFG1_REG

PRU_ICSSG_CFG Registers

- [ICSSG_PRU1_ED_CH0_CFG1_REG Register \(Offset = 10Ch\) \[reset = 0h\]: \[0\]](#)

15.5.61 ICSSG_PRU1_ED_CH1_CFG0_REG Register (Offset = 110h) [reset = 0h]

ICSSG_PRU1_ED_CH1_CFG0_REG is shown in Figure 15-88 and described in Table 15-272.

Return to [Summary Table](#).

PRU1 ED Channel 1 Configuration 0 Register.

Table 15-271. ICSSG_PRU1_ED_CH1_CFG0_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6110h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6110h

Figure 15-88. ICSSG_PRU1_ED_CH1_CFG0_REG Register

31	30	29	28	27	26	25	24
PRU1_ED_TX_FIFO_SWAP_BITS1	PRU1_ED_SW_CLK_OUT1	PRU1_ED_CLK_OUT_OVERRIDE_EN1	PRU1_ED_RX_SNOOP1	PRU1_ED_RX_FRAME_SIZE1			
R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h			
23	22	21	20	19	18	17	16
PRU1_ED_RX_FRAME_SIZE1							
R/W-0h							
15	14	13	12	11	10	9	8
PRU1_ED_TX_FRAME_SIZE1					PRU1_ED_TX_WDLY1		
R/W-0h					R/W-0h		
7	6	5	4	3	2	1	0
PRU1_ED_TX_WDLY1							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-272. ICSSG_PRU1_ED_CH1_CFG0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRU1_ED_TX_FIFO_SWAP_BITS1	R/W	0h	This enables the swapping of the bits when they are loaded into the TX FIFO. 0h = no swap [7:0] -> [7:0] 1h = swap [7:0] -> [0:7]
30	PRU1_ED_SW_CLK_OUT1	R/W	0h	This controls the state of pru<n>_endat<m>_clk when endat_clk_out_override_en is set
29	PRU1_ED_CLK_OUT_OVERRIDE_EN1	R/W	0h	When set, this gives the software the ability to have direct control of pru<n>_endat<m>_clk. CAREFUL consideration to not override clock during free running mode of this will cause clock duty cycle violation.
28	PRU1_ED_RX_SNOOP1	R	0h	Direct Read of pru<n>_endat<m>_in state

Table 15-272. ICSSG_PRU1_ED_CH1_CFG0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27-16	PRU1_ED_RX_FRAME_SIZE1	R/W	0h	RX frame size, after SB is detected 0h = Special case for TX only phase, ignores SB, in this case tx_clk out will stop after last TX 1 = tx_clk out will stop after 1 X Over Sample 8 = tx_clk out will stop after 8 X Over Sample 9 = tx_clk out will stop after 9 X Over Sample . . 4095 tx_clk out will stop after 2047 X Over Sample Note: X Over Sample means the number of VAL events 1 VAL per Over Sample event When the TX CLOCK MODE is either 00 or 01, when this rx frame size is reached the tx controller clock out will remain high or low RULE: The software should not de-assert rx_en before rx_frame_size expires
15-11	PRU1_ED_TX_FRAME_SIZE1	R/W	0h	TX frame size 0h = disabled, the FIFO will transmit until empty then stop 1h = TX FIFO will transmit 1 bits then stop 2h = TX FIFO will transmit 2 bits then stop 8h = TX FIFO will transmit 8 bits then stop 9h = TX FIFO will transmit 9 bits then stop . . 31h = TX FIFO will transmit 31 bits then stop Note: when TX stop. Then endat<n>_out_en will de-assert
10-0	PRU1_ED_TX_WDLY1	R/W	0h	EnDAT TX wire delay using 200 MHz steps (CORE clock). Software should program a number divisible by 5. (Hw) 0h = no delay 5h = 5 ns delay Ah = 10 ns delay Fh = 15 ns delay 7FDh = 2.045 us delay This is used during TX state when CLK_OUT goes from high to low, this transmission can be compensated Hardware will keep count of clocks and add 5 each time. Note: the first rising edge of EnDAT CLK from a TX GO event is ED_TX_WDLY + ED_TST_DELAY_COUNTER + ½ EnDAT CLK period +/- 15 ns

Table 15-273. Register Call Summary for ICSSG_PRU1_ED_CH1_CFG0_REG

PRU_ICSSG_CFG Registers

- [ICSSG_PRU1_ED_CH1_CFG0_REG Register \(Offset = 110h\) \[reset = 0h\]: \[0\]](#)

15.5.62 ICSSG_PRU1_ED_CH1_CFG1_REG Register (Offset = 114h) [reset = 0h]

ICSSG_PRU1_ED_CH1_CFG1_REG is shown in Figure 15-89 and described in Table 15-275.

Return to [Summary Table](#).

PRU1 ED Channel 1 Configuration 1 Register.

Table 15-274. ICSSG_PRU1_ED_CH1_CFG1_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6114h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6114h

Figure 15-89. ICSSG_PRU1_ED_CH1_CFG1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRU1_ED_RX_EN_COUNTER1															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRU1_ED_TST_DELAY_COUNTER1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-275. ICSSG_PRU1_ED_CH1_CFG1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PRU1_ED_RX_EN_COUNTER1	R/W	0h	This counter will start counting after the last TX bit is sent and when it expires the HW will automatically arm the receiver (rx_en = 1). Program to 0 if hardware support is not required. Counts in CORE cycles. Software should program value in increments of 5 (hardware will count by 5s) For example 30, will be 6 ICSSGn_CORE_CLK cycles All channels must use this feature if enabled. The HW does not allow support of some channels with auto enable and others manual enable. They can have different values , but all must be 0h or all none 0h
15-0	PRU1_ED_TST_DELAY_COUNTER1	R/W	0h	This counter will start after the tx_wire_delay has been met. After this counter expires the 1st transmit clock will be driven high. Counts in CORE cycles. Software programs value divisible by 5, and hardware will count by 5. For example 30, will be 6 ICSSGn_CORE_CLK cycles Note the first rising edge of EnDAT CLK from a TX GO event is ED_TX_WDLY + ED_TST_DELAY_COUNTER + ½ EnDAT CLK period +/- 15 ns

Table 15-276. Register Call Summary for ICSSG_PRU1_ED_CH1_CFG1_REG

PRU_ICSSG_CFG Registers

- [ICSSG_PRU1_ED_CH1_CFG1_REG Register \(Offset = 114h\) \[reset = 0h\]: \[0\]](#)

15.5.63 ICSSG_PRU1_ED_CH2_CFG0_REG Register (Offset = 118h) [reset = 0h]

ICSSG_PRU1_ED_CH2_CFG0_REG is shown in Figure 15-90 and described in Table 15-278.

Return to [Summary Table](#).

PRU1 ED Channel 2 Configuration 0 Register.

Table 15-277. ICSSG_PRU1_ED_CH2_CFG0_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6118h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6118h

Figure 15-90. ICSSG_PRU1_ED_CH2_CFG0_REG Register

31	30	29	28	27	26	25	24
PRU1_ED_TX_FIFO_SWAP_BITS2	PRU1_ED_SW_CLK_OUT2	PRU1_ED_CLK_OUT_OVR_EN2	PRU1_ED_RX_SNOOP2	PRU1_ED_RX_FRAME_SIZE2			
R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h			
23	22	21	20	19	18	17	16
PRU1_ED_RX_FRAME_SIZE2							
R/W-0h							
15	14	13	12	11	10	9	8
PRU1_ED_TX_FRAME_SIZE2					PRU1_ED_TX_WDLY2		
R/W-0h					R/W-0h		
7	6	5	4	3	2	1	0
PRU1_ED_TX_WDLY2							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-278. ICSSG_PRU1_ED_CH2_CFG0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRU1_ED_TX_FIFO_SWAP_BITS2	R/W	0h	This enables the swapping of the bits when they are loaded into the TX FIFO. 0h = no swap [7:0] -> [7:0] 1h = swap [7:0] -> [0:7]
30	PRU1_ED_SW_CLK_OUT2	R/W	0h	This controls the state of pru<n>_endat<m>_clk when endat_clk_out_override_en is set
29	PRU1_ED_CLK_OUT_OVR_EN2	R/W	0h	When set, this gives the software the ability to have direct control of pru<n>_endat<m>_clk. CAREFUL consideration to not override clock during free running mode of this will cause clock duty cycle violation.
28	PRU1_ED_RX_SNOOP2	R	0h	Direct Read of pru<n>_endat<m>_in state

Table 15-278. ICSSG_PRU1_ED_CH2_CFG0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27-16	PRU1_ED_RX_FRAME_SIZE2	R/W	0h	RX frame size, after SB is detected 0h = Special case for TX only phase, ignores SB, in this case tx_clk out will stop after last TX 1 = tx_clk out will stop after 1 X Over Sample 8 = tx_clk out will stop after 8 X Over Sample 9 = tx_clk out will stop after 9 X Over Sample . . 4095 tx_clk out will stop after 2047 X Over Sample Note: X Over Sample means the number of VAL events 1 VAL per Over Sample event When the TX CLOCK MODE is either 00 or 01, when this rx frame size is reached the tx controller clock out will remain high or low RULE: The software should not de-assert rx_en before rx_frame_size expires
15-11	PRU1_ED_TX_FRAME_SIZE2	R/W	0h	TX frame size 0h = disabled, the FIFO will transmit until empty then stop 1h = TX FIFO will transmit 1 bits then stop 2h = TX FIFO will transmit 2 bits then stop 8h = TX FIFO will transmit 8 bits then stop 9h = TX FIFO will transmit 9 bits then stop . . 31h = TX FIFO will transmit 31 bits then stop Note: when TX stop. Then endat<n>_out_en will de-assert
10-0	PRU1_ED_TX_WDLY2	R/W	0h	EnDAT TX wire delay using 200 MHz steps (CORE clock). Software should program a number divisible by 5. (Hw) 0h = no delay 5h = 5 ns delay Ah = 10 ns delay Fh = 15 ns delay 7FDh = 2.045 us delay This is used during TX state when CLK_OUT goes from high to low, this transmission can be compensated Hardware will keep count of clocks and add 5 each time. Note: the first rising edge of EnDAT CLK from a TX GO event is ED_TX_WDLY + ED_TST_DELAY_COUNTER + ½ EnDAT CLK period +/- 15 ns

Table 15-279. Register Call Summary for ICSSG_PRU1_ED_CH2_CFG0_REG

PRU_ICSSG_CFG Registers

- [ICSSG_PRU1_ED_CH2_CFG0_REG Register \(Offset = 118h\) \[reset = 0h\]: \[0\]](#)

15.5.64 ICSSG_PRU1_ED_CH2_CFG1_REG Register (Offset = 11Ch) [reset = 0h]

ICSSG_PRU1_ED_CH2_CFG1_REG is shown in [Figure 15-91](#) and described in [Table 15-281](#).

Return to [Summary Table](#).

PRU1 ED Channel 2 Configuration 1 Register.

Table 15-280. ICSSG_PRU1_ED_CH2_CFG1_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 611Ch
PRU_ICSSG1_PR1_CFG_SLV	0B12 611Ch

Figure 15-91. ICSSG_PRU1_ED_CH2_CFG1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRU1_ED_RX_EN_COUNTER2															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRU1_ED_TST_DELAY_COUNTER2															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-281. ICSSG_PRU1_ED_CH2_CFG1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PRU1_ED_RX_EN_COUNTER2	R/W	0h	This counter will start counting after the last TX bit is sent and when it expires the HW will automatically arm the receiver (rx_en = 1). Program to 0 if hardware support is no required. Counts in CORE cycles. Software should program value in increments of 5 (hardware will count by 5 s) For example 30, will be 6 ICSSGn_CORE_CLK cycles All channels must use this feature if enabled. The HW does not allow support of some channels with auto enable and others manual enable. They can have different values , but all must be 0h or all none 0h
15-0	PRU1_ED_TST_DELAY_COUNTER2	R/W	0h	This counter will start after the tx_wire_delay has been met. After this counter expires the 1st transmit clock will be driven high. Counts in CORE cycles. Software programs value divisible by 5, and hardware will count by 5. For example 30, will be 6 ICSSGn_CORE_CLK cycles Note: the first rising edge of EnDAT CLK from a TX GO event is ED_TX_WDLY + ED_TST_DELAY_COUNTER + ½ EnDAT CLK period +/- 15 ns

Table 15-282. Register Call Summary for ICSSG_PRU1_ED_CH2_CFG1_REG

PRU_ICSSG_CFG Registers

- [ICSSG_PRU1_ED_CH2_CFG1_REG Register \(Offset = 11Ch\) \[reset = 0h\]: \[0\]](#)

15.5.65 ICSSG_RTU0_POKE_EN0_REG Register (Offset = 124h) [reset = 0h]

ICSSG_RTU0_POKE_EN0_REG is shown in Figure 15-92 and described in Table 15-284.

Return to [Summary Table](#).

RTU0 Poke Enable 0 Register.

Table 15-283. ICSSG_RTU0_POKE_EN0_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6124h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6124h

Figure 15-92. ICSSG_RTU0_POKE_EN0_REG Register

31	30	29	28	27	26	25	24
RTU0_POKE_R27_EN				RTU0_POKE_R26_EN			
R/W-0h				R/W-0h			
23	22	21	20	19	18	17	16
RTU0_POKE_R25_EN				RTU0_POKE_R24_EN			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
RTU0_POKE_R23_EN				RTU0_POKE_R22_EN			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
RTU0_POKE_R21_EN				RTU0_POKE_R20_EN			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-284. ICSSG_RTU0_POKE_EN0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RTU0_POKE_R27_EN	R/W	0h	This enables the external values to get poked into PRU's internal register [x] = 0 Disable poke for that byte [x] = 1 Enable poke for that byte
27-24	RTU0_POKE_R26_EN	R/W	0h	This enables the external values to get poked into PRU's internal register [x] = 0 Disable poke for that byte [x] = 1 Enable poke for that byte
23-20	RTU0_POKE_R25_EN	R/W	0h	This enables the external values to get poked into PRU's internal register [x] = 0 Disable poke for that byte [x] = 1 Enable poke for that byte
19-16	RTU0_POKE_R24_EN	R/W	0h	This enables the external values to get poked into PRU's internal register [x] = 0 Disable poke for that byte [x] = 1 Enable poke for that byte
15-12	RTU0_POKE_R23_EN	R/W	0h	This enables the external values to get poked into PRU's internal register [x] = 0 Disable poke for that byte [x] = 1 Enable poke for that byte

Table 15-284. ICSSG_RTU0_POKE_EN0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-8	RTU0_POKE_R22_EN	R/W	0h	This enables the external values to get poked into PRU's internal register [x] = 0 Disable poke for that byte [x] = 1 Enable poke for that byte
7-4	RTU0_POKE_R21_EN	R/W	0h	This enables the external values to get poked into PRU's internal register [x] = 0 Disable poke for that byte [x] = 1 Enable poke for that byte
3-0	RTU0_POKE_R20_EN	R/W	0h	This enables the external values to get poked into PRU's internal register [x] = 0 Disable poke for that byte [x] = 1 Enable poke for that byte

Table 15-285. Register Call Summary for ICSSG_RTU0_POKE_EN0_REG

PRU_ICSSG_CFG Registers

- [ICSSG_RTU0_POKE_EN0_REG Register \(Offset = 124h\) \[reset = 0h\]: \[0\]](#)

15.5.66 ICSSG_RTU1_POKE_EN0_REG Register (Offset = 12Ch) [reset = 0h]

ICSSG_RTU1_POKE_EN0_REG is shown in Figure 15-93 and described in Table 15-287.

Return to [Summary Table](#).

RTU1 Poke Enable 0 Register.

Table 15-286. ICSSG_RTU1_POKE_EN0_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 612Ch
PRU_ICSSG1_PR1_CFG_SLV	0B12 612Ch

Figure 15-93. ICSSG_RTU1_POKE_EN0_REG Register

31	30	29	28	27	26	25	24
RTU1_POKE_R27_EN				RTU1_POKE_R26_EN			
R/W-0h				R/W-0h			
23	22	21	20	19	18	17	16
RTU1_POKE_R25_EN				RTU1_POKE_R24_EN			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
RTU1_POKE_R23_EN				RTU1_POKE_R22_EN			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
RTU1_POKE_R21_EN				RTU1_POKE_R20_EN			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-287. ICSSG_RTU1_POKE_EN0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RTU1_POKE_R27_EN	R/W	0h	This enables the external values to get poked into PRU's internal register [x] = 0 Disable poke for that byte [x] = 1 Enable poke for that byte
27-24	RTU1_POKE_R26_EN	R/W	0h	This enables the external values to get poked into PRU's internal register [x] = 0 Disable poke for that byte [x] = 1 Enable poke for that byte
23-20	RTU1_POKE_R25_EN	R/W	0h	This enables the external values to get poked into PRU's internal register [x] = 0 Disable poke for that byte [x] = 1 Enable poke for that byte
19-16	RTU1_POKE_R24_EN	R/W	0h	This enables the external values to get poked into PRU's internal register [x] = 0 Disable poke for that byte [x] = 1 Enable poke for that byte
15-12	RTU1_POKE_R23_EN	R/W	0h	This enables the external values to get poked into PRU's internal register [x] = 0 Disable poke for that byte [x] = 1 Enable poke for that byte

Table 15-287. ICSSG_RTU1_POKE_EN0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-8	RTU1_POKE_R22_EN	R/W	0h	This enables the external values to get poked into PRU's internal register [x] = 0 Disable poke for that byte [x] = 1 Enable poke for that byte
7-4	RTU1_POKE_R21_EN	R/W	0h	This enables the external values to get poked into PRU's internal register [x] = 0 Disable poke for that byte [x] = 1 Enable poke for that byte
3-0	RTU1_POKE_R20_EN	R/W	0h	This enables the external values to get poked into PRU's internal register [x] = 0 Disable poke for that byte [x] = 1 Enable poke for that byte

Table 15-288. Register Call Summary for ICSSG_RTU1_POKE_EN0_REG

PRU_ICSSG_CFG Registers

- [ICSSG_RTU1_POKE_EN0_REG Register \(Offset = 12Ch\) \[reset = 0h\]: \[0\]](#)

15.5.67 ICSSG_PWM0 Register (Offset = 130h) [reset = X]

ICSSG_PWM0 is shown in [Figure 15-94](#) and described in [Table 15-290](#).

Return to [Summary Table](#).

PWM0 Trip Configuration Register.

Table 15-289. ICSSG_PWM0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6130h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6130h

Figure 15-94. ICSSG_PWM0 Register

31	30	29	28	27	26	25	24
RESERVED	PWM0_TRIP_S	PWM0_TRIP_VEC					
R/W-X	R/W-0h	R-0h					
23	22	21	20	19	18	17	16
PWM0_TRIP_VEC			PWM0_POS_ERR_TRIP	PWM0_OVER_ERR_TRIP	PWM0_TRIP_RESET	PWM0_TRIP_CMP0_EN	PWM0_TRIP_MASK
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
PWM0_TRIP_MASK							
R/W-0h							
7	6	5	4	3	2	1	0
PWM0_DEBOUNCE_VALUE							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-290. ICSSG_PWM0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30	PWM0_TRIP_S	R/W	0h	Trip status. Cleared by trip reset.
29-21	PWM0_TRIP_VEC	R	0h	Trip trigger cause vector. Cleared by trip reset. 0h: PWM0_POS_ERR_TRIP (trip_e5) 1h: PWM0_OVER_ERR_TRIP (trip_e4) 2h: PWM0_0_SD_SHORT_ERR_TRIP (trip_e3_0) 3h: PWM0_1_SD_SHORT_ERR_TRIP (trip_e3_1) 4h: PWM0_2_SD_SHORT_ERR_TRIP (trip_e3_2) 5h: PWM0_DEBOUNCE_TRIP_IN (trip_e2) 6h: PWM0_0_DEBOUNCE_TRIP (trip_e1_0) 7h: PWM0_1_DEBOUNCE_TRIP (trip_e1_1) 8h: PWM0_2_DEBOUNCE_TRIP (trip_e1_2)
20	PWM0_POS_ERR_TRIP	R/W	0h	Software position feedback error trip
19	PWM0_OVER_ERR_TRIP	R/W	0h	Software overcurrent error trip
18	PWM0_TRIP_RESET	R/W	0h	Software trip reset
17	PWM0_TRIP_CMP0_EN	R/W	0h	CMP0 reset trip clear enable
16-8	PWM0_TRIP_MASK	R/W	0h	Software mask for trip, one hot

Table 15-290. ICSSG_PWM0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	PWM0_DEBOUNCE_VAL UE	R/W	0h	Debounce counter , defines the number of core_clk required for the pulse not to get rejected

Table 15-291. Register Call Summary for ICSSG_PWM0

PRU_ICSSG PWM Module
• PRU_ICSSG PWM Trip State Logic: [0] [1] • PRU_ICSSG PWM Glitch Filter: [0]
PRU_ICSSG_CFG Registers
• ICSSG_PWM0 Register (Offset = 130h) [reset = X]: [0]

15.5.68 ICSSG_PWM1 Register (Offset = 134h) [reset = X]

ICSSG_PWM1 is shown in [Figure 15-95](#) and described in [Table 15-293](#).

Return to [Summary Table](#).

PWM1 Trip Configuration Register.

Table 15-292. ICSSG_PWM1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6134h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6134h

Figure 15-95. ICSSG_PWM1 Register

31	30	29	28	27	26	25	24
RESERVED	PWM1_TRIP_S	PWM1_TRIP_VEC					
R/W-X	R/W-0h	R-0h					
23	22	21	20	19	18	17	16
PWM1_TRIP_VEC			PWM1_POS_ERR_TRIP	PWM1_OVER_ERR_TRIP	PWM1_TRIP_RESET	PWM1_TRIP_CMP0_EN	PWM1_TRIP_MASK
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
PWM1_TRIP_MASK							
R/W-0h							
7	6	5	4	3	2	1	0
PWM1_DEBOUNCE_VALUE							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-293. ICSSG_PWM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30	PWM1_TRIP_S	R/W	0h	Trip status. Cleared by trip reset.
29-21	PWM1_TRIP_VEC	R	0h	Trip trigger cause vector. Cleared by trip reset. 0h: PWM1_POS_ERR_TRIP (trip_e5) 1h: PWM1_OVER_ERR_TRIP (trip_e4) 2h: PWM1_0_SD_SHORT_ERR_TRIP (trip_e3_0) 3h: PWM1_1_SD_SHORT_ERR_TRIP (trip_e3_1) 4h: PWM1_2_SD_SHORT_ERR_TRIP (trip_e3_2) 5h: PWM1_DEBOUNCE_TRIP_IN (trip_e2) 6h: PWM1_0_DEBOUNCE_TRIP (trip_e1_0) 7h: PWM1_1_DEBOUNCE_TRIP (trip_e1_1) 8h: PWM1_2_DEBOUNCE_TRIP (trip_e1_2)
20	PWM1_POS_ERR_TRIP	R/W	0h	Software position feedback error trip
19	PWM1_OVER_ERR_TRIP	R/W	0h	Software overcurrent error trip
18	PWM1_TRIP_RESET	R/W	0h	Software trip reset
17	PWM1_TRIP_CMP0_EN	R/W	0h	CMP0 reset trip clear enable
16-8	PWM1_TRIP_MASK	R/W	0h	Software mask for trip, one hot

Table 15-293. ICSSG_PWM1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	PWM1_DEBOUNCE_VAL UE	R/W	0h	Debounce counter, defines the number of core_clk required for the pulse not to get rejected

Table 15-294. Register Call Summary for ICSSG_PWM1

PRU_ICSSG PWM Module
PRU_ICSSG PWM Trip State Logic: [0]
PRU_ICSSG_CFG Registers
ICSSG_PWM1 Register (Offset = 134h) [reset = X]: [0]

15.5.69 ICSSG_PWM2 Register (Offset = 138h) [reset = X]

ICSSG_PWM2 is shown in [Figure 15-96](#) and described in [Table 15-296](#).

Return to [Summary Table](#).

PWM2 Trip Configuration Register.

Table 15-295. ICSSG_PWM2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6138h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6138h

Figure 15-96. ICSSG_PWM2 Register

31	30	29	28	27	26	25	24
RESERVED	PWM2_TRIP_S	PWM2_TRIP_VEC					
R/W-X	R/W-0h	R-0h					
23	22	21	20	19	18	17	16
PWM2_TRIP_VEC			PWM2_POS_ERR_TRIP	PWM2_OVER_ERR_TRIP	PWM2_TRIP_RESET	PWM2_TRIP_CMP0_EN	PWM2_TRIP_MASK
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
PWM2_TRIP_MASK							
R/W-0h							
7	6	5	4	3	2	1	0
PWM2_DEBOUNCE_VALUE							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-296. ICSSG_PWM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30	PWM2_TRIP_S	R/W	0h	Trip status. Cleared by trip reset.
29-21	PWM2_TRIP_VEC	R	0h	Trip trigger cause vector. Cleared by trip reset. 0h: PWM2_POS_ERR_TRIP (trip_e5) 1h: PWM2_OVER_ERR_TRIP (trip_e4) 2h: PWM2_0_SD_SHORT_ERR_TRIP (trip_e3_0) 3h: PWM2_1_SD_SHORT_ERR_TRIP (trip_e3_1) 4h: PWM2_2_SD_SHORT_ERR_TRIP (trip_e3_2) 5h: PWM2_DEBOUNCE_TRIP_IN (trip_e2) 6h: PWM2_0_DEBOUNCE_TRIP (trip_e1_0) 7h: PWM2_1_DEBOUNCE_TRIP (trip_e1_1) 8h: PWM2_2_DEBOUNCE_TRIP (trip_e1_2)
20	PWM2_POS_ERR_TRIP	R/W	0h	Software position feedback error trip
19	PWM2_OVER_ERR_TRIP	R/W	0h	Software overcurrent error trip
18	PWM2_TRIP_RESET	R/W	0h	Software trip reset
17	PWM2_TRIP_CMP0_EN	R/W	0h	CMP0 reset trip clear enable
16-8	PWM2_TRIP_MASK	R/W	0h	Software mask for trip, one hot

Table 15-296. ICSSG_PWM2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	PWM2_DEBOUNCE_VAL UE	R/W	0h	Debounce counter, defines the number of core_clk required for the pulse not to get rejected

Table 15-297. Register Call Summary for ICSSG_PWM2

PRU_ICSSG PWM Module
PRU_ICSSG PWM Trip State Logic: [0]
PRU_ICSSG_CFG Registers
ICSSG_PWM2 Register (Offset = 138h) [reset = X]: [0]

15.5.70 ICSSG_PWM3 Register (Offset = 13Ch) [reset = X]

ICSSG_PWM3 is shown in [Figure 15-97](#) and described in [Table 15-299](#).

Return to [Summary Table](#).

PWM3 Trip Configuration Register

Table 15-298. ICSSG_PWM3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 613Ch
PRU_ICSSG1_PR1_CFG_SLV	0B12 613Ch

Figure 15-97. ICSSG_PWM3 Register

31	30	29	28	27	26	25	24
RESERVED	PWM3_TRIP_S	PWM3_TRIP_VEC					
R/W-X	R/W-0h	R-0h					
23	22	21	20	19	18	17	16
PWM3_TRIP_VEC			PWM3_POS_ERR_TRIP	PWM3_OVER_ERR_TRIP	PWM3_TRIP_RESET	PWM3_TRIP_CMP0_EN	PWM3_TRIP_MASK
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
PWM3_TRIP_MASK							
R/W-0h							
7	6	5	4	3	2	1	0
PWM3_DEBOUNCE_VALUE							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-299. ICSSG_PWM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30	PWM3_TRIP_S	R/W	0h	Trip status.
29-21	PWM3_TRIP_VEC	R	0h	Trip trigger cause vector. Cleared by trip reset. 0h: PWM3_POS_ERR_TRIP (trip_e5) 1h: PWM3_OVER_ERR_TRIP (trip_e4) 2h: PWM3_0_SD_SHORT_ERR_TRIP (trip_e3_0) 3h: PWM3_1_SD_SHORT_ERR_TRIP (trip_e3_1) 4h: PWM3_2_SD_SHORT_ERR_TRIP (trip_e3_2) 5h: PWM3_DEBOUNCE_TRIP_IN (trip_e2) 6h: PWM3_0_DEBOUNCE_TRIP (trip_e1_0) 7h: PWM3_1_DEBOUNCE_TRIP (trip_e1_1) 8h: PWM3_2_DEBOUNCE_TRIP (trip_e1_2)
20	PWM3_POS_ERR_TRIP	R/W	0h	Software position feedback error trip
19	PWM3_OVER_ERR_TRIP	R/W	0h	Software overcurrent error trip
18	PWM3_TRIP_RESET	R/W	0h	Software trip reset
17	PWM3_TRIP_CMP0_EN	R/W	0h	CMP0 reset trip clear enable
16-8	PWM3_TRIP_MASK	R/W	0h	Software mask for trip, one hot
7-0	PWM3_DEBOUNCE_VALUE	R/W	0h	Debounce counter, defines the number of core_clk required for the pulse not to get rejected

Table 15-300. Register Call Summary for ICSSG_PWM3

PRU_ICSSG PWM Module PRU_ICSSG PWM Trip State Logic: [0]
PRU_ICSSG_CFG Registers ICSSG_PWM3 Register (Offset = 13Ch) [reset = X]: [0]

15.5.71 ICSSG_PWM0_0 Register (Offset = 140h) [reset = X]

ICSSG_PWM0_0 is shown in [Figure 15-98](#) and described in [Table 15-302](#).

Return to [Summary Table](#).

PWM0 State Configuration 0 Register.

Table 15-301. ICSSG_PWM0_0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6140h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6140h

Figure 15-98. ICSSG_PWM0_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED				PWM0_0_NEG_ACT		PWM0_0_POS_ACT	
R/W-X				R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
PWM0_0_NEG_TRIP		PWM0_0_POS_TRIP		PWM0_0_NEG_INIT		PWM0_0_POS_INIT	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-302. ICSSG_PWM0_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-10	PWM0_0_NEG_ACT	R/W	0h	Active negative state 0h = Toggle 1h = L 2h = H
9-8	PWM0_0_POS_ACT	R/W	0h	Active positive state 0h = Toggle 1h = L 2h = H
7-6	PWM0_0_NEG_TRIP	R/W	0h	Trip negative state 0h = Z 1h = L 2h = H
5-4	PWM0_0_POS_TRIP	R/W	0h	Trip positive state 0h = Z 1h = L 2h = H
3-2	PWM0_0_NEG_INIT	R/W	0h	Initial negative state 0h = Z 1h = L 2h = H

Table 15-302. ICSSG_PWM0_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	PWM0_0_POS_INIT	R/W	0h	Initial positive state 0h = Z 1h = L 2h = H

Table 15-303. Register Call Summary for ICSSG_PWM0_0

PRU_ICSSG_CFG Registers

- [ICSSG_PWM0_0 Register \(Offset = 140h\) \[reset = X\]: \[0\]](#)

15.5.72 ICSSG_PWM0_1 Register (Offset = 144h) [reset = X]

ICSSG_PWM0_1 is shown in [Figure 15-99](#) and described in [Table 15-305](#).

Return to [Summary Table](#).

PWM0 State Configuration 1 Register.

Table 15-304. ICSSG_PWM0_1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6144h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6144h

Figure 15-99. ICSSG_PWM0_1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED				PWM0_1_NEG_ACT		PWM0_1_POS_ACT	
R/W-X				R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
PWM0_1_NEG_TRIP		PWM0_1_POS_TRIP		PWM0_1_NEG_INIT		PWM0_1_POS_INIT	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-305. ICSSG_PWM0_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-10	PWM0_1_NEG_ACT	R/W	0h	Active negative state 0h = Toggle 1h = L 2h = H
9-8	PWM0_1_POS_ACT	R/W	0h	Active positive state 0h = Toggle 1h = L 2h = H
7-6	PWM0_1_NEG_TRIP	R/W	0h	Trip negative state 0h = Z 1h = L 2h = H
5-4	PWM0_1_POS_TRIP	R/W	0h	Trip positive state 0h = Z 1h = L 2h = H
3-2	PWM0_1_NEG_INIT	R/W	0h	Initial negative state 0h = Z 1h = L 2h = H

Table 15-305. ICSSG_PWM0_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	PWM0_1_POS_INIT	R/W	0h	Initial positive state 0h = Z 1h = L 2h = H

Table 15-306. Register Call Summary for ICSSG_PWM0_1

PRU_ICSSG_CFG Registers

- [ICSSG_PWM0_1 Register \(Offset = 144h\) \[reset = X\]: \[0\]](#)

15.5.73 ICSSG_PWM0_2 Register (Offset = 148h) [reset = X]

ICSSG_PWM0_2 is shown in [Figure 15-100](#) and described in [Table 15-308](#).

Return to [Summary Table](#).

PWM0 State Configuration 2 Register.

Table 15-307. ICSSG_PWM0_2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6148h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6148h

Figure 15-100. ICSSG_PWM0_2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED				PWM0_2_NEG_ACT		PWM0_2_POS_ACT	
R/W-X				R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
PWM0_2_NEG_TRIP		PWM0_2_POS_TRIP		PWM0_2_NEG_INIT		PWM0_2_POS_INIT	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-308. ICSSG_PWM0_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-10	PWM0_2_NEG_ACT	R/W	0h	Active negative state 0h = Toggle 1h = L 2h = H
9-8	PWM0_2_POS_ACT	R/W	0h	Active positive state 0h = Toggle 1h = L 2h = H
7-6	PWM0_2_NEG_TRIP	R/W	0h	Trip negative state 0h = Z 1h = L 2h = H
5-4	PWM0_2_POS_TRIP	R/W	0h	Trip positive state 0h = Z 1h = L 2h = H
3-2	PWM0_2_NEG_INIT	R/W	0h	Initial negative state 0h = Z 1h = L 2h = H

Table 15-308. ICSSG_PWM0_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	PWM0_2_POS_INIT	R/W	0h	Initial positive state 0h = Z 1h = L 2h = H

Table 15-309. Register Call Summary for ICSSG_PWM0_2

PRU_ICSSG_CFG Registers

- [ICSSG_PWM0_2 Register \(Offset = 148h\) \[reset = X\]: \[0\]](#)

15.5.74 ICSSG_PWM1_0 Register (Offset = 14Ch) [reset = X]

ICSSG_PWM1_0 is shown in [Figure 15-101](#) and described in [Table 15-311](#).

Return to [Summary Table](#).

PWM1 State Configuration 0 Register.

Table 15-310. ICSSG_PWM1_0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 614Ch
PRU_ICSSG1_PR1_CFG_SLV	0B12 614Ch

Figure 15-101. ICSSG_PWM1_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED				PWM1_0_NEG_ACT		PWM1_0_POS_ACT	
R/W-X				R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
PWM1_0_NEG_TRIP		PWM1_0_POS_TRIP		PWM1_0_NEG_INIT		PWM1_0_POS_INIT	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-311. ICSSG_PWM1_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-10	PWM1_0_NEG_ACT	R/W	0h	Active negative state 0h = Toggle 1h = L 2h = H
9-8	PWM1_0_POS_ACT	R/W	0h	Active positive state 0h = Toggle 1h = L 2h = H
7-6	PWM1_0_NEG_TRIP	R/W	0h	Trip negative state 0h = Z 1h = L 2h = H
5-4	PWM1_0_POS_TRIP	R/W	0h	Trip positive state 0h = Z 1h = L 2h = H
3-2	PWM1_0_NEG_INIT	R/W	0h	Initial negative state 0h = Z 1h = L 2h = H

Table 15-311. ICSSG_PWM1_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	PWM1_0_POS_INIT	R/W	0h	Initial positive state 0h = Z 1h = L 2h = H

Table 15-312. Register Call Summary for ICSSG_PWM1_0

PRU_ICSSG_CFG Registers

- [ICSSG_PWM1_0 Register \(Offset = 14Ch\) \[reset = X\]: \[0\]](#)

15.5.75 ICSSG_PWM1_1 Register (Offset = 150h) [reset = X]

ICSSG_PWM1_1 is shown in [Figure 15-102](#) and described in [Table 15-314](#).

Return to [Summary Table](#).

PWM1 State Configuration 1 Register.

Table 15-313. ICSSG_PWM1_1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6150h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6150h

Figure 15-102. ICSSG_PWM1_1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED				PWM1_1_NEG_ACT		PWM1_1_POS_ACT	
R/W-X				R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
PWM1_1_NEG_TRIP		PWM1_1_POS_TRIP		PWM1_1_NEG_INIT		PWM1_1_POS_INIT	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-314. ICSSG_PWM1_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-10	PWM1_1_NEG_ACT	R/W	0h	Active negative state 0h = Toggle 1h = L 2h = H
9-8	PWM1_1_POS_ACT	R/W	0h	Active positive state 0h = Toggle 1h = L 2h = H
7-6	PWM1_1_NEG_TRIP	R/W	0h	Trip negative state 0h = Z 1h = L 2h = H
5-4	PWM1_1_POS_TRIP	R/W	0h	Trip positive state 0h = Z 1h = L 2h = H
3-2	PWM1_1_NEG_INIT	R/W	0h	Initial negative state 0h = Z 1h = L 2h = H

Table 15-314. ICSSG_PWM1_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	PWM1_1_POS_INIT	R/W	0h	Initial positive state 0h = Z 1h = L 2h = H

Table 15-315. Register Call Summary for ICSSG_PWM1_1

PRU_ICSSG_CFG Registers

- [ICSSG_PWM1_1 Register \(Offset = 150h\) \[reset = X\]: \[0\]](#)

15.5.76 ICSSG_PWM1_2 Register (Offset = 154h) [reset = X]

ICSSG_PWM1_2 is shown in [Figure 15-103](#) and described in [Table 15-317](#).

Return to [Summary Table](#).

PWM1 State Configuration 2 Register.

Table 15-316. ICSSG_PWM1_2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6154h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6154h

Figure 15-103. ICSSG_PWM1_2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED				PWM1_2_NEG_ACT		PWM1_2_POS_ACT	
R/W-X				R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
PWM1_2_NEG_TRIP		PWM1_2_POS_TRIP		PWM1_2_NEG_INIT		PWM1_2_POS_INIT	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-317. ICSSG_PWM1_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-10	PWM1_2_NEG_ACT	R/W	0h	Active negative state 0h = Toggle 1h = L 2h = H
9-8	PWM1_2_POS_ACT	R/W	0h	Active positive state 0h = Toggle 1h = L 2h = H
7-6	PWM1_2_NEG_TRIP	R/W	0h	Trip negative state 0h = Z 1h = L 2h = H
5-4	PWM1_2_POS_TRIP	R/W	0h	Trip positive state 0h = Z 1h = L 2h = H
3-2	PWM1_2_NEG_INIT	R/W	0h	Initial negative state 0h = Z 1h = L 2h = H

Table 15-317. ICSSG_PWM1_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	PWM1_2_POS_INIT	R/W	0h	Initial positive state 0h = Z 1h = L 2h = H

Table 15-318. Register Call Summary for ICSSG_PWM1_2

PRU_ICSSG_CFG Registers

- [ICSSG_PWM1_2 Register \(Offset = 154h\) \[reset = X\]: \[0\]](#)

15.5.77 ICSSG_PWM2_0 Register (Offset = 158h) [reset = X]

ICSSG_PWM2_0 is shown in [Figure 15-104](#) and described in [Table 15-320](#).

Return to [Summary Table](#).

PWM2 State Configuration 0 Register.

Table 15-319. ICSSG_PWM2_0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6158h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6158h

Figure 15-104. ICSSG_PWM2_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED				PWM2_0_NEG_ACT		PWM2_0_POS_ACT	
R/W-X				R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
PWM2_0_NEG_TRIP		PWM2_0_POS_TRIP		PWM2_0_NEG_INIT		PWM2_0_POS_INIT	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-320. ICSSG_PWM2_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-10	PWM2_0_NEG_ACT	R/W	0h	Active negative state 0h = Toggle 1h = L 2h = H
9-8	PWM2_0_POS_ACT	R/W	0h	Active positive state 0h = Toggle 1h = L 2h = H
7-6	PWM2_0_NEG_TRIP	R/W	0h	Trip negative state 0h = Z 1h = L 2h = H
5-4	PWM2_0_POS_TRIP	R/W	0h	Trip positive state 0h = Z 1h = L 2h = H
3-2	PWM2_0_NEG_INIT	R/W	0h	Initial negative state 0h = Z 1h = L 2h = H

Table 15-320. ICSSG_PWM2_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	PWM2_0_POS_INIT	R/W	0h	Initial positive state 0h = Z 1h = L 2h = H

Table 15-321. Register Call Summary for ICSSG_PWM2_0

PRU_ICSSG_CFG Registers

- [ICSSG_PWM2_0 Register \(Offset = 158h\) \[reset = X\]: \[0\]](#)

15.5.78 ICSSG_PWM2_1 Register (Offset = 15Ch) [reset = X]

ICSSG_PWM2_1 is shown in [Figure 15-105](#) and described in [Table 15-323](#).

Return to [Summary Table](#).

PWM2 State Configuration 1 Register.

Table 15-322. ICSSG_PWM2_1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 615Ch
PRU_ICSSG1_PR1_CFG_SLV	0B12 615Ch

Figure 15-105. ICSSG_PWM2_1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED				PWM2_1_NEG_ACT		PWM2_1_POS_ACT	
R/W-X				R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
PWM2_1_NEG_TRIP		PWM2_1_POS_TRIP		PWM2_1_NEG_INIT		PWM2_1_POS_INIT	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-323. ICSSG_PWM2_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-10	PWM2_1_NEG_ACT	R/W	0h	Active negative state 0h = Toggle 1h = L 2h = H
9-8	PWM2_1_POS_ACT	R/W	0h	Active positive state 0h = Toggle 1h = L 2h = H
7-6	PWM2_1_NEG_TRIP	R/W	0h	Trip negative state 0h = Z 1h = L 2h = H
5-4	PWM2_1_POS_TRIP	R/W	0h	Trip positive state 0h = Z 1h = L 2h = H
3-2	PWM2_1_NEG_INIT	R/W	0h	Initial negative state 0h = Z 1h = L 2h = H

Table 15-323. ICSSG_PWM2_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	PWM2_1_POS_INIT	R/W	0h	Initial positive state 0h = Z 1h = L 2h = H

Table 15-324. Register Call Summary for ICSSG_PWM2_1

PRU_ICSSG_CFG Registers

- [ICSSG_PWM2_1 Register \(Offset = 15Ch\) \[reset = X\]: \[0\]](#)

15.5.79 ICSSG_PWM2_2 Register (Offset = 160h) [reset = X]

ICSSG_PWM2_2 is shown in [Figure 15-106](#) and described in [Table 15-326](#).

Return to [Summary Table](#).

PWM2 State Configuration 2 Register.

Table 15-325. ICSSG_PWM2_2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6160h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6160h

Figure 15-106. ICSSG_PWM2_2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED				PWM2_2_NEG_ACT		PWM2_2_POS_ACT	
R/W-X				R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
PWM2_2_NEG_TRIP		PWM2_2_POS_TRIP		PWM2_2_NEG_INIT		PWM2_2_POS_INIT	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-326. ICSSG_PWM2_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-10	PWM2_2_NEG_ACT	R/W	0h	Active negative state 0h = Toggle 1h = L 2h = H
9-8	PWM2_2_POS_ACT	R/W	0h	Active positive state 0h = Toggle 1h = L 2h = H
7-6	PWM2_2_NEG_TRIP	R/W	0h	Trip negative state 0h = Z 1h = L 2h = H
5-4	PWM2_2_POS_TRIP	R/W	0h	Trip positive state 0h = Z 1h = L 2h = H
3-2	PWM2_2_NEG_INIT	R/W	0h	Initial negative state 0h = Z 1h = L 2h = H

Table 15-326. ICSSG_PWM2_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	PWM2_2_POS_INIT	R/W	0h	Initial positive state 0h = Z 1h = L 2h = H

Table 15-327. Register Call Summary for ICSSG_PWM2_2

PRU_ICSSG_CFG Registers

- [ICSSG_PWM2_2 Register \(Offset = 160h\) \[reset = X\]: \[0\]](#)

15.5.80 ICSSG_PWM3_0 Register (Offset = 164h) [reset = X]

ICSSG_PWM3_0 is shown in [Figure 15-107](#) and described in [Table 15-329](#).

Return to [Summary Table](#).

PWM3 State Configuration 0 Register.

Table 15-328. ICSSG_PWM3_0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6164h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6164h

Figure 15-107. ICSSG_PWM3_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED				PWM3_0_NEG_ACT		PWM3_0_POS_ACT	
R/W-X				R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
PWM3_0_NEG_TRIP		PWM3_0_POS_TRIP		PWM3_0_NEG_INIT		PWM3_0_POS_INIT	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-329. ICSSG_PWM3_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-10	PWM3_0_NEG_ACT	R/W	0h	Active negative state 0h = Toggle 1h = L 2h = H
9-8	PWM3_0_POS_ACT	R/W	0h	Active positive state 0h = Toggle 1h = L 2h = H
7-6	PWM3_0_NEG_TRIP	R/W	0h	Trip negative state 0h = Z 1h = L 2h = H
5-4	PWM3_0_POS_TRIP	R/W	0h	Trip positive state 0h = Z 1h = L 2h = H
3-2	PWM3_0_NEG_INIT	R/W	0h	Initial negative state 0h = Z 1h = L 2h = H

Table 15-329. ICSSG_PWM3_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	PWM3_0_POS_INIT	R/W	0h	Initial positive state 0h = Z 1h = L 2h = H

Table 15-330. Register Call Summary for ICSSG_PWM3_0

PRU_ICSSG_CFG Registers

- [ICSSG_PWM3_0 Register \(Offset = 164h\) \[reset = X\]: \[0\]](#)

15.5.81 ICSSG_PWM3_1 Register (Offset = 168h) [reset = X]

ICSSG_PWM3_1 is shown in [Figure 15-108](#) and described in [Table 15-332](#).

Return to [Summary Table](#).

PWM3 State Configuration 1 Register.

Table 15-331. ICSSG_PWM3_1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6168h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6168h

Figure 15-108. ICSSG_PWM3_1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED				PWM3_1_NEG_ACT		PWM3_1_POS_ACT	
R/W-X				R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
PWM3_1_NEG_TRIP		PWM3_1_POS_TRIP		PWM3_1_NEG_INIT		PWM3_1_POS_INIT	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-332. ICSSG_PWM3_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-10	PWM3_1_NEG_ACT	R/W	0h	Active negative state 0h = Toggle 1h = L 2h = H
9-8	PWM3_1_POS_ACT	R/W	0h	Active positive state 0h = Toggle 1h = L 2h = H
7-6	PWM3_1_NEG_TRIP	R/W	0h	Trip negative state 0h = Z 1h = L 2h = H
5-4	PWM3_1_POS_TRIP	R/W	0h	Trip positive state 0h = Z 1h = L 2h = H
3-2	PWM3_1_NEG_INIT	R/W	0h	Initial negative state 0h = Z 1h = L 2h = H

Table 15-332. ICSSG_PWM3_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	PWM3_1_POS_INIT	R/W	0h	Initial positive state 0h = Z 1h = L 2h = H

Table 15-333. Register Call Summary for ICSSG_PWM3_1

PRU_ICSSG_CFG Registers

- [ICSSG_PWM3_1 Register \(Offset = 168h\) \[reset = X\]: \[0\]](#)

15.5.82 ICSSG_PWM3_2 Register (Offset = 16Ch) [reset = X]

ICSSG_PWM3_2 is shown in [Figure 15-109](#) and described in [Table 15-335](#).

Return to [Summary Table](#).

PWM3 State Configuration 2 Register.

Table 15-334. ICSSG_PWM3_2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 616Ch
PRU_ICSSG1_PR1_CFG_SLV	0B12 616Ch

Figure 15-109. ICSSG_PWM3_2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED				PWM3_2_NEG_ACT		PWM3_2_POS_ACT	
R/W-X				R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
PWM3_2_NEG_TRIP		PWM3_2_POS_TRIP		PWM3_2_NEG_INIT		PWM3_2_POS_INIT	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-335. ICSSG_PWM3_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-10	PWM3_2_NEG_ACT	R/W	0h	Active negative state 0h = Toggle 1h = L 2h = H
9-8	PWM3_2_POS_ACT	R/W	0h	Active positive state 0h = Toggle 1h = L 2h = H
7-6	PWM3_2_NEG_TRIP	R/W	0h	Trip negative state 0h = Z 1h = L 2h = H
5-4	PWM3_2_POS_TRIP	R/W	0h	Trip positive state 0h = Z 1h = L 2h = H
3-2	PWM3_2_NEG_INIT	R/W	0h	Initial negative state 0h = Z 1h = L 2h = H

Table 15-335. ICSSG_PWM3_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	PWM3_2_POS_INIT	R/W	0h	Initial positive state 0h = Z 1h = L 2h = H

Table 15-336. Register Call Summary for ICSSG_PWM3_2

PRU_ICSSG_CFG Registers

- [ICSSG_PWM3_2 Register \(Offset = 16Ch\) \[reset = X\]: \[0\]](#)

15.5.83 ICSSG_SPIN_LOCK0 Register (Offset = 170h) [reset = X]

ICSSG_SPIN_LOCK0 is shown in [Figure 15-110](#) and described in [Table 15-338](#).

Return to [Summary Table](#).

Spin Lock 0 Register.

Table 15-337. ICSSG_SPIN_LOCK0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6170h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6170h

Figure 15-110. ICSSG_SPIN_LOCK0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED		MMR_OWN_REQ_VECTOR_0					
R/W-X		R/W-0h					
7	6	5	4	3	2	1	0
RESERVED						MMR_OWN_R EQ_CLR_0	MMR_OWN_R EQ_STATUS_0
R/W-X						W-0h	R-X

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 15-338. ICSSG_SPIN_LOCK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-8	MMR_OWN_REQ_VECTOR_0	R/W	0h	Spin Lock flag Vector
7-2	RESERVED	R/W	X	
1	MMR_OWN_REQ_CLR_0	W	0h	Spin Lock Status Clear
0	MMR_OWN_REQ_STATUS_0	R	X	Spin Lock Status

Table 15-339. Register Call Summary for ICSSG_SPIN_LOCK0

PRU_ICSSG_CFG Registers
• ICSSG_SPIN_LOCK0 Register (Offset = 170h) [reset = X]: [0]
PRU_ICSSG Broadside Accelerators
• PRU_ICSSG Spinlock: [0] [1] [2] [3]

15.5.84 ICSSG_SPIN_LOCK1 Register (Offset = 174h) [reset = X]

ICSSG_SPIN_LOCK1 is shown in Figure 15-111 and described in Table 15-341.

Return to [Summary Table](#).

Spin Lock 1 Register.

Table 15-340. ICSSG_SPIN_LOCK1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6174h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6174h

Figure 15-111. ICSSG_SPIN_LOCK1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED		MMR_OWN_REQ_VECTOR_1					
R/W-X		R/W-0h					
7	6	5	4	3	2	1	0
RESERVED						MMR_OWN_R EQ_CLR_1	MMR_OWN_R EQ_STATUS_1
R/W-X						W-0h	R-X

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 15-341. ICSSG_SPIN_LOCK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-8	MMR_OWN_REQ_VECTOR_1	R/W	0h	Spin Lock flag Vector
7-2	RESERVED	R/W	X	
1	MMR_OWN_REQ_CLR_1	W	0h	Spin Lock Status Clear
0	MMR_OWN_REQ_STATUS_1	R	X	Spin Lock Status

Table 15-342. Register Call Summary for ICSSG_SPIN_LOCK1

PRU_ICSSG_CFG Registers
ICSSG_SPIN_LOCK1 Register (Offset = 174h) [reset = X]: [0]
PRU_ICSSG Broadside Accelerators
PRU_ICSSG Spinlock: [0]

15.5.85 ICSSG_PA_STAT_PDSP_CFG0 Register (Offset = 178h) [reset = 0h]

ICSSG_PA_STAT_PDSP_CFG0 is shown in Figure 15-112 and described in Table 15-344.

Return to [Summary Table](#).

PA STATS PRU Vector 0 Register.

Table 15-343. ICSSG_PA_STAT_PDSP_CFG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6178h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6178h

Figure 15-112. ICSSG_PA_STAT_PDSP_CFG0 Register

31	30	29	28	27	26	25	24
PA_PDSP0_INC_TYPE	PA_PDSP0_INC_VAL						
R/W-0h	R/W-0h						
23	22	21	20	19	18	17	16
PA_PDSP0_INC_VAL							
R/W-0h							
15	14	13	12	11	10	9	8
PA_PDSP0_INC_VAL	PA_PDSP0_INDEX						
R/W-0h	R/W-0h						
7	6	5	4	3	2	1	0
PA_PDSP0_INDEX							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-344. ICSSG_PA_STAT_PDSP_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PA_PDSP0_INC_TYPE	R/W	0h	pa_pdsp0_inc_type
30-14	PA_PDSP0_INC_VAL	R/W	0h	pa_pdsp0_inc_val
13-0	PA_PDSP0_INDEX	R/W	0h	pa_pdsp0_index

Table 15-345. Register Call Summary for ICSSG_PA_STAT_PDSP_CFG0

PRU_ICSSG_CFG Registers

- [ICSSG_PA_STAT_PDSP_CFG0 Register \(Offset = 178h\) \[reset = 0h\]: \[0\]](#)

15.5.86 ICSSG_PA_STAT_PDSP_STAT0 Register (Offset = 17Ch) [reset = X]

ICSSG_PA_STAT_PDSP_STAT0 is shown in [Figure 15-113](#) and described in [Table 15-347](#).

Return to [Summary Table](#).

PA STATS PRU Status 0 Register.

**Table 15-346. ICSSG_PA_STAT_PDSP_STAT0
Instances**

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 617Ch
PRU_ICSSG1_PR1_CFG_SLV	0B12 617Ch

Figure 15-113. ICSSG_PA_STAT_PDSP_STAT0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED				PA_PDSP0_STATUS		PA_PDSP0_READY	
R-X				R-0h		R-0h	

LEGEND: R = Read Only; -n = value after reset

Table 15-347. ICSSG_PA_STAT_PDSP_STAT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	X	
3-1	PA_PDSP0_STATUS	R	0h	pa_pdsp0_status
0	PA_PDSP0_READY	R	0h	pa_pdsp0_ready

Table 15-348. Register Call Summary for ICSSG_PA_STAT_PDSP_STAT0

PRU_ICSSG_CFG Registers

- [ICSSG_PA_STAT_PDSP_STAT0 Register \(Offset = 17Ch\) \[reset = X\]: \[0\]](#)

15.5.87 ICSSG_PA_STAT_PDSP_CFG1 Register (Offset = 180h) [reset = 0h]

ICSSG_PA_STAT_PDSP_CFG1 is shown in Figure 15-114 and described in Table 15-350.

Return to [Summary Table](#).

PA STATS PRU Vector 1 Register.

Table 15-349. ICSSG_PA_STAT_PDSP_CFG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6180h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6180h

Figure 15-114. ICSSG_PA_STAT_PDSP_CFG1 Register

31	30	29	28	27	26	25	24
PA_PDSP1_INC_TYPE	PA_PDSP1_INC_VAL						
R/W-0h	R/W-0h						
23	22	21	20	19	18	17	16
PA_PDSP1_INC_VAL							
R/W-0h							
15	14	13	12	11	10	9	8
PA_PDSP1_INC_VAL	PA_PDSP1_INDEX						
R/W-0h	R/W-0h						
7	6	5	4	3	2	1	0
PA_PDSP1_INDEX							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-350. ICSSG_PA_STAT_PDSP_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PA_PDSP1_INC_TYPE	R/W	0h	pa_pdsp1_inc_type
30-14	PA_PDSP1_INC_VAL	R/W	0h	pa_pdsp1_inc_val
13-0	PA_PDSP1_INDEX	R/W	0h	pa_pdsp1_index

Table 15-351. Register Call Summary for ICSSG_PA_STAT_PDSP_CFG1

PRU_ICSSG_CFG Registers

- ICSSG_PA_STAT_PDSP_CFG1 Register (Offset = 180h) [reset = 0h]: [0]

15.5.88 ICSSG_PA_STAT_PDSP_STAT1 Register (Offset = 184h) [reset = X]

ICSSG_PA_STAT_PDSP_STAT1 is shown in [Figure 15-115](#) and described in [Table 15-353](#).

Return to [Summary Table](#).

PA STATS PRU Status 1 Register.

**Table 15-352. ICSSG_PA_STAT_PDSP_STAT1
Instances**

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6184h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6184h

Figure 15-115. ICSSG_PA_STAT_PDSP_STAT1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED				PA_PDSP1_STATUS		PA_PDSP1_READY	
R-X				R-0h		R-0h	

LEGEND: R = Read Only; -n = value after reset

Table 15-353. ICSSG_PA_STAT_PDSP_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	X	
3-1	PA_PDSP1_STATUS	R	0h	pa_pdsp1_status
0	PA_PDSP1_READY	R	0h	pa_pdsp1_ready

Table 15-354. Register Call Summary for ICSSG_PA_STAT_PDSP_STAT1

PRU_ICSSG_CFG Registers

- [ICSSG_PA_STAT_PDSP_STAT1 Register \(Offset = 184h\) \[reset = X\]: \[0\]](#)

15.5.89 ICSSG_PA_STAT_PDSP_CFG2 Register (Offset = 188h) [reset = 0h]

ICSSG_PA_STAT_PDSP_CFG2 is shown in Figure 15-116 and described in Table 15-356.

Return to [Summary Table](#).

PA STATS PRU Vector 2 Register.

Table 15-355. ICSSG_PA_STAT_PDSP_CFG2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6188h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6188h

Figure 15-116. ICSSG_PA_STAT_PDSP_CFG2 Register

31	30	29	28	27	26	25	24
PA_PDSP2_INC_TYPE	PA_PDSP2_INC_VAL						
R/W-0h	R/W-0h						
23	22	21	20	19	18	17	16
PA_PDSP2_INC_VAL							
R/W-0h							
15	14	13	12	11	10	9	8
PA_PDSP2_INC_VAL		PA_PDSP2_INDEX					
R/W-0h		R/W-0h					
7	6	5	4	3	2	1	0
PA_PDSP2_INDEX							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-356. ICSSG_PA_STAT_PDSP_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PA_PDSP2_INC_TYPE	R/W	0h	pa_pdsp2_inc_type
30-14	PA_PDSP2_INC_VAL	R/W	0h	pa_pdsp2_inc_val
13-0	PA_PDSP2_INDEX	R/W	0h	pa_pdsp2_index

Table 15-357. Register Call Summary for ICSSG_PA_STAT_PDSP_CFG2

PRU_ICSSG_CFG Registers

- [ICSSG_PA_STAT_PDSP_CFG2 Register \(Offset = 188h\) \[reset = 0h\]: \[0\]](#)

15.5.90 ICSSG_PA_STAT_PDSP_STAT2 Register (Offset = 18Ch) [reset = X]

ICSSG_PA_STAT_PDSP_STAT2 is shown in [Figure 15-117](#) and described in [Table 15-359](#).

Return to [Summary Table](#).

PA STATS PRU Status 2 Register.

**Table 15-358. ICSSG_PA_STAT_PDSP_STAT2
Instances**

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 618Ch
PRU_ICSSG1_PR1_CFG_SLV	0B12 618Ch

Figure 15-117. ICSSG_PA_STAT_PDSP_STAT2 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED				PA_PDSP2_STATUS		PA_PDSP2_READY	
R-X				R-0h		R-0h	

LEGEND: R = Read Only; -n = value after reset

Table 15-359. ICSSG_PA_STAT_PDSP_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	X	
3-1	PA_PDSP2_STATUS	R	0h	pa_pdsp2_status
0	PA_PDSP2_READY	R	0h	pa_pdsp2_ready

Table 15-360. Register Call Summary for ICSSG_PA_STAT_PDSP_STAT2

PRU_ICSSG_CFG Registers

- [ICSSG_PA_STAT_PDSP_STAT2 Register \(Offset = 18Ch\) \[reset = X\]: \[0\]](#)

15.5.91 ICSSG_PA_STAT_PDSP_CFG3 Register (Offset = 190h) [reset = 0h]

ICSSG_PA_STAT_PDSP_CFG3 is shown in Figure 15-118 and described in Table 15-362.

Return to [Summary Table](#).

PA STATS PRU Vector 3 Register.

Table 15-361. ICSSG_PA_STAT_PDSP_CFG3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6190h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6190h

Figure 15-118. ICSSG_PA_STAT_PDSP_CFG3 Register

31	30	29	28	27	26	25	24
PA_PDSP3_INC_TYPE	PA_PDSP3_INC_VAL						
R/W-0h	R/W-0h						
23	22	21	20	19	18	17	16
PA_PDSP3_INC_VAL							
R/W-0h							
15	14	13	12	11	10	9	8
PA_PDSP3_INC_VAL	PA_PDSP3_INDEX						
R/W-0h	R/W-0h						
7	6	5	4	3	2	1	0
PA_PDSP3_INDEX							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-362. ICSSG_PA_STAT_PDSP_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PA_PDSP3_INC_TYPE	R/W	0h	pa_pdsp3_inc_type
30-14	PA_PDSP3_INC_VAL	R/W	0h	pa_pdsp3_inc_val
13-0	PA_PDSP3_INDEX	R/W	0h	pa_pdsp3_index

Table 15-363. Register Call Summary for ICSSG_PA_STAT_PDSP_CFG3

PRU_ICSSG_CFG Registers

- [ICSSG_PA_STAT_PDSP_CFG3 Register \(Offset = 190h\) \[reset = 0h\]: \[0\]](#)

15.5.92 ICSSG_PA_STAT_PDSP_STAT3 Register (Offset = 194h) [reset = X]

ICSSG_PA_STAT_PDSP_STAT3 is shown in [Figure 15-119](#) and described in [Table 15-365](#).

Return to [Summary Table](#).

PA STATS PRU Status 3 Register.

**Table 15-364. ICSSG_PA_STAT_PDSP_STAT3
Instances**

Instance	Physical Address
PRU_ICSSG0_PR1_CFG_SLV	0B02 6194h
PRU_ICSSG1_PR1_CFG_SLV	0B12 6194h

Figure 15-119. ICSSG_PA_STAT_PDSP_STAT3 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED				PA_PDSP3_STATUS		PA_PDSP3_READY	
R-X				R-0h		R-0h	

LEGEND: R = Read Only; -n = value after reset

Table 15-365. ICSSG_PA_STAT_PDSP_STAT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	X	
3-1	PA_PDSP3_STATUS	R	0h	pa_pdsp3_status
0	PA_PDSP3_READY	R	0h	pa_pdsp3_ready

Table 15-366. Register Call Summary for ICSSG_PA_STAT_PDSP_STAT3

PRU_ICSSG_CFG Registers

- [ICSSG_PA_STAT_PDSP_STAT3 Register \(Offset = 194h\) \[reset = X\]: \[0\]](#)

15.6 PRU_ECAP_ECAP0 Registers

Table 15-368 lists the memory-mapped registers for the PRU_ECAP_ECAP0 registers. All register offset addresses not listed in Table 15-368 should be considered as reserved locations and the register contents should not be modified.

Table 15-367. PRU_ECAP_ECAP0 Instances

Instance	Base Address
PRU_ICSSG0_PR1_ICSS_ECAP0_ECAP_SLV	0B03 0000h
PRU_ICSSG1_PR1_ICSS_ECAP0_ECAP_SLV	0B13 0000h

Table 15-368. PRU_ECAP_ECAP0 Registers

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_ICSS_ECAP0_ECAP_SLV Physical Address	PRU_ICSSG1_PR1_ICSS_ECAP0_ECAP_SLV Physical Address
0h	ECAP_TSCNT	Time Stamp Counter Register	0B03 0000h	0B13 0000h
4h	ECAP_CNTPHS	Counter Phase Control Register	0B03 0004h	0B13 0004h
8h	ECAP_CAP1	Capture-1 Register	0B03 0008h	0B13 0008h
Ch	ECAP_CAP2	Capture-2 Register	0B03 000Ch	0B13 000Ch
10h	ECAP_CAP3	Capture-3 Register	0B03 0010h	0B13 0010h
14h	ECAP_CAP4	Capture-4 Register	0B03 0014h	0B13 0014h
28h	ECAP_ECCTL2_ECCTL1	ECAP Control Register 1	0B03 0028h	0B13 0028h
2Ch	ECAP_ECFLG_ECEINT	ECAP Interrupt Enable Register	0B03 002Ch	0B13 002Ch
30h	ECAP_ECCLR	ECAP Interrupt Clear Register	0B03 0030h	0B13 0030h
34h	ECAP_ECFRC	ECAP Interrupt Forcing Register	0B03 0034h	0B13 0034h
5Ch	ECAP_PID	ECAP Peripheral Id Register	0B03 005Ch	0B13 005Ch

15.6.1 ECAP_TSCNT Register (Offset = 0h) [reset = 0h]

ECAP_TSCNT is shown in [Figure 15-120](#) and described in [Table 15-370](#).

Return to [Summary Table](#).

Time Stamp Counter Register.

Table 15-369. ECAP_TSCNT Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_ECAP0_ECAP_SLV	0B03 0000h
PRU_ICSSG1_PR1_ICSS_ECAP0_ECAP_SLV	0B13 0000h

Figure 15-120. ECAP_TSCNT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSCNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-370. ECAP_TSCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TSCNT	R/W	0h	Active 32-bit counter register which is used as the capture time-base.

Table 15-371. Register Call Summary for ECAP_TSCNT

PRU_ECAP_ECAP0 Registers

- [ECAP_CNTPHS Register \(Offset = 4h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [ECAP_ECCTL2_ECCTL1 Register \(Offset = 28h\) \[reset = 00060000h\]: \[0\] \[1\] \[2\] \[3\] \[4\] \[5\] \[6\] \[7\] \[8\] \[9\] \[10\]](#)
- [PRU_ECAP_ECAP0 Registers: \[0\]](#)
- [ECAP_ECFLG_ECEINT Register \(Offset = 2Ch\) \[reset = 0h\]: \[0\] \[1\] \[2\]](#)
- [ECAP_TSCNT Register \(Offset = 0h\) \[reset = 0h\]: \[0\]](#)

15.6.2 ECAP_CNTPHS Register (Offset = 4h) [reset = 0h]

ECAP_CNTPHS is shown in [Figure 15-121](#) and described in [Table 15-373](#).

Return to [Summary Table](#).

Counter Phase Control Register.

Table 15-372. ECAP_CNTPHS Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_ECAPH0_ECAPH_SLV	0B03 0004h
PRU_ICSSG1_PR1_ICSS_ECAPH0_ECAPH_SLV	0B13 0004h

Figure 15-121. ECAP_CNTPHS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNTPHS																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-373. ECAP_CNTPHS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CNTPHS	R/W	0h	Counter phase value register that can be programmed for phase lag/lead. This register shadows ECAP_TSCNT and is loaded into ECAP_TSCNT upon either a SYNCI event or software force via a control bit. Used to achieve phase control synchronization with respect to other ECAP and EPWM time-bases.

Table 15-374. Register Call Summary for ECAP_CNTPHS

PRU_ECAPH_ECAPH0 Registers
ECAP_CNTPHS Register (Offset = 4h) [reset = 0h]: [0] ECAP_ECCTL2_ECCTL1 Register (Offset = 28h) [reset = 00060000h]: [0] PRU_ECAPH_ECAPH0 Registers: [0]

15.6.3 ECAP_CAP1 Register (Offset = 8h) [reset = 0h]

ECAP_CAP1 is shown in [Figure 15-122](#) and described in [Table 15-376](#).

Return to [Summary Table](#).

Capture-1 Register.

Table 15-375. ECAP_CAP1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_ECAP0_ECAP_SLV	0B03 0008h
PRU_ICSSG1_PR1_ICSS_ECAP0_ECAP_SLV	0B13 0008h

Figure 15-122. ECAP_CAP1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAP1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-376. ECAP_CAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAP1	R/W	0h	This register can be loaded (written) by the following: a) Time-stamp (that is, counter value) during a capture event. b) Software may be useful for test purposes/initialization. c) APRD shadow register (that is, ECAP_CAP3) when used in APWM mode.

Table 15-377. Register Call Summary for ECAP_CAP1

PRU_ECAP_ECAP0 Registers

- [ECAP_ECCTL2_ECCTL1 Register \(Offset = 28h\) \[reset = 00060000h\]: \[0\] \[1\] \[2\] \[3\]](#)
- [ECAP_CAP3 Register \(Offset = 10h\) \[reset = 0h\]: \[0\]](#)
- [PRU_ECAP_ECAP0 Registers: \[0\]](#)
- [ECAP_CAP1 Register \(Offset = 8h\) \[reset = 0h\]: \[0\]](#)

15.6.4 ECAP_CAP2 Register (Offset = Ch) [reset = 0h]

ECAP_CAP2 is shown in [Figure 15-123](#) and described in [Table 15-379](#).

Return to [Summary Table](#).

Capture-2 Register.

Table 15-378. ECAP_CAP2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_ECAP0_ECAP_SLV	0B03 000Ch
PRU_ICSSG1_PR1_ICSS_ECAP0_ECAP_SLV	0B13 000Ch

Figure 15-123. ECAP_CAP2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAP2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-379. ECAP_CAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAP2	R/W	0h	This register can be loaded (written) by the following: a) Time-stamp (that is, counter value) during a capture event. b) Software may be useful for test purposes. c) ACMP shadow register (that is, ECAP_CAP4) when used in APWM mode.

Table 15-380. Register Call Summary for ECAP_CAP2

PRU_ECAP_ECAP0 Registers

- [ECAP_ECCTL2_ECCTL1 Register \(Offset = 28h\) \[reset = 00060000h\]: \[0\] \[1\]](#)
- [ECAP_CAP4 Register \(Offset = 14h\) \[reset = 0h\]: \[0\]](#)
- [ECAP_CAP2 Register \(Offset = Ch\) \[reset = 0h\]: \[0\]](#)
- [PRU_ECAP_ECAP0 Registers: \[0\]](#)

15.6.5 ECAP_CAP3 Register (Offset = 10h) [reset = 0h]

ECAP_CAP3 is shown in [Figure 15-124](#) and described in [Table 15-382](#).

Return to [Summary Table](#).

Capture-3 Register.

Table 15-381. ECAP_CAP3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_ECAP0_ECAP_SLV	0B03 0010h
PRU_ICSSG1_PR1_ICSS_ECAP0_ECAP_SLV	0B13 0010h

Figure 15-124. ECAP_CAP3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAP3																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-382. ECAP_CAP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAP3	R/W	0h	In CMP mode this is a time-stamp capture register. In APWM mode this is the period shadow (APER) register. User updates the PWM period value via this register. In this mode ECAP_CAP3 (APRD) shadows ECAP_CAP1 .

Table 15-383. Register Call Summary for ECAP_CAP3

PRU_ECAP_ECAP0 Registers

- [ECAP_CAP3 Register \(Offset = 10h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [PRU_ECAP_ECAP0 Registers: \[0\]](#)
- [ECAP_CAP1 Register \(Offset = 8h\) \[reset = 0h\]: \[0\]](#)

15.6.6 ECAP_CAP4 Register (Offset = 14h) [reset = 0h]

ECAP_CAP4 is shown in [Figure 15-125](#) and described in [Table 15-385](#).

Return to [Summary Table](#).

Capture-4 Register.

Table 15-384. ECAP_CAP4 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_ECAPH0_ECAPH_SLV	0B03 0014h
PRU_ICSSG1_PR1_ICSS_ECAPH0_ECAPH_SLV	0B13 0014h

Figure 15-125. ECAP_CAP4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAP4																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-385. ECAP_CAP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAP4	R/W	0h	In CMP mode this is a time-stamp capture register. In APWM mode this is the compare shadow (ACMP) register. User updates the PWM compare value via this register. In this mode ECAP_CAP4 (ACMP) shadows ECAP_CAP2 .

Table 15-386. Register Call Summary for ECAP_CAP4

PRU_ECAPH_ECAPH0 Registers	
•	ECAPH_ECCTL2_ECCTL1 Register (Offset = 28h) [reset = 00060000h]: [0] [1]
•	ECAPH_CAP4 Register (Offset = 14h) [reset = 0h]: [0] [1]
•	ECAPH_CAP2 Register (Offset = Ch) [reset = 0h]: [0]
•	PRU_ECAPH_ECAPH0 Registers: [0]

15.6.7 ECAP_ECCTL2_ECCTL1 Register (Offset = 28h) [reset = 00060000h]

ECAP_ECCTL2_ECCTL1 is shown in [Figure 15-126](#) and described in [Table 15-388](#).

Return to [Summary Table](#).

ECAP Control Register 1.

Table 15-387. ECAP_ECCTL2_ECCTL1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_ECAP0_ECAP_SLV	0B03 0028h
PRU_ICSSG1_PR1_ICSS_ECAP0_ECAP_SLV	0B13 0028h

Figure 15-126. ECAP_ECCTL2_ECCTL1 Register

31	30	29	28	27	26	25	24
FILTER					APWMPOL	CAP_APWM	SWSYNC
R-0h					R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
SYNCO_SEL		SYNCL_EN	TSCNTSTP	REARM_RESE T	STOPVALUE		CONT_ONESH T
R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-3h		R/W-0h
15	14	13	12	11	10	9	8
FREE	SOFT	EVTFLTPS					CAPLDEN
R/W-0h	R/W-0h	R/W-0h					R/W-0h
7	6	5	4	3	2	1	0
CTRRST4	CAP4POL	CTRRST3	CAP3POL	CTRRST2	CAP2POL	CTRRST1	CAP1POL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-388. ECAP_ECCTL2_ECCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	FILTER	R	0h	
26	APWMPOL	R/W	0h	APWM output polarity select: 0h = Output is active high (that is, compare value defines high time) 1h = Output is active low (that is, compare value defines low time) Note: This is applicable only in APWM operating mode.
25	CAP_APWM	R/W	0h	CAP/APWM operating mode select: 0h = ECAP module operates in capture mode. This mode forces the following configuration: a) Inhibits ECAP_TSCNT resets via CTR = PRD event b) Inhibits shadow loads on ECAP_CAP1 and ECAP_CAP2 registers. c) Permits user to enable ECAP_CAP1 to ECAP_CAP4 register load. d) ECAP input/APWM output pin operates as a capture input. 1h = ECAP module operates in APWM mode. This mode forces the following configuration: a) Resets TSCNT on CTR = PRD event (period boundary). b) Permits shadow loading on ECAP_CAP1 and ECAP_CAP2 registers. c) Disables loading of time-stamps into ECAP_CAP1 to ECAP_CAP4 registers. d) ECAP input/APWM output pin operates as a APWM output.

Table 15-388. ECAP_ECCTL2_ECCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	SWSYNC	R/W	0h	Software forced counter (ECAP_TSCNT) synchronizing: 0h = Writing a zero has no effect will always return a zero 1h = Writing a one will force a ECAP_TSCNT shadow load of current ECAP module and any ECAP modules down-stream providing the SYNCO_SEL bits are 0b00. After writing a one this bit returns to a zero. Note: This provides a convenient software method to synchronize some or all ECAP timebases. In APWM mode, the synchronizing can also be done via the CTR = PRD event.
23-22	SYNCO_SEL	R/W	0h	Sync-out select: 0h = Select sync-in event to be the sync-out signal (pass through) 1h = Select CTR = PRD event to be the sync-out signal 2h = Disable sync out signal 3h = Disable sync out signal Note: Selection CTR = PRD is meaningful only in APWM mode, however can still be chosen in CAP mode, if user believes it to be useful.
21	SYNCl_EN	R/W	0h	Counter (ECAP_TSCNT) sync-in select mode: 0h = Disable sync-in option 1h = Enable counter (ECAP_TSCNT) to be loaded from ECAP_CNTPHS register upon either a SYNCl signal or a software force event
20	TSCNTSTP	R/W	0h	Counter stop (freeze) control: 0h = Counter stopped 1h = Counter free running
19	REARM_RESET	R/W	0h	One-shot re-arming, that is, wait for stop trigger: 0h = Writing a zero has no effect (reading always returns a 0) 1h = Writing a one arms the one-shot sequence as follows: 1) resets the mod4 counter to zero 2) un-freezes the mod4 counter 3) enables capture register loads Note: The re-arm function is valid in oneshot or continuous mode.
18-17	STOPVALUE	R/W	3h	Stop value for one-shot mode. This is the number (between 1-4) of captures allowed to occur before the CAP(1-4) registers are frozen, that is, capture sequence is stopped. 0h = Stop after capture event 1 1h = Stop after capture event 2 2h = Stop after capture event 3 3h = Stop after capture event 4 Note: STOPVALUE is compared to mod4 counter, and when equal, the following two actions occur: (1) Mod4 counter is stopped (frozen). (2) Capture register loads are inhibited. Note: In one shot mode, further interrupt events are blocked until re-armed, once the number of events captured has been reached .
16	CONT_ONESHT	R/W	0h	Continuous or one-shot mode control (applicable only in capture mode): 0h = Operate in continuous mode 1h = Operate in one-shot mode

Table 15-388. ECAP_ECCTL2_ECCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	FREE	R/W	0h	Emulation control. 0h = ECAP_TSCNT counter stops immediately on emulation suspend 1h = ECAP_TSCNT counter runs until = 0 0b1x = ECAP_TSCNT counter is unaffected by emulation suspend (run free)
14	SOFT	R/W	0h	Emulation control. 0h = ECAP_TSCNT counter stops immediately on emulation suspend 1h = ECAP_TSCNT counter runs until = 0 0b1x = ECAP_TSCNT counter is unaffected by emulation suspend (run free)
13-9	EVTFLTPS	R/W	0h	Event filter prescale select: 0h = Divide by 1 (that is, no prescale, by-pass the prescaler) 1h = Divide by 2 2h = Divide by 4 3h = Divide by 6 4h = Divide by 8 5h = Divide by 10 1Eh = Divide by 60 1Fh = Divide by 62
8	CAPLDEN	R/W	0h	Enable loading of CAP(1-4) registers on a capture event: 0h = Disable CAP (1-4) register loads at capture event time 1h = Enable CAP(1-4) register loads at capture event time
7	CTRRST4	R/W	0h	Counter reset on capture event 4: 0h = Do not reset counter on capture event 4 (absolute time stamp) 1h = Reset counter after event 4 time-stamp has been captured (used in difference mode operation)
6	CAP4POL	R/W	0h	Capture event 4 polarity select: 0h = Capture event 4 triggered on a rising edge (RE) 1h = Capture event 4 triggered on a falling edge (FE)
5	CTRRST3	R/W	0h	Counter reset on capture event 3: 0h = Do not reset counter on capture event 3 (absolute time stamp) 1h = Reset counter after event 3 time-stamp has been captured (used in difference mode operation)
4	CAP3POL	R/W	0h	Capture event 3 polarity select: 0h = Capture event 3 triggered on a rising edge (RE) 1h = Capture event 3 triggered on a falling edge (FE)
3	CTRRST2	R/W	0h	Counter reset on capture event 2: 0h = Do not reset counter on capture event 2 (absolute time stamp) 1h = Reset counter after event 2 time-stamp has been captured (used in difference mode operation)
2	CAP2POL	R/W	0h	Capture event 2 polarity select: 0h = Capture event 2 triggered on a rising edge (RE) 1h = Capture event 2 triggered on a falling edge (FE)
1	CTRRST1	R/W	0h	Counter reset on capture event 1: 0h = Do not reset counter on capture event 1 (absolute time stamp) 1h = Reset counter after event 1 time-stamp has been captured (used in difference mode operation)

Table 15-388. ECAP_ECCTL2_ECCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CAP1POL	R/W	0h	Capture event 1 polarity select: 0h = Capture event 1 triggered on a rising edge (RE) 1h = Capture event 1 triggered on a falling edge (FE)

Table 15-389. Register Call Summary for ECAP_ECCTL2_ECCTL1

PRU_ICSSG ECAP Module
PRU_ICSSG ECAP Functional Description: [0] [1]
PRU_ECAP_ECAP0 Registers
ECAP_ECCTL2_ECCTL1 Register (Offset = 28h) [reset = 00060000h]: [0] PRU_ECAP_ECAP0 Registers: [0]

15.6.8 ECAP_ECFLG_ECEINT Register (Offset = 2Ch) [reset = 0h]

ECAP_ECFLG_ECEINT is shown in [Figure 15-127](#) and described in [Table 15-391](#).

Return to [Summary Table](#).

ECAP Interrupt Enable Register.

Table 15-390. ECAP_ECFLG_ECEINT Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_ECAP0_ECAP_SLV	0B03 002Ch
PRU_ICSSG1_PR1_ICSS_ECAP0_ECAP_SLV	0B13 002Ch

Figure 15-127. ECAP_ECFLG_ECEINT Register

31	30	29	28	27	26	25	24
FLAG_RESV0							
R-0h							
23	22	21	20	19	18	17	16
FLAG_CMPEQ	FLAG_PRDEQ	FLAG_CNTOV F	FLAG_CEV4	FLAG_CEV3	FLAG_CEV2	FLAG_CEV1	FLAG_INT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
EN__RESV1							
R-0h							
7	6	5	4	3	2	1	0
EN_CMPEQ	EN_PRDEQ	EN_CNTOV F	EN_CEV4	EN_CEV3	EN_CEV2	EN_CEV1	EN_RESV0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-391. ECAP_ECFLG_ECEINT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	FLAG_RESV0	R	0h	
23	FLAG_CMPEQ	R	0h	Compare equal status flag: 0h = Indicates no event occurred 1h = Indicates the counter (ECAP_TSCNT) reached the compare register value (ACMP) Note: This flag is only active in APWM mode.
22	FLAG_PRDEQ	R	0h	Period equal status flag: 0h = Indicates no event occurred 1h = Indicates the counter (ECAP_TSCNT) reached the period register value (APER) and was reset Note: This flag is only active in APWM mode.
21	FLAG_CNTOVF	R	0h	Counter overflow status flag: 0h = Indicates no event occurred 1h = Indicates the counter (ECAP_TSCNT) has made the transition from FFFFFFFFh to 00000000h Note: This flag is active in CAP and APWM mode.
20	FLAG_CEV4	R	0h	Capture event 4 status flag: 0h = Indicates no event occurred 1h = Indicates the fourth event occurred at ECAPx pin Note: This flag is only active in CAP mode.

Table 15-391. ECAP_ECFLG_ECEINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	FLAG_C EVT3	R	0h	Capture event 3 status flag: 0h = Indicates no event occurred 1h = Indicates the third event occurred at ECAPx pin Note: This flag is only active in CAP mode.
18	FLAG_C EVT2	R	0h	Capture event 2 status flag: 0h = Indicates no event occurred 1h = Indicates the second event occurred at ECAPx pin Note: This flag is only active in CAP mode.
17	FLAG_C EVT1	R	0h	Capture event 1 status flag: 0h = Indicates no event occurred 1h = Indicates the first event occurred at ECAPx pin Note: This flag is only active in CAP mode.
16	FLAG_INT	R	0h	Global interrupt status flag: 0h = Indicates no interrupt generated 1h = Indicates that an interrupt was generated from one of the following events
15-8	EN__RESV1	R	0h	
7	EN_CMPEQ	R/W	0h	Compare equal interrupt enable: 0h = Disable compare equal as an interrupt source 1h = Enable compare equal as an interrupt source
6	EN_PRDEQ	R/W	0h	Period equal interrupt enable: 0h = Disable period equal as an interrupt source 1h = Enable period equal as an interrupt source
5	EN_CNTOVF	R/W	0h	Counter overflow interrupt enable: 0h = Disable counter overflow as an interrupt source 1h = Enable counter overflow as an interrupt source
4	EN_C EVT4	R/W	0h	Capture event 4 interrupt enable: 0h = Disable capture event 1 as an interrupt source 1h = Enable capture event 1 as an interrupt source
3	EN_C EVT3	R/W	0h	Capture event 3 interrupt enable: 0h = Disable capture event 1 as an interrupt source 1h = Enable capture event 1 as an interrupt source
2	EN_C EVT2	R/W	0h	Capture event 2 interrupt enable: 0h = Disable capture event 1 as an interrupt source 1h = Enable capture event 1 as an interrupt source
1	EN_C EVT1	R/W	0h	Capture event 1 interrupt enable: 0h = Disable capture event 1 as an interrupt source 1h = Enable capture event 1 as an interrupt source
0	EN_RESV0	R	0h	

Table 15-392. Register Call Summary for ECAP_ECFLG_ECEINT

PRU_ECAP_ECAP0 Registers

- [PRU_ECAP_ECAP0 Registers: \[0\]](#)
- [ECAP_ECFLG_ECEINT Register \(Offset = 2Ch\) \[reset = 0h\]: \[0\]](#)

15.6.9 ECAP_ECCLR Register (Offset = 30h) [reset = X]

ECAP_ECCLR is shown in [Figure 15-128](#) and described in [Table 15-394](#).

Return to [Summary Table](#).

ECAP Interrupt Clear Register.

Table 15-393. ECAP_ECCLR Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_ECAP0_ECAP_SLV	0B03 0030h
PRU_ICSSG1_PR1_ICSS_ECAP0_ECAP_SLV	0B13 0030h

Figure 15-128. ECAP_ECCLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
_RESV0							
R-0h							
7	6	5	4	3	2	1	0
CMPEQ	PRDEQ	CNTOVF	CEVT4	CEVT3	CEVT2	CEVT1	INT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-394. ECAP_ECCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-8	_RESV0	R	0h	
7	CMPEQ	R/W	0h	Compare equal status flag: 0h = Writing a 0 has no effect. Always reads back a 0. 1h = Writing a 1 clears the status flag condition
6	PRDEQ	R/W	0h	Period equal status flag: 0h = Writing a 0 has no effect. Always reads back a 0. 1h = Writing a 1 clears the status flag condition
5	CNTOVF	R/W	0h	Counter overflow status flag: 0h = Writing a 0 has no effect. Always reads back a 0. 1h = Writing a 1 clears the status flag condition
4	CEVT4	R/W	0h	Capture event 4 status flag: 0h = Writing a 0 has no effect. Always reads back a 0. 1h = Writing a 1 clears the status flag condition
3	CEVT3	R/W	0h	Capture event 3 status flag: 0h = Writing a 0 has no effect. Always reads back a 0. 1h = Writing a 1 clears the status flag condition
2	CEVT2	R/W	0h	Capture event 2 status flag: 0h = Writing a 0 has no effect. Always reads back a 0. 1h = Writing a 1 clears the status flag condition

Table 15-394. ECAP_ECCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CEVT1	R/W	0h	Capture event 1 status flag: 0h = Writing a 0 has no effect. Always reads back a 0. 1h = Writing a 1 clears the status flag condition
0	INT	R/W	0h	Global interrupt clear flag: 0h = Writing a 0 has no effect. Always reads back a 0. 1h = Writing a 1 clears the clear flag and enable further interrupts to be generated if any of the clear flags are set to 1

Table 15-395. Register Call Summary for ECAP_ECCLR

PRU_ECAP_ECAP0 Registers

- [PRU_ECAP_ECAP0 Registers: \[0\]](#)
- [ECAP_ECCLR Register \(Offset = 30h\) \[reset = X\]: \[0\]](#)

15.6.10 ECAP_ECFRC Register (Offset = 34h) [reset = X]

ECAP_ECFRC is shown in [Figure 15-129](#) and described in [Table 15-397](#).

Return to [Summary Table](#).

ECAP Interrupt Forcing Register.

Table 15-396. ECAP_ECFRC Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_ECAP0_ECAP_SLV	0B03 0034h
PRU_ICSSG1_PR1_ICSS_ECAP0_ECAP_SLV	0B13 0034h

Figure 15-129. ECAP_ECFRC Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
_RESV1							
R-0h							
7	6	5	4	3	2	1	0
CMPEQ	PRDEQ	CNTOVF	CEVT4	CEVT3	CEVT2	CEVT1	_RESV0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-397. ECAP_ECFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-8	_RESV1	R	0h	
7	CMPEQ	R/W	0h	Force compare equal: 0h = Writing of 0 is ignored. Always reads back a 0. 1h = Writing a 1 sets the the CMPEQ flag bit
6	PRDEQ	R/W	0h	Force period equal: 0h = Writing of 0 is ignored. Always reads back a 0. 1h = Writing a 1 sets the PRDEQ flag bit
5	CNTOVF	R/W	0h	Force counter overflow: 0h = Writing of 0 is ignored. Always reads back a 0. 1h = Writing a 1 sets the CNTOVF flag bit
4	CEVT4	R/W	0h	Force capture event 4: 0h = Writing of 0 is ignored. Always reads back a 0. 1h = Writing a 1 sets the CEVT4 flag bit
3	CEVT3	R/W	0h	Force capture event 3: 0h = Writing of 0 is ignored. Always reads back a 0. 1h = Writing a 1 sets the CEVT3 flag bit
2	CEVT2	R/W	0h	Force capture event 2: 0h = Writing of 0 is ignored. Always reads back a 0. 1h = Writing a 1 sets the CEVT2 flag bit

Table 15-397. ECAP_ECFRC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CEVT1	R/W	0h	Force capture event 1: 0h = Writing of 0 is ignored. Always reads back a 0. 1h = Writing a 1 sets the CEVT1 flag bit
0	_RESV0	R	0h	

Table 15-398. Register Call Summary for ECAP_ECFRC

PRU_ECAP_ECAPH Registers

- [ECAP_ECFRC Register \(Offset = 34h\) \[reset = X\]: \[0\]](#)
- [PRU_ECAP_ECAPH Registers: \[0\]](#)

15.6.11 ECAP_PID Register (Offset = 5Ch) [reset = 44D22100h]

ECAP_PID is shown in [Figure 15-130](#) and described in [Table 15-400](#).

Return to [Summary Table](#).

ECAP Peripheral Id Register.

Table 15-399. ECAP_PID Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_ECAP0_ECAP_SLV	0B03 005Ch
PRU_ICSSG1_PR1_ICSS_ECAP0_ECAP_SLV	0B13 005Ch

Figure 15-130. ECAP_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVID																															
R-44D22100h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-400. ECAP_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REVID	R	44D22100h	TI internal data.

Table 15-401. Register Call Summary for ECAP_PID

PRU_ECAP_ECAP0 Registers

- [ECAP_PID Register \(Offset = 5Ch\) \[reset = 44D22100h\]: \[0\]](#)
- [PRU_ECAP_ECAP0 Registers: \[0\]](#)

15.7 PRU_ICSS_INTC_INTC Registers

Table 15-403 lists the memory-mapped registers for the PRU_ICSS_INTC_INTC registers. All register offset addresses not listed in Table 15-403 should be considered as reserved locations and the register contents should not be modified.

Table 15-402. PRU_ICSS_INTC_INTC Instances

Instance	Base Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0000h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0000h

Table 15-403. PRU_ICSS_INTC_INTC Registers

Offset	Acronym	Register Name	PRU_ICSSG0_P R1_ICSS_INTC_I NTC_SLV Physical Address	PRU_ICSSG1_P R1_ICSS_INTC_I NTC_SLV Physical Address
0h	ICSS_INTC_REVISION_REG	Revision Register	0B02 0000h	0B12 0000h
4h	ICSS_INTC_CONTROL_REG	Control Register	0B02 0004h	0B12 0004h
10h	ICSS_INTC_GLOBAL_ENABLE_HINT_REG	Global Host Int Enable Register	0B02 0010h	0B12 0010h
1Ch	ICSS_INTC_GLB_NEST_LEVEL_REG	Global Nesting Level Register	0B02 001Ch	0B12 001Ch
20h	ICSS_INTC_STATUS_SET_INDEX_REG	Status Set Index Register	0B02 0020h	0B12 0020h
24h	ICSS_INTC_STATUS_CLR_INDEX_REG	Status Clear Index Register	0B02 0024h	0B12 0024h
28h	ICSS_INTC_ENABLE_SET_INDEX_REG	Enable Set Index Register	0B02 0028h	0B12 0028h
2Ch	ICSS_INTC_ENABLE_CLR_INDEX_REG	Enable Clear Index Register	0B02 002Ch	0B12 002Ch
34h	ICSS_INTC_HINT_ENABLE_SET_INDEX_REG	Host Int Enable Set Index Register	0B02 0034h	0B12 0034h
38h	ICSS_INTC_HINT_ENABLE_CLR_INDEX_REG	Host Int Enable Clear Index Register	0B02 0038h	0B12 0038h
80h	ICSS_INTC_GLB_PRI_INTR_REG	Global Prioritized Interrupt Register	0B02 0080h	0B12 0080h
200h	ICSS_INTC_RAW_STATUS_REG0	Raw Status Register 0	0B02 0200h	0B12 0200h
204h	ICSS_INTC_RAW_STATUS_REG1	Raw Status Register 1	0B02 0204h	0B12 0204h
208h	ICSS_INTC_RAW_STATUS_REG2	Raw Status Register 2	0B02 0208h	0B12 0208h
20Ch	ICSS_INTC_RAW_STATUS_REG3	Raw Status Register 3	0B02 020Ch	0B12 020Ch
210h	ICSS_INTC_RAW_STATUS_REG4	Raw Status Register 4	0B02 0210h	0B12 0210h
280h	ICSS_INTC_ENA_STATUS_REG0	Enabled Status Register 0	0B02 0280h	0B12 0280h
284h	ICSS_INTC_ENA_STATUS_REG1	Enabled Status Register 1	0B02 0284h	0B12 0284h
288h	ICSS_INTC_ENA_STATUS_REG2	Enabled Status Register 2	0B02 0288h	0B12 0288h
28Ch	ICSS_INTC_ENA_STATUS_REG3	Enabled Status Register 3	0B02 028Ch	0B12 028Ch
290h	ICSS_INTC_ENA_STATUS_REG4	Enabled Status Register 4	0B02 0290h	0B12 0290h
300h	ICSS_INTC_ENABLE_REG0	Enable Register 0	0B02 0300h	0B12 0300h
304h	ICSS_INTC_ENABLE_REG1	Enable Register 1	0B02 0304h	0B12 0304h
308h	ICSS_INTC_ENABLE_REG2	Enable Register 2	0B02 0308h	0B12 0308h
30Ch	ICSS_INTC_ENABLE_REG3	Enable Register 3	0B02 030Ch	0B12 030Ch
310h	ICSS_INTC_ENABLE_REG4	Enable Register 4	0B02 0310h	0B12 0310h
380h	ICSS_INTC_ENABLE_CLR_REG0	Enable Clear Register 0	0B02 0380h	0B12 0380h
384h	ICSS_INTC_ENABLE_CLR_REG1	Enable Clear Register 1	0B02 0384h	0B12 0384h
388h	ICSS_INTC_ENABLE_CLR_REG2	Enable Clear Register 2	0B02 0388h	0B12 0388h
38Ch	ICSS_INTC_ENABLE_CLR_REG3	Enable Clear Register 3	0B02 038Ch	0B12 038Ch
390h	ICSS_INTC_ENABLE_CLR_REG4	Enable Clear Register 4	0B02 0390h	0B12 0390h
400h	ICSS_INTC_CH_MAP_REG0	Interrupt Channel Map Register for 0 to 0+3	0B02 0400h	0B12 0400h

Table 15-403. PRU_ICSS_INTC_INTC Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG0_P R1_ICSS_INTC_I NTC_SLV Physical Address	PRU_ICSSG1_P R1_ICSS_INTC_I NTC_SLV Physical Address
404h	ICSS_INTC_CH_MAP_REG1	Interrupt Channel Map Register for 4 to 4+3	0B02 0404h	0B12 0404h
408h	ICSS_INTC_CH_MAP_REG2	Interrupt Channel Map Register for 8 to 8+3	0B02 0408h	0B12 0408h
40Ch	ICSS_INTC_CH_MAP_REG3	Interrupt Channel Map Register for 12 to 12+3	0B02 040Ch	0B12 040Ch
410h	ICSS_INTC_CH_MAP_REG4	Interrupt Channel Map Register for 16 to 16+3	0B02 0410h	0B12 0410h
414h	ICSS_INTC_CH_MAP_REG5	Interrupt Channel Map Register for 20 to 20+3	0B02 0414h	0B12 0414h
418h	ICSS_INTC_CH_MAP_REG6	Interrupt Channel Map Register for 24 to 24+3	0B02 0418h	0B12 0418h
41Ch	ICSS_INTC_CH_MAP_REG7	Interrupt Channel Map Register for 28 to 28+3	0B02 041Ch	0B12 041Ch
420h	ICSS_INTC_CH_MAP_REG8	Interrupt Channel Map Register for 32 to 32+3	0B02 0420h	0B12 0420h
424h	ICSS_INTC_CH_MAP_REG9	Interrupt Channel Map Register for 36 to 36+3	0B02 0424h	0B12 0424h
428h	ICSS_INTC_CH_MAP_REG10	Interrupt Channel Map Register for 40 to 40+3	0B02 0428h	0B12 0428h
42Ch	ICSS_INTC_CH_MAP_REG11	Interrupt Channel Map Register for 44 to 44+3	0B02 042Ch	0B12 042Ch
430h	ICSS_INTC_CH_MAP_REG12	Interrupt Channel Map Register for 48 to 48+3	0B02 0430h	0B12 0430h
434h	ICSS_INTC_CH_MAP_REG13	Interrupt Channel Map Register for 52 to 52+3	0B02 0434h	0B12 0434h
438h	ICSS_INTC_CH_MAP_REG14	Interrupt Channel Map Register for 56 to 56+3	0B02 0438h	0B12 0438h
43Ch	ICSS_INTC_CH_MAP_REG15	Interrupt Channel Map Register for 60 to 60+3	0B02 043Ch	0B12 043Ch
440h	ICSS_INTC_CH_MAP_REG16	Interrupt Channel Map Register for 64 to 64+3	0B02 0440h	0B12 0440h
444h	ICSS_INTC_CH_MAP_REG17	Interrupt Channel Map Register for 68 to 68+3	0B02 0444h	0B12 0444h
448h	ICSS_INTC_CH_MAP_REG18	Interrupt Channel Map Register for 72 to 72+3	0B02 0448h	0B12 0448h
44Ch	ICSS_INTC_CH_MAP_REG19	Interrupt Channel Map Register for 76 to 76+3	0B02 044Ch	0B12 044Ch
450h	ICSS_INTC_CH_MAP_REG20	Interrupt Channel Map Register for 80 to 80+3	0B02 0450h	0B12 0450h
454h	ICSS_INTC_CH_MAP_REG21	Interrupt Channel Map Register for 84 to 84+3	0B02 0454h	0B12 0454h
458h	ICSS_INTC_CH_MAP_REG22	Interrupt Channel Map Register for 88 to 88+3	0B02 0458h	0B12 0458h
45Ch	ICSS_INTC_CH_MAP_REG23	Interrupt Channel Map Register for 92 to 92+3	0B02 045Ch	0B12 045Ch
460h	ICSS_INTC_CH_MAP_REG24	Interrupt Channel Map Register for 96 to 96+3	0B02 0460h	0B12 0460h
464h	ICSS_INTC_CH_MAP_REG25	Interrupt Channel Map Register for 100 to 100+3	0B02 0464h	0B12 0464h
468h	ICSS_INTC_CH_MAP_REG26	Interrupt Channel Map Register for 104 to 104+3	0B02 0468h	0B12 0468h

Table 15-403. PRU_ICSS_INTC_INTC Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG0_P R1_ICSS_INTC_I NTC_SLV Physical Address	PRU_ICSSG1_P R1_ICSS_INTC_I NTC_SLV Physical Address
46Ch	ICSS_INTC_CH_MAP_REG27	Interrupt Channel Map Register for 108 to 108+3	0B02 046Ch	0B12 046Ch
470h	ICSS_INTC_CH_MAP_REG28	Interrupt Channel Map Register for 112 to 112+3	0B02 0470h	0B12 0470h
474h	ICSS_INTC_CH_MAP_REG29	Interrupt Channel Map Register for 116 to 116+3	0B02 0474h	0B12 0474h
478h	ICSS_INTC_CH_MAP_REG30	Interrupt Channel Map Register for 120 to 120+3	0B02 0478h	0B12 0478h
47Ch	ICSS_INTC_CH_MAP_REG31	Interrupt Channel Map Register for 124 to 124+3	0B02 047Ch	0B12 047Ch
480h	ICSS_INTC_CH_MAP_REG32	Interrupt Channel Map Register for 128 to 128+3	0B02 0480h	0B12 0480h
484h	ICSS_INTC_CH_MAP_REG33	Interrupt Channel Map Register for 132 to 132+3	0B02 0484h	0B12 0484h
488h	ICSS_INTC_CH_MAP_REG34	Interrupt Channel Map Register for 136 to 136+3	0B02 0488h	0B12 0488h
48Ch	ICSS_INTC_CH_MAP_REG35	Interrupt Channel Map Register for 140 to 140+3	0B02 048Ch	0B12 048Ch
490h	ICSS_INTC_CH_MAP_REG36	Interrupt Channel Map Register for 144 to 144+3	0B02 0490h	0B12 0490h
494h	ICSS_INTC_CH_MAP_REG37	Interrupt Channel Map Register for 148 to 148+3	0B02 0494h	0B12 0494h
498h	ICSS_INTC_CH_MAP_REG38	Interrupt Channel Map Register for 152 to 152+3	0B02 0498h	0B12 0498h
49Ch	ICSS_INTC_CH_MAP_REG39	Interrupt Channel Map Register for 156 to 156+3	0B02 049Ch	0B12 049Ch
800h	ICSS_INTC_HINT_MAP_REG0	Host Interrupt Map Register for 0 to 0+3	0B02 0800h	0B12 0800h
804h	ICSS_INTC_HINT_MAP_REG1	Host Interrupt Map Register for 4 to 4+3	0B02 0804h	0B12 0804h
808h	ICSS_INTC_HINT_MAP_REG2	Host Interrupt Map Register for 8 to 8+3	0B02 0808h	0B12 0808h
80Ch	ICSS_INTC_HINT_MAP_REG3	Host Interrupt Map Register for 12 to 12+3	0B02 080Ch	0B12 080Ch
810h	ICSS_INTC_HINT_MAP_REG4	Host Interrupt Map Register for 16 to 16+4	0B02 0810h	0B12 0810h
900h	ICSS_INTC_PRI_HINT_REG0	Host Int 0 Prioritized Interrupt Register	0B02 0900h	0B12 0900h
904h	ICSS_INTC_PRI_HINT_REG1	Host Int 1 Prioritized Interrupt Register	0B02 0904h	0B12 0904h
908h	ICSS_INTC_PRI_HINT_REG2	Host Int 2 Prioritized Interrupt Register	0B02 0908h	0B12 0908h
90Ch	ICSS_INTC_PRI_HINT_REG3	Host Int 3 Prioritized Interrupt Register	0B02 090Ch	0B12 090Ch
910h	ICSS_INTC_PRI_HINT_REG4	Host Int 4 Prioritized Interrupt Register	0B02 0910h	0B12 0910h
914h	ICSS_INTC_PRI_HINT_REG5	Host Int 5 Prioritized Interrupt Register	0B02 0914h	0B12 0914h
918h	ICSS_INTC_PRI_HINT_REG6	Host Int 6 Prioritized Interrupt Register	0B02 0918h	0B12 0918h
91Ch	ICSS_INTC_PRI_HINT_REG7	Host Int 7 Prioritized Interrupt Register	0B02 091Ch	0B12 091Ch
920h	ICSS_INTC_PRI_HINT_REG8	Host Int 8 Prioritized Interrupt Register	0B02 0920h	0B12 0920h
924h	ICSS_INTC_PRI_HINT_REG9	Host Int 9 Prioritized Interrupt Register	0B02 0924h	0B12 0924h
928h	ICSS_INTC_PRI_HINT_REG10	Host Int 10 Prioritized Interrupt Register	0B02 0928h	0B12 0928h
92Ch	ICSS_INTC_PRI_HINT_REG11	Host Int 11 Prioritized Interrupt Register	0B02 092Ch	0B12 092Ch
930h	ICSS_INTC_PRI_HINT_REG12	Host Int 12 Prioritized Interrupt Register	0B02 0930h	0B12 0930h
934h	ICSS_INTC_PRI_HINT_REG13	Host Int 13 Prioritized Interrupt Register	0B02 0934h	0B12 0934h
938h	ICSS_INTC_PRI_HINT_REG14	Host Int 14 Prioritized Interrupt Register	0B02 0938h	0B12 0938h
93Ch	ICSS_INTC_PRI_HINT_REG15	Host Int 15 Prioritized Interrupt Register	0B02 093Ch	0B12 093Ch

Table 15-403. PRU_ICSS_INTC_INTC Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG0_P R1_ICSS_INTC_I NTC_SLV Physical Address	PRU_ICSSG1_P R1_ICSS_INTC_I NTC_SLV Physical Address
940h	ICSS_INTC_PRI_HINT_REG16	Host Int 16 Prioritized Interrupt Register	0B02 0940h	0B12 0940h
944h	ICSS_INTC_PRI_HINT_REG17	Host Int 17 Prioritized Interrupt Register	0B02 0944h	0B12 0944h
948h	ICSS_INTC_PRI_HINT_REG18	Host Int 18 Prioritized Interrupt Register	0B02 0948h	0B12 0948h
94Ch	ICSS_INTC_PRI_HINT_REG19	Host Int 19 Prioritized Interrupt Register	0B02 094Ch	0B12 094Ch
D00h	ICSS_INTC_POLARITY_REG0	Polarity Register 0	0B02 0D00h	0B12 0D00h
D04h	ICSS_INTC_POLARITY_REG1	Polarity Register 1	0B02 0D04h	0B12 0D04h
D08h	ICSS_INTC_POLARITY_REG2	Polarity Register 2	0B02 0D08h	0B12 0D08h
D0Ch	ICSS_INTC_POLARITY_REG3	Polarity Register 3	0B02 0D0Ch	0B12 0D0Ch
D10h	ICSS_INTC_POLARITY_REG4	Polarity Register 4	0B02 0D10h	0B12 0D10h
D80h	ICSS_INTC_TYPE_REG0	Type Register 0	0B02 0D80h	0B12 0D80h
D84h	ICSS_INTC_TYPE_REG1	Type Register 1	0B02 0D84h	0B12 0D84h
D88h	ICSS_INTC_TYPE_REG2	Type Register 2	0B02 0D88h	0B12 0D88h
D8Ch	ICSS_INTC_TYPE_REG3	Type Register 3	0B02 0D8Ch	0B12 0D8Ch
D90h	ICSS_INTC_TYPE_REG4	Type Register 4	0B02 0D90h	0B12 0D90h
1100h	ICSS_INTC_NEST_LEVEL_REG0	Host Int 0 Nesting Level Register	0B02 1100h	0B12 1100h
1104h	ICSS_INTC_NEST_LEVEL_REG1	Host Int 1 Nesting Level Register	0B02 1104h	0B12 1104h
1108h	ICSS_INTC_NEST_LEVEL_REG2	Host Int 2 Nesting Level Register	0B02 1108h	0B12 1108h
110Ch	ICSS_INTC_NEST_LEVEL_REG3	Host Int 3 Nesting Level Register	0B02 110Ch	0B12 110Ch
1110h	ICSS_INTC_NEST_LEVEL_REG4	Host Int 4 Nesting Level Register	0B02 1110h	0B12 1110h
1114h	ICSS_INTC_NEST_LEVEL_REG5	Host Int 5 Nesting Level Register	0B02 1114h	0B12 1114h
1118h	ICSS_INTC_NEST_LEVEL_REG6	Host Int 6 Nesting Level Register	0B02 1118h	0B12 1118h
111Ch	ICSS_INTC_NEST_LEVEL_REG7	Host Int 7 Nesting Level Register	0B02 111Ch	0B12 111Ch
1120h	ICSS_INTC_NEST_LEVEL_REG8	Host Int 8 Nesting Level Register	0B02 1120h	0B12 1120h
1124h	ICSS_INTC_NEST_LEVEL_REG9	Host Int 9 Nesting Level Register	0B02 1124h	0B12 1124h
1128h	ICSS_INTC_NEST_LEVEL_REG10	Host Int 10 Nesting Level Register	0B02 1128h	0B12 1128h
112Ch	ICSS_INTC_NEST_LEVEL_REG11	Host Int 11 Nesting Level Register	0B02 112Ch	0B12 112Ch
1130h	ICSS_INTC_NEST_LEVEL_REG12	Host Int 12 Nesting Level Register	0B02 1130h	0B12 1130h
1134h	ICSS_INTC_NEST_LEVEL_REG13	Host Int 13 Nesting Level Register	0B02 1134h	0B12 1134h
1138h	ICSS_INTC_NEST_LEVEL_REG14	Host Int 14 Nesting Level Register	0B02 1138h	0B12 1138h
113Ch	ICSS_INTC_NEST_LEVEL_REG15	Host Int 15 Nesting Level Register	0B02 113Ch	0B12 113Ch
1140h	ICSS_INTC_NEST_LEVEL_REG16	Host Int 16 Nesting Level Register	0B02 1140h	0B12 1140h
1144h	ICSS_INTC_NEST_LEVEL_REG17	Host Int 17 Nesting Level Register	0B02 1144h	0B12 1144h
1148h	ICSS_INTC_NEST_LEVEL_REG18	Host Int 18 Nesting Level Register	0B02 1148h	0B12 1148h
114Ch	ICSS_INTC_NEST_LEVEL_REG19	Host Int 19 Nesting Level Register	0B02 114Ch	0B12 114Ch
1500h	ICSS_INTC_ENABLE_HINT_REG0	Host Int Enable Register 0	0B02 1500h	0B12 1500h

15.7.1 ICSS_INTC_REVISION_REG Register (Offset = 0h) [reset = X]

ICSS_INTC_REVISION_REG is shown in Figure 15-131 and described in Table 15-405.

Return to [Summary Table](#).

Revision Register

Table 15-404. ICSS_INTC_REVISION_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTCL_SLV	0B02 0000h
PRU_ICSSG1_PR1_ICSS_INTC_INTCL_SLV	0B12 0000h

Figure 15-131. ICSS_INTC_REVISION_REG Register

31	30	29	28	27	26	25	24
REV_SCHEME		RESERVED		REV_MODULE			
R-1h		R-X		R-E82h			
23	22	21	20	19	18	17	16
REV_MODULE							
R-E82h							
15	14	13	12	11	10	9	8
REV_RTL					REV_MAJOR		
R-15h					R-1h		
7	6	5	4	3	2	1	0
REV_CUSTOM		REV_MINOR					
R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 15-405. ICSS_INTC_REVISION_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	REV_SCHEME	R	1h	Scheme
29-28	RESERVED	R	X	
27-16	REV_MODULE	R	E82h	Module ID
15-11	REV_RTL	R	15h	RTL revisions
10-8	REV_MAJOR	R	1h	Major revision
7-6	REV_CUSTOM	R	0h	Custom revision
5-0	REV_MINOR	R	0h	Minor revision

Table 15-406. Register Call Summary for ICSS_INTC_REVISION_REG

PRU_ICSS_INTCL_INTCL Registers

- [ICSS_INTCL_REVISION_REG Register \(Offset = 0h\) \[reset = X\]: \[0\]](#)
- [PRU_ICSS_INTCL_INTCL Registers: \[0\]](#)

15.7.2 ICSS_INTC_CONTROL_REG Register (Offset = 4h) [reset = X]

ICSS_INTC_CONTROL_REG is shown in [Figure 15-132](#) and described in [Table 15-408](#).

Return to [Summary Table](#).

Control Register

Table 15-407. ICSS_INTC_CONTROL_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTCLV	0B02 0004h
PRU_ICSSG1_PR1_ICSS_INTC_INTCLV	0B12 0004h

Figure 15-132. ICSS_INTC_CONTROL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED			PRIORITY_HOLD_MODE	NEST_MODE		WAKEUP_MODE	RESERVED
R/W-X			R/W-0h	R/W-0h		R/W-0h	R/W-X

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-408. ICSS_INTC_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R/W	X	
4	PRIORITY_HOLD_MODE	R/W	0h	Priority Holding Mode
3-2	NEST_MODE	R/W	0h	Nesting Mode
1	WAKEUP_MODE	R/W	0h	Wakeup mode enable
0	RESERVED	R/W	X	

Table 15-409. Register Call Summary for ICSS_INTC_CONTROL_REG

PRU_ICSS_INTC_INTCLV Registers

- [PRU_ICSS_INTC_INTCLV Registers: \[0\]](#)
- [ICSS_INTC_CONTROL_REG Register \(Offset = 4h\) \[reset = X\]: \[0\]](#)

15.7.3 ICSS_INTC_GLOBAL_ENABLE_HINT_REG Register (Offset = 10h) [reset = X]

ICSS_INTC_GLOBAL_ENABLE_HINT_REG is shown in [Figure 15-133](#) and described in [Table 15-411](#).

Return to [Summary Table](#).

Global Host Int Enable Register

Table 15-410. ICSS_INTC_GLOBAL_ENABLE_HINT_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0010h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0010h

Figure 15-133. ICSS_INTC_GLOBAL_ENABLE_HINT_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							ENABLE_HINT_ANY
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-411. ICSS_INTC_GLOBAL_ENABLE_HINT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	ENABLE_HINT_ANY	R/W	0h	Global Enable for all Host Interrupts

Table 15-412. Register Call Summary for ICSS_INTC_GLOBAL_ENABLE_HINT_REG

PRU_ICSS_INTC_INTC Registers
PRU_ICSS_INTC_INTC Registers: [0] ICSS_INTC_GLOBAL_ENABLE_HINT_REG Register (Offset = 10h) [reset = X]: [0]
PRU_ICSSG Local INTC
PRU_ICSSG Interrupt Controller Basic Programming Model: [0]
PRU_ICSSG Interrupt Controller Functional Description
PRU_ICSSG Interrupt Enabling: [0]

15.7.4 ICSS_INTC_GLB_NEST_LEVEL_REG Register (Offset = 1Ch) [reset = X]

ICSS_INTC_GLB_NEST_LEVEL_REG is shown in [Figure 15-134](#) and described in [Table 15-414](#).

Return to [Summary Table](#).

Global Nesting Level Register

Table 15-413. ICSS_INTC_GLB_NEST_LEVEL_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 001Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 001Ch

Figure 15-134. ICSS_INTC_GLB_NEST_LEVEL_REG Register

31	30	29	28	27	26	25	24
GLB_NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							GLB_NEST_LEVEL
R/W-X							R/W-100h
7	6	5	4	3	2	1	0
GLB_NEST_LEVEL							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 15-414. ICSS_INTC_GLB_NEST_LEVEL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GLB_NEST_AUTO_OVR	W	X	Global Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	GLB_NEST_LEVEL	R/W	100h	Global Nesting Level

Table 15-415. Register Call Summary for ICSS_INTC_GLB_NEST_LEVEL_REG

PRU_ICSS_INTC_INTC Registers
- ICSS_INTC_GLB_NEST_LEVEL_REG Register (Offset = 1Ch) [reset = X]: [0] - PRU_ICSS_INTC_INTC Registers: [0]
PRU_ICSSG Interrupt Controller Functional Description
PRU_ICSSG Interrupt Nesting: [0]

15.7.5 ICSS_INTC_STATUS_SET_INDEX_REG Register (Offset = 20h) [reset = X]

ICSS_INTC_STATUS_SET_INDEX_REG is shown in Figure 15-135 and described in Table 15-417.

Return to [Summary Table](#).

Status Set Index Register

Table 15-416. ICSS_INTC_STATUS_SET_INDEX_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0020h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0020h

Figure 15-135. ICSS_INTC_STATUS_SET_INDEX_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								STATUS_SET_INDEX							
W-X								W-0h							

LEGEND: W = Write Only; -n = value after reset

Table 15-417. ICSS_INTC_STATUS_SET_INDEX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	W	X	
9-0	STATUS_SET_INDEX	W	0h	Status Set Index Register (write index to set status)

Table 15-418. Register Call Summary for ICSS_INTC_STATUS_SET_INDEX_REG

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_STATUS_SET_INDEX_REG Register \(Offset = 20h\) \[reset = X\]: \[0\]](#)

15.7.6 ICSS_INTC_STATUS_CLR_INDEX_REG Register (Offset = 24h) [reset = X]

ICSS_INTC_STATUS_CLR_INDEX_REG is shown in Figure 15-136 and described in Table 15-420.

Return to [Summary Table](#).

Status Clear Index Register

Table 15-419. ICSS_INTC_STATUS_CLR_INDEX_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0024h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0024h

Figure 15-136. ICSS_INTC_STATUS_CLR_INDEX_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								STATUS_CLR_INDEX							
W-X								W-0h							

LEGEND: W = Write Only; -n = value after reset

Table 15-420. ICSS_INTC_STATUS_CLR_INDEX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	W	X	
9-0	STATUS_CLR_INDEX	W	0h	Status Clear Index Register (write index to clear status of)

Table 15-421. Register Call Summary for ICSS_INTC_STATUS_CLR_INDEX_REG

PRU_ICSS_INTC_INTC Registers	
PRU_ICSS_INTC_INTC Registers: [0] ICSS_INTC_STATUS_CLR_INDEX_REG Register (Offset = 24h) [reset = X]: [0]	
PRU_ICSSG Interrupt Controller Functional Description	
PRU_ICSSG Interrupt Status Clearing: [0]	

15.7.7 ICSS_INTC_ENABLE_SET_INDEX_REG Register (Offset = 28h) [reset = X]

ICSS_INTC_ENABLE_SET_INDEX_REG is shown in Figure 15-137 and described in Table 15-423.

Return to [Summary Table](#).

Enable Set Index Register

Table 15-422. ICSS_INTC_ENABLE_SET_INDEX_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTCLV	0B02 0028h
PRU_ICSSG1_PR1_ICSS_INTC_INTCLV	0B12 0028h

Figure 15-137. ICSS_INTC_ENABLE_SET_INDEX_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								ENABLE_SET_INDEX							
W-X								W1S-0h							

LEGEND: W = Write Only; W1S = Write 1 to Set Bit; -n = value after reset

Table 15-423. ICSS_INTC_ENABLE_SET_INDEX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	W	X	
9-0	ENABLE_SET_INDEX	W1S	0h	Enable Set Index Register (write index to set enable of)

Table 15-424. Register Call Summary for ICSS_INTC_ENABLE_SET_INDEX_REG

PRU_ICSS_INTCLV Registers
PRU_ICSS_INTCLV Registers: [0] ICSS_INTCLV_ENABLE_SET_INDEX_REG Register (Offset = 28h) [reset = X]: [0]
PRU_ICSSG Interrupt Controller Functional Description
PRU_ICSSG Interrupt Enabling: [0]

15.7.8 ICSS_INTC_ENABLE_CLR_INDEX_REG Register (Offset = 2Ch) [reset = X]

ICSS_INTC_ENABLE_CLR_INDEX_REG is shown in [Figure 15-138](#) and described in [Table 15-426](#).

Return to [Summary Table](#).

Enable Clear Index Register

Table 15-425. ICSS_INTC_ENABLE_CLR_INDEX_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTCLV	0B02 002Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTCLV	0B12 002Ch

Figure 15-138. ICSS_INTC_ENABLE_CLR_INDEX_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								ENABLE_CLR_INDEX							
W-X								W1C-0h							

LEGEND: W = Write Only; W1C = Write 1 to Clear Bit; -n = value after reset

Table 15-426. ICSS_INTC_ENABLE_CLR_INDEX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	W	X	
9-0	ENABLE_CLR_INDEX	W1C	0h	Enable Clear Index Register (write index to clear enable of)

Table 15-427. Register Call Summary for ICSS_INTC_ENABLE_CLR_INDEX_REG

PRU_ICSS_INTCLV Registers
PRU_ICSS_INTCLV Registers: [0] ICSS_INTC_ENABLE_CLR_INDEX_REG Register (Offset = 2Ch) [reset = X]: [0]
PRU_ICSSG Interrupt Controller Functional Description
PRU_ICSSG Interrupt Disabling: [0]

15.7.9 ICSS_INTC_HINT_ENABLE_SET_INDEX_REG Register (Offset = 34h) [reset = X]

ICSS_INTC_HINT_ENABLE_SET_INDEX_REG is shown in Figure 15-139 and described in Table 15-429.

Return to [Summary Table](#).

Host Int Enable Set Index Register

Table 15-428. ICSS_INTC_HINT_ENABLE_SET_INDEX_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0034h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0034h

Figure 15-139. ICSS_INTC_HINT_ENABLE_SET_INDEX_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								HINT_ENABLE_SET_INDEX							
W-X								W1S-0h							

LEGEND: W = Write Only; W1S = Write 1 to Set Bit; -n = value after reset

Table 15-429. ICSS_INTC_HINT_ENABLE_SET_INDEX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	W	X	
9-0	HINT_ENABLE_SET_INDEX	W1S	0h	Enable SET for Host Interrupts

Table 15-430. Register Call Summary for ICSS_INTC_HINT_ENABLE_SET_INDEX_REG

PRU_ICSS_INTC_INTC Registers
PRU_ICSS_INTC_INTC Registers: [0] ICSS_INTC_HINT_ENABLE_SET_INDEX_REG Register (Offset = 34h) [reset = X]: [0]
PRU_ICSSG Local INTC
PRU_ICSSG Interrupt Controller Basic Programming Model: [0]
PRU_ICSSG Interrupt Controller Functional Description
PRU_ICSSG Interrupt Enabling: [0]

15.7.10 ICSS_INTC_HINT_ENABLE_CLR_INDEX_REG Register (Offset = 38h) [reset = X]

ICSS_INTC_HINT_ENABLE_CLR_INDEX_REG is shown in Figure 15-140 and described in Table 15-432.

Return to [Summary Table](#).

Host Int Enable Clear Index Register

Table 15-431. ICSS_INTC_HINT_ENABLE_CLR_INDEX_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0038h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0038h

Figure 15-140. ICSS_INTC_HINT_ENABLE_CLR_INDEX_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						HINT_ENABLE_CLR_INDEX									
W-X						W1C-0h									

LEGEND: W = Write Only; W1C = Write 1 to Clear Bit; -n = value after reset

Table 15-432. ICSS_INTC_HINT_ENABLE_CLR_INDEX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	W	X	
9-0	HINT_ENABLE_CLR_INDEX	W1C	0h	Enable CLEAR for Host Interrupts

Table 15-433. Register Call Summary for ICSS_INTC_HINT_ENABLE_CLR_INDEX_REG

PRU_ICSS_INTC_INTC Registers

- [ICSS_INTC_HINT_ENABLE_CLR_INDEX_REG Register \(Offset = 38h\) \[reset = X\]: \[0\]](#)
- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)

15.7.11 ICSS_INTC_GLB_PRI_INTR_REG Register (Offset = 80h) [reset = X]

ICSS_INTC_GLB_PRI_INTR_REG is shown in Figure 15-141 and described in Table 15-435.

Return to [Summary Table](#).

Global Prioritized Interrupt Register

Table 15-434. ICSS_INTC_GLB_PRI_INTR_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0080h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0080h

Figure 15-141. ICSS_INTC_GLB_PRI_INTR_REG Register

31	30	29	28	27	26	25	24
GLB_NONE	RESERVED						
R-1h	R-X						
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED						GLB_PRI_INTR	
R-X						R-0h	
7	6	5	4	3	2	1	0
GLB_PRI_INTR							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 15-435. ICSS_INTC_GLB_PRI_INTR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GLB_NONE	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	GLB_PRI_INTR	R	0h	Prioritized Interrupt

Table 15-436. Register Call Summary for ICSS_INTC_GLB_PRI_INTR_REG

PRU_ICSS_INTC_INTC Registers
PRU_ICSS_INTC_INTC Registers: [0] ICSS_INTC_GLB_PRI_INTR_REG Register (Offset = 80h) [reset = X]: [0]
PRU_ICSSG Interrupt Controller Functional Description
PRU_ICSSG Interrupt Prioritization: [0]

15.7.12 ICSS_INTC_RAW_STATUS_REG0 Register (Offset = 200h) [reset = 0h]

ICSS_INTC_RAW_STATUS_REG0 is shown in Figure 15-142 and described in Table 15-438.

Return to [Summary Table](#).

Raw Status Register 0

Table 15-437. ICSS_INTC_RAW_STATUS_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0200h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0200h

Figure 15-142. ICSS_INTC_RAW_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RAW_STATUS_31	RAW_STATUS_30	RAW_STATUS_29	RAW_STATUS_28	RAW_STATUS_27	RAW_STATUS_26	RAW_STATUS_25	RAW_STATUS_24
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
23	22	21	20	19	18	17	16
RAW_STATUS_23	RAW_STATUS_22	RAW_STATUS_21	RAW_STATUS_20	RAW_STATUS_19	RAW_STATUS_18	RAW_STATUS_17	RAW_STATUS_16
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
15	14	13	12	11	10	9	8
RAW_STATUS_15	RAW_STATUS_14	RAW_STATUS_13	RAW_STATUS_12	RAW_STATUS_11	RAW_STATUS_10	RAW_STATUS_9	RAW_STATUS_8
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
7	6	5	4	3	2	1	0
RAW_STATUS_7	RAW_STATUS_6	RAW_STATUS_5	RAW_STATUS_4	RAW_STATUS_3	RAW_STATUS_2	RAW_STATUS_1	RAW_STATUS_0
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h

LEGEND: W1S = Write 1 to Set Bit; -n = value after reset

Table 15-438. ICSS_INTC_RAW_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RAW_STATUS_31	W1S	0h	Raw Status (write 1 to set) for intr_in[31]
30	RAW_STATUS_30	W1S	0h	Raw Status (write 1 to set) for intr_in[30]
29	RAW_STATUS_29	W1S	0h	Raw Status (write 1 to set) for intr_in[29]
28	RAW_STATUS_28	W1S	0h	Raw Status (write 1 to set) for intr_in[28]
27	RAW_STATUS_27	W1S	0h	Raw Status (write 1 to set) for intr_in[27]
26	RAW_STATUS_26	W1S	0h	Raw Status (write 1 to set) for intr_in[26]
25	RAW_STATUS_25	W1S	0h	Raw Status (write 1 to set) for intr_in[25]
24	RAW_STATUS_24	W1S	0h	Raw Status (write 1 to set) for intr_in[24]
23	RAW_STATUS_23	W1S	0h	Raw Status (write 1 to set) for intr_in[23]
22	RAW_STATUS_22	W1S	0h	Raw Status (write 1 to set) for intr_in[22]
21	RAW_STATUS_21	W1S	0h	Raw Status (write 1 to set) for intr_in[21]
20	RAW_STATUS_20	W1S	0h	Raw Status (write 1 to set) for intr_in[20]
19	RAW_STATUS_19	W1S	0h	Raw Status (write 1 to set) for intr_in[19]
18	RAW_STATUS_18	W1S	0h	Raw Status (write 1 to set) for intr_in[18]
17	RAW_STATUS_17	W1S	0h	Raw Status (write 1 to set) for intr_in[17]
16	RAW_STATUS_16	W1S	0h	Raw Status (write 1 to set) for intr_in[16]
15	RAW_STATUS_15	W1S	0h	Raw Status (write 1 to set) for intr_in[15]
14	RAW_STATUS_14	W1S	0h	Raw Status (write 1 to set) for intr_in[14]

Table 15-438. ICSS_INTC_RAW_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	RAW_STATUS_13	W1S	0h	Raw Status (write 1 to set) for intr_in[13]
12	RAW_STATUS_12	W1S	0h	Raw Status (write 1 to set) for intr_in[12]
11	RAW_STATUS_11	W1S	0h	Raw Status (write 1 to set) for intr_in[11]
10	RAW_STATUS_10	W1S	0h	Raw Status (write 1 to set) for intr_in[10]
9	RAW_STATUS_9	W1S	0h	Raw Status (write 1 to set) for intr_in[9]
8	RAW_STATUS_8	W1S	0h	Raw Status (write 1 to set) for intr_in[8]
7	RAW_STATUS_7	W1S	0h	Raw Status (write 1 to set) for intr_in[7]
6	RAW_STATUS_6	W1S	0h	Raw Status (write 1 to set) for intr_in[6]
5	RAW_STATUS_5	W1S	0h	Raw Status (write 1 to set) for intr_in[5]
4	RAW_STATUS_4	W1S	0h	Raw Status (write 1 to set) for intr_in[4]
3	RAW_STATUS_3	W1S	0h	Raw Status (write 1 to set) for intr_in[3]
2	RAW_STATUS_2	W1S	0h	Raw Status (write 1 to set) for intr_in[2]
1	RAW_STATUS_1	W1S	0h	Raw Status (write 1 to set) for intr_in[1]
0	RAW_STATUS_0	W1S	0h	Raw Status (write 1 to set) for intr_in[0]

Table 15-439. Register Call Summary for ICSS_INTC_RAW_STATUS_REG0

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_RAW_STATUS_REG0 Register \(Offset = 200h\) \[reset = 0h\]: \[0\]](#)

15.7.13 ICSS_INTC_RAW_STATUS_REG1 Register (Offset = 204h) [reset = 0h]

ICSS_INTC_RAW_STATUS_REG1 is shown in Figure 15-143 and described in Table 15-441.

Return to [Summary Table](#).

Raw Status Register 1

Table 15-440. ICSS_INTC_RAW_STATUS_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0204h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0204h

Figure 15-143. ICSS_INTC_RAW_STATUS_REG1 Register

31	30	29	28	27	26	25	24
RAW_STATUS_63	RAW_STATUS_62	RAW_STATUS_61	RAW_STATUS_60	RAW_STATUS_59	RAW_STATUS_58	RAW_STATUS_57	RAW_STATUS_56
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
23	22	21	20	19	18	17	16
RAW_STATUS_55	RAW_STATUS_54	RAW_STATUS_53	RAW_STATUS_52	RAW_STATUS_51	RAW_STATUS_50	RAW_STATUS_49	RAW_STATUS_48
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
15	14	13	12	11	10	9	8
RAW_STATUS_47	RAW_STATUS_46	RAW_STATUS_45	RAW_STATUS_44	RAW_STATUS_43	RAW_STATUS_42	RAW_STATUS_41	RAW_STATUS_40
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
7	6	5	4	3	2	1	0
RAW_STATUS_39	RAW_STATUS_38	RAW_STATUS_37	RAW_STATUS_36	RAW_STATUS_35	RAW_STATUS_34	RAW_STATUS_33	RAW_STATUS_32
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h

LEGEND: W1S = Write 1 to Set Bit; -n = value after reset

Table 15-441. ICSS_INTC_RAW_STATUS_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RAW_STATUS_63	W1S	0h	Raw Status (write 1 to set) for intr_in[63]
30	RAW_STATUS_62	W1S	0h	Raw Status (write 1 to set) for intr_in[62]
29	RAW_STATUS_61	W1S	0h	Raw Status (write 1 to set) for intr_in[61]
28	RAW_STATUS_60	W1S	0h	Raw Status (write 1 to set) for intr_in[60]
27	RAW_STATUS_59	W1S	0h	Raw Status (write 1 to set) for intr_in[59]
26	RAW_STATUS_58	W1S	0h	Raw Status (write 1 to set) for intr_in[58]
25	RAW_STATUS_57	W1S	0h	Raw Status (write 1 to set) for intr_in[57]
24	RAW_STATUS_56	W1S	0h	Raw Status (write 1 to set) for intr_in[56]
23	RAW_STATUS_55	W1S	0h	Raw Status (write 1 to set) for intr_in[55]
22	RAW_STATUS_54	W1S	0h	Raw Status (write 1 to set) for intr_in[54]
21	RAW_STATUS_53	W1S	0h	Raw Status (write 1 to set) for intr_in[53]
20	RAW_STATUS_52	W1S	0h	Raw Status (write 1 to set) for intr_in[52]
19	RAW_STATUS_51	W1S	0h	Raw Status (write 1 to set) for intr_in[51]
18	RAW_STATUS_50	W1S	0h	Raw Status (write 1 to set) for intr_in[50]
17	RAW_STATUS_49	W1S	0h	Raw Status (write 1 to set) for intr_in[49]
16	RAW_STATUS_48	W1S	0h	Raw Status (write 1 to set) for intr_in[48]
15	RAW_STATUS_47	W1S	0h	Raw Status (write 1 to set) for intr_in[47]
14	RAW_STATUS_46	W1S	0h	Raw Status (write 1 to set) for intr_in[46]

Table 15-441. ICSS_INTC_RAW_STATUS_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	RAW_STATUS_45	W1S	0h	Raw Status (write 1 to set) for intr_in[45]
12	RAW_STATUS_44	W1S	0h	Raw Status (write 1 to set) for intr_in[44]
11	RAW_STATUS_43	W1S	0h	Raw Status (write 1 to set) for intr_in[43]
10	RAW_STATUS_42	W1S	0h	Raw Status (write 1 to set) for intr_in[42]
9	RAW_STATUS_41	W1S	0h	Raw Status (write 1 to set) for intr_in[41]
8	RAW_STATUS_40	W1S	0h	Raw Status (write 1 to set) for intr_in[40]
7	RAW_STATUS_39	W1S	0h	Raw Status (write 1 to set) for intr_in[39]
6	RAW_STATUS_38	W1S	0h	Raw Status (write 1 to set) for intr_in[38]
5	RAW_STATUS_37	W1S	0h	Raw Status (write 1 to set) for intr_in[37]
4	RAW_STATUS_36	W1S	0h	Raw Status (write 1 to set) for intr_in[36]
3	RAW_STATUS_35	W1S	0h	Raw Status (write 1 to set) for intr_in[35]
2	RAW_STATUS_34	W1S	0h	Raw Status (write 1 to set) for intr_in[34]
1	RAW_STATUS_33	W1S	0h	Raw Status (write 1 to set) for intr_in[33]
0	RAW_STATUS_32	W1S	0h	Raw Status (write 1 to set) for intr_in[32]

Table 15-442. Register Call Summary for ICSS_INTC_RAW_STATUS_REG1

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_RAW_STATUS_REG1 Register \(Offset = 204h\) \[reset = 0h\]: \[0\]](#)

15.7.14 ICSS_INTC_RAW_STATUS_REG2 Register (Offset = 208h) [reset = 0h]

ICSS_INTC_RAW_STATUS_REG2 is shown in Figure 15-144 and described in Table 15-444.

Return to [Summary Table](#).

Raw Status Register 2

Table 15-443. ICSS_INTC_RAW_STATUS_REG2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0208h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0208h

Figure 15-144. ICSS_INTC_RAW_STATUS_REG2 Register

31	30	29	28	27	26	25	24
RAW_STATUS_95	RAW_STATUS_94	RAW_STATUS_93	RAW_STATUS_92	RAW_STATUS_91	RAW_STATUS_90	RAW_STATUS_89	RAW_STATUS_88
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
23	22	21	20	19	18	17	16
RAW_STATUS_87	RAW_STATUS_86	RAW_STATUS_85	RAW_STATUS_84	RAW_STATUS_83	RAW_STATUS_82	RAW_STATUS_81	RAW_STATUS_80
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
15	14	13	12	11	10	9	8
RAW_STATUS_79	RAW_STATUS_78	RAW_STATUS_77	RAW_STATUS_76	RAW_STATUS_75	RAW_STATUS_74	RAW_STATUS_73	RAW_STATUS_72
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
7	6	5	4	3	2	1	0
RAW_STATUS_71	RAW_STATUS_70	RAW_STATUS_69	RAW_STATUS_68	RAW_STATUS_67	RAW_STATUS_66	RAW_STATUS_65	RAW_STATUS_64
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h

LEGEND: W1S = Write 1 to Set Bit; -n = value after reset

Table 15-444. ICSS_INTC_RAW_STATUS_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RAW_STATUS_95	W1S	0h	Raw Status (write 1 to set) for slv_events_in[31]
30	RAW_STATUS_94	W1S	0h	Raw Status (write 1 to set) for slv_events_in[30]
29	RAW_STATUS_93	W1S	0h	Raw Status (write 1 to set) for slv_events_in[29]
28	RAW_STATUS_92	W1S	0h	Raw Status (write 1 to set) for slv_events_in[28]
27	RAW_STATUS_91	W1S	0h	Raw Status (write 1 to set) for slv_events_in[27]
26	RAW_STATUS_90	W1S	0h	Raw Status (write 1 to set) for slv_events_in[26]
25	RAW_STATUS_89	W1S	0h	Raw Status (write 1 to set) for slv_events_in[25]
24	RAW_STATUS_88	W1S	0h	Raw Status (write 1 to set) for slv_events_in[24]
23	RAW_STATUS_87	W1S	0h	Raw Status (write 1 to set) for slv_events_in[23]
22	RAW_STATUS_86	W1S	0h	Raw Status (write 1 to set) for slv_events_in[22]
21	RAW_STATUS_85	W1S	0h	Raw Status (write 1 to set) for slv_events_in[21]
20	RAW_STATUS_84	W1S	0h	Raw Status (write 1 to set) for slv_events_in[20]
19	RAW_STATUS_83	W1S	0h	Raw Status (write 1 to set) for slv_events_in[19]
18	RAW_STATUS_82	W1S	0h	Raw Status (write 1 to set) for slv_events_in[18]
17	RAW_STATUS_81	W1S	0h	Raw Status (write 1 to set) for slv_events_in[17]
16	RAW_STATUS_80	W1S	0h	Raw Status (write 1 to set) for slv_events_in[16]
15	RAW_STATUS_79	W1S	0h	Raw Status (write 1 to set) for slv_events_in[15]
14	RAW_STATUS_78	W1S	0h	Raw Status (write 1 to set) for slv_events_in[14]

Table 15-444. ICSS_INTC_RAW_STATUS_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	RAW_STATUS_77	W1S	0h	Raw Status (write 1 to set) for slv_events_in[13]
12	RAW_STATUS_76	W1S	0h	Raw Status (write 1 to set) for slv_events_in[12]
11	RAW_STATUS_75	W1S	0h	Raw Status (write 1 to set) for slv_events_in[11]
10	RAW_STATUS_74	W1S	0h	Raw Status (write 1 to set) for slv_events_in[10]
9	RAW_STATUS_73	W1S	0h	Raw Status (write 1 to set) for slv_events_in[9]
8	RAW_STATUS_72	W1S	0h	Raw Status (write 1 to set) for slv_events_in[8]
7	RAW_STATUS_71	W1S	0h	Raw Status (write 1 to set) for slv_events_in[7]
6	RAW_STATUS_70	W1S	0h	Raw Status (write 1 to set) for slv_events_in[6]
5	RAW_STATUS_69	W1S	0h	Raw Status (write 1 to set) for slv_events_in[5]
4	RAW_STATUS_68	W1S	0h	Raw Status (write 1 to set) for slv_events_in[4]
3	RAW_STATUS_67	W1S	0h	Raw Status (write 1 to set) for slv_events_in[3]
2	RAW_STATUS_66	W1S	0h	Raw Status (write 1 to set) for slv_events_in[2]
1	RAW_STATUS_65	W1S	0h	Raw Status (write 1 to set) for slv_events_in[1]
0	RAW_STATUS_64	W1S	0h	Raw Status (write 1 to set) for slv_events_in[0]

Table 15-445. Register Call Summary for ICSS_INTC_RAW_STATUS_REG2

PRU_ICSS_INTC_INTC Registers

- [ICSS_INTC_RAW_STATUS_REG2 Register \(Offset = 208h\) \[reset = 0h\]: \[0\]](#)
- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)

15.7.15 ICSS_INTC_RAW_STATUS_REG3 Register (Offset = 20Ch) [reset = 0h]

ICSS_INTC_RAW_STATUS_REG3 is shown in [Figure 15-145](#) and described in [Table 15-447](#).

Return to [Summary Table](#).

Raw Status Register 3

Table 15-446. ICSS_INTC_RAW_STATUS_REG3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTCLV	0B02 020Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTCLV	0B12 020Ch

Figure 15-145. ICSS_INTC_RAW_STATUS_REG3 Register

31	30	29	28	27	26	25	24
RAW_STATUS_ 127	RAW_STATUS_ 126	RAW_STATUS_ 125	RAW_STATUS_ 124	RAW_STATUS_ 123	RAW_STATUS_ 122	RAW_STATUS_ 121	RAW_STATUS_ 120
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
23	22	21	20	19	18	17	16
RAW_STATUS_ 119	RAW_STATUS_ 118	RAW_STATUS_ 117	RAW_STATUS_ 116	RAW_STATUS_ 115	RAW_STATUS_ 114	RAW_STATUS_ 113	RAW_STATUS_ 112
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
15	14	13	12	11	10	9	8
RAW_STATUS_ 111	RAW_STATUS_ 110	RAW_STATUS_ 109	RAW_STATUS_ 108	RAW_STATUS_ 107	RAW_STATUS_ 106	RAW_STATUS_ 105	RAW_STATUS_ 104
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
7	6	5	4	3	2	1	0
RAW_STATUS_ 103	RAW_STATUS_ 102	RAW_STATUS_ 101	RAW_STATUS_ 100	RAW_STATUS_ 99	RAW_STATUS_ 98	RAW_STATUS_ 97	RAW_STATUS_ 96
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h

LEGEND: W1S = Write 1 to Set Bit; -n = value after reset

Table 15-447. ICSS_INTC_RAW_STATUS_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RAW_STATUS_127	W1S	0h	Raw Status (write 1 to set) for slv_events_in[63]
30	RAW_STATUS_126	W1S	0h	Raw Status (write 1 to set) for slv_events_in[62]
29	RAW_STATUS_125	W1S	0h	Raw Status (write 1 to set) for slv_events_in[61]
28	RAW_STATUS_124	W1S	0h	Raw Status (write 1 to set) for slv_events_in[60]
27	RAW_STATUS_123	W1S	0h	Raw Status (write 1 to set) for slv_events_in[59]
26	RAW_STATUS_122	W1S	0h	Raw Status (write 1 to set) for slv_events_in[58]
25	RAW_STATUS_121	W1S	0h	Raw Status (write 1 to set) for slv_events_in[57]
24	RAW_STATUS_120	W1S	0h	Raw Status (write 1 to set) for slv_events_in[56]
23	RAW_STATUS_119	W1S	0h	Raw Status (write 1 to set) for slv_events_in[55]
22	RAW_STATUS_118	W1S	0h	Raw Status (write 1 to set) for slv_events_in[54]
21	RAW_STATUS_117	W1S	0h	Raw Status (write 1 to set) for slv_events_in[53]
20	RAW_STATUS_116	W1S	0h	Raw Status (write 1 to set) for slv_events_in[52]
19	RAW_STATUS_115	W1S	0h	Raw Status (write 1 to set) for slv_events_in[51]
18	RAW_STATUS_114	W1S	0h	Raw Status (write 1 to set) for slv_events_in[50]
17	RAW_STATUS_113	W1S	0h	Raw Status (write 1 to set) for slv_events_in[49]
16	RAW_STATUS_112	W1S	0h	Raw Status (write 1 to set) for slv_events_in[48]
15	RAW_STATUS_111	W1S	0h	Raw Status (write 1 to set) for slv_events_in[47]
14	RAW_STATUS_110	W1S	0h	Raw Status (write 1 to set) for slv_events_in[46]

Table 15-447. ICSS_INTC_RAW_STATUS_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	RAW_STATUS_109	W1S	0h	Raw Status (write 1 to set) for slv_events_in[45]
12	RAW_STATUS_108	W1S	0h	Raw Status (write 1 to set) for slv_events_in[44]
11	RAW_STATUS_107	W1S	0h	Raw Status (write 1 to set) for slv_events_in[43]
10	RAW_STATUS_106	W1S	0h	Raw Status (write 1 to set) for slv_events_in[42]
9	RAW_STATUS_105	W1S	0h	Raw Status (write 1 to set) for slv_events_in[41]
8	RAW_STATUS_104	W1S	0h	Raw Status (write 1 to set) for slv_events_in[40]
7	RAW_STATUS_103	W1S	0h	Raw Status (write 1 to set) for slv_events_in[39]
6	RAW_STATUS_102	W1S	0h	Raw Status (write 1 to set) for slv_events_in[38]
5	RAW_STATUS_101	W1S	0h	Raw Status (write 1 to set) for slv_events_in[37]
4	RAW_STATUS_100	W1S	0h	Raw Status (write 1 to set) for slv_events_in[36]
3	RAW_STATUS_99	W1S	0h	Raw Status (write 1 to set) for slv_events_in[35]
2	RAW_STATUS_98	W1S	0h	Raw Status (write 1 to set) for slv_events_in[34]
1	RAW_STATUS_97	W1S	0h	Raw Status (write 1 to set) for slv_events_in[33]
0	RAW_STATUS_96	W1S	0h	Raw Status (write 1 to set) for slv_events_in[32]

Table 15-448. Register Call Summary for ICSS_INTC_RAW_STATUS_REG3

PRU_ICSS_INTC_INTC Registers

- [ICSS_INTC_RAW_STATUS_REG3 Register \(Offset = 20Ch\) \[reset = 0h\]: \[0\]](#)
- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)

15.7.16 ICSS_INTC_RAW_STATUS_REG4 Register (Offset = 210h) [reset = 0h]

ICSS_INTC_RAW_STATUS_REG4 is shown in Figure 15-146 and described in Table 15-450.

Return to [Summary Table](#).

Raw Status Register 4

Table 15-449. ICSS_INTC_RAW_STATUS_REG4 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0210h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0210h

Figure 15-146. ICSS_INTC_RAW_STATUS_REG4 Register

31	30	29	28	27	26	25	24
RAW_STATUS_ 159	RAW_STATUS_ 158	RAW_STATUS_ 157	RAW_STATUS_ 156	RAW_STATUS_ 155	RAW_STATUS_ 154	RAW_STATUS_ 153	RAW_STATUS_ 152
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
23	22	21	20	19	18	17	16
RAW_STATUS_ 151	RAW_STATUS_ 150	RAW_STATUS_ 149	RAW_STATUS_ 148	RAW_STATUS_ 147	RAW_STATUS_ 146	RAW_STATUS_ 145	RAW_STATUS_ 144
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
15	14	13	12	11	10	9	8
RAW_STATUS_ 143	RAW_STATUS_ 142	RAW_STATUS_ 141	RAW_STATUS_ 140	RAW_STATUS_ 139	RAW_STATUS_ 138	RAW_STATUS_ 137	RAW_STATUS_ 136
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
7	6	5	4	3	2	1	0
RAW_STATUS_ 135	RAW_STATUS_ 134	RAW_STATUS_ 133	RAW_STATUS_ 132	RAW_STATUS_ 131	RAW_STATUS_ 130	RAW_STATUS_ 129	RAW_STATUS_ 128
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h

LEGEND: W1S = Write 1 to Set Bit; -n = value after reset

Table 15-450. ICSS_INTC_RAW_STATUS_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RAW_STATUS_159	W1S	0h	Raw Status (write 1 to set) for slv_events_in[95]
30	RAW_STATUS_158	W1S	0h	Raw Status (write 1 to set) for slv_events_in[94]
29	RAW_STATUS_157	W1S	0h	Raw Status (write 1 to set) for slv_events_in[93]
28	RAW_STATUS_156	W1S	0h	Raw Status (write 1 to set) for slv_events_in[92]
27	RAW_STATUS_155	W1S	0h	Raw Status (write 1 to set) for slv_events_in[91]
26	RAW_STATUS_154	W1S	0h	Raw Status (write 1 to set) for slv_events_in[90]
25	RAW_STATUS_153	W1S	0h	Raw Status (write 1 to set) for slv_events_in[89]
24	RAW_STATUS_152	W1S	0h	Raw Status (write 1 to set) for slv_events_in[88]
23	RAW_STATUS_151	W1S	0h	Raw Status (write 1 to set) for slv_events_in[87]
22	RAW_STATUS_150	W1S	0h	Raw Status (write 1 to set) for slv_events_in[86]
21	RAW_STATUS_149	W1S	0h	Raw Status (write 1 to set) for slv_events_in[85]
20	RAW_STATUS_148	W1S	0h	Raw Status (write 1 to set) for slv_events_in[84]
19	RAW_STATUS_147	W1S	0h	Raw Status (write 1 to set) for slv_events_in[83]
18	RAW_STATUS_146	W1S	0h	Raw Status (write 1 to set) for slv_events_in[82]
17	RAW_STATUS_145	W1S	0h	Raw Status (write 1 to set) for slv_events_in[81]
16	RAW_STATUS_144	W1S	0h	Raw Status (write 1 to set) for slv_events_in[80]
15	RAW_STATUS_143	W1S	0h	Raw Status (write 1 to set) for slv_events_in[79]
14	RAW_STATUS_142	W1S	0h	Raw Status (write 1 to set) for slv_events_in[78]

Table 15-450. ICSS_INTC_RAW_STATUS_REG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	RAW_STATUS_141	W1S	0h	Raw Status (write 1 to set) for slv_events_in[77]
12	RAW_STATUS_140	W1S	0h	Raw Status (write 1 to set) for slv_events_in[76]
11	RAW_STATUS_139	W1S	0h	Raw Status (write 1 to set) for slv_events_in[75]
10	RAW_STATUS_138	W1S	0h	Raw Status (write 1 to set) for slv_events_in[74]
9	RAW_STATUS_137	W1S	0h	Raw Status (write 1 to set) for slv_events_in[73]
8	RAW_STATUS_136	W1S	0h	Raw Status (write 1 to set) for slv_events_in[72]
7	RAW_STATUS_135	W1S	0h	Raw Status (write 1 to set) for slv_events_in[71]
6	RAW_STATUS_134	W1S	0h	Raw Status (write 1 to set) for slv_events_in[70]
5	RAW_STATUS_133	W1S	0h	Raw Status (write 1 to set) for slv_events_in[69]
4	RAW_STATUS_132	W1S	0h	Raw Status (write 1 to set) for slv_events_in[68]
3	RAW_STATUS_131	W1S	0h	Raw Status (write 1 to set) for slv_events_in[67]
2	RAW_STATUS_130	W1S	0h	Raw Status (write 1 to set) for slv_events_in[66]
1	RAW_STATUS_129	W1S	0h	Raw Status (write 1 to set) for slv_events_in[65]
0	RAW_STATUS_128	W1S	0h	Raw Status (write 1 to set) for slv_events_in[64]

Table 15-451. Register Call Summary for ICSS_INTC_RAW_STATUS_REG4

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_RAW_STATUS_REG4 Register \(Offset = 210h\) \[reset = 0h\]: \[0\]](#)

15.7.17 ICSS_INTC_ENA_STATUS_REG0 Register (Offset = 280h) [reset = 0h]

ICSS_INTC_ENA_STATUS_REG0 is shown in [Figure 15-147](#) and described in [Table 15-453](#).

Return to [Summary Table](#).

Enabled Status Register 0

Table 15-452. ICSS_INTC_ENA_STATUS_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0280h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0280h

Figure 15-147. ICSS_INTC_ENA_STATUS_REG0 Register

31	30	29	28	27	26	25	24
ENA_STATUS_ 31	ENA_STATUS_ 30	ENA_STATUS_ 29	ENA_STATUS_ 28	ENA_STATUS_ 27	ENA_STATUS_ 26	ENA_STATUS_ 25	ENA_STATUS_ 24
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
23	22	21	20	19	18	17	16
ENA_STATUS_ 23	ENA_STATUS_ 22	ENA_STATUS_ 21	ENA_STATUS_ 20	ENA_STATUS_ 19	ENA_STATUS_ 18	ENA_STATUS_ 17	ENA_STATUS_ 16
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
15	14	13	12	11	10	9	8
ENA_STATUS_ 15	ENA_STATUS_ 14	ENA_STATUS_ 13	ENA_STATUS_ 12	ENA_STATUS_ 11	ENA_STATUS_ 10	ENA_STATUS_ 9	ENA_STATUS_ 8
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
7	6	5	4	3	2	1	0
ENA_STATUS_ 7	ENA_STATUS_ 6	ENA_STATUS_ 5	ENA_STATUS_ 4	ENA_STATUS_ 3	ENA_STATUS_ 2	ENA_STATUS_ 1	ENA_STATUS_ 0
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h

LEGEND: W1C = Write 1 to Clear Bit; -n = value after reset

Table 15-453. ICSS_INTC_ENA_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENA_STATUS_31	W1C	0h	Enabled Status for intr_in[31]
30	ENA_STATUS_30	W1C	0h	Enabled Status for intr_in[30]
29	ENA_STATUS_29	W1C	0h	Enabled Status for intr_in[29]
28	ENA_STATUS_28	W1C	0h	Enabled Status for intr_in[28]
27	ENA_STATUS_27	W1C	0h	Enabled Status for intr_in[27]
26	ENA_STATUS_26	W1C	0h	Enabled Status for intr_in[26]
25	ENA_STATUS_25	W1C	0h	Enabled Status for intr_in[25]
24	ENA_STATUS_24	W1C	0h	Enabled Status for intr_in[24]
23	ENA_STATUS_23	W1C	0h	Enabled Status for intr_in[23]
22	ENA_STATUS_22	W1C	0h	Enabled Status for intr_in[22]
21	ENA_STATUS_21	W1C	0h	Enabled Status for intr_in[21]
20	ENA_STATUS_20	W1C	0h	Enabled Status for intr_in[20]
19	ENA_STATUS_19	W1C	0h	Enabled Status for intr_in[19]
18	ENA_STATUS_18	W1C	0h	Enabled Status for intr_in[18]
17	ENA_STATUS_17	W1C	0h	Enabled Status for intr_in[17]
16	ENA_STATUS_16	W1C	0h	Enabled Status for intr_in[16]
15	ENA_STATUS_15	W1C	0h	Enabled Status for intr_in[15]
14	ENA_STATUS_14	W1C	0h	Enabled Status for intr_in[14]

Table 15-453. ICSS_INTC_ENA_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	ENA_STATUS_13	W1C	0h	Enabled Status for intr_in[13]
12	ENA_STATUS_12	W1C	0h	Enabled Status for intr_in[12]
11	ENA_STATUS_11	W1C	0h	Enabled Status for intr_in[11]
10	ENA_STATUS_10	W1C	0h	Enabled Status for intr_in[10]
9	ENA_STATUS_9	W1C	0h	Enabled Status for intr_in[9]
8	ENA_STATUS_8	W1C	0h	Enabled Status for intr_in[8]
7	ENA_STATUS_7	W1C	0h	Enabled Status for intr_in[7]
6	ENA_STATUS_6	W1C	0h	Enabled Status for intr_in[6]
5	ENA_STATUS_5	W1C	0h	Enabled Status for intr_in[5]
4	ENA_STATUS_4	W1C	0h	Enabled Status for intr_in[4]
3	ENA_STATUS_3	W1C	0h	Enabled Status for intr_in[3]
2	ENA_STATUS_2	W1C	0h	Enabled Status for intr_in[2]
1	ENA_STATUS_1	W1C	0h	Enabled Status for intr_in[1]
0	ENA_STATUS_0	W1C	0h	Enabled Status for intr_in[0]

Table 15-454. Register Call Summary for ICSS_INTC_ENA_STATUS_REG0

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_ENA_STATUS_REG0 Register \(Offset = 280h\) \[reset = 0h\]: \[0\]](#)

15.7.18 ICSS_INTC_ENA_STATUS_REG1 Register (Offset = 284h) [reset = 0h]

ICSS_INTC_ENA_STATUS_REG1 is shown in Figure 15-148 and described in Table 15-456.

Return to [Summary Table](#).

Enabled Status Register 1

Table 15-455. ICSS_INTC_ENA_STATUS_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0284h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0284h

Figure 15-148. ICSS_INTC_ENA_STATUS_REG1 Register

31	30	29	28	27	26	25	24
ENA_STATUS_ 63	ENA_STATUS_ 62	ENA_STATUS_ 61	ENA_STATUS_ 60	ENA_STATUS_ 59	ENA_STATUS_ 58	ENA_STATUS_ 57	ENA_STATUS_ 56
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
23	22	21	20	19	18	17	16
ENA_STATUS_ 55	ENA_STATUS_ 54	ENA_STATUS_ 53	ENA_STATUS_ 52	ENA_STATUS_ 51	ENA_STATUS_ 50	ENA_STATUS_ 49	ENA_STATUS_ 48
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
15	14	13	12	11	10	9	8
ENA_STATUS_ 47	ENA_STATUS_ 46	ENA_STATUS_ 45	ENA_STATUS_ 44	ENA_STATUS_ 43	ENA_STATUS_ 42	ENA_STATUS_ 41	ENA_STATUS_ 40
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
7	6	5	4	3	2	1	0
ENA_STATUS_ 39	ENA_STATUS_ 38	ENA_STATUS_ 37	ENA_STATUS_ 36	ENA_STATUS_ 35	ENA_STATUS_ 34	ENA_STATUS_ 33	ENA_STATUS_ 32
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h

LEGEND: W1C = Write 1 to Clear Bit; -n = value after reset

Table 15-456. ICSS_INTC_ENA_STATUS_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENA_STATUS_63	W1C	0h	Enabled Status for intr_in[63]
30	ENA_STATUS_62	W1C	0h	Enabled Status for intr_in[62]
29	ENA_STATUS_61	W1C	0h	Enabled Status for intr_in[61]
28	ENA_STATUS_60	W1C	0h	Enabled Status for intr_in[60]
27	ENA_STATUS_59	W1C	0h	Enabled Status for intr_in[59]
26	ENA_STATUS_58	W1C	0h	Enabled Status for intr_in[58]
25	ENA_STATUS_57	W1C	0h	Enabled Status for intr_in[57]
24	ENA_STATUS_56	W1C	0h	Enabled Status for intr_in[56]
23	ENA_STATUS_55	W1C	0h	Enabled Status for intr_in[55]
22	ENA_STATUS_54	W1C	0h	Enabled Status for intr_in[54]
21	ENA_STATUS_53	W1C	0h	Enabled Status for intr_in[53]
20	ENA_STATUS_52	W1C	0h	Enabled Status for intr_in[52]
19	ENA_STATUS_51	W1C	0h	Enabled Status for intr_in[51]
18	ENA_STATUS_50	W1C	0h	Enabled Status for intr_in[50]
17	ENA_STATUS_49	W1C	0h	Enabled Status for intr_in[49]
16	ENA_STATUS_48	W1C	0h	Enabled Status for intr_in[48]
15	ENA_STATUS_47	W1C	0h	Enabled Status for intr_in[47]
14	ENA_STATUS_46	W1C	0h	Enabled Status for intr_in[46]

Table 15-456. ICSS_INTC_ENA_STATUS_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	ENA_STATUS_45	W1C	0h	Enabled Status for intr_in[45]
12	ENA_STATUS_44	W1C	0h	Enabled Status for intr_in[44]
11	ENA_STATUS_43	W1C	0h	Enabled Status for intr_in[43]
10	ENA_STATUS_42	W1C	0h	Enabled Status for intr_in[42]
9	ENA_STATUS_41	W1C	0h	Enabled Status for intr_in[41]
8	ENA_STATUS_40	W1C	0h	Enabled Status for intr_in[40]
7	ENA_STATUS_39	W1C	0h	Enabled Status for intr_in[39]
6	ENA_STATUS_38	W1C	0h	Enabled Status for intr_in[38]
5	ENA_STATUS_37	W1C	0h	Enabled Status for intr_in[37]
4	ENA_STATUS_36	W1C	0h	Enabled Status for intr_in[36]
3	ENA_STATUS_35	W1C	0h	Enabled Status for intr_in[35]
2	ENA_STATUS_34	W1C	0h	Enabled Status for intr_in[34]
1	ENA_STATUS_33	W1C	0h	Enabled Status for intr_in[33]
0	ENA_STATUS_32	W1C	0h	Enabled Status for intr_in[32]

Table 15-457. Register Call Summary for ICSS_INTC_ENA_STATUS_REG1

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_ENA_STATUS_REG1 Register \(Offset = 284h\) \[reset = 0h\]: \[0\]](#)

15.7.19 ICSS_INTC_ENA_STATUS_REG2 Register (Offset = 288h) [reset = 0h]

ICSS_INTC_ENA_STATUS_REG2 is shown in [Figure 15-149](#) and described in [Table 15-459](#).

Return to [Summary Table](#).

Enabled Status Register 2

Table 15-458. ICSS_INTC_ENA_STATUS_REG2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTCLV	0B02 0288h
PRU_ICSSG1_PR1_ICSS_INTC_INTCLV	0B12 0288h

Figure 15-149. ICSS_INTC_ENA_STATUS_REG2 Register

31	30	29	28	27	26	25	24
ENA_STATUS_95	ENA_STATUS_94	ENA_STATUS_93	ENA_STATUS_92	ENA_STATUS_91	ENA_STATUS_90	ENA_STATUS_89	ENA_STATUS_88
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
23	22	21	20	19	18	17	16
ENA_STATUS_87	ENA_STATUS_86	ENA_STATUS_85	ENA_STATUS_84	ENA_STATUS_83	ENA_STATUS_82	ENA_STATUS_81	ENA_STATUS_80
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
15	14	13	12	11	10	9	8
ENA_STATUS_79	ENA_STATUS_78	ENA_STATUS_77	ENA_STATUS_76	ENA_STATUS_75	ENA_STATUS_74	ENA_STATUS_73	ENA_STATUS_72
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
7	6	5	4	3	2	1	0
ENA_STATUS_71	ENA_STATUS_70	ENA_STATUS_69	ENA_STATUS_68	ENA_STATUS_67	ENA_STATUS_66	ENA_STATUS_65	ENA_STATUS_64
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h

LEGEND: W1C = Write 1 to Clear Bit; -n = value after reset

Table 15-459. ICSS_INTC_ENA_STATUS_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENA_STATUS_95	W1C	0h	Enabled Status for slv_events_in[31]
30	ENA_STATUS_94	W1C	0h	Enabled Status for slv_events_in[30]
29	ENA_STATUS_93	W1C	0h	Enabled Status for slv_events_in[29]
28	ENA_STATUS_92	W1C	0h	Enabled Status for slv_events_in[28]
27	ENA_STATUS_91	W1C	0h	Enabled Status for slv_events_in[27]
26	ENA_STATUS_90	W1C	0h	Enabled Status for slv_events_in[26]
25	ENA_STATUS_89	W1C	0h	Enabled Status for slv_events_in[25]
24	ENA_STATUS_88	W1C	0h	Enabled Status for slv_events_in[24]
23	ENA_STATUS_87	W1C	0h	Enabled Status for slv_events_in[23]
22	ENA_STATUS_86	W1C	0h	Enabled Status for slv_events_in[22]
21	ENA_STATUS_85	W1C	0h	Enabled Status for slv_events_in[21]
20	ENA_STATUS_84	W1C	0h	Enabled Status for slv_events_in[20]
19	ENA_STATUS_83	W1C	0h	Enabled Status for slv_events_in[19]
18	ENA_STATUS_82	W1C	0h	Enabled Status for slv_events_in[18]
17	ENA_STATUS_81	W1C	0h	Enabled Status for slv_events_in[17]
16	ENA_STATUS_80	W1C	0h	Enabled Status for slv_events_in[16]
15	ENA_STATUS_79	W1C	0h	Enabled Status for slv_events_in[15]
14	ENA_STATUS_78	W1C	0h	Enabled Status for slv_events_in[14]

Table 15-459. ICSS_INTC_ENA_STATUS_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	ENA_STATUS_77	W1C	0h	Enabled Status for slv_events_in[13]
12	ENA_STATUS_76	W1C	0h	Enabled Status for slv_events_in[12]
11	ENA_STATUS_75	W1C	0h	Enabled Status for slv_events_in[11]
10	ENA_STATUS_74	W1C	0h	Enabled Status for slv_events_in[10]
9	ENA_STATUS_73	W1C	0h	Enabled Status for slv_events_in[9]
8	ENA_STATUS_72	W1C	0h	Enabled Status for slv_events_in[8]
7	ENA_STATUS_71	W1C	0h	Enabled Status for slv_events_in[7]
6	ENA_STATUS_70	W1C	0h	Enabled Status for slv_events_in[6]
5	ENA_STATUS_69	W1C	0h	Enabled Status for slv_events_in[5]
4	ENA_STATUS_68	W1C	0h	Enabled Status for slv_events_in[4]
3	ENA_STATUS_67	W1C	0h	Enabled Status for slv_events_in[3]
2	ENA_STATUS_66	W1C	0h	Enabled Status for slv_events_in[2]
1	ENA_STATUS_65	W1C	0h	Enabled Status for slv_events_in[1]
0	ENA_STATUS_64	W1C	0h	Enabled Status for slv_events_in[0]

Table 15-460. Register Call Summary for ICSS_INTC_ENA_STATUS_REG2

PRU_ICSS_INTC_INTC Registers

- [ICSS_INTC_ENA_STATUS_REG2 Register \(Offset = 288h\) \[reset = 0h\]: \[0\]](#)
- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)

15.7.20 ICSS_INTC_ENA_STATUS_REG3 Register (Offset = 28Ch) [reset = 0h]

ICSS_INTC_ENA_STATUS_REG3 is shown in Figure 15-150 and described in Table 15-462.

Return to [Summary Table](#).

Enabled Status Register 3

Table 15-461. ICSS_INTC_ENA_STATUS_REG3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTCLV	0B02 028Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTCLV	0B12 028Ch

Figure 15-150. ICSS_INTC_ENA_STATUS_REG3 Register

31	30	29	28	27	26	25	24
ENA_STATUS_ 127	ENA_STATUS_ 126	ENA_STATUS_ 125	ENA_STATUS_ 124	ENA_STATUS_ 123	ENA_STATUS_ 122	ENA_STATUS_ 121	ENA_STATUS_ 120
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
23	22	21	20	19	18	17	16
ENA_STATUS_ 119	ENA_STATUS_ 118	ENA_STATUS_ 117	ENA_STATUS_ 116	ENA_STATUS_ 115	ENA_STATUS_ 114	ENA_STATUS_ 113	ENA_STATUS_ 112
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
15	14	13	12	11	10	9	8
ENA_STATUS_ 111	ENA_STATUS_ 110	ENA_STATUS_ 109	ENA_STATUS_ 108	ENA_STATUS_ 107	ENA_STATUS_ 106	ENA_STATUS_ 105	ENA_STATUS_ 104
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
7	6	5	4	3	2	1	0
ENA_STATUS_ 103	ENA_STATUS_ 102	ENA_STATUS_ 101	ENA_STATUS_ 100	ENA_STATUS_ 99	ENA_STATUS_ 98	ENA_STATUS_ 97	ENA_STATUS_ 96
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h

LEGEND: W1C = Write 1 to Clear Bit; -n = value after reset

Table 15-462. ICSS_INTC_ENA_STATUS_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENA_STATUS_127	W1C	0h	Enabled Status for slv_events_in[63]
30	ENA_STATUS_126	W1C	0h	Enabled Status for slv_events_in[62]
29	ENA_STATUS_125	W1C	0h	Enabled Status for slv_events_in[61]
28	ENA_STATUS_124	W1C	0h	Enabled Status for slv_events_in[60]
27	ENA_STATUS_123	W1C	0h	Enabled Status for slv_events_in[59]
26	ENA_STATUS_122	W1C	0h	Enabled Status for slv_events_in[58]
25	ENA_STATUS_121	W1C	0h	Enabled Status for slv_events_in[57]
24	ENA_STATUS_120	W1C	0h	Enabled Status for slv_events_in[56]
23	ENA_STATUS_119	W1C	0h	Enabled Status for slv_events_in[55]
22	ENA_STATUS_118	W1C	0h	Enabled Status for slv_events_in[54]
21	ENA_STATUS_117	W1C	0h	Enabled Status for slv_events_in[53]
20	ENA_STATUS_116	W1C	0h	Enabled Status for slv_events_in[52]
19	ENA_STATUS_115	W1C	0h	Enabled Status for slv_events_in[51]
18	ENA_STATUS_114	W1C	0h	Enabled Status for slv_events_in[50]
17	ENA_STATUS_113	W1C	0h	Enabled Status for slv_events_in[49]
16	ENA_STATUS_112	W1C	0h	Enabled Status for slv_events_in[48]
15	ENA_STATUS_111	W1C	0h	Enabled Status for slv_events_in[47]
14	ENA_STATUS_110	W1C	0h	Enabled Status for slv_events_in[46]

Table 15-462. ICSS_INTC_ENA_STATUS_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	ENA_STATUS_109	W1C	0h	Enabled Status for slv_events_in[45]
12	ENA_STATUS_108	W1C	0h	Enabled Status for slv_events_in[44]
11	ENA_STATUS_107	W1C	0h	Enabled Status for slv_events_in[43]
10	ENA_STATUS_106	W1C	0h	Enabled Status for slv_events_in[42]
9	ENA_STATUS_105	W1C	0h	Enabled Status for slv_events_in[41]
8	ENA_STATUS_104	W1C	0h	Enabled Status for slv_events_in[40]
7	ENA_STATUS_103	W1C	0h	Enabled Status for slv_events_in[39]
6	ENA_STATUS_102	W1C	0h	Enabled Status for slv_events_in[38]
5	ENA_STATUS_101	W1C	0h	Enabled Status for slv_events_in[37]
4	ENA_STATUS_100	W1C	0h	Enabled Status for slv_events_in[36]
3	ENA_STATUS_99	W1C	0h	Enabled Status for slv_events_in[35]
2	ENA_STATUS_98	W1C	0h	Enabled Status for slv_events_in[34]
1	ENA_STATUS_97	W1C	0h	Enabled Status for slv_events_in[33]
0	ENA_STATUS_96	W1C	0h	Enabled Status for slv_events_in[32]

Table 15-463. Register Call Summary for ICSS_INTC_ENA_STATUS_REG3

PRU_ICSS_INTC_INTC Registers

- [ICSS_INTC_ENA_STATUS_REG3 Register \(Offset = 28Ch\) \[reset = 0h\]: \[0\]](#)
- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)

15.7.21 ICSS_INTC_ENA_STATUS_REG4 Register (Offset = 290h) [reset = 0h]

ICSS_INTC_ENA_STATUS_REG4 is shown in Figure 15-151 and described in Table 15-465.

Return to [Summary Table](#).

Enabled Status Register 4

Table 15-464. ICSS_INTC_ENA_STATUS_REG4 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTCLV	0B02 0290h
PRU_ICSSG1_PR1_ICSS_INTC_INTCLV	0B12 0290h

Figure 15-151. ICSS_INTC_ENA_STATUS_REG4 Register

31	30	29	28	27	26	25	24
ENA_STATUS_159	ENA_STATUS_158	ENA_STATUS_157	ENA_STATUS_156	ENA_STATUS_155	ENA_STATUS_154	ENA_STATUS_153	ENA_STATUS_152
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
23	22	21	20	19	18	17	16
ENA_STATUS_151	ENA_STATUS_150	ENA_STATUS_149	ENA_STATUS_148	ENA_STATUS_147	ENA_STATUS_146	ENA_STATUS_145	ENA_STATUS_144
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
15	14	13	12	11	10	9	8
ENA_STATUS_143	ENA_STATUS_142	ENA_STATUS_141	ENA_STATUS_140	ENA_STATUS_139	ENA_STATUS_138	ENA_STATUS_137	ENA_STATUS_136
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
7	6	5	4	3	2	1	0
ENA_STATUS_135	ENA_STATUS_134	ENA_STATUS_133	ENA_STATUS_132	ENA_STATUS_131	ENA_STATUS_130	ENA_STATUS_129	ENA_STATUS_128
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h

LEGEND: W1C = Write 1 to Clear Bit; -n = value after reset

Table 15-465. ICSS_INTC_ENA_STATUS_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENA_STATUS_159	W1C	0h	Enabled Status for slv_events_in[95]
30	ENA_STATUS_158	W1C	0h	Enabled Status for slv_events_in[94]
29	ENA_STATUS_157	W1C	0h	Enabled Status for slv_events_in[93]
28	ENA_STATUS_156	W1C	0h	Enabled Status for slv_events_in[92]
27	ENA_STATUS_155	W1C	0h	Enabled Status for slv_events_in[91]
26	ENA_STATUS_154	W1C	0h	Enabled Status for slv_events_in[90]
25	ENA_STATUS_153	W1C	0h	Enabled Status for slv_events_in[89]
24	ENA_STATUS_152	W1C	0h	Enabled Status for slv_events_in[88]
23	ENA_STATUS_151	W1C	0h	Enabled Status for slv_events_in[87]
22	ENA_STATUS_150	W1C	0h	Enabled Status for slv_events_in[86]
21	ENA_STATUS_149	W1C	0h	Enabled Status for slv_events_in[85]
20	ENA_STATUS_148	W1C	0h	Enabled Status for slv_events_in[84]
19	ENA_STATUS_147	W1C	0h	Enabled Status for slv_events_in[83]
18	ENA_STATUS_146	W1C	0h	Enabled Status for slv_events_in[82]
17	ENA_STATUS_145	W1C	0h	Enabled Status for slv_events_in[81]
16	ENA_STATUS_144	W1C	0h	Enabled Status for slv_events_in[80]
15	ENA_STATUS_143	W1C	0h	Enabled Status for slv_events_in[79]
14	ENA_STATUS_142	W1C	0h	Enabled Status for slv_events_in[78]

Table 15-465. ICSS_INTC_ENA_STATUS_REG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	ENA_STATUS_141	W1C	0h	Enabled Status for slv_events_in[77]
12	ENA_STATUS_140	W1C	0h	Enabled Status for slv_events_in[76]
11	ENA_STATUS_139	W1C	0h	Enabled Status for slv_events_in[75]
10	ENA_STATUS_138	W1C	0h	Enabled Status for slv_events_in[74]
9	ENA_STATUS_137	W1C	0h	Enabled Status for slv_events_in[73]
8	ENA_STATUS_136	W1C	0h	Enabled Status for slv_events_in[72]
7	ENA_STATUS_135	W1C	0h	Enabled Status for slv_events_in[71]
6	ENA_STATUS_134	W1C	0h	Enabled Status for slv_events_in[70]
5	ENA_STATUS_133	W1C	0h	Enabled Status for slv_events_in[69]
4	ENA_STATUS_132	W1C	0h	Enabled Status for slv_events_in[68]
3	ENA_STATUS_131	W1C	0h	Enabled Status for slv_events_in[67]
2	ENA_STATUS_130	W1C	0h	Enabled Status for slv_events_in[66]
1	ENA_STATUS_129	W1C	0h	Enabled Status for slv_events_in[65]
0	ENA_STATUS_128	W1C	0h	Enabled Status for slv_events_in[64]

Table 15-466. Register Call Summary for ICSS_INTC_ENA_STATUS_REG4

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_ENA_STATUS_REG4 Register \(Offset = 290h\) \[reset = 0h\]: \[0\]](#)

15.7.22 ICSS_INTC_ENABLE_REG0 Register (Offset = 300h) [reset = 0h]

ICSS_INTC_ENABLE_REG0 is shown in Figure 15-152 and described in Table 15-468.

Return to [Summary Table](#).

Enable Register 0

Table 15-467. ICSS_INTC_ENABLE_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0300h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0300h

Figure 15-152. ICSS_INTC_ENABLE_REG0 Register

31	30	29	28	27	26	25	24
ENABLE_31	ENABLE_30	ENABLE_29	ENABLE_28	ENABLE_27	ENABLE_26	ENABLE_25	ENABLE_24
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
23	22	21	20	19	18	17	16
ENABLE_23	ENABLE_22	ENABLE_21	ENABLE_20	ENABLE_19	ENABLE_18	ENABLE_17	ENABLE_16
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
15	14	13	12	11	10	9	8
ENABLE_15	ENABLE_14	ENABLE_13	ENABLE_12	ENABLE_11	ENABLE_10	ENABLE_9	ENABLE_8
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
7	6	5	4	3	2	1	0
ENABLE_7	ENABLE_6	ENABLE_5	ENABLE_4	ENABLE_3	ENABLE_2	ENABLE_1	ENABLE_0
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h

LEGEND: W1S = Write 1 to Set Bit; -n = value after reset

Table 15-468. ICSS_INTC_ENABLE_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE_31	W1S	0h	Enable (set) for intr_in[31]
30	ENABLE_30	W1S	0h	Enable (set) for intr_in[30]
29	ENABLE_29	W1S	0h	Enable (set) for intr_in[29]
28	ENABLE_28	W1S	0h	Enable (set) for intr_in[28]
27	ENABLE_27	W1S	0h	Enable (set) for intr_in[27]
26	ENABLE_26	W1S	0h	Enable (set) for intr_in[26]
25	ENABLE_25	W1S	0h	Enable (set) for intr_in[25]
24	ENABLE_24	W1S	0h	Enable (set) for intr_in[24]
23	ENABLE_23	W1S	0h	Enable (set) for intr_in[23]
22	ENABLE_22	W1S	0h	Enable (set) for intr_in[22]
21	ENABLE_21	W1S	0h	Enable (set) for intr_in[21]
20	ENABLE_20	W1S	0h	Enable (set) for intr_in[20]
19	ENABLE_19	W1S	0h	Enable (set) for intr_in[19]
18	ENABLE_18	W1S	0h	Enable (set) for intr_in[18]
17	ENABLE_17	W1S	0h	Enable (set) for intr_in[17]
16	ENABLE_16	W1S	0h	Enable (set) for intr_in[16]
15	ENABLE_15	W1S	0h	Enable (set) for intr_in[15]
14	ENABLE_14	W1S	0h	Enable (set) for intr_in[14]
13	ENABLE_13	W1S	0h	Enable (set) for intr_in[13]
12	ENABLE_12	W1S	0h	Enable (set) for intr_in[12]
11	ENABLE_11	W1S	0h	Enable (set) for intr_in[11]

Table 15-468. ICSS_INTC_ENABLE_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	ENABLE_10	W1S	0h	Enable (set) for intr_in[10]
9	ENABLE_9	W1S	0h	Enable (set) for intr_in[9]
8	ENABLE_8	W1S	0h	Enable (set) for intr_in[8]
7	ENABLE_7	W1S	0h	Enable (set) for intr_in[7]
6	ENABLE_6	W1S	0h	Enable (set) for intr_in[6]
5	ENABLE_5	W1S	0h	Enable (set) for intr_in[5]
4	ENABLE_4	W1S	0h	Enable (set) for intr_in[4]
3	ENABLE_3	W1S	0h	Enable (set) for intr_in[3]
2	ENABLE_2	W1S	0h	Enable (set) for intr_in[2]
1	ENABLE_1	W1S	0h	Enable (set) for intr_in[1]
0	ENABLE_0	W1S	0h	Enable (set) for intr_in[0]

Table 15-469. Register Call Summary for ICSS_INTC_ENABLE_REG0

PRU_ICSS_INTC_INTC Registers

- [ICSS_INTC_ENABLE_REG0 Register \(Offset = 300h\) \[reset = 0h\]: \[0\]](#)
- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)

15.7.23 ICSS_INTC_ENABLE_REG1 Register (Offset = 304h) [reset = 0h]

ICSS_INTC_ENABLE_REG1 is shown in Figure 15-153 and described in Table 15-471.

Return to [Summary Table](#).

Enable Register 1

Table 15-470. ICSS_INTC_ENABLE_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0304h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0304h

Figure 15-153. ICSS_INTC_ENABLE_REG1 Register

31	30	29	28	27	26	25	24
ENABLE_63	ENABLE_62	ENABLE_61	ENABLE_60	ENABLE_59	ENABLE_58	ENABLE_57	ENABLE_56
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
23	22	21	20	19	18	17	16
ENABLE_55	ENABLE_54	ENABLE_53	ENABLE_52	ENABLE_51	ENABLE_50	ENABLE_49	ENABLE_48
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
15	14	13	12	11	10	9	8
ENABLE_47	ENABLE_46	ENABLE_45	ENABLE_44	ENABLE_43	ENABLE_42	ENABLE_41	ENABLE_40
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
7	6	5	4	3	2	1	0
ENABLE_39	ENABLE_38	ENABLE_37	ENABLE_36	ENABLE_35	ENABLE_34	ENABLE_33	ENABLE_32
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h

LEGEND: W1S = Write 1 to Set Bit; -n = value after reset

Table 15-471. ICSS_INTC_ENABLE_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE_63	W1S	0h	Enable (set) for intr_in[63]
30	ENABLE_62	W1S	0h	Enable (set) for intr_in[62]
29	ENABLE_61	W1S	0h	Enable (set) for intr_in[61]
28	ENABLE_60	W1S	0h	Enable (set) for intr_in[60]
27	ENABLE_59	W1S	0h	Enable (set) for intr_in[59]
26	ENABLE_58	W1S	0h	Enable (set) for intr_in[58]
25	ENABLE_57	W1S	0h	Enable (set) for intr_in[57]
24	ENABLE_56	W1S	0h	Enable (set) for intr_in[56]
23	ENABLE_55	W1S	0h	Enable (set) for intr_in[55]
22	ENABLE_54	W1S	0h	Enable (set) for intr_in[54]
21	ENABLE_53	W1S	0h	Enable (set) for intr_in[53]
20	ENABLE_52	W1S	0h	Enable (set) for intr_in[52]
19	ENABLE_51	W1S	0h	Enable (set) for intr_in[51]
18	ENABLE_50	W1S	0h	Enable (set) for intr_in[50]
17	ENABLE_49	W1S	0h	Enable (set) for intr_in[49]
16	ENABLE_48	W1S	0h	Enable (set) for intr_in[48]
15	ENABLE_47	W1S	0h	Enable (set) for intr_in[47]
14	ENABLE_46	W1S	0h	Enable (set) for intr_in[46]
13	ENABLE_45	W1S	0h	Enable (set) for intr_in[45]
12	ENABLE_44	W1S	0h	Enable (set) for intr_in[44]
11	ENABLE_43	W1S	0h	Enable (set) for intr_in[43]

Table 15-471. ICSS_INTC_ENABLE_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	ENABLE_42	W1S	0h	Enable (set) for intr_in[42]
9	ENABLE_41	W1S	0h	Enable (set) for intr_in[41]
8	ENABLE_40	W1S	0h	Enable (set) for intr_in[40]
7	ENABLE_39	W1S	0h	Enable (set) for intr_in[39]
6	ENABLE_38	W1S	0h	Enable (set) for intr_in[38]
5	ENABLE_37	W1S	0h	Enable (set) for intr_in[37]
4	ENABLE_36	W1S	0h	Enable (set) for intr_in[36]
3	ENABLE_35	W1S	0h	Enable (set) for intr_in[35]
2	ENABLE_34	W1S	0h	Enable (set) for intr_in[34]
1	ENABLE_33	W1S	0h	Enable (set) for intr_in[33]
0	ENABLE_32	W1S	0h	Enable (set) for intr_in[32]

Table 15-472. Register Call Summary for ICSS_INTC_ENABLE_REG1

PRU_ICSS_INTC_INTC Registers

- [ICSS_INTC_ENABLE_REG1 Register \(Offset = 304h\) \[reset = 0h\]: \[0\]](#)
- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)

15.7.24 ICSS_INTC_ENABLE_REG2 Register (Offset = 308h) [reset = 0h]

ICSS_INTC_ENABLE_REG2 is shown in Figure 15-154 and described in Table 15-474.

Return to [Summary Table](#).

Enable Register 2

Table 15-473. ICSS_INTC_ENABLE_REG2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTCL_SLV	0B02 0308h
PRU_ICSSG1_PR1_ICSS_INTC_INTCL_SLV	0B12 0308h

Figure 15-154. ICSS_INTC_ENABLE_REG2 Register

31	30	29	28	27	26	25	24
ENABLE_95	ENABLE_94	ENABLE_93	ENABLE_92	ENABLE_91	ENABLE_90	ENABLE_89	ENABLE_88
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
23	22	21	20	19	18	17	16
ENABLE_87	ENABLE_86	ENABLE_85	ENABLE_84	ENABLE_83	ENABLE_82	ENABLE_81	ENABLE_80
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
15	14	13	12	11	10	9	8
ENABLE_79	ENABLE_78	ENABLE_77	ENABLE_76	ENABLE_75	ENABLE_74	ENABLE_73	ENABLE_72
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
7	6	5	4	3	2	1	0
ENABLE_71	ENABLE_70	ENABLE_69	ENABLE_68	ENABLE_67	ENABLE_66	ENABLE_65	ENABLE_64
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h

LEGEND: W1S = Write 1 to Set Bit; -n = value after reset

Table 15-474. ICSS_INTC_ENABLE_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE_95	W1S	0h	Enable (set) for slv_events_in[31]
30	ENABLE_94	W1S	0h	Enable (set) for slv_events_in[30]
29	ENABLE_93	W1S	0h	Enable (set) for slv_events_in[29]
28	ENABLE_92	W1S	0h	Enable (set) for slv_events_in[28]
27	ENABLE_91	W1S	0h	Enable (set) for slv_events_in[27]
26	ENABLE_90	W1S	0h	Enable (set) for slv_events_in[26]
25	ENABLE_89	W1S	0h	Enable (set) for slv_events_in[25]
24	ENABLE_88	W1S	0h	Enable (set) for slv_events_in[24]
23	ENABLE_87	W1S	0h	Enable (set) for slv_events_in[23]
22	ENABLE_86	W1S	0h	Enable (set) for slv_events_in[22]
21	ENABLE_85	W1S	0h	Enable (set) for slv_events_in[21]
20	ENABLE_84	W1S	0h	Enable (set) for slv_events_in[20]
19	ENABLE_83	W1S	0h	Enable (set) for slv_events_in[19]
18	ENABLE_82	W1S	0h	Enable (set) for slv_events_in[18]
17	ENABLE_81	W1S	0h	Enable (set) for slv_events_in[17]
16	ENABLE_80	W1S	0h	Enable (set) for slv_events_in[16]
15	ENABLE_79	W1S	0h	Enable (set) for slv_events_in[15]
14	ENABLE_78	W1S	0h	Enable (set) for slv_events_in[14]
13	ENABLE_77	W1S	0h	Enable (set) for slv_events_in[13]
12	ENABLE_76	W1S	0h	Enable (set) for slv_events_in[12]
11	ENABLE_75	W1S	0h	Enable (set) for slv_events_in[11]

Table 15-474. ICSS_INTC_ENABLE_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	ENABLE_74	W1S	0h	Enable (set) for slv_events_in[10]
9	ENABLE_73	W1S	0h	Enable (set) for slv_events_in[9]
8	ENABLE_72	W1S	0h	Enable (set) for slv_events_in[8]
7	ENABLE_71	W1S	0h	Enable (set) for slv_events_in[7]
6	ENABLE_70	W1S	0h	Enable (set) for slv_events_in[6]
5	ENABLE_69	W1S	0h	Enable (set) for slv_events_in[5]
4	ENABLE_68	W1S	0h	Enable (set) for slv_events_in[4]
3	ENABLE_67	W1S	0h	Enable (set) for slv_events_in[3]
2	ENABLE_66	W1S	0h	Enable (set) for slv_events_in[2]
1	ENABLE_65	W1S	0h	Enable (set) for slv_events_in[1]
0	ENABLE_64	W1S	0h	Enable (set) for slv_events_in[0]

Table 15-475. Register Call Summary for ICSS_INTC_ENABLE_REG2

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_ENABLE_REG2 Register \(Offset = 308h\) \[reset = 0h\]: \[0\]](#)

15.7.25 ICSS_INTC_ENABLE_REG3 Register (Offset = 30Ch) [reset = 0h]

ICSS_INTC_ENABLE_REG3 is shown in Figure 15-155 and described in Table 15-477.

Return to [Summary Table](#).

Enable Register 3

Table 15-476. ICSS_INTC_ENABLE_REG3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTCLV	0B02 030Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTCLV	0B12 030Ch

Figure 15-155. ICSS_INTC_ENABLE_REG3 Register

31	30	29	28	27	26	25	24
ENABLE_127	ENABLE_126	ENABLE_125	ENABLE_124	ENABLE_123	ENABLE_122	ENABLE_121	ENABLE_120
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
23	22	21	20	19	18	17	16
ENABLE_119	ENABLE_118	ENABLE_117	ENABLE_116	ENABLE_115	ENABLE_114	ENABLE_113	ENABLE_112
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
15	14	13	12	11	10	9	8
ENABLE_111	ENABLE_110	ENABLE_109	ENABLE_108	ENABLE_107	ENABLE_106	ENABLE_105	ENABLE_104
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
7	6	5	4	3	2	1	0
ENABLE_103	ENABLE_102	ENABLE_101	ENABLE_100	ENABLE_99	ENABLE_98	ENABLE_97	ENABLE_96
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h

LEGEND: W1S = Write 1 to Set Bit; -n = value after reset

Table 15-477. ICSS_INTC_ENABLE_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE_127	W1S	0h	Enable (set) for slv_events_in[63]
30	ENABLE_126	W1S	0h	Enable (set) for slv_events_in[62]
29	ENABLE_125	W1S	0h	Enable (set) for slv_events_in[61]
28	ENABLE_124	W1S	0h	Enable (set) for slv_events_in[60]
27	ENABLE_123	W1S	0h	Enable (set) for slv_events_in[59]
26	ENABLE_122	W1S	0h	Enable (set) for slv_events_in[58]
25	ENABLE_121	W1S	0h	Enable (set) for slv_events_in[57]
24	ENABLE_120	W1S	0h	Enable (set) for slv_events_in[56]
23	ENABLE_119	W1S	0h	Enable (set) for slv_events_in[55]
22	ENABLE_118	W1S	0h	Enable (set) for slv_events_in[54]
21	ENABLE_117	W1S	0h	Enable (set) for slv_events_in[53]
20	ENABLE_116	W1S	0h	Enable (set) for slv_events_in[52]
19	ENABLE_115	W1S	0h	Enable (set) for slv_events_in[51]
18	ENABLE_114	W1S	0h	Enable (set) for slv_events_in[50]
17	ENABLE_113	W1S	0h	Enable (set) for slv_events_in[49]
16	ENABLE_112	W1S	0h	Enable (set) for slv_events_in[48]
15	ENABLE_111	W1S	0h	Enable (set) for slv_events_in[47]
14	ENABLE_110	W1S	0h	Enable (set) for slv_events_in[46]
13	ENABLE_109	W1S	0h	Enable (set) for slv_events_in[45]
12	ENABLE_108	W1S	0h	Enable (set) for slv_events_in[44]
11	ENABLE_107	W1S	0h	Enable (set) for slv_events_in[43]

Table 15-477. ICSS_INTC_ENABLE_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	ENABLE_106	W1S	0h	Enable (set) for slv_events_in[42]
9	ENABLE_105	W1S	0h	Enable (set) for slv_events_in[41]
8	ENABLE_104	W1S	0h	Enable (set) for slv_events_in[40]
7	ENABLE_103	W1S	0h	Enable (set) for slv_events_in[39]
6	ENABLE_102	W1S	0h	Enable (set) for slv_events_in[38]
5	ENABLE_101	W1S	0h	Enable (set) for slv_events_in[37]
4	ENABLE_100	W1S	0h	Enable (set) for slv_events_in[36]
3	ENABLE_99	W1S	0h	Enable (set) for slv_events_in[35]
2	ENABLE_98	W1S	0h	Enable (set) for slv_events_in[34]
1	ENABLE_97	W1S	0h	Enable (set) for slv_events_in[33]
0	ENABLE_96	W1S	0h	Enable (set) for slv_events_in[32]

Table 15-478. Register Call Summary for ICSS_INTC_ENABLE_REG3

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_ENABLE_REG3 Register \(Offset = 30Ch\) \[reset = 0h\]: \[0\]](#)

15.7.26 ICSS_INTC_ENABLE_REG4 Register (Offset = 310h) [reset = 0h]

ICSS_INTC_ENABLE_REG4 is shown in Figure 15-156 and described in Table 15-480.

Return to [Summary Table](#).

Enable Register 4

Table 15-479. ICSS_INTC_ENABLE_REG4 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTCLV	0B02 0310h
PRU_ICSSG1_PR1_ICSS_INTC_INTCLV	0B12 0310h

Figure 15-156. ICSS_INTC_ENABLE_REG4 Register

31	30	29	28	27	26	25	24
ENABLE_159	ENABLE_158	ENABLE_157	ENABLE_156	ENABLE_155	ENABLE_154	ENABLE_153	ENABLE_152
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
23	22	21	20	19	18	17	16
ENABLE_151	ENABLE_150	ENABLE_149	ENABLE_148	ENABLE_147	ENABLE_146	ENABLE_145	ENABLE_144
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
15	14	13	12	11	10	9	8
ENABLE_143	ENABLE_142	ENABLE_141	ENABLE_140	ENABLE_139	ENABLE_138	ENABLE_137	ENABLE_136
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h
7	6	5	4	3	2	1	0
ENABLE_135	ENABLE_134	ENABLE_133	ENABLE_132	ENABLE_131	ENABLE_130	ENABLE_129	ENABLE_128
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h

LEGEND: W1S = Write 1 to Set Bit; -n = value after reset

Table 15-480. ICSS_INTC_ENABLE_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE_159	W1S	0h	Enable (set) for slv_events_in[95]
30	ENABLE_158	W1S	0h	Enable (set) for slv_events_in[94]
29	ENABLE_157	W1S	0h	Enable (set) for slv_events_in[93]
28	ENABLE_156	W1S	0h	Enable (set) for slv_events_in[92]
27	ENABLE_155	W1S	0h	Enable (set) for slv_events_in[91]
26	ENABLE_154	W1S	0h	Enable (set) for slv_events_in[90]
25	ENABLE_153	W1S	0h	Enable (set) for slv_events_in[89]
24	ENABLE_152	W1S	0h	Enable (set) for slv_events_in[88]
23	ENABLE_151	W1S	0h	Enable (set) for slv_events_in[87]
22	ENABLE_150	W1S	0h	Enable (set) for slv_events_in[86]
21	ENABLE_149	W1S	0h	Enable (set) for slv_events_in[85]
20	ENABLE_148	W1S	0h	Enable (set) for slv_events_in[84]
19	ENABLE_147	W1S	0h	Enable (set) for slv_events_in[83]
18	ENABLE_146	W1S	0h	Enable (set) for slv_events_in[82]
17	ENABLE_145	W1S	0h	Enable (set) for slv_events_in[81]
16	ENABLE_144	W1S	0h	Enable (set) for slv_events_in[80]
15	ENABLE_143	W1S	0h	Enable (set) for slv_events_in[79]
14	ENABLE_142	W1S	0h	Enable (set) for slv_events_in[78]
13	ENABLE_141	W1S	0h	Enable (set) for slv_events_in[77]
12	ENABLE_140	W1S	0h	Enable (set) for slv_events_in[76]
11	ENABLE_139	W1S	0h	Enable (set) for slv_events_in[75]

Table 15-480. ICSS_INTC_ENABLE_REG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	ENABLE_138	W1S	0h	Enable (set) for slv_events_in[74]
9	ENABLE_137	W1S	0h	Enable (set) for slv_events_in[73]
8	ENABLE_136	W1S	0h	Enable (set) for slv_events_in[72]
7	ENABLE_135	W1S	0h	Enable (set) for slv_events_in[71]
6	ENABLE_134	W1S	0h	Enable (set) for slv_events_in[70]
5	ENABLE_133	W1S	0h	Enable (set) for slv_events_in[69]
4	ENABLE_132	W1S	0h	Enable (set) for slv_events_in[68]
3	ENABLE_131	W1S	0h	Enable (set) for slv_events_in[67]
2	ENABLE_130	W1S	0h	Enable (set) for slv_events_in[66]
1	ENABLE_129	W1S	0h	Enable (set) for slv_events_in[65]
0	ENABLE_128	W1S	0h	Enable (set) for slv_events_in[64]

Table 15-481. Register Call Summary for ICSS_INTC_ENABLE_REG4

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_ENABLE_REG4 Register \(Offset = 310h\) \[reset = 0h\]: \[0\]](#)

15.7.27 ICSS_INTC_ENABLE_CLR_REG0 Register (Offset = 380h) [reset = 0h]

ICSS_INTC_ENABLE_CLR_REG0 is shown in Figure 15-157 and described in Table 15-483.

Return to [Summary Table](#).

Enable Clear Register 0

Table 15-482. ICSS_INTC_ENABLE_CLR_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTCLV	0B02 0380h
PRU_ICSSG1_PR1_ICSS_INTC_INTCLV	0B12 0380h

Figure 15-157. ICSS_INTC_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
ENABLE_31_CLR	ENABLE_30_CLR	ENABLE_29_CLR	ENABLE_28_CLR	ENABLE_27_CLR	ENABLE_26_CLR	ENABLE_25_CLR	ENABLE_24_CLR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
23	22	21	20	19	18	17	16
ENABLE_23_CLR	ENABLE_22_CLR	ENABLE_21_CLR	ENABLE_20_CLR	ENABLE_19_CLR	ENABLE_18_CLR	ENABLE_17_CLR	ENABLE_16_CLR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
15	14	13	12	11	10	9	8
ENABLE_15_CLR	ENABLE_14_CLR	ENABLE_13_CLR	ENABLE_12_CLR	ENABLE_11_CLR	ENABLE_10_CLR	ENABLE_9_CLR	ENABLE_8_CLR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
7	6	5	4	3	2	1	0
ENABLE_7_CLR	ENABLE_6_CLR	ENABLE_5_CLR	ENABLE_4_CLR	ENABLE_3_CLR	ENABLE_2_CLR	ENABLE_1_CLR	ENABLE_0_CLR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h

LEGEND: W1C = Write 1 to Clear Bit; -n = value after reset

Table 15-483. ICSS_INTC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE_31_CLR	W1C	0h	Enable clear for intr_in[31]
30	ENABLE_30_CLR	W1C	0h	Enable clear for intr_in[30]
29	ENABLE_29_CLR	W1C	0h	Enable clear for intr_in[29]
28	ENABLE_28_CLR	W1C	0h	Enable clear for intr_in[28]
27	ENABLE_27_CLR	W1C	0h	Enable clear for intr_in[27]
26	ENABLE_26_CLR	W1C	0h	Enable clear for intr_in[26]
25	ENABLE_25_CLR	W1C	0h	Enable clear for intr_in[25]
24	ENABLE_24_CLR	W1C	0h	Enable clear for intr_in[24]
23	ENABLE_23_CLR	W1C	0h	Enable clear for intr_in[23]
22	ENABLE_22_CLR	W1C	0h	Enable clear for intr_in[22]
21	ENABLE_21_CLR	W1C	0h	Enable clear for intr_in[21]
20	ENABLE_20_CLR	W1C	0h	Enable clear for intr_in[20]
19	ENABLE_19_CLR	W1C	0h	Enable clear for intr_in[19]
18	ENABLE_18_CLR	W1C	0h	Enable clear for intr_in[18]
17	ENABLE_17_CLR	W1C	0h	Enable clear for intr_in[17]
16	ENABLE_16_CLR	W1C	0h	Enable clear for intr_in[16]
15	ENABLE_15_CLR	W1C	0h	Enable clear for intr_in[15]
14	ENABLE_14_CLR	W1C	0h	Enable clear for intr_in[14]

Table 15-483. ICSS_INTC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	ENABLE_13_CLR	W1C	0h	Enable clear for intr_in[13]
12	ENABLE_12_CLR	W1C	0h	Enable clear for intr_in[12]
11	ENABLE_11_CLR	W1C	0h	Enable clear for intr_in[11]
10	ENABLE_10_CLR	W1C	0h	Enable clear for intr_in[10]
9	ENABLE_9_CLR	W1C	0h	Enable clear for intr_in[9]
8	ENABLE_8_CLR	W1C	0h	Enable clear for intr_in[8]
7	ENABLE_7_CLR	W1C	0h	Enable clear for intr_in[7]
6	ENABLE_6_CLR	W1C	0h	Enable clear for intr_in[6]
5	ENABLE_5_CLR	W1C	0h	Enable clear for intr_in[5]
4	ENABLE_4_CLR	W1C	0h	Enable clear for intr_in[4]
3	ENABLE_3_CLR	W1C	0h	Enable clear for intr_in[3]
2	ENABLE_2_CLR	W1C	0h	Enable clear for intr_in[2]
1	ENABLE_1_CLR	W1C	0h	Enable clear for intr_in[1]
0	ENABLE_0_CLR	W1C	0h	Enable clear for intr_in[0]

Table 15-484. Register Call Summary for ICSS_INTC_ENABLE_CLR_REG0

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_ENABLE_CLR_REG0 Register \(Offset = 380h\) \[reset = 0h\]: \[0\]](#)

PRU_ICSSG Local INTC

- [PRU_ICSSG Interrupt Controller Basic Programming Model: \[0\]](#)

PRU_ICSSG Interrupt Controller Functional Description

- [PRU_ICSSG Interrupt Status Checking: \[0\] \[1\]](#)
- [PRU_ICSSG Interrupt Disabling: \[0\]](#)
- [PRU_ICSSG Interrupt Status Clearing: \[0\]](#)

15.7.28 ICSS_INTC_ENABLE_CLR_REG1 Register (Offset = 384h) [reset = 0h]

ICSS_INTC_ENABLE_CLR_REG1 is shown in Figure 15-158 and described in Table 15-486.

Return to [Summary Table](#).

Enable Clear Register 1

Table 15-485. ICSS_INTC_ENABLE_CLR_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTCLV	0B02 0384h
PRU_ICSSG1_PR1_ICSS_INTC_INTCLV	0B12 0384h

Figure 15-158. ICSS_INTC_ENABLE_CLR_REG1 Register

31	30	29	28	27	26	25	24
ENABLE_63_C LR	ENABLE_62_C LR	ENABLE_61_C LR	ENABLE_60_C LR	ENABLE_59_C LR	ENABLE_58_C LR	ENABLE_57_C LR	ENABLE_56_C LR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
23	22	21	20	19	18	17	16
ENABLE_55_C LR	ENABLE_54_C LR	ENABLE_53_C LR	ENABLE_52_C LR	ENABLE_51_C LR	ENABLE_50_C LR	ENABLE_49_C LR	ENABLE_48_C LR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
15	14	13	12	11	10	9	8
ENABLE_47_C LR	ENABLE_46_C LR	ENABLE_45_C LR	ENABLE_44_C LR	ENABLE_43_C LR	ENABLE_42_C LR	ENABLE_41_C LR	ENABLE_40_C LR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
7	6	5	4	3	2	1	0
ENABLE_39_C LR	ENABLE_38_C LR	ENABLE_37_C LR	ENABLE_36_C LR	ENABLE_35_C LR	ENABLE_34_C LR	ENABLE_33_C LR	ENABLE_32_C LR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h

LEGEND: W1C = Write 1 to Clear Bit; -n = value after reset

Table 15-486. ICSS_INTC_ENABLE_CLR_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE_63_CLR	W1C	0h	Enable clear for intr_in[63]
30	ENABLE_62_CLR	W1C	0h	Enable clear for intr_in[62]
29	ENABLE_61_CLR	W1C	0h	Enable clear for intr_in[61]
28	ENABLE_60_CLR	W1C	0h	Enable clear for intr_in[60]
27	ENABLE_59_CLR	W1C	0h	Enable clear for intr_in[59]
26	ENABLE_58_CLR	W1C	0h	Enable clear for intr_in[58]
25	ENABLE_57_CLR	W1C	0h	Enable clear for intr_in[57]
24	ENABLE_56_CLR	W1C	0h	Enable clear for intr_in[56]
23	ENABLE_55_CLR	W1C	0h	Enable clear for intr_in[55]
22	ENABLE_54_CLR	W1C	0h	Enable clear for intr_in[54]
21	ENABLE_53_CLR	W1C	0h	Enable clear for intr_in[53]
20	ENABLE_52_CLR	W1C	0h	Enable clear for intr_in[52]
19	ENABLE_51_CLR	W1C	0h	Enable clear for intr_in[51]
18	ENABLE_50_CLR	W1C	0h	Enable clear for intr_in[50]
17	ENABLE_49_CLR	W1C	0h	Enable clear for intr_in[49]
16	ENABLE_48_CLR	W1C	0h	Enable clear for intr_in[48]
15	ENABLE_47_CLR	W1C	0h	Enable clear for intr_in[47]
14	ENABLE_46_CLR	W1C	0h	Enable clear for intr_in[46]

Table 15-486. ICSS_INTC_ENABLE_CLR_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	ENABLE_45_CLR	W1C	0h	Enable clear for intr_in[45]
12	ENABLE_44_CLR	W1C	0h	Enable clear for intr_in[44]
11	ENABLE_43_CLR	W1C	0h	Enable clear for intr_in[43]
10	ENABLE_42_CLR	W1C	0h	Enable clear for intr_in[42]
9	ENABLE_41_CLR	W1C	0h	Enable clear for intr_in[41]
8	ENABLE_40_CLR	W1C	0h	Enable clear for intr_in[40]
7	ENABLE_39_CLR	W1C	0h	Enable clear for intr_in[39]
6	ENABLE_38_CLR	W1C	0h	Enable clear for intr_in[38]
5	ENABLE_37_CLR	W1C	0h	Enable clear for intr_in[37]
4	ENABLE_36_CLR	W1C	0h	Enable clear for intr_in[36]
3	ENABLE_35_CLR	W1C	0h	Enable clear for intr_in[35]
2	ENABLE_34_CLR	W1C	0h	Enable clear for intr_in[34]
1	ENABLE_33_CLR	W1C	0h	Enable clear for intr_in[33]
0	ENABLE_32_CLR	W1C	0h	Enable clear for intr_in[32]

Table 15-487. Register Call Summary for ICSS_INTC_ENABLE_CLR_REG1

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_ENABLE_CLR_REG1 Register \(Offset = 384h\) \[reset = 0h\]: \[0\]](#)

15.7.29 ICSS_INTC_ENABLE_CLR_REG2 Register (Offset = 388h) [reset = 0h]

ICSS_INTC_ENABLE_CLR_REG2 is shown in Figure 15-159 and described in Table 15-489.

Return to [Summary Table](#).

Enable Clear Register 2

Table 15-488. ICSS_INTC_ENABLE_CLR_REG2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTCLV	0B02 0388h
PRU_ICSSG1_PR1_ICSS_INTC_INTCLV	0B12 0388h

Figure 15-159. ICSS_INTC_ENABLE_CLR_REG2 Register

31	30	29	28	27	26	25	24
ENABLE_95_C LR	ENABLE_94_C LR	ENABLE_93_C LR	ENABLE_92_C LR	ENABLE_91_C LR	ENABLE_90_C LR	ENABLE_89_C LR	ENABLE_88_C LR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
23	22	21	20	19	18	17	16
ENABLE_87_C LR	ENABLE_86_C LR	ENABLE_85_C LR	ENABLE_84_C LR	ENABLE_83_C LR	ENABLE_82_C LR	ENABLE_81_C LR	ENABLE_80_C LR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
15	14	13	12	11	10	9	8
ENABLE_79_C LR	ENABLE_78_C LR	ENABLE_77_C LR	ENABLE_76_C LR	ENABLE_75_C LR	ENABLE_74_C LR	ENABLE_73_C LR	ENABLE_72_C LR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
7	6	5	4	3	2	1	0
ENABLE_71_C LR	ENABLE_70_C LR	ENABLE_69_C LR	ENABLE_68_C LR	ENABLE_67_C LR	ENABLE_66_C LR	ENABLE_65_C LR	ENABLE_64_C LR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h

LEGEND: W1C = Write 1 to Clear Bit; -n = value after reset

Table 15-489. ICSS_INTC_ENABLE_CLR_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE_95_CLR	W1C	0h	Enable clear for slv_events_in[31]
30	ENABLE_94_CLR	W1C	0h	Enable clear for slv_events_in[30]
29	ENABLE_93_CLR	W1C	0h	Enable clear for slv_events_in[29]
28	ENABLE_92_CLR	W1C	0h	Enable clear for slv_events_in[28]
27	ENABLE_91_CLR	W1C	0h	Enable clear for slv_events_in[27]
26	ENABLE_90_CLR	W1C	0h	Enable clear for slv_events_in[26]
25	ENABLE_89_CLR	W1C	0h	Enable clear for slv_events_in[25]
24	ENABLE_88_CLR	W1C	0h	Enable clear for slv_events_in[24]
23	ENABLE_87_CLR	W1C	0h	Enable clear for slv_events_in[23]
22	ENABLE_86_CLR	W1C	0h	Enable clear for slv_events_in[22]
21	ENABLE_85_CLR	W1C	0h	Enable clear for slv_events_in[21]
20	ENABLE_84_CLR	W1C	0h	Enable clear for slv_events_in[20]
19	ENABLE_83_CLR	W1C	0h	Enable clear for slv_events_in[19]
18	ENABLE_82_CLR	W1C	0h	Enable clear for slv_events_in[18]
17	ENABLE_81_CLR	W1C	0h	Enable clear for slv_events_in[17]
16	ENABLE_80_CLR	W1C	0h	Enable clear for slv_events_in[16]
15	ENABLE_79_CLR	W1C	0h	Enable clear for slv_events_in[15]
14	ENABLE_78_CLR	W1C	0h	Enable clear for slv_events_in[14]

Table 15-489. ICSS_INTC_ENABLE_CLR_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	ENABLE_77_CLR	W1C	0h	Enable clear for slv_events_in[13]
12	ENABLE_76_CLR	W1C	0h	Enable clear for slv_events_in[12]
11	ENABLE_75_CLR	W1C	0h	Enable clear for slv_events_in[11]
10	ENABLE_74_CLR	W1C	0h	Enable clear for slv_events_in[10]
9	ENABLE_73_CLR	W1C	0h	Enable clear for slv_events_in[9]
8	ENABLE_72_CLR	W1C	0h	Enable clear for slv_events_in[8]
7	ENABLE_71_CLR	W1C	0h	Enable clear for slv_events_in[7]
6	ENABLE_70_CLR	W1C	0h	Enable clear for slv_events_in[6]
5	ENABLE_69_CLR	W1C	0h	Enable clear for slv_events_in[5]
4	ENABLE_68_CLR	W1C	0h	Enable clear for slv_events_in[4]
3	ENABLE_67_CLR	W1C	0h	Enable clear for slv_events_in[3]
2	ENABLE_66_CLR	W1C	0h	Enable clear for slv_events_in[2]
1	ENABLE_65_CLR	W1C	0h	Enable clear for slv_events_in[1]
0	ENABLE_64_CLR	W1C	0h	Enable clear for slv_events_in[0]

Table 15-490. Register Call Summary for ICSS_INTC_ENABLE_CLR_REG2

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_ENABLE_CLR_REG2 Register \(Offset = 388h\) \[reset = 0h\]: \[0\]](#)

15.7.30 ICSS_INTC_ENABLE_CLR_REG3 Register (Offset = 38Ch) [reset = 0h]

ICSS_INTC_ENABLE_CLR_REG3 is shown in Figure 15-160 and described in Table 15-492.

Return to [Summary Table](#).

Enable Clear Register 3

Table 15-491. ICSS_INTC_ENABLE_CLR_REG3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTCLV	0B02 038Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTCLV	0B12 038Ch

Figure 15-160. ICSS_INTC_ENABLE_CLR_REG3 Register

31	30	29	28	27	26	25	24
ENABLE_127_CLR	ENABLE_126_CLR	ENABLE_125_CLR	ENABLE_124_CLR	ENABLE_123_CLR	ENABLE_122_CLR	ENABLE_121_CLR	ENABLE_120_CLR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
23	22	21	20	19	18	17	16
ENABLE_119_CLR	ENABLE_118_CLR	ENABLE_117_CLR	ENABLE_116_CLR	ENABLE_115_CLR	ENABLE_114_CLR	ENABLE_113_CLR	ENABLE_112_CLR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
15	14	13	12	11	10	9	8
ENABLE_111_CLR	ENABLE_110_CLR	ENABLE_109_CLR	ENABLE_108_CLR	ENABLE_107_CLR	ENABLE_106_CLR	ENABLE_105_CLR	ENABLE_104_CLR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
7	6	5	4	3	2	1	0
ENABLE_103_CLR	ENABLE_102_CLR	ENABLE_101_CLR	ENABLE_100_CLR	ENABLE_99_CLR	ENABLE_98_CLR	ENABLE_97_CLR	ENABLE_96_CLR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h

LEGEND: W1C = Write 1 to Clear Bit; -n = value after reset

Table 15-492. ICSS_INTC_ENABLE_CLR_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE_127_CLR	W1C	0h	Enable clear for slv_events_in[63]
30	ENABLE_126_CLR	W1C	0h	Enable clear for slv_events_in[62]
29	ENABLE_125_CLR	W1C	0h	Enable clear for slv_events_in[61]
28	ENABLE_124_CLR	W1C	0h	Enable clear for slv_events_in[60]
27	ENABLE_123_CLR	W1C	0h	Enable clear for slv_events_in[59]
26	ENABLE_122_CLR	W1C	0h	Enable clear for slv_events_in[58]
25	ENABLE_121_CLR	W1C	0h	Enable clear for slv_events_in[57]
24	ENABLE_120_CLR	W1C	0h	Enable clear for slv_events_in[56]
23	ENABLE_119_CLR	W1C	0h	Enable clear for slv_events_in[55]
22	ENABLE_118_CLR	W1C	0h	Enable clear for slv_events_in[54]
21	ENABLE_117_CLR	W1C	0h	Enable clear for slv_events_in[53]
20	ENABLE_116_CLR	W1C	0h	Enable clear for slv_events_in[52]
19	ENABLE_115_CLR	W1C	0h	Enable clear for slv_events_in[51]
18	ENABLE_114_CLR	W1C	0h	Enable clear for slv_events_in[50]
17	ENABLE_113_CLR	W1C	0h	Enable clear for slv_events_in[49]
16	ENABLE_112_CLR	W1C	0h	Enable clear for slv_events_in[48]
15	ENABLE_111_CLR	W1C	0h	Enable clear for slv_events_in[47]
14	ENABLE_110_CLR	W1C	0h	Enable clear for slv_events_in[46]

Table 15-492. ICSS_INTC_ENABLE_CLR_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	ENABLE_109_CLR	W1C	0h	Enable clear for slv_events_in[45]
12	ENABLE_108_CLR	W1C	0h	Enable clear for slv_events_in[44]
11	ENABLE_107_CLR	W1C	0h	Enable clear for slv_events_in[43]
10	ENABLE_106_CLR	W1C	0h	Enable clear for slv_events_in[42]
9	ENABLE_105_CLR	W1C	0h	Enable clear for slv_events_in[41]
8	ENABLE_104_CLR	W1C	0h	Enable clear for slv_events_in[40]
7	ENABLE_103_CLR	W1C	0h	Enable clear for slv_events_in[39]
6	ENABLE_102_CLR	W1C	0h	Enable clear for slv_events_in[38]
5	ENABLE_101_CLR	W1C	0h	Enable clear for slv_events_in[37]
4	ENABLE_100_CLR	W1C	0h	Enable clear for slv_events_in[36]
3	ENABLE_99_CLR	W1C	0h	Enable clear for slv_events_in[35]
2	ENABLE_98_CLR	W1C	0h	Enable clear for slv_events_in[34]
1	ENABLE_97_CLR	W1C	0h	Enable clear for slv_events_in[33]
0	ENABLE_96_CLR	W1C	0h	Enable clear for slv_events_in[32]

Table 15-493. Register Call Summary for ICSS_INTC_ENABLE_CLR_REG3

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_ENABLE_CLR_REG3 Register \(Offset = 38Ch\) \[reset = 0h\]: \[0\]](#)

15.7.31 ICSS_INTC_ENABLE_CLR_REG4 Register (Offset = 390h) [reset = 0h]

ICSS_INTC_ENABLE_CLR_REG4 is shown in Figure 15-161 and described in Table 15-495.

Return to [Summary Table](#).

Enable Clear Register 4

Table 15-494. ICSS_INTC_ENABLE_CLR_REG4 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTCLV	0B02 0390h
PRU_ICSSG1_PR1_ICSS_INTC_INTCLV	0B12 0390h

Figure 15-161. ICSS_INTC_ENABLE_CLR_REG4 Register

31	30	29	28	27	26	25	24
ENABLE_159_CLR	ENABLE_158_CLR	ENABLE_157_CLR	ENABLE_156_CLR	ENABLE_155_CLR	ENABLE_154_CLR	ENABLE_153_CLR	ENABLE_152_CLR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
23	22	21	20	19	18	17	16
ENABLE_151_CLR	ENABLE_150_CLR	ENABLE_149_CLR	ENABLE_148_CLR	ENABLE_147_CLR	ENABLE_146_CLR	ENABLE_145_CLR	ENABLE_144_CLR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
15	14	13	12	11	10	9	8
ENABLE_143_CLR	ENABLE_142_CLR	ENABLE_141_CLR	ENABLE_140_CLR	ENABLE_139_CLR	ENABLE_138_CLR	ENABLE_137_CLR	ENABLE_136_CLR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h
7	6	5	4	3	2	1	0
ENABLE_135_CLR	ENABLE_134_CLR	ENABLE_133_CLR	ENABLE_132_CLR	ENABLE_131_CLR	ENABLE_130_CLR	ENABLE_129_CLR	ENABLE_128_CLR
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h

LEGEND: W1C = Write 1 to Clear Bit; -n = value after reset

Table 15-495. ICSS_INTC_ENABLE_CLR_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE_159_CLR	W1C	0h	Enable clear for slv_events_in[95]
30	ENABLE_158_CLR	W1C	0h	Enable clear for slv_events_in[94]
29	ENABLE_157_CLR	W1C	0h	Enable clear for slv_events_in[93]
28	ENABLE_156_CLR	W1C	0h	Enable clear for slv_events_in[92]
27	ENABLE_155_CLR	W1C	0h	Enable clear for slv_events_in[91]
26	ENABLE_154_CLR	W1C	0h	Enable clear for slv_events_in[90]
25	ENABLE_153_CLR	W1C	0h	Enable clear for slv_events_in[89]
24	ENABLE_152_CLR	W1C	0h	Enable clear for slv_events_in[88]
23	ENABLE_151_CLR	W1C	0h	Enable clear for slv_events_in[87]
22	ENABLE_150_CLR	W1C	0h	Enable clear for slv_events_in[86]
21	ENABLE_149_CLR	W1C	0h	Enable clear for slv_events_in[85]
20	ENABLE_148_CLR	W1C	0h	Enable clear for slv_events_in[84]
19	ENABLE_147_CLR	W1C	0h	Enable clear for slv_events_in[83]
18	ENABLE_146_CLR	W1C	0h	Enable clear for slv_events_in[82]
17	ENABLE_145_CLR	W1C	0h	Enable clear for slv_events_in[81]
16	ENABLE_144_CLR	W1C	0h	Enable clear for slv_events_in[80]
15	ENABLE_143_CLR	W1C	0h	Enable clear for slv_events_in[79]
14	ENABLE_142_CLR	W1C	0h	Enable clear for slv_events_in[78]

Table 15-495. ICSS_INTC_ENABLE_CLR_REG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	ENABLE_141_CLR	W1C	0h	Enable clear for slv_events_in[77]
12	ENABLE_140_CLR	W1C	0h	Enable clear for slv_events_in[76]
11	ENABLE_139_CLR	W1C	0h	Enable clear for slv_events_in[75]
10	ENABLE_138_CLR	W1C	0h	Enable clear for slv_events_in[74]
9	ENABLE_137_CLR	W1C	0h	Enable clear for slv_events_in[73]
8	ENABLE_136_CLR	W1C	0h	Enable clear for slv_events_in[72]
7	ENABLE_135_CLR	W1C	0h	Enable clear for slv_events_in[71]
6	ENABLE_134_CLR	W1C	0h	Enable clear for slv_events_in[70]
5	ENABLE_133_CLR	W1C	0h	Enable clear for slv_events_in[69]
4	ENABLE_132_CLR	W1C	0h	Enable clear for slv_events_in[68]
3	ENABLE_131_CLR	W1C	0h	Enable clear for slv_events_in[67]
2	ENABLE_130_CLR	W1C	0h	Enable clear for slv_events_in[66]
1	ENABLE_129_CLR	W1C	0h	Enable clear for slv_events_in[65]
0	ENABLE_128_CLR	W1C	0h	Enable clear for slv_events_in[64]

Table 15-496. Register Call Summary for ICSS_INTC_ENABLE_CLR_REG4

PRU_ICSS_INTC_INTC Registers ICSS_INTC_ENABLE_CLR_REG4 Register (Offset = 390h) [reset = 0h]: [0] PRU_ICSS_INTC_INTC Registers: [0]
PRU_ICSSG Local INTC PRU_ICSSG Interrupt Controller Basic Programming Model: [0]
PRU_ICSSG Interrupt Controller Functional Description PRU_ICSSG Interrupt Status Checking: [0] [1] PRU_ICSSG Interrupt Disabling: [0] PRU_ICSSG Interrupt Status Clearing: [0]

15.7.32 ICSS_INTC_CH_MAP_REG0 Register (Offset = 400h) [reset = X]

ICSS_INTC_CH_MAP_REG0 is shown in Figure 15-162 and described in Table 15-498.

Return to [Summary Table](#).

Interrupt Channel Map Register for 0 to 0+3

Table 15-497. ICSS_INTC_CH_MAP_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0400h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0400h

Figure 15-162. ICSS_INTC_CH_MAP_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_3				RESERVED				CH_MAP_2			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_1				RESERVED				CH_MAP_0			
R/W-X				R/W-0h				R/W-X				W-0h			

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 15-498. ICSS_INTC_CH_MAP_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_3	R/W	0h	Interrupt Channel Map for intr_in[3]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_2	R/W	0h	Interrupt Channel Map for intr_in[2]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_1	R/W	0h	Interrupt Channel Map for intr_in[1]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_0	W	0h	Interrupt Channel Map for intr_in[0]

Table 15-499. Register Call Summary for ICSS_INTC_CH_MAP_REG0

PRU_ICSS_INTC_INTC Registers

- [ICSS_INTC_CH_MAP_REG0 Register \(Offset = 400h\) \[reset = X\]: \[0\]](#)
- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)

15.7.33 ICSS_INTC_CH_MAP_REG1 Register (Offset = 404h) [reset = X]

ICSS_INTC_CH_MAP_REG1 is shown in Figure 15-163 and described in Table 15-501.

Return to [Summary Table](#).

Interrupt Channel Map Register for 4 to 4+3

Table 15-500. ICSS_INTC_CH_MAP_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0404h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0404h

Figure 15-163. ICSS_INTC_CH_MAP_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_7				RESERVED				CH_MAP_6			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_5				RESERVED				CH_MAP_4			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-501. ICSS_INTC_CH_MAP_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_7	R/W	0h	Interrupt Channel Map for intr_in[7]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_6	R/W	0h	Interrupt Channel Map for intr_in[6]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_5	R/W	0h	Interrupt Channel Map for intr_in[5]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_4	R/W	0h	Interrupt Channel Map for intr_in[4]

Table 15-502. Register Call Summary for ICSS_INTC_CH_MAP_REG1

PRU_ICSS_INTC_INTC Registers

- [ICSS_INTC_CH_MAP_REG1 Register \(Offset = 404h\) \[reset = X\]: \[0\]](#)
- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)

15.7.34 ICSS_INTC_CH_MAP_REG2 Register (Offset = 408h) [reset = X]

ICSS_INTC_CH_MAP_REG2 is shown in [Figure 15-164](#) and described in [Table 15-504](#).

Return to [Summary Table](#).

Interrupt Channel Map Register for 8 to 8+3

Table 15-503. ICSS_INTC_CH_MAP_REG2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0408h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0408h

Figure 15-164. ICSS_INTC_CH_MAP_REG2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_11				RESERVED				CH_MAP_10			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_9				RESERVED				CH_MAP_8			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-504. ICSS_INTC_CH_MAP_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_11	R/W	0h	Interrupt Channel Map for intr_in[11]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_10	R/W	0h	Interrupt Channel Map for intr_in[10]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_9	R/W	0h	Interrupt Channel Map for intr_in[9]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_8	R/W	0h	Interrupt Channel Map for intr_in[8]

Table 15-505. Register Call Summary for ICSS_INTC_CH_MAP_REG2

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_CH_MAP_REG2 Register \(Offset = 408h\) \[reset = X\]: \[0\]](#)

15.7.35 ICSS_INTC_CH_MAP_REG3 Register (Offset = 40Ch) [reset = X]

ICSS_INTC_CH_MAP_REG3 is shown in Figure 15-165 and described in Table 15-507.

Return to [Summary Table](#).

Interrupt Channel Map Register for 12 to 12+3

Table 15-506. ICSS_INTC_CH_MAP_REG3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 040Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 040Ch

Figure 15-165. ICSS_INTC_CH_MAP_REG3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_15				RESERVED				CH_MAP_14			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_13				RESERVED				CH_MAP_12			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-507. ICSS_INTC_CH_MAP_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_15	R/W	0h	Interrupt Channel Map for intr_in[15]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_14	R/W	0h	Interrupt Channel Map for intr_in[14]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_13	R/W	0h	Interrupt Channel Map for intr_in[13]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_12	R/W	0h	Interrupt Channel Map for intr_in[12]

Table 15-508. Register Call Summary for ICSS_INTC_CH_MAP_REG3

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_CH_MAP_REG3 Register \(Offset = 40Ch\) \[reset = X\]: \[0\]](#)

15.7.36 ICSS_INTC_CH_MAP_REG4 Register (Offset = 410h) [reset = X]

ICSS_INTC_CH_MAP_REG4 is shown in [Figure 15-166](#) and described in [Table 15-510](#).

Return to [Summary Table](#).

Interrupt Channel Map Register for 16 to 16+3

Table 15-509. ICSS_INTC_CH_MAP_REG4 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0410h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0410h

Figure 15-166. ICSS_INTC_CH_MAP_REG4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_19				RESERVED				CH_MAP_18			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_17				RESERVED				CH_MAP_16			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-510. ICSS_INTC_CH_MAP_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_19	R/W	0h	Interrupt Channel Map for intr_in[19]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_18	R/W	0h	Interrupt Channel Map for intr_in[18]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_17	R/W	0h	Interrupt Channel Map for intr_in[17]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_16	R/W	0h	Interrupt Channel Map for intr_in[16]

Table 15-511. Register Call Summary for ICSS_INTC_CH_MAP_REG4

PRU_ICSS_INTC_INTC Registers
PRU_ICSS_INTC_INTC Registers: [0] ICSS_INTC_CH_MAP_REG4 Register (Offset = 410h) [reset = X]: [0]

15.7.37 ICSS_INTC_CH_MAP_REG5 Register (Offset = 414h) [reset = X]

ICSS_INTC_CH_MAP_REG5 is shown in Figure 15-167 and described in Table 15-513.

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Interrupt Channel Map Register for 20 to 20+3

Table 15-512. ICSS_INTC_CH_MAP_REG5 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0414h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0414h

Figure 15-167. ICSS_INTC_CH_MAP_REG5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_23				RESERVED				CH_MAP_22			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_21				RESERVED				CH_MAP_20			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-513. ICSS_INTC_CH_MAP_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_23	R/W	0h	Interrupt Channel Map for intr_in[23]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_22	R/W	0h	Interrupt Channel Map for intr_in[22]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_21	R/W	0h	Interrupt Channel Map for intr_in[21]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_20	R/W	0h	Interrupt Channel Map for intr_in[20]

Table 15-514. Register Call Summary for ICSS_INTC_CH_MAP_REG5

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_CH_MAP_REG5 Register \(Offset = 414h\) \[reset = X\]: \[0\]](#)

15.7.38 ICSS_INTC_CH_MAP_REG6 Register (Offset = 418h) [reset = X]

ICSS_INTC_CH_MAP_REG6 is shown in Figure 15-168 and described in Table 15-516.

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Interrupt Channel Map Register for 24 to 24+3

Table 15-515. ICSS_INTC_CH_MAP_REG6 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0418h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0418h

Figure 15-168. ICSS_INTC_CH_MAP_REG6 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_27				RESERVED				CH_MAP_26			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_25				RESERVED				CH_MAP_24			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-516. ICSS_INTC_CH_MAP_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_27	R/W	0h	Interrupt Channel Map for intr_in[27]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_26	R/W	0h	Interrupt Channel Map for intr_in[26]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_25	R/W	0h	Interrupt Channel Map for intr_in[25]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_24	R/W	0h	Interrupt Channel Map for intr_in[24]

Table 15-517. Register Call Summary for ICSS_INTC_CH_MAP_REG6

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_CH_MAP_REG6 Register \(Offset = 418h\) \[reset = X\]: \[0\]](#)

15.7.39 ICSS_INTC_CH_MAP_REG7 Register (Offset = 41Ch) [reset = X]

ICSS_INTC_CH_MAP_REG7 is shown in Figure 15-169 and described in Table 15-519.

Return to [Summary Table](#).

Interrupt Channel Map Register for 28 to 28+3

Table 15-518. ICSS_INTC_CH_MAP_REG7 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 041Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 041Ch

Figure 15-169. ICSS_INTC_CH_MAP_REG7 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_31				RESERVED				CH_MAP_30			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_29				RESERVED				CH_MAP_28			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-519. ICSS_INTC_CH_MAP_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_31	R/W	0h	Interrupt Channel Map for intr_in[31]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_30	R/W	0h	Interrupt Channel Map for intr_in[30]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_29	R/W	0h	Interrupt Channel Map for intr_in[29]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_28	R/W	0h	Interrupt Channel Map for intr_in[28]

Table 15-520. Register Call Summary for ICSS_INTC_CH_MAP_REG7

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_CH_MAP_REG7 Register \(Offset = 41Ch\) \[reset = X\]: \[0\]](#)

15.7.40 ICSS_INTC_CH_MAP_REG8 Register (Offset = 420h) [reset = X]

ICSS_INTC_CH_MAP_REG8 is shown in Figure 15-170 and described in Table 15-522.

Return to [Summary Table](#).

Interrupt Channel Map Register for 32 to 32+3

Table 15-521. ICSS_INTC_CH_MAP_REG8 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0420h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0420h

Figure 15-170. ICSS_INTC_CH_MAP_REG8 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_35				RESERVED				CH_MAP_34			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_33				RESERVED				CH_MAP_32			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-522. ICSS_INTC_CH_MAP_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_35	R/W	0h	Interrupt Channel Map for intr_in[35]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_34	R/W	0h	Interrupt Channel Map for intr_in[34]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_33	R/W	0h	Interrupt Channel Map for intr_in[33]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_32	R/W	0h	Interrupt Channel Map for intr_in[32]

Table 15-523. Register Call Summary for ICSS_INTC_CH_MAP_REG8

PRU_ICSS_INTC_INTC Registers

- [ICSS_INTC_CH_MAP_REG8 Register \(Offset = 420h\) \[reset = X\]: \[0\]](#)
- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)

15.7.41 ICSS_INTC_CH_MAP_REG9 Register (Offset = 424h) [reset = X]

ICSS_INTC_CH_MAP_REG9 is shown in Figure 15-171 and described in Table 15-525.

Return to [Summary Table](#).

Interrupt Channel Map Register for 36 to 36+3

Table 15-524. ICSS_INTC_CH_MAP_REG9 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0424h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0424h

Figure 15-171. ICSS_INTC_CH_MAP_REG9 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_39				RESERVED				CH_MAP_38			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_37				RESERVED				CH_MAP_36			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-525. ICSS_INTC_CH_MAP_REG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_39	R/W	0h	Interrupt Channel Map for intr_in[39]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_38	R/W	0h	Interrupt Channel Map for intr_in[38]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_37	R/W	0h	Interrupt Channel Map for intr_in[37]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_36	R/W	0h	Interrupt Channel Map for intr_in[36]

Table 15-526. Register Call Summary for ICSS_INTC_CH_MAP_REG9

PRU_ICSS_INTC_INTC Registers

- [ICSS_INTC_CH_MAP_REG9 Register \(Offset = 424h\) \[reset = X\]: \[0\]](#)
- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)

15.7.42 ICSS_INTC_CH_MAP_REG10 Register (Offset = 428h) [reset = X]

ICSS_INTC_CH_MAP_REG10 is shown in [Figure 15-172](#) and described in [Table 15-528](#).

[Return to Summary Table.](#)

Interrupt Channel Map Register for 40 to 40+3

Table 15-527. ICSS_INTC_CH_MAP_REG10 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0428h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0428h

Figure 15-172. ICSS_INTC_CH_MAP_REG10 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_43				RESERVED				CH_MAP_42			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_41				RESERVED				CH_MAP_40			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-528. ICSS_INTC_CH_MAP_REG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_43	R/W	0h	Interrupt Channel Map for intr_in[43]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_42	R/W	0h	Interrupt Channel Map for intr_in[42]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_41	R/W	0h	Interrupt Channel Map for intr_in[41]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_40	R/W	0h	Interrupt Channel Map for intr_in[40]

Table 15-529. Register Call Summary for ICSS_INTC_CH_MAP_REG10

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_CH_MAP_REG10 Register \(Offset = 428h\) \[reset = X\]: \[0\]](#)

15.7.43 ICSS_INTC_CH_MAP_REG11 Register (Offset = 42Ch) [reset = X]

ICSS_INTC_CH_MAP_REG11 is shown in Figure 15-173 and described in Table 15-531.

Return to [Summary Table](#).

Interrupt Channel Map Register for 44 to 44+3

Table 15-530. ICSS_INTC_CH_MAP_REG11 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 042Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 042Ch

Figure 15-173. ICSS_INTC_CH_MAP_REG11 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_47				RESERVED				CH_MAP_46			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_45				RESERVED				CH_MAP_44			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-531. ICSS_INTC_CH_MAP_REG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_47	R/W	0h	Interrupt Channel Map for intr_in[47]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_46	R/W	0h	Interrupt Channel Map for intr_in[46]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_45	R/W	0h	Interrupt Channel Map for intr_in[45]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_44	R/W	0h	Interrupt Channel Map for intr_in[44]

Table 15-532. Register Call Summary for ICSS_INTC_CH_MAP_REG11

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_CH_MAP_REG11 Register \(Offset = 42Ch\) \[reset = X\]: \[0\]](#)

15.7.44 ICSS_INTC_CH_MAP_REG12 Register (Offset = 430h) [reset = X]

ICSS_INTC_CH_MAP_REG12 is shown in [Figure 15-174](#) and described in [Table 15-534](#).

Return to [Summary Table](#).

Interrupt Channel Map Register for 48 to 48+3

Table 15-533. ICSS_INTC_CH_MAP_REG12 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0430h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0430h

Figure 15-174. ICSS_INTC_CH_MAP_REG12 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_51				RESERVED				CH_MAP_50			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_49				RESERVED				CH_MAP_48			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-534. ICSS_INTC_CH_MAP_REG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_51	R/W	0h	Interrupt Channel Map for intr_in[51]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_50	R/W	0h	Interrupt Channel Map for intr_in[50]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_49	R/W	0h	Interrupt Channel Map for intr_in[49]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_48	R/W	0h	Interrupt Channel Map for intr_in[48]

Table 15-535. Register Call Summary for ICSS_INTC_CH_MAP_REG12

PRU_ICSS_INTC_INTC Registers

- [ICSS_INTC_CH_MAP_REG12 Register \(Offset = 430h\) \[reset = X\]: \[0\]](#)
- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)

15.7.45 ICSS_INTC_CH_MAP_REG13 Register (Offset = 434h) [reset = X]

ICSS_INTC_CH_MAP_REG13 is shown in Figure 15-175 and described in Table 15-537.

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Interrupt Channel Map Register for 52 to 52+3

Table 15-536. ICSS_INTC_CH_MAP_REG13 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0434h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0434h

Figure 15-175. ICSS_INTC_CH_MAP_REG13 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_55				RESERVED				CH_MAP_54			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_53				RESERVED				CH_MAP_52			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-537. ICSS_INTC_CH_MAP_REG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_55	R/W	0h	Interrupt Channel Map for intr_in[55]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_54	R/W	0h	Interrupt Channel Map for intr_in[54]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_53	R/W	0h	Interrupt Channel Map for intr_in[53]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_52	R/W	0h	Interrupt Channel Map for intr_in[52]

Table 15-538. Register Call Summary for ICSS_INTC_CH_MAP_REG13

PRU_ICSS_INTC_INTC Registers

- [ICSS_INTC_CH_MAP_REG13 Register \(Offset = 434h\) \[reset = X\]: \[0\]](#)
- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)

15.7.46 ICSS_INTC_CH_MAP_REG14 Register (Offset = 438h) [reset = X]

ICSS_INTC_CH_MAP_REG14 is shown in [Figure 15-176](#) and described in [Table 15-540](#).

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Interrupt Channel Map Register for 56 to 56+3

Table 15-539. ICSS_INTC_CH_MAP_REG14 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0438h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0438h

Figure 15-176. ICSS_INTC_CH_MAP_REG14 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_59				RESERVED				CH_MAP_58			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_57				RESERVED				CH_MAP_56			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-540. ICSS_INTC_CH_MAP_REG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_59	R/W	0h	Interrupt Channel Map for intr_in[59]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_58	R/W	0h	Interrupt Channel Map for intr_in[58]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_57	R/W	0h	Interrupt Channel Map for intr_in[57]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_56	R/W	0h	Interrupt Channel Map for intr_in[56]

Table 15-541. Register Call Summary for ICSS_INTC_CH_MAP_REG14

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_CH_MAP_REG14 Register \(Offset = 438h\) \[reset = X\]: \[0\]](#)

15.7.47 ICSS_INTC_CH_MAP_REG15 Register (Offset = 43Ch) [reset = X]

ICSS_INTC_CH_MAP_REG15 is shown in [Figure 15-177](#) and described in [Table 15-543](#).

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Interrupt Channel Map Register for 60 to 60+3

Table 15-542. ICSS_INTC_CH_MAP_REG15 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 043Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 043Ch

Figure 15-177. ICSS_INTC_CH_MAP_REG15 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_63				RESERVED				CH_MAP_62			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_61				RESERVED				CH_MAP_60			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-543. ICSS_INTC_CH_MAP_REG15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_63	R/W	0h	Interrupt Channel Map for intr_in[63]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_62	R/W	0h	Interrupt Channel Map for intr_in[62]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_61	R/W	0h	Interrupt Channel Map for intr_in[61]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_60	R/W	0h	Interrupt Channel Map for intr_in[60]

Table 15-544. Register Call Summary for ICSS_INTC_CH_MAP_REG15

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_CH_MAP_REG15 Register \(Offset = 43Ch\) \[reset = X\]: \[0\]](#)

15.7.48 ICSS_INTC_CH_MAP_REG16 Register (Offset = 440h) [reset = X]

ICSS_INTC_CH_MAP_REG16 is shown in [Figure 15-178](#) and described in [Table 15-546](#).

Return to [Summary Table](#).

Interrupt Channel Map Register for 64 to 64+3

Table 15-545. ICSS_INTC_CH_MAP_REG16 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0440h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0440h

Figure 15-178. ICSS_INTC_CH_MAP_REG16 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_67				RESERVED				CH_MAP_66			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_65				RESERVED				CH_MAP_64			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-546. ICSS_INTC_CH_MAP_REG16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_67	R/W	0h	Interrupt Channel Map for slv_events_in[3]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_66	R/W	0h	Interrupt Channel Map for slv_events_in[2]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_65	R/W	0h	Interrupt Channel Map for slv_events_in[1]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_64	R/W	0h	Interrupt Channel Map for slv_events_in[0]

Table 15-547. Register Call Summary for ICSS_INTC_CH_MAP_REG16

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_CH_MAP_REG16 Register \(Offset = 440h\) \[reset = X\]: \[0\]](#)

15.7.49 ICSS_INTC_CH_MAP_REG17 Register (Offset = 444h) [reset = X]

ICSS_INTC_CH_MAP_REG17 is shown in [Figure 15-179](#) and described in [Table 15-549](#).

Return to [Summary Table](#).

Interrupt Channel Map Register for 68 to 68+3

Table 15-548. ICSS_INTC_CH_MAP_REG17 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0444h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0444h

Figure 15-179. ICSS_INTC_CH_MAP_REG17 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_71				RESERVED				CH_MAP_70			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_69				RESERVED				CH_MAP_68			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-549. ICSS_INTC_CH_MAP_REG17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_71	R/W	0h	Interrupt Channel Map for slv_events_in[7]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_70	R/W	0h	Interrupt Channel Map for slv_events_in[6]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_69	R/W	0h	Interrupt Channel Map for slv_events_in[5]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_68	R/W	0h	Interrupt Channel Map for slv_events_in[4]

Table 15-550. Register Call Summary for ICSS_INTC_CH_MAP_REG17

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_CH_MAP_REG17 Register \(Offset = 444h\) \[reset = X\]: \[0\]](#)

15.7.50 ICSS_INTC_CH_MAP_REG18 Register (Offset = 448h) [reset = X]

ICSS_INTC_CH_MAP_REG18 is shown in [Figure 15-180](#) and described in [Table 15-552](#).

Return to [Summary Table](#).

Interrupt Channel Map Register for 72 to 72+3

Table 15-551. ICSS_INTC_CH_MAP_REG18 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0448h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0448h

Figure 15-180. ICSS_INTC_CH_MAP_REG18 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_75				RESERVED				CH_MAP_74			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_73				RESERVED				CH_MAP_72			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-552. ICSS_INTC_CH_MAP_REG18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_75	R/W	0h	Interrupt Channel Map for slv_events_in[11]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_74	R/W	0h	Interrupt Channel Map for slv_events_in[10]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_73	R/W	0h	Interrupt Channel Map for slv_events_in[9]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_72	R/W	0h	Interrupt Channel Map for slv_events_in[8]

Table 15-553. Register Call Summary for ICSS_INTC_CH_MAP_REG18

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_CH_MAP_REG18 Register \(Offset = 448h\) \[reset = X\]: \[0\]](#)

15.7.51 ICSS_INTC_CH_MAP_REG19 Register (Offset = 44Ch) [reset = X]

ICSS_INTC_CH_MAP_REG19 is shown in [Figure 15-181](#) and described in [Table 15-555](#).

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Interrupt Channel Map Register for 76 to 76+3

Table 15-554. ICSS_INTC_CH_MAP_REG19 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 044Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 044Ch

Figure 15-181. ICSS_INTC_CH_MAP_REG19 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_79				RESERVED				CH_MAP_78			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_77				RESERVED				CH_MAP_76			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-555. ICSS_INTC_CH_MAP_REG19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_79	R/W	0h	Interrupt Channel Map for slv_events_in[15]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_78	R/W	0h	Interrupt Channel Map for slv_events_in[14]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_77	R/W	0h	Interrupt Channel Map for slv_events_in[13]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_76	R/W	0h	Interrupt Channel Map for slv_events_in[12]

Table 15-556. Register Call Summary for ICSS_INTC_CH_MAP_REG19

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_CH_MAP_REG19 Register \(Offset = 44Ch\) \[reset = X\]: \[0\]](#)

15.7.52 ICSS_INTC_CH_MAP_REG20 Register (Offset = 450h) [reset = X]

ICSS_INTC_CH_MAP_REG20 is shown in [Figure 15-182](#) and described in [Table 15-558](#).

[Return to Summary Table.](#)

Interrupt Channel Map Register for 80 to 80+3

Table 15-557. ICSS_INTC_CH_MAP_REG20 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0450h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0450h

Figure 15-182. ICSS_INTC_CH_MAP_REG20 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_83				RESERVED				CH_MAP_82			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_81				RESERVED				CH_MAP_80			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-558. ICSS_INTC_CH_MAP_REG20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_83	R/W	0h	Interrupt Channel Map for slv_events_in[19]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_82	R/W	0h	Interrupt Channel Map for slv_events_in[18]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_81	R/W	0h	Interrupt Channel Map for slv_events_in[17]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_80	R/W	0h	Interrupt Channel Map for slv_events_in[16]

Table 15-559. Register Call Summary for ICSS_INTC_CH_MAP_REG20

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_CH_MAP_REG20 Register \(Offset = 450h\) \[reset = X\]: \[0\]](#)

15.7.53 ICSS_INTC_CH_MAP_REG21 Register (Offset = 454h) [reset = X]

ICSS_INTC_CH_MAP_REG21 is shown in [Figure 15-183](#) and described in [Table 15-561](#).

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Interrupt Channel Map Register for 84 to 84+3

Table 15-560. ICSS_INTC_CH_MAP_REG21 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTIC_SLV	0B02 0454h
PRU_ICSSG1_PR1_ICSS_INTC_INTIC_SLV	0B12 0454h

Figure 15-183. ICSS_INTC_CH_MAP_REG21 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_87				RESERVED				CH_MAP_86			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_85				RESERVED				CH_MAP_84			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-561. ICSS_INTC_CH_MAP_REG21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_87	R/W	0h	Interrupt Channel Map for slv_events_in[23]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_86	R/W	0h	Interrupt Channel Map for slv_events_in[22]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_85	R/W	0h	Interrupt Channel Map for slv_events_in[21]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_84	R/W	0h	Interrupt Channel Map for slv_events_in[20]

Table 15-562. Register Call Summary for ICSS_INTC_CH_MAP_REG21

PRU_ICSS_INTC_INTIC Registers

- [PRU_ICSS_INTC_INTIC Registers: \[0\]](#)
- [ICSS_INTC_CH_MAP_REG21 Register \(Offset = 454h\) \[reset = X\]: \[0\]](#)

15.7.54 ICSS_INTC_CH_MAP_REG22 Register (Offset = 458h) [reset = X]

ICSS_INTC_CH_MAP_REG22 is shown in [Figure 15-184](#) and described in [Table 15-564](#).

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Interrupt Channel Map Register for 88 to 88+3

Table 15-563. ICSS_INTC_CH_MAP_REG22 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0458h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0458h

Figure 15-184. ICSS_INTC_CH_MAP_REG22 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_91				RESERVED				CH_MAP_90			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_89				RESERVED				CH_MAP_88			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-564. ICSS_INTC_CH_MAP_REG22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_91	R/W	0h	Interrupt Channel Map for slv_events_in[27]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_90	R/W	0h	Interrupt Channel Map for slv_events_in[26]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_89	R/W	0h	Interrupt Channel Map for slv_events_in[25]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_88	R/W	0h	Interrupt Channel Map for slv_events_in[24]

Table 15-565. Register Call Summary for ICSS_INTC_CH_MAP_REG22

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_CH_MAP_REG22 Register \(Offset = 458h\) \[reset = X\]: \[0\]](#)

15.7.55 ICSS_INTC_CH_MAP_REG23 Register (Offset = 45Ch) [reset = X]

ICSS_INTC_CH_MAP_REG23 is shown in [Figure 15-185](#) and described in [Table 15-567](#).

Return to [Summary Table](#).

Interrupt Channel Map Register for 92 to 92+3

Table 15-566. ICSS_INTC_CH_MAP_REG23 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 045Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 045Ch

Figure 15-185. ICSS_INTC_CH_MAP_REG23 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_95				RESERVED				CH_MAP_94			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_93				RESERVED				CH_MAP_92			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-567. ICSS_INTC_CH_MAP_REG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_95	R/W	0h	Interrupt Channel Map for slv_events_in[31]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_94	R/W	0h	Interrupt Channel Map for slv_events_in[30]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_93	R/W	0h	Interrupt Channel Map for slv_events_in[29]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_92	R/W	0h	Interrupt Channel Map for slv_events_in[28]

Table 15-568. Register Call Summary for ICSS_INTC_CH_MAP_REG23

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_CH_MAP_REG23 Register \(Offset = 45Ch\) \[reset = X\]: \[0\]](#)

15.7.56 ICSS_INTC_CH_MAP_REG24 Register (Offset = 460h) [reset = X]

ICSS_INTC_CH_MAP_REG24 is shown in [Figure 15-186](#) and described in [Table 15-570](#).

Return to [Summary Table](#).

Interrupt Channel Map Register for 96 to 96+3

Table 15-569. ICSS_INTC_CH_MAP_REG24 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0460h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0460h

Figure 15-186. ICSS_INTC_CH_MAP_REG24 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_99				RESERVED				CH_MAP_98			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_97				RESERVED				CH_MAP_96			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-570. ICSS_INTC_CH_MAP_REG24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_99	R/W	0h	Interrupt Channel Map for slv_events_in[35]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_98	R/W	0h	Interrupt Channel Map for slv_events_in[34]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_97	R/W	0h	Interrupt Channel Map for slv_events_in[33]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_96	R/W	0h	Interrupt Channel Map for slv_events_in[32]

Table 15-571. Register Call Summary for ICSS_INTC_CH_MAP_REG24

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_CH_MAP_REG24 Register \(Offset = 460h\) \[reset = X\]: \[0\]](#)

15.7.57 ICSS_INTC_CH_MAP_REG25 Register (Offset = 464h) [reset = X]

ICSS_INTC_CH_MAP_REG25 is shown in Figure 15-187 and described in Table 15-573.

Return to [Summary Table](#).

Interrupt Channel Map Register for 100 to 100+3

Table 15-572. ICSS_INTC_CH_MAP_REG25 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTIC_SLV	0B02 0464h
PRU_ICSSG1_PR1_ICSS_INTC_INTIC_SLV	0B12 0464h

Figure 15-187. ICSS_INTC_CH_MAP_REG25 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_103				RESERVED				CH_MAP_102			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_101				RESERVED				CH_MAP_100			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-573. ICSS_INTC_CH_MAP_REG25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_103	R/W	0h	Interrupt Channel Map for slv_events_in[39]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_102	R/W	0h	Interrupt Channel Map for slv_events_in[38]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_101	R/W	0h	Interrupt Channel Map for slv_events_in[37]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_100	R/W	0h	Interrupt Channel Map for slv_events_in[36]

Table 15-574. Register Call Summary for ICSS_INTC_CH_MAP_REG25

PRU_ICSS_INTC_INTIC Registers

- [PRU_ICSS_INTC_INTIC Registers: \[0\]](#)
- [ICSS_INTC_CH_MAP_REG25 Register \(Offset = 464h\) \[reset = X\]: \[0\]](#)

15.7.58 ICSS_INTC_CH_MAP_REG26 Register (Offset = 468h) [reset = X]

ICSS_INTC_CH_MAP_REG26 is shown in [Figure 15-188](#) and described in [Table 15-576](#).

Return to [Summary Table](#).

Interrupt Channel Map Register for 104 to 104+3

Table 15-575. ICSS_INTC_CH_MAP_REG26 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0468h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0468h

Figure 15-188. ICSS_INTC_CH_MAP_REG26 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_107				RESERVED				CH_MAP_106			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_105				RESERVED				CH_MAP_104			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-576. ICSS_INTC_CH_MAP_REG26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_107	R/W	0h	Interrupt Channel Map for slv_events_in[43]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_106	R/W	0h	Interrupt Channel Map for slv_events_in[42]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_105	R/W	0h	Interrupt Channel Map for slv_events_in[41]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_104	R/W	0h	Interrupt Channel Map for slv_events_in[40]

Table 15-577. Register Call Summary for ICSS_INTC_CH_MAP_REG26

PRU_ICSS_INTC_INTC Registers

- [ICSS_INTC_CH_MAP_REG26 Register \(Offset = 468h\) \[reset = X\]: \[0\]](#)
- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)

15.7.59 ICSS_INTC_CH_MAP_REG27 Register (Offset = 46Ch) [reset = X]

ICSS_INTC_CH_MAP_REG27 is shown in [Figure 15-189](#) and described in [Table 15-579](#).

Return to [Summary Table](#).

Interrupt Channel Map Register for 108 to 108+3

Table 15-578. ICSS_INTC_CH_MAP_REG27 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 046Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 046Ch

Figure 15-189. ICSS_INTC_CH_MAP_REG27 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_111				RESERVED				CH_MAP_110			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_109				RESERVED				CH_MAP_108			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-579. ICSS_INTC_CH_MAP_REG27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_111	R/W	0h	Interrupt Channel Map for slv_events_in[47]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_110	R/W	0h	Interrupt Channel Map for slv_events_in[46]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_109	R/W	0h	Interrupt Channel Map for slv_events_in[45]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_108	R/W	0h	Interrupt Channel Map for slv_events_in[44]

Table 15-580. Register Call Summary for ICSS_INTC_CH_MAP_REG27

PRU_ICSS_INTC_INTC Registers

- [ICSS_INTC_CH_MAP_REG27 Register \(Offset = 46Ch\) \[reset = X\]: \[0\]](#)
- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)

15.7.60 ICSS_INTC_CH_MAP_REG28 Register (Offset = 470h) [reset = X]

ICSS_INTC_CH_MAP_REG28 is shown in [Figure 15-190](#) and described in [Table 15-582](#).

Return to [Summary Table](#).

Interrupt Channel Map Register for 112 to 112+3

Table 15-581. ICSS_INTC_CH_MAP_REG28 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0470h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0470h

Figure 15-190. ICSS_INTC_CH_MAP_REG28 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_115				RESERVED				CH_MAP_114			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_113				RESERVED				CH_MAP_112			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-582. ICSS_INTC_CH_MAP_REG28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_115	R/W	0h	Interrupt Channel Map for slv_events_in[51]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_114	R/W	0h	Interrupt Channel Map for slv_events_in[50]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_113	R/W	0h	Interrupt Channel Map for slv_events_in[49]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_112	R/W	0h	Interrupt Channel Map for slv_events_in[48]

Table 15-583. Register Call Summary for ICSS_INTC_CH_MAP_REG28

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_CH_MAP_REG28 Register \(Offset = 470h\) \[reset = X\]: \[0\]](#)

15.7.61 ICSS_INTC_CH_MAP_REG29 Register (Offset = 474h) [reset = X]

ICSS_INTC_CH_MAP_REG29 is shown in [Figure 15-191](#) and described in [Table 15-585](#).

Return to [Summary Table](#).

Interrupt Channel Map Register for 116 to 116+3

Table 15-584. ICSS_INTC_CH_MAP_REG29 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0474h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0474h

Figure 15-191. ICSS_INTC_CH_MAP_REG29 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_119				RESERVED				CH_MAP_118			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_117				RESERVED				CH_MAP_116			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-585. ICSS_INTC_CH_MAP_REG29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_119	R/W	0h	Interrupt Channel Map for slv_events_in[55]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_118	R/W	0h	Interrupt Channel Map for slv_events_in[54]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_117	R/W	0h	Interrupt Channel Map for slv_events_in[53]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_116	R/W	0h	Interrupt Channel Map for slv_events_in[52]

Table 15-586. Register Call Summary for ICSS_INTC_CH_MAP_REG29

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_CH_MAP_REG29 Register \(Offset = 474h\) \[reset = X\]: \[0\]](#)

15.7.62 ICSS_INTC_CH_MAP_REG30 Register (Offset = 478h) [reset = X]

ICSS_INTC_CH_MAP_REG30 is shown in [Figure 15-192](#) and described in [Table 15-588](#).

Return to [Summary Table](#).

Interrupt Channel Map Register for 120 to 120+3

Table 15-587. ICSS_INTC_CH_MAP_REG30 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0478h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0478h

Figure 15-192. ICSS_INTC_CH_MAP_REG30 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_123				RESERVED				CH_MAP_122			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_121				RESERVED				CH_MAP_120			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-588. ICSS_INTC_CH_MAP_REG30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_123	R/W	0h	Interrupt Channel Map for slv_events_in[59]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_122	R/W	0h	Interrupt Channel Map for slv_events_in[58]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_121	R/W	0h	Interrupt Channel Map for slv_events_in[57]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_120	R/W	0h	Interrupt Channel Map for slv_events_in[56]

Table 15-589. Register Call Summary for ICSS_INTC_CH_MAP_REG30

PRU_ICSS_INTC_INTC Registers
PRU_ICSS_INTC_INTC Registers: [0] ICSS_INTC_CH_MAP_REG30 Register (Offset = 478h) [reset = X]: [0]

15.7.63 ICSS_INTC_CH_MAP_REG31 Register (Offset = 47Ch) [reset = X]

ICSS_INTC_CH_MAP_REG31 is shown in [Figure 15-193](#) and described in [Table 15-591](#).

Return to [Summary Table](#).

Interrupt Channel Map Register for 124 to 124+3

Table 15-590. ICSS_INTC_CH_MAP_REG31 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 047Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 047Ch

Figure 15-193. ICSS_INTC_CH_MAP_REG31 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_127				RESERVED				CH_MAP_126			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_125				RESERVED				CH_MAP_124			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-591. ICSS_INTC_CH_MAP_REG31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_127	R/W	0h	Interrupt Channel Map for slv_events_in[63]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_126	R/W	0h	Interrupt Channel Map for slv_events_in[62]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_125	R/W	0h	Interrupt Channel Map for slv_events_in[61]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_124	R/W	0h	Interrupt Channel Map for slv_events_in[60]

Table 15-592. Register Call Summary for ICSS_INTC_CH_MAP_REG31

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_CH_MAP_REG31 Register \(Offset = 47Ch\) \[reset = X\]: \[0\]](#)

15.7.64 ICSS_INTC_CH_MAP_REG32 Register (Offset = 480h) [reset = X]

ICSS_INTC_CH_MAP_REG32 is shown in [Figure 15-194](#) and described in [Table 15-594](#).

Return to [Summary Table](#).

Interrupt Channel Map Register for 128 to 128+3

Table 15-593. ICSS_INTC_CH_MAP_REG32 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0480h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0480h

Figure 15-194. ICSS_INTC_CH_MAP_REG32 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_131				RESERVED				CH_MAP_130			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_129				RESERVED				CH_MAP_128			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-594. ICSS_INTC_CH_MAP_REG32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_131	R/W	0h	Interrupt Channel Map for slv_events_in[67]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_130	R/W	0h	Interrupt Channel Map for slv_events_in[66]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_129	R/W	0h	Interrupt Channel Map for slv_events_in[65]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_128	R/W	0h	Interrupt Channel Map for slv_events_in[64]

Table 15-595. Register Call Summary for ICSS_INTC_CH_MAP_REG32

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_CH_MAP_REG32 Register \(Offset = 480h\) \[reset = X\]: \[0\]](#)

15.7.65 ICSS_INTC_CH_MAP_REG33 Register (Offset = 484h) [reset = X]

ICSS_INTC_CH_MAP_REG33 is shown in [Figure 15-195](#) and described in [Table 15-597](#).

Return to [Summary Table](#).

Interrupt Channel Map Register for 132 to 132+3

Table 15-596. ICSS_INTC_CH_MAP_REG33 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0484h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0484h

Figure 15-195. ICSS_INTC_CH_MAP_REG33 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_135				RESERVED				CH_MAP_134			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_133				RESERVED				CH_MAP_132			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-597. ICSS_INTC_CH_MAP_REG33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_135	R/W	0h	Interrupt Channel Map for slv_events_in[71]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_134	R/W	0h	Interrupt Channel Map for slv_events_in[70]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_133	R/W	0h	Interrupt Channel Map for slv_events_in[69]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_132	R/W	0h	Interrupt Channel Map for slv_events_in[68]

Table 15-598. Register Call Summary for ICSS_INTC_CH_MAP_REG33

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_CH_MAP_REG33 Register \(Offset = 484h\) \[reset = X\]: \[0\]](#)

15.7.66 ICSS_INTC_CH_MAP_REG34 Register (Offset = 488h) [reset = X]

ICSS_INTC_CH_MAP_REG34 is shown in [Figure 15-196](#) and described in [Table 15-600](#).

Return to [Summary Table](#).

Interrupt Channel Map Register for 136 to 136+3

Table 15-599. ICSS_INTC_CH_MAP_REG34 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0488h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0488h

Figure 15-196. ICSS_INTC_CH_MAP_REG34 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_139				RESERVED				CH_MAP_138			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_137				RESERVED				CH_MAP_136			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-600. ICSS_INTC_CH_MAP_REG34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_139	R/W	0h	Interrupt Channel Map for slv_events_in[75]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_138	R/W	0h	Interrupt Channel Map for slv_events_in[74]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_137	R/W	0h	Interrupt Channel Map for slv_events_in[73]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_136	R/W	0h	Interrupt Channel Map for slv_events_in[72]

Table 15-601. Register Call Summary for ICSS_INTC_CH_MAP_REG34

PRU_ICSS_INTC_INTC Registers

- [ICSS_INTC_CH_MAP_REG34 Register \(Offset = 488h\) \[reset = X\]: \[0\]](#)
- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)

15.7.67 ICSS_INTC_CH_MAP_REG35 Register (Offset = 48Ch) [reset = X]

ICSS_INTC_CH_MAP_REG35 is shown in [Figure 15-197](#) and described in [Table 15-603](#).

Return to [Summary Table](#).

Interrupt Channel Map Register for 140 to 140+3

Table 15-602. ICSS_INTC_CH_MAP_REG35 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 048Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 048Ch

Figure 15-197. ICSS_INTC_CH_MAP_REG35 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_143				RESERVED				CH_MAP_142			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_141				RESERVED				CH_MAP_140			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-603. ICSS_INTC_CH_MAP_REG35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_143	R/W	0h	Interrupt Channel Map for slv_events_in[79]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_142	R/W	0h	Interrupt Channel Map for slv_events_in[78]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_141	R/W	0h	Interrupt Channel Map for slv_events_in[77]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_140	R/W	0h	Interrupt Channel Map for slv_events_in[76]

Table 15-604. Register Call Summary for ICSS_INTC_CH_MAP_REG35

PRU_ICSS_INTC_INTC Registers

- [ICSS_INTC_CH_MAP_REG35 Register \(Offset = 48Ch\) \[reset = X\]: \[0\]](#)
- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)

15.7.68 ICSS_INTC_CH_MAP_REG36 Register (Offset = 490h) [reset = X]

ICSS_INTC_CH_MAP_REG36 is shown in [Figure 15-198](#) and described in [Table 15-606](#).

Return to [Summary Table](#).

Interrupt Channel Map Register for 144 to 144+3

Table 15-605. ICSS_INTC_CH_MAP_REG36 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTIC_SLV	0B02 0490h
PRU_ICSSG1_PR1_ICSS_INTC_INTIC_SLV	0B12 0490h

Figure 15-198. ICSS_INTC_CH_MAP_REG36 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_147				RESERVED				CH_MAP_146			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_145				RESERVED				CH_MAP_144			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-606. ICSS_INTC_CH_MAP_REG36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_147	R/W	0h	Interrupt Channel Map for slv_events_in[83]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_146	R/W	0h	Interrupt Channel Map for slv_events_in[82]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_145	R/W	0h	Interrupt Channel Map for slv_events_in[81]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_144	R/W	0h	Interrupt Channel Map for slv_events_in[80]

Table 15-607. Register Call Summary for ICSS_INTC_CH_MAP_REG36

PRU_ICSS_INTC_INTIC Registers

- [PRU_ICSS_INTC_INTIC Registers: \[0\]](#)
- [ICSS_INTC_CH_MAP_REG36 Register \(Offset = 490h\) \[reset = X\]: \[0\]](#)

15.7.69 ICSS_INTC_CH_MAP_REG37 Register (Offset = 494h) [reset = X]

ICSS_INTC_CH_MAP_REG37 is shown in [Figure 15-199](#) and described in [Table 15-609](#).

Return to [Summary Table](#).

Interrupt Channel Map Register for 148 to 148+3

Table 15-608. ICSS_INTC_CH_MAP_REG37 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0494h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0494h

Figure 15-199. ICSS_INTC_CH_MAP_REG37 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_151				RESERVED				CH_MAP_150			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_149				RESERVED				CH_MAP_148			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-609. ICSS_INTC_CH_MAP_REG37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_151	R/W	0h	Interrupt Channel Map for slv_events_in[87]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_150	R/W	0h	Interrupt Channel Map for slv_events_in[86]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_149	R/W	0h	Interrupt Channel Map for slv_events_in[85]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_148	R/W	0h	Interrupt Channel Map for slv_events_in[84]

Table 15-610. Register Call Summary for ICSS_INTC_CH_MAP_REG37

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_CH_MAP_REG37 Register \(Offset = 494h\) \[reset = X\]: \[0\]](#)

15.7.70 ICSS_INTC_CH_MAP_REG38 Register (Offset = 498h) [reset = X]

ICSS_INTC_CH_MAP_REG38 is shown in [Figure 15-200](#) and described in [Table 15-612](#).

Return to [Summary Table](#).

Interrupt Channel Map Register for 152 to 152+3

Table 15-611. ICSS_INTC_CH_MAP_REG38 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0498h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0498h

Figure 15-200. ICSS_INTC_CH_MAP_REG38 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_155				RESERVED				CH_MAP_154			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_153				RESERVED				CH_MAP_152			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-612. ICSS_INTC_CH_MAP_REG38 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_155	R/W	0h	Interrupt Channel Map for slv_events_in[91]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_154	R/W	0h	Interrupt Channel Map for slv_events_in[90]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_153	R/W	0h	Interrupt Channel Map for slv_events_in[89]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_152	R/W	0h	Interrupt Channel Map for slv_events_in[88]

Table 15-613. Register Call Summary for ICSS_INTC_CH_MAP_REG38

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_CH_MAP_REG38 Register \(Offset = 498h\) \[reset = X\]: \[0\]](#)

15.7.71 ICSS_INTC_CH_MAP_REG39 Register (Offset = 49Ch) [reset = X]

ICSS_INTC_CH_MAP_REG39 is shown in [Figure 15-201](#) and described in [Table 15-615](#).

Return to [Summary Table](#).

Interrupt Channel Map Register for 156 to 156+3

Table 15-614. ICSS_INTC_CH_MAP_REG39 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 049Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 049Ch

Figure 15-201. ICSS_INTC_CH_MAP_REG39 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_159				RESERVED				CH_MAP_158			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_157				RESERVED				CH_MAP_156			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-615. ICSS_INTC_CH_MAP_REG39 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	CH_MAP_159	R/W	0h	Interrupt Channel Map for slv_events_in[95]
23-21	RESERVED	R/W	X	
20-16	CH_MAP_158	R/W	0h	Interrupt Channel Map for slv_events_in[94]
15-13	RESERVED	R/W	X	
12-8	CH_MAP_157	R/W	0h	Interrupt Channel Map for slv_events_in[93]
7-5	RESERVED	R/W	X	
4-0	CH_MAP_156	R/W	0h	Interrupt Channel Map for slv_events_in[92]

Table 15-616. Register Call Summary for ICSS_INTC_CH_MAP_REG39

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_CH_MAP_REG39 Register \(Offset = 49Ch\) \[reset = X\]: \[0\]](#)

15.7.72 ICSS_INTC_HINT_MAP_REG0 Register (Offset = 800h) [reset = X]

ICSS_INTC_HINT_MAP_REG0 is shown in [Figure 15-202](#) and described in [Table 15-618](#).

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Host Interrupt Map Register for 0 to 0+3

Table 15-617. ICSS_INTC_HINT_MAP_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0800h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0800h

Figure 15-202. ICSS_INTC_HINT_MAP_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				HINT_MAP_3				RESERVED				HINT_MAP_2			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				HINT_MAP_1				RESERVED				HINT_MAP_0			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-618. ICSS_INTC_HINT_MAP_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	HINT_MAP_3	R/W	0h	Host Interrupt Map for Channel 3
23-21	RESERVED	R/W	X	
20-16	HINT_MAP_2	R/W	0h	Host Interrupt Map for Channel 2
15-13	RESERVED	R/W	X	
12-8	HINT_MAP_1	R/W	0h	Host Interrupt Map for Channel 1
7-5	RESERVED	R/W	X	
4-0	HINT_MAP_0	R/W	0h	Host Interrupt Map for Channel 0

Table 15-619. Register Call Summary for ICSS_INTC_HINT_MAP_REG0

PRU_ICSS_INTC_INTC Registers
PRU_ICSS_INTC_INTC Registers: [0] ICSS_INTC_HINT_MAP_REG0 Register (Offset = 800h) [reset = X]: [0]
PRU_ICSSG Local INTC
PRU_ICSSG Interrupt Controller Basic Programming Model: [0]
PRU_ICSSG Interrupt Controller Functional Description
PRU_ICSSG Host Interrupt Mapping: [0]

15.7.73 ICSS_INTC_HINT_MAP_REG1 Register (Offset = 804h) [reset = X]

ICSS_INTC_HINT_MAP_REG1 is shown in [Figure 15-203](#) and described in [Table 15-621](#).

Return to [Summary Table](#).

Host Interrupt Map Register for 4 to 4+3

Table 15-620. ICSS_INTC_HINT_MAP_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0804h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0804h

Figure 15-203. ICSS_INTC_HINT_MAP_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				HINT_MAP_7				RESERVED				HINT_MAP_6			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				HINT_MAP_5				RESERVED				HINT_MAP_4			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-621. ICSS_INTC_HINT_MAP_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	HINT_MAP_7	R/W	0h	Host Interrupt Map for Channel 7
23-21	RESERVED	R/W	X	
20-16	HINT_MAP_6	R/W	0h	Host Interrupt Map for Channel 6
15-13	RESERVED	R/W	X	
12-8	HINT_MAP_5	R/W	0h	Host Interrupt Map for Channel 5
7-5	RESERVED	R/W	X	
4-0	HINT_MAP_4	R/W	0h	Host Interrupt Map for Channel 4

Table 15-622. Register Call Summary for ICSS_INTC_HINT_MAP_REG1

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_HINT_MAP_REG1 Register \(Offset = 804h\) \[reset = X\]: \[0\]](#)

15.7.74 ICSS_INTC_HINT_MAP_REG2 Register (Offset = 808h) [reset = X]

ICSS_INTC_HINT_MAP_REG2 is shown in [Figure 15-204](#) and described in [Table 15-624](#).

Return to [Summary Table](#).

Host Interrupt Map Register for 8 to 8+3

Table 15-623. ICSS_INTC_HINT_MAP_REG2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0808h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0808h

Figure 15-204. ICSS_INTC_HINT_MAP_REG2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				HINT_MAP_11				RESERVED				HINT_MAP_10			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				HINT_MAP_9				RESERVED				HINT_MAP_8			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-624. ICSS_INTC_HINT_MAP_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	HINT_MAP_11	R/W	0h	Host Interrupt Map for Channel 11
23-21	RESERVED	R/W	X	
20-16	HINT_MAP_10	R/W	0h	Host Interrupt Map for Channel 10
15-13	RESERVED	R/W	X	
12-8	HINT_MAP_9	R/W	0h	Host Interrupt Map for Channel 9
7-5	RESERVED	R/W	X	
4-0	HINT_MAP_8	R/W	0h	Host Interrupt Map for Channel 8

Table 15-625. Register Call Summary for ICSS_INTC_HINT_MAP_REG2

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_HINT_MAP_REG2 Register \(Offset = 808h\) \[reset = X\]: \[0\]](#)

15.7.75 ICSS_INTC_HINT_MAP_REG3 Register (Offset = 80Ch) [reset = X]

ICSS_INTC_HINT_MAP_REG3 is shown in [Figure 15-205](#) and described in [Table 15-627](#).

Return to [Summary Table](#).

Host Interrupt Map Register for 12 to 12+3

Table 15-626. ICSS_INTC_HINT_MAP_REG3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 080Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 080Ch

Figure 15-205. ICSS_INTC_HINT_MAP_REG3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				HINT_MAP_15				RESERVED				HINT_MAP_14			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				HINT_MAP_13				RESERVED				HINT_MAP_12			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-627. ICSS_INTC_HINT_MAP_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	HINT_MAP_15	R/W	0h	Host Interrupt Map for Channel 15
23-21	RESERVED	R/W	X	
20-16	HINT_MAP_14	R/W	0h	Host Interrupt Map for Channel 14
15-13	RESERVED	R/W	X	
12-8	HINT_MAP_13	R/W	0h	Host Interrupt Map for Channel 13
7-5	RESERVED	R/W	X	
4-0	HINT_MAP_12	R/W	0h	Host Interrupt Map for Channel 12

Table 15-628. Register Call Summary for ICSS_INTC_HINT_MAP_REG3

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers](#): [0]
- [ICSS_INTC_HINT_MAP_REG3 Register \(Offset = 80Ch\) \[reset = X\]](#): [0]

15.7.76 ICSS_INTC_HINT_MAP_REG4 Register (Offset = 810h) [reset = X]

ICSS_INTC_HINT_MAP_REG4 is shown in [Figure 15-206](#) and described in [Table 15-630](#).

Return to [Summary Table](#).

Host Interrupt Map Register for 16 to 16+4

Table 15-629. ICSS_INTC_HINT_MAP_REG4 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0810h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0810h

Figure 15-206. ICSS_INTC_HINT_MAP_REG4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				HINT_MAP_19				RESERVED				HINT_MAP_18			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				HINT_MAP_17				RESERVED				HINT_MAP_16			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-630. ICSS_INTC_HINT_MAP_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	HINT_MAP_19	R/W	0h	Host Interrupt Map for Channel 19
23-21	RESERVED	R/W	X	
20-16	HINT_MAP_18	R/W	0h	Host Interrupt Map for Channel 18
15-13	RESERVED	R/W	X	
12-8	HINT_MAP_17	R/W	0h	Host Interrupt Map for Channel 17
7-5	RESERVED	R/W	X	
4-0	HINT_MAP_16	R/W	0h	Host Interrupt Map for Channel 16

Table 15-631. Register Call Summary for ICSS_INTC_HINT_MAP_REG4

PRU_ICSS_INTC_INTC Registers
- ICSS_INTC_HINT_MAP_REG4 Register (Offset = 810h) [reset = X]: [0] - PRU_ICSS_INTC_INTC Registers: [0]
PRU_ICSSG Local INTC
PRU_ICSSG Interrupt Controller Basic Programming Model: [0]
PRU_ICSSG Interrupt Controller Functional Description
PRU_ICSSG Host Interrupt Mapping: [0]

15.7.77 ICSS_INTC_PRI_HINT_REG0 Register (Offset = 900h) [reset = X]

ICSS_INTC_PRI_HINT_REG0 is shown in [Figure 15-207](#) and described in [Table 15-633](#).

Return to [Summary Table](#).

Host Int 0 Prioritized Interrupt Register

Table 15-632. ICSS_INTC_PRI_HINT_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0900h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0900h

Figure 15-207. ICSS_INTC_PRI_HINT_REG0 Register

31	30	29	28	27	26	25	24
NONE_HINT_0	RESERVED						
R-1h	R-X						
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_0	
R-X						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT_0							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 15-633. ICSS_INTC_PRI_HINT_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_0	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_0	R	0h	Host Int 0 Prioritized Interrupt

Table 15-634. Register Call Summary for ICSS_INTC_PRI_HINT_REG0

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_PRI_HINT_REG0 Register \(Offset = 900h\) \[reset = X\]: \[0\]](#)

15.7.78 ICSS_INTC_PRI_HINT_REG1 Register (Offset = 904h) [reset = X]

ICSS_INTC_PRI_HINT_REG1 is shown in [Figure 15-208](#) and described in [Table 15-636](#).

Return to [Summary Table](#).

Host Int 1 Prioritized Interrupt Register

Table 15-635. ICSS_INTC_PRI_HINT_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0904h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0904h

Figure 15-208. ICSS_INTC_PRI_HINT_REG1 Register

31	30	29	28	27	26	25	24
NONE_HINT_1	RESERVED						
R-1h	R-X						
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_1	
R-X						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT_1							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 15-636. ICSS_INTC_PRI_HINT_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_1	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_1	R	0h	Host Int 1 Prioritized Interrupt

Table 15-637. Register Call Summary for ICSS_INTC_PRI_HINT_REG1

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_PRI_HINT_REG1 Register \(Offset = 904h\) \[reset = X\]: \[0\]](#)

15.7.79 ICSS_INTC_PRI_HINT_REG2 Register (Offset = 908h) [reset = X]

ICSS_INTC_PRI_HINT_REG2 is shown in Figure 15-209 and described in Table 15-639.

Return to [Summary Table](#).

Host Int 2 Prioritized Interrupt Register

Table 15-638. ICSS_INTC_PRI_HINT_REG2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTCLV	0B02 0908h
PRU_ICSSG1_PR1_ICSS_INTC_INTCLV	0B12 0908h

Figure 15-209. ICSS_INTC_PRI_HINT_REG2 Register

31	30	29	28	27	26	25	24
NONE_HINT_2	RESERVED						
R-1h	R-X						
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_2	
R-X						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT_2							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 15-639. ICSS_INTC_PRI_HINT_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_2	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_2	R	0h	Host Int 2 Prioritized Interrupt

Table 15-640. Register Call Summary for ICSS_INTC_PRI_HINT_REG2

PRU_ICSS_INTCLV Registers

- [ICSS_INTC_PRI_HINT_REG2 Register \(Offset = 908h\) \[reset = X\]: \[0\]](#)
- [PRU_ICSS_INTCLV Registers: \[0\]](#)

15.7.80 ICSS_INTC_PRI_HINT_REG3 Register (Offset = 90Ch) [reset = X]

ICSS_INTC_PRI_HINT_REG3 is shown in Figure 15-210 and described in Table 15-642.

Return to [Summary Table](#).

Host Int 3 Prioritized Interrupt Register

Table 15-641. ICSS_INTC_PRI_HINT_REG3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 090Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 090Ch

Figure 15-210. ICSS_INTC_PRI_HINT_REG3 Register

31	30	29	28	27	26	25	24
NONE_HINT_3	RESERVED						
R-1h	R-X						
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_3	
R-X						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT_3							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 15-642. ICSS_INTC_PRI_HINT_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_3	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_3	R	0h	Host Int 3 Prioritized Interrupt

Table 15-643. Register Call Summary for ICSS_INTC_PRI_HINT_REG3

PRU_ICSS_INTC_INTC Registers

- [ICSS_INTC_PRI_HINT_REG3 Register \(Offset = 90Ch\) \[reset = X\]: \[0\]](#)
- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)

15.7.81 ICSS_INTC_PRI_HINT_REG4 Register (Offset = 910h) [reset = X]

ICSS_INTC_PRI_HINT_REG4 is shown in Figure 15-211 and described in Table 15-645.

Return to [Summary Table](#).

Host Int 4 Prioritized Interrupt Register

Table 15-644. ICSS_INTC_PRI_HINT_REG4 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0910h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0910h

Figure 15-211. ICSS_INTC_PRI_HINT_REG4 Register

31	30	29	28	27	26	25	24
NONE_HINT_4	RESERVED						
R-1h	R-X						
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_4	
R-X						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT_4							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 15-645. ICSS_INTC_PRI_HINT_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_4	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_4	R	0h	Host Int 4 Prioritized Interrupt

Table 15-646. Register Call Summary for ICSS_INTC_PRI_HINT_REG4

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_PRI_HINT_REG4 Register \(Offset = 910h\) \[reset = X\]: \[0\]](#)

15.7.82 ICSS_INTC_PRI_HINT_REG5 Register (Offset = 914h) [reset = X]

ICSS_INTC_PRI_HINT_REG5 is shown in [Figure 15-212](#) and described in [Table 15-648](#).

Return to [Summary Table](#).

Host Int 5 Prioritized Interrupt Register

Table 15-647. ICSS_INTC_PRI_HINT_REG5 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0914h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0914h

Figure 15-212. ICSS_INTC_PRI_HINT_REG5 Register

31	30	29	28	27	26	25	24
NONE_HINT_5	RESERVED						
R-1h	R-X						
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_5	
R-X						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT_5							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 15-648. ICSS_INTC_PRI_HINT_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_5	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_5	R	0h	Host Int 5 Prioritized Interrupt

Table 15-649. Register Call Summary for ICSS_INTC_PRI_HINT_REG5

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_PRI_HINT_REG5 Register \(Offset = 914h\) \[reset = X\]: \[0\]](#)

15.7.83 ICSS_INTC_PRI_HINT_REG6 Register (Offset = 918h) [reset = X]

ICSS_INTC_PRI_HINT_REG6 is shown in Figure 15-213 and described in Table 15-651.

Return to [Summary Table](#).

Host Int 6 Prioritized Interrupt Register

Table 15-650. ICSS_INTC_PRI_HINT_REG6 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0918h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0918h

Figure 15-213. ICSS_INTC_PRI_HINT_REG6 Register

31	30	29	28	27	26	25	24
NONE_HINT_6	RESERVED						
R-1h	R-X						
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_6	
R-X						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT_6							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 15-651. ICSS_INTC_PRI_HINT_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_6	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_6	R	0h	Host Int 6 Prioritized Interrupt

Table 15-652. Register Call Summary for ICSS_INTC_PRI_HINT_REG6

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_PRI_HINT_REG6 Register \(Offset = 918h\) \[reset = X\]: \[0\]](#)

15.7.84 ICSS_INTC_PRI_HINT_REG7 Register (Offset = 91Ch) [reset = X]

ICSS_INTC_PRI_HINT_REG7 is shown in [Figure 15-214](#) and described in [Table 15-654](#).

Return to [Summary Table](#).

Host Int 7 Prioritized Interrupt Register

Table 15-653. ICSS_INTC_PRI_HINT_REG7 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 091Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 091Ch

Figure 15-214. ICSS_INTC_PRI_HINT_REG7 Register

31	30	29	28	27	26	25	24
NONE_HINT_7	RESERVED						
R-1h	R-X						
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_7	
R-X						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT_7							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 15-654. ICSS_INTC_PRI_HINT_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_7	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_7	R	0h	Host Int 7 Prioritized Interrupt

Table 15-655. Register Call Summary for ICSS_INTC_PRI_HINT_REG7

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_PRI_HINT_REG7 Register \(Offset = 91Ch\) \[reset = X\]: \[0\]](#)

15.7.85 ICSS_INTC_PRI_HINT_REG8 Register (Offset = 920h) [reset = X]

ICSS_INTC_PRI_HINT_REG8 is shown in Figure 15-215 and described in Table 15-657.

Return to [Summary Table](#).

Host Int 8 Prioritized Interrupt Register

Table 15-656. ICSS_INTC_PRI_HINT_REG8 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTCLV	0B02 0920h
PRU_ICSSG1_PR1_ICSS_INTC_INTCLV	0B12 0920h

Figure 15-215. ICSS_INTC_PRI_HINT_REG8 Register

31	30	29	28	27	26	25	24
NONE_HINT_8	RESERVED						
R-1h	R-X						
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_8	
R-X						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT_8							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 15-657. ICSS_INTC_PRI_HINT_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_8	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_8	R	0h	Host Int 8 Prioritized Interrupt

Table 15-658. Register Call Summary for ICSS_INTC_PRI_HINT_REG8

PRU_ICSS_INTC_INTCLV Registers

- [PRU_ICSS_INTC_INTCLV Registers: \[0\]](#)
- [ICSS_INTC_PRI_HINT_REG8 Register \(Offset = 920h\) \[reset = X\]: \[0\]](#)

15.7.86 ICSS_INTC_PRI_HINT_REG9 Register (Offset = 924h) [reset = X]

ICSS_INTC_PRI_HINT_REG9 is shown in Figure 15-216 and described in Table 15-660.

Return to [Summary Table](#).

Host Int 9 Prioritized Interrupt Register

Table 15-659. ICSS_INTC_PRI_HINT_REG9 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0924h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0924h

Figure 15-216. ICSS_INTC_PRI_HINT_REG9 Register

31	30	29	28	27	26	25	24
NONE_HINT_9	RESERVED						
R-1h	R-X						
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_9	
R-X						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT_9							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 15-660. ICSS_INTC_PRI_HINT_REG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_9	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_9	R	0h	Host Int 9 Prioritized Interrupt

Table 15-661. Register Call Summary for ICSS_INTC_PRI_HINT_REG9

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_PRI_HINT_REG9 Register \(Offset = 924h\) \[reset = X\]: \[0\]](#)

15.7.87 ICSS_INTC_PRI_HINT_REG10 Register (Offset = 928h) [reset = X]

ICSS_INTC_PRI_HINT_REG10 is shown in [Figure 15-217](#) and described in [Table 15-663](#).

Return to [Summary Table](#).

Host Int 10 Prioritized Interrupt Register

Table 15-662. ICSS_INTC_PRI_HINT_REG10 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0928h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0928h

Figure 15-217. ICSS_INTC_PRI_HINT_REG10 Register

31	30	29	28	27	26	25	24
NONE_HINT_1 0	RESERVED						
R-1h	R-X						
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_10	
R-X						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT_10							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 15-663. ICSS_INTC_PRI_HINT_REG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_10	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_10	R	0h	Host Int 10 Prioritized Interrupt

Table 15-664. Register Call Summary for ICSS_INTC_PRI_HINT_REG10

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_PRI_HINT_REG10 Register \(Offset = 928h\) \[reset = X\]: \[0\]](#)

15.7.88 ICSS_INTC_PRI_HINT_REG11 Register (Offset = 92Ch) [reset = X]

ICSS_INTC_PRI_HINT_REG11 is shown in [Figure 15-218](#) and described in [Table 15-666](#).

Return to [Summary Table](#).

Host Int 11 Prioritized Interrupt Register

Table 15-665. ICSS_INTC_PRI_HINT_REG11 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 092Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 092Ch

Figure 15-218. ICSS_INTC_PRI_HINT_REG11 Register

31	30	29	28	27	26	25	24
NONE_HINT_1 1	RESERVED						
R-1h	R-X						
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_11	
R-X						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT_11							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 15-666. ICSS_INTC_PRI_HINT_REG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_11	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_11	R	0h	Host Int 11 Prioritized Interrupt

Table 15-667. Register Call Summary for ICSS_INTC_PRI_HINT_REG11

PRU_ICSS_INTC_INTC Registers
PRU_ICSS_INTC_INTC Registers: [0] ICSS_INTC_PRI_HINT_REG11 Register (Offset = 92Ch) [reset = X]: [0]

15.7.89 ICSS_INTC_PRI_HINT_REG12 Register (Offset = 930h) [reset = X]

ICSS_INTC_PRI_HINT_REG12 is shown in [Figure 15-219](#) and described in [Table 15-669](#).

Return to [Summary Table](#).

Host Int 12 Prioritized Interrupt Register

Table 15-668. ICSS_INTC_PRI_HINT_REG12 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0930h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0930h

Figure 15-219. ICSS_INTC_PRI_HINT_REG12 Register

31	30	29	28	27	26	25	24
NONE_HINT_1 2	RESERVED						
R-1h	R-X						
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_12	
R-X						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT_12							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 15-669. ICSS_INTC_PRI_HINT_REG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_12	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_12	R	0h	Host Int 12 Prioritized Interrupt

Table 15-670. Register Call Summary for ICSS_INTC_PRI_HINT_REG12

PRU_ICSS_INTC_INTC Registers

- ICSS_INTC_PRI_HINT_REG12 Register (Offset = 930h) [reset = X]: [0]
- PRU_ICSS_INTC_INTC Registers: [0]

15.7.90 ICSS_INTC_PRI_HINT_REG13 Register (Offset = 934h) [reset = X]

ICSS_INTC_PRI_HINT_REG13 is shown in [Figure 15-220](#) and described in [Table 15-672](#).

Return to [Summary Table](#).

Host Int 13 Prioritized Interrupt Register

Table 15-671. ICSS_INTC_PRI_HINT_REG13 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0934h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0934h

Figure 15-220. ICSS_INTC_PRI_HINT_REG13 Register

31	30	29	28	27	26	25	24
NONE_HINT_1 3	RESERVED						
R-1h	R-X						
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_13	
R-X						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT_13							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 15-672. ICSS_INTC_PRI_HINT_REG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_13	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_13	R	0h	Host Int 13 Prioritized Interrupt

Table 15-673. Register Call Summary for ICSS_INTC_PRI_HINT_REG13

PRU_ICSS_INTC_INTC Registers
- ICSS_INTC_PRI_HINT_REG13 Register (Offset = 934h) [reset = X]: [0] - PRU_ICSS_INTC_INTC Registers: [0]

15.7.91 ICSS_INTC_PRI_HINT_REG14 Register (Offset = 938h) [reset = X]

ICSS_INTC_PRI_HINT_REG14 is shown in [Figure 15-221](#) and described in [Table 15-675](#).

Return to [Summary Table](#).

Host Int 14 Prioritized Interrupt Register

Table 15-674. ICSS_INTC_PRI_HINT_REG14 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0938h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0938h

Figure 15-221. ICSS_INTC_PRI_HINT_REG14 Register

31	30	29	28	27	26	25	24
NONE_HINT_1 4	RESERVED						
R-1h	R-X						
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_14	
R-X						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT_14							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 15-675. ICSS_INTC_PRI_HINT_REG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_14	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_14	R	0h	Host Int 14 Prioritized Interrupt

Table 15-676. Register Call Summary for ICSS_INTC_PRI_HINT_REG14

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_PRI_HINT_REG14 Register \(Offset = 938h\) \[reset = X\]: \[0\]](#)

15.7.92 ICSS_INTC_PRI_HINT_REG15 Register (Offset = 93Ch) [reset = X]

ICSS_INTC_PRI_HINT_REG15 is shown in [Figure 15-222](#) and described in [Table 15-678](#).

Return to [Summary Table](#).

Host Int 15 Prioritized Interrupt Register

Table 15-677. ICSS_INTC_PRI_HINT_REG15 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 093Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 093Ch

Figure 15-222. ICSS_INTC_PRI_HINT_REG15 Register

31	30	29	28	27	26	25	24
NONE_HINT_1 5	RESERVED						
R-1h	R-X						
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_15	
R-X						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT_15							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 15-678. ICSS_INTC_PRI_HINT_REG15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_15	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_15	R	0h	Host Int 15 Prioritized Interrupt

Table 15-679. Register Call Summary for ICSS_INTC_PRI_HINT_REG15

PRU_ICSS_INTC_INTC Registers
PRU_ICSS_INTC_INTC Registers: [0] ICSS_INTC_PRI_HINT_REG15 Register (Offset = 93Ch) [reset = X]: [0]

15.7.93 ICSS_INTC_PRI_HINT_REG16 Register (Offset = 940h) [reset = X]

ICSS_INTC_PRI_HINT_REG16 is shown in [Figure 15-223](#) and described in [Table 15-681](#).

Return to [Summary Table](#).

Host Int 16 Prioritized Interrupt Register

Table 15-680. ICSS_INTC_PRI_HINT_REG16 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0940h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0940h

Figure 15-223. ICSS_INTC_PRI_HINT_REG16 Register

31	30	29	28	27	26	25	24
NONE_HINT_16	RESERVED						
R-1h	R-X						
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_16	
R-X						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT_16							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 15-681. ICSS_INTC_PRI_HINT_REG16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_16	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_16	R	0h	Host Int 16 Prioritized Interrupt

Table 15-682. Register Call Summary for ICSS_INTC_PRI_HINT_REG16

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_PRI_HINT_REG16 Register \(Offset = 940h\) \[reset = X\]: \[0\]](#)

15.7.94 ICSS_INTC_PRI_HINT_REG17 Register (Offset = 944h) [reset = X]

ICSS_INTC_PRI_HINT_REG17 is shown in [Figure 15-224](#) and described in [Table 15-684](#).

[Return to Summary Table.](#)

Host Int 17 Prioritized Interrupt Register

Table 15-683. ICSS_INTC_PRI_HINT_REG17 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0944h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0944h

Figure 15-224. ICSS_INTC_PRI_HINT_REG17 Register

31	30	29	28	27	26	25	24
NONE_HINT_1 7	RESERVED						
R-1h	R-X						
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_17	
R-X						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT_17							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 15-684. ICSS_INTC_PRI_HINT_REG17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_17	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_17	R	0h	Host Int 17 Prioritized Interrupt

Table 15-685. Register Call Summary for ICSS_INTC_PRI_HINT_REG17

PRU_ICSS_INTC_INTC Registers
PRU_ICSS_INTC_INTC Registers: [0] ICSS_INTC_PRI_HINT_REG17 Register (Offset = 944h) [reset = X]: [0]

15.7.95 ICSS_INTC_PRI_HINT_REG18 Register (Offset = 948h) [reset = X]

ICSS_INTC_PRI_HINT_REG18 is shown in [Figure 15-225](#) and described in [Table 15-687](#).

Return to [Summary Table](#).

Host Int 18 Prioritized Interrupt Register

Table 15-686. ICSS_INTC_PRI_HINT_REG18 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0948h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0948h

Figure 15-225. ICSS_INTC_PRI_HINT_REG18 Register

31	30	29	28	27	26	25	24
NONE_HINT_18	RESERVED						
R-1h	R-X						
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_18	
R-X						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT_18							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 15-687. ICSS_INTC_PRI_HINT_REG18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_18	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_18	R	0h	Host Int 18 Prioritized Interrupt

Table 15-688. Register Call Summary for ICSS_INTC_PRI_HINT_REG18

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_PRI_HINT_REG18 Register \(Offset = 948h\) \[reset = X\]: \[0\]](#)

15.7.96 ICSS_INTC_PRI_HINT_REG19 Register (Offset = 94Ch) [reset = X]

ICSS_INTC_PRI_HINT_REG19 is shown in [Figure 15-226](#) and described in [Table 15-690](#).

Return to [Summary Table](#).

Host Int 19 Prioritized Interrupt Register

Table 15-689. ICSS_INTC_PRI_HINT_REG19 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 094Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 094Ch

Figure 15-226. ICSS_INTC_PRI_HINT_REG19 Register

31	30	29	28	27	26	25	24
NONE_HINT_19	RESERVED						
R-1h	R-X						
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_19	
R-X						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT_19							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 15-690. ICSS_INTC_PRI_HINT_REG19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_19	R	1h	No interrupt pending flag
30-10	RESERVED	R	X	
9-0	PRI_HINT_19	R	0h	Host Int 19 Prioritized Interrupt

Table 15-691. Register Call Summary for ICSS_INTC_PRI_HINT_REG19

PRU_ICSS_INTC_INTC Registers
PRU_ICSS_INTC_INTC Registers: [0] ICSS_INTC_PRI_HINT_REG19 Register (Offset = 94Ch) [reset = X]: [0]

15.7.97 ICSS_INTC_POLARITY_REG0 Register (Offset = D00h) [reset = FFFFFFFFh]

ICSS_INTC_POLARITY_REG0 is shown in [Figure 15-227](#) and described in [Table 15-693](#).

Return to [Summary Table](#).

Polarity Register 0

Table 15-692. ICSS_INTC_POLARITY_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTCLV	0B02 0D00h
PRU_ICSSG1_PR1_ICSS_INTC_INTCLV	0B12 0D00h

Figure 15-227. ICSS_INTC_POLARITY_REG0 Register

31	30	29	28	27	26	25	24
POLARITY_31	POLARITY_30	POLARITY_29	POLARITY_28	POLARITY_27	POLARITY_26	POLARITY_25	POLARITY_24
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
23	22	21	20	19	18	17	16
POLARITY_23	POLARITY_22	POLARITY_21	POLARITY_20	POLARITY_19	POLARITY_18	POLARITY_17	POLARITY_16
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
15	14	13	12	11	10	9	8
POLARITY_15	POLARITY_14	POLARITY_13	POLARITY_12	POLARITY_11	POLARITY_10	POLARITY_9	POLARITY_8
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
7	6	5	4	3	2	1	0
POLARITY_7	POLARITY_6	POLARITY_5	POLARITY_4	POLARITY_3	POLARITY_2	POLARITY_1	POLARITY_0
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-693. ICSS_INTC_POLARITY_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POLARITY_31	R/W	1h	Polarity for intr_in[31] 0=low
30	POLARITY_30	R/W	1h	Polarity for intr_in[30] 0=low
29	POLARITY_29	R/W	1h	Polarity for intr_in[29] 0=low
28	POLARITY_28	R/W	1h	Polarity for intr_in[28] 0=low
27	POLARITY_27	R/W	1h	Polarity for intr_in[27] 0=low
26	POLARITY_26	R/W	1h	Polarity for intr_in[26] 0=low
25	POLARITY_25	R/W	1h	Polarity for intr_in[25] 0=low
24	POLARITY_24	R/W	1h	Polarity for intr_in[24] 0=low
23	POLARITY_23	R/W	1h	Polarity for intr_in[23] 0=low
22	POLARITY_22	R/W	1h	Polarity for intr_in[22] 0=low
21	POLARITY_21	R/W	1h	Polarity for intr_in[21] 0=low
20	POLARITY_20	R/W	1h	Polarity for intr_in[20] 0=low

Table 15-693. ICSS_INTC_POLARITY_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	POLARITY_19	R/W	1h	Polarity for intr_in[19] 0=low
18	POLARITY_18	R/W	1h	Polarity for intr_in[18] 0=low
17	POLARITY_17	R/W	1h	Polarity for intr_in[17] 0=low
16	POLARITY_16	R/W	1h	Polarity for intr_in[16] 0=low
15	POLARITY_15	R/W	1h	Polarity for intr_in[15] 0=low
14	POLARITY_14	R/W	1h	Polarity for intr_in[14] 0=low
13	POLARITY_13	R/W	1h	Polarity for intr_in[13] 0=low
12	POLARITY_12	R/W	1h	Polarity for intr_in[12] 0=low
11	POLARITY_11	R/W	1h	Polarity for intr_in[11] 0=low
10	POLARITY_10	R/W	1h	Polarity for intr_in[10] 0=low
9	POLARITY_9	R/W	1h	Polarity for intr_in[9] 0=low
8	POLARITY_8	R/W	1h	Polarity for intr_in[8] 0=low
7	POLARITY_7	R/W	1h	Polarity for intr_in[7] 0=low
6	POLARITY_6	R/W	1h	Polarity for intr_in[6] 0=low
5	POLARITY_5	R/W	1h	Polarity for intr_in[5] 0=low
4	POLARITY_4	R/W	1h	Polarity for intr_in[4] 0=low
3	POLARITY_3	R/W	1h	Polarity for intr_in[3] 0=low
2	POLARITY_2	R/W	1h	Polarity for intr_in[2] 0=low
1	POLARITY_1	R/W	1h	Polarity for intr_in[1] 0=low
0	POLARITY_0	R/W	1h	Polarity for intr_in[0] 0=low

Table 15-694. Register Call Summary for ICSS_INTC_POLARITY_REG0

PRU_ICSS_INTC_INTC Registers • ICSS_INTC_POLARITY_REG0 Register (Offset = D00h) [reset = FFFFFFFh]: [0] • PRU_ICSS_INTC_INTC Registers: [0]
PRU_ICSSG Local INTC • PRU_ICSSG Interrupt Controller Basic Programming Model: [0]

15.7.98 ICSS_INTC_POLARITY_REG1 Register (Offset = D04h) [reset = FFFFFFFFh]

ICSS_INTC_POLARITY_REG1 is shown in [Figure 15-228](#) and described in [Table 15-696](#).

Return to [Summary Table](#).

Polarity Register 1

Table 15-695. ICSS_INTC_POLARITY_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0D04h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0D04h

Figure 15-228. ICSS_INTC_POLARITY_REG1 Register

31	30	29	28	27	26	25	24
POLARITY_63	POLARITY_62	POLARITY_61	POLARITY_60	POLARITY_59	POLARITY_58	POLARITY_57	POLARITY_56
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
23	22	21	20	19	18	17	16
POLARITY_55	POLARITY_54	POLARITY_53	POLARITY_52	POLARITY_51	POLARITY_50	POLARITY_49	POLARITY_48
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
15	14	13	12	11	10	9	8
POLARITY_47	POLARITY_46	POLARITY_45	POLARITY_44	POLARITY_43	POLARITY_42	POLARITY_41	POLARITY_40
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
7	6	5	4	3	2	1	0
POLARITY_39	POLARITY_38	POLARITY_37	POLARITY_36	POLARITY_35	POLARITY_34	POLARITY_33	POLARITY_32
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-696. ICSS_INTC_POLARITY_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POLARITY_63	R/W	1h	Polarity for intr_in[63] 0=low
30	POLARITY_62	R/W	1h	Polarity for intr_in[62] 0=low
29	POLARITY_61	R/W	1h	Polarity for intr_in[61] 0=low
28	POLARITY_60	R/W	1h	Polarity for intr_in[60] 0=low
27	POLARITY_59	R/W	1h	Polarity for intr_in[59] 0=low
26	POLARITY_58	R/W	1h	Polarity for intr_in[58] 0=low
25	POLARITY_57	R/W	1h	Polarity for intr_in[57] 0=low
24	POLARITY_56	R/W	1h	Polarity for intr_in[56] 0=low
23	POLARITY_55	R/W	1h	Polarity for intr_in[55] 0=low
22	POLARITY_54	R/W	1h	Polarity for intr_in[54] 0=low
21	POLARITY_53	R/W	1h	Polarity for intr_in[53] 0=low
20	POLARITY_52	R/W	1h	Polarity for intr_in[52] 0=low

Table 15-696. ICSS_INTC_POLARITY_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	POLARITY_51	R/W	1h	Polarity for intr_in[51] 0=low
18	POLARITY_50	R/W	1h	Polarity for intr_in[50] 0=low
17	POLARITY_49	R/W	1h	Polarity for intr_in[49] 0=low
16	POLARITY_48	R/W	1h	Polarity for intr_in[48] 0=low
15	POLARITY_47	R/W	1h	Polarity for intr_in[47] 0=low
14	POLARITY_46	R/W	1h	Polarity for intr_in[46] 0=low
13	POLARITY_45	R/W	1h	Polarity for intr_in[45] 0=low
12	POLARITY_44	R/W	1h	Polarity for intr_in[44] 0=low
11	POLARITY_43	R/W	1h	Polarity for intr_in[43] 0=low
10	POLARITY_42	R/W	1h	Polarity for intr_in[42] 0=low
9	POLARITY_41	R/W	1h	Polarity for intr_in[41] 0=low
8	POLARITY_40	R/W	1h	Polarity for intr_in[40] 0=low
7	POLARITY_39	R/W	1h	Polarity for intr_in[39] 0=low
6	POLARITY_38	R/W	1h	Polarity for intr_in[38] 0=low
5	POLARITY_37	R/W	1h	Polarity for intr_in[37] 0=low
4	POLARITY_36	R/W	1h	Polarity for intr_in[36] 0=low
3	POLARITY_35	R/W	1h	Polarity for intr_in[35] 0=low
2	POLARITY_34	R/W	1h	Polarity for intr_in[34] 0=low
1	POLARITY_33	R/W	1h	Polarity for intr_in[33] 0=low
0	POLARITY_32	R/W	1h	Polarity for intr_in[32] 0=low

Table 15-697. Register Call Summary for ICSS_INTC_POLARITY_REG1

PRU_ICSS_INTC_INTC Registers

- [ICSS_INTC_POLARITY_REG1 Register \(Offset = D04h\) \[reset = FFFFFFFh\]: \[0\]](#)
- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)

15.7.99 ICSS_INTC_POLARITY_REG2 Register (Offset = D08h) [reset = FFFFFFFFh]

ICSS_INTC_POLARITY_REG2 is shown in [Figure 15-229](#) and described in [Table 15-699](#).

Return to [Summary Table](#).

Polarity Register 2

Table 15-698. ICSS_INTC_POLARITY_REG2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTCLV	0B02 0D08h
PRU_ICSSG1_PR1_ICSS_INTC_INTCLV	0B12 0D08h

Figure 15-229. ICSS_INTC_POLARITY_REG2 Register

31	30	29	28	27	26	25	24
POLARITY_95	POLARITY_94	POLARITY_93	POLARITY_92	POLARITY_91	POLARITY_90	POLARITY_89	POLARITY_88
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
23	22	21	20	19	18	17	16
POLARITY_87	POLARITY_86	POLARITY_85	POLARITY_84	POLARITY_83	POLARITY_82	POLARITY_81	POLARITY_80
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
15	14	13	12	11	10	9	8
POLARITY_79	POLARITY_78	POLARITY_77	POLARITY_76	POLARITY_75	POLARITY_74	POLARITY_73	POLARITY_72
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
7	6	5	4	3	2	1	0
POLARITY_71	POLARITY_70	POLARITY_69	POLARITY_68	POLARITY_67	POLARITY_66	POLARITY_65	POLARITY_64
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-699. ICSS_INTC_POLARITY_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POLARITY_95	R/W	1h	Polarity for slv_events_in[31] 0=low
30	POLARITY_94	R/W	1h	Polarity for slv_events_in[30] 0=low
29	POLARITY_93	R/W	1h	Polarity for slv_events_in[29] 0=low
28	POLARITY_92	R/W	1h	Polarity for slv_events_in[28] 0=low
27	POLARITY_91	R/W	1h	Polarity for slv_events_in[27] 0=low
26	POLARITY_90	R/W	1h	Polarity for slv_events_in[26] 0=low
25	POLARITY_89	R/W	1h	Polarity for slv_events_in[25] 0=low
24	POLARITY_88	R/W	1h	Polarity for slv_events_in[24] 0=low
23	POLARITY_87	R/W	1h	Polarity for slv_events_in[23] 0=low
22	POLARITY_86	R/W	1h	Polarity for slv_events_in[22] 0=low
21	POLARITY_85	R/W	1h	Polarity for slv_events_in[21] 0=low
20	POLARITY_84	R/W	1h	Polarity for slv_events_in[20] 0=low

Table 15-699. ICSS_INTC_POLARITY_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	POLARITY_83	R/W	1h	Polarity for slv_events_in[19] 0=low
18	POLARITY_82	R/W	1h	Polarity for slv_events_in[18] 0=low
17	POLARITY_81	R/W	1h	Polarity for slv_events_in[17] 0=low
16	POLARITY_80	R/W	1h	Polarity for slv_events_in[16] 0=low
15	POLARITY_79	R/W	1h	Polarity for slv_events_in[15] 0=low
14	POLARITY_78	R/W	1h	Polarity for slv_events_in[14] 0=low
13	POLARITY_77	R/W	1h	Polarity for slv_events_in[13] 0=low
12	POLARITY_76	R/W	1h	Polarity for slv_events_in[12] 0=low
11	POLARITY_75	R/W	1h	Polarity for slv_events_in[11] 0=low
10	POLARITY_74	R/W	1h	Polarity for slv_events_in[10] 0=low
9	POLARITY_73	R/W	1h	Polarity for slv_events_in[9] 0=low
8	POLARITY_72	R/W	1h	Polarity for slv_events_in[8] 0=low
7	POLARITY_71	R/W	1h	Polarity for slv_events_in[7] 0=low
6	POLARITY_70	R/W	1h	Polarity for slv_events_in[6] 0=low
5	POLARITY_69	R/W	1h	Polarity for slv_events_in[5] 0=low
4	POLARITY_68	R/W	1h	Polarity for slv_events_in[4] 0=low
3	POLARITY_67	R/W	1h	Polarity for slv_events_in[3] 0=low
2	POLARITY_66	R/W	1h	Polarity for slv_events_in[2] 0=low
1	POLARITY_65	R/W	1h	Polarity for slv_events_in[1] 0=low
0	POLARITY_64	R/W	1h	Polarity for slv_events_in[0] 0=low

Table 15-700. Register Call Summary for ICSS_INTC_POLARITY_REG2

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_POLARITY_REG2 Register \(Offset = D08h\) \[reset = FFFFFFFFh\]: \[0\]](#)

15.7.100 ICSS_INTC_POLARITY_REG3 Register (Offset = D0Ch) [reset = FFFFFFFFh]

ICSS_INTC_POLARITY_REG3 is shown in [Figure 15-230](#) and described in [Table 15-702](#).

Return to [Summary Table](#).

Polarity Register 3

Table 15-701. ICSS_INTC_POLARITY_REG3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTCLV	0B02 0D0Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTCLV	0B12 0D0Ch

Figure 15-230. ICSS_INTC_POLARITY_REG3 Register

31	30	29	28	27	26	25	24
POLARITY_127	POLARITY_126	POLARITY_125	POLARITY_124	POLARITY_123	POLARITY_122	POLARITY_121	POLARITY_120
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
23	22	21	20	19	18	17	16
POLARITY_119	POLARITY_118	POLARITY_117	POLARITY_116	POLARITY_115	POLARITY_114	POLARITY_113	POLARITY_112
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
15	14	13	12	11	10	9	8
POLARITY_111	POLARITY_110	POLARITY_109	POLARITY_108	POLARITY_107	POLARITY_106	POLARITY_105	POLARITY_104
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
7	6	5	4	3	2	1	0
POLARITY_103	POLARITY_102	POLARITY_101	POLARITY_100	POLARITY_99	POLARITY_98	POLARITY_97	POLARITY_96
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-702. ICSS_INTC_POLARITY_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POLARITY_127	R/W	1h	Polarity for slv_events_in[63] 0=low
30	POLARITY_126	R/W	1h	Polarity for slv_events_in[62] 0=low
29	POLARITY_125	R/W	1h	Polarity for slv_events_in[61] 0=low
28	POLARITY_124	R/W	1h	Polarity for slv_events_in[60] 0=low
27	POLARITY_123	R/W	1h	Polarity for slv_events_in[59] 0=low
26	POLARITY_122	R/W	1h	Polarity for slv_events_in[58] 0=low
25	POLARITY_121	R/W	1h	Polarity for slv_events_in[57] 0=low
24	POLARITY_120	R/W	1h	Polarity for slv_events_in[56] 0=low
23	POLARITY_119	R/W	1h	Polarity for slv_events_in[55] 0=low
22	POLARITY_118	R/W	1h	Polarity for slv_events_in[54] 0=low
21	POLARITY_117	R/W	1h	Polarity for slv_events_in[53] 0=low
20	POLARITY_116	R/W	1h	Polarity for slv_events_in[52] 0=low

Table 15-702. ICSS_INTC_POLARITY_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	POLARITY_115	R/W	1h	Polarity for slv_events_in[51] 0=low
18	POLARITY_114	R/W	1h	Polarity for slv_events_in[50] 0=low
17	POLARITY_113	R/W	1h	Polarity for slv_events_in[49] 0=low
16	POLARITY_112	R/W	1h	Polarity for slv_events_in[48] 0=low
15	POLARITY_111	R/W	1h	Polarity for slv_events_in[47] 0=low
14	POLARITY_110	R/W	1h	Polarity for slv_events_in[46] 0=low
13	POLARITY_109	R/W	1h	Polarity for slv_events_in[45] 0=low
12	POLARITY_108	R/W	1h	Polarity for slv_events_in[44] 0=low
11	POLARITY_107	R/W	1h	Polarity for slv_events_in[43] 0=low
10	POLARITY_106	R/W	1h	Polarity for slv_events_in[42] 0=low
9	POLARITY_105	R/W	1h	Polarity for slv_events_in[41] 0=low
8	POLARITY_104	R/W	1h	Polarity for slv_events_in[40] 0=low
7	POLARITY_103	R/W	1h	Polarity for slv_events_in[39] 0=low
6	POLARITY_102	R/W	1h	Polarity for slv_events_in[38] 0=low
5	POLARITY_101	R/W	1h	Polarity for slv_events_in[37] 0=low
4	POLARITY_100	R/W	1h	Polarity for slv_events_in[36] 0=low
3	POLARITY_99	R/W	1h	Polarity for slv_events_in[35] 0=low
2	POLARITY_98	R/W	1h	Polarity for slv_events_in[34] 0=low
1	POLARITY_97	R/W	1h	Polarity for slv_events_in[33] 0=low
0	POLARITY_96	R/W	1h	Polarity for slv_events_in[32] 0=low

Table 15-703. Register Call Summary for ICSS_INTC_POLARITY_REG3

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_POLARITY_REG3 Register \(Offset = D0Ch\) \[reset = FFFFFFFh\]: \[0\]](#)

15.7.101 ICSS_INTC_POLARITY_REG4 Register (Offset = D10h) [reset = FFFFFFFFh]

ICSS_INTC_POLARITY_REG4 is shown in [Figure 15-231](#) and described in [Table 15-705](#).

Return to [Summary Table](#).

Polarity Register 4

Table 15-704. ICSS_INTC_POLARITY_REG4 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTCLV	0B02 0D10h
PRU_ICSSG1_PR1_ICSS_INTC_INTCLV	0B12 0D10h

Figure 15-231. ICSS_INTC_POLARITY_REG4 Register

31	30	29	28	27	26	25	24
POLARITY_159	POLARITY_158	POLARITY_157	POLARITY_156	POLARITY_155	POLARITY_154	POLARITY_153	POLARITY_152
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
23	22	21	20	19	18	17	16
POLARITY_151	POLARITY_150	POLARITY_149	POLARITY_148	POLARITY_147	POLARITY_146	POLARITY_145	POLARITY_144
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
15	14	13	12	11	10	9	8
POLARITY_143	POLARITY_142	POLARITY_141	POLARITY_140	POLARITY_139	POLARITY_138	POLARITY_137	POLARITY_136
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
7	6	5	4	3	2	1	0
POLARITY_135	POLARITY_134	POLARITY_133	POLARITY_132	POLARITY_131	POLARITY_130	POLARITY_129	POLARITY_128
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-705. ICSS_INTC_POLARITY_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POLARITY_159	R/W	1h	Polarity for slv_events_in[95] 0=low
30	POLARITY_158	R/W	1h	Polarity for slv_events_in[94] 0=low
29	POLARITY_157	R/W	1h	Polarity for slv_events_in[93] 0=low
28	POLARITY_156	R/W	1h	Polarity for slv_events_in[92] 0=low
27	POLARITY_155	R/W	1h	Polarity for slv_events_in[91] 0=low
26	POLARITY_154	R/W	1h	Polarity for slv_events_in[90] 0=low
25	POLARITY_153	R/W	1h	Polarity for slv_events_in[89] 0=low
24	POLARITY_152	R/W	1h	Polarity for slv_events_in[88] 0=low
23	POLARITY_151	R/W	1h	Polarity for slv_events_in[87] 0=low
22	POLARITY_150	R/W	1h	Polarity for slv_events_in[86] 0=low
21	POLARITY_149	R/W	1h	Polarity for slv_events_in[85] 0=low
20	POLARITY_148	R/W	1h	Polarity for slv_events_in[84] 0=low

Table 15-705. ICSS_INTC_POLARITY_REG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	POLARITY_147	R/W	1h	Polarity for slv_events_in[83] 0=low
18	POLARITY_146	R/W	1h	Polarity for slv_events_in[82] 0=low
17	POLARITY_145	R/W	1h	Polarity for slv_events_in[81] 0=low
16	POLARITY_144	R/W	1h	Polarity for slv_events_in[80] 0=low
15	POLARITY_143	R/W	1h	Polarity for slv_events_in[79] 0=low
14	POLARITY_142	R/W	1h	Polarity for slv_events_in[78] 0=low
13	POLARITY_141	R/W	1h	Polarity for slv_events_in[77] 0=low
12	POLARITY_140	R/W	1h	Polarity for slv_events_in[76] 0=low
11	POLARITY_139	R/W	1h	Polarity for slv_events_in[75] 0=low
10	POLARITY_138	R/W	1h	Polarity for slv_events_in[74] 0=low
9	POLARITY_137	R/W	1h	Polarity for slv_events_in[73] 0=low
8	POLARITY_136	R/W	1h	Polarity for slv_events_in[72] 0=low
7	POLARITY_135	R/W	1h	Polarity for slv_events_in[71] 0=low
6	POLARITY_134	R/W	1h	Polarity for slv_events_in[70] 0=low
5	POLARITY_133	R/W	1h	Polarity for slv_events_in[69] 0=low
4	POLARITY_132	R/W	1h	Polarity for slv_events_in[68] 0=low
3	POLARITY_131	R/W	1h	Polarity for slv_events_in[67] 0=low
2	POLARITY_130	R/W	1h	Polarity for slv_events_in[66] 0=low
1	POLARITY_129	R/W	1h	Polarity for slv_events_in[65] 0=low
0	POLARITY_128	R/W	1h	Polarity for slv_events_in[64] 0=low

Table 15-706. Register Call Summary for ICSS_INTC_POLARITY_REG4

PRU_ICSS_INTC_INTC Registers PRU_ICSS_INTC_INTC Registers: [0] ICSS_INTC_POLARITY_REG4 Register (Offset = D10h) [reset = FFFFFFFh]: [0]
PRU_ICSSG Local INTC PRU_ICSSG Interrupt Controller Basic Programming Model: [0]

15.7.102 ICSS_INTC_TYPE_REG0 Register (Offset = D80h) [reset = 0h]

ICSS_INTC_TYPE_REG0 is shown in [Figure 15-232](#) and described in [Table 15-708](#).

Return to [Summary Table](#).

Type Register 0

Table 15-707. ICSS_INTC_TYPE_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0D80h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0D80h

Figure 15-232. ICSS_INTC_TYPE_REG0 Register

31	30	29	28	27	26	25	24
TYPE_31	TYPE_30	TYPE_29	TYPE_28	TYPE_27	TYPE_26	TYPE_25	TYPE_24
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
TYPE_23	TYPE_22	TYPE_21	TYPE_20	TYPE_19	TYPE_18	TYPE_17	TYPE_16
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
TYPE_15	TYPE_14	TYPE_13	TYPE_12	TYPE_11	TYPE_10	TYPE_9	TYPE_8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TYPE_7	TYPE_6	TYPE_5	TYPE_4	TYPE_3	TYPE_2	TYPE_1	TYPE_0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-708. ICSS_INTC_TYPE_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TYPE_31	R/W	0h	Type for intr_in[31] 0=level
30	TYPE_30	R/W	0h	Type for intr_in[30] 0=level
29	TYPE_29	R/W	0h	Type for intr_in[29] 0=level
28	TYPE_28	R/W	0h	Type for intr_in[28] 0=level
27	TYPE_27	R/W	0h	Type for intr_in[27] 0=level
26	TYPE_26	R/W	0h	Type for intr_in[26] 0=level
25	TYPE_25	R/W	0h	Type for intr_in[25] 0=level
24	TYPE_24	R/W	0h	Type for intr_in[24] 0=level
23	TYPE_23	R/W	0h	Type for intr_in[23] 0=level
22	TYPE_22	R/W	0h	Type for intr_in[22] 0=level
21	TYPE_21	R/W	0h	Type for intr_in[21] 0=level
20	TYPE_20	R/W	0h	Type for intr_in[20] 0=level

Table 15-708. ICSS_INTC_TYPE_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	TYPE_19	R/W	0h	Type for intr_in[19] 0=level
18	TYPE_18	R/W	0h	Type for intr_in[18] 0=level
17	TYPE_17	R/W	0h	Type for intr_in[17] 0=level
16	TYPE_16	R/W	0h	Type for intr_in[16] 0=level
15	TYPE_15	R/W	0h	Type for intr_in[15] 0=level
14	TYPE_14	R/W	0h	Type for intr_in[14] 0=level
13	TYPE_13	R/W	0h	Type for intr_in[13] 0=level
12	TYPE_12	R/W	0h	Type for intr_in[12] 0=level
11	TYPE_11	R/W	0h	Type for intr_in[11] 0=level
10	TYPE_10	R/W	0h	Type for intr_in[10] 0=level
9	TYPE_9	R/W	0h	Type for intr_in[9] 0=level
8	TYPE_8	R/W	0h	Type for intr_in[8] 0=level
7	TYPE_7	R/W	0h	Type for intr_in[7] 0=level
6	TYPE_6	R/W	0h	Type for intr_in[6] 0=level
5	TYPE_5	R/W	0h	Type for intr_in[5] 0=level
4	TYPE_4	R/W	0h	Type for intr_in[4] 0=level
3	TYPE_3	R/W	0h	Type for intr_in[3] 0=level
2	TYPE_2	R/W	0h	Type for intr_in[2] 0=level
1	TYPE_1	R/W	0h	Type for intr_in[1] 0=level
0	TYPE_0	R/W	0h	Type for intr_in[0] 0=level

Table 15-709. Register Call Summary for ICSS_INTC_TYPE_REG0

PRU_ICSS_INTC_INTC Registers - PRU_ICSS_INTC_INTC Registers: [0] - ICSS_INTC_TYPE_REG0 Register (Offset = D80h) [reset = 0h]: [0]
PRU_ICSSG Local INTC PRU_ICSSG Interrupt Controller Basic Programming Model: [0]

15.7.103 ICSS_INTC_TYPE_REG1 Register (Offset = D84h) [reset = 0h]

ICSS_INTC_TYPE_REG1 is shown in [Figure 15-233](#) and described in [Table 15-711](#).

Return to [Summary Table](#).

Type Register 1

Table 15-710. ICSS_INTC_TYPE_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 0D84h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 0D84h

Figure 15-233. ICSS_INTC_TYPE_REG1 Register

31	30	29	28	27	26	25	24
TYPE_63	TYPE_62	TYPE_61	TYPE_60	TYPE_59	TYPE_58	TYPE_57	TYPE_56
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
TYPE_55	TYPE_54	TYPE_53	TYPE_52	TYPE_51	TYPE_50	TYPE_49	TYPE_48
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
TYPE_47	TYPE_46	TYPE_45	TYPE_44	TYPE_43	TYPE_42	TYPE_41	TYPE_40
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TYPE_39	TYPE_38	TYPE_37	TYPE_36	TYPE_35	TYPE_34	TYPE_33	TYPE_32
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-711. ICSS_INTC_TYPE_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TYPE_63	R/W	0h	Type for intr_in[63] 0=level
30	TYPE_62	R/W	0h	Type for intr_in[62] 0=level
29	TYPE_61	R/W	0h	Type for intr_in[61] 0=level
28	TYPE_60	R/W	0h	Type for intr_in[60] 0=level
27	TYPE_59	R/W	0h	Type for intr_in[59] 0=level
26	TYPE_58	R/W	0h	Type for intr_in[58] 0=level
25	TYPE_57	R/W	0h	Type for intr_in[57] 0=level
24	TYPE_56	R/W	0h	Type for intr_in[56] 0=level
23	TYPE_55	R/W	0h	Type for intr_in[55] 0=level
22	TYPE_54	R/W	0h	Type for intr_in[54] 0=level
21	TYPE_53	R/W	0h	Type for intr_in[53] 0=level
20	TYPE_52	R/W	0h	Type for intr_in[52] 0=level

Table 15-711. ICSS_INTC_TYPE_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	TYPE_51	R/W	0h	Type for intr_in[51] 0=level
18	TYPE_50	R/W	0h	Type for intr_in[50] 0=level
17	TYPE_49	R/W	0h	Type for intr_in[49] 0=level
16	TYPE_48	R/W	0h	Type for intr_in[48] 0=level
15	TYPE_47	R/W	0h	Type for intr_in[47] 0=level
14	TYPE_46	R/W	0h	Type for intr_in[46] 0=level
13	TYPE_45	R/W	0h	Type for intr_in[45] 0=level
12	TYPE_44	R/W	0h	Type for intr_in[44] 0=level
11	TYPE_43	R/W	0h	Type for intr_in[43] 0=level
10	TYPE_42	R/W	0h	Type for intr_in[42] 0=level
9	TYPE_41	R/W	0h	Type for intr_in[41] 0=level
8	TYPE_40	R/W	0h	Type for intr_in[40] 0=level
7	TYPE_39	R/W	0h	Type for intr_in[39] 0=level
6	TYPE_38	R/W	0h	Type for intr_in[38] 0=level
5	TYPE_37	R/W	0h	Type for intr_in[37] 0=level
4	TYPE_36	R/W	0h	Type for intr_in[36] 0=level
3	TYPE_35	R/W	0h	Type for intr_in[35] 0=level
2	TYPE_34	R/W	0h	Type for intr_in[34] 0=level
1	TYPE_33	R/W	0h	Type for intr_in[33] 0=level
0	TYPE_32	R/W	0h	Type for intr_in[32] 0=level

Table 15-712. Register Call Summary for ICSS_INTC_TYPE_REG1

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_TYPE_REG1 Register \(Offset = D84h\) \[reset = 0h\]: \[0\]](#)

15.7.104 ICSS_INTC_TYPE_REG2 Register (Offset = D88h) [reset = 0h]

ICSS_INTC_TYPE_REG2 is shown in [Figure 15-234](#) and described in [Table 15-714](#).

Return to [Summary Table](#).

Type Register 2

Table 15-713. ICSS_INTC_TYPE_REG2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTCLV	0B02 0D88h
PRU_ICSSG1_PR1_ICSS_INTC_INTCLV	0B12 0D88h

Figure 15-234. ICSS_INTC_TYPE_REG2 Register

31	30	29	28	27	26	25	24
TYPE_95	TYPE_94	TYPE_93	TYPE_92	TYPE_91	TYPE_90	TYPE_89	TYPE_88
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
TYPE_87	TYPE_86	TYPE_85	TYPE_84	TYPE_83	TYPE_82	TYPE_81	TYPE_80
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
TYPE_79	TYPE_78	TYPE_77	TYPE_76	TYPE_75	TYPE_74	TYPE_73	TYPE_72
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TYPE_71	TYPE_70	TYPE_69	TYPE_68	TYPE_67	TYPE_66	TYPE_65	TYPE_64
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-714. ICSS_INTC_TYPE_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TYPE_95	R/W	0h	Type for slv_events_in[31] 0=level
30	TYPE_94	R/W	0h	Type for slv_events_in[30] 0=level
29	TYPE_93	R/W	0h	Type for slv_events_in[29] 0=level
28	TYPE_92	R/W	0h	Type for slv_events_in[28] 0=level
27	TYPE_91	R/W	0h	Type for slv_events_in[27] 0=level
26	TYPE_90	R/W	0h	Type for slv_events_in[26] 0=level
25	TYPE_89	R/W	0h	Type for slv_events_in[25] 0=level
24	TYPE_88	R/W	0h	Type for slv_events_in[24] 0=level
23	TYPE_87	R/W	0h	Type for slv_events_in[23] 0=level
22	TYPE_86	R/W	0h	Type for slv_events_in[22] 0=level
21	TYPE_85	R/W	0h	Type for slv_events_in[21] 0=level
20	TYPE_84	R/W	0h	Type for slv_events_in[20] 0=level

Table 15-714. ICSS_INTC_TYPE_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	TYPE_83	R/W	0h	Type for slv_events_in[19] 0=level
18	TYPE_82	R/W	0h	Type for slv_events_in[18] 0=level
17	TYPE_81	R/W	0h	Type for slv_events_in[17] 0=level
16	TYPE_80	R/W	0h	Type for slv_events_in[16] 0=level
15	TYPE_79	R/W	0h	Type for slv_events_in[15] 0=level
14	TYPE_78	R/W	0h	Type for slv_events_in[14] 0=level
13	TYPE_77	R/W	0h	Type for slv_events_in[13] 0=level
12	TYPE_76	R/W	0h	Type for slv_events_in[12] 0=level
11	TYPE_75	R/W	0h	Type for slv_events_in[11] 0=level
10	TYPE_74	R/W	0h	Type for slv_events_in[10] 0=level
9	TYPE_73	R/W	0h	Type for slv_events_in[9] 0=level
8	TYPE_72	R/W	0h	Type for slv_events_in[8] 0=level
7	TYPE_71	R/W	0h	Type for slv_events_in[7] 0=level
6	TYPE_70	R/W	0h	Type for slv_events_in[6] 0=level
5	TYPE_69	R/W	0h	Type for slv_events_in[5] 0=level
4	TYPE_68	R/W	0h	Type for slv_events_in[4] 0=level
3	TYPE_67	R/W	0h	Type for slv_events_in[3] 0=level
2	TYPE_66	R/W	0h	Type for slv_events_in[2] 0=level
1	TYPE_65	R/W	0h	Type for slv_events_in[1] 0=level
0	TYPE_64	R/W	0h	Type for slv_events_in[0] 0=level

Table 15-715. Register Call Summary for ICSS_INTC_TYPE_REG2

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_TYPE_REG2 Register \(Offset = D88h\) \[reset = 0h\]: \[0\]](#)

15.7.105 ICSS_INTC_TYPE_REG3 Register (Offset = D8Ch) [reset = 0h]

ICSS_INTC_TYPE_REG3 is shown in [Figure 15-235](#) and described in [Table 15-717](#).

Return to [Summary Table](#).

Type Register 3

Table 15-716. ICSS_INTC_TYPE_REG3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTCLV	0B02 0D8Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTCLV	0B12 0D8Ch

Figure 15-235. ICSS_INTC_TYPE_REG3 Register

31	30	29	28	27	26	25	24
TYPE_127	TYPE_126	TYPE_125	TYPE_124	TYPE_123	TYPE_122	TYPE_121	TYPE_120
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
TYPE_119	TYPE_118	TYPE_117	TYPE_116	TYPE_115	TYPE_114	TYPE_113	TYPE_112
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
TYPE_111	TYPE_110	TYPE_109	TYPE_108	TYPE_107	TYPE_106	TYPE_105	TYPE_104
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TYPE_103	TYPE_102	TYPE_101	TYPE_100	TYPE_99	TYPE_98	TYPE_97	TYPE_96
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-717. ICSS_INTC_TYPE_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TYPE_127	R/W	0h	Type for slv_events_in[63] 0=level
30	TYPE_126	R/W	0h	Type for slv_events_in[62] 0=level
29	TYPE_125	R/W	0h	Type for slv_events_in[61] 0=level
28	TYPE_124	R/W	0h	Type for slv_events_in[60] 0=level
27	TYPE_123	R/W	0h	Type for slv_events_in[59] 0=level
26	TYPE_122	R/W	0h	Type for slv_events_in[58] 0=level
25	TYPE_121	R/W	0h	Type for slv_events_in[57] 0=level
24	TYPE_120	R/W	0h	Type for slv_events_in[56] 0=level
23	TYPE_119	R/W	0h	Type for slv_events_in[55] 0=level
22	TYPE_118	R/W	0h	Type for slv_events_in[54] 0=level
21	TYPE_117	R/W	0h	Type for slv_events_in[53] 0=level
20	TYPE_116	R/W	0h	Type for slv_events_in[52] 0=level

Table 15-717. ICSS_INTC_TYPE_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	TYPE_115	R/W	0h	Type for slv_events_in[51] 0=level
18	TYPE_114	R/W	0h	Type for slv_events_in[50] 0=level
17	TYPE_113	R/W	0h	Type for slv_events_in[49] 0=level
16	TYPE_112	R/W	0h	Type for slv_events_in[48] 0=level
15	TYPE_111	R/W	0h	Type for slv_events_in[47] 0=level
14	TYPE_110	R/W	0h	Type for slv_events_in[46] 0=level
13	TYPE_109	R/W	0h	Type for slv_events_in[45] 0=level
12	TYPE_108	R/W	0h	Type for slv_events_in[44] 0=level
11	TYPE_107	R/W	0h	Type for slv_events_in[43] 0=level
10	TYPE_106	R/W	0h	Type for slv_events_in[42] 0=level
9	TYPE_105	R/W	0h	Type for slv_events_in[41] 0=level
8	TYPE_104	R/W	0h	Type for slv_events_in[40] 0=level
7	TYPE_103	R/W	0h	Type for slv_events_in[39] 0=level
6	TYPE_102	R/W	0h	Type for slv_events_in[38] 0=level
5	TYPE_101	R/W	0h	Type for slv_events_in[37] 0=level
4	TYPE_100	R/W	0h	Type for slv_events_in[36] 0=level
3	TYPE_99	R/W	0h	Type for slv_events_in[35] 0=level
2	TYPE_98	R/W	0h	Type for slv_events_in[34] 0=level
1	TYPE_97	R/W	0h	Type for slv_events_in[33] 0=level
0	TYPE_96	R/W	0h	Type for slv_events_in[32] 0=level

Table 15-718. Register Call Summary for ICSS_INTC_TYPE_REG3

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_TYPE_REG3 Register \(Offset = D8Ch\) \[reset = 0h\]: \[0\]](#)

15.7.106 ICSS_INTC_TYPE_REG4 Register (Offset = D90h) [reset = 0h]

ICSS_INTC_TYPE_REG4 is shown in [Figure 15-236](#) and described in [Table 15-720](#).

Return to [Summary Table](#).

Type Register 4

Table 15-719. ICSS_INTC_TYPE_REG4 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTCLV	0B02 0D90h
PRU_ICSSG1_PR1_ICSS_INTC_INTCLV	0B12 0D90h

Figure 15-236. ICSS_INTC_TYPE_REG4 Register

31	30	29	28	27	26	25	24
TYPE_159	TYPE_158	TYPE_157	TYPE_156	TYPE_155	TYPE_154	TYPE_153	TYPE_152
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
TYPE_151	TYPE_150	TYPE_149	TYPE_148	TYPE_147	TYPE_146	TYPE_145	TYPE_144
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
TYPE_143	TYPE_142	TYPE_141	TYPE_140	TYPE_139	TYPE_138	TYPE_137	TYPE_136
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TYPE_135	TYPE_134	TYPE_133	TYPE_132	TYPE_131	TYPE_130	TYPE_129	TYPE_128
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-720. ICSS_INTC_TYPE_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TYPE_159	R/W	0h	Type for slv_events_in[95] 0=level
30	TYPE_158	R/W	0h	Type for slv_events_in[94] 0=level
29	TYPE_157	R/W	0h	Type for slv_events_in[93] 0=level
28	TYPE_156	R/W	0h	Type for slv_events_in[92] 0=level
27	TYPE_155	R/W	0h	Type for slv_events_in[91] 0=level
26	TYPE_154	R/W	0h	Type for slv_events_in[90] 0=level
25	TYPE_153	R/W	0h	Type for slv_events_in[89] 0=level
24	TYPE_152	R/W	0h	Type for slv_events_in[88] 0=level
23	TYPE_151	R/W	0h	Type for slv_events_in[87] 0=level
22	TYPE_150	R/W	0h	Type for slv_events_in[86] 0=level
21	TYPE_149	R/W	0h	Type for slv_events_in[85] 0=level
20	TYPE_148	R/W	0h	Type for slv_events_in[84] 0=level

Table 15-720. ICSS_INTC_TYPE_REG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	TYPE_147	R/W	0h	Type for slv_events_in[83] 0=level
18	TYPE_146	R/W	0h	Type for slv_events_in[82] 0=level
17	TYPE_145	R/W	0h	Type for slv_events_in[81] 0=level
16	TYPE_144	R/W	0h	Type for slv_events_in[80] 0=level
15	TYPE_143	R/W	0h	Type for slv_events_in[79] 0=level
14	TYPE_142	R/W	0h	Type for slv_events_in[78] 0=level
13	TYPE_141	R/W	0h	Type for slv_events_in[77] 0=level
12	TYPE_140	R/W	0h	Type for slv_events_in[76] 0=level
11	TYPE_139	R/W	0h	Type for slv_events_in[75] 0=level
10	TYPE_138	R/W	0h	Type for slv_events_in[74] 0=level
9	TYPE_137	R/W	0h	Type for slv_events_in[73] 0=level
8	TYPE_136	R/W	0h	Type for slv_events_in[72] 0=level
7	TYPE_135	R/W	0h	Type for slv_events_in[71] 0=level
6	TYPE_134	R/W	0h	Type for slv_events_in[70] 0=level
5	TYPE_133	R/W	0h	Type for slv_events_in[69] 0=level
4	TYPE_132	R/W	0h	Type for slv_events_in[68] 0=level
3	TYPE_131	R/W	0h	Type for slv_events_in[67] 0=level
2	TYPE_130	R/W	0h	Type for slv_events_in[66] 0=level
1	TYPE_129	R/W	0h	Type for slv_events_in[65] 0=level
0	TYPE_128	R/W	0h	Type for slv_events_in[64] 0=level

Table 15-721. Register Call Summary for ICSS_INTC_TYPE_REG4

PRU_ICSS_INTC_INTC Registers • ICSS_INTC_TYPE_REG4 Register (Offset = D90h) [reset = 0h]: [0] • PRU_ICSS_INTC_INTC Registers: [0]
PRU_ICSSG Local INTC • PRU_ICSSG Interrupt Controller Basic Programming Model: [0]

15.7.107 ICSS_INTC_NEST_LEVEL_REG0 Register (Offset = 1100h) [reset = X]

ICSS_INTC_NEST_LEVEL_REG0 is shown in [Figure 15-237](#) and described in [Table 15-723](#).

Return to [Summary Table](#).

Host Int 0 Nesting Level Register

Table 15-722. ICSS_INTC_NEST_LEVEL_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 1100h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 1100h

Figure 15-237. ICSS_INTC_NEST_LEVEL_REG0 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_0
R/W-X							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT_0							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 15-723. ICSS_INTC_NEST_LEVEL_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_0	R/W	100h	Host Int 0 Nesting Level

Table 15-724. Register Call Summary for ICSS_INTC_NEST_LEVEL_REG0

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_NEST_LEVEL_REG0 Register \(Offset = 1100h\) \[reset = X\]: \[0\]](#)

15.7.108 ICSS_INTC_NEST_LEVEL_REG1 Register (Offset = 1104h) [reset = X]

ICSS_INTC_NEST_LEVEL_REG1 is shown in [Figure 15-238](#) and described in [Table 15-726](#).

Return to [Summary Table](#).

Host Int 1 Nesting Level Register

Table 15-725. ICSS_INTC_NEST_LEVEL_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 1104h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 1104h

Figure 15-238. ICSS_INTC_NEST_LEVEL_REG1 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_1
R/W-X							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT_1							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 15-726. ICSS_INTC_NEST_LEVEL_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_1	R/W	100h	Host Int 1 Nesting Level

Table 15-727. Register Call Summary for ICSS_INTC_NEST_LEVEL_REG1

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_NEST_LEVEL_REG1 Register \(Offset = 1104h\) \[reset = X\]: \[0\]](#)

15.7.109 ICSS_INTC_NEST_LEVEL_REG2 Register (Offset = 1108h) [reset = X]

ICSS_INTC_NEST_LEVEL_REG2 is shown in [Figure 15-239](#) and described in [Table 15-729](#).

Return to [Summary Table](#).

Host Int 2 Nesting Level Register

Table 15-728. ICSS_INTC_NEST_LEVEL_REG2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 1108h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 1108h

Figure 15-239. ICSS_INTC_NEST_LEVEL_REG2 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_2
R/W-X							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT_2							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 15-729. ICSS_INTC_NEST_LEVEL_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_2	R/W	100h	Host Int 2 Nesting Level

Table 15-730. Register Call Summary for ICSS_INTC_NEST_LEVEL_REG2

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_NEST_LEVEL_REG2 Register \(Offset = 1108h\) \[reset = X\]: \[0\]](#)

15.7.110 ICSS_INTC_NEST_LEVEL_REG3 Register (Offset = 110Ch) [reset = X]

ICSS_INTC_NEST_LEVEL_REG3 is shown in [Figure 15-240](#) and described in [Table 15-732](#).

Return to [Summary Table](#).

Host Int 3 Nesting Level Register

Table 15-731. ICSS_INTC_NEST_LEVEL_REG3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 110Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 110Ch

Figure 15-240. ICSS_INTC_NEST_LEVEL_REG3 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_3
R/W-X							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT_3							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 15-732. ICSS_INTC_NEST_LEVEL_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_3	R/W	100h	Host Int 3 Nesting Level

Table 15-733. Register Call Summary for ICSS_INTC_NEST_LEVEL_REG3

- PRU_ICSS_INTC_INTC Registers
- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
 - [ICSS_INTC_NEST_LEVEL_REG3 Register \(Offset = 110Ch\) \[reset = X\]: \[0\]](#)

15.7.111 ICSS_INTC_NEST_LEVEL_REG4 Register (Offset = 1110h) [reset = X]

ICSS_INTC_NEST_LEVEL_REG4 is shown in [Figure 15-241](#) and described in [Table 15-735](#).

Return to [Summary Table](#).

Host Int 4 Nesting Level Register

Table 15-734. ICSS_INTC_NEST_LEVEL_REG4 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 1110h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 1110h

Figure 15-241. ICSS_INTC_NEST_LEVEL_REG4 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_4
R/W-X							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT_4							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 15-735. ICSS_INTC_NEST_LEVEL_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_4	R/W	100h	Host Int 4 Nesting Level

Table 15-736. Register Call Summary for ICSS_INTC_NEST_LEVEL_REG4

- PRU_ICSS_INTC_INTC Registers
- [ICSS_INTC_NEST_LEVEL_REG4 Register \(Offset = 1110h\) \[reset = X\]: \[0\]](#)
 - [PRU_ICSS_INTC_INTC Registers: \[0\]](#)

15.7.112 ICSS_INTC_NEST_LEVEL_REG5 Register (Offset = 1114h) [reset = X]

ICSS_INTC_NEST_LEVEL_REG5 is shown in [Figure 15-242](#) and described in [Table 15-738](#).

Return to [Summary Table](#).

Host Int 5 Nesting Level Register

Table 15-737. ICSS_INTC_NEST_LEVEL_REG5 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 1114h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 1114h

Figure 15-242. ICSS_INTC_NEST_LEVEL_REG5 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_5
R/W-X							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT_5							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 15-738. ICSS_INTC_NEST_LEVEL_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_5	R/W	100h	Host Int 5 Nesting Level

Table 15-739. Register Call Summary for ICSS_INTC_NEST_LEVEL_REG5

- PRU_ICSS_INTC_INTC Registers
- [ICSS_INTC_NEST_LEVEL_REG5 Register \(Offset = 1114h\) \[reset = X\]: \[0\]](#)
 - [PRU_ICSS_INTC_INTC Registers: \[0\]](#)

15.7.113 ICSS_INTC_NEST_LEVEL_REG6 Register (Offset = 1118h) [reset = X]

ICSS_INTC_NEST_LEVEL_REG6 is shown in [Figure 15-243](#) and described in [Table 15-741](#).

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Host Int 6 Nesting Level Register

Table 15-740. ICSS_INTC_NEST_LEVEL_REG6 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 1118h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 1118h

Figure 15-243. ICSS_INTC_NEST_LEVEL_REG6 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_6
R/W-X							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT_6							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 15-741. ICSS_INTC_NEST_LEVEL_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_6	R/W	100h	Host Int 6 Nesting Level

Table 15-742. Register Call Summary for ICSS_INTC_NEST_LEVEL_REG6

- PRU_ICSS_INTC_INTC Registers
- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
 - [ICSS_INTC_NEST_LEVEL_REG6 Register \(Offset = 1118h\) \[reset = X\]: \[0\]](#)

15.7.114 ICSS_INTC_NEST_LEVEL_REG7 Register (Offset = 111Ch) [reset = X]

ICSS_INTC_NEST_LEVEL_REG7 is shown in [Figure 15-244](#) and described in [Table 15-744](#).

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Host Int 7 Nesting Level Register

Table 15-743. ICSS_INTC_NEST_LEVEL_REG7 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 111Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 111Ch

Figure 15-244. ICSS_INTC_NEST_LEVEL_REG7 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_7
R/W-X							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT_7							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 15-744. ICSS_INTC_NEST_LEVEL_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_7	R/W	100h	Host Int 7 Nesting Level

Table 15-745. Register Call Summary for ICSS_INTC_NEST_LEVEL_REG7

- PRU_ICSS_INTC_INTC Registers
- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
 - [ICSS_INTC_NEST_LEVEL_REG7 Register \(Offset = 111Ch\) \[reset = X\]: \[0\]](#)

15.7.115 ICSS_INTC_NEST_LEVEL_REG8 Register (Offset = 1120h) [reset = X]

ICSS_INTC_NEST_LEVEL_REG8 is shown in [Figure 15-245](#) and described in [Table 15-747](#).

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Host Int 8 Nesting Level Register

Table 15-746. ICSS_INTC_NEST_LEVEL_REG8 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 1120h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 1120h

Figure 15-245. ICSS_INTC_NEST_LEVEL_REG8 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_8
R/W-X							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT_8							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 15-747. ICSS_INTC_NEST_LEVEL_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_8	R/W	100h	Host Int 8 Nesting Level

Table 15-748. Register Call Summary for ICSS_INTC_NEST_LEVEL_REG8

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_NEST_LEVEL_REG8 Register \(Offset = 1120h\) \[reset = X\]: \[0\]](#)

15.7.116 ICSS_INTC_NEST_LEVEL_REG9 Register (Offset = 1124h) [reset = X]

ICSS_INTC_NEST_LEVEL_REG9 is shown in [Figure 15-246](#) and described in [Table 15-750](#).

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Host Int 9 Nesting Level Register

Table 15-749. ICSS_INTC_NEST_LEVEL_REG9 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 1124h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 1124h

Figure 15-246. ICSS_INTC_NEST_LEVEL_REG9 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_9
R/W-X							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT_9							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 15-750. ICSS_INTC_NEST_LEVEL_REG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_9	R/W	100h	Host Int 9 Nesting Level

Table 15-751. Register Call Summary for ICSS_INTC_NEST_LEVEL_REG9

- PRU_ICSS_INTC_INTC Registers
- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
 - [ICSS_INTC_NEST_LEVEL_REG9 Register \(Offset = 1124h\) \[reset = X\]: \[0\]](#)

15.7.117 ICSS_INTC_NEST_LEVEL_REG10 Register (Offset = 1128h) [reset = X]

ICSS_INTC_NEST_LEVEL_REG10 is shown in [Figure 15-247](#) and described in [Table 15-753](#).

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Host Int 10 Nesting Level Register

Table 15-752. ICSS_INTC_NEST_LEVEL_REG10 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 1128h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 1128h

Figure 15-247. ICSS_INTC_NEST_LEVEL_REG10 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_10
R/W-X							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT_10							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 15-753. ICSS_INTC_NEST_LEVEL_REG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_10	R/W	100h	Host Int 10 Nesting Level

Table 15-754. Register Call Summary for ICSS_INTC_NEST_LEVEL_REG10

PRU_ICSS_INTC_INTC Registers
ICSS_INTC_NEST_LEVEL_REG10 Register (Offset = 1128h) [reset = X]: [0] PRU_ICSS_INTC_INTC Registers: [0]

15.7.118 ICSS_INTC_NEST_LEVEL_REG11 Register (Offset = 112Ch) [reset = X]

ICSS_INTC_NEST_LEVEL_REG11 is shown in [Figure 15-248](#) and described in [Table 15-756](#).

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Host Int 11 Nesting Level Register

Table 15-755. ICSS_INTC_NEST_LEVEL_REG11 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 112Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 112Ch

Figure 15-248. ICSS_INTC_NEST_LEVEL_REG11 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_11
R/W-X							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT_11							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 15-756. ICSS_INTC_NEST_LEVEL_REG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_11	R/W	100h	Host Int 11 Nesting Level

Table 15-757. Register Call Summary for ICSS_INTC_NEST_LEVEL_REG11

PRU_ICSS_INTC_INTC Registers

- [ICSS_INTC_NEST_LEVEL_REG11 Register \(Offset = 112Ch\) \[reset = X\]: \[0\]](#)
- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)

15.7.119 ICSS_INTC_NEST_LEVEL_REG12 Register (Offset = 1130h) [reset = X]

ICSS_INTC_NEST_LEVEL_REG12 is shown in [Figure 15-249](#) and described in [Table 15-759](#).

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Host Int 11 Nesting Level Register

Table 15-758. ICSS_INTC_NEST_LEVEL_REG12 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 1130h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 1130h

Figure 15-249. ICSS_INTC_NEST_LEVEL_REG12 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_12
R/W-X							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT_12							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 15-759. ICSS_INTC_NEST_LEVEL_REG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_12	R/W	100h	Host Int 12 Nesting Level

Table 15-760. Register Call Summary for ICSS_INTC_NEST_LEVEL_REG12

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_NEST_LEVEL_REG12 Register \(Offset = 1130h\) \[reset = X\]: \[0\]](#)

15.7.120 ICSS_INTC_NEST_LEVEL_REG13 Register (Offset = 1134h) [reset = X]

ICSS_INTC_NEST_LEVEL_REG13 is shown in [Figure 15-250](#) and described in [Table 15-762](#).

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Host Int 11 Nesting Level Register

Table 15-761. ICSS_INTC_NEST_LEVEL_REG13 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 1134h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 1134h

Figure 15-250. ICSS_INTC_NEST_LEVEL_REG13 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_13
R/W-X							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT_13							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 15-762. ICSS_INTC_NEST_LEVEL_REG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_13	R/W	100h	Host Int 13 Nesting Level

Table 15-763. Register Call Summary for ICSS_INTC_NEST_LEVEL_REG13

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_NEST_LEVEL_REG13 Register \(Offset = 1134h\) \[reset = X\]: \[0\]](#)

15.7.121 ICSS_INTC_NEST_LEVEL_REG14 Register (Offset = 1138h) [reset = X]

ICSS_INTC_NEST_LEVEL_REG14 is shown in [Figure 15-251](#) and described in [Table 15-765](#).

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Host Int 11 Nesting Level Register

Table 15-764. ICSS_INTC_NEST_LEVEL_REG14 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 1138h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 1138h

Figure 15-251. ICSS_INTC_NEST_LEVEL_REG14 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_14
R/W-X							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT_14							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 15-765. ICSS_INTC_NEST_LEVEL_REG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_14	R/W	100h	Host Int 14 Nesting Level

Table 15-766. Register Call Summary for ICSS_INTC_NEST_LEVEL_REG14

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_NEST_LEVEL_REG14 Register \(Offset = 1138h\) \[reset = X\]: \[0\]](#)

15.7.122 ICSS_INTC_NEST_LEVEL_REG15 Register (Offset = 113Ch) [reset = X]

ICSS_INTC_NEST_LEVEL_REG15 is shown in [Figure 15-252](#) and described in [Table 15-768](#).

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Host Int 11 Nesting Level Register

Table 15-767. ICSS_INTC_NEST_LEVEL_REG15 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 113Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 113Ch

Figure 15-252. ICSS_INTC_NEST_LEVEL_REG15 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_15
R/W-X							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT_15							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 15-768. ICSS_INTC_NEST_LEVEL_REG15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_15	R/W	100h	Host Int 15 Nesting Level

Table 15-769. Register Call Summary for ICSS_INTC_NEST_LEVEL_REG15

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_NEST_LEVEL_REG15 Register \(Offset = 113Ch\) \[reset = X\]: \[0\]](#)

15.7.123 ICSS_INTC_NEST_LEVEL_REG16 Register (Offset = 1140h) [reset = X]

ICSS_INTC_NEST_LEVEL_REG16 is shown in Figure 15-253 and described in Table 15-771.

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Host Int 11 Nesting Level Register

Table 15-770. ICSS_INTC_NEST_LEVEL_REG16 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 1140h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 1140h

Figure 15-253. ICSS_INTC_NEST_LEVEL_REG16 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_16
R/W-X							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT_16							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 15-771. ICSS_INTC_NEST_LEVEL_REG16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_16	R/W	100h	Host Int 16 Nesting Level

Table 15-772. Register Call Summary for ICSS_INTC_NEST_LEVEL_REG16

PRU_ICSS_INTC_INTC Registers

- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)
- [ICSS_INTC_NEST_LEVEL_REG16 Register \(Offset = 1140h\) \[reset = X\]: \[0\]](#)

15.7.124 ICSS_INTC_NEST_LEVEL_REG17 Register (Offset = 1144h) [reset = X]

ICSS_INTC_NEST_LEVEL_REG17 is shown in [Figure 15-254](#) and described in [Table 15-774](#).

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Host Int 11 Nesting Level Register

Table 15-773. ICSS_INTC_NEST_LEVEL_REG17 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 1144h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 1144h

Figure 15-254. ICSS_INTC_NEST_LEVEL_REG17 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_17
R/W-X							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT_17							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 15-774. ICSS_INTC_NEST_LEVEL_REG17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_17	R/W	100h	Host Int 17 Nesting Level

Table 15-775. Register Call Summary for ICSS_INTC_NEST_LEVEL_REG17

PRU_ICSS_INTC_INTC Registers
PRU_ICSS_INTC_INTC Registers: [0] ICSS_INTC_NEST_LEVEL_REG17 Register (Offset = 1144h) [reset = X]: [0]

15.7.125 ICSS_INTC_NEST_LEVEL_REG18 Register (Offset = 1148h) [reset = X]

ICSS_INTC_NEST_LEVEL_REG18 is shown in [Figure 15-255](#) and described in [Table 15-777](#).

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Host Int 11 Nesting Level Register

Table 15-776. ICSS_INTC_NEST_LEVEL_REG18 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 1148h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 1148h

Figure 15-255. ICSS_INTC_NEST_LEVEL_REG18 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_18
R/W-X							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT_18							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 15-777. ICSS_INTC_NEST_LEVEL_REG18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_18	R/W	100h	Host Int 18 Nesting Level

Table 15-778. Register Call Summary for ICSS_INTC_NEST_LEVEL_REG18

PRU_ICSS_INTC_INTC Registers

- [ICSS_INTC_NEST_LEVEL_REG18 Register \(Offset = 1148h\) \[reset = X\]: \[0\]](#)
- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)

15.7.126 ICSS_INTC_NEST_LEVEL_REG19 Register (Offset = 114Ch) [reset = X]

ICSS_INTC_NEST_LEVEL_REG19 is shown in [Figure 15-256](#) and described in [Table 15-780](#).

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Host Int 11 Nesting Level Register

Table 15-779. ICSS_INTC_NEST_LEVEL_REG19 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 114Ch
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 114Ch

Figure 15-256. ICSS_INTC_NEST_LEVEL_REG19 Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W-X	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_19
R/W-X							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT_19							
R/W-100h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 15-780. ICSS_INTC_NEST_LEVEL_REG19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	X	Nesting Level Override Automatic
30-9	RESERVED	R/W	X	
8-0	NEST_HINT_19	R/W	100h	Host Int 19 Nesting Level

Table 15-781. Register Call Summary for ICSS_INTC_NEST_LEVEL_REG19

- PRU_ICSS_INTC_INTC Registers
- [ICSS_INTC_NEST_LEVEL_REG19 Register \(Offset = 114Ch\) \[reset = X\]: \[0\]](#)
 - [PRU_ICSS_INTC_INTC Registers: \[0\]](#)

15.7.127 ICSS_INTC_ENABLE_HINT_REG0 Register (Offset = 1500h) [reset = X]

ICSS_INTC_ENABLE_HINT_REG0 is shown in [Figure 15-257](#) and described in [Table 15-783](#).

Return to [Summary Table](#).

Host Int Enable Register 0

Table 15-782. ICSS_INTC_ENABLE_HINT_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_INTC_INTC_SLV	0B02 1500h
PRU_ICSSG1_PR1_ICSS_INTC_INTC_SLV	0B12 1500h

Figure 15-257. ICSS_INTC_ENABLE_HINT_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				ENABLE_HINT_19	ENABLE_HINT_18	ENABLE_HINT_17	ENABLE_HINT_16
R/W-X				R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
ENABLE_HINT_15	ENABLE_HINT_14	ENABLE_HINT_13	ENABLE_HINT_12	ENABLE_HINT_11	ENABLE_HINT_10	ENABLE_HINT_9	ENABLE_HINT_8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
ENABLE_HINT_7	ENABLE_HINT_6	ENABLE_HINT_5	ENABLE_HINT_4	ENABLE_HINT_3	ENABLE_HINT_2	ENABLE_HINT_1	ENABLE_HINT_0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-783. ICSS_INTC_ENABLE_HINT_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19	ENABLE_HINT_19	R/W	0h	Enable for Host Int 19
18	ENABLE_HINT_18	R/W	0h	Enable for Host Int 18
17	ENABLE_HINT_17	R/W	0h	Enable for Host Int 17
16	ENABLE_HINT_16	R/W	0h	Enable for Host Int 16
15	ENABLE_HINT_15	R/W	0h	Enable for Host Int 15
14	ENABLE_HINT_14	R/W	0h	Enable for Host Int 14
13	ENABLE_HINT_13	R/W	0h	Enable for Host Int 13
12	ENABLE_HINT_12	R/W	0h	Enable for Host Int 12
11	ENABLE_HINT_11	R/W	0h	Enable for Host Int 11
10	ENABLE_HINT_10	R/W	0h	Enable for Host Int 10
9	ENABLE_HINT_9	R/W	0h	Enable for Host Int 9
8	ENABLE_HINT_8	R/W	0h	Enable for Host Int 8
7	ENABLE_HINT_7	R/W	0h	Enable for Host Int 7
6	ENABLE_HINT_6	R/W	0h	Enable for Host Int 6
5	ENABLE_HINT_5	R/W	0h	Enable for Host Int 5
4	ENABLE_HINT_4	R/W	0h	Enable for Host Int 4
3	ENABLE_HINT_3	R/W	0h	Enable for Host Int 3
2	ENABLE_HINT_2	R/W	0h	Enable for Host Int 2

Table 15-783. ICSS_INTC_ENABLE_HINT_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ENABLE_HINT_1	R/W	0h	Enable for Host Int 1
0	ENABLE_HINT_0	R/W	0h	Enable for Host Int 0

Table 15-784. Register Call Summary for ICSS_INTC_ENABLE_HINT_REG0

PRU_ICSS_INTC_INTC Registers

- [ICSS_INTC_ENABLE_HINT_REG0 Register \(Offset = 1500h\) \[reset = X\]: \[0\]](#)
- [PRU_ICSS_INTC_INTC Registers: \[0\]](#)

15.8 PRU_UART_UART0 Registers

Table 15-786 lists the memory-mapped registers for the PRU_UART_UART0 registers. All register offset addresses not listed in Table 15-786 should be considered as reserved locations and the register contents should not be modified.

Table 15-785. PRU_UART_UART0 Instances

Instance	Base Address
PRU_ICSSG0_PR1_ICSS_UART_UART_SLV	0B02 8000h
PRU_ICSSG1_PR1_ICSS_UART_UART_SLV	0B12 8000h

Table 15-786. PRU_UART_UART0 Registers

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_ICSS_UART_UART_SLV Physical Address	PRU_ICSSG1_PR1_ICSS_UART_UART_SLV Physical Address
0h	UART_RBR_TBR	Receive and Transmit Buffer Registers	0B02 8000h	0B12 8000h
4h	UART_INT_EN	UART Interrupt Enable Register	0B02 8004h	0B12 8004h
8h	UART_INT_FIFO	Interrupt Identification Register / FIFO Control Register	0B02 8008h	0B12 8008h
Ch	UART_LCTR	Line Control Register	0B02 800Ch	0B12 800Ch
10h	UART_MCTR	Modem Control Register	0B02 8010h	0B12 8010h
14h	UART_LSR1	Line Status Register1	0B02 8014h	0B12 8014h
18h	UART_MSR	Modem Status Register	0B02 8018h	0B12 8018h
1Ch	UART_SCRATCH	UART Scratch Register	0B02 801Ch	0B12 801Ch
20h	UART_DIVLSB	UART Divisor Register	0B02 8020h	0B12 8020h
24h	UART_DIVMSB	UART Divisor Register	0B02 8024h	0B12 8024h
28h	UART_PID	Peripheral ID Register	0B02 8028h	0B12 8028h
30h	UART_PWR	UART Power Management and Emulation Register	0B02 8030h	0B12 8030h
34h	UART_MODE	UART Mode Definition Register	0B02 8034h	0B12 8034h

15.8.1 UART_RBR_TBR Register (Offset = 0h) [reset = X]

UART_RBR_TBR is shown in [Figure 15-258](#) and described in [Table 15-788](#).

Return to [Summary Table](#).

UART_RBR_TBR Registers

Table 15-787. UART_RBR_TBR Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_UART_UART_SLV	0B02 8000h
PRU_ICSSG1_PR1_ICSS_UART_UART_SLV	0B12 8000h

Figure 15-258. UART_RBR_TBR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														TBR_DATA							RBR_DATA										
R/W-X														W-0h							R-0h										

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 15-788. UART_RBR_TBR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-8	TBR_DATA	W	0h	Transmit Buffer Register
7-0	RBR_DATA	R	0h	Receive Buffer Register

Table 15-789. Register Call Summary for UART_RBR_TBR

PRU_UART_UART0 Registers
• UART_RBR_TBR Register (Offset = 0h) [reset = X]: [0] [1] • PRU_UART_UART0 Registers: [0]
PRU_ICSSG UART Environment
• PRU_ICSSG UART Transmission Protocol: [0] • PRU_ICSSG UART Reception Protocol: [0]
PRU_ICSSG UART Module
• PRU_ICSSG UART Functional Description:
PRU_ICSSG UART Functional Description
• PRU_ICSSG UART Interrupt Support: • PRU_ICSSG UART DMA Event Support: [0] [1] • PRU_ICSSG UART FIFO Poll Mode: [0] • PRU_ICSSG UART FIFO Interrupt Mode: [0]

15.8.2 UART_INT_EN Register (Offset = 4h) [reset = X]

UART_INT_EN is shown in [Figure 15-259](#) and described in [Table 15-791](#).

Return to [Summary Table](#).

UART Interrupt Enable Register

Table 15-790. UART_INT_EN Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_UART_UART_SLV	0B02 8004h
PRU_ICSSG1_PR1_ICSS_UART_UART_SLV	0B12 8004h

Figure 15-259. UART_INT_EN Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				EDSSI	ELSI	ETBEI	ERBI
R/W-X				R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-791. UART_INT_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3	EDSSI	R/W	0h	Enable for Modem Status Interrupt
2	ELSI	R/W	0h	Enable for Receiver Line Status Interrupt
1	ETBEI	R/W	0h	Enable for Transmitter Holding Register Empty Interrupt
0	ERBI	R/W	0h	Enable for Receiver Data Available Interrupt

Table 15-792. Register Call Summary for UART_INT_EN

PRU_UART_UART0 Registers UART_INT_EN Register (Offset = 4h) [reset = X]: [0] PRU_UART_UART0 Registers: [0]
PRU_ICSSG UART Environment PRU_ICSSG UART Transmission Protocol: [0] PRU_ICSSG UART Reception Protocol: [0]
PRU_ICSSG UART Functional Description PRU_ICSSG UART Interrupt Events and Requests: [0] PRU_ICSSG UART Interrupt Support: PRU_ICSSG UART FIFO Poll Mode: [0] PRU_ICSSG UART FIFO Interrupt Mode: [0] [1]

15.8.3 UART_INT_FIFO Register (Offset = 8h) [reset = X]

UART_INT_FIFO is shown in Figure 15-260 and described in Table 15-794.

Return to [Summary Table](#).

Interrupt Identification Register / FIFO Control Register

Table 15-793. UART_INT_FIFO Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_UART_UART_SLV	0B02 8008h
PRU_ICSSG1_PR1_ICSS_UART_UART_SLV	0B12 8008h

Figure 15-260. UART_INT_FIFO Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
FCR_RXFIFTL	RESERVED			FCR_DMAMODE1	FCR_TXCLR	FCR_RXCLR	FCR_FIFOEN
W-0h	R/W-X			W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
IIR_FIFOEN	RESERVED			IIR_INTID		IIR_IPEND	
R-0h	R/W-X			R-0h		R-1h	

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 15-794. UART_INT_FIFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-14	FCR_RXFIFTL	W	0h	Receiver Trigger Level
13-12	RESERVED	R/W	X	
11	FCR_DMAMODE1	W	0h	DMA Mode Select
10	FCR_TXCLR	W	0h	Transmitter FIFO Reset
9	FCR_RXCLR	W	0h	Receiver FIFO Reset
8	FCR_FIFOEN	W	0h	FIFO Enable Register
7-6	IIR_FIFOEN	R	0h	FIFOs enabled
5-4	RESERVED	R/W	X	
3-1	IIR_INTID	R	0h	Interrupt Type
0	IIR_IPEND	R	1h	Receiver Data Available Interrupt Pending

Table 15-795. Register Call Summary for UART_INT_FIFO

PRU_UART_UART0 Registers
- UART_INT_FIFO Register (Offset = 8h) [reset = X]: [0] - PRU_UART_UART0 Registers: [0]
PRU_ICSSG UART Environment
- PRU_ICSSG UART Transmission Protocol: [0] [1] - PRU_ICSSG UART Reception Protocol: [0]

Table 15-795. Register Call Summary for UART_INT_FIFO (continued)

PRU_ICSSG UART Module PRU_ICSSG UART Functional Description:
PRU_ICSSG UART Functional Description PRU_ICSSG UART Interrupt Events and Requests: [0] [1] [2] PRU_ICSSG UART Interrupt Support: PRU_ICSSG UART FIFO Poll Mode: [0] [1] [2] PRU_ICSSG UART FIFO Interrupt Mode: [0] [1] [2] PRU_ICSSG UART DMA Event Support: [0] PRU_ICSSG UART Emulation Considerations: [0]

15.8.4 UART_LCTR Register (Offset = Ch) [reset = X]

UART_LCTR is shown in [Figure 15-261](#) and described in [Table 15-797](#).

Return to [Summary Table](#).

Line Control Register

Table 15-796. UART_LCTR Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_UART_UART_SLV	0B02 800Ch
PRU_ICSSG1_PR1_ICSS_UART_UART_SLV	0B12 800Ch

Figure 15-261. UART_LCTR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
DLAB	BC	SP	EPS	PEN	STB	WLS1	WLS0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-797. UART_LCTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7	DLAB	R/W	0h	Divisor Latch Access Bit
6	BC	R/W	0h	Break Control
5	SP	R/W	0h	Stick Parity
4	EPS	R/W	0h	Even Parity Select
3	PEN	R/W	0h	Parity Enable
2	STB	R/W	0h	Number of Stop Bits
1	WLS1	R/W	0h	Word Length Select Bit 1
0	WLS0	R/W	0h	Word Length Select Bit 0

Table 15-798. Register Call Summary for UART_LCTR

PRU_UART_UART0 Registers
PRU_UART_UART0 Registers: [0] UART_LCTR Register (Offset = Ch) [reset = X]: [0]
PRU_ICSSG UART Environment
Frame Formatting: [0] [1] [2] [3] [4] [5] PRU_ICSSG UART Transmission Protocol: [0] PRU_ICSSG UART Reception Protocol: [0]
PRU_ICSSG UART Functional Description
PRU_ICSSG UART FIFO Interrupt Mode: [0]

15.8.5 UART_MCTR Register (Offset = 10h) [reset = X]

UART_MCTR is shown in [Figure 15-262](#) and described in [Table 15-800](#).

Return to [Summary Table](#).

Modem Control Register

Table 15-799. UART_MCTR Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_UART_UART_SLV	0B02 8010h
PRU_ICSSG1_PR1_ICSS_UART_UART_SLV	0B12 8010h

Figure 15-262. UART_MCTR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED		AFE	LOOP	OUT2	OUT1	RTS	DTR
R/W-X		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-800. UART_MCTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	X	
5	AFE	R/W	0h	Autoflow Control Enable
4	LOOP	R/W	0h	LOOP Bit
3	OUT2	R/W	0h	Out2 Bit
2	OUT1	R/W	0h	Out1 Bit
1	RTS	R/W	0h	Ready to Send
0	DTR	R/W	0h	Data Terminal Ready

Table 15-801. Register Call Summary for UART_MCTR

PRU_UART_UART0 Registers UART_MCTR Register (Offset = 10h) [reset = X]: [0] PRU_UART_UART0 Registers: [0]
PRU_ICSSG UART Functional Description PRU_ICSSG UART Autoflow Control: [0] PRU_ICSSG UART Loopback Control: [0]

15.8.6 UART_LSR1 Register (Offset = 14h) [reset = X]

UART_LSR1 is shown in [Figure 15-263](#) and described in [Table 15-803](#).

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Line Status Register1

Table 15-802. UART_LSR1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_UART_UART_SLV	0B02 8014h
PRU_ICSSG1_PR1_ICSS_UART_UART_SLV	0B12 8014h

Figure 15-263. UART_LSR1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RXFIFOE	TEMT	THRE	BI	FE	PE	OE	DR
R-0h	R-1h	R-1h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 15-803. UART_LSR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	X	
7	RXFIFOE	R	0h	Receiver FIFO Error
6	TEMT	R	1h	Transmitter Empty
5	THRE	R	1h	Transmitter Holding Register
4	BI	R	0h	Break Interrupt
3	FE	R	0h	Framing Error
2	PE	R	0h	Parity Error
1	OE	R	0h	Overrun Error
0	DR	R	0h	Data Ready

Table 15-804. Register Call Summary for UART_LSR1

PRU_UART_UART0 Registers
• UART_LSR1 Register (Offset = 14h) [reset = X]: [0] • PRU_UART_UART0 Registers: [0]
PRU_ICSSG UART Module
• PRU_ICSSG UART Functional Description:
PRU_ICSSG UART Functional Description
• PRU_ICSSG UART Interrupt Support: • PRU_ICSSG UART FIFO Poll Mode: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] • PRU_ICSSG UART FIFO Interrupt Mode: [0]

15.8.7 UART_MSR Register (Offset = 18h) [reset = X]

UART_MSR is shown in [Figure 15-264](#) and described in [Table 15-806](#).

Return to [Summary Table](#).

Modem Status Register

Table 15-805. UART_MSR Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_UART_UART_SLV	0B02 8018h
PRU_ICSSG1_PR1_ICSS_UART_UART_SLV	0B12 8018h

Figure 15-264. UART_MSR Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
CD	RI	DSR	CTS	DCD	TERI	DDSR	DCTS
R-X	R-X	R-X	R-X	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 15-806. UART_MSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	X	
7	CD	R	X	Carrier Detect
6	RI	R	X	Ring Indicator
5	DSR	R	X	Data Set Ready
4	CTS	R	X	Clear To Send
3	DCD	R	0h	Delta Carrier Detect
2	TERI	R	0h	Trailing Edge Ring Indicator
1	DDSR	R	0h	Delta Set Ready
0	DCTS	R	0h	Delta Clear To Send

Table 15-807. Register Call Summary for UART_MSR

PRU_UART_UART0 Registers

- [UART_MSR Register \(Offset = 18h\) \[reset = X\]: \[0\]](#)
- [PRU_UART_UART0 Registers: \[0\]](#)

15.8.8 UART_SCRATCH Register (Offset = 1Ch) [reset = X]

UART_SCRATCH is shown in [Figure 15-265](#) and described in [Table 15-809](#).

Return to [Summary Table](#).

UART Scratch Register

Table 15-808. UART_SCRATCH Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_UART_UART_SLV	0B02 801Ch
PRU_ICSSG1_PR1_ICSS_UART_UART_SLV	0B12 801Ch

Figure 15-265. UART_SCRATCH Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DATA							
R/W-X																								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-809. UART_SCRATCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	DATA	R/W	0h	Scratch Register Bits

Table 15-810. Register Call Summary for UART_SCRATCH

PRU_UART_UART0 Registers

- [PRU_UART_UART0 Registers: \[0\]](#)
- [UART_SCRATCH Register \(Offset = 1Ch\) \[reset = X\]: \[0\]](#)

15.8.9 UART_DIVLSB Register (Offset = 20h) [reset = X]

UART_DIVLSB is shown in [Figure 15-266](#) and described in [Table 15-812](#).

Return to [Summary Table](#).

UART Divisor Register

Table 15-811. UART_DIVLSB Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_UART_UART_SLV	0B02 8020h
PRU_ICSSG1_PR1_ICSS_UART_UART_SLV	0B12 8020h

Figure 15-266. UART_DIVLSB Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DLL							
R/W-X																								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-812. UART_DIVLSB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	DLL	R/W	0h	Divisor Latch [LSB]

Table 15-813. Register Call Summary for UART_DIVLSB

PRU_UART_UART0 Registers
PRU_UART_UART0 Registers: [0] UART_DIVLSB Register (Offset = 20h) [reset = X]: [0]
PRU_ICSSG UART Environment
PRU_ICSSG UART Clock Generation and Control: [0]

15.8.10 UART_DIVMSB Register (Offset = 24h) [reset = X]

UART_DIVMSB is shown in [Figure 15-267](#) and described in [Table 15-815](#).

Return to [Summary Table](#).

UART Divisor Register

Table 15-814. UART_DIVMSB Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_UART_UART_SLV	0B02 8024h
PRU_ICSSG1_PR1_ICSS_UART_UART_SLV	0B12 8024h

Figure 15-267. UART_DIVMSB Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DLH							
R/W-X																								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-815. UART_DIVMSB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	DLH	R/W	0h	Divisor Latch [MSB]

Table 15-816. Register Call Summary for UART_DIVMSB

PRU_UART_UART0 Registers
PRU_UART_UART0 Registers: [0] UART_DIVMSB Register (Offset = 24h) [reset = X]: [0]
PRU_ICSSG UART Environment
PRU_ICSSG UART Clock Generation and Control: [0]

15.8.11 UART_PID Register (Offset = 28h) [reset = 44141102h]

UART_PID is shown in [Figure 15-268](#) and described in [Table 15-818](#).

Return to [Summary Table](#).

Peripheral ID Register

Table 15-817. UART_PID Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_UART_UART_SLV	0B02 8028h
PRU_ICSSG1_PR1_ICSS_UART_UART_SLV	0B12 8028h

Figure 15-268. UART_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID																															
R-44141102h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-818. UART_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PID	R	44141102h	

Table 15-819. Register Call Summary for UART_PID

PRU_UART_UART0 Registers

- [UART_PID Register \(Offset = 28h\) \[reset = 44141102h\]: \[0\]](#)
- [PRU_UART_UART0 Registers: \[0\]](#)

15.8.12 UART_PWR Register (Offset = 30h) [reset = X]

UART_PWR is shown in [Figure 15-269](#) and described in [Table 15-821](#).

Return to [Summary Table](#).

UART PowerManagement and Emulation Register

Table 15-820. UART_PWR Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_UART_UART_SLV	0B02 8030h
PRU_ICSSG1_PR1_ICSS_UART_UART_SLV	0B12 8030h

Figure 15-269. UART_PWR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
URST	UTRST	URRST	RESERVED				
R/W-0h	R/W-0h	R/W-0h	R/W-X				
7	6	5	4	3	2	1	0
RESERVED						RES	FREE
R/W-X						R-1h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-821. UART_PWR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	URST	R/W	0h	UART Reset
14	UTRST	R/W	0h	UART Transmitter Reset
13	URRST	R/W	0h	UART Receiver Reset
12-2	RESERVED	R/W	X	
1	RES	R	1h	Free
0	FREE	R/W	0h	Free

Table 15-822. Register Call Summary for UART_PWR

PRU_UART_UART0 Registers
UART_PWR Register (Offset = 30h) [reset = X]: [0] PRU_UART_UART0 Registers: [0]
PRU_ICSSG UART Module
PRU_ICSSG UART Functional Description:
PRU_ICSSG UART Functional Description
PRU_ICSSG UART Software Reset Considerations: [0] PRU_ICSSG UART DMA Event Support: [0] PRU_ICSSG UART Emulation Considerations: [0] [1] [2] [3]

15.8.13 UART_MODE Register (Offset = 34h) [reset = X]

UART_MODE is shown in Figure 15-270 and described in Table 15-824.

Return to [Summary Table](#).

UART Mode Definition Register

Table 15-823. UART_MODE Instances

Instance	Physical Address
PRU_ICSSG0_PR1_ICSS_UART_UART_SLV	0B02 8034h
PRU_ICSSG1_PR1_ICSS_UART_UART_SLV	0B12 8034h

Figure 15-270. UART_MODE Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							OSM_SEL
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-824. UART_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	OSM_SEL	R/W	0h	Oversampling Mode Select

Table 15-825. Register Call Summary for UART_MODE

PRU_UART_UART0 Registers
- UART_MODE Register (Offset = 34h) [reset = X]: [0] - PRU_UART_UART0 Registers: [0]
PRU_ICSSG UART Environment
PRU_ICSSG UART Clock Generation and Control: [0]

15.9 PRU_IEP_IEP Registers

Table 15-827 lists the memory-mapped registers for the PRU_IEP_IEP registers. All register offset addresses not listed in Table 15-827 should be considered as reserved locations and the register contents should not be modified.

Table 15-826. PRU_IEP_IEP Instances

Instance	Base Address
PRU_ICSSG0_IEP0	0B02 E000h
PRU_ICSSG0_IEP1	0B02 F000h
PRU_ICSSG1_IEP0	0B12 E000h
PRU_ICSSG1_IEP1	0B12 F000h

Table 15-827. PRU_ICSSG0_IEP Registers

Offset	Acronym	Register Name	PRU_ICSSG0_I EP0 Physical Address	PRU_ICSSG0_I EP1 Physical Address
0h	IEP_GLOBAL_CFG_REG	Global Configuration Register	0B02 E000h	0B02 F000h
4h	IEP_GLOBAL_STATUS_REG	Status Register	0B02 E004h	0B02 F004h
8h	IEP_COMPEN_REG	Compensation Register	0B02 E008h	0B02 F008h
Ch	IEP_SLOW_COMPEN_REG	Slow Compensation Register	0B02 E00Ch	0B02 F00Ch
10h	IEP_COUNT_REG0	64-bit Count Value Low Register	0B02 E010h	0B02 F010h
14h	IEP_COUNT_REG1	64-bit Count Value High Register	0B02 E014h	0B02 F014h
18h	IEP_CAP_CFG_REG	Capture Configuration Register	0B02 E018h	0B02 F018h
1Ch	IEP_CAP_STATUS_REG	Capture Status Register	0B02 E01Ch	0B02 F01Ch
20h	IEP_CAPR0_REG0	Capture Rise 0 Low Register	0B02 E020h	0B02 F020h
24h	IEP_CAPR0_REG1	Capture Rise 0 High Register	0B02 E024h	0B02 F024h
28h	IEP_CAPR1_REG0	Capture Rise 1 Low Register	0B02 E028h	0B02 F028h
2Ch	IEP_CAPR1_REG1	Capture Rise 1 High Register	0B02 E02Ch	0B02 F02Ch
30h	IEP_CAPR2_REG0	Capture Rise 2 Low Register	0B02 E030h	0B02 F030h
34h	IEP_CAPR2_REG1	Capture Rise 2 High Register	0B02 E034h	0B02 F034h
38h	IEP_CAPR3_REG0	Capture Rise 3 Low Register	0B02 E038h	0B02 F038h
3Ch	IEP_CAPR3_REG1	Capture Rise 3 High Register	0B02 E03Ch	0B02 F03Ch
40h	IEP_CAPR4_REG0	Capture Rise 4 Low Register	0B02 E040h	0B02 F040h
44h	IEP_CAPR4_REG1	Capture Rise 4 High Register	0B02 E044h	0B02 F044h
48h	IEP_CAPR5_REG0	Capture Rise 5 Low Register	0B02 E048h	0B02 F048h
4Ch	IEP_CAPR5_REG1	Capture Rise 5 High Register	0B02 E04Ch	0B02 F04Ch
50h	IEP_CAPR6_REG0	Capture Rise 6 Low Register	0B02 E050h	0B02 F050h
54h	IEP_CAPR6_REG1	Capture Rise 6 High Register	0B02 E054h	0B02 F054h
58h	IEP_CAPF6_REG0	Capture Fall 6 Low Register	0B02 E058h	0B02 F058h
5Ch	IEP_CAPF6_REG1	Capture Fall 6 High Register	0B02 E05Ch	0B02 F05Ch
60h	IEP_CAPR7_REG0	Capture Rise 7 Low Register	0B02 E060h	0B02 F060h
64h	IEP_CAPR7_REG1	Capture Rise 7 High Register	0B02 E064h	0B02 F064h
68h	IEP_CAPF7_REG0	Capture Fall 7 Low Register	0B02 E068h	0B02 F068h
6Ch	IEP_CAPF7_REG1	Capture Fall 7 High Register	0B02 E06Ch	0B02 F06Ch
70h	IEP_CMP_CFG_REG	Compare Configuration Register	0B02 E070h	0B02 F070h
74h	IEP_CMP_STATUS_REG	Compare Status Register	0B02 E074h	0B02 F074h
78h	IEP_CMP0_REG0	Compare 0 Low Register	0B02 E078h	0B02 F078h
7Ch	IEP_CMP0_REG1	Compare 0 High Register	0B02 E07Ch	0B02 F07Ch
80h	IEP_CMP1_REG0	Compare 1 Low Register	0B02 E080h	0B02 F080h
84h	IEP_CMP1_REG1	Compare 1 High Register	0B02 E084h	0B02 F084h

Table 15-827. PRU_ICSSG0_I EP Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG0_I EP0 Physical Address	PRU_ICSSG0_I EP1 Physical Address
88h	IEP_CMP2_REG0	Compare 2 Low Register	0B02 E088h	0B02 F088h
8Ch	IEP_CMP2_REG1	Compare 2 High Register	0B02 E08Ch	0B02 F08Ch
90h	IEP_CMP3_REG0	Compare 3 Low Register	0B02 E090h	0B02 F090h
94h	IEP_CMP3_REG1	Compare 3 High Register	0B02 E094h	0B02 F094h
98h	IEP_CMP4_REG0	Compare 4 Low Register	0B02 E098h	0B02 F098h
9Ch	IEP_CMP4_REG1	Compare 4 High Register	0B02 E09Ch	0B02 F09Ch
A0h	IEP_CMP5_REG0	Compare 5 Low Register	0B02 E0A0h	0B02 F0A0h
A4h	IEP_CMP5_REG1	Compare 5 High Register	0B02 E0A4h	0B02 F0A4h
A8h	IEP_CMP6_REG0	Compare 6 Low Register	0B02 E0A8h	0B02 F0A8h
ACh	IEP_CMP6_REG1	Compare 6 High Register	0B02 E0ACh	0B02 F0ACh
B0h	IEP_CMP7_REG0	Compare 7 Low Register	0B02 E0B0h	0B02 F0B0h
B4h	IEP_CMP7_REG1	Compare 7 High Register	0B02 E0B4h	0B02 F0B4h
B8h	IEP_RXIPG0_REG	Status for the RX port which is attached to PRU0 Register	0B02 E0B8h	0B02 F0B8h
BCh	IEP_RXIPG1_REG	Status for the RX port which is attached to PRU1 Register	0B02 E0BCh	0B02 F0BCh
C0h	IEP_CMP8_REG0	Compare 8 Low Register	0B02 E0C0h	0B02 F0C0h
C4h	IEP_CMP8_REG1	Compare 8 High Register	0B02 E0C4h	0B02 F0C4h
C8h	IEP_CMP9_REG0	Compare 9 Low Register	0B02 E0C8h	0B02 F0C8h
CCh	IEP_CMP9_REG1	Compare 9 High Register	0B02 E0CCh	0B02 F0CCh
D0h	IEP_CMP10_REG0	Compare 10 Low Register	0B02 E0D0h	0B02 F0D0h
D4h	IEP_CMP10_REG1	Compare 10 High Register	0B02 E0D4h	0B02 F0D4h
D8h	IEP_CMP11_REG0	Compare 11 Low Register	0B02 E0D8h	0B02 F0D8h
DCh	IEP_CMP11_REG1	Compare 11 High Register	0B02 E0DCh	0B02 F0DCh
E0h	IEP_CMP12_REG0	Compare 12 Low Register	0B02 E0E0h	0B02 F0E0h
E4h	IEP_CMP12_REG1	Compare 12 High Register	0B02 E0E4h	0B02 F0E4h
E8h	IEP_CMP13_REG0	Compare 13 Low Register	0B02 E0E8h	0B02 F0E8h
ECh	IEP_CMP13_REG1	Compare 13 High Register	0B02 E0ECh	0B02 F0ECh
F0h	IEP_CMP14_REG0	Compare 14 Low Register	0B02 E0F0h	0B02 F0F0h
F4h	IEP_CMP14_REG1	Compare 14 High Register	0B02 E0F4h	0B02 F0F4h
F8h	IEP_CMP15_REG0	Compare 15 Low Register	0B02 E0F8h	0B02 F0F8h
FCh	IEP_CMP15_REG1	Compare 15 High Register	0B02 E0FCh	0B02 F0FCh
100h	IEP_COUNT_RESET_VAL_REG0	Reset value of the Controller Counter (lower 32-bits) Register	0B02 E100h	0B02 F100h
104h	IEP_COUNT_RESET_VAL_REG1	Reset value of the Controller Counter (upper 32-bits) Register	0B02 E104h	0B02 F104h
108h	IEP_PWM_REG	PWM Sync Out Register	0B02 E108h	0B02 F108h
10Ch	IEP_CAPR0_BI_REG0	Capture Big Endian Rise00 Register	0B02 E10Ch	0B02 F10Ch
110h	IEP_CAPR0_BI_REG1	Capture Big Endian Rise10 Register	0B02 E110h	0B02 F110h
114h	IEP_CAPR1_BI_REG0	Capture Big Endian Rise01 Register	0B02 E114h	0B02 F114h
118h	IEP_CAPR1_BI_REG1	Capture Big Endian Rise11 Register	0B02 E118h	0B02 F118h
11Ch	IEP_CAPR2_BI_REG0	Capture Big Endian Rise02 Register	0B02 E11Ch	0B02 F11Ch
120h	IEP_CAPR2_BI_REG1	Capture Big Endian Rise12 Register	0B02 E120h	0B02 F120h
124h	IEP_CAPR3_BI_REG0	Capture Big Endian Rise03 Register	0B02 E124h	0B02 F124h
128h	IEP_CAPR3_BI_REG1	Capture Big Endian Rise13 Register	0B02 E128h	0B02 F128h
12Ch	IEP_CAPR4_BI_REG0	Capture Big Endian Rise04 Register	0B02 E12Ch	0B02 F12Ch
130h	IEP_CAPR4_BI_REG1	Capture Big Endian Rise14 Register	0B02 E130h	0B02 F130h

Table 15-827. PRU_ICSSG0_I EP Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG0_I EP0 Physical Address	PRU_ICSSG0_I EP1 Physical Address
134h	IEP_CAPR5_BI_REG0	Capture Big Endian Rise05 Register	0B02 E134h	0B02 F134h
138h	IEP_CAPR5_BI_REG1	Capture Big Endian Rise15 Register	0B02 E138h	0B02 F138h
13Ch	IEP_CAPR6_BI_REG0	Capture Big Endian Rise06 Register	0B02 E13Ch	0B02 F13Ch
140h	IEP_CAPR6_BI_REG1	Capture Big Endian Rise16 Register	0B02 E140h	0B02 F140h
144h	IEP_CAPF6_BI_REG0	Capture Big Endian Fall06 Register	0B02 E144h	0B02 F144h
148h	IEP_CAPF6_BI_REG1	Capture Big Endian Fall16 Register	0B02 E148h	0B02 F148h
14Ch	IEP_CAPR7_BI_REG0	Capture Big Endian Rise07 Register	0B02 E14Ch	0B02 F14Ch
150h	IEP_CAPR7_BI_REG1	Capture Big Endian Rise17 Register	0B02 E150h	0B02 F150h
154h	IEP_CAPF7_BI_REG0	Capture Big Endian Fall07 Register	0B02 E154h	0B02 F154h
158h	IEP_CAPF7_BI_REG1	Capture Big Endian Fall17 Register	0B02 E158h	0B02 F158h
180h	IEP_SYNC_CTRL_REG	Sync Generation Control Register	0B02 E180h	0B02 F180h
184h	IEP_SYNC_FIRST_STAT_REG	Sync Generation First Event Status Register	0B02 E184h	0B02 F184h
188h	IEP_SYNC0_STAT_REG	Sync 0 Status Register	0B02 E188h	0B02 F188h
18Ch	IEP_SYNC1_STAT_REG	Sync 1 Status Register	0B02 E18Ch	0B02 F18Ch
190h	IEP_SYNC_PWIDTH_REG	Sync Pulse Width Configure Register	0B02 E190h	0B02 F190h
194h	IEP_SYNC0_PERIOD_REG	Sync 0 Period Configure Register	0B02 E194h	0B02 F194h
198h	IEP_SYNC1_DELAY_REG	Sync 1 Delay Register	0B02 E198h	0B02 F198h
19Ch	IEP_SYNC_START_REG	Sync Start Configure Register	0B02 E19Ch	0B02 F19Ch
200h	IEP_WD_PREDIV_REG	Watchdog Pre-Divider Register	0B02 E200h	0B02 F200h
204h	IEP_PDI_WD_TIM_REG	PDI Watchdog Timer Configure Register	0B02 E204h	0B02 F204h
208h	IEP_PD_WD_TIM_REG	PD Watchdog Timer Configure Register	0B02 E208h	0B02 F208h
20Ch	IEP_WD_STATUS_REG	Watchdog Status Register	0B02 E20Ch	0B02 F20Ch
210h	IEP_WD_EXP_CNT_REG	Watchdog Timer Expiration Counter Register	0B02 E210h	0B02 F210h
214h	IEP_WD_CTRL_REG	Watchdog Control Register	0B02 E214h	0B02 F214h
300h	IEP_DIGIO_CTRL_REG	DIGIO Control Register	0B02 E300h	0B02 F300h
304h	IEP_DIGIO_STATUS_REG	DIGIO Status Register	0B02 E304h	0B02 F304h
308h	IEP_DIGIO_DATA_IN_REG	DIGIO Data Input Register	0B02 E308h	0B02 F308h
30Ch	IEP_DIGIO_DATA_IN_RAW_REG	DIGIO Data Input Direct Sample Register	0B02 E30Ch	0B02 F30Ch
310h	IEP_DIGIO_DATA_OUT_REG	DIGIO Data Output Register	0B02 E310h	0B02 F310h
314h	IEP_DIGIO_DATA_OUT_EN_REG	DIGIO Data Input which controls tri-state of pr<k>_edio_data_out_en[3:0] Register	0B02 E314h	0B02 F314h
318h	IEP_DIGIO_EXP_REG	DIGIO, Defines which RX_EOF is used Register	0B02 E318h	0B02 F318h

Table 15-828. PRU_ICSSG1_I EP Registers

Offset	Acronym	Register Name	PRU_ICSSG1_I EP0 Physical Address	PRU_ICSSG1_I EP1 Physical Address
0h	IEP_GLOBAL_CFG_REG	Global Configuration Register	0B12 E000h	0B12 F000h
4h	IEP_GLOBAL_STATUS_REG	Status Register	0B12 E004h	0B12 F004h
8h	IEP_COMPEN_REG	Compensation Register	0B12 E008h	0B12 F008h
Ch	IEP_SLOW_COMPEN_REG	Slow Compensation Register	0B12 E00Ch	0B12 F00Ch
10h	IEP_COUNT_REG0	64-bit Count Value Low Register	0B12 E010h	0B12 F010h
14h	IEP_COUNT_REG1	64-bit Count Value High Register	0B12 E014h	0B12 F014h
18h	IEP_CAP_CFG_REG	Capture Configuration Register	0B12 E018h	0B12 F018h
1Ch	IEP_CAP_STATUS_REG	Capture Status Register	0B12 E01Ch	0B12 F01Ch

Table 15-828. PRU_ICSSG1_IEP Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG1_IEP0 Physical Address	PRU_ICSSG1_IEP1 Physical Address
20h	IEP_CAPR0_REG0	Capture Rise 0 Low Register	0B12 E020h	0B12 F020h
24h	IEP_CAPR0_REG1	Capture Rise 0 High Register	0B12 E024h	0B12 F024h
28h	IEP_CAPR1_REG0	Capture Rise 1 Low Register	0B12 E028h	0B12 F028h
2Ch	IEP_CAPR1_REG1	Capture Rise 1 High Register	0B12 E02Ch	0B12 F02Ch
30h	IEP_CAPR2_REG0	Capture Rise 2 Low Register	0B12 E030h	0B12 F030h
34h	IEP_CAPR2_REG1	Capture Rise 2 High Register	0B12 E034h	0B12 F034h
38h	IEP_CAPR3_REG0	Capture Rise 3 Low Register	0B12 E038h	0B12 F038h
3Ch	IEP_CAPR3_REG1	Capture Rise 3 High Register	0B12 E03Ch	0B12 F03Ch
40h	IEP_CAPR4_REG0	Capture Rise 4 Low Register	0B12 E040h	0B12 F040h
44h	IEP_CAPR4_REG1	Capture Rise 4 High Register	0B12 E044h	0B12 F044h
48h	IEP_CAPR5_REG0	Capture Rise 5 Low Register	0B12 E048h	0B12 F048h
4Ch	IEP_CAPR5_REG1	Capture Rise 5 High Register	0B12 E04Ch	0B12 F04Ch
50h	IEP_CAPR6_REG0	Capture Rise 6 Low Register	0B12 E050h	0B12 F050h
54h	IEP_CAPR6_REG1	Capture Rise 6 High Register	0B12 E054h	0B12 F054h
58h	IEP_CAPF6_REG0	Capture Fall 6 Low Register	0B12 E058h	0B12 F058h
5Ch	IEP_CAPF6_REG1	Capture Fall 6 High Register	0B12 E05Ch	0B12 F05Ch
60h	IEP_CAPR7_REG0	Capture Rise 7 Low Register	0B12 E060h	0B12 F060h
64h	IEP_CAPR7_REG1	Capture Rise 7 High Register	0B12 E064h	0B12 F064h
68h	IEP_CAPF7_REG0	Capture Fall 7 Low Register	0B12 E068h	0B12 F068h
6Ch	IEP_CAPF7_REG1	Capture Fall 7 High Register	0B12 E06Ch	0B12 F06Ch
70h	IEP_CMP_CFG_REG	Compare Configuration Register	0B12 E070h	0B12 F070h
74h	IEP_CMP_STATUS_REG	Compare Status Register	0B12 E074h	0B12 F074h
78h	IEP_CMP0_REG0	Compare 0 Low Register	0B12 E078h	0B12 F078h
7Ch	IEP_CMP0_REG1	Compare 0 High Register	0B12 E07Ch	0B12 F07Ch
80h	IEP_CMP1_REG0	Compare 1 Low Register	0B12 E080h	0B12 F080h
84h	IEP_CMP1_REG1	Compare 1 High Register	0B12 E084h	0B12 F084h
88h	IEP_CMP2_REG0	Compare 2 Low Register	0B12 E088h	0B12 F088h
8Ch	IEP_CMP2_REG1	Compare 2 High Register	0B12 E08Ch	0B12 F08Ch
90h	IEP_CMP3_REG0	Compare 3 Low Register	0B12 E090h	0B12 F090h
94h	IEP_CMP3_REG1	Compare 3 High Register	0B12 E094h	0B12 F094h
98h	IEP_CMP4_REG0	Compare 4 Low Register	0B12 E098h	0B12 F098h
9Ch	IEP_CMP4_REG1	Compare 4 High Register	0B12 E09Ch	0B12 F09Ch
A0h	IEP_CMP5_REG0	Compare 5 Low Register	0B12 E0A0h	0B12 F0A0h
A4h	IEP_CMP5_REG1	Compare 5 High Register	0B12 E0A4h	0B12 F0A4h
A8h	IEP_CMP6_REG0	Compare 6 Low Register	0B12 E0A8h	0B12 F0A8h
ACh	IEP_CMP6_REG1	Compare 6 High Register	0B12 E0ACh	0B12 F0ACh
B0h	IEP_CMP7_REG0	Compare 7 Low Register	0B12 E0B0h	0B12 F0B0h
B4h	IEP_CMP7_REG1	Compare 7 High Register	0B12 E0B4h	0B12 F0B4h
B8h	IEP_RXIPG0_REG	Status for the RX port which is attached to PRU0 Register	0B12 E0B8h	0B12 F0B8h
BCh	IEP_RXIPG1_REG	Status for the RX port which is attached to PRU1 Register	0B12 E0BCh	0B12 F0BCh
C0h	IEP_CMP8_REG0	Compare 8 Low Register	0B12 E0C0h	0B12 F0C0h
C4h	IEP_CMP8_REG1	Compare 8 High Register	0B12 E0C4h	0B12 F0C4h
C8h	IEP_CMP9_REG0	Compare 9 Low Register	0B12 E0C8h	0B12 F0C8h

Table 15-828. PRU_ICSSG1_IEP Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG1_IEP0 Physical Address	PRU_ICSSG1_IEP1 Physical Address
CCh	IEP_CMP9_REG1	Compare 9 High Register	0B12 E0CCh	0B12 F0CCh
D0h	IEP_CMP10_REG0	Compare 10 Low Register	0B12 E0D0h	0B12 F0D0h
D4h	IEP_CMP10_REG1	Compare 10 High Register	0B12 E0D4h	0B12 F0D4h
D8h	IEP_CMP11_REG0	Compare 11 Low Register	0B12 E0D8h	0B12 F0D8h
DCh	IEP_CMP11_REG1	Compare 11 High Register	0B12 E0DCh	0B12 F0DCh
E0h	IEP_CMP12_REG0	Compare 12 Low Register	0B12 E0E0h	0B12 F0E0h
E4h	IEP_CMP12_REG1	Compare 12 High Register	0B12 E0E4h	0B12 F0E4h
E8h	IEP_CMP13_REG0	Compare 13 Low Register	0B12 E0E8h	0B12 F0E8h
ECh	IEP_CMP13_REG1	Compare 13 High Register	0B12 E0ECh	0B12 F0ECh
F0h	IEP_CMP14_REG0	Compare 14 Low Register	0B12 E0F0h	0B12 F0F0h
F4h	IEP_CMP14_REG1	Compare 14 High Register	0B12 E0F4h	0B12 F0F4h
F8h	IEP_CMP15_REG0	Compare 15 Low Register	0B12 E0F8h	0B12 F0F8h
FCh	IEP_CMP15_REG1	Compare 15 High Register	0B12 E0FCh	0B12 F0FCh
100h	IEP_COUNT_RESET_VAL_REG0	Reset value of the Controller Counter (lower 32-bits) Register	0B12 E100h	0B12 F100h
104h	IEP_COUNT_RESET_VAL_REG1	Reset value of the Controller Counter (upper 32-bits) Register	0B12 E104h	0B12 F104h
108h	IEP_PWM_REG	PWM Sync Out Register	0B12 E108h	0B12 F108h
10Ch	IEP_CAPR0_BI_REG0	Capture Big Endian Rise00 Register	0B12 E10Ch	0B12 F10Ch
110h	IEP_CAPR0_BI_REG1	Capture Big Endian Rise10 Register	0B12 E110h	0B12 F110h
114h	IEP_CAPR1_BI_REG0	Capture Big Endian Rise01 Register	0B12 E114h	0B12 F114h
118h	IEP_CAPR1_BI_REG1	Capture Big Endian Rise11 Register	0B12 E118h	0B12 F118h
11Ch	IEP_CAPR2_BI_REG0	Capture Big Endian Rise02 Register	0B12 E11Ch	0B12 F11Ch
120h	IEP_CAPR2_BI_REG1	Capture Big Endian Rise12 Register	0B12 E120h	0B12 F120h
124h	IEP_CAPR3_BI_REG0	Capture Big Endian Rise03 Register	0B12 E124h	0B12 F124h
128h	IEP_CAPR3_BI_REG1	Capture Big Endian Rise13 Register	0B12 E128h	0B12 F128h
12Ch	IEP_CAPR4_BI_REG0	Capture Big Endian Rise04 Register	0B12 E12Ch	0B12 F12Ch
130h	IEP_CAPR4_BI_REG1	Capture Big Endian Rise14 Register	0B12 E130h	0B12 F130h
134h	IEP_CAPR5_BI_REG0	Capture Big Endian Rise05 Register	0B12 E134h	0B12 F134h
138h	IEP_CAPR5_BI_REG1	Capture Big Endian Rise15 Register	0B12 E138h	0B12 F138h
13Ch	IEP_CAPR6_BI_REG0	Capture Big Endian Rise06 Register	0B12 E13Ch	0B12 F13Ch
140h	IEP_CAPR6_BI_REG1	Capture Big Endian Rise16 Register	0B12 E140h	0B12 F140h
144h	IEP_CAPF6_BI_REG0	Capture Big Endian Fall06 Register	0B12 E144h	0B12 F144h
148h	IEP_CAPF6_BI_REG1	Capture Big Endian Fall16 Register	0B12 E148h	0B12 F148h
14Ch	IEP_CAPR7_BI_REG0	Capture Big Endian Rise07 Register	0B12 E14Ch	0B12 F14Ch
150h	IEP_CAPR7_BI_REG1	Capture Big Endian Rise17 Register	0B12 E150h	0B12 F150h
154h	IEP_CAPF7_BI_REG0	Capture Big Endian Fall07 Register	0B12 E154h	0B12 F154h
158h	IEP_CAPF7_BI_REG1	Capture Big Endian Fall17 Register	0B12 E158h	0B12 F158h
180h	IEP_SYNC_CTRL_REG	Sync Generation Control Register	0B12 E180h	0B12 F180h
184h	IEP_SYNC_FIRST_STAT_REG	Sync Generation First Event Status Register	0B12 E184h	0B12 F184h
188h	IEP_SYNC0_STAT_REG	Sync 0 Status Register	0B12 E188h	0B12 F188h
18Ch	IEP_SYNC1_STAT_REG	Sync 1 Status Register	0B12 E18Ch	0B12 F18Ch
190h	IEP_SYNC_PWIDTH_REG	Sync Pulse Width Configure Register	0B12 E190h	0B12 F190h
194h	IEP_SYNC0_PERIOD_REG	Sync 0 Period Configure Register	0B12 E194h	0B12 F194h
198h	IEP_SYNC1_DELAY_REG	Sync 1 Delay Register	0B12 E198h	0B12 F198h

Table 15-828. PRU_ICSSG1_IEP Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG1_IEP0 Physical Address	PRU_ICSSG1_IEP1 Physical Address
19Ch	IEP_SYNC_START_REG	Sync Start Configure Register	0B12 E19Ch	0B12 F19Ch
200h	IEP_WD_PREDIV_REG	Watchdog Pre-Divider Register	0B12 E200h	0B12 F200h
204h	IEP_PDI_WD_TIM_REG	PDI Watchdog Timer Configure Register	0B12 E204h	0B12 F204h
208h	IEP_PD_WD_TIM_REG	PD Watchdog Timer Configure Register	0B12 E208h	0B12 F208h
20Ch	IEP_WD_STATUS_REG	Watchdog Status Register	0B12 E20Ch	0B12 F20Ch
210h	IEP_WD_EXP_CNT_REG	Watchdog Timer Expiration Counter Register	0B12 E210h	0B12 F210h
214h	IEP_WD_CTRL_REG	Watchdog Control Register	0B12 E214h	0B12 F214h
300h	IEP_DIGIO_CTRL_REG	DIGIO Control Register	0B12 E300h	0B12 F300h
304h	IEP_DIGIO_STATUS_REG	DIGIO Status Register	0B12 E304h	0B12 F304h
308h	IEP_DIGIO_DATA_IN_REG	DIGIO Data Input Register	0B12 E308h	0B12 F308h
30Ch	IEP_DIGIO_DATA_IN_RAW_REG	DIGIO Data Input Direct Sample Register	0B12 E30Ch	0B12 F30Ch
310h	IEP_DIGIO_DATA_OUT_REG	DIGIO Data Output Register	0B12 E310h	0B12 F310h
314h	IEP_DIGIO_DATA_OUT_EN_REG	DIGIO Data Input which controls tri-state of pr<k>_edio_data_out_en[3:0] Register	0B12 E314h	0B12 F314h
318h	IEP_DIGIO_EXP_REG	DIGIO, Defines which RX_EOF is used Register	0B12 E318h	0B12 F318h

15.9.1 IEP_GLOBAL_CFG_REG Register (Offset = 0h) [reset = X]

IEP_GLOBAL_CFG_REG is shown in [Figure 15-271](#) and described in [Table 15-830](#).

Return to [Summary Table](#).

Global Configuration Register.

Table 15-829. IEP_GLOBAL_CFG_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E000h
PRU_ICSSG0_IEP1	0B02 F000h
PRU_ICSSG1_IEP0	0B12 E000h
PRU_ICSSG1_IEP1	0B12 F000h

Figure 15-271. IEP_GLOBAL_CFG_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				CMP_INC			
R/W-X				R/W-5h			
15	14	13	12	11	10	9	8
CMP_INC							
R/W-5h							
7	6	5	4	3	2	1	0
DEFAULT_INC				RESERVED			CNT_ENABLE
R/W-5h				R/W-X			R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-830. IEP_GLOBAL_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-8	CMP_INC	R/W	5h	Defines the increment value when compensation is active
7-4	DEFAULT_INC	R/W	5h	Defines the default increment value
3-1	RESERVED	R/W	X	
0	CNT_ENABLE	R/W	0h	Counter enable. 0h = Disables the counter. The counter maintains the current count. 1h = Enables the counter.

Table 15-831. Register Call Summary for IEP_GLOBAL_CFG_REG

PRU_IEP_IEP Registers
IEP_GLOBAL_CFG_REG Register (Offset = 0h) [reset = X]: [0]
PRU_ICSSG IEP
PRU_ICSSG IEP Timer Basic Programming Sequence: [0] [1] [2] 32-Bit Shadow Mode: [0] [1]

15.9.2 IEP_GLOBAL_STATUS_REG Register (Offset = 4h) [reset = X]

IEP_GLOBAL_STATUS_REG is shown in Figure 15-272 and described in Table 15-833.

Return to [Summary Table](#).

Status Register.

Table 15-832. IEP_GLOBAL_STATUS_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E004h
PRU_ICSSG0_IEP1	0B02 F004h
PRU_ICSSG1_IEP0	0B12 E004h
PRU_ICSSG1_IEP1	0B12 F004h

Figure 15-272. IEP_GLOBAL_STATUS_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							CNT_OVF
R/W-X							R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 15-833. IEP_GLOBAL_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	CNT_OVF	R/W1C	0h	Counter overflow status. 0h = No overflow 1h = Overflow occurred

Table 15-834. Register Call Summary for IEP_GLOBAL_STATUS_REG

PRU_IEP_IEP Registers
IEP_GLOBAL_STATUS_REG Register (Offset = 4h) [reset = X]: [0]
PRU_ICSSG IEP
PRU_ICSSG IEP Timer Basic Programming Sequence: [0] [1]

15.9.3 IEP_COMPEN_REG Register (Offset = 8h) [reset = X]

IEP_COMPEN_REG is shown in [Figure 15-273](#) and described in [Table 15-836](#).

Return to [Summary Table](#).

Compensation Register.

Table 15-835. IEP_COMPEN_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E008h
PRU_ICSSG0_IEP1	0B02 F008h
PRU_ICSSG1_IEP0	0B12 E008h
PRU_ICSSG1_IEP1	0B12 F008h

Figure 15-273. IEP_COMPEN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									COMPEN_CNT																						
R/W-X									R/W-0h																						

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-836. IEP_COMPEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22-0	COMPEN_CNT	R/W	0h	0h = Compensation is disabled counter inc by default_inc <value> compensation is enabled until compen_cnt decrements to 0 rd see the current compen_cnt decremented on every iep_clk when the value in [22-0]COMPEN_CNT is not equal to 0h, then count increments by cmp_inc. Note: that slow_compen_cnt must be set to zero if compen_cnt is not zero.

Table 15-837. Register Call Summary for IEP_COMPEN_REG

PRU_IEP_IEP Registers
IEP_COMPEN_REG Register (Offset = 8h) [reset = X]: [0]
PRU_ICSSG IEP
PRU_ICSSG IEP Timer Basic Programming Sequence: [0]

15.9.4 IEP_SLOW_COMPEN_REG Register (Offset = Ch) [reset = 0h]

IEP_SLOW_COMPEN_REG is shown in [Figure 15-274](#) and described in [Table 15-839](#).

Return to [Summary Table](#).

Slow Compensation Register.

Table 15-838. IEP_SLOW_COMPEN_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E00Ch
PRU_ICSSG0_IEP1	0B02 F00Ch
PRU_ICSSG1_IEP0	0B12 E00Ch
PRU_ICSSG1_IEP1	0B12 F00Ch

Figure 15-274. IEP_SLOW_COMPEN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLOW_COMPEN_CNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-839. IEP_SLOW_COMPEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SLOW_COMPEN_CNT	R/W	0h	Slow compensation counter. Write 0h = Slow compensation is disabled and counter will increment by DEFAULT_INC. Write Nh = Compensation is enabled for 1 count for every SLOW_COMPEN_CNT cycle, this is free running and continuous until software clears the MMR. For example, SLOW_COMPEN_CNT = 16, every 16 clock cycles the compensation value is used for 1 count. Note: COMPEN_CNT MUST be set to zero IF SLOW_COMPEN_CNT is not zero. Software can read the number of cycles left until the compensation event. For example, software writes SLOW_COMPEN_CNT = 100h and reads SLOW_COMPEN_CNT = 7h = This means in 6 more IEP_CLK cycles before the counter reaches 1h for the compensation event. If software writes SLOW_COMPEN_CNT = 8000h before compensation event, then the counter will reset to 8000h.

Table 15-840. Register Call Summary for IEP_SLOW_COMPEN_REG

PRU_IEP_IEP Registers

- [IEP_SLOW_COMPEN_REG Register \(Offset = Ch\) \[reset = 0h\]: \[0\]](#)

15.9.5 IEP_COUNT_REG0 Register (Offset = 10h) [reset = 0h]

IEP_COUNT_REG0 is shown in [Figure 15-275](#) and described in [Table 15-842](#).

Return to [Summary Table](#).

64-bit Count Value Low Register.

Table 15-841. IEP_COUNT_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E010h
PRU_ICSSG0_IEP1	0B02 F010h
PRU_ICSSG1_IEP0	0B12 E010h
PRU_ICSSG1_IEP1	0B12 F010h

Figure 15-275. IEP_COUNT_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT_LO																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-842. IEP_COUNT_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT_LO	R/W	0h	When Shadow Mode is disabled, this is the 64-bit count value (lower 32-bits). The count is incremented (DEFAULT_INC or CMP_INC) on every positive edge of ICSSGn_IEP_CLK (200MHz) or ICSSGn_ICLK. In 64-bit mode, reading this value locks the IEP_COUNT_REG1 [31-0] COUNT_HI value. When Shadow Mode is enabled, the counter will be in 32-bit mode.

Table 15-843. Register Call Summary for IEP_COUNT_REG0

PRU_IEP_IEP Registers
IEP_COUNT_REG0 Register (Offset = 10h) [reset = 0h]: [0] IEP_COUNT_REG1 Register (Offset = 14h) [reset = 0h]: [0]
PRU_ICSSG IEP
PRU_ICSSG IEP Timer Basic Programming Sequence: [0]

15.9.6 IEP_COUNT_REG1 Register (Offset = 14h) [reset = 0h]

IEP_COUNT_REG1 is shown in [Figure 15-276](#) and described in [Table 15-845](#).

Return to [Summary Table](#).

64-bit Count Value High Register.

Table 15-844. IEP_COUNT_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E014h
PRU_ICSSG0_IEP1	0B02 F014h
PRU_ICSSG1_IEP0	0B12 E014h
PRU_ICSSG1_IEP1	0B12 F014h

Figure 15-276. IEP_COUNT_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT_HI																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-845. IEP_COUNT_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT_HI	R/W	0h	When Shadow Mode is disabled: The controller upper 32-bits of the 64-bit count value. The count is incremented (DEFAULT_INC or CMP_INC) on every positive edge of ICSSGn_IEP_CLK (200MHz) or ICSSGn_ICLK. This value only updates when software reads IEP_COUNT_REG0[31-0] COUNT_LO. When Shadow Mode is enabled: This counts the counter reset events caused by CMP0. But, limited to 24-bit counter, so software must clear before this threshold is met.

Table 15-846. Register Call Summary for IEP_COUNT_REG1

PRU_IEP_IEP Registers IEP_COUNT_REG0 Register (Offset = 10h) [reset = 0h]: [0] IEP_COUNT_REG1 Register (Offset = 14h) [reset = 0h]: [0]
PRU_ICSSG IEP PRU_ICSSG IEP Timer Basic Programming Sequence: [0]

15.9.7 IEP_CAP_CFG_REG Register (Offset = 18h) [reset = X]

IEP_CAP_CFG_REG is shown in [Figure 15-277](#) and described in [Table 15-848](#).

Return to [Summary Table](#).

Capture Configuration Register.

Table 15-847. IEP_CAP_CFG_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E018h
PRU_ICSSG0_IEP1	0B02 F018h
PRU_ICSSG1_IEP0	0B12 E018h
PRU_ICSSG1_IEP1	0B12 F018h

Figure 15-277. IEP_CAP_CFG_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								EXT_CAP_EN				CAP_ASYNC_EN			
R/W-X								R/W-0h				R/W-7Fh			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAP_ASYNC_EN								CAP_EN							
R/W-7Fh								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-848. IEP_CAP_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-18	EXT_CAP_EN	R/W	0h	
17-10	CAP_ASYNC_EN	R/W	7Fh	Synchronization of the capture inputs to the ICSS_IEP_CLK/ ICSS_VCLK_CLK enable. Note if input capture signal is asynchronous to ICSS_IEP_CLK, enabling synchronization will cause the capture contents to be invalid. CAP_ASYNC_EN[n] maps to CAPR[n]. 0h = Disable synchronization 1h = Enable synchronization
9-0	CAP_EN	R/W	0h	

Table 15-849. Register Call Summary for IEP_CAP_CFG_REG

PRU_IEP_IEP Registers

- [IEP_CAP_CFG_REG Register \(Offset = 18h\) \[reset = X\]: \[0\]](#)

15.9.8 IEP_CAP_STATUS_REG Register (Offset = 1Ch) [reset = X]

IEP_CAP_STATUS_REG is shown in Figure 15-278 and described in Table 15-851.

Return to [Summary Table](#).

Capture Status Register.

Table 15-850. IEP_CAP_STATUS_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E01Ch
PRU_ICSSG0_IEP1	0B02 F01Ch
PRU_ICSSG1_IEP0	0B12 E01Ch
PRU_ICSSG1_IEP1	0B12 F01Ch

Figure 15-278. IEP_CAP_STATUS_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								CAP_RAW							
R-X								R-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CAP_VALID							
R-X								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 15-851. IEP_CAP_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	X	
23-16	CAP_RAW	R	0h	Raw/Current status bit for each of the capture registers, where CAP_RAW[n] maps to CAPR[n]. 0h = Current state is low. 1h = Current state is high.
15-11	RESERVED	R	X	
10-0	CAP_VALID	R	0h	A Capture Valid Status , OR tree 0h = No Hit for any cap event 1h = Hit for 1 or more cap event is pending

Table 15-852. Register Call Summary for IEP_CAP_STATUS_REG

PRU_IEP_IEP Registers

- [IEP_CAP_STATUS_REG Register \(Offset = 1Ch\) \[reset = X\]: \[0\]](#)

15.9.9 IEP_CAPR0_REG0 Register (Offset = 20h) [reset = 0h]

IEP_CAPR0_REG0 is shown in [Figure 15-279](#) and described in [Table 15-854](#).

[Return to Summary Table.](#)

Capture Rise 0 Low Register.

Table 15-853. IEP_CAPR0_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E020h
PRU_ICSSG0_IEP1	0B02 F020h
PRU_ICSSG1_IEP0	0B12 E020h
PRU_ICSSG1_IEP1	0B12 F020h

Figure 15-279. IEP_CAPR0_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR0_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-854. IEP_CAPR0_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR0_0	R	0h	Value captured for CAPR<i> (fall) event, where i = 0 to 5. Lower 32-bits.

Table 15-855. Register Call Summary for IEP_CAPR0_REG0

PRU_IEP_IEP Registers
IEP_CAPR0_REG0 Register (Offset = 20h) [reset = 0h]: [0]
PRU_ICSSG IEP
Industrial Ethernet Mapping: [0]

15.9.10 IEP_CAPR0_REG1 Register (Offset = 24h) [reset = 0h]

IEP_CAPR0_REG1 is shown in [Figure 15-280](#) and described in [Table 15-857](#).

Return to [Summary Table](#).

Capture Rise 0 High Register.

Table 15-856. IEP_CAPR0_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E024h
PRU_ICSSG0_IEP1	0B02 F024h
PRU_ICSSG1_IEP0	0B12 E024h
PRU_ICSSG1_IEP1	0B12 F024h

Figure 15-280. IEP_CAPR0_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR0_1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-857. IEP_CAPR0_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR0_1	R	0h	Value captured for CAPR<i> (rise) event, where i = 0 to 5. Upper 32-bits.

Table 15-858. Register Call Summary for IEP_CAPR0_REG1

PRU_IEP_IEP Registers
IEP_CAPR0_REG1 Register (Offset = 24h) [reset = 0h]: [0]
PRU_ICSSG IEP
Industrial Ethernet Mapping: [0]

15.9.11 IEP_CAPR1_REG0 Register (Offset = 28h) [reset = 0h]

IEP_CAPR1_REG0 is shown in [Figure 15-281](#) and described in [Table 15-860](#).

Return to [Summary Table](#).

Capture Rise 1 Low Register.

Table 15-859. IEP_CAPR1_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E028h
PRU_ICSSG0_IEP1	0B02 F028h
PRU_ICSSG1_IEP0	0B12 E028h
PRU_ICSSG1_IEP1	0B12 F028h

Figure 15-281. IEP_CAPR1_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR1_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-860. IEP_CAPR1_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR1_0	R	0h	Value captured for CAPR<i> (fall) event, where i = 0 to 5. Lower 32-bits.

Table 15-861. Register Call Summary for IEP_CAPR1_REG0

PRU_IEP_IEP Registers
IEP_CAPR1_REG0 Register (Offset = 28h) [reset = 0h]: [0]
PRU_ICSSG IEP
Industrial Ethernet Mapping: [0]

15.9.12 IEP_CAPR1_REG1 Register (Offset = 2Ch) [reset = 0h]

IEP_CAPR1_REG1 is shown in [Figure 15-282](#) and described in [Table 15-863](#).

Return to [Summary Table](#).

Capture Rise 1 High Register.

Table 15-862. IEP_CAPR1_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E02Ch
PRU_ICSSG0_IEP1	0B02 F02Ch
PRU_ICSSG1_IEP0	0B12 E02Ch
PRU_ICSSG1_IEP1	0B12 F02Ch

Figure 15-282. IEP_CAPR1_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR1_1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-863. IEP_CAPR1_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR1_1	R	0h	Value captured for CAPR<i> (rise) event, where i = 0 to 5. Upper 32-bits.

Table 15-864. Register Call Summary for IEP_CAPR1_REG1

PRU_IEP_IEP Registers
IEP_CAPR1_REG1 Register (Offset = 2Ch) [reset = 0h]: [0]
PRU_ICSSG IEP
Industrial Ethernet Mapping: [0]

15.9.13 IEP_CAPR2_REG0 Register (Offset = 30h) [reset = 0h]

IEP_CAPR2_REG0 is shown in [Figure 15-283](#) and described in [Table 15-866](#).

Return to [Summary Table](#).

Capture Rise 2 Low Register

Table 15-865. IEP_CAPR2_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E030h
PRU_ICSSG0_IEP1	0B02 F030h
PRU_ICSSG1_IEP0	0B12 E030h
PRU_ICSSG1_IEP1	0B12 F030h

Figure 15-283. IEP_CAPR2_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR2_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-866. IEP_CAPR2_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR2_0	R	0h	Value captured for CAPR<i> (fall) event, where i = 0 to 5. Lower 32-bits.

Table 15-867. Register Call Summary for IEP_CAPR2_REG0

PRU_IEP_IEP Registers
IEP_CAPR2_REG0 Register (Offset = 30h) [reset = 0h]: [0]
PRU_ICSSG IEP
Industrial Ethernet Mapping: [0]

15.9.14 IEP_CAPR2_REG1 Register (Offset = 34h) [reset = 0h]

IEP_CAPR2_REG1 is shown in [Figure 15-284](#) and described in [Table 15-869](#).

Return to [Summary Table](#).

Capture Rise 2 High Register.

Table 15-868. IEP_CAPR2_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E034h
PRU_ICSSG0_IEP1	0B02 F034h
PRU_ICSSG1_IEP0	0B12 E034h
PRU_ICSSG1_IEP1	0B12 F034h

Figure 15-284. IEP_CAPR2_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR2_1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-869. IEP_CAPR2_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR2_1	R	0h	Value captured for CAPR<i> (rise) event, where i = 0 to 5. Upper 32-bits.

Table 15-870. Register Call Summary for IEP_CAPR2_REG1

PRU_IEP_IEP Registers
IEP_CAPR2_REG1 Register (Offset = 34h) [reset = 0h]: [0]
PRU_ICSSG IEP
Industrial Ethernet Mapping: [0]

15.9.15 IEP_CAPR3_REG0 Register (Offset = 38h) [reset = 0h]

IEP_CAPR3_REG0 is shown in [Figure 15-285](#) and described in [Table 15-872](#).

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Capture Rise 3 Low Register.

Table 15-871. IEP_CAPR3_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E038h
PRU_ICSSG0_IEP1	0B02 F038h
PRU_ICSSG1_IEP0	0B12 E038h
PRU_ICSSG1_IEP1	0B12 F038h

Figure 15-285. IEP_CAPR3_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR3_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-872. IEP_CAPR3_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR3_0	R	0h	Value captured for CAPR<i> (fall) event, where i = 0 to 5. Lower 32-bits.

Table 15-873. Register Call Summary for IEP_CAPR3_REG0

PRU_IEP_IEP Registers
IEP_CAPR3_REG0 Register (Offset = 38h) [reset = 0h]: [0]
PRU_ICSSG IEP
Industrial Ethernet Mapping: [0]

15.9.16 IEP_CAPR3_REG1 Register (Offset = 3Ch) [reset = 0h]

IEP_CAPR3_REG1 is shown in Figure 15-286 and described in Table 15-875.

Return to [Summary Table](#).

Capture Rise 3 High Register.

Table 15-874. IEP_CAPR3_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E03Ch
PRU_ICSSG0_IEP1	0B02 F03Ch
PRU_ICSSG1_IEP0	0B12 E03Ch
PRU_ICSSG1_IEP1	0B12 F03Ch

Figure 15-286. IEP_CAPR3_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR3_1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-875. IEP_CAPR3_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR3_1	R	0h	Value captured for CAPR<i> (rise) event, where i = 0 to 5. Upper 32-bits.

Table 15-876. Register Call Summary for IEP_CAPR3_REG1

PRU_IEP_IEP Registers
IEP_CAPR3_REG1 Register (Offset = 3Ch) [reset = 0h]: [0]
PRU_ICSSG IEP
Industrial Ethernet Mapping: [0]

15.9.17 IEP_CAPR4_REG0 Register (Offset = 40h) [reset = 0h]

IEP_CAPR4_REG0 is shown in [Figure 15-287](#) and described in [Table 15-878](#).

Return to [Summary Table](#).

Capture Rise 4 Low Register.

Table 15-877. IEP_CAPR4_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E040h
PRU_ICSSG0_IEP1	0B02 F040h
PRU_ICSSG1_IEP0	0B12 E040h
PRU_ICSSG1_IEP1	0B12 F040h

Figure 15-287. IEP_CAPR4_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR4_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-878. IEP_CAPR4_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR4_0	R	0h	Value captured for CAPR<i> (fall) event, where i = 0 to 5. Lower 32-bits.

Table 15-879. Register Call Summary for IEP_CAPR4_REG0

PRU_IEP_IEP Registers
IEP_CAPR4_REG0 Register (Offset = 40h) [reset = 0h]: [0]
PRU_ICSSG IEP
Industrial Ethernet Mapping: [0]

15.9.18 IEP_CAPR4_REG1 Register (Offset = 44h) [reset = 0h]

IEP_CAPR4_REG1 is shown in Figure 15-288 and described in Table 15-881.

Return to [Summary Table](#).

Capture Rise 4 High Register.

Table 15-880. IEP_CAPR4_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E044h
PRU_ICSSG0_IEP1	0B02 F044h
PRU_ICSSG1_IEP0	0B12 E044h
PRU_ICSSG1_IEP1	0B12 F044h

Figure 15-288. IEP_CAPR4_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR4_1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-881. IEP_CAPR4_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR4_1	R	0h	Value captured for CAPR<i> (rise) event, where i = 0 to 5. Upper 32-bits.

Table 15-882. Register Call Summary for IEP_CAPR4_REG1

PRU_IEP_IEP Registers
IEP_CAPR4_REG1 Register (Offset = 44h) [reset = 0h]: [0]
PRU_ICSSG IEP
Industrial Ethernet Mapping: [0]

15.9.19 IEP_CAPR5_REG0 Register (Offset = 48h) [reset = 0h]

IEP_CAPR5_REG0 is shown in [Figure 15-289](#) and described in [Table 15-884](#).

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Capture Rise 5 Low Register.

Table 15-883. IEP_CAPR5_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E048h
PRU_ICSSG0_IEP1	0B02 F048h
PRU_ICSSG1_IEP0	0B12 E048h
PRU_ICSSG1_IEP1	0B12 F048h

Figure 15-289. IEP_CAPR5_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR5_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-884. IEP_CAPR5_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR5_0	R	0h	Value captured for CAPR<i> (fall) event, where i = 0 to 5. Lower 32-bits.

Table 15-885. Register Call Summary for IEP_CAPR5_REG0

PRU_IEP_IEP Registers
IEP_CAPR5_REG0 Register (Offset = 48h) [reset = 0h]: [0]
PRU_ICSSG IEP
Industrial Ethernet Mapping: [0]

15.9.20 IEP_CAPR5_REG1 Register (Offset = 4Ch) [reset = 0h]

IEP_CAPR5_REG1 is shown in Figure 15-290 and described in Table 15-887.

Return to [Summary Table](#).

Capture Rise 5 High Register.

Table 15-886. IEP_CAPR5_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E04Ch
PRU_ICSSG0_IEP1	0B02 F04Ch
PRU_ICSSG1_IEP0	0B12 E04Ch
PRU_ICSSG1_IEP1	0B12 F04Ch

Figure 15-290. IEP_CAPR5_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR5_1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-887. IEP_CAPR5_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR5_1	R	0h	Value captured for CAPR<i> (rise) event, where i = 0 to 5. Upper 32-bits.

Table 15-888. Register Call Summary for IEP_CAPR5_REG1

PRU_IEP_IEP Registers
IEP_CAPR5_REG1 Register (Offset = 4Ch) [reset = 0h]: [0]
PRU_ICSSG IEP
Industrial Ethernet Mapping: [0]

15.9.21 IEP_CAPR6_REG0 Register (Offset = 50h) [reset = 0h]

IEP_CAPR6_REG0 is shown in [Figure 15-291](#) and described in [Table 15-890](#).

Return to [Summary Table](#).

Capture Rise 6 Low Register.

Table 15-889. IEP_CAPR6_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E050h
PRU_ICSSG0_IEP1	0B02 F050h
PRU_ICSSG1_IEP0	0B12 E050h
PRU_ICSSG1_IEP1	0B12 F050h

Figure 15-291. IEP_CAPR6_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR6_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-890. IEP_CAPR6_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR6_0	R	0h	Value captured for CAPR6 event. Lower 32-bits.

Table 15-891. Register Call Summary for IEP_CAPR6_REG0

PRU_IEP_IEP Registers
IEP_CAPR6_REG0 Register (Offset = 50h) [reset = 0h]: [0]
PRU_ICSSG IEP
Industrial Ethernet Mapping: [0] PRU_ICSSG IEP Timer Features: [0]

15.9.22 IEP_CAPR6_REG1 Register (Offset = 54h) [reset = 0h]

IEP_CAPR6_REG1 is shown in [Figure 15-292](#) and described in [Table 15-893](#).

Return to [Summary Table](#).

Capture Rise 6 High Register.

Table 15-892. IEP_CAPR6_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E054h
PRU_ICSSG0_IEP1	0B02 F054h
PRU_ICSSG1_IEP0	0B12 E054h
PRU_ICSSG1_IEP1	0B12 F054h

Figure 15-292. IEP_CAPR6_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR6_1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-893. IEP_CAPR6_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR6_1	R	0h	Value captured for CAPR6 event. Upper 32-bits.

Table 15-894. Register Call Summary for IEP_CAPR6_REG1

PRU_IEP_IEP Registers
IEP_CAPR6_REG1 Register (Offset = 54h) [reset = 0h]: [0]
PRU_ICSSG IEP
Industrial Ethernet Mapping: [0] PRU_ICSSG IEP Timer Features: [0]

15.9.23 IEP_CAPF6_REG0 Register (Offset = 58h) [reset = 0h]

IEP_CAPF6_REG0 is shown in [Figure 15-293](#) and described in [Table 15-896](#).

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Capture Fall 6 Low Register.

Table 15-895. IEP_CAPF6_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E058h
PRU_ICSSG0_IEP1	0B02 F058h
PRU_ICSSG1_IEP0	0B12 E058h
PRU_ICSSG1_IEP1	0B12 F058h

Figure 15-293. IEP_CAPF6_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPF6_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-896. IEP_CAPF6_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPF6_0	R	0h	Value captured for CAPF6 (fall) event. Lower 32-bits.

Table 15-897. Register Call Summary for IEP_CAPF6_REG0

PRU_IEP_IEP Registers
IEP_CAPF6_REG0 Register (Offset = 58h) [reset = 0h]: [0]
PRU_ICSSG IEP
Industrial Ethernet Mapping: [0] PRU_ICSSG IEP Timer Features: [0]

15.9.24 IEP_CAPF6_REG1 Register (Offset = 5Ch) [reset = 0h]

IEP_CAPF6_REG1 is shown in [Figure 15-294](#) and described in [Table 15-899](#).

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Capture Fall 6 High Register.

Table 15-898. IEP_CAPF6_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E05Ch
PRU_ICSSG0_IEP1	0B02 F05Ch
PRU_ICSSG1_IEP0	0B12 E05Ch
PRU_ICSSG1_IEP1	0B12 F05Ch

Figure 15-294. IEP_CAPF6_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPF6_1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-899. IEP_CAPF6_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPF6_1	R	0h	Value captured for CAPF6 (fall) event. Lower 32-bits.

Table 15-900. Register Call Summary for IEP_CAPF6_REG1

PRU_IEP_IEP Registers
IEP_CAPF6_REG1 Register (Offset = 5Ch) [reset = 0h]: [0]
PRU_ICSSG IEP
Industrial Ethernet Mapping: [0] PRU_ICSSG IEP Timer Features: [0]

15.9.25 IEP_CAPR7_REG0 Register (Offset = 60h) [reset = 0h]

IEP_CAPR7_REG0 is shown in [Figure 15-295](#) and described in [Table 15-902](#).

Return to [Summary Table](#).

Capture Rise 7 Low Register.

Table 15-901. IEP_CAPR7_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E060h
PRU_ICSSG0_IEP1	0B02 F060h
PRU_ICSSG1_IEP0	0B12 E060h
PRU_ICSSG1_IEP1	0B12 F060h

Figure 15-295. IEP_CAPR7_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR7_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-902. IEP_CAPR7_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR7_0	R	0h	Value captured for CAPR7 (rise) event. Lower 32-bits.

Table 15-903. Register Call Summary for IEP_CAPR7_REG0

PRU_IEP_IEP Registers
IEP_CAPR7_REG0 Register (Offset = 60h) [reset = 0h]: [0]
PRU_ICSSG IEP
Industrial Ethernet Mapping: [0] PRU_ICSSG IEP Timer Features: [0]

15.9.26 IEP_CAPR7_REG1 Register (Offset = 64h) [reset = 0h]

IEP_CAPR7_REG1 is shown in [Figure 15-296](#) and described in [Table 15-905](#).

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Capture Rise 7 High Register.

Table 15-904. IEP_CAPR7_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E064h
PRU_ICSSG0_IEP1	0B02 F064h
PRU_ICSSG1_IEP0	0B12 E064h
PRU_ICSSG1_IEP1	0B12 F064h

Figure 15-296. IEP_CAPR7_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR7_1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-905. IEP_CAPR7_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR7_1	R	0h	Value captured for CAPR7 (rise) event. Upper 32-bits.

Table 15-906. Register Call Summary for IEP_CAPR7_REG1

PRU_IEP_IEP Registers
IEP_CAPR7_REG1 Register (Offset = 64h) [reset = 0h]: [0]
PRU_ICSSG IEP
Industrial Ethernet Mapping: [0] PRU_ICSSG IEP Timer Features: [0]

15.9.27 IEP_CAPF7_REG0 Register (Offset = 68h) [reset = 0h]

IEP_CAPF7_REG0 is shown in [Figure 15-297](#) and described in [Table 15-908](#).

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Capture Fall 7 Low Register.

Table 15-907. IEP_CAPF7_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E068h
PRU_ICSSG0_IEP1	0B02 F068h
PRU_ICSSG1_IEP0	0B12 E068h
PRU_ICSSG1_IEP1	0B12 F068h

Figure 15-297. IEP_CAPF7_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPF7_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-908. IEP_CAPF7_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPF7_0	R	0h	Value captured for CAPF7 (fall) event. Lower 32-bits.

Table 15-909. Register Call Summary for IEP_CAPF7_REG0

PRU_IEP_IEP Registers
IEP_CAPF7_REG0 Register (Offset = 68h) [reset = 0h]: [0]
PRU_ICSSG IEP
Industrial Ethernet Mapping: [0] PRU_ICSSG IEP Timer Features: [0]

15.9.28 IEP_CAPF7_REG1 Register (Offset = 6Ch) [reset = 0h]

IEP_CAPF7_REG1 is shown in [Figure 15-298](#) and described in [Table 15-911](#).

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Capture Fall 7 High Register.

Table 15-910. IEP_CAPF7_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E06Ch
PRU_ICSSG0_IEP1	0B02 F06Ch
PRU_ICSSG1_IEP0	0B12 E06Ch
PRU_ICSSG1_IEP1	0B12 F06Ch

Figure 15-298. IEP_CAPF7_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPF7_1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-911. IEP_CAPF7_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPF7_1	R	0h	Value captured for CAPF7 (fall) event. Upper 32-bits.

Table 15-912. Register Call Summary for IEP_CAPF7_REG1

PRU_IEP_IEP Registers
IEP_CAPF7_REG1 Register (Offset = 6Ch) [reset = 0h]: [0]
PRU_ICSSG IEP
Industrial Ethernet Mapping: [0] PRU_ICSSG IEP Timer Features: [0]

15.9.29 IEP_CMP_CFG_REG Register (Offset = 70h) [reset = X]

IEP_CMP_CFG_REG is shown in [Figure 15-299](#) and described in [Table 15-914](#).

Return to [Summary Table](#).

Compare Configuration Register.

Table 15-913. IEP_CMP_CFG_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E070h
PRU_ICSSG0_IEP1	0B02 F070h
PRU_ICSSG1_IEP0	0B12 E070h
PRU_ICSSG1_IEP1	0B12 F070h

Figure 15-299. IEP_CMP_CFG_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						SHADOW_EN	CMP_EN
R/W-X						R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
CMP_EN							
R/W-0h							
7	6	5	4	3	2	1	0
CMP_EN						CMP0_RST_CNT_EN	
R/W-0h						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-914. IEP_CMP_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17	SHADOW_EN	R/W	0h	
16-1	CMP_EN	R/W	0h	Enable bits for each of the compare registers 0h = Disables CMPj/k Event 1h = Enables CMPj/k Event CMP_EN[0] (bit 1 of register) maps to CMP0 event
0	CMP0_RST_CNT_EN	R/W	0h	Enable the reset of the counter 0h = Disable 1h = Enable the reset of the counter if a CMP0 event occurs

Table 15-915. Register Call Summary for IEP_CMP_CFG_REG

PRU_IEP_IEP Registers
IEP_CMP_CFG_REG Register (Offset = 70h) [reset = X]: [0]
PRU_ICSSG IEP
PRU_ICSSG IEP Timer Basic Programming Sequence: [0] 32-Bit Shadow Mode: [0] [1] [2] [3] [4] [5] [6] PRU_ICSSG IEP Timer Features: [0] [1]

15.9.30 IEP_CMP_STATUS_REG Register (Offset = 74h) [reset = X]

IEP_CMP_STATUS_REG is shown in [Figure 15-300](#) and described in [Table 15-917](#).

Return to [Summary Table](#).

Compare Status Register.

Table 15-916. IEP_CMP_STATUS_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E074h
PRU_ICSSG0_IEP1	0B02 F074h
PRU_ICSSG1_IEP0	0B12 E074h
PRU_ICSSG1_IEP1	0B12 F074h

Figure 15-300. IEP_CMP_STATUS_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CMP_STATUS															
R/W-X																R/W1C-0h															

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 15-917. IEP_CMP_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	CMP_STATUS	R/W1C	0h	Status bit for each of the compare registers. "Match" indicates the current counter is greater than or equal to the compare value. Note: it is the firmware's responsibility to handle the IEP overflow. 0h = No match has occurred 1h = A match occurred. The associated hardware event signal will assert and remain high until the status is cleared. Shadow Mode Disabled: Any write to a CMP register will cause the corresponding CMP_STATUS bit to get cleared Shadow Mode Enabled: Any write to the active CMP<n>_0 will cause the corresponding CMP_STATUS to get cleared. Any write to the shadow CMP<n>_1 will have no effect on pending state

Table 15-918. Register Call Summary for IEP_CMP_STATUS_REG

PRU_IEP_IEP Registers IEP_CMP_STATUS_REG Register (Offset = 74h) [reset = X]: [0]
PRU_ICSSG IEP PRU_ICSSG IEP Timer Basic Programming Sequence: [0] PRU_ICSSG IEP Timer Features: [0]

15.9.31 IEP_CMP0_REG0 Register (Offset = 78h) [reset = 0h]

IEP_CMP0_REG0 is shown in [Figure 15-301](#) and described in [Table 15-920](#).

Return to [Summary Table](#).

Compare 0 Low Register.

Table 15-919. IEP_CMP0_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E078h
PRU_ICSSG0_IEP1	0B02 F078h
PRU_ICSSG1_IEP0	0B12 E078h
PRU_ICSSG1_IEP1	0B12 F078h

Figure 15-301. IEP_CMP0_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP0_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-920. IEP_CMP0_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP0_0	R/W	0h	Compare 0 low value

Table 15-921. Register Call Summary for IEP_CMP0_REG0

PRU_IEP_IEP Registers

- [IEP_CMP0_REG0 Register \(Offset = 78h\) \[reset = 0h\]: \[0\]](#)

15.9.32 IEP_CMP0_REG1 Register (Offset = 7Ch) [reset = 0h]

IEP_CMP0_REG1 is shown in [Figure 15-302](#) and described in [Table 15-923](#).

Return to [Summary Table](#).

Compare 0 High Register.

Table 15-922. IEP_CMP0_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E07Ch
PRU_ICSSG0_IEP1	0B02 F07Ch
PRU_ICSSG1_IEP0	0B12 E07Ch
PRU_ICSSG1_IEP1	0B12 F07Ch

Figure 15-302. IEP_CMP0_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP0_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-923. IEP_CMP0_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP0_1	R/W	0h	Compare 0 high value

Table 15-924. Register Call Summary for IEP_CMP0_REG1

PRU_IEP_IEP Registers
IEP_CMP0_REG1 Register (Offset = 7Ch) [reset = 0h]: [0]
PRU_ICSSG IEP
32-Bit Shadow Mode: [0]

15.9.33 IEP_CMP1_REG0 Register (Offset = 80h) [reset = 0h]

IEP_CMP1_REG0 is shown in [Figure 15-303](#) and described in [Table 15-926](#).

Return to [Summary Table](#).

Compare 1 Low Register.

Table 15-925. IEP_CMP1_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E080h
PRU_ICSSG0_IEP1	0B02 F080h
PRU_ICSSG1_IEP0	0B12 E080h
PRU_ICSSG1_IEP1	0B12 F080h

Figure 15-303. IEP_CMP1_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP1_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-926. IEP_CMP1_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP1_0	R/W	0h	Compare 1 low value

Table 15-927. Register Call Summary for IEP_CMP1_REG0

PRU_IEP_IEP Registers
IEP_CMP1_REG0 Register (Offset = 80h) [reset = 0h]: [0]
PRU_ICSSG IEP
Industrial Ethernet Mapping: [0] PRU_ICSSG IEP Sync0/Sync1 Features: [0]

15.9.34 IEP_CMP1_REG1 Register (Offset = 84h) [reset = 0h]

IEP_CMP1_REG1 is shown in [Figure 15-304](#) and described in [Table 15-929](#).

Return to [Summary Table](#).

Compare 1 High Register.

Table 15-928. IEP_CMP1_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E084h
PRU_ICSSG0_IEP1	0B02 F084h
PRU_ICSSG1_IEP0	0B12 E084h
PRU_ICSSG1_IEP1	0B12 F084h

Figure 15-304. IEP_CMP1_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP1_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-929. IEP_CMP1_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP1_1	R/W	0h	Compare 1 high value

Table 15-930. Register Call Summary for IEP_CMP1_REG1

PRU_IEP_IEP Registers
IEP_CMP1_REG1 Register (Offset = 84h) [reset = 0h]: [0]
PRU_ICSSG IEP
Industrial Ethernet Mapping: [0] PRU_ICSSG IEP Sync0/Sync1 Features: [0]

15.9.35 IEP_CMP2_REG0 Register (Offset = 88h) [reset = 0h]

IEP_CMP2_REG0 is shown in [Figure 15-305](#) and described in [Table 15-932](#).

Return to [Summary Table](#).

Compare 2 Low Register.

Table 15-931. IEP_CMP2_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E088h
PRU_ICSSG0_IEP1	0B02 F088h
PRU_ICSSG1_IEP0	0B12 E088h
PRU_ICSSG1_IEP1	0B12 F088h

Figure 15-305. IEP_CMP2_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP2_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-932. IEP_CMP2_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP2_0	R/W	0h	Compare 2 low value

Table 15-933. Register Call Summary for IEP_CMP2_REG0

PRU_IEP_IEP Registers
IEP_CMP2_REG0 Register (Offset = 88h) [reset = 0h]: [0]
PRU_ICSSG IEP
Industrial Ethernet Mapping: [0] PRU_ICSSG IEP Sync0/Sync1 Features: [0]

15.9.36 IEP_CMP2_REG1 Register (Offset = 8Ch) [reset = 0h]

IEP_CMP2_REG1 is shown in [Figure 15-306](#) and described in [Table 15-935](#).

Return to [Summary Table](#).

Compare 2 High Register.

Table 15-934. IEP_CMP2_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E08Ch
PRU_ICSSG0_IEP1	0B02 F08Ch
PRU_ICSSG1_IEP0	0B12 E08Ch
PRU_ICSSG1_IEP1	0B12 F08Ch

Figure 15-306. IEP_CMP2_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP2_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-935. IEP_CMP2_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP2_1	R/W	0h	Compare 2 high value

Table 15-936. Register Call Summary for IEP_CMP2_REG1

PRU_IEP_IEP Registers
IEP_CMP2_REG1 Register (Offset = 8Ch) [reset = 0h]: [0]
PRU_ICSSG IEP
Industrial Ethernet Mapping: [0] PRU_ICSSG IEP Sync0/Sync1 Features: [0]

15.9.37 IEP_CMP3_REG0 Register (Offset = 90h) [reset = 0h]

IEP_CMP3_REG0 is shown in [Figure 15-307](#) and described in [Table 15-938](#).

Return to [Summary Table](#).

Compare 3 Low Register.

Table 15-937. IEP_CMP3_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E090h
PRU_ICSSG0_IEP1	0B02 F090h
PRU_ICSSG1_IEP0	0B12 E090h
PRU_ICSSG1_IEP1	0B12 F090h

Figure 15-307. IEP_CMP3_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP3_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-938. IEP_CMP3_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP3_0	R/W	0h	Compare 3 low value

Table 15-939. Register Call Summary for IEP_CMP3_REG0

PRU_IEP_IEP Registers
IEP_CMP3_REG0 Register (Offset = 90h) [reset = 0h]: [0]
PRU_ICSSG IEP
Industrial Ethernet Mapping: [0]

15.9.38 IEP_CMP3_REG1 Register (Offset = 94h) [reset = 0h]

IEP_CMP3_REG1 is shown in [Figure 15-308](#) and described in [Table 15-941](#).

Return to [Summary Table](#).

Compare 3 High Register.

Table 15-940. IEP_CMP3_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E094h
PRU_ICSSG0_IEP1	0B02 F094h
PRU_ICSSG1_IEP0	0B12 E094h
PRU_ICSSG1_IEP1	0B12 F094h

Figure 15-308. IEP_CMP3_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP3_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-941. IEP_CMP3_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP3_1	R/W	0h	Compare 3 high value

Table 15-942. Register Call Summary for IEP_CMP3_REG1

PRU_IEP_IEP Registers
IEP_CMP3_REG1 Register (Offset = 94h) [reset = 0h]: [0]
PRU_ICSSG IEP
Industrial Ethernet Mapping: [0]

15.9.39 IEP_CMP4_REG0 Register (Offset = 98h) [reset = 0h]

IEP_CMP4_REG0 is shown in [Figure 15-309](#) and described in [Table 15-944](#).

Return to [Summary Table](#).

Compare 4 Low Register.

Table 15-943. IEP_CMP4_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E098h
PRU_ICSSG0_IEP1	0B02 F098h
PRU_ICSSG1_IEP0	0B12 E098h
PRU_ICSSG1_IEP1	0B12 F098h

Figure 15-309. IEP_CMP4_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP4_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-944. IEP_CMP4_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP4_0	R/W	0h	Compare 4 low value

Table 15-945. Register Call Summary for IEP_CMP4_REG0

PRU_IEP_IEP Registers
IEP_CMP4_REG0 Register (Offset = 98h) [reset = 0h]: [0]
PRU_ICSSG IEP
Industrial Ethernet Mapping: [0]

15.9.40 IEP_CMP4_REG1 Register (Offset = 9Ch) [reset = 0h]

IEP_CMP4_REG1 is shown in [Figure 15-310](#) and described in [Table 15-947](#).

Return to [Summary Table](#).

Compare 4 High Register.

Table 15-946. IEP_CMP4_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E09Ch
PRU_ICSSG0_IEP1	0B02 F09Ch
PRU_ICSSG1_IEP0	0B12 E09Ch
PRU_ICSSG1_IEP1	0B12 F09Ch

Figure 15-310. IEP_CMP4_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP4_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-947. IEP_CMP4_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP4_1	R/W	0h	Compare 4 high value

Table 15-948. Register Call Summary for IEP_CMP4_REG1

PRU_IEP_IEP Registers
IEP_CMP4_REG1 Register (Offset = 9Ch) [reset = 0h]: [0]
PRU_ICSSG IEP
Industrial Ethernet Mapping: [0]

15.9.41 IEP_CMP5_REG0 Register (Offset = A0h) [reset = 0h]

IEP_CMP5_REG0 is shown in [Figure 15-311](#) and described in [Table 15-950](#).

Return to [Summary Table](#).

Compare 5 Low Register.

Table 15-949. IEP_CMP5_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E0A0h
PRU_ICSSG0_IEP1	0B02 F0A0h
PRU_ICSSG1_IEP0	0B12 E0A0h
PRU_ICSSG1_IEP1	0B12 F0A0h

Figure 15-311. IEP_CMP5_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP5_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-950. IEP_CMP5_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP5_0	R/W	0h	Compare 5 low value

Table 15-951. Register Call Summary for IEP_CMP5_REG0

PRU_IEP_IEP Registers

- [IEP_CMP5_REG0 Register \(Offset = A0h\) \[reset = 0h\]: \[0\]](#)

15.9.42 IEP_CMP5_REG1 Register (Offset = A4h) [reset = 0h]

IEP_CMP5_REG1 is shown in [Figure 15-312](#) and described in [Table 15-953](#).

Return to [Summary Table](#).

Compare 5 High Register.

Table 15-952. IEP_CMP5_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E0A4h
PRU_ICSSG0_IEP1	0B02 F0A4h
PRU_ICSSG1_IEP0	0B12 E0A4h
PRU_ICSSG1_IEP1	0B12 F0A4h

Figure 15-312. IEP_CMP5_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP5_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-953. IEP_CMP5_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP5_1	R/W	0h	Compare 5 high value

Table 15-954. Register Call Summary for IEP_CMP5_REG1

PRU_IEP_IEP Registers

- [IEP_CMP5_REG1 Register \(Offset = A4h\) \[reset = 0h\]: \[0\]](#)

15.9.43 IEP_CMP6_REG0 Register (Offset = A8h) [reset = 0h]

IEP_CMP6_REG0 is shown in [Figure 15-313](#) and described in [Table 15-956](#).

Return to [Summary Table](#).

Compare 6 Low Register.

Table 15-955. IEP_CMP6_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E0A8h
PRU_ICSSG0_IEP1	0B02 F0A8h
PRU_ICSSG1_IEP0	0B12 E0A8h
PRU_ICSSG1_IEP1	0B12 F0A8h

Figure 15-313. IEP_CMP6_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP6_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-956. IEP_CMP6_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP6_0	R/W	0h	Compare 6 low value

Table 15-957. Register Call Summary for IEP_CMP6_REG0

PRU_IEP_IEP Registers

- [IEP_CMP6_REG0 Register \(Offset = A8h\) \[reset = 0h\]: \[0\]](#)

15.9.44 IEP_CMP6_REG1 Register (Offset = ACh) [reset = 0h]

IEP_CMP6_REG1 is shown in [Figure 15-314](#) and described in [Table 15-959](#).

Return to [Summary Table](#).

Compare 6 High Register.

Table 15-958. IEP_CMP6_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E0ACh
PRU_ICSSG0_IEP1	0B02 F0ACh
PRU_ICSSG1_IEP0	0B12 E0ACh
PRU_ICSSG1_IEP1	0B12 F0ACh

Figure 15-314. IEP_CMP6_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP6_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-959. IEP_CMP6_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP6_1	R/W	0h	Compare 6 high value

Table 15-960. Register Call Summary for IEP_CMP6_REG1

PRU_IEP_IEP Registers

- [IEP_CMP6_REG1 Register \(Offset = ACh\) \[reset = 0h\]: \[0\]](#)

15.9.45 IEP_CMP7_REG0 Register (Offset = B0h) [reset = 0h]

IEP_CMP7_REG0 is shown in [Figure 15-315](#) and described in [Table 15-962](#).

Return to [Summary Table](#).

Compare 7 Low Register.

Table 15-961. IEP_CMP7_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E0B0h
PRU_ICSSG0_IEP1	0B02 F0B0h
PRU_ICSSG1_IEP0	0B12 E0B0h
PRU_ICSSG1_IEP1	0B12 F0B0h

Figure 15-315. IEP_CMP7_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP7_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-962. IEP_CMP7_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP7_0	R/W	0h	Compare 7 low value

Table 15-963. Register Call Summary for IEP_CMP7_REG0

PRU_IEP_IEP Registers

- [IEP_CMP7_REG0 Register \(Offset = B0h\) \[reset = 0h\]: \[0\]](#)

15.9.46 IEP_CMP7_REG1 Register (Offset = B4h) [reset = 0h]

IEP_CMP7_REG1 is shown in [Figure 15-316](#) and described in [Table 15-965](#).

Return to [Summary Table](#).

Compare 7 High Register.

Table 15-964. IEP_CMP7_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E0B4h
PRU_ICSSG0_IEP1	0B02 F0B4h
PRU_ICSSG1_IEP0	0B12 E0B4h
PRU_ICSSG1_IEP1	0B12 F0B4h

Figure 15-316. IEP_CMP7_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP7_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-965. IEP_CMP7_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP7_1	R/W	0h	Compare 7 high value

Table 15-966. Register Call Summary for IEP_CMP7_REG1

PRU_IEP_IEP Registers

- [IEP_CMP7_REG1 Register \(Offset = B4h\) \[reset = 0h\]: \[0\]](#)

15.9.47 IEP_RXIPG0_REG Register (Offset = B8h) [reset = FFFF0000h]

IEP_RXIPG0_REG is shown in [Figure 15-317](#) and described in [Table 15-968](#).

Return to [Summary Table](#).

Status for the RX port which is attached to PRU0 Register.

Table 15-967. IEP_RXIPG0_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E0B8h
PRU_ICSSG0_IEP1	0B02 F0B8h
PRU_ICSSG1_IEP0	0B12 E0B8h
PRU_ICSSG1_IEP1	0B12 F0B8h

Figure 15-317. IEP_RXIPG0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_MIN_IPG0																RX_IPG0															
R/W-FFFFh																R-0h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-968. IEP_RXIPG0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_MIN_IPG0	R/W	FFFFh	Defines the minimum number of ICSS_IEP_CLK/ICCS_VCLK_CLK cycles that is RX_DV is sampled low. It stores the smallest RX_IPG duration. It can be read at any time and gets updated after RX_IPG is updated, if RX_MIN_IPG is greater than RX_IPG.
15-0	RX_IPG0	R	0h	Records the current number of ICSS_IEP_CLK/ICCS_VCLK_CLK cycles RX_DV is sampled low. Value is updated after RX_DV transitions from low to high. It will saturate at FFFFh.

Table 15-969. Register Call Summary for IEP_RXIPG0_REG

PRU_IEP_IEP Registers

- [IEP_RXIPG0_REG Register \(Offset = B8h\) \[reset = FFFF0000h\]: \[0\]](#)

15.9.48 IEP_RXIPG1_REG Register (Offset = BCh) [reset = FFFF0000h]

IEP_RXIPG1_REG is shown in Figure 15-318 and described in Table 15-971.

Return to [Summary Table](#).

Status for the RX port which is attached to PRU1 Register.

Table 15-970. IEP_RXIPG1_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E0BCh
PRU_ICSSG0_IEP1	0B02 F0BCh
PRU_ICSSG1_IEP0	0B12 E0BCh
PRU_ICSSG1_IEP1	0B12 F0BCh

Figure 15-318. IEP_RXIPG1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_MIN_IPG1																RX_IPG1															
R/W-FFFFh																R-0h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-971. IEP_RXIPG1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_MIN_IPG1	R/W	FFFFh	Defines the minimum number of ICSS_IEP_CLK/ICSS_VCLK_CLK cycles that is RX_DV is sampled low. It stores the smallest RX_IPG duration. It can be read at any time and gets updated after RX_IPG is updated, if RX_MIN_IPG is greater than RX_IPG.
15-0	RX_IPG1	R	0h	Records the current number of ICSS_IEP_CLK/ICSS_VCLK_CLK cycles RX_DV is sampled low. Value is updated after RX_DV transitions from low to high. It will saturate at FFFFh.

Table 15-972. Register Call Summary for IEP_RXIPG1_REG

PRU_IEP_IEP Registers

- [IEP_RXIPG1_REG Register \(Offset = BCh\) \[reset = FFFF0000h\]: \[0\]](#)

15.9.49 IEP_CMP8_REG0 Register (Offset = C0h) [reset = 0h]

IEP_CMP8_REG0 is shown in [Figure 15-319](#) and described in [Table 15-974](#).

Return to [Summary Table](#).

Compare 8 Low Register.

Table 15-973. IEP_CMP8_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E0C0h
PRU_ICSSG0_IEP1	0B02 F0C0h
PRU_ICSSG1_IEP0	0B12 E0C0h
PRU_ICSSG1_IEP1	0B12 F0C0h

Figure 15-319. IEP_CMP8_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP8_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-974. IEP_CMP8_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP8_0	R/W	0h	Compare 8 low value

Table 15-975. Register Call Summary for IEP_CMP8_REG0

PRU_IEP_IEP Registers

- [IEP_CMP8_REG0 Register \(Offset = C0h\) \[reset = 0h\]: \[0\]](#)

15.9.50 IEP_CMP8_REG1 Register (Offset = C4h) [reset = 0h]

IEP_CMP8_REG1 is shown in [Figure 15-320](#) and described in [Table 15-977](#).

Return to [Summary Table](#).

Compare 8 High Register.

Table 15-976. IEP_CMP8_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E0C4h
PRU_ICSSG0_IEP1	0B02 F0C4h
PRU_ICSSG1_IEP0	0B12 E0C4h
PRU_ICSSG1_IEP1	0B12 F0C4h

Figure 15-320. IEP_CMP8_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP8_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-977. IEP_CMP8_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP8_1	R/W	0h	Compare 8 high value

Table 15-978. Register Call Summary for IEP_CMP8_REG1

PRU_IEP_IEP Registers

- [IEP_CMP8_REG1 Register \(Offset = C4h\) \[reset = 0h\]: \[0\]](#)

15.9.51 IEP_CMP9_REG0 Register (Offset = C8h) [reset = 0h]

IEP_CMP9_REG0 is shown in [Figure 15-321](#) and described in [Table 15-980](#).

Return to [Summary Table](#).

Compare 9 Low Register.

Table 15-979. IEP_CMP9_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E0C8h
PRU_ICSSG0_IEP1	0B02 F0C8h
PRU_ICSSG1_IEP0	0B12 E0C8h
PRU_ICSSG1_IEP1	0B12 F0C8h

Figure 15-321. IEP_CMP9_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP9_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-980. IEP_CMP9_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP9_0	R/W	0h	Compare 9 low value

Table 15-981. Register Call Summary for IEP_CMP9_REG0

PRU_IEP_IEP Registers

- [IEP_CMP9_REG0 Register \(Offset = C8h\) \[reset = 0h\]: \[0\]](#)

15.9.52 IEP_CMP9_REG1 Register (Offset = CCh) [reset = 0h]

IEP_CMP9_REG1 is shown in [Figure 15-322](#) and described in [Table 15-983](#).

Return to [Summary Table](#).

Compare 9 High Register.

Table 15-982. IEP_CMP9_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E0CCh
PRU_ICSSG0_IEP1	0B02 F0CCh
PRU_ICSSG1_IEP0	0B12 E0CCh
PRU_ICSSG1_IEP1	0B12 F0CCh

Figure 15-322. IEP_CMP9_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP9_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-983. IEP_CMP9_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP9_1	R/W	0h	Compare 9 high value

Table 15-984. Register Call Summary for IEP_CMP9_REG1

PRU_IEP_IEP Registers

- [IEP_CMP9_REG1 Register \(Offset = CCh\) \[reset = 0h\]: \[0\]](#)

15.9.53 IEP_CMP10_REG0 Register (Offset = D0h) [reset = 0h]

IEP_CMP10_REG0 is shown in [Figure 15-323](#) and described in [Table 15-986](#).

Return to [Summary Table](#).

Compare 10 Low Register.

Table 15-985. IEP_CMP10_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E0D0h
PRU_ICSSG0_IEP1	0B02 F0D0h
PRU_ICSSG1_IEP0	0B12 E0D0h
PRU_ICSSG1_IEP1	0B12 F0D0h

Figure 15-323. IEP_CMP10_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP10_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-986. IEP_CMP10_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP10_0	R/W	0h	Compare 10 low value

Table 15-987. Register Call Summary for IEP_CMP10_REG0

PRU_IEP_IEP Registers

- [IEP_CMP10_REG0 Register \(Offset = D0h\) \[reset = 0h\]: \[0\]](#)

15.9.54 IEP_CMP10_REG1 Register (Offset = D4h) [reset = 0h]

IEP_CMP10_REG1 is shown in [Figure 15-324](#) and described in [Table 15-989](#).

Return to [Summary Table](#).

Compare 10 High Register.

Table 15-988. IEP_CMP10_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E0D4h
PRU_ICSSG0_IEP1	0B02 F0D4h
PRU_ICSSG1_IEP0	0B12 E0D4h
PRU_ICSSG1_IEP1	0B12 F0D4h

Figure 15-324. IEP_CMP10_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP10_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-989. IEP_CMP10_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP10_1	R/W	0h	Compare 10 high value

Table 15-990. Register Call Summary for IEP_CMP10_REG1

PRU_IEP_IEP Registers

- [IEP_CMP10_REG1 Register \(Offset = D4h\) \[reset = 0h\]: \[0\]](#)

15.9.55 IEP_CMP11_REG0 Register (Offset = D8h) [reset = 0h]

IEP_CMP11_REG0 is shown in Figure 15-325 and described in Table 15-992.

Return to [Summary Table](#).

Compare 11 Low Register.

Table 15-991. IEP_CMP11_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E0D8h
PRU_ICSSG0_IEP1	0B02 F0D8h
PRU_ICSSG1_IEP0	0B12 E0D8h
PRU_ICSSG1_IEP1	0B12 F0D8h

Figure 15-325. IEP_CMP11_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP11_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-992. IEP_CMP11_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP11_0	R/W	0h	Compare 11 low value

Table 15-993. Register Call Summary for IEP_CMP11_REG0

PRU_IEP_IEP Registers

- [IEP_CMP11_REG0 Register \(Offset = D8h\) \[reset = 0h\]: \[0\]](#)

15.9.56 IEP_CMP11_REG1 Register (Offset = DCh) [reset = 0h]

IEP_CMP11_REG1 is shown in [Figure 15-326](#) and described in [Table 15-995](#).

Return to [Summary Table](#).

Compare 11 High Register.

Table 15-994. IEP_CMP11_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E0DCh
PRU_ICSSG0_IEP1	0B02 F0DCh
PRU_ICSSG1_IEP0	0B12 E0DCh
PRU_ICSSG1_IEP1	0B12 F0DCh

Figure 15-326. IEP_CMP11_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP11_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-995. IEP_CMP11_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP11_1	R/W	0h	Compare 11 high value

Table 15-996. Register Call Summary for IEP_CMP11_REG1

PRU_IEP_IEP Registers

- [IEP_CMP11_REG1 Register \(Offset = DCh\) \[reset = 0h\]: \[0\]](#)

15.9.57 IEP_CMP12_REG0 Register (Offset = E0h) [reset = 0h]

IEP_CMP12_REG0 is shown in [Figure 15-327](#) and described in [Table 15-998](#).

Return to [Summary Table](#).

Compare 12 Low Register.

Table 15-997. IEP_CMP12_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E0E0h
PRU_ICSSG0_IEP1	0B02 F0E0h
PRU_ICSSG1_IEP0	0B12 E0E0h
PRU_ICSSG1_IEP1	0B12 F0E0h

Figure 15-327. IEP_CMP12_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP12_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-998. IEP_CMP12_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP12_0	R/W	0h	Compare 12 low value

Table 15-999. Register Call Summary for IEP_CMP12_REG0

PRU_IEP_IEP Registers

- [IEP_CMP12_REG0 Register \(Offset = E0h\) \[reset = 0h\]: \[0\]](#)

15.9.58 IEP_CMP12_REG1 Register (Offset = E4h) [reset = 0h]

IEP_CMP12_REG1 is shown in [Figure 15-328](#) and described in [Table 15-1001](#).

Return to [Summary Table](#).

Compare 12 High Register.

Table 15-1000. IEP_CMP12_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E0E4h
PRU_ICSSG0_IEP1	0B02 F0E4h
PRU_ICSSG1_IEP0	0B12 E0E4h
PRU_ICSSG1_IEP1	0B12 F0E4h

Figure 15-328. IEP_CMP12_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP12_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1001. IEP_CMP12_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP12_1	R/W	0h	Compare 12 high value

Table 15-1002. Register Call Summary for IEP_CMP12_REG1

PRU_IEP_IEP Registers

- [IEP_CMP12_REG1 Register \(Offset = E4h\) \[reset = 0h\]: \[0\]](#)

15.9.59 IEP_CMP13_REG0 Register (Offset = E8h) [reset = 0h]

IEP_CMP13_REG0 is shown in [Figure 15-329](#) and described in [Table 15-1004](#).

Return to [Summary Table](#).

Compare 13 Low Register.

Table 15-1003. IEP_CMP13_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E0E8h
PRU_ICSSG0_IEP1	0B02 F0E8h
PRU_ICSSG1_IEP0	0B12 E0E8h
PRU_ICSSG1_IEP1	0B12 F0E8h

Figure 15-329. IEP_CMP13_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP13_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1004. IEP_CMP13_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP13_0	R/W	0h	Compare 13 low value

Table 15-1005. Register Call Summary for IEP_CMP13_REG0

PRU_IEP_IEP Registers

- [IEP_CMP13_REG0 Register \(Offset = E8h\) \[reset = 0h\]: \[0\]](#)

15.9.60 IEP_CMP13_REG1 Register (Offset = ECh) [reset = 0h]

IEP_CMP13_REG1 is shown in [Figure 15-330](#) and described in [Table 15-1007](#).

Return to [Summary Table](#).

Compare 13 High Register.

Table 15-1006. IEP_CMP13_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E0ECh
PRU_ICSSG0_IEP1	0B02 F0ECh
PRU_ICSSG1_IEP0	0B12 E0ECh
PRU_ICSSG1_IEP1	0B12 F0ECh

Figure 15-330. IEP_CMP13_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP13_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1007. IEP_CMP13_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP13_1	R/W	0h	Compare 13 high value

Table 15-1008. Register Call Summary for IEP_CMP13_REG1

PRU_IEP_IEP Registers

- [IEP_CMP13_REG1 Register \(Offset = ECh\) \[reset = 0h\]: \[0\]](#)

15.9.61 IEP_CMP14_REG0 Register (Offset = F0h) [reset = 0h]

IEP_CMP14_REG0 is shown in [Figure 15-331](#) and described in [Table 15-1010](#).

Return to [Summary Table](#).

Compare 14 Low Register.

Table 15-1009. IEP_CMP14_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E0F0h
PRU_ICSSG0_IEP1	0B02 F0F0h
PRU_ICSSG1_IEP0	0B12 E0F0h
PRU_ICSSG1_IEP1	0B12 F0F0h

Figure 15-331. IEP_CMP14_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP14_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1010. IEP_CMP14_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP14_0	R/W	0h	Compare 14 low value

Table 15-1011. Register Call Summary for IEP_CMP14_REG0

PRU_IEP_IEP Registers

- [IEP_CMP14_REG0 Register \(Offset = F0h\) \[reset = 0h\]: \[0\]](#)

15.9.62 IEP_CMP14_REG1 Register (Offset = F4h) [reset = 0h]

IEP_CMP14_REG1 is shown in [Figure 15-332](#) and described in [Table 15-1013](#).

Return to [Summary Table](#).

Compare 14 High Register.

Table 15-1012. IEP_CMP14_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E0F4h
PRU_ICSSG0_IEP1	0B02 F0F4h
PRU_ICSSG1_IEP0	0B12 E0F4h
PRU_ICSSG1_IEP1	0B12 F0F4h

Figure 15-332. IEP_CMP14_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP14_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1013. IEP_CMP14_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP14_1	R/W	0h	Compare 14 high value

Table 15-1014. Register Call Summary for IEP_CMP14_REG1

PRU_IEP_IEP Registers

- [IEP_CMP14_REG1 Register \(Offset = F4h\) \[reset = 0h\]: \[0\]](#)

15.9.63 IEP_CMP15_REG0 Register (Offset = F8h) [reset = 0h]

IEP_CMP15_REG0 is shown in [Figure 15-333](#) and described in [Table 15-1016](#).

Return to [Summary Table](#).

Compare 15 Low Register.

Table 15-1015. IEP_CMP15_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E0F8h
PRU_ICSSG0_IEP1	0B02 F0F8h
PRU_ICSSG1_IEP0	0B12 E0F8h
PRU_ICSSG1_IEP1	0B12 F0F8h

Figure 15-333. IEP_CMP15_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP15_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1016. IEP_CMP15_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP15_0	R/W	0h	Compare 15 low value

Table 15-1017. Register Call Summary for IEP_CMP15_REG0

PRU_IEP_IEP Registers

- [IEP_CMP15_REG0 Register \(Offset = F8h\) \[reset = 0h\]: \[0\]](#)

15.9.64 IEP_CMP15_REG1 Register (Offset = FCh) [reset = 0h]

IEP_CMP15_REG1 is shown in [Figure 15-334](#) and described in [Table 15-1019](#).

Return to [Summary Table](#).

Compare 15 High Register.

Table 15-1018. IEP_CMP15_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E0FCh
PRU_ICSSG0_IEP1	0B02 F0FCh
PRU_ICSSG1_IEP0	0B12 E0FCh
PRU_ICSSG1_IEP1	0B12 F0FCh

Figure 15-334. IEP_CMP15_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP15_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1019. IEP_CMP15_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP15_1	R/W	0h	Compare 15 high value

Table 15-1020. Register Call Summary for IEP_CMP15_REG1

PRU_IEP_IEP Registers

- [IEP_CMP15_REG1 Register \(Offset = FCh\) \[reset = 0h\]: \[0\]](#)

15.9.65 IEP_COUNT_RESET_VAL_REG0 Register (Offset = 100h) [reset = 0h]

IEP_COUNT_RESET_VAL_REG0 is shown in [Figure 15-335](#) and described in [Table 15-1022](#).

Return to [Summary Table](#).

Reset value of the Controller Counter (lower 32-bits) Register.

Table 15-1021. IEP_COUNT_RESET_VAL_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E100h
PRU_ICSSG0_IEP1	0B02 F100h
PRU_ICSSG1_IEP0	0B12 E100h
PRU_ICSSG1_IEP1	0B12 F100h

Figure 15-335. IEP_COUNT_RESET_VAL_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET_VAL_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1022. IEP_COUNT_RESET_VAL_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESET_VAL_0	R/W	0h	Reset value (lower 32-bits). This register enables SW to define the reset state of the Controller Counter, which can be reset by the following events (if enabled): CMP0 event; eHRPWM0_SYNCO event; eHRPWM3_SYNCO event. The RESET_VAL should be in increments of the DEFAULT_INC (default state is 5). For example, 0000_000Ah.

Table 15-1023. Register Call Summary for IEP_COUNT_RESET_VAL_REG0

PRU_IEP_IEP Registers

- [IEP_COUNT_RESET_VAL_REG0 Register \(Offset = 100h\) \[reset = 0h\]: \[0\]](#)

15.9.66 IEP_COUNT_RESET_VAL_REG1 Register (Offset = 104h) [reset = 0h]

IEP_COUNT_RESET_VAL_REG1 is shown in [Figure 15-336](#) and described in [Table 15-1025](#).

Return to [Summary Table](#).

Reset value of the Controller Counter (upper 32-bits) Register.

Table 15-1024. IEP_COUNT_RESET_VAL_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E104h
PRU_ICSSG0_IEP1	0B02 F104h
PRU_ICSSG1_IEP0	0B12 E104h
PRU_ICSSG1_IEP1	0B12 F104h

Figure 15-336. IEP_COUNT_RESET_VAL_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET_VAL_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1025. IEP_COUNT_RESET_VAL_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESET_VAL_1	R/W	0h	This enables SW to define the reset state of the Controller counter when it gets reset do to the following 3 possible events if enabled: CMP0 event; eHRPWM0_SYNCO event; eHRPWM3_SYNCO event. It should be in increments of the DEFAULT_INC, default state is 5 For example, 0000_000Ah

Table 15-1026. Register Call Summary for IEP_COUNT_RESET_VAL_REG1

PRU_IEP_IEP Registers

- [IEP_COUNT_RESET_VAL_REG1 Register \(Offset = 104h\) \[reset = 0h\]: \[0\]](#)

15.9.67 IEP_PWM_REG Register (Offset = 108h) [reset = X]

IEP_PWM_REG is shown in [Figure 15-337](#) and described in [Table 15-1028](#).

Return to [Summary Table](#).

PWM Sync Out Register.

Table 15-1027. IEP_PWM_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E108h
PRU_ICSSG0_IEP1	0B02 F108h
PRU_ICSSG1_IEP0	0B12 E108h
PRU_ICSSG1_IEP1	0B12 F108h

Figure 15-337. IEP_PWM_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				PWM3_HIT	PWM3_RST_CNT_EN	PWM0_HIT	PWM0_RST_CNT_EN
R/W-X				R/W1C-0h	R/W-0h	R/W1C-0h	R/W-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 15-1028. IEP_PWM_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3	PWM3_HIT	R/W1C	0h	The raw status bit of eHRPWM3_SYNCO event. 0h = No eHRPWM3_SYNCO event 1h = eHRPWM3_SYNCO event occurred Write 1 to Clear.
2	PWM3_RST_CNT_EN	R/W	0h	Enable the reset of the counter by a eHRPWM3_SYNCO event. 0h = Disable 1h = Enable the reset of the counter if a eHRPWM3_SYNCO event occurs
1	PWM0_HIT	R/W1C	0h	The raw status bit of eHRPWM0_SYNCO event. 0h = No eHRPWM0_SYNCO event 1h = eHRPWM0_SYNCO event occurred Write 1 to Clear.
0	PWM0_RST_CNT_EN	R/W	0h	Enable the reset of the counter by a eHRPWM0_SYNCO event. 0h = Disable 1h = Enable the reset of the counter if a eHRPWM0_SYNCO event occurs

Table 15-1029. Register Call Summary for IEP_PWM_REG

PRU_IEP_IEP Registers

- [IEP_PWM_REG Register \(Offset = 108h\) \[reset = X\]: \[0\]](#)

15.9.68 IEP_CAPR0_BI_REG0 Register (Offset = 10Ch) [reset = 0h]

IEP_CAPR0_BI_REG0 is shown in [Figure 15-338](#) and described in [Table 15-1031](#).

Return to [Summary Table](#).

Capture Big Endian Rise00 Register.

Table 15-1030. IEP_CAPR0_BI_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E10Ch
PRU_ICSSG0_IEP1	0B02 F10Ch
PRU_ICSSG1_IEP0	0B12 E10Ch
PRU_ICSSG1_IEP1	0B12 F10Ch

Figure 15-338. IEP_CAPR0_BI_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR0_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-1031. IEP_CAPR0_BI_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR0_0	R	0h	Capture Value for CAPR0 event. Big Endian Format The bytes are the same order. Within the byte, the bits are flipped.

Table 15-1032. Register Call Summary for IEP_CAPR0_BI_REG0

PRU_IEP_IEP Registers

- [IEP_CAPR0_BI_REG0 Register \(Offset = 10Ch\) \[reset = 0h\]: \[0\]](#)

15.9.69 IEP_CAPR0_BI_REG1 Register (Offset = 110h) [reset = 0h]

IEP_CAPR0_BI_REG1 is shown in [Figure 15-339](#) and described in [Table 15-1034](#).

Return to [Summary Table](#).

Capture Big Endian Rise10 Register.

Table 15-1033. IEP_CAPR0_BI_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E110h
PRU_ICSSG0_IEP1	0B02 F110h
PRU_ICSSG1_IEP0	0B12 E110h
PRU_ICSSG1_IEP1	0B12 F110h

Figure 15-339. IEP_CAPR0_BI_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR0_1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-1034. IEP_CAPR0_BI_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR0_1	R	0h	Capture Value for CAPR0 event. Big Endian Format The bytes are the same order. Within the byte, the bits are flipped.

Table 15-1035. Register Call Summary for IEP_CAPR0_BI_REG1

PRU_IEP_IEP Registers

- [IEP_CAPR0_BI_REG1 Register \(Offset = 110h\) \[reset = 0h\]: \[0\]](#)

15.9.70 IEP_CAPR1_BI_REG0 Register (Offset = 114h) [reset = 0h]

IEP_CAPR1_BI_REG0 is shown in [Figure 15-340](#) and described in [Table 15-1037](#).

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Capture Big Endian Rise01 Register.

Table 15-1036. IEP_CAPR1_BI_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E114h
PRU_ICSSG0_IEP1	0B02 F114h
PRU_ICSSG1_IEP0	0B12 E114h
PRU_ICSSG1_IEP1	0B12 F114h

Figure 15-340. IEP_CAPR1_BI_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR1_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-1037. IEP_CAPR1_BI_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR1_0	R	0h	Capture Value for CAPR1 event. The bytes are the same order. Within the byte, the bits are flipped.

Table 15-1038. Register Call Summary for IEP_CAPR1_BI_REG0

PRU_IEP_IEP Registers

- [IEP_CAPR1_BI_REG0 Register \(Offset = 114h\) \[reset = 0h\]: \[0\]](#)

15.9.71 IEP_CAPR1_BI_REG1 Register (Offset = 118h) [reset = 0h]

IEP_CAPR1_BI_REG1 is shown in [Figure 15-341](#) and described in [Table 15-1040](#).

Return to [Summary Table](#).

Capture Big Endian Rise11 Register

Table 15-1039. IEP_CAPR1_BI_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E118h
PRU_ICSSG0_IEP1	0B02 F118h
PRU_ICSSG1_IEP0	0B12 E118h
PRU_ICSSG1_IEP1	0B12 F118h

Figure 15-341. IEP_CAPR1_BI_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR1_1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-1040. IEP_CAPR1_BI_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR1_1	R	0h	Capture Value for CAPR1 event. The bytes are the same order. Within the byte, the bits are flipped.

Table 15-1041. Register Call Summary for IEP_CAPR1_BI_REG1

PRU_IEP_IEP Registers

- [IEP_CAPR1_BI_REG1 Register \(Offset = 118h\) \[reset = 0h\]: \[0\]](#)

15.9.72 IEP_CAPR2_BI_REG0 Register (Offset = 11Ch) [reset = 0h]

IEP_CAPR2_BI_REG0 is shown in [Figure 15-342](#) and described in [Table 15-1043](#).

Return to [Summary Table](#).

Capture Big Endian Rise02 Register.

Table 15-1042. IEP_CAPR2_BI_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E11Ch
PRU_ICSSG0_IEP1	0B02 F11Ch
PRU_ICSSG1_IEP0	0B12 E11Ch
PRU_ICSSG1_IEP1	0B12 F11Ch

Figure 15-342. IEP_CAPR2_BI_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR2_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-1043. IEP_CAPR2_BI_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR2_0	R	0h	Capture Value for CAPR2 event. The bytes are the same order. Within the byte, the bits are flipped.

Table 15-1044. Register Call Summary for IEP_CAPR2_BI_REG0

PRU_IEP_IEP Registers

- [IEP_CAPR2_BI_REG0 Register \(Offset = 11Ch\) \[reset = 0h\]: \[0\]](#)

15.9.73 IEP_CAPR2_BI_REG1 Register (Offset = 120h) [reset = 0h]

IEP_CAPR2_BI_REG1 is shown in [Figure 15-343](#) and described in [Table 15-1046](#).

Return to [Summary Table](#).

Capture Big Endian Rise12 Register.

Table 15-1045. IEP_CAPR2_BI_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E120h
PRU_ICSSG0_IEP1	0B02 F120h
PRU_ICSSG1_IEP0	0B12 E120h
PRU_ICSSG1_IEP1	0B12 F120h

Figure 15-343. IEP_CAPR2_BI_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR2_1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-1046. IEP_CAPR2_BI_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR2_1	R	0h	Capture Value for CAPR2 event. The bytes are the same order. Within the byte, the bits are flipped.

Table 15-1047. Register Call Summary for IEP_CAPR2_BI_REG1

PRU_IEP_IEP Registers

- [IEP_CAPR2_BI_REG1 Register \(Offset = 120h\) \[reset = 0h\]: \[0\]](#)

15.9.74 IEP_CAPR3_BI_REG0 Register (Offset = 124h) [reset = 0h]

IEP_CAPR3_BI_REG0 is shown in [Figure 15-344](#) and described in [Table 15-1049](#).

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Capture Big Endian Rise03 Register.

Table 15-1048. IEP_CAPR3_BI_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E124h
PRU_ICSSG0_IEP1	0B02 F124h
PRU_ICSSG1_IEP0	0B12 E124h
PRU_ICSSG1_IEP1	0B12 F124h

Figure 15-344. IEP_CAPR3_BI_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR3_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-1049. IEP_CAPR3_BI_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR3_0	R	0h	Capture Value for CAPR3 event. The bytes are the same order. Within the byte, the bits are flipped.

Table 15-1050. Register Call Summary for IEP_CAPR3_BI_REG0

PRU_IEP_IEP Registers

- [IEP_CAPR3_BI_REG0 Register \(Offset = 124h\) \[reset = 0h\]: \[0\]](#)

15.9.75 IEP_CAPR3_BI_REG1 Register (Offset = 128h) [reset = 0h]

IEP_CAPR3_BI_REG1 is shown in [Figure 15-345](#) and described in [Table 15-1052](#).

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Capture Big Endian Rise13 Register.

Table 15-1051. IEP_CAPR3_BI_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E128h
PRU_ICSSG0_IEP1	0B02 F128h
PRU_ICSSG1_IEP0	0B12 E128h
PRU_ICSSG1_IEP1	0B12 F128h

Figure 15-345. IEP_CAPR3_BI_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR3_1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-1052. IEP_CAPR3_BI_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR3_1	R	0h	Capture Value for CAPR3 event. The bytes are the same order. Within the byte, the bits are flipped.

Table 15-1053. Register Call Summary for IEP_CAPR3_BI_REG1

PRU_IEP_IEP Registers

- [IEP_CAPR3_BI_REG1 Register \(Offset = 128h\) \[reset = 0h\]: \[0\]](#)

15.9.76 IEP_CAPR4_BI_REG0 Register (Offset = 12Ch) [reset = 0h]

IEP_CAPR4_BI_REG0 is shown in [Figure 15-346](#) and described in [Table 15-1055](#).

[Return to Summary Table.](#)

Capture Big Endian Rise04 Register.

Table 15-1054. IEP_CAPR4_BI_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E12ch
PRU_ICSSG0_IEP1	0B02 F12ch
PRU_ICSSG1_IEP0	0B12 E12ch
PRU_ICSSG1_IEP1	0B12 F12ch

Figure 15-346. IEP_CAPR4_BI_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR4_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-1055. IEP_CAPR4_BI_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR4_0	R	0h	Capture Value for CAPR4 event. The bytes are the same order. Within the byte, the bits are flipped.

Table 15-1056. Register Call Summary for IEP_CAPR4_BI_REG0

PRU_IEP_IEP Registers

- [IEP_CAPR4_BI_REG0 Register \(Offset = 12Ch\) \[reset = 0h\]: \[0\]](#)

15.9.77 IEP_CAPR4_BI_REG1 Register (Offset = 130h) [reset = 0h]

IEP_CAPR4_BI_REG1 is shown in [Figure 15-347](#) and described in [Table 15-1058](#).

Return to [Summary Table](#).

Capture Big Endian Rise14 Register.

Table 15-1057. IEP_CAPR4_BI_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E130h
PRU_ICSSG0_IEP1	0B02 F130h
PRU_ICSSG1_IEP0	0B12 E130h
PRU_ICSSG1_IEP1	0B12 F130h

Figure 15-347. IEP_CAPR4_BI_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR4_1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-1058. IEP_CAPR4_BI_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR4_1	R	0h	Capture Value for CAPR4 event. The bytes are the same order. Within the byte, the bits are flipped.

Table 15-1059. Register Call Summary for IEP_CAPR4_BI_REG1

PRU_IEP_IEP Registers

- [IEP_CAPR4_BI_REG1 Register \(Offset = 130h\) \[reset = 0h\]: \[0\]](#)

15.9.78 IEP_CAPR5_BI_REG0 Register (Offset = 134h) [reset = 0h]

IEP_CAPR5_BI_REG0 is shown in [Figure 15-348](#) and described in [Table 15-1061](#).

[Return to Summary Table.](#)

Capture Big Endian Rise05 Register.

Table 15-1060. IEP_CAPR5_BI_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E134h
PRU_ICSSG0_IEP1	0B02 F134h
PRU_ICSSG1_IEP0	0B12 E134h
PRU_ICSSG1_IEP1	0B12 F134h

Figure 15-348. IEP_CAPR5_BI_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR5_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-1061. IEP_CAPR5_BI_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR5_0	R	0h	Capture Value for CAPR5 event. The bytes are the same order. Within the byte, the bits are flipped.

Table 15-1062. Register Call Summary for IEP_CAPR5_BI_REG0

PRU_IEP_IEP Registers

- [IEP_CAPR5_BI_REG0 Register \(Offset = 134h\) \[reset = 0h\]: \[0\]](#)

15.9.79 IEP_CAPR5_BI_REG1 Register (Offset = 138h) [reset = 0h]

IEP_CAPR5_BI_REG1 is shown in [Figure 15-349](#) and described in [Table 15-1064](#).

Return to [Summary Table](#).

Capture Big Endian Rise15 Register.

Table 15-1063. IEP_CAPR5_BI_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E138h
PRU_ICSSG0_IEP1	0B02 F138h
PRU_ICSSG1_IEP0	0B12 E138h
PRU_ICSSG1_IEP1	0B12 F138h

Figure 15-349. IEP_CAPR5_BI_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR5_1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-1064. IEP_CAPR5_BI_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR5_1	R	0h	Capture Value for CAPR5 event. The bytes are the same order. Within the byte, the bits are flipped.

Table 15-1065. Register Call Summary for IEP_CAPR5_BI_REG1

PRU_IEP_IEP Registers

- [IEP_CAPR5_BI_REG1 Register \(Offset = 138h\) \[reset = 0h\]: \[0\]](#)

15.9.80 IEP_CAPR6_BI_REG0 Register (Offset = 13Ch) [reset = 0h]

IEP_CAPR6_BI_REG0 is shown in [Figure 15-350](#) and described in [Table 15-1067](#).

Return to [Summary Table](#).

Capture Big Endian Rise06 Register.

Table 15-1066. IEP_CAPR6_BI_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E13Ch
PRU_ICSSG0_IEP1	0B02 F13Ch
PRU_ICSSG1_IEP0	0B12 E13Ch
PRU_ICSSG1_IEP1	0B12 F13Ch

Figure 15-350. IEP_CAPR6_BI_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR6_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-1067. IEP_CAPR6_BI_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR6_0	R	0h	Capture Value for CAPR6 event. The bytes are the same order. Within the byte, the bits are flipped.

Table 15-1068. Register Call Summary for IEP_CAPR6_BI_REG0

PRU_IEP_IEP Registers

- [IEP_CAPR6_BI_REG0 Register \(Offset = 13Ch\) \[reset = 0h\]: \[0\]](#)

15.9.81 IEP_CAPR6_BI_REG1 Register (Offset = 140h) [reset = 0h]

IEP_CAPR6_BI_REG1 is shown in [Figure 15-351](#) and described in [Table 15-1070](#).

Return to [Summary Table](#).

Capture Big Endian Rise16 Register.

Table 15-1069. IEP_CAPR6_BI_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E140h
PRU_ICSSG0_IEP1	0B02 F140h
PRU_ICSSG1_IEP0	0B12 E140h
PRU_ICSSG1_IEP1	0B12 F140h

Figure 15-351. IEP_CAPR6_BI_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR6_1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-1070. IEP_CAPR6_BI_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR6_1	R	0h	Capture Value for CAPR6 event. The bytes are the same order. Within the byte, the bits are flipped.

Table 15-1071. Register Call Summary for IEP_CAPR6_BI_REG1

PRU_IEP_IEP Registers

- [IEP_CAPR6_BI_REG1 Register \(Offset = 140h\) \[reset = 0h\]: \[0\]](#)

15.9.82 IEP_CAPF6_BI_REG0 Register (Offset = 144h) [reset = 0h]

IEP_CAPF6_BI_REG0 is shown in [Figure 15-352](#) and described in [Table 15-1073](#).

Return to [Summary Table](#).

Capture Big Endian Fall06 Register.

Table 15-1072. IEP_CAPF6_BI_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E144h
PRU_ICSSG0_IEP1	0B02 F144h
PRU_ICSSG1_IEP0	0B12 E144h
PRU_ICSSG1_IEP1	0B12 F144h

Figure 15-352. IEP_CAPF6_BI_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPF6_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-1073. IEP_CAPF6_BI_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPF6_0	R	0h	Capture Value for CAPF6 event. The bytes are the same order. Within the byte, the bits are flipped.

Table 15-1074. Register Call Summary for IEP_CAPF6_BI_REG0

PRU_IEP_IEP Registers

- [IEP_CAPF6_BI_REG0 Register \(Offset = 144h\) \[reset = 0h\]: \[0\]](#)

15.9.83 IEP_CAPF6_BI_REG1 Register (Offset = 148h) [reset = 0h]

IEP_CAPF6_BI_REG1 is shown in [Figure 15-353](#) and described in [Table 15-1076](#).

Return to [Summary Table](#).

Capture Big Endian Fall16 Register.

Table 15-1075. IEP_CAPF6_BI_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E148h
PRU_ICSSG0_IEP1	0B02 F148h
PRU_ICSSG1_IEP0	0B12 E148h
PRU_ICSSG1_IEP1	0B12 F148h

Figure 15-353. IEP_CAPF6_BI_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPF6_1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-1076. IEP_CAPF6_BI_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPF6_1	R	0h	Capture Value for CAPF6 event.

Table 15-1077. Register Call Summary for IEP_CAPF6_BI_REG1

PRU_IEP_IEP Registers

- [IEP_CAPF6_BI_REG1 Register \(Offset = 148h\) \[reset = 0h\]: \[0\]](#)

15.9.84 IEP_CAPR7_BI_REG0 Register (Offset = 14Ch) [reset = 0h]

IEP_CAPR7_BI_REG0 is shown in [Figure 15-354](#) and described in [Table 15-1079](#).

Return to [Summary Table](#).

Capture Big Endian Rise07 Register.

Table 15-1078. IEP_CAPR7_BI_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E14Ch
PRU_ICSSG0_IEP1	0B02 F14Ch
PRU_ICSSG1_IEP0	0B12 E14Ch
PRU_ICSSG1_IEP1	0B12 F14Ch

Figure 15-354. IEP_CAPR7_BI_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR7_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-1079. IEP_CAPR7_BI_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR7_0	R	0h	Capture Value for CAPR7 event. The bytes are the same order. Within the byte, the bits are flipped.

Table 15-1080. Register Call Summary for IEP_CAPR7_BI_REG0

PRU_IEP_IEP Registers

- [IEP_CAPR7_BI_REG0 Register \(Offset = 14Ch\) \[reset = 0h\]: \[0\]](#)

15.9.85 IEP_CAPR7_BI_REG1 Register (Offset = 150h) [reset = 0h]

IEP_CAPR7_BI_REG1 is shown in [Figure 15-355](#) and described in [Table 15-1082](#).

Return to [Summary Table](#).

Capture Big Endian Rise17 Register.

Table 15-1081. IEP_CAPR7_BI_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E150h
PRU_ICSSG0_IEP1	0B02 F150h
PRU_ICSSG1_IEP0	0B12 E150h
PRU_ICSSG1_IEP1	0B12 F150h

Figure 15-355. IEP_CAPR7_BI_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR7_1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-1082. IEP_CAPR7_BI_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR7_1	R	0h	Capture Value for CAPR7 event. The bytes are the same order. Within the byte, the bits are flipped.

Table 15-1083. Register Call Summary for IEP_CAPR7_BI_REG1

PRU_IEP_IEP Registers

- [IEP_CAPR7_BI_REG1 Register \(Offset = 150h\) \[reset = 0h\]: \[0\]](#)

15.9.86 IEP_CAPF7_BI_REG0 Register (Offset = 154h) [reset = 0h]

IEP_CAPF7_BI_REG0 is shown in [Figure 15-356](#) and described in [Table 15-1085](#).

Return to [Summary Table](#).

Capture Big Endian Fall07 Register.

Table 15-1084. IEP_CAPF7_BI_REG0 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E154h
PRU_ICSSG0_IEP1	0B02 F154h
PRU_ICSSG1_IEP0	0B12 E154h
PRU_ICSSG1_IEP1	0B12 F154h

Figure 15-356. IEP_CAPF7_BI_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPF7_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-1085. IEP_CAPF7_BI_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPF7_0	R	0h	Capture Value for CAPF7 event. The bytes are the same order. Within the byte, the bits are flipped.

Table 15-1086. Register Call Summary for IEP_CAPF7_BI_REG0

PRU_IEP_IEP Registers

- [IEP_CAPF7_BI_REG0 Register \(Offset = 154h\) \[reset = 0h\]: \[0\]](#)

15.9.87 IEP_CAPF7_BI_REG1 Register (Offset = 158h) [reset = 0h]

IEP_CAPF7_BI_REG1 is shown in [Figure 15-357](#) and described in [Table 15-1088](#).

Return to [Summary Table](#).

Capture Big Endian Fall17 Register.

Table 15-1087. IEP_CAPF7_BI_REG1 Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E158h
PRU_ICSSG0_IEP1	0B02 F158h
PRU_ICSSG1_IEP0	0B12 E158h
PRU_ICSSG1_IEP1	0B12 F158h

Figure 15-357. IEP_CAPF7_BI_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPF7_1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-1088. IEP_CAPF7_BI_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPF7_1	R	0h	Capture Value for CAPF7 event. The bytes are the same order. Within the byte, the bits are flipped.

Table 15-1089. Register Call Summary for IEP_CAPF7_BI_REG1

PRU_IEP_IEP Registers

- [IEP_CAPF7_BI_REG1 Register \(Offset = 158h\) \[reset = 0h\]: \[0\]](#)

15.9.88 IEP_SYNC_CTRL_REG Register (Offset = 180h) [reset = X]

IEP_SYNC_CTRL_REG is shown in Figure 15-358 and described in Table 15-1091.

Return to [Summary Table](#).

Sync Generation Control Register.

Table 15-1090. IEP_SYNC_CTRL_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E180h
PRU_ICSSG0_IEP1	0B02 F180h
PRU_ICSSG1_IEP0	0B12 E180h
PRU_ICSSG1_IEP1	0B12 F180h

Figure 15-358. IEP_SYNC_CTRL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED					RESERVED	RESERVED	SYNC1_IND_EN
R/W-X					R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SYNC1_CYCLIC_EN	SYNC1_ACK_EN	SYNC0_CYCLIC_EN	SYNC0_ACK_EN	RESERVED	SYNC1_EN	SYNC0_EN	SYNC_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-X	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1091. IEP_SYNC_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R/W	X	
10-9	RESERVED	R/W	0h	
8	SYNC1_IND_EN	R/W	0h	SYNC1 independent mode enable. Independent mode means the SYNC1 signal can be different from SYNC0. 0h = Dependent mode. SYNC1 is dependent on SYNC0 1h = Independent mode
7	SYNC1_CYCLIC_EN	R/W	0h	SYNC1 single shot or cyclic/auto generation mode enable 0h = Disable, single shot mode 1h = Enable, cyclic generation mode
6	SYNC1_ACK_EN	R/W	0h	SYNC1 acknowledgement mode enable 0h = Disable, SYNC1 will go low after pulse width is met. 1h = Enable, SYNC1 will remain asserted until receiving software acknowledges by writing "1" IEP_SYNC1_STAT_REG which clears on write.
5	SYNC0_CYCLIC_EN	R/W	0h	SYNC0 single shot or cyclic/auto generation mode enable 0h = Disable, single shot mode 1h = Enable, cyclic generation mode

Table 15-1091. IEP_SYNC_CTRL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SYNC0_ACK_EN	R/W	0h	SYNC0 acknowledgement mode enable 0h = Disable, SYNC0 will go low after pulse width is met. 1h = Enable, SYNC0 will remain asserted until receiving software acknowledges by writing IEP_SYNC0_STAT_REG which clears on write.
3	RESERVED	R/W	X	
2	SYNC1_EN	R/W	0h	SYNC1 generation enable 0h = Disable SYNC1 generation. If SYNC1 is low, it will stop immediately. If SYNC1 is high, it will stop after SYNC1 goes low 1h = Enable SYNC1 generation
1	SYNC0_EN	R/W	0h	SYNC0 generation enable 0h = Disable SYNC0 generation. If SYNC0 is low, it will stop immediately. If SYNC0 is high, it will stop after SYNC0 goes low 1h = Enable SYNC0 generation
0	SYNC_EN	R/W	0h	SYNC generation enable 0h = Disable the generation and clocking of SYNC0 and SYNC1 logic. If SYNC0 AND SYNC1 is low, it will stop immediately. If SYNC0 OR SYNC1 is high, it will stop after SYNC0 AND SYNC1 goes low. Note: that you might get 1 extra high pulse if this is disabled during a high pulse of one and the 2nd pulse goes high before the last pulse low if you do not de-assert sync0_en and sync1_en at the same time. SW should always de-assert both sync1_en and sync0_en at the same time as sync_en is de-asserted 1h = Enables SYNC0 and SYNC1 generation

Table 15-1092. Register Call Summary for IEP_SYNC_CTRL_REG

PRU_IEP_IEP Registers

- [IEP_SYNC_CTRL_REG Register \(Offset = 180h\) \[reset = X\]: \[0\]](#)

PRU_ICSSG IEP

- [\[4\]](#)

15.9.89 IEP_SYNC_FIRST_STAT_REG Register (Offset = 184h) [reset = X]

IEP_SYNC_FIRST_STAT_REG is shown in [Figure 15-359](#) and described in [Table 15-1094](#).

Return to [Summary Table](#).

Sync Generation First Event Status Register.

**Table 15-1093. IEP_SYNC_FIRST_STAT_REG
Instances**

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E184h
PRU_ICSSG0_IEP1	0B02 F184h
PRU_ICSSG1_IEP0	0B12 E184h
PRU_ICSSG1_IEP1	0B12 F184h

Figure 15-359. IEP_SYNC_FIRST_STAT_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED						FIRST_SYNC1	FIRST_SYNC0
R-X						R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 15-1094. IEP_SYNC_FIRST_STAT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	X	
1	FIRST_SYNC1	R	0h	SYNC1 First Event status 0h = SYNC1 first event has NOT occurred 1h = SYNC1 first event has occurred. This bits is cleared when sync1_en = 0
0	FIRST_SYNC0	R	0h	SYNC0 First Event status 0h = SYNC0 first event has not occurred 1h = SYNC0 first event has occurred. This bits is cleared when sync0_en = 0

Table 15-1095. Register Call Summary for IEP_SYNC_FIRST_STAT_REG

PRU_IEP_IEP Registers

- [IEP_SYNC_FIRST_STAT_REG Register \(Offset = 184h\) \[reset = X\]: \[0\]](#)

15.9.90 IEP_SYNC0_STAT_REG Register (Offset = 188h) [reset = X]

IEP_SYNC0_STAT_REG is shown in [Figure 15-360](#) and described in [Table 15-1097](#).

Return to [Summary Table](#).

Sync 0 Status Register.

Table 15-1096. IEP_SYNC0_STAT_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E188h
PRU_ICSSG0_IEP1	0B02 F188h
PRU_ICSSG1_IEP0	0B12 E188h
PRU_ICSSG1_IEP1	0B12 F188h

Figure 15-360. IEP_SYNC0_STAT_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							SYNC0_PEND
R-X							R-0h

LEGEND: R = Read Only; -n = value after reset

Table 15-1097. IEP_SYNC0_STAT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	SYNC0_PEND	R	0h	SYNC0 pending state 0h = SYNC0 is not pending 1h = SYNC0 is pending or has occurred when SYNC0_ACK_EN = 0 (Disable). Write "1" to clear

Table 15-1098. Register Call Summary for IEP_SYNC0_STAT_REG

PRU_IEP_IEP Registers

- [IEP_SYNC0_STAT_REG Register \(Offset = 188h\) \[reset = X\]: \[0\]](#)

15.9.91 IEP_SYNC1_STAT_REG Register (Offset = 18Ch) [reset = X]

IEP_SYNC1_STAT_REG is shown in [Figure 15-361](#) and described in [Table 15-1100](#).

Return to [Summary Table](#).

Sync 1 Status Register.

Table 15-1099. IEP_SYNC1_STAT_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E18Ch
PRU_ICSSG0_IEP1	0B02 F18Ch
PRU_ICSSG1_IEP0	0B12 E18Ch
PRU_ICSSG1_IEP1	0B12 F18Ch

Figure 15-361. IEP_SYNC1_STAT_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							SYNC1_PEND
R-X							R-0h

LEGEND: R = Read Only; -n = value after reset

Table 15-1100. IEP_SYNC1_STAT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	SYNC1_PEND	R	0h	SYNC1 pending state 0h = SYNC1 is not pending 1h = SYNC1 is pending or has occurred when SYNC1_ACK_EN = 0 (Disable). Write "1" to Clear

Table 15-1101. Register Call Summary for IEP_SYNC1_STAT_REG

PRU_IEP_IEP Registers

- [IEP_SYNC1_STAT_REG Register \(Offset = 18Ch\) \[reset = X\]: \[0\]](#)

15.9.92 IEP_SYNC_PWIDTH_REG Register (Offset = 190h) [reset = 0h]

IEP_SYNC_PWIDTH_REG is shown in [Figure 15-362](#) and described in [Table 15-1103](#).

Return to [Summary Table](#).

Sync Pulse Width Configure Register.

Table 15-1102. IEP_SYNC_PWIDTH_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E190h
PRU_ICSSG0_IEP1	0B02 F190h
PRU_ICSSG1_IEP0	0B12 E190h
PRU_ICSSG1_IEP1	0B12 F190h

Figure 15-362. IEP_SYNC_PWIDTH_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNC_HPWW																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1103. IEP_SYNC_PWIDTH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SYNC_HPWW	R/W	0h	Defines the number of clock cycles SYNC0/1 will be high. Note if SYNC0/1 is disabled during pulse width time (that is, SYNC_CTRL[SYNC0_EN SYNC1_EN SYNC_EN] = 0), the ongoing pulse will be terminated. 0h = 1 clock cycle. 1h = 2 clock cycles. Nh: N+1 clock cycles.

Table 15-1104. Register Call Summary for IEP_SYNC_PWIDTH_REG

PRU_IEP_IEP Registers
IEP_SYNC_PWIDTH_REG Register (Offset = 190h) [reset = 0h]: [0]
PRU_ICSSG IEP
PRU_ICSSG IEP Sync0/Sync1 Generation Modes: [0]

15.9.93 IEP_SYNC0_PERIOD_REG Register (Offset = 194h) [reset = 1h]

IEP_SYNC0_PERIOD_REG is shown in [Figure 15-363](#) and described in [Table 15-1106](#).

Return to [Summary Table](#).

Sync 0 Period Configure Register.

Table 15-1105. IEP_SYNC0_PERIOD_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E194h
PRU_ICSSG0_IEP1	0B02 F194h
PRU_ICSSG1_IEP0	0B12 E194h
PRU_ICSSG1_IEP1	0B12 F194h

Figure 15-363. IEP_SYNC0_PERIOD_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNC0_PERIOD																															
R/W-1h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1106. IEP_SYNC0_PERIOD_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SYNC0_PERIOD	R/W	1h	Defines the period between the rising edges of SYNC0. 0h = Reserved 1h = 2 clk cycles period N: N+1 clk cycles period

Table 15-1107. Register Call Summary for IEP_SYNC0_PERIOD_REG

PRU_IEP_IEP Registers
IEP_SYNC0_PERIOD_REG Register (Offset = 194h) [reset = 1h]: [0]
PRU_ICSSG IEP
PRU_ICSSG IEP Sync0/Sync1 Generation Modes: [0]

15.9.94 IEP_SYNC1_DELAY_REG Register (Offset = 198h) [reset = 0h]

IEP_SYNC1_DELAY_REG is shown in Figure 15-364 and described in Table 15-1109.

Return to [Summary Table](#).

Sync 1 Delay Register.

Table 15-1108. IEP_SYNC1_DELAY_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E198h
PRU_ICSSG0_IEP1	0B02 F198h
PRU_ICSSG1_IEP0	0B12 E198h
PRU_ICSSG1_IEP1	0B12 F198h

Figure 15-364. IEP_SYNC1_DELAY_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNC1_DELAY																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1109. IEP_SYNC1_DELAY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SYNC1_DELAY	R/W	0h	When SYNC1_IND_EN = 0, defines number of clock cycles from the start of SYNC0 to the start of SYNC1. Note: this is the delay before the start of SYNC1. 0h = No delay. 1h = 1 clock cycle delay. Nh: N clock cycles delay. When SYNC1_IND_EN = 1, defines the period between the rising edges of SYNC1. 0h = Reserved. 1h = 2 clock cycles period. Nh: N+1 clock cycles period.

Table 15-1110. Register Call Summary for IEP_SYNC1_DELAY_REG

PRU_IEP_IEP Registers IEP_SYNC1_DELAY_REG Register (Offset = 198h) [reset = 0h]: [0]
PRU_ICSSG IEP PRU_ICSSG IEP Sync0/Sync1 Generation Modes: [0] [1]

15.9.95 IEP_SYNC_START_REG Register (Offset = 19Ch) [reset = 0h]

IEP_SYNC_START_REG is shown in [Figure 15-365](#) and described in [Table 15-1112](#).

Return to [Summary Table](#).

Sync Start Configure Register.

Table 15-1111. IEP_SYNC_START_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E19Ch
PRU_ICSSG0_IEP1	0B02 F19Ch
PRU_ICSSG1_IEP0	0B12 E19Ch
PRU_ICSSG1_IEP1	0B12 F19Ch

Figure 15-365. IEP_SYNC_START_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNC_START																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1112. IEP_SYNC_START_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SYNC_START	R/W	0h	Defines the start time after the activation event. 0h = 1 clock cycle delay. Nh: N+1 clock cycles delay.

Table 15-1113. Register Call Summary for IEP_SYNC_START_REG

PRU_IEP_IEP Registers
IEP_SYNC_START_REG Register (Offset = 19Ch) [reset = 0h]: [0]
PRU_ICSSG IEP
PRU_ICSSG IEP Sync0/Sync1 Generation Modes: [0]

15.9.96 IEP_WD_PREDIV_REG Register (Offset = 200h) [reset = X]

IEP_WD_PREDIV_REG is shown in Figure 15-366 and described in Table 15-1115.

Return to [Summary Table](#).

Watchdog Pre-Divider Register

Table 15-1114. IEP_WD_PREDIV_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E200h
PRU_ICSSG0_IEP1	0B02 F200h
PRU_ICSSG1_IEP0	0B12 E200h
PRU_ICSSG1_IEP1	0B12 F200h

Figure 15-366. IEP_WD_PREDIV_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PRE_DIV															
R/W-X																R/W-4E20h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1115. IEP_WD_PREDIV_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	PRE_DIV	R/W	4E20h	Defines the number of ICSS_IEP_CLK cycles per WD clock event. Note that the WD clock is a free-running clock. The value 0x4e20 (or 20000) generates a rate of 100 us if ICSS_IEP_CLK is 200 MHz. seconds/(WD event) = (clock cycles per WD event)/(clock cycles per second) = 20000/(200 x [10]^6) = 100us

Table 15-1116. Register Call Summary for IEP_WD_PREDIV_REG

PRU_IEP_IEP Registers

- [IEP_WD_PREDIV_REG Register \(Offset = 200h\) \[reset = X\]: \[0\]](#)

15.9.97 IEP_PDI_WD_TIM_REG Register (Offset = 204h) [reset = X]

IEP_PDI_WD_TIM_REG is shown in [Figure 15-367](#) and described in [Table 15-1118](#).

Return to [Summary Table](#).

PDI Watchdog Timer Configure Register.

Table 15-1117. IEP_PDI_WD_TIM_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E204h
PRU_ICSSG0_IEP1	0B02 F204h
PRU_ICSSG1_IEP0	0B12 E204h
PRU_ICSSG1_IEP1	0B12 F204h

Figure 15-367. IEP_PDI_WD_TIM_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PDI_WD_TIME															
R/W-X																R/W-3E8h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1118. IEP_PDI_WD_TIM_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	PDI_WD_TIME	R/W	3E8h	Defines the number of WD ticks (or increments) for PDI WD, that is, the number of WD increments. If PRUSS_IEP_WD_PREDIV[15-0] PRE_DIV is set to 100us, then the value 0x03e8 (or 1000) provides a rate of 100ms. Read returns the current count. Counter is reset by software write to register or when Digital Data In capture occurs. WD is disabled if WD time is set to 0x0. Note: when an expiration event occurs, the expiration counter (PDI_EXP_CNT) increments and status (PDI_WD_STAT) clears.

Table 15-1119. Register Call Summary for IEP_PDI_WD_TIM_REG

PRU_IEP_IEP Registers

- [IEP_PDI_WD_TIM_REG Register \(Offset = 204h\) \[reset = X\]: \[0\]](#)

15.9.98 IEP_PD_WD_TIM_REG Register (Offset = 208h) [reset = X]

IEP_PD_WD_TIM_REG is shown in Figure 15-368 and described in Table 15-1121.

Return to [Summary Table](#).

PD Watchdog Timer Configure Register.

Table 15-1120. IEP_PD_WD_TIM_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E208h
PRU_ICSSG0_IEP1	0B02 F208h
PRU_ICSSG1_IEP0	0B12 E208h
PRU_ICSSG1_IEP1	0B12 F208h

Figure 15-368. IEP_PD_WD_TIM_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PD_WD_TIME															
R/W-X																R/W-3E8h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1121. IEP_PD_WD_TIM_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	PD_WD_TIME	R/W	3E8h	Defines the number of WD ticks (or increments) for PD WD, that is, the number of WD increments. If PRUSS_IEP_WD_PREDIV[15-0] PRE_DIV is set to 100us, then 0x03e8 (or 1000) provides a rate of 100ms. Read returns the current count. Counter is reset by software write to register or every write access to Sync Managers with WD trigger enable bit set. WD is disabled if WD time is set to 0x0. Expiration actions: Increment expiration counter, clear status. Digital Data out forced to zero if pr[k]_edio_oe_ext = 1 and PRUSS_IEP_DIGIO_EXP[0] SW_DATA_OUT_UPDATE = 0.

Table 15-1122. Register Call Summary for IEP_PD_WD_TIM_REG

PRU_IEP_IEP Registers

- [IEP_PD_WD_TIM_REG Register \(Offset = 208h\) \[reset = X\]: \[0\]](#)

15.9.99 IEP_WD_STATUS_REG Register (Offset = 20Ch) [reset = X]

IEP_WD_STATUS_REG is shown in [Figure 15-369](#) and described in [Table 15-1124](#).

Return to [Summary Table](#).

Watchdog Status Register.

Table 15-1123. IEP_WD_STATUS_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E20Ch
PRU_ICSSG0_IEP1	0B02 F20Ch
PRU_ICSSG1_IEP0	0B12 E20Ch
PRU_ICSSG1_IEP1	0B12 F20Ch

Figure 15-369. IEP_WD_STATUS_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							PDI_WD_STAT
R-X							R-1h
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							PD_WD_STAT
R-X							R-1h

LEGEND: R = Read Only; -n = value after reset

Table 15-1124. IEP_WD_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	X	
16	PDI_WD_STAT	R	1h	WD PDI status. 0h = Expired (PDI_WD_EXP event generated) 1h = Active or disabled
15-1	RESERVED	R	X	
0	PD_WD_STAT	R	1h	WD PD status (triggered by Sync Mangers status). 0h = Expired (PD_WD_EXP event generated) 1h = Active or disabled

Table 15-1125. Register Call Summary for IEP_WD_STATUS_REG

PRU_IEP_IEP Registers
IEP_WD_STATUS_REG Register (Offset = 20Ch) [reset = X]: [0]
PRU_ICSSG IEP
PRU_ICSSG IEP DIGIO:

15.9.100 IEP_WD_EXP_CNT_REG Register (Offset = 210h) [reset = X]

IEP_WD_EXP_CNT_REG is shown in [Figure 15-370](#) and described in [Table 15-1127](#).

Return to [Summary Table](#).

Watchdog Timer Expiration Counter Register.

Table 15-1126. IEP_WD_EXP_CNT_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E210h
PRU_ICSSG0_IEP1	0B02 F210h
PRU_ICSSG1_IEP0	0B12 E210h
PRU_ICSSG1_IEP1	0B12 F210h

Figure 15-370. IEP_WD_EXP_CNT_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PD_EXP_CNT								PDI_EXP_CNT							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1127. IEP_WD_EXP_CNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-8	PD_EXP_CNT	R/W	0h	WD PD expiration counter. Counter increments on every PD time out and stops at FFh.
7-0	PDI_EXP_CNT	R/W	0h	WD PDI expiration counter. Counter increments on every PDI time out and stops at FFh.

Table 15-1128. Register Call Summary for IEP_WD_EXP_CNT_REG

PRU_IEP_IEP Registers

- [IEP_WD_EXP_CNT_REG Register \(Offset = 210h\) \[reset = X\]: \[0\]](#)

15.9.101 IEP_WD_CTRL_REG Register (Offset = 214h) [reset = X]

IEP_WD_CTRL_REG is shown in [Figure 15-371](#) and described in [Table 15-1130](#).

Return to [Summary Table](#).

Watchdog Control Register.

Table 15-1129. IEP_WD_CTRL_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E214h
PRU_ICSSG0_IEP1	0B02 F214h
PRU_ICSSG1_IEP0	0B12 E214h
PRU_ICSSG1_IEP1	0B12 F214h

Figure 15-371. IEP_WD_CTRL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							PDI_WD_EN
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							PD_WD_EN
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1130. IEP_WD_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16	PDI_WD_EN	R/W	0h	Watchdog PDI 0h = Disable 1h = Enable
15-1	RESERVED	R/W	X	
0	PD_WD_EN	R/W	0h	Watchdog PD 0h = Disable 1h = Enable

Table 15-1131. Register Call Summary for IEP_WD_CTRL_REG

PRU_IEP_IEP Registers

- [IEP_WD_CTRL_REG Register \(Offset = 214h\) \[reset = X\]: \[0\]](#)

15.9.102 IEP_DIGIO_CTRL_REG Register (Offset = 300h) [reset = X]

IEP_DIGIO_CTRL_REG is shown in Figure 15-372 and described in Table 15-1133.

Return to [Summary Table](#).

DIGIO Control Register.

Table 15-1132. IEP_DIGIO_CTRL_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E300h
PRU_ICSSG0_IEP1	0B02 F300h
PRU_ICSSG1_IEP0	0B12 E300h
PRU_ICSSG1_IEP1	0B12 F300h

Figure 15-372. IEP_DIGIO_CTRL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
OUT_MODE		IN_MODE		WD_MODE	BIDI_MODE	OUTVALID_MODE	OUTVALID_PO L
R/W-0h		R/W-0h		R/W-0h	R-1h	R/W-0h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-1133. IEP_DIGIO_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-6	OUT_MODE	R/W	0h	Defines events that triggers data out to be updated. Note if OUTVALID_MODE is set, then data out is forced to zero if a WD PD expiration occurs (PD_WD_EXP) from the WD block and pr<k>_edio_oe_ext = 1. 0h = PRU0/1_RX_EOF 1h = Reserved 2h: DC SYNC0 event 3h = DC SYNC1 event After ML release keep Reserved in filter2 and delete Reserved without filter

Table 15-1133. IEP_DIGIO_CTRL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	IN_MODE	R/W	0h	Defines event that triggers data in to be sampled 0h = PRU0/1_RX_SOF After ML release put PRU0/1_RX_SOF to filter1; delete Reserved without filter 1h = Rising edge of external PR<k>_EDC_LATCH0_IN signal 2h: DC rising edge of SYNC0 event After ML release put DC rising edge of SYNC0 event to filter1; delete Reserved without filter 3h = DC rising edge of SYNC1 event After ML release put DC rising edge of SYNC1 event to filter1; delete Reserved without filter
3	WD_MODE	R/W	0h	Defines Watchdog behavior 0h = Outputs are reset immediately after watchdog expires 1h = Outputs are reset with next output event that follows watchdog expiration After ML release keep Reserved in filter2 and delete Reserved without filter
2	BIDI_MODE	R	1h	Defines the digital input/output direction. NOTE THAT DUE TO INTEGRATION, ACTUAL MODE IS UNIDIRECTIONAL IN THIS DEVICE. 0h = Unidirectional mode: digital input/output direction of pins configured individually 1h = Bidirectional mode: all I/O pins are bidirectional and direction configuration is ignored After ML release keep Reserved in filter2 and delete Reserved without filter
1	OUTVALID_MODE	R/W	0h	Defines the outvalid mode behavior. 0h = Output event signaling 1h = Output data is updated if watchdog is triggered. Output data is forced to zero if PD_WD_EXP from the WD block and pr1_edio_oe_ext = 1 After ML release keep Reserved in filter2 and delete Reserved without filter
0	OUTVALID_POL	R	0h	Defines OUTVALID polarity 0h = Active High 1h = Active Low After ML release keep Reserved in filter2 and delete Reserved without filter

Table 15-1134. Register Call Summary for IEP_DIGIO_CTRL_REG

PRU_IEP_IEP Registers

- [IEP_DIGIO_CTRL_REG Register \(Offset = 300h\) \[reset = X\]: \[0\]](#)

PRU_ICSSG IEP

- [PRU_ICSSG IEP DIGIO Block Diagrams: \[0\] \[1\]](#)
- [PRU_ICSSG IEP Basic Programming Model: \[0\]](#)
- [PRU_ICSSG IEP DIGIO: \[0\]](#)

15.9.103 IEP_DIGIO_STATUS_REG Register (Offset = 304h) [reset = 0h]

IEP_DIGIO_STATUS_REG is shown in Figure 15-373 and described in Table 15-1136.

Return to [Summary Table](#).

DIGIO Status Register.

Table 15-1135. IEP_DIGIO_STATUS_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E304h
PRU_ICSSG0_IEP1	0B02 F304h
PRU_ICSSG1_IEP0	0B12 E304h
PRU_ICSSG1_IEP1	0B12 F304h

Figure 15-373. IEP_DIGIO_STATUS_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIGIO_STAT																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-1136. IEP_DIGIO_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DIGIO_STAT	R	0h	Reserved

Table 15-1137. Register Call Summary for IEP_DIGIO_STATUS_REG

PRU_IEP_IEP Registers

- [PRU_IEP_IEP Registers: \[0\] \[2\]](#)
- [IEP_DIGIO_STATUS_REG Register \(Offset = 304h\) \[reset = 0h\]: \[0\]](#)

15.9.104 IEP_DIGIO_DATA_IN_REG Register (Offset = 308h) [reset = 0h]

IEP_DIGIO_DATA_IN_REG is shown in [Figure 15-374](#) and described in [Table 15-1139](#).

Return to [Summary Table](#).

DIGIO Data Input Register.

Table 15-1138. IEP_DIGIO_DATA_IN_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E308h
PRU_ICSSG0_IEP1	0B02 F308h
PRU_ICSSG1_IEP0	0B12 E308h
PRU_ICSSG1_IEP1	0B12 F308h

Figure 15-374. IEP_DIGIO_DATA_IN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA_IN																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-1139. IEP_DIGIO_DATA_IN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA_IN	R	0h	Data input. Digital inputs can be configured to be sampled in four ways. 1h = Digital inputs are sampled at the start of each frame. The SOF signal can be used externally to update the input data, because the SOF is signaled before input data is sampled. 2h: The sample time can be controlled externally by using the PR<k>_EDC_LATCH0_IN signal. 3h = Digital inputs are sampled at SYNC0 events. 4h = Digital inputs are sampled at SYNC1 events. These can be configured by [5-4] IN_MODE bit field in the PRUSS_IEP_DIGIO_CTRL register.

Table 15-1140. Register Call Summary for IEP_DIGIO_DATA_IN_REG

PRU_IEP_IEP Registers IEP_DIGIO_DATA_IN_REG Register (Offset = 308h) [reset = 0h]: [0]
PRU_ICSSG IEP PRU_ICSSG IEP Basic Programming Model: [0] PRU_ICSSG IEP DIGIO Features: [0]

15.9.105 IEP_DIGIO_DATA_IN_RAW_REG Register (Offset = 30Ch) [reset = 0h]

IEP_DIGIO_DATA_IN_RAW_REG is shown in [Figure 15-375](#) and described in [Table 15-1142](#).

Return to [Summary Table](#).

DIGIO Data Input Direct Sample Register.

Table 15-1141. IEP_DIGIO_DATA_IN_RAW_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E30Ch
PRU_ICSSG0_IEP1	0B02 F30Ch
PRU_ICSSG1_IEP0	0B12 E30Ch
PRU_ICSSG1_IEP1	0B12 F30Ch

Figure 15-375. IEP_DIGIO_DATA_IN_RAW_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA_IN_RAW																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-1142. IEP_DIGIO_DATA_IN_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA_IN_RAW	R	0h	Data input which direct sample of PR<k>_EDIO_DATA[0:31]. Only PR<k>_EDIO_DATA[0:3] are exported to device pins in this device.

Table 15-1143. Register Call Summary for IEP_DIGIO_DATA_IN_RAW_REG

PRU_IEP_IEP Registers
IEP_DIGIO_DATA_IN_RAW_REG Register (Offset = 30Ch) [reset = 0h]: [0]
PRU_ICSSG IEP
PRU_ICSSG IEP Basic Programming Model: [0] PRU_ICSSG IEP DIGIO Features: [0]

15.9.106 IEP_DIGIO_DATA_OUT_REG Register (Offset = 310h) [reset = 0h]

IEP_DIGIO_DATA_OUT_REG is shown in [Figure 15-376](#) and described in [Table 15-1145](#).

Return to [Summary Table](#).

DIGIO Data Output Register.

**Table 15-1144. IEP_DIGIO_DATA_OUT_REG
Instances**

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E310h
PRU_ICSSG0_IEP1	0B02 F310h
PRU_ICSSG1_IEP0	0B12 E310h
PRU_ICSSG1_IEP1	0B12 F310h

Figure 15-376. IEP_DIGIO_DATA_OUT_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA_OUT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1145. IEP_DIGIO_DATA_OUT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA_OUT	R/W	0h	Data output. Digital outputs can be configured to be updated in four ways. 1h = Digital outputs are updated at the end of each frame (EOF mode). 2h: Digital outputs are updated with SYNC0 events 3h = Digital outputs are updated SYNC1 events. 4h = Digital outputs are updated at the end of a frame which triggered the Process Data Watchdog. Digital Outputs are only updated if the frame was correct (WD_TRIG mode). These can be configured by [7-6] OUT_MODE bit field in the PRUSS_IEP_DIGIO_CTRL.

Table 15-1146. Register Call Summary for IEP_DIGIO_DATA_OUT_REG

PRU_IEP_IEP Registers
IEP_DIGIO_DATA_OUT_REG Register (Offset = 310h) [reset = 0h]: [0]
PRU_ICSSG IEP
PRU_ICSSG IEP Basic Programming Model: [0] [1]

15.9.107 IEP_DIGIO_DATA_OUT_EN_REG Register (Offset = 314h) [reset = 0h]

IEP_DIGIO_DATA_OUT_EN_REG is shown in [Figure 15-377](#) and described in [Table 15-1148](#).

Return to [Summary Table](#).

DIGIO Data Input which controls tri-state of pr<k>_edio_data_out_en[3:0] Register.

Table 15-1147. IEP_DIGIO_DATA_OUT_EN_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E314h
PRU_ICSSG0_IEP1	0B02 F314h
PRU_ICSSG1_IEP0	0B12 E314h
PRU_ICSSG1_IEP1	0B12 F314h

Figure 15-377. IEP_DIGIO_DATA_OUT_EN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA_OUT_EN																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1148. IEP_DIGIO_DATA_OUT_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA_OUT_EN	R/W	0h	Data input which controls tri-state of PR<k>_EDIO_DATA[0:3] 0h = Driver enabled. 1h = Sets outputs to HiZ.

Table 15-1149. Register Call Summary for IEP_DIGIO_DATA_OUT_EN_REG

PRU_IEP_IEP Registers
IEP_DIGIO_DATA_OUT_EN_REG Register (Offset = 314h) [reset = 0h]: [0]
PRU_ICSSG IEP
PRU_ICSSG IEP Basic Programming Model: [0]

15.9.108 IEP_DIGIO_EXP_REG Register (Offset = 318h) [reset = X]

IEP_DIGIO_EXP_REG is shown in [Figure 15-378](#) and described in [Table 15-1151](#).

Return to [Summary Table](#).

DIGIO, Defines which RX_EOF is used Register.

Table 15-1150. IEP_DIGIO_EXP_REG Instances

Instance	Physical Address
PRU_ICSSG0_IEP0	0B02 E318h
PRU_ICSSG0_IEP1	0B02 F318h
PRU_ICSSG1_IEP0	0B12 E318h
PRU_ICSSG1_IEP1	0B12 F318h

Figure 15-378. IEP_DIGIO_EXP_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED		EOF_SEL	SOF_SEL	SOF_DLY			
R/W-X		R/W-0h	R/W-0h	R/W-0h			
7	6	5	4	3	2	1	0
OUTVALID_DLY				RESERVED	SW_OUTVALID	OUTVALID_OV R_EN	SW_DATA_OU T_UP
R/W-2h				R/W-X	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1151. IEP_DIGIO_EXP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13	EOF_SEL	R/W	0h	Defines which RX_EOF is used for PR<k>_EDIO_DATA_IN[0:3] capture 0h = PRU0_RX_EOF 1h = PRU1_RX_EOF After ML release keep Reserved in filter2 and delete Reserved without filter
12	SOF_SEL	R/W	0h	Defines which RX_SOF is used for PR<k>_EDIO_DATA_IN[0:3] capture 0h = PRU0_RX_SOF 1h = PRU1_RX_SOF After ML release keep Reserved in filter2 and delete Reserved without filter
11-8	SOF_DLY	R/W	0h	Define the number of iep_clk (ICSS_IEP_CLK) cycle delay of SOF PR<k>_EDIO_DATA_IN[0:3] capture After ML release keep Reserved in filter2 and delete Reserved without filter

Table 15-1151. IEP_DIGIO_EXP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-4	OUTVALID_DLY	R/W	2h	Define the number of iep_clk (ICSS_IEP_CLK) cycle delay on assertion of PR<k>_EDIO_OUTVALID. Min is 2 clock cycles. Max is 16 clock cycles After ML release keep Reserved in filter2 and delete Reserved without filter
3	RESERVED	R/W	X	
2	SW_OUTVALID	R/W	0h	PR<k>_EDIO_OUTVALID = SW_OUTVALID, only if OUTVALID_OVR_EN is set. After ML release keep Reserved in filter2 and delete Reserved without filter
1	OUTVALID_OVR_EN	R/W	0h	Software override enable 0h = Disable override 1h = Enable override
0	SW_DATA_OUT_UP	R/W	0h	Defines the value of pr<k>_edio_data_out when OUTVALID_OVR_EN = 1. Read 0h = Start bit event has not occurred Read 1h = Start bit event occurred Write 0h = No effect Write 1h = Causes an update of pr<k>_edio_data_out by software data out

Table 15-1152. Register Call Summary for IEP_DIGIO_EXP_REG

PRU_IEP_IEP Registers
IEP_DIGIO_EXP_REG Register (Offset = 318h) [reset = X]: [0]
PRU_ICSSG IEP
PRU_ICSSG IEP DIGIO Block Diagrams: [0] [1] PRU_ICSSG IEP Basic Programming Model: [0] [1] PRU_ICSSG IEP DIGIO: [0]

15.10 PRU_MDIO_MDIO Registers

Table 15-1154 lists the memory-mapped registers for the PRU_MDIO_MDIO registers. All register offset addresses not listed in Table 15-1154 should be considered as reserved locations and the register contents should not be modified.

Table 15-1153. PRU_MDIO_MDIO Instances

Instance	Base Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDIO	0B03 2400h
PRU_ICSSG1_PR1_MDIO_V1P7_MDIO	0B13 2400h

Table 15-1154. PRU_MDIO_MDIO Registers

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_MDIO_V1P7_MDIO Physical Address	PRU_ICSSG1_PR1_MDIO_V1P7_MDIO Physical Address
0h	MDIO_VERSION_REG	MDIO Version Register	0B03 2400h	0B13 2400h
4h	MDIO_CONTROL_REG	MDIO Control Register	0B03 2404h	0B13 2404h
8h	MDIO_ALIVE_REG	MDIO Alive Register	0B03 2408h	0B13 2408h
Ch	MDIO_LINK_REG	MDIO Link Register	0B03 240Ch	0B13 240Ch
10h	MDIO_LINK_INT_RAW_REG	MDIO Link Interrupt Raw Register	0B03 2410h	0B13 2410h
14h	MDIO_LINK_INT_MASKED_REG	MDIO Link Interrupt Masked Register	0B03 2414h	0B13 2414h
18h	MDIO_LINK_INT_MASK_SET_REG	MDIO Link Interrupt Mask Set Register	0B03 2418h	0B13 2418h
1Ch	MDIO_LINK_INT_MASK_CLEAR_REG	MDIO Link Interrupt Mask Clear Register	0B03 241Ch	0B13 241Ch
20h	MDIO_USER_INT_RAW_REG	MDIO User Interrupt Raw Register	0B03 2420h	0B13 2420h
24h	MDIO_USER_INT_MASKED_REG	MDIO User Interrupt Masked Register	0B03 2424h	0B13 2424h
28h	MDIO_USER_INT_MASK_SET_REG	MDIO User Interrupt Mask Set Register	0B03 2428h	0B13 2428h
2Ch	MDIO_USER_INT_MASK_CLEAR_REG	MDIO User Interrupt Mask Clear Register	0B03 242Ch	0B13 242Ch
30h	MDIO_MANUAL_IF_REG	MDIO Manual Interface Register	0B03 2430h	0B13 2430h
34h	MDIO_POLL_REG	MDIO Poll Inter Register	0B03 2434h	0B13 2434h
38h	MDIO_POLL_EN_REG	MDIO Poll Enable Register	0B03 2438h	0B13 2438h
3Ch	MDIO_CLAUS45_REG	Clause 45 Register	0B03 243Ch	0B13 243Ch
40h	MDIO_USER_ADDR0_REG	MDIO User Address 0 Register	0B03 2440h	0B13 2440h
44h	MDIO_USER_ADDR1_REG	MDIO User Address 1 Register	0B03 2444h	0B13 2444h
80h	MDIO_USER_ACCESS_REG_j	MDIO User Access j Register	0B03 2480h	0B13 2480h
84h	MDIO_USER_PHY_SEL_REG_j	MDIO User PHY Select j Register	0B03 2484h	0B13 2484h

15.10.1 MDIO_VERSION_REG Register (Offset = 0h) [reset = 00070107h]

MDIO_VERSION_REG is shown in [Figure 15-379](#) and described in [Table 15-1156](#).

[Return to Summary Table.](#)

MDIO Version Register.

Table 15-1155. MDIO_VERSION_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDI O	0B03 2400h
PRU_ICSSG1_PR1_MDIO_V1P7_MDI O	0B13 2400h

Figure 15-379. MDIO_VERSION_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MODID																REVMAJ								REVMINOR							
R-7h																R-1h								R-7h							

LEGEND: R = Read Only; -n = value after reset

Table 15-1156. MDIO_VERSION_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	7h	Module Identification value
15-8	REVMAJ	R	1h	Major revision value
7-0	REVMINOR	R	7h	Minor revision value

Table 15-1157. Register Call Summary for MDIO_VERSION_REG

PRU_MDIO_MDIO Registers

- [PRU_MDIO_MDIO Registers](#): [0]
- [MDIO_VERSION_REG Register \(Offset = 0h\) \[reset = 00070107h\]](#): [0]

15.10.2 MDIO_CONTROL_REG Register (Offset = 4h) [reset = X]

MDIO_CONTROL_REG is shown in Figure 15-380 and described in Table 15-1159.

Return to [Summary Table](#).

MDIO Control Register.

Table 15-1158. MDIO_CONTROL_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDIO	0B03 2404h
PRU_ICSSG1_PR1_MDIO_V1P7_MDIO	0B13 2404h

Figure 15-380. MDIO_CONTROL_REG Register

31	30	29	28	27	26	25	24
IDLE	ENABLE	RESERVED	HIGHEST_USER_CHANNEL				
R-1h	R/W-0h	R/W-X	R-1h				
23	22	21	20	19	18	17	16
RESERVED			PREAMBLE	FAULT	FAULT_DETECT_ENABLE	INT_TEST_ENABLE	RESERVED
R/W-X			R/W-0h	R/W1C-0h	R/W-0h	R/W-0h	R/W-X
15	14	13	12	11	10	9	8
CLKDIV							
R/W-FFh							
7	6	5	4	3	2	1	0
CLKDIV							
R/W-FFh							

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 15-1159. MDIO_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IDLE	R	1h	MDIO state machine IDLE. Set to 1h when the state machine is in the idle state.
30	ENABLE	R/W	0h	Enable control. Writing a 1 to this bit enables the MDIO state machine, writing a 0h disables it. If the MDIO state machine is active at the time it is disabled, it will complete the current operation before halting and setting the idle bit. If using byte access, the enable bit has to be the last bit written in this register.
29	RESERVED	R/W	X	
28-24	HIGHEST_USER_CHANNEL	R	1h	Highest user channel. This field specifies the highest user access channel that is available in the module and is currently set to 1h. This implies that MDIO_USER_ACCESS_REG_1 is the highest available user access channel.
23-21	RESERVED	R/W	X	
20	PREAMBLE	R/W	0h	Preamble disable. Writing a 1h to this bit disables this device from sending MDIO frame preambles in clause 22 mode of operation. This bit has no effect in clause 45 mode of operation.

Table 15-1159. MDIO_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	FAULT	R/W1C	0h	Fault indicator. This bit is set to 1h if the MDIO pins fail to read back what the device is driving onto them. This indicates a physical layer fault and the module state machine is reset. Writing a 1 to it clears this bit.
18	FAULT_DETECT_ENABLE	R/W	0h	Fault detect enable. This bit has to be set to 1h to enable the physical layer fault detection.
17	INT_TEST_ENABLE	R/W	0h	Interrupt test enable. This bit can be set to 1h to enable the host to set the userint and linkint bits for test purposes.
16	RESERVED	R/W	X	
15-0	CLKDIV	R/W	FFh	Clock Divider. This field specifies the division ratio between CLK and the frequency of MDCLK. MDCLK is disabled when [15-0] CLKDIV is set to 0h. MDCLK frequency = clk frequency/(clkdiv+1).

Table 15-1160. Register Call Summary for MDIO_CONTROL_REG

PRU_MDIO_MDIO Registers - MDIO_LINK_INT_RAW_REG Register (Offset = 10h) [reset = X]: [0] [1] - PRU_MDIO_MDIO Registers: [0] - MDIO_USER_INT_MASKED_REG Register (Offset = 24h) [reset = X]: [0] - MDIO_USER_INT_RAW_REG Register (Offset = 20h) [reset = X]: [0] - MDIO_CONTROL_REG Register (Offset = 4h) [reset = X]: [0]
PRU_ICSSG MII MDIO Functional Description PRU_ICSSG MII MDIO Interractions: [0]
PRU_ICSSG MII MDIO Module PRU_ICSSG MII MDIO Receive/Transmit Frame Host Software Interface: [0] [1] [2]

15.10.3 MDIO_ALIVE_REG Register (Offset = 8h) [reset = 0h]

MDIO_ALIVE_REG is shown in [Figure 15-381](#) and described in [Table 15-1162](#).

Return to [Summary Table](#).

MDIO Alive Register.

Table 15-1161. MDIO_ALIVE_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDI O	0B03 2408h
PRU_ICSSG1_PR1_MDIO_V1P7_MDI O	0B13 2408h

Figure 15-381. MDIO_ALIVE_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALIVE																															
R/W1C-0h																															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 15-1162. MDIO_ALIVE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ALIVE	R/W1C	0h	MDIO Alive. Each of the 32 bits of this register is set if the most recent access to the PHY with address corresponding to the register bit number was acknowledged by the PHY, the bit is reset if the PHY fails to acknowledge the access. Both the user and polling accesses to a PHY will cause the corresponding alive bit to be updated. The alive bits are intended to be used to give an indication of the presence or not of the PHY with the corresponding address. Writing a 1 to any bit will clear it, writing a 0 has no effect.

Table 15-1163. Register Call Summary for MDIO_ALIVE_REG

PRU_MDIO_MDIO Registers
PRU_MDIO_MDIO Registers: [0] MDIO_ALIVE_REG Register (Offset = 8h) [reset = 0h]: [0]
PRU_ICSSG MII MDIO Functional Description
State Change Mode ([30]STATECHANGEMODE = 1h): [0] PRU_ICSSG MII MDIO Interractions: [0] [1] [2]
PRU_ICSSG MII MDIO Module
PRU_ICSSG MII MDIO Receive/Transmit Frame Host Software Interface: [0] [1]

15.10.4 MDIO_LINK_REG Register (Offset = Ch) [reset = 0h]

MDIO_LINK_REG is shown in [Figure 15-382](#) and described in [Table 15-1165](#).

Return to [Summary Table](#).

MDIO Link Register.

Table 15-1164. MDIO_LINK_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDI O	0B03 240Ch
PRU_ICSSG1_PR1_MDIO_V1P7_MDI O	0B13 240Ch

Figure 15-382. MDIO_LINK_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LINK																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-1165. MDIO_LINK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LINK	R	0h	MDIO Link state. This register is updated after a read of the Generic Status Register of a PHY. The corresponding bit is set if the PHY with the corresponding address has link and the PHY acknowledges the read transaction. The bit is cleared to zero if the PHY indicates it does not have link or fails to acknowledge the read transaction. Writes to the register have no effect. In addition, in Normal Mode Operation, the status of the two PHYs specified in the MDIO_USER_PHY_SEL_REG_j register can be determined using the MLINK input pins. This is determined by the linksel bit in the MDIO_USER_PHY_SEL_REG_j register. In State Change Mode the MLINK input pins are unused.

Table 15-1166. Register Call Summary for MDIO_LINK_REG

PRU_MDIO_MDIO Registers MDIO_LINK_INT_RAW_REG Register (Offset = 10h) [reset = X]: [0] [1] PRU_MDIO_MDIO Registers: [0] MDIO_LINK_INT_MASKED_REG Register (Offset = 14h) [reset = X]: [0] MDIO_LINK_REG Register (Offset = Ch) [reset = 0h]: [0]
PRU_ICSSG MII MDIO Functional Description State Change Mode ([30]STATECHANGEMODE = 1h): [0] PRU_ICSSG MII MDIO Interactions: [0] [1]
PRU_ICSSG MII MDIO Module PRU_ICSSG MII MDIO Receive/Transmit Frame Host Software Interface: [0] [1]

15.10.5 MDIO_LINK_INT_RAW_REG Register (Offset = 10h) [reset = X]

MDIO_LINK_INT_RAW_REG is shown in Figure 15-383 and described in Table 15-1168.

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MDIO Link Interrupt Raw Register.

Table 15-1167. MDIO_LINK_INT_RAW_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDIO	0B03 2410h
PRU_ICSSG1_PR1_MDIO_V1P7_MDIO	0B13 2410h

Figure 15-383. MDIO_LINK_INT_RAW_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						LINKINTRAW	
R/W-X						R/W1C-0h	

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 15-1168. MDIO_LINK_INT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	

Table 15-1168. MDIO_LINK_INT_RAW_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	LINKINTRAW	R/W1C	0h	MDIO link change event raw value. Normal mode operation: When asserted '1', a bit indicates that there was an MDIO link change event (that is, change in the MDIO_LINK_REG register) corresponding to the PHY address in the MDIO_USER_PHY_SEL_REG_j register. LINKINTRAW[0] and LINKINTRAW[1] correspond to MDIO_USER_PHY_SEL_REG_0 and MDIO_USER_PHY_SEL_REG_1, respectively. Writing a 1h will clear the event and writing 0 has no effect. If the int_test bit in the MDIO_CONTROL_REG register is set, the host may set LINKINTRAW bits to a 1h which may be used for test purposes. MDIO link change event raw value. State Change Mode operation: The LINKINTRAW[0] bit will be asserted '1' when any bit (for any PHY) in the MDIOAlive or MDIO_LINK_REG registers changes due to MDIO operations. The LINKINTRAW[1] bit is unused in State Change Mode. State Change Mode allows any state change in any PHY to issue an interrupt. If the int_test bit in the MDIO_CONTROL_REG register is set, the host may set the LINKINTRAW[0] bit to a 1h which may be used for test purposes.

Table 15-1169. Register Call Summary for MDIO_LINK_INT_RAW_REG

PRU_MDIO_MDIO Registers MDIO_LINK_INT_RAW_REG Register (Offset = 10h) [reset = X]: [0] PRU_MDIO_MDIO Registers: [0]
PRU_ICSSG MII MDIO Functional Description PRU_ICSSG MII MDIO Interractions: [0] [1]
PRU_ICSSG MII MDIO Module PRU_ICSSG MII MDIO Receive/Transmit Frame Host Software Interface: [0]

15.10.6 MDIO_LINK_INT_MASKED_REG Register (Offset = 14h) [reset = X]

MDIO_LINK_INT_MASKED_REG is shown in [Figure 15-384](#) and described in [Table 15-1171](#).

Return to [Summary Table](#).

MDIO Link Interrupt Masked Register.

Table 15-1170. MDIO_LINK_INT_MASKED_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDIO	0B03 2414h
PRU_ICSSG1_PR1_MDIO_V1P7_MDIO	0B13 2414h

Figure 15-384. MDIO_LINK_INT_MASKED_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						LINKINTMASKED	
R/W-X						R/W1C-0h	

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 15-1171. MDIO_LINK_INT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1-0	LINKINTMASKED	R/W1C	0h	MDIO link change interrupt masked value. Normal mode operation: When asserted '1', a bit indicates that there was an MDIO link change event (that is, change in the MDIO_LINK_REG register) corresponding to the PHY address in the MDIO_USER_PHY_SEL_REG_j register and the corresponding linkint_enable bit was set. linkintmasked[0] and linkintmasked[1] correspond to MDIO_USER_PHY_SEL_REG_0 and MDIO_USER_PHY_SEL_REG_1, respectively. Writing a 1h will clear the interrupt and writing 0 has no effect. These masked interrupt bits are the MDIO_LINKINT[1:0] pin values. MDIO link change interrupt masked value. State Change Mode operation: The linkintmasked[0] bit will be asserted '1' when LINKINTRAW[0] is asserted '1' and when the linkintmaskset bit is set to 1h. Writing a 1h will clear linkintmasked[0] (and the MDIO_LINKINT[0] output) and writing 0h has no effect. The linkintmasked[1] bit is not used in State Change Mode (MDIO_LINKINT[1] is therefore also unused in State Change Mode).

Table 15-1172. Register Call Summary for MDIO_LINK_INT_MASKED_REG

PRU_MDIO_MDIO Registers - MDIO_LINK_INT_MASKED_REG Register (Offset = 14h) [reset = X]: [0] - PRU_MDIO_MDIO Registers: [0]
PRU_ICSSG MII MDIO Functional Description - State Change Mode ([30]STATECHANGEMODE = 1h): [0] - PRU_ICSSG MII MDIO Interractions: [0] - Normal Mode ([30]STATECHANGEMODE = 0h): [0]
PRU_ICSSG MII MDIO Module PRU_ICSSG MII MDIO Receive/Transmit Frame Host Software Interface: [0]

15.10.7 MDIO_LINK_INT_MASK_SET_REG Register (Offset = 18h) [reset = X]

MDIO_LINK_INT_MASK_SET_REG is shown in [Figure 15-385](#) and described in [Table 15-1174](#).

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MDIO Link Interrupt Mask Set Register.

Table 15-1173. MDIO_LINK_INT_MASK_SET_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDIO	0B03 2418h
PRU_ICSSG1_PR1_MDIO_V1P7_MDIO	0B13 2418h

Figure 15-385. MDIO_LINK_INT_MASK_SET_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							LINKINTMASK SET
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 15-1174. MDIO_LINK_INT_MASK_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	LINKINTMASKSET	R/W1S	0h	MDIO link interrupt mask set. Normal Mode Operation: This register is not used in normal mode. In normal mode the MDIO_LINKINT[1:0] interrupts are enabled with the linkint_enable bit in the associated MDIO_USER_PHY_SEL_REG_j register. MDIO link interrupt mask set. State Change Mode Operation: Writing this bit to 1h will enable the MDIO link status change interrupt (MDIO_LINKINT[0]) to be asserted when LINKINTRAW[0] is asserted.

Table 15-1175. Register Call Summary for MDIO_LINK_INT_MASK_SET_REG

PRU_MDIO_MDIO Registers
MDIO_LINK_INT_MASK_SET_REG Register (Offset = 18h) [reset = X]: [0] PRU_MDIO_MDIO Registers: [0]
PRU_ICSSG MII MDIO Module
PRU_ICSSG MII MDIO Receive/Transmit Frame Host Software Interface: [0]

15.10.8 MDIO_LINK_INT_MASK_CLEAR_REG Register (Offset = 1Ch) [reset = X]

MDIO_LINK_INT_MASK_CLEAR_REG is shown in [Figure 15-386](#) and described in [Table 15-1177](#).

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MDIO Link Interrupt Mask Clear Register.

Table 15-1176. MDIO_LINK_INT_MASK_CLEAR_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDIO	0B03 241Ch
PRU_ICSSG1_PR1_MDIO_V1P7_MDIO	0B13 241Ch

Figure 15-386. MDIO_LINK_INT_MASK_CLEAR_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							LINKINTMASK CLR
R/W-X							R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 15-1177. MDIO_LINK_INT_MASK_CLEAR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	LINKINTMASKCLR	R/W1C	0h	MDIO link interrupt mask clear. Normal Mode Operation: This register is not used in normal mode. In normal mode the MDIO_LINKINT[1:0] interrupts are enabled with the linkint_enable bit in the associated MDIO_USER_PHY_SEL_REG_j register. MDIO link interrupt mask clear. State Change Mode Operation: Writing this bit to 1h will disable the MDIO link status change interrupt (MDIO_LINKINT[0]) regardless of the LINKINTRAW[0] bit value.

Table 15-1178. Register Call Summary for MDIO_LINK_INT_MASK_CLEAR_REG

PRU_MDIO_MDIO Registers
PRU_MDIO_MDIO Registers: [0] MDIO_LINK_INT_MASK_CLEAR_REG Register (Offset = 1Ch) [reset = X]: [0]
PRU_ICSSG MII MDIO Module
PRU_ICSSG MII MDIO Receive/Transmit Frame Host Software Interface: [0]

15.10.9 MDIO_USER_INT_RAW_REG Register (Offset = 20h) [reset = X]

MDIO_USER_INT_RAW_REG is shown in [Figure 15-387](#) and described in [Table 15-1180](#).

Return to [Summary Table](#).

MDIO User Interrupt Raw Register.

**Table 15-1179. MDIO_USER_INT_RAW_REG
Instances**

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDIO	0B03 2420h
PRU_ICSSG1_PR1_MDIO_V1P7_MDIO	0B13 2420h

Figure 15-387. MDIO_USER_INT_RAW_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						USERINTRAW	
R/W-X						R/W1C-0h	

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 15-1180. MDIO_USER_INT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1-0	USERINTRAW	R/W1C	0h	Raw value of MDIO user command complete event for MDIO_USER_ACCESS_REG_1 through MDIO_USER_ACCESS_REG_0, respectively. When asserted '1', a bit indicates that the previously scheduled PHY read or write command using that particular MDIO_USER_ACCESS_REG_j register has completed. Writing a 1h will clear the event and writing 0h has no effect. If the int_test bit in the MDIO_CONTROL_REG register is set, the host may set the userintraw bits to a 1h. This mode may be used for test purposes.

Table 15-1181. Register Call Summary for MDIO_USER_INT_RAW_REG

PRU_MDIO_MDIO Registers
PRU_MDIO_MDIO Registers: [0] MDIO_USER_INT_RAW_REG Register (Offset = 20h) [reset = X]: [0]
PRU_ICSSG MII MDIO Functional Description
PRU_ICSSG MII MDIO Interractions: [0]

Table 15-1181. Register Call Summary for MDIO_USER_INT_RAW_REG (continued)

PRU_ICSSG MII MDIO Module

- [PRU_ICSSG MII MDIO Receive/Transmit Frame Host Software Interface: \[0\] \[1\]](#)

15.10.10 MDIO_USER_INT_MASKED_REG Register (Offset = 24h) [reset = X]

MDIO_USER_INT_MASKED_REG is shown in Figure 15-388 and described in Table 15-1183.

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MDIO User Interrupt Masked Register.

Table 15-1182. MDIO_USER_INT_MASKED_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDIO	0B03 2424h
PRU_ICSSG1_PR1_MDIO_V1P7_MDIO	0B13 2424h

Figure 15-388. MDIO_USER_INT_MASKED_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						USERINTMASKED	
R/W-X						R/W1C-0h	

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 15-1183. MDIO_USER_INT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1-0	USERINTMASKED	R/W1C	0h	Masked value of MDIO user command complete interrupt for MDIO_USER_ACCESS_REG_1 through MDIO_USER_ACCESS_REG_0, respectively. When asserted '1', a bit indicates that the previously scheduled PHY read or write command using that particular MDIO_USER_ACCESS_REG_j register has completed and the corresponding userintmaskset bit is set to 1h. Writing a 1h will clear the interrupt and writing 0h has no effect. If the int_test bit in the MDIO_CONTROL_REG register is set, the host may set the USERINTMASKED bits to a 1h. This mode may be used for test purposes.

Table 15-1184. Register Call Summary for MDIO_USER_INT_MASKED_REG

PRU_MDIO_MDIO Registers
- PRU_MDIO_MDIO Registers: [0] - MDIO_USER_INT_MASKED_REG Register (Offset = 24h) [reset = X]: [0]
PRU_ICSSG MII MDIO Functional Description
- PRU_ICSSG MII MDIO Interactions: [0] - Normal Mode ([30]STATECHANGEMODE = 0h): [0]

Table 15-1184. Register Call Summary for MDIO_USER_INT_MASKED_REG (continued)

PRU_ICSSG MII MDIO Module

- [PRU_ICSSG MII MDIO Receive/Transmit Frame Host Software Interface: \[0\] \[1\] \[2\] \[3\]](#)

15.10.11 MDIO_USER_INT_MASK_SET_REG Register (Offset = 28h) [reset = X]

MDIO_USER_INT_MASK_SET_REG is shown in Figure 15-389 and described in Table 15-1186.

Return to [Summary Table](#).

MDIO User Interrupt Mask Set Register.

Table 15-1185. MDIO_USER_INT_MASK_SET_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDI O	0B03 2428h
PRU_ICSSG1_PR1_MDIO_V1P7_MDI O	0B13 2428h

Figure 15-389. MDIO_USER_INT_MASK_SET_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						USERINTMASKSET	
R/W-X						R/W1S-0h	

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 15-1186. MDIO_USER_INT_MASK_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1-0	USERINTMASKSET	R/W1S	0h	MDIO user interrupt mask set for USERINTMASKED[1:0], respectively. Writing a bit to 1h will enable MDIO user command complete interrupts for that particular MDIO_USER_ACCESS_REG_j register. MDIO user interrupt for a particular MDIO_USER_ACCESS_REG_j register is disabled if the corresponding bit is 0h. Writing a 0h to this register has no effect.

Table 15-1187. Register Call Summary for MDIO_USER_INT_MASK_SET_REG

PRU_MDIO_MDIO Registers
PRU_MDIO_MDIO Registers: [0] MDIO_USER_INT_MASK_SET_REG Register (Offset = 28h) [reset = X]: [0]
PRU_ICSSG MII MDIO Functional Description
PRU_ICSSG MII MDIO Interractions: [0] Normal Mode ([30]STATECHANGEMODE = 0h): [0]
PRU_ICSSG MII MDIO Module
PRU_ICSSG MII MDIO Receive/Transmit Frame Host Software Interface: [0] [1] [2] [3]

15.10.12 MDIO_USER_INT_MASK_CLEAR_REG Register (Offset = 2Ch) [reset = X]

MDIO_USER_INT_MASK_CLEAR_REG is shown in Figure 15-390 and described in Table 15-1189.

Return to [Summary Table](#).

MDIO User Interrupt Mask Clear Register.

Table 15-1188.
MDIO_USER_INT_MASK_CLEAR_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDIO	0B03 242Ch
PRU_ICSSG1_PR1_MDIO_V1P7_MDIO	0B13 242Ch

Figure 15-390. MDIO_USER_INT_MASK_CLEAR_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						USERINTMASKCLR	
R/W-X						R/W1C-0h	

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 15-1189. MDIO_USER_INT_MASK_CLEAR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1-0	USERINTMASKCLR	R/W1C	0h	MDIO user command complete interrupt mask clear for USERINTMASKED[1:0], respectively. Writing a bit to 1h will disable further user command complete interrupts for that particular MDIO_USER_ACCESS_REG_j register. Writing a 0h to this register has no effect.

Table 15-1190. Register Call Summary for MDIO_USER_INT_MASK_CLEAR_REG

PRU_MDIO_MDIO Registers
- PRU_MDIO_MDIO Registers: [0] - MDIO_USER_INT_MASK_CLEAR_REG Register (Offset = 2Ch) [reset = X]: [0]
PRU_ICSSG MII MDIO Functional Description
PRU_ICSSG MII MDIO Interractions: [0]
PRU_ICSSG MII MDIO Module
PRU_ICSSG MII MDIO Receive/Transmit Frame Host Software Interface: [0]

15.10.13 MDIO_MANUAL_IF_REG Register (Offset = 30h) [reset = X]

MDIO_MANUAL_IF_REG is shown in [Figure 15-391](#) and described in [Table 15-1192](#).

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MDIO Manual Interface Register.

Table 15-1191. MDIO_MANUAL_IF_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDI O	0B03 2430h
PRU_ICSSG1_PR1_MDIO_V1P7_MDI O	0B13 2430h

Figure 15-391. MDIO_MANUAL_IF_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED					MDIO_MDCLK_ O	MDIO_OE	MDIO_PIN
R/W-X					R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1192. MDIO_MANUAL_IF_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	X	
2	MDIO_MDCLK_O	R/W	0h	MDIO Clock Output. This value is the MDCLK_O output value when the MANUALMODE bit is set in the MDIO_POLL_REG register.
1	MDIO_OE	R/W	0h	MDIO Output Enable. This value is inverted and output on the MDIO_OE_N output when the MANUALMODE bit is set in the MDIO_POLL_REG register.
0	MDIO_PIN	R/W	0h	MDIO_Pin Value. This is the external MDIO data pin value when the MANUALMODE bit is set in the MDIO_POLL_REG register. That is, this value is driven on the MDIO_O (the MDIO serial data output) when MDIO_OE is asserted '1'. The read value for this bit comes from MDIO_I (the MDIO serial data input). If MDIO_OE is asserted '1' and MDIO_PIN is written with a 1h then MDIO_PIN should read a 1h if there are no external devices pulling the MDIO data line low.

Table 15-1193. Register Call Summary for MDIO_MANUAL_IF_REG

PRU_MDIO_MDIO Registers • MDIO_MANUAL_IF_REG Register (Offset = 30h) [reset = X]: [0] • PRU_MDIO_MDIO Registers: [0] • MDIO_POLL_REG Register (Offset = 34h) [reset = X]: [0]
PRU_ICSSG MII MDIO Module • PRU_ICSSG MII MDIO Receive/Transmit Frame Host Software Interface: [0]

15.10.14 MDIO_POLL_REG Register (Offset = 34h) [reset = X]

MDIO_POLL_REG is shown in Figure 15-392 and described in Table 15-1195.

Return to [Summary Table](#).

MDIO Poll Inter Register.

Table 15-1194. MDIO_POLL_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDI O	0B03 2434h
PRU_ICSSG1_PR1_MDIO_V1P7_MDI O	0B13 2434h

Figure 15-392. MDIO_POLL_REG Register

31	30	29	28	27	26	25	24
MANUALMODE	STATECHANG EMODE	RESERVED					
R/W-0h	R/W-0h	R/W-X					
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
IPG							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1195. MDIO_POLL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MANUALMODE	R/W	0h	Manual Mode. When set 1h, the MDIO pins are directly controlled by software through the bits in the MDIO_MANUAL_IF_REG register
30	STATECHANGEMODE	R/W	0h	State Change Mode. When set, the MDIO is operating in State Change Mode. When clear, the MDIO is operating in normal mode. State change mode effects interrupt operations.
29-8	RESERVED	R/W	X	
7-0	IPG	R/W	0h	Polling Inter Packet Gap Value. This value is the number of MDCLK_O clocks between each poll when polling is enabled.

Table 15-1196. Register Call Summary for MDIO_POLL_REG

PRU_MDIO_MDIO Registers
MDIO_MANUAL_IF_REG Register (Offset = 30h) [reset = X]: [0] [1] [2] PRU_MDIO_MDIO Registers: [0] MDIO_POLL_REG Register (Offset = 34h) [reset = X]: [0]
PRU_ICSSG MII MDIO Functional Description
Manual Mode: [0]

Table 15-1196. Register Call Summary for MDIO_POLL_REG (continued)

PRU_ICSSG MII MDIO Module

- [PRU_ICSSG MII MDIO Receive/Transmit Frame Host Software Interface: \[0\]](#)

15.10.15 MDIO_POLL_EN_REG Register (Offset = 38h) [reset = FFFFFFFFh]

MDIO_POLL_EN_REG is shown in [Figure 15-393](#) and described in [Table 15-1198](#).

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MDIO Poll Enable Register.

Table 15-1197. MDIO_POLL_EN_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDI O	0B03 2438h
PRU_ICSSG1_PR1_MDIO_V1P7_MDI O	0B13 2438h

Figure 15-393. MDIO_POLL_EN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POLL_EN																															
R/W-FFFFFFFh																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1198. MDIO_POLL_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	POLL_EN	R/W	FFFFFFFh	Poll Enable. When set, the bit indicates that the associated PHY will be included in polling operations. When clear, the associated PHY will not be polled. Each bit in this field is associated with a PHY. Bit zero is associated with PHY 0 and so on. Due to a limitation in the hardware, bit 31 must always be set (regardless of the value of the preamble disable bit in the MDIO_CONTROL register. However, there does not have to be a PHY at address 31.

Table 15-1199. Register Call Summary for MDIO_POLL_EN_REG

PRU_MDIO_MDIO Registers PRU_MDIO_MDIO Registers: [0] MDIO_POLL_EN_REG Register (Offset = 38h) [reset = FFFFFFFFh]: [0]
PRU_ICSSG MII MDIO Functional Description PRU_ICSSG MII MDIO Interactions: [0]
PRU_ICSSG MII MDIO Module PRU_ICSSG MII MDIO Receive/Transmit Frame Host Software Interface: [0]

15.10.16 MDIO_CLAUS45_REG Register (Offset = 3Ch) [reset = 0h]

MDIO_CLAUS45_REG is shown in [Figure 15-394](#) and described in [Table 15-1201](#).

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Claus 45 Register.

Table 15-1200. MDIO_CLAUS45_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDI O	0B03 243Ch
PRU_ICSSG1_PR1_MDIO_V1P7_MDI O	0B13 243Ch

Figure 15-394. MDIO_CLAUS45_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLAUSE45																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1201. MDIO_CLAUS45_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CLAUSE45	R/W	0h	MDIO clause 45 mode. When a CLAUSE45 bit is cleared to 0h, the PHY associated with the CLAUSE45 bit is operating in the clause 22 mode. When set 1h, the PHY associated with the CLAUSE45 bit is operating in the clause 45 mode. Bit 0 is associated with PHY 0 and so on.

Table 15-1202. Register Call Summary for MDIO_CLAUS45_REG

PRU_MDIO_MDIO Registers
PRU_MDIO_MDIO Registers: [0] MDIO_CLAUS45_REG Register (Offset = 3Ch) [reset = 0h]: [0]
PRU_ICSSG MII MDIO Module
PRU_ICSSG MII MDIO Receive/Transmit Frame Host Software Interface: [0]

15.10.17 MDIO_USER_ADDR0_REG Register (Offset = 40h) [reset = X]

MDIO_USER_ADDR0_REG is shown in [Figure 15-395](#) and described in [Table 15-1204](#).

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MDIO User Address 0 Register.

Table 15-1203. MDIO_USER_ADDR0_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDI O	0B03 2440h
PRU_ICSSG1_PR1_MDIO_V1P7_MDI O	0B13 2440h

Figure 15-395. MDIO_USER_ADDR0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																USER_ADDR0															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1204. MDIO_USER_ADDR0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	USER_ADDR0	R/W	0h	User Address 0. In clause 45 mode, this field value is the address transferred in the address transfer initiated before each MDIO_USER_ACCESS_REG_0 access. This is not used for PHY's operating in clause22 mode as there is no address transfer preceding each MDIO_USER_ACCESS_REG_0 access.

Table 15-1205. Register Call Summary for MDIO_USER_ADDR0_REG

PRU_MDIO_MDIO Registers
PRU_MDIO_MDIO Registers: [0] MDIO_USER_ADDR0_REG Register (Offset = 40h) [reset = X]: [0]
PRU_ICSSG MII MDIO Functional Description
MDIO Clause 45 Frame Formats: [0] [1]
PRU_ICSSG MII MDIO Module
PRU_ICSSG MII MDIO Receive/Transmit Frame Host Software Interface: [0]

15.10.18 MDIO_USER_ADDR1_REG Register (Offset = 44h) [reset = X]

MDIO_USER_ADDR1_REG is shown in [Figure 15-396](#) and described in [Table 15-1207](#).

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MDIO User Address 1 Register.

Table 15-1206. MDIO_USER_ADDR1_REG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDI O	0B03 2444h
PRU_ICSSG1_PR1_MDIO_V1P7_MDI O	0B13 2444h

Figure 15-396. MDIO_USER_ADDR1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																USER_ADDR1															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1207. MDIO_USER_ADDR1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	USER_ADDR1	R/W	0h	User Address 1. In clause 45 mode, this field value is the address transferred in the address transfer initiated before each MDIO_USER_ACCESS_REG_1 access. This is not used for PHY's operating in clause22 mode as there is no address transfer preceding each MDIO_USER_ACCESS_REG_1 access.

Table 15-1208. Register Call Summary for MDIO_USER_ADDR1_REG

PRU_MDIO_MDIO Registers
PRU_MDIO_MDIO Registers: [0] MDIO_USER_ADDR1_REG Register (Offset = 44h) [reset = X]: [0]
PRU_ICSSG MII MDIO Functional Description
MDIO Clause 45 Frame Formats: [0] [1]
PRU_ICSSG MII MDIO Module
PRU_ICSSG MII MDIO Receive/Transmit Frame Host Software Interface: [0]

15.10.19 MDIO_USER_ACCESS_REG_j Register (Offset = 80h) [reset = X]

MDIO_USER_ACCESS_REG_j is shown in [Figure 15-397](#) and described in [Table 15-1210](#).

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MDIO User Access j Register.

**Table 15-1209. MDIO_USER_ACCESS_REG_j
Instances**

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDIO O	0B03 2480h
PRU_ICSSG1_PR1_MDIO_V1P7_MDIO O	0B13 2480h

Figure 15-397. MDIO_USER_ACCESS_REG_j Register

31	30	29	28	27	26	25	24
GO	WRITE	ACK	RESERVED			REGADR	
R/W1S-0h	R/W-0h	R/W-0h	R/W-X			R/W-0h	
23	22	21	20	19	18	17	16
REGADR			PHYADR				
R/W-0h			R/W-0h				
15	14	13	12	11	10	9	8
DATA							
R/W-0h							
7	6	5	4	3	2	1	0
DATA							
R/W-0h							

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 15-1210. MDIO_USER_ACCESS_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GO	R/W1S	0h	Go. Writing a 1h to this bit causes the MDIO state machine to perform an MDIO access when it is convenient for it to do so, this is not an instantaneous process. writing a 0h to this bit has no effect. This bit is write able only if the MDIO state machine is enabled. This bit will self clear when the requested access has been completed. Any writes to the MDIO_USER_ACCESS_REG_0 register are blocked when the go bit is 1h. If byte access is being used, the go bit should be written last.
30	WRITE	R/W	0h	Write enable. Setting this bit to a 1 causes the MDIO transaction to be a register write, otherwise it is a register read.
29	ACK	R/W	0h	Acknowledge. This bit is set if the PHY acknowledged the read transaction.
28-26	RESERVED	R/W	X	
25-21	REGADR	R/W	0h	Register address. This field specifies the PHY register to be accessed for this transaction in clause 22 mode or the MMD value in clause 45 mode.
20-16	PHYADR	R/W	0h	PHY address. This field specifies the PHY to be accessed for this transaction.

Table 15-1210. MDIO_USER_ACCESS_REG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-0	DATA	R/W	0h	User data. The data value read from or to be written to the specified PHY register.

Table 15-1211. Register Call Summary for MDIO_USER_ACCESS_REG_j

PRU_MDIO_MDIO Registers PRU_MDIO_MDIO Registers: [0] MDIO_USER_INT_RAW_REG Register (Offset = 20h) [reset = X]: [0] MDIO_USER_INT_MASK_SET_REG Register (Offset = 28h) [reset = X]: [0] [1] MDIO_USER_INT_MASK_CLEAR_REG Register (Offset = 2Ch) [reset = X]: [0] MDIO_USER_INT_MASKED_REG Register (Offset = 24h) [reset = X]: [0] MDIO_USER_ACCESS_REG_j Register (Offset = 80h) [reset = X]: [0]
PRU_ICSSG MII MDIO Functional Description Normal Mode ([30]STATECHANGEMODE = 0h): [0]
PRU_ICSSG MII MDIO Module PRU_ICSSG MII MDIO Receive/Transmit Frame Host Software Interface: [0] [1] [2] [3] [4] [5] [6]

15.10.20 MDIO_USER_PHY_SEL_REG_j Register (Offset = 84h) [reset = X]

MDIO_USER_PHY_SEL_REG_j is shown in Figure 15-398 and described in Table 15-1213.

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MDIO User PHY Select j Register.

**Table 15-1212. MDIO_USER_PHY_SEL_REG_j
Instances**

Instance	Physical Address
PRU_ICSSG0_PR1_MDIO_V1P7_MDIO	0B03 2484h
PRU_ICSSG1_PR1_MDIO_V1P7_MDIO	0B13 2484h

Figure 15-398. MDIO_USER_PHY_SEL_REG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
LINKSEL	LINKINT_ENABLE	RESERVED	PHYADR_MON				
R/W-0h	R/W-0h	R/W-X	R/W-0h				

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1213. MDIO_USER_PHY_SEL_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7	LINKSEL	R/W	0h	Link status determination select. Set to 1h to determine link status using the MLINK pin. Default value is 0h which implies that the link status is determined by the MDIO state machine.
6	LINKINT_ENABLE	R/W	0h	Link change interrupt enable. Set to 1h to enable link change status interrupts for PHY address specified in PHYADR_MON. Link change interrupts are disabled if this bit is set to 0h.
5	RESERVED	R/W	X	
4-0	PHYADR_MON	R/W	0h	PHY address whose link status is to be monitored.

Table 15-1214. Register Call Summary for MDIO_USER_PHY_SEL_REG_j

PRU_MDIO_MDIO Registers - PRU_MDIO_MDIO Registers: [0] - MDIO_LINK_INT_MASKED_REG Register (Offset = 14h) [reset = X]: [0] - MDIO_USER_PHY_SEL_REG_j Register (Offset = 84h) [reset = X]: [0] - MDIO_LINK_REG Register (Offset = Ch) [reset = 0h]: [0] [1] - MDIO_LINK_INT_RAW_REG Register (Offset = 10h) [reset = X]: [0] - MDIO_LINK_INT_MASK_SET_REG Register (Offset = 18h) [reset = X]: [0] - MDIO_LINK_INT_MASK_CLEAR_REG Register (Offset = 1Ch) [reset = X]: [0]
PRU_ICSSG MII MDIO Functional Description - State Change Mode ([30]STATECHANGEMODE = 1h): [0] - Normal Mode ([30]STATECHANGEMODE = 0h): [0]
PRU_ICSSG MII MDIO Module PRU_ICSSG MII MDIO Receive/Transmit Frame Host Software Interface: [0] [1] [2]

15.11 PRU_MII_RT_MII_RT Registers

Table 15-1216 lists the memory-mapped registers for the PRU_MII_RT_MII_RT registers. All register offset addresses not listed in Table 15-1216 should be considered as reserved locations and the register contents should not be modified.

Table 15-1215. PRU_MII_RT_MII_RT Instances

Instance	Base Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	0B03 2000h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	0B13 2000h

Table 15-1216. PRU_MII_RT_MII_RT Registers

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG Physical Address	PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG Physical Address
0h	MII_RT_RXCFG0	RX Configuration 0 Register	0B03 2000h	0B13 2000h
4h	MII_RT_RXCFG1	RX Configuration 1 Register	0B03 2004h	0B13 2004h
10h	MII_RT_TXCFG0	TX Control Register 0	0B03 2010h	0B13 2010h
14h	MII_RT_TXCFG1	TX Control Register 1	0B03 2014h	0B13 2014h
20h	MII_RT_TX_CRC0	Transmit CRC32 Register 0	0B03 2020h	0B13 2020h
24h	MII_RT_TX_CRC1	Transmit CRC32 Register 1	0B03 2024h	0B13 2024h
30h	MII_RT_TX_IPG0	TX IPG Register 0	0B03 2030h	0B13 2030h
34h	MII_RT_TX_IPG1	TX IPG Register 1	0B03 2034h	0B13 2034h
38h	MII_RT_PRS0	PORT_RAW_STATUS Register 0	0B03 2038h	0B13 2038h
3Ch	MII_RT_PRS1	PORT_RAW_STATUS Register 1	0B03 203Ch	0B13 203Ch
40h	MII_RT_RX_FRMS0	RX Frame Size Register 0	0B03 2040h	0B13 2040h
44h	MII_RT_RX_FRMS1	RX Frame Size Register 1	0B03 2044h	0B13 2044h
48h	MII_RT_RX_PCNT0	RX Preamble Cnt Register 0	0B03 2048h	0B13 2048h
4Ch	MII_RT_RX_PCNT1	RX Preamble Cnt Register 1	0B03 204Ch	0B13 204Ch
50h	MII_RT_RX_ERR0	RX Error Register 0	0B03 2050h	0B13 2050h
54h	MII_RT_RX_ERR1	RX Error Register 1	0B03 2054h	0B13 2054h
60h	MII_RT_RX_FIFO_LEVEL0	RX FIFO Level 0 Register	0B03 2060h	0B13 2060h
64h	MII_RT_RX_FIFO_LEVEL1	RX FIFO Level 1 Register	0B03 2064h	0B13 2064h
68h	MII_RT_TX_FIFO_LEVEL0	TX FIFO Register 0	0B03 2068h	0B13 2068h
6Ch	MII_RT_TX_FIFO_LEVEL1	TX FIFO Register 1	0B03 206Ch	0B13 206Ch

15.11.1 MII_RT_RXCFG0 Register (Offset = 0h) [reset = X]

MIIRT_RXCFG0 is shown in [Figure 15-399](#) and described in [Table 15-1218](#).

Return to [Summary Table](#).

RX Configuration 0 Register. This register contains the configuration variables for the RX path. MIIRT_RXCFG0 is attached to PRU0 core and controls which RX port is attached to PRU0.

Table 15-1217. MIIRT_RXCFG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	0B03 2000h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	0B13 2000h

Figure 15-399. MIIRT_RXCFG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED						RX_EOF_SCLR_DIS0	RX_ERR_RAW0
R-0h						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RX_SFD_RAW0	RX_AUTO_FWD_PRE0	RX_BYTE_SWAP0	RX_L2_EN0	RX_MUX_SEL0	RX_CUT_PRE_AMBLE0	RX_DATA_RDY_MODE_DIS0	RX_ENABLED0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1218. MIIRT_RXCFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	
9	RX_EOF_SCLR_DIS0	R/W	0h	0h = RX_EOF flag in R31 and RXL2 is selfcleared by HW when RX2L is enabled 1h = RX_EOF flag in R31 and RXL2 is not selfcleared by HW when RX2L is enabled. A RX_EOF_CLR must get issued
8	RX_ERR_RAW0	R/W	0h	0h = ERR Raw Mode Disabled RX_ERR qualified with RX_DV RX_DV must be 1 before RX_ERR action/event is generated 1h = ERR Raw Mode Enabled RX_ERR is not qualified with RX_DV RX_ERR action/event is generated , even if RX_DV = 0
7	RX_SFD_RAW0	R/W	0h	0h = SFD Raw Mode Disabled RX_SFD requires a pattern of 5D 1h = SFD Raw Mode Enable The first byte of any pattern after RX_DV assertion will trigger RX_SFD event. The first nibble of the frame(RX_DV = 1) will be in the RX FIFO

Table 15-1218. MII_RT_RXCFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	RX_AUTO_FWD_PRE0	R/W	0h	Auto Forward Preamble Mode 0h = Disable 1h = Enable If Enabled, RX_CUT_PREAMBLE and TX_AUTO_PREAMBLE must be disabled This will forward the preamble nibbles including the SFD to the TX FIFO that is attached to the PRU. First data byte seen by PRU R31 and/or RX L2 is DA Note: Odd number of preamble nibbles is supported in this mode. For example, 0x55D Note that new RX should only occur after the current TX completes
5	RX_BYTE_SWAP0	R/W	0h	Controls the order of the Byte0/1 placement for RX R31 and RX L2. 0h = Byte1 is the high byte for R31 and RX L2 MSB {Byte1:Byte0} LSB RX R31 15:8 = Byte1 RX R31 7:0 = Byte0 1h = Byte1 is the low byte for R31 and RX L2 MSB {Byte0:Byte1} LSB RX R31 15:8 = Byte0 RX R31 7:0 = Byte1 Must be selected /updated when the port is disabled or no traffic It only effects R31 and RX L2 order Note this cannot get enabled if TX_AUTO_SEQUENCE enabled since TX_BYTE_SWAP on swaps the PRU output.
4	RX_L2_EN0	R/W	0h	0h = Disables RX L2 buffer. Can be used as generic scratch pad. 1h = Enables RX L2 buffer
3	RX_MUX_SEL0	R/W	0h	0h = Select MII RX Data from Port 0 1h = Select MII RX Data from Port 1 The encoding is identical for both MII Ports and PRUs. Typically, the setting for this will not be identical for the two MII Receive Configuration registers.
2	RX_CUT_PREAMBLE0	R/W	0h	0h = All data from Ethernet PHY are passed on to PRU register. This assume Ethernet PHY which does not shorten the preamble 1h = MII interface suppresses preamble and sync frame delimiter. First data byte seen by PRU register is DA
1	RX_DATA_RDY_MODE_DIS0	R/W	0h	0h = R31:16 is DATA_RDY mapped 1h = R31:16 is TX_EOF mapped
0	RX_ENABLE0	R/W	0h	This enables RX traffic which is currently selected by RX_MUX_SELECT

Table 15-1219. Register Call Summary for MII_RT_RXCFG0

PRU_MII_RT_MII_RT Registers

- [MII_RT_RXCFG0 Register \(Offset = 0h\) \[reset = X\]: \[0\] \[1\]](#)

Table 15-1219. Register Call Summary for MII_RT_RXCFG0 (continued)

PRU_ICSSG MII_G_RT Module

- [PRU and MII Port Multiplexer: \[0\]](#)
- [Nibble and Byte Order: \[0\] \[1\] \[2\]](#)
- [RX L2 Scratch Pad: \[0\]](#)
- [RX MII Receive Data Latch: \[0\]](#)
- [RX MII Port → RX L1 FIFO → RX L2 Buffer → PRU: \[0\]](#)
- [TX Data Path Options to TX L1 FIFO: \[0\] \[1\]](#)

15.11.2 MII_RT_RXCFG1 Register (Offset = 4h) [reset = X]

MIIRT_RXCFG1 is shown in [Figure 15-400](#) and described in [Table 15-1221](#).

Return to [Summary Table](#).

RX Configuration 1 Register. This register contains the configuration variables for the RX path. MII_RT_RXCFG1 is attached to PRU1 core and controls which RX port is attached to PRU1.

Table 15-1220. MII_RT_RXCFG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	0B03 2004h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	0B13 2004h

Figure 15-400. MII_RT_RXCFG1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED						RX_EOF_SCLR_DIS1	RX_ERR_RAW1
R-0h						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RX_SFD_RAW1	RX_AUTO_FW_D_PRE1	RX_BYTE_SW_AP1	RX_L2_EN1	RX_MUX_SEL1	RX_CUT_PRE_AMBLE1	RX_DATA_RDY_MODE_DIS1	RX_ENABLE1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1221. MII_RT_RXCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	
9	RX_EOF_SCLR_DIS1	R/W	0h	0h = RX_EOF flag in R31 and RXL2 is self cleared by HW when RX2L is enabled 1h = RX_EOF flag in R31 and RXL2 is not self cleared by HW when RX2L is enabled. A RX_EOF_CLR must get issued
8	RX_ERR_RAW1	R/W	0h	0h = ERR Raw Mode Disabled RX_ERR qualified with RX_DV RX_DV must be 1 before RX_ERR action/event is generated 1h = ERR Raw Mode Enabled RX_ERR is not qualified with RX_DV RX_ERR action/event is generated , even if RX_DV = 0
7	RX_SFD_RAW1	R/W	0h	0h = SFD Raw Mode Disabled RX_SFD requires a pattern of 5D 1h = SFD Raw Mode Enable The first byte of any pattern after RX_DV assertion will trigger RX_SFD event. The first nibble of the frame(RX_DV = 1) will be in the RX FIFO

Table 15-1221. MII_RT_RXCFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	RX_AUTO_FWD_PRE1	R/W	0h	Auto Forward Preamble Mode 0h = Disable 1h = Enable If Enabled, RX_CUT_PREAMBLE and TX_AUTO_PREAMBLE must be disabled This will forward the preamble nibbles including the SFD to the TX FIFO that is attached to the PRU. First data byte seen by PRU R31 and/or RX L2 is DA Note: Odd number of preamble nibbles is supported in this mode. For example, 0x55D Note that new RX should only occur after the current TX completes
5	RX_BYTE_SWAP1	R/W	0h	Controls the order of the Byte0/1 placement for RX R31 and RX L2. 0h = Byte1 is the high byte for R31 and RX L2 MSB {Byte1:Byte0} LSB RX R31 15:8 = Byte1 RX R31 7:0 = Byte0 1h = Byte1 is the low byte for R31 and RX L2 MSB {Byte0:Byte1} LSB RX R31 15:8 = Byte0 RX R31 7:0 = Byte1 Must be selected /updated when the port is disabled or no traffic It only effects R31 and RX L2 order Note this cannot get enabled if TX_AUTO_SEQUENCE enabled since TX_BYTE_SWAP on swaps the PRU output.
4	RX_L2_EN1	R/W	0h	0h = Disables RX L2 buffer. Can be used as generic scratch pad. 1h = Enables RX L2 buffer
3	RX_MUX_SEL1	R/W	1h	0h = Select MII RX Data from Port 0 1h = Select MII RX Data from Port 1 The encoding is identical for both MII Ports and PRUs. Typically, the setting for this will not be identical for the two MII Receive Configuration registers.
2	RX_CUT_PREAMBLE1	R/W	0h	0h = All data from Ethernet PHY are passed on to PRU register. This assume Ethernet PHY which does not shorten the preamble 1h = MII interface suppresses preamble and sync frame delimiter. First data byte seen by PRU register is DA
1	RX_DATA_RDY_MODE_DIS1	R/W	0h	0h = R31:16 is DATA_RDY mapped 1h = R31:16 is TX_EOF mapped
0	RX_ENABLE1	R/W	0h	This enables RX traffic which is currently selected by RX_MUX_SELECT

Table 15-1222. Register Call Summary for MII_RT_RXCFG1

PRU_MII_RT_MII_RT Registers

- [MII_RT_RXCFG1 Register \(Offset = 4h\) \[reset = X\]: \[0\] \[1\]](#)

PRU_ICSSG MII_G_RT Module

- [RX MII Port → RX L1 FIFO → RX L2 Buffer → PRU: \[0\]](#)
- [RX MII Receive Data Latch: \[0\]](#)

15.11.3 MII_RT_TXCFG0 Register (Offset = 10h) [reset = X]

MIIRT_TXCFG0 is shown in Figure 15-401 and described in Table 15-1224.

Return to [Summary Table](#).

TX Control Register 0. This register contains the control information for the transmit path on one of the MII interfaces. MIIRT_TXCFG0 is attached to Port TX0 and controls which PRU core is selected for TX0.

Table 15-1223. MIIRT_TXCFG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	0B03 2010h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	0B13 2010h

Figure 15-401. MIIRT_TXCFG0 Register

31	30	29	28	27	26	25	24
RESERVED	TX_CLK_DELAY0			RESERVED	TX_START_DELAY0		
R-0h	R/W-0h			R-0h	R/W-40h		
23	22	21	20	19	18	17	16
TX_START_DELAY0							
R/W-40h							
15	14	13	12	11	10	9	8
RESERVED			TX_IPG_WIR E_CLK_EN	TX_32_MODE_EN0	PRE_TX_AUT O_ESC_ERR0	PRE_TX_AUT O_SEQUENC E0	TX_MUX_SEL 0
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h
7	6	5	4	3	2	1	0
RESERVED			TX_BYTE_SWAP0	TX_EN_MOD E0	TX_AUTO_PR EAMBLE0	TX_ENABLE0	
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1224. MIIRT_TXCFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	
30-28	TX_CLK_DELAY0	R/W	0h	Number of MII_RT clock cycles to wait before launching data on the MII interface. This can be tweaked to meet setup/hold time requirements on the MII TXCLK. The range is one to seven cycles after the MII Transmit edge has been synchronized to MII_RT clock domain. For example TX_CLK_DELAY Delay (ns) 0h = (10-15) + SoC delay 1h = (15-20) + SoC delay <n> (<n>*5 + 10/+15) + SoC delay Note that the switch event can get pushed into the next TXCLK cycle.
27-26	RESERVED	R	0h	

Table 15-1224. MII_RT_TXCFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25-16	TX_START_DELAY0	R/W	40h	The time interval after which transmit interface starts sending data to MII interface after receiving RXDV for the current frame. This is programmed in number of MII_RT clock cycles. Default should be to have 320ns of delay which is optimized for min latency at 16 bit processing. Counter is started with RXDV signal going active. Transmit interface stops sending data when no more data is written into transmit interface by PRU along with TX_EOF marker bit set. Uses core_clk Note: it will not start until the TX FIFO is not empty. This delay only defines the minimum delay. If the TX FIFO has data when the delay expires, then TX will start sending data. If the TX FIFO is empty, it will not start until it is not empty. If TX_AUTO_PREAMBLE is enabled, TX FIFO will not get preamble until the first wrt occurs. Note: the TX FIFO size is 64Bytes. It is possible to overflow the TX FIFO with the max delay setting when auto forwarding is enabled since the time delay is larger than the amount of data it needs to store. If TX_OVERFLOW occurs, then SW will need to issue a TX_RESET to reset the TX FIFO. The total delay is 64Byte times, but you need to allow delays for synchronization. Due to this fact, a MAX delay should be 80ns less when auto forwarding is enabled. 0x3F0 is the max in this configuration
15-13	RESERVED	R	0h	
12	TX_IPG_WIRE_CLK_EN	R/W	0h	0h = Use ICSSGn_CORE_CLK (where n = 0 to 1) core clock for the TX_IPG counter 1h = Use the TX interface clock for the TX_IPG counter Note: Using TX interface clock the user should see zero jitter as long as the data is ready to transmit. MUST BE SET THE SAME FOR BOTH PORTS
11	TX_32_MODE_EN0	R/W	0h	0h = Disable 32-bit Data Push mode 1h = Enabled 32-bit, 16-bit, and 8-bit Data Push mode with TX_MASK disabled In this mode, the internal PRU R30 byte write strobes are used and NOT the R31 CMD TX_PUSH Any update to R30 will trigger an TX PUSH See TX_PUSH Table
10	PRE_TX_AUTO_ESC_ER0	R/W	0h	This bit enables the HW actions required to implement the ESC Error handling table.
9	PRE_TX_AUTO_SEQUEN0	R/W	0h	When set to one, it enables automated sequencing of transmit state machine based on events on receiver path that is connected to the respective transmitter. The transmit data source is determined by TX_MUX_SEL setting. When this bit is set, the masking logic that allows for a Boolean combination of PRU or MII data to be transmitted is disabled and only the MII data is used.

Table 15-1224. MII_RT_TXCFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	TX_MUX_SELO	R/W	1h	0h = TX data from PRU0 is selected 1h = TX data from PRU1 is selected The default/reset setting for TX Port 0 is 1h. This setting permits MII TX Port 0 to receive data from PRU1 and the MII RX Port 1 which is connected to PRU1 by default. For MII TX Port 1, the default is zero which allows it to receive data from PRU0 and MII0 that is connected to PRU0 by default.
7-4	RESERVED	R	0h	
3	TX_BYTE_SWAP0	R/W	0h	Controls the order of the Byte0/1 placement for TX R30. 0h = Byte1 is the high byte for R30 MSB {Byte1:Byte0} LSB TX R30 15:8 = Byte1 TX R30 7:0 = Byte0 TX R30 31:24 = TX_MASK[15:8] TX R30 23:16 = TX_MASK[7:0] 1h = Byte1 is the low byte for R30 MSB {Byte0:Byte1} LSB TX R30 15:8 = Byte0 TX R30 7:0 = Byte1 TX R30 31:24 = TX_MASK[7:0] TX R30 23:16 = TX_MASK[15:8] Must be selected/updated when the port is disabled or no traffic It only effects R30 pulling order
2	TX_EN_MODE0	R/W	0h	0h = Disables TX_ENABLE self clear for a TX_EOF event iep_cmp[3] for TX0 and iep_cmp[4] for TX1 1h = Enables TX_ENABLE self clr for a TX_EOF event iep_cmp[3] for TX0 and iep_cmp[4] for TX1 Note when enabled, iep_cmp[3] must be set before the TX will start for TX0, and iep_cmp[4] for TX1 This is just a new dependency to start transmission to the current set of dependencies, which are FIFO NOT empty and TX_START_DELAY met.
1	TX_AUTO_PREAMBLE0	R/W	0h	0h = PRU will provide full pre-amble 1h = TX FIFO will insert pre-amble automatically Note that the TX FIFO does not get preloaded with the preamble until the first write occurs. This can cause the latency to be larger the min latency.
0	TX_ENABLE0	R/W	0h	0h = TX PORT is disabled/stopped immediately 1h = TX PORT is enabled and the frame will start once the IPG counter expired and TX Start Delay counter has expired When read value is zero, TX is disabled When read value is one, TX is enabled If TX_EN_MODE is set then TX_ENABLE will self clear during a TX_EOF event Note: SW can use this to pre-fill the TX FIFO and then start the TX Frame during none ECS operations.

Table 15-1225. Register Call Summary for MII_RT_TXCFG0

PRU_ICSSG IEP

- [Industrial Ethernet Mapping: \[0\] \[1\]](#)

Table 15-1225. Register Call Summary for MII_RT_TXCFG0 (continued)

PRU_MII_RT_MII_RT Registers • MII_RT_TX_IPG0 Register (Offset = 30h) [reset = X]: [0] • MII_RT_TX_IPG1 Register (Offset = 34h) [reset = X]: [0] • MII_RT_TXCFG1 Register (Offset = 14h) [reset = X]: [0]
PRU_ICSSG MII_G_RT Module • PRU R31 Command Interface: [0] [1] • PRU and MII Port Multiplexer: [0] • PRU_ICSSG MII_G_RT Introduction: [0] • Nibble and Byte Order: [0] [1] [2] [3] [4] [5] [6] • TX Data Path Options to TX L1 FIFO: [0] [8] [9]

15.11.4 MII_RT_TXCFG1 Register (Offset = 14h) [reset = X]

MIIRT_TXCFG1 is shown in [Figure 15-402](#) and described in [Table 15-1227](#).

Return to [Summary Table](#).

TX Control Register 1. This register contains the control information for the transmit path on one of the MII interfaces. MIIRT_TXCFG1 is attached to Port TX1 and controls which PRU core is selected for TX1.

Table 15-1226. MIIRT_TXCFG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MIIRT_PR1_MIIRT_CFG	0B03 2014h
PRU_ICSSG1_PR1_MIIRT_PR1_MIIRT_CFG	0B13 2014h

Figure 15-402. MIIRT_TXCFG1 Register

31	30	29	28	27	26	25	24
RESERVED	TX_CLK_DELAY1			RESERVED	TX_START_DELAY1		
R-0h	R/W-0h			R-0h	R/W-40h		
23	22	21	20	19	18	17	16
TX_START_DELAY1							
R/W-40h							
15	14	13	12	11	10	9	8
RESERVED			TX_IPG_WIRE_CLK_EN	TX_32_MODE_EN1	PRE_TX_AUTO_ESC_ERR1	PRE_TX_AUTO_SEQUENCE1	TX_MUX_SEL1
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED			TX_BYTE_SWA_P1	TX_EN_MODE_1	TX_AUTO_PRE_AMBLE1	TX_ENABLE1	
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1227. MIIRT_TXCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	
30-28	TX_CLK_DELAY1	R/W	0h	Number of MIIRT clock cycles to wait before launching data on the MII interface. This can be tweaked to meet setup/hold time requirements on the MII TXCLK. The range is one to seven cycles after the MII Transmit edge has been synchronized to MIIRT clock domain. For example TX_CLK_DELAY Delay (ns) 0h = (10-15) + SOC delay 1h = (15-20) + SOC delay <n> (<n>*5 +10/+15) + SOC delay Note that the switch event can get pushed into the next TXCLK cycle. Note: In order to guarantee the MIIRT_G_RT I/O timing values published in the device data sheet, the PRU_ICSSG ICSSGn_CORE_CLK (where n = 0 to 2) core clock must be configured for 200 MHz, 225 MHz or 250 MHz and the TX_CLK_DELAY0 bit field in the MIIRT_TXCFG0 register must be set to 0h (default value).
27-26	RESERVED	R	0h	

Table 15-1227. MII_RT_TXCFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25-16	TX_START_DELAY1	R/W	40h	The time interval after which transmit interface starts sending data to MII interface after receiving RXDV for the current frame. This is programmed in number of MII_RT clock cycles. Default should be to have 320 ns of delay which is optimized for min latency at 16 bit processing. Counter is started with RXDV signal going active. Transmit interface stops sending data when no more data is written into transmit interface by PRU along with TX_EOF marker bit set. Uses core_clk Note it will not start until the TX FIFO is not empty. This delay only defines the minimum delay. If the TX FIFO has data when the delay expires, then TX will start sending data. If the TX FIFO is empty, it will not start until it is not empty. If TX_AUTO_PREAMBLE is enabled, TX FIFO will not get preamble until the first wrt occurs. Note the TX FIFO size is 64 Bytes. It is possible to overflow the TX FIFO with the max delay setting when auto forwarding is enabled since the time delay is larger than the amount of data it needs to store. If TX OVERFLOW occurs, then SW will need to issue a TX_RESET to reset the TX FIFO. The total delay is 64 Byte times, but you need to allow delays for synchronization. Do to this fact; a MAX delay should be 80 ns less when auto forwarding is enabled. 0x3F0 is the max in this configuration
15-13	RESERVED	R	0h	
12	TX_IPG_WIRE_CLK_EN	R/W	0h	0h = Use ICSSGn_CORE_CLK (where n = 0 to 1) core clock for the TX_IPG counter 1h = Use the TX interface clock for the TX_IPG counter Note: Using TX interface clock the user should see zero jitter as long as the data is ready to transmit. MUST BE SET THE SAME FOR BOTH PORTS
11	TX_32_MODE_EN1	R/W	0h	0h = Disable 32-bit Data Push mode 1h = Enabled 32-bit, 16-bit, and 8 Data Push mode with TX_MASK disabled In this mode, the internal PRU R30 byte write strobes are used and NOT the R31 CMD TX_PUSH Any update to R30 will trigger an TX PUSH See TX_PUSH Table
10	PRE_TX_AUTO_ESC_ER1	R/W	0h	This bit enables the HW actions required to implement the ESC Error handling table.
9	PRE_TX_AUTO_SEQUEN1	R/W	0h	When set to one, it enables automated sequencing of transmit state machine based on events on receiver path that is connected to the respective transmitter. The transmit data source is determined by TX_MUX_SEL setting. When this bit is set, the masking logic that allows for a Boolean combination of PRU or MII data to be transmitted is disabled and only the MII data is used.

Table 15-1227. MII_RT_TXCFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	TX_MUX_SEL1	R/W	0h	0h = TX data from PRU0 is selected 1h = TX data from PRU1 is selected The default/reset setting for TX Port 0 is 1. This setting permits MII TX Port 0 to receive data from PRU1 and the MII RX Port 1 which is connected to PRU1 by default. For MII TX Port 1, the default is zero which allows it to receive data from PRU0 and MII0 that is connected to PRU0 by default.
7-4	RESERVED	R	0h	
3	TX_BYTE_SWAP1	R/W	0h	Controls the order of the Byte0/1 placement for TX R30. 0h = Byte1 is the high byte for R30 MSB {Byte1:Byte0} LSB TX R30 15:8 = Byte1 TX R30 7:0 = Byte0 TX R30 31:24 = TX_MASK[15:8] TX R30 23:16 = TX_MASK[7:0] 1h = Byte1 is the low byte for R30 MSB {Byte0:Byte1} LSB TX R30 15:8 = Byte0 TX R30 7:0 = Byte1 TX R30 31:24 = TX_MASK[7:0] TX R30 23:16 = TX_MASK[15:8] Must be selected /updated when the port is disabled or no traffic It only effects R30 pulling order
2	TX_EN_MODE1	R/W	0h	0h = Disables TX_ENABLE self clr for a TX_EOF event iep_cmp[3] for TX0 and iep_cmp[4] for TX1 1h = Enables TX_ENABLE self clr for a TX_EOF event iep_cmp[3] for TX0 and iep_cmp[4] for TX1 Note when enabled, iep_cmp[3] must be set before the TX will start for TX0, and iep_cmp[4] for TX1 This is just a new dependency to start transmission to the current set of dependencies, which are FIFO NOT empty and TX_START_DELAY met.
1	TX_AUTO_PREAMBLE1	R/W	0h	0h = PRU will provide full pre-amble 1h = TX FIFO will insert pre-amble automatically Note that the TX FIFO does not get preloaded with the preamble until the first write occurs. This can cause the latency to be larger the min latency.
0	TX_ENABLE1	R/W	0h	0h = TX PORT is disabled/stopped immediately 1h = TX PORT is enabled and the frame will start once the IPG counter expired and TX Start Delay counter has expired When read value is zero, TX is disabled When read value is one, TX is enabled If TX_EN_MODE is set then TX_ENABLE will self clear during a TX_EOF event Note SW can use this to pre-fill the TX FIFO and then start the TX Frame during none ECS operations.

Table 15-1228. Register Call Summary for MII_RT_TXCFG1

PRU_MII_RT_MII_RT Registers

- [MII_RT_TXCFG1 Register \(Offset = 14h\) \[reset = X\]: \[0\] \[1\]](#)

15.11.5 MII_RT_TX_CRC0 Register (Offset = 20h) [reset = 0h]

MI RT_TX_CRC0 is shown in [Figure 15-403](#) and described in [Table 15-1230](#).

Return to [Summary Table](#).

Transmit CRC32 Register 0. It contains CRC which PRU core can read.

Table 15-1229. MII_RT_TX_CRC0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	0B03 2020h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	0B13 2020h

Figure 15-403. MII_RT_TX_CRC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_CRC0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-1230. MII_RT_TX_CRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TX_CRC0	R	0h	FCS (CRC32) data can be read by PRU core for diagnostics It is only valid after 6 clocks after a TX_CRC_HIGH command is given.

Table 15-1231. Register Call Summary for MII_RT_TX_CRC0

PRU_MII_RT_MII_RT Registers

- [MI RT_TX_CRC0 Register \(Offset = 20h\) \[reset = 0h\]: \[0\]](#)

15.11.6 MII_RT_TX_CRC1 Register (Offset = 24h) [reset = 0h]

MI RT_TX_CRC1 is shown in [Figure 15-404](#) and described in [Table 15-1233](#).

Return to [Summary Table](#).

Transmit CRC32 Register 1. It contains CRC which PRU core can read.

Table 15-1232. MII_RT_TX_CRC1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	0B03 2024h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	0B13 2024h

Figure 15-404. MII_RT_TX_CRC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_CRC1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-1233. MII_RT_TX_CRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TX_CRC1	R	0h	FCS (CRC32) data can be read by PRU for diagnostics It is only valid after 6 clocks after a TX_CRC_HIGH command is given.

Table 15-1234. Register Call Summary for MII_RT_TX_CRC1

PRU_MII_RT_MII_RT Registers

- [MI RT_TX_CRC1 Register \(Offset = 24h\) \[reset = 0h\]: \[0\]](#)

15.11.7 MII_RT_TX_IPG0 Register (Offset = 30h) [reset = X]

MIIRT_TX_IPG0 is shown in [Figure 15-405](#) and described in [Table 15-1236](#).

Return to [Summary Table](#).

TX IPG Register 0.

Table 15-1235. MII_RT_TX_IPG0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	0B03 2030h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	0B13 2030h

Figure 15-405. MII_RT_TX_IPG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						TX_IPG0									
R-0h																						R/W-28h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1236. MII_RT_TX_IPG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	
15-0	TX_IPG0	R/W	28h	Define the minimum Inter Packet Gap. When MIIRT_TXCFG0[12] TX_IPG_WIRE_CLK_EN = 0h. This defines the minimum of ICSSGn_CORE_CLK (4 ns/5 ns) cycles between the de-assertion of TX_EN and the assertion of TX_EN. The start of the TX will get delayed when the incoming packet IPG is less than defined minimum. In general, software should program in increments of 8, 40 ns to insure the extra delays takes effect. When TX_IPG_WIRE_CLK_EN = 1h. This defines the minimum of TX interface clock cycles between the end of a frame and the start of a new frame 0h = 1 TX interface clock 3h = 4 TX interface clocks (96 ns for 1G) <n> = <n> + 1 TX interface clocks expect for in SGMII 100M mode Note: In SGMII 100M mode, it will be <n> = <n> + 5 TX interface clocks When software does an update, it takes 4 SGMII/RGMII/MII TX_CLKs before it goes into effect Min Values: MII >= 10 RGMII/SGMII 1G >= 11 (8 ns period) RGMII 100M >= 8 (40 ns period) SGMII 100M >= 24 (8 ns period) If the user violate, will get a jitter. The root cause most likely is that the data is not ready. TX MII Odd Nibble is NOT supported in this mode.

Table 15-1237. Register Call Summary for MII_RT_TX_IPG0

PRU_MII_RT_MII_RT Registers

- [MIIRT_TX_IPG0 Register \(Offset = 30h\) \[reset = X\]: \[0\]](#)

15.11.8 MII_RT_TX_IPG1 Register (Offset = 34h) [reset = X]

MIIRT_TX_IPG1 is shown in [Figure 15-406](#) and described in [Table 15-1239](#).

Return to [Summary Table](#).

TX IPG Register 1.

Table 15-1238. MII_RT_TX_IPG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	0B03 2034h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	0B13 2034h

Figure 15-406. MII_RT_TX_IPG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_IPG1															
R/W-X																R/W-28h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1239. MII_RT_TX_IPG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_IPG1	R/W	28h	Define the minimum Inter Packet Gap. When MIIRT_TXCFG0[12] TX_IPG_WIRE_CLK_EN = 0h. This defines the minimum of ICSSGn_CORE_CLK (4 ns/5 ns) cycles between the de-assertion of TX_EN and the assertion of TX_EN. The start of the TX will get delayed when the incoming packet IPG is less than defined minimum. In general, software should program in increments of 8, 40 ns to insure the extra delays takes effect. When TX_IPG_WIRE_CLK_EN = 1h. This defines the minimum of TX interface clock cycles between the end of a frame and the start of a new frame 0h = 1 TX interface clock 3h = 4 TX interface clocks (96 ns for 1G) <n> = <n> + 1 TX interface clocks expect for in SGMII 100M mode Note: In SGMII 100M mode, it will be <n> = <n> + 5 TX interface clocks When software does an update, it takes 4 SGMII/RGMII/MII TX_CLKs before it goes into effect Min Values: MII >= 10 RGMII/SGMII 1G >= 11 (8 ns period) RGMII 100M >= 8 (40 ns period) SGMII 100M >= 24 (8 ns period) If the user violate, will get a jitter. The root cause most likely is that the data is not ready. TX MII Odd Nibble is NOT supported in this mode.

Table 15-1240. Register Call Summary for MII_RT_TX_IPG1

PRU_MII_RT_MII_RT Registers

- [MIIRT_TX_IPG1 Register \(Offset = 34h\) \[reset = X\]: \[0\]](#)

15.11.9 MII_RT_PRS0 Register (Offset = 38h) [reset = X]

MIIRT_PRS0 is shown in Figure 15-407 and described in Table 15-1242.

Return to [Summary Table](#).

PORT_RAW_STATUS Register 0.

Table 15-1241. MII_RT_PRS0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	0B03 2038h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	0B13 2038h

Figure 15-407. MII_RT_PRS0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						SYNC_MII0_C RS	SYNC_MII0_C OL
R-0h						R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 15-1242. MII_RT_PRS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	
1	SYNC_MII0_CRS	R	0h	Read the current state of PR1_MII0_CRS
0	SYNC_MII0_COL	R	0h	Read the current state of PR1_MII0_COL

Table 15-1243. Register Call Summary for MII_RT_PRS0

PRU_MII_RT_MII_RT Registers

- [MIIRT_PRS0 Register \(Offset = 38h\) \[reset = X\]: \[0\]](#)

15.11.10 MII_RT_PRS1 Register (Offset = 3Ch) [reset = X]

MIIRTPRS1 is shown in [Figure 15-408](#) and described in [Table 15-1245](#).

Return to [Summary Table](#).

PORT_RAW_STATUS Register 1.

Table 15-1244. MII_RT_PRS1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	0B03 203Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	0B13 203Ch

Figure 15-408. MII_RT_PRS1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						SYNC_MII1_C RS	SYNC_MII1_C OL
R-0h						R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 15-1245. MII_RT_PRS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	
1	SYNC_MII1_CRS	R	0h	Read the current state of PR1_MII1_CRS
0	SYNC_MII1_COL	R	0h	Read the current state of PR1_MII1_COL

Table 15-1246. Register Call Summary for MII_RT_PRS1

PRU_MII_RT_MII_RT Registers

- [MIIRTPRS1 Register \(Offset = 3Ch\) \[reset = X\]: \[0\]](#)

15.11.11 MII_RT_RX_FRMS0 Register (Offset = 40h) [reset = 05F1003Fh]

MIIRT_RX_FRMS0 is shown in [Figure 15-409](#) and described in [Table 15-1248](#).

Return to [Summary Table](#).

RX Frame Size Register 0.

Table 15-1247. MII_RT_RX_FRMS0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	0B03 2040h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	0B13 2040h

Figure 15-409. MII_RT_RX_FRMS0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_MAX_FRM0																RX_MIN_FRM0															
R/W-5F1h																R/W-3Fh															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1248. MII_RT_RX_FRMS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_MAX_FRM0	R/W	5F1h	If the FRAME total byte count is more than defined value, RX_MAX_FRM_ERR will get set. 0h = 1 byte after SFD and including CRC N=N+1 bytes after SFD and including CRC Notes if the incoming frame is truncated at the marker. So, RX CRC and RX ODD NIBBLE will not get asserted. If the PRU is moving the data the TX frame size will be aligned to the size of the push. For example push32, mod 4 bytes example push16, mod 2 bytes so, software should set the RX_MAX_FRM_CNT in this mode to align with the max push size. The event is always byte aligned. The final TX size is aligned to the push size.
15-0	RX_MIN_FRM0	R/W	3Fh	If the FRAME total byte count is less than defined value, RX_MIN_FRM_ERR will get set. 0h = 1 byte after SFD and including CRC N=N+1 bytes after SFD and including CRC Notes: If the PRU is moving the data the TX frame size will be aligned to the size of the push. For example push32, mod 4 bytes example push16, mod 2 bytes so, software should set the RX_MIN_FRM_CNT in this mode to align with the max push size. The event is always byte aligned. The final TX size is aligned to the push size

Table 15-1249. Register Call Summary for MII_RT_RX_FRMS0

PRU_MII_RT_MII_RT Registers

- [MIIRT_RX_FRMS0 Register \(Offset = 40h\) \[reset = 05F1003Fh\]: \[0\]](#)

15.11.12 MII_RT_RX_FRMS1 Register (Offset = 44h) [reset = 05F1003Fh]

MIIRT_RX_FRMS1 is shown in [Figure 15-410](#) and described in [Table 15-1251](#).

Return to [Summary Table](#).

RX Frame Size Register 1.

Table 15-1250. MII_RT_RX_FRMS1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	0B03 2044h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	0B13 2044h

Figure 15-410. MII_RT_RX_FRMS1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_MAX_FRM1																RX_MIN_FRM1															
R/W-5F1h																R/W-3Fh															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1251. MII_RT_RX_FRMS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_MAX_FRM1	R/W	5F1h	If the FRAME total byte count is more than defined value, RX_MAX_FRM_ERR will get set. 0h = 1 byte after SFD and including CRC N=N+1 bytes after SFD and including CRC Notes if the incoming frame is truncated at the marker. So, RX CRC and RX ODD NIBBLE will not get asserted. If the PRU is moving the data the TX frame size will be aligned to the size of the push. For example push32, mod 4 bytes example push16, mod 2 bytes so, software should set the RX_MAX_FRM_CNT in this mode to align with the max push size. The event is always byte aligned. The final TX size is aligned to the push size.
15-0	RX_MIN_FRM1	R/W	3Fh	If the FRAME total byte count is less than defined value, RX_MIN_FRM_ERR will get set. 0h = 1 byte after SFD and including CRC N=N+1 bytes after SFD and including CRC Notes: If the PRU is moving the data the TX frame size will be aligned to the size of the push. For example push32, mod 4 bytes example push16, mod 2 bytes so, software should set the RX_MIN_FRM_CNT in this mode to align with the max push size. The event is always byte aligned. The final TX size is aligned to the push size

Table 15-1252. Register Call Summary for MII_RT_RX_FRMS1

PRU_MII_RT_MII_RT Registers

- [MIIRT_RX_FRMS1 Register \(Offset = 44h\) \[reset = 05F1003Fh\]: \[0\]](#)

15.11.13 MII_RT_RX_PCNT0 Register (Offset = 48h) [reset = X]

MIIRT_RX_PCNT0 is shown in [Figure 15-411](#) and described in [Table 15-1254](#).

Return to [Summary Table](#).

RX Preamble Cnt Register 0.

Table 15-1253. MII_RT_RX_PCNT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	0B03 2048h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	0B13 2048h

Figure 15-411. MII_RT_RX_PCNT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RX_MAX_PCNT0				RX_MIN_PCNT0			
R-0h								R/W-Eh				R/W-1h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1254. MII_RT_RX_PCNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	
8-4	RX_MAX_PCNT0	R/W	Eh	Define the max number of nibbles until first SFD/SMD is matched. RX_MAX_PRE_COUNT_ERR will set if the preamble count more than 0h= Disabled 1h = Reserved 2h = 4th nibble needs to have built 0xD5/SMD Eh= 16th nibble needs to have built 0xD5/SMD if not matched then 16th nibble will cause the error to assert and truncate the incoming frame. Note the 16th nibble is transmitted Any valid IET SMD or 0xD5 If > max then, hardware will issue a SFD and set error flags CRC can/will be bad for this packet
3-0	RX_MIN_PCNT0	R/W	1h	Define the minimum number of nibbles before SFD 0xD5 RX_MIN_PRE_COUNT_ERR will set if the preamble count less than 0h = is Disabled 1h = Minimum of 1 0x5 before 0xD5 2h = Minimum of 2 0x5 before 0xD5 <n> minimum of <n> 0x5 before 0xD5 Note it does not need to be "0x5"

Table 15-1255. Register Call Summary for MII_RT_RX_PCNT0

PRU_MII_RT_MII_RT Registers

- [MIIRT_RX_PCNT0 Register \(Offset = 48h\) \[reset = X\]: \[0\]](#)

15.11.14 MII_RT_RX_PCNT1 Register (Offset = 4Ch) [reset = X]

MIIRT_RX_PCNT1 is shown in [Figure 15-412](#) and described in [Table 15-1257](#).

Return to [Summary Table](#).

RX Preamble Cnt Register 1.

Table 15-1256. MII_RT_RX_PCNT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	0B03 204Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	0B13 204Ch

Figure 15-412. MII_RT_RX_PCNT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RX_MAX_PCNT1				RX_MIN_PCNT1			
R-0h								R/W-Eh				R/W-1h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1257. MII_RT_RX_PCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	
8-4	RX_MAX_PCNT1	R/W	Eh	Define the max number of nibbles until first SFD/SMD is matched. RX_MAX_PRE_COUNT_ERR will set if the preamble count more than 0h = Disabled 1h = Reserved 2h = 4th nibble needs to have built 0xD5/SMD Eh= 16th nibble needs to have built 0xD5/SMD if not matched then 16th nibble will cause the error to assert and truncate the incoming frame. Note the 16th nibble is transmitted Any valid IET SMD or 0xD5 If > max then, hardware will issue a SFD and set error flags CRC can/will be bad for this packet
3-0	RX_MIN_PCNT1	R/W	1h	Define the minimum number of nibbles before SFD 0xD5 RX_MIN_PRE_COUNT_ERR will set if the preamble count less than 0h = is Disabled 1h = Minimum of 1 0x5 before 0xD5 2h = Minimum of 2 0x5 before 0xD5 <n> minimum of <n> 0x5 before 0xD5 Note it does not need to be "0x5"

Table 15-1258. Register Call Summary for MII_RT_RX_PCNT1

PRU_MII_RT_MII_RT Registers

- [MIIRT_RX_PCNT1 Register \(Offset = 4Ch\) \[reset = X\]: \[0\]](#)

15.11.15 MII_RT_RX_ERR0 Register (Offset = 50h) [reset = X]

MIIRT_RX_ERR0 is shown in Figure 15-413 and described in Table 15-1260.

Return to [Summary Table](#).

RX Error Register 0.

Table 15-1259. MII_RT_RX_ERR0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	0B03 2050h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	0B13 2050h

Figure 15-413. MII_RT_RX_ERR0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				RX_MAX_FRM_ERR0	RX_MIN_FRM_ERR0	RX_MAX_PCNT_ERR0	RX_MIN_PCNT_ERR0
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1260. MII_RT_RX_ERR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	
3	RX_MAX_FRM_ERR0	R/W	0h	Set when the FRAME total byte count is more than defined value. Write 1 to Clear
2	RX_MIN_FRM_ERR0	R/W	0h	Set when the FRAME total byte count is less than defined value. Write 1 to Clear
1	RX_MAX_PCNT_ERR0	R/W	0h	Set when of x nibbles before SFD 0xD5 is more than defined value. Write 1 to Clear
0	RX_MIN_PCNT_ERR0	R/W	0h	Set when of 0x5 before SFD 0xD5 is less than defined value. Write 1 to Clear

Table 15-1261. Register Call Summary for MII_RT_RX_ERR0

PRU_MII_RT_MII_RT Registers

- [MIIRT_RX_ERR0 Register \(Offset = 50h\) \[reset = X\]: \[0\]](#)

15.11.16 MII_RT_RX_ERR1 Register (Offset = 54h) [reset = X]

MIIRT_RX_ERR1 is shown in Figure 15-414 and described in Table 15-1263.

Return to [Summary Table](#).

RX Error Register 1.

Table 15-1262. MII_RT_RX_ERR1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	0B03 2054h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	0B13 2054h

Figure 15-414. MII_RT_RX_ERR1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				RX_MAX_FRM_ERR1	RX_MIN_FRM_ERR1	RX_MAX_PCNT_ERR1	RX_MIN_PCNT_ERR1
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1263. MII_RT_RX_ERR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	
3	RX_MAX_FRM_ERR1	R/W	0h	Set when the FRAME total byte count is more than defined value. Write 1 to Clear
2	RX_MIN_FRM_ERR1	R/W	0h	Set when the FRAME total byte count is less than defined value. Write 1 to Clear
1	RX_MAX_PCNT_ERR1	R/W	0h	Set when of x nibbles before SFD 0xD5 is more than defined value. Write 1 to Clear
0	RX_MIN_PCNT_ERR1	R/W	0h	Set when of 0x5 before SFD 0xD5 is less than defined value. Write 1 to Clear

Table 15-1264. Register Call Summary for MII_RT_RX_ERR1

PRU_MII_RT_MII_RT Registers

- [MIIRT_RX_ERR1 Register \(Offset = 54h\) \[reset = X\]: \[0\]](#)

15.11.17 MII_RT_RX_FIFO_LEVEL0 Register (Offset = 60h) [reset = X]

MIIRT_RX_FIFO_LEVEL0 is shown in [Figure 15-415](#) and described in [Table 15-1266](#).

Return to [Summary Table](#).

RX FIFO Level 0 Register.

Table 15-1265. MII_RT_RX_FIFO_LEVEL0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	0B03 2060h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	0B13 2060h

Figure 15-415. MII_RT_RX_FIFO_LEVEL0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RX_FIFO_LEVEL0							
R-0h								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 15-1266. MII_RT_RX_FIFO_LEVEL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	RX_FIFO_LEVEL0	R	0h	Define the number of valid bytes in the RX FIFO. 0h = Empty 1h = 1 Byte/ 2 Nibbles 2h = 2 Byte/ 4 Nibble ... 20h = 32 Bytes/ 64 Nibbles

Table 15-1267. Register Call Summary for MII_RT_RX_FIFO_LEVEL0

PRU_MII_RT_MII_RT Registers
MIIRT_RX_FIFO_LEVEL0 Register (Offset = 60h) [reset = X]: [0]

15.11.18 MII_RT_RX_FIFO_LEVEL1 Register (Offset = 64h) [reset = X]

MIIRT_RX_FIFO_LEVEL1 is shown in [Figure 15-416](#) and described in [Table 15-1269](#).

Return to [Summary Table](#).

RX FIFO Level 1 Register.

Table 15-1268. MII_RT_RX_FIFO_LEVEL1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	0B03 2064h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	0B13 2064h

Figure 15-416. MII_RT_RX_FIFO_LEVEL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RX_FIFO_LEVEL1							
R-0h								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 15-1269. MII_RT_RX_FIFO_LEVEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	RX_FIFO_LEVEL1	R	0h	Define the number of valid bytes in the RX FIFO. 0h = Empty 1h = 1 Byte/ 2 Nibbles 2h = 2 Byte/ 4 Nibble ... 20h = 32 Bytes/ 64 Nibbles

Table 15-1270. Register Call Summary for MII_RT_RX_FIFO_LEVEL1

PRU_MII_RT_MII_RT Registers

- [MIIRT_RX_FIFO_LEVEL1 Register \(Offset = 64h\) \[reset = X\]: \[0\]](#)

15.11.19 MII_RT_TX_FIFO_LEVEL0 Register (Offset = 68h) [reset = X]

MIIRT_TX_FIFO_LEVEL0 is shown in [Figure 15-417](#) and described in [Table 15-1272](#).

Return to [Summary Table](#).

TX FIFO Register 0.

Table 15-1271. MII_RT_TX_FIFO_LEVEL0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	0B03 2068h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	0B13 2068h

Figure 15-417. MII_RT_TX_FIFO_LEVEL0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TX_FIFO_LEVEL0							
R-0h								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 15-1272. MII_RT_TX_FIFO_LEVEL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	TX_FIFO_LEVEL0	R	0h	Define the number of valid nibbles in the TX FIFO. 0 = Empty 1 = 1 Nibble 2 = 1 Byte/ 2 Nibble ... 128 = 64 Bytes/ 128 Nibbles

Table 15-1273. Register Call Summary for MII_RT_TX_FIFO_LEVEL0

PRU_MII_RT_MII_RT Registers
• MIIRT_TX_FIFO_LEVEL0 Register (Offset = 68h) [reset = X]: [0]

15.11.20 MII_RT_TX_FIFO_LEVEL1 Register (Offset = 6Ch) [reset = X]

MI RT_TX_FIFO_LEVEL1 is shown in [Figure 15-418](#) and described in [Table 15-1275](#).

Return to [Summary Table](#).

TX FIFO Register 1.

Table 15-1274. MII_RT_TX_FIFO_LEVEL1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_CFG	0B03 206Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_CFG	0B13 206Ch

Figure 15-418. MII_RT_TX_FIFO_LEVEL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TX_FIFO_LEVEL1							
R-X								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 15-1275. MII_RT_TX_FIFO_LEVEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	TX_FIFO_LEVEL1	R	0h	Define the number of valid nibbles in the TX FIFO. 0 = Empty 1 = 1 Nibble 2 = 1 Byte/ 2 Nibble ... 128 = 64 Bytes/ 128 Nibbles

Table 15-1276. Register Call Summary for MII_RT_TX_FIFO_LEVEL1

PRU_MII_RT_MII_RT Registers

- [MI RT_TX_FIFO_LEVEL1 Register \(Offset = 6Ch\) \[reset = X\]: \[0\]](#)

15.12 PRU_MII_G_RT_MII_G_RT Registers

Table 15-1278 lists the memory-mapped registers for the PRU_MII_G_RT_MII_G_RT registers. All register offset addresses not listed in Table 15-1278 should be considered as reserved locations and the register contents should not be modified.

Table 15-1277. PRU_MII_G_RT_MII_G_RT Instances

Instance	Base Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3000h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3000h

Table 15-1278. PRU_MII_G_RT_MII_G_RT Registers

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G Physical Address	PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G Physical Address
0h	MII_G_RT_ICSS_G_CFG	ICSSG Configuration Register	0B03 3000h	0B13 3000h
4h	MII_G_RT_RGMII_CFG	RGMII Configuration Register	0B03 3004h	0B13 3004h
8h	MII_G_RT_MAC_PRU0_0	PRU0 MAC (DA3:DA0)	0B03 3008h	0B13 3008h
Ch	MII_G_RT_MAC_PRU0_1	PRU0 MAC (DA5:DA4)	0B03 300Ch	0B13 300Ch
10h	MII_G_RT_MAC_PRU1_0	PRU1 MAC (DA3:DA0)	0B03 3010h	0B13 3010h
14h	MII_G_RT_MAC_PRU1_1	PRU0 MAC (DA5:DA4)	0B03 3014h	0B13 3014h
18h	MII_G_RT_MAC_INTERFACE_0	MAC Host Interface (DA3:DA0)	0B03 3018h	0B13 3018h
1Ch	MII_G_RT_MAC_INTERFACE_1	MAC Host Interface (DA5:DA4)	0B03 301Ch	0B13 301Ch
20h	MII_G_RT_PREEMPT_CFG	Preempt Configuration Register	0B03 3020h	0B13 3020h
24h	MII_G_RT_SMDT1S_CFG	SMD Type1S Preemptable Frame Start Configuration	0B03 3024h	0B13 3024h
28h	MII_G_RT_SMDT1C_CFG	SMD Type1C None Initial Frag Configuration	0B03 3028h	0B13 3028h
34h	MII_G_RT_FRAG_CNT_CFG	Frag Count Configuration	0B03 3034h	0B13 3034h
40h	MII_G_RT_PA_STAT_PUSH0	Pa Stat Push0	0B03 3040h	0B13 3040h
44h	MII_G_RT_PA_STAT_PUSH1	Pa Stat Push1	0B03 3044h	0B13 3044h
48h	MII_G_RT_PA_STAT_PUSH2	Pa Stat Push2	0B03 3048h	0B13 3048h
4Ch	MII_G_RT_PA_STAT_PUSH3	Pa Stat Push3	0B03 304Ch	0B13 304Ch
60h	MII_G_RT_FDB_GEN_CFG1	FDB Configuration1	0B03 3060h	0B13 3060h
64h	MII_G_RT_FDB_GEN_CFG2	FDB Configuration2	0B03 3064h	0B13 3064h
6Ch	MII_G_RT_FDB_DF_VLAN	FDB Default PRU VLAN	0B03 306Ch	0B13 306Ch
70h	MII_G_RT_FDB_HOST_DA0	FDB HOST DA3:0 Configuration	0B03 3070h	0B13 3070h
74h	MII_G_RT_FDB_HOST_DA1	FDB HOST DA5:4 Configuration	0B03 3074h	0B13 3074h
78h	MII_G_RT_FDB_HOST_SA0	FDB HOST SA3:0 Configuration	0B03 3078h	0B13 3078h
7Ch	MII_G_RT_FDB_HOST_VLAN_SA1	FDB HOST VLAN SA5:4 Configuration	0B03 307Ch	0B13 307Ch
80h	MII_G_RT_FT1_START_LEN_PRU0	Filter1 Start and Length (PRU0)	0B03 3080h	0B13 3080h
84h	MII_G_RT_FT1_CFG_PRU0	Filter1 Configuration (PRU0)	0B03 3084h	0B13 3084h
88h + formula	MII_G_RT_FT1_k_DA0_PRU0	Filter1<k> DA0 (PRU0)	0B03 3088h + formula	0B13 3088h + formula
8Ch + formula	MII_G_RT_FT1_k_DA1_PRU0	Filter1<k> DA1 (PRU0)	0B03 308Ch + formula	0B13 308Ch + formula
90h + formula	MII_G_RT_FT1_k_DA_MASK0_PRU0	Filter1<k> DA0 Mask (PRU0)	0B03 3090h + formula	0B13 3090h + formula
94h + formula	MII_G_RT_FT1_k_DA_MASK1_PRU0	Filter1<k> DA1 Mask (PRU0)	0B03 3094h + formula	0B13 3094h + formula

Table 15-1278. PRU_MII_G_RT_MII_G_RT Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G Physical Address	PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G Physical Address
108h + formula	MII_G_RT_FT3_m_START_PRU0	Filter3 Byte Count Start for PRU0	0B03 3108h + formula	0B13 3108h + formula
10Ch + formula	MII_G_RT_FT3_m_START_AUTO_P RU0	Filter3 Byte Count Start for Auto Skip mode	0B03 310Ch + formula	0B13 310Ch + formula
110h + formula	MII_G_RT_FT3_m_START_LEN_PR U0	Filter3 Start Offset for PRU0	0B03 3110h + formula	0B13 3110h + formula
114h + formula	MII_G_RT_FT3_m_JMP_OFFSET_P RU0	Filter3 Jump Offset for PRU0for PRU0	0B03 3114h + formula	0B13 3114h + formula
118h + formula	MII_G_RT_FT3_m_LEN_PRU0	Filter3 Length Offset for PRU0	0B03 3118h + formula	0B13 3118h + formula
11Ch + formula	MII_G_RT_FT3_m_CFG_PRU0	Filter3 Configuration for PRU0	0B03 311Ch + formula	0B13 311Ch + formula
120h + formula	MII_G_RT_FT3_m_T_PRU0	Filter3 Type for PRU0	0B03 3120h + formula	0B13 3120h + formula
124h + formula	MII_G_RT_FT3_m_T_MASK_PRU0	Filter3 Mask for PRU0	0B03 3124h + formula	0B13 3124h + formula
308h + formula	MII_G_RT_FT3_m_P0_PRU0	Filter3 PRU0 (P4:P1)	0B03 3308h + formula	0B13 3308h + formula
30Ch + formula	MII_G_RT_FT3_m_P1_PRU0	Filter3 PRU0 (P8:P5)	0B03 330Ch + formula	0B13 330Ch + formula
310h + formula	MII_G_RT_FT3_n_P_MASK0_PRU0	Filter3 Mask0 (MP4:MP1)	0B03 3310h + formula	0B13 3310h + formula
314h + formula	MII_G_RT_FT3_n_P_MASK1_PRU0	Filter3 Mask1 (MP8:MP5)	0B03 3314h + formula	0B13 3314h + formula
408h	MII_G_RT_FT_RX_PTR_PRU0	RX Current Filter Byte Count (PRU0)	0B03 3408h	0B13 3408h
40Ch + formula	MII_G_RT_RX_CLASSm_AND_EN_ PRU0	RX Class AND Enable Register	0B03 340Ch + formula	0B13 340Ch + formula
410h + formula	MII_G_RT_RX_CLASSm_OR_EN_P RU0	RX Class OR Enable Register	0B03 3410h	0B13 3410h
48Ch	MII_G_RT_RX_CLASS_CFG1_PRU 0	RX Class Configuration 1 Register	0B03 348Ch	0B13 348Ch
490h	MII_G_RT_RX_CLASS_CFG2_PRU 0	RX Class Configuration 2 Register	0B03 3490h	0B13 3490h
494h + formula	MII_G_RT_RX_CLASS_GATESm_P RU0	RX Class Gate Configuration PRU0 Register	0B03 3494h + formula	0B13 3494h + formula
4D4h	MII_G_RT_RX_GREEN_PRU0	RX Green Status PRU0	0B03 34D4h	0B13 34D4h
4D8h	MII_G_RT_SA_HASH_PRU0	SA Hash Seed PRU0	0B03 34D8h	0B13 34D8h
4DCh	MII_G_RT_CONN_HASH_PRU0	Connection Hash Seed PRU0	0B03 34DCh	0B13 34DCh
4E0h	MII_G_RT_CONN_HASH_START_P RU0	Connection Hash Start PRU0	0B03 34E0h	0B13 34E0h
4E4h + formula	MII_G_RT_RX_RATE_CFGn_PRU0	RX Rate Configuration Register	0B03 34E4h + formula	0B13 34E4h + formula
504h	MII_G_RT_RX_RATE_SRC_SEL0_P RU0	RX Rate Source Select0	0B03 3504h	0B13 3504h
508h	MII_G_RT_RX_RATE_SRC_SEL1_P RU0	RX Rate Source Select1	0B03 3508h	0B13 3508h
50Ch + formula	MII_G_RT_TX_RATE_CFG1_n_PRU 0	TX Rate Configuration1 Register	0B03 350Ch + formula	0B13 350Ch + formula
510h + formula	MII_G_RT_TX_RATE_CFG2_n_PRU 0	TX Rate Configuration2 Register	0B03 3510h + formula	0B13 3510h + formula
54Ch	MII_G_RT_RX_STAT_GOOD_PRU0	RX Good Frame Count (PRU0)	0B03 354Ch	0B13 354Ch
550h	MII_G_RT_RX_STAT_BC_PRU0	RX BC Frame Count (PRU0)	0B03 3550h	0B13 3550h

Table 15-1278. PRU_MII_G_RT_MII_G_RT Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G Physical Address	PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G Physical Address
554h	MII_G_RT_RX_STAT_MC_PRU0	RX MC Frame Count (PRU0)	0B03 3554h	0B13 3554h
558h	MII_G_RT_RX_STAT_CRC_ERR_PRU0	RX CRC Error Frame Count (PRU0)	0B03 3558h	0B13 3558h
55Ch	MII_G_RT_RX_STAT_MII_ERR_PRU0	RX MII Error Frame Count (PRU0)	0B03 355Ch	0B13 355Ch
560h	MII_G_RT_RX_STAT_ODD_ERR_PRU0	RX Odd Nibble Frame Count (PRU0)	0B03 3560h	0B13 3560h
564h	MII_G_RT_RX_STAT_MAX_SIZE_PRU0	RX Max Size Frame Count (PRU0)	0B03 3564h	0B13 3564h
568h	MII_G_RT_RX_STAT_MAX_ERR_PRU0	RX Max Size Error Frame Count (PRU0)	0B03 3568h	0B13 3568h
56Ch	MII_G_RT_RX_STAT_MIN_SIZE_PRU0	RX Min Size Frame Count (PRU0)	0B03 356Ch	0B13 356Ch
570h	MII_G_RT_RX_STAT_MIN_ERR_PRU0	RX Min Size Error Frame Count (PRU0)	0B03 3570h	0B13 3570h
574h	MII_G_RT_RX_STAT_OVERRUN_ERR_PRU0	RX Overrun Frame Count (PRU0)	0B03 3574h	0B13 3574h
578h + formula	MII_G_RT_RX_STAT_CLASSm_HIT_PRU0	RX Class<m> Hit	0B03 3578h + formula	0B13 3578h + formula
5B8h	MII_G_RT_RX_STAT_SMD_FRAG_ERR_PRU0	RX SMD Frag Error Count (PRU0)	0B03 35B8h	0B13 35B8h
5BCh	MII_G_RT_RX_STAT_BKT1_SIZE_PRU0	RX Bucket1 Size Configuration (PRU0)	0B03 35BCh	0B13 35BCh
5C0h	MII_G_RT_RX_STAT_BKT2_SIZE_PRU0	RX Bucket2 Size Configuration (PRU0)	0B03 35C0h	0B13 35C0h
5C4h	MII_G_RT_RX_STAT_BKT3_SIZE_PRU0	RX Bucket3 Size Configuration (PRU0)	0B03 35C4h	0B13 35C4h
5C8h	MII_G_RT_RX_STAT_BKT4_SIZE_PRU0	RX Bucket4 Size Configuration (PRU0)	0B03 35C8h	0B13 35C8h
5CCh	MII_G_RT_RX_STAT_64_PRU0	RX 64B Sized Frame Count (PRU0)	0B03 35CCh	0B13 35CCh
5D0h	MII_G_RT_RX_STAT_BKT1_PRU0	RX Bucket1 Sized Frame Count (PRU0)	0B03 35D0h	0B13 35D0h
5D4h	MII_G_RT_RX_STAT_BKT2_PRU0	RX Bucket2 Sized Frame Count (PRU0)	0B03 35D4h	0B13 35D4h
5D8h	MII_G_RT_RX_STAT_BKT3_PRU0	RX Bucket3 Sized Frame Count (PRU0)	0B03 35D8h	0B13 35D8h
5DCh	MII_G_RT_RX_STAT_BKT4_PRU0	RX Bucket4 Sized Frame Count (PRU0)	0B03 35DCh	0B13 35DCh
5E0h	MII_G_RT_RX_STAT_BKT5_PRU0	RX Bucket5 Sized Frame Count (PRU0)	0B03 35E0h	0B13 35E0h
5E4h	MII_G_RT_RX_STAT_TOTAL_BYTES_PRU0	RX Total Byte Count (PRU0)	0B03 35E4h	0B13 35E4h
5E8h	MII_G_RT_RXTX_STAT_TOTAL_BYTES_PRU0	RX TX Total Byte Count (PRU0)	0B03 35E8h	0B13 35E8h
5ECh	MII_G_RT_TX_STAT_GOOD_PORT0	TX Good Frame Count Port0	0B03 35ECh	0B13 35ECh
5F0h	MII_G_RT_TX_STAT_BC_PORT0	TX BC Frame Count Port0	0B03 35F0h	0B13 35F0h
5F4h	MII_G_RT_TX_STAT_MC_PORT0	TX MC Frame Count Port0	0B03 35F4h	0B13 35F4h
5F8h	MII_G_RT_TX_STAT_ODD_ERR_PORT0	TX Odd Nibble Frame Count Port0	0B03 35F8h	0B13 35F8h
5FCh	MII_G_RT_TX_STAT_UNDERFLOW_ERR_PORT0	TX Under Flow Error Count Port0	0B03 35FCh	0B13 35FCh

Table 15-1278. PRU_MII_G_RT_MII_G_RT Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G Physical Address	PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G Physical Address
600h	MII_G_RT_TX_STAT_MAX_SIZE_PORT0	TX Max Size Frame Port0	0B03 3600h	0B13 3600h
604h	MII_G_RT_TX_STAT_MAX_ERR_PORT0	TX Max Size Error Frame Count Port0	0B03 3604h	0B13 3604h
608h	MII_G_RT_TX_STAT_MIN_SIZE_PORT0	TX Min Size Frame Port0	0B03 3608h	0B13 3608h
60Ch	MII_G_RT_TX_STAT_MIN_ERR_PORT0	TX Min Size ErrorFrame Count Port0	0B03 360Ch	0B13 360Ch
610h	MII_G_RT_TX_STAT_BKT1_SIZE_PORT0	TX Bucket1 Size Configuration Port0	0B03 3610h	0B13 3610h
614h	MII_G_RT_TX_STAT_BKT2_SIZE_PORT0	TX Bucket2 Size Configuration Port0	0B03 3614h	0B13 3614h
618h	MII_G_RT_TX_STAT_BKT3_SIZE_PORT0	TX Bucket3 Size Configuration Port0	0B03 3618h	0B13 3618h
61Ch	MII_G_RT_TX_STAT_BKT4_SIZE_PORT0	TX Bucket4 Size Configuration Port0	0B03 361Ch	0B13 361Ch
620h	MII_G_RT_TX_STAT_64_PORT0	TX 64B Sized Frame Count Port0	0B03 3620h	0B13 3620h
624h	MII_G_RT_TX_STAT_BKT1_PORT0	TX Bucket1 Sized Frame Count Port0	0B03 3624h	0B13 3624h
628h	MII_G_RT_TX_STAT_BKT2_PORT0	TX Bucket2 Sized Frame Count Port0	0B03 3628h	0B13 3628h
62Ch	MII_G_RT_TX_STAT_BKT3_PORT0	TX Bucket3 Sized Frame Count Port0	0B03 362Ch	0B13 362Ch
630h	MII_G_RT_TX_STAT_BKT4_PORT0	TX Bucket4 Sized Frame Count Port0	0B03 3630h	0B13 3630h
634h	MII_G_RT_TX_STAT_BKT5_PORT0	TX Bucket5 Sized Frame Count Port0	0B03 3634h	0B13 3634h
638h	MII_G_RT_TX_STAT_TOTAL_BYTES_PORT0	TX Total Byte Count Port0	0B03 3638h	0B13 3638h
63Ch	MII_G_RT_TX_HSR_TAG_PORT0	TX HSR TAG Port0	0B03 363Ch	0B13 363Ch
640h	MII_G_RT_TX_HSR_SEQ_PORT0	TX HSR Seq Port0	0B03 3640h	0B13 3640h
644h	MII_G_RT_TX_VLAN_TYPE_TAG_PORT0	TX VLAN Type TAG Port0	0B03 3644h	0B13 3644h
648h	MII_G_RT_TX_VLAN_INS_TAG_PORT0	TX VLAN Insertion TAG Port0	0B03 3648h	0B13 3648h
64Ch	MII_G_RT_FT1_START_LEN_PRU1	Filter1 Start and Length (PRU1)	0B03 364Ch	0B13 364Ch
650h	MII_G_RT_FT1_CFG_PRU1	Filter1 Configuration (PRU1)	0B03 3650h	0B13 3650h
654h + formula	MII_G_RT_FT1_k_DA0_PRU1	Filter1<k> DA0 (PRU1)	0B03 3654h + formula	0B13 3654h + formula
658h + formula	MII_G_RT_FT1_k_DA1_PRU1	Filter1<k> DA1 (PRU1)	0B03 3658h + formula	0B13 3658h + formula
65Ch + formula	MII_G_RT_FT1_k_DA_MASK0_PRU1	Filter1<k> DA0 Mask (PRU1)	0B03 365Ch + formula	0B13 365Ch + formula
660h + formula	MII_G_RT_FT1_k_DA_MASK1_PRU1	Filter1<k> DA1 Mask (PRU1)	0B03 3660h + formula	0B13 3660h + formula
6D4h + formula	MII_G_RT_FT3_m_START_PRU1	Filter3<m> Start (PRU1)	0B03 36D4h + formula	0B13 36D4h + formula
6D8h + formula	MII_G_RT_FT3_m_START_AUTO_PRU1	Filter3<m> Start Auto (PRU1)	0B03 36D8h + formula	0B13 36D8h + formula
6DCh + formula	MII_G_RT_FT3_m_START_LEN_PRU1	Filter3<m> Start offset (PRU1)	0B03 36DCh + formula	0B13 36DCh + formula
6E0h + formula	MII_G_RT_FT3_m_JMP_OFFSET_PRU1	Filter3<m> Jmp offset (PRU1)	0B03 36E0h + formula	0B13 36E0h + formula
6E4h + formula	MII_G_RT_FT3_m_LEN_PRU1	Filter3 Length Offset for (PRU1)	0B03 36E4h + formula	0B13 36E4h + formula

Table 15-1278. PRU_MII_G_RT_MII_G_RT Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G Physical Address	PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G Physical Address
6E8h + formula	MII_G_RT_FT3_m_CFG_PRU1	Filter3<m> Configuration (PRU1)	0B03 36E8h + formula	0B13 36E8h + formula
6ECh + formula	MII_G_RT_FT3_m_T_PRU1	Filter3<m> T (PRU1)	0B03 36ECh + formula	0B13 36ECh + formula
6F0h + formula	MII_G_RT_FT3_m_T_MASK_PRU1	Filter3<m> T Mask (PRU1)	0B03 36F0h + formula	0B13 36F0h + formula
8D4h + formula	MII_G_RT_FT3_m_P0_PRU1	Filter3<m>P0 (PRU1)	0B03 38D4h + formula	0B13 38D4h + formula
8D8h + formula	MII_G_RT_FT3_m_P1_PRU1	Filter3<m>P1 (PRU1)	0B03 38D8h + formula	0B13 38D8h + formula
8DCh + formula	MII_G_RT_FT3_m_P_MASK0_PRU1	Filter3 P Mask0 (PRU1)	0B03 38DCh + formula	0B13 38DCh + formula
8E0h + formula	MII_G_RT_FT3_m_P_MASK1_PRU1	Filter3 P Mask1 (PRU1)	0B03 38E0h + formula	0B13 38E0h + formula
9D4h	MII_G_RT_FT_RX_PTR_PRU1	Filter Byte Count (PRU1)	0B03 39D4h	0B13 39D4h
9D8h + formula	MII_G_RT_RX_CLASSm_AND_EN_PRU1	RX Class<m> AND Enable (PRU1)	0B03 39D8h + formula	0B13 39D8h + formula
9DCh + formula	MII_G_RT_RX_CLASSm_OR_EN_PRU1	RX Class<m> OR Enable (PRU1)	0B03 39DCh + formula	0B13 39DCh + formula
A58h	MII_G_RT_RX_CLASS_CFG1_PRU1	RX Class Configuration 1 Register	0B03 3A58h	0B13 3A58h
A5Ch	MII_G_RT_RX_CLASS_CFG2_PRU1	RX Class Configuration 2 Register	0B03 3A5Ch	0B13 3A5Ch
A60h + formula	MII_G_RT_RX_CLASS_GATESm_PRU1	RX Class Gate Configuration PRU1 Register	0B03 3A60h + formula	0B13 3A60h + formula
AA0h	MII_G_RT_RX_GREEN_PRU1	RX Green Status PRU1	0B03 3AA0h	0B13 3AA0h
AA4h	MII_G_RT_SA_HASH_PRU1	SA Hash Seed PRU1	0B03 3AA4h	0B13 3AA4h
AA8h	MII_G_RT_CONN_HASH_PRU1	Connection Hash Seed PRU1	0B03 3AA8h	0B13 3AA8h
AACH	MII_G_RT_CONN_HASH_START_PRU1	Connection Hash Start PRU1	0B03 3AACH	0B13 3AACH
AB0h + formula	MII_G_RT_RX_RATE_CFGn_PRU1	RX Rate Configuration Register	0B03 3AB0h + formula	0B13 3AB0h + formula
AD0h	MII_G_RT_RX_RATE_SRC_SEL0_PRU1	RX Rate Source Select0	0B03 3AD0h	0B13 3AD0h
AD4h	MII_G_RT_RX_RATE_SRC_SEL1_PRU1	RX Rate Source Select1	0B03 3AD4h	0B13 3AD4h
AD8h + formula	MII_G_RT_TX_RATE_CFG1_n_PRU1	TX Rate Configuration1 Register	0B03 3AD8h + formula	0B13 3AD8h + formula
ADCh + formula	MII_G_RT_TX_RATE_CFG2_n_PRU1	TX Rate Configuration2 Register	0B03 3ADCh + formula	0B13 3ADCh + formula
B18h	MII_G_RT_RX_STAT_GOOD_PRU1	RX Good Frame Count (PRU1)	0B03 3B18h	0B13 3B18h
B1Ch	MII_G_RT_RX_STAT_BC_PRU1	RX BC Frame Count (PRU1)	0B03 3B1Ch	0B13 3B1Ch
B20h	MII_G_RT_RX_STAT_MC_PRU1	RX MC Frame Count (PRU1)	0B03 3B20h	0B13 3B20h
B24h	MII_G_RT_RX_STAT_CRC_ERR_PRU1	RX CRC Error Frame Count (PRU1)	0B03 3B24h	0B13 3B24h
B28h	MII_G_RT_RX_STAT_MII_ERR_PRU1	RX MII Error Frame Count (PRU1)	0B03 3B28h	0B13 3B28h
B2Ch	MII_G_RT_RX_STAT_ODD_ERR_PRU1	RX Odd Nibble Frame Count (PRU1)	0B03 3B2Ch	0B13 3B2Ch
B30h	MII_G_RT_RX_STAT_MAX_SIZE_PRU1	RX Max Size Frame (PRU1)	0B03 3B30h	0B13 3B30h

Table 15-1278. PRU_MII_G_RT_MII_G_RT Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G Physical Address	PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G Physical Address
B34h	MII_G_RT_RX_STAT_MAX_ERR_PRU1	RX Max Size Error Frame Count (PRU1)	0B03 3B34h	0B13 3B34h
B38h	MII_G_RT_RX_STAT_MIN_SIZE_PRU1	RX Min Size Frame (PRU1)	0B03 3B38h	0B13 3B38h
B3Ch	MII_G_RT_RX_STAT_MIN_ERR_PRU1	RX Min Size Error Frame Count (PRU1)	0B03 3B3Ch	0B13 3B3Ch
B40h	MII_G_RT_RX_STAT_OVERRUN_ERR_PRU1	RX Overrun Frame Count (PRU1)	0B03 3B40h	0B13 3B40h
B44h + formula	MII_G_RT_RX_STAT_CLASSm_HIT_PRU1	RX Class<m>	0B03 3B44h + formula	0B13 3B44h + formula
B84h	MII_G_RT_RX_STAT_SMD_FRAG_ERR_PRU1	RX SMD Frag Error Count (PRU1)	0B03 3B84h	0B13 3B84h
B88h	MII_G_RT_RX_STAT_BKT1_SIZE_PRU1	RX Bucket1 Size Configuration (PRU1)	0B03 3B88h	0B13 3B88h
B8Ch	MII_G_RT_RX_STAT_BKT2_SIZE_PRU1	RX Bucket2 Size Configuration (PRU1)	0B03 3B8Ch	0B13 3B8Ch
B90h	MII_G_RT_RX_STAT_BKT3_SIZE_PRU1	RX Bucket3 Size Configuration (PRU1)	0B03 3B90h	0B13 3B90h
B94h	MII_G_RT_RX_STAT_BKT4_SIZE_PRU1	RX Bucket4 Size Configuration (PRU1)	0B03 3B94h	0B13 3B94h
B98h	MII_G_RT_RX_STAT_64_PRU1	RX 64B Sized Frame Count (PRU1)	0B03 3B98h	0B13 3B98h
B9Ch	MII_G_RT_RX_STAT_BKT1_PRU1	RX Bucket1 Sized Frame Count (PRU1)	0B03 3B9Ch	0B13 3B9Ch
BA0h	MII_G_RT_RX_STAT_BKT2_PRU1	RX Bucket2 Sized Frame Count (PRU1)	0B03 3BA0h	0B13 3BA0h
BA4h	MII_G_RT_RX_STAT_BKT3_PRU1	RX Bucket3 Sized Frame Count (PRU1)	0B03 3BA4h	0B13 3BA4h
BA8h	MII_G_RT_RX_STAT_BKT4_PRU1	RX Bucket4 Sized Frame Count (PRU1)	0B03 3BA8h	0B13 3BA8h
BACh	MII_G_RT_RX_STAT_BKT5_PRU1	RX Bucket5 Sized Frame Count (PRU1)	0B03 3BACh	0B13 3BACh
BB0h	MII_G_RT_RX_STAT_TOTAL_BYTES_PRU1	RX Total Byte Count (PRU1)	0B03 3BB0h	0B13 3BB0h
BB4h	MII_G_RT_RXTX_STAT_TOTAL_BYTES_PRU1	RX TX Total Byte Count (PRU1)	0B03 3BB4h	0B13 3BB4h
BB8h	MII_G_RT_TX_STAT_GOOD_PORT1	TX Good Frame Count Port1	0B03 3BB8h	0B13 3BB8h
BBCh	MII_G_RT_TX_STAT_BC_PORT1	TX BC Frame Count Port1	0B03 3BBCh	0B13 3BBCh
BC0h	MII_G_RT_TX_STAT_MC_PORT1	TX MC Frame Count Port1	0B03 3BC0h	0B13 3BC0h
BC4h	MII_G_RT_TX_STAT_ODD_ERR_PORT1	TX Odd Nibble Frame Count Port1	0B03 3BC4h	0B13 3BC4h
BC8h	MII_G_RT_TX_STAT_UNDERFLOW_ERR_PORT1	TX Under Flow Error Count Port1	0B03 3BC8h	0B13 3BC8h
BCCh	MII_G_RT_TX_STAT_MAX_SIZE_PORT1	TX Max Size Frame Port1	0B03 3BCCh	0B13 3BCCh
BD0h	MII_G_RT_TX_STAT_MAX_ERR_PORT1	TX Max Size Error Frame Count Port1	0B03 3BD0h	0B13 3BD0h
BD4h	MII_G_RT_TX_STAT_MIN_SIZE_PORT1	TX Min Size Frame Port1	0B03 3BD4h	0B13 3BD4h
BD8h	MII_G_RT_TX_STAT_MIN_ERR_PORT1	TX Min Size Error Frame Count Port1	0B03 3BD8h	0B13 3BD8h
BDCh	MII_G_RT_TX_STAT_BKT1_SIZE_PORT1	TX Bucket1 Size Configuration Port1	0B03 3BDCh	0B13 3BDCh

Table 15-1278. PRU_MII_G_RT_MII_G_RT Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G Physical Address	PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G Physical Address
BE0h	MII_G_RT_TX_STAT_BKT2_SIZE_PORT1	TX Bucket2 Size Configuration Port1	0B03 3BE0h	0B13 3BE0h
BE4h	MII_G_RT_TX_STAT_BKT3_SIZE_PORT1	TX Bucket3 Size Configuration Port1	0B03 3BE4h	0B13 3BE4h
BE8h	MII_G_RT_TX_STAT_BKT4_SIZE_PORT1	TX Bucket4 Size Configuration Port1	0B03 3BE8h	0B13 3BE8h
BECh	MII_G_RT_TX_STAT_64_PORT1	TX 64B Sized Frame Count Port1	0B03 3BECh	0B13 3BECh
BF0h	MII_G_RT_TX_STAT_BKT1_PORT1	TX Bucket1 Sized Frame Count Port1	0B03 3BF0h	0B13 3BF0h
BF4h	MII_G_RT_TX_STAT_BKT2_PORT1	TX Bucket2 Sized Frame Count Port1	0B03 3BF4h	0B13 3BF4h
BF8h	MII_G_RT_TX_STAT_BKT3_PORT1	TX Bucket3 Sized Frame Count Port1	0B03 3BF8h	0B13 3BF8h
BFCh	MII_G_RT_TX_STAT_BKT4_PORT1	TX Bucket4 Sized Frame Count Port1	0B03 3BFCh	0B13 3BFCh
C00h	MII_G_RT_TX_STAT_BKT5_PORT1	TX Bucket5 Sized Frame Count Port1	0B03 3C00h	0B13 3C00h
C04h	MII_G_RT_TX_STAT_TOTAL_BYTE_S_PORT1	TX Total Byte Count Port1	0B03 3C04h	0B13 3C04h
C08h	MII_G_RT_TX_HSR_TAG_PORT1	TX HSR TAG Port1	0B03 3C08h	0B13 3C08h
C0Ch	MII_G_RT_TX_HSR_SEQ_PORT1	TX HSR Seq Port1	0B03 3C0Ch	0B13 3C0Ch
C10h	MII_G_RT_TX_VLAN_TYPE_TAG_PORT1	TX VLAN Type TAG Port1	0B03 3C10h	0B13 3C10h
C14h	MII_G_RT_TX_VLAN_INS_TAG_PORT1	TX VLAN Insertion TAG Port1	0B03 3C14h	0B13 3C14h
D00h + formula	MII_G_RT_QUEUEk	Queue<k>	0B03 3D00h + formula	0B13 3D00h + formula
E00h + formula	MII_G_RT_QUEUE_PEEKm	Queue Peek<m>	0B03 3E00h + formula	0B13 3E00h + formula
E40h + formula	MII_G_RT_QUEUE_CNTk	Queue Count<k>	0B03 3E40h + formula	0B13 3E40h + formula
F40h	MII_G_RT_QUEUE_RESET	Queue Reset	0B03 3F40h	0B13 3F40h

15.12.1 MII_G_RT_ICSS_G_CFG Register (Offset = 0h) [reset = X]

MIIG_RT_ICSS_G_CFG is shown in [Figure 15-419](#) and described in [Table 15-1280](#).

Return to [Summary Table](#).

ICSS_G Config

Table 15-1279. MII_G_RT_ICSS_G_CFG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3000h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3000h

Figure 15-419. MII_G_RT_ICSS_G_CFG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							SGMII_MODE
R/W-X							R/W-1h
15	14	13	12	11	10	9	8
RESERVED				TX_PRU_EN	RX_SFD_TX_SOF_EN	RTU_PRU_PSI_SHARE_EN	IEP1_TX_EN
R/W-X				R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED	MII1_MODE		MII0_MODE		RX_L2_G_EN	TX_L2_EN	TX_L1_EN
R/W-X	R/W-0h		R/W-0h		R/W-0h	R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1280. MII_G_RT_ICSS_G_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16	SGMII_MODE	R/W	1h	SGMII MODE 0: Fiber MODE 1: SGMII MODE
15-12	RESERVED	R/W	X	
11	TX_PRU_EN	R/W	0h	Enable TX_PRU to gain control of MII TXL2
10	RX_SFD_TX_SOF_EN	R/W	0h	Enable the remapping of tx_sof to rx_sfd if auto fwd is enable
9	RTU_PRU_PSI_SHARE_EN	R/W	0h	Enable the sharing of xfr2psi attached to PRU for PRU RTU AND HW FIFO
8	IEP1_TX_EN	R/W	0h	Enable IEP1 for TX Enable 0: Use IEP0 CMP3_4 1: Use IEP1 CMP3_4
7	RESERVED	R/W	X	
6-5	MII1_MODE	R/W	0h	MII1 MODE 0: MII 1: RGMII 2: SGMII SGMII mode is supported only for PRU_ICSSG1 instance.
4-3	MII0_MODE	R/W	0h	MII0 MODE 0: MII 1: RGMII 2: SGMII SGMII mode is supported only for PRU_ICSSG1 instance.

Table 15-1280. MII_G_RT_ICSS_G_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RX_L2_G_EN	R/W	0h	Enable new RX L2 mode of operation for non-EtherCAT Target protocols. 0: Disabled 1: Enabled Disable for EtherCAT Target protocols, enable for all other protocols.
1	TX_L2_EN	R/W	0h	Enable the TX L2 FIFO 0: Disabled 1: Enabled
0	TX_L1_EN	R/W	1h	Enable the TX L1 FIFO 0: Disabled 1: Enabled

Table 15-1281. Register Call Summary for MII_G_RT_ICSS_G_CFG

Programmable Real-Time Unit and Industrial Communication Subsystem - Gigabit(SR2.0) • PRU_ICSSG Top Level Resources Functional Description: [0]
PRU_MII_G_RT_MII_G_RT Registers • MII_G_RT_ICSS_G_CFG Register (Offset = 0h) [reset = X]: [0]
PRU_ICSSG Broadside Accelerators • RTU_PRU/ PRU to XFR2VBUS Interface: [0]
PRU_ICSSG MII_G_RT Module • RX MII Port → RX L1 FIFO → RX L2 Buffer → PRU: [0] [1] [2]

15.12.2 MII_G_RT_RGMII_CFG Register (Offset = 4h) [reset = X]

MIIG_RT_RGMII_CFG is shown in Figure 15-420 and described in Table 15-1283.

Return to [Summary Table](#).

RGMII

Table 15-1282. MII_G_RT_RGMII_CFG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3004h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3004h

Figure 15-420. MII_G_RT_RGMII_CFG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED	RGMII1_FULLDUPLEX_IN	RGMII1_GIG_IN	RGMII1_INBAND	RESERVED	RGMII0_FULLDUPLEX_IN	RGMII0_GIG_IN	RGMII0_INBAND
R/W-X	R/W-1h	R/W-1h	R/W-0h	R/W-X	R/W-1h	R/W-1h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED						RGMII_EEE_P HY_ONLY	RGMII_EEE_E N
R/W-X						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RGMII1_FULLDUPLEX	RGMII1_SPEED		RGMII1_LINK	RGMII0_FULLDUPLEX	RGMII0_SPEED		RGMII0_LINK
R-0h	R-0h		R-0h	R-0h	R-0h		R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-1283. MII_G_RT_RGMII_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22	RGMII1_FULLDUPLEX_IN	R/W	1h	RGMII Full duplex override 0: half 1: full
21	RGMII1_GIG_IN	R/W	1h	RGMII GigBit Enable 0: 100 Mbs 1: 1000 Mbs
20	RGMII1_INBAND	R/W	0h	RGMII In Band Enable or Force 0: InBAND is Disabled 1: InBAND Enable
19	RESERVED	R/W	X	
18	RGMII0_FULLDUPLEX_IN	R/W	1h	RGMII Full duplex override 0: half 1: full
17	RGMII0_GIG_IN	R/W	1h	RGMII GigBit Enable 0: 100 Mbs 1: 1000 Mbs
16	RGMII0_INBAND	R/W	0h	RGMII In Band Enable or Force 0: InBAND is Disabled 1: InBAND Enable
15-10	RESERVED	R/W	X	

Table 15-1283. MII_G_RT_RGMII_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	RGMII_EEE_PHY_ONLY	R/W	0h	RGMII Phy Only Low Power 0: disable 1: enable
8	RGMII_EEE_EN	R/W	0h	RGMII Energy Efficient Enable 0: disable 1: enable
7	RGMII1_FULLDUPLEX	R	0h	RGMII Fullduplex 0: half duplex 1: full duplex
6-5	RGMII1_SPEED	R	0h	RGMII Speed 00: 10 Mbps 01: 100 Mbps 10: 1000 Mbps
4	RGMII1_LINK	R	0h	RGMII Link Status 0: link is down 1: link is up
3	RGMII0_FULLDUPLEX	R	0h	RGMII Fullduplex 0: half duplex 1: full duplex
2-1	RGMII0_SPEED	R	0h	RGMII Speed 00: 10 Mbps 01: 100 Mbps 10: 1000 Mbps
0	RGMII0_LINK	R	0h	RGMII Link Status 0: link is down 1: link is up

Table 15-1284. Register Call Summary for MII_G_RT_RGMII_CFG

PRU_MII_G_RT_MII_G_RT Registers

- [MII_G_RT_RGMII_CFG Register \(Offset = 4h\) \[reset = X\]: \[0\]](#)

15.12.3 MII_G_RT_MAC_PRU0_0 Register (Offset = 8h) [reset = 0h]

MIIG_RT_MAC_PRU0_0 is shown in [Figure 15-421](#) and described in [Table 15-1286](#).

Return to [Summary Table](#).

PRU0 MAC (DA3:DA0).

Table 15-1285. MII_G_RT_MAC_PRU0_0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3008h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3008h

Figure 15-421. MII_G_RT_MAC_PRU0_0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAC_PRU0_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1286. MII_G_RT_MAC_PRU0_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MAC_PRU0_0	R/W	0h	MAC PRU0 DA3:DA0 Used for SAV and DA match

Table 15-1287. Register Call Summary for MII_G_RT_MAC_PRU0_0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_MAC_PRU0_0 Register \(Offset = 8h\) \[reset = 0h\]: \[0\]](#)

15.12.4 MII_G_RT_MAC_PRU0_1 Register (Offset = Ch) [reset = X]

MIIG_RT_MAC_PRU0_1 is shown in [Figure 15-422](#) and described in [Table 15-1289](#).

Return to [Summary Table](#).

PRU0 MAC (DA5:DA4).

Table 15-1288. MII_G_RT_MAC_PRU0_1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 300Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 300Ch

Figure 15-422. MII_G_RT_MAC_PRU0_1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																MAC_PRU0_1															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1289. MII_G_RT_MAC_PRU0_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	MAC_PRU0_1	R/W	0h	MAC PRU0 DA5:DA4 Used for SAV and DA match

Table 15-1290. Register Call Summary for MII_G_RT_MAC_PRU0_1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_MAC_PRU0_1 Register \(Offset = Ch\) \[reset = X\]: \[0\]](#)

15.12.5 MII_G_RT_MAC_PRU1_0 Register (Offset = 10h) [reset = 0h]

MIIG_RT_MAC_PRU1_0 is shown in [Figure 15-423](#) and described in [Table 15-1292](#).

Return to [Summary Table](#).

PRU1 MAC (DA3:DA0).

Table 15-1291. MII_G_RT_MAC_PRU1_0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3010h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3010h

Figure 15-423. MII_G_RT_MAC_PRU1_0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAC_PRU1_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1292. MII_G_RT_MAC_PRU1_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MAC_PRU1_0	R/W	0h	MAC PRU1 DA3:DA0 Used for SAV and DA match

Table 15-1293. Register Call Summary for MII_G_RT_MAC_PRU1_0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_MAC_PRU1_0 Register \(Offset = 10h\) \[reset = 0h\]: \[0\]](#)

15.12.6 MII_G_RT_MAC_PRU1_1 Register (Offset = 14h) [reset = X]

MIIG_RT_MAC_PRU1_1 is shown in Figure 15-424 and described in Table 15-1295.

Return to [Summary Table](#).

PRU1 MAC (DA5:DA4).

Table 15-1294. MII_G_RT_MAC_PRU1_1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3014h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3014h

Figure 15-424. MII_G_RT_MAC_PRU1_1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																MAC_PRU1_1															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1295. MII_G_RT_MAC_PRU1_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	MAC_PRU1_1	R/W	0h	MAC PRU1 DA5:DA4 Used for SAV and DA match

Table 15-1296. Register Call Summary for MII_G_RT_MAC_PRU1_1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_MAC_PRU1_1 Register \(Offset = 14h\) \[reset = X\]: \[0\]](#)

15.12.7 MII_G_RT_MAC_INTERFACE_0 Register (Offset = 18h) [reset = 0h]

MIIG_RT_MAC_INTERFACE_0 is shown in [Figure 15-425](#) and described in [Table 15-1298](#).

Return to [Summary Table](#).

MAC Host Interface (DA3:DA0).

Table 15-1297. MII_G_RT_MAC_INTERFACE_0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3018h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3018h

Figure 15-425. MII_G_RT_MAC_INTERFACE_0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAC_INF_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1298. MII_G_RT_MAC_INTERFACE_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MAC_INF_0	R/W	0h	MAC Host interface DA3:DA0 Used for SAV and DA match

Table 15-1299. Register Call Summary for MII_G_RT_MAC_INTERFACE_0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_MAC_INTERFACE_0 Register \(Offset = 18h\) \[reset = 0h\]: \[0\]](#)

15.12.8 MII_G_RT_MAC_INTERFACE_1 Register (Offset = 1Ch) [reset = X]

MIIG_RT_MAC_INTERFACE_1 is shown in Figure 15-426 and described in Table 15-1301.

Return to [Summary Table](#).

MAC Host Interface (DA5:DA4).

Table 15-1300. MII_G_RT_MAC_INTERFACE_1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 301Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 301Ch

Figure 15-426. MII_G_RT_MAC_INTERFACE_1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																MAC_INF_1															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1301. MII_G_RT_MAC_INTERFACE_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	MAC_INF_1	R/W	0h	MAC Host interface DA 5:DA4 Used for SAV and DA match

Table 15-1302. Register Call Summary for MII_G_RT_MAC_INTERFACE_1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_MAC_INTERFACE_1 Register \(Offset = 1Ch\) \[reset = X\]: \[0\]](#)

15.12.9 MII_G_RT_PREEMPT_CFG Register (Offset = 20h) [reset = X]

MIIG_RT_PREEMPT_CFG is shown in [Figure 15-427](#) and described in [Table 15-1304](#).

Return to [Summary Table](#).

Preempt Configuration Register.

Table 15-1303. MII_G_RT_PREEMPT_CFG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3020h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3020h

Figure 15-427. MII_G_RT_PREEMPT_CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMD_R								SMD_V								EXP_SMD								RESERVED							
R/W-19h								R/W-7h								R/W-D5h								R/W-X							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1304. MII_G_RT_PREEMPT_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	SMD_R	R/W	19h	Response frame TAG
23-16	SMD_V	R/W	7h	Verification frame TAG
15-8	EXP_SMD	R/W	D5h	None pre-emptable frame start, or express frame
7-0	RESERVED	R/W	X	

Table 15-1305. Register Call Summary for MII_G_RT_PREEMPT_CFG

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_PREEMPT_CFG Register \(Offset = 20h\) \[reset = X\]: \[0\]](#)

15.12.10 MII_G_RT_SMDT1S_CFG Register (Offset = 24h) [reset = B37F4CE6h]

MIIG_RT_SMDT1S_CFG is shown in Figure 15-428 and described in Table 15-1307.

Return to [Summary Table](#).

SMD Type1S Preemptable Frame Start Configuration.

Table 15-1306. MII_G_RT_SMDT1S_CFG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3024h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3024h

Figure 15-428. MII_G_RT_SMDT1S_CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMDT1S_3								SMDT1S_2								SMDT1S_1								SMDT1S_0							
R/W-B3h								R/W-7Fh								R/W-4Ch								R/W-E6h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1307. MII_G_RT_SMDT1S_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	SMDT1S_3	R/W	B3h	SMDT1S3 pattern
23-16	SMDT1S_2	R/W	7Fh	SMDT1S2 pattern
15-8	SMDT1S_1	R/W	4Ch	SMDT1S1 pattern
7-0	SMDT1S_0	R/W	E6h	SMDT1S0 pattern

Table 15-1308. Register Call Summary for MII_G_RT_SMDT1S_CFG

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_SMDT1S_CFG Register \(Offset = 24h\) \[reset = B37F4CE6h\]: \[0\]](#)

15.12.11 MII_G_RT_SMDT1C_CFG Register (Offset = 28h) [reset = 2A9E5261h]

MIIG_RT_SMDT1C_CFG is shown in Figure 15-429 and described in Table 15-1310.

Return to [Summary Table](#).

SMD Type1C None Initial Frag Configuration.

Table 15-1309. MII_G_RT_SMDT1C_CFG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3028h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3028h

Figure 15-429. MII_G_RT_SMDT1C_CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMDT1C_3								SMDT1C_2								SMDT1C_1								SMDT1C_0							
R/W-2Ah								R/W-9Eh								R/W-52h								R/W-61h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1310. MII_G_RT_SMDT1C_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	SMDT1C_3	R/W	2Ah	SMDT1C3 pattern
23-16	SMDT1C_2	R/W	9Eh	SMDT1C2 pattern
15-8	SMDT1C_1	R/W	52h	SMDT1C1 pattern
7-0	SMDT1C_0	R/W	61h	SMDT1C0 pattern

Table 15-1311. Register Call Summary for MII_G_RT_SMDT1C_CFG

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_SMDT1C_CFG Register \(Offset = 28h\) \[reset = 2A9E5261h\]: \[0\]](#)

15.12.12 MII_G_RT_FRAG_CNT_CFG Register (Offset = 34h) [reset = B37F4CE6h]

MIIG_RT_FRAG_CNT_CFG is shown in Figure 15-430 and described in Table 15-1313.

Return to [Summary Table](#).

Frag Count Configuration.

Table 15-1312. MII_G_RT_FRAG_CNT_CFG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3034h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3034h

Figure 15-430. MII_G_RT_FRAG_CNT_CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FRAG_CNT_3								FRAG_CNT_2							
R/W-B3h								R/W-7Fh							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRAG_CNT_1								FRAG_CNT_0							
R/W-4Ch								R/W-E6h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1313. MII_G_RT_FRAG_CNT_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	FRAG_CNT_3	R/W	B3h	FRAG Cnt3 pattern
23-16	FRAG_CNT_2	R/W	7Fh	FRAG Cnt2 pattern
15-8	FRAG_CNT_1	R/W	4Ch	FRAG Cnt1 pattern
7-0	FRAG_CNT_0	R/W	E6h	FRAG Cnt0 pattern

Table 15-1314. Register Call Summary for MII_G_RT_FRAG_CNT_CFG

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FRAG_CNT_CFG Register \(Offset = 34h\) \[reset = B37F4CE6h\]: \[0\]](#)

15.12.13 MII_G_RT_PA_STAT_PUSH0 Register (Offset = 40h) [reset = 0h]

MIIG_RT_PA_STAT_PUSH0 is shown in [Figure 15-431](#) and described in [Table 15-1316](#).

Return to [Summary Table](#).

Pa Stat Push0.

Table 15-1315. MII_G_RT_PA_STAT_PUSH0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3040h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3040h

Figure 15-431. MII_G_RT_PA_STAT_PUSH0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PA_STAT_PUSH3_0								PA_STAT_PUSH2_0							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PA_STAT_PUSH1_0								PA_STAT_PUSH0_0							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1316. MII_G_RT_PA_STAT_PUSH0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PA_STAT_PUSH3_0	R/W	0h	pa stat push3
23-16	PA_STAT_PUSH2_0	R/W	0h	pa stat push2
15-8	PA_STAT_PUSH1_0	R/W	0h	pa stat push1
7-0	PA_STAT_PUSH0_0	R/W	0h	pa stat push0

Table 15-1317. Register Call Summary for MII_G_RT_PA_STAT_PUSH0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_PA_STAT_PUSH0 Register \(Offset = 40h\) \[reset = 0h\]: \[0\]](#)

15.12.14 MII_G_RT_PA_STAT_PUSH1 Register (Offset = 44h) [reset = 0h]

MIIG_RT_PA_STAT_PUSH1 is shown in Figure 15-432 and described in Table 15-1319.

Return to [Summary Table](#).

Pa Stat Push1.

Table 15-1318. MII_G_RT_PA_STAT_PUSH1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3044h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3044h

Figure 15-432. MII_G_RT_PA_STAT_PUSH1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PA_STAT_PUSH3_1								PA_STAT_PUSH2_1							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PA_STAT_PUSH1_1								PA_STAT_PUSH0_1							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1319. MII_G_RT_PA_STAT_PUSH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PA_STAT_PUSH3_1	R/W	0h	pa stat push3
23-16	PA_STAT_PUSH2_1	R/W	0h	pa stat push2
15-8	PA_STAT_PUSH1_1	R/W	0h	pa stat push1
7-0	PA_STAT_PUSH0_1	R/W	0h	pa stat push0

Table 15-1320. Register Call Summary for MII_G_RT_PA_STAT_PUSH1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_PA_STAT_PUSH1 Register \(Offset = 44h\) \[reset = 0h\]: \[0\]](#)

15.12.15 MII_G_RT_PA_STAT_PUSH2 Register (Offset = 48h) [reset = 0h]

MIIG_RT_PA_STAT_PUSH2 is shown in Figure 15-433 and described in Table 15-1322.

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Pa Stat Push2.

Table 15-1321. MII_G_RT_PA_STAT_PUSH2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3048h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3048h

Figure 15-433. MII_G_RT_PA_STAT_PUSH2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PA_STAT_PUSH3_2								PA_STAT_PUSH2_2							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PA_STAT_PUSH1_2								PA_STAT_PUSH0_2							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1322. MII_G_RT_PA_STAT_PUSH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PA_STAT_PUSH3_2	R/W	0h	pa stat push3
23-16	PA_STAT_PUSH2_2	R/W	0h	pa stat push2
15-8	PA_STAT_PUSH1_2	R/W	0h	pa stat push1
7-0	PA_STAT_PUSH0_2	R/W	0h	pa stat push0

Table 15-1323. Register Call Summary for MII_G_RT_PA_STAT_PUSH2

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_PA_STAT_PUSH2 Register \(Offset = 48h\) \[reset = 0h\]: \[0\]](#)

15.12.16 MII_G_RT_PA_STAT_PUSH3 Register (Offset = 4Ch) [reset = 0h]

MIIG_RT_PA_STAT_PUSH3 is shown in Figure 15-434 and described in Table 15-1325.

Return to [Summary Table](#).

Pa Stat Push3.

Table 15-1324. MII_G_RT_PA_STAT_PUSH3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 304Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 304Ch

Figure 15-434. MII_G_RT_PA_STAT_PUSH3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PA_STAT_PUSH3_3								PA_STAT_PUSH2_3							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PA_STAT_PUSH1_3								PA_STAT_PUSH0_3							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1325. MII_G_RT_PA_STAT_PUSH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PA_STAT_PUSH3_3	R/W	0h	pa stat push3
23-16	PA_STAT_PUSH2_3	R/W	0h	pa stat push2
15-8	PA_STAT_PUSH1_3	R/W	0h	pa stat push1
7-0	PA_STAT_PUSH0_3	R/W	0h	pa stat push0

Table 15-1326. Register Call Summary for MII_G_RT_PA_STAT_PUSH3

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_PA_STAT_PUSH3 Register \(Offset = 4Ch\) \[reset = 0h\]: \[0\]](#)

15.12.17 MII_G_RT_FDB_GEN_CFG1 Register (Offset = 60h) [reset = X]

MIIG_RT_FDB_GEN_CFG1 is shown in Figure 15-435 and described in Table 15-1328.

Return to [Summary Table](#).

FDB Configuration1.

Table 15-1327. MII_G_RT_FDB_GEN_CFG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3060h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3060h

Figure 15-435. MII_G_RT_FDB_GEN_CFG1 Register

31	30	29	28	27	26	25	24
RESERVED						SMEM_VLAN_OFFSET	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
SMEM_VLAN_OFFSET							
R/W-0h							
15	14	13	12	11	10	9	8
SMEM_VLAN_OFFSET							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED	FDB_HASH_SIZE				RESERVED	FDB_BUCKET_SIZE	
R/W-X	R/W-4h				R/W-X	R/W-2h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1328. MII_G_RT_FDB_GEN_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-8	SMEM_VLAN_OFFSET	R/W	0h	SMEM VLAN FID table base address
7	RESERVED	R/W	X	
6-3	FDB_HASH_SIZE	R/W	4h	FDB hash size (Slots) 0: 64 1: 128 2: 256 3: 512 4: 1024 5: 2048
2	RESERVED	R/W	X	
1-0	FDB_BUCKET_SIZE	R/W	2h	FDB bucket size 0: 1 1: 2 2: 4 3: 8

Table 15-1329. Register Call Summary for MII_G_RT_FDB_GEN_CFG1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FDB_GEN_CFG1 Register \(Offset = 60h\) \[reset = X\]: \[0\]](#)

15.12.18 MII_G_RT_FDB_GEN_CFG2 Register (Offset = 64h) [reset = X]

MIIG_RT_FDB_GEN_CFG2 is shown in Figure 15-436 and described in Table 15-1331.

Return to [Summary Table](#).

FDB Configuration2.

Table 15-1330. MII_G_RT_FDB_GEN_CFG2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3064h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3064h

Figure 15-436. MII_G_RT_FDB_GEN_CFG2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED			FDB_GEN_MODE_BYTE_EN			FDB_GEN_MODE_EN_BK1	
R/W-X			R/W-0h			R/W-0h	
7	6	5	4	3	2	1	0
FDB_GEN_MODE_EN_BK0	FDB_VLAN_EN	FDB_HSR_EN	RESERVED		FDB_HOST_EN	FDB_PRU1_EN	FDB_PRU0_EN
R/W-0h	R/W-0h	R/W-0h	R/W-X		R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1331. MII_G_RT_FDB_GEN_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R/W	X	
12-9	FDB_GEN_MODE_BYTE_EN	R/W	0h	FDB General Mode Byte compare size 0 = 1 Byte, 15 = 16 Bytes
8	FDB_GEN_MODE_EN_BK1	R/W	0h	FDB General Mode Enable Bank1 if set PRU0/PRU1/HOST will get disabled
7	FDB_GEN_MODE_EN_BK0	R/W	0h	FDB General Mode Enable Bank0 if set PRU0/PRU1/HOST will get disabled
6	FDB_VLAN_EN	R/W	0h	FDB Global VLAN Enable
5	FDB_HSR_EN	R/W	0h	FDB Global HSR Enable Note: VLAN must be disabled
4-3	RESERVED	R/W	X	
2	FDB_HOST_EN	R/W	0h	FDB HOST Enable
1	FDB_PRU1_EN	R/W	0h	FDB PRU1 Enable
0	FDB_PRU0_EN	R/W	0h	FDB PRU0 Enable

Table 15-1332. Register Call Summary for MII_G_RT_FDB_GEN_CFG2

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FDB_GEN_CFG2 Register \(Offset = 64h\) \[reset = X\]: \[0\]](#)

Table 15-1332. Register Call Summary for MII_G_RT_FDB_GEN_CFG2 (continued)

PRU_ICSSG Broadside Accelerators

- [FDB Modes of operation: \[0\] \[7\] \[8\] \[9\] \[10\] \[11\]](#)

15.12.19 MII_G_RT_FDB_DF_VLAN Register (Offset = 6Ch) [reset = X]

MIIG_RT_FDB_DF_VLAN is shown in Figure 15-437 and described in Table 15-1334.

Return to [Summary Table](#).

FDB Default PRU VLAN.

Table 15-1333. MII_G_RT_FDB_DF_VLAN Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 306Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 306Ch

Figure 15-437. MII_G_RT_FDB_DF_VLAN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				FDB_PRU1_DF_VLAN											
R/W-X				R/W-1h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				FDB_PRU0_DF_VLAN											
R/W-X				R/W-1h											

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1334. MII_G_RT_FDB_DF_VLAN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	FDB_PRU1_DF_VLAN	R/W	1h	FDB Default VLAN for PRU1
15-12	RESERVED	R/W	X	
11-0	FDB_PRU0_DF_VLAN	R/W	1h	FDB Default VLAN for PRU0

Table 15-1335. Register Call Summary for MII_G_RT_FDB_DF_VLAN

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FDB_DF_VLAN Register \(Offset = 6Ch\) \[reset = X\]: \[0\]](#)

15.12.20 MII_G_RT_FDB_HOST_DA0 Register (Offset = 70h) [reset = 0h]

MIIG_RT_FDB_HOST_DA0 is shown in [Figure 15-438](#) and described in [Table 15-1337](#).

Return to [Summary Table](#).

FDB HOST DA3:0 Configuration.

Table 15-1336. MII_G_RT_FDB_HOST_DA0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3070h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3070h

Figure 15-438. MII_G_RT_FDB_HOST_DA0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FDB_HOST_DA0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1337. MII_G_RT_FDB_HOST_DA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FDB_HOST_DA0	R/W	0h	FDB HOST DA3:0

Table 15-1338. Register Call Summary for MII_G_RT_FDB_HOST_DA0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FDB_HOST_DA0 Register \(Offset = 70h\) \[reset = 0h\]: \[0\]](#)

15.12.21 MII_G_RT_FDB_HOST_DA1 Register (Offset = 74h) [reset = X]

MIIG_RT_FDB_HOST_DA1 is shown in [Figure 15-439](#) and described in [Table 15-1340](#).

Return to [Summary Table](#).

FDB HOST DA5:4 Configuration.

Table 15-1339. MII_G_RT_FDB_HOST_DA1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3074h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3074h

Figure 15-439. MII_G_RT_FDB_HOST_DA1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FDB_HOST_DA1															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1340. MII_G_RT_FDB_HOST_DA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	FDB_HOST_DA1	R/W	0h	FDB HOST DA 5:4

Table 15-1341. Register Call Summary for MII_G_RT_FDB_HOST_DA1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FDB_HOST_DA1 Register \(Offset = 74h\) \[reset = X\]: \[0\]](#)

15.12.22 MII_G_RT_FDB_HOST_SA0 Register (Offset = 78h) [reset = 0h]

MIIG_RT_FDB_HOST_SA0 is shown in [Figure 15-440](#) and described in [Table 15-1343](#).

Return to [Summary Table](#).

FDB HOST SA3:0 Configuration.

Table 15-1342. MII_G_RT_FDB_HOST_SA0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3078h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3078h

Figure 15-440. MII_G_RT_FDB_HOST_SA0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FDB_HOST_SA0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1343. MII_G_RT_FDB_HOST_SA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FDB_HOST_SA0	R/W	0h	FDB HOST SA3:0

Table 15-1344. Register Call Summary for MII_G_RT_FDB_HOST_SA0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FDB_HOST_SA0 Register \(Offset = 78h\) \[reset = 0h\]: \[0\]](#)

15.12.23 MII_G_RT_FDB_HOST_VLAN_SA1 Register (Offset = 7Ch) [reset = 00010000h]

MIIG_RT_FDB_HOST_VLAN_SA1 is shown in [Figure 15-441](#) and described in [Table 15-1346](#).

Return to [Summary Table](#).

FDB HOST VLAN SA5:4 Configuration.

Table 15-1345. MII_G_RT_FDB_HOST_VLAN_SA1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 307Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 307Ch

Figure 15-441. MII_G_RT_FDB_HOST_VLAN_SA1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FDB_HOST_VLAN_HSR															
R/W-1h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FDB_HOST_SA1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1346. MII_G_RT_FDB_HOST_VLAN_SA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	FDB_HOST_VLAN_HSR	R/W	1h	FDB HOST VLAN[11:0] OR HSR [15:0]
15-0	FDB_HOST_SA1	R/W	0h	FDB HOST SA 5:4

Table 15-1347. Register Call Summary for MII_G_RT_FDB_HOST_VLAN_SA1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FDB_HOST_VLAN_SA1 Register \(Offset = 7Ch\) \[reset = 00010000h\]: \[0\]](#)

15.12.24 MII_G_RT_FT1_START_LEN_PRU0 Register (Offset = 80h) [reset = X]

MIIG_RT_FT1_START_LEN_PRU0 is shown in [Figure 15-442](#) and described in [Table 15-1349](#).

Return to [Summary Table](#).

Filter1 Start and Length (PRU0).

Table 15-1348. MII_G_RT_FT1_START_LEN_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3080h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3080h

Figure 15-442. MII_G_RT_FT1_START_LEN_PRU0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				FT1_LEN			
R/W-X				R/W-6h			
15	14	13	12	11	10	9	8
RESERVED	FT1_START						
R/W-X	R/W-0h						
7	6	5	4	3	2	1	0
FT1_START							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1349. MII_G_RT_FT1_START_LEN_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	FT1_LEN	R/W	6h	Defines the total number of Bytes Filter1 will check before Valid bit is set
15	RESERVED	R/W	X	
14-0	FT1_START	R/W	0h	Byte count start for Filter1. Any write will clear all Filter1 Status Bits

Table 15-1350. Register Call Summary for MII_G_RT_FT1_START_LEN_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT1_START_LEN_PRU0 Register \(Offset = 80h\) \[reset = X\]: \[0\]](#)

15.12.25 MII_G_RT_FT1_CFG_PRU0 Register (Offset = 84h) [reset = X]

MIIG_RT_FT1_CFG_PRU0 is shown in [Figure 15-443](#) and described in [Table 15-1352](#).

Return to [Summary Table](#).

Filter1 Configuration (PRU0).

Table 15-1351. MII_G_RT_FT1_CFG_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3084h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3084h

Figure 15-443. MII_G_RT_FT1_CFG_PRU0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
FT1_7CFG		FT1_6CFG		FT1_5CFG		FT1_4CFG	
R/W-1h		R/W-1h		R/W-1h		R/W-1h	
7	6	5	4	3	2	1	0
FT1_3CFG		FT1_2CFG		FT1_1CFG		FT1_0CFG	
R/W-1h		R/W-1h		R/W-1h		R/W-1h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1352. MII_G_RT_FT1_CFG_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-14	FT1_7CFG	R/W	1h	0h = Disabled 1h = Equal 2h = Greater Than 3h = Less Than
13-12	FT1_6CFG	R/W	1h	0h = Disabled 1h = Equal 2h = Greater Than 3h = Less Than
11-10	FT1_5CFG	R/W	1h	0h = Disabled 1h = Equal 2h = Greater Than 3h = Less Than
9-8	FT1_4CFG	R/W	1h	0h = Disabled 1h = Equal 2h = Greater Than 3h = Less Than
7-6	FT1_3CFG	R/W	1h	0h = Disabled 1h = Equal 2h = Greater Than 3h = Less Than
5-4	FT1_2CFG	R/W	1h	0h = Disabled 1h = Equal 2h = Greater Than 3h = Less Than

Table 15-1352. MII_G_RT_FT1_CFG_PRU0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	FT1_1CFG	R/W	1h	0h = Disabled 1h = Equal 2h = Greater Than 3h = Less Than
1-0	FT1_0CFG	R/W	1h	0h = Disabled 1h = Equal 2h = Greater Than 3h = Less Than

Table 15-1353. Register Call Summary for MII_G_RT_FT1_CFG_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MII_G_RT_FT1_CFG_PRU0 Register \(Offset = 84h\) \[reset = X\]: \[0\]](#)

15.12.26 MII_G_RT_FT1_k_DA0_PRU0 Register (Offset = 88h + formula) [reset = 0h]

MIIG_RT_FT1_k_DA0_PRU0 is shown in [Figure 15-444](#) and described in [Table 15-1355](#).

Return to [Summary Table](#).

Filter1<k> DA0 (Pru0).

Offset = 88h + (k * 10h); where k = 0h to 7h

Table 15-1354. MII_G_RT_FT1_k_DA0_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3088h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3088h + formula

Figure 15-444. MII_G_RT_FT1_k_DA0_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FT1_k_DA0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1355. MII_G_RT_FT1_k_DA0_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT1_k_DA0	R/W	0h	Filter1 DA4:DA1

Table 15-1356. Register Call Summary for MII_G_RT_FT1_k_DA0_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT1_k_DA0_PRU0 Register \(Offset = 88h + formula\) \[reset = 0h\]: \[0\]](#)

15.12.27 MII_G_RT_FT1_k_DA1_PRU0 Register (Offset = 8Ch + formula) [reset = X]

MIIG_RT_FT1_k_DA1_PRU0 is shown in [Figure 15-445](#) and described in [Table 15-1358](#).

Return to [Summary Table](#).

Filter1<k> DA1 (PRU0).

Offset = 8Ch + (k * 10h); where k = 0h to 7h

Table 15-1357. MII_G_RT_FT1_k_DA1_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 308Ch + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 308Ch + formula

Figure 15-445. MII_G_RT_FT1_k_DA1_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FT1_k_DA1															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1358. MII_G_RT_FT1_k_DA1_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	FT1_k_DA1	R/W	0h	Filter1 DA6:DA5

Table 15-1359. Register Call Summary for MII_G_RT_FT1_k_DA1_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT1_k_DA1_PRU0 Register \(Offset = 8Ch + formula\) \[reset = X\]: \[0\]](#)

15.12.28 MII_G_RT_FT1_k_DA_MASK0_PRU0 Register (Offset = 90h + formula) [reset = 0h]

MIIG_RT_FT1_k_DA_MASK0_PRU0 is shown in [Figure 15-446](#) and described in [Table 15-1361](#).

Return to [Summary Table](#).

Filter1<k> DA0 Mask (PRU0).

Offset = 90h + (k * 10h); where k = 0h to 7h

Table 15-1360. MII_G_RT_FT1_k_DA_MASK0_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3090h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3090h + formula

Figure 15-446. MII_G_RT_FT1_k_DA_MASK0_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FT1_k_DA_MASK0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1361. MII_G_RT_FT1_k_DA_MASK0_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT1_k_DA_MASK0	R/W	0h	Filter1 MDA4:MDA1 set to 1 to mask corresponding bit

Table 15-1362. Register Call Summary for MII_G_RT_FT1_k_DA_MASK0_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT1_k_DA_MASK0_PRU0 Register \(Offset = 90h + formula\) \[reset = 0h\]: \[0\]](#)

15.12.29 MII_G_RT_FT1_k_DA_MASK1_PRU0 Register (Offset = 94h + formula) [reset = X]

MIIG_RT_FT1_k_DA_MASK1_PRU0 is shown in [Figure 15-447](#) and described in [Table 15-1364](#).

Return to [Summary Table](#).

Filter1<k> DA1 Mask (PRU0).

Offset = 94h + (k * 10h); where k = 0h to 7h

Table 15-1363. MII_G_RT_FT1_k_DA_MASK1_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3094h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3094h + formula

Figure 15-447. MII_G_RT_FT1_k_DA_MASK1_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FT1_k_DA_MASK1															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1364. MII_G_RT_FT1_k_DA_MASK1_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	FT1_k_DA_MASK1	R/W	0h	Filter1 MDA6:MDA5 set to 1 to mask corresponding bit

Table 15-1365. Register Call Summary for MII_G_RT_FT1_k_DA_MASK1_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT1_k_DA_MASK1_PRU0 Register \(Offset = 94h + formula\) \[reset = X\]: \[0\]](#)

15.12.30 MII_G_RT_FT3_m_START_PRU0 Register (Offset = 108h + formula) [reset = X]

MIIG_RT_FT3_m_START_PRU0 is shown in [Figure 15-448](#) and described in [Table 15-1367](#).

Return to [Summary Table](#).

Filter3 Byte Count Start.

Offset = 108h + (m * 20h); where m = 0h to Fh

Table 15-1366. MII_G_RT_FT3_m_START_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3108h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3108h + formula

Figure 15-448. MII_G_RT_FT3_m_START_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FT3_START															
R/W-X																R/W-Ch															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1367. MII_G_RT_FT3_m_START_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R/W	X	
14-0	FT3_START	R/W	Ch	Byte count start for Filter3. Any write will clear all Filter3 Status Bits SW can read to determine next start during Auto

Table 15-1368. Register Call Summary for MII_G_RT_FT3_m_START_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT3_m_START_PRU0 Register \(Offset = 108h + formula\) \[reset = X\]: \[0\]](#)

15.12.31 MII_G_RT_FT3_m_START_AUTO_PRU0 Register (Offset = 10Ch + formula) [reset = X]

MIIG_RT_FT3_m_START_AUTO_PRU0 is shown in [Figure 15-449](#) and described in [Table 15-1370](#).

Return to [Summary Table](#).

Filter3 Byte Count Start for Auto Skip mode.

Offset = 10Ch + (m * 20h); where m = 0h to Fh

Table 15-1369. MII_G_RT_FT3_m_START_AUTO_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 310Ch + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 310Ch + formula

Figure 15-449. MII_G_RT_FT3_m_START_AUTO_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FT3_START_AUTO															
R-X																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 15-1370. MII_G_RT_FT3_m_START_AUTO_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	X	
14-0	FT3_START_AUTO	R	0h	Byte count start for Auto skip mode

Table 15-1371. Register Call Summary for MII_G_RT_FT3_m_START_AUTO_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT3_m_START_AUTO_PRU0 Register \(Offset = 10Ch + formula\) \[reset = X\]: \[0\]](#)

15.12.32 MII_G_RT_FT3_m_START_LEN_PRU0 Register (Offset = 110h + formula) [reset = X]

MIIG_RT_FT3_m_START_LEN_PRU0 is shown in Figure 15-450 and described in Table 15-1373.

Return to [Summary Table](#).

Filter3 Start Offset for PRU0.

Offset = 110h + (m * 20h); where m = 0h to Fh

Table 15-1372. MII_G_RT_FT3_m_START_LEN_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3110h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3110h + formula

Figure 15-450. MII_G_RT_FT3_m_START_LEN_PRU0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED	FT3_OFFSET_END			RESERVED	FT3_OFFSET_START		
R/W-X	R/W-0h			R/W-X	R/W-0h		
15	14	13	12	11	10	9	8
RESERVED	FT3_OFFSET						
R/W-X	R/W-0h						
7	6	5	4	3	2	1	0
FT3_OFFSET							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1373. MII_G_RT_FT3_m_START_LEN_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22-20	FT3_OFFSET_END	R/W	0h	Defines which byte within FT3_[N]P[63:0] to end the compare at set the Valid flag, rule ft3_offset_end >= ft3_offset_start To disable pattern compare set start and end to zero
19	RESERVED	R/W	X	
18-16	FT3_OFFSET_START	R/W	0h	Defines which byte within FT3_[N]P[63:0] to start the compare
15	RESERVED	R/W	X	
14-0	FT3_OFFSET	R/W	0h	Determine which byte to start FT3_[N]P[63:0] operation it will start on the next byte after FT3_T completes if set to zero

Table 15-1374. Register Call Summary for MII_G_RT_FT3_m_START_LEN_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT3_m_START_LEN_PRU0 Register \(Offset = 110h + formula\) \[reset = X\]: \[0\]](#)

15.12.33 MII_G_RT_FT3_m_JMP_OFFSET_PRU0 Register (Offset = 114h + formula) [reset = X]

MIIG_RT_FT3_m_JMP_OFFSET_PRU0 is shown in [Figure 15-451](#) and described in [Table 15-1376](#).

Return to [Summary Table](#).

Filter3 Jump Offset for PRU0.

Offset = 114h + (m * 20h); where m = 0h to Fh

Table 15-1375. MII_G_RT_FT3_m_JMP_OFFSET_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3114h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3114h + formula

Figure 15-451. MII_G_RT_FT3_m_JMP_OFFSET_PRU0 Register

31	30	29	28	27	26	25	24
RESERVED	FT3_m_NJMP_OFFSET_PRU0						
R/W-X	R/W-0h						
23	22	21	20	19	18	17	16
FT3_m_NJMP_OFFSET_PRU0							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED	FT3_m_IJMP_OFFSET_PRU0						
R/W-X	R/W-0h						
7	6	5	4	3	2	1	0
FT3_m_IJMP_OFFSET_PRU0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1376. MII_G_RT_FT3_m_JMP_OFFSET_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-16	FT3_m_NJMP_OFFSET_PRU0	R/W	0h	Defines the Next Offset to compare when auto arm jump is enabled
15	RESERVED	R/W	X	
14-0	FT3_m_IJMP_OFFSET_PRU0	R/W	0h	Defines the Initial Offset to compare when auto arm jump is enabled

Table 15-1377. Register Call Summary for MII_G_RT_FT3_m_JMP_OFFSET_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT3_m_JMP_OFFSET_PRU0 Register \(Offset = 114h + formula\) \[reset = X\]: \[0\]](#)

15.12.34 MII_G_RT_FT3_m_LEN_PRU0 Register (Offset = 118h + formula) [reset = X]

MIIG_RT_FT3_m_LEN_PRU0 is shown in [Figure 15-452](#) and described in [Table 15-1379](#).

Return to [Summary Table](#).

Filter3 Length Offset for PRU0.

Offset = 118h + (m * 20h); where m = 0h to Fh

Table 15-1378. MII_G_RT_FT3_m_LEN_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3118h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3118h + formula

Figure 15-452. MII_G_RT_FT3_m_LEN_PRU0 Register

31	30	29	28	27	26	25	24
RESERVED							FT3_m_LEN_BIG_EN_PRU0
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED				FT3_m_LEN_SIZE_BIT_PRU0			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED							FT3_m_LEN_START_BIT_PRU0
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
FT3_m_LEN_START_BIT_PRU0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1379. MII_G_RT_FT3_m_LEN_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	FT3_m_LEN_BIG_EN_PRU0	R/W	0h	Enable Big Indian on Length
23-20	RESERVED	R/W	X	
19-16	FT3_m_LEN_SIZE_BIT_PRU0	R/W	0h	Defines number of bits to extract the length for the auto skip function
15-9	RESERVED	R/W	X	
8-0	FT3_m_LEN_START_BIT_PRU0	R/W	0h	Defines relative bit offset from the HIT byte location upto 512 bit offset the extraction to determine the on the fly length byte offset

Table 15-1380. Register Call Summary for MII_G_RT_FT3_m_LEN_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT3_m_LEN_PRU0 Register \(Offset = 118h + formula\) \[reset = X\]: \[0\]](#)

15.12.35 MII_G_RT_FT3_m_CFG_PRU0 Register (Offset = 11Ch + formula) [reset = X]

MIIG_RT_FT3_m_CFG_PRU0 is shown in Figure 15-453 and described in Table 15-1382.

Return to [Summary Table](#).

Filter3 Configuration for PRU0.

Offset = 11Ch + (m * 20h); where m = 0h to Fh

Table 15-1381. MII_G_RT_FT3_m_CFG_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 311Ch + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 311Ch + formula

Figure 15-453. MII_G_RT_FT3_m_CFG_PRU0 Register

31	30	29	28	27	26	25	24
FT3_m_TRIG_OR_EN							
R/W-0h							
23	22	21	20	19	18	17	16
FT3_m_TRIG_OR_EN							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED					FT3_m_VLAN_SKIP_EN	FT3_mCFG	
R/W-X					R/W-1h	R/W-1h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1382. MII_G_RT_FT3_m_CFG_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	FT3_m_TRIG_OR_EN	R/W	0h	Trigger ft3 select for auto skip enable, if one or more set the function is enabled note you can not select the same ft3 only others
15-3	RESERVED	R/W	X	
2	FT3_m_VLAN_SKIP_EN	R/W	1h	0: Disabled 1: Enable
1-0	FT3_mCFG	R/W	1h	0: Disabled 1: EQ 2: GT 3: LT

Table 15-1383. Register Call Summary for MII_G_RT_FT3_m_CFG_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT3_m_CFG_PRU0 Register \(Offset = 11Ch + formula\) \[reset = X\]: \[0\]](#)

15.12.36 MII_G_RT_FT3_m_T_PRU0 Register (Offset = 120h + formula) [reset = 0h]

MIIG_RT_FT3_m_T_PRU0 is shown in [Figure 15-454](#) and described in [Table 15-1385](#).

Return to [Summary Table](#).

Filter3 Type for PRU0.

Offset = 120h + (m * 20h); where m = 0h to Fh

Table 15-1384. MII_G_RT_FT3_m_T_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3120h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3120h + formula

Figure 15-454. MII_G_RT_FT3_m_T_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FT3_m_T																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1385. MII_G_RT_FT3_m_T_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT3_m_T	R/W	0h	Filter3 T4:T1 Note if Auto Skip is enabled then Type filter is not enabled

Table 15-1386. Register Call Summary for MII_G_RT_FT3_m_T_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT3_m_T_PRU0 Register \(Offset = 120h + formula\) \[reset = 0h\]: \[0\]](#)

15.12.37 MII_G_RT_FT3_m_T_MASK_PRU0 Register (Offset = 124h + formula) [reset = 0h]

MIIG_RT_FT3_m_T_MASK_PRU0 is shown in [Figure 15-455](#) and described in [Table 15-1388](#).

Return to [Summary Table](#).

Filter3 Mask for PRU0.

Offset = 124h + (m * 20h); where m = 0h to Fh

Table 15-1387. MII_G_RT_FT3_m_T_MASK_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3124h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3124h + formula

Figure 15-455. MII_G_RT_FT3_m_T_MASK_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FT3_m_T_MASK																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1388. MII_G_RT_FT3_m_T_MASK_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT3_m_T_MASK	R/W	0h	Filter3 MT4:MT1 Note: if Auto Skip is enabled then Type filter is not enabled set to 1 to mask corresponding bit

Table 15-1389. Register Call Summary for MII_G_RT_FT3_m_T_MASK_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT3_m_T_MASK_PRU0 Register \(Offset = 124h + formula\) \[reset = 0h\]: \[0\]](#)

15.12.38 MII_G_RT_FT3_m_P0_PRU0 Register (Offset = 308h + formula) [reset = 0h]

MIIG_RT_FT3_m_P0_PRU0 is shown in Figure 15-456 and described in Table 15-1391.

Return to [Summary Table](#).

Filter3 PRU0 (P4:P1).

Offset = 308h + (m * 10h); where m = 0h to Fh

Table 15-1390. MII_G_RT_FT3_m_P0_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3308h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3308h + formula

Figure 15-456. MII_G_RT_FT3_m_P0_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FT3_m_P0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1391. MII_G_RT_FT3_m_P0_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT3_m_P0	R/W	0h	Filter3 P4:P1

Table 15-1392. Register Call Summary for MII_G_RT_FT3_m_P0_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT3_m_P0_PRU0 Register \(Offset = 308h + formula\) \[reset = 0h\]: \[0\]](#)

15.12.39 MII_G_RT_FT3_m_P1_PRU0 Register (Offset = 30Ch + formula) [reset = 0h]

MIIG_RT_FT3_m_P1_PRU0 is shown in [Figure 15-457](#) and described in [Table 15-1394](#).

Return to [Summary Table](#).

Filter3 PRU0 (P8:P5).

Offset = 30Ch + (m * 10h); where m = 0h to Fh

Table 15-1393. MII_G_RT_FT3_m_P1_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 330Ch + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 330Ch + formula

Figure 15-457. MII_G_RT_FT3_m_P1_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FT3_m_P1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1394. MII_G_RT_FT3_m_P1_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT3_m_P1	R/W	0h	Filter3 P8:P5

Table 15-1395. Register Call Summary for MII_G_RT_FT3_m_P1_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT3_m_P1_PRU0 Register \(Offset = 30Ch + formula\) \[reset = 0h\]: \[0\]](#)

15.12.40 MII_G_RT_FT3_n_P_MASK0_PRU0 Register (Offset = 310h + formula) [reset = 0h]

MIIG_RT_FT3_n_P_MASK0_PRU0 is shown in [Figure 15-458](#) and described in [Table 15-1397](#).

Return to [Summary Table](#).

Filter3 Mask0 (MP4:MP1).

Offset = 310h + (n * 10h); where n = 0h to Fh

Table 15-1396. MII_G_RT_FT3_n_P_MASK0_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3310h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3310h + formula

Figure 15-458. MII_G_RT_FT3_n_P_MASK0_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FT3_n_P_MASK0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1397. MII_G_RT_FT3_n_P_MASK0_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT3_n_P_MASK0	R/W	0h	Filter3 MP4:MP1 set to 1 to mask corresponding bit

Table 15-1398. Register Call Summary for MII_G_RT_FT3_n_P_MASK0_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT3_n_P_MASK0_PRU0 Register \(Offset = 310h + formula\) \[reset = 0h\]: \[0\]](#)

15.12.41 MII_G_RT_FT3_n_P_MASK1_PRU0 Register (Offset = 314h + formula) [reset = 0h]

MIIG_RT_FT3_n_P_MASK1_PRU0 is shown in [Figure 15-459](#) and described in [Table 15-1400](#).

Return to [Summary Table](#).

Filter3 Mask1 (MP8:MP5).

Offset = 314h + (n * 10h); where n = 0h to Fh

Table 15-1399. MII_G_RT_FT3_n_P_MASK1_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3314h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3314h + formula

Figure 15-459. MII_G_RT_FT3_n_P_MASK1_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FT3_n_P_MASK1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1400. MII_G_RT_FT3_n_P_MASK1_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT3_n_P_MASK1	R/W	0h	Filter3 MP8:MP5 set to 1 to mask corresponding bit

Table 15-1401. Register Call Summary for MII_G_RT_FT3_n_P_MASK1_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT3_n_P_MASK1_PRU0 Register \(Offset = 314h + formula\) \[reset = 0h\]: \[0\]](#)

15.12.42 MII_G_RT_FT_RX_PTR_PRU0 Register (Offset = 408h) [reset = 0h]

MIIG_RT_FT_RX_PTR_PRU0 is shown in [Figure 15-460](#) and described in [Table 15-1403](#).

Return to [Summary Table](#).

RX Current Filter Byte Count (PRU0).

Table 15-1402. MII_G_RT_FT_RX_PTR_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3408h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3408h

Figure 15-460. MII_G_RT_FT_RX_PTR_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FT_RX_PTR_PRU0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1403. MII_G_RT_FT_RX_PTR_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT_RX_PTR_PRU0	R/W	0h	RX current filter Byte Count

Table 15-1404. Register Call Summary for MII_G_RT_FT_RX_PTR_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT_RX_PTR_PRU0 Register \(Offset = 408h\) \[reset = 0h\]: \[0\]](#)

15.12.43 MII_G_RT_RX_CLASSm_AND_EN_PRU0 Register (Offset = 40Ch + formula) [reset = 0h]

MIIG_RT_RX_CLASSm_AND_EN_PRU0 is shown in [Figure 15-461](#) and described in [Table 15-1406](#).

Return to [Summary Table](#).

RX Class<m> AND Enable Register.

Offset = 40Ch + (m * 8h); where m = 0h to Fh

Table 15-1405. MII_G_RT_RX_CLASSm_AND_EN_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 340Ch + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 340Ch + formula

Figure 15-461. MII_G_RT_RX_CLASSm_AND_EN_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_CLASSm_AND_EN																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1406. MII_G_RT_RX_CLASSm_AND_EN_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RX_CLASSm_AND_EN	R/W	0h	rx class AND enable

Table 15-1407. Register Call Summary for MII_G_RT_RX_CLASSm_AND_EN_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_CLASSm_AND_EN_PRU0 Register \(Offset = 40Ch + formula\) \[reset = 0h\]: \[0\]](#)

15.12.44 MII_G_RT_RX_CLASSm_OR_EN_PRU0 Register (Offset = 410h + formula) [reset = 0h]

MIIG_RT_RX_CLASSm_OR_EN_PRU0 is shown in [Figure 15-462](#) and described in [Table 15-1409](#).

Return to [Summary Table](#).

RX Class<m> OR Enable Register.

Offset = 410h + (m * 8h); where m = 0h to Fh

Table 15-1408. MII_G_RT_RX_CLASSm_OR_EN_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3410h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3410h + formula

Figure 15-462. MII_G_RT_RX_CLASSm_OR_EN_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_CLASSm_OR_EN																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1409. MII_G_RT_RX_CLASSm_OR_EN_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RX_CLASSm_OR_EN	R/W	0h	rx class OR enable

Table 15-1410. Register Call Summary for MII_G_RT_RX_CLASSm_OR_EN_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_CLASSm_OR_EN_PRU0 Register \(Offset = 410h + formula\) \[reset = 0h\]: \[0\]](#)

15.12.45 MII_G_RT_RX_CLASS_CFG1_PRU0 Register (Offset = 48Ch) [reset = 0h]

MIIG_RT_RX_CLASS_CFG1_PRU0 is shown in Figure 15-463 and described in Table 15-1412.

Return to [Summary Table](#).

RX Class Configuration 1 Register.

Table 15-1411. MII_G_RT_RX_CLASS_CFG1_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 348Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 348Ch

Figure 15-463. MII_G_RT_RX_CLASS_CFG1_PRU0 Register

31	30	29	28	27	26	25	24
RX_CLASS15_SEL		RX_CLASS14_SEL		RX_CLASS13_SEL		RX_CLASS12_SEL	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
23	22	21	20	19	18	17	16
RX_CLASS11_SEL		RX_CLASS10_SEL		RX_CLASS9_SEL		RX_CLASS8_SEL	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8
RX_CLASS7_SEL		RX_CLASS6_SEL		RX_CLASS5_SEL		RX_CLASS4_SEL	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
RX_CLASS3_SEL		RX_CLASS2_SEL		RX_CLASS1_SEL		RX_CLASS0_SEL	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1412. MII_G_RT_RX_CLASS_CFG1_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RX_CLASS15_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
29-28	RX_CLASS14_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
27-26	RX_CLASS13_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
25-24	RX_CLASS12_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
23-22	RX_CLASS11_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND

Table 15-1412. MII_G_RT_RX_CLASS_CFG1_PRU0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	RX_CLASS10_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
19-18	RX_CLASS9_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
17-16	RX_CLASS8_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
15-14	RX_CLASS7_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
13-12	RX_CLASS6_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
11-10	RX_CLASS5_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
9-8	RX_CLASS4_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
7-6	RX_CLASS3_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
5-4	RX_CLASS2_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
3-2	RX_CLASS1_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
1-0	RX_CLASS0_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND

Table 15-1413. Register Call Summary for MII_G_RT_RX_CLASS_CFG1_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MII_G_RT_RX_CLASS_CFG1_PRU0 Register \(Offset = 48Ch\) \[reset = 0h\]: \[0\]](#)

15.12.46 MII_G_RT_RX_CLASS_CFG2_PRU0 Register (Offset = 490h) [reset = 0h]

MIIG_RT_RX_CLASS_CFG2_PRU0 is shown in [Figure 15-464](#) and described in [Table 15-1415](#).

Return to [Summary Table](#).

RX Class Configuration 2 Register.

Table 15-1414. MII_G_RT_RX_CLASS_CFG2_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3490h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3490h

Figure 15-464. MII_G_RT_RX_CLASS_CFG2_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_CLASS_OR_NV																RX_CLASS_AND_NV															
R/W-0h																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1415. MII_G_RT_RX_CLASS_CFG2_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_CLASS_OR_NV	R/W	0h	RX class invert OR not invert enable
15-0	RX_CLASS_AND_NV	R/W	0h	RX class invert AND not invert enable

Table 15-1416. Register Call Summary for MII_G_RT_RX_CLASS_CFG2_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_CLASS_CFG2_PRU0 Register \(Offset = 490h\) \[reset = 0h\]: \[0\]](#)

15.12.47 MII_G_RT_RX_CLASS_GATESm_PRU0 Register (Offset = 494h + formula) [reset = X]

MIIG_RT_RX_CLASS_GATESm_PRU0 is shown in Figure 15-465 and described in Table 15-1418.

Return to [Summary Table](#).

RX Class Gate<m> Configuration PRU0 Register.

Offset = 494h + (m * 4h); where m = 0h to Fh

Table 15-1417. MII_G_RT_RX_CLASS_GATESm_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3494h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3494h + formula

Figure 15-465. MII_G_RT_RX_CLASS_GATESm_PRU0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							RX_RED_PHASE_ENm
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED	RX_ALLOW_MASKm	RX_CLASS_RAW_MASKm	RX_PHASE_MASKm	RESERVED	RX_RATE_GATE_SELm		
R/W-X	R/W-1h	R/W-1h	R/W-1h	R/W-X	R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1418. MII_G_RT_RX_CLASS_GATESm_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	RX_RED_PHASE_ENm	R/W	0h	red phase enable 0: disable 1: enable
7	RESERVED	R/W	X	
6	RX_ALLOW_MASKm	R/W	1h	allow mask 0: unmask 1: mask
5	RX_CLASS_RAW_MASKm	R/W	1h	class raw mask 0: unmask 1: mask
4	RX_PHASE_MASKm	R/W	1h	time phase mask 0: unmask 1: mask
3	RESERVED	R/W	X	
2-0	RX_RATE_GATE_SELm	R/W	0h	defines which rx_rate will gate rx_class

Table 15-1419. Register Call Summary for MII_G_RT_RX_CLASS_GATESm_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_CLASS_GATESm_PRU0 Register \(Offset = 494h + formula\) \[reset = X\]: \[0\]](#)

15.12.48 MII_G_RT_RX_GREEN_PRU0 Register (Offset = 4D4h) [reset = X]

MIIG_RT_RX_GREEN_PRU0 is shown in [Figure 15-466](#) and described in [Table 15-1421](#).

Return to [Summary Table](#).

RX Green Status PRU0.

Table 15-1420. MII_G_RT_RX_GREEN_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 34D4h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 34D4h

Figure 15-466. MII_G_RT_RX_GREEN_PRU0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED			RX_GREEN_VAL	RX_GREEN_CMP_SEL			
R/W-X			R-0h	R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-1421. MII_G_RT_RX_GREEN_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R/W	X	
4	RX_GREEN_VAL	R	0h	0: RED, 1: GREEN status
3-0	RX_GREEN_CMP_SEL	R/W	0h	define which IEP CMP start green

Table 15-1422. Register Call Summary for MII_G_RT_RX_GREEN_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_GREEN_PRU0 Register \(Offset = 4D4h\) \[reset = X\]: \[0\]](#)

15.12.49 MII_G_RT_SA_HASH_PRU0 Register (Offset = 4D8h) [reset = X]

MIIG_RT_SA_HASH_PRU0 is shown in Figure 15-467 and described in Table 15-1424.

Return to [Summary Table](#).

SA Hash Seed PRU0.

Table 15-1423. MII_G_RT_SA_HASH_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 34D8h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 34D8h

Figure 15-467. MII_G_RT_SA_HASH_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SA_HASH_SEED							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1424. MII_G_RT_SA_HASH_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	SA_HASH_SEED	R/W	0h	SA Hash Seed

Table 15-1425. Register Call Summary for MII_G_RT_SA_HASH_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_SA_HASH_PRU0 Register \(Offset = 4D8h\) \[reset = X\]: \[0\]](#)

15.12.50 MII_G_RT_CONN_HASH_PRU0 Register (Offset = 4DCh) [reset = X]

MIIG_RT_CONN_HASH_PRU0 is shown in [Figure 15-468](#) and described in [Table 15-1427](#).

Return to [Summary Table](#).

Connection Hash Seed PRU0.

Table 15-1426. MII_G_RT_CONN_HASH_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 34DCh
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 34DCh

Figure 15-468. MII_G_RT_CONN_HASH_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						CONN_HASH_SEED									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1427. MII_G_RT_CONN_HASH_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	CONN_HASH_SEED	R/W	0h	Connection Hash Seed

Table 15-1428. Register Call Summary for MII_G_RT_CONN_HASH_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_CONN_HASH_PRU0 Register \(Offset = 4DCh\) \[reset = X\]: \[0\]](#)

15.12.51 MII_G_RT_CONN_HASH_START_PRU0 Register (Offset = 4E0h) [reset = X]

MIIG_RT_CONN_HASH_START_PRU0 is shown in Figure 15-469 and described in Table 15-1430.

Return to [Summary Table](#).

Connection Hash Start PRU0.

Table 15-1429. MII_G_RT_CONN_HASH_START_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 34E0h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 34E0h

Figure 15-469. MII_G_RT_CONN_HASH_START_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CONN_HASH_START															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1430. MII_G_RT_CONN_HASH_START_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R/W	X	
14-0	CONN_HASH_START	R/W	0h	Connection Hash Start which 4 Bytes to hash

Table 15-1431. Register Call Summary for MII_G_RT_CONN_HASH_START_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_CONN_HASH_START_PRU0 Register \(Offset = 4E0h\) \[reset = X\]: \[0\]](#)

15.12.52 MII_G_RT_RX_RATE_CFGn_PRU0 Register (Offset = 4E4h + formula) [reset = 0h]

MIIG_RT_RX_RATE_CFGn_PRU0 is shown in [Figure 15-470](#) and described in [Table 15-1433](#).

Return to [Summary Table](#).

RX Rate Configuration<n> Register.

Offset = 4E4h + (n * 4h); where n = 0h to 7h

Table 15-1432. MII_G_RT_RX_RATE_CFGn_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 34E4h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 34E4h + formula

Figure 15-470. MII_G_RT_RX_RATE_CFGn_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_RATE_CIR_IDLEn																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1433. MII_G_RT_RX_RATE_CFGn_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RX_RATE_CIR_IDLEn	R/W	0h	RX Rate Peak Information Rate Idle Increment Value - The number added to the PIR counter every clock cycle including EOF. The PIR counter is disabled with a zero value and packets will not be marked RED

Table 15-1434. Register Call Summary for MII_G_RT_RX_RATE_CFGn_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_RATE_CFGn_PRU0 Register \(Offset = 4E4h + formula\) \[reset = 0h\]: \[0\]](#)

15.12.53 MII_G_RT_RX_RATE_SRC_SEL0_PRU0 Register (Offset = 504h) [reset = X]

MIIG_RT_RX_RATE_SRC_SEL0_PRU0 is shown in Figure 15-471 and described in Table 15-1436.

Return to [Summary Table](#).

RX Rate Source Select0.

Table 15-1435. MII_G_RT_RX_RATE_SRC_SEL0_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3504h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3504h

Figure 15-471. MII_G_RT_RX_RATE_SRC_SEL0_PRU0 Register

31	30	29	28	27	26	25	24
RESERVED				RX_RATE_SRC_SEL3			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				RX_RATE_SRC_SEL2			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				RX_RATE_SRC_SEL1			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				RX_RATE_SRC_SEL0			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1436. MII_G_RT_RX_RATE_SRC_SEL0_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	RX_RATE_SRC_SEL3	R/W	0h	Map which filter/flag/class hit that rate logic uses, see RX Rate hit Mapping table for mapping
23-22	RESERVED	R/W	X	
21-16	RX_RATE_SRC_SEL2	R/W	0h	Map which filter/flag/class hit that rate logic uses, see RX Rate hit Mapping table for mapping
15-14	RESERVED	R/W	X	
13-8	RX_RATE_SRC_SEL1	R/W	0h	Map which filter/flag/class hit that rate logic uses, see RX Rate hit Mapping table for mapping
7-6	RESERVED	R/W	X	
5-0	RX_RATE_SRC_SEL0	R/W	0h	Map which filter/flag/class hit that rate logic uses, see RX Rate hit Mapping table for mapping

Table 15-1437. Register Call Summary for MII_G_RT_RX_RATE_SRC_SEL0_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_RATE_SRC_SEL0_PRU0 Register \(Offset = 504h\) \[reset = X\]: \[0\]](#)

15.12.54 MII_G_RT_RX_RATE_SRC_SEL1_PRU0 Register (Offset = 508h) [reset = X]

MIIG_RT_RX_RATE_SRC_SEL1_PRU0 is shown in Figure 15-472 and described in Table 15-1439.

Return to [Summary Table](#).

RX Rate Source Select1.

Table 15-1438. MII_G_RT_RX_RATE_SRC_SEL1_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3508h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3508h

Figure 15-472. MII_G_RT_RX_RATE_SRC_SEL1_PRU0 Register

31	30	29	28	27	26	25	24
RESERVED				RX_RATE_SRC_SEL7			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				RX_RATE_SRC_SEL6			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				RX_RATE_SRC_SEL5			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				RX_RATE_SRC_SEL4			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1439. MII_G_RT_RX_RATE_SRC_SEL1_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	RX_RATE_SRC_SEL7	R/W	0h	Map which filter/flag/class hit that rate logic uses, see RX Rate hit Mapping table for mapping
23-22	RESERVED	R/W	X	
21-16	RX_RATE_SRC_SEL6	R/W	0h	Map which filter/flag/class hit that rate logic uses, see RX Rate hit Mapping table for mapping
15-14	RESERVED	R/W	X	
13-8	RX_RATE_SRC_SEL5	R/W	0h	Map which filter/flag/class hit that rate logic uses, see RX Rate hit Mapping table for mapping
7-6	RESERVED	R/W	X	
5-0	RX_RATE_SRC_SEL4	R/W	0h	Map which filter/flag/class hit that rate logic uses, see RX Rate hit Mapping table for mapping

Table 15-1440. Register Call Summary for MII_G_RT_RX_RATE_SRC_SEL1_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_RATE_SRC_SEL1_PRU0 Register \(Offset = 508h\) \[reset = X\]: \[0\]](#)

15.12.55 MII_G_RT_TX_RATE_CFG1_n_PRU0 Register (Offset = 50Ch + formula) [reset = 0h]

MIIG_RT_TX_RATE_CFG1_n_PRU0 is shown in [Figure 15-473](#) and described in [Table 15-1442](#).

Return to [Summary Table](#).

TX Rate Configuration1 Register.

Offset = 50Ch + (n * 8h); where n = 0h to 7h

Table 15-1441. MII_G_RT_TX_RATE_CFG1_n_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 350Ch + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 350Ch + formula

Figure 15-473. MII_G_RT_TX_RATE_CFG1_n_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_RATE_CIR_IDLEn																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1442. MII_G_RT_TX_RATE_CFG1_n_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TX_RATE_CIR_IDLEn	R/W	0h	TX Rate Peak Information Rate Idle Increment Value - The number added to the PIR counter every clock cycle including EOF. The PIR counter is disabled with a zero value and packets will not be marked RED

Table 15-1443. Register Call Summary for MII_G_RT_TX_RATE_CFG1_n_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_RATE_CFG1_n_PRU0 Register \(Offset = 50Ch + formula\) \[reset = 0h\]: \[0\]](#)

15.12.56 MII_G_RT_TX_RATE_CFG2_n_PRU0 Register (Offset = 510h + formula) [reset = X]

MIIG_RT_TX_RATE_CFG2_n_PRU0 is shown in Figure 15-474 and described in Table 15-1445.

Return to [Summary Table](#).

TX Rate Configuration2 Register.

Offset = 510h + (n * 8h); where n = 0h to 7h

Table 15-1444. MII_G_RT_TX_RATE_CFG2_n_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3510h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3510h + formula

Figure 15-474. MII_G_RT_TX_RATE_CFG2_n_PRU0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						TX_RATE_ALL OWN	TX_RATE_ENn
R/W-X						R-0h	R/W-0h
15	14	13	12	11	10	9	8
TX_RATE_LENn							
R/W-0h							
7	6	5	4	3	2	1	0
TX_RATE_LENn							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-1445. MII_G_RT_TX_RATE_CFG2_n_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17	TX_RATE_ALLOWn	R	0h	TX Rate Pkt Enable
16	TX_RATE_ENn	R/W	0h	TX Rate Pkt Enable
15-0	TX_RATE_LENn	R/W	0h	TX Rate Pkt Length

Table 15-1446. Register Call Summary for MII_G_RT_TX_RATE_CFG2_n_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_RATE_CFG2_n_PRU0 Register \(Offset = 510h + formula\) \[reset = X\]: \[0\]](#)

15.12.57 MII_G_RT_RX_STAT_GOOD_PRU0 Register (Offset = 54Ch + formula) [reset = 0h]

MIIG_RT_RX_STAT_GOOD_PRU0 is shown in [Figure 15-475](#) and described in [Table 15-1448](#).

Return to [Summary Table](#).

RX Good Frame Count (PRU0).

Table 15-1447. MII_G_RT_RX_STAT_GOOD_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 354Ch + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 354Ch + formula

Figure 15-475. MII_G_RT_RX_STAT_GOOD_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_GOOD_FRM_CNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1448. MII_G_RT_RX_STAT_GOOD_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RX_GOOD_FRM_CNT	R/W	0h	RX Good Frame Count Increment on none min err max err CRC err odd err, Write to subtract

Table 15-1449. Register Call Summary for MII_G_RT_RX_STAT_GOOD_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_GOOD_PRU0 Register \(Offset = 54Ch + formula\) \[reset = 0h\]: \[0\]](#)

15.12.58 MII_G_RT_RX_STAT_BC_PRU0 Register (Offset = 550h) [reset = X]

MIIG_RT_RX_STAT_BC_PRU0 is shown in [Figure 15-476](#) and described in [Table 15-1451](#).

Return to [Summary Table](#).

RX BC Frame Count (PRU0).

Table 15-1450. MII_G_RT_RX_STAT_BC_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3550h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3550h

Figure 15-476. MII_G_RT_RX_STAT_BC_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RX_BC_FRM_CNT															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1451. MII_G_RT_RX_STAT_BC_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_BC_FRM_CNT	R/W	0h	RX BC Frame Count Increment on BC type, Write to subtract

Table 15-1452. Register Call Summary for MII_G_RT_RX_STAT_BC_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_BC_PRU0 Register \(Offset = 550h\) \[reset = X\]: \[0\]](#)

15.12.59 MII_G_RT_RX_STAT_MC_PRU0 Register (Offset = 554h) [reset = X]

MIIG_RT_RX_STAT_MC_PRU0 is shown in [Figure 15-477](#) and described in [Table 15-1454](#).

Return to [Summary Table](#).

RX MC Frame Count (PRU0).

Table 15-1453. MII_G_RT_RX_STAT_MC_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3554h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3554h

Figure 15-477. MII_G_RT_RX_STAT_MC_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RX_MC_FRM_CNT															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1454. MII_G_RT_RX_STAT_MC_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_MC_FRM_CNT	R/W	0h	RX MC Frame Count Increment on MC type, Write to subtract

Table 15-1455. Register Call Summary for MII_G_RT_RX_STAT_MC_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_MC_PRU0 Register \(Offset = 554h\) \[reset = X\]: \[0\]](#)

15.12.60 MII_G_RT_RX_STAT_CRC_ERR_PRU0 Register (Offset = 558h) [reset = X]

MIIG_RT_RX_STAT_CRC_ERR_PRU0 is shown in [Figure 15-478](#) and described in [Table 15-1457](#).

Return to [Summary Table](#).

RX CRC Error Frame Count (PRU0).

Table 15-1456. MII_G_RT_RX_STAT_CRC_ERR_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3558h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3558h

Figure 15-478. MII_G_RT_RX_STAT_CRC_ERR_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_CRC_ERR_FRM_CNT															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1457. MII_G_RT_RX_STAT_CRC_ERR_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_CRC_ERR_FRM_CNT	R/W	0h	RX CRC Err Frame Count Increment on CRC error, Write to subtract

Table 15-1458. Register Call Summary for MII_G_RT_RX_STAT_CRC_ERR_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_CRC_ERR_PRU0 Register \(Offset = 558h\) \[reset = X\]: \[0\]](#)

15.12.61 MII_G_RT_RX_STAT_MII_ERR_PRU0 Register (Offset = 55Ch) [reset = X]

MIIG_RT_RX_STAT_MII_ERR_PRU0 is shown in Figure 15-479 and described in Table 15-1460.

Return to [Summary Table](#).

RX MII Error Frame Count (PRU0).

Table 15-1459. MII_G_RT_RX_STAT_MII_ERR_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 355Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 355Ch

Figure 15-479. MII_G_RT_RX_STAT_MII_ERR_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_MII_ERR_FRM_CNT															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1460. MII_G_RT_RX_STAT_MII_ERR_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_MII_ERR_FRM_CNT	R/W	0h	RX MII Err Frame Count Increment on MII, SGMII, RGMII error, Write to subtract

Table 15-1461. Register Call Summary for MII_G_RT_RX_STAT_MII_ERR_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_MII_ERR_PRU0 Register \(Offset = 55Ch\) \[reset = X\]: \[0\]](#)

15.12.62 MII_G_RT_RX_STAT_ODD_ERR_PRU0 Register (Offset = 560h) [reset = X]

MIIG_RT_RX_STAT_ODD_ERR_PRU0 is shown in [Figure 15-480](#) and described in [Table 15-1463](#).

Return to [Summary Table](#).

RX Odd Nibble Frame Count (PRU0).

Table 15-1462. MII_G_RT_RX_STAT_ODD_ERR_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3560h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3560h

Figure 15-480. MII_G_RT_RX_STAT_ODD_ERR_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_ODD_ERR_FRM_CNT															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1463. MII_G_RT_RX_STAT_ODD_ERR_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_ODD_ERR_FRM_CNT	R/W	0h	RX Odd Nibble Frame Count Increment on odd nibble MII, Write to subtract

Table 15-1464. Register Call Summary for MII_G_RT_RX_STAT_ODD_ERR_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_ODD_ERR_PRU0 Register \(Offset = 560h\) \[reset = X\]: \[0\]](#)

15.12.63 MII_G_RT_RX_STAT_MAX_SIZE_PRU0 Register (Offset = 564h) [reset = X]

MIIG_RT_RX_STAT_MAX_SIZE_PRU0 is shown in [Figure 15-481](#) and described in [Table 15-1466](#).

Return to [Summary Table](#).

RX Max Size Frame Count (PRU0).

Table 15-1465. MII_G_RT_RX_STAT_MAX_SIZE_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3564h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3564h

Figure 15-481. MII_G_RT_RX_STAT_MAX_SIZE_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RX_MAX_SIZE_FRM															
R/W-X																R/W-7D0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1466. MII_G_RT_RX_STAT_MAX_SIZE_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_MAX_SIZE_FRM	R/W	7D0h	RX MAX Size Frame Count Limit

Table 15-1467. Register Call Summary for MII_G_RT_RX_STAT_MAX_SIZE_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_MAX_SIZE_PRU0 Register \(Offset = 564h\) \[reset = X\]: \[0\]](#)

15.12.64 MII_G_RT_RX_STAT_MAX_ERR_PRU0 Register (Offset = 568h) [reset = X]

MIIG_RT_RX_STAT_MAX_ERR_PRU0 is shown in [Figure 15-482](#) and described in [Table 15-1469](#).

Return to [Summary Table](#).

RX Max Size Error Frame Count (PRU0).

Table 15-1468. MII_G_RT_RX_STAT_MAX_ERR_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3568h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3568h

Figure 15-482. MII_G_RT_RX_STAT_MAX_ERR_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_MAX_ERR_FRM_CNT															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1469. MII_G_RT_RX_STAT_MAX_ERR_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_MAX_ERR_FRM_CNT	R/W	0h	RX MAX Size Err Frame Count Increment if > than Limit, Write to subtract

Table 15-1470. Register Call Summary for MII_G_RT_RX_STAT_MAX_ERR_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_MAX_ERR_PRU0 Register \(Offset = 568h\) \[reset = X\]: \[0\]](#)

15.12.65 MII_G_RT_RX_STAT_MIN_SIZE_PRU0 Register (Offset = 56Ch) [reset = X]

MIIG_RT_RX_STAT_MIN_SIZE_PRU0 is shown in Figure 15-483 and described in Table 15-1472.

Return to [Summary Table](#).

RX Min Size Frame Count (PRU0).

Table 15-1471. MII_G_RT_RX_STAT_MIN_SIZE_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 356Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 356Ch

Figure 15-483. MII_G_RT_RX_STAT_MIN_SIZE_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RX_MIN_SIZE_FRM															
R/W-X																R/W-40h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1472. MII_G_RT_RX_STAT_MIN_SIZE_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_MIN_SIZE_FRM	R/W	40h	RX MIN Size Frame Limit

Table 15-1473. Register Call Summary for MII_G_RT_RX_STAT_MIN_SIZE_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_MIN_SIZE_PRU0 Register \(Offset = 56Ch\) \[reset = X\]: \[0\]](#)

15.12.66 MII_G_RT_RX_STAT_MIN_ERR_PRU0 Register (Offset = 570h) [reset = X]

MIIG_RT_RX_STAT_MIN_ERR_PRU0 is shown in [Figure 15-484](#) and described in [Table 15-1475](#).

Return to [Summary Table](#).

RX Min Size Error Frame Count (PRU0).

Table 15-1474. MII_G_RT_RX_STAT_MIN_ERR_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3570h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3570h

Figure 15-484. MII_G_RT_RX_STAT_MIN_ERR_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_MIN_ERR_FRM_CNT															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1475. MII_G_RT_RX_STAT_MIN_ERR_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_MIN_ERR_FRM_CNT	R/W	0h	RX MIN Size Frame Count Increment if < than limit, Write to subtract

Table 15-1476. Register Call Summary for MII_G_RT_RX_STAT_MIN_ERR_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_MIN_ERR_PRU0 Register \(Offset = 570h\) \[reset = X\]: \[0\]](#)

15.12.67 MII_G_RT_RX_STAT_OVERRUN_ERR_PRU0 Register (Offset = 574h) [reset = X]

MIIG_RT_RX_STAT_OVERRUN_ERR_PRU0 is shown in Figure 15-485 and described in Table 15-1478.

Return to [Summary Table](#).

RX Overrun Frame Count (PRU0).

Table 15-1477. MII_G_RT_RX_STAT_OVERRUN_ERR_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3574h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3574h

Figure 15-485. MII_G_RT_RX_STAT_OVERRUN_ERR_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_OVERRUN_ERR_FRM_CNT															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1478. MII_G_RT_RX_STAT_OVERRUN_ERR_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_OVERRUN_ERR_FRM_CNT	R/W	0h	RX L1 FIFO overflow Frame Count. Increment on overflow event, Write to subtract

Table 15-1479. Register Call Summary for MII_G_RT_RX_STAT_OVERRUN_ERR_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_OVERRUN_ERR_PRU0 Register \(Offset = 574h\) \[reset = X\]: \[0\]](#)

15.12.68 MII_G_RT_RX_STAT_CLASSm_HIT_PRU0 Register (Offset = 578h + formula) [reset = 0h]

MIIG_RT_RX_STAT_CLASSm_HIT_PRU0 is shown in [Figure 15-486](#) and described in [Table 15-1481](#).

Return to [Summary Table](#).

RX Class<m> Hit.

Offset = 578h + (n * 4h); where m = 0h to Fh

Table 15-1480. MII_G_RT_RX_STAT_CLASSm_HIT_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3578h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3578h + formula

Figure 15-486. MII_G_RT_RX_STAT_CLASSm_HIT_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_STAT_CLASSm_PRU0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1481. MII_G_RT_RX_STAT_CLASSm_HIT_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RX_STAT_CLASSm_PRU0	R/W	0h	RX Class<m> Hit Count (where m = 0 to 15). Write to subtract

Table 15-1482. Register Call Summary for MII_G_RT_RX_STAT_CLASSm_HIT_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_CLASSm_HIT_PRU0 Register \(Offset = 578h + formula\) \[reset = 0h\]: \[0\]](#)

15.12.69 MII_G_RT_RX_STAT_SMD_FRAG_ERR_PRU0 Register (Offset = 5B8h) [reset = 0h]

MIIG_RT_RX_STAT_SMD_FRAG_ERR_PRU0 is shown in Figure 15-487 and described in Table 15-1484.

Return to [Summary Table](#).

RX SMD Frag Error Count PRU0.

Table 15-1483. MII_G_RT_RX_STAT_SMD_FRAG_ERR_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 35B8h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 35B8h

Figure 15-487. MII_G_RT_RX_STAT_SMD_FRAG_ERR_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RX_STAT_SMD_ERR_PRU0								RX_STAT_FRAG_ERR_PRU0							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_STAT_SMD_ERR_PRU0								RX_STAT_SMD_ERR_PRU0							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1484. MII_G_RT_RX_STAT_SMD_FRAG_ERR_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RX_STAT_SMD_ERR_PRU0	R/W	0h	RX SMD Error Count, Increment when first none 0x55 does not match any valid SMD, Write to subtract
23-16	RX_STAT_FRAG_ERR_PRU0	R/W	0h	RX Frag_Cnt Seq Error Count, Write to subtract
15-8	RX_STAT_SMD_ERR_PRU0	R/W	0h	RX SMDx Seq Error Count, Write to subtract
7-0	RX_STAT_SMD_ERR_PRU0	R/W	0h	RX SMDx Seq Error Count, Write to subtract

Table 15-1485. Register Call Summary for MII_G_RT_RX_STAT_SMD_FRAG_ERR_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_SMD_FRAG_ERR_PRU0 Register \(Offset = 5B8h\) \[reset = 0h\]: \[0\]](#)

15.12.70 MII_G_RT_RX_STAT_BKT1_SIZE_PRU0 Register (Offset = 5BCh) [reset = X]

MIIG_RT_RX_STAT_BKT1_SIZE_PRU0 is shown in [Figure 15-488](#) and described in [Table 15-1487](#).

Return to [Summary Table](#).

RX Bucket1 Size Configuration (PRU0).

Table 15-1486. MII_G_RT_RX_STAT_BKT1_SIZE_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 35BCh
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 35BCh

Figure 15-488. MII_G_RT_RX_STAT_BKT1_SIZE_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		RX_STAT_BKT1_SIZE													
R/W-X		R/W-40h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1487. MII_G_RT_RX_STAT_BKT1_SIZE_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	RX_STAT_BKT1_SIZE	R/W	40h	RX Bucket1 Byte Size

Table 15-1488. Register Call Summary for MII_G_RT_RX_STAT_BKT1_SIZE_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_BKT1_SIZE_PRU0 Register \(Offset = 5BCh\) \[reset = X\]: \[0\]](#)

15.12.71 MII_G_RT_RX_STAT_BKT2_SIZE_PRU0 Register (Offset = 5C0h) [reset = X]

MIIG_RT_RX_STAT_BKT2_SIZE_PRU0 is shown in [Figure 15-489](#) and described in [Table 15-1490](#).

Return to [Summary Table](#).

RX Bucket2 Size Configuration (PRU0).

Table 15-1489. MII_G_RT_RX_STAT_BKT2_SIZE_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 35C0h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 35C0h

Figure 15-489. MII_G_RT_RX_STAT_BKT2_SIZE_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		RX_STAT_BKT2_SIZE													
R/W-X		R/W-80h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1490. MII_G_RT_RX_STAT_BKT2_SIZE_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	RX_STAT_BKT2_SIZE	R/W	80h	RX Bucket2 Byte Size

Table 15-1491. Register Call Summary for MII_G_RT_RX_STAT_BKT2_SIZE_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_BKT2_SIZE_PRU0 Register \(Offset = 5C0h\) \[reset = X\]: \[0\]](#)

15.12.72 MII_G_RT_RX_STAT_BKT3_SIZE_PRU0 Register (Offset = 5C4h) [reset = X]

MIIG_RT_RX_STAT_BKT3_SIZE_PRU0 is shown in [Figure 15-490](#) and described in [Table 15-1493](#).

Return to [Summary Table](#).

RX Bucket3 Size Configuration (PRU0).

Table 15-1492. MII_G_RT_RX_STAT_BKT3_SIZE_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 35C4h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 35C4h

Figure 15-490. MII_G_RT_RX_STAT_BKT3_SIZE_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		RX_STAT_BKT3_SIZE													
R/W-X		R/W-100h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1493. MII_G_RT_RX_STAT_BKT3_SIZE_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	RX_STAT_BKT3_SIZE	R/W	100h	RX Bucket3 Byte Size

Table 15-1494. Register Call Summary for MII_G_RT_RX_STAT_BKT3_SIZE_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_BKT3_SIZE_PRU0 Register \(Offset = 5C4h\) \[reset = X\]: \[0\]](#)

15.12.73 MII_G_RT_RX_STAT_BKT4_SIZE_PRU0 Register (Offset = 5C8h) [reset = X]

MIIG_RT_RX_STAT_BKT4_SIZE_PRU0 is shown in [Figure 15-491](#) and described in [Table 15-1496](#).

Return to [Summary Table](#).

RX Bucket4 Size Configuration (PRU0).

Table 15-1495. MII_G_RT_RX_STAT_BKT4_SIZE_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 35C8h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 35C8h

Figure 15-491. MII_G_RT_RX_STAT_BKT4_SIZE_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		RX_STAT_BKT4_SIZE													
R/W-X		R/W-200h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1496. MII_G_RT_RX_STAT_BKT4_SIZE_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	RX_STAT_BKT4_SIZE	R/W	200h	RX Bucket4 Byte Size

Table 15-1497. Register Call Summary for MII_G_RT_RX_STAT_BKT4_SIZE_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_BKT4_SIZE_PRU0 Register \(Offset = 5C8h\) \[reset = X\]: \[0\]](#)

15.12.74 MII_G_RT_RX_STAT_64_PRU0 Register (Offset = 5CCh) [reset = X]

MIIG_RT_RX_STAT_64_PRU0 is shown in Figure 15-492 and described in Table 15-1499.

Return to [Summary Table](#).

RX 64B Sized Frame Count (PRU0).

Table 15-1498. MII_G_RT_RX_STAT_64_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 35CCh
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 35CCh

Figure 15-492. MII_G_RT_RX_STAT_64_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RX_64_FRM_CNT															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1499. MII_G_RT_RX_STAT_64_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_64_FRM_CNT	R/W	0h	RX 64 Byte Frame Count Increment if 64 B size

Table 15-1500. Register Call Summary for MII_G_RT_RX_STAT_64_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_64_PRU0 Register \(Offset = 5CCh\) \[reset = X\]: \[0\]](#)

15.12.75 MII_G_RT_RX_STAT_BKT1_PRU0 Register (Offset = 5D0h) [reset = X]

MIIG_RT_RX_STAT_BKT1_PRU0 is shown in [Figure 15-493](#) and described in [Table 15-1502](#).

Return to [Summary Table](#).

RX Bucket1 Sized Frame Count (PRU0).

Table 15-1501. MII_G_RT_RX_STAT_BKT1_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 35D0h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 35D0h

Figure 15-493. MII_G_RT_RX_STAT_BKT1_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RX_STAT_BKT1															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1502. MII_G_RT_RX_STAT_BKT1_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_STAT_BKT1	R/W	0h	RX Bucket1 Frame Count Increment if <= than Bucket1 Byte Size

Table 15-1503. Register Call Summary for MII_G_RT_RX_STAT_BKT1_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_BKT1_PRU0 Register \(Offset = 5D0h\) \[reset = X\]: \[0\]](#)

15.12.76 MII_G_RT_RX_STAT_BKT2_PRU0 Register (Offset = 5D4h) [reset = X]

MIIG_RT_RX_STAT_BKT2_PRU0 is shown in [Figure 15-494](#) and described in [Table 15-1505](#).

Return to [Summary Table](#).

RX Bucket2 Sized Frame Count (PRU0).

Table 15-1504. MII_G_RT_RX_STAT_BKT2_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 35D4h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 35D4h

Figure 15-494. MII_G_RT_RX_STAT_BKT2_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RX_STAT_BKT2															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1505. MII_G_RT_RX_STAT_BKT2_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_STAT_BKT2	R/W	0h	RX Bucket2 Frame Count Increment if <= than Bucket2 Byte Size and if > than Bucket1 Byte Size

Table 15-1506. Register Call Summary for MII_G_RT_RX_STAT_BKT2_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_BKT2_PRU0 Register \(Offset = 5D4h\) \[reset = X\]: \[0\]](#)

15.12.77 MII_G_RT_RX_STAT_BKT3_PRU0 Register (Offset = 5D8h) [reset = X]

MIIG_RT_RX_STAT_BKT3_PRU0 is shown in [Figure 15-495](#) and described in [Table 15-1508](#).

Return to [Summary Table](#).

RX Bucket3 Sized Frame Count (PRU0).

Table 15-1507. MII_G_RT_RX_STAT_BKT3_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 35D8h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 35D8h

Figure 15-495. MII_G_RT_RX_STAT_BKT3_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RX_STAT_BKT3															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1508. MII_G_RT_RX_STAT_BKT3_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_STAT_BKT3	R/W	0h	RX Bucket3 Frame Count Increment if <= than Bucket3 Byte Size and if > than Bucket2 Byte Size

Table 15-1509. Register Call Summary for MII_G_RT_RX_STAT_BKT3_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_BKT3_PRU0 Register \(Offset = 5D8h\) \[reset = X\]: \[0\]](#)

15.12.78 MII_G_RT_RX_STAT_BKT4_PRU0 Register (Offset = 5DCh) [reset = X]

MIIG_RT_RX_STAT_BKT4_PRU0 is shown in [Figure 15-496](#) and described in [Table 15-1511](#).

Return to [Summary Table](#).

RX Bucket4 Sized Frame Count (PRU0).

Table 15-1510. MII_G_RT_RX_STAT_BKT4_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 35DCh
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 35DCh

Figure 15-496. MII_G_RT_RX_STAT_BKT4_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RX_STAT_BKT4															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1511. MII_G_RT_RX_STAT_BKT4_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_STAT_BKT4	R/W	0h	RX Bucket4 Frame Count Increment if <= than Bucket4 Byte Size and if > than Bucket3 Byte Size

Table 15-1512. Register Call Summary for MII_G_RT_RX_STAT_BKT4_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_BKT4_PRU0 Register \(Offset = 5DCh\) \[reset = X\]: \[0\]](#)

15.12.79 MII_G_RT_RX_STAT_BKT5_PRU0 Register (Offset = 5E0h) [reset = X]

MIIG_RT_RX_STAT_BKT5_PRU0 is shown in [Figure 15-497](#) and described in [Table 15-1514](#).

Return to [Summary Table](#).

RX Bucket5 Sized Frame Count (PRU0).

Table 15-1513. MII_G_RT_RX_STAT_BKT5_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 35E0h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 35E0h

Figure 15-497. MII_G_RT_RX_STAT_BKT5_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RX_STAT_BKT5															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1514. MII_G_RT_RX_STAT_BKT5_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_STAT_BKT5	R/W	0h	RX Bucket5 Frame Count Increment if > than Bucket4 Byte Size

Table 15-1515. Register Call Summary for MII_G_RT_RX_STAT_BKT5_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_BKT5_PRU0 Register \(Offset = 5E0h\) \[reset = X\]: \[0\]](#)

15.12.80 MII_G_RT_RX_STAT_TOTAL_BYTES_PRU0 Register (Offset = 5E4h) [reset = 0h]

MIIG_RT_RX_STAT_TOTAL_BYTES_PRU0 is shown in [Figure 15-498](#) and described in [Table 15-1517](#).

Return to [Summary Table](#).

RX Total Byte Count (PRU0).

Table 15-1516. MII_G_RT_RX_STAT_TOTAL_BYTES_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 35E4h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 35E4h

Figure 15-498. MII_G_RT_RX_STAT_TOTAL_BYTES_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_STAT_TOTAL_BYTES_PRU																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1517. MII_G_RT_RX_STAT_TOTAL_BYTES_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RX_STAT_TOTAL_BYTES_PRU	R/W	0h	RX Total Byte Count

Table 15-1518. Register Call Summary for MII_G_RT_RX_STAT_TOTAL_BYTES_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_TOTAL_BYTES_PRU0 Register \(Offset = 5E4h\) \[reset = 0h\]: \[0\]](#)

15.12.81 MII_G_RT_RXTX_STAT_TOTAL_BYTES_PRU0 Register (Offset = 5E8h) [reset = 0h]

MIIG_RT_RXTX_STAT_TOTAL_BYTES_PRU0 is shown in Figure 15-499 and described in Table 15-1520.

Return to [Summary Table](#).

RX TX Total Byte Count (PRU0).

Table 15-1519. MII_G_RT_RXTX_STAT_TOTAL_BYTES_PRU0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 35E8h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 35E8h

Figure 15-499. MII_G_RT_RXTX_STAT_TOTAL_BYTES_PRU0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXTX_STAT_TOTAL_BYTES_PRU																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1520. MII_G_RT_RXTX_STAT_TOTAL_BYTES_PRU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RXTX_STAT_TOTAL_BYTES_PRU	R/W	0h	RX and TX Total Byte Count

Table 15-1521. Register Call Summary for MII_G_RT_RXTX_STAT_TOTAL_BYTES_PRU0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RXTX_STAT_TOTAL_BYTES_PRU0 Register \(Offset = 5E8h\) \[reset = 0h\]: \[0\]](#)

15.12.82 MII_G_RT_TX_STAT_GOOD_PORT0 Register (Offset = 5ECh) [reset = 0h]

MIIG_RT_TX_STAT_GOOD_PORT0 is shown in [Figure 15-500](#) and described in [Table 15-1523](#).

Return to [Summary Table](#).

TX Good Frame Count Port0.

Table 15-1522. MII_G_RT_TX_STAT_GOOD_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 35ECh
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 35ECh

Figure 15-500. MII_G_RT_TX_STAT_GOOD_PORT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_GOOD_FRM_CNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1523. MII_G_RT_TX_STAT_GOOD_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TX_GOOD_FRM_CNT	R/W	0h	TX Good Frame Count Increment if no min size err max size err or MII odd nibble

Table 15-1524. Register Call Summary for MII_G_RT_TX_STAT_GOOD_PORT0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_GOOD_PORT0 Register \(Offset = 5ECh\) \[reset = 0h\]: \[0\]](#)

15.12.83 MII_G_RT_TX_STAT_BC_PORT0 Register (Offset = 5F0h) [reset = X]

MIIG_RT_TX_STAT_BC_PORT0 is shown in [Figure 15-501](#) and described in [Table 15-1526](#).

Return to [Summary Table](#).

TX BC Frame Count Port0.

Table 15-1525. MII_G_RT_TX_STAT_BC_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 35F0h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 35F0h

Figure 15-501. MII_G_RT_TX_STAT_BC_PORT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_BC_FRM_CNT															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1526. MII_G_RT_TX_STAT_BC_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_BC_FRM_CNT	R/W	0h	TX BC Frame Count Increment if BC

Table 15-1527. Register Call Summary for MII_G_RT_TX_STAT_BC_PORT0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_BC_PORT0 Register \(Offset = 5F0h\) \[reset = X\]: \[0\]](#)

15.12.84 MII_G_RT_TX_STAT_MC_PORT0 Register (Offset = 5F4h) [reset = X]

MIIG_RT_TX_STAT_MC_PORT0 is shown in [Figure 15-502](#) and described in [Table 15-1529](#).

Return to [Summary Table](#).

TX MC Frame Count Port0.

Table 15-1528. MII_G_RT_TX_STAT_MC_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 35F4h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 35F4h

Figure 15-502. MII_G_RT_TX_STAT_MC_PORT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_MC_FRM_CNT															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1529. MII_G_RT_TX_STAT_MC_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_MC_FRM_CNT	R/W	0h	TX MC Frame Count. Increment if MC

Table 15-1530. Register Call Summary for MII_G_RT_TX_STAT_MC_PORT0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_MC_PORT0 Register \(Offset = 5F4h\) \[reset = X\]: \[0\]](#)

15.12.85 MII_G_RT_TX_STAT_ODD_ERR_PORT0 Register (Offset = 5F8h) [reset = X]

MIIG_RT_TX_STAT_ODD_ERR_PORT0 is shown in [Figure 15-503](#) and described in [Table 15-1532](#).

Return to [Summary Table](#).

TX Odd Nibble Frame Count Port0.

Table 15-1531. MII_G_RT_TX_STAT_ODD_ERR_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 35F8h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 35F8h

Figure 15-503. MII_G_RT_TX_STAT_ODD_ERR_PORT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_ODD_ERR_FRM_CNT															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1532. MII_G_RT_TX_STAT_ODD_ERR_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_ODD_ERR_FRM_CNT	R/W	0h	TX Odd Nibble Frame Count Increment if MII odd nibble

Table 15-1533. Register Call Summary for MII_G_RT_TX_STAT_ODD_ERR_PORT0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_ODD_ERR_PORT0 Register \(Offset = 5F8h\) \[reset = X\]: \[0\]](#)

15.12.86 MII_G_RT_TX_STAT_UNDERFLOW_ERR_PORT0 Register (Offset = 5FCh) [reset = X]

MIIG_RT_TX_STAT_UNDERFLOW_ERR_PORT0 is shown in [Figure 15-504](#) and described in [Table 15-1535](#).

Return to [Summary Table](#).

TX Under Flow Error Count Port0.

Table 15-1534. MII_G_RT_TX_STAT_UNDERFLOW_ERR_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 35FCh
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 35FCh

Figure 15-504. MII_G_RT_TX_STAT_UNDERFLOW_ERR_PORT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_UNDERFLOW_CNT															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1535. MII_G_RT_TX_STAT_UNDERFLOW_ERR_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_UNDERFLOW_CNT	R/W	0h	TX MAX Underflow Error Cnt

Table 15-1536. Register Call Summary for MII_G_RT_TX_STAT_UNDERFLOW_ERR_PORT0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_UNDERFLOW_ERR_PORT0 Register \(Offset = 5FCh\) \[reset = X\]: \[0\]](#)

15.12.87 MII_G_RT_TX_STAT_MAX_SIZE_PORT0 Register (Offset = 600h) [reset = X]

MIIG_RT_TX_STAT_MAX_SIZE_PORT0 is shown in Figure 15-505 and described in Table 15-1538.

Return to [Summary Table](#).

TX Max Size Frame Port0.

Table 15-1537. MII_G_RT_TX_STAT_MAX_SIZE_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3600h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3600h

Figure 15-505. MII_G_RT_TX_STAT_MAX_SIZE_PORT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_MAX_SIZE_FRM															
R/W-X																R/W-7D0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1538. MII_G_RT_TX_STAT_MAX_SIZE_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_MAX_SIZE_FRM	R/W	7D0h	TX MAX Size Frame Count Limit

Table 15-1539. Register Call Summary for MII_G_RT_TX_STAT_MAX_SIZE_PORT0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_MAX_SIZE_PORT0 Register \(Offset = 600h\) \[reset = X\]: \[0\]](#)

15.12.88 MII_G_RT_TX_STAT_MAX_ERR_PORT0 Register (Offset = 604h) [reset = X]

MIIG_RT_TX_STAT_MAX_ERR_PORT0 is shown in Figure 15-506 and described in Table 15-1541.

Return to [Summary Table](#).

TX Max Size Error Frame Count Port0.

Table 15-1540. MII_G_RT_TX_STAT_MAX_ERR_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3604h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3604h

Figure 15-506. MII_G_RT_TX_STAT_MAX_ERR_PORT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_MAX_ERR_FRM_CNT															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1541. MII_G_RT_TX_STAT_MAX_ERR_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_MAX_ERR_FRM_CNT	R/W	0h	TX MAX Size Err Frame Count Increment if > max Limit

Table 15-1542. Register Call Summary for MII_G_RT_TX_STAT_MAX_ERR_PORT0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_MAX_ERR_PORT0 Register \(Offset = 604h\) \[reset = X\]: \[0\]](#)

15.12.89 MII_G_RT_TX_STAT_MIN_SIZE_PORT0 Register (Offset = 608h) [reset = X]

MIIG_RT_TX_STAT_MIN_SIZE_PORT0 is shown in [Figure 15-507](#) and described in [Table 15-1544](#).

Return to [Summary Table](#).

TX Min Size Frame Port0.

Table 15-1543. MII_G_RT_TX_STAT_MIN_SIZE_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3608h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3608h

Figure 15-507. MII_G_RT_TX_STAT_MIN_SIZE_PORT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_MIN_SIZE_FRM															
R/W-X																R/W-40h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1544. MII_G_RT_TX_STAT_MIN_SIZE_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_MIN_SIZE_FRM	R/W	40h	TX MIN Size Frame Count Limit

Table 15-1545. Register Call Summary for MII_G_RT_TX_STAT_MIN_SIZE_PORT0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_MIN_SIZE_PORT0 Register \(Offset = 608h\) \[reset = X\]: \[0\]](#)

15.12.90 MII_G_RT_TX_STAT_MIN_ERR_PORT0 Register (Offset = 60Ch) [reset = X]

MIIG_RT_TX_STAT_MIN_ERR_PORT0 is shown in [Figure 15-508](#) and described in [Table 15-1547](#).

Return to [Summary Table](#).

TX Min Size ErrorFrame Count Port0.

Table 15-1546. MII_G_RT_TX_STAT_MIN_ERR_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 360Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 360Ch

Figure 15-508. MII_G_RT_TX_STAT_MIN_ERR_PORT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_MIN_ERR_FRM_CNT															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1547. MII_G_RT_TX_STAT_MIN_ERR_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_MIN_ERR_FRM_CNT	R/W	0h	TX MIN Size Err Frame Count Increment if < min Limit

Table 15-1548. Register Call Summary for MII_G_RT_TX_STAT_MIN_ERR_PORT0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_MIN_ERR_PORT0 Register \(Offset = 60Ch\) \[reset = X\]: \[0\]](#)

15.12.91 MII_G_RT_TX_STAT_BKT1_SIZE_PORT0 Register (Offset = 610h) [reset = X]

MIIG_RT_TX_STAT_BKT1_SIZE_PORT0 is shown in Figure 15-509 and described in Table 15-1550.

Return to [Summary Table](#).

TX Bucket1 Size Configuration Port0.

Table 15-1549. MII_G_RT_TX_STAT_BKT1_SIZE_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3610h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3610h

Figure 15-509. MII_G_RT_TX_STAT_BKT1_SIZE_PORT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TX_STAT_BKT1_SIZE													
R/W-X		R/W-40h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1550. MII_G_RT_TX_STAT_BKT1_SIZE_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TX_STAT_BKT1_SIZE	R/W	40h	TX Bucket1 Byte Size

Table 15-1551. Register Call Summary for MII_G_RT_TX_STAT_BKT1_SIZE_PORT0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_BKT1_SIZE_PORT0 Register \(Offset = 610h\) \[reset = X\]: \[0\]](#)

15.12.92 MII_G_RT_TX_STAT_BKT2_SIZE_PORT0 Register (Offset = 614h) [reset = X]

MIIG_RT_TX_STAT_BKT2_SIZE_PORT0 is shown in Figure 15-510 and described in Table 15-1553.

Return to [Summary Table](#).

TX Bucket2 Size Configuration Port0.

Table 15-1552. MII_G_RT_TX_STAT_BKT2_SIZE_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3614h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3614h

Figure 15-510. MII_G_RT_TX_STAT_BKT2_SIZE_PORT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TX_STAT_BKT2_SIZE													
R/W-X		R/W-80h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1553. MII_G_RT_TX_STAT_BKT2_SIZE_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TX_STAT_BKT2_SIZE	R/W	80h	TX Bucket2 Byte Size

Table 15-1554. Register Call Summary for MII_G_RT_TX_STAT_BKT2_SIZE_PORT0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_BKT2_SIZE_PORT0 Register \(Offset = 614h\) \[reset = X\]: \[0\]](#)

15.12.93 MII_G_RT_TX_STAT_BKT3_SIZE_PORT0 Register (Offset = 618h) [reset = X]

MIIG_RT_TX_STAT_BKT3_SIZE_PORT0 is shown in Figure 15-511 and described in Table 15-1556.

Return to [Summary Table](#).

TX Bucket3 Size Configuration Port0.

Table 15-1555. MII_G_RT_TX_STAT_BKT3_SIZE_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3618h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3618h

Figure 15-511. MII_G_RT_TX_STAT_BKT3_SIZE_PORT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TX_STAT_BKT3_SIZE													
R/W-X		R/W-100h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1556. MII_G_RT_TX_STAT_BKT3_SIZE_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TX_STAT_BKT3_SIZE	R/W	100h	TX Bucket3 Byte Size

Table 15-1557. Register Call Summary for MII_G_RT_TX_STAT_BKT3_SIZE_PORT0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_BKT3_SIZE_PORT0 Register \(Offset = 618h\) \[reset = X\]: \[0\]](#)

15.12.94 MII_G_RT_TX_STAT_BKT4_SIZE_PORT0 Register (Offset = 61Ch) [reset = X]

MIIG_RT_TX_STAT_BKT4_SIZE_PORT0 is shown in Figure 15-512 and described in Table 15-1559.

Return to [Summary Table](#).

TX Bucket4 Size Configuration Port0.

Table 15-1558. MII_G_RT_TX_STAT_BKT4_SIZE_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 361Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 361Ch

Figure 15-512. MII_G_RT_TX_STAT_BKT4_SIZE_PORT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TX_STAT_BKT4_SIZE													
R/W-X		R/W-200h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1559. MII_G_RT_TX_STAT_BKT4_SIZE_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TX_STAT_BKT4_SIZE	R/W	200h	TX Bucket4 Byte Size

Table 15-1560. Register Call Summary for MII_G_RT_TX_STAT_BKT4_SIZE_PORT0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_BKT4_SIZE_PORT0 Register \(Offset = 61Ch\) \[reset = X\]: \[0\]](#)

15.12.95 MII_G_RT_TX_STAT_64_PORT0 Register (Offset = 620h) [reset = X]

MIIG_RT_TX_STAT_64_PORT0 is shown in [Figure 15-513](#) and described in [Table 15-1562](#).

Return to [Summary Table](#).

TX 64B Sized Frame Count Port0.

Table 15-1561. MII_G_RT_TX_STAT_64_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3620h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3620h

Figure 15-513. MII_G_RT_TX_STAT_64_PORT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_64_FRM_CNT															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1562. MII_G_RT_TX_STAT_64_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_64_FRM_CNT	R/W	0h	TX 64 Byte Frame Count. Increment if 64 B

Table 15-1563. Register Call Summary for MII_G_RT_TX_STAT_64_PORT0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_64_PORT0 Register \(Offset = 620h\) \[reset = X\]: \[0\]](#)

15.12.96 MII_G_RT_TX_STAT_BKT1_PORT0 Register (Offset = 624h) [reset = X]

MIIG_RT_TX_STAT_BKT1_PORT0 is shown in [Figure 15-514](#) and described in [Table 15-1565](#).

Return to [Summary Table](#).

TX Bucket1 Sized Frame Count Port0.

Table 15-1564. MII_G_RT_TX_STAT_BKT1_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3624h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3624h

Figure 15-514. MII_G_RT_TX_STAT_BKT1_PORT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_STAT_BKT1															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1565. MII_G_RT_TX_STAT_BKT1_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_STAT_BKT1	R/W	0h	TX Bucket1 Increment if <= than Bucket1

Table 15-1566. Register Call Summary for MII_G_RT_TX_STAT_BKT1_PORT0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_BKT1_PORT0 Register \(Offset = 624h\) \[reset = X\]: \[0\]](#)

15.12.97 MII_G_RT_TX_STAT_BKT2_PORT0 Register (Offset = 628h) [reset = X]

MIIG_RT_TX_STAT_BKT2_PORT0 is shown in [Figure 15-515](#) and described in [Table 15-1568](#).

Return to [Summary Table](#).

TX Bucket2 Sized Frame Count Port0.

Table 15-1567. MII_G_RT_TX_STAT_BKT2_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3628h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3628h

Figure 15-515. MII_G_RT_TX_STAT_BKT2_PORT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_STAT_BKT2															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1568. MII_G_RT_TX_STAT_BKT2_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_STAT_BKT2	R/W	0h	TX Bucket2 Increment if <= than Bucket2 Byte Size and if > than Bucket1 Byte Size

Table 15-1569. Register Call Summary for MII_G_RT_TX_STAT_BKT2_PORT0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_BKT2_PORT0 Register \(Offset = 628h\) \[reset = X\]: \[0\]](#)

15.12.98 MII_G_RT_TX_STAT_BKT3_PORT0 Register (Offset = 62Ch) [reset = X]

MIIG_RT_TX_STAT_BKT3_PORT0 is shown in [Figure 15-516](#) and described in [Table 15-1571](#).

Return to [Summary Table](#).

TX Bucket3 Sized Frame Count Port0.

Table 15-1570. MII_G_RT_TX_STAT_BKT3_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 362Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 362Ch

Figure 15-516. MII_G_RT_TX_STAT_BKT3_PORT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_STAT_BKT3															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1571. MII_G_RT_TX_STAT_BKT3_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_STAT_BKT3	R/W	0h	TX Bucket3 Increment if <= than Bucket3 Byte Size and if > than Bucket2 Byte Size

Table 15-1572. Register Call Summary for MII_G_RT_TX_STAT_BKT3_PORT0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_BKT3_PORT0 Register \(Offset = 62Ch\) \[reset = X\]: \[0\]](#)

15.12.99 MII_G_RT_TX_STAT_BKT4_PORT0 Register (Offset = 630h) [reset = X]

MIIG_RT_TX_STAT_BKT4_PORT0 is shown in [Figure 15-517](#) and described in [Table 15-1574](#).

Return to [Summary Table](#).

TX Bucket4 Sized Frame Count Port0.

Table 15-1573. MII_G_RT_TX_STAT_BKT4_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3630h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3630h

Figure 15-517. MII_G_RT_TX_STAT_BKT4_PORT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_STAT_BKT4															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1574. MII_G_RT_TX_STAT_BKT4_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_STAT_BKT4	R/W	0h	TX Bucket4 Increment if <= than Bucket4 Byte Size and if > than Bucket3 Byte Size

Table 15-1575. Register Call Summary for MII_G_RT_TX_STAT_BKT4_PORT0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_BKT4_PORT0 Register \(Offset = 630h\) \[reset = X\]: \[0\]](#)

15.12.100 MII_G_RT_TX_STAT_BKT5_PORT0 Register (Offset = 634h) [reset = X]

MIIG_RT_TX_STAT_BKT5_PORT0 is shown in [Figure 15-518](#) and described in [Table 15-1577](#).

Return to [Summary Table](#).

TX Bucket5 Sized Frame Count Port0.

Table 15-1576. MII_G_RT_TX_STAT_BKT5_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3634h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3634h

Figure 15-518. MII_G_RT_TX_STAT_BKT5_PORT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_STAT_BKT5															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1577. MII_G_RT_TX_STAT_BKT5_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_STAT_BKT5	R/W	0h	TX Bucket5 Increment if > than Bucket4 Byte Size

Table 15-1578. Register Call Summary for MII_G_RT_TX_STAT_BKT5_PORT0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_BKT5_PORT0 Register \(Offset = 634h\) \[reset = X\]: \[0\]](#)

15.12.101 MII_G_RT_TX_STAT_TOTAL_BYTES_PORT0 Register (Offset = 638h) [reset = 0h]

MIIG_RT_TX_STAT_TOTAL_BYTES_PORT0 is shown in [Figure 15-519](#) and described in [Table 15-1580](#).

Return to [Summary Table](#).

TX Total Byte Count Port0.

Table 15-1579. MII_G_RT_TX_STAT_TOTAL_BYTES_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3638h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3638h

Figure 15-519. MII_G_RT_TX_STAT_TOTAL_BYTES_PORT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_TOTAL_STAT_BYTES_PORT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1580. MII_G_RT_TX_STAT_TOTAL_BYTES_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TX_TOTAL_STAT_BYTES_PORT	R/W	0h	TX Total Byte Count of all Frames

Table 15-1581. Register Call Summary for MII_G_RT_TX_STAT_TOTAL_BYTES_PORT0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_TOTAL_BYTES_PORT0 Register \(Offset = 638h\) \[reset = 0h\]: \[0\]](#)

15.12.102 MII_G_RT_TX_HSR_TAG_PORT0 Register (Offset = 63Ch) [reset = 892Fh]

MIIG_RT_TX_HSR_TAG_PORT0 is shown in [Figure 15-520](#) and described in [Table 15-1583](#).

Return to [Summary Table](#).

TX HSR TAG Port0.

Table 15-1582. MII_G_RT_TX_HSR_TAG_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 363Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 363Ch

Figure 15-520. MII_G_RT_TX_HSR_TAG_PORT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_HSR_TAG																															
R/W-892Fh																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1583. MII_G_RT_TX_HSR_TAG_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TX_HSR_TAG	R/W	892Fh	HSR TAG

Table 15-1584. Register Call Summary for MII_G_RT_TX_HSR_TAG_PORT0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_HSR_TAG_PORT0 Register \(Offset = 63Ch\) \[reset = 892Fh\]: \[0\]](#)

15.12.103 MII_G_RT_TX_HSR_SEQ_PORT0 Register (Offset = 640h) [reset = X]

MIIG_RT_TX_HSR_SEQ_PORT0 is shown in [Figure 15-521](#) and described in [Table 15-1586](#).

Return to [Summary Table](#).

TX HSR Seq Port0.

Table 15-1585. MII_G_RT_TX_HSR_SEQ_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3640h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3640h

Figure 15-521. MII_G_RT_TX_HSR_SEQ_PORT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_HSR_SEQ															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1586. MII_G_RT_TX_HSR_SEQ_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_HSR_SEQ	R/W	0h	HSR Seq count. It will incr for every HSR type

Table 15-1587. Register Call Summary for MII_G_RT_TX_HSR_SEQ_PORT0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_HSR_SEQ_PORT0 Register \(Offset = 640h\) \[reset = X\]: \[0\]](#)

15.12.104 MII_G_RT_TX_VLAN_TYPE_TAG_PORT0 Register (Offset = 644h) [reset = X]

MIIG_RT_TX_VLAN_TYPE_TAG_PORT0 is shown in [Figure 15-522](#) and described in [Table 15-1589](#).

Return to [Summary Table](#).

TX VLAN Type TAG Port0.

Table 15-1588. MII_G_RT_TX_VLAN_TYPE_TAG_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3644h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3644h

Figure 15-522. MII_G_RT_TX_VLAN_TYPE_TAG_PORT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_VLAN_TYPE_TAG															
R/W-X																R/W-81h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1589. MII_G_RT_TX_VLAN_TYPE_TAG_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_VLAN_TYPE_TAG	R/W	81h	TX VLAN Type Tag, match to enable VLAN removal

Table 15-1590. Register Call Summary for MII_G_RT_TX_VLAN_TYPE_TAG_PORT0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_VLAN_TYPE_TAG_PORT0 Register \(Offset = 644h\) \[reset = X\]: \[0\]](#)

15.12.105 MII_G_RT_TX_VLAN_INS_TAG_PORT0 Register (Offset = 648h) [reset = 1h]

MIIG_RT_TX_VLAN_INS_TAG_PORT0 is shown in [Figure 15-523](#) and described in [Table 15-1592](#).

Return to [Summary Table](#).

TX VLAN Insertion TAG Port0.

Table 15-1591. MII_G_RT_TX_VLAN_INS_TAG_PORT0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3648h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3648h

Figure 15-523. MII_G_RT_TX_VLAN_INS_TAG_PORT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_VLAN_INS_TAG																															
R/W-1h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1592. MII_G_RT_TX_VLAN_INS_TAG_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TX_VLAN_INS_TAG	R/W	1h	TX VLAN Insertion

Table 15-1593. Register Call Summary for MII_G_RT_TX_VLAN_INS_TAG_PORT0

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_VLAN_INS_TAG_PORT0 Register \(Offset = 648h\) \[reset = 1h\]: \[0\]](#)

15.12.106 MII_G_RT_FT1_START_LEN_PRU1 Register (Offset = 64Ch) [reset = X]

MIIG_RT_FT1_START_LEN_PRU1 is shown in [Figure 15-524](#) and described in [Table 15-1595](#).

Return to [Summary Table](#).

Filter1 Start and Length (PRU1).

Table 15-1594. MII_G_RT_FT1_START_LEN_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 364Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 364Ch

Figure 15-524. MII_G_RT_FT1_START_LEN_PRU1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				FT1_LEN			
R/W-X				R/W-6h			
15	14	13	12	11	10	9	8
RESERVED	FT1_START						
R/W-X	R/W-0h						
7	6	5	4	3	2	1	0
FT1_START							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1595. MII_G_RT_FT1_START_LEN_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	FT1_LEN	R/W	6h	Defines the total number of Bytes Filter1 will check before Valid bit is set
15	RESERVED	R/W	X	
14-0	FT1_START	R/W	0h	Byte count start for Filter1. Any write will clear all Filter1 Status Bits

Table 15-1596. Register Call Summary for MII_G_RT_FT1_START_LEN_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT1_START_LEN_PRU1 Register \(Offset = 64Ch\) \[reset = X\]: \[0\]](#)

15.12.107 MII_G_RT_FT1_CFG_PRU1 Register (Offset = 650h) [reset = X]

MIIG_RT_FT1_CFG_PRU1 is shown in Figure 15-525 and described in Table 15-1598.

Return to [Summary Table](#).

Filter1 Configuration (PRU1).

Table 15-1597. MII_G_RT_FT1_CFG_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3650h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3650h

Figure 15-525. MII_G_RT_FT1_CFG_PRU1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
FT1_7CFG		FT1_6CFG		FT1_5CFG		FT1_4CFG	
R/W-1h		R/W-1h		R/W-1h		R/W-1h	
7	6	5	4	3	2	1	0
FT1_3CFG		FT1_2CFG		FT1_1CFG		FT1_0CFG	
R/W-1h		R/W-1h		R/W-1h		R/W-1h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1598. MII_G_RT_FT1_CFG_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-14	FT1_7CFG	R/W	1h	0h = Disabled 1h = Equal 2h = Greater Than 3h = Less Than
13-12	FT1_6CFG	R/W	1h	0h = Disabled 1h = Equal 2h = Greater Than 3h = Less Than
11-10	FT1_5CFG	R/W	1h	0h = Disabled 1h = Equal 2h = Greater Than 3h = Less Than
9-8	FT1_4CFG	R/W	1h	0h = Disabled 1h = Equal 2h = Greater Than 3h = Less Than
7-6	FT1_3CFG	R/W	1h	0h = Disabled 1h = Equal 2h = Greater Than 3h = Less Than
5-4	FT1_2CFG	R/W	1h	0h = Disabled 1h = Equal 2h = Greater Than 3h = Less Than

Table 15-1598. MII_G_RT_FT1_CFG_PRU1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	FT1_1CFG	R/W	1h	0h = Disabled 1h = Equal 2h = Greater Than 3h = Less Than
1-0	FT1_0CFG	R/W	1h	0h = Disabled 1h = Equal 2h = Greater Than 3h = Less Than

Table 15-1599. Register Call Summary for MII_G_RT_FT1_CFG_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MII_G_RT_FT1_CFG_PRU1 Register \(Offset = 650h\) \[reset = X\]: \[0\]](#)

15.12.108 MII_G_RT_FT1_k_DA0_PRU1 Register (Offset = 654h + formula) [reset = 0h]

MIIG_RT_FT1_k_DA0_PRU1 is shown in [Figure 15-526](#) and described in [Table 15-1601](#).

Return to [Summary Table](#).

Filter1<k> DA0 (PRU1).

Offset = 654h + (k * 10h); where k = 0h to 7h

Table 15-1600. MII_G_RT_FT1_k_DA0_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3654h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3654h + formula

Figure 15-526. MII_G_RT_FT1_k_DA0_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FT1_k_DA0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1601. MII_G_RT_FT1_k_DA0_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT1_k_DA0	R/W	0h	Filter1 DA4:DA1

Table 15-1602. Register Call Summary for MII_G_RT_FT1_k_DA0_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT1_k_DA0_PRU1 Register \(Offset = 654h + formula\) \[reset = 0h\]: \[0\]](#)

15.12.109 MII_G_RT_FT1_k_DA1_PRU1 Register (Offset = 658h + formula) [reset = X]

MIIG_RT_FT1_k_DA1_PRU1 is shown in [Figure 15-527](#) and described in [Table 15-1604](#).

Return to [Summary Table](#).

Filter1<k> DA1 (PRU1).

Offset = 658h + (k * 10h); where k = 0h to 7h

Table 15-1603. MII_G_RT_FT1_k_DA1_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3658h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3658h + formula

Figure 15-527. MII_G_RT_FT1_k_DA1_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FT1_k_DA1															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1604. MII_G_RT_FT1_k_DA1_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	FT1_k_DA1	R/W	0h	Filter1 DA6:DA5

Table 15-1605. Register Call Summary for MII_G_RT_FT1_k_DA1_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT1_k_DA1_PRU1 Register \(Offset = 658h + formula\) \[reset = X\]: \[0\]](#)

15.12.110 MII_G_RT_FT1_k_DA_MASK0_PRU1 Register (Offset = 65Ch + formula) [reset = 0h]

MIIG_RT_FT1_k_DA_MASK0_PRU1 is shown in [Figure 15-528](#) and described in [Table 15-1607](#).

Return to [Summary Table](#).

Filter1<k> DA0 Mask (PRU1).

Offset = 65Ch + (k * 10h); where k = 0h to 7h

Table 15-1606. MII_G_RT_FT1_k_DA_MASK0_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 365Ch + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 365Ch + formula

Figure 15-528. MII_G_RT_FT1_k_DA_MASK0_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FT1_k_DA_MASK0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1607. MII_G_RT_FT1_k_DA_MASK0_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT1_k_DA_MASK0	R/W	0h	Filter1 MDA4:MDA1 set to 1 to mask corresponding bit

Table 15-1608. Register Call Summary for MII_G_RT_FT1_k_DA_MASK0_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT1_k_DA_MASK0_PRU1 Register \(Offset = 65Ch + formula\) \[reset = 0h\]: \[0\]](#)

15.12.111 MII_G_RT_FT1_k_DA_MASK1_PRU1 Register (Offset = 660h + formula) [reset = X]

MIIG_RT_FT1_k_DA_MASK1_PRU1 is shown in [Figure 15-529](#) and described in [Table 15-1610](#).

Return to [Summary Table](#).

Filter1<k> DA1 Mask (PRU1).

Offset = 660h + (k * 10h); where k = 0h to 7h

Table 15-1609. MII_G_RT_FT1_k_DA_MASK1_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3660h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3660h + formula

Figure 15-529. MII_G_RT_FT1_k_DA_MASK1_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FT1_k_DA_MASK1															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1610. MII_G_RT_FT1_k_DA_MASK1_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	FT1_k_DA_MASK1	R/W	0h	Filter1 MDA6:MDA5 set to 1 to mask corresponding bit

Table 15-1611. Register Call Summary for MII_G_RT_FT1_k_DA_MASK1_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT1_k_DA_MASK1_PRU1 Register \(Offset = 660h + formula\) \[reset = X\]: \[0\]](#)

15.12.112 MII_G_RT_FT3_m_START_PRU1 Register (Offset = 6D4h + formula) [reset = X]

MIIG_RT_FT3_m_START_PRU1 is shown in [Figure 15-530](#) and described in [Table 15-1613](#).

Return to [Summary Table](#).

Filter3<m> Start (PRU1).

Offset = 6D4h + (m * 20h); where m = 0h to Fh

Table 15-1612. MII_G_RT_FT3_m_START_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 36D4h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 36D4h + formula

Figure 15-530. MII_G_RT_FT3_m_START_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FT3_START															
R/W-X																R/W-Ch															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1613. MII_G_RT_FT3_m_START_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R/W	X	
14-0	FT3_START	R/W	Ch	Byte count start for Filter3. Any write will clear all Filter3 Status Bits SW can read to determine next start during Auto

Table 15-1614. Register Call Summary for MII_G_RT_FT3_m_START_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT3_m_START_PRU1 Register \(Offset = 6D4h + formula\) \[reset = X\]: \[0\]](#)

15.12.113 MII_G_RT_FT3_m_START_AUTO_PRU1 Register (Offset = 6D8h + formula) [reset = X]

MIIG_RT_FT3_m_START_AUTO_PRU1 is shown in [Figure 15-531](#) and described in [Table 15-1616](#).

Return to [Summary Table](#).

Filter3<m> Start Auto (PRU1).

Offset = 6D8h + (m * 20h); where m = 0h to Fh

Table 15-1615. MII_G_RT_FT3_m_START_AUTO_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 36D8h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 36D8h + formula

Figure 15-531. MII_G_RT_FT3_m_START_AUTO_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FT3_START_AUTO															
R-X																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 15-1616. MII_G_RT_FT3_m_START_AUTO_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	X	
14-0	FT3_START_AUTO	R	0h	Byte count start for Auto skip mode

Table 15-1617. Register Call Summary for MII_G_RT_FT3_m_START_AUTO_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT3_m_START_AUTO_PRU1 Register \(Offset = 6D8h + formula\) \[reset = X\]: \[0\]](#)

15.12.114 MII_G_RT_FT3_m_START_LEN_PRU1 Register (Offset = 6DCh + formula) [reset = X]

MIIG_RT_FT3_m_START_LEN_PRU1 is shown in [Figure 15-532](#) and described in [Table 15-1619](#).

Return to [Summary Table](#).

Filter3<m> Start offset (PRU1).

Offset = 6DCh + (m * 20h); where m = 0h to Fh

Table 15-1618. MII_G_RT_FT3_m_START_LEN_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 36DCh + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 36DCh + formula

Figure 15-532. MII_G_RT_FT3_m_START_LEN_PRU1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED	FT3_OFFSET_END			RESERVED	FT3_OFFSET_START		
R/W-X	R/W-0h			R/W-X	R/W-0h		
15	14	13	12	11	10	9	8
RESERVED	FT3_OFFSET						
R/W-X	R/W-0h						
7	6	5	4	3	2	1	0
FT3_OFFSET							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1619. MII_G_RT_FT3_m_START_LEN_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22-20	FT3_OFFSET_END	R/W	0h	Defines which byte within FT3_[N]P[63:0] to end the compare at set the Valid flag, rule ft3_offset_end >= ft3_offset_start To disable pattern compare set start and end to zero
19	RESERVED	R/W	X	
18-16	FT3_OFFSET_START	R/W	0h	Defines which byte within FT3_[N]P[63:0] to start the compare
15	RESERVED	R/W	X	
14-0	FT3_OFFSET	R/W	0h	Determine which byte to start FT3_[N]P[63:0] operation it will start on the next byte after FT3_T completes if set to zero

Table 15-1620. Register Call Summary for MII_G_RT_FT3_m_START_LEN_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT3_m_START_LEN_PRU1 Register \(Offset = 6DCh + formula\) \[reset = X\]: \[0\]](#)

15.12.115 MII_G_RT_FT3_m_JMP_OFFSET_PRU1 Register (Offset = 6E0h + formula) [reset = X]

MIIG_RT_FT3_m_JMP_OFFSET_PRU1 is shown in [Figure 15-533](#) and described in [Table 15-1622](#).

Return to [Summary Table](#).

Filter3<m> Jump offset (PRU1).

Offset = 6E0h + (m * 20h); where m = 0h to Fh

Table 15-1621. MII_G_RT_FT3_m_JMP_OFFSET_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 36E0h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 36E0h + formula

Figure 15-533. MII_G_RT_FT3_m_JMP_OFFSET_PRU1 Register

31	30	29	28	27	26	25	24
RESERVED	FT3_m_NJMP_OFFSET_PRU1						
R/W-X	R/W-0h						
23	22	21	20	19	18	17	16
FT3_m_NJMP_OFFSET_PRU1							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED	FT3_m_IJMP_OFFSET_PRU1						
R/W-X	R/W-0h						
7	6	5	4	3	2	1	0
FT3_m_IJMP_OFFSET_PRU1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1622. MII_G_RT_FT3_m_JMP_OFFSET_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-16	FT3_m_NJMP_OFFSET_PRU1	R/W	0h	Defines the Next Offset to compare when auto arm jump is enabled
15	RESERVED	R/W	X	
14-0	FT3_m_IJMP_OFFSET_PRU1	R/W	0h	Defines the Initial Offset to compare when auto arm jump is enabled

Table 15-1623. Register Call Summary for MII_G_RT_FT3_m_JMP_OFFSET_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT3_m_JMP_OFFSET_PRU1 Register \(Offset = 6E0h + formula\) \[reset = X\]: \[0\]](#)

15.12.116 MII_G_RT_FT3_m_LEN_PRU1 Register (Offset = 6E4h + formula) [reset = X]

MIIG_RT_FT3_m_LEN_PRU1 is shown in [Figure 15-534](#) and described in [Table 15-1625](#).

Return to [Summary Table](#).

Filter3 Length Offset for (PRU1).

Offset = 6E4h + (m * 20h); where m = 0h to Fh

Table 15-1624. MII_G_RT_FT3_m_LEN_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 36E4h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 36E4h + formula

Figure 15-534. MII_G_RT_FT3_m_LEN_PRU1 Register

31	30	29	28	27	26	25	24
RESERVED							FT3_m_LEN_BIG_EN_PRU1
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED				FT3_m_LEN_SIZE_BIT_PRU1			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED							FT3_m_LEN_START_BIT_PRU1
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
FT3_m_LEN_START_BIT_PRU1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1625. MII_G_RT_FT3_m_LEN_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	FT3_m_LEN_BIG_EN_PRU1	R/W	0h	Enable Big Indian on Length
23-20	RESERVED	R/W	X	
19-16	FT3_m_LEN_SIZE_BIT_PRU1	R/W	0h	Defines number of bits to extract the length for the auto skip function
15-9	RESERVED	R/W	X	
8-0	FT3_m_LEN_START_BIT_PRU1	R/W	0h	Defines relative bit offset from the HIT byte location upto 512 bit offset the extraction to determine the on the fly length byte offset

Table 15-1626. Register Call Summary for MII_G_RT_FT3_m_LEN_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT3_m_LEN_PRU1 Register \(Offset = 6E4h + formula\) \[reset = X\]: \[0\]](#)

15.12.117 MII_G_RT_FT3_m_CFG_PRU1 Register (Offset = 6E8h + formula) [reset = X]

MIIG_RT_FT3_m_CFG_PRU1 is shown in [Figure 15-535](#) and described in [Table 15-1628](#).

Return to [Summary Table](#).

Filter3<m> Configuration (PRU1).

Offset = 6E8h + (m * 20h); where m = 0h to Fh

Table 15-1627. MII_G_RT_FT3_m_CFG_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 36E8h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 36E8h + formula

Figure 15-535. MII_G_RT_FT3_m_CFG_PRU1 Register

31	30	29	28	27	26	25	24
FT3_m_TRIG_OR_EN							
R/W-0h							
23	22	21	20	19	18	17	16
FT3_m_TRIG_OR_EN							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED					FT3_m_VLAN_SKIP_EN	FT3_mCFG	
R/W-X					R/W-1h	R/W-1h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1628. MII_G_RT_FT3_m_CFG_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	FT3_m_TRIG_OR_EN	R/W	0h	Trigger ft3 select for auto skip enable, if one or more set the function is enabled note you can not select the same ft3 only others
15-3	RESERVED	R/W	X	
2	FT3_m_VLAN_SKIP_EN	R/W	1h	0: Disabled 1: Enable
1-0	FT3_mCFG	R/W	1h	0: Disabled 1: EQ 2: GT 3: LT

Table 15-1629. Register Call Summary for MII_G_RT_FT3_m_CFG_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT3_m_CFG_PRU1 Register \(Offset = 6E8h + formula\) \[reset = X\]: \[0\]](#)

15.12.118 MII_G_RT_FT3_m_T_PRU1 Register (Offset = 6ECh + formula) [reset = 0h]

MIIG_RT_FT3_m_T_PRU1 is shown in [Figure 15-536](#) and described in [Table 15-1631](#).

Return to [Summary Table](#).

Filter3<m> T (PRU1).

Offset = 6ECh + (m * 20h); where m = 0h to Fh

Table 15-1630. MII_G_RT_FT3_m_T_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 36ECh + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 36ECh + formula

Figure 15-536. MII_G_RT_FT3_m_T_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FT3_m_T																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1631. MII_G_RT_FT3_m_T_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT3_m_T	R/W	0h	Filter3 T4:T1 Note: if Auto Skip is enabled then Type filter is not enabled

Table 15-1632. Register Call Summary for MII_G_RT_FT3_m_T_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT3_m_T_PRU1 Register \(Offset = 6ECh + formula\) \[reset = 0h\]: \[0\]](#)

15.12.119 MII_G_RT_FT3_m_T_MASK_PRU1 Register (Offset = 6F0h + formula) [reset = 0h]

MIIG_RT_FT3_m_T_MASK_PRU1 is shown in [Figure 15-537](#) and described in [Table 15-1634](#).

Return to [Summary Table](#).

Filter3<m> T Mask (PRU1).

Offset = 6F0h + (m * 20h); where m = 0h to Fh

Table 15-1633. MII_G_RT_FT3_m_T_MASK_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 36F0h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 36F0h + formula

Figure 15-537. MII_G_RT_FT3_m_T_MASK_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FT3_m_T_MASK																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1634. MII_G_RT_FT3_m_T_MASK_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT3_m_T_MASK	R/W	0h	Filter3 MT4:MT1 Note: if Auto Skip is enabled then Type filter is not enabled set to 1 to mask corresponding bit

Table 15-1635. Register Call Summary for MII_G_RT_FT3_m_T_MASK_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT3_m_T_MASK_PRU1 Register \(Offset = 6F0h + formula\) \[reset = 0h\]: \[0\]](#)

15.12.120 MII_G_RT_FT3_m_P0_PRU1 Register (Offset = 8D4h + formula) [reset = 0h]

MIIG_RT_FT3_m_P0_PRU1 is shown in [Figure 15-538](#) and described in [Table 15-1637](#).

Return to [Summary Table](#).

Filter3<m> P0 (PRU1).

Offset = 8D4h + (m * 10h); where m = 0h to Fh

Table 15-1636. MII_G_RT_FT3_m_P0_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 38D4h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 38D4h + formula

Figure 15-538. MII_G_RT_FT3_m_P0_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FT3_m_P0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1637. MII_G_RT_FT3_m_P0_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT3_m_P0	R/W	0h	Filter3 P4:P1

Table 15-1638. Register Call Summary for MII_G_RT_FT3_m_P0_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT3_m_P0_PRU1 Register \(Offset = 8D4h + formula\) \[reset = 0h\]: \[0\]](#)

15.12.121 MII_G_RT_FT3_m_P1_PRU1 Register (Offset = 8D8h + formula) [reset = 0h]

MIIG_RT_FT3_m_P1_PRU1 is shown in [Figure 15-539](#) and described in [Table 15-1640](#).

Return to [Summary Table](#).

Filter3<m> P1 (PRU1).

Offset = 8D8h + (m * 10h); where m = 0h to Fh

Table 15-1639. MII_G_RT_FT3_m_P1_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 38D8h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 38D8h + formula

Figure 15-539. MII_G_RT_FT3_m_P1_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FT3_m_P1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1640. MII_G_RT_FT3_m_P1_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT3_m_P1	R/W	0h	Filter3 P8:P5

Table 15-1641. Register Call Summary for MII_G_RT_FT3_m_P1_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT3_m_P1_PRU1 Register \(Offset = 8D8h + formula\) \[reset = 0h\]: \[0\]](#)

15.12.122 MII_G_RT_FT3_m_P_MASK0_PRU1 Register (Offset = 8DCh + formula) [reset = 0h]

MIIG_RT_FT3_m_P_MASK0_PRU1 is shown in Figure 15-540 and described in Table 15-1643.

Return to [Summary Table](#).

Filter3<m> P Mask0 (PRU1).

Offset = 8DCh + (m * 10h); where m = 0h to Fh

Table 15-1642. MII_G_RT_FT3_m_P_MASK0_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 38DCh + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 38DCh + formula

Figure 15-540. MII_G_RT_FT3_m_P_MASK0_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FT3_m_P_MASK0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1643. MII_G_RT_FT3_m_P_MASK0_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT3_m_P_MASK0	R/W	0h	Filter3 MP4:MP1 set to 1 to mask corresponding bit

Table 15-1644. Register Call Summary for MII_G_RT_FT3_m_P_MASK0_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT3_m_P_MASK0_PRU1 Register \(Offset = 8DCh + formula\) \[reset = 0h\]: \[0\]](#)

15.12.123 MII_G_RT_FT3_m_P_MASK1_PRU1 Register (Offset = 8E0h + formula) [reset = 0h]

MIIG_RT_FT3_m_P_MASK1_PRU1 is shown in Figure 15-541 and described in Table 15-1646.

Return to [Summary Table](#).

Filter3<m> P Mask1 (PRU1).

Offset = 8E0h + (m * 10h); where m = 0h to Fh

Table 15-1645. MII_G_RT_FT3_m_P_MASK1_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 38E0h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 38E0h + formula

Figure 15-541. MII_G_RT_FT3_m_P_MASK1_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FT3_m_P_MASK1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1646. MII_G_RT_FT3_m_P_MASK1_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT3_m_P_MASK1	R/W	0h	Filter3 MP8:MP5 set to 1 to mask corresponding bit

Table 15-1647. Register Call Summary for MII_G_RT_FT3_m_P_MASK1_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT3_m_P_MASK1_PRU1 Register \(Offset = 8E0h + formula\) \[reset = 0h\]: \[0\]](#)

15.12.124 MII_G_RT_FT_RX_PTR_PRU1 Register (Offset = 9D4h) [reset = 0h]

MIIG_RT_FT_RX_PTR_PRU1 is shown in [Figure 15-542](#) and described in [Table 15-1649](#).

Return to [Summary Table](#).

Filter Byte Count (PRU1).

Table 15-1648. MII_G_RT_FT_RX_PTR_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 39D4h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 39D4h

Figure 15-542. MII_G_RT_FT_RX_PTR_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FT_RX_PTR_PRU1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1649. MII_G_RT_FT_RX_PTR_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FT_RX_PTR_PRU1	R/W	0h	RX current filter Byte Count

Table 15-1650. Register Call Summary for MII_G_RT_FT_RX_PTR_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_FT_RX_PTR_PRU1 Register \(Offset = 9D4h\) \[reset = 0h\]: \[0\]](#)

15.12.125 MII_G_RT_RX_CLASSm_AND_EN_PRU1 Register (Offset = 9D8h + formula) [reset = 0h]

MIIG_RT_RX_CLASSm_AND_EN_PRU1 is shown in [Figure 15-543](#) and described in [Table 15-1652](#).

Return to [Summary Table](#).

RX Class<m> AND Enable (PRU1).

Offset = 9D8h + (m * 8h); where m = 0h to Fh

Table 15-1651. MII_G_RT_RX_CLASSm_AND_EN_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 39D8h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 39D8h + formula

Figure 15-543. MII_G_RT_RX_CLASSm_AND_EN_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_CLASSm_AND_EN																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1652. MII_G_RT_RX_CLASSm_AND_EN_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RX_CLASSm_AND_EN	R/W	0h	RX class AND enable

Table 15-1653. Register Call Summary for MII_G_RT_RX_CLASSm_AND_EN_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_CLASSm_AND_EN_PRU1 Register \(Offset = 9D8h + formula\) \[reset = 0h\]: \[0\]](#)

15.12.126 MII_G_RT_RX_CLASSm_OR_EN_PRU1 Register (Offset = 9DCh + formula) [reset = 0h]

MIIG_RT_RX_CLASSm_OR_EN_PRU1 is shown in [Figure 15-544](#) and described in [Table 15-1655](#).

Return to [Summary Table](#).

RX Class<m> OR Enable (PRU1).

Offset = 9DCh + (m * 8h); where m = 0h to Fh

Table 15-1654. MII_G_RT_RX_CLASSm_OR_EN_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 39DCh + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 39DCh + formula

Figure 15-544. MII_G_RT_RX_CLASSm_OR_EN_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_CLASSm_OR_EN																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1655. MII_G_RT_RX_CLASSm_OR_EN_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RX_CLASSm_OR_EN	R/W	0h	RX class OR enable.

Table 15-1656. Register Call Summary for MII_G_RT_RX_CLASSm_OR_EN_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_CLASSm_OR_EN_PRU1 Register \(Offset = 9DCh + formula\) \[reset = 0h\]: \[0\]](#)

15.12.127 MII_G_RT_RX_CLASS_CFG1_PRU1 Register (Offset = A58h) [reset = 0h]

MIIG_RT_RX_CLASS_CFG1_PRU1 is shown in [Figure 15-545](#) and described in [Table 15-1658](#).

Return to [Summary Table](#).

RX Class Configuration 1 Register.

Table 15-1657. MII_G_RT_RX_CLASS_CFG1_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3A58h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3A58h

Figure 15-545. MII_G_RT_RX_CLASS_CFG1_PRU1 Register

31	30	29	28	27	26	25	24
RX_CLASS15_SEL		RX_CLASS14_SEL		RX_CLASS13_SEL		RX_CLASS12_SEL	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
23	22	21	20	19	18	17	16
RX_CLASS11_SEL		RX_CLASS10_SEL		RX_CLASS9_SEL		RX_CLASS8_SEL	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8
RX_CLASS7_SEL		RX_CLASS6_SEL		RX_CLASS5_SEL		RX_CLASS4_SEL	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
RX_CLASS3_SEL		RX_CLASS2_SEL		RX_CLASS1_SEL		RX_CLASS0_SEL	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1658. MII_G_RT_RX_CLASS_CFG1_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RX_CLASS15_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
29-28	RX_CLASS14_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
27-26	RX_CLASS13_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
25-24	RX_CLASS12_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
23-22	RX_CLASS11_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND

Table 15-1658. MII_G_RT_RX_CLASS_CFG1_PRU1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	RX_CLASS10_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
19-18	RX_CLASS9_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
17-16	RX_CLASS8_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
15-14	RX_CLASS7_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
13-12	RX_CLASS6_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
11-10	RX_CLASS5_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
9-8	RX_CLASS4_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
7-6	RX_CLASS3_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
5-4	RX_CLASS2_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
3-2	RX_CLASS1_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND
1-0	RX_CLASS0_SEL	R/W	0h	rx class final term selection 00: OR 01: AND 10: OR AND AND 11: OR OR AND

Table 15-1659. Register Call Summary for MII_G_RT_RX_CLASS_CFG1_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MII_G_RT_RX_CLASS_CFG1_PRU1 Register \(Offset = A58h\) \[reset = 0h\]: \[0\]](#)

15.12.128 MII_G_RT_RX_CLASS_CFG2_PRU1 Register (Offset = A5Ch) [reset = 0h]

MIIG_RT_RX_CLASS_CFG2_PRU1 is shown in [Figure 15-546](#) and described in [Table 15-1661](#).

Return to [Summary Table](#).

RX Class Configuration 2 Register.

Table 15-1660. MII_G_RT_RX_CLASS_CFG2_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3A5Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3A5Ch

Figure 15-546. MII_G_RT_RX_CLASS_CFG2_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_CLASS_OR_NV																RX_CLASS_AND_NV															
R/W-0h																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1661. MII_G_RT_RX_CLASS_CFG2_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_CLASS_OR_NV	R/W	0h	RX class or nv enable
15-0	RX_CLASS_AND_NV	R/W	0h	RX class AND nv enable

Table 15-1662. Register Call Summary for MII_G_RT_RX_CLASS_CFG2_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_CLASS_CFG2_PRU1 Register \(Offset = A5Ch\) \[reset = 0h\]: \[0\]](#)

15.12.129 MII_G_RT_RX_CLASS_GATESm_PRU1 Register (Offset = A60h + formula) [reset = X]

MIIG_RT_RX_CLASS_GATESm_PRU1 is shown in Figure 15-547 and described in Table 15-1664.

Return to [Summary Table](#).

RX Class Gate Configuration PRU1 Register.

Offset = A60h + (m * 4h); where m = 0h to Fh

Table 15-1663. MII_G_RT_RX_CLASS_GATESm_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3A60h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3A60h + formula

Figure 15-547. MII_G_RT_RX_CLASS_GATESm_PRU1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							RX_RED_PHASE_ENm
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED	RX_ALLOW_MASKm	RX_CLASS_RAW_MASKm	RX_PHASE_MASKm	RESERVED	RX_RATE_GATE_SELm		
R/W-X	R/W-1h	R/W-1h	R/W-1h	R/W-X	R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1664. MII_G_RT_RX_CLASS_GATESm_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	RX_RED_PHASE_ENm	R/W	0h	red phase enable 0: disable 1: enable
7	RESERVED	R/W	X	
6	RX_ALLOW_MASKm	R/W	1h	allow mask 0: unmask 1: mask
5	RX_CLASS_RAW_MASKm	R/W	1h	class raw mask 0: unmask 1: mask
4	RX_PHASE_MASKm	R/W	1h	time phase mask 0: unmask 1: mask
3	RESERVED	R/W	X	
2-0	RX_RATE_GATE_SELm	R/W	0h	defines which rx_rate will gate rx_class

Table 15-1665. Register Call Summary for MII_G_RT_RX_CLASS_GATESm_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_CLASS_GATESm_PRU1 Register \(Offset = A60h + formula\) \[reset = X\]: \[0\]](#)

15.12.130 MII_G_RT_RX_GREEN_PRU1 Register (Offset = AA0h) [reset = X]

MIIG_RT_RX_GREEN_PRU1 is shown in [Figure 15-548](#) and described in [Table 15-1667](#).

Return to [Summary Table](#).

RX Green Status PRU1.

Table 15-1666. MII_G_RT_RX_GREEN_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3AA0h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3AA0h

Figure 15-548. MII_G_RT_RX_GREEN_PRU1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED			RX_GREEN_VAL	RX_GREEN_CMP_SEL			
R/W-X			R-0h	R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-1667. MII_G_RT_RX_GREEN_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R/W	X	
4	RX_GREEN_VAL	R	0h	0: RED, 1: GREEN status
3-0	RX_GREEN_CMP_SEL	R/W	0h	define which IEP CMP start green

Table 15-1668. Register Call Summary for MII_G_RT_RX_GREEN_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_GREEN_PRU1 Register \(Offset = AA0h\) \[reset = X\]: \[0\]](#)

15.12.131 MII_G_RT_SA_HASH_PRU1 Register (Offset = AA4h) [reset = X]

MIIG_RT_SA_HASH_PRU1 is shown in [Figure 15-549](#) and described in [Table 15-1670](#).

Return to [Summary Table](#).

SA Hash Seed PRU1.

Table 15-1669. MII_G_RT_SA_HASH_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3AA4h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3AA4h

Figure 15-549. MII_G_RT_SA_HASH_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						SA_HASH_SEED									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1670. MII_G_RT_SA_HASH_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	SA_HASH_SEED	R/W	0h	SA Hash Seed

Table 15-1671. Register Call Summary for MII_G_RT_SA_HASH_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_SA_HASH_PRU1 Register \(Offset = AA4h\) \[reset = X\]: \[0\]](#)

15.12.132 MII_G_RT_CONN_HASH_PRU1 Register (Offset = AA8h) [reset = X]

MIIG_RT_CONN_HASH_PRU1 is shown in [Figure 15-550](#) and described in [Table 15-1673](#).

Return to [Summary Table](#).

Connection Hash Seed PRU1.

Table 15-1672. MII_G_RT_CONN_HASH_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3AA8h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3AA8h

Figure 15-550. MII_G_RT_CONN_HASH_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						CONN_HASH_SEED									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1673. MII_G_RT_CONN_HASH_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	CONN_HASH_SEED	R/W	0h	Connection Hash Seed

Table 15-1674. Register Call Summary for MII_G_RT_CONN_HASH_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_CONN_HASH_PRU1 Register \(Offset = AA8h\) \[reset = X\]: \[0\]](#)

15.12.133 MII_G_RT_CONN_HASH_START_PRU1 Register (Offset = AACH) [reset = X]

MIIG_RT_CONN_HASH_START_PRU1 is shown in [Figure 15-551](#) and described in [Table 15-1676](#).

Return to [Summary Table](#).

Connection Hash Start PRU1.

Table 15-1675. MII_G_RT_CONN_HASH_START_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3AACH
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3AACH

Figure 15-551. MII_G_RT_CONN_HASH_START_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CONN_HASH_START															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1676. MII_G_RT_CONN_HASH_START_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R/W	X	
14-0	CONN_HASH_START	R/W	0h	Connection Hash Start which 4 Bytes to hash

Table 15-1677. Register Call Summary for MII_G_RT_CONN_HASH_START_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_CONN_HASH_START_PRU1 Register \(Offset = AACH\) \[reset = X\]: \[0\]](#)

15.12.134 MII_G_RT_RX_RATE_CFGn_PRU1 Register (Offset = AB0h + formula) [reset = 0h]

MIIG_RT_RX_RATE_CFGn_PRU1 is shown in [Figure 15-552](#) and described in [Table 15-1679](#).

Return to [Summary Table](#).

RX Rate Configuration Register.

Offset = AB0h + (n * 4h); where n = 0h to 7h

Table 15-1678. MII_G_RT_RX_RATE_CFGn_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3AB0h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3AB0h + formula

Figure 15-552. MII_G_RT_RX_RATE_CFGn_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_RATE_CIR_IDLEn																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1679. MII_G_RT_RX_RATE_CFGn_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RX_RATE_CIR_IDLEn	R/W	0h	RX Rate Peak Information Rate Idle Increment Value - The number added to the PIR counter every clock cycle including EOF. The PIR counter is disabled with a zero value and packets will not be marked RED

Table 15-1680. Register Call Summary for MII_G_RT_RX_RATE_CFGn_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_RATE_CFGn_PRU1 Register \(Offset = AB0h + formula\) \[reset = 0h\]: \[0\]](#)

15.12.135 MII_G_RT_RX_RATE_SRC_SEL0_PRU1 Register (Offset = AD0h) [reset = X]

MIIG_RT_RX_RATE_SRC_SEL0_PRU1 is shown in Figure 15-553 and described in Table 15-1682.

Return to [Summary Table](#).

RX Rate Source Select0.

Table 15-1681. MII_G_RT_RX_RATE_SRC_SEL0_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3AD0h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3AD0h

Figure 15-553. MII_G_RT_RX_RATE_SRC_SEL0_PRU1 Register

31	30	29	28	27	26	25	24
RESERVED				RX_RATE_SRC_SEL3			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				RX_RATE_SRC_SEL2			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				RX_RATE_SRC_SEL1			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				RX_RATE_SRC_SEL0			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1682. MII_G_RT_RX_RATE_SRC_SEL0_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	RX_RATE_SRC_SEL3	R/W	0h	Map which filter/flag/class hit that rate logic uses, see table for mapping
23-22	RESERVED	R/W	X	
21-16	RX_RATE_SRC_SEL2	R/W	0h	Map which filter/flag/class hit that rate logic uses, see table for mapping
15-14	RESERVED	R/W	X	
13-8	RX_RATE_SRC_SEL1	R/W	0h	Map which filter/flag/class hit that rate logic uses, see table for mapping
7-6	RESERVED	R/W	X	
5-0	RX_RATE_SRC_SEL0	R/W	0h	Map which filter/flag/class hit that rate logic uses, see table for mapping

Table 15-1683. Register Call Summary for MII_G_RT_RX_RATE_SRC_SEL0_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_RATE_SRC_SEL0_PRU1 Register \(Offset = AD0h\) \[reset = X\]: \[0\]](#)

15.12.136 MII_G_RT_RX_RATE_SRC_SEL1_PRU1 Register (Offset = AD4h) [reset = X]

MIIG_RT_RX_RATE_SRC_SEL1_PRU1 is shown in Figure 15-554 and described in Table 15-1685.

Return to [Summary Table](#).

RX Rate Source Select1.

Table 15-1684. MII_G_RT_RX_RATE_SRC_SEL1_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3AD4h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3AD4h

Figure 15-554. MII_G_RT_RX_RATE_SRC_SEL1_PRU1 Register

31	30	29	28	27	26	25	24
RESERVED				RX_RATE_SRC_SEL7			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				RX_RATE_SRC_SEL6			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				RX_RATE_SRC_SEL5			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				RX_RATE_SRC_SEL4			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1685. MII_G_RT_RX_RATE_SRC_SEL1_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	RX_RATE_SRC_SEL7	R/W	0h	Map which filter/flag/class hit that rate logic uses, see table for mapping
23-22	RESERVED	R/W	X	
21-16	RX_RATE_SRC_SEL6	R/W	0h	Map which filter/flag/class hit that rate logic uses, see table for mapping
15-14	RESERVED	R/W	X	
13-8	RX_RATE_SRC_SEL5	R/W	0h	Map which filter/flag/class hit that rate logic uses, see table for mapping
7-6	RESERVED	R/W	X	
5-0	RX_RATE_SRC_SEL4	R/W	0h	Map which filter/flag/class hit that rate logic uses, see table for mapping

Table 15-1686. Register Call Summary for MII_G_RT_RX_RATE_SRC_SEL1_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_RATE_SRC_SEL1_PRU1 Register \(Offset = AD4h\) \[reset = X\]: \[0\]](#)

15.12.137 MII_G_RT_TX_RATE_CFG1_n_PRU1 Register (Offset = AD8h + formula) [reset = 0h]

MIIG_RT_TX_RATE_CFG1_n_PRU1 is shown in [Figure 15-555](#) and described in [Table 15-1688](#).

Return to [Summary Table](#).

TX Rate Configuration 1 Register.

Offset = AD8h + (n * 8h); where n = 0h to 7h

Table 15-1687. MII_G_RT_TX_RATE_CFG1_n_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3AD8h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3AD8h + formula

Figure 15-555. MII_G_RT_TX_RATE_CFG1_n_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_RATE_CIR_IDLEn																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1688. MII_G_RT_TX_RATE_CFG1_n_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TX_RATE_CIR_IDLEn	R/W	0h	TX Rate Peak Information Rate Idle Increment Value - The number added to the PIR counter every clock cycle including EOF. The PIR counter is disabled with a zero value and packets will not be marked RED

Table 15-1689. Register Call Summary for MII_G_RT_TX_RATE_CFG1_n_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_RATE_CFG1_n_PRU1 Register \(Offset = AD8h + formula\) \[reset = 0h\]: \[0\]](#)

15.12.138 MII_G_RT_TX_RATE_CFG2_n_PRU1 Register (Offset = ADCh + formula) [reset = X]

MIIG_RT_TX_RATE_CFG2_n_PRU1 is shown in [Figure 15-556](#) and described in [Table 15-1691](#).

Return to [Summary Table](#).

TX Rate Configuration 2 Register.

Offset = ADCh + (n * 8h); where n = 0h to 7h

Table 15-1690. MII_G_RT_TX_RATE_CFG2_n_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3ADCh + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3ADCh + formula

Figure 15-556. MII_G_RT_TX_RATE_CFG2_n_PRU1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						TX_RATE_ALL OWN	TX_RATE_ENn
R/W-X						R-0h	R/W-0h
15	14	13	12	11	10	9	8
TX_RATE_LENn							
R/W-0h							
7	6	5	4	3	2	1	0
TX_RATE_LENn							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-1691. MII_G_RT_TX_RATE_CFG2_n_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17	TX_RATE_ALLOWn	R	0h	TX Rate Pkt Enable
16	TX_RATE_ENn	R/W	0h	TX Rate Pkt Enable
15-0	TX_RATE_LENn	R/W	0h	TX Rate Pkt Length

Table 15-1692. Register Call Summary for MII_G_RT_TX_RATE_CFG2_n_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_RATE_CFG2_n_PRU1 Register \(Offset = ADCh + formula\) \[reset = X\]: \[0\]](#)

15.12.139 MII_G_RT_RX_STAT_GOOD_PRU1 Register (Offset = B18h) [reset = 0h]

MIIG_RT_RX_STAT_GOOD_PRU1 is shown in [Figure 15-557](#) and described in [Table 15-1694](#).

Return to [Summary Table](#).

RX Good Frame Count (PRU1).

Table 15-1693. MII_G_RT_RX_STAT_GOOD_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3B18h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3B18h

Figure 15-557. MII_G_RT_RX_STAT_GOOD_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_GOOD_FRM_CNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1694. MII_G_RT_RX_STAT_GOOD_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RX_GOOD_FRM_CNT	R/W	0h	RX Good Frame Count. increment on none min err max err CRC err odd err, Write to subtract

Table 15-1695. Register Call Summary for MII_G_RT_RX_STAT_GOOD_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_GOOD_PRU1 Register \(Offset = B18h\) \[reset = 0h\]: \[0\]](#)

15.12.140 MII_G_RT_RX_STAT_BC_PRU1 Register (Offset = B1Ch) [reset = X]

MIIG_RT_RX_STAT_BC_PRU1 is shown in [Figure 15-558](#) and described in [Table 15-1697](#).

Return to [Summary Table](#).

RX BC Frame Count (PRU1).

Table 15-1696. MII_G_RT_RX_STAT_BC_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3B1Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3B1Ch

Figure 15-558. MII_G_RT_RX_STAT_BC_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RX_BC_FRM_CNT															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1697. MII_G_RT_RX_STAT_BC_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_BC_FRM_CNT	R/W	0h	RX BC Frame Count increment on BC type, Write to subtract

Table 15-1698. Register Call Summary for MII_G_RT_RX_STAT_BC_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_BC_PRU1 Register \(Offset = B1Ch\) \[reset = X\]: \[0\]](#)

15.12.141 MII_G_RT_RX_STAT_MC_PRU1 Register (Offset = B20h) [reset = X]

MIIG_RT_RX_STAT_MC_PRU1 is shown in Figure 15-559 and described in Table 15-1700.

Return to [Summary Table](#).

RX MC Frame Count (PRU1).

Table 15-1699. MII_G_RT_RX_STAT_MC_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3B20h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3B20h

Figure 15-559. MII_G_RT_RX_STAT_MC_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RX_MC_FRM_CNT															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1700. MII_G_RT_RX_STAT_MC_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_MC_FRM_CNT	R/W	0h	RX MC Frame Count increment on MC type, Write to subtract

Table 15-1701. Register Call Summary for MII_G_RT_RX_STAT_MC_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_MC_PRU1 Register \(Offset = B20h\) \[reset = X\]: \[0\]](#)

15.12.142 MII_G_RT_RX_STAT_CRC_ERR_PRU1 Register (Offset = B24h) [reset = X]

MIIG_RT_RX_STAT_CRC_ERR_PRU1 is shown in [Figure 15-560](#) and described in [Table 15-1703](#).

Return to [Summary Table](#).

RX CRC Error Frame Count (PRU1).

Table 15-1702. MII_G_RT_RX_STAT_CRC_ERR_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3B24h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3B24h

Figure 15-560. MII_G_RT_RX_STAT_CRC_ERR_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_CRC_ERR_FRM_CNT															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1703. MII_G_RT_RX_STAT_CRC_ERR_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_CRC_ERR_FRM_CNT	R/W	0h	RX CRC Err Frame Count increment on CRC error, Write to subtract

Table 15-1704. Register Call Summary for MII_G_RT_RX_STAT_CRC_ERR_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_CRC_ERR_PRU1 Register \(Offset = B24h\) \[reset = X\]: \[0\]](#)

15.12.143 MII_G_RT_RX_STAT_MII_ERR_PRU1 Register (Offset = B28h) [reset = X]

MIIG_RT_RX_STAT_MII_ERR_PRU1 is shown in Figure 15-561 and described in Table 15-1706.

Return to [Summary Table](#).

RX MII Error Frame Count (PRU1).

Table 15-1705. MII_G_RT_RX_STAT_MII_ERR_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3B28h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3B28h

Figure 15-561. MII_G_RT_RX_STAT_MII_ERR_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_MII_ERR_FRM_CNT															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1706. MII_G_RT_RX_STAT_MII_ERR_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_MII_ERR_FRM_CNT	R/W	0h	RX MII Err Frame Count increment on MII, SGMII, RGMII error, Write to subtract

Table 15-1707. Register Call Summary for MII_G_RT_RX_STAT_MII_ERR_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_MII_ERR_PRU1 Register \(Offset = B28h\) \[reset = X\]: \[0\]](#)

15.12.144 MII_G_RT_RX_STAT_ODD_ERR_PRU1 Register (Offset = B2Ch) [reset = X]

MIIG_RT_RX_STAT_ODD_ERR_PRU1 is shown in [Figure 15-562](#) and described in [Table 15-1709](#).

Return to [Summary Table](#).

RX Odd Nibble Frame Count (PRU1).

Table 15-1708. MII_G_RT_RX_STAT_ODD_ERR_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3B2Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3B2Ch

Figure 15-562. MII_G_RT_RX_STAT_ODD_ERR_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_ODD_ERR_FRM_CNT															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1709. MII_G_RT_RX_STAT_ODD_ERR_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_ODD_ERR_FRM_CNT	R/W	0h	RX Odd Nibble Frame Count increment on odd nibble MII, Write to subtract

Table 15-1710. Register Call Summary for MII_G_RT_RX_STAT_ODD_ERR_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_ODD_ERR_PRU1 Register \(Offset = B2Ch\) \[reset = X\]: \[0\]](#)

15.12.145 MII_G_RT_RX_STAT_MAX_SIZE_PRU1 Register (Offset = B30h) [reset = X]

MIIG_RT_RX_STAT_MAX_SIZE_PRU1 is shown in Figure 15-563 and described in Table 15-1712.

Return to [Summary Table](#).

RX Max Size Frame (PRU1).

Table 15-1711. MII_G_RT_RX_STAT_MAX_SIZE_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3B30h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3B30h

Figure 15-563. MII_G_RT_RX_STAT_MAX_SIZE_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RX_MAX_SIZE_FRM															
R/W-X																R/W-7D0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1712. MII_G_RT_RX_STAT_MAX_SIZE_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_MAX_SIZE_FRM	R/W	7D0h	RX MAX Size Frame Count Limit

Table 15-1713. Register Call Summary for MII_G_RT_RX_STAT_MAX_SIZE_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_MAX_SIZE_PRU1 Register \(Offset = B30h\) \[reset = X\]: \[0\]](#)

15.12.146 MII_G_RT_RX_STAT_MAX_ERR_PRU1 Register (Offset = B34h) [reset = X]

MIIG_RT_RX_STAT_MAX_ERR_PRU1 is shown in [Figure 15-564](#) and described in [Table 15-1715](#).

Return to [Summary Table](#).

RX Max Size Error Frame Count (PRU1).

Table 15-1714. MII_G_RT_RX_STAT_MAX_ERR_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3B34h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3B34h

Figure 15-564. MII_G_RT_RX_STAT_MAX_ERR_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_MAX_ERR_FRM_CNT															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1715. MII_G_RT_RX_STAT_MAX_ERR_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_MAX_ERR_FRM_CNT	R/W	0h	RX MAX Size Err Frame Count increment if > than Limit, Write to subtract

Table 15-1716. Register Call Summary for MII_G_RT_RX_STAT_MAX_ERR_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_MAX_ERR_PRU1 Register \(Offset = B34h\) \[reset = X\]: \[0\]](#)

15.12.147 MII_G_RT_RX_STAT_MIN_SIZE_PRU1 Register (Offset = B38h) [reset = X]

MIIG_RT_RX_STAT_MIN_SIZE_PRU1 is shown in Figure 15-565 and described in Table 15-1718.

Return to [Summary Table](#).

RX Min Size Frame (PRU1).

Table 15-1717. MII_G_RT_RX_STAT_MIN_SIZE_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3B38h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3B38h

Figure 15-565. MII_G_RT_RX_STAT_MIN_SIZE_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RX_MIN_SIZE_FRM															
R/W-X																R/W-40h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1718. MII_G_RT_RX_STAT_MIN_SIZE_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_MIN_SIZE_FRM	R/W	40h	RX MIN Size Frame Limit

Table 15-1719. Register Call Summary for MII_G_RT_RX_STAT_MIN_SIZE_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_MIN_SIZE_PRU1 Register \(Offset = B38h\) \[reset = X\]: \[0\]](#)

15.12.148 MII_G_RT_RX_STAT_MIN_ERR_PRU1 Register (Offset = B3Ch) [reset = X]

MIIG_RT_RX_STAT_MIN_ERR_PRU1 is shown in [Figure 15-566](#) and described in [Table 15-1721](#).

Return to [Summary Table](#).

RX Min Size Error Frame Count (PRU1).

Table 15-1720. MII_G_RT_RX_STAT_MIN_ERR_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3B3Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3B3Ch

Figure 15-566. MII_G_RT_RX_STAT_MIN_ERR_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_MIN_ERR_FRM_CNT															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1721. MII_G_RT_RX_STAT_MIN_ERR_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_MIN_ERR_FRM_CNT	R/W	0h	RX MIN Size Frame Count increment if < than limit, Write to subtract

Table 15-1722. Register Call Summary for MII_G_RT_RX_STAT_MIN_ERR_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_MIN_ERR_PRU1 Register \(Offset = B3Ch\) \[reset = X\]: \[0\]](#)

15.12.149 MII_G_RT_RX_STAT_OVERRUN_ERR_PRU1 Register (Offset = B40h) [reset = X]

MIIG_RT_RX_STAT_OVERRUN_ERR_PRU1 is shown in Figure 15-567 and described in Table 15-1724.

Return to [Summary Table](#).

RX Overrun Frame Count (PRU1).

Table 15-1723. MII_G_RT_RX_STAT_OVERRUN_ERR_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3B40h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3B40h

Figure 15-567. MII_G_RT_RX_STAT_OVERRUN_ERR_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_OVERRUN_ERR_FRM_CNT															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1724. MII_G_RT_RX_STAT_OVERRUN_ERR_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_OVERRUN_ERR_FRM_CNT	R/W	0h	RX L1 FIFO overflow Frame Count increment on overflow event, Write to subtract

Table 15-1725. Register Call Summary for MII_G_RT_RX_STAT_OVERRUN_ERR_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_OVERRUN_ERR_PRU1 Register \(Offset = B40h\) \[reset = X\]: \[0\]](#)

15.12.150 MII_G_RT_RX_STAT_CLASSm_HIT_PRU1 Register (Offset = B44h + formula) [reset = 0h]

MIIG_RT_RX_STAT_CLASSm_HIT_PRU1 is shown in [Figure 15-568](#) and described in [Table 15-1727](#).

Return to [Summary Table](#).

RX Class<m>.

Offset = B44h + (m * 4h); where m = 0h to Fh

Table 15-1726. MII_G_RT_RX_STAT_CLASSm_HIT_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3B44h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3B44h + formula

Figure 15-568. MII_G_RT_RX_STAT_CLASSm_HIT_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_STAT_CLASSm_PRU1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1727. MII_G_RT_RX_STAT_CLASSm_HIT_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RX_STAT_CLASSm_PRU1	R/W	0h	RX Class<m> Hit Count (where m = 0 to 15). Write to subtract

Table 15-1728. Register Call Summary for MII_G_RT_RX_STAT_CLASSm_HIT_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_CLASSm_HIT_PRU1 Register \(Offset = B44h + formula\) \[reset = 0h\]: \[0\]](#)

15.12.151 MII_G_RT_RX_STAT_SMD_FRAG_ERR_PRU1 Register (Offset = B84h) [reset = 0h]

MIIG_RT_RX_STAT_SMD_FRAG_ERR_PRU1 is shown in Figure 15-569 and described in Table 15-1730.

Return to [Summary Table](#).

RX SMD Frag Error Count (PRU1).

Table 15-1729. MII_G_RT_RX_STAT_SMD_FRAG_ERR_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3B84h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3B84h

Figure 15-569. MII_G_RT_RX_STAT_SMD_FRAG_ERR_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RX_STAT_SMD_ERR_PRU1								RX_STAT_FRAG_ERR_PRU1							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_STAT_SMD_ERR_PRU1								RX_STAT_SMD_ERR_PRU1							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1730. MII_G_RT_RX_STAT_SMD_FRAG_ERR_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RX_STAT_SMD_ERR_PRU1	R/W	0h	RX SMD Error Count, increment when first none 0x55 does not match any valid SMD, Write to subtract
23-16	RX_STAT_FRAG_ERR_PRU1	R/W	0h	RX Frag_Cnt Seq Error Count, Write to subtract
15-8	RX_STAT_SMD_ERR_PRU1	R/W	0h	RX SMDx Seq Error Count, Write to subtract
7-0	RX_STAT_SMD_ERR_PRU1	R/W	0h	RX SMDx Seq Error Count, Write to subtract

Table 15-1731. Register Call Summary for MII_G_RT_RX_STAT_SMD_FRAG_ERR_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_SMD_FRAG_ERR_PRU1 Register \(Offset = B84h\) \[reset = 0h\]: \[0\]](#)

15.12.152 MII_G_RT_RX_STAT_BKT1_SIZE_PRU1 Register (Offset = B88h) [reset = X]

MIIG_RT_RX_STAT_BKT1_SIZE_PRU1 is shown in Figure 15-570 and described in Table 15-1733.

Return to [Summary Table](#).

RX Bucket1 Size Configuration (PRU1).

Table 15-1732. MII_G_RT_RX_STAT_BKT1_SIZE_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3B88h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3B88h

Figure 15-570. MII_G_RT_RX_STAT_BKT1_SIZE_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		RX_STAT_BKT1_SIZE													
R/W-X		R/W-40h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1733. MII_G_RT_RX_STAT_BKT1_SIZE_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	RX_STAT_BKT1_SIZE	R/W	40h	RX Bucket1 Byte Size

Table 15-1734. Register Call Summary for MII_G_RT_RX_STAT_BKT1_SIZE_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_BKT1_SIZE_PRU1 Register \(Offset = B88h\) \[reset = X\]: \[0\]](#)

15.12.153 MII_G_RT_RX_STAT_BKT2_SIZE_PRU1 Register (Offset = B8Ch) [reset = X]

MIIG_RT_RX_STAT_BKT2_SIZE_PRU1 is shown in Figure 15-571 and described in Table 15-1736.

Return to [Summary Table](#).

RX Bucket2 Size Configuration (PRU1).

Table 15-1735. MII_G_RT_RX_STAT_BKT2_SIZE_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3B8Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3B8Ch

Figure 15-571. MII_G_RT_RX_STAT_BKT2_SIZE_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		RX_STAT_BKT2_SIZE													
R/W-X		R/W-80h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1736. MII_G_RT_RX_STAT_BKT2_SIZE_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	RX_STAT_BKT2_SIZE	R/W	80h	RX Bucket2 Byte Size

Table 15-1737. Register Call Summary for MII_G_RT_RX_STAT_BKT2_SIZE_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_BKT2_SIZE_PRU1 Register \(Offset = B8Ch\) \[reset = X\]: \[0\]](#)

15.12.154 MII_G_RT_RX_STAT_BKT3_SIZE_PRU1 Register (Offset = B90h) [reset = X]

MIIG_RT_RX_STAT_BKT3_SIZE_PRU1 is shown in [Figure 15-572](#) and described in [Table 15-1739](#).

Return to [Summary Table](#).

RX Bucket3 Size Configuration (PRU1).

Table 15-1738. MII_G_RT_RX_STAT_BKT3_SIZE_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3B90h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3B90h

Figure 15-572. MII_G_RT_RX_STAT_BKT3_SIZE_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		RX_STAT_BKT3_SIZE													
R/W-X		R/W-100h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1739. MII_G_RT_RX_STAT_BKT3_SIZE_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	RX_STAT_BKT3_SIZE	R/W	100h	RX Bucket3 Byte Size

Table 15-1740. Register Call Summary for MII_G_RT_RX_STAT_BKT3_SIZE_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_BKT3_SIZE_PRU1 Register \(Offset = B90h\) \[reset = X\]: \[0\]](#)

15.12.155 MII_G_RT_RX_STAT_BKT4_SIZE_PRU1 Register (Offset = B94h) [reset = X]

MIIG_RT_RX_STAT_BKT4_SIZE_PRU1 is shown in Figure 15-573 and described in Table 15-1742.

Return to [Summary Table](#).

RX Bucket4 Size Configuration (PRU1).

Table 15-1741. MII_G_RT_RX_STAT_BKT4_SIZE_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3B94h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3B94h

Figure 15-573. MII_G_RT_RX_STAT_BKT4_SIZE_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		RX_STAT_BKT4_SIZE													
R/W-X		R/W-200h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1742. MII_G_RT_RX_STAT_BKT4_SIZE_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	RX_STAT_BKT4_SIZE	R/W	200h	RX Bucket4 Byte Size

Table 15-1743. Register Call Summary for MII_G_RT_RX_STAT_BKT4_SIZE_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_BKT4_SIZE_PRU1 Register \(Offset = B94h\) \[reset = X\]: \[0\]](#)

15.12.156 MII_G_RT_RX_STAT_64_PRU1 Register (Offset = B98h) [reset = X]

MIIG_RT_RX_STAT_64_PRU1 is shown in [Figure 15-574](#) and described in [Table 15-1745](#).

Return to [Summary Table](#).

RX 64B Sized Frame Count (PRU1).

Table 15-1744. MII_G_RT_RX_STAT_64_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3B98h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3B98h

Figure 15-574. MII_G_RT_RX_STAT_64_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RX_64_FRM_CNT															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1745. MII_G_RT_RX_STAT_64_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_64_FRM_CNT	R/W	0h	RX 64 Byte Frame Count increment if 64 B size

Table 15-1746. Register Call Summary for MII_G_RT_RX_STAT_64_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_64_PRU1 Register \(Offset = B98h\) \[reset = X\]: \[0\]](#)

15.12.157 MII_G_RT_RX_STAT_BKT1_PRU1 Register (Offset = B9Ch) [reset = X]

MIIG_RT_RX_STAT_BKT1_PRU1 is shown in [Figure 15-575](#) and described in [Table 15-1748](#).

Return to [Summary Table](#).

RX Bucket1 Sized Frame Count (PRU1).

Table 15-1747. MII_G_RT_RX_STAT_BKT1_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3B9Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3B9Ch

Figure 15-575. MII_G_RT_RX_STAT_BKT1_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RX_STAT_BKT1															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1748. MII_G_RT_RX_STAT_BKT1_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_STAT_BKT1	R/W	0h	RX Bucket1 Frame Count increment if <= than Bucket1 Byte Size

Table 15-1749. Register Call Summary for MII_G_RT_RX_STAT_BKT1_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_BKT1_PRU1 Register \(Offset = B9Ch\) \[reset = X\]: \[0\]](#)

15.12.158 MII_G_RT_RX_STAT_BKT2_PRU1 Register (Offset = BA0h) [reset = X]

MIIG_RT_RX_STAT_BKT2_PRU1 is shown in [Figure 15-576](#) and described in [Table 15-1751](#).

Return to [Summary Table](#).

RX Bucket2 Sized Frame Count (PRU1).

Table 15-1750. MII_G_RT_RX_STAT_BKT2_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3BA0h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3BA0h

Figure 15-576. MII_G_RT_RX_STAT_BKT2_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RX_STAT_BKT2															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1751. MII_G_RT_RX_STAT_BKT2_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_STAT_BKT2	R/W	0h	RX Bucket2 Frame Count increment if <= than Bucket2 Byte Size and if > than Bucket1 Byte Size

Table 15-1752. Register Call Summary for MII_G_RT_RX_STAT_BKT2_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_BKT2_PRU1 Register \(Offset = BA0h\) \[reset = X\]: \[0\]](#)

15.12.159 MII_G_RT_RX_STAT_BKT3_PRU1 Register (Offset = BA4h) [reset = X]

MIIG_RT_RX_STAT_BKT3_PRU1 is shown in [Figure 15-577](#) and described in [Table 15-1754](#).

Return to [Summary Table](#).

RX Bucket3 Sized Frame Count (PRU1).

Table 15-1753. MII_G_RT_RX_STAT_BKT3_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3BA4h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3BA4h

Figure 15-577. MII_G_RT_RX_STAT_BKT3_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RX_STAT_BKT3															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1754. MII_G_RT_RX_STAT_BKT3_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_STAT_BKT3	R/W	0h	RX Bucket3 Frame Count increment if <= than Bucket3 Byte Size and if > than Bucket2 Byte Size

Table 15-1755. Register Call Summary for MII_G_RT_RX_STAT_BKT3_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_BKT3_PRU1 Register \(Offset = BA4h\) \[reset = X\]: \[0\]](#)

15.12.160 MII_G_RT_RX_STAT_BKT4_PRU1 Register (Offset = BA8h) [reset = X]

MIIG_RT_RX_STAT_BKT4_PRU1 is shown in [Figure 15-578](#) and described in [Table 15-1757](#).

Return to [Summary Table](#).

RX Bucket4 Sized Frame Count (PRU1).

Table 15-1756. MII_G_RT_RX_STAT_BKT4_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3BA8h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3BA8h

Figure 15-578. MII_G_RT_RX_STAT_BKT4_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RX_STAT_BKT4															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1757. MII_G_RT_RX_STAT_BKT4_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_STAT_BKT4	R/W	0h	RX Bucket4 Frame Count increment if <= than Bucket4 Byte Size and if > than Bucket3 Byte Size

Table 15-1758. Register Call Summary for MII_G_RT_RX_STAT_BKT4_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_BKT4_PRU1 Register \(Offset = BA8h\) \[reset = X\]: \[0\]](#)

15.12.161 MII_G_RT_RX_STAT_BKT5_PRU1 Register (Offset = BACH) [reset = X]

MIIG_RT_RX_STAT_BKT5_PRU1 is shown in [Figure 15-579](#) and described in [Table 15-1760](#).

Return to [Summary Table](#).

RX Bucket5 Sized Frame Count (PRU1).

Table 15-1759. MII_G_RT_RX_STAT_BKT5_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3BACH
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3BACH

Figure 15-579. MII_G_RT_RX_STAT_BKT5_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RX_STAT_BKT5															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1760. MII_G_RT_RX_STAT_BKT5_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_STAT_BKT5	R/W	0h	RX Bucket5 Frame Count increment if > than Bucket4 Byte Size

Table 15-1761. Register Call Summary for MII_G_RT_RX_STAT_BKT5_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_BKT5_PRU1 Register \(Offset = BACH\) \[reset = X\]: \[0\]](#)

15.12.162 MII_G_RT_RX_STAT_TOTAL_BYTES_PRU1 Register (Offset = BB0h) [reset = 0h]

MIIG_RT_RX_STAT_TOTAL_BYTES_PRU1 is shown in [Figure 15-580](#) and described in [Table 15-1763](#).

Return to [Summary Table](#).

RX Total Byte Count (PRU1).

Table 15-1762. MII_G_RT_RX_STAT_TOTAL_BYTES_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3BB0h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3BB0h

Figure 15-580. MII_G_RT_RX_STAT_TOTAL_BYTES_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_STAT_TOTAL_BYTES_PRU																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1763. MII_G_RT_RX_STAT_TOTAL_BYTES_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RX_STAT_TOTAL_BYTES_PRU	R/W	0h	RX Total Byte Count

Table 15-1764. Register Call Summary for MII_G_RT_RX_STAT_TOTAL_BYTES_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RX_STAT_TOTAL_BYTES_PRU1 Register \(Offset = BB0h\) \[reset = 0h\]: \[0\]](#)

15.12.163 MII_G_RT_RXTX_STAT_TOTAL_BYTES_PRU1 Register (Offset = BB4h) [reset = 0h]

MIIG_RT_RXTX_STAT_TOTAL_BYTES_PRU1 is shown in Figure 15-581 and described in Table 15-1766.

Return to [Summary Table](#).

RX TX Total Byte Count (PRU1).

Table 15-1765. MII_G_RT_RXTX_STAT_TOTAL_BYTES_PRU1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3BB4h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3BB4h

Figure 15-581. MII_G_RT_RXTX_STAT_TOTAL_BYTES_PRU1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXTX_STAT_TOTAL_BYTES_PRU																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1766. MII_G_RT_RXTX_STAT_TOTAL_BYTES_PRU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RXTX_STAT_TOTAL_BYTES_PRU	R/W	0h	RX and TX Total Byte Count

Table 15-1767. Register Call Summary for MII_G_RT_RXTX_STAT_TOTAL_BYTES_PRU1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_RXTX_STAT_TOTAL_BYTES_PRU1 Register \(Offset = BB4h\) \[reset = 0h\]: \[0\]](#)

15.12.164 MII_G_RT_TX_STAT_GOOD_PORT1 Register (Offset = BB8h) [reset = 0h]

MIIG_RT_TX_STAT_GOOD_PORT1 is shown in [Figure 15-582](#) and described in [Table 15-1769](#).

Return to [Summary Table](#).

TX Good Frame Count Port1.

Table 15-1768. MII_G_RT_TX_STAT_GOOD_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3BB8h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3BB8h

Figure 15-582. MII_G_RT_TX_STAT_GOOD_PORT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_GOOD_FRM_CNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1769. MII_G_RT_TX_STAT_GOOD_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TX_GOOD_FRM_CNT	R/W	0h	TX Good Frame Count increment if no min size err max size err or MII odd nibble

Table 15-1770. Register Call Summary for MII_G_RT_TX_STAT_GOOD_PORT1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_GOOD_PORT1 Register \(Offset = BB8h\) \[reset = 0h\]: \[0\]](#)

15.12.165 MII_G_RT_TX_STAT_BC_PORT1 Register (Offset = BBCh) [reset = X]

MIIG_RT_TX_STAT_BC_PORT1 is shown in [Figure 15-583](#) and described in [Table 15-1772](#).

Return to [Summary Table](#).

TX BC Frame Count Port1.

Table 15-1771. MII_G_RT_TX_STAT_BC_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3BBCh
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3BBCh

Figure 15-583. MII_G_RT_TX_STAT_BC_PORT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_BC_FRM_CNT															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1772. MII_G_RT_TX_STAT_BC_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_BC_FRM_CNT	R/W	0h	TX BC Frame Count increment if BC

Table 15-1773. Register Call Summary for MII_G_RT_TX_STAT_BC_PORT1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_BC_PORT1 Register \(Offset = BBCh\) \[reset = X\]: \[0\]](#)

15.12.166 MII_G_RT_TX_STAT_MC_PORT1 Register (Offset = BC0h) [reset = X]

MIIGRTTXSTATMCPORT1 is shown in [Figure 15-584](#) and described in [Table 15-1775](#).

Return to [Summary Table](#).

TX MC Frame Count Port1.

Table 15-1774. MII_G_RT_TX_STAT_MC_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3BC0h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3BC0h

Figure 15-584. MII_G_RT_TX_STAT_MC_PORT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_MC_FRM_CNT															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1775. MII_G_RT_TX_STAT_MC_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_MC_FRM_CNT	R/W	0h	TX MC Frame Count increment if MC

Table 15-1776. Register Call Summary for MII_G_RT_TX_STAT_MC_PORT1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIGRTTXSTATMCPORT1 Register \(Offset = BC0h\) \[reset = X\]: \[0\]](#)

15.12.167 MII_G_RT_TX_STAT_ODD_ERR_PORT1 Register (Offset = BC4h) [reset = X]

MIIG_RT_TX_STAT_ODD_ERR_PORT1 is shown in [Figure 15-585](#) and described in [Table 15-1778](#).

Return to [Summary Table](#).

TX Odd Nibble Frame Count Port1.

Table 15-1777. MII_G_RT_TX_STAT_ODD_ERR_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3BC4h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3BC4h

Figure 15-585. MII_G_RT_TX_STAT_ODD_ERR_PORT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_ODD_ERR_FRM_CNT															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1778. MII_G_RT_TX_STAT_ODD_ERR_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_ODD_ERR_FRM_CNT	R/W	0h	TX Odd Nibble Frame Count increment if MII odd nibble

Table 15-1779. Register Call Summary for MII_G_RT_TX_STAT_ODD_ERR_PORT1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_ODD_ERR_PORT1 Register \(Offset = BC4h\) \[reset = X\]: \[0\]](#)

15.12.168 MII_G_RT_TX_STAT_UNDERFLOW_ERR_PORT1 Register (Offset = BC8h) [reset = X]

MIIG_RT_TX_STAT_UNDERFLOW_ERR_PORT1 is shown in [Figure 15-586](#) and described in [Table 15-1781](#).

Return to [Summary Table](#).

TX Under Flow Error Count Port1.

Table 15-1780. MII_G_RT_TX_STAT_UNDERFLOW_ERR_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3BC8h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3BC8h

Figure 15-586. MII_G_RT_TX_STAT_UNDERFLOW_ERR_PORT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_UNDERFLOW_CNT															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1781. MII_G_RT_TX_STAT_UNDERFLOW_ERR_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_UNDERFLOW_CNT	R/W	0h	TX MAX Underflow Error Count

Table 15-1782. Register Call Summary for MII_G_RT_TX_STAT_UNDERFLOW_ERR_PORT1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_UNDERFLOW_ERR_PORT1 Register \(Offset = BC8h\) \[reset = X\]: \[0\]](#)

15.12.169 MII_G_RT_TX_STAT_MAX_SIZE_PORT1 Register (Offset = BCCh) [reset = X]

MIIG_RT_TX_STAT_MAX_SIZE_PORT1 is shown in [Figure 15-587](#) and described in [Table 15-1784](#).

Return to [Summary Table](#).

TX Max Size Frame Port1.

Table 15-1783. MII_G_RT_TX_STAT_MAX_SIZE_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3BCCh
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3BCCh

Figure 15-587. MII_G_RT_TX_STAT_MAX_SIZE_PORT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_MAX_SIZE_FRM															
R/W-X																R/W-7D0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1784. MII_G_RT_TX_STAT_MAX_SIZE_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_MAX_SIZE_FRM	R/W	7D0h	TX MAX Size Frame Count Limit

Table 15-1785. Register Call Summary for MII_G_RT_TX_STAT_MAX_SIZE_PORT1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_MAX_SIZE_PORT1 Register \(Offset = BCCh\) \[reset = X\]: \[0\]](#)

15.12.170 MII_G_RT_TX_STAT_MAX_ERR_PORT1 Register (Offset = BD0h) [reset = X]

MIIG_RT_TX_STAT_MAX_ERR_PORT1 is shown in [Figure 15-588](#) and described in [Table 15-1787](#).

Return to [Summary Table](#).

TX Max Size Error Frame Count Port1.

Table 15-1786. MII_G_RT_TX_STAT_MAX_ERR_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3BD0h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3BD0h

Figure 15-588. MII_G_RT_TX_STAT_MAX_ERR_PORT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_MAX_ERR_FRM_CNT															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1787. MII_G_RT_TX_STAT_MAX_ERR_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_MAX_ERR_FRM_CNT	R/W	0h	TX MAX Size Err Frame Count increment if > max Limit

Table 15-1788. Register Call Summary for MII_G_RT_TX_STAT_MAX_ERR_PORT1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_MAX_ERR_PORT1 Register \(Offset = BD0h\) \[reset = X\]: \[0\]](#)

15.12.171 MII_G_RT_TX_STAT_MIN_SIZE_PORT1 Register (Offset = BD4h) [reset = X]

MIIG_RT_TX_STAT_MIN_SIZE_PORT1 is shown in Figure 15-589 and described in Table 15-1790.

Return to [Summary Table](#).

TX Min Size Frame Port1.

Table 15-1789. MII_G_RT_TX_STAT_MIN_SIZE_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3BD4h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3BD4h

Figure 15-589. MII_G_RT_TX_STAT_MIN_SIZE_PORT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_MIN_SIZE_FRM															
R/W-X																R/W-40h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1790. MII_G_RT_TX_STAT_MIN_SIZE_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_MIN_SIZE_FRM	R/W	40h	TX MIN Size Frame Count Limit

Table 15-1791. Register Call Summary for MII_G_RT_TX_STAT_MIN_SIZE_PORT1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_MIN_SIZE_PORT1 Register \(Offset = BD4h\) \[reset = X\]: \[0\]](#)

15.12.172 MII_G_RT_TX_STAT_MIN_ERR_PORT1 Register (Offset = BD8h) [reset = X]

MIIG_RT_TX_STAT_MIN_ERR_PORT1 is shown in [Figure 15-590](#) and described in [Table 15-1793](#).

Return to [Summary Table](#).

TX Min Size Error Frame Count Port1.

Table 15-1792. MII_G_RT_TX_STAT_MIN_ERR_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3BD8h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3BD8h

Figure 15-590. MII_G_RT_TX_STAT_MIN_ERR_PORT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_MIN_ERR_FRM_CNT															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1793. MII_G_RT_TX_STAT_MIN_ERR_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_MIN_ERR_FRM_CNT	R/W	0h	TX MIN Size Err Frame Count increment if < min Limit

Table 15-1794. Register Call Summary for MII_G_RT_TX_STAT_MIN_ERR_PORT1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_MIN_ERR_PORT1 Register \(Offset = BD8h\) \[reset = X\]: \[0\]](#)

15.12.173 MII_G_RT_TX_STAT_BKT1_SIZE_PORT1 Register (Offset = BDCh) [reset = X]

MIIG_RT_TX_STAT_BKT1_SIZE_PORT1 is shown in Figure 15-591 and described in Table 15-1796.

Return to [Summary Table](#).

TX Bucket1 Size Configuration Port1.

Table 15-1795. MII_G_RT_TX_STAT_BKT1_SIZE_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3BDCh
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3BDCh

Figure 15-591. MII_G_RT_TX_STAT_BKT1_SIZE_PORT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TX_STAT_BKT1_SIZE													
R/W-X		R/W-40h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1796. MII_G_RT_TX_STAT_BKT1_SIZE_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TX_STAT_BKT1_SIZE	R/W	40h	TX Bucket1 Byte Size

Table 15-1797. Register Call Summary for MII_G_RT_TX_STAT_BKT1_SIZE_PORT1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_BKT1_SIZE_PORT1 Register \(Offset = BDCh\) \[reset = X\]: \[0\]](#)

15.12.174 MII_G_RT_TX_STAT_BKT2_SIZE_PORT1 Register (Offset = BE0h) [reset = X]

MIIG_RT_TX_STAT_BKT2_SIZE_PORT1 is shown in Figure 15-592 and described in Table 15-1799.

Return to [Summary Table](#).

TX Bucket2 Size Configuration Port1.

Table 15-1798. MII_G_RT_TX_STAT_BKT2_SIZE_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3BE0h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3BE0h

Figure 15-592. MII_G_RT_TX_STAT_BKT2_SIZE_PORT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TX_STAT_BKT2_SIZE													
R/W-X		R/W-80h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1799. MII_G_RT_TX_STAT_BKT2_SIZE_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TX_STAT_BKT2_SIZE	R/W	80h	TX Bucket2 Byte Size

Table 15-1800. Register Call Summary for MII_G_RT_TX_STAT_BKT2_SIZE_PORT1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_BKT2_SIZE_PORT1 Register \(Offset = BE0h\) \[reset = X\]: \[0\]](#)

15.12.175 MII_G_RT_TX_STAT_BKT3_SIZE_PORT1 Register (Offset = BE4h) [reset = X]

MIIG_RT_TX_STAT_BKT3_SIZE_PORT1 is shown in Figure 15-593 and described in Table 15-1802.

Return to [Summary Table](#).

TX Bucket3 Size Configuration Port1.

Table 15-1801. MII_G_RT_TX_STAT_BKT3_SIZE_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3BE4h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3BE4h

Figure 15-593. MII_G_RT_TX_STAT_BKT3_SIZE_PORT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TX_STAT_BKT3_SIZE													
R/W-X		R/W-100h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1802. MII_G_RT_TX_STAT_BKT3_SIZE_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TX_STAT_BKT3_SIZE	R/W	100h	TX Bucket3 Byte Size

Table 15-1803. Register Call Summary for MII_G_RT_TX_STAT_BKT3_SIZE_PORT1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_BKT3_SIZE_PORT1 Register \(Offset = BE4h\) \[reset = X\]: \[0\]](#)

15.12.176 MII_G_RT_TX_STAT_BKT4_SIZE_PORT1 Register (Offset = BE8h) [reset = X]

MIIG_RT_TX_STAT_BKT4_SIZE_PORT1 is shown in Figure 15-594 and described in Table 15-1805.

Return to [Summary Table](#).

TX Bucket4 Size Configuration Port1.

Table 15-1804. MII_G_RT_TX_STAT_BKT4_SIZE_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3BE8h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3BE8h

Figure 15-594. MII_G_RT_TX_STAT_BKT4_SIZE_PORT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TX_STAT_BKT4_SIZE													
R/W-X		R/W-200h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1805. MII_G_RT_TX_STAT_BKT4_SIZE_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TX_STAT_BKT4_SIZE	R/W	200h	TX Bucket4 Byte Size

Table 15-1806. Register Call Summary for MII_G_RT_TX_STAT_BKT4_SIZE_PORT1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_BKT4_SIZE_PORT1 Register \(Offset = BE8h\) \[reset = X\]: \[0\]](#)

15.12.177 MII_G_RT_TX_STAT_64_PORT1 Register (Offset = BECh) [reset = X]

MIIG_RT_TX_STAT_64_PORT1 is shown in Figure 15-595 and described in Table 15-1808.

Return to [Summary Table](#).

TX 64B Sized Frame Count Port1.

Table 15-1807. MII_G_RT_TX_STAT_64_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3BECh
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3BECh

Figure 15-595. MII_G_RT_TX_STAT_64_PORT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_64_FRM_CNT															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1808. MII_G_RT_TX_STAT_64_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_64_FRM_CNT	R/W	0h	TX 64 Byte Frame Count increment if 64 B

Table 15-1809. Register Call Summary for MII_G_RT_TX_STAT_64_PORT1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_64_PORT1 Register \(Offset = BECh\) \[reset = X\]: \[0\]](#)

15.12.178 MII_G_RT_TX_STAT_BKT1_PORT1 Register (Offset = BF0h) [reset = X]

MIIG_RT_TX_STAT_BKT1_PORT1 is shown in [Figure 15-596](#) and described in [Table 15-1811](#).

Return to [Summary Table](#).

TX Bucket1 Sized Frame Count Port1.

Table 15-1810. MII_G_RT_TX_STAT_BKT1_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3BF0h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3BF0h

Figure 15-596. MII_G_RT_TX_STAT_BKT1_PORT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_STAT_BKT1															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1811. MII_G_RT_TX_STAT_BKT1_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_STAT_BKT1	R/W	0h	TX Bucket1 increment if <= than Bucket1

Table 15-1812. Register Call Summary for MII_G_RT_TX_STAT_BKT1_PORT1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_BKT1_PORT1 Register \(Offset = BF0h\) \[reset = X\]: \[0\]](#)

15.12.179 MII_G_RT_TX_STAT_BKT2_PORT1 Register (Offset = BF4h) [reset = X]

MIIG_RT_TX_STAT_BKT2_PORT1 is shown in [Figure 15-597](#) and described in [Table 15-1814](#).

Return to [Summary Table](#).

TX Bucket2 Sized Frame Count Port1.

Table 15-1813. MII_G_RT_TX_STAT_BKT2_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3BF4h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3BF4h

Figure 15-597. MII_G_RT_TX_STAT_BKT2_PORT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_STAT_BKT2															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1814. MII_G_RT_TX_STAT_BKT2_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_STAT_BKT2	R/W	0h	TX Bucket2 increment if <= than Bucket2 Byte Size and if > than Bucket1 Byte Size

Table 15-1815. Register Call Summary for MII_G_RT_TX_STAT_BKT2_PORT1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_BKT2_PORT1 Register \(Offset = BF4h\) \[reset = X\]: \[0\]](#)

15.12.180 MII_G_RT_TX_STAT_BKT3_PORT1 Register (Offset = BF8h) [reset = X]

MIIG_RT_TX_STAT_BKT3_PORT1 is shown in [Figure 15-598](#) and described in [Table 15-1817](#).

Return to [Summary Table](#).

TX Bucket3 Sized Frame Count Port1.

Table 15-1816. MII_G_RT_TX_STAT_BKT3_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3BF8h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3BF8h

Figure 15-598. MII_G_RT_TX_STAT_BKT3_PORT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_STAT_BKT3															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1817. MII_G_RT_TX_STAT_BKT3_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_STAT_BKT3	R/W	0h	TX Bucket3 increment if <= than Bucket3 Byte Size and if > than Bucket2 Byte Size

Table 15-1818. Register Call Summary for MII_G_RT_TX_STAT_BKT3_PORT1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_BKT3_PORT1 Register \(Offset = BF8h\) \[reset = X\]: \[0\]](#)

15.12.181 MII_G_RT_TX_STAT_BKT4_PORT1 Register (Offset = BFCh) [reset = X]

MIIG_RT_TX_STAT_BKT4_PORT1 is shown in [Figure 15-599](#) and described in [Table 15-1820](#).

Return to [Summary Table](#).

TX Bucket4 Sized Frame Count Port1.

Table 15-1819. MII_G_RT_TX_STAT_BKT4_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3BFCh
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3BFCh

Figure 15-599. MII_G_RT_TX_STAT_BKT4_PORT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_STAT_BKT4															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1820. MII_G_RT_TX_STAT_BKT4_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_STAT_BKT4	R/W	0h	TX Bucket4 increment if <= than Bucket4 Byte Size and if > than Bucket3 Byte Size

Table 15-1821. Register Call Summary for MII_G_RT_TX_STAT_BKT4_PORT1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_BKT4_PORT1 Register \(Offset = BFCh\) \[reset = X\]: \[0\]](#)

15.12.182 MII_G_RT_TX_STAT_BKT5_PORT1 Register (Offset = C00h) [reset = X]

MIIG_RT_TX_STAT_BKT5_PORT1 is shown in [Figure 15-600](#) and described in [Table 15-1823](#).

Return to [Summary Table](#).

TX Bucket5 Sized Frame Count Port1.

Table 15-1822. MII_G_RT_TX_STAT_BKT5_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3C00h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3C00h

Figure 15-600. MII_G_RT_TX_STAT_BKT5_PORT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_STAT_BKT5															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1823. MII_G_RT_TX_STAT_BKT5_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_STAT_BKT5	R/W	0h	TX Bucket5 increment if > than Bucket4 Byte Size

Table 15-1824. Register Call Summary for MII_G_RT_TX_STAT_BKT5_PORT1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_BKT5_PORT1 Register \(Offset = C00h\) \[reset = X\]: \[0\]](#)

15.12.183 MII_G_RT_TX_STAT_TOTAL_BYTES_PORT1 Register (Offset = C04h) [reset = 0h]

MIIG_RT_TX_STAT_TOTAL_BYTES_PORT1 is shown in [Figure 15-601](#) and described in [Table 15-1826](#).

Return to [Summary Table](#).

TX Total Byte Count Port1.

Table 15-1825. MII_G_RT_TX_STAT_TOTAL_BYTES_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3C04h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3C04h

Figure 15-601. MII_G_RT_TX_STAT_TOTAL_BYTES_PORT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_TOTAL_STAT_BYTES_PORT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1826. MII_G_RT_TX_STAT_TOTAL_BYTES_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TX_TOTAL_STAT_BYTES_PORT	R/W	0h	TX Total Byte Count of all Frames

Table 15-1827. Register Call Summary for MII_G_RT_TX_STAT_TOTAL_BYTES_PORT1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_STAT_TOTAL_BYTES_PORT1 Register \(Offset = C04h\) \[reset = 0h\]: \[0\]](#)

15.12.184 MII_G_RT_TX_HSR_TAG_PORT1 Register (Offset = C08h) [reset = 892Fh]

MIIG_RT_TX_HSR_TAG_PORT1 is shown in [Figure 15-602](#) and described in [Table 15-1829](#).

Return to [Summary Table](#).

TX HSR TAG Port1.

Table 15-1828. MII_G_RT_TX_HSR_TAG_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3C08h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3C08h

Figure 15-602. MII_G_RT_TX_HSR_TAG_PORT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_HSR_TAG																															
R/W-892Fh																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1829. MII_G_RT_TX_HSR_TAG_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TX_HSR_TAG	R/W	892Fh	HSR TAG

Table 15-1830. Register Call Summary for MII_G_RT_TX_HSR_TAG_PORT1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_HSR_TAG_PORT1 Register \(Offset = C08h\) \[reset = 892Fh\]: \[0\]](#)

15.12.185 MII_G_RT_TX_HSR_SEQ_PORT1 Register (Offset = C0Ch) [reset = X]

MIIG_RT_TX_HSR_SEQ_PORT1 is shown in Figure 15-603 and described in Table 15-1832.

Return to [Summary Table](#).

TX HSR Seq Port1.

Table 15-1831. MII_G_RT_TX_HSR_SEQ_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3C0Ch
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3C0Ch

Figure 15-603. MII_G_RT_TX_HSR_SEQ_PORT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_HSR_SEQ															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1832. MII_G_RT_TX_HSR_SEQ_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_HSR_SEQ	R/W	0h	HSR Seq count. It will increment for every HSR type

Table 15-1833. Register Call Summary for MII_G_RT_TX_HSR_SEQ_PORT1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_HSR_SEQ_PORT1 Register \(Offset = C0Ch\) \[reset = X\]: \[0\]](#)

15.12.186 MII_G_RT_TX_VLAN_TYPE_TAG_PORT1 Register (Offset = C10h) [reset = X]

MIIG_RT_TX_VLAN_TYPE_TAG_PORT1 is shown in [Figure 15-604](#) and described in [Table 15-1835](#).

Return to [Summary Table](#).

TX VLAN Type TAG Port1.

Table 15-1834. MII_G_RT_TX_VLAN_TYPE_TAG_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3C10h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3C10h

Figure 15-604. MII_G_RT_TX_VLAN_TYPE_TAG_PORT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_VLAN_TYPE_TAG															
R/W-X																R/W-81h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1835. MII_G_RT_TX_VLAN_TYPE_TAG_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_VLAN_TYPE_TAG	R/W	81h	TX VLAN Type Tag, match to enable VLAN removal

Table 15-1836. Register Call Summary for MII_G_RT_TX_VLAN_TYPE_TAG_PORT1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_VLAN_TYPE_TAG_PORT1 Register \(Offset = C10h\) \[reset = X\]: \[0\]](#)

15.12.187 MII_G_RT_TX_VLAN_INS_TAG_PORT1 Register (Offset = C14h) [reset = 1h]

MIIG_RT_TX_VLAN_INS_TAG_PORT1 is shown in [Figure 15-605](#) and described in [Table 15-1838](#).

Return to [Summary Table](#).

TX VLAN Insertion TAG Port1.

Table 15-1837. MII_G_RT_TX_VLAN_INS_TAG_PORT1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3C14h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3C14h

Figure 15-605. MII_G_RT_TX_VLAN_INS_TAG_PORT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_VLAN_INS_TAG																															
R/W-1h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1838. MII_G_RT_TX_VLAN_INS_TAG_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TX_VLAN_INS_TAG	R/W	1h	TX VLAN Insertion

Table 15-1839. Register Call Summary for MII_G_RT_TX_VLAN_INS_TAG_PORT1

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_TX_VLAN_INS_TAG_PORT1 Register \(Offset = C14h\) \[reset = 1h\]: \[0\]](#)

15.12.188 MII_G_RT_QUEUEk Register (Offset = D00h + formula) [reset = X]

MIIG_RT_QUEUEk is shown in [Figure 15-606](#) and described in [Table 15-1841](#).

Return to [Summary Table](#).

Queue<k>.

Offset = D00h + (k * 4h); where k = 0h to 3Fh

Table 15-1840. MII_G_RT_QUEUEk Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3D00h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3D00h + formula

Figure 15-606. MII_G_RT_QUEUEk Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																QUEUE_H_PTRk															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1841. MII_G_RT_QUEUEk Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	QUEUE_H_PTRk	R/W	0h	Queue <k> (where k = 0 to 63).

Table 15-1842. Register Call Summary for MII_G_RT_QUEUEk

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_QUEUEk Register \(Offset = D00h + formula\) \[reset = X\]: \[0\]](#)

15.12.189 MII_G_RT_QUEUE_PEEKm Register (Offset = E00h + formula) [reset = X]

MIIG_RT_QUEUE_PEEKm is shown in [Figure 15-607](#) and described in [Table 15-1844](#).

Return to [Summary Table](#).

Queue Peek<m>

Offset = E00h + (m * 4h); where m = 0h to Fh

Table 15-1843. MII_G_RT_QUEUE_PEEKm Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3E00h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3E00h + formula

Figure 15-607. MII_G_RT_QUEUE_PEEKm Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QUEUE_H_PEEK_PTRm															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 15-1844. MII_G_RT_QUEUE_PEEKm Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	QUEUE_H_PEEK_PTRm	R	0h	Queue <m> Peek portal (where m = 0 to 15).

Table 15-1845. Register Call Summary for MII_G_RT_QUEUE_PEEKm

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_QUEUE_PEEKm Register \(Offset = E00h + formula\) \[reset = X\]: \[0\]](#)

15.12.190 MII_G_RT_QUEUE_CNTk Register (Offset = E40h + formula) [reset = 0h]

MIIG_RT_QUEUE_CNTk is shown in [Figure 15-608](#) and described in [Table 15-1847](#).

Return to [Summary Table](#).

Queue Count<k>

Offset = E40h + (k * 4h); where k = 0h to 3Fh

Table 15-1846. MII_G_RT_QUEUE_CNTk Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3E40h + formula
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3E40h + formula

Figure 15-608. MII_G_RT_QUEUE_CNTk Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QUEUE_CNT_ENTRIESk															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 15-1847. MII_G_RT_QUEUE_CNTk Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	QUEUE_CNT_ENTRIESk	R	0h	Queue Entry Count<k> (where k = 0 to 63).

Table 15-1848. Register Call Summary for MII_G_RT_QUEUE_CNTk

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_QUEUE_CNTk Register \(Offset = E40h + formula\) \[reset = 0h\]: \[0\]](#)

15.12.191 MII_G_RT_QUEUE_RESET Register (Offset = F40h) [reset = 0h]

MIIG_RT_QUEUE_RESET is shown in [Figure 15-609](#) and described in [Table 15-1850](#).

Return to [Summary Table](#).

Queue Reset

Table 15-1849. MII_G_RT_QUEUE_RESET Instances

Instance	Physical Address
PRU_ICSSG0_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B03 3F40h
PRU_ICSSG1_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G	0B13 3F40h

Figure 15-609. MII_G_RT_QUEUE_RESET Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										RESET_QUEUE_ID					
R/W-0h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-1850. MII_G_RT_QUEUE_RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-0	RESET_QUEUE_ID	R/W	0h	Reset Queue ID.

Table 15-1851. Register Call Summary for MII_G_RT_QUEUE_RESET

PRU_MII_G_RT_MII_G_RT Registers

- [MIIG_RT_QUEUE_RESET Register \(Offset = F40h\) \[reset = 0h\]: \[0\]](#)

15.13 PRU_SGMII_SGMII Registers

Table 15-1853 lists the memory-mapped registers for the PRU_SGMII_SGMII registers. All register offset addresses not listed in Table 15-1853 should be considered as reserved locations and the register contents should not be modified.

Note

SGMII mode is supported only for PRU_ICSSG1 instance.

Table 15-1852. PRU_SGMII_SGMII Instances

Instance	Base Address
PRU_ICSSG1_PR1_MII_RT_PR1_SGMII0_CFG_SGMII0	0B13 2100h
PRU_ICSSG1_PR1_MII_RT_PR1_SGMII1_CFG_SGMII1	0B13 2200h

Table 15-1853. PRU_SGMII_SGMII Registers

Offset	Acronym	Register Name	PRU_ICSSG1_P R1_MII_RT_PR1 _SGMII0_CFG_S GMII0 Physical Address	PRU_ICSSG1_P R1_MII_RT_PR1 _SGMII1_CFG_ SGMII1 Physical Address
0h	SGMII_IDVER_REG	Identification and Version Register	0B13 2100h	0B13 2200h
4h	SGMII_SOFT_RESET_REG	Software Reset Register	0B13 2104h	0B13 2204h
10h	SGMII_CONTROL_REG	Control Register	0B13 2110h	0B13 2210h
14h	SGMII_STATUS_REG	Status Register	0B13 2114h	0B13 2214h
18h	SGMII_MR_ADV_ABILITY_REG	Advertised Ability Register	0B13 2118h	0B13 2218h
1Ch	SGMII_MR_NP_TX_REG	Next Page Transmit Register	0B13 211Ch	0B13 221Ch
20h	SGMII_MR_LP_ADV_ABILITY_REG	Link Partner Advertised Ability Register	0B13 2120h	0B13 2220h
24h	SGMII_MR_LP_NP_RX_REG	Link Partner Next Page Received Register	0B13 2124h	0B13 2224h
30h	SGMII_TX_CFG_REG	Transmit Configuration Register	0B13 2130h	0B13 2230h
34h	SGMII_RX_CFG_REG	Receive Configuration Register	0B13 2134h	0B13 2234h
38h	SGMII_AUX_CFG_REG	Auxiliary Configuration Register	0B13 2138h	0B13 2238h
40h	SGMII_DIAG_CLEAR_REG	Diagnostics Clear Register	0B13 2140h	0B13 2240h
44h	SGMII_DIAG_CONTROL_REG	Diagnostics Control Register	0B13 2144h	0B13 2244h
48h	SGMII_DIAG_STATUS_REG	Diagnostics Status Register	0B13 2148h	0B13 2248h

15.13.1 SGMII_IDVER_REG Register (Offset = 0h) [reset = 4EC20902h]

SGMII_IDVER_REG is shown in [Figure 15-610](#) and described in [Table 15-1855](#).

[Return to Summary Table.](#)

Identification and Version Register.

Table 15-1854. SGMII_IDVER_REG Instances

Instance	Physical Address
PRU_ICSSG1_PR1_MII_RT_PR1_SGMII0_CFG_SGMII0	0B13 2100h
PRU_ICSSG1_PR1_MII_RT_PR1_SGMII1_CFG_SGMII1	0B13 2200h

Figure 15-610. SGMII_IDVER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TX_IDENT															
R-4EC2h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL_VER					MAJOR_VER					MINOR_VER					
R-1h					R-1h					R-2h					

LEGEND: R = Read Only; -n = value after reset

Table 15-1855. SGMII_IDVER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TX_IDENT	R	4EC2h	TX Identification Value
15-11	RTL_VER	R	1h	RTL version value
10-8	MAJOR_VER	R	1h	Major Version Value
7-0	MINOR_VER	R	2h	Minor Version Value

Table 15-1856. Register Call Summary for SGMII_IDVER_REG

PRU_SGMII_SGMII Registers

- [PRU_SGMII_SGMII Registers](#): [0]
- [SGMII_IDVER_REG Register \(Offset = 0h\) \[reset = 4EC20902h\]](#): [0]

15.13.2 SGMII_SOFT_RESET_REG Register (Offset = 4h) [reset = X]

SGMII_SOFT_RESET_REG is shown in [Figure 15-611](#) and described in [Table 15-1858](#).

Return to [Summary Table](#).

Software reset register.

Table 15-1857. SGMII_SOFT_RESET_REG Instances

Instance	Physical Address
PRU_ICSSG1_PR1_MII_RT_PR1_SGMII0_CFG_SGMII0	0B13 2104h
PRU_ICSSG1_PR1_MII_RT_PR1_SGMII1_CFG_SGMII1	0B13 2204h

Figure 15-611. SGMII_SOFT_RESET_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						RT_SOFT_RESET	SOFT_RESET
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1858. SGMII_SOFT_RESET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	RT_SOFT_RESET	R/W	0h	Transmit and Receive Software Reset. Writing a one to this bit causes the CPSGMII transmit and receive logic to be in the reset condition (the vbusp_clk domain is not reset). The reset condition is removed when a zero is written to this bit. This bit is intended to be used when changing between loopback mode and normal mode of operation. Note: This bit is not supported.
0	SOFT_RESET	R/W	0h	Software Reset. Writing a one to this bit causes the CPSGMII logic to be reset. Software reset occurs immediately. This bit reads as a zero. Note: This bit is not supported.

Table 15-1859. Register Call Summary for SGMII_SOFT_RESET_REG

SGMII Mode Of Operation
CPSGMII Loopback: [0] [1] [2]
PRU_SGMII_SGMII Registers
- SGMII_SOFT_RESET_REG Register (Offset = 4h) [reset = X]: [0] - PRU_SGMII_SGMII Registers: [0]

15.13.3 SGMII_CONTROL_REG Register (Offset = 10h) [reset = X]

SGMII_CONTROL_REG is shown in Figure 15-612 and described in Table 15-1861.

Return to [Summary Table](#).

Control Register.

Table 15-1860. SGMII_CONTROL_REG Instances

Instance	Physical Address
PRU_ICSSG1_PR1_MII_RT_PR1_SGMII0_CFG_SGMII0	0B13 2110h
PRU_ICSSG1_PR1_MII_RT_PR1_SGMII1_CFG_SGMII1	0B13 2210h

Figure 15-612. SGMII_CONTROL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED	TEST_PATTERN_EN	MASTER	LOOPBACK	MR_NP_LOAD_ED	FAST_LINK_TIMER	MR_AN_REST_ART	MR_AN_ENABLE
R/W-X	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1861. SGMII_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R/W	X	
6	TEST_PATTERN_EN	R/W	0h	Test Pattern Enable. Force the output of K28.5 on TX_ENC for test purposes. 0h = Normal operation 1h = Forced K28.5 on transmit output
5	MASTER	R/W	0h	Master Mode. 0h = Slave Mode 1h = Master mode – Set to one for one side of a direct connection. When this bit is set, the control logic uses the SGMII_MR_ADV_ABILITY_REG register to determine speed and duplexity instead of the SGMII_MR_LP_ADV_ABILITY_REG register. Master mode allows a CPSGMII direct connection with auto-negotiation or with a forced link.
4	LOOPBACK	R/W	0h	Loopback mode. 0h = Not in internal loopback mode 1h = Internal loopback mode. The transmit clock (TX_CLK) is used for transmit and receive.

Table 15-1861. SGMII_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	MR_NP_LOADED	R/W	0h	Next Page Loaded. Writing a one to this bit informs the auto-negotiation process that the next page register has been loaded. This bit is cleared by the auto-negotiation state machine before the SGMII_STATUS_REG [3] MR_PAGE_RX status bit is set. This bit is not used when the SGMII_MODE input is asserted.
2	FAST_LINK_TIMER	R/W	0h	Fast Link Timer. 0h = The link timer value is 10ms in FIBER mode and 1.6ms in SGMII mode. 1h = The link timer value is 2us in FIBER and SGMII mode. This is included for test purposes.
1	MR_AN_RESTART	R/W	0h	Auto-Negotiation Restart. Writing a one and then a zero to this bit causes the auto-negotiation process to be restarted.
0	MR_AN_ENABLE	R/W	0h	Auto-Negotiation Enable. Writing a one to this bit enables the auto-negotiation process.

Table 15-1862. Register Call Summary for SGMII_CONTROL_REG

SGMII Mode Of Operation
• CPSGMII Mode - CPGMAC to PHY: [0] • CPSGMII Loopback: [0] [1] [2] • SGMII Mode - CPGMAC to CPGMAC (generic MAC) with forced link: [0] • SGMII Mode - CPGMAC to CPGMAC (with auto-negotiation): [0] [1] • Fiber Mode - CPGMAC to PHY: [0]
PRU_SGMII_SGMII Registers
• PRU_SGMII_SGMII Registers: [0] • SGMII_CONTROL_REG Register (Offset = 10h) [reset = X]: [0]

15.13.4 SGMII_STATUS_REG Register (Offset = 14h) [reset = X]

SGMII_STATUS_REG is shown in Figure 15-613 and described in Table 15-1864.

Return to [Summary Table](#).

Status Register.

Table 15-1863. SGMII_STATUS_REG Instances

Instance	Physical Address
PRU_ICSSG1_PR1_MII_RT_PR1_SGMII0_CFG_SGMII0	0B13 2114h
PRU_ICSSG1_PR1_MII_RT_PR1_SGMII1_CFG_SGMII1	0B13 2214h

Figure 15-613. SGMII_STATUS_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED		FIB_SIG_DETECT	LOCK	MR_PAGE_RX	MR_AN_COMPLETE	AN_ERROR	LINK
R-X		R-X	R-X	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 15-1864. SGMII_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	X	
5	FIB_SIG_DETECT	R	X	Fiber Signal Detect. This is the FIB_SIG_DETECT input pin.
4	LOCK	R	X	Lock. This is the LOCK input pin. Indicates that the SERDES PLL is locked.
3	MR_PAGE_RX	R	0h	Next Page Received. This bit is set to one by the auto-negotiation state machine when the next page has been received. This bit is cleared to zero by a host write of a one to the mr_np_loaded bit in the Control register. This value is not valid until the lock status bit is asserted.
2	MR_AN_COMPLETE	R	0h	Auto-negotiation complete. This value is not valid until the lock status bit is asserted. 0h = Auto-negotiation is not complete 1h = Auto-negotiation is completed.

Table 15-1864. SGMII_STATUS_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	AN_ERROR	R	0h	Auto-negotiation error. For SGMII mode, an autonegotiation error occurs when halfduplex gigabit is commanded. For FIBER mode, an autonegotiation error occurs if both sides cannot be full duplex. This value is not valid until the lock status bit is asserted. 0h = No auto-negotiation error 1h = Auto-negotiation error
0	LINK	R	0h	Link indicator. This value is not valid until the lock status bit is asserted. 0h = Link is not up. 1h = Link is up.

Table 15-1865. Register Call Summary for SGMII_STATUS_REG

SGMII Mode Of Operation

- [CPSGMII Mode - CPGMAC to PHY: \[0\] \[1\]](#)
- [SGMII Mode - CPGMAC to CPGMAC \(generic MAC\) with forced link: \[0\]](#)
- [SGMII Mode - CPGMAC to CPGMAC \(with auto-negotiation\): \[0\] \[1\] \[2\]](#)
- [Fiber Mode - CPGMAC to PHY: \[0\] \[1\]](#)

PRU_SGMII_SGMII Registers

- [SGMII_STATUS_REG Register \(Offset = 14h\) \[reset = X\]: \[0\]](#)
- [PRU_SGMII_SGMII Registers: \[0\]](#)
- [SGMII_CONTROL_REG Register \(Offset = 10h\) \[reset = X\]: \[0\]](#)

15.13.5 SGMII_MR_ADV_ABILITY_REG Register (Offset = 18h) [reset = X]

SGMII_MR_ADV_ABILITY_REG is shown in Figure 15-614 and described in Table 15-1867.

Return to [Summary Table](#).

Advertised Ability Register.

Table 15-1866. SGMII_MR_ADV_ABILITY_REG Instances

Instance	Physical Address
PRU_ICSSG1_PR1_MII_RT_PR1_SGMII0_CFG_SGMII0	0B13 2118h
PRU_ICSSG1_PR1_MII_RT_PR1_SGMII1_CFG_SGMII1	0B13 2218h

Figure 15-614. SGMII_MR_ADV_ABILITY_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																MR_ADV_ABILITY															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1867. SGMII_MR_ADV_ABILITY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	MR_ADV_ABILITY	R/W	0h	Advertised Ability. When in FIBER mode, this value corresponds to the mr_adv_ability[16:1] in the IEEE specification and is loaded into the IEEE specification tx_config_reg[15:0]. When in SGMII mode, this value corresponds to the tx_config_reg[15:0] register value in the Serial-GMII specification.

Table 15-1868. Register Call Summary for SGMII_MR_ADV_ABILITY_REG

SGMII Mode Of Operation
- CPSGMII Mode - CPGMAC to PHY: [0] - SGMII Mode - CPGMAC to CPGMAC (generic MAC) with forced link: [0] - SGMII Mode - CPGMAC to CPGMAC (with auto-negotiation): [0] [1] - Fiber Mode - CPGMAC to PHY: [0]
PRU_SGMII_SGMII Registers
- SGMII_MR_ADV_ABILITY_REG Register (Offset = 18h) [reset = X]: [0] - PRU_SGMII_SGMII Registers: [0] - SGMII_CONTROL_REG Register (Offset = 10h) [reset = X]: [0]

15.13.6 SGMII_MR_NP_TX_REG Register (Offset = 1Ch) [reset = X]

SGMII_MR_NP_TX_REG is shown in [Figure 15-615](#) and described in [Table 15-1870](#).

Return to [Summary Table](#).

Next Page Transmit Register.

Table 15-1869. SGMII_MR_NP_TX_REG Instances

Instance	Physical Address
PRU_ICSSG1_PR1_MII_RT_PR1_SGMII0_CFG_SGMII0	0B13 211Ch
PRU_ICSSG1_PR1_MII_RT_PR1_SGMII1_CFG_SGMII1	0B13 221Ch

Figure 15-615. SGMII_MR_NP_TX_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																MR_NP_TX															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1870. SGMII_MR_NP_TX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	MR_NP_TX	R/W	0h	Next Page Transmit. This value corresponds to the mr_np_tx[16:1] value in the IEEE specification. Next page is used only in FIBER mode.

Table 15-1871. Register Call Summary for SGMII_MR_NP_TX_REG

PRU_SGMII_SGMII Registers

- [SGMII_MR_NP_TX_REG Register \(Offset = 1Ch\) \[reset = X\]: \[0\]](#)
- [PRU_SGMII_SGMII Registers: \[0\]](#)

15.13.7 SGMII_MR_LP_ADV_ABILITY_REG Register (Offset = 20h) [reset = X]

SGMII_MR_LP_ADV_ABILITY_REG is shown in [Figure 15-616](#) and described in [Table 15-1873](#).

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Link Partner Advertised Ability Register.

Table 15-1872. SGMII_MR_LP_ADV_ABILITY_REG Instances

Instance	Physical Address
PRU_ICSSG1_PR1_MII_RT_PR1_SGMII0_CFG_SGMII0	0B13 2120h
PRU_ICSSG1_PR1_MII_RT_PR1_SGMII1_CFG_SGMII1	0B13 2220h

Figure 15-616. SGMII_MR_LP_ADV_ABILITY_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MR_LP_ADV_ABILITY															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 15-1873. SGMII_MR_LP_ADV_ABILITY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	MR_LP_ADV_ABILITY	R	0h	Link Partner Advertised Ability. readable when auto-negotiation is complete. When in FIBER mode, this value corresponds to the mr_lp_adv_ability[16:1] in the IEEE. When in SGMII mode, this value corresponds to the tx_config_reg[15:0] register value in the Serial-GMII specification.

Table 15-1874. Register Call Summary for SGMII_MR_LP_ADV_ABILITY_REG

SGMII Mode Of Operation
Fiber Mode - CPGMAC to PHY: [0]
PRU_SGMII_SGMII Registers
SGMII_MR_LP_ADV_ABILITY_REG Register (Offset = 20h) [reset = X]: [0] PRU_SGMII_SGMII Registers: [0] SGMII_CONTROL_REG Register (Offset = 10h) [reset = X]: [0]

15.13.8 SGMII_MR_LP_NP_RX_REG Register (Offset = 24h) [reset = X]

SGMII_MR_LP_NP_RX_REG is shown in [Figure 15-617](#) and described in [Table 15-1876](#).

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Link Partner Next Page Received Register.

**Table 15-1875. SGMII_MR_LP_NP_RX_REG
Instances**

Instance	Physical Address
PRU_ICSSG1_PR1_MII_RT_PR1_SGM II0_CFG_SGMII0	0B13 2124h
PRU_ICSSG1_PR1_MII_RT_PR1_SGM II1_CFG_SGMII1	0B13 2224h

Figure 15-617. SGMII_MR_LP_NP_RX_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																MR_LP_NP_RX															
R-X																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 15-1876. SGMII_MR_LP_NP_RX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	MR_LP_NP_RX	R	0h	Link Partner Next Page Received. Readable when the next page is received. These bits are as defined in the IEEE 802.3 standard. Next page is used only in FIBER mode.

Table 15-1877. Register Call Summary for SGMII_MR_LP_NP_RX_REG

PRU_SGMII_SGMII Registers

- [SGMII_MR_LP_NP_RX_REG Register \(Offset = 24h\) \[reset = X\]: \[0\]](#)
- [PRU_SGMII_SGMII Registers: \[0\]](#)

15.13.9 SGMII_TX_CFG_REG Register (Offset = 30h) [reset = 0h]

SGMII_TX_CFG_REG is shown in [Figure 15-618](#) and described in [Table 15-1879](#).

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Transmit Configuration Register.

Table 15-1878. SGMII_TX_CFG_REG Instances

Instance	Physical Address
PRU_ICSSG1_PR1_MII_RT_PR1_SGMII0_CFG_SGMII0	0B13 2130h
PRU_ICSSG1_PR1_MII_RT_PR1_SGMII1_CFG_SGMII1	0B13 2230h

Figure 15-618. SGMII_TX_CFG_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_CFG																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1879. SGMII_TX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TX_CFG	R/W	0h	Transmit configuration register output

Table 15-1880. Register Call Summary for SGMII_TX_CFG_REG

PRU_SGMII_SGMII Registers
- SGMII_TX_CFG_REG Register (Offset = 30h) [reset = 0h]: [0] - PRU_SGMII_SGMII Registers: [0]

15.13.10 SGMII_RX_CFG_REG Register (Offset = 34h) [reset = 0h]

SGMII_RX_CFG_REG is shown in [Figure 15-619](#) and described in [Table 15-1882](#).

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Receive Configuration Register.

Table 15-1881. SGMII_RX_CFG_REG Instances

Instance	Physical Address
PRU_ICSSG1_PR1_MII_RT_PR1_SGMII0_CFG_SGMII0	0B13 2134h
PRU_ICSSG1_PR1_MII_RT_PR1_SGMII1_CFG_SGMII1	0B13 2234h

Figure 15-619. SGMII_RX_CFG_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_CFG																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1882. SGMII_RX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RX_CFG	R/W	0h	Receive configuration register output

Table 15-1883. Register Call Summary for SGMII_RX_CFG_REG

- PRU_SGMII_SGMII Registers
- [SGMII_RX_CFG_REG Register \(Offset = 34h\) \[reset = 0h\]: \[0\]](#)
 - [PRU_SGMII_SGMII Registers: \[0\]](#)

15.13.11 SGMII_AUX_CFG_REG Register (Offset = 38h) [reset = 0h]

SGMII_AUX_CFG_REG is shown in Figure 15-620 and described in Table 15-1885.

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Auxiliary Configuration Register.

Table 15-1884. SGMII_AUX_CFG_REG Instances

Instance	Physical Address
PRU_ICSSG1_PR1_MII_RT_PR1_SGMII0_CFG_SGMII0	0B13 2138h
PRU_ICSSG1_PR1_MII_RT_PR1_SGMII1_CFG_SGMII1	0B13 2238h

Figure 15-620. SGMII_AUX_CFG_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AUX_CFG																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1885. SGMII_AUX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	AUX_CFG	R/W	0h	Auxiliary configuration register output

Table 15-1886. Register Call Summary for SGMII_AUX_CFG_REG

PRU_SGMII_SGMII Registers

- [PRU_SGMII_SGMII Registers: \[0\]](#)
- [SGMII_AUX_CFG_REG Register \(Offset = 38h\) \[reset = 0h\]: \[0\]](#)

15.13.12 SGMII_DIAG_CLEAR_REG Register (Offset = 40h) [reset = X]

SGMII_DIAG_CLEAR_REG is shown in [Figure 15-621](#) and described in [Table 15-1888](#).

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Diagnostics Clear Register.

Table 15-1887. SGMII_DIAG_CLEAR_REG Instances

Instance	Physical Address
PRU_ICSSG1_PR1_MII_RT_PR1_SGMII0_CFG_SGMII0	0B13 2140h
PRU_ICSSG1_PR1_MII_RT_PR1_SGMII1_CFG_SGMII1	0B13 2240h

Figure 15-621. SGMII_DIAG_CLEAR_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							DIAG_CLEAR
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1888. SGMII_DIAG_CLEAR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	DIAG_CLEAR	R/W	0h	Diagnostics Clear. Clears all diagnostic status bits when set to one. Some bits may be set back to one immediately following reset. The reset requires several clocks due to synchronizers.

Table 15-1889. Register Call Summary for SGMII_DIAG_CLEAR_REG

PRU_SGMII_SGMII Registers

- [SGMII_DIAG_CLEAR_REG Register \(Offset = 40h\) \[reset = X\]: \[0\]](#)
- [PRU_SGMII_SGMII Registers: \[0\]](#)

15.13.13 SGMII_DIAG_CONTROL_REG Register (Offset = 44h) [reset = X]

SGMII_DIAG_CONTROL_REG is shown in [Figure 15-622](#) and described in [Table 15-1891](#).

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Diagnostics Control Register.

Table 15-1890. SGMII_DIAG_CONTROL_REG Instances

Instance	Physical Address
PRU_ICSSG1_PR1_MII_RT_PR1_SGM II0_CFG_SGMII0	0B13 2144h
PRU_ICSSG1_PR1_MII_RT_PR1_SGM II1_CFG_SGMII1	0B13 2244h

Figure 15-622. SGMII_DIAG_CONTROL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED	DIAG_SM_SEL			RESERVED	DIAG_EDGE_SEL		
R/W-X	R/W-0h			R/W-X	R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1891. SGMII_DIAG_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R/W	X	
6-4	DIAG_SM_SEL	R/W	0h	Diagnostic Select. Determines which internal diagnostic bits are muxed onto SGMII_DIAG_STATUS_REG [15-0] DIAG_STATUS. 0h = Reserved 1h = Diagnostic Hold Signals 2h = Diagnostic Sync Status (sync_sm state machine) 3h = Diagnostic AN Status (amsm state machine) 4h = Diagnostic TXOS Status (txos state machine) 5h = Diagnostic TXCG Status (txcg state machine) 6h = Diagnostic RXSM Status (rxsm state machine lower bits) 7h = Diagnostic RXSM Status (rxsm state machine upper bits)
3-2	RESERVED	R/W	X	
1-0	DIAG_EDGE_SEL	R/W	0h	Diagnostic Hold Signals Edge Select 0h = Diagnostic Hold Signals Level 1h = Diagnostic Hold Signals rising edge detected 2h = Diagnostic Hold Signals falling edge detected 3h = Diagnostic Hold Signals ether (both) edge detected

Table 15-1892. Register Call Summary for SGMII_DIAG_CONTROL_REG

PRU_SGMII_SGMII Registers

- [SGMII_DIAG_CONTROL_REG Register \(Offset = 44h\) \[reset = X\]: \[0\]](#)
- [PRU_SGMII_SGMII Registers: \[0\]](#)

15.13.14 SGMII_DIAG_STATUS_REG Register (Offset = 48h) [reset = X]

SGMII_DIAG_STATUS_REG is shown in Figure 15-623 and described in Table 15-1894.

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Diagnostics Status Register.

Table 15-1893. SGMII_DIAG_STATUS_REG Instances

Instance	Physical Address
PRU_ICSSG1_PR1_MII_RT_PR1_SGMII0_CFG_SGMII0	0B13 2148h
PRU_ICSSG1_PR1_MII_RT_PR1_SGMII1_CFG_SGMII1	0B13 2248h

Figure 15-623. SGMII_DIAG_STATUS_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DIAG_STATUS															
R-X																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 15-1894. SGMII_DIAG_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	DIAG_STATUS	R	0h	Diagnostics Status

Table 15-1895. Register Call Summary for SGMII_DIAG_STATUS_REG

PRU_SGMII_SGMII Registers

- [SGMII_DIAG_CONTROL_REG Register \(Offset = 44h\) \[reset = X\]: \[0\]](#)
- [SGMII_DIAG_STATUS_REG Register \(Offset = 48h\) \[reset = X\]: \[0\]](#)
- [PRU_SGMII_SGMII Registers: \[0\]](#)

15.14 PRU_ICSSG_PA_STAT Registers

Table 15-1897 lists the PRU_ICSSG_PA_STAT registers. All register offset addresses not listed in Table 15-1897 should be considered as reserved locations and the register contents should not be modified.

Control registers

Table 15-1896. PRU_ICSSG_PA_STAT Instances

Instance	Base Address
PRU_ICSSG0_PA_STAT_WRAP_PA_SLV	0B03 C000h
PRU_ICSSG1_PA_STAT_WRAP_PA_SLV	0B13 C000h

Table 15-1897. PRU_ICSSG_PA_STAT Registers

Offset	Acronym	Register Name	PRU_ICSSG0_PA_STAT_WRAP_PA_SLV Physical Address	PRU_ICSSG1_PA_STAT_WRAP_PA_SLV Physical Address
0h	ICSSG_PA_STAT_REVID	Revision Register	0B03 C000h	0B13 C000h
4h	ICSSG_PA_STAT_SRESET	Soft Reset Register	0B03 C004h	0B13 C004h
8h	ICSSG_PA_STAT_EAC	Enable and Allocation Control Register	0B03 C008h	0B13 C008h
10h	ICSSG_PA_STAT_TCTL	Timer Control Register	0B03 C010h	0B13 C010h
14h	ICSSG_PA_STAT_TLD	Timer Load Register	0B03 C014h	0B13 C014h
18h	ICSSG_PA_STAT_TVL	Timer Value Register	0B03 C018h	0B13 C018h

15.14.1 ICSSG_PA_STAT_REVID Register (Offset = 0h) [reset = 0EF50100h]

ICSSG_PA_STAT_REVID is shown in [Figure 15-624](#) and described in [Table 15-1899](#).

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The Revision Register contains the ID and revision information.

Table 15-1898. ICSSG_PA_STAT_REVID Instances

Instance	Physical Address
PRU_ICSSG0_PA_STAT_WRAP_PA_S LV	0B03 C000h
PRU_ICSSG1_PA_STAT_WRAP_PA_S LV	0B13 C000h

Figure 15-624. ICSSG_PA_STAT_REVID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVID																															
R-0EF50100h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-1899. ICSSG_PA_STAT_REVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REVID	R	0EF50100h	Module ID and revision information.

Table 15-1900. Register Call Summary for ICSSG_PA_STAT_REVID

PRU_ICSSG_PA_STAT Registers

- [ICSSG_PA_STAT_REVID Register \(Offset = 0h\) \[reset = 0EF50100h\]: \[0\]](#)
- [PRU_ICSSG_PA_STAT Registers: \[0\]](#)

15.14.2 ICSSG_PA_STAT_SRESET Register (Offset = 4h) [reset = 0h]

ICSSG_PA_STAT_SRESET is shown in [Figure 15-625](#) and described in [Table 15-1902](#).

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The Soft Reset Register is written in order to clear the contents of all statistics.

Table 15-1901. ICSSG_PA_STAT_SRESET Instances

Instance	Physical Address
PRU_ICSSG0_PA_STAT_WRAP_PA_S LV	0B03 C004h
PRU_ICSSG1_PA_STAT_WRAP_PA_S LV	0B13 C004h

Figure 15-625. ICSSG_PA_STAT_SRESET Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRIGGER																															
W-0h																															

LEGEND: W = Write Only; -n = value after reset

Table 15-1902. ICSSG_PA_STAT_SRESET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TRIGGER	W	0h	Writing anything to this field causes the command FIFOs to be emptied, all statistics to be cleared and all bit masks to be reset to 1. The write to this register will be acknowledged (wready will be asserted) after the reset process is completed.

Table 15-1903. Register Call Summary for ICSSG_PA_STAT_SRESET

PRU_ICSSG_PA_STAT Registers

- [ICSSG_PA_STAT_SRESET Register \(Offset = 4h\) \[reset = 0h\]: \[0\]](#)
- [PRU_ICSSG_PA_STAT Registers: \[0\]](#)

15.14.3 ICSSG_PA_STAT_EAC Register (Offset = 8h) [reset = X]

ICSSG_PA_STAT_EAC is shown in [Figure 15-626](#) and described in [Table 15-1905](#).

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The register contains the enable for the engine and controls the allocation of 64-bit counters in the memory. It is possible to configure the engine to only have 32-bit counters by setting the 64-bit cnt field to zero.

Table 15-1904. ICSSG_PA_STAT_EAC Instances

Instance	Physical Address
PRU_ICSSG0_PA_STAT_WRAP_PA_S LV	0B03 C008h
PRU_ICSSG1_PA_STAT_WRAP_PA_S LV	0B13 C008h

Figure 15-626. ICSSG_PA_STAT_EAC Register

31	30	29	28	27	26	25	24
ENABLE	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED		CNT					
R/W-X		R/W-200h					
7	6	5	4	3	2	1	0
CNT							
R/W-200h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1905. ICSSG_PA_STAT_EAC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE	R/W	0h	Enables stat engine. If the module is not in enabled state, no stats increment is processed and both input and output streaming interfaces are disabled.
30-14	RESERVED	R/W	X	Always read as 0. Writes have no effect.
13-0	CNT	R/W	200h	Defines the number of 64-bit counters in the memory (must be even number). If this number multiplied by 8-byte is less than 4 KB (stats memory space), then the remaining space is allocated for 32-bit counters.

Table 15-1906. Register Call Summary for ICSSG_PA_STAT_EAC

PRU_ICSSG_PA_STAT Registers

- [ICSSG_PA_STAT_EAC Register \(Offset = 8h\) \[reset = X\]: \[0\]](#)
- [PRU_ICSSG_PA_STAT Registers: \[0\]](#)

15.14.4 ICSSG_PA_STAT_TCTL Register (Offset = 10h) [reset = X]

ICSSG_PA_STAT_TCTL is shown in [Figure 15-627](#) and described in [Table 15-1908](#).

Return to the [Summary Table](#).

The Control Timer Register controls a 16-bit timer.

Table 15-1907. ICSSG_PA_STAT_TCTL Instances

Instance	Physical Address
PRU_ICSSG0_PA_STAT_WRAP_PA_S LV	0B03 C010h
PRU_ICSSG1_PA_STAT_WRAP_PA_S LV	0B13 C010h

Figure 15-627. ICSSG_PA_STAT_TCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLK_EN	RESERVED						
R/W-0h	R/W-X						
7	6	5	4	3	2	1	0
RESERVED		PRE_VAL				RESERVED	
R/W-X		R/W-0h				R/W-X	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1908. ICSSG_PA_STAT_TCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	Always read as 0. Writes have no effect.
15	CLK_EN	R/W	0h	0 = Disable prescaler 1 = Enable prescaler
14-6	RESERVED	R/W	X	Always read as 0. Writes have no effect.
5-2	PRE_VAL	R/W	0h	0000 Divide by 2 0001 Divide by 4 0010 Divide by 8 0011 Divide by 16 0100 Divide by 32 0101 Divide by 64 0110 Divide by 128 0111 Divide by 256 1000 Divide by 512 1001 Divide by 1024 1010 Divide by 2048 1011 Divide by 1024 1100 Divide by 8192 1101 Disable timer 1110 Disable timer 1111 Disable timer
1-0	RESERVED	R/W	X	Always read as 0. Writes have no effect.

Table 15-1909. Register Call Summary for ICSSG_PA_STAT_TCTL

PRU_ICSSG_PA_STAT Registers

- [PRU_ICSSG_PA_STAT Registers: \[0\]](#)
- [ICSSG_PA_STAT_TCTL Register \(Offset = 10h\) \[reset = X\]: \[0\]](#)

15.14.5 ICSSG_PA_STAT_TLD Register (Offset = 14h) [reset = X]

ICSSG_PA_STAT_TLD is shown in [Figure 15-628](#) and described in [Table 15-1911](#).

Return to the [Summary Table](#).

The Load Timer Register contains the starting count down value for the 16-bit timer. This register should be written with some value before the timer is started by write on the timer control register.

Table 15-1910. ICSSG_PA_STAT_TLD Instances

Instance	Physical Address
PRU_ICSSG0_PA_STAT_WRAP_PA_S LV	0B03 C014h
PRU_ICSSG1_PA_STAT_WRAP_PA_S LV	0B13 C014h

Figure 15-628. ICSSG_PA_STAT_TLD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LOAD_VAL															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1911. ICSSG_PA_STAT_TLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	Always read as 0. Writes have no effect.
15-0	LOAD_VAL	R/W	0h	16-bit timer value.

Table 15-1912. Register Call Summary for ICSSG_PA_STAT_TLD

PRU_ICSSG_PA_STAT Registers

- [PRU_ICSSG_PA_STAT Registers: \[0\]](#)
- [ICSSG_PA_STAT_TLD Register \(Offset = 14h\) \[reset = X\]: \[0\]](#)

15.14.6 ICSSG_PA_STAT_TVL Register (Offset = 18h) [reset = X]

ICSSG_PA_STAT_TVL is shown in [Figure 15-629](#) and described in [Table 15-1914](#).

Return to the [Summary Table](#).

The Timer Value Register contains the current value of the timer.

Table 15-1913. ICSSG_PA_STAT_TVL Instances

Instance	Physical Address
PRU_ICSSG0_PA_STAT_WRAP_PA_S LV	0B03 C018h
PRU_ICSSG1_PA_STAT_WRAP_PA_S LV	0B13 C018h

Figure 15-629. ICSSG_PA_STAT_TVL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CUR_VAL															
R-X																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 15-1914. ICSSG_PA_STAT_TVL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	Always read as 0. Writes have no effect.
15-0	CUR_VAL	R	0h	Current value of the 16-bit timer.

Table 15-1915. Register Call Summary for ICSSG_PA_STAT_TVL

PRU_ICSSG_PA_STAT Registers

- [ICSSG_PA_STAT_TVL Register \(Offset = 18h\) \[reset = X\]: \[0\]](#)
- [PRU_ICSSG_PA_STAT Registers: \[0\]](#)

15.15 PRU_ICSSG_PA_STAT_QSTAT Registers

Table 15-1917 lists the PRU_ICSSG_PA_STAT_QSTAT registers. All register offset addresses not listed in Table 15-1917 should be considered as reserved locations and the register contents should not be modified.

Statics query mode RAM stores statistic values

**Table 15-1916. PRU_ICSSG_PA_STAT_QSTAT
Instances**

Instance	Base Address
PRU_ICSSG0_PA_STAT_WRAP_PA_SLV_QSTAT	0B02 7000h
PRU_ICSSG1_PA_STAT_WRAP_PA_SLV_QSTAT	0B12 7000h

Table 15-1917. PRU_ICSSG_PA_STAT_QSTAT Registers

Offset	Acronym	Register Name	PRU_ICSSG0_PA_STAT_WRAP_PA_SLV_QSTAT Physical Address	PRU_ICSSG1_PA_STAT_WRAP_PA_SLV_QSTAT Physical Address
0h + formula	ICSSG_PA_STAT_QRAM_n	32-bit Statistics (Query Mode)	0B02 7000h + formula	0B12 7000h + formula

15.15.1 ICSSG_PA_STAT_QRAM_n Register (Offset = 0h + formula) [reset = 0h]

ICSSG_PA_STAT_QRAM_n is shown in [Figure 15-630](#) and described in [Table 15-1919](#).

Return to the [Summary Table](#).

Query mode RAM.

Reading directly to a particular statistics memory address returns the current statistics values. In query mode, the stats are not reset after the read completes. To accommodate debug, setting a counter value in the stats memory via the register write is also allowed. However, if there is a stat bump and a register write on the same stat that occur simultaneously, the value in the register write may be ignored.

"n" is the number of 32-bit stats that are supported in the module.

Offset = 0h + (n * 4h); where n = 0h to 3FFh

Table 15-1918. ICSSG_PA_STAT_QRAM_n Instances

Instance	Physical Address
PRU_ICSSG0_PA_STAT_WRAP_PA_S LV_QSTAT	0B02 7000h + formula
PRU_ICSSG1_PA_STAT_WRAP_PA_S LV_QSTAT	0B12 7000h + formula

Figure 15-630. ICSSG_PA_STAT_QRAM_n Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1919. ICSSG_PA_STAT_QRAM_n Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VALUE	R/W	0h	Query statistic. 32-bit statistic value at counter "n".

Table 15-1920. Register Call Summary for ICSSG_PA_STAT_QRAM_n

PRU_ICSSG_PA_STAT_QSTAT Registers

- [ICSSG_PA_STAT_QRAM_n Register \(Offset = 0h + formula\) \[reset = 0h\]: \[0\]](#)
- [PRU_ICSSG_PA_STAT_QSTAT Registers: \[0\]](#)

15.16 PRU_ICSSG_PA_STAT_CSTAT Registers

Table 15-1922 lists the PRU_ICSSG_PA_STAT_CSTAT registers. All register offset addresses not listed in Table 15-1922 should be considered as reserved locations and the register contents should not be modified.

Statics collect mode RAM stores statistic values

**Table 15-1921. PRU_ICSSG_PA_STAT_CSTAT
Instances**

Instance	Base Address
PRU_ICSSG0_PA_STAT_WRAP_PA_SLV_CSTAT	0B02 C000h
PRU_ICSSG1_PA_STAT_WRAP_PA_SLV_CSTAT	0B12 C000h

Table 15-1922. PRU_ICSSG_PA_STAT_CSTAT Registers

Offset	Acronym	Register Name	PRU_ICSSG0_PA_STAT_WRAP_PA_SLV_CSTAT Physical Address	PRU_ICSSG1_PA_STAT_WRAP_PA_SLV_CSTAT Physical Address
0h + formula	ICSSG_PA_STAT_CRAM_n	32-bit Statistics (Collect Mode)	0B02 C000h + formula	0B12 C000h + formula

15.16.1 ICSSG_PA_STAT_CRAM_n Register (Offset = 0h + formula) [reset = 0h]

ICSSG_PA_STAT_CRAM_n is shown in [Figure 15-631](#) and described in [Table 15-1924](#).

Return to the [Summary Table](#).

Collect mode RAM.

Reading directly to a particular statistics memory address returns the current statistics values. In collect mode, the stats are reset to 0 after the read completes. To accommodate debug, setting a counter value in the stats memory via the register write is also allowed. However, if there is a stat bump and a register write on the same stat that occur simultaneously, the value in the register write may be ignored.

"n" is the number of 32-bit stats that are supported in the module.

Offset = 0h + (n * 4h); where n = 0h to 3FFh

Table 15-1923. ICSSG_PA_STAT_CRAM_n Instances

Instance	Physical Address
PRU_ICSSG0_PA_STAT_WRAP_PA_S LV_CSTAT	0B02 C000h + formula
PRU_ICSSG1_PA_STAT_WRAP_PA_S LV_CSTAT	0B12 C000h + formula

Figure 15-631. ICSSG_PA_STAT_CRAM_n Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1924. ICSSG_PA_STAT_CRAM_n Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VALUE	R/W	0h	Collect statistic. 32-bit statistic value at counter "n".

Table 15-1925. Register Call Summary for ICSSG_PA_STAT_CRAM_n

PRU_ICSSG_PA_STAT_CSTAT Registers

- [ICSSG_PA_STAT_CRAM_n Register \(Offset = 0h + formula\) \[reset = 0h\]: \[0\]](#)
- [PRU_ICSSG_PA_STAT_CSTAT Registers: \[0\]](#)

15.17 PRU_PROT_PROTECT Registers

Table 15-1927 lists the memory-mapped registers for the PRU_PROT_PROTECT registers. All register offset addresses not listed in Table 15-1927 should be considered as reserved locations and the register contents should not be modified.

Table 15-1926. PRU_PROT_PROTECT Instances

Instance	Base Address
PRU_ICSSG0_PR1_PROT_SLV	0x0B02 4C00h
PRU_ICSSG1_PR1_PROT_SLV	0x0B12 4C00h

Table 15-1927. PRU_PROT_PROTECT Registers

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_PROT_SLV Physical Address	PRU_ICSSG1_PR1_PROT_SLV Physical Address
0h	PROT_UNLOCK_KEY	Unlock key	0B02 4C00h	0B12 4C00h
4h	PROT_CFG	Config	0B02 4C04h	0B12 4C04h

15.17.1 PROT_UNLOCK_KEY Register (Offset = 0h) [reset = 0h]

PROT_UNLOCK_KEY is shown in Figure 15-632 and described in Table 15-1929.

Return to [Summary Table](#).

Unlock key

Table 15-1928. PROT_UNLOCK_KEY Instances

Instance	Physical Address
PRU_ICSSG0_PR1_PROT_SLV	0B02 4C00h
PRU_ICSSG1_PR1_PROT_SLV	0B12 4C00h

Figure 15-632. PROT_UNLOCK_KEY Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UNLOCK_KEY																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1929. PROT_UNLOCK_KEY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	UNLOCK_KEY	R/W	0h	UnLock Key Pattern. 0x83E7_0B13 to UnLock. 0x0000_0000 to Lock. Unlock enables update of registers.

Table 15-1930. Register Call Summary for PROT_UNLOCK_KEY

PRU_ICSSG Top Level Resources Functional Description
PRU_ICSSG Protect: [0]
PRU_PROT_PROTECT Registers
PRU_PROT_PROTECT Registers: [0] PROT_UNLOCK_KEY Register (Offset = 0h) [reset = 0h]: [0]

15.17.2 PROT_CFG Register (Offset = 4h) [reset = X]

PROT_CFG is shown in [Figure 15-633](#) and described in [Table 15-1932](#).

Return to [Summary Table](#).

Config

Table 15-1931. PROT_CFG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_PROT_SLV	0B02 4C04h
PRU_ICSSG1_PR1_PROT_SLV	0B12 4C04h

Figure 15-633. PROT_CFG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED	PRU1_DMEM1_LOCK_EN	PRU0_DMEM0_LOCK_EN	ICSS_CFG_WP_EN	RTU1_PRU_WP_EN	RTU0_PRU_WP_EN	PRU1_WP_EN	PRU0_WP_EN
R/W-X	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1932. PROT_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R/W	X	
6	PRU1_DMEM1_LOCK_EN	R/W	0h	Write Protect DMEM1 0: disable 1: enable When enabled only PRU1 can write to DMEM1
5	PRU0_DMEM0_LOCK_EN	R/W	0h	Write Protect DMEM0 0: disable 1: enable When enabled only PRU0 can write to DMEM0
4	ICSS_CFG_WP_EN	R/W	0h	Write Protect ICSS_CFG 0: disable 1: enable
3	RTU1_PRU_WP_EN	R/W	0h	Write Protect RTU1_PRU access Debug IMEM 0: disable 1: enable
2	RTU0_PRU_WP_EN	R/W	0h	Write Protect RTU0_PRU access Debug IMEM 0: disable 1: enable
1	PRU1_WP_EN	R/W	0h	Write Protect PRU1 and TX_PRU1 access Debug IMEM 0: disable 1: enable
0	PRU0_WP_EN	R/W	0h	Write Protect PRU0 and TX_PRU0 access Debug IMEM 0: disable 1: enable

Table 15-1933. Register Call Summary for PROT_CFG

PRU_ICSSG Top Level Resources Functional Description • PRU_ICSSG Protect: [0]
PRU_PROT_PROTECT Registers • PRU_PROT_PROTECT Registers: [0] • PROT_CFG Register (Offset = 4h) [reset = X]: [0]

15.18 PRU_RAT_SLICE_RAT_SLICE Registers

Table 15-1935 lists the memory-mapped registers for the PRU_RAT_SLICE_RAT_SLICE registers. All register offset addresses not listed in Table 15-1935 should be considered as reserved locations and the register contents should not be modified.

**Table 15-1934. PRU_RAT_SLICE_RAT_SLICE
Instances**

Instance	Base Address
PRU_ICSSG0_RAT_SLICE0_CFG	0B00 8000h
PRU_ICSSG0_RAT_SLICE1_CFG	0B00 9000h
PRU_ICSSG1_RAT_SLICE0_CFG	0B10 8000h
PRU_ICSSG1_RAT_SLICE1_CFG	0B10 9000h

Table 15-1935. PRU_ICSSG0_RAT_SLICE Registers

Offset	Acronym	Register Name	PRU_ICSSG0_RAT_SLICE0_CFG Physical Address	PRU_ICSSG0_RAT_SLICE1_CFG Physical Address
0h	RAT_SLICE_PID	Revision Register	0B00 8000h	0B00 9000h
4h	RAT_SLICE_CONFIG	Config Register	0B00 8004h	0B00 9004h
20h + formula	RAT_SLICE_CTRL_j	Region Control Register	0B00 8020h + formula	0B00 9020h + formula
24h + formula	RAT_SLICE_BASE_j	Region Base Register	0B00 8024h + formula	0B00 9024h + formula
28h + formula	RAT_SLICE_TRANS_L_j	Region Translated Lower Address	0B00 8028h + formula	0B00 9028h + formula
2Ch + formula	RAT_SLICE_TRANS_U_j	Region Translated Upper Address	0B00 802Ch + formula	0B00 902Ch + formula
804h	RAT_SLICE_DESTINATION_ID	Destination ID Register	0B00 8804h	0B00 9804h
820h	RAT_SLICE_EXCEPTION_LOGGING_CONTROL	Exception Logging Control Register	0B00 8820h	0B00 9820h
824h	RAT_SLICE_EXCEPTION_LOGGING_HEADER0	Exception Logging Header 0 Register	0B00 8824h	0B00 9824h
828h	RAT_SLICE_EXCEPTION_LOGGING_HEADER1	Exception Logging Header 1 Register	0B00 8828h	0B00 9828h
82Ch	RAT_SLICE_EXCEPTION_LOGGING_DATA0	Exception Logging Data 0 Register	0B00 882Ch	0B00 982Ch
830h	RAT_SLICE_EXCEPTION_LOGGING_DATA1	Exception Logging Data 1 Register	0B00 8830h	0B00 9830h
834h	RAT_SLICE_EXCEPTION_LOGGING_DATA2	Exception Logging Data 2 Register	0B00 8834h	0B00 9834h
838h	RAT_SLICE_EXCEPTION_LOGGING_DATA3	Exception Logging Data 3 Register	0B00 8838h	0B00 9838h
840h	RAT_SLICE_EXCEPTION_PEND_SET	Exception Logging Interrupt Pending Set Register	0B00 8840h	0B00 9840h
844h	RAT_SLICE_EXCEPTION_PEND_CLEAR	Exception Logging Interrupt Pending Clear Register	0B00 8844h	0B00 9844h
848h	RAT_SLICE_EXCEPTION_ENABLE_SET	Exception Logging Interrupt Enable Set Register	0B00 8848h	0B00 9848h
84Ch	RAT_SLICE_EXCEPTION_ENABLE_CLEAR	Exception Logging Interrupt Enable Clear Register	0B00 884Ch	0B00 984Ch
850h	RAT_SLICE_EOI_REG	EOI Register	0B00 8850h	0B00 9850h

Table 15-1936. PRU_ICSSG1_RAT_SLICE Registers

Offset	Acronym	Register Name	PRU_ICSSG1_RAT_SLICE0_CFG Physical Address	PRU_ICSSG1_RAT_SLICE1_CFG Physical Address
0h	RAT_SLICE_PID	Revision Register	0B10 8000h	0B10 9000h
4h	RAT_SLICE_CONFIG	Config Register	0B10 8004h	0B10 9004h

Table 15-1936. PRU_ICSSG1_RAT_SLICE Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG1_R AT_SLICE0_CFG Physical Address	PRU_ICSSG1_R AT_SLICE1_CFG Physical Address
20h	RAT_SLICE_CTRL_J	Region Control Register	0B10 8020h	0B10 9020h
24h	RAT_SLICE_BASE_J	Region Base Register	0B10 8024h	0B10 9024h
28h	RAT_SLICE_TRANS_I_J	Region Translated Lower Address	0B10 8028h	0B10 9028h
2Ch	RAT_SLICE_TRANS_U_J	Region Translated Upper Address	0B10 802Ch	0B10 902Ch
804h	RAT_SLICE_DESTINATION_ID	Destination ID Register	0B10 8804h	0B10 9804h
820h	RAT_SLICE_EXCEPTION_LOGGING_CONTROL	Exception Logging Control Register	0B10 8820h	0B10 9820h
824h	RAT_SLICE_EXCEPTION_LOGGING_HEADER0	Exception Logging Header 0 Register	0B10 8824h	0B10 9824h
828h	RAT_SLICE_EXCEPTION_LOGGING_HEADER1	Exception Logging Header 1 Register	0B10 8828h	0B10 9828h
82Ch	RAT_SLICE_EXCEPTION_LOGGING_DATA0	Exception Logging Data 0 Register	0B10 882Ch	0B10 982Ch
830h	RAT_SLICE_EXCEPTION_LOGGING_DATA1	Exception Logging Data 1 Register	0B10 8830h	0B10 9830h
834h	RAT_SLICE_EXCEPTION_LOGGING_DATA2	Exception Logging Data 2 Register	0B10 8834h	0B10 9834h
838h	RAT_SLICE_EXCEPTION_LOGGING_DATA3	Exception Logging Data 3 Register	0B10 8838h	0B10 9838h
840h	RAT_SLICE_EXCEPTION_PEND_SET	Exception Logging Interrupt Pending Set Register	0B10 8840h	0B10 9840h
844h	RAT_SLICE_EXCEPTION_PEND_CLEAR	Exception Logging Interrupt Pending Clear Register	0B10 8844h	0B10 9844h
848h	RAT_SLICE_EXCEPTION_ENABLE_SET	Exception Logging Interrupt Enable Set Register	0B10 8848h	0B10 9848h
84Ch	RAT_SLICE_EXCEPTION_ENABLE_CLEAR	Exception Logging Interrupt Enable Clear Register	0B10 884Ch	0B10 984Ch
850h	RAT_SLICE_EOI_REG	EOI Register	0B10 8850h	0B10 9850h

15.18.1 RAT_SLICE_PID Register (Offset = 0h) [reset = 66802900h]

RAT_SLICE_PID is shown in [Figure 15-634](#) and described in [Table 15-1938](#).

Return to [Summary Table](#).

The Revision Register contains the major and minor revisions for the module.

Table 15-1937. RAT_SLICE_PID Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	0B00 8000h
PRU_ICSSG0_RAT_SLICE1_CFG	0B00 9000h
PRU_ICSSG1_RAT_SLICE0_CFG	0B10 8000h
PRU_ICSSG1_RAT_SLICE1_CFG	0B10 9000h

Figure 15-634. RAT_SLICE_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		FUNC											
R-1h		R-2h		R-680h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM			MINOR				
R-5h					R-1h			R-0h			R-0h				

LEGEND: R = Read Only; -n = value after reset

Table 15-1938. RAT_SLICE_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	RAT_SLICE_PID register scheme
29-28	BU	R	2h	Business Unit: 10 = Processors
27-16	FUNC	R	680h	Module ID
15-11	RTL	R	5h	RTL revision. Will vary depending on release.
10-8	MAJOR	R	1h	Major revision
7-6	CUSTOM	R	0h	Custom
5-0	MINOR	R	0h	Minor revision

Table 15-1939. Register Call Summary for RAT_SLICE_PID

PRU_RAT_SLICE_RAT_SLICE Registers

- [RAT_SLICE_PID Register \(Offset = 0h\) \[reset = 66802900h\]: \[0\] \[1\]](#)
- [PRU_RAT_SLICE_RAT_SLICE Registers: \[0\] \[1\]](#)

15.18.2 RAT_SLICE_CONFIG Register (Offset = 4h) [reset = X]

RAT_SLICE_CONFIG is shown in Figure 15-635 and described in Table 15-1941.

Return to [Summary Table](#).

The Config Register contains the configuration values for the module.

Table 15-1940. RAT_SLICE_CONFIG Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	0B00 8004h
PRU_ICSSG0_RAT_SLICE1_CFG	0B00 9004h
PRU_ICSSG1_RAT_SLICE0_CFG	0B10 8004h
PRU_ICSSG1_RAT_SLICE1_CFG	0B10 9004h

Figure 15-635. RAT_SLICE_CONFIG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								ADDR_WIDTH							
R-X								R-30h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRS								REGIONS							
R-3h								R-4h							

LEGEND: R = Read Only; -n = value after reset

Table 15-1941. RAT_SLICE_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	X	
23-16	ADDR_WIDTH	R	30h	Number of address bits
15-8	ADDRS	R	3h	Number of addresses
7-0	REGIONS	R	4h	Number of regions

Table 15-1942. Register Call Summary for RAT_SLICE_CONFIG

PRU_RAT_SLICE_RAT_SLICE Registers

- [RAT_SLICE_CONFIG Register \(Offset = 4h\) \[reset = X\]: \[0\]](#)
- [PRU_RAT_SLICE_RAT_SLICE Registers: \[0\] \[1\]](#)

15.18.3 RAT_SLICE_CTRL_j Register (Offset = 20h + formula) [reset = X]

RAT_SLICE_CTRL_j is shown in [Figure 15-636](#) and described in [Table 15-1944](#).

Return to [Summary Table](#).

The Control for Region a.

Offset = 20h + (j * 10h); where j = 0h to 3h

Table 15-1943. RAT_SLICE_CTRL_j Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	0B00 8020h + formula
PRU_ICSSG0_RAT_SLICE1_CFG	0B00 9020h + formula
PRU_ICSSG1_RAT_SLICE0_CFG	0B10 8020h + formula
PRU_ICSSG1_RAT_SLICE1_CFG	0B10 9020h + formula

Figure 15-636. RAT_SLICE_CTRL_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EN	RESERVED														
R/W-0h								R/W-X							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										SIZE					
R/W-X										R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1944. RAT_SLICE_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EN	R/W	0h	Enable for the Region
30-6	RESERVED	R/W	X	
5-0	SIZE	R/W	0h	Size of the Region in Address Bits. 0 = 1 byte, 1 = 2 B, 2 = 4 B, 3 = 8 B, etc. up to 32 = 4 GB. Note: The Size of the Region in Address Bits is 2 to the power of N, where N is 0..32

Table 15-1945. Register Call Summary for RAT_SLICE_CTRL_j

PRU_RAT_SLICE_RAT_SLICE Registers

- [RAT_SLICE_CTRL_j Register \(Offset = 20h + formula\) \[reset = X\]: \[0\]](#)
- [PRU_RAT_SLICE_RAT_SLICE Registers: \[0\] \[1\]](#)

15.18.4 RAT_SLICE_BASE_j Register (Offset = 24h + formula) [reset = 0h]

RAT_SLICE_BASE_j is shown in Figure 15-637 and described in Table 15-1947.

Return to [Summary Table](#).

The Base Address for Region a. This is the source address for matching to a region.

Offset = 24h + (j * 10h); where j = 0h to 3h

Table 15-1946. RAT_SLICE_BASE_j Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	0B00 8024h + formula
PRU_ICSSG0_RAT_SLICE1_CFG	0B00 9024h + formula
PRU_ICSSG1_RAT_SLICE0_CFG	0B10 8024h + formula
PRU_ICSSG1_RAT_SLICE1_CFG	0B10 9024h + formula

Figure 15-637. RAT_SLICE_BASE_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1947. RAT_SLICE_BASE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BASE	R/W	0h	Base Address for the Region. It must be aligned to the programmed size.

Table 15-1948. Register Call Summary for RAT_SLICE_BASE_j

PRU_RAT_SLICE_RAT_SLICE Registers

- [RAT_SLICE_BASE_j Register \(Offset = 24h + formula\) \[reset = 0h\]: \[0\]](#)
- [PRU_RAT_SLICE_RAT_SLICE Registers: \[0\] \[1\]](#)

15.18.5 RAT_SLICE_TRANS_I_j Register (Offset = 28h + formula) [reset = 0h]

RAT_SLICE_TRANS_I_j is shown in Figure 15-638 and described in Table 15-1950.

Return to [Summary Table](#).

The Translated Lower Address Bits for Region a.

Offset = 28h + (j * 10h); where j = 0h to 3h

Table 15-1949. RAT_SLICE_TRANS_I_j Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	0B00 8028h + formula
PRU_ICSSG0_RAT_SLICE1_CFG	0B00 9028h + formula
PRU_ICSSG1_RAT_SLICE0_CFG	0B10 8028h + formula
PRU_ICSSG1_RAT_SLICE1_CFG	0B10 9028h + formula

Figure 15-638. RAT_SLICE_TRANS_I_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOWER																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1950. RAT_SLICE_TRANS_I_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LOWER	R/W	0h	Translated Lower Address Bits for the Region. It must be aligned to the programmed size.

Table 15-1951. Register Call Summary for RAT_SLICE_TRANS_I_j

PRU_RAT_SLICE_RAT_SLICE Registers

- [RAT_SLICE_TRANS_I_j Register \(Offset = 28h + formula\) \[reset = 0h\]: \[0\]](#)
- [PRU_RAT_SLICE_RAT_SLICE Registers: \[0\] \[1\]](#)

15.18.6 RAT_SLICE_TRANS_U_j Register (Offset = 2Ch + formula) [reset = X]

RAT_SLICE_TRANS_U_j is shown in [Figure 15-639](#) and described in [Table 15-1953](#).

Return to [Summary Table](#).

The Translated Upper Address Bits for Region a.

Offset = 2Ch + (j * 10h); where j = 0h to 3h

Table 15-1952. RAT_SLICE_TRANS_U_j Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	0B00 802Ch + formula
PRU_ICSSG0_RAT_SLICE1_CFG	0B00 902Ch + formula
PRU_ICSSG1_RAT_SLICE0_CFG	0B10 802Ch + formula
PRU_ICSSG1_RAT_SLICE1_CFG	0B10 902Ch + formula

Figure 15-639. RAT_SLICE_TRANS_U_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																UPPER															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1953. RAT_SLICE_TRANS_U_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	UPPER	R/W	0h	Translated Upper Address Bits for the Region

Table 15-1954. Register Call Summary for RAT_SLICE_TRANS_U_j

PRU_RAT_SLICE_RAT_SLICE Registers

- [RAT_SLICE_TRANS_U_j Register \(Offset = 2Ch + formula\) \[reset = X\]: \[0\]](#)
- [PRU_RAT_SLICE_RAT_SLICE Registers: \[0\] \[1\]](#)

15.18.7 RAT_SLICE_DESTINATION_ID Register (Offset = 804h) [reset = X]

[RAT_SLICE_DESTINATION_ID](#) is shown in [Figure 15-640](#) and described in [Table 15-1956](#).

Return to [Summary Table](#).

The Destination ID Register defines the destination ID value for error messages.

**Table 15-1955. RAT_SLICE_DESTINATION_ID
Instances**

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	0B00 8804h
PRU_ICSSG0_RAT_SLICE1_CFG	0B00 9804h
PRU_ICSSG1_RAT_SLICE0_CFG	0B10 8804h
PRU_ICSSG1_RAT_SLICE1_CFG	0B10 9804h

Figure 15-640. RAT_SLICE_DESTINATION_ID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DEST_ID							
R/W-X																								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1956. RAT_SLICE_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	DEST_ID	R/W	0h	The destination ID.

Table 15-1957. Register Call Summary for RAT_SLICE_DESTINATION_ID

PRU_RAT_SLICE_RAT_SLICE Registers

- [RAT_SLICE_DESTINATION_ID Register \(Offset = 804h\) \[reset = X\]: \[0\]](#)
- [PRU_RAT_SLICE_RAT_SLICE Registers: \[0\] \[1\]](#)

15.18.8 RAT_SLICE_EXCEPTION_LOGGING_CONTROL Register (Offset = 820h) [reset = X]

RAT_SLICE_EXCEPTION_LOGGING_CONTROL is shown in [Figure 15-641](#) and described in [Table 15-1959](#).

Return to [Summary Table](#).

The Exception Logging Control Register controls the exception logging.

Table 15-1958.
RAT_SLICE_EXCEPTION_LOGGING_CONTROL
Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	0B00 8820h
PRU_ICSSG0_RAT_SLICE1_CFG	0B00 9820h
PRU_ICSSG1_RAT_SLICE0_CFG	0B10 8820h
PRU_ICSSG1_RAT_SLICE1_CFG	0B10 9820h

Figure 15-641. RAT_SLICE_EXCEPTION_LOGGING_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						DISABLE_INTR	DISABLE_F
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1959. RAT_SLICE_EXCEPTION_LOGGING_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	DISABLE_INTR	R/W	0h	Disables logging interrupt when set.
0	DISABLE_F	R/W	0h	Disables logging when set.

Table 15-1960. Register Call Summary for RAT_SLICE_EXCEPTION_LOGGING_CONTROL

PRU_RAT_SLICE_RAT_SLICE Registers

- [RAT_SLICE_EXCEPTION_LOGGING_CONTROL Register \(Offset = 820h\) \[reset = X\]: \[0\]](#)
- [PRU_RAT_SLICE_RAT_SLICE Registers: \[0\] \[1\]](#)

15.18.9 RAT_SLICE_EXCEPTION_LOGGING_HEADER0 Register (Offset = 824h) [reset = 0h]

RAT_SLICE_EXCEPTION_LOGGING_HEADER0 is shown in [Figure 15-642](#) and described in [Table 15-1962](#).

Return to [Summary Table](#).

The Exception Logging Header 0 Register contains the first word of the header.

Table 15-1961.
RAT_SLICE_EXCEPTION_LOGGING_HEADER0
Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	0B00 8824h
PRU_ICSSG0_RAT_SLICE1_CFG	0B00 9824h
PRU_ICSSG1_RAT_SLICE0_CFG	0B10 8824h
PRU_ICSSG1_RAT_SLICE1_CFG	0B10 9824h

Figure 15-642. RAT_SLICE_EXCEPTION_LOGGING_HEADER0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TYPE_F								SRC_ID								DEST_ID															
R-0h								R-0h								R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 15-1962. RAT_SLICE_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TYPE_F	R	0h	Type. 4 = RAT.
23-8	SRC_ID	R	0h	Source ID.
7-0	DEST_ID	R	0h	Destination ID.

Table 15-1963. Register Call Summary for RAT_SLICE_EXCEPTION_LOGGING_HEADER0

PRU_RAT_SLICE_RAT_SLICE Registers

- [RAT_SLICE_EXCEPTION_LOGGING_HEADER0 Register \(Offset = 824h\) \[reset = 0h\]: \[0\]](#)
- [PRU_RAT_SLICE_RAT_SLICE Registers: \[0\] \[1\]](#)

15.18.10 RAT_SLICE_EXCEPTION_LOGGING_HEADER1 Register (Offset = 828h) [reset = X]

RAT_SLICE_EXCEPTION_LOGGING_HEADER1 is shown in Figure 15-643 and described in Table 15-1965.

Return to [Summary Table](#).

The Exception Logging Header 1 Register contains the second word of the header.

Table 15-1964.
RAT_SLICE_EXCEPTION_LOGGING_HEADER1
Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	0B00 8828h
PRU_ICSSG0_RAT_SLICE1_CFG	0B00 9828h
PRU_ICSSG1_RAT_SLICE0_CFG	0B10 8828h
PRU_ICSSG1_RAT_SLICE1_CFG	0B10 9828h

Figure 15-643. RAT_SLICE_EXCEPTION_LOGGING_HEADER1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GROUP								CODE								RESERVED															
R-0h								R-0h								R-X															

LEGEND: R = Read Only; -n = value after reset

Table 15-1965. RAT_SLICE_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	GROUP	R	0h	Group.
23-16	CODE	R	0h	Code. 1 = Boundary crossing error.
15-0	RESERVED	R	X	

Table 15-1966. Register Call Summary for RAT_SLICE_EXCEPTION_LOGGING_HEADER1

PRU_RAT_SLICE_RAT_SLICE Registers

- [RAT_SLICE_EXCEPTION_LOGGING_HEADER1 Register \(Offset = 828h\) \[reset = X\]: \[0\]](#)
- [PRU_RAT_SLICE_RAT_SLICE Registers: \[0\] \[1\]](#)

15.18.11 RAT_SLICE_EXCEPTION_LOGGING_DATA0 Register (Offset = 82Ch) [reset = 0h]

RAT_SLICE_EXCEPTION_LOGGING_DATA0 is shown in [Figure 15-644](#) and described in [Table 15-1968](#).

Return to [Summary Table](#).

The Exception Logging Data 0 Register contains the first word of the data.

Table 15-1967.
RAT_SLICE_EXCEPTION_LOGGING_DATA0
Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	0B00 882Ch
PRU_ICSSG0_RAT_SLICE1_CFG	0B00 982Ch
PRU_ICSSG1_RAT_SLICE0_CFG	0B10 882Ch
PRU_ICSSG1_RAT_SLICE1_CFG	0B10 982Ch

Figure 15-644. RAT_SLICE_EXCEPTION_LOGGING_DATA0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR_L																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 15-1968. RAT_SLICE_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDR_L	R	0h	Address lower 32 bits.

Table 15-1969. Register Call Summary for RAT_SLICE_EXCEPTION_LOGGING_DATA0

PRU_RAT_SLICE_RAT_SLICE Registers

- [RAT_SLICE_EXCEPTION_LOGGING_DATA0 Register \(Offset = 82Ch\) \[reset = 0h\]: \[0\]](#)
- [PRU_RAT_SLICE_RAT_SLICE Registers: \[0\] \[1\]](#)

15.18.12 RAT_SLICE_EXCEPTION_LOGGING_DATA1 Register (Offset = 830h) [reset = X]

RAT_SLICE_EXCEPTION_LOGGING_DATA1 is shown in [Figure 15-645](#) and described in [Table 15-1971](#).

Return to [Summary Table](#).

The Exception Logging Data 1 Register contains the second word of the data.

Table 15-1970.
RAT_SLICE_EXCEPTION_LOGGING_DATA1
Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	0B00 8830h
PRU_ICSSG0_RAT_SLICE1_CFG	0B00 9830h
PRU_ICSSG1_RAT_SLICE0_CFG	0B10 8830h
PRU_ICSSG1_RAT_SLICE1_CFG	0B10 9830h

Figure 15-645. RAT_SLICE_EXCEPTION_LOGGING_DATA1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ADDR_H															
R-X																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 15-1971. RAT_SLICE_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	ADDR_H	R	0h	Address upper 12 bits.

Table 15-1972. Register Call Summary for RAT_SLICE_EXCEPTION_LOGGING_DATA1

PRU_RAT_SLICE_RAT_SLICE Registers

- [RAT_SLICE_EXCEPTION_LOGGING_DATA1 Register \(Offset = 830h\) \[reset = X\]: \[0\]](#)
- [PRU_RAT_SLICE_RAT_SLICE Registers: \[0\] \[1\]](#)

15.18.13 RAT_SLICE_EXCEPTION_LOGGING_DATA2 Register (Offset = 834h) [reset = X]

RAT_SLICE_EXCEPTION_LOGGING_DATA2 is shown in [Figure 15-646](#) and described in [Table 15-1974](#).

Return to [Summary Table](#).

The Exception Logging Data 2 Register contains the third word of the data.

Table 15-1973.
RAT_SLICE_EXCEPTION_LOGGING_DATA2
Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	0B00 8834h
PRU_ICSSG0_RAT_SLICE1_CFG	0B00 9834h
PRU_ICSSG1_RAT_SLICE0_CFG	0B10 8834h
PRU_ICSSG1_RAT_SLICE1_CFG	0B10 9834h

Figure 15-646. RAT_SLICE_EXCEPTION_LOGGING_DATA2 Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
R-X				R-0h			
23	22	21	20	19	18	17	16
ROUTEID							
R-0h							
15	14	13	12	11	10	9	8
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
R-X		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
PRIV_ID							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 15-1974. RAT_SLICE_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	X	
27-16	ROUTEID	R	0h	Route ID.
15-14	RESERVED	R	X	
13	WRITE	R	0h	Write.
12	READ	R	0h	Read.
11	DEBUG	R	0h	Debug.
10	CACHEABLE	R	0h	Cacheable.
9	PRIV	R	0h	Priv.
8	SECURE	R	0h	Secure.
7-0	PRIV_ID	R	0h	Priv ID.

Table 15-1975. Register Call Summary for RAT_SLICE_EXCEPTION_LOGGING_DATA2

PRU_RAT_SLICE_RAT_SLICE Registers

- [RAT_SLICE_EXCEPTION_LOGGING_DATA2 Register \(Offset = 834h\) \[reset = X\]: \[0\]](#)
- [PRU_RAT_SLICE_RAT_SLICE Registers: \[0\] \[1\]](#)

15.18.14 RAT_SLICE_EXCEPTION_LOGGING_DATA3 Register (Offset = 838h) [reset = X]

RAT_SLICE_EXCEPTION_LOGGING_DATA3 is shown in [Figure 15-647](#) and described in [Table 15-1977](#).

Return to [Summary Table](#).

The Exception Logging Data 3 Register contains the fourth word of the data. Reading this register will clear the error pending bit.

Table 15-1976.
RAT_SLICE_EXCEPTION_LOGGING_DATA3
Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	0B00 8838h
PRU_ICSSG0_RAT_SLICE1_CFG	0B00 9838h
PRU_ICSSG1_RAT_SLICE0_CFG	0B10 8838h
PRU_ICSSG1_RAT_SLICE1_CFG	0B10 9838h

Figure 15-647. RAT_SLICE_EXCEPTION_LOGGING_DATA3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
RESERVED																						BYTECNT															
R-X																						R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 15-1977. RAT_SLICE_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	X	
9-0	BYTECNT	R	0h	Byte count.

Table 15-1978. Register Call Summary for RAT_SLICE_EXCEPTION_LOGGING_DATA3

PRU_RAT_SLICE_RAT_SLICE Registers

- [RAT_SLICE_EXCEPTION_LOGGING_DATA3 Register \(Offset = 838h\) \[reset = X\]: \[0\]](#)
- [PRU_RAT_SLICE_RAT_SLICE Registers: \[0\] \[1\]](#)

15.18.15 RAT_SLICE_EXCEPTION_PEND_SET Register (Offset = 840h) [reset = X]

RAT_SLICE_EXCEPTION_PEND_SET is shown in [Figure 15-648](#) and described in [Table 15-1980](#).

Return to [Summary Table](#).

The Exception Logging Interrupt Pending Set Register allows to set the pend signal.

Table 15-1979. RAT_SLICE_EXCEPTION_PEND_SET Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	0B00 8840h
PRU_ICSSG0_RAT_SLICE1_CFG	0B00 9840h
PRU_ICSSG1_RAT_SLICE0_CFG	0B10 8840h
PRU_ICSSG1_RAT_SLICE1_CFG	0B10 9840h

Figure 15-648. RAT_SLICE_EXCEPTION_PEND_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							PEND_SET
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 15-1980. RAT_SLICE_EXCEPTION_PEND_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	PEND_SET	R/W1S	0h	Write a 1 to set the exception pend signal.

Table 15-1981. Register Call Summary for RAT_SLICE_EXCEPTION_PEND_SET

PRU_RAT_SLICE_RAT_SLICE Registers

- [RAT_SLICE_EXCEPTION_PEND_SET Register \(Offset = 840h\) \[reset = X\]: \[0\]](#)
- [PRU_RAT_SLICE_RAT_SLICE Registers: \[0\] \[1\]](#)

15.18.16 RAT_SLICE_EXCEPTION_PEND_CLEAR Register (Offset = 844h) [reset = X]

RAT_SLICE_EXCEPTION_PEND_CLEAR is shown in Figure 15-649 and described in Table 15-1983.

Return to [Summary Table](#).

The Exception Logging Interrupt Pending Clear Register allows to clear the pend signal.

Table 15-1982.

RAT_SLICE_EXCEPTION_PEND_CLEAR Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	0B00 8844h
PRU_ICSSG0_RAT_SLICE1_CFG	0B00 9844h
PRU_ICSSG1_RAT_SLICE0_CFG	0B10 8844h
PRU_ICSSG1_RAT_SLICE1_CFG	0B10 9844h

Figure 15-649. RAT_SLICE_EXCEPTION_PEND_CLEAR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							PEND_CLR
R/W-X							R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 15-1983. RAT_SLICE_EXCEPTION_PEND_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	PEND_CLR	R/W1C	0h	Write a 1 to clear the exception pend signal.

Table 15-1984. Register Call Summary for RAT_SLICE_EXCEPTION_PEND_CLEAR

PRU_RAT_SLICE_RAT_SLICE Registers

- [RAT_SLICE_EXCEPTION_PEND_CLEAR Register \(Offset = 844h\) \[reset = X\]: \[0\]](#)
- [PRU_RAT_SLICE_RAT_SLICE Registers: \[0\] \[1\]](#)

15.18.17 RAT_SLICE_EXCEPTION_ENABLE_SET Register (Offset = 848h) [reset = X]

RAT_SLICE_EXCEPTION_ENABLE_SET is shown in [Figure 15-650](#) and described in [Table 15-1986](#).

Return to [Summary Table](#).

The Exception Logging Interrupt Enable Set Register allows to set the interrupt enable signal.

Table 15-1985.

RAT_SLICE_EXCEPTION_ENABLE_SET Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	0B00 8848h
PRU_ICSSG0_RAT_SLICE1_CFG	0B00 9848h
PRU_ICSSG1_RAT_SLICE0_CFG	0B10 8848h
PRU_ICSSG1_RAT_SLICE1_CFG	0B10 9848h

Figure 15-650. RAT_SLICE_EXCEPTION_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							ENABLE_SET
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 15-1986. RAT_SLICE_EXCEPTION_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	ENABLE_SET	R/W1S	0h	Write a 1 to set the exception interrupt enable signal.

Table 15-1987. Register Call Summary for RAT_SLICE_EXCEPTION_ENABLE_SET

PRU_RAT_SLICE_RAT_SLICE Registers

- [RAT_SLICE_EXCEPTION_ENABLE_SET Register \(Offset = 848h\) \[reset = X\]: \[0\]](#)
- [PRU_RAT_SLICE_RAT_SLICE Registers: \[0\] \[1\]](#)

15.18.18 RAT_SLICE_EXCEPTION_ENABLE_CLEAR Register (Offset = 84Ch) [reset = X]

RAT_SLICE_EXCEPTION_ENABLE_CLEAR is shown in [Figure 15-651](#) and described in [Table 15-1989](#).

Return to [Summary Table](#).

The Exception Logging Interrupt Enable Clear Register allows to clear the interrupt enable signal.

Table 15-1988.
RAT_SLICE_EXCEPTION_ENABLE_CLEAR
Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	0B00 884Ch
PRU_ICSSG0_RAT_SLICE1_CFG	0B00 984Ch
PRU_ICSSG1_RAT_SLICE0_CFG	0B10 884Ch
PRU_ICSSG1_RAT_SLICE1_CFG	0B10 984Ch

Figure 15-651. RAT_SLICE_EXCEPTION_ENABLE_CLEAR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							ENABLE_CLR
R/W-X							R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 15-1989. RAT_SLICE_EXCEPTION_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	ENABLE_CLR	R/W1C	0h	Write a 1 to clear the exception interrupt enable signal.

Table 15-1990. Register Call Summary for RAT_SLICE_EXCEPTION_ENABLE_CLEAR

PRU_RAT_SLICE_RAT_SLICE Registers

- [RAT_SLICE_EXCEPTION_ENABLE_CLEAR Register \(Offset = 84Ch\) \[reset = X\]: \[0\]](#)
- [PRU_RAT_SLICE_RAT_SLICE Registers: \[0\] \[1\]](#)

15.18.19 RAT_SLICE_EOI_REG Register (Offset = 850h) [reset = X]

RAT_SLICE_EOI_REG is shown in [Figure 15-652](#) and described in [Table 15-1992](#).

Return to [Summary Table](#).

EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 15-1991. RAT_SLICE_EOI_REG Instances

Instance	Physical Address
PRU_ICSSG0_RAT_SLICE0_CFG	0B00 8850h
PRU_ICSSG0_RAT_SLICE1_CFG	0B00 9850h
PRU_ICSSG1_RAT_SLICE0_CFG	0B10 8850h
PRU_ICSSG1_RAT_SLICE1_CFG	0B10 9850h

Figure 15-652. RAT_SLICE_EOI_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																EOI_WR															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-1992. RAT_SLICE_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	EOI_WR	R/W	0h	EOI Register

Table 15-1993. Register Call Summary for RAT_SLICE_EOI_REG

PRU_RAT_SLICE_RAT_SLICE Registers

- [RAT_SLICE_EOI_REG Register \(Offset = 850h\) \[reset = X\]: \[0\]](#)
- [PRU_RAT_SLICE_RAT_SLICE Registers: \[0\] \[1\]](#)

15.19 PRU_TASKS_MGR_TASKS_MGR_PRU_RTU_TX Registers

Table 15-1995, Table 15-1996, Table 15-1997, Table 15-1998, Table 15-1999, and Table 15-2000 list the memory-mapped registers for the PRU_TASKS_MGR_TASKS_MGR_PRU0, PRU_TASKS_MGR_TASKS_MGR_RTU0, PRU_TASKS_MGR_TASKS_MGR_PRU1, PRU_TASKS_MGR_TASKS_MGR_RTU1, PRU_TASKS_MGR_TASKS_MGR_PRU_TX0 and PRU_TASKS_MGR_TASKS_MGR_PRU_TX1. All register offset addresses not listed in Table 15-1995 to Table 15-2000 should be considered as reserved locations and the register contents should not be modified.

Table 15-1994. PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Instances

Instance	Base Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B02 A000h
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B12 A000h
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B02 A100h
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B12 A100h
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B02 A200h
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B12 A200h
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B02 A300h
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B12 A300h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h

Table 15-1995. PRU_TASKS_MGR_TASKS_MGR_PRU0 Registers

Offset	Acronym	Register Name	PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR Physical Address	PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR Physical Address
0h	TASKS_MGR_GLOBAL_CFG	Global Configuration	0B02 A000h	0B12 A000h
4h	TASKS_MGR_GLOBAL_STATUS	Global Status	0B02 A004h	0B12 A004h
8h	TASKS_MGR_TS1_PC_S0	Task1 Subroutine0 PC	0B02 A008h	0B12 A008h
Ch	TASKS_MGR_TS1_PC_S1	Task1 Subroutine1 PC	0B02 A00Ch	0B12 A00Ch
10h	TASKS_MGR_TS1_PC_S2	Task1 Subroutine2 PC	0B02 A010h	0B12 A010h
14h	TASKS_MGR_TS1_PC_S3	Task1 Subroutine3 PC	0B02 A014h	0B12 A014h
18h	TASKS_MGR_TS1_PC_S4	Task1 Subroutine4 PC	0B02 A018h	0B12 A018h
1Ch	TASKS_MGR_TS2_PC_S0	Task2 Subroutine0 PC	0B02 A01Ch	0B12 A01Ch
20h	TASKS_MGR_TS2_PC_S1	Task2 Subroutine1 PC	0B02 A020h	0B12 A020h
24h	TASKS_MGR_TS2_PC_S2	Task2 Subroutine2 PC	0B02 A024h	0B12 A024h
28h	TASKS_MGR_TS2_PC_S3	Task2 Subroutine3 PC	0B02 A028h	0B12 A028h
2Ch	TASKS_MGR_TS2_PC_S4	Task2 Subroutine4 PC	0B02 A02Ch	0B12 A02Ch
30h	TASKS_MGR_RX_CFG	RX Configuration	0B02 A030h	0B12 A030h
34h	TASKS_MGR_TX_CFG	TX Configuration	0B02 A034h	0B12 A034h
38h	TASKS_MGR_TS1_GEN_CFG1	Generic TS1 Configuration1	0B02 A038h	0B12 A038h
3Ch	TASKS_MGR_TS1_GEN_CFG2	Generic TS1 Configuration2	0B02 A03Ch	0B12 A03Ch
40h	TASKS_MGR_TS2_GEN_CFG1	Generic TS2 Configuration1	0B02 A040h	0B12 A040h
44h	TASKS_MGR_TS2_GEN_CFG2	Generic TS2 Configuration2	0B02 A044h	0B12 A044h
48h	TASKS_MGR_CAP_EN_CFG	Enable Capture new Event Configuration	0B02 A048h	0B12 A048h

Table 15-1996. PRU_TASKS_MGR_TASKS_MGR_RTU0 Registers

Offset	Acronym	Register Name	PRU_ICSSG0_PR 1_TASKS_MGR_ RTU0_PR1_TASK S_MGR_RTU0_M MR Physical Address	PRU_ICSSG1_PR 1_TASKS_MGR_ RTU0_PR1_TASK S_MGR_RTU0_M MR Physical Address
0h	TASKS_MGR_GLOBAL_CFG	Global Configuration	0B02 A100h	0B12 A100h
4h	TASKS_MGR_GLOBAL_STATUS	Global Status	0B02 A104h	0B12 A104h
8h	TASKS_MGR_TS1_PC_S0	Task1 Subroutine0 PC	0B02 A108h	0B12 A108h
Ch	TASKS_MGR_TS1_PC_S1	Task1 Subroutine1 PC	0B02 A10Ch	0B12 A10Ch
10h	TASKS_MGR_TS1_PC_S2	Task1 Subroutine2 PC	0B02 A110h	0B12 A110h
14h	TASKS_MGR_TS1_PC_S3	Task1 Subroutine3 PC	0B02 A114h	0B12 A114h
18h	TASKS_MGR_TS1_PC_S4	Task1 Subroutine4 PC	0B02 A118h	0B12 A118h
1Ch	TASKS_MGR_TS2_PC_S0	Task2 Subroutine0 PC	0B02 A11Ch	0B12 A11Ch
20h	TASKS_MGR_TS2_PC_S1	Task2 Subroutine1 PC	0B02 A120h	0B12 A120h
24h	TASKS_MGR_TS2_PC_S2	Task2 Subroutine2 PC	0B02 A124h	0B12 A124h
28h	TASKS_MGR_TS2_PC_S3	Task2 Subroutine3 PC	0B02 A128h	0B12 A128h
2Ch	TASKS_MGR_TS2_PC_S4	Task2 Subroutine4 PC	0B02 A12Ch	0B12 A12Ch
30h	TASKS_MGR_RX_CFG	RX Configuration	0B02 A130h	0B12 A130h
34h	TASKS_MGR_TX_CFG	TX Configuration	0B02 A134h	0B12 A134h
38h	TASKS_MGR_TS1_GEN_CFG1	Generic TS1 Configuration1	0B02 A138h	0B12 A138h
3Ch	TASKS_MGR_TS1_GEN_CFG2	Generic TS1 Configuration2	0B02 A13Ch	0B12 A13Ch
40h	TASKS_MGR_TS2_GEN_CFG1	Generic TS2 Configuration1	0B02 A140h	0B12 A140h
44h	TASKS_MGR_TS2_GEN_CFG2	Generic TS2 Configuration2	0B02 A144h	0B12 A144h
48h	TASKS_MGR_CAP_EN_CFG	Enable Capture new Event Configuration	0B02 A148h	0B12 A148h

Table 15-1997. PRU_TASKS_MGR_TASKS_MGR_PRU1 Registers

Offset	Acronym	Register Name	PRU_ICSSG0_PR 1_TASKS_MGR_ PRU1_PR1_TASK S_MGR_PRU1_M MR Physical Address	PRU_ICSSG1_PR 1_TASKS_MGR_ PRU1_PR1_TASK S_MGR_PRU1_M MR Physical Address
0h	TASKS_MGR_GLOBAL_CFG	Global Configuration	0B02 A200h	0B12 A200h
4h	TASKS_MGR_GLOBAL_STATUS	Global Status	0B02 A204h	0B12 A204h
8h	TASKS_MGR_TS1_PC_S0	TS1 Sub0 PC	0B02 A208h	0B12 A208h
Ch	TASKS_MGR_TS1_PC_S1	TS1 Sub1 PC	0B02 A20Ch	0B12 A20Ch
10h	TASKS_MGR_TS1_PC_S2	TS1 Sub2 PC	0B02 A210h	0B12 A210h
14h	TASKS_MGR_TS1_PC_S3	TS1 Sub3 PC	0B02 A214h	0B12 A214h
18h	TASKS_MGR_TS1_PC_S4	TS1 Sub4 PC	0B02 A218h	0B12 A218h
1Ch	TASKS_MGR_TS2_PC_S0	TS2 Sub0 PC	0B02 A21Ch	0B12 A21Ch
20h	TASKS_MGR_TS2_PC_S1	TS2 Sub1 PC	0B02 A220h	0B12 A220h
24h	TASKS_MGR_TS2_PC_S2	TS2 Sub2 PC	0B02 A224h	0B12 A224h
28h	TASKS_MGR_TS2_PC_S3	TS2 Sub3 PC	0B02 A228h	0B12 A228h
2Ch	TASKS_MGR_TS2_PC_S4	TS2 Sub4 PC	0B02 A22Ch	0B12 A22Ch
30h	TASKS_MGR_RX_CFG	RX Configuration	0B02 A230h	0B12 A230h
34h	TASKS_MGR_TX_CFG	TX Configuration	0B02 A234h	0B12 A234h
38h	TASKS_MGR_TS1_GEN_CFG1	Generic TS1 Configuration1	0B02 A238h	0B12 A238h
3Ch	TASKS_MGR_TS1_GEN_CFG2	Generic TS1 Configuration2	0B02 A23Ch	0B12 A23Ch
40h	TASKS_MGR_TS2_GEN_CFG1	Generic TS2 Configuration1	0B02 A240h	0B12 A240h
44h	TASKS_MGR_TS2_GEN_CFG2	Generic TS2 Configuration2	0B02 A244h	0B12 A244h

Table 15-1997. PRU_TASKS_MGR_TASKS_MGR_PRU1 Registers (continued)

Offset	Acronym	Register Name	PRU_ICSSG0_PR 1_TASKS_MGR_ PRU1_PR1_TASK S_MGR_PRU1_M MR Physical Address	PRU_ICSSG1_PR 1_TASKS_MGR_ PRU1_PR1_TASK S_MGR_PRU1_M MR Physical Address
48h	TASKS_MGR_CAP_EN_CFG	Enable capture new event cfg	0B02 A248h	0B12 A248h

Table 15-1998. PRU_TASKS_MGR_TASKS_MGR_RTU1 Registers

Offset	Acronym	Register Name	PRU_ICSSG0_PR 1_TASKS_MGR_ RTU1_PR1_TASK S_MGR_RTU1_M MR Physical Address	PRU_ICSSG1_PR 1_TASKS_MGR_ RTU1_PR1_TASK S_MGR_RTU1_M MR Physical Address
0h	TASKS_MGR_GLOBAL_CFG	Global Configuration	0B02 A300h	0B12 A300h
4h	TASKS_MGR_GLOBAL_STATUS	Global Status	0B02 A304h	0B12 A304h
8h	TASKS_MGR_TS1_PC_S0	Task1 Subroutine0 PC	0B02 A308h	0B12 A308h
Ch	TASKS_MGR_TS1_PC_S1	Task1 Subroutine1 PC	0B02 A30Ch	0B12 A30Ch
10h	TASKS_MGR_TS1_PC_S2	Task1 Subroutine2 PC	0B02 A310h	0B12 A310h
14h	TASKS_MGR_TS1_PC_S3	Task1 Subroutine3 PC	0B02 A314h	0B12 A314h
18h	TASKS_MGR_TS1_PC_S4	Task1 Subroutine4 PC	0B02 A318h	0B12 A318h
1Ch	TASKS_MGR_TS2_PC_S0	Task2 Subroutine0 PC	0B02 A31Ch	0B12 A31Ch
20h	TASKS_MGR_TS2_PC_S1	Task2 Subroutine1 PC	0B02 A320h	0B12 A320h
24h	TASKS_MGR_TS2_PC_S2	Task2 Subroutine2 PC	0B02 A324h	0B12 A324h
28h	TASKS_MGR_TS2_PC_S3	Task2 Subroutine3 PC	0B02 A328h	0B12 A328h
2Ch	TASKS_MGR_TS2_PC_S4	Task2 Subroutine4 PC	0B02 A32Ch	0B12 A32Ch
30h	TASKS_MGR_RX_CFG	RX Configuration	0B02 A330h	0B12 A330h
34h	TASKS_MGR_TX_CFG	TX Configuration	0B02 A334h	0B12 A334h
38h	TASKS_MGR_TS1_GEN_CFG1	Generic TS1 Configuration1	0B02 A338h	0B12 A338h
3Ch	TASKS_MGR_TS1_GEN_CFG2	Generic TS1 Configuration2	0B02 A33Ch	0B12 A33Ch
40h	TASKS_MGR_TS2_GEN_CFG1	Generic TS2 Configuration1	0B02 A340h	0B12 A340h
44h	TASKS_MGR_TS2_GEN_CFG2	Generic TS2 Configuration2	0B02 A344h	0B12 A344h
48h	TASKS_MGR_CAP_EN_CFG	Enable Capture new Event Configuration	0B02 A348h	0B12 A348h

Table 15-1999. PRU_TASKS_MGR_TASKS_MGR_PRU_TX0

Offset	Acronym	Register Name	PRU_ICSSG0_PR 1_TASKS_MGR_ PRU_TX0_PR1_T ASKS_MGR_PRU _TX0_MMR Physical Address	PRU_ICSSG1_PR 1_TASKS_MGR_ PRU_TX0_PR1_T ASKS_MGR_PR _TX0_MMR Physical Address
0h	TASKS_MGR_GLOBAL_CFG	Global Configuration	A400h	A400h
4h	TASKS_MGR_GLOBAL_STATUS	Global Status	A404h	A404h
8h	TASKS_MGR_TS1_PC_S0	Task1 Subroutine0 PC	A408h	A408h
Ch	TASKS_MGR_TS1_PC_S1	Task1 Subroutine1 PC	A40Ch	A40Ch
10h	TASKS_MGR_TS1_PC_S2	Task1 Subroutine2 PC	A410h	A410h
14h	TASKS_MGR_TS1_PC_S3	Task1 Subroutine3 PC	A414h	A414h
18h	TASKS_MGR_TS1_PC_S4	Task1 Subroutine4 PC	A418h	A418h
1Ch	TASKS_MGR_TS2_PC_S0	Task2 Subroutine0 PC	A41Ch	A41Ch
20h	TASKS_MGR_TS2_PC_S1	Task2 Subroutine1 PC	A420h	A420h
24h	TASKS_MGR_TS2_PC_S2	Task2 Subroutine2 PC	A424h	A424h

Table 15-1999. PRU_TASKS_MGR_TASKS_MGR_PRU_TX0 (continued)

Offset	Acronym	Register Name	PRU_ICSSG0_PR 1_TASKS_MGR_ PRU_TX0_PR1_T ASKS_MGR_PRU _TX0_MMR Physical Address	PRU_ICSSG1_PR 1_TASKS_MGR_ PRU_TX0_PR1_T ASKS_MGR_PR U_TX0_MMR Physical Address
28h	TASKS_MGR_TS2_PC_S3	Task2 Subroutine3 PC	A428h	A428h
2Ch	TASKS_MGR_TS2_PC_S4	Task2 Subroutine4 PC	A42Ch	A42Ch
30h	TASKS_MGR_RX_CFG	RX Configuration	A430h	A430h
34h	TASKS_MGR_TX_CFG	TX Configuration	A434h	A434h
38h	TASKS_MGR_TS1_GEN_CFG1	Generic TS1 Configuration1	A438h	A438h
3Ch	TASKS_MGR_TS1_GEN_CFG2	Generic TS1 Configuration2	A43Ch	A43Ch
40h	TASKS_MGR_TS2_GEN_CFG1	Generic TS2 Configuration1	A440h	A440h
44h	TASKS_MGR_TS2_GEN_CFG2	Generic TS2 Configuration2	A444h	A444h
48h	TASKS_MGR_CAP_EN_CFG	Enable Capture new Event Configuration	A448h	A448h

Table 15-2000. PRU_TASKS_MGR_TASKS_MGR_PRU_TX1

Offset	Acronym	Register Name	PRU_ICSSG0_PR 1_TASKS_MGR_ PRU_TX1_PR1_T ASKS_MGR_PRU _TX1_MMR Physical Address	PRU_ICSSG1_PR 1_TASKS_MGR_ PRU_TX1_PR1_T ASKS_MGR_PR U_TX1_MMR Physical Address
0h	TASKS_MGR_GLOBAL_CFG	Global Configuration	A500h	A500h
4h	TASKS_MGR_GLOBAL_STATUS	Global Status	A504h	A504h
8h	TASKS_MGR_TS1_PC_S0	Task1 Subroutine0 PC	A508h	A508h
Ch	TASKS_MGR_TS1_PC_S1	Task1 Subroutine1 PC	A50Ch	A50Ch
10h	TASKS_MGR_TS1_PC_S2	Task1 Subroutine2 PC	A510h	A510h
14h	TASKS_MGR_TS1_PC_S3	Task1 Subroutine3 PC	A514h	A514h
18h	TASKS_MGR_TS1_PC_S4	Task1 Subroutine4 PC	A518h	A518h
1Ch	TASKS_MGR_TS2_PC_S0	Task2 Subroutine0 PC	A51Ch	A51Ch
20h	TASKS_MGR_TS2_PC_S1	Task2 Subroutine1 PC	A520h	A520h
24h	TASKS_MGR_TS2_PC_S2	Task2 Subroutine2 PC	A524h	A524h
28h	TASKS_MGR_TS2_PC_S3	Task2 Subroutine3 PC	A528h	A528h
2Ch	TASKS_MGR_TS2_PC_S4	Task2 Subroutine4 PC	A52Ch	A52Ch
30h	TASKS_MGR_RX_CFG	RX Configuration	A530h	A530h
34h	TASKS_MGR_TX_CFG	TX Configuration	A534h	A534h
38h	TASKS_MGR_TS1_GEN_CFG1	Generic TS1 Configuration1	A538h	A538h
3Ch	TASKS_MGR_TS1_GEN_CFG2	Generic TS1 Configuration2	A53Ch	A53Ch
40h	TASKS_MGR_TS2_GEN_CFG1	Generic TS2 Configuration1	A540h	A540h
44h	TASKS_MGR_TS2_GEN_CFG2	Generic TS2 Configuration2	A544h	A544h
48h	TASKS_MGR_CAP_EN_CFG	Enable Capture new Event Configuration	A548h	A548h

15.19.1 TASKS_MGR_GLOBAL_CFG Register (Offset = 0h) [reset = X]

TASKS_MGR_GLOBAL_CFG is shown in Figure 15-653 and described in Table 15-2002.

Return to [Summary Table](#).

Global Configuration

Table 15-2001. TASKS_MGR_GLOBAL_CFG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B02 A000h
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B12 A000h
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B02 A100h
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B12 A100h
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B02 A200h
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B12 A200h
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B02 A300h
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B12 A300h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h

Figure 15-653. TASKS_MGR_GLOBAL_CFG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED				TS2_EN_S4	TS2_EN_S3	TS2_EN_S2	TS2_EN_S1
R/W-X				R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TS2_EN_S0	TS1_EN_S4	TS1_EN_S3	TS1_EN_S2	TS1_EN_S1	TS1_EN_S0	TASKS_MGR_MODE	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-2002. TASKS_MGR_GLOBAL_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11	TS2_EN_S4	R/W	0h	TS2 Sub4 0: Disabled 1: Enabled
10	TS2_EN_S3	R/W	0h	TS2 Sub3 0: Disabled 1: Enabled
9	TS2_EN_S2	R/W	0h	TS2 Sub2 0: Disabled 1: Enabled
8	TS2_EN_S1	R/W	0h	TS2 Sub1 0: Disabled 1: Enabled

Table 15-2002. TASKS_MGR_GLOBAL_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	TS2_EN_S0	R/W	0h	TS2 Sub0 0: Disabled 1: Enabled
6	TS1_EN_S4	R/W	0h	TS1 Sub4 0: Disabled 1: Enabled
5	TS1_EN_S3	R/W	0h	TS1 Sub3 0: Disabled 1: Enabled
4	TS1_EN_S2	R/W	0h	TS1 Sub2 0: Disabled 1: Enabled
3	TS1_EN_S1	R/W	0h	TS1 Sub1 0: Disabled 1: Enabled
2	TS1_EN_S0	R/W	0h	TS1 Sub0 0: Disabled 1: Enabled
1-0	TASKS_MGR_MODE	R/W	0h	TaskSwap Mode 0: Disabled 1: RXTX 2: General_HW

Table 15-2003. Register Call Summary for TASKS_MGR_GLOBAL_CFG

PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers

- [PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers: \[0\] \[1\] \[2\] \[3\]](#)
- [TASKS_MGR_GLOBAL_CFG Register \(Offset = 0h\) \[reset = X\]: \[0\]](#)

15.19.2 TASKS_MGR_GLOBAL_STATUS Register (Offset = 4h) [reset = X]

TASKS_MGR_GLOBAL_STATUS is shown in [Figure 15-654](#) and described in [Table 15-2005](#).

Return to [Summary Table](#).

Global Status

Table 15-2004. TASKS_MGR_GLOBAL_STATUS Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B02 A004h
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B12 A004h
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B02 A104h
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B12 A104h
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B02 A204h
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B12 A204h
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B02 A304h
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B12 A304h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h

Figure 15-654. TASKS_MGR_GLOBAL_STATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED						TS2_SUB_PEN D_4	TS2_SUB_PEN D_3
R-X						R-0h	R-0h
15	14	13	12	11	10	9	8
TS2_SUB_PEN D_2	TS2_SUB_PEN D_1	TS2_SUB_PEN D_0	TS1_SUB_PEN D_4	TS1_SUB_PEN D_3	TS1_SUB_PEN D_2	TS1_SUB_PEN D_1	TS1_SUB_PEN D_0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
TS2_STATE				TS1_STATE			
R-0h				R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 15-2005. TASKS_MGR_GLOBAL_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	X	
17	TS2_SUB_PEND_4	R	0h	Task2 Sub4 Pend State
16	TS2_SUB_PEND_3	R	0h	Task2 Sub3 Pend State
15	TS2_SUB_PEND_2	R	0h	Task2 Sub2 Pend State
14	TS2_SUB_PEND_1	R	0h	Task2 Sub1 Pend State
13	TS2_SUB_PEND_0	R	0h	Task2 Sub0 Pend State
12	TS1_SUB_PEND_4	R	0h	Task1 Sub4 Pend State
11	TS1_SUB_PEND_3	R	0h	Task1 Sub3 Pend State
10	TS1_SUB_PEND_2	R	0h	Task1 Sub2 Pend State
9	TS1_SUB_PEND_1	R	0h	Task1 Sub1 Pend State
8	TS1_SUB_PEND_0	R	0h	Task1 Sub0 Pend State

Table 15-2005. TASKS_MGR_GLOBAL_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-4	TS2_STATE	R	0h	Task2 State
3-0	TS1_STATE	R	0h	Task1 State

Table 15-2006. Register Call Summary for TASKS_MGR_GLOBAL_STATUS

PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers

- [PRU_TASKS_MGR_TASKS_MGR_PRU_RTU](#) Registers: [0] [1] [2] [3]
- [TASKS_MGR_GLOBAL_STATUS](#) Register (Offset = 4h) [reset = X]: [0]

15.19.3 TASKS_MGR_TS1_PC_S0 Register (Offset = 8h) [reset = X]

TASKS_MGR_TS1_PC_S0 is shown in [Figure 15-655](#) and described in [Table 15-2008](#).

Return to [Summary Table](#).

TS1 Sub0 PC

Table 15-2007. TASKS_MGR_TS1_PC_S0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B02 A008h
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B12 A008h
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B02 A108h
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B12 A108h
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B02 A208h
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B12 A208h
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B02 A308h
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B12 A308h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h

Figure 15-655. TASKS_MGR_TS1_PC_S0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TS1_PC_S0															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-2008. TASKS_MGR_TS1_PC_S0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TS1_PC_S0	R/W	0h	TS1 Sub0 PC

Table 15-2009. Register Call Summary for TASKS_MGR_TS1_PC_S0

- PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers
- [PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers: \[0\] \[1\] \[2\] \[3\]](#)
 - [TASKS_MGR_TS1_PC_S0 Register \(Offset = 8h\) \[reset = X\]: \[0\]](#)

15.19.4 TASKS_MGR_TS1_PC_S1 Register (Offset = Ch) [reset = X]

TASKS_MGR_TS1_PC_S1 is shown in [Figure 15-656](#) and described in [Table 15-2011](#).

Return to [Summary Table](#).

TS1 Sub1 PC

Table 15-2010. TASKS_MGR_TS1_PC_S1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B02 A00Ch
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B12 A00Ch
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B02 A10Ch
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B12 A10Ch
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B02 A20Ch
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B12 A20Ch
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B02 A30Ch
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B12 A30Ch
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h

Figure 15-656. TASKS_MGR_TS1_PC_S1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		TS1_PC_S1													
R/W-X																		R/W-0h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-2011. TASKS_MGR_TS1_PC_S1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TS1_PC_S1	R/W	0h	TS1 Sub1 PC

Table 15-2012. Register Call Summary for TASKS_MGR_TS1_PC_S1

PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers

- [PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers: \[0\] \[1\] \[2\] \[3\]](#)
- [TASKS_MGR_TS1_PC_S1 Register \(Offset = Ch\) \[reset = X\]: \[0\]](#)

15.19.5 TASKS_MGR_TS1_PC_S2 Register (Offset = 10h) [reset = X]

TASKS_MGR_TS1_PC_S2 is shown in [Figure 15-657](#) and described in [Table 15-2014](#).

Return to [Summary Table](#).

TS1 Sub2 PC

Table 15-2013. TASKS_MGR_TS1_PC_S2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B02 A010h
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B12 A010h
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B02 A110h
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B12 A110h
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B02 A210h
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B12 A210h
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B02 A310h
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B12 A310h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h

Figure 15-657. TASKS_MGR_TS1_PC_S2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TS1_PC_S2															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-2014. TASKS_MGR_TS1_PC_S2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TS1_PC_S2	R/W	0h	TS1 Sub2 PC

Table 15-2015. Register Call Summary for TASKS_MGR_TS1_PC_S2

- PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers
- [PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers: \[0\] \[1\] \[2\] \[3\]](#)
 - [TASKS_MGR_TS1_PC_S2 Register \(Offset = 10h\) \[reset = X\]: \[0\]](#)

15.19.6 TASKS_MGR_TS1_PC_S3 Register (Offset = 14h) [reset = X]

TASKS_MGR_TS1_PC_S3 is shown in [Figure 15-658](#) and described in [Table 15-2017](#).

Return to [Summary Table](#).

TS1 Sub3 PC

Table 15-2016. TASKS_MGR_TS1_PC_S3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B02 A014h
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B12 A014h
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B02 A114h
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B12 A114h
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B02 A214h
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B12 A214h
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B02 A314h
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B12 A314h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h

Figure 15-658. TASKS_MGR_TS1_PC_S3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		TS1_PC_S3													
R/W-X																		R/W-0h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-2017. TASKS_MGR_TS1_PC_S3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TS1_PC_S3	R/W	0h	TS1 Sub3 PC

Table 15-2018. Register Call Summary for TASKS_MGR_TS1_PC_S3

PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers

- [PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers: \[0\] \[1\] \[2\] \[3\]](#)
- [TASKS_MGR_TS1_PC_S3 Register \(Offset = 14h\) \[reset = X\]: \[0\]](#)

15.19.7 TASKS_MGR_TS1_PC_S4 Register (Offset = 18h) [reset = X]

TASKS_MGR_TS1_PC_S4 is shown in [Figure 15-659](#) and described in [Table 15-200](#).

Return to [Summary Table](#).

TS1 Sub4 PC

Table 15-2019. TASKS_MGR_TS1_PC_S4 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B02 A018h
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B12 A018h
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B02 A118h
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B12 A118h
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B02 A218h
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B12 A218h
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B02 A318h
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B12 A318h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h

Figure 15-659. TASKS_MGR_TS1_PC_S4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		TS1_PC_S4													
R/W-X																		R/W-0h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-2020. TASKS_MGR_TS1_PC_S4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TS1_PC_S4	R/W	0h	TS1 Sub4 PC

Table 15-2021. Register Call Summary for TASKS_MGR_TS1_PC_S4

- PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers
- [PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers: \[0\] \[1\] \[2\] \[3\]](#)
 - [TASKS_MGR_TS1_PC_S4 Register \(Offset = 18h\) \[reset = X\]: \[0\]](#)

15.19.8 TASKS_MGR_TS2_PC_S0 Register (Offset = 1Ch) [reset = X]

TASKS_MGR_TS2_PC_S0 is shown in [Figure 15-660](#) and described in [Table 15-2023](#).

Return to [Summary Table](#).

TS2 Sub0 PC

Table 15-2022. TASKS_MGR_TS2_PC_S0 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B02 A01Ch
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B12 A01Ch
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B02 A11Ch
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B12 A11Ch
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B02 A21Ch
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B12 A21Ch
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B02 A31Ch
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B12 A31Ch
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h

Figure 15-660. TASKS_MGR_TS2_PC_S0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		TS2_PC_S0													
R/W-X																		R/W-0h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-2023. TASKS_MGR_TS2_PC_S0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TS2_PC_S0	R/W	0h	TS2 Sub0 PC

Table 15-2024. Register Call Summary for TASKS_MGR_TS2_PC_S0

PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers

- [TASKS_MGR_TS2_PC_S0 Register \(Offset = 1Ch\) \[reset = X\]: \[0\]](#)
- [PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers: \[0\] \[1\] \[2\] \[3\]](#)

15.19.9 TASKS_MGR_TS2_PC_S1 Register (Offset = 20h) [reset = X]

TASKS_MGR_TS2_PC_S1 is shown in [Figure 15-661](#) and described in [Table 15-2026](#).

Return to [Summary Table](#).

TS2 Sub1 PC

Table 15-2025. TASKS_MGR_TS2_PC_S1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B02 A020h
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B12 A020h
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B02 A120h
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B12 A120h
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B02 A220h
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B12 A220h
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B02 A320h
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B12 A320h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h

Figure 15-661. TASKS_MGR_TS2_PC_S1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		TS2_PC_S1													
R/W-X																		R/W-0h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-2026. TASKS_MGR_TS2_PC_S1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TS2_PC_S1	R/W	0h	TS2 Sub1 PC

Table 15-2027. Register Call Summary for TASKS_MGR_TS2_PC_S1

PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers

- [TASKS_MGR_TS2_PC_S1 Register \(Offset = 20h\) \[reset = X\]: \[0\]](#)
- [PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers: \[0\] \[1\] \[2\] \[3\]](#)

15.19.10 TASKS_MGR_TS2_PC_S2 Register (Offset = 24h) [reset = X]

TASKS_MGR_TS2_PC_S2 is shown in [Figure 15-662](#) and described in [Table 15-209](#).

Return to [Summary Table](#).

TS2 Sub2 PC

Table 15-2028. TASKS_MGR_TS2_PC_S2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B02 A024h
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B12 A024h
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B02 A124h
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B12 A124h
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B02 A224h
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B12 A224h
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B02 A324h
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B12 A324h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h

Figure 15-662. TASKS_MGR_TS2_PC_S2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TS2_PC_S2															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-2029. TASKS_MGR_TS2_PC_S2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TS2_PC_S2	R/W	0h	TS2 Sub2 PC

Table 15-2030. Register Call Summary for TASKS_MGR_TS2_PC_S2

- PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers
- [PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers: \[0\] \[1\] \[2\] \[3\]](#)
 - [TASKS_MGR_TS2_PC_S2 Register \(Offset = 24h\) \[reset = X\]: \[0\]](#)

15.19.11 TASKS_MGR_TS2_PC_S3 Register (Offset = 28h) [reset = X]

TASKS_MGR_TS2_PC_S3 is shown in [Figure 15-663](#) and described in [Table 15-2032](#).

Return to [Summary Table](#).

TS2 Sub3 PC

Table 15-2031. TASKS_MGR_TS2_PC_S3 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B02 A028h
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B12 A028h
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B02 A128h
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B12 A128h
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B02 A228h
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B12 A228h
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B02 A328h
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B12 A328h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h

Figure 15-663. TASKS_MGR_TS2_PC_S3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TS2_PC_S3															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-2032. TASKS_MGR_TS2_PC_S3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TS2_PC_S3	R/W	0h	TS2 Sub3 PC

Table 15-2033. Register Call Summary for TASKS_MGR_TS2_PC_S3

PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers

- [PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers: \[0\] \[1\] \[2\] \[3\]](#)
- [TASKS_MGR_TS2_PC_S3 Register \(Offset = 28h\) \[reset = X\]: \[0\]](#)

15.19.12 TASKS_MGR_TS2_PC_S4 Register (Offset = 2Ch) [reset = X]

TASKS_MGR_TS2_PC_S4 is shown in [Figure 15-664](#) and described in [Table 15-2035](#).

Return to [Summary Table](#).

TS2 Sub4 PC

Table 15-2034. TASKS_MGR_TS2_PC_S4 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B02 A02Ch
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B12 A02Ch
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B02 A12Ch
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B12 A12Ch
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B02 A22Ch
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B12 A22Ch
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B02 A32Ch
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B12 A32Ch
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h

Figure 15-664. TASKS_MGR_TS2_PC_S4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		TS2_PC_S4													
R/W-X																		R/W-0h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-2035. TASKS_MGR_TS2_PC_S4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TS2_PC_S4	R/W	0h	TS2 Sub4 PC

Table 15-2036. Register Call Summary for TASKS_MGR_TS2_PC_S4

PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers

- [PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers: \[0\] \[1\] \[2\] \[3\]](#)
- [TASKS_MGR_TS2_PC_S4 Register \(Offset = 2Ch\) \[reset = X\]: \[0\]](#)

15.19.13 TASKS_MGR_RX_CFG Register (Offset = 30h) [reset = X]

TASKS_MGR_RX_CFG is shown in Figure 15-665 and described in Table 15-2038.

Return to [Summary Table](#).

RX Configuration

Table 15-2037. TASKS_MGR_RX_CFG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B02 A030h
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B12 A030h
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B02 A130h
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B12 A130h
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B02 A230h
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B12 A230h
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B02 A330h
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B12 A330h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h

Figure 15-665. TASKS_MGR_RX_CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESE RVED	BKN_SIZE					BK2_SIZE					BK1_SIZE				
R/W-X	R/W-1Fh					R/W-1Fh					R/W-1Fh				

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-2038. TASKS_MGR_RX_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R/W	X	
14-10	BKN_SIZE	R/W	1Fh	RX BKN Size, After BK1 and BK2, then after another 1 to 32 Bytes
9-5	BK2_SIZE	R/W	1Fh	RX BK2 Size, The Second 1 to 32 Bytes trigger
4-0	BK1_SIZE	R/W	1Fh	RX BK1 Size, The first 1 to 32 Bytes trigger

Table 15-2039. Register Call Summary for TASKS_MGR_RX_CFG

PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers

- [PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers: \[0\] \[1\] \[2\] \[3\]](#)
- [TASKS_MGR_RX_CFG Register \(Offset = 30h\) \[reset = X\]: \[0\]](#)

15.19.14 TASKS_MGR_TX_CFG Register (Offset = 34h) [reset = X]

TASKS_MGR_TX_CFG is shown in [Figure 15-666](#) and described in [Table 15-2041](#).

Return to [Summary Table](#).

TX Configuration

Table 15-2040. TASKS_MGR_TX_CFG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B02 A034h
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B12 A034h
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B02 A134h
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B12 A134h
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B02 A234h
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B12 A234h
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B02 A334h
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B12 A334h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h

Figure 15-666. TASKS_MGR_TX_CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								TX_WM							
R/W-X																								R/W-1Fh							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-2041. TASKS_MGR_TX_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	X	
5-0	TX_WM	R/W	1Fh	TX L2 Water Mark Level 1 to 64 Bytes

Table 15-2042. Register Call Summary for TASKS_MGR_TX_CFG

PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers

- [PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers: \[0\] \[1\] \[2\] \[3\]](#)
- [TASKS_MGR_TX_CFG Register \(Offset = 34h\) \[reset = X\]: \[0\]](#)

15.19.15 TASKS_MGR_TS1_GEN_CFG1 Register (Offset = 38h) [reset = 0h]

TASKS_MGR_TS1_GEN_CFG1 is shown in Figure 15-667 and described in Table 15-2044.

Return to [Summary Table](#).

Generic TS1 Configuration1

Table 15-2043. TASKS_MGR_TS1_GEN_CFG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B02 A038h
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B12 A038h
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B02 A138h
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B12 A138h
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B02 A238h
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B12 A238h
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B02 A338h
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B12 A338h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h

Figure 15-667. TASKS_MGR_TS1_GEN_CFG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TS1_GEN_S3_MX								TS1_GEN_S2_MX							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS1_GEN_S1_MX								TS1_GEN_S0_MX							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-2044. TASKS_MGR_TS1_GEN_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TS1_GEN_S3_MX	R/W	0h	TS1 Generic Sub3 MX Select
23-16	TS1_GEN_S2_MX	R/W	0h	TS1 Generic Sub2 MX Select
15-8	TS1_GEN_S1_MX	R/W	0h	TS1 Generic Sub1 MX Select
7-0	TS1_GEN_S0_MX	R/W	0h	TS1 Generic Sub0 MX Select

Table 15-2045. Register Call Summary for TASKS_MGR_TS1_GEN_CFG1

PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers

- [TASKS_MGR_TS1_GEN_CFG1 Register \(Offset = 38h\) \[reset = 0h\]: \[0\]](#)
- [PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers: \[0\] \[1\] \[2\] \[3\]](#)

15.19.16 TASKS_MGR_TS1_GEN_CFG2 Register (Offset = 3Ch) [reset = X]

TASKS_MGR_TS1_GEN_CFG2 is shown in Figure 15-668 and described in Table 15-2047.

Return to [Summary Table](#).

Generic TS1 Configuration2

Table 15-2046. TASKS_MGR_TS1_GEN_CFG2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B02 A03Ch
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B12 A03Ch
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B02 A13Ch
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B12 A13Ch
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B02 A23Ch
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B12 A23Ch
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B02 A33Ch
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B12 A33Ch
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h

Figure 15-668. TASKS_MGR_TS1_GEN_CFG2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TS1_GEN_S4_MX							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-2047. TASKS_MGR_TS1_GEN_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	TS1_GEN_S4_MX	R/W	0h	TS1 Generic Sub4 MX Select

Table 15-2048. Register Call Summary for TASKS_MGR_TS1_GEN_CFG2

PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers

- [PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers: \[0\] \[1\] \[2\] \[3\]](#)
- [TASKS_MGR_TS1_GEN_CFG2 Register \(Offset = 3Ch\) \[reset = X\]: \[0\]](#)

15.19.17 TASKS_MGR_TS2_GEN_CFG1 Register (Offset = 40h) [reset = 0h]

TASKS_MGR_TS2_GEN_CFG1 is shown in Figure 15-669 and described in Table 15-2050.

Return to [Summary Table](#).

Generic TS2 Configuration1

Table 15-2049. TASKS_MGR_TS2_GEN_CFG1 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B02 A040h
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B12 A040h
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B02 A140h
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B12 A140h
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B02 A240h
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B12 A240h
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B02 A340h
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B12 A340h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h

Figure 15-669. TASKS_MGR_TS2_GEN_CFG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TS2_GEN_S3_MX								TS2_GEN_S2_MX							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS2_GEN_S1_MX								TS2_GEN_S0_MX							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-2050. TASKS_MGR_TS2_GEN_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TS2_GEN_S3_MX	R/W	0h	TS2 Generic Sub3 MX Select
23-16	TS2_GEN_S2_MX	R/W	0h	TS2 Generic Sub2 MX Select
15-8	TS2_GEN_S1_MX	R/W	0h	TS2 Generic Sub1 MX Select
7-0	TS2_GEN_S0_MX	R/W	0h	TS2 Generic Sub0 MX Select

Table 15-2051. Register Call Summary for TASKS_MGR_TS2_GEN_CFG1

PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers

- [PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers: \[0\] \[1\] \[2\] \[3\]](#)
- [TASKS_MGR_TS2_GEN_CFG1 Register \(Offset = 40h\) \[reset = 0h\]: \[0\]](#)

15.19.18 TASKS_MGR_TS2_GEN_CFG2 Register (Offset = 44h) [reset = X]

TASKS_MGR_TS2_GEN_CFG2 is shown in Figure 15-670 and described in Table 15-2053.

Return to [Summary Table](#).

Generic TS2 Configuration2

Table 15-2052. TASKS_MGR_TS2_GEN_CFG2 Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B02 A044h
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B12 A044h
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B02 A144h
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B12 A144h
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B02 A244h
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B12 A244h
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B02 A344h
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B12 A344h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h

Figure 15-670. TASKS_MGR_TS2_GEN_CFG2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TS2_GEN_S4_MX							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-2053. TASKS_MGR_TS2_GEN_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	TS2_GEN_S4_MX	R/W	0h	TS2 Generic Sub4 MX Select

Table 15-2054. Register Call Summary for TASKS_MGR_TS2_GEN_CFG2

PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers

- [PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers: \[0\] \[1\] \[2\] \[3\]](#)
- [TASKS_MGR_TS2_GEN_CFG2 Register \(Offset = 44h\) \[reset = X\]: \[0\]](#)

15.19.19 TASKS_MGR_CAP_EN_CFG Register (Offset = 48h) [reset = X]

TASKS_MGR_CAP_EN_CFG is shown in Figure 15-671 and described in Table 15-2056.

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This register allows you to enable a capture of a new event when you are active in the sub task. By default, all new events to the same active task are masked until you exit that sub task from being captured. When disabled (reset state). All new events to the current active task are masked from being captured. Only when this task is completed a new event can get captured for that task. When enabled, a new event which occurs in a current active task will get captured, when that task yields it will reenter that same task if not other higher priority events are pending.

Table 15-2055. TASKS_MGR_CAP_EN_CFG Instances

Instance	Physical Address
PRU_ICSSG0_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B02 A048h
PRU_ICSSG1_PR1_TASKS_MGR_PRU0_PR1_TASKS_MGR_PRU0_MMR	0B12 A048h
PRU_ICSSG0_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B02 A148h
PRU_ICSSG1_PR1_TASKS_MGR_RTU0_PR1_TASKS_MGR_RTU0_MMR	0B12 A148h
PRU_ICSSG0_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B02 A248h
PRU_ICSSG1_PR1_TASKS_MGR_PRU1_PR1_TASKS_MGR_PRU1_MMR	0B12 A248h
PRU_ICSSG0_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B02 A348h
PRU_ICSSG1_PR1_TASKS_MGR_RTU1_PR1_TASKS_MGR_RTU1_MMR	0B12 A348h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX0_PR1_TASKS_MGR_PRU_TX0_MMR	A400h
PRU_ICSSG0_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h
PRU_ICSSG1_PR1_TASKS_MGR_PRU_TX1_PR1_TASKS_MGR_PRU_TX1_MMR	A500h

Figure 15-671. TASKS_MGR_CAP_EN_CFG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED			CAP_NEW_TS1_EN_S4	CAP_NEW_TS1_EN_S3	CAP_NEW_TS1_EN_S2	CAP_NEW_TS1_EN_S1	CAP_NEW_TS1_EN_S0
R/W-X			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-2056. TASKS_MGR_CAP_EN_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R/W	X	
4	CAP_NEW_TS1_EN_S4	R/W	0h	Capture new event enable. TS1 Sub4.
3	CAP_NEW_TS1_EN_S3	R/W	0h	Capture new event enable. TS1 Sub3.
2	CAP_NEW_TS1_EN_S2	R/W	0h	Capture new event enable. TS1 Sub2.
1	CAP_NEW_TS1_EN_S1	R/W	0h	Capture new event enable. TS1 Sub1.
0	CAP_NEW_TS1_EN_S0	R/W	0h	Capture new event enable. TS1 Sub0.

Table 15-2057. Register Call Summary for TASKS_MGR_CAP_EN_CFG

PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers

- [PRU_TASKS_MGR_TASKS_MGR_PRU_RTU Registers: \[0\] \[1\] \[2\] \[3\]](#)
- [TASKS_MGR_CAP_EN_CFG Register \(Offset = 48h\) \[reset = X\]: \[0\]](#)

15.20 PRU_ICSSG_RAM Registers

Table 15-2059 lists the memory-mapped registers for the PRU_ICSSG_RAM registers. All register offset addresses not listed in Table 15-2059 should be considered as reserved locations and the register contents should not be modified.

Table 15-2058. PRU_ICSSG_RAM Instances

Instance	Base Address
PRU_ICSSG0_RAM_SLV_RAM	0B01 0000h
PRU_ICSSG1_RAM_SLV_RAM	0B11 0000h

Table 15-2059. PRU_ICSSG_RAM Registers

Offset	Acronym	Register Name	PRU_ICSSG0_RAM_SLV_RAM Physical Address	PRU_ICSSG1_RAM_SLV_RAM Physical Address
0h + formula	ICSSG_RAM_REG_y	RAM memory word	0B01 0000h + formula	0B11 0000h + formula

15.20.1 ICSSG_RAM_REG_y Register (Offset = 0h + formula) [reset = 0h]

ICSSG_RAM_REG_y is shown in Figure 15-672 and described in Table 15-2061.

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The RAM memory words provide memory mapped random access data storage.

Offset = 0h + (y * 4h); where y = 0h to 3FFFh

Table 15-2060. ICSSG_RAM_REG_y Instances

Instance	Physical Address
PRU_ICSSG0_RAM_SLV_RAM	0B01 0000h + formula
PRU_ICSSG1_RAM_SLV_RAM	0B11 0000h + formula

Figure 15-672. ICSSG_RAM_REG_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BYTE3								BYTE2								BYTE1								BYTE0							
R/W-0h								R/W-0h								R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-2061. ICSSG_RAM_REG_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	BYTE3	R/W	0h	This is the MSB (Most Significant Byte)
23-16	BYTE2	R/W	0h	This is the UMB (Upper Middle Byte)
15-8	BYTE1	R/W	0h	This is the LMB (Lower Middle Byte)
7-0	BYTE0	R/W	0h	This is the LSB (Least Significant Byte)

Table 15-2062. Register Call Summary for ICSSG_RAM_REG_y

PRU_ICSSG_RAM Registers

- [PRU_ICSSG_RAM Registers](#): [0]
- [ICSSG_RAM_REG_y Register \(Offset = 0h + formula\) \[reset = 0h\]](#): [0]

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