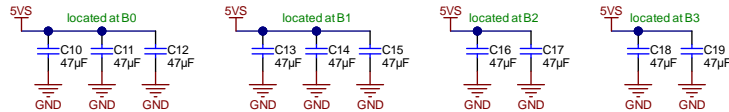
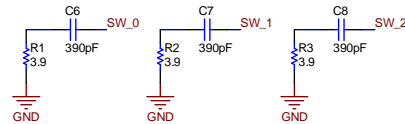


Sequencing:

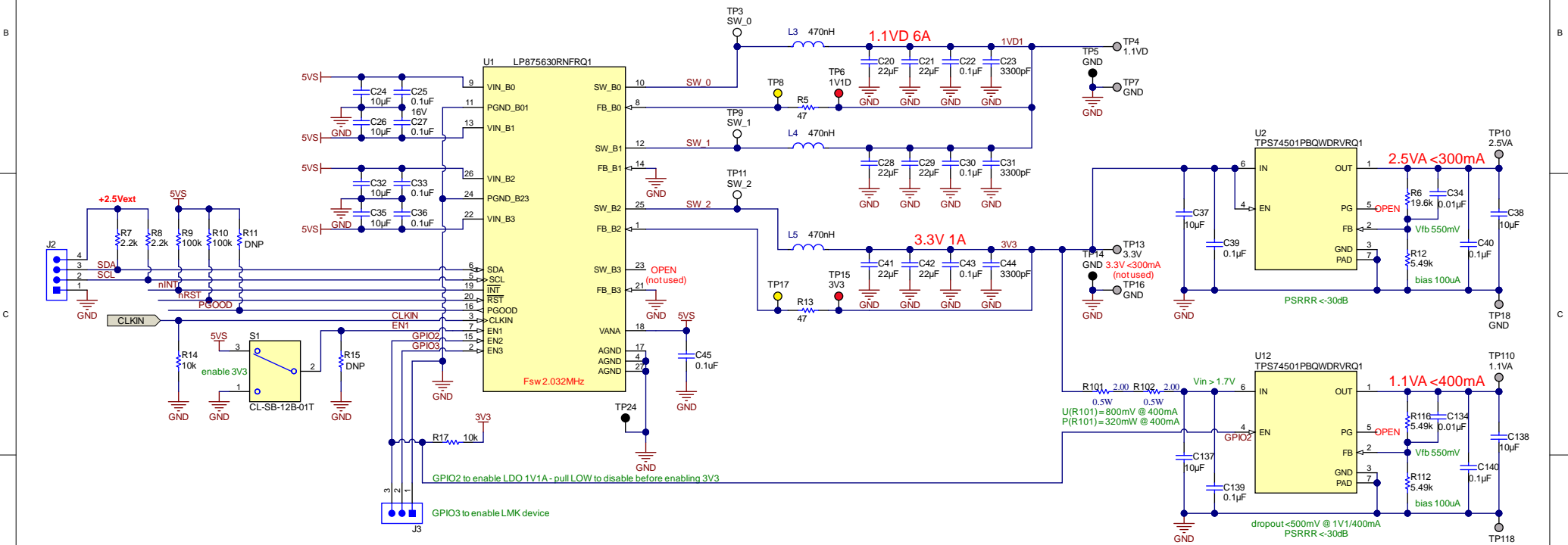
SWITCH S1 sets EN1 and rises 3V3; -> O.K.
 output voltage 3V3 enables LDO 2V5; -> O.K.
 1V1A and 1V1D are enabled with 7ms..15ms delay regarding rise of 2V5.
 (to be adjusted by OTP file); -> measured delay around 11ms, O.K.



bulk capacitors located to each power stage input



recommended RC snubber circuits to each switch node



Revision History	
Revision	Notes
A	*** preliminary *** Single LDO - used ph3
B	*** preliminary *** Two LDOs - ph 3 NOT used
B1	removed snubber for BUCK3, FB_B3 to GND
C	C6, C7 and C8 changed size to 0603 new LDO, built & tested

Design Notes:
 1) R5, R13 for test purposes only
 2) silk screen 1.1VA is swapped - electrically OK

RevC, LDO TPS74501
RevB, proposal w/ LDO 1V1A - third phase PMIC unused

Orderable:	Designed for: Public Release	Mod. Date: 6/8/2022
TID #: 1VA	Project Title: Automotive Supply using PMIC	
Number: PMP30819	Rev: C1	Sheet Title: PMP30819RevC1
SVN Rev: Not in version control	Assembly Variant: [No Variations]	Sheet 1 of 1
Drawn By: B.Geck	File: PMP30819RevC1_schematic.SCHDOC	Size: A3
Engineer: B.Geck	Contact: http://www.ti.com/support	© Texas Instruments 2020

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