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TI Designs - Precision: Verified Design
Isolated, Shunt-Based Current Sensing Reference Design

TEXAS INSTRUMENTS

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Design Resources

Design Archive	All design files
TINA-TI™	SPICE simulator
AMC1304	Product folder
TMS320F28377D	Product folder
TPS79533	Product folder
SN6501	Product folder

Circuit Description

This isolated data acquisition system based on an isolated delta-sigma (ΔΣ) modulator and a microcontroller can accurately measure currents in the -10 A to 10 A range when used with the appropriate current shunts. This circuit was designed to provide excellent galvanic isolation and accuracy targeted primarily for a current sensing application. The design provides dual functionality for a high resolution channel and an additional over-current or short-circuit detection channel.

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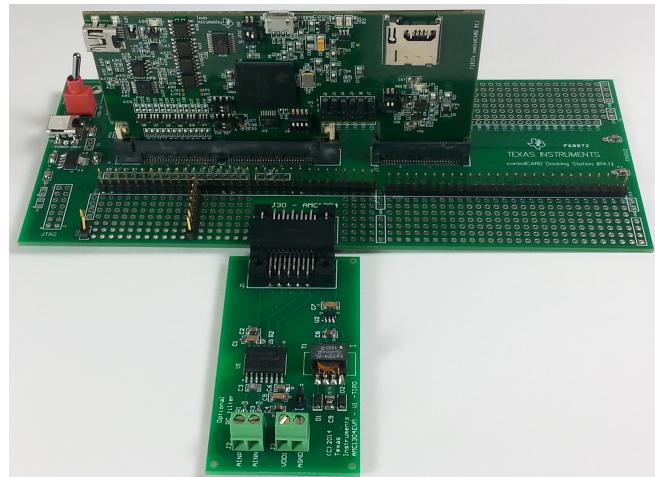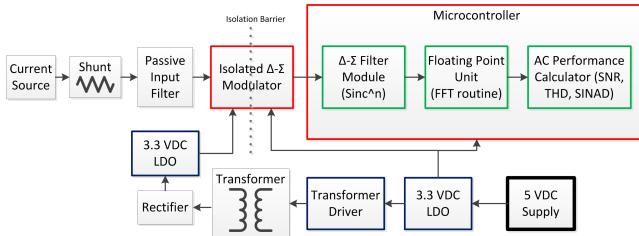
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1 Design Summary

The primary objective for this TI Precision Design is to create a isolated data acquisition system to meet the following specifications:

- Maximum current range in normal operation: 10 A$_{peak}$
- Uncalibrated accuracy (only for measurement of voltage drop across the shunt): 0.3% FSR
- Signal to noise ratio (SNR) at 1 kHz: 78dB
- Minimum sampling rate: 70 kSPS
- Minimum bandwidth: 20 kHz
- Supply level: 5 V

The design goals and performance are summarized in Table 1. The output of the acquisition system for a full scale input 1kHz signal is shown in response in Figure 1.

Table 1. Comparison of Design Goal, Simulation, and Measured Performance

PARAMETER	GOAL	SIMULATED / CALCULATED	MEASURED
Uncalibrated accuracy (%)	0.3	0.022	0.102
Signal to noise ratio at 1 kHz (dB)	78	85	83.41
Bandwidth (kHz)	20	20.47	20.4
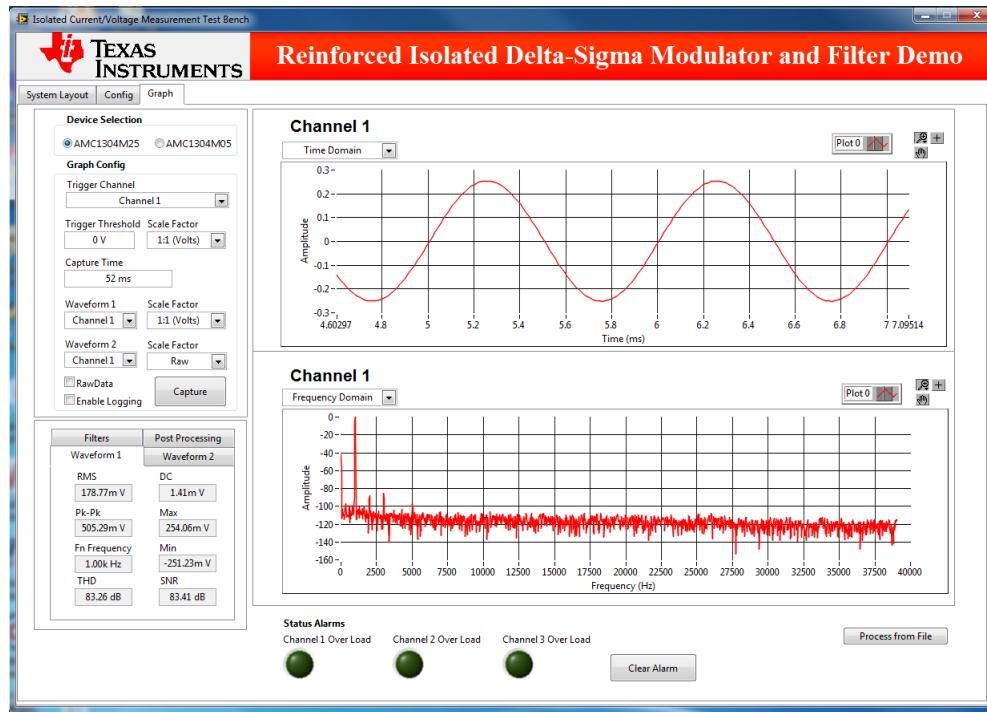
Figure 1. System Output for a Full Scale, 1kHz Input signal

2   Theory of Operation

Galvanic isolation is a key requirement in many industrial applications. Isolation provides not only technical advantages such as breaking noisy ground loops in the signal path, but also protects the end user and sensitive equipment in the controller side from potentially dangerous high voltage and transients on the analog input side (also commonly referred to as the high side). For the case of current monitoring, an isolated acquisition system could be constructed as shown in Figure 2, where the input current is transformed into an analog voltage signal with a current shunt, and such voltage is filtered and then fed to the input of an isolated delta-sigma modulator.
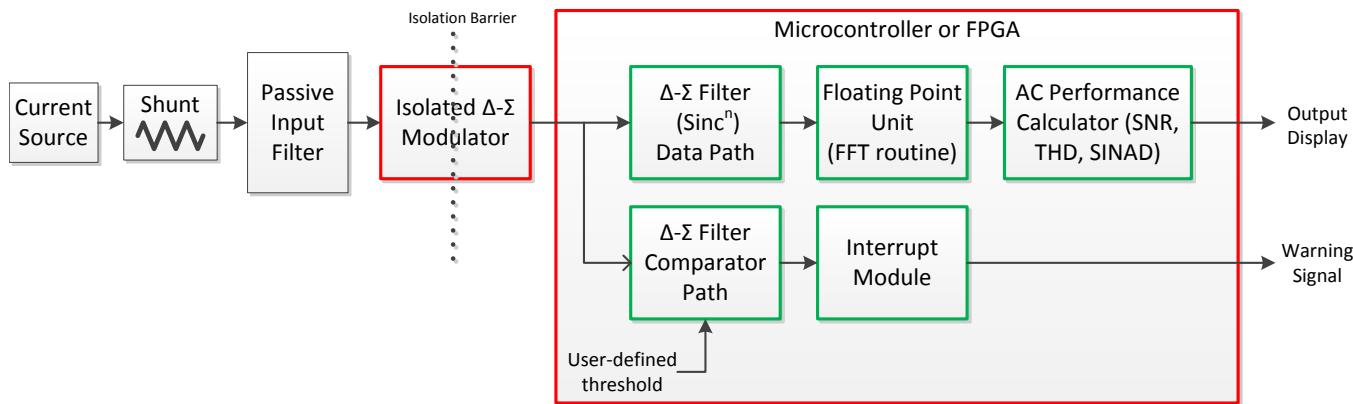

Figure 2. Data Acquisition System Using Isolated Delta-Sigma Modulator

Although the primary task of most isolated acquisition systems is to achieve high precision and accuracy at the required data rate, there is a secondary function that can be implemented by choosing the system architecture depicted in Figure 2. Since the user obtains a delta-sigma modulated bit stream on the controller side, two digital signal processing paths can be implemented. For the sake of illustration suppose that the primary path decimates the incoming bit stream (for example supplied at 20 MHz) by a factor of 256. This primary digital signal processing path yields a high-resolution current measurement at 78.1 kSPS. Then, a secondary digital signal processing path can be implemented with the objective of generating a warning signal if there is a sudden current spike (as in the case of an over-current or a short-circuit event). This secondary digital signal processing path takes the same single-bit, delta-sigma modulated stream that is concurrently processed by the primary path but it applies a much lower decimation factor. If for example the secondary decimation factor is chosen as 4, the user obtains a secondary signal output at 5 MSPS and this signal can be compared in real time to a pre-set threshold. If the threshold is exceeded, an appropriate command signal can be issued in order to open a safety relay or de-energize sensitive components in the application. Using a single delta-sigma modulator allows the user to implement these two digital signal processing paths.

The integration of the digital isolation barrier into a single IC allows the solution shown in Figure 2 to save board space and lower the component count of the system. These are important features because they bring about simplified board assembly, higher board reliability and lower overall solution cost.

As shown in Figure 2, the analog signal path starts with the current to be sensed. Such current causes a voltage drop across the resistive shunt and this voltage drop is transformed into a digital bit stream by an isolated delta-sigma modulator. The digital output of the isolated delta-sigma modulator is then filtered and decimated to obtain codewords of a desired length.

2.1 Shunt Resistor Sizing

The first step in the design is to select a resistive current shunt. Figure 3 shows the typical location of the current shunt in isolated current sensing applications.
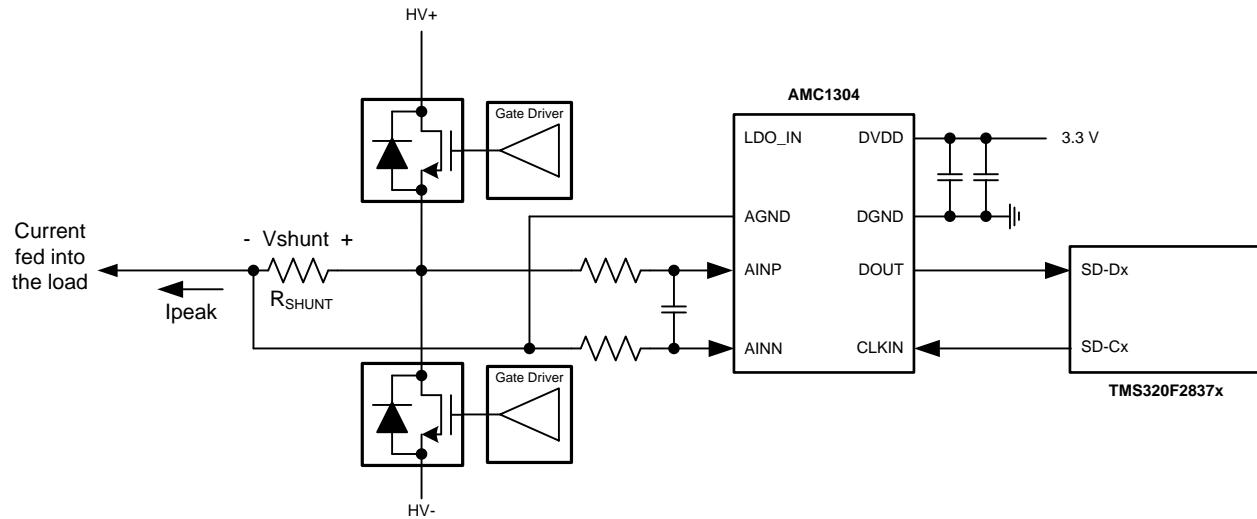

Figure 3. Typical Shunt Location

The current shunt is sized according to Equation 1.

$$R_{shunt} = \frac{V_{shunt}}{I_{peak}} = \frac{\text{Maximum of linear input range to } \Delta\Sigma \text{ mod}}{I_{peak}}$$

(1)

V_{shunt} is the voltage drop produced when the peak current (I_{peak}) flows through the shunt. Such voltage drop can be readily fed into the delta sigma modulator. Note that in order to optimize the acquisition system, the choice of R_{shunt} should be done such that the voltage drop across it is equal to the maximum input available in the linear input range of the delta sigma modulator.

In addition to the method described above, there are designs where the shunt sizing is performed based on the maximum power dissipation allowed on the shunt. Section 8 explains this alternative method.

2.2 *Input Passive Filter Design*

Depending on the characteristics of the delta-sigma modulator input it may be necessary to include a passive filter between the current shunt and the modulator input. The purpose of the filter is to reject signals with frequencies outside the band of interest and that may be aliased into the band of interest during the analog to digital conversion process. The constraint to keep in mind in the filter design is that, if the corner frequency of the filter is too low, fast signals (such as those present in a short circuit event) could be distorted to the point where the system becomes ineffective or reacts too slowly to these events. A compromise needs to be made between aggressive filtering and the system's response to a step input.

A passive filter such as that depicted in Figure 4 has a corner frequency determined by Equation 2.

$$f_{-3dB} = \frac{1}{2\pi(R_1 + R_2)C}$$

(2)
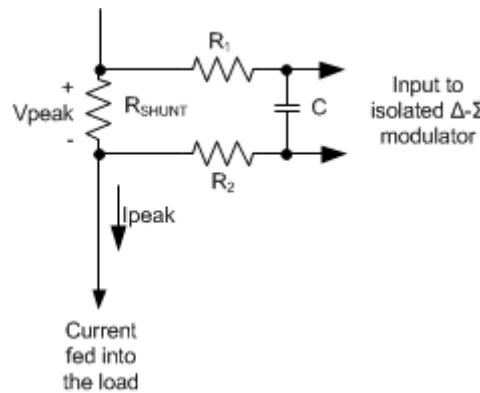
Figure 4. Analog Input Filter

Note that an input passive filter is not needed in every application. In some cases, the filtering provided by the analog front end of the delta-sigma modulator is sufficient for the application needs. For example, as shown in Section 3.3, the AMC1304M25 has a 1 MHz bandwidth.

Note also that the digital filter included in the design provides also a level of filtering as shown in Figure 10.

2.3 *Delta-Sigma Modulator*

Figure 5 shows the block diagram of a second-order, switched-capacitor, feed-forward delta-sigma modulator (also referred to as ΔΣ modulator). For this type of modulator, the analog input voltage V_{IN} and the output V_5 of the 1-bit digital-to-analog converter (DAC) are differentiated, providing an analog voltage V_1 at the input of the first integrator stage. The output of the first integrator feeds the input of the second integrator stage, resulting in output voltage V_3 that is differentiated with the input signal V_{IN} and the output of the first integrator V_2. The output of the clocked comparator changes depending on the polarity of the resulting signal V_4 and such output is sent to the DOUT pin of the IC. Note that the feedback loop is closed by the 1-bit DAC which responds on the next clock pulse by changing its analog output voltage V_5, causing the integrators to progress in the opposite direction while forcing the value of the integrator output to track the average value of the input.
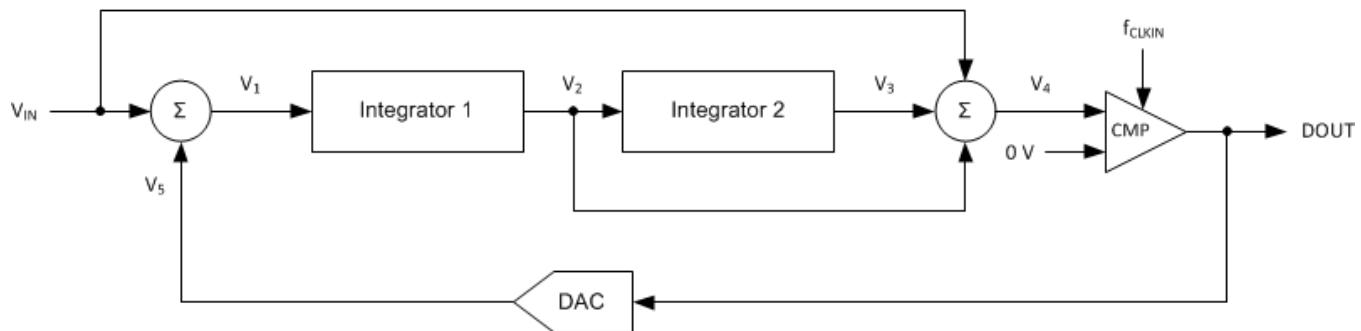
Figure 5. Block Diagram of a Second-Order ΔΣ Modulator

This type of delta-sigma modulator shifts the quantization noise to high frequencies, as shown in Figure 6.
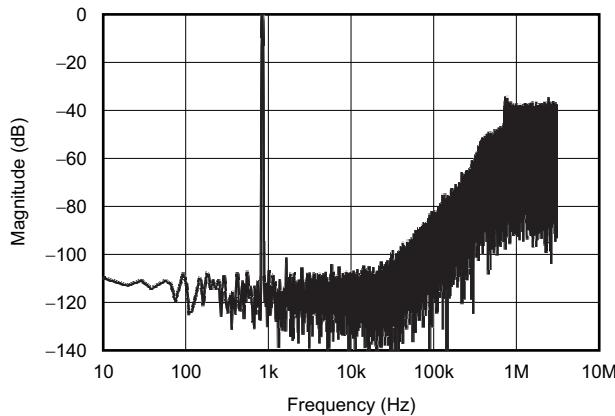
Figure 6. Quantization Noise Shaping

2.4 Digital Filter

As explained in Section 2.3, the delta-sigma modulator shapes the quantization noise such that it is shifted into high frequency. Given this fact, the natural progression in the design is to filter the delta-sigma modulator output such that one can observe the signal present in the band of interest while attenuating the quantization noise that fall outside such band. At the same time, the digital filtering will serve the purpose of decimating the output of the delta-sigma modulator from values typically in the millions of bits per second range (MBPS) to the thousands of samples per second range (kSPS).

There are many types of digital filters that could be used in this application; however, this design will only consider a family of digital filters known as Cascaded Integrator-Comb (CIC) filters. These filters are commonly used to process the output of delta-sigma modulators because of the performance they offer at a low level of complexity and relatively small implementation size.

CIC filters are often used for implementing large sample rate changes in digital systems. They are typically employed in applications that have a large excess sample rate. That is, the system sample rate (20 MSPS in the example described at the beginning of Section 2) is much larger than the bandwidth occupied by the processed signal (20 kHz as derived from the bandwidth requirement prescribed in Section 1). Implementations of CIC filters have structures that use only adder-subtractors and delay elements. These structures make CIC filters appealing for their hardware-efficient implementations of multirate filtering.

There are two sections to the CIC decimator filter:

- An integrator section with N integrator stages that processes input data samples at sampling rate fs, and
- A comb section that operates at the lower sampling rate fs / R. This comb section consists of N comb stages with a differential delay of M samples per stage. The down sampling operation decimates the output of the integrator section by passing only every Rth sample to the comb section of the filter.

Figure 7 shows a block diagram of a CIC filter.
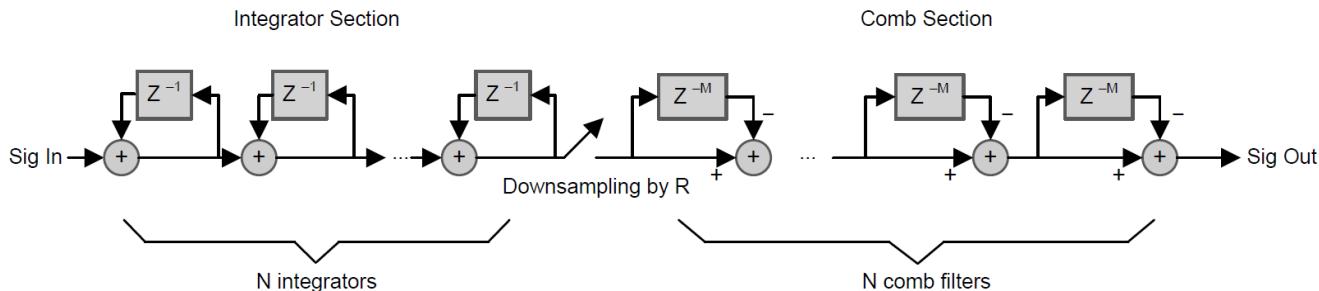
Figure 7. CIC Filter Structure

2.4.1 CIC Integrator Stage

The block diagram of a CIC integrator stage is illustrated in Figure 8 . The difference equation that describes the integrator stage is given by:

$$y(n) = x(n) + y(n-1) \tag{3}$$
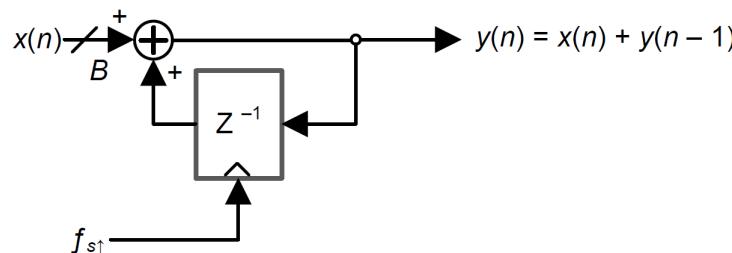
Figure 8. CIC Integrator Section

The corresponding z-transform and transfer function is given by

$$H_I(z) = \frac{1}{1 - z^{-1}}$$

(4)

The transfer function of N concatenated integrators is given by

$$[H_I(z)]^N = \left[\frac{1}{1 - z^{-1}}\right]^N$$

(5)

2.4.2 CIC Comb Filter Stage

Figure 9 illustrates the general form of the comb filter architecture where the parameter M specifies the programmable comb filter differential delay. The output sequence generated by this structure is given by the difference equation

y(n) = x(n) - x(n-M)

(6)
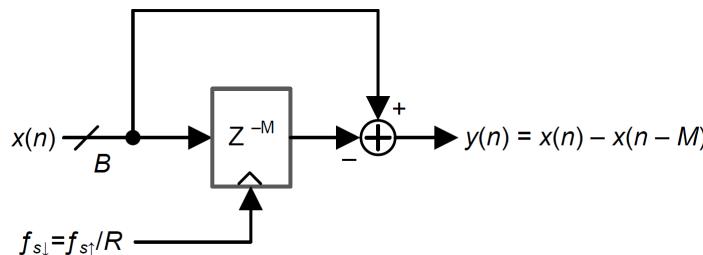
Figure 9. CIC Comb Filter Section

Although M could take on many possible values, the best CIC filter performance is generally obtained by limiting M to be 1 or 2. Taking the Z transform of both sides of Equation 6 yields:

y(n) = (1 - $(z_c)^{-M}$) X(z_c)

(7)

Therefore, the corresponding transfer function is:Equation 8

$$H_C(z_C) = 1 - z_C^{-M}$$

(8)

The transfer function of N concatenated comb filter sections is given by

$$[H_C(z_C)]^N = \left[1 - z_C^{-M}\right]^N$$

(9)

2.4.3 Overall CIC Transfer Function

Equation 10 shows the overall CIC filter response, which is composed of both the comb frequency response $H_C(z)$ and the integrator frequency response $H_I(z)$ in cascade.

$$H_{CIC\_filter} = \left[\frac{1 - z_C^{-M}}{1 - z^{-1}} \right]^N$$

(10)

Note that the comb section and the integrator section operate at different rates. Such rates can be expressed by evaluating the complex variables "z" and "z_c" in the unit circle as:

$$z = e^{j\varpi}$$

(11)

$$z_c = e^{jR\varpi}$$

(12)

The frequency response of the CIC filter is found by substituting Equation 11 and Equation 12 into Equation 10. The substitution yields:

$$H(\varpi) = \left[\frac{1 - e^{-j\varpi RM}}{1 - e^{-j\varpi}} \right]^N$$

(13)

Substituting M = 1 in Equation 13 yields the frequency response of a Sinc^N filter. Figure 10 shows an example of the magnitude in dB of the Sinc3 filter transfer function. Note that Sinc3 filters have significant attenuation (notches) at integer multiples of the output data rate (calculated as $f_{DATA} = f_{CLK} / R$). Also, the –3dB point is located at $0.262 f_{DATA}$.

$f_{DATA} = 20MHz/64 = 312.5kHz$
-3dB: 81.9kHz
OSR = 64
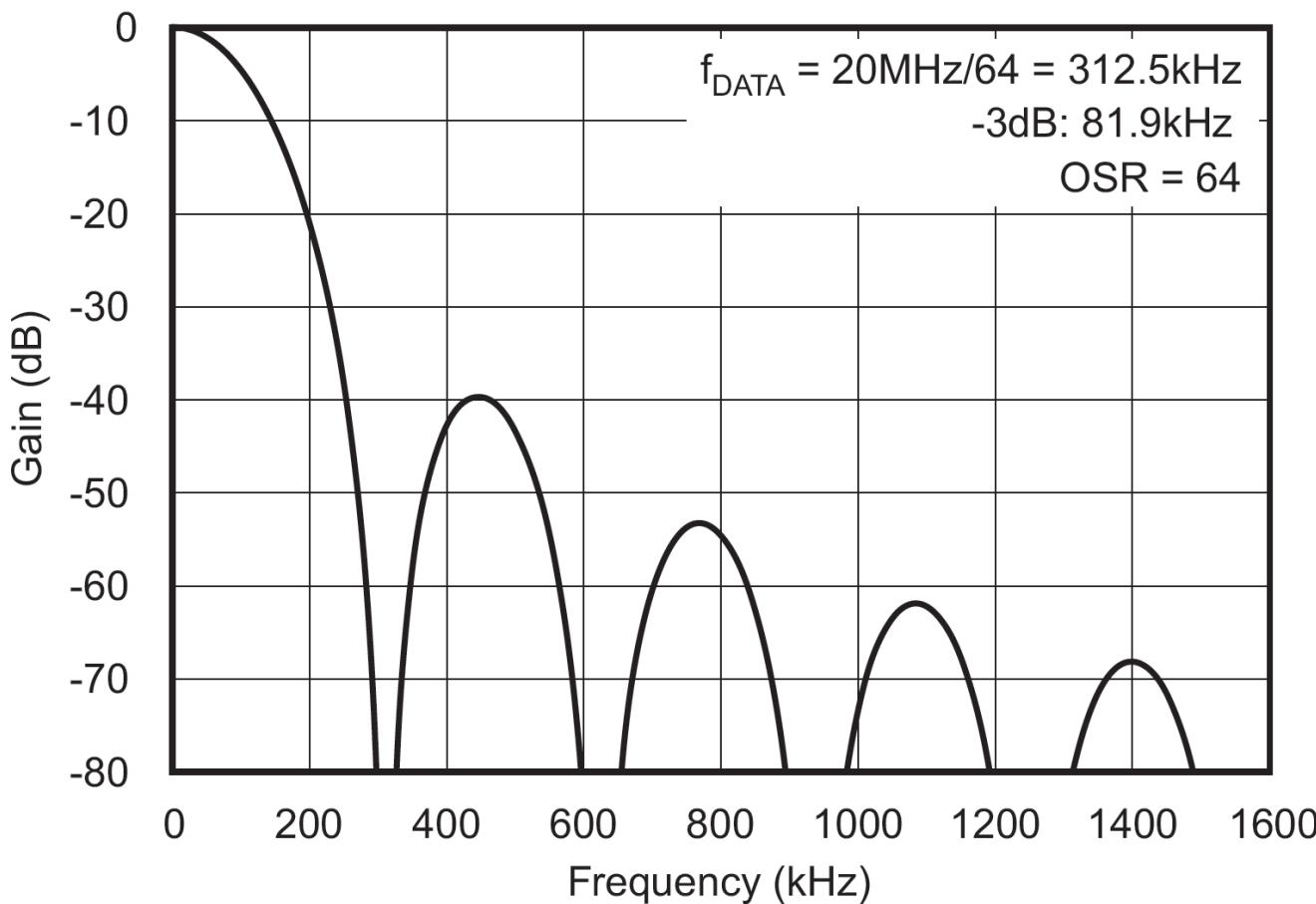
Figure 10. Frequency Response of Sinc3 Filter - Magnitude vs. Frequency

3 Component Selection

With the theoretical background explained in Section 2 one can now proceed to select the components needed to meet the design requirements in Section 1.

The following subsections will explain the rationale behind the specific choices in each part of the design; however, the system is so inter-related that it is not possible to design the sections without having some previous information on the rest of the portions of the design. For this reason it is better to establish now that two of the components chosen in the design are the AMC1304M25 isolated sigma-delta modulator and the TMS320F28377D dual-core Delfino™ microcontroller.

Figure 11 shows the block diagram of the complete design including the power management section.
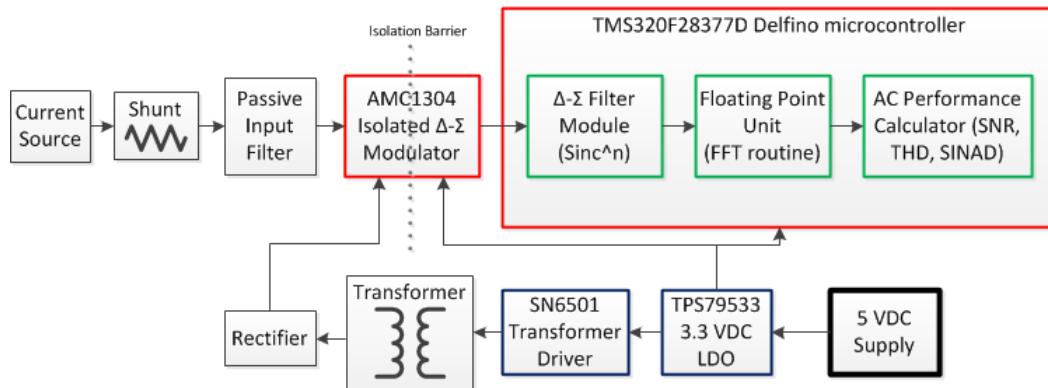
Figure 11. Block Diagram of the Complete Design

3.1 Current Shunt

As indicated in Section 1, this design is specifically targeted for measuring up to 10 A of peak current. The current shunt selection needs to allow a full-scale input voltage that matches as closely as possible the linear input range of the AMC1304M25. According to the AMC1304M25 datasheet, the linear input range of the device extends from -250 mV to 250 mV; therefore, the 25 mΩ Y14740R02500D0W current shunt is chosen. The Y14740R02500D0W has a resistance tolerance of 0.5% and a power rating of 4 W (12.6 A maximum continuous current).

3.2 Input Passive Filter

The input passive filter needs to attenuate noise signals picked up in the connections between the current source, the current shunt and the AMC1304M25 analog input. Inherently the needs of the system dictate the use of a low-pass filter and the first step in designing such passive filter is to establish a sensible range of frequencies where one could possibly choose the location of the filter's cutoff.

First let us examine the minimum bound for the range of cut-off frequencies. As indicated in Section 1, this design needs to perform current measurements at a rate of at least 70 kSPS. Given this sampling rate constraint and invoking the Nyquist-Shannon sampling theorem, the input passive filter must allow all signals below 35 kHz to pass freely into the AMC1304 input.

The upper bound on the filter's cutoff frequency depends on the inherent characteristics of the AMC1304M25 analog front end. According to the AMC1304M25 datahseet, the input bandwidth of the device is 1 MHz. With this in mind, if an input passive filter is included (note that not every application will require one), it must have a cutoff frequency above 35 kHz and below 1 MHz.

If the only functionality desired is high precision data acquisition at 70 kSPS or more, then a filter with cutoff frequency chosen between 35 kHz and 1 MHz will suffice; however, one of the requirements for this design is to have the capability to issue a warning signal in the event that an over-current event or short-circuit occurs (see Section 1). Because of this requirement, the step response of the input passive filter will play a role in the total time it takes the system to identify an over-current event. Departing from the assumption that the over-current event exhibits the waveform shown in Figure 12, the time it takes for the filter output (directly connected to the input to the AMC1304M25) is given by Equation 14.
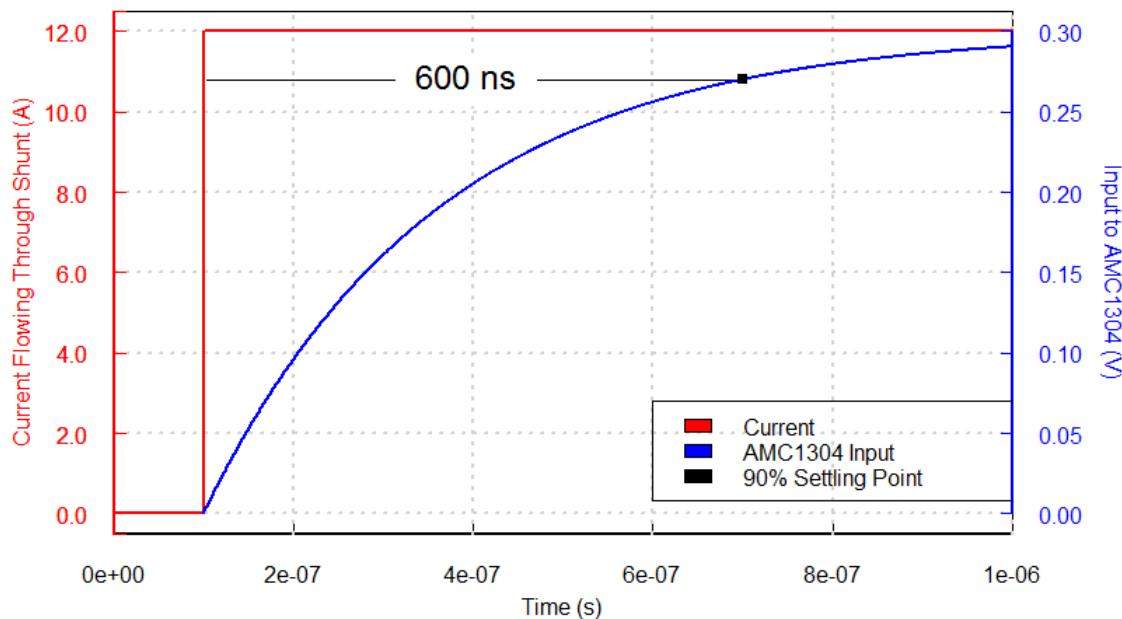
**Figure 12. Typical Step Response of RC Passive Filter**

$$t = -RC\ln(1 - Settling)$$

(14)

Setting a 0.6 µs time budget for the delay in the input filter settling, the time constant of the filter (RC term in Equation 14) can be calculated for a 90 percent settling of the input to the AMC1304 when a 12 A over-current event occurs.

Substituting t = 0.6 µs, Settling = 0.9, and solving for RC in Equation 14 yields: RC = 260.6 ns.

$$RC = \frac{-t}{\ln(1 - Settling)} = \frac{-0.6\mu s}{\ln(1 - 0.9)} = 260.6ns$$

(15)

According to the AMC1304M25 datahseet, the typical input bias current of the AMC1304M25 is 60 µA. A choice of R1 = R2 = 20 Ω allows the voltage drop on either leg of the input filter to be 1.2 mV. Such small voltage will not move the AMC1304M25 input outside of its common-mode range during normal operation.

The maximum capacitor value (in order to comply with the 90% settling constraint set) can be readily found as C = (260.6 ns)÷(40 Ω) = 6.51 nF. The values selected for this design are 20 Ω and 5.6 nF as shown in Figure 13.
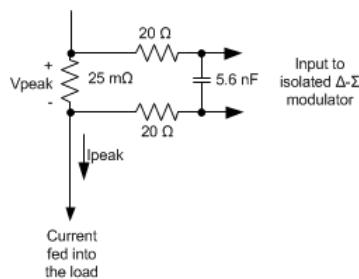
Figure 13. RC Passive Filter Selected

3.3 Delta-Sigma Modulator

The selection of an appropriate delta-sigma modulator for this design is based on the following criteria:

- Isolation voltage: the AMC1304 family provides an outstanding combination of isolation characteristics. Among them are 1 kV_{RMS} of working insulation voltage over the life of the part, 10 kV surge immunity and 7 kV_{peak}transient over-voltage.

- Analog input range: there are two options in the AMC1304 family that could be used for this design. There are devices with +/- 250 mV input range and there are devices with +/- 50 mV input range. For this design the AMC1304M25 is chosen (+/- 250 mV range) and the implications of choosing the alternative option are discussed in Section 6.

- Analog input bandwidth: once again, there are two options in the AMC1304 family that could be used for this design. There are devices with 1 MHz of input bandwidth (corresponding to the +/- 250 mV input range devices) and there are devices with 800 kHz of input bandwidth (corresponding to the +/- 50 mV input range devices). For this design the AMC1304M25 is chosen (1 MHz of input bandwidth and +/- 250 mV range) and the implications of choosing the alternative option are discussed in Section 6.

- AC performance: according to the AMC1304M25 datahseet, the typical signal to noise ratio (SNR) achievable at 1 kHz meets the design requirements established in Section 1 when the digital filter used is a Sinc3 filter with over-sampling ratio of 256.

- DC performance: offset error, gain error and non-linearity are the key specifications of the AMC1304 that determine the dc performance of the design. Among all TI's isolated ΔΣ modulators, the family of AMC1304 products offers the best dc performance specifications.

- Stability over temperature: gain error offset drift and offset error thermal drift of the AMC1304 determine the maximum variation of the system accuracy when temperature changes. Among all TI's isolated ΔΣ modulators, the family of AMC1304 products offers the best stability over temperature specifications.

- Clock frequency: the typical input clock frequency of the AMC1304 products is 20 MHz. The AMC1304 operating at 20 MHz and feeding into a Sinc3 filter with over-sampling ratio of 256 allows this design to meet the ac performance and sampling rate requirements provided in Section 1.

- Digital interface: there are two digital interface options in the AMC1304 family; however, the CMOS interface option makes the most sense for this design since the physical location of the isolated ΔΣ modulator with respect to the microcontroller is not a design constraint. The implications of choosing the alternative option are discussed in Section 6.

In order to properly process the AMC1304 output bit-stream one needs to keep in mind that a differential input signal of 0 V ideally produces a stream of ones and zeros that are high 50% of the time. A differential input of 250 mV (for the AMC1304x25) or 50 mV (for the AMC1304x05) produces a stream of ones and zeros that are high 90% of the time. A differential input of –250 mV (–50 mV for the AMC1304x05) produces a stream of ones and zeros that are high 10% of the time. These input voltages are also the specified linear ranges of the different AMC1304 versions with performance as specified in the AMC1304M25 datahseet. If the input voltage value exceeds these ranges, the output of the modulator shows non-linear behavior while the quantization noise increases. The output of the modulator would clip with a stream of only zeros with an input less than or equal to –312.5 mV (–62.5 mV for the AMC1304x05) or with a stream of only ones with an input greater than or equal to 312.5 mV (62.5 mV for the AMC1304x05). In this case, however, the AMC1304 generates a single 1 (if the input is at negative full-scale) or 0 every 128 clock cycles to indicate proper device function (consult the Detailed Description section of the AMC1304M25 datahseet for more details). The input voltage versus the output modulator signal is shown in Figure 14.

The density of ones in the output bit-stream for any input voltage value (with the exception of a full-scale input signal as described in the Detailed Description section of the AMC1304M25 datahseet) can be calculated using Equation 16:

$$\frac{V_{IN} + V_{Clipping}}{2 * V_{Clipping}}$$

(16)

The AMC1304 system clock in this design can be provided directly from the TMS320F28377D microcontroller or it can be provided externally by an arbitrary waveform or clock generator. Data are synchronously provided from the AMC1304M25 into the TMS320F28377D at the clock rate through the DOUT pin. Bits coming out of the AMC1304 transition at the CLKIN falling edge.
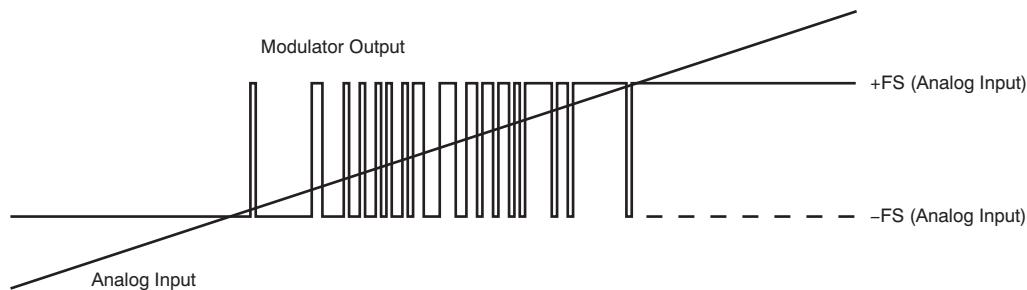
Figure 14. Analog Input versus AMC1304 Modulator Output

Table 2 provides a summary of the AMC1304M25 specifications relevant in this design.

Table 2. Important AMC1304M25 Specifications

Specification	Value
Maximum working insulation voltage	1000 V_{RMS}
Analog input range	± 250 mV
Offset error	40 µV
SNR	85 dB
Analog input bandwidth	1 MHz
Gain error	0.02 % FSR
Integral non-linearity	1.5 LSB
Common-mode rejection ratio	76 dB

3.4   Digital Filter

The application and implementation section of the AMC1304M25 datahseet shows the effective number of bits that can be obtained for different types of filters and over-sampling ratios.

In particular, Figure 15 is duplicated from the AMC1304M25 datahseet and can be used to determine what combination of filter and oversampling ratio (OSR) can be selected to achieve a particular effective number of bits (ENOB).
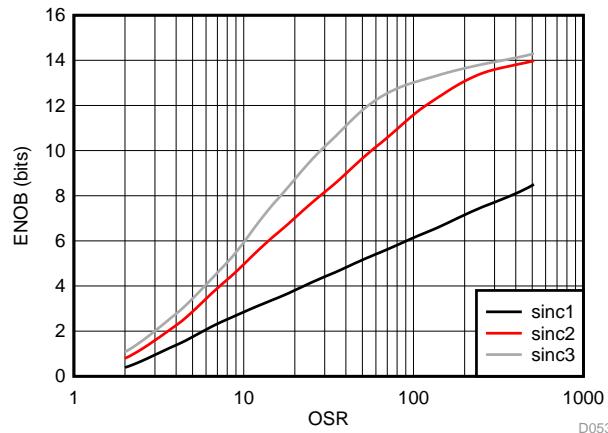
Figure 15. Measured Effective Number of Bits versus Oversampling Ratio

The relationship between ENOB and SNR is given by Equation 17.

$$ENOB = \frac{SNR - 1.76dB}{6.02dB}$$

<div align="right">(17)</div>

From Figure 15 and Equation 17 one can deduce the minimum OSR needed to achieve the required performance. Specifically, from the graph shows that a Sinc2 filter with OSR greater than 200 will yield SNRs higher than the required 78 dB stipulated in Section 1. Similarly, a Sinc 3 filter with OSR greater than 110 will yield SNRs above the design requirement.

In order to find an upper limit to the possible values of OSR, divide the clock frequency of the AMC1304M25 by the minimum required sampling rate stipulated in Section 1. For example, if the clock frequency of the AMC1304M25 is set to 20 MHz, the maximum OSR that can be used is 285.

3.5 Microcontroller

The microcontroller selected for this design is the TMS320F28377D because it has two integrated filter modules that allow the user to choose between Sinc1, Sinc2, Sinc3 and Sincfast filters. The filter modules in the TMS320F28377D are known as the Sigma-Delta Filter Modules (SDFM1, SDFM2). Each sigma-delta filter module supports four channels that can be connected to individual delta-sigma modulators allowing the user to monitor up to eight signals consecutively. As shown in Figure 16, each filter channel has two digital signal processing paths: 1) a data path, and 2) a comparator path.
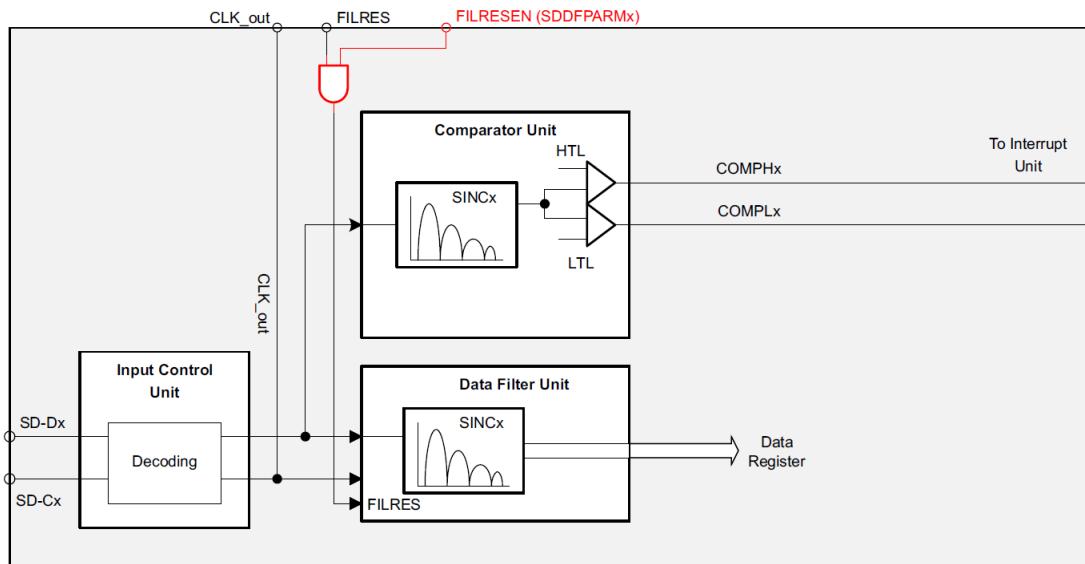
Figure 16. Block Diagram of Each SDFM channel in the TMS320F28377D

The data path in each channel of the sigma-delta filter modules has a configurable OSR from 1 to 256 and the type of filter can be selected as Sinc1, Sinc2, Sinc3, or Sincfast .

The comparator path has the same filter type options as the data path and its OSR can be configured from 1 to 32. Two threshold levels can be selected fo the comparator path such that interrupt flags can be triggered when the comparator unit result exceed either threshold level. This feature is used in order to generate an over-current or short circuit warning signal in this design.

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3.6   Power Management

The power supply stipulated in Section 1 is 5 V; however, 3.3 V are needed to supply power for the controller side of the AMC1304M25, and the V_{DDIO} pins of the TMS320F28377D.

As shown in Figure 11, the TPS79533 low-dropout, linear voltage regulator provides the required power for the controller side of the system.

On the high side of the system, the user has two options. Before delving into them it is important to note a detail on Figure 11: for the high-side of the AMC1304, there is no linear voltage regulator depicted in the system. This is because the AMC1304M25 has an integrated low-dropout, linear voltage regulator that allows the user to supply an unregulated voltage up to 18 V.

This section covers the option of supplying the high side of the AMC1304 with the filtered signal coming from the isolated side of a transformer and Section 8 explains an alternative option.

Figure 17 shows the schematic for the isolated power supply implemented in the design.
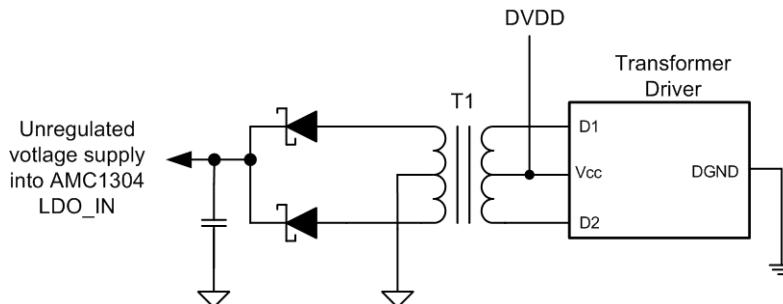
Figure 17. Isolated Power Supply for High Side of AMC1304

Note that the filtered signal on the isolated side of T1 is generated from the power supplied to the controller side of the AMC1304 (DVDD). The transformer driver and T1 form a push-pull dc-to-dc converter where the controller-side winding of T1 is driven and the signal on the high-side is rectified and filtered.

The design of the isolated, unregulated power source to the AMC1304 LDO input closely follows the TIPD121 Design Reference Guide, *0-5 A, Single-Supply, 2 kV Isolated Current Sensing Solution (SLAU521)*.

The SN6501 transformer driver is used because it is designed for low-power, push-pull converters with input voltages in the range of 3 V to 5.5 V; such voltage range fits well within the AMC1304 controller-side supply range. Two important components in the dc-dc converter are the isolation transformer and the rectifier diode.

3.6.1   Transformer Selection

To prevent the isolation transformer from saturating, its volt-seconds (V-t) product must be greater than the maximum volt-seconds product applied by the SN6501. The maximum voltage delivered by the SN6501 is the nominal converter input plus a 10% margin. The maximum time this voltage is applied to the primary is half the period of the lowest frequency at the specified input voltage. The minimum switching frequency of the SN6501 at 5-V operation is 300 kHz. Therefore, the transformer minimum V-t product under these conditions, as determined by equations (1) and (2) in the SN6501 data sheet data sheet, is 9.1 Vµs. The specified V-t product of the isolation transformer selected (DA2304) is well above this 9.1-Vµs requirement.

When searching for a suitable transformer, the minimum turns ratio required must be determined; such a ratio allows the push-pull converter to operate over the specified current and temperature range. The minimum turns ratio required can be expressed through the ratio of secondary to primary voltage multiplied by a correction factor that takes into account the transformer typical efficiency. Equations (3) through (8) in the SN6501 data sheet show the specific requirements for determining the minimum turns ratio for a given application. The DA2304 has a 1:2.2 turns ratio; such a ratio produces an unregulated, open-circuit voltage output well within the AMC1304 low-dropout regulator input range.

3.6.2 Rectifier Diode Selection

The chosen rectifier diode must possess low forward voltage to provide as much voltage to the converter output as possible. When used in high-frequency switching applications, the rectifier must also possess a short recovery time. Schottky diodes meet both of these requirements. The MBR0520L with a typical forward voltage of approximately 100 mV at 8-mA forward current is used in this low-voltage design. Figure 18 illustrates the forward voltage versus forward current characteristics of the MBR0520L diode.
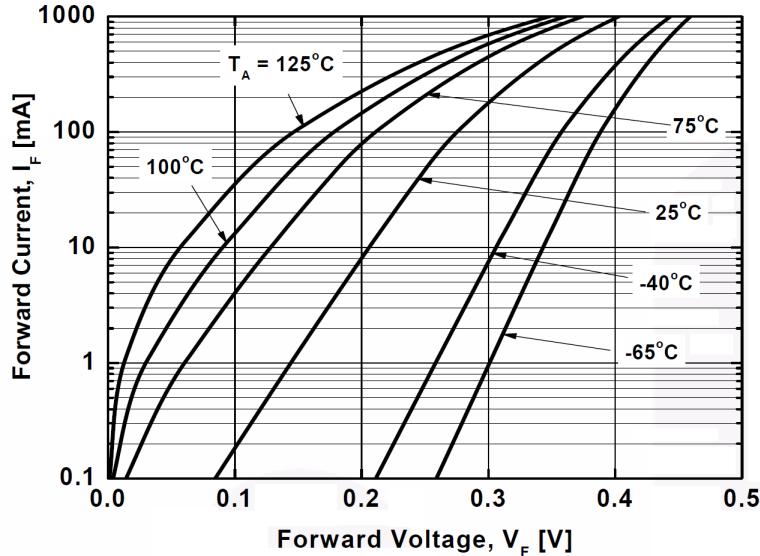
Figure 18. Forward Voltage of the Rectifier Diode

4   Simulation and Error Calculation

Input Passive Filter Simulation

The TINA-TI™ schematic shown in Figure 19 includes the passive final component values obtained in the design process.
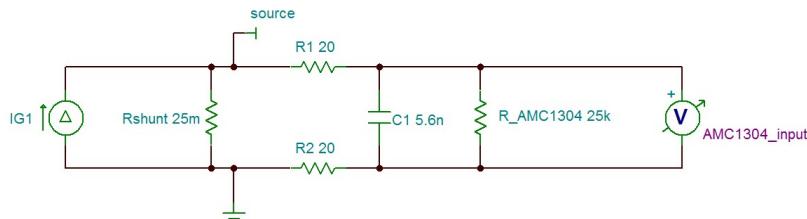
Figure 19. TINA-TI™ Schematic - Input Passive Filter

Figure 20 shows the simulation results for a step input current of 12 A that resembles an over-current event. This simulation allows to observe the expected delay time in the input passive filter from the time when the over-current event starts (0 s) to the time when the input to the AMC1304 reaches 90 percent of the final expected value. Note that R_AMC1304 is included as means to simulate the AMC1304M25 input impedance.
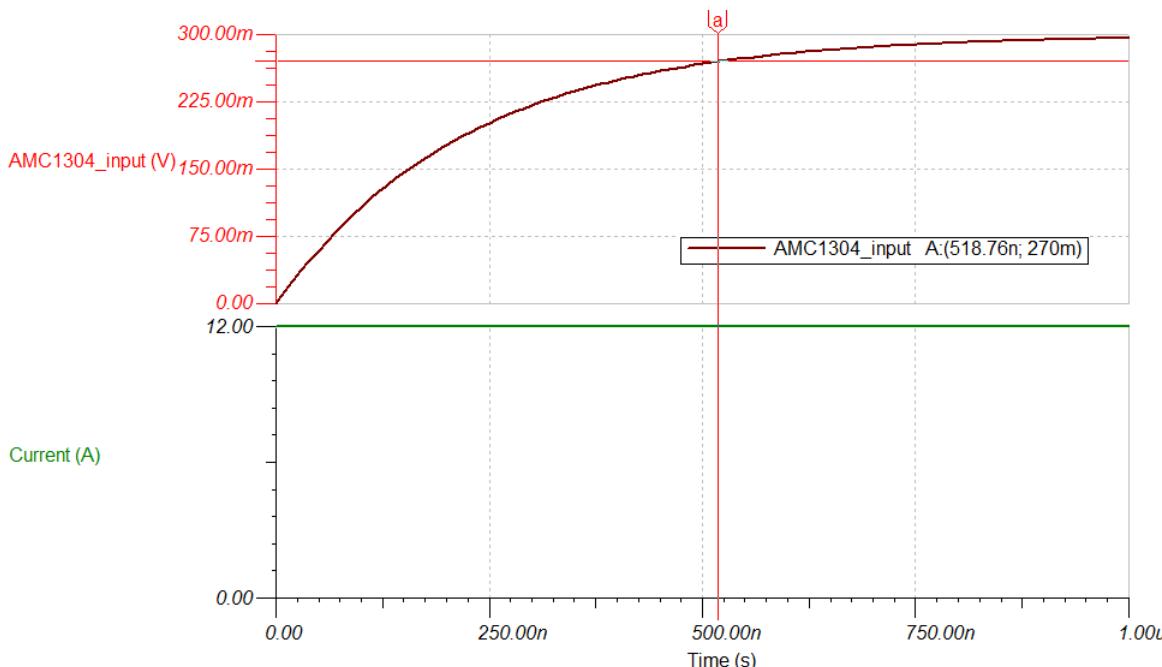
Figure 20. TINA-TI™ Simulation Result - Step Input to Passive Filter

The simulated 518.76 ns obtained in simulation is in line with the expected theoretical calculation in Equation 18.

$$t = -RC \ln(1 - 0.9) = -(40\Omega)(5.6\text{nF}) \ln(1 - 0.9) = 515.8\text{ns}$$

(18)

Figure 21 shows the ac sweep performed in TINA-TI™.
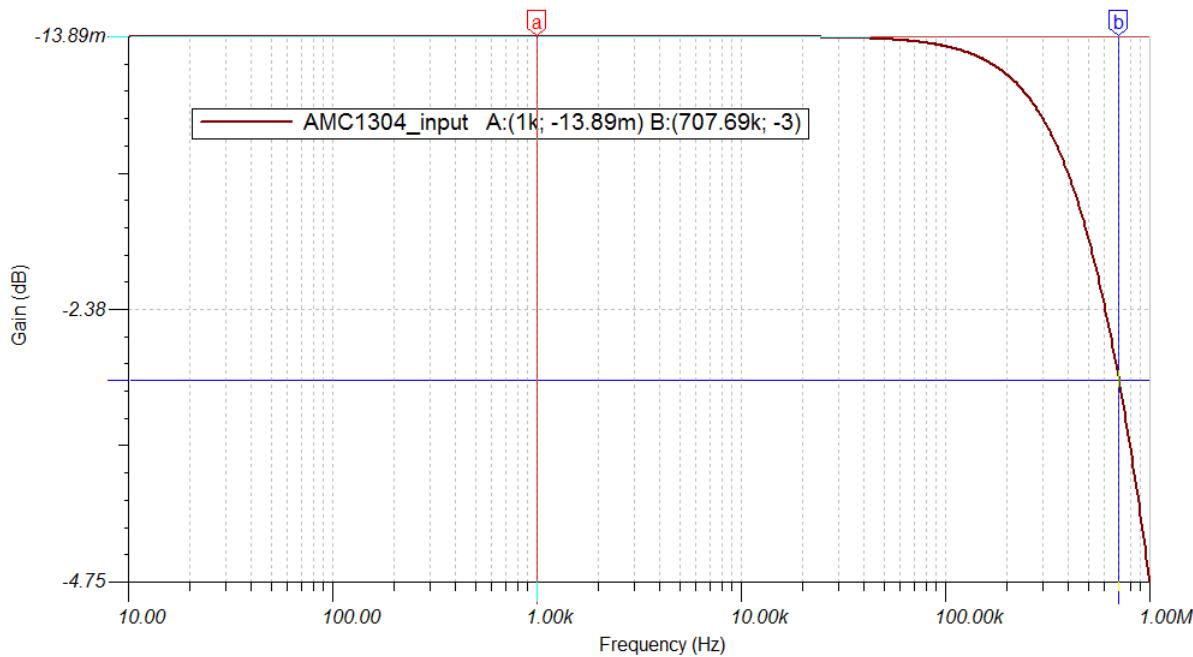
Figure 21. TINA-TI™ Simulation Result - AC Sweep

4.1 *System Error Budget*

There are four main contributors to the measurement error associated with the AMC1304: a) gain error, b) offset, c) integral non-linearity and d) common mode rejection ratio. The fifth contributor to measurement errors is the shunt resistor tolerance.

In order to account for all measurement errors the first step will be to express all of them in parts per million (ppm).

4.1.1 AMC1304M25 Gain Error

The AMC1304M25 has a typical gain error of 0.02 percent with respect to the full linear scale of the device (specified as - 250 mV to + 250 mV). The equivalent gain error expressed in ppm is:

$$G_{err\_typ\_ppm} = (0.02)(10^4) = 200 ppm$$

(19)

4.1.2 AMC1304M25 Offset Error

The AMC1304M25 has a typical offset error of 40 μV. The equivalent offset error expressed in ppm with respect to the full linear scale of the device is:

$$V_{os\_typ\_ppm} = (40\mu V)\frac{10^6}{0.5V} = 80 ppm$$

(20)

4.1.3 AMC1304M25 Integral Non-linearity Error

The AMC1304M25 has a typical integral non-linearity (INL) of 1.5 least significant bits (LSB) with respect to a resolution of 16 bits. The equivalent INL error expressed in ppm with respect to the full linear scale of the device is:

$$INL_{err\_typ\_ppm} = \frac{10^6 INL}{2^{Resolution}} = \frac{10^6(1.5)}{2^{16}} = 22.9 ppm$$

(21)

4.1.4 AMC1304M25 Common-mode Rejection Ratio Error

The AMC1304M25 has a typical common-mode rejection ratio (CMRR) of 76 dB. The maximum common-mode signal is 0.125 V which is equivalent to one-half the maximum differential signal. The equivalent common-mode rejection ratio error expressed in ppm with respect to the full linear scale of the device is:

$$CMRR_{typ\_ppm} = \frac{10^6 V_{CM}}{FSR\left(10^{\frac{CMRR}{20}}\right)} = \frac{10^6(0.125)}{0.5\left(10^{\frac{76}{20}}\right)} = 39.6 ppm$$

(22)

Combined AMC1304 Error

Combining the results obtained in Equation 19, Equation 20, Equation 21, and Equation 22 yields:

$$E_{AMC\_typ\_ppm} = \sqrt{G_{err\_typ\_ppm}^2 + V_{os\_typ\_ppm}^2 + INL_{err\_typ\_ppm}^2 + CMRR_{typ\_ppm}^2} = 220.2 ppm$$

(23)

4.1.5 Shunt Resistor Tolerance

The contribution of the shunt resistance tolerance to the system error is:

$$E_{SHUNT\_tol\_max\_ppm} = (0.5)10^4 = 5000 ppm$$

(24)

4.1.6 Total System Error

The total system error is:

$$
E_{TOT\_ppm} = \sqrt{E_{AMC\_typ\_ppm}{}^2 + E_{SHUNT\_tol\_max\_ppm}{}^2} = 5005\,ppm
$$

(25)

5 PCB Design

This reference design consists of three printed circuit boards (PCB). One PCB contains the AMC1304M25, passive filter and power management circuitry to supply the high side of the delta sigma modulator. A second PCB contains the TMS320F2837xD Dual-Core Delfino Microcontroller and support circuitry to enable isolated JTAG emulation, USB and isolated UART/SCI connectivity among others. The third PCB is a docking station with additional jumper headers to allow for the configuration of the AMC1304M25 clock signals and raw modulator bit-stream acquisition.

All the design files (schematic, layout and BOM) for all three boards are available in the TIPD165 Design File available at ti.com

The PCB schematic and bill of materials for the AMC1304M25 board and the docking station can be found in Section 11.

5.1 AMC1304 PCB Layout

The most important considerations in designing the PCB layout for this system are discussed below:

- The decoupling capacitors C1, C2, C5 and C6 are located as close as possible to the IC terminals.
- The traces for the power supply connections to DVDD and LDO_IN are 20 mils wide to lower the series resistance of those connections.
- As indicated in the AMC1304M25 datasheet, the spacing between the high side ground plane and controller side ground plane is longer than 8.1mm in order to maintain the recommended clearance for the AMC1304 isolation rating.

The AMC1304 PCB layout is shown in Section 11.
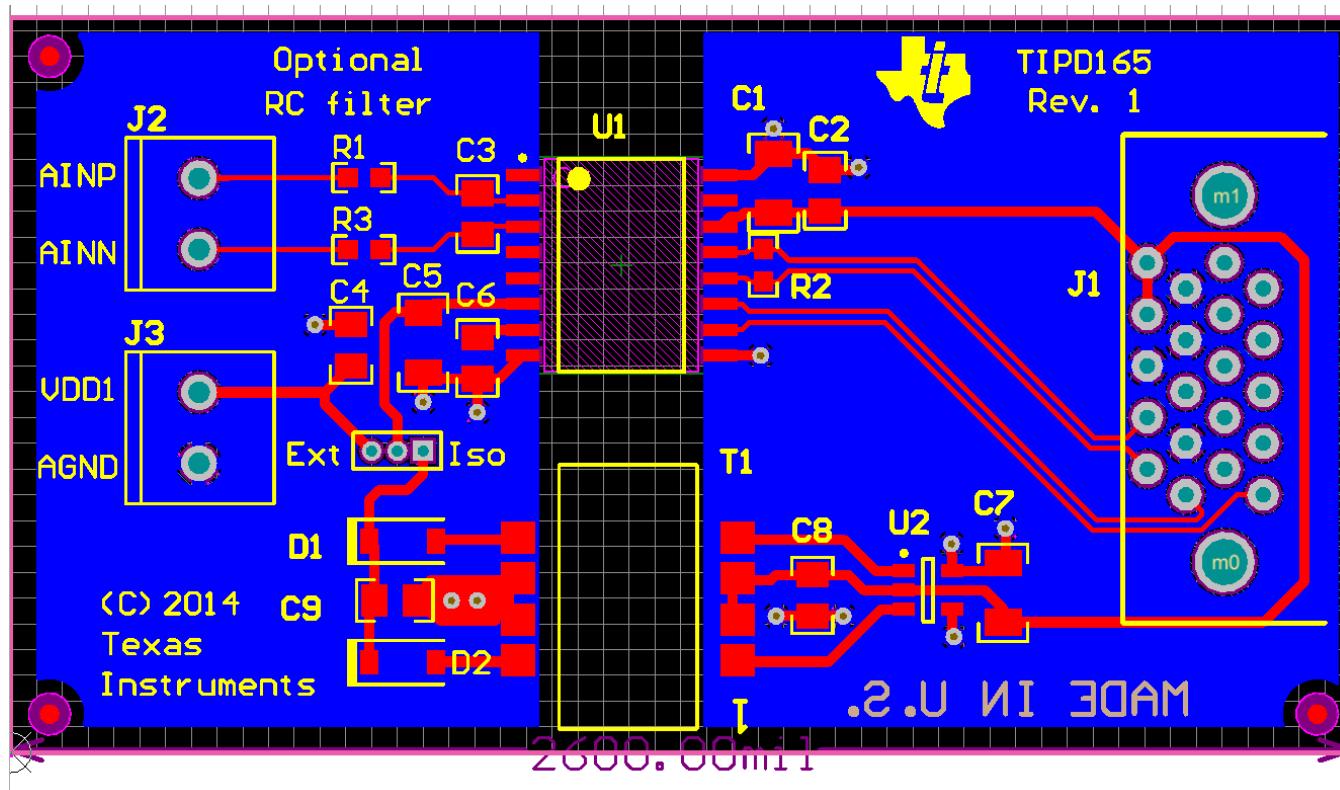
Figure 22. AMC1304 PCB Layout

Note that the 25 mΩ current shunt is not included in the AMC1304M25 board. However, the signal corresponding to the voltage drop across the shunt should be connected to the terminals in J2 as shown in Figure 3.

There are two options to power the high side of the AMC1304M25. The default option to supply the AMC1304 LDO_IN from T1 by shorting the jumper pin labeled "ISO" in Figure 22 to the center of jumper pin (as shown in Figure 23) so that the common node of D1 and D2 are connected to the LDO_IN of the AMC1304.
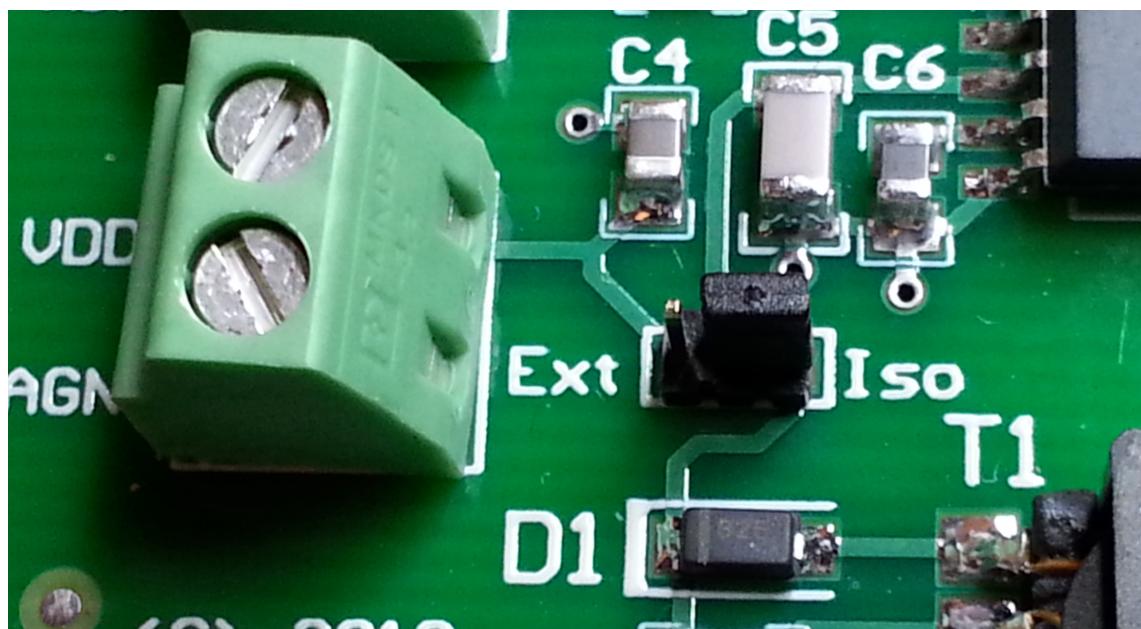
Figure 23. High Side of AMC1304 Supplied from T1

5.2 TMS320F28377D Control Card PCB Layout

The TMS320F28377D Control Card PCB layout is shown in Figure 24.
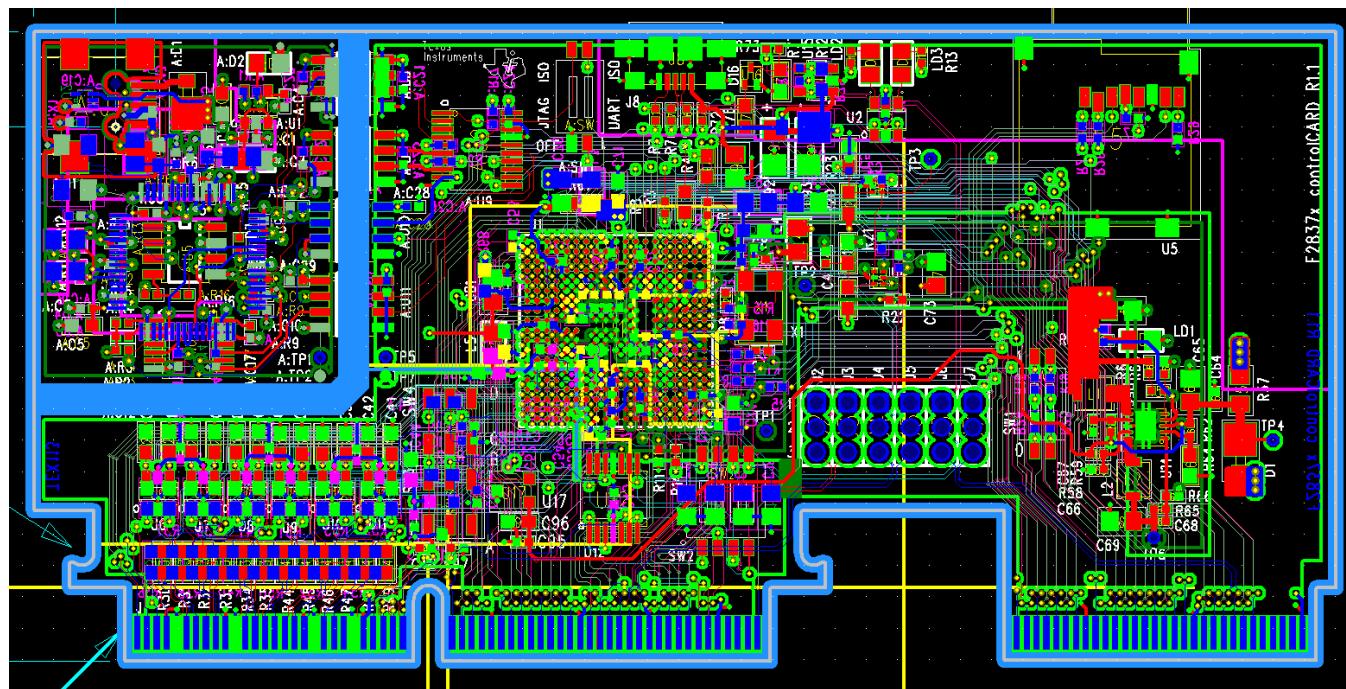
Figure 24. TMS320F28377D Control Card PCB Layout

The PCB schematic and bill of materials for the TMS320F28377D control card can be also found at www.ti.com/tool/tmdxcncd28377d.

5.3 Docking Station PCB Layout

The Docking Station PCB layout is shown in Figure 25.
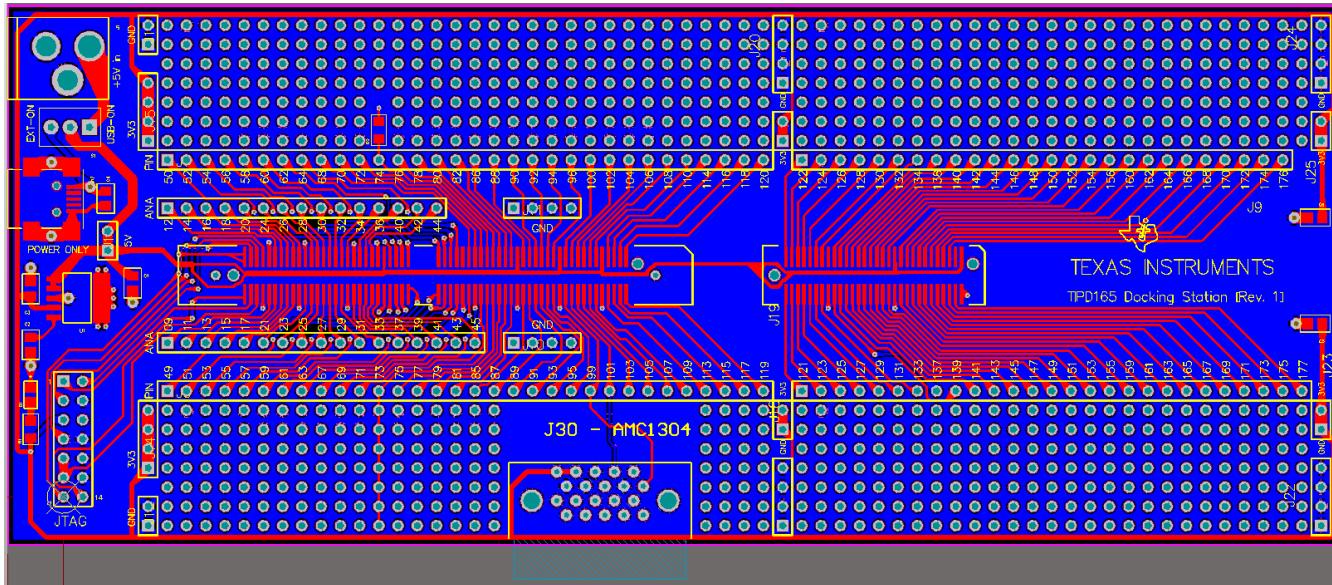
Figure 25. Docking Station PCB Layout

Figure 26 shows the default configuration of the docking station. The configuration is as follows:

- Connect pin 73 (clock generated by TMS320F28377D) to pin 101 (AMC1304M25 clock input).
- Connect pin 73 (clock generated by TMS320F28377D) to pin 79 (clock input for raw delta-sigma modulator capture as shown in Section 7.3).
- Connect pin 99 (AMC1304M25 data output) to pin 75 (data input to TMS320F28377D Sigma-Delta filter module).
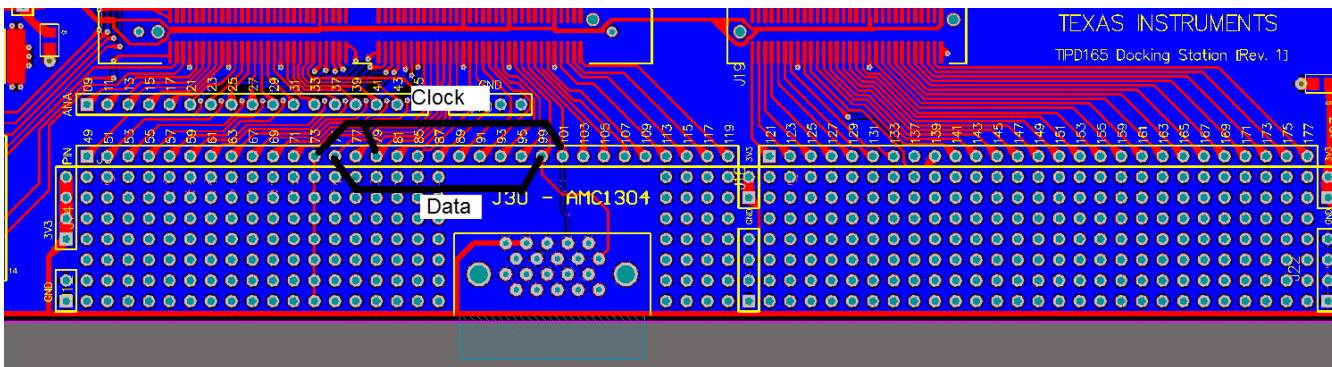
Figure 26. Docking Station - Default Configuration

6   Verification and Measured Performance

The measurement results for verification of this TI Precision Design are listed in this section.

6.1   Transfer Function

Figure 27 depicts the transfer function of the system with the voltage drop across the current shunt as the input variable and the codewords from the TMS320F28377D sigma-delta filter module as the output variable. Note that the output codewords can be read from the right hand side vertical axis and the equivalent calculated input-referred voltage to the system can be read on the left had side vertical axis of Figure 27. The transfer function was obtained with the TMS320F28377D generating a 20 MHz clock for the AMC1304M25, with Sinc3 selected and OSR of 256.
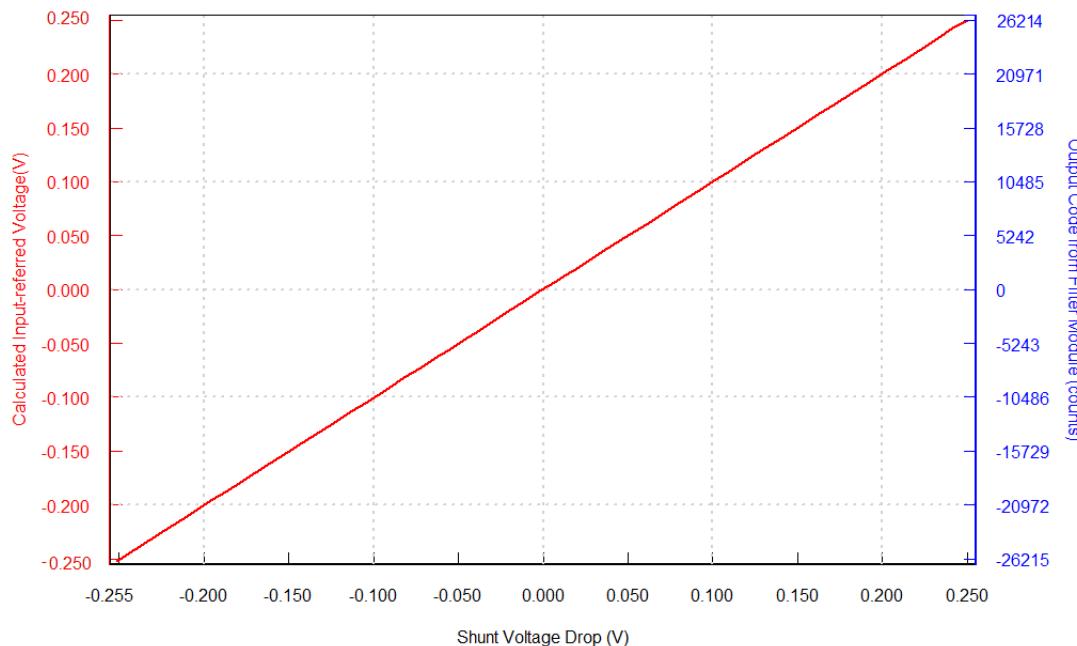
Figure 27. Transfer Function of the System

As described in the Sigma Delta Filter Module (SDFM) chapter of the TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual, the peak data values obtained from the TMS320F28377D sigma-delta filter module depend on the type of filter selected (Sinc1, Sinc2, Sinc3 or Sincfast), the oversampling ratio (OSR) used and the chosen data filter output representation.

The software that is provided with this reference design uses a 16-bit data filter output representation. Note that the software aligns the filtered data such that the -32768 codeword corresponds to the negative analog input voltage that would cause clipping (denoted by $-V_{Clipping}$ and with a value of -312.5 mV), whereas the 32767 codeword corresponds to the positive analog input voltage that would cause clipping (denoted by $V_{Clipping}$ and with a value of 312.5 mV).

Equation 26 shows how to calculate the input voltage to the AMC1304M25 for a given codeword read from the output data register of the TMS320F28377D sigma-delta filter module.

$$V_{IN\_calc} = \frac{\left(V_{Clipping}\right)(Codeword)}{\left|Codeword_{peak}\right|}$$

(26)

From Equation 26:

- V_{IN_calc} is the calculated input voltage to the AMC1304M25.
- $V_{Clipping}$ is the maximum differential voltage input (312.5 mV) as indicated in the AMC1304M25 datasheet and in Section 3.3.
- Codeword is the binary sequence read from the output data register of the TMS320F28377D sigma-delta filter module expressed as a decimal number.

- Codeword$_{peak}$is the extrema of the range of codewords put out by the reference design software. Since the software uses a 16-bit data filter output representation, the absolute value of Codeword$_{peak}$ is 32768.

For example, Equation 27 shows the calculated input voltage to the AMC1304M25 for a codeword of 10485.

$$V_{IN\_calc} = \frac{(0.3125\ V)10,485}{\left|-32,768\right|} = 0.099993\ V$$

(27)

6.2 System Error

Figure 28 shows the measured uncalibrated system error based on the transfer function shown in Figure 27. This error is obtained by subtracting the actual input voltage from the calculated input voltage and as such, it does not include the shunt tolerance.

Figure 27 takes into account only the error based on the difference between the voltage input signal (measured with a 6 1/2 digit multimeter) and the input-referred voltage calculated from the output codewords.

For convenience, the error can be read in µV on the left hand side vertical axis or percentage of FSR and parts per million of FSR (ppm) in the right hand side.
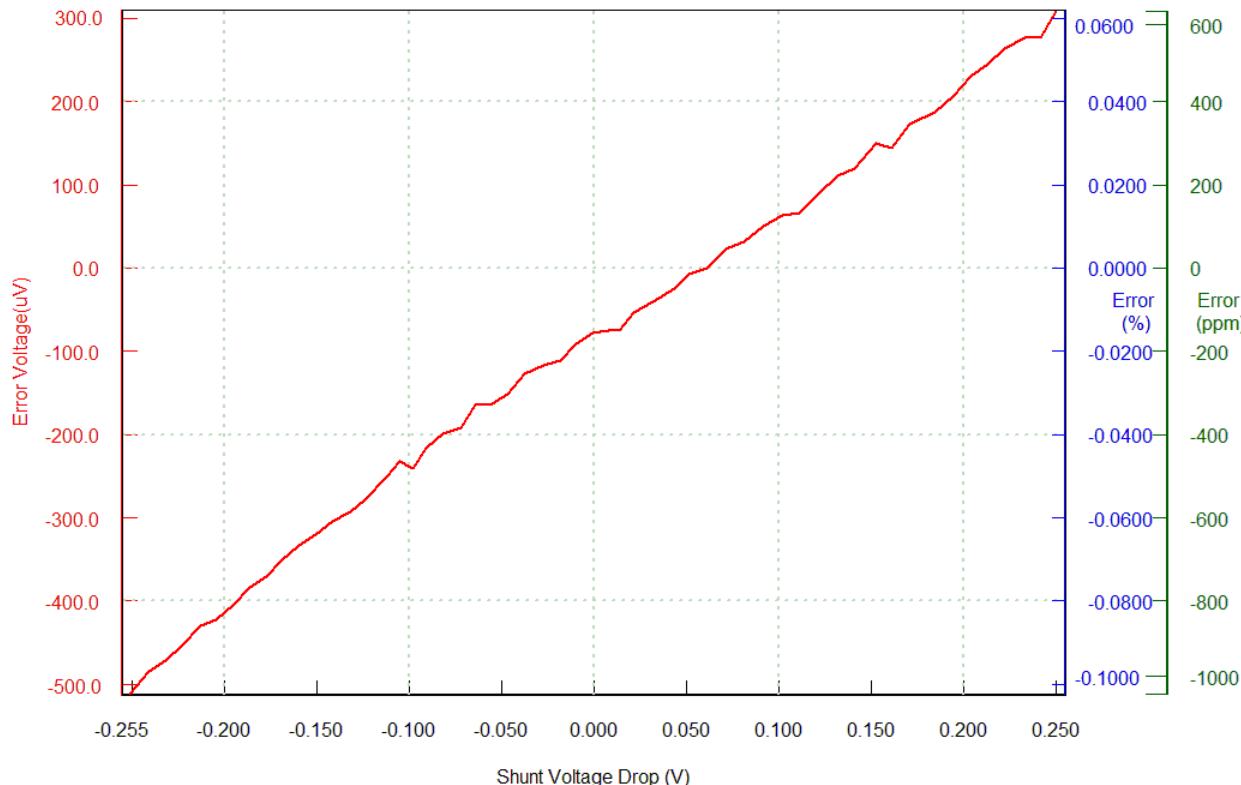
Figure 28. Measured Uncalibrated System Error

6.3   AC Measurement

The system performance was measured for a 1 kHz, full scale input. Figure 29 shows the time domain and frequency domain plots of the acquired signal using a 20 MHz clock for the AMC1304M25 and a Sinc3 filter with OSR of 256.
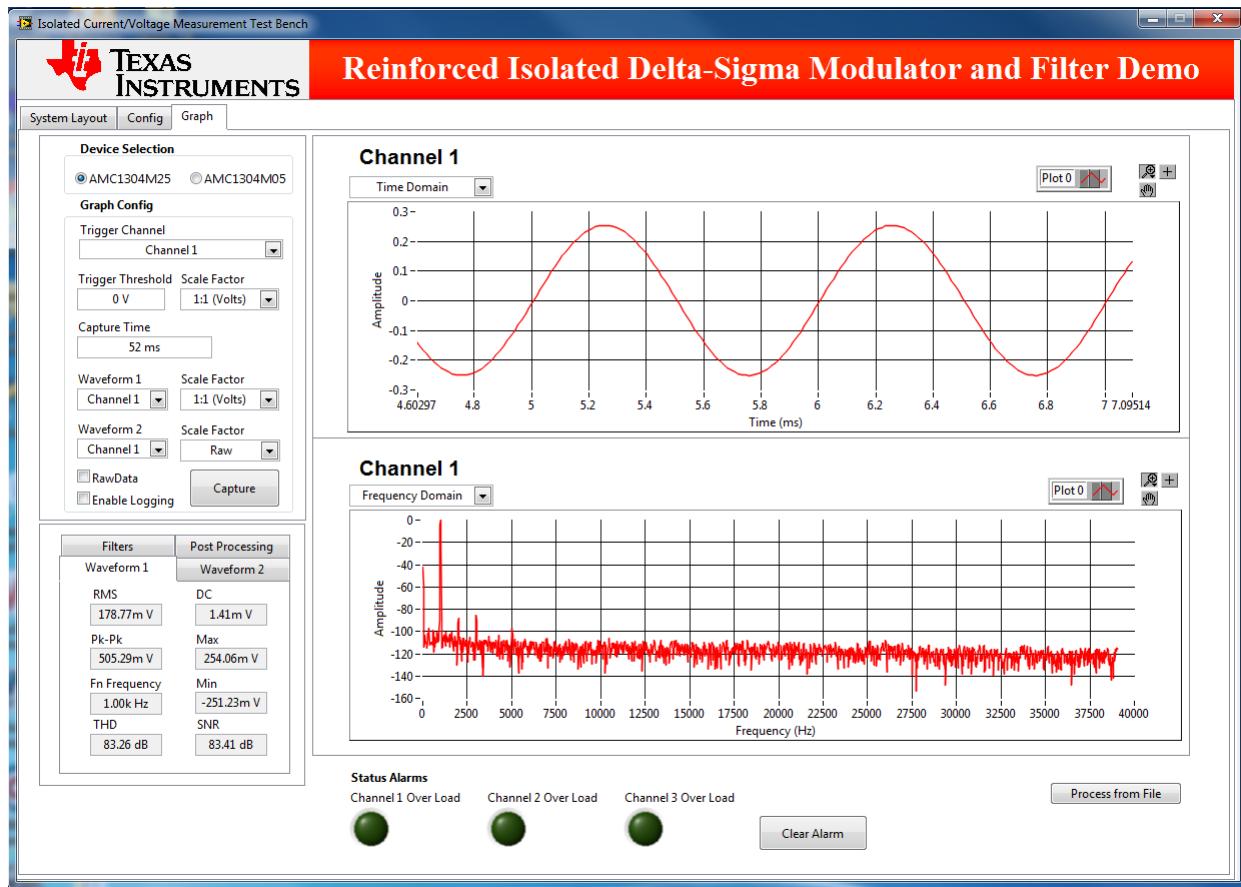
Figure 29. Measured AC Performance

6.3.1 Bandwidth Measurement

Figure 30 shows the signal acquired for a 20.4 kHz, full scale input. Note that both the maximum and minimum measured values are 3 dB below those shown in Figure 29.
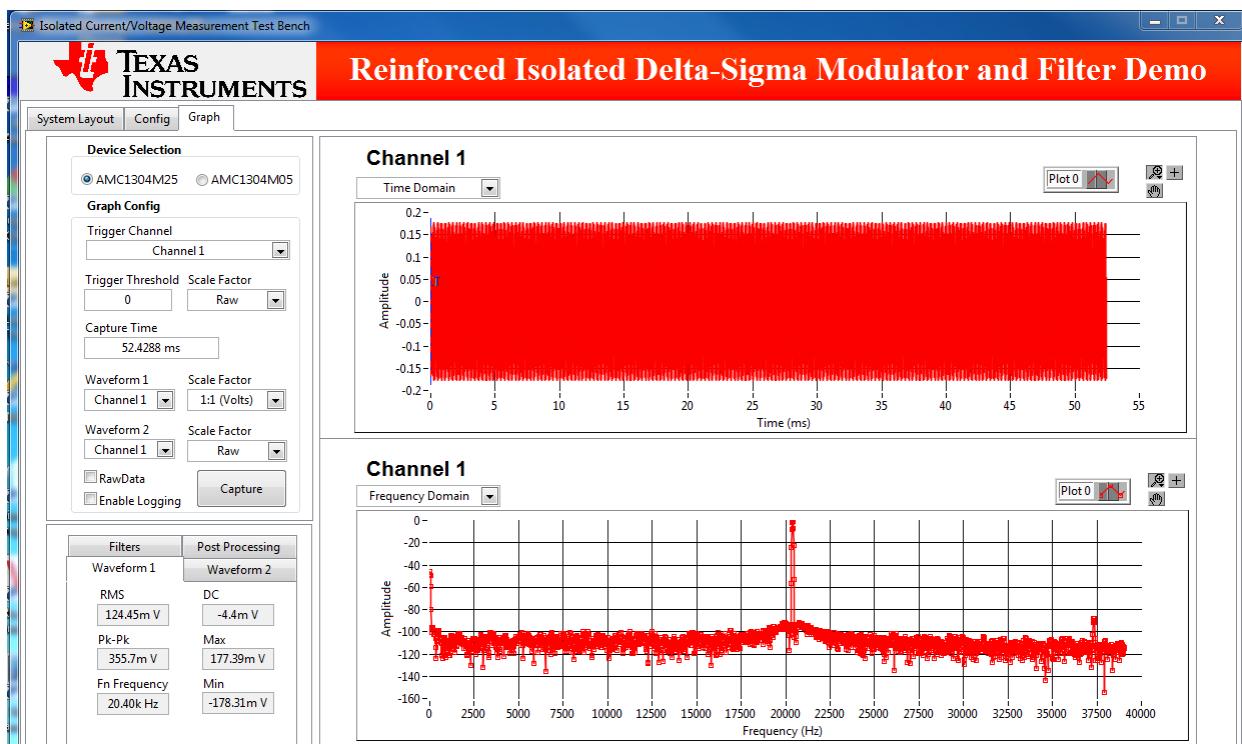
Figure 30. Measured Bandwidth

6.4 Warning Signal Latency

There are two means of measuring the system latency when a warning signal is issued in response to an over-current or short circuit event: a) through a pair of general purpose input/output (GPIO) pins of the TMS320F28377D, and b) through the Graph page of the graphical user interface (GUI).

6.4.1 Warning Signal Issued on GPIO

The firmware provided in this reference design uses GPIO-00 and GPIO-01 of the TMS320F28377D to issue warning signals when the comparator module thresholds of channel 1 are crossed.

The GPIO-00 is connected to pin 49 of the docking station and GPIO-01 is connected to pin 51 of the docking station. To properly utilize the GPIO warning signals, the user must select channel 1 as the triggering channel for acquisition as shown in Figure 43.

As explained in the Sigma Delta Filter Module (SDFM) chapter of the TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual, the comparator filter unit and the data filter unit differ in the way they handle input data. The comparator filter unit translates a low input bit to a '0' and a high input bit to a '1', whereas the data filter unit uses '–1' and '1'. The resulting calculations give only positive values for the output of the comparator filter. The data representation is straight binary.

In order to issue a warning signal when a +12 A over-current event occurs, the high-level threshold of channel 1 is set to 94% as shown in Figure 31. The 94% level is calculated for 90% settling of the input voltage when a 12 A input is applied as shown in Equation 28.
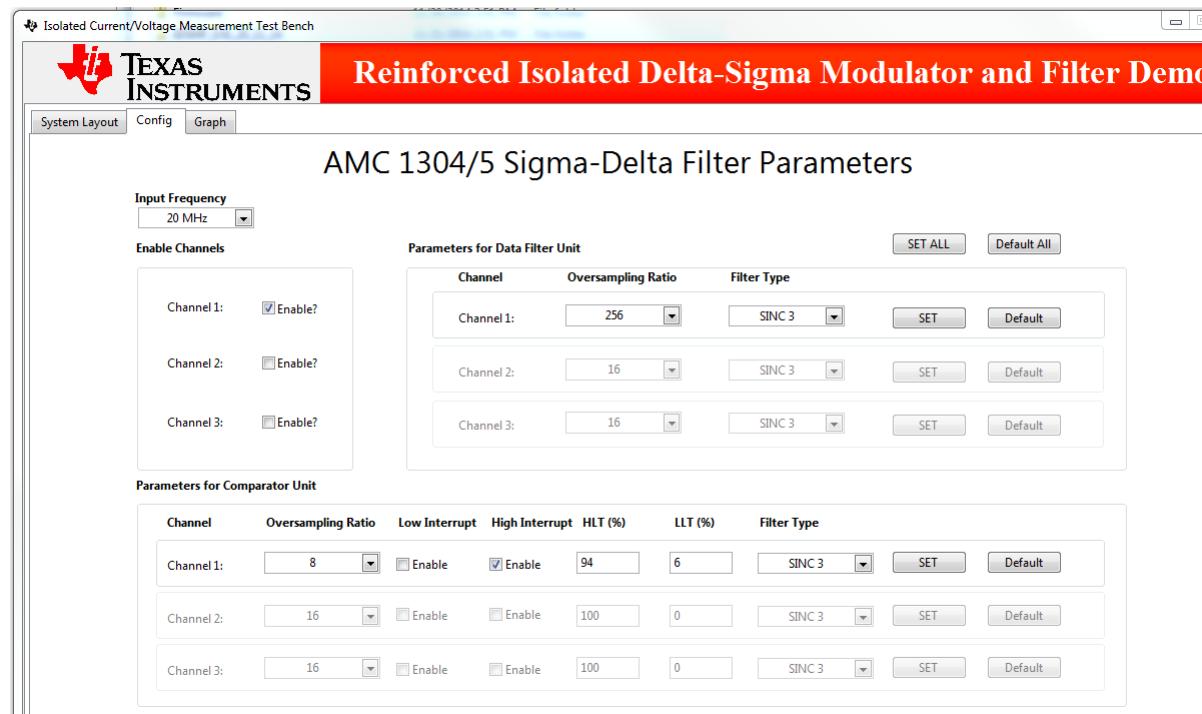
Figure 31. Threshold Settings for Over-current Detection

$$\text{HLT} = \left[0.9(+12\,\text{A})(0.025\,\Omega) - (-0.3125\,\text{V})\right]\frac{100\,\%}{0.3125\,\text{V} - (-0.3125\,\text{V})} = 93.2\%$$

(28)

Similarly, in order to issue a warning signal when a -12 A over-current event occurs, the low-level threshold of channel 1 is set to 6%. As shown in Figure 31. The 6% level is calculated for 90% settling of the input voltage when a –12 A input is applied as shown in Equation 29.

$$\text{LLT} = \left[0.9(-12\,\text{A})(0.025\,\Omega) - (-0.3125\,\text{V})\right]\frac{100\,\%}{0.3125\,\text{V} - (-0.3125\,\text{V})} = 6.8\%$$

(29)

The firmware sets both GPIO-00 and GPIO-01 to logical low (0 V) when the user clicks on the "Capture" button. Both GPIOs transition to logical high (DVDD) when the output of the data path of the sigma delta filter module 1 crosses the acquisition threshold entered by the user. The warning signal is issued in GPIO-00 by resetting the GPIO to logical low (0 V) when (for channel 1) the comparator filter module high-level threshold is crossed. Similarly, GPIO-01 is reset to logical low (0 V) when (for channel 1) the comparator filter module low-level threshold is crossed. Note that there are three thresholds involved: one is for the acquisition of data based on a triggering channel (as shown in Figure 43) and two are for the comparator levels (corresponding to over-current events).

Figure 32 shows the behavior of GPIO-00. Figure 32 shows the input signal to the AMC1304M25 connected to channel 1 (blue trace) and the voltage on GPIO-00 (yellow trace). Channel 1 is set in the GUI to begin acquisition when a 0 V threshold is crossed. The input signal applied to channel 1 (blue signal in Figure 32) begins at –20 mV, then it has a step jump to +70 mV and remains there for about 3.2 ms. The over-current event corresponds to the step jump from 70 mV to 300 mV (note that 300 mV corresponds to 12 A flowing through the shunt).
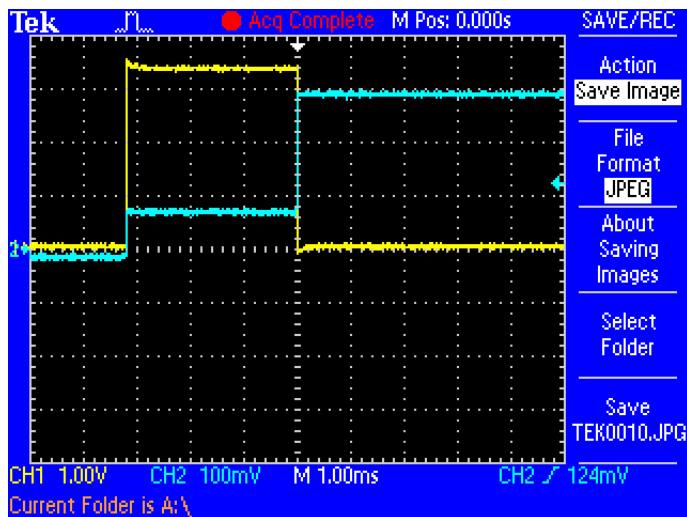
Figure 32. Response of GPIO-00 to Over-current Event

Figure 33 shows a zoomed-in version of Figure 32. Note that there is a time delay of 3.9 µs between the beginning of the over-current event and the time when the warning signal is issued. This time delay is caused by the combination of the 520 ns delay in the analog filter (as shown in Section 3.2 and Input Passive Filter Simulation) plus 1.2 µs delay in the comparator path plus 2.18 µs delay in the interrupt service routine to issue the warning signal by setting the GPIO to a low state.
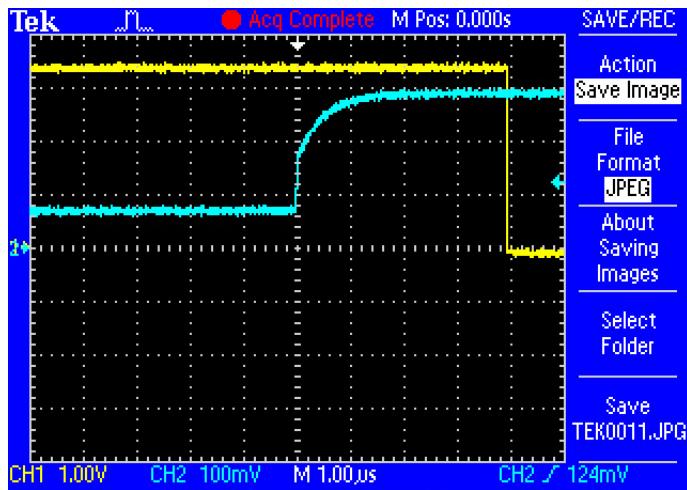
Figure 33. Response of GPIO-00 to Over-current Event - Zoomed In

It is important to mention that the 1.2 µs delay in the comparator path depends directly on the selection of the modulator clock frequency, OSR and type of filter. Equation 30 shows how to calculate the delay caused by the digital filter feeding the comparator.

$$\text{time delay}_{\text{comparator}} = \frac{(\text{OSR})(\text{order})}{F_{\text{CLK}}} = \frac{(8)(3)}{20 \times 10^6} = 1.2\,\mu\text{s}$$

(30)

In Equation 30, the variable *order* refers to the order of the digital filter in the comparator path and the value of 3 is used for a Sinc^3 filter (note that 2 would be used for a Sinc^2 filter and 1 for a Sinc^1 filter). Moreover, note that using a 10 MHz modulator clock would double the time delay.

6.4.2 Time Domain Plot in GUI

The second method to measure the system latency in issuing a warning signal is through the Graph page in the GUI. In the time domain plot, the Graph page draws a vertical line to indicate the point in time where the comparator threshold is crossed. A blue line marked HLT indicates a crossing of the high level threshold and a green line marked LLT indicates a crossing of the low level threshold.

Figure 34 shows the GUI time domain plot of the input signal corresponding to the oscilloscope capture shown in Figure 32 and Figure 33.
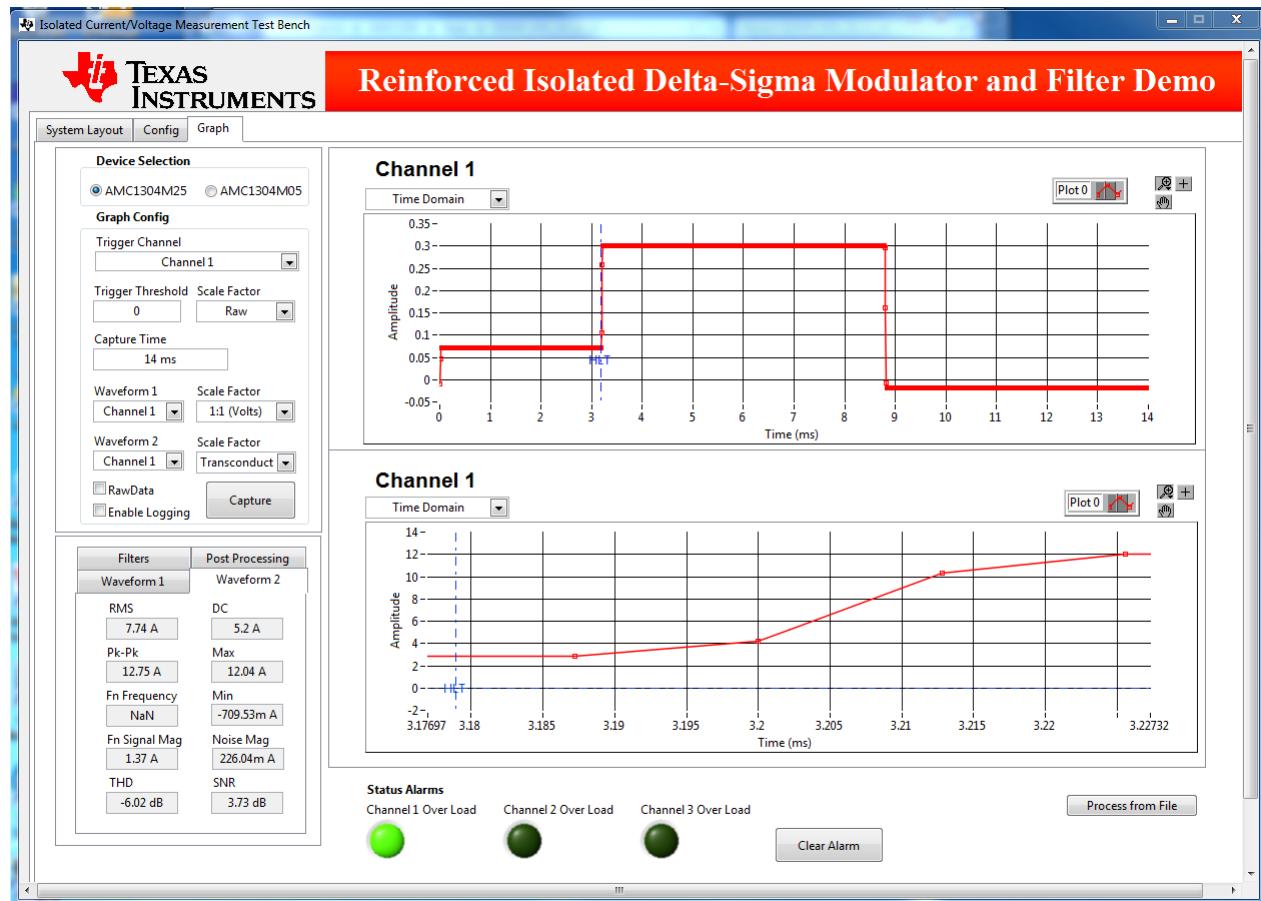
Figure 34. GUI Indicator of Comparator Threshold Crossing

Note that in addition to the vertical marker a green indicator lights up in the Status Alarms section of the Graph page.

The blue vertical line indicating the comparator crossing occurs before the data path samples because the OSR in both channels is different. The delay in the data path is longer than the delay in the comparator path. From Figure 34 one can estimate the location of the input over-current step by subtracting the time corresponding to three data path samples from the time location of the sample closest to a 10.8 A level. Note that 10.8 A corresponds to 90% of the 12 A over-current event and it is the threshold used for the comparator module as shown in Figure 31.

For the case depicted in Figure 34, the three samples figure is used because a Sinc[3] filter takes approximately three full samples in order to settle for a step input. Note that a Sinc[2] filter takes about two samples and a Sinc[1] filter takes only one sample.

The system time delay is calculated as shown in Equation 31.

$$\text{time delay} = 3.179\,\text{ms} - \left[3.2128\,\text{ms} - 3\left(\frac{256}{20\text{x}10^{6}}\right)1000 \right] = 4.6\,\mu\text{s}$$

(31)

The 3.179 ms figure is the time location of the vertical HLT marker and 3.2128 ms figure is the estimated time location of the sample closest to the comparator threshold level.

Note that the time delay measurement performed with an oscilloscope is accurate whereas the calculation performed from the GUI is approximate due to the difference in OSR of the two paths and the discrete nature of the data path sampling times.

7 Graphical User Interface

The associated graphical user interface (GUI) for this design allows the user to experiment with different filter settings and display the input to the system. The GUI is structured into three tabs: System Layout, Config and Graph.

7.1 System Layout

This tab presents a generic block diagram of an isolated, acquisition system. The diagram provides general information on the components used in the design.

Figure 35 shows the System Layout tab.
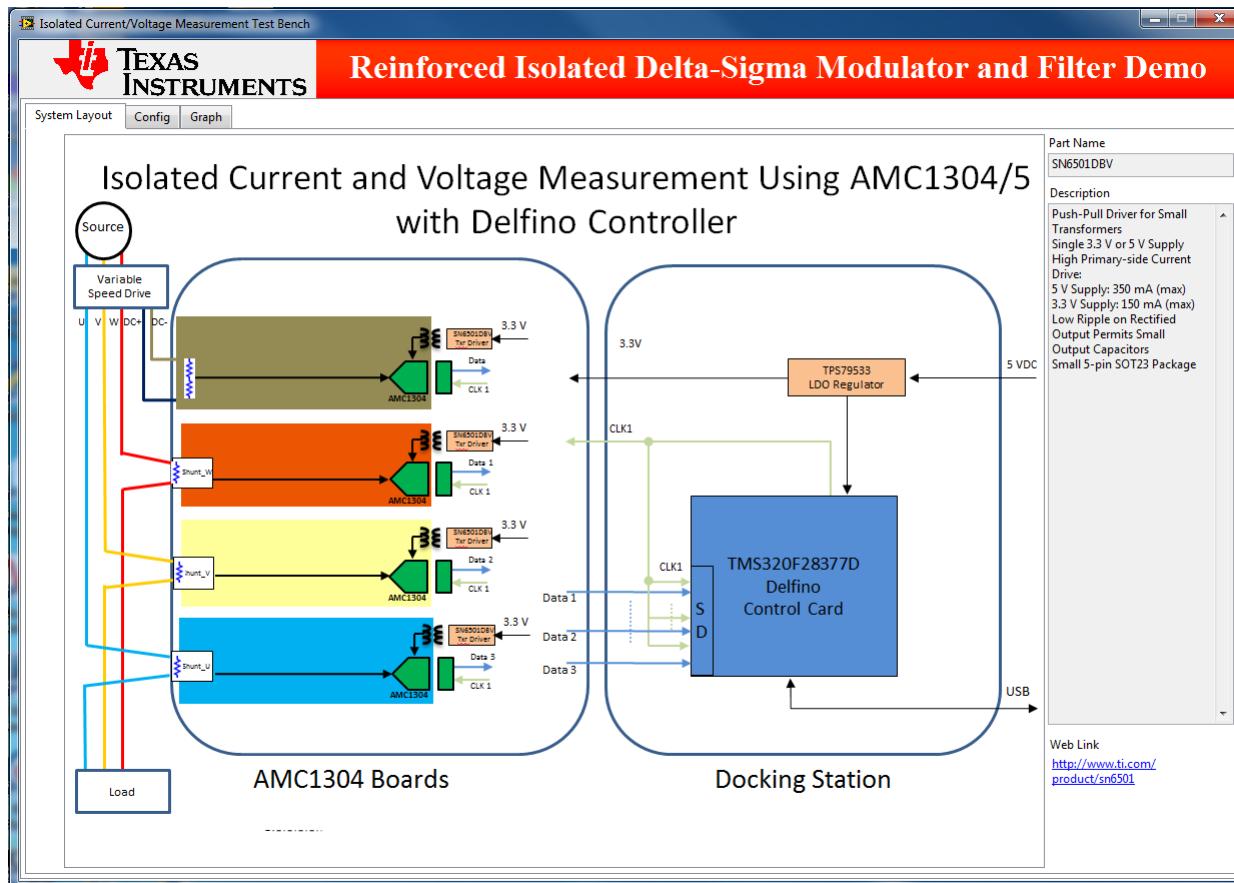
Figure 35. GUI - System Layout Tab

7.2 Config Tab

As shown in Figure 36, the Config tab allows the user to select the frequency generated by the TMS320F28377D microcontroller fed into the AMC1304M25.
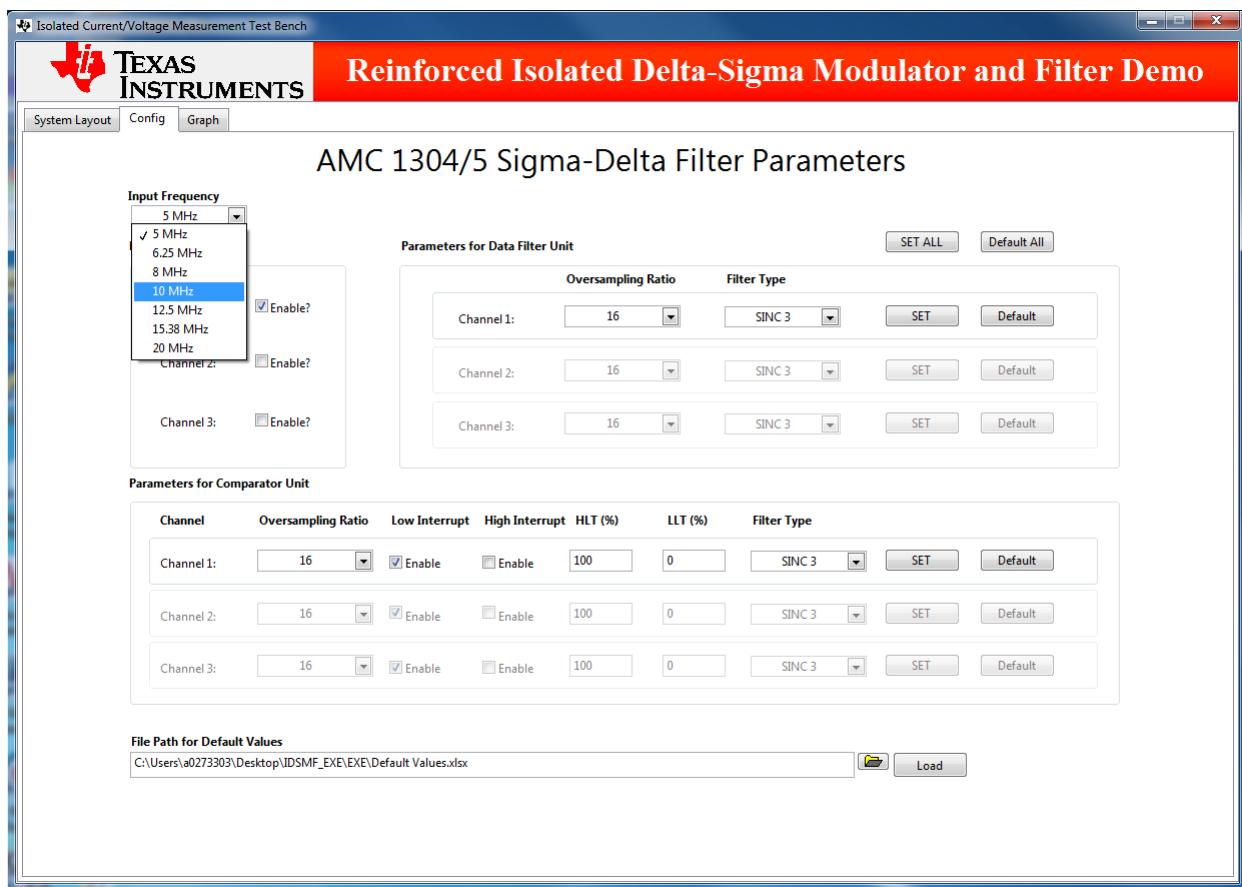
Figure 36. GUI - Frequency Selection - Config Tab
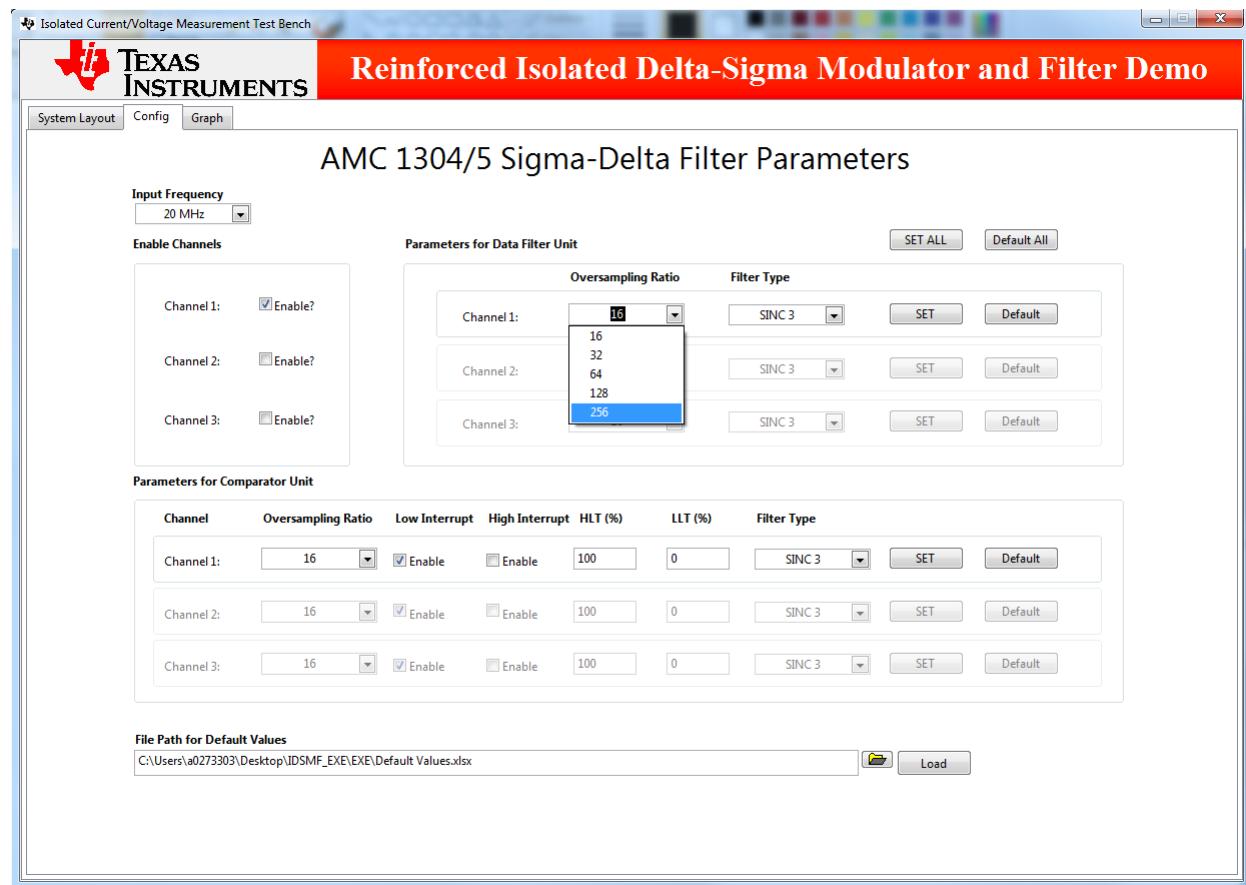
Figure 37. GUI - OSR Selection for Data Filter Unit - Config Tab

Figure 37 shows how to select the desired OSR for the data filter unit of the TMS320F28377D microcontroller. Note also how channels can be enabled/disabled on the left side "Enable Channels" section of the tab.
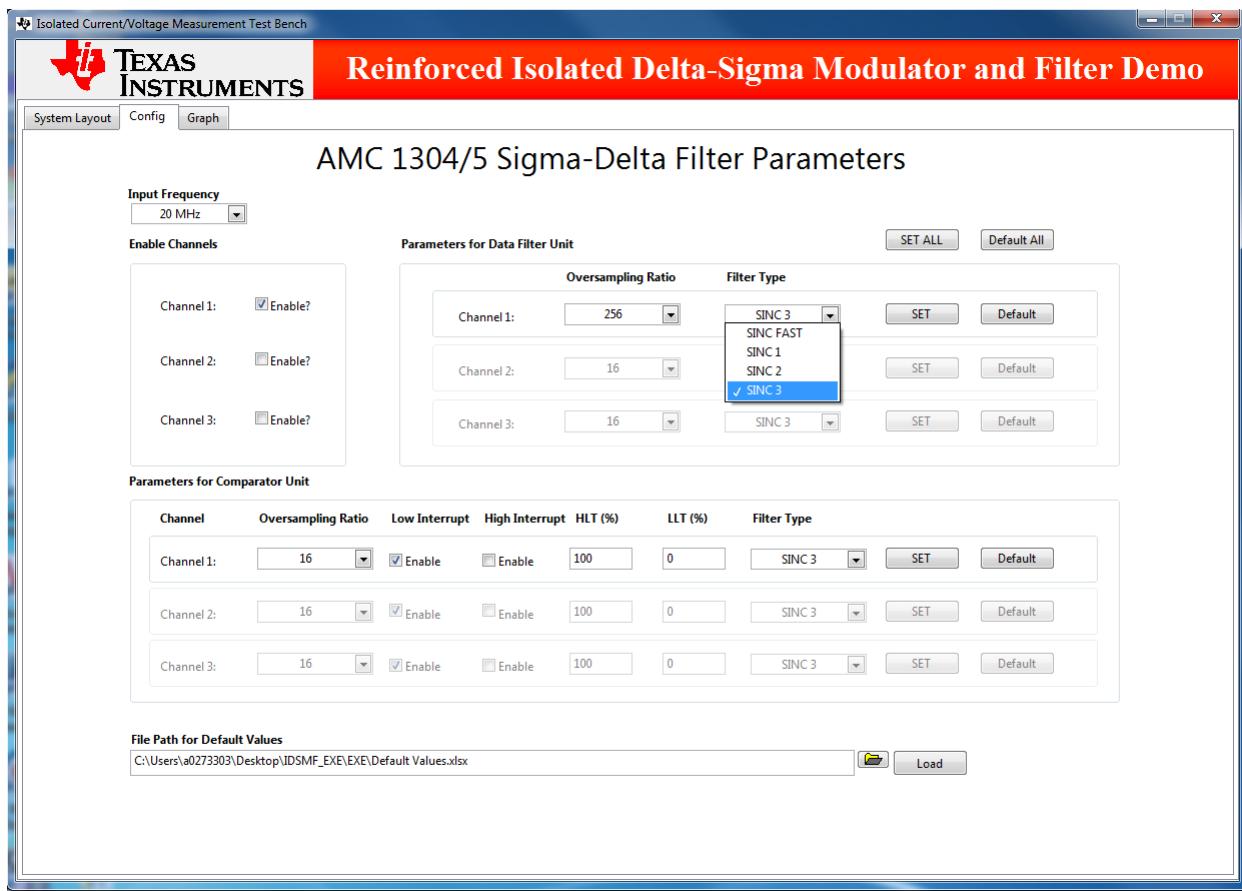
Figure 38. GUI - Data Path Filter Selection - Config Tab

The filter type of the data filter unit can be selected as shown in Figure 38.
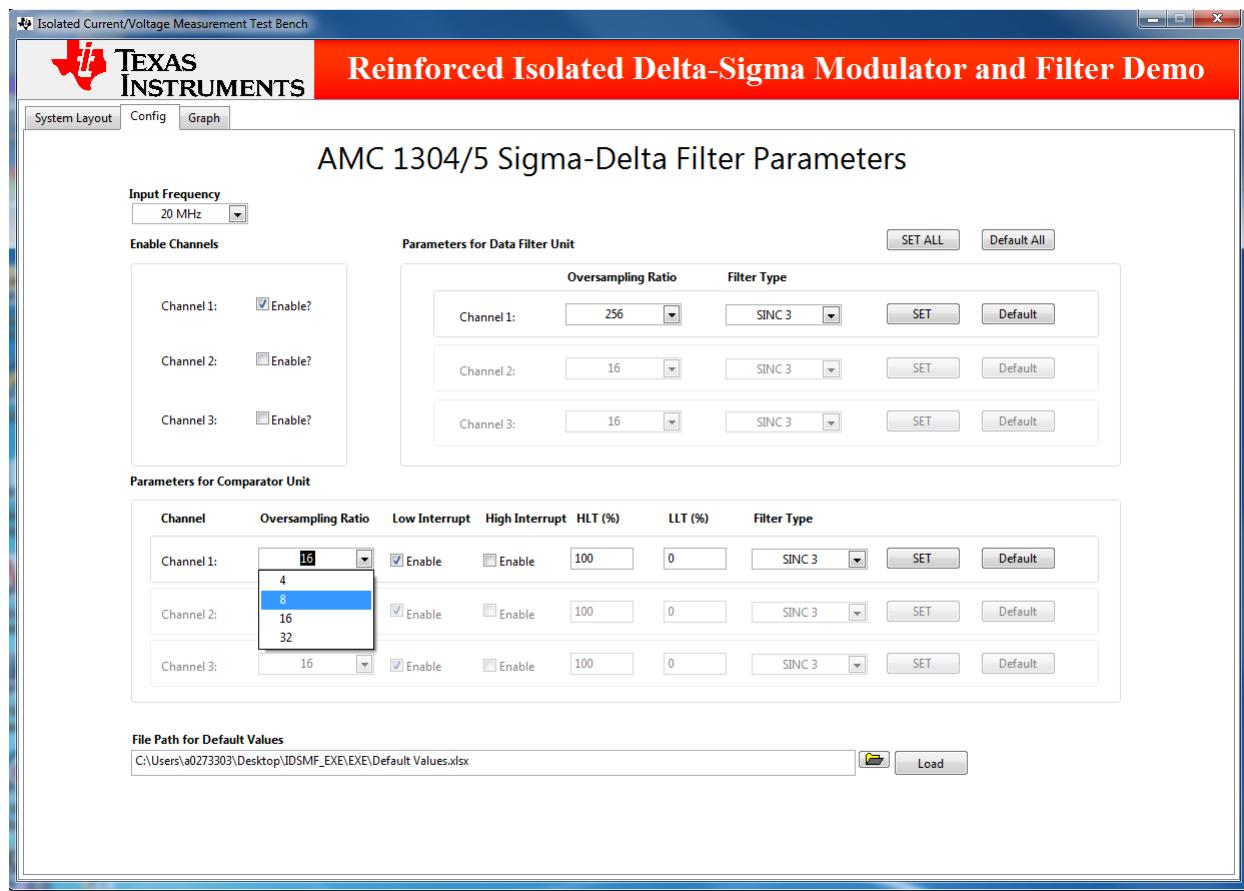
Figure 39. GUI - OSR Selection for Comparator Unit - Config Tab

Figure 39 shows how to select the desired OSR for the comparator unit of the TMS320F28377D microcontroller. This is the alternative digital signal processing path that can be use to issue a warning signal when an over-current event is detected by the acquisition system.
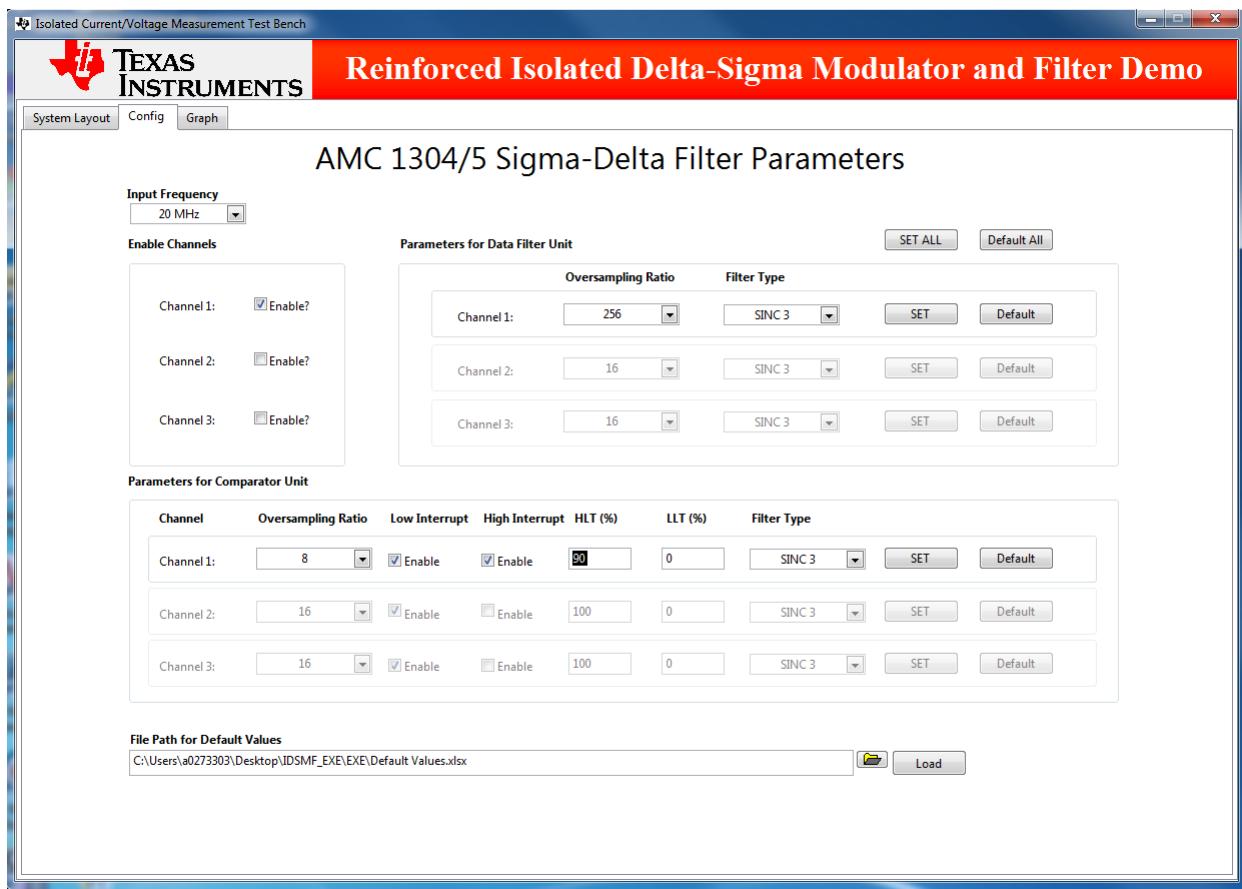
Figure 40. GUI - Comparator Unit - High Level Threshold Setting

A warning signal can be issued for two types of events: a) an over-current event that exceeds a low level threshold, and b) an over-current event that exceeds a high level threshold. The thresholds are set by the user as shown in Figure 40.
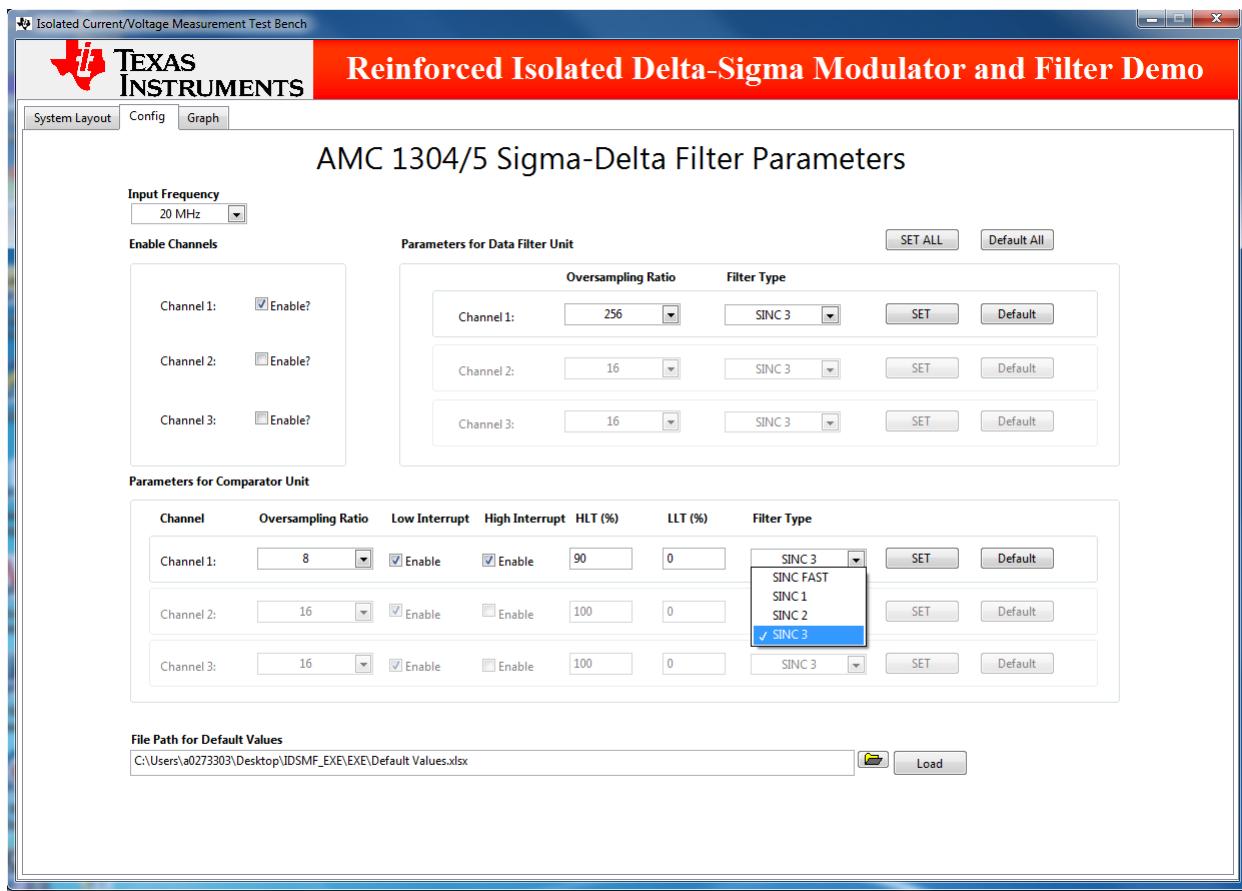
Figure 41. GUI - Comparator Unit Filter Selection - Config Tab

The filter type of the comparator unit can be selected as shown in Figure 41

Once all parameters have been entered, the user clicks the "SET" button in order to write into the appropriate TMS320F28377D registers.

7.3   Graph Tab

The Graph tab of the GUI is shown in Figure 42. Note that the user selects the type of isolated delta-sigma modulator connected to the TMS320F28377D microcontroller.
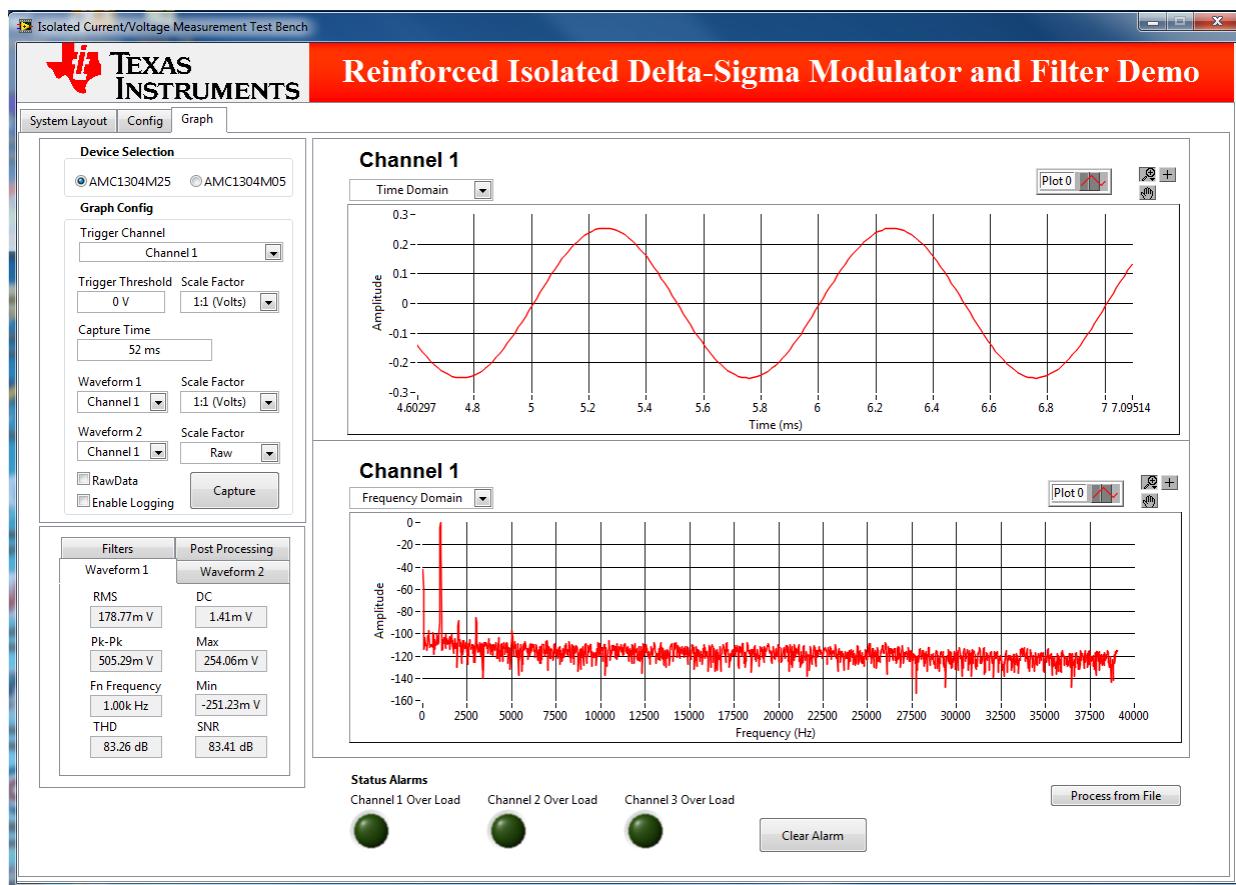
Figure 42. GUI - Graph Tab

As shown in Figure 43, the Graph tab allows the user to select a triggering channel and a triggering threshold. The behavior of this function is the same as that of an oscilloscope triggering on a rising signal. Acquisition will start when the first sample is below the threshold level and the second sample is above the threshold level. Note also that if no channel is selected as the trigger channel, acquisition will begin as soon as the "Capture" button is pressed regardless of the level of the acquired signal.
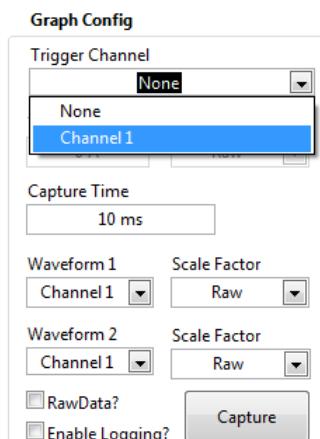
Figure 43. GUI - Trigger Channel

Figure 44 shows how the user can select a scale factor to display the time domain graph of the acquired signal. Selecting "Raw" displays the actual codewords read from the TMS320F28377D. The other scale factors convert the codeword values read from the TMS320F28377D filter output to input-referred signals.
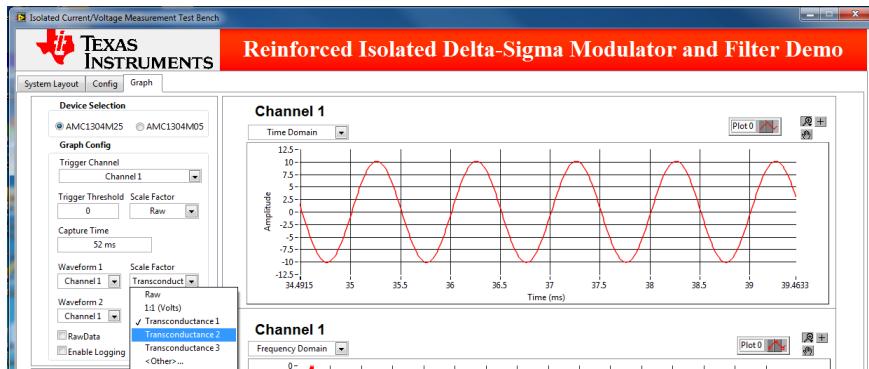
Figure 44. GUI - Scale Factors

Section 6.1 describes the procedure to convert from codewords to voltage drop across the shunt and selecting the scale factor "1:1 (Volts)" corresponds to performing such calculation. The scale factors "Transconductance 1", "Transconductance 2", and "Transconductance 3" go one step further and express the acquired signal in amps by taking into account the value of the shunt resistor used.

The scale factor "Transconductance 1" corresponds to a 25 mΩ shunt, "Transconductance 2" corresponds to a 20 mΩ shunt, and "Transconductance 3" corresponds to a 10 mΩ shunt.

The file "Scale Factor.csv", which is located on the root folder where the GUI is installed, allows the user to modify the constants associated with the scale factors. Figure 45 shows the constants included by default in Scale Factor.csv.

Figure 45. Default Constants in "Scale Factor.csv" File

All the constants in the file "Scale Factor.csv" need to be calculated only for OSR of 256 and the Sinc^3 filter option; the GUI takes these constants and performs further calculations to express the acquired data properly even if the user chooses OSR other than 256 and filter type different from Sinc^3. For example, the constant corresponding to the "1:1 (Volts)" scale factor is calculated as shown in Equation 32. For this design, the constant corresponding to the "Transconductance 1" scale factor has been calculated using the 25 mΩ shunt value selected in Section 3.1.

Equation 33 shows the calculation of the constant corresponding to the "Transconductance 1" scale factor and Figure 46 shows the measured time domain plot when "Transconductance 1" is used as a scale factor.

$$1:1_{Scale\_factor} = \frac{V_{Clipping}}{\left|Codeword_{peak}\right|} = \frac{0.3125\ V}{\left|-32,768\right|} = 9.5367\ x10^{-6}$$

(32)

$$Transconduc\tan ce\_1_{Scale\_factor} = \frac{V_{Clipping}}{\left|Codeword_{peak}\right|\left|R_{shunt}\right|} = \frac{0.3125\ V}{\left|-32,768\right|0.025} = 3.8147\ x10^{-4}$$

(33)
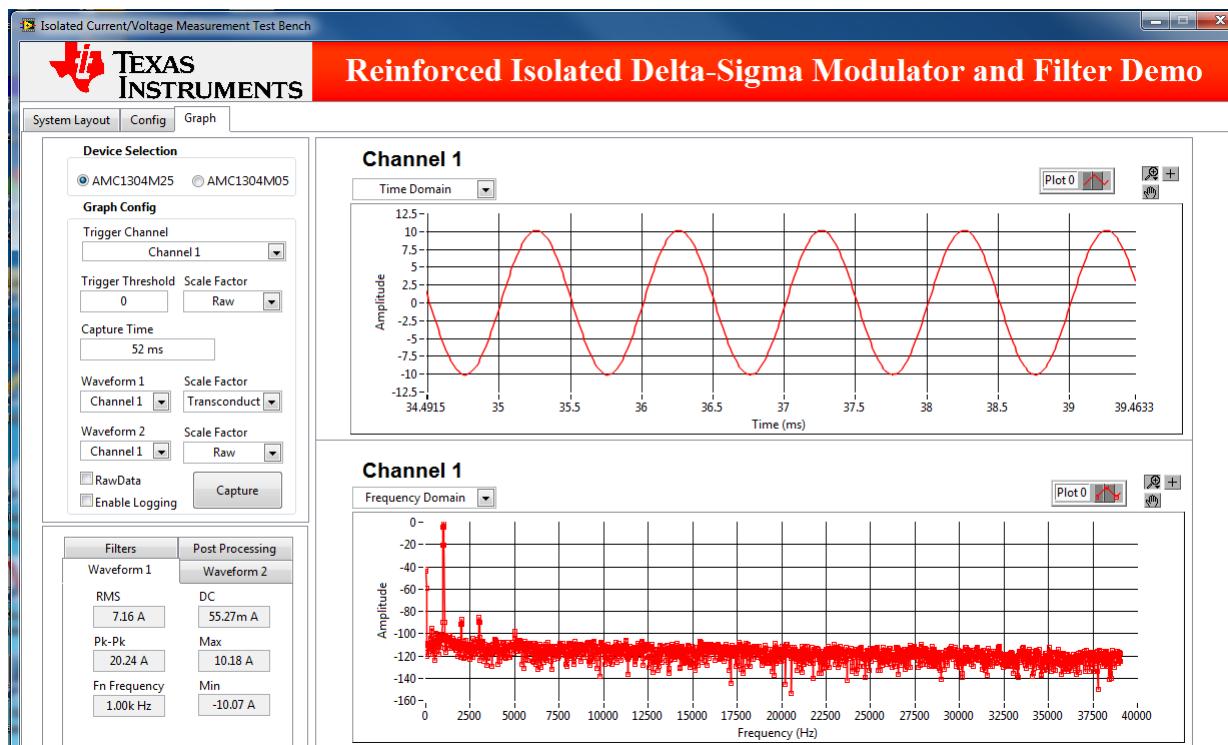
Figure 46. GUI - AC Results Expressed in Amps

The Post Processing tab of the GUI allows the user to select from a variety of windows that can be applied to the acquired signal for the purpose of frequency domain data display. Figure 47 shows the windows available.
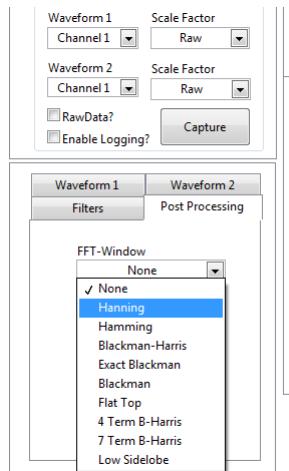
Figure 47. GUI - Post Processing Tab

Another important feature of this design is the ability to monitor and capture the raw bit-stream from the AMC1304M25. This may be useful for users interested in applying a different type of digital filtering from that available in the Sigma-Delta Filter Modules of the TMS320F28377D. Figure 48 shows the raw bit-stream capture displayed in the Graph tab.
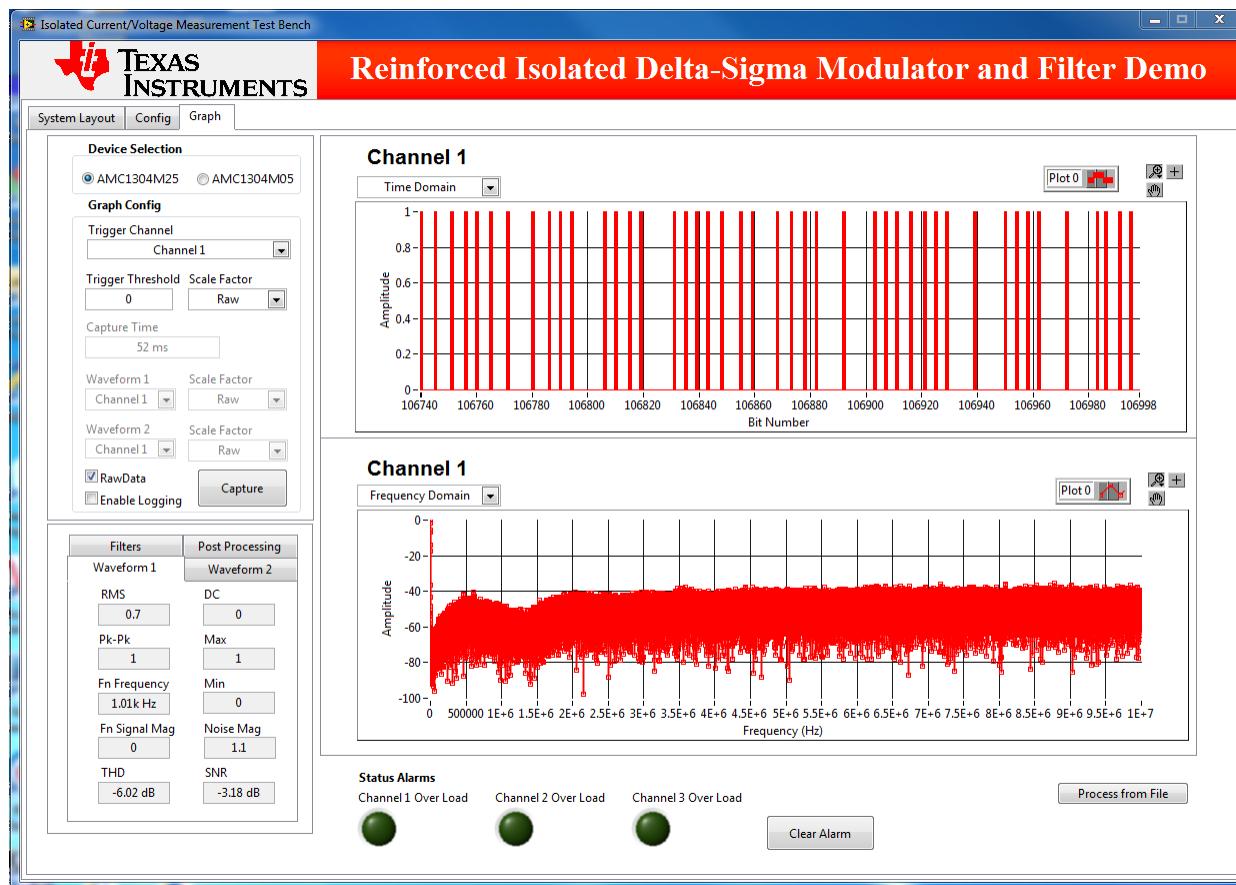
Figure 48. GUI - AMC1304M25 Raw Bit-stream Display

8   Modifications

The components and settings selected for this design are optimized to meet the design goals mentioned in Section 1; however, the user can make several modifications in order to adapt the design to their particular needs.

There are designs where the power dissipation in the current shunt is more important than maximizing the input range to the delta sigma modulator. In such cases the shunt resistor value is calculated using Equation 34.

$$R_{shunt} = \frac{P_{max}}{I^2_{max}}$$

(34)

If the user requires lower isolation capabilities, the AMC1304 can be replaced by the AMC1204, another isolated delta-sigma modulator which provides up to 1.2 kV$_{peak}$ of working insulation voltage and 5.1 kV$_{peak}$ of transient overvoltage.

If the user has an isolated voltage supply for the AMC1304 high side, then all is needed is to:

*   Set the jumper JP1 of the AMC1304M25 PCB to the position labeled *Ext* as shown in Figure 49, and
*   Connect the supply to the two-wire screw terminal at J3.
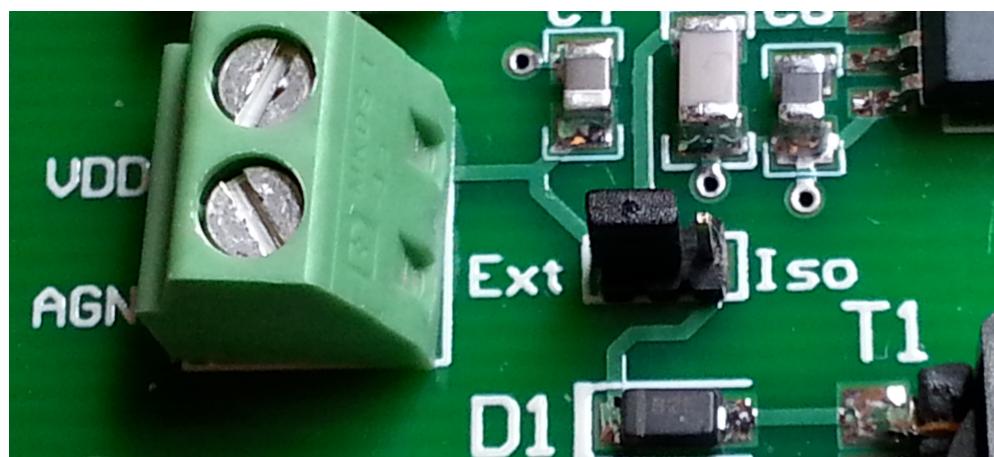
Figure 49. Jumper Setting for External Supply to AMC1304M25

As an alternative to the sigma-delta filter modules in the TMS320F28377D, the designer can use the AMC1210, four-channel digital filter with functionality equivalent to that provided by the TMS320F28377D in this design. Note however, that a host processor would still be needed in order to properly configure the AMC1210.

If the user desires to feed a clock frequency different from those shown in Figure 36, the user just needs to connect the external clock source to pin 101 of the docking station and the bit stream from the AMC1304M25 can be acquired from pin 99 of the docking station.

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9 About the Author

Jose Duenas is an Applications Engineer in the Precision Analog, Energy Solutions team at Texas Instruments based in Tucson, Arizona.

10 References and Acknowledgments

1. Oljaca, M, & Hendrick, T. *Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications*, Application Report published by Texas Instruments, available at: SBAA094

2. The author would like to thank Matthias Taenzer (Systems & Applications Manager), Tom Hendrick (Senior Applications Engineer at TI), Arek Spring (Product Definer), Navaneeth Kumar (Systems Architect at TI) and Nelson Alexander (Systems Engineer at TI) for their technical contributions to this design.

3. The author would like to thank Peter Semig (Applications Engineer at TI) and Collin Wells (Applications Engineer at TI) for their valuable revisions and technical contributions to this document.

11 Appendix

11.1 Electrical Schematic and Bill of Materials for AMC1304M25 PCB

The schematic and Bill of Materials for the AMC1304M25 PCB are shown in Figure 50 and Figure 51 respectively.
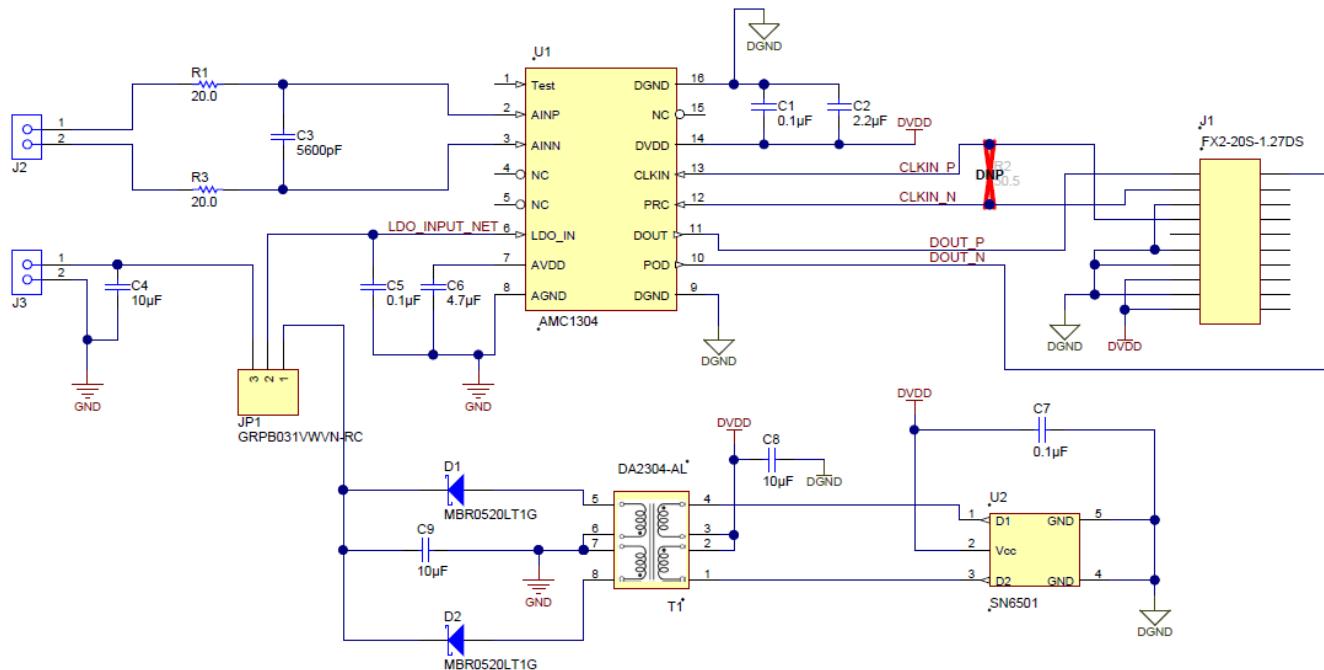
Figure 50. Schematic for AMC1304M25 Board

Item	Quantity	Designator	Description	Manufacturer	PartNumber
1	1	!PCB1	Printed Circuit Board	Any	AMC1304EVM - TIPD
2	3	C1, C5, C7	CAP, CERM, 0.1uF, 25V, +/-5%, C0G/NP0, 1206	TDK	C3216C0G1E104J
3	1	C2	CAP, CERM, 2.2uF, 16V, +/-10%, X7R, 0805	Taiyo Yuden	EMK212B7225KG-T
4	1	C3	CAP, CERM, 5600pF, 25V, +/-5%, C0G/NP0, 0805	TDK	C2012C0G1E562J
5	3	C4, C8, C9	CAP, CERM, 10uF, 16V, +/-10%, X5R, 0805	Taiyo Yuden	EMK212BJ106KG-T
6	1	C6	CAP, CERM, 4.7uF, 10V, +/-10%, X5R, 0805	Kemet	C0805C475K8PACTU
7	2	D1, D2	Diode, Schottky, 20V, 0.5A, SOD-123	ON Semiconductor	MBR0520LT1G
8	3	FID1, FID2, FID3	Fiducial mark. There is nothing to buy or mount.	N/A	N/A
9	1	J1	1.27mm Pitch Multi-function Two Piece Connector	Hirose	FX2-20S-1.27DS
10	2	J2, J3	Conn Term Block, 2POS, 3.5mm, TH	Phoenix Contact	1751248
11	1	JP1	Header, 3-Pin	Sullins Connector Solutions	
12	2	R1, R3	RES, 20.0 ohm, 0.1%, 0.1W, 0603	Yageo America	RT0603BRD0720RL
13	1	SH-J1	Shunt, 1.27 mm	Harwin Inc	M50-2000005
14	1	T1	1:2.2 Isolation Transformer	Coilcraft	DA2304-AL
15	1	U1	AMC1304Mx in 16-pin DW (SOIC) package	Texas Instruments	AMC1304
16	1	U2	SN6501 transformer driver	Texas Instruments	SN6501
17	0	R2	RES, 50.5 ohm, 0.1%, 0.1W, 0603	Yageo America	RT0603BRD0750R5L

Figure 51. Bill of Materials for AMC1304M25 Board

11.2 Electrical Schematic and Bill of Materials for the Docking Station

The schematic and Bill of Materials for the Docking Station are shown in Figure 52, Figure 53 and Figure 54 respectively.
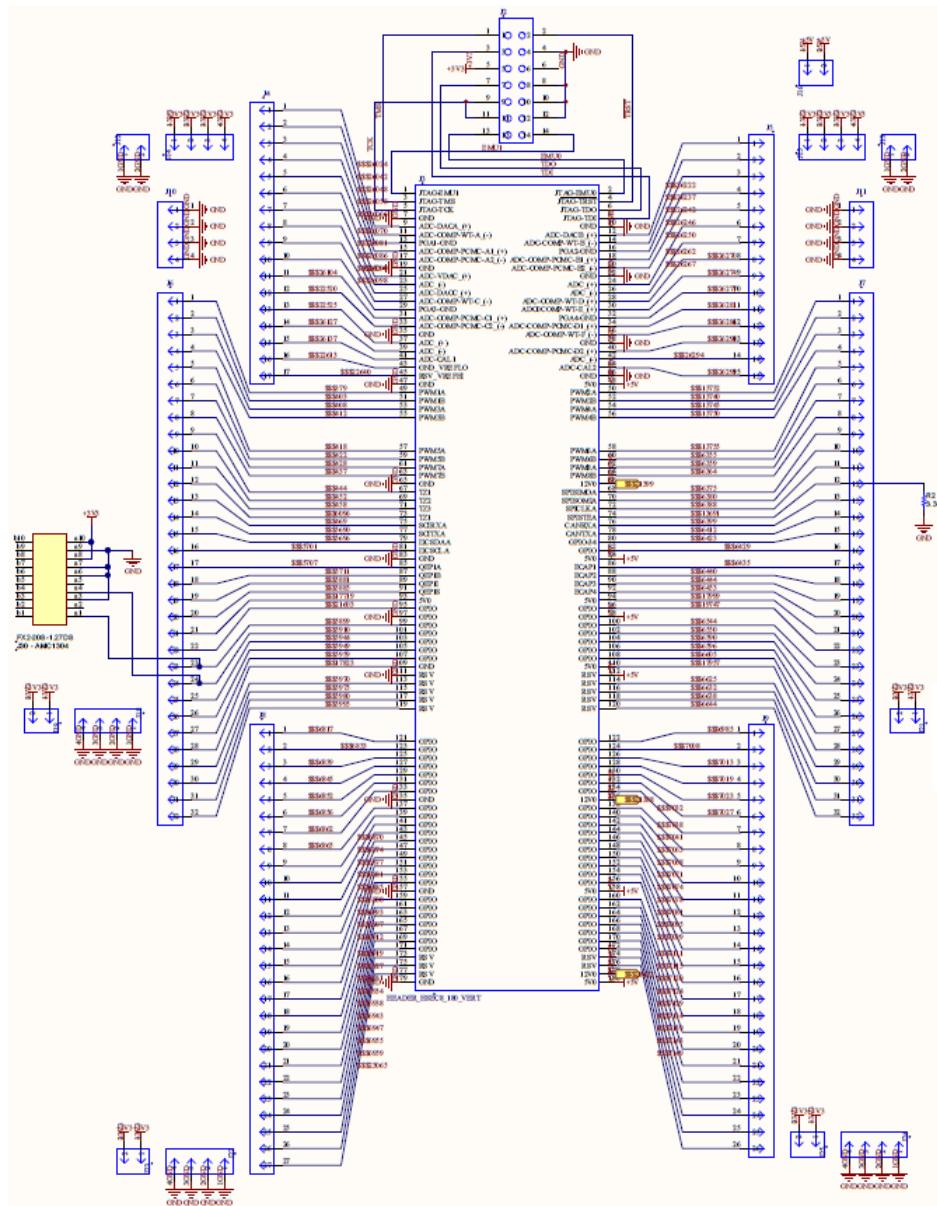
Figure 52. Schematic for Docking Station - Part 1
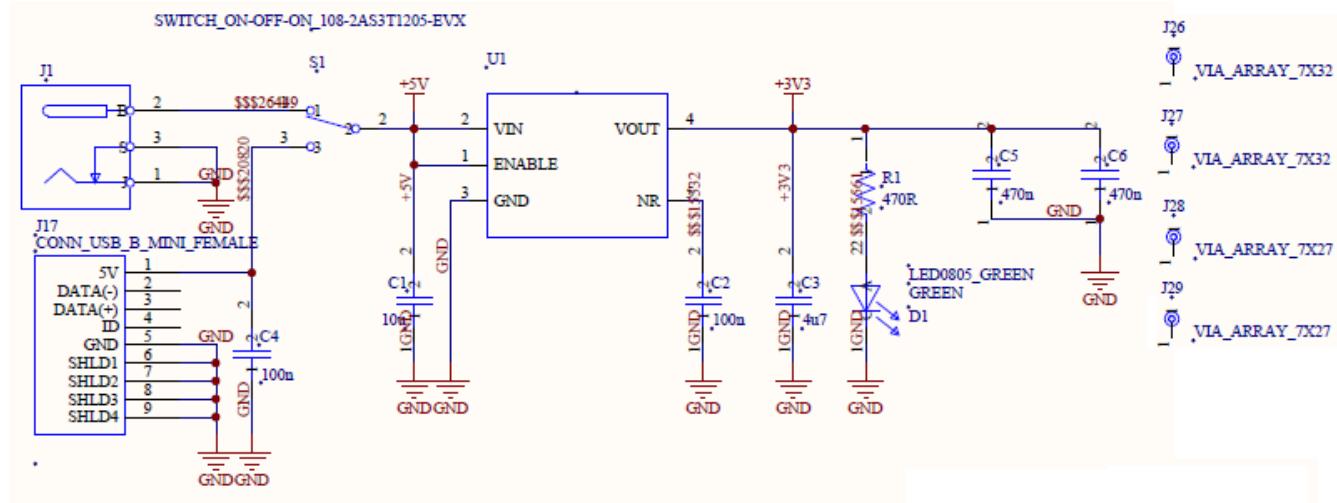
Figure 53. Schematic for Docking Station - Part 2

Item	Quantity	Designator	Value	Description	Manufacturer	PartNumber
1	1	C1	10u	CAP CER 6V3 10% X5R 0805	Taiyo Yuden	JMK212BJ106KD-T
2	2	C2 C4	100n	CAP CER 6V3 10% X7R 0805	Kemet	C0805C104K9RACTU
3	1	C3	4u7	CAP CER 6V3 10% X5R 0805	Taiyo Yuden	JMK212BJ475KG-T
4	2	C5-6	470n	CAP CER 6V3 10% X7R 0805	TDK Corporation	CGJ4J2X7R0J474K125AA
5	1	D1	GREEN	LED GREEN 0805 SMD, Diffused, 567nm	Stanley Electric Co	PG1112H-TR
6	1	J1		CONN PWR JACK 2.5X5.5MM HIGH CUR	CUI Inc	PJ-002BH
7	1	J2		Header, Male, 7x2-pin, 100mil spacing, remove pin 6	FCI	67996-114HLF
8	1	J3		180 pin (120 + 60) HSEC8 socket	Samtec	HSEC8-130-01-L-DV-A & HSEC8-160-01-L-DV-A-BL
9	1	J4		Header, Male, 1x17-pin, 100mil spacing	Harwin Inc	M20-9731746
10	1	J5		Header, Male, 1x15-pin, 100mil spacing	Harwin Inc	M20-9991546
11	2	J6-7		Header, Male, 1x32-pin, 100mil spacing	Harwin Inc	M20-9993246
12	1	J8		Header, Male, 1x27-pin, 100mil spacing	Harwin Inc	M20-9992746
13	1	J9		Header, Male, 1x26-pin, 100mil spacing	Harwin Inc	M20-9992646
14	8	J10-11 J14-15 J18 J20 J22 J24		Header, Male, 1x4-pin, 100mil spacing	3M	961104-6404-AR
15	7	J12-13 J16 J19 J21 J23 J25		Header, Male, 1x2-pin, 100mil spacing	3M	961102-6404-AR
16	1	J17		CONN RECEPT MINI USB2.0 5POS	Hirose Electric Co Ltd	UX60-MB-5ST
17	1	R1	470R	RES 1/8W 5% 0805 SMD	Stackpole Electronics Inc	RMCF0805JT470R
18	1	S1		Toggle Switches SPDT ON-ON PC MOUNT	E-Switch	200AWMSP1T1A1M2QE
19	1	U1		IC LDO REG 3.3V 500MA SOT223-6	Texas Instruments	TPS79533DCQ

Figure 54. Bill of Materials for Docking Station

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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