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# *Ultra-Thin, Small Footprint 1-W, 12- to 36-V Isolated Power Supply With ±15 V and 5 V for Analog PLC Modules*

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## Design Resources

| | |
|---|---|
| TIDA-00237 | Design Files |
| TIDA-00129 | Associated Design |
| LM5017 | Product Folder |
| TPS62175 | Product Folder |
| TPS7A4901 | Product Folder |
| TPS7A3001 | Product Folder |

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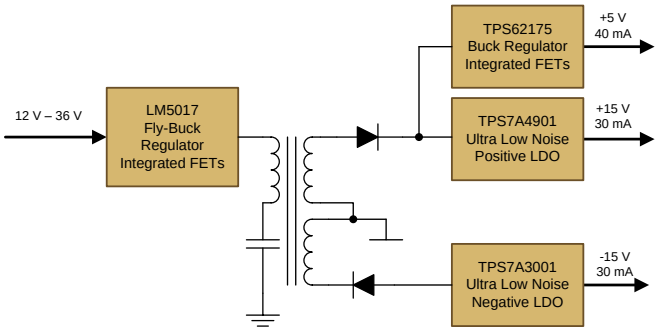
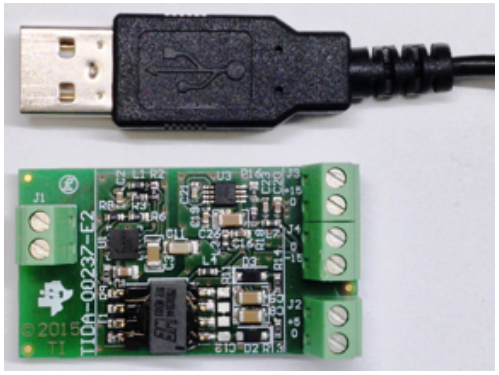
## Design Features

- Wide Input Voltage Range: 12 to 36 V (24 $V_{NOM}$)
- Three Isolated Outputs:
  - 15 $V_{ISO}$ at 30-mA Ultra-Low Noise
  - –15 $V_{ISO}$ at 30-mA Ultra-Low Noise
  - 5 $V_{ISO}$ at 40-mA
- ±2.5% Output Voltage Accuracy
- Ultra-Low Profile < 5 mm
- IEC 61131-2 Compliant

## Featured Applications

- PLC, DCS, and PAC
  - Analog Input Module
  - Analog Output Module
  - Transducer Module

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# 1 Key System Specifications

**Table 1. Key System Specifications**

| SYMBOL | PARAMETER | CONDITIONS | SPECIFICATION | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| $V_{IN}$ | Input voltage | Normal operation | 12[1] | 24 | 36 | V |
| $I_Q$ | Quiescent current | No output load | — | 9 | 15 | mA |
| $V_{J2}$ | Output voltage connector J2 | Normal operation | 4.9 | 5 | 5.1 | V |
| $V_{J3}$ | Output voltage connector J3 | Normal operation | 14.8 | 15 | 15.2 | V |
| $V_{J4}$ | Output voltage connector J4 | Normal operation | –14.8 | –15 | –15.2 | V |
| $I_{J2}$ | Output current | $V_{IN} > V_{IN}$(min) | 0 | — | 40 | mA |
| $I_{J3}$ | Output current | $V_{IN} > V_{IN}$(min) | 0 | — | 30 | mA |
| $I_{J4}$ | Output current | $V_{IN} > V_{IN}$(min) | 0 | — | –30 | mA |
| $P_{OUT}$ | Output power | | 0 | — | 1.1 | W |
| $V_{ISO(AC)}$ | Isolation voltage | AC, 1 min | 490 | | — | V |
| $V_{ISO(DC)}$ | Isolation voltage | DC, 1 min | 700 | | — | V |
| $V_{ISO(PERM)}$ | Isolation voltage | DC, infinite min | 70 | | — | V |
| η | Efficiency | $V_{IN}$ = 12 V, $P_{OUT}$ = max | — | 74 | — | % |
| | | $V_{IN}$ = 24 V, $P_{OUT}$ = max | — | 67 | — | % |
| | | $V_{IN}$ = 36 V, $P_{OUT}$ = max | — | 60 | — | % |
| $d_{CREEP}$ | Creeping distance | | 1 | — | — | mm |
| H1 | Component height above PCB | | — | 4.9 | — | mm |
| H2 | Component height below PCB | | — | 0.9 | — | mm |
| $A_A$ | Active area size | | — | 25.4 × 25.4 | — | $mm^2$ |
| $V_U$ | Undervoltage lockout hysteresis | $V_{IN}$ ramping up | — | 3.4 | — | V |

(1) Turn-off voltage during operation, turn-on voltage is $V_{IN(min)} + V_U$, typically 15.4 V.

## 2 System Description

A programmable logic controller (PLC) is a key component in factory automation. The PLC monitors input and output (I/O) modules in real-time and control the process according to the requirements. Thanks to flexible I/O modules, they can adapt to many different process requirements. The analog I/O modules, local or remote, acquire process data and set outputs to actuate the process. Figure 1 exhibits an analog input module with an emphasize on the power block.

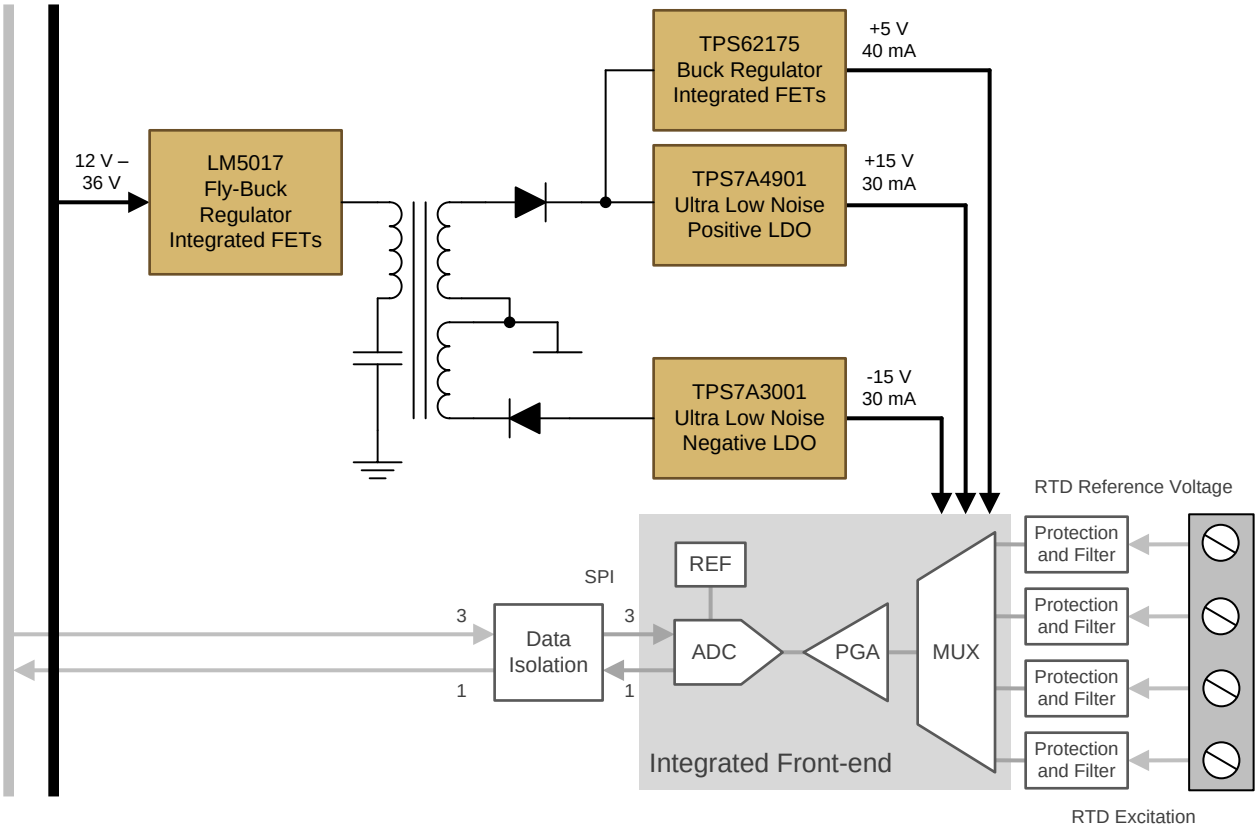


**Figure 1. Generic Illustration of Analog Input Module**

Analog input modules represent about 10% of all PLC I/O modules, and analog output modules represent about 5%. Typical signaling are 4- to 20-mA current loop or ±10-V analog. The analog I/O modules use ADC and DACs to convert analog process signals to digital values or vice versa in the output module. A proper data conversion requires an ADC or DAC and potentially an amplifier stage to drive, level shift, filter, or impedance match the data converter to the input or output signal. To ensure the expected performance from the data converter and the amplifier stage, a dedicated low-noise isolated power supply solution is required, which is the main topic of the TIDA-00237. Figure 2 shows a block diagram of the design.

## 3 Block Diagram

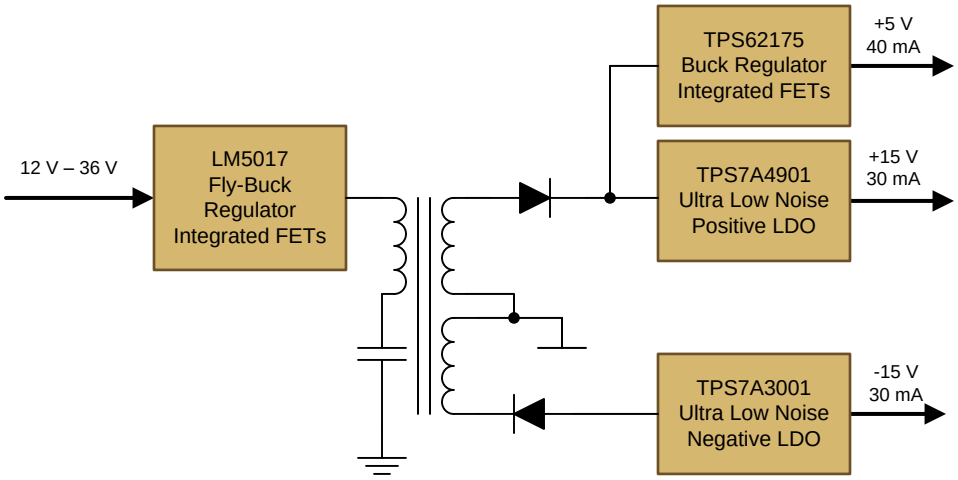


**Figure 2. TIDA-00237 Isolated Power Supply Diagram for Analog Input Module**

### *3.1 Highlighted Products*

The TIDA-00237 provides the isolated analog and digital supply voltages for PLC analog I/O modules. For the analog section of the module, TIDA-00237 generates 15 and –15 V. These voltages are highly accurate and have minimal noise. An additional 5 V can be used as the digital supply for the data converter, a microcontroller, and the isolation device. To keep the transformer small, this voltage is created from the 15-V rail by using a high efficiency DC/DC converter.

#### 3.1.1 LM5017

The LM5017 is a 100-V, 600-mA synchronous step-down regulator with integrated high-side and low-side MOSFETs. The constant on-time (COT) control scheme employed in the LM5017 requires no loop compensation, provides excellent transient response, and enables very high step-down ratios. The on-time varies inversely with the input voltage resulting in nearly constant frequency over the input voltage range. A high-voltage startup regulator provides bias power for internal operation of the IC and for integrated gate drivers.

A peak current limit circuit protects against overload conditions. The undervoltage lockout (UVLO) circuit allows the input under voltage threshold and hysteresis to be independently programmed. Other protection features include thermal shutdown and bias supply undervoltage lockout (VCC UVLO).

#### 3.1.2 TPS7A4901

The TPS7A4901 is a positive, high-voltage (36 V), ultra-low-noise (15.4-$\mu V_{RMS}$, 72-dB PSRR) linear regulator capable of sourcing a load of 150 mA.

This linear regulator includes a capacitor-programmable soft-start function that allows for delaying the output voltage generation until the power source is operating stable. Other features available include built-in current limit and thermal shutdown protection to safeguard the device and system during fault conditions.

The TPS7A4901 is designed using bipolar technology and is ideal for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This design makes the device an excellent choice to power operational amplifiers, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and other high-performance analog circuitry.

In addition, the TPS7A4901 is suitable for post DC/DC converter regulation. By filtering out the output voltage ripple inherent to DC/DC switching conversion, maximum system performance is provided in sensitive instrumentation, test and measurement, audio, and RF applications.

### 3.1.3 TPS7A3001

The TPS7A3001 is the complementing device to the TPS7A4901 described in the previous paragraph. It is a negative, high-voltage (–36 V), ultra-low-noise (15.1-$\mu V_{RMS}$, 72-dB PSRR) linear regulator capable of sourcing a maximum load of 200 mA. The feature list of the TPS3001 is a 1:1 equivalent to the one of the TPS7A4901.

### 3.1.4 TPS62175

The TPS62175 is a high efficiency synchronous step-down DC-DC converter, based on the DCS-Control topology, with a wide operating range of input voltage from 4.75 to 28 V providing up to a 500-mA output current.

The TPS62175 automatically enters power save mode at light loads, to maintain high efficiency across the whole load range. As well, it features a Sleep mode to supply applications with advanced power save modes like ultra-low-power microcontrollers. The Power Good output may be used for power sequencing or power-on reset.

The device features a typical quiescent current of 22 µA in normal mode and 4.8 µA in sleep mode. In sleep mode, the efficiency at very low load currents can be increased by as much as 20%. In shutdown mode, the shutdown current is less than 2 µA and the output is actively discharged.

## 4 System Design Theory

For a 1-W isolated power supply with a wide input voltage range, no opto-coupler feedback and low number of external components the Fly-Buck™ topology is superior to a flyback design. This topology also allows design flexibility for a primary non-isolated power supply. For a high-end post regulation, LDOs with high PSRR are chosen to ensure a clean power supply for analog circuits. The 5-V rail is derived from the 18-V transformer output using a high efficiency buck regulator. The Fly-Buck is implemented using an LM5017. This part fulfils the Fly-Buck requirements, allowing a small circuit footprint and arrives at a low BOM cost. Figure 3 shows the architecture of the LM5017.

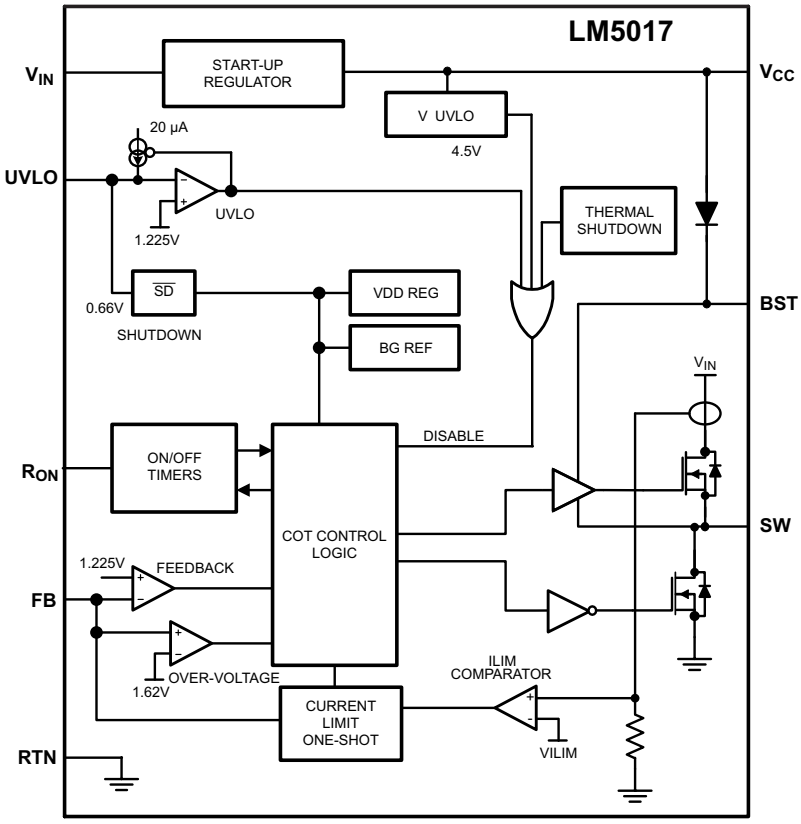


**Figure 3. LM5017 Circuit Diagram**

As most of the analog PLC I/O modules are space constrained, the TIDA-00237 aims at keeping the transformer height below 5 mm and a small overall footprint. This has a major influence on the component selection, which is described in Table 2. As the transformer T1 has to be below 5-mm height, an ER9.5 core is the largest acceptable size. To keep transformer cost down, the AWG has to be below or equal to 38. A 50% bobbin fill split between primary and secondary winding provides the best performance. Therefore, the secondary winding is limited to approximately 36 turns with this transformer core. Assuming a 1:3 ratio, this corresponds with 12 turns on the primary side; at 1:2 this is 18 turns. Due to limitations based on core saturation, dependencies exist as shown in Table 2.

**Table 2. Transformer Dependencies**

| PRIMARY TURNS | SATURATION CURRENT (mA) | INDUCTANCE (µH) | MAXIMUM TURN RATIO | NOTES |
|---|---|---|---|---|
| 12 | 980 | 22 | 1:3 | Larger air gap |
| 12 | 780 | 35 | 1:3 | |
| 15 | 620 | 56 | 1:2.4 | Selected as transformer T1 using 1:2.1 turn ration |
| 18 | 520 | 80 | 1:2 | |

## 4.1 Primary Side Output Voltage, $V_{C1}$

The primary side voltage, $V_{C1}$, is depending on multiple factors. As a rule of thumb, the duty cycle should be below 50%; otherwise, the transfer time for the energy required to maintain the minimum secondary voltage at maximum current is too short. This short time leads to larger peak currents, inferior load regulation performance, and larger drop voltages at the secondary side rectifier diodes, D2 and D3, and the synchronous rectifier in the LM5017. In TIDA-00237, this would correspond to a primary side voltage of 6 V and a turn ratio of approximately 1:3. However, a turn ratio of 1:3 increases the peak current in the forward MOSFET of the LM5017 at high input voltage and the given inductance. With a turn ration of 1:2 and the max input voltage of 36 V, it is still possible to keep the peak current below the maximum spec for LM5017. A primary voltage of 9 V at C1 is required to support the 1:2 ratio with 18 V at the output. Therefore, the duty cycle of 75% at 12 V ($V_{IN(MIN)}$) is needed. At this duty cycle, the design is still working stable even though maximum efficiency is no longer achieved at input voltages below 18 V. A smaller capacitor C1 is increasing the power capabilities at a 75% duty cycle. The LM5017 is regulating the output voltage such that the bottom voltage of the output ripple matches the reference voltage of the LM5017. Therefore, a larger ripple at C1 at lower input voltage and larger output currents increases the average $V_{C1}$. This leads to the higher energy transfer and a better load regulation with the same transformer size. A ripple between 1 and 1.5 V on C1 at maximum output power has been selected.

## 4.2 Transformer Calculation

In Section 4.1, the primary voltage of the transformer has been selected as well as the winding ratio. The detailed calculation to verify the potential for correct operation is shown in Table 3.

**Table 3. $V_{J3/J4}$ Transformer T1 Voltage Calculation**

| PARAMETER | CONDITIONS | VALUE |
|---|---|---|
| $V_{J3/J4}$ | Full load | 15.000 V |
| LDO (U2, U3) drop-out voltage | 30 mA, 125°C | + 00.180 V |
| Diode D2 and D3 drop-out voltage | 260 mA (average forward current(1)) | + 00.750 V |
| Transformer T1, secondary winding loss | 0.75 Ω, 260 mA (average forward current(1)) | + 00.195 V |
| Required transformer T1, secondary winding voltage | | = 16.125 V |
| Load regulation accuracy | $V_{IN(MIN)}$ to $V_{IN(MAX)}$ | + 01.610 V (10%) |
| Required transformer T1, secondary winding voltage (including load reg.) | $V_{IN(MIN)}$ to $V_{IN(MAX)}$ | = 17.375 V |
| | | |
| Transformer T1, primary winding voltage | Winding ratio 1:2.1 | 8.27 V |
| Transformer T1, primary winding loss | 0.3 Ω, 500 mA (average forward current(1)) | + 0.15 V |
| U1 synchronous switch loss | 1 Ω, 500 mA (average forward current(1)) | + 0.50 V |
| Required $V_{C1}$ voltage | Average | = 8.92 V |
| | | |
| $V_{IN(MIN)}$ duty cycle | $V_{IN(MIN)}$ = 12 V | 74.30% |
| | $V_{C1(MIN)}$ = 9 V | |

(1) Average current while the synchronous switch is on – simulated value

The relevant current for the saturation calculation of the transformer consists of two elements, which are the current ripple and the DC current offset as shown in Equation 3. The current ripple is determined by the switching process as in Equation 1 and the DC offset current from the required transfer power as in Equation 2:

$$I_{ripple} = \frac{\Delta t \times \Delta V}{L} = \frac{\Delta t \times \left(V_{IN} - V_{C1}\right)}{L_{T1}} \quad (1)$$

$$I_{DC} = \frac{P_{tot}}{V_{C1}} \quad (2)$$

$$I_{sat} = I_{DC} + \frac{1}{2} \times I_{ripple} \quad (3)$$

The starting point for the calculation is the selected voltage $V_{C1}$, which determines the duty cycle and as such affects the relevant timing for the ripple current. On the secondary side, a minimum voltage of 17.8 V is required as per the calculation in Table 3. The outputs J3 and J4 need a total of 60 mA. For the output J2 (5 V) with its 200-mW requirement at 15.18 V (see line 2 in the Table 3), a current of 16.5 mA is needed assuming an efficiency of the DC/DC converter of 80%.

Calculating with a DC current of 80 mA on the secondary side includes some guard band. Transfer power is therefore 17.8 V × 0.08 A = 1.42 W. Based on this power, Equation 2 above calculates the DC current in the primary side of the transformer to 160 mA.

The selected transformer T1 has a rated maximum saturation current of 520 mA according to Table 2. At a DC current of 160 mA per Equation 3 above, this leaves room for 720 mA ripple current peak to peak. Based on Equation 1, this allows an on-time of 19.2 µs at a $V_{IN}$ of 12 V and 2.13 µs at $V_{IN}$ of 36 V. In order to support 36 V, the minimum frequency has to be calculated from the 1.9 µs. With the duty cycle of 25% at 36 V, the cycle time is 7.6 µs corresponding to a frequency of 117 kHz. Therefore, 200 kHz is safe to use and leaves enough guard band to prevent core saturation.

$V_{C1}$ needs to be on average 8.9 V. For an accurate regulated voltage, the voltage ripple of C1 has to be considered. The regulator sets its switching trip point according to the bottom level of the ripple voltage so that the average voltage is higher by approximately half the ripple voltage. With the capacitance of 1.5 µF (0.75 µF degraded) and a ripple current of 600 mA at a frequency of 200 kHz the ripple voltage is simulated to be ~900 mV resulting in an average increase of 450 mV. R5, C6, R7, and C7 add an artificial ripple with the amplitude of 30 mV to the feedback input, which corresponds to a virtual ripple of 200 mV at C1 and an average increase of further 100 mV totaling to 550 mV. Therefore, the feedback network has to be calculated for 8.35 V.

The feedback resistor network calculates as per the following formulas. The resistor RFB1 is set to 2 kΩ, resulting in a divider current of ~0.6 mA or a power loss of 10 mW. If the design is located in a noise-free environment, a smaller divider current could be selected. However, 2 kΩ is a good starting point for an industrial design.

$$V_{OUT} = V_{FB} \times \left(\frac{R_{FB2}}{R_{FB1}} + 1\right) = 1.225\ V \times \left(\frac{R_{R8}}{R_{R6}} + 1\right) \quad (4)$$

$$\frac{R_{R8}}{R_{R6}} = \frac{8.35\ V}{1.225\ V} - 1 = 5.82$$
$$\Rightarrow R_{R8} = 11.63\ k\Omega \text{ and } R_{R6} = 2\ k\Omega \quad (5)$$

R8 = 11.8 kΩ and R6 = 2 kΩ are chosen to respect standard resistor values.

### 4.3 Operating Switching Frequency

In Section 4.2, the switching frequency was determined with 200 kHz. It provides an efficiency of > 85% for the DC/DC converter and sets the time for energy transfer from the primary to the secondary transformer side to 1 µs even at 75% duty cycle. R4 sets the nominal switching frequency based on Equation 6:

$$f_{SW} = \frac{V_{C1}}{10^{-10} \times R_{R4}}$$

$$R_{R4} = \frac{V_{C1}}{10^{-10} \times f_{sw}}$$

$$R_{R4} = \frac{9\ V}{10^{-10}\ A \times 200000} = 450\ k\Omega \quad (6)$$

The next closest standard resistor value is 453 kΩ.

### 4.4 Output Ripple Configuration

The LM5017 uses a constant on-time control scheme, which requires an appropriate voltage ripple of > 25 mV at the feedback node. To ensure the correct ripple injection in the regulation loop, three different schemes are possible. This design follows the scheme as per *AN-2292 Designing an Isolated Buck (Flybuck) Converter* [2] with some modifications required to support the large input voltage range and low input voltage.

## 5 Getting Started With the Hardware

The design can be operated directly out of the box. Load resistors with a power rating of at least 500 mW can be connected directly to the output terminals. For performing a maximum power test, use 470 Ω on the 15-V (J3) and –15-V (J4) terminals and 120 Ω for the 5-V output (J2). $I_{J3}$ and $I_{J4}$ will settle to 32 mA and $I_{J2}$ to 42 mA.

## 6 Test Setup

This design is tested for a minimum input voltage of 12 V ($V_{IN(MIN)}$) and maximum of 36 V ($V_{IN(MAX)}$). Output currents are hereby set to 0, 3, 10, and 32 mA for the ±15-V outputs symmetric as well as asymmetric. The 5-V output is loaded with 0, 4, 14, and 42 mA either at the same time as the ±15-V outputs also alone. Startup behavior is checked with no load and 100% load.

Table 4 shows the tested scenarios.

**Table 4. Test Settings**

| INPUT VOLTAGE $V_{IN}$ (V) | OUTPUT CURRENTS (mA) | | | OUTPUT VOLTAGES (V) | | |
|---|---|---|---|---|---|---|
| | $I_{J3}$ | $I_{J4}$ | $I_{J2}$ | $V_{J3}$ | $V_{J4}$ | $V_{J2}$ |
| 12 | 0 | 0 | 0 | 14.88 | –14.83 | 5.07 |
| 24 | | | | 14.88 | –14.83 | 5.07 |
| 36 | | | | 14.88 | –14.83 | 5.07 |
| 12 | 3 | — | — | 14.87 | –14.84 | 5.07 |
| | — | 3 | — | 14.88 | –14.83 | 5.07 |
| | — | 0 | 4 | 14.88 | –14.83 | 5.07 |
| | 3 | 3 | 4 | 14.87 | –14.83 | 5.07 |
| | 12 | — | — | 14.87 | –14.84 | 5.07 |
| | — | 12 | — | 14.88 | –14.83 | 5.07 |
| | — | — | 14 | 14.88 | –14.83 | 5.07 |
| | 12 | 12 | 14 | 14.87 | –14.83 | 5.07 |
| | 32 | — | — | 14.86 | –14.83 | 5.07 |
| | — | 32 | — | 14.88 | –14.81 | 5.07 |
| | — | — | 42 | 14.88 | –14.83 | 5.06 |
| | 32 | 32 | 42 | 14.86 | –14.81 | 5.06 |
| 24 | 3 | — | — | 14.87 | –14.84 | 5.07 |
| | — | 3 | — | 14.88 | –14.83 | 5.07 |
| | — | 0 | 4 | 14.88 | –14.83 | 5.07 |
| | 3 | 3 | 4 | 14.87 | –14.83 | 5.07 |
| | 12 | — | — | 14.87 | –14.84 | 5.07 |
| | — | 12 | — | 14.88 | –14.83 | 5.07 |
| | — | — | 14 | 14.88 | –14.83 | 5.06 |
| | 12 | 12 | 14 | 14.87 | –14.83 | 5.07 |
| | 32 | — | — | 14.86 | –14.83 | 5.07 |
| | — | 32 | — | 14.88 | –14.81 | 5.07 |
| | — | — | 42 | 14.88 | –14.83 | 5.06 |
| | 32 | 32 | 42 | 14.86 | –14.81 | 5.06 |
| 36 | 3 | — | — | 14.87 | –14.84 | 5.07 |
| | — | 3 | — | 14.88 | –14.83 | 5.07 |
| | — | 0 | 4 | 14.88 | –14.83 | 5.07 |
| | 3 | 3 | 4 | 14.87 | –14.83 | 5.07 |
| | 12 | — | — | 14.87 | –14.84 | 5.07 |
| | — | 12 | — | 14.88 | –14.83 | 5.07 |
| | — | — | 14 | 14.88 | –14.83 | 5.06 |
| | 12 | 12 | 14 | 14.87 | –14.83 | 5.07 |
| | 32 | — | — | 14.86 | –14.83 | 5.07 |
| | — | 32 | — | 14.88 | –14.81 | 5.07 |
| | — | — | 42 | 14.88 | –14.83 | 5.06 |
| | 32 | 32 | 42 | 14.86 | –14.81 | 5.06 |

# 7 Tests Results

The following paragraphs show the test results.

## 7.1 Startup and Shutdown

Figure 4 through Figure 11 are reflecting the design behavior during startup and shutdown mode. All measurements have been taken with all outputs loaded 30% ($V_{J3}$ = 15 V at 10 mA, $V_{J4}$ = –15 V at 10 mA, and $V_{J2}$ = 5 V at 10 mA).

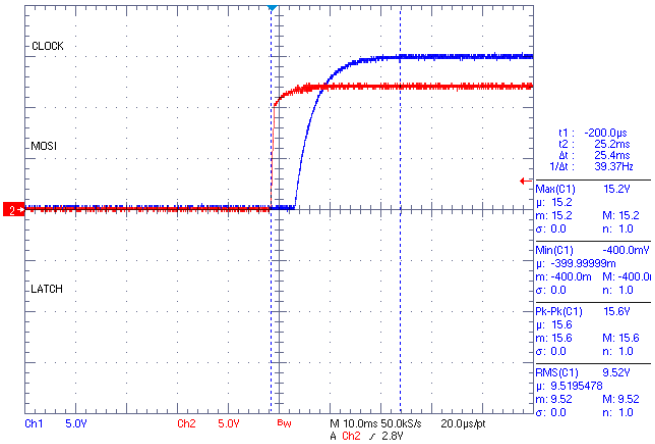


**Figure 4. Startup of $V_{J3}$ = 15 V at $V_{IN}$ = 12 V**

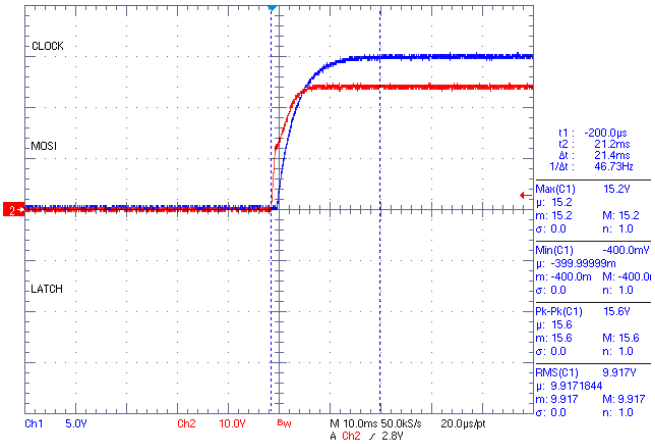


**Figure 5. Startup of $V_{J3}$ = 15 V at $V_{IN}$ = 24 V**

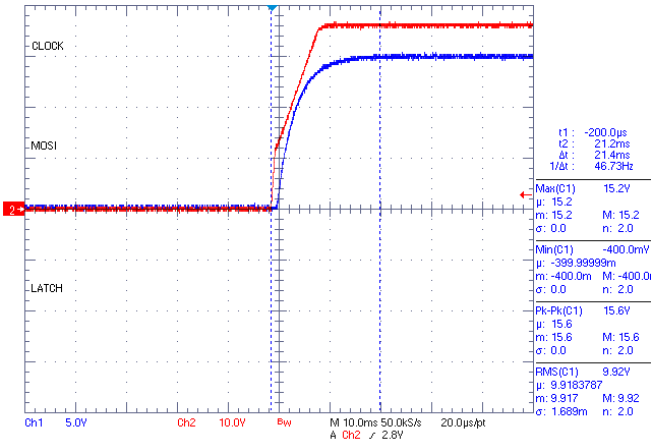


**Figure 6. Startup of $V_{J3}$ = 15 V at $V_{IN}$ = 36 V**

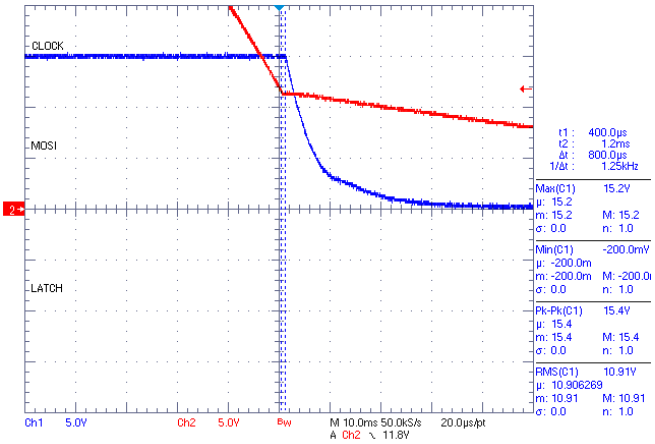


**Figure 7. Shutdown of $V_{J3}$ = 15 V at $V_{IN}$ = 24 V**

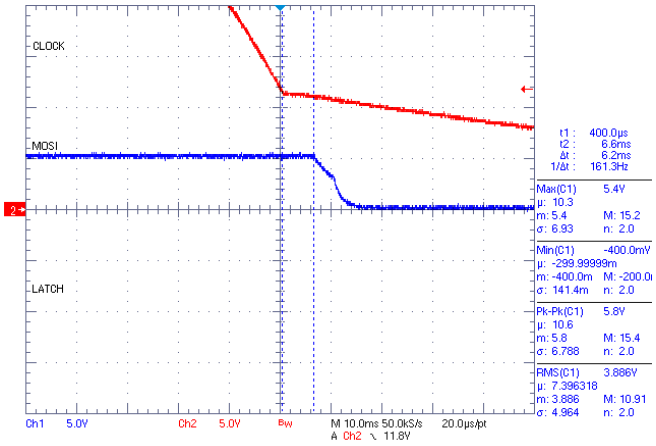


**Figure 8. Shutdown of $V_{J2}$ = 5 V at $V_{IN}$ = 24 V**

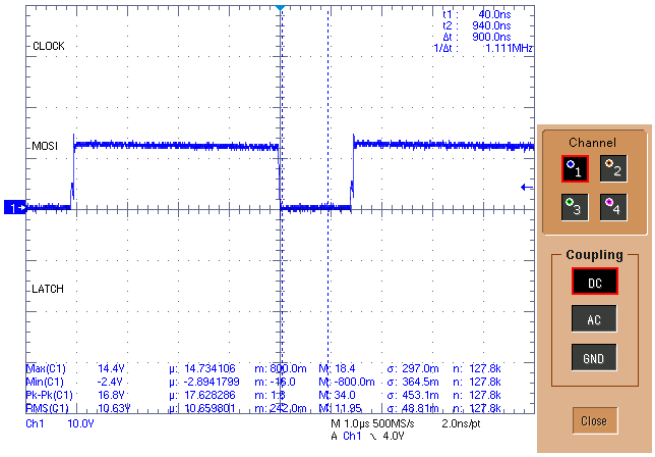


**Figure 9. Switching at $V_{IN}$ = 12 V**

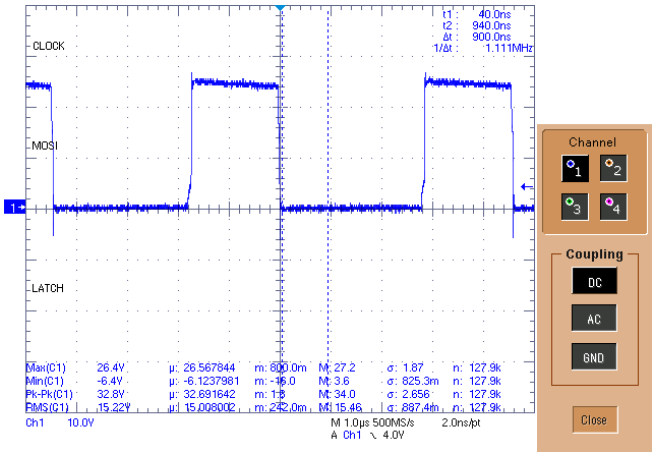


**Figure 10. Switching at $V_{IN}$ = 24 V**

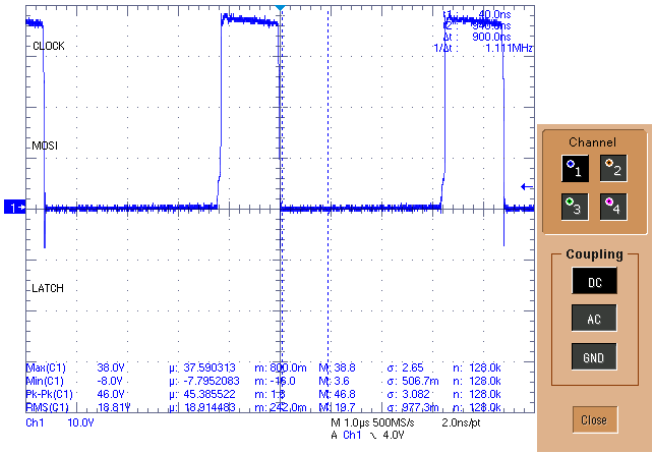


**Figure 11. Switching at $V_{IN}$ = 36 V**

## 7.2 Efficiency

Input current at 12 V ($V_{IN(MIN)}$) is measured as 135 mA under full load, which corresponds to an input power of 1.62 W. The output power ($P_{OUT}$) at full load is 5 V × 42 mA + 2 × 15 V × 32 mA, which equals 1.17 W. This result in efficiency is 72%. $V_{IN(MAX)}$ the input current is 50 mA under full load, which corresponds to 1.8 W. In this case, the efficiency is 65%.

Figure 12 shows the efficiency depending on input voltage, $V_{IN}$. Due to the post regulation with LDOs, the efficiency peak comes at $V_{IN(MIN)}$ 12 V since the voltage drop in U2 and U3 is lower than at higher $V_{IN}$. The isolating converter has a line voltage dependency with regards to its output voltage. At higher input voltages, the output voltage increases, and as a consequence the voltage also drops are larger at the LDOs. This fluctuation loses efficiency at higher input voltages. The effect could be mitigated by using a larger form-factor transformer with higher inductance and tighter coupling between primary and secondary windings. By specifying a tighter $V_{IN(MIN)}$-to-$V_{IN(MAX)}$ range, the regulation could be improved so that a smaller voltage drop at the LDOs could be used.

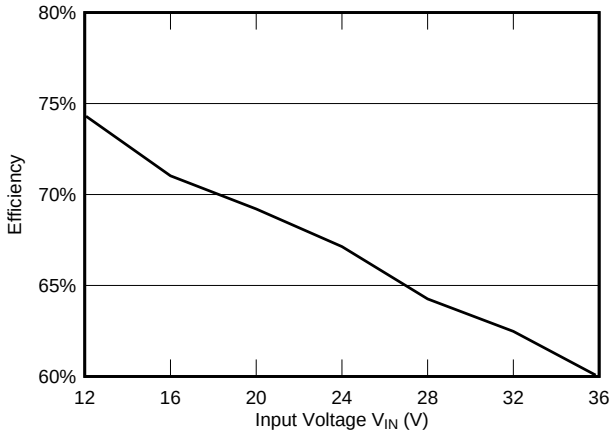


**Figure 12. Overall Efficiency versus Input Voltage**

## 7.3 Load and Line Regulation

Table 4 shows that the output voltages are not affected by different load and line conditions. This is the effect of the post regulation using precision LDOs and a high-efficiency DC/DC converter for 5 V.

## 7.4 Thermal Analysis

Figure 13, Figure 14, and Figure 15 have been captured with a FLUKE Ti40FT with 26°C. The scale in the three figures has been adjusted so the color coding matches.

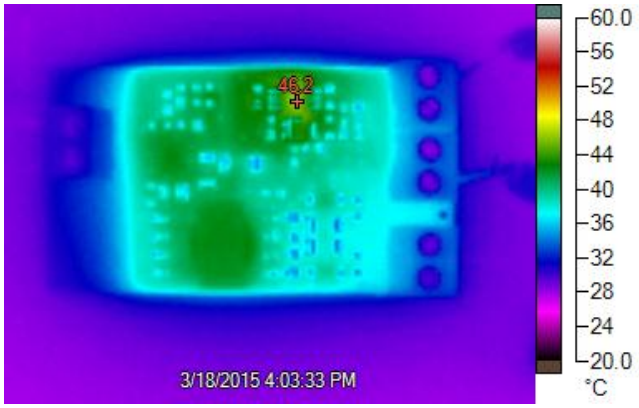


**Figure 13. TIDA-00237 Thermal Analysis Full Load $V_{IN}$ = 24 V**

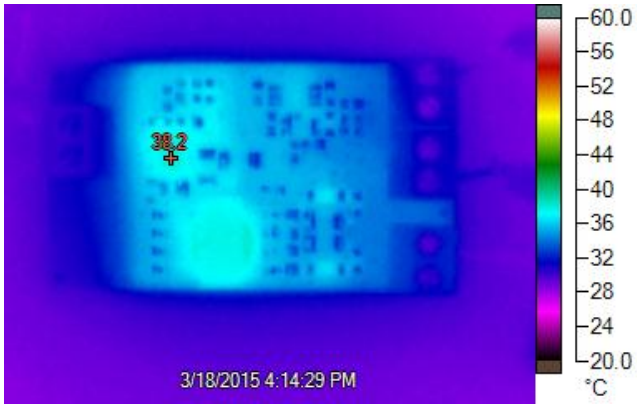


**Figure 14. TIDA-00237 Thermal Analysis Full Load, $V_{IN}$ = 12 V**

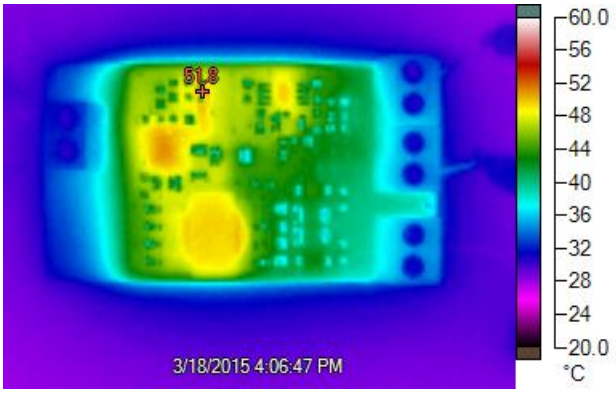


**Figure 15. TIDA-00237 Thermal Analysis Full Load, $V_{IN}$ = 36 V**

The thermal images show that under worst case conditions ($V_{IN}$ = 36 V, full load) the maximum temperature rise is still below 26°C. Because the circuit has been designed for temperatures of 125°C, operation at an ambient temperature above 85°C is feasible.

# 8 Design Files

## 8.1 Schematics

To download the schematics, see the design files at TIDA-00237.

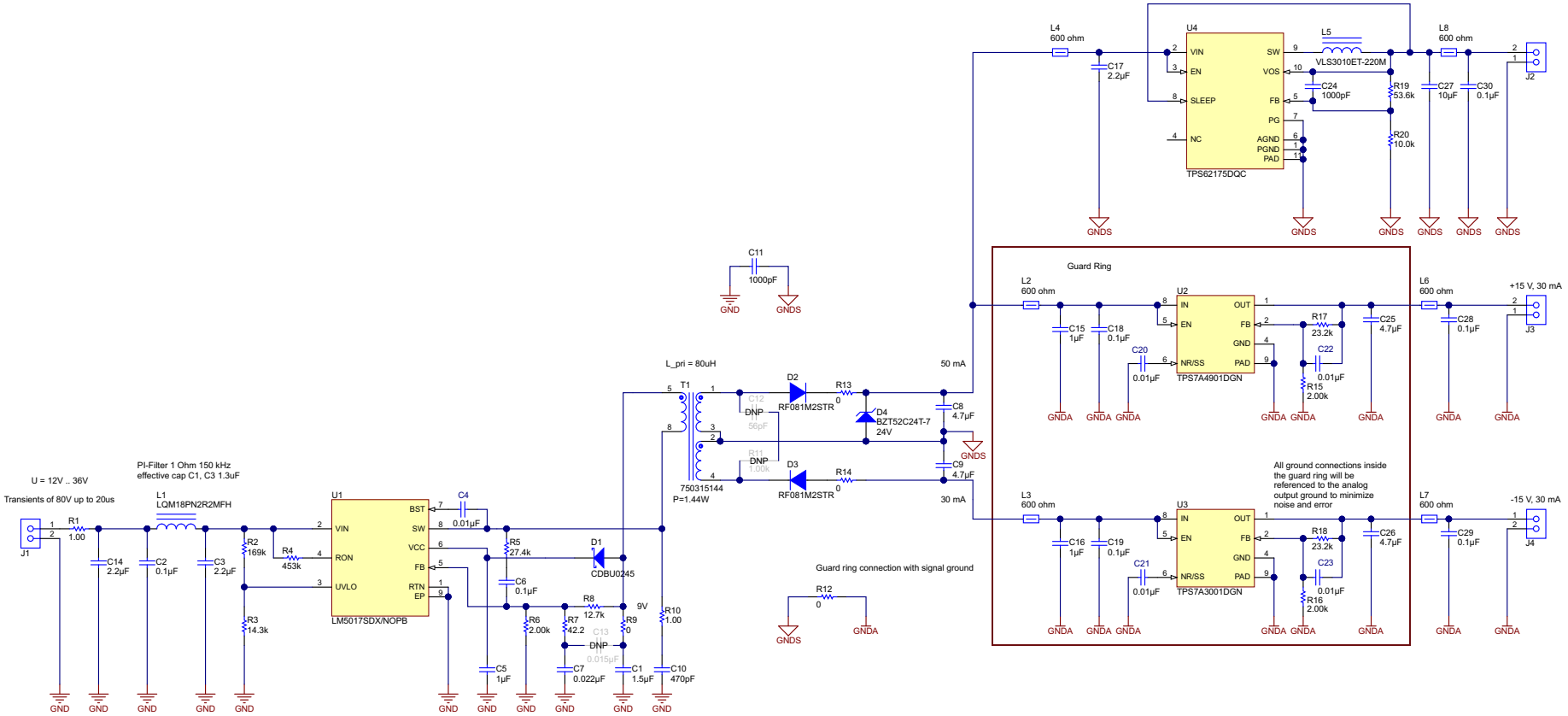


**Figure 16. TIDA-00237 Schematic**

## 8.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00237.

**Table 5. BOM**

| ITEM | QTY | REFERENCE | DESCRIPTION | MANUFACTURER | MANUFACTURER PARTNUMBER | PCB FOOTPRINT |
|---|---|---|---|---|---|---|
| 1 | 1 | C1 | CAP, CERM, 1.5 µF, 25 V, +/- 10%, X7R, 0805 | MuRata | GRM21BR71E155KA 88L | 0805 |
| 2 | 6 | C2, C18, C19, C28, C29, C30 | CAP, CERM, 0.1 µF, 50 V, +/- 10%, X7R, 0603 | TDK | C1608X7R1H104K | 0603 |
| 3 | 2 | C3, C14 | CAP, CERM, 2.2 µF, 50 V, +/- 10%, X7R, 1206 | Taiyo Yuden | UMK316B7225KD-T | 1206 |
| 4 | 5 | C4, C20, C21, C22, C23 | CAP, CERM, 0.01 µF, 50 V, +/- 5%, X7R, 0603 | Kemet | C0603C103J5RACTU | 0603 |
| 5 | 1 | C5 | CAP, CERM, 1 µF, 25 V, +/- 10%, X7R, 0603 | MuRata | GRM188R71E105KA 12D | 0603 |
| 6 | 1 | C6 | CAP, CERM, 0.1 µF, 50 V, +/- 10%, X7R, 0603 | MuRata | GCM188R71H104KA 57D | 0603 |
| 7 | 1 | C7 | CAP, CERM, 0.022 µF, 50 V, +/- 10%, X7R, 0603 | MuRata | GRM188R71H223KA 01D | 0603 |
| 8 | 2 | C8, C9 | CAP, CERM, 4.7 µF, 25 V, +/- 10%, X7R, 1206 | MuRata | GRM31CR71E475KA 88L | 1206 |
| 9 | 1 | C10 | CAP, CERM, 470 pF, 50 V, +/- 10%, X7R, 0603 | Kemet | C0603C471K5RACT U | 0603 |
| 10 | 1 | C11 | CAP, CERM, 1000 pF, 2000 V, +/- 10%, X7R, 1206_190 | Johanson Technology | 202R18W102KV4E | 1206_190 |
| 11 | 2 | C15, C16 | CAP, CERM, 1 µF, 25 V, +/- 10%, X7R, 0603_950 | Kemet | C0603C105K3RACT U | 0603_950 |
| 12 | 1 | C17 | CAP, CERM, 2.2 µF, 35 V, +/- 10%, X7R, 0805 | TDK | C2012X7R1V225K08 5AC | 0805 |
| 13 | 1 | C24 | CAP, CERM, 1000 pF, 25 V, +/- 10%, X7R, 0603 | MuRata | GRM188R71E102KA 01D | 0603 |
| 14 | 2 | C25, C26 | CAP, CERM, 4.7 µF, 25 V, +/- 10%, X7R, 1206 | TDK | C3216X7R1E475K08 5AB | 1206 |
| 15 | 1 | C27 | CAP, CERM, 10 µF, 10 V, +/- 20%, X7R, 1206 | TDK | C3216X7R1A106M08 5AC | 1206 |
| 16 | 1 | D1 | Diode, Schottky, 45 V, 0.2 A, SOD-523F | Comchip Technology | CDBU0245 | SOD-523F |
| 17 | 2 | D2, D3 | Diode, Fast Rectifier, 200 V, 0.8 A, SOD-123 | Rohm | RF081M2STR | SOD-123 |
| 18 | 1 | D4 | Diode, Zener, 24 V, 300 mW, SOD-523 | Diodes Inc. | BZT52C24T-7 | SOD-523 |
| 19 | 4 | J1, J2, J3, J4 | Conn Term Block, 2POS, 3.5mm, TH | Phoenix Contact | 1751248 | 11x8.5x7.3mm |
| 20 | 1 | L1 | Inductor, Ferrite, 2.2 µH, 0.35 A, 0.38 ohm, SMD | MuRata | LQM18PN2R2MFH | 0603 |
| 21 | 6 | L2, L3, L4, L6, L7, L8 | Ferrite Bead, 600 ohm @ 100 MHz, 1.3 A, 0603 | MuRata | BLM18KG601SN1D | 0603 |
| 22 | 1 | L5 | Inductor, Shielded, Ferrite, 22 µH, 0.38 A, 0.9 ohm, SMD | TDK | VLS3010ET-220M | Inductor, 3x1x3mm |
| 23 | 2 | R1, R10 | RES, 1.00, 1%, 0.1 W, 0603 | Vishay-Dale | CRCW06031R00FKE A | 0603 |
| 24 | 1 | R2 | RES, 169 k, 1%, 0.1 W, 0603 | Vishay-Dale | CRCW0603169KFKE A | 0603 |
| 25 | 1 | R3 | RES, 14.3 k, 1%, 0.1 W, 0603 | Vishay-Dale | CRCW060314K3FKE A | 0603 |
| 26 | 1 | R4 | RES, 453 k, 1%, 0.1 W, 0603 | Vishay-Dale | CRCW0603453KFKE A | 0603 |

**Table 5. BOM (continued)**

| ITEM | QTY | REFERENCE | DESCRIPTION | MANUFACTURER | MANUFACTURER PARTNUMBER | PCB FOOTPRINT |
|---|---|---|---|---|---|---|
| 27 | 1 | R5 | RES, 27.4 k, 1%, 0.1 W, 0603 | Vishay-Dale | CRCW060327K4FKEA | 0603 |
| 28 | 3 | R6, R15, R16 | RES, 2.00 k, 1%, 0.1 W, 0603 | Vishay-Dale | CRCW06032K00FKEA | 0603 |
| 29 | 1 | R7 | RES, 42.2, 1%, 0.1 W, 0603 | Vishay-Dale | CRCW060342R2FKEA | 0603 |
| 30 | 1 | R8 | RES, 12.7 k, 1%, 0.1 W, 0603 | Vishay-Dale | CRCW060312K7FKEA | 0603 |
| 31 | 4 | R9, R12, R13, R14 | RES, 0, 5%, 0.1 W, 0603 | Vishay-Dale | CRCW06030000Z0EA | 0603 |
| 32 | 2 | R17, R18 | RES, 23.2 k, 1%, 0.1 W, 0603 | Vishay-Dale | CRCW060323K2FKEA | 0603 |
| 33 | 1 | R19 | RES, 53.6 k, 1%, 0.1 W, 0603 | Vishay-Dale | CRCW060353K6FKEA | 0603 |
| 34 | 1 | R20 | RES, 10.0 k, 1%, 0.1 W, 0603 | Vishay-Dale | CRCW060310K0FKEA | 0603 |
| 35 | 1 | T1 | Transformer, 80 uH, SMT | Wurth Elektronik eiSos | 750315144 | SMD, Body 9.7x10mm |
| 36 | 1 | U1 | 100V, 600mA Constant On-Time Synchronous Buck Regulator, NGU0008B | Texas Instruments | LM5017SDX/NOPB | NGU0008B |
| 37 | 1 | U2 | +36V, +150mA, Ultralow-Noise, Positive LINEAR REGULATOR, DGN0008D | Texas Instruments | TPS7A4901DGN | DGN0008D |
| 38 | 1 | U3 | -36V, -200mA, Ultralow-Noise, High PSRR, Adjustable -1.18 to -33 V Output, Negative Linear Regulator, 8-pin MSOP (DGN), -40 to 125 degC, Green (RoHS & no Sb/Br) | Texas Instruments | TPS7A3001DGN | DGN0008D |
| 39 | 1 | U4 | 28V, 0.5A Step-Down Converter with Sleep Mode, DQC0010A | Texas Instruments | TPS62175DQC | DQC0010A |

## 8.3 PCB Layout Recommendations

The PCB layout is determined by contradicting requirements. The first design goal was a small form-factor design. The second design goal addresses cost. The other two goals were usability in industrial environment at ambient temperatures of up to 85°C and low EMI as well as low output voltage noise. To get a small form factor, all components have been grouped together as much as possible without violating placement rules. It was also necessary to distribute components on both sides of the PCB. The bottom side components were selected because their height is less than 1 mm. To keep the cost low, only 0603-sized or larger components are used in the design. The layout has been implemented on a two layer board with 35-µm copper. Each IC got enough copper heat sink area to provide the maximum specified power at an ambient temperature of 85˚C. The analog section got guard rings on top and bottom layers to reach the EMI and noise goal. Figure 17 shows the path of the switching current. During $t_{OFF}$ the current follows path G4 from capacitor C1 into the transformer and from there follows G1 through the synchronous switch in the LM5017 into the GND connection and back to C1. C1 acts as local power supply. Therefore, the capacitor C1 has to be located as close to the LM5017 ground connection as possible. During $t_{ON}$, the current follows path G2 through capacitor C3 into the switching transistor of the LM5017 to the transformer, then through the path G4 into C1 and through path G3 back to capacitor C3. Here, C3 acts as the local power supply and it must be located also close to the LM5017. To keep the current path G3 short and to prevent introducing switching noise into the ground path C3 must also be located close to C1. The layout shows as an example how to achieve both requirements. Heat from LM5017 is dissipated through both of the layers, bottom, and top.

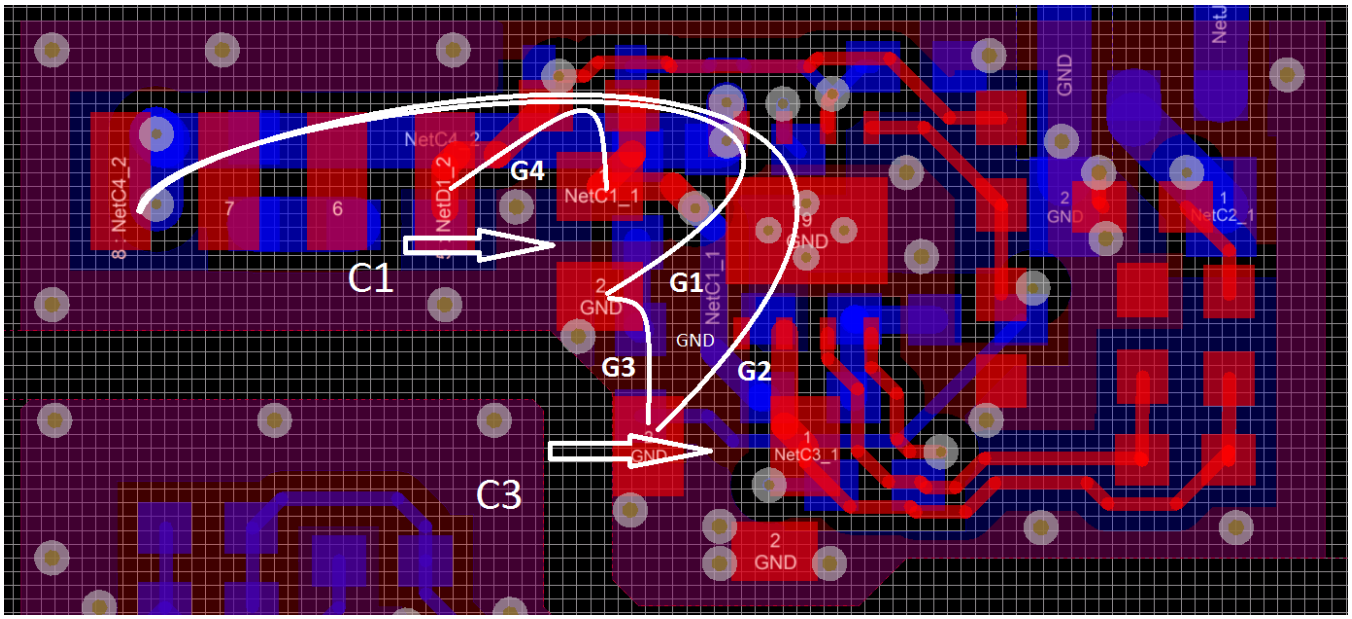


**Figure 17. Isolating Converter Primary Side**

Figure 18 shows the critical parts of the layout for the secondary side. To provide already good filtering of the unregulated voltage the current loops shown by ellipses G8 and G9 are kept as small as possible. The rectified and filtered supply is guided through a strong ground reference to the guard rings of the analog section. They enter the ring through EMI filter ferrites into a filter capacitor. The layout inside the guard ring is then only critical in terms of heat distribution. A symmetric layout on top and bottom layers for positive and negative analog supply made it easy to achieve cooling on top and bottom layers.

The guard ring and the ground plane of the switching side are separated as indicated with graph G5. The only connection is through zero-Ω R12 close and parallel to both the positive and negative supply voltages. Keep the ground of the analog supply and the digital supply separate if the supplied analog allows for separation. The analog supply section is referenced to its ground output, thus eliminating switching noise all together.

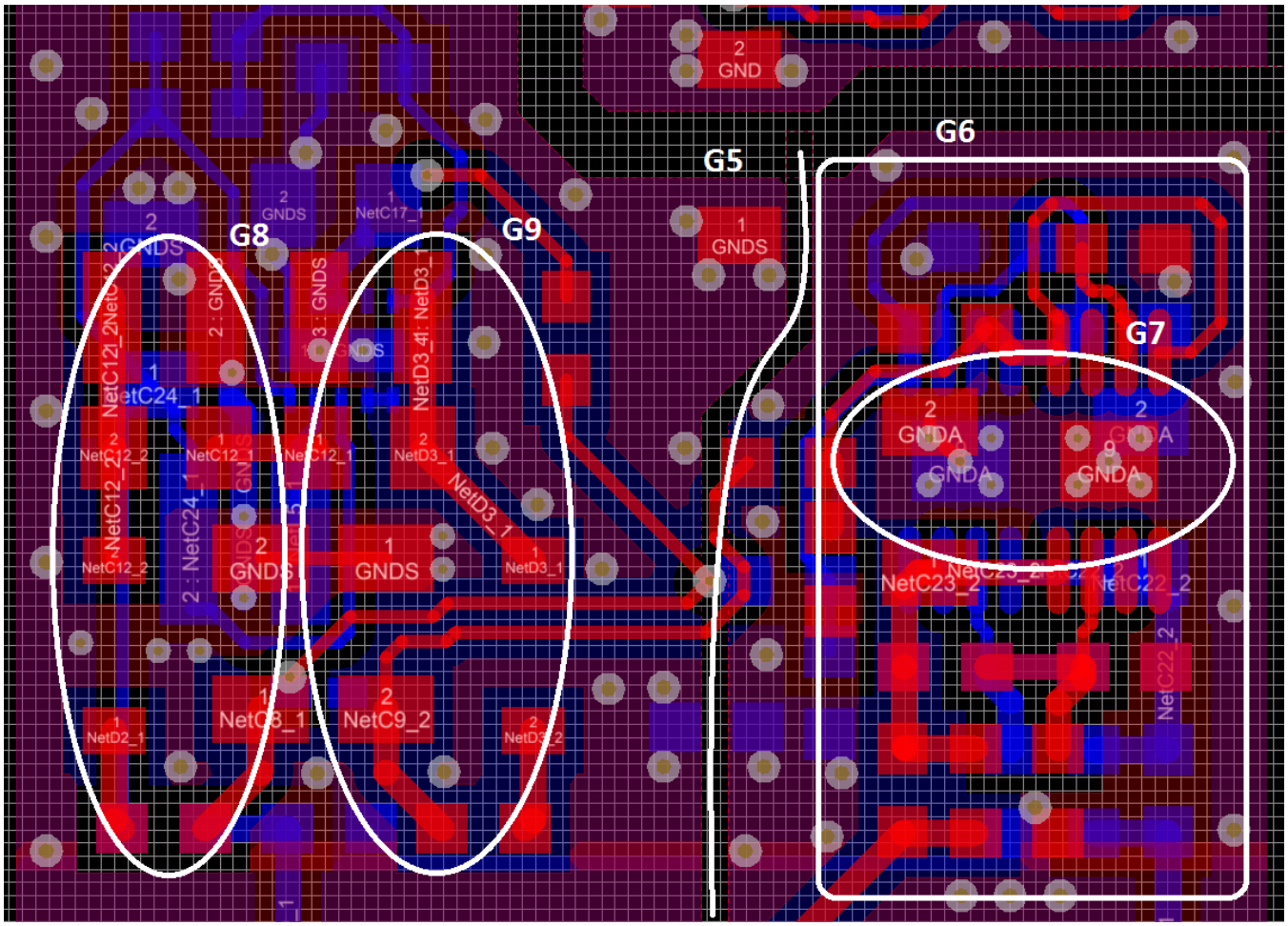


**Figure 18. Secondary Side and Analog**

### 8.3.1 Layer Plots

To download the layer plots, see the design files at TIDA-00237.

**NOTE:** All layer plots are viewed from the top.

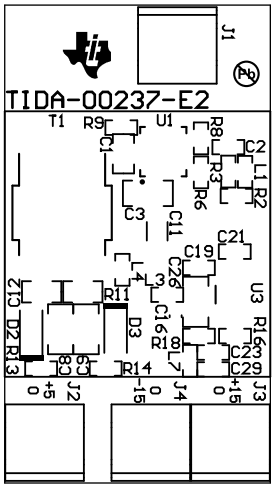


**Figure 19. Top Overlay**

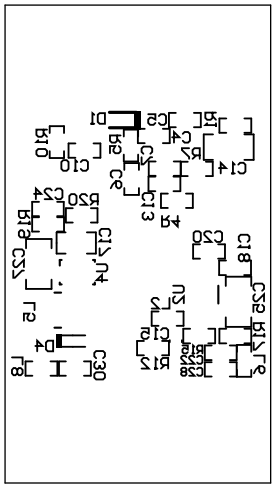

**Figure 20. Bottom Overlay**

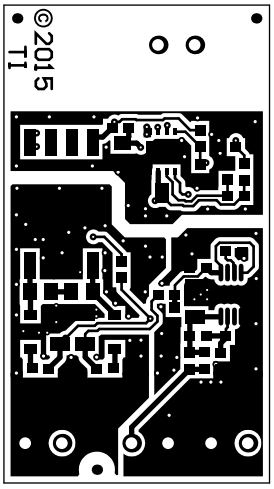


**Figure 21. Top Layer**

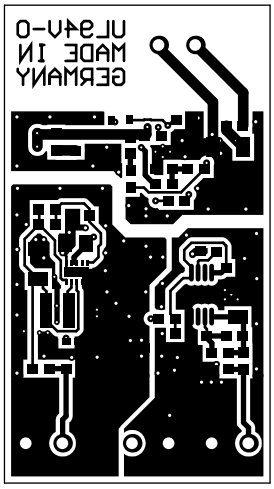


**Figure 22. Bottom Layer**

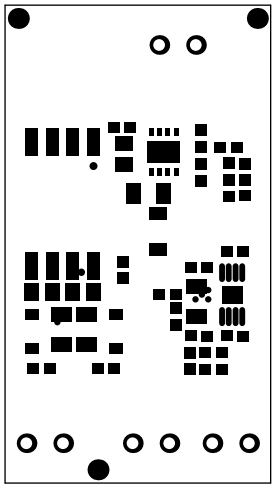

**Figure 23. Top Solder**

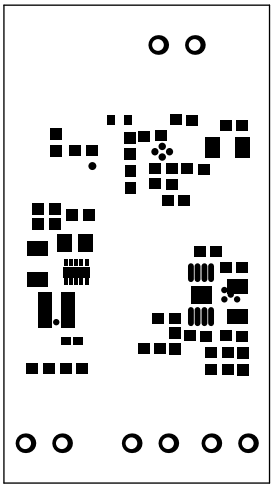

**Figure 24. Bottom Solder**

## 8.4 Altium Project

To download the Altium project files for each board, see the design files at TIDA-00237.

## 8.5 Gerber Files

To download the Gerber files for each board, see the design files at TIDA-00237.

## 9 References

1. Texas Instruments, *1-W Small Form Factor Power Supply with Isolated Dual Output for PLC I/O Modules*, TIDA-00129 Design Guide (TIDU263)
2. Texas Instruments, *AN-2292 Designing an Isolated Buck (Flybuck) Converter*, Application Note (SNVA674)

## 10 About the Author

**INGOLF FRANK** is a systems engineer in the Texas Instruments Factory Automation and Control Team, focusing on PLC I/O modules. Ingolf works across multiple product families and technologies to leverage the best solutions possible for system level application design. Ingolf earned his electrical engineering degree (Dipl. Ing. (FH)) in the field of information technology at the University of Applied Sciences Bielefeld, Germany in 1991.

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