TI Designs

25-W, 88% Efficiency, Multiple Isolated Output, Auxiliary Supply Reference Design for AC-DC Power Supply

TI Designs

This design is a 25-W, multiple output, auxiliary power supply designed for use in power converters targeted for server, telecom, and industrial system applications. This solution is a multiple output flyback converter implemented using the UCC28700 to provide constant-voltage (CV) and constant-current (CC) output regulation and uses quasi-resonant valley-switching to achieve higher efficiency. The design is compact and affordable due to minimal component count with all the necessary built-in protections such as output overcurrent and output short circuit. Hardware is designed and tested to pass EFT requirements and aids to meet low power efficiency performance of the Department of Energy (DoE) Level VI standards. Additionally, the design has a built-in eFuse for fault isolation on the 12-V main rail without affecting any other output.

Design Resources

TIDA-00706	Design Folder
UCC28700	Product Folder
TPS259241	Product Folder

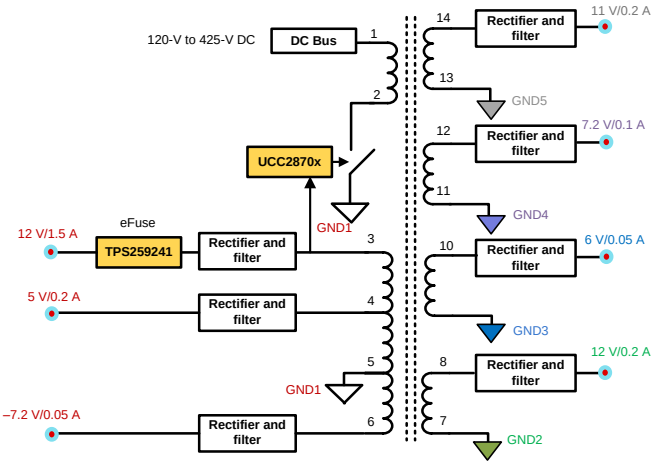
TI E2E™ Community — ASK Our E2E Experts

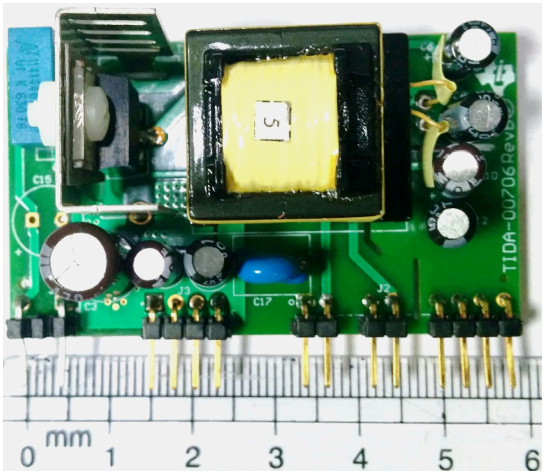
Design Features

- High Average Efficiency of 83.8% at 400-V DC and 87.2% at 165-V DC to Meet DoE Level VI and EU CoC Tier-2 Energy Efficiency Norms
- Peak Efficiency of ~86% at 400-V DC and ~88% at 165-V DC at Full Load
- Low Standby Power (< 100 mW) to Help Meet No-Load Condition Limits of Multiple Energy Norms (DoE Level VI and EU CoC Tier-2)
- Wide Input Voltage Range From 120-V to 425-V DC to Power Universal Input AC-DC Converters
- Multiple Outputs: –7.2, 5, and 12 V and Isolated 6, 7.2, 11, and 12 V to Address All System Rails in One Unit
- Robust Supply Protected for Input Brownout, Output Overcurrent, Short-Circuit, and Output Overvoltage Conditions
- Compact Form-Factor (35 mm × 60 mm) to Achieve High-Power Density Solutions

Featured Applications

- Auxiliary Unit for AC-DC Power Converters
- Server Power Supply
- Telecom Rectifiers
- UPS and Industrial Power Supplies
- Battery Chargers





1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	TEST CONDITIONS		MIN	NOM	MAX	UNIT
INPUT CONDITIONS						
Input voltage (V_{INDC})	–		120	325	425	VDC
No load power (P_{NL})	V_{INDC} = 400 V, I_{OUT} = 0 A		–	0.1	–	W
Brownout voltage (V_{IN_UVLO})	–		–	70	–	V
OUTPUT CONDITIONS						
Output voltage 1 (non-isolated)	–		11.4	12	12.6	V
Output current 1	–		–	–	1.5	A
Output voltage 2 (non-isolated)	–		4.8	5	5.6	V
Output current 2	–		–	–	0.2	A
Output voltage 3 (non-isolated)	–		–7.8	–7.2	–7	V
Output current 3	–		–	–	0.05	A
Output voltage 4 (isolated)	–		12	12.5	13.5	V
Output current 4	–		–	–	0.2	A
Output voltage 5 (isolated)	–		6.8	7	7.8	V
Output current 5	–		–	–	0.05	A
Output voltage 6 (isolated)	–		7	7.2	7.5	V
Output current 6	–		–	–	0.1	A
Output voltage 7 (isolated)	–		10.5	11	11.8	V
Output current 7	–		–	–	0.2	A
Line regulation	At full load V_{IN}: 120-V to 425-V DC	12 V	–0.2	–	0.2	%
		5 V	–0.2	–	0.2	
		–7.2 V	–0.2	–	0.2	
		12 V_ISO	–0.2	–	0.2	
		6 V_ISO	–1.5	–	1.5	
		7.2 V_ISO	–0.2	–	0.2	
		11 V_ISO	–1	–	1	
Load regulation	V_{IN}: 120-V to 425-V DC Load: 10% to 100%	12 V	–0.4	–	0.4	%
		5 V	–0.9	–	0.9	
		–7.2 V	–0.6	–	0.6	
		12 V_ISO	–0.5	–	0.5	
		6 V_ISO	–1	–	1	
		7.2 V_ISO	–2	–	2	
		11 V_ISO	–0.5	–	0.5	
Output voltage ripple	At full load	12 V	–	–	500	mV
		5 V	–	–	600	
		–7.2 V	–	–	500	
		12 V_ISO	–	–	500	
		6 V_ISO	–	–	500	
		7.2 V_ISO	–	–	500	
		11 V_ISO	–	–	400	
Output power	–		–	25	27	W
Primary to secondary insulation	–		–	3.75	–	kV

Table 2. System Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Efficiency (η)	V_{IN} = V_{NOM} I_{OUT} = 25%, 50%, 75%, and 100% full load	80.7	–	88.1	%
Protections	Output overvoltage				
	Input undervoltage				
	Overcurrent				
	Short-circuit and power limit				
	Open loop protection				
Operating ambient	Open frame	–40	25	60	°C
EFT	–	As per IEC 61000-4-4			–
Dimensions	Length × Breadth × Height	35 × 60 × 17			mm

2 System Description

High-power converters used in server, telecom, and industrial systems need auxiliary power supplies to support house-keeping needs of the power supply unit (PSU). An auxiliary power supply is commonly used to power the internal control electronics and voltage and current feedback sensing electronics of the PSU. It is an isolated DC-DC converter generating multiple isolated outputs to power primary and secondary side control devices. The typical usage of auxiliary power supply is shown in Figure 1. The number of isolated rails needed vary from simple two outputs to as high as six to seven outputs based on the isolated current sense circuitry, isolated intra-communication, intra-communication between subsystems of the PSU, and isolated external communication between multiple PSUs.

The auxiliary power supplies are independent isolated DC-DC converters as power converters have an EMI filter, a diode-bridge rectifier, and a bulk capacitor present in the system, generating a rectified DC bus. These supplies operate over a wide input range from 100-V to 450-V DC and keep system electronics powered under all conditions to detect faults such as undervoltage, overvoltage, and overcurrent. Typically, auxiliary power supplies generate multiple outputs delivering a power from 5 to 30 W; based on the configuration of the power supply, such as high wattage, > 12 W is needed to power internal fans.

These supplies need to have very low standby power to meet the stringent norms such as the Department of Energy (DoE) and Code of Conduct (CoC). In addition, these need to have high efficiency from 10% load to 100% loads, ensuring low system power loss under all operating conditions.

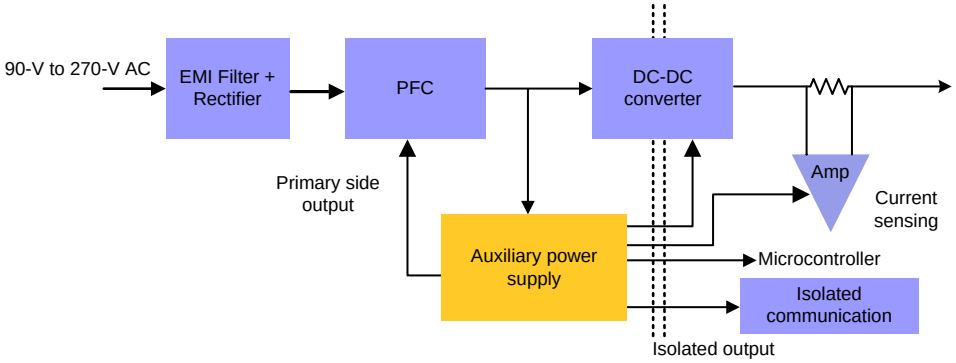


Figure 1. Typical Block Diagram of Server, Telecom, and Industrial Power Supply

This reference design is a 25-W auxiliary power supply, designed specifically to meet very low standby power needs of < 100 mW, high efficiency of > 80% for a wide load range from 20% to 100%, and over entire input operating voltage range. This reference design is a simple, low component, low cost primary side regulated (PSR) flyback converter implemented using the device UCC28700 that regulates constant-voltage (CV) and constant-current (CC) output and uses quasi-resonant valley switching for higher efficiency. The design operates over wide input range of 120-V to 425-V DC, delivering a total power of 25 W from seven outputs (12 V, 5 V, –7.2 V, 11 V_ISO, 7.2 V_ISO, 6 V_ISO, and 12 V_ISO).

This TI Design meets the key challenges of the auxiliary power supply to provide safe and reliable power while delivering high performance with low power consumption and low bill-of-material (BOM) cost.

3 Block Diagram

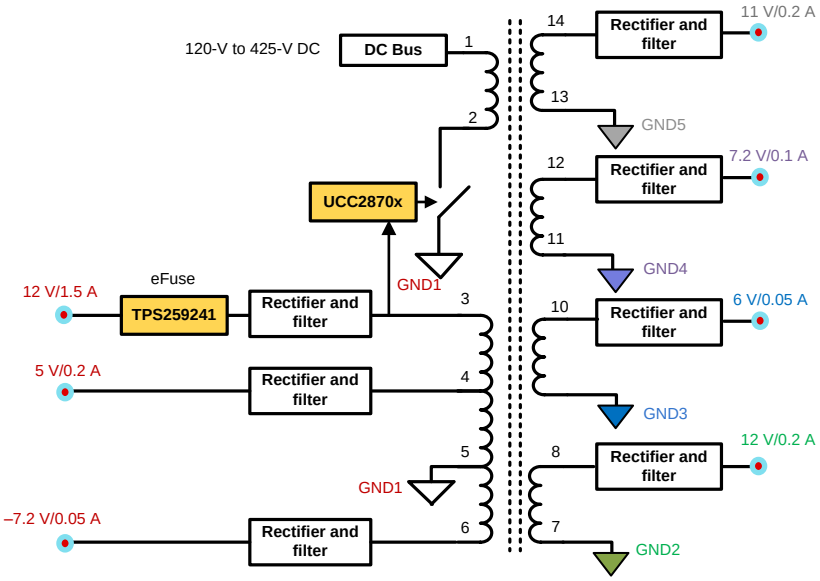


Figure 2. Block Diagram of 25-W Auxiliary Power Supply

3.1 Highlighted Products and Key Advantages

This section highlights the key features for selecting the devices for this reference design. Find the complete details of the highlighted devices in their respective product datasheets.

3.1.1 UCC28700 CV-CC Controller With PSR

The UCC28700 flyback power supply controller provides CV and CC output regulation without the use of an optical coupler. The device processes information from the primary power switch and an auxiliary flyback winding for precise control of output voltage and current. Its low start-up current, dynamically controlled operating states, and a tailored modulation profile support very low standby power without sacrificing start-up time or output transient response. Control algorithms in the UCC28700 allow operating efficiencies to meet or exceed applicable standards. The output drive interfaces to a MOSFET power switch. Discontinuous conduction mode (DCM) with valley switching reduces switching losses. Modulating the switching frequency and primary current peak amplitude (FM and AM) keeps the conversion efficiency high across the entire load and line ranges. The controller has a maximum switching frequency of 130 kHz and always maintains control of the peak-primary current in the transformer. Protection features help keep primary and secondary component stresses in check. Key features that make this device unique are:

- <30-mW no-load power for five-star rating
- PSR eliminates optocoupler
- ±5% voltage and current regulation
- 130-kHz maximum switching frequency enables high-power density designs
- Quasi-resonant (QR) valley-switching operation for highest overall efficiency
- Wide VDD range allows small bias capacitor
- Clamped gate drive output for MOSFET
- Protection functions: overvoltage, low-line, and overcurrent

3.1.2 TPS259241 12-V eFuse With Overvoltage Protection and Blocking FET Control

The TPS259241 eFuse is a highly integrated circuit protection and power management solution in a tiny package. The device uses few external components and provide multiple protection modes. The TPS259241 is a robust defense against overloads, shorts circuits, voltage surges, excessive inrush current, and reverse current.

The current limit level can be set with a single external resistor. Overvoltage events are limited by internal clamping circuits to a safe fixed maximum with no external components required.

Key features that make this device unique are:

- $V_{OPERATING}$ = 4.5 to 13.8 V, V_{ABSMAX} = 20 V
- Integrated 28-mΩ pass MOSFET
- Fixed 15-V overvoltage clamp
- 1- to 5-A adjustable I_{LIMIT}
- ±8% I_{LIMIT} accuracy at 3.7 A
- Reverse current blocking support
- Programmable OUT slew rate, UVLO
- Built-in thermal shutdown
- Safe during single-point failure test (UL60950)
- Small footprint: 10L (3×3-mm) VSON

4 System Design Theory

This reference design provides 25 W of continuous power over a wide DC input range from 120-V to 425-V DC. The design has a flyback power stage implemented using the UCC28700 QR PSR CC-CV flyback controller to deliver seven outputs, three outputs referred to the primary ground of the transformer, and four completely isolated outputs. In total, there are four isolated grounds. The system efficiency is around 88% with a 165-V DC input and around 86% with a 400-V DC input under full load conditions. In addition, several protections are embedded into this design, which includes input under voltage protection and output short-circuit protection.

Overall, the main focus of this design is to achieve high efficiency and very low standby power to meet 80Plus (Titanium) standard for server PSU, DoE Level VI, and EU CoC Tier-2 norms in compact form-factor to address high power density converters.

4.1 QR Flyback Converter With PSR

Flyback converters provide a cost effective solution for DC-DC conversion needs. They are widely used for DC-DC converters up to 150 W. There are three modes of operation, namely discontinuous mode (DCM), QR mode, and continuous conduction mode (CCM). For lower power applications, DCM or QR mode is preferred as they have reduced power losses and optimal peak currents in low power applications. As the output wattage increases, the CCM becomes more efficient due to the reduced peak and RMS currents.

Flyback converters designed with PSR flyback controllers eliminate the use of conventional optocoupler-based feedback. The PSR flyback controllers sense the voltage feedback through auxiliary winding and current feedback through current sense resistor used in series with switching FET. In addition PSR flyback controllers provide wide range of protections and accurate limiting of both current and power. The UCC28700 controller has PSR feedback eliminating opto-feedback, thus reducing the component count.

4.2 Flyback Circuit Component Design

The UCC28700 is a flyback power supply controller that provides accurate CV and CC regulation with primary-side feedback, eliminating the need for optocoupler feedback circuits. The controller operates in DCM with valley switching to minimize switching losses. The modulation scheme is a combination of frequency and primary peak current modulation to provide high conversation efficiency across the load range.

This design guide illustrates the process and component selection for this design. All design calculations are available in "TIDA-00706_Design_Calculator" (TIDCBW1).

4.2.1 Design Goal Parameters

Table 3 lists the design goal parameters for this design. These parameters are used in further calculations to select components.

Table 3. Design Goal Parameters

PARAMETER		MIN	TYP	MAX	UNIT
INPUT					
V_{IN}	Input voltage	120.0	325.0	425.0	VDC
OUTPUT					
V_{OUT_1}	Output voltage (non-isolated)	11.4	12.0	12.6	VDC
I_{OUT_1}	Output current (non-isolated)	–	1.5	–	A
V_{OUT_2}	Output voltage (non-isolated)	4.8	5.0	5.6	VDC
I_{OUT_2}	Output current (non-isolated)	–	0.2	–	A
V_{OUT_3}	Output voltage (non-isolated)	–7.8	–7.2	–7.0	VDC
I_{OUT_3}	Output current (non-isolated)	–	0.05	–	A
V_{OUT_4}	Output voltage (isolated)	12.0	12.5	13.5	VDC
I_{OUT_4}	Output current (isolated)	–	0.2	–	A
V_{OUT_5}	Output voltage (isolated)	6.8	7.0	7.8	VDC
I_{OUT_5}	Output current (isolated)	–	0.05	–	A
V_{OUT_6}	Output voltage (isolated)	7.0	7.2	7.5	VDC
I_{OUT_6}	Output current (isolated)	–	0.1	–	A
V_{OUT_7}	Output voltage (isolated)	10.5	11.0	11.8	VDC
I_{OUT_7}	Output current (isolated)	–	0.2	–	VDC
P_{OUT}	Output power	–	25.0	–	W
	Line regulation (165-V to 400-V DC)	–	–	< 2%	–
	Load regulation (10% to 100% load)	–	–	< 2%	–
F_{MAX}	Maximum desired switching frequency	–	–	120.0	kHz
η	Targeted efficiency	–	86%	–	–

As stated in Table 3, 12-V/1.5-A winding is the main winding that has been used for feedback and the design of transformer parameters.

4.2.2 Transformer Parameter Calculations: Turns Ratio, Primary Inductance, and Peak Primary Current

The target maximum switching frequency at full-load, the minimum input capacitor bulk voltage, and the estimated DCM QR time determine the maximum primary-to-secondary turns-ratio of the transformer.

Initially determine the maximum available duty cycle and secondary conduction time based on target switching frequency and DCM resonant time. For DCM resonant time, assume 500 kHz if there is no estimate from previous designs. To limit the operation to transition mode, the period required from the end of secondary current conduction to the first valley of the V_{DS} voltage is ½ of the DCM resonant period, or 1 µs assuming a 500-kHz resonant frequency. D_{MAX} can be determined using Equation 1.

$$D_{MAX} = 1 - \left(\frac{T_R}{2} \times F_{MAX} \right) - D_{MAGCC} \tag{1}$$

where

- T_R is the estimated period of the LC resonant frequency at the switch node
- DM_{AGCC} is defined as the secondary-diode conduction duty cycle during CC operation and is fixed internally by the UCC28700 at 0.425.

$$T_R = 2\ \mu s$$

$$D_{MAX} = 1 - 120\ kHz \times \frac{2\ \mu s}{2} - 0.425 = 0.455$$

To make sure the operation of the flyback converter is always in DCM, the value chosen for D_{MAX} for further calculation must be lesser than 0.455. For this design, the value used for D_{MAX} is 0.445.

When D_{MAX} is known, the maximum primary-to-secondary turns ratio is determined with Equation 2. The total voltage on the secondary winding must be determined, which is the sum of V_{OCV}, V_F, and V_{OCBC}.

$$N_{PS(max)} = \frac{D_{MAX} \times V_{DC(min)}}{D_{MAGCC} \times \left(V_{OCV} + V_F + V_{OCBC} \right)} \tag{2}$$

where

- V_{OCBC} is the additional voltage drop of post filter inductor and any other target cable-compensation voltage added to V_{OCV} (provided by an external adjustment circuit applied to the shunt regulator). Set this variable equal to 0 V if not used.

$$N_{PS(max)} = \frac{0.445 \times 120\ V}{0.425 \times (12\ V + 0.5\ V)} = 10.05$$

With this value of N_{PS}, the reflected voltage is:

$$V_{REF} = (V_{OUT} + V_F) \times N_{PS} = (12 + 0.5) \times 10.05 = 125.625\ V \tag{3}$$

However, the desired value of reflected voltage must not exceed 100 V to keep V_{DS} of MOSFET within safe limits for wide input range such as 425-V DC. Thus, the chosen value of N_{PS} is 8 for this design. The transformer turns ratio selected affects the MOSFET V_{DS} and secondary rectifier reverse voltage, so review these variables before moving forward.

The UCC28700 controller requires a minimum on time of the MOSFET ($T_{ON(min)}$) and minimum secondary rectifier conduction time ($T_{DMAG(min)}$) in the high line and minimum load condition. The selection of F_{MAX}, L_P, and R_{CS} affects the minimum $T_{ON(min)}$ and $T_{DMAG(min)}$.

Determine the secondary rectifier and MOSFET voltage stress with Equation 4 and Equation 5.

$$V_{REV} = \frac{V_{IN(max)}}{N_{PS}} + V_{OCV} + V_{OCBC} \tag{4}$$

For the MOSFET V_{DS} voltage stress, include an estimated leakage inductance voltage spike (V_{LK}).

$$V_{DSPK} = V_{IN(max)} + \left(V_{OCV} + V_{OCBC} + V_F \right) \times N_{PS} + V_{LK} \tag{5}$$

Equation 6 determines if $T_{ON(min)}$ exceeds the minimum T_{ON} target of 300 ns. Equation 7 verifies that $T_{DMAG(min)}$ exceeds the minimum T_{DMAG} target of 1.1 µs.

$$T_{ON(min)} = \frac{L_P}{V_{IN(max)}} \times \frac{I_{PP(max)} \times V_{CST(min)}}{V_{CST(max)}} \quad (6)$$

$$T_{DMAG(min)} = \frac{T_{ON(min)} \times V_{IN(max)}}{N_{PS} \times \left(V_{OCV} + V_F\right)} \quad (7)$$

To determine the optimum turns ratio (N_{PS}), design iterations are generally necessary to optimize and evaluate system-level performance trade-offs and parameters mentioned in Equation 4 to Equation 7. The design spreadsheet (TIDCBW1) provides easy way to perform the iterations and arrive at optimum value for NPS.

When the optimum turns ratio (N_{PS}) is determined from a detailed transformer design, use this ratio for the following parameters.

The UCC28700 controller CC regulation is achieved by maintaining a maximum D_{MAG} duty cycle of 0.425 at the maximum primary current setting. The transformer turns ratio and CC regulating voltage determine the current sense resistor for a target output current as seen in Equation 8.

$$R_{CS} = \frac{V_{CCR} \times N_{PS}}{2 \times I_{OCC}} \times \eta_{XFMR} \quad (8)$$

where

- V_{CCR} is the CC regulating level given as 0.319 V in the UCC28700 datasheet (SLUSB41)
- I_{OCC} is the converter output CC target, which is around 2 A for this design
- η_{XFMR} is the estimated efficiency of transformer

Since a small portion of the energy stored in the transformer does not transfer to the output, a transformer efficiency term is included in Equation 8. This efficiency number includes the core and winding losses, the leakage-inductance ratio, and a bias-power-to-maximum-output-power ratio. For example, an overall-transformer efficiency of 0.9 is a good estimate based on 3.5% leakage inductance, 5% core and winding loss, and 0.5% bias power. Adjust these estimates as appropriate based on each specific application.

$$R_{CS} = \frac{0.319\ V \times 8 \times 0.9}{2 \times 2\ A} = 0.5742\ \Omega$$

Standard value of current sense resistor selected is R_{CS} = 0.6 Ω; A parallel resistor to R_{CS} is added in the schematic to adjust its value easily.

To calculate primary inductance, first determine the primary peak current of the transformer using Equation 10. The peak primary current must not exceed the maximum allowed limit calculated by Equation 9.

$$I_{PP(max)} = \frac{V_{CST(max)}}{R_{CS}} = \frac{0.775\ V}{0.6\ \Omega} = 1.29\ A \quad (9)$$

$$I_{PP(nom)} = \frac{P_{OUT} \times 2}{\eta \times V_{IN(min)} \times D_{max}} = \frac{25\ W \times 2}{0.86 \times 120\ V \times 0.455} = 1.065\ A \quad (10)$$

The actual value of primary peak current chosen for the transformer design is 1.06 A, which is clear by the design spreadsheet.

Calculate the primary transformer inductance using the standard energy storage equation for flyback transformers. The primary current, maximum switching frequency, output voltage, and transformer power losses are included in Equation 11.

$$L_P = \frac{2 \times \left(V_{OCV} + V_F + V_{OCBC}\right) \times I_{OCC}}{\eta_{XFMR} \times I_{PP(nom)}^2 \times f_{MAX}} = \frac{2 \times (12\,V + 0.5\,V + 0\,V) \times 2}{0.9 \times 1.06\,A^2 \times 120\ kHz} = 412.035\ \mu H \quad (11)$$

The actual primary inductance selected is L_P = 410 µH.

This design uses the main 12-V/5-A rail for feedback and the same winding also serves the purpose of auxiliary winding. Therefore, it is not necessary to calculate the auxiliary winding transformer turns ratio (N_{AS}) separately. The value of N_{PS1} (= 8) is used for any calculation involving auxiliary winding transformer turns ratio.

4.2.3 Transformer Parameter Calculations: Primary and Secondary RMS Currents

The transformer primary RMS current (I_{PRMS}) is calculated using Equation 12.

$$I_{PRMS} = I_{PP(nom)} \times \sqrt{\frac{D_{MAX}}{3}} = 1.06\ A \times \sqrt{\frac{0.445}{3}} = 0.408\ A \quad (12)$$

Calculate the transformer secondary peak currents and RMS currents using Equation 13 and Equation 14, respectively.

$$I_{SPK1} = \frac{2 \times P_{OUT1}}{V_{OUT1} \times D_{MAG}} \quad (13)$$

$$I_{SRMS1} = I_{SPK1} \times \sqrt{\frac{D_{MAG}}{3}} \quad (14)$$

For the 12-V/16-W output, the value of secondary peak and RMS currents are:

$$I_{SPK1} = \frac{2 \times 8}{12 \times 0.425} = 7.0588\ A$$

$$I_{SRMS1} = 7.0588 \times \sqrt{\frac{0.425}{3}} = 2.656\ A$$

For the 5-V/1-W output, the value of secondary peak and RMS currents are:

$$I_{SPK2} = \frac{2 \times 1}{5 \times 0.425} = 0.941\ A$$

$$I_{SRMS2} = 0.941 \times \sqrt{\frac{0.425}{3}} = 0.354\ A$$

For the –7.2-V/0.36-W output, the value of secondary peak and RMS currents are:

$$I_{SPK3} = \frac{2 \times 0.36}{7.2 \times 0.425} = 0.235\ A$$

$$I_{SRMS3} = 0.235 \times \sqrt{\frac{0.425}{3}} = 0.0886\ A$$

For the 12-V/2.4-W output, the value of secondary peak and RMS currents are:

$$I_{SPK4} = \frac{2 \times 2.4}{12 \times 0.425} = 0.941\ A$$

$$I_{SRMS4} = 0.941 \times \sqrt{\frac{0.425}{3}} = 0.354\ A$$

For the 6-V/0.3-W output, the value of secondary peak and RMS currents are:

$$I_{SPK5} = \frac{2 \times 0.3}{6 \times 0.425} = 0.235\ A$$

$$I_{SRMS5} = 0.235 \times \sqrt{\frac{0.425}{3}} = 0.0886\ A$$

For the 7.2-V/0.72-W output, the value of secondary peak and RMS currents are:

$$I_{SPK6} = \frac{2 \times 0.72}{7.2 \times 0.425} = 0.471\ A$$

$$I_{SRMS6} = 0.471 \times \sqrt{\frac{0.425}{3}} = 0.177\ A$$

For the 11-V/2.2-W output, the value of secondary peak and RMS currents are:

$$I_{SPK7} = \frac{2 \times 2.2}{11 \times 0.425} = 0.941\ A$$

$$I_{SRMS7} = 0.941 \times \sqrt{\frac{0.425}{3}} = 0.354\ A$$

Based on these calculations, a Würth Elektronik transformer was designed for this application, part number 750343154, which has the following specifications:

- N_{PS1} = 8; N_{PS2} = 18.67; N_{PS3} = 14; N_{PS4} = 8; N_{PS5} = 14; N_{PS6} = 14; N_{PS7} = 9.33
- L_P = 410 µH
- L_{LK} = 7 µH (primary leakage inductance)

4.2.4 Main Switching Power MOSFET Selection

The drain-to-source RMS current, I_{DS_RMS}, through the switching FET is same as the transformer primary RMS current as calculated earlier using Equation 12. Select a MOSFET with five times the I_{DS_RMS} calculated.

The maximum voltage across the FET can be estimated using Equation 5. Considering a de-rating of 25%, the voltage rating of the MOSFET must be 650-V DC.

AOTF7S65L MOSFET of 650 V and 7 A at 25°C is selected for current design because of its very low C_{OSS} and Q_g.

Calculate the recommended clamping voltage on drain with Equation 15.

$$V_{DRAIN\_CLAMP} = 0.95 \times V_{DS} - \left(V_{IN(max)} + N_{PS} \times \left(V_{OCV} + V_F + V_{OCBC}\right)\right) \quad (15)$$

$$V_{DRAIN\_CLAMP} = 0.95 \times 650\ V - \left(425\ V + 8 \times \left(12.5\ V\right)\right) = 92.5\ V$$

4.2.5 Rectifying Diode Selection

Calculate the secondary output diode reverse voltage or blocking voltage needed ($V_{DIODE\_BLOCKING}$) using Equation 16.

$$V_{DIODE\_BLOCKING} = \frac{V_{IN(max)}}{N_{PS}} + V_{OUT\_OVP} + V_{OCBC} + V_F \quad (16)$$

For 12-V and 12-V_ISO output rails, calculate the blocking voltage for diode as follows:

$$V_{DIODE\_BLOCKING} = \frac{425\ V}{8} + 12\ V + 0\ V + 0.5 = 65.625\ V$$

For –7.2-V and 7.2-V_ISO output rails, calculate the blocking voltage for diode as follows:

$$V_{DIODE\_BLOCKING} = \frac{425\ V}{14} + 7.2\ V + 0\ V + 0.5 = 38.057\ V$$

Blocking voltages of the rectifier diode for 5 V, 11 V_ISO, and 6 V_ISO are also calculated in a similar way. The calculated values of the reverse blocking voltage are 28.27 V for a 5-V output, 57.052 V for an 11-V_ISO output, and 36.86 V for a 6-V_ISO output.

A 100-V, 12-A, TO-277 package Schottky diode was used for the 12-V/1.5-A rail while a 100-V, 2-A Schottky diode was chosen for all the other six outputs. A high current rated and cost optimized diode is selected to minimize the forward drop of diode and hence reduce power loss.

4.2.6 Select Output Capacitors

For this design, the output capacitor (C_{OUT}) was selected to have a 1% ripple of all the outputs with an operating frequency of 120 kHz. Calculate the value of the output capacitors for all seven outputs using Equation 17 and Equation 18.

$$C_{OUTx} \gg \frac{I_{OUT}}{f \times V_{RIPPLE}} \tag{17}$$

$$I_{COUTx\_RMS} = \sqrt{\left(I_{RMSx}\right)^2 - \left(I_{OUTx}\right)^2} \tag{18}$$

$$C_{OUT1} \gg \frac{1.5\ A}{120\ kHz \times 0.12\ V} = 104.17\ \mu F$$

$$I_{COUT1\_RMS} = \sqrt{(2.656)^2 - (1.5)^2} = 2.193\ A$$

$$C_{OUT2} \gg \frac{0.2\ A}{120\ kHz \times 0.05\ V} = 33.33\ \mu F$$

$$I_{COUT2\_RMS} = \sqrt{(0.354)^2 - (0.2)^2} = 0.292\ A$$

The same equations are used to calculate the value of the output capacitor for other output rails, and the calculated values are:

- C_{OUT3} >> 5.79 µF , I_{COUT3_RMS} = 0.073 A
- C_{OUT4} >> 13.88 µF , I_{COUT4_RMS} = 0.292 A
- C_{OUT5} >> 6.94 µF , I_{COUT5_RMS} = 0.073 A
- C_{OUT6} >> 11.57 µF , I_{COUT6_RMS} = 0.146 A
- C_{OUT7} >> 15.152 µF , I_{COUT7_RMS} = 0.292 A

A 470-µF, 25-V capacitor is used for the 12-V/1.5-A output rail. A 100-µF, 25-V capacitor is used for 5-V/0.2-A, 12-V/0.2-A, 7.2-V/0.1-A, and 11-V/0.2-A output rails. A 47-µF, 25-V capacitor is used for –7.2-V/0.05-A and 6-V/0.05-A output rails.

A higher value of capacitance or a low ESR capacitor is recommended to achieve the reduced ripple.

4.2.7 Capacitance on VDD Pin

The capacitance on VDD needs to supply the device operating current until the output of the converter reaches the target minimum operating voltage in CC regulation.

The total output current available to the load and to charge the output capacitors is the CC regulation target.

With a startup resistance (R_{STR}) of 3 MΩ and a desired startup time (dt_{CVDD}) of 5 s, calculate the C_{VDD} using Equation 19.

$$C_{VDD} = \left(\frac{V_{IN(min)}}{R_{STR}} - I_{START} \right) \times \frac{dt_{CVDD}}{V_{DD(on)}} \tag{19}$$

where

- I_{START} is the startup bias supply current = 1.5 µA (UCC28700 datasheet [SLUSB41])
- $V_{DD(on)}$ is the UVLO turn-on voltage threshold = 21 V (UCC28700 datasheet [SLUSB41])

$$C_{VDD} = \left(\frac{100}{3\ M\Omega} - 1.5\ \mu A \right) \times \frac{5}{21} = 7.58\ \mu F$$

The chosen value of the C_{VDD} capacitor is 10 µF to ensure the turn-on is even at full load.

4.2.8 VS Resistor Divider and Line Compensation Resistor

The VS divider resistors determine the output voltage regulation point of the flyback converter. Also, the high-side divider resistor (R_{S1}) determines the line voltage at which the controller enables continuous DRV operation. R_{S1} is initially determined based on transformer auxiliary-to-primary turns ratio and desired input voltage operating threshold as seen by Equation 20.

$$R_{S1} = \frac{V_{IN(run)}}{N_{PA} \times I_{VSL(run)}} \tag{20}$$

where

- $V_{IN(run)}$ is the converter input startup (run) voltage = 100-V DC
- $I_{VSL(run)}$ is the run-threshold for the current pulled out of the VS pin during the MOSFET on-time = 220 µA (UCC28700 datasheet [SLUSB41])
- N_{PA} is the transformer primary-to-auxiliary turns ratio

$$R_{S1} = \frac{100}{8 \times 220\ \mu A} = 56.82\ k\Omega$$

The actual value used for R_{S1} is 56.2 kΩ. The low-side VS pin resistor is selected based on desired VO regulation voltage as seen by Equation 21.

$$R_{S2} = \frac{R_{S1} \times V_{VSR}}{N_{AS} \times (V_{OCV} + V_F) - V_{VSR}} \tag{21}$$

where

- V_{VSR} is the CV regulating level at the VS input = 4.05 (UCC28700 datasheet [SLUSB41])
- N_{AS} is the transformer auxiliary-to-secondary turns ratio = 1 (Since the main 12-V/1.5-A secondary itself is used as auxiliary)
- V_{OCV} is the regulated output voltage of the converter
- V_F is the secondary rectifier diode forward voltage drop at near-zero current

$$R_{S2} = \frac{56.2\ k\Omega \times 4.05}{1 \times (12\ V + 0.5\ V) - 4.05} = 26.93\ k\Omega$$

The actual value used for R_{S2} is 25.5 kΩ.

This design can maintain tight CC regulation over the input line by using the line compensation feature. The line compensation resistor (R_{LC}) value is determined by current flowing in R_{S1} and the expected gate drive and MOSFET turn-off delay.

Calculate the drain-to-source rise time of the MOSFET using Equation 22.

$$T_R = 2 \times \frac{Q_g}{I_{DRV}} \tag{22}$$

where

- Q_g of MOSFET used is 9.2 nC and I_{DRV} is 0.35 A

$$T_R = 2 \times \frac{9.2\ nC}{0.35} = 52.57\ ns$$

Assuming a 50-ns internal delay in the controller, calculate the value of R_{LC} using Equation 23.

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times T_D \times N_{PA}}{L_P} \quad (23)$$

where

- K_{LC} is a current scaling constant = 25 A/A (UCC28700 datasheet [SLUSB41])
- R_{CS} is the current-sense resistor value = 0.6 Ω (Calculated earlier)
- T_D is the current-sense delay including MOSFET turn-off delay; add ~50 ns to MOSFET delay = 52.57 ns + 50 ns = 102.57 ns

$$R_{LC} = \frac{25 \times 56.2\ k\Omega \times 0.6\ \Omega \times 102.57\ ns \times 8}{410\ \mu H} = 1.687\ k\Omega$$

To have better regulation and improvement in efficiency, a capacitor of 1 nF is connected to the current sense pin. To avoid a high time constant of the RC circuit at the current sense pin, the selected value of R_{LC} is smaller than the calculated value. With experimental results, the chosen value for R_{LC} is 220 Ω.

4.3 eFuse Component Selection

4.3.1 V_{IN}

This pin is the input voltage to the device. Place a ceramic bypass capacitor close to the device from V_{IN} to GND to alleviate bus transients. The recommended operating voltage range is 4.5 to 13.8 V.

4.3.2 dV/dT

A capacitor can be connected to this pin to GND to control the slew rate of the output voltage at power-on. The dV/dT pin can be left floating to obtain a predetermined slew rate (minimum $T_{dV/dT}$) on the output. The slew rate at startup is determined by Equation 24:

$$\frac{dV_{OUT}}{dT} = \frac{I_{dVdT} \times GAIN_{dVdT}}{C_{dVdT} + C_{INT}} \tag{24}$$

where

- I_{dVdT} is the dV/dT charging current = 220 nA (TPS259241 datasheet [SLVSCU9])
- C_{INT} = 70 pF (TPS259241 datasheet [SLVSCU9])
- $GAIN_{dVdT}$ is dV/dT to OUT gain = 4.85 (TPS259241 datasheet [SLVSCU9])

With a desired output slew rate of 1 kV/s, the value of C_{dVdT} is calculated as:

$$C_{dVdT} = \left(\frac{I_{dVdT} \times GAIN_{dVdT}}{\frac{dV_{OUT}}{dT}} \right) - C_{INT}$$

$$C_{dVdT} = \left(\frac{220\ nA \times 4.85}{1000\ V/s} \right) - 70\ pF = 997\ pF$$

This design uses a standard 1000-pF capacitor.

4.3.3 Current Limiting Resistor

The eFuse continuously monitors the load current and keeps it limited to the value programmed by R_{ILIM}. After the start-up event and during normal operation, the current limit is set to I_{OL} (overload current limit).

With a desired overcurrent limited to 2 A, the value of R_{ILIM} is calculated with Equation 25.

$$R_{ILIM} = \frac{I_{ILIM} - 0.7}{3 \times 10^{-5}} = \frac{2 - 0.7}{3 \times 10^{-5}} = 43.33\ k\Omega \tag{25}$$

This design uses a standard 43.2-kΩ resistor to limit current.

5 Getting Started Hardware

5.1 Test Equipment Needed to Validate Board

- DC source: 0- to 450-V rated
- Digital oscilloscope
- 6 ½ digit multi-meter (×3)
- Electronic or resistive load (seven numbers)

5.2 Test Conditions

Input voltage range
The DC source must be capable of varying between a V_{INDC} of 100-V to 450-V DC. Set the input current limit to 1 A.

Output
Connect an electronic load capable of 20 V to all the outputs. The load must be variable and capable of 2 A for V_{OUT1} and 0.3 A for all other outputs. A rheostat or resistive decade box can also be used in place of an electronic load.

5.3 Test Procedure

1. Connect the DC source at the input terminals (Pin-1 and Pin-3 of connector J1) of the reference board with Pin-1 being the ground reference.
2. Connect the following output terminals:
   - Connector J3 details:
     (a) Pin-1,2 for 12 V/1.5 A with Pin-1 = 12 V and Pin-2 = PGND
     (b) Pin-3,2 for –7.2 V/0.05 A with Pin-3 = –7.2 V and Pin-2 = PGND
     (c) Pin-4,2 for 5 V/0.2 A with Pin-4 = 12 V and Pin-2 = PGND
   - Connector J2 details:
     (a) Pin-1,2 for 11 V_ISO/0.2 A with Pin-2 = 11 V and Pin-1 = SGND2
     (b) Pin-4,5 for 7.2 V_ISO/0.1 A with Pin-5 = 7.2 V and Pin-4 = SGND1
     (c) Pin-7,8 for 12 V_ISO/0.2 A with Pin-8 = 12 V and Pin-7 = PGND2
     (d) Pin-9,10 for 6 V_ISO/0.05 A with Pin-10 = 6 V and Pin-9 = PGND3
3. Set and maintain a minimum load of about 10 mA.
4. Gradually increase the input voltage from 0 V to a turn-on voltage of 120 V.
5. Turn on the load to draw current from the output terminals of the converter.
6. Observe the startup conditions and smooth switching waveforms.

6 Test Results

The test results are divided into multiple sections that cover the steady state performance measurements, functional performance waveforms and test data, transient performance waveforms, thermal measurements, and surge measurements.

6.1 Performance Data

6.1.1 Efficiency and Regulation With Load Variation

Table 4 shows the efficiency and regulation performance data at a 165-V DC input.

Table 4. Efficiency and Regulation at 165-V DC Input

LOAD %	I_{INDC} (A)	P_{INDC} (W)	V_{OUT1} (V)	I_{OUT1} (A)	V_{OUT2} (V)	I_{OUT2} (A)	V_{OUT3} (V)	I_{OUT3} (A)	V_{OUT4} (V)	I_{OUT4} (A)	V_{OUT5} (V)	I_{OUT5} (A)	V_{OUT6} (V)	I_{OUT6} (A)	V_{OUT7} (V)	I_{OUT7} (A)	P_{OUT} (W)	EFF (%)	% REG V_{OUT1}	% REG V_{OUT2}	% REG V_{OUT3}	% REG V_{OUT4}	% REG V_{OUT5}	% REG V_{OUT6}	% REG V_{OUT7}	PWR LOSS (W)
0	0.00	0.033	14.31	–	9.14	–	7.070	–	13.33	–	8.94	–	13.91	–	7.57	–	0.00	0.0	–	–	–	–	–	–	–	0.03
10	0.02	3.140	12.58	0.15	7.20	0.00	5.023	0.02	10.67	0.02	7.44	0.011	12.65	0.021	7.06	0.01	2.62	83.5	–0.04	0.41	0.12	–0.08	1.50	–0.08	–0.20	0.52
25	0.05	7.549	12.57	0.37	7.18	0.01	5.008	0.05	10.66	0.05	7.45	0.025	12.64	0.052	7.06	0.01	6.48	85.8	–0.12	0.13	–0.18	–0.18	1.63	–0.16	–0.20	1.07
50	0.09	14.949	12.57	0.75	7.13	0.02	4.995	0.10	10.66	0.10	7.22	0.049	12.64	0.105	7.07	0.03	13.03	87.2	–0.12	–0.57	–0.44	–0.18	–1.50	–0.16	–0.05	1.92
75	0.14	22.391	12.59	1.13	7.16	0.04	5.020	0.15	10.68	0.15	7.25	0.070	12.67	0.158	7.08	0.04	19.59	87.5	0.07	–0.13	0.06	0.04	–1.08	0.07	0.12	2.80
100	0.18	29.613	12.61	1.50	7.18	0.05	5.040	0.19	10.72	0.20	7.29	0.092	12.70	0.210	7.10	0.06	26.09	88.1	0.20	0.16	0.45	0.40	–0.55	0.32	0.33	3.53

Table 5 shows the efficiency and regulation performance data at a 250-V DC input.

Table 5. Efficiency and Regulation at 250-V DC Input

LOAD %	I_{INDC} (A)	P_{INDC} (W)	V_{OUT1} (V)	I_{OUT1} (A)	V_{OUT2} (V)	I_{OUT2} (A)	V_{OUT3} (V)	I_{OUT3} (A)	V_{OUT4} (V)	I_{OUT4} (A)	V_{OUT5} (V)	I_{OUT5} (A)	V_{OUT6} (V)	I_{OUT6} (A)	V_{OUT7} (V)	I_{OUT7} (A)	P_{OUT} (W)	EFF (%)	% REG V_{OUT1}	% REG V_{OUT2}	% REG V_{OUT3}	% REG V_{OUT4}	% REG V_{OUT5}	% REG V_{OUT6}	% REG V_{OUT7}	PWR LOSS (W)
0	0.00	0.04	14.53	–	9.330	–	7.390	–	13.34	–	8.94	–	13.97	–	7.57	–	0.00	0.0	–	–	–	–	–	–	–	0.04
10	0.01	3.23	12.57	0.151	7.150	0.005	5.014	0.020	10.66	0.019	7.25	0.010	12.67	0.021	7.04	0.006	2.61	80.9	–0.12	–0.29	–0.06	–0.11	–1.15	–0.08	–0.51	0.62
25	0.03	7.70	12.56	0.374	7.190	0.012	5.003	0.047	10.65	0.048	7.49	0.025	12.65	0.052	7.07	0.014	6.48	84.2	–0.20	0.27	–0.28	–0.21	2.13	–0.24	–0.08	1.22
50	0.06	15.13	12.58	0.753	7.140	0.025	4.995	0.097	10.66	0.097	7.28	0.049	12.66	0.105	7.06	0.027	13.04	86.2	–0.04	–0.43	–0.44	–0.11	–0.74	–0.16	–0.23	2.08
75	0.09	22.64	12.60	1.127	7.165	0.036	5.020	0.148	10.68	0.148	7.31	0.071	12.69	0.158	7.08	0.043	19.61	86.6	0.14	–0.08	0.06	0.07	–0.33	0.09	0.06	3.02
100	0.12	30.03	12.63	1.501	7.196	0.048	5.040	0.194	10.71	0.196	7.34	0.093	12.73	0.212	7.13	0.057	26.17	87.1	0.36	0.35	0.45	0.36	0.08	0.39	0.76	3.86

Table 6 shows the efficiency and regulation performance data at a 325-V DC input.

Table 6. Efficiency and Regulation at 325-V DC Input

LOAD %	I_{INDC} (A)	P_{INDC} (W)	V_{OUT1} (V)	I_{OUT1} (A)	V_{OUT2} (V)	I_{OUT2} (A)	V_{OUT3} (V)	I_{OUT3} (A)	V_{OUT4} (V)	I_{OUT4} (A)	V_{OUT5} (V)	I_{OUT5} (A)	V_{OUT6} (V)	I_{OUT6} (A)	V_{OUT7} (V)	I_{OUT7} (A)	P_{OUT} (W)	EFF (%)	% REG V_{OUT1}	% REG V_{OUT2}	% REG V_{OUT3}	% REG V_{OUT4}	% REG V_{OUT5}	% REG V_{OUT6}	% REG V_{OUT7}	PWR LOSS (W)
0	0.00	0.05	14.73	–	9.41	–	7.480	–	13.34	–	8.94	–	13.950	–	7.57	–	0.00	0.0	–	–	–	–	–	–	–	0.05
10	0.01	3.36	12.56	0.151	7.13	0.005	5.006	0.019	10.65	0.019	7.19	0.010	12.664	0.021	7.03	0.006	2.61	77.7	–0.20	–0.57	–0.22	–0.22	–1.78	–0.12	–0.94	0.75
25	0.02	7.85	12.56	0.375	7.14	0.012	4.996	0.050	10.65	0.049	7.30	0.025	12.650	0.052	7.05	0.014	6.50	82.8	–0.20	–0.43	–0.42	–0.22	–0.27	–0.23	–0.66	1.35
50	0.05	15.39	12.57	0.753	7.15	0.025	4.991	0.097	10.67	0.097	7.37	0.050	12.660	0.106	7.08	0.028	13.06	84.8	–0.12	–0.29	–0.52	–0.04	0.68	–0.15	–0.24	2.33
75	0.07	22.91	12.59	1.127	7.17	0.036	5.011	0.148	10.69	0.148	7.36	0.071	12.684	0.158	7.12	0.044	19.60	85.5	0.01	–0.01	–0.12	0.15	0.55	0.03	0.33	3.31
100	0.09	30.42	12.61	1.500	7.19	0.050	5.040	0.190	10.71	0.200	7.38	0.090	12.740	0.220	7.20	0.060	26.27	86.4	0.22	0.33	0.35	0.34	0.82	0.48	1.51	4.15

Table 7 shows the efficiency and regulation performance data at a 400-V DC input.

Table 7. Efficiency and Regulation at 400-V DC Input

LOAD %	I_{INDC} (A)	P_{INDC} (W)	V_{OUT1} (V)	I_{OUT1} (A)	V_{OUT2} (V)	I_{OUT2} (A)	V_{OUT3} (V)	I_{OUT3} (A)	V_{OUT4} (V)	I_{OUT4} (A)	V_{OUT5} (V)	I_{OUT5} (A)	V_{OUT6} (V)	I_{OUT6} (A)	V_{OUT7} (V)	I_{OUT7} (A)	P_{OUT} (W)	EFF (%)	% REG V_{OUT1}	% REG V_{OUT2}	% REG V_{OUT3}	% REG V_{OUT4}	% REG V_{OUT5}	% REG V_{OUT6}	% REG V_{OUT7}	PWR LOSS (W)
0	0.00	0.08	14.81	–	9.26	–	7.660	–	13.34	–	8.94	–	13.960	–	7.57	–	0.00	0.0	–	–	–	–	–	–	–	0.08
10	0.01	3.51	12.56	0.151	7.11	0.005	5.005	0.019	10.65	0.019	7.12	0.010	12.657	0.021	7.03	0.006	2.61	74.2	–0.20	–0.85	–0.24	–0.23	–2.55	–0.22	–0.57	0.91
25	0.02	8.07	12.57	0.375	7.12	0.012	4.995	0.050	10.66	0.049	7.16	0.024	12.679	0.053	7.04	0.014	6.52	80.7	–0.12	–0.71	–0.44	–0.13	–2.00	–0.05	–0.42	1.56
50	0.04	15.65	12.58	0.753	7.15	0.025	4.989	0.096	10.68	0.097	7.38	0.050	12.690	0.106	7.08	0.028	13.08	83.6	–0.04	–0.29	–0.56	0.05	1.01	0.04	0.14	2.57
75	0.06	23.18	12.60	1.128	7.17	0.036	5.010	0.147	10.69	0.148	7.39	0.071	12.702	0.159	7.09	0.043	19.64	84.7	0.10	–0.01	–0.18	0.16	1.16	0.13	0.28	3.54
100	0.08	30.33	12.61	1.500	7.19	0.050	5.030	0.190	10.69	0.200	7.48	0.100	12.700	0.210	7.11	0.060	26.12	86.1	0.20	0.30	0.26	0.15	2.38	0.10	0.57	4.20

Table 8 shows the line regulation of all outputs over the input voltage range for full load.

Table 8. Line Regulation at Full Load

V_{INPUT} (V)	V_{OUT1} (V)	V_{OUT2} (V)	V_{OUT3} (V)	V_{OUT4} (V)	V_{OUT5} (V)	V_{OUT6} (V)	V_{OUT7} (V)	% REG V_{OUT1}	% REG V_{OUT2}	% REG V_{OUT3}	% REG V_{OUT4}	% REG V_{OUT5}	% REG V_{OUT6}	% REG V_{OUT7}
165	12.61	7.182	5.04	10.72	7.29	12.701	7.097	–0.044	–0.125	0.074	0.124	–1.119	–0.128	–0.535
250	12.63	7.196	5.04	10.71	7.34	12.730	7.130	0.115	0.070	0.074	0.021	–0.441	0.100	–0.073
325	12.61	7.194	5.04	10.71	7.38	12.740	7.204	–0.028	0.042	–0.025	0.021	0.102	0.179	0.961
400	12.61	7.192	5.03	10.69	7.48	12.698	7.110	–0.044	0.014	–0.124	–0.166	1.458	–0.151	–0.353

6.1.2 Standby Power

The standby power was noted at multiple DC input voltages with no load on the output DC bus. The results are shown in Table 9:

Table 9. No Load Power Across the Input

V_{INDC} (VDC)	I_{INDC} (mA)	P_{INDC} (mW)
165	0.20	33.00
250	0.16	39.50
325	0.16	52.33
400	0.20	80.00

6.2 Performance Curves

6.2.1 Efficiency With Load Variation

Figure 3 shows the measured efficiency of the system with DC input voltage variation.

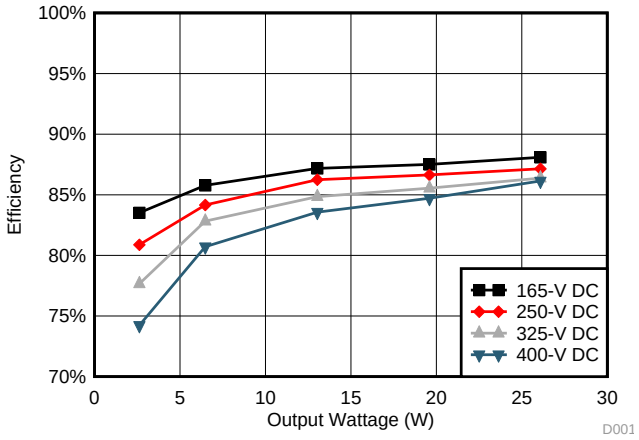


Figure 3. Efficiency versus Output Power

6.2.2 Load Regulation in CV and CC Modes

Figure 4 shows the measured load regulation of the 12-V / 1.5-A output:

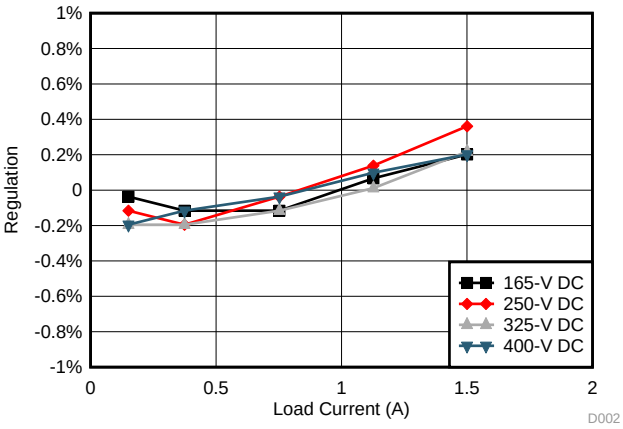


Figure 4. 12-V Output Voltage Variation With Load Current in CV Mode

Figure 5 shows the measured load regulation of the 5-V / 0.2-A output:

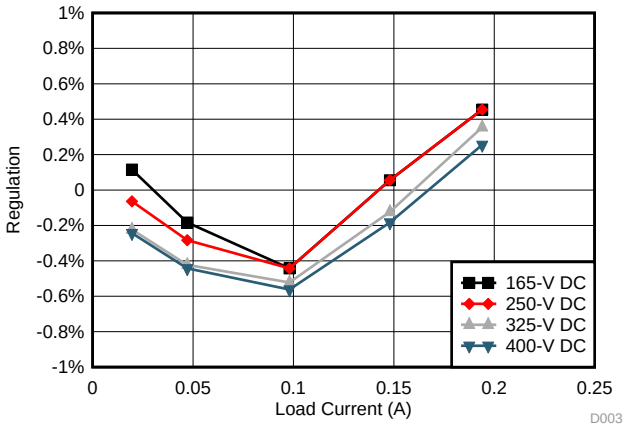


Figure 5. 5-V Output Voltage Variation With Load Current in CV Mode

Figure 6 shows the measured load regulation of the 11-V_ISO / 0.2-A output:

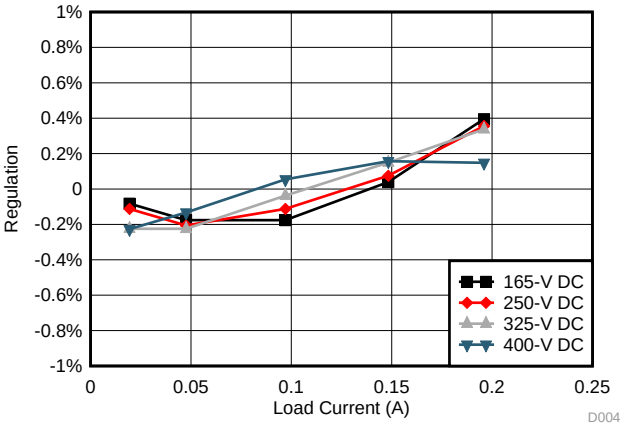


Figure 6. 11-V_ISO Output Voltage Variation With Load Current in CV Mode

Figure 7 shows the measured load regulation of the 12-V_ISO / 0.2-A output:

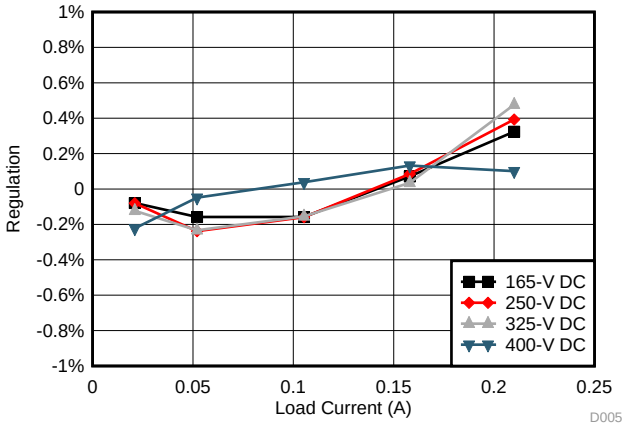


Figure 7. 12-V_ISO Output Voltage Variation With Load Current in CV Mode

6.3 Functional Waveforms

6.3.1 Flyback MOSFET Switching Node Waveforms

Waveforms at the flyback switching (SW) node were observed along with the MOSFET current for 165-V and 400-V DC under full load conditions.

Figure 8 and Figure 9 show the SW node waveform along with MOSFET current for a 165-V DC input and a 400-V DC input, respectively, with all the rails loaded fully.

NOTE: Red trace: Drain voltage, 200 V/div; Green trace: Drain current, 2 A/div

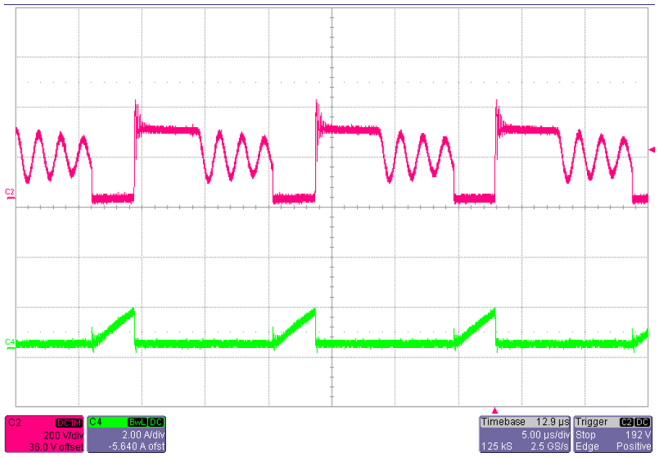


Figure 8. SW Node Waveform and MOSFET Current at V_{INDC} = 165-V DC, Full Load

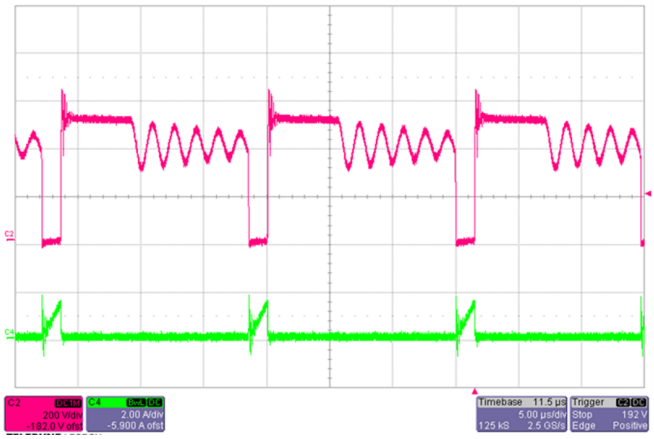


Figure 9. SW Node Waveform and MOSFET Current at V_{INDC} = 400-V DC, Full Load

6.3.2 Output Rectifier Diode Voltage (V_D) Waveforms

Waveforms at all the secondary output rectifier diodes were observed along at a 400-V DC input under full load conditions. The maximum voltage across the diodes is well within their breakdown voltage limit. Figure 10, Figure 11, Figure 12, and Figure 13 show the voltage waveforms at the 12-V, 5-V, 11-V_ISO, and 12-V_ISO output rectifier diodes, respectively.

NOTE: Red trace: Drain-to-source voltage, 10 V/div;

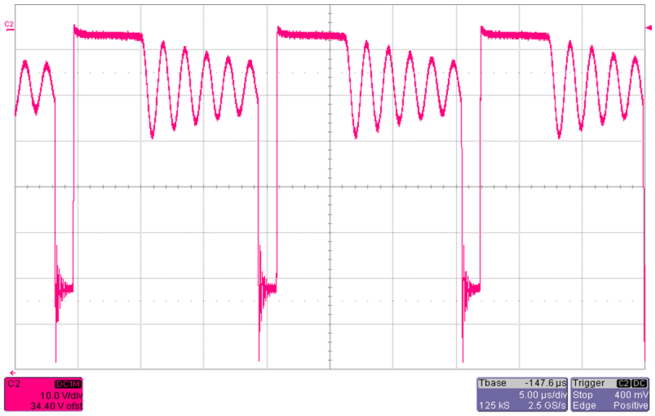


Figure 10. Output Rectifier Diode for 12-V Output (V_{D1}) Waveform at V_{INDC} = 400-V DC, Full Load

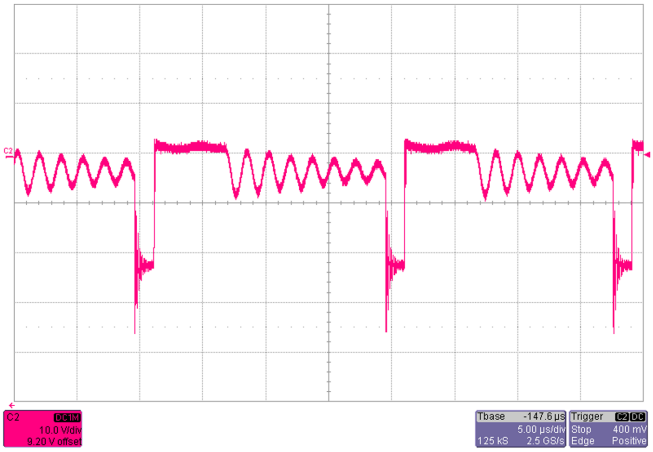


Figure 11. Output Rectifier Diode for 5-V Output (V_{D2}) Waveform at V_{INDC} = 400-V DC, Full Load

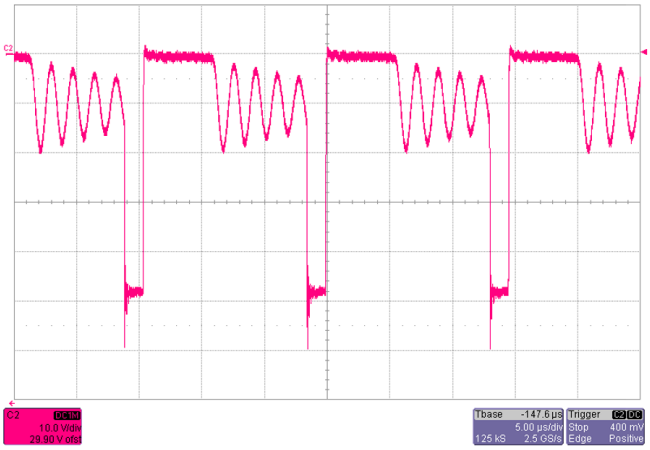


Figure 12. Output Rectifier Diode for 11-V_ISO Output (V_{D3}) Waveform at V_{INDC} = 400-V DC, Full Load

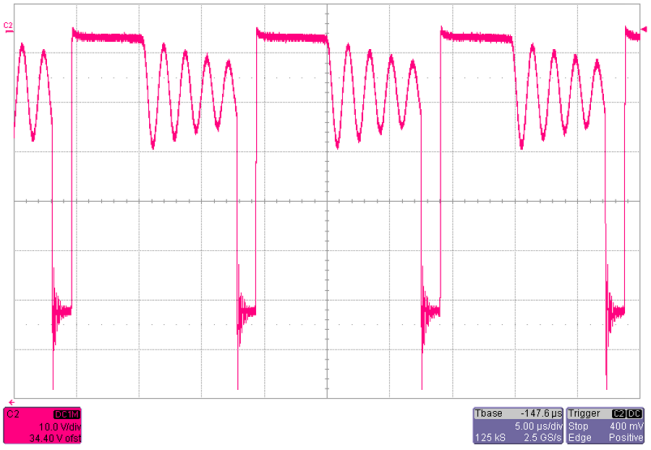


Figure 13. Output Rectifier Diode for 12-V_ISO Output (V_{D4}) Waveform at V_{INDC} = 400-V DC, Full Load

6.3.3 Output Ripple

For the following figures, a ripple is observed at all outputs at full load for 400-V DC input.

The peak–to-peak ripple voltage is around 500 mV. Figure 14, Figure 15, Figure 16, and Figure 17 show the ripple for 12-V, 5-V, 11-V_ISO, and 12-V_ISO outputs at 400-V DC input, respectively.

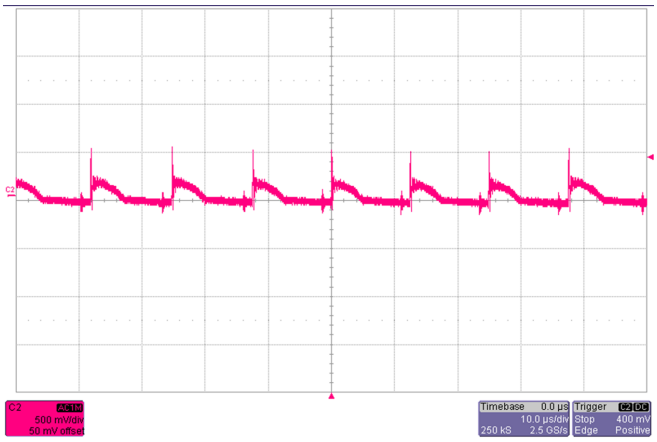


Figure 14. 12-V Output Voltage Ripple at V_{INDC} = 400-V DC and Full Load

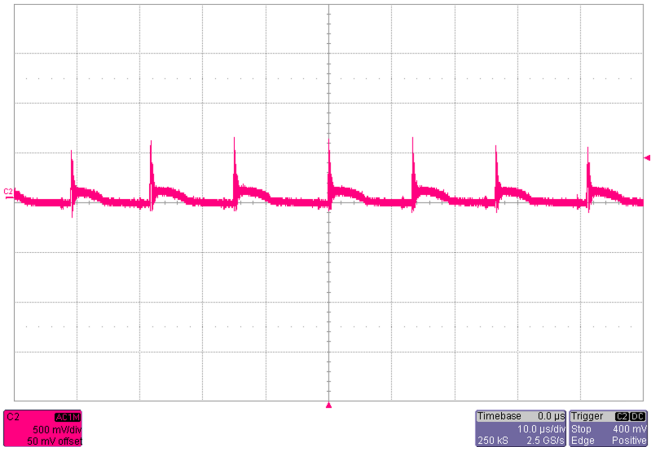


Figure 15. 5-V Output Voltage Ripple at V_{INDC} = 400-V DC and Full Load

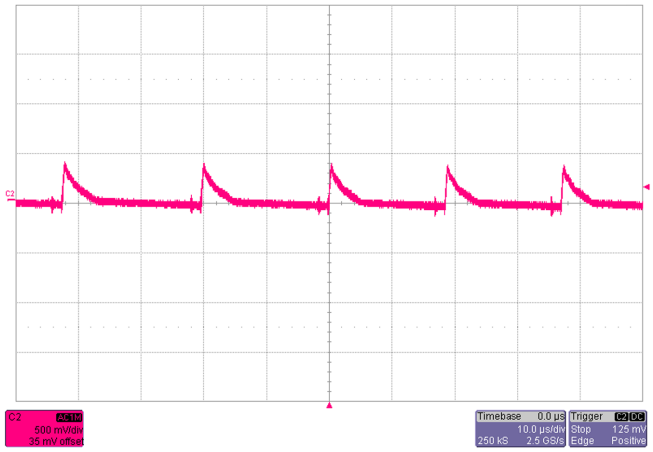


Figure 16. 11-V_ISO Output Voltage Ripple at V_{INDC} = 400-VDC and Full Load

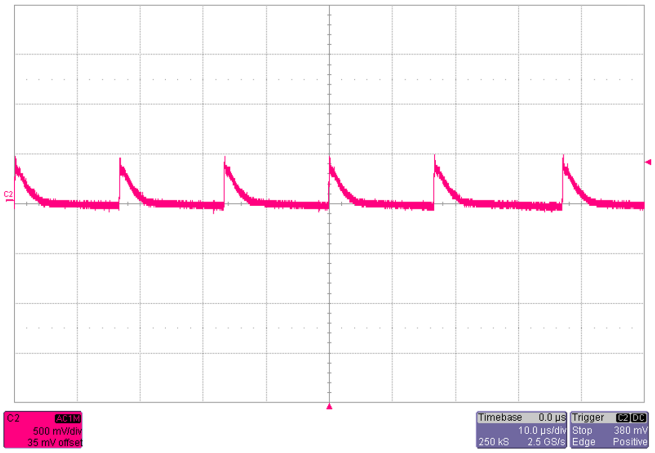


Figure 17. 12-V_ISO Output Voltage Ripple at V_{INDC} = 400-V DC and Full Load

6.4 Transient Waveforms

6.4.1 Turn-On Characteristics

The output turn-on of all the outputs was observed with a resistive load. Figure 18 and Figure 19 show the turn-on waveforms for the 12-V rail at 165-V DC and 400-V DC input voltages, full load, respectively.

NOTE: Red trace: Output voltage, 5 V/div; Green trace: Output current, 1 A/div

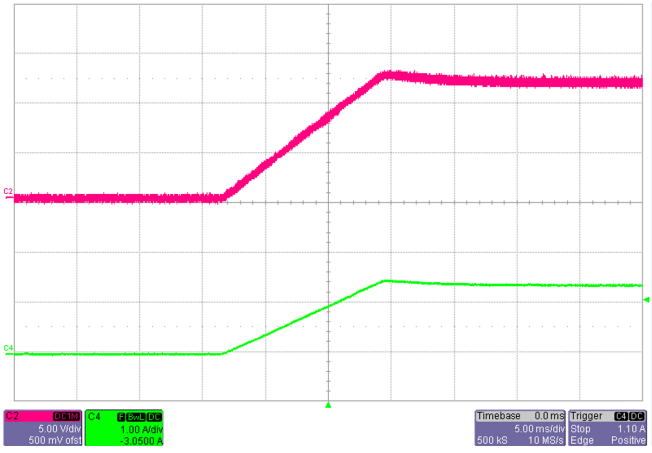


Figure 18. Output Turn-on Waveform for 12-V Output at 165-V DC Input

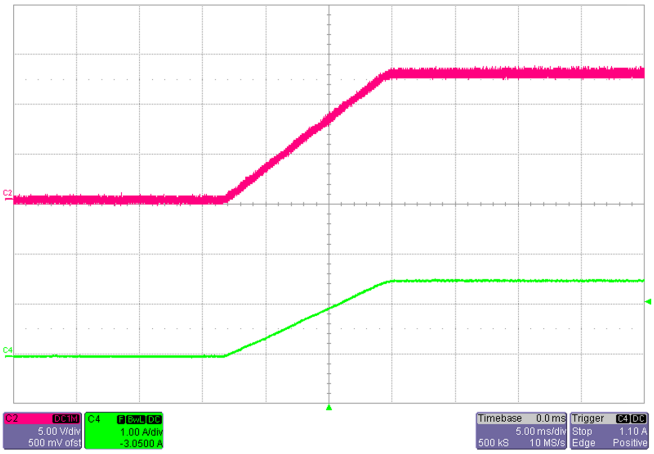


Figure 19. Output Turn-on Waveform for 12-V Output at 400-V DC Input

Figure 20 and Figure 21 show the turn-on waveforms for the 5-V rail at 165-V DC and 400-V DC input voltages, full load, respectively.

NOTE: Red trace: Output voltage, 5 V/div; Green trace: Output current, 0.1 A/div

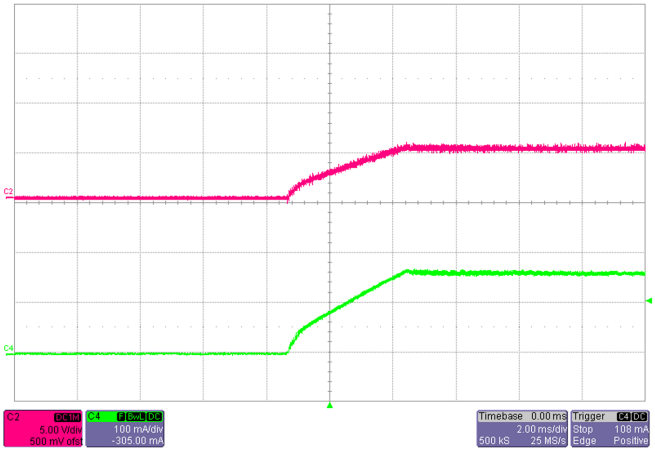


Figure 20. Output Turn-on Waveform for 5-V Output at 165-V DC Input

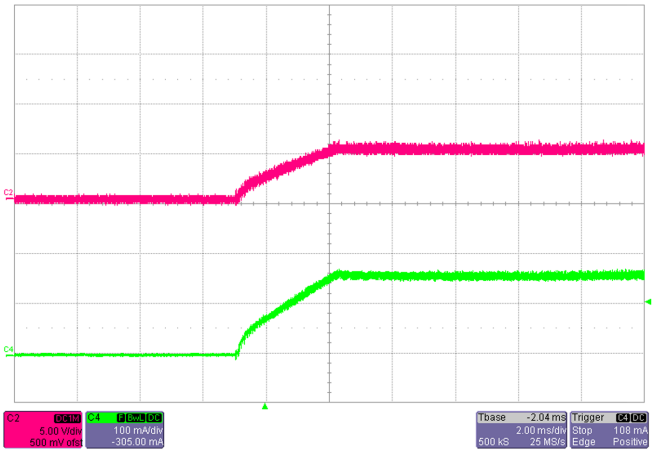


Figure 21. Output Turn-on Waveform for 5-V Output at 400-V DC Input

Figure 22 and Figure 23 show the turn-on waveforms for the 11-V_ISO rail at 165-V DC and 400-V DC input voltages, full load, respectively.

NOTE: Red trace: Output voltage, 5 V/div; Green trace: Output current, 0.1 A/div

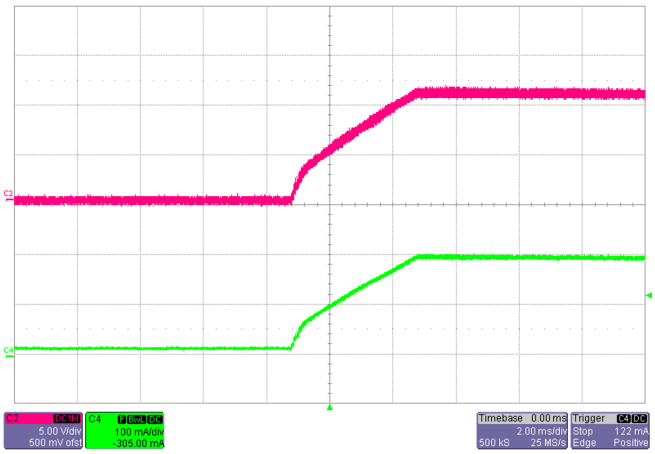


Figure 22. Output Turn-on Waveform for 11-V_ISO Output at 165-V DC Input

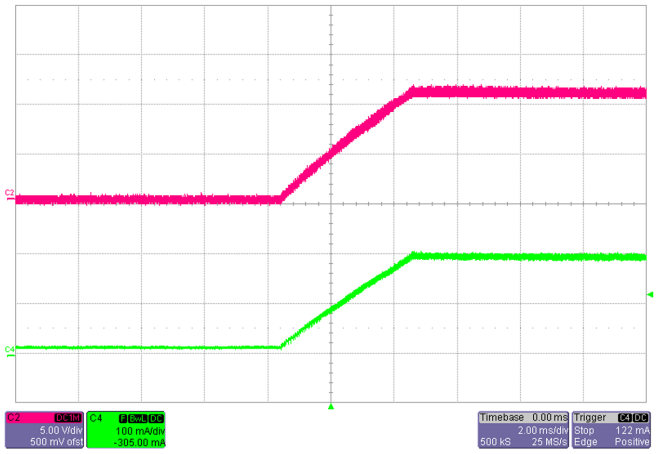


Figure 23. Output Turn-on Waveform for 11-V_ISO Output at 400-V DC Input

Figure 24 and Figure 25 show the turn-on waveforms for the 12-V_ISO rail at 165-V DC and 400-V DC input voltages, full load, respectively.

NOTE: Red trace: Output voltage, 5 V/div; Green trace: Output current, 0.1 A/div

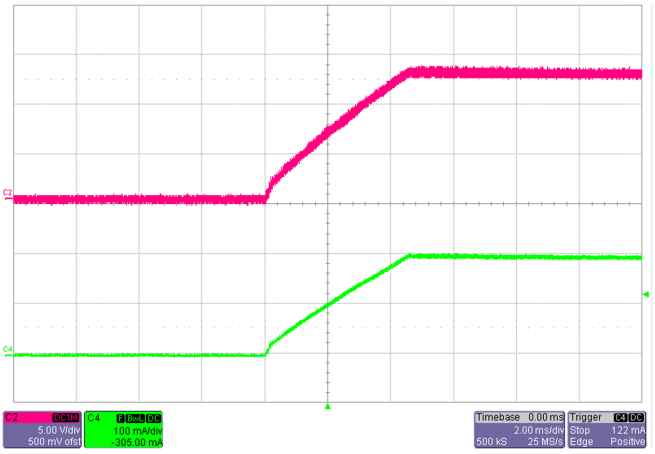


Figure 24. Output Turn-on Waveform for 12-V_ISO Output at 165-V DC Input

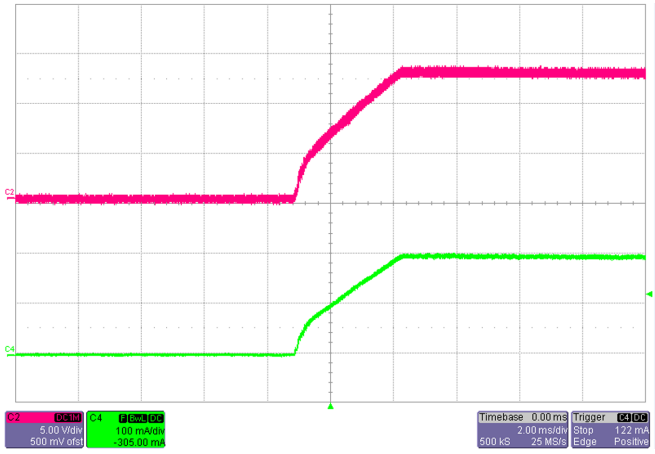


Figure 25. Output Turn-on Waveform for 12-V_ISO Output at 400-V DC Input

6.4.2 Transient Load Response

Load transient performance was observed for all the loads with the load switched at a 0.2-m wire length. The load transient was observed for output switch on from 10% to 100% and output switch off from 100% to 10% load.

Figure 26 and Figure 27 depict the transient load response for a 12-V output at a 400-V DC input with a load transient from 0.15 to 1.5 A and from 1.5 to 0.15 A, respectively.

NOTE: Red trace: Output voltage, 5 V/div; Green trace: Output current, 1 A/div

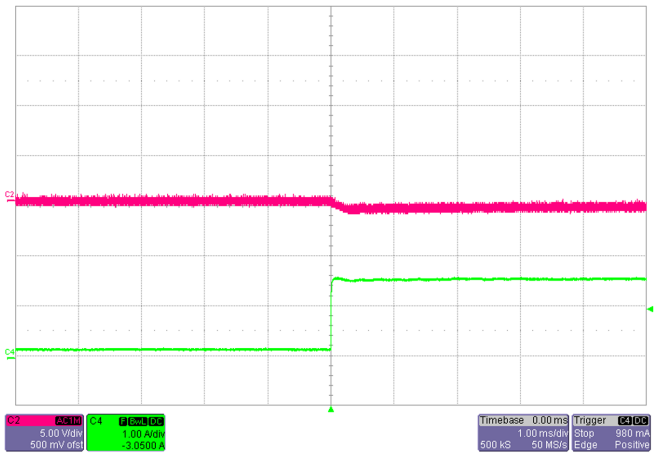


Figure 26. 12-V Output Voltage Waveform, Load Transient From 0.15 to 1.5 A

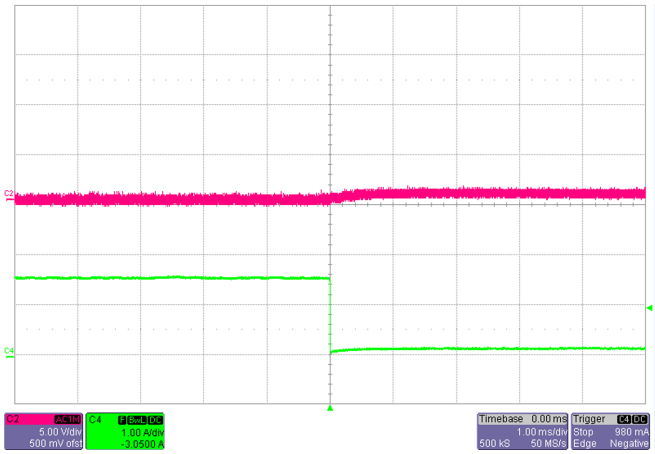


Figure 27. 12-V Output Voltage Waveform, Load Transient From 1.5 to 0.15 A

Figure 28 and Figure 29 depict the transient load response for a 5-V output at a 400-V DC input with a load transient from 0.02 to 0.2 A and from 0.2 to 0.02 A, respectively.

NOTE: Red trace: Output voltage, 5 V/div; Green trace: Output current, 0.1 A/div

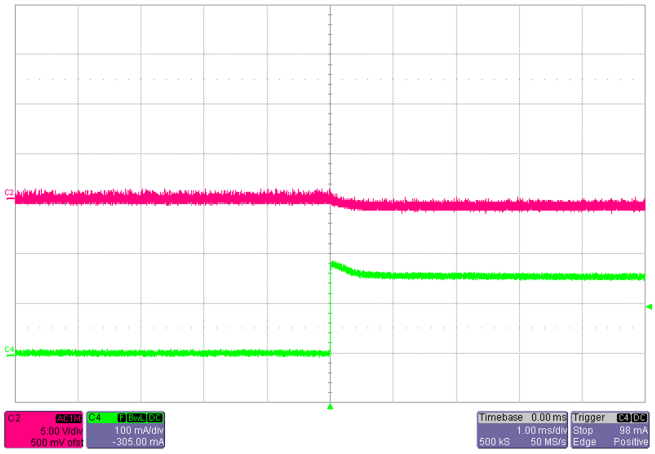


Figure 28. 5-V Output Voltage Waveform, Load Transient From 0.02 to 0.2 A

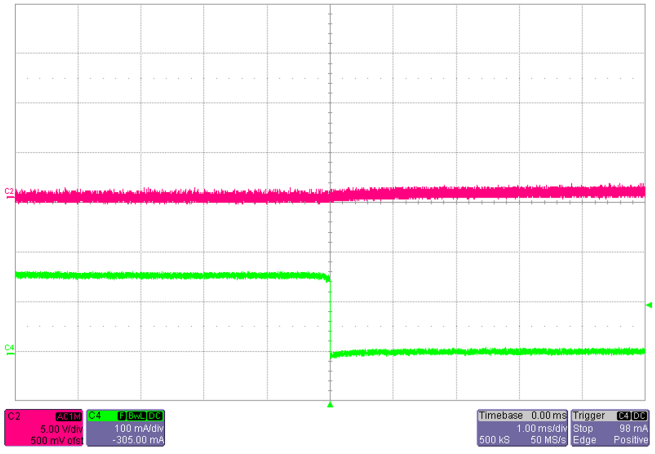


Figure 29. 5-V Output Voltage Waveform, Load Transient From 0.2 to 0.02 A

Figure 30 and Figure 31 depict the transient load response for a 11-V_ISO output at a 400-V DC input with a load transient from 0.02 to 0.2 A and from 0.2 to 0.02 A, respectively.

NOTE: Red trace: Output voltage, 5 V/div; Green trace: Output current, 0.1 A/div

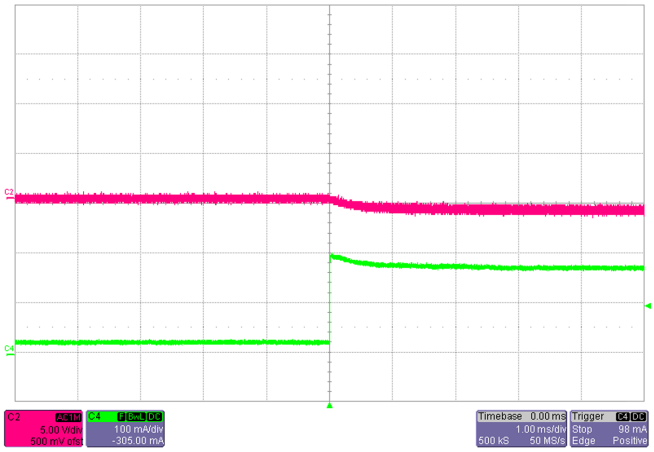


Figure 30. 11-V Output Voltage Waveform, Load Transient From 0.02 to 0.2 A

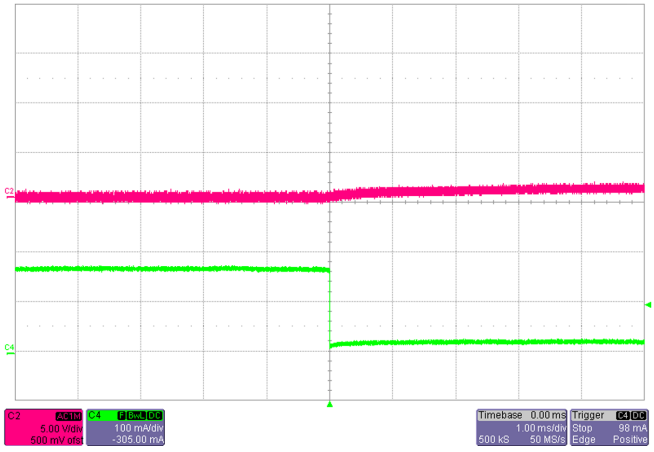


Figure 31. 11-V Output Voltage Waveform, Load Transient From 0.2 to 0.02 A

Figure 32 and Figure 33 depict the transient load response for a 12-V_ISO output at a 400-V DC input with a load transient from 0.02 to 0.2 A and from 0.2 to 0.02 A, respectively.

NOTE: Red trace: Output voltage, 5 V/div; Green trace: Output current, 0.1 A/div

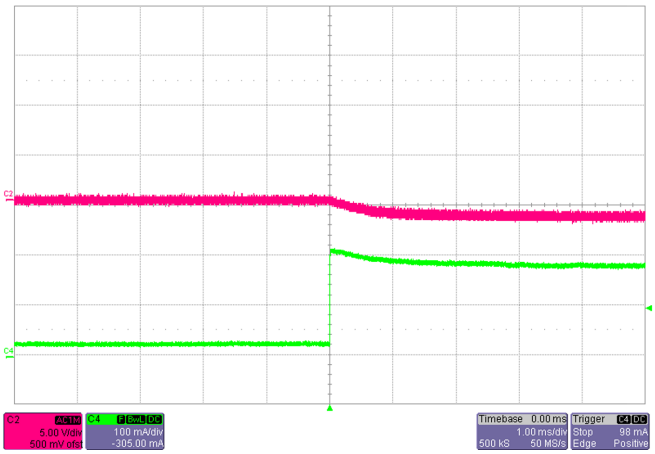


Figure 32. 12-V Output Voltage Waveform, Load Transient From 0.02 to 0.2 A

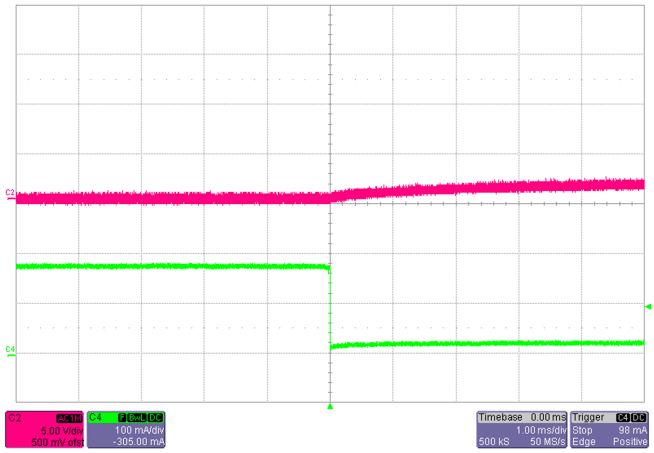


Figure 33. 12-V Output Voltage Waveform, Load Transient From 0.2 to 0.02 A

6.4.3 Short Circuit Response

A short was applied and removed to observe the output turn-off and auto-recovery cycle. When the short is applied, the converter shuts down and goes into hiccup mode; when the short is removed, the converter recovers back to normal operation. Figure 34 shows the short-circuit output current and voltage waveform, which shows the hiccup mode with the short applied and the converter's recovery with the short removed.

NOTE: Red trace: Output voltage, 5 V/div; Green trace: Output current, 5 A/div

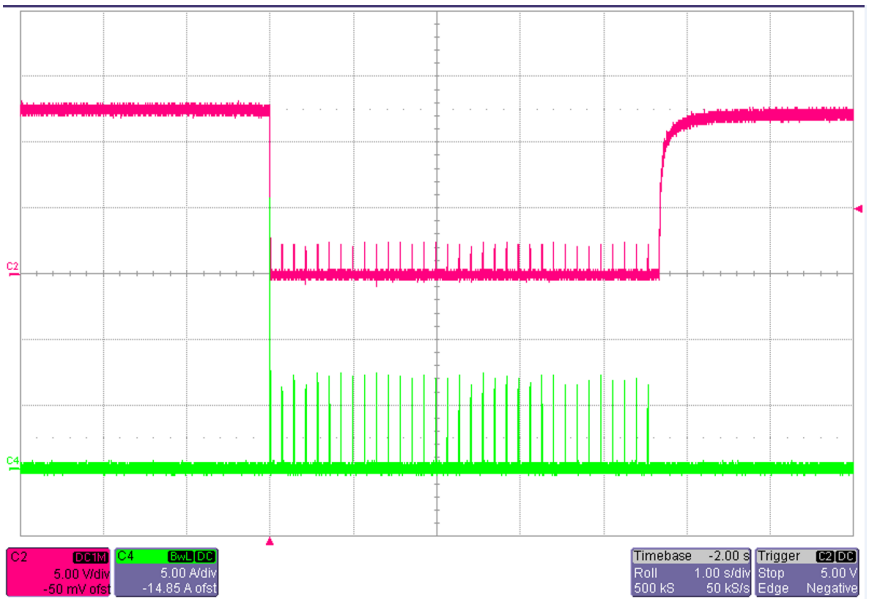


Figure 34. Response During Short-Circuit and Auto-Recovery When Short is Removed

6.5 Thermal Measurements

Thermal images are plotted at room temperature (25°C) with a closed enclosure, 100LFM fan cooling, 20 cm from the board, and after keeping the board continuously switched on for 30 minutes before capturing the image.

Figure 35 shows the thermal image with an input voltage of 400-V DC, all rails full loaded, and a 25-W output power.

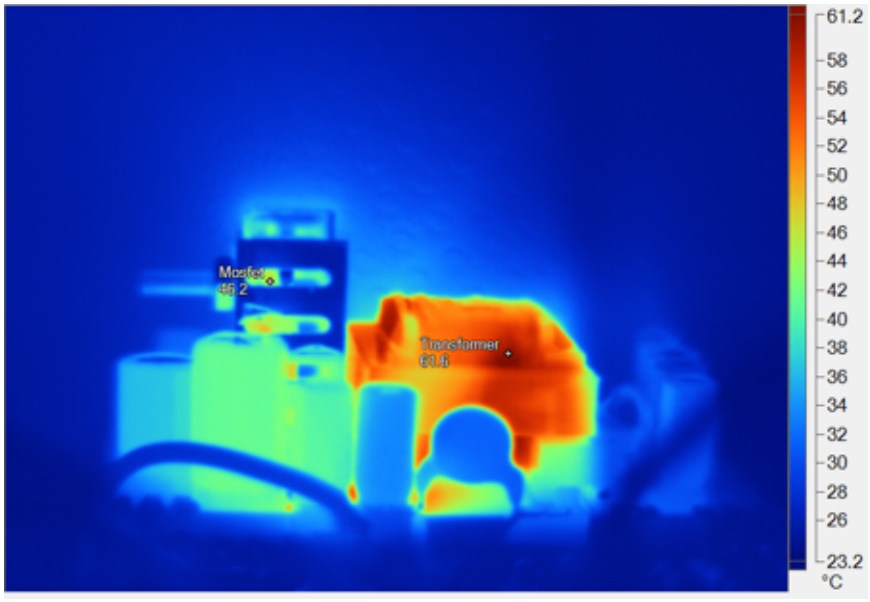


Figure 35. Top Side Thermal Image at 400-V DC Input

Table 10. Highlighted Image Markers

NAME	TEMPERATURE
Ambient	26°C
Flyback FET (Q1)	46.2°C
Transformer (T1)	61.6°C

The temperatures are well contained to low values and have higher margins from the respective junction temperatures of the devices.

7 Design Files

7.1 Schematics

To download the schematics, see the design files at TIDA-00706.

7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00706.

7.3 PCB Layout Recommendations

A careful PCB layout is critical and extremely important in a fast-switching circuit involving magnetics to provide appropriate device operation and design robustness.

7.3.1 Power Stage Specific Guidelines

Follow these key guidelines for routing power stage components:

- Minimize the loop area and trace length of the power path circuits, which contain high frequency switching currents. This helps to reduce EMI and improve converter overall performance.
- Keep the switch node as short as possible. A short and optimal trace width helps to reduce induced ringing caused by parasitic inductance.
- Keep traces with high dV/dt potential and high di/dt capability away from or shielded from sensitive signal traces with adequate clearance and ground shielding.
- For each power supply stage, keep power ground and control ground separate. Tie them together (if they are electrically connected) in one point near DC input return or output return of the given stage correspondingly.
- Place protection devices such as TVS, snubbers, capacitors, or diodes physically close to the device they are intended to protect, and route them with short traces to reduce inductance.
- Choose the width of PCB traces based on acceptable temperature rise at the rated current as per IPC2152 as well as acceptable DC and AC impedances. Also, the traces should withstand the fault currents (such as short circuit current) before the activation of electronic protection such as fuse or circuit breaker.
- Determine the distances between various traces of the circuit according to the requirements of applicable standards. For this design, follow the UL 60950-1 safety standard to maintain the creepage and clearance from live line to neutral line and to safety ground as defined in the Tables 2K through 2N of this standard.
- Adapt thermal management to fit the end-equipment requirements.
- Place bulk input capacitors close to the transformer and to the ground.

7.3.2 Controller Specific Guidelines

Follow these key guidelines for routing controller components and signal circuits:

- Place VS resistors as close to VS pin as possible.
- For the VDD decoupling capacitor, put multiple vias in parallel from the VDD capacitor to the ground plane and from the ground plane to the GND pin. Put as many vias in parallel as possible.
- Place current sense components as close to CS pin as possible.
- See the placement and routing guidelines and layout example presented in the UCC28700 datasheet (SLUSB41).

7.3.3 Layout Prints

To download the layer plots, see the design files at TIDA-00706.

7.4 Altium Project

To download the Altium project files, see the design files at TIDA-00706.

7.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00706.

7.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00706.

7.7 Design Calculator Spreadsheet

To download the design spreadsheet calculator for this reference design, please see the link at TIDA-00706.

8 References

1. Texas Instruments, *Control Challenges for Low Power AC/DC Converters*, Unitrode Power Supply Design Seminar SEM2100 (SLUP325)
2. Texas Instruments, *Snubber Circuits: Theory, Design and Applications*, Seminar 900 Topic 2 (SLUP100)
3. Texas Instruments, *Choosing Standard Recovery Diode or Ultra-Fast Diode in Snubber*, Snubber Application Note (SNVA744)
4. Texas Instruments, *Using the UCC28700EVM-068*, UCC28700 User's Guide (SLUU968)

9 About the Authors

NEHA NAIN is a systems engineer at Texas Instruments where she is responsible for developing reference design solutions for the power delivery, industrial segment. Neha earned her bachelor of electrical and electronics engineering from the PES Institute of Technology (now PES University), Bangalore.

LATIF AMEER BABU is a systems architect at Texas Instruments, where he is responsible for developing reference design solutions for the industrial segment. Latif brings to this role his extensive experience in power electronics, high frequency DC-DC converters, and analog circuit design. Latif earned his master of technology in power electronics and power systems from the Indian Institute of Technology, Mumbai; IN. Latif is a member of the Institute of Electrical and Electronics Engineers (IEEE) and has one US patent.

Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (May 2016) to A Revision	Page
• Changed from preview page	1

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