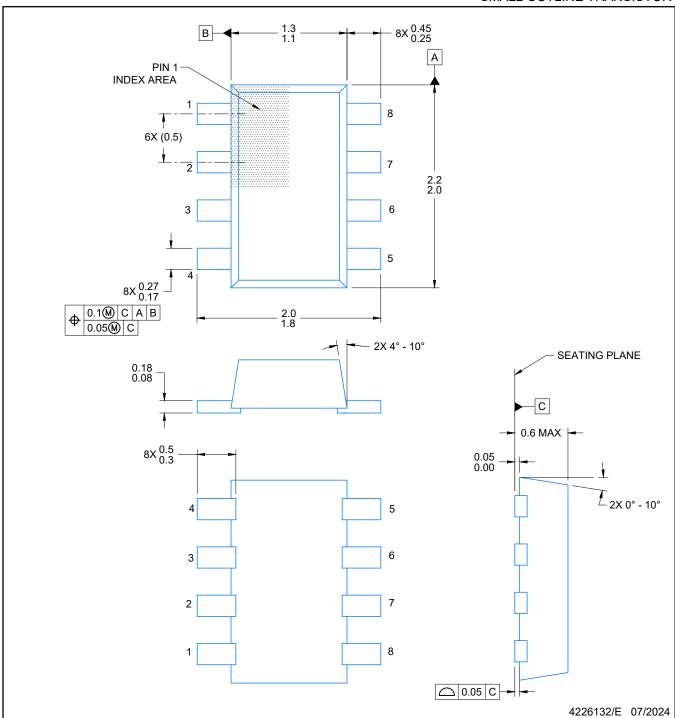
SMALL OUTLINE TRANSISTOR

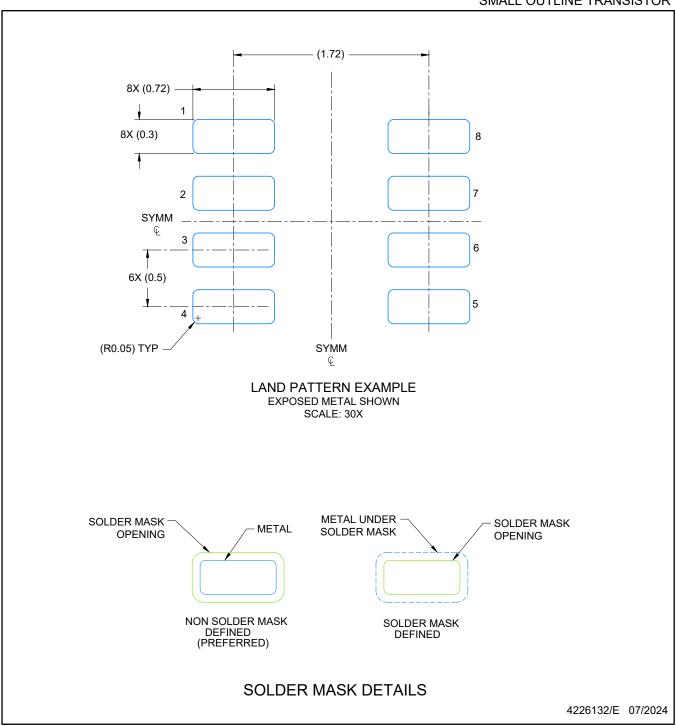


NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 This drawing is subject to change without notice.
- Body dimensions do not incude mold flash, protrusions or gate burrs. Mold flash, interlead flash, protrusions or gate burrs shall not exceed 0.15 per end or side



SMALL OUTLINE TRANSISTOR

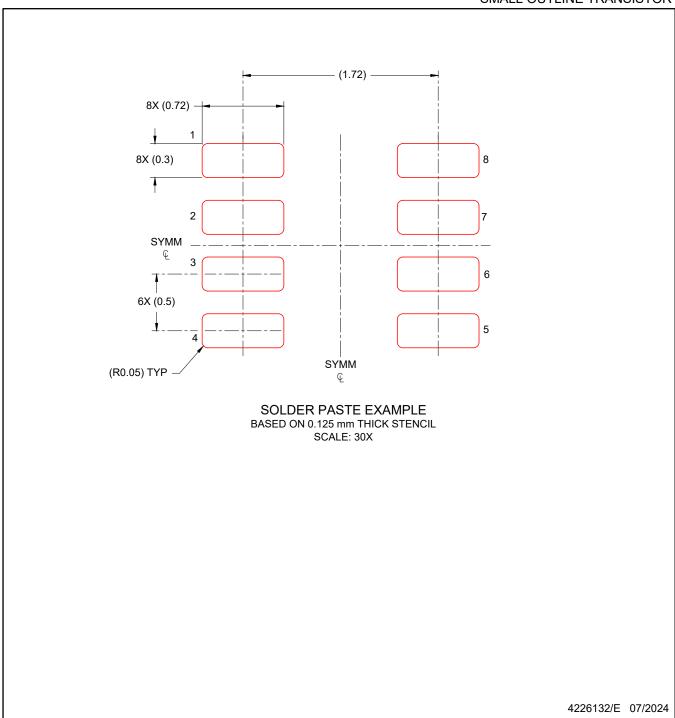


NOTES: (continued)

- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
- 6. Land pad design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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