

Four-Channel, Differential Input, DAQ Front-End Circuit With Configurable Voltage and Current Inputs



Victor Salomon

Feature	Value	Units
Number of channels	4	Differential channels
Data rate	≤10	kSPS
Voltage input range	±10.0	Volts
Current input range	0 to 20	mA
Voltage accuracy	0.05 typical 0.10 maximum	%FS
Current accuracy	0.10 typical 0.20 maximum	%FS

Power Supplies

AVDD	HV-AVDD	HV-AVSS
5.0V	15.0V	-15.0V

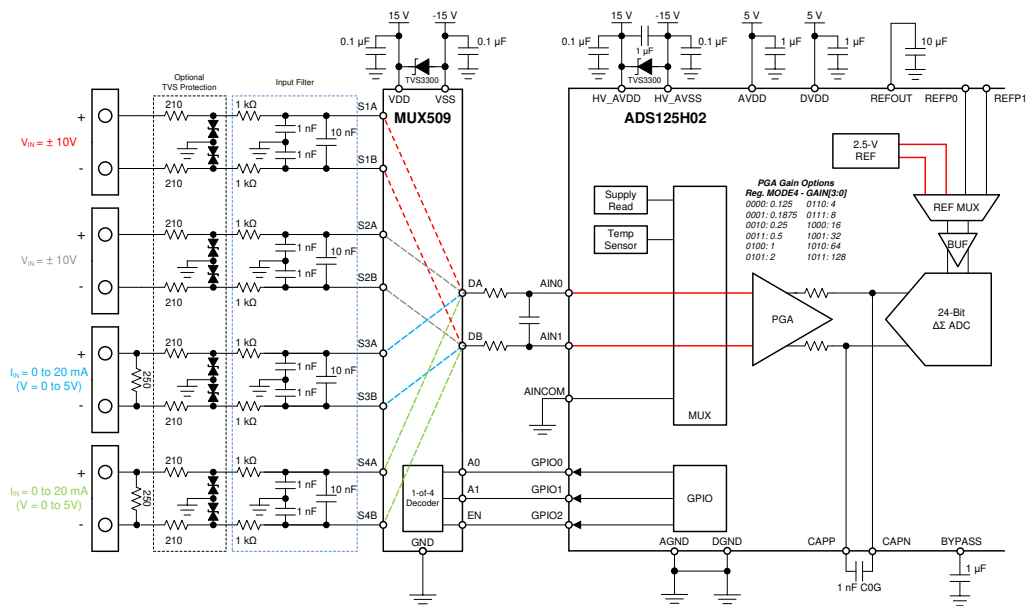
Design Description

This circuit design describes how to use an [ADS125H02](#) with integrated reference and programmable gain amplifier (PGA) to make voltage and current measurements on various ranges.

This circuit can be used in applications such as

1. [Analog input modules](#) for PLCs
2. Avionics [remote data concentrators](#)
3. [Lab and field instrumentation](#)
4. [Test and measurement](#)

Thermocouples and RTD are also common temperature sensors used in similar applications. For more information about making precision ADC measurements with a variety of RTD wiring configurations, see the [A Basic Guide to Thermocouple Measurements Application Report](#).



Design Notes

- Use supply decoupling capacitors for both the analog and digital supplies. For the high-voltage analog supply (HV_AVDD and HV_AVSS), place a 1.0- μ F capacitor between the pins and place 0.1- μ F capacitors from each supply to the ground plane. Connect 0.1- μ F and 10- μ F capacitors in parallel at AVDD to the ground plane. Connect a 1.0- μ F capacitor from DVDD to the ground plane. Connect a 1.0- μ F capacitor from BYPASS to the ground plane. For details on power supply recommendations, see the [ADS125H02 \$\pm\$ 20-V Input, 2-Channel, 40-kSPS, 24-Bit, Delta-Sigma ADC With PGA and Voltage Reference](#) data sheet.
- To minimize input current leakage, connect unused analog inputs to AGND when operating the device with bipolar supplies, or connect unused inputs to AVDD when operating the device with a unipolar supply.
- Program unused GPIOs as outputs (default setting). If any GPIOs are programmed as inputs, the GPIO must not be allowed to float (unconnected), floating can result in AVDD power-supply leakage current.
- Consider adding TVS diodes between the high-voltage supplies (HV_AVDD to HV_AVSS) to provide overvoltage protection and avoid violating the absolute maximum rating of 38V. A TVS diode such as the [TVS3300](#) provides a 33.0-V stand-off voltage (V_R), which is below the 30.0-V supply required, minimizing the current leakage of the diode, but has a typical break-down voltage (V_{BR}) and clamping voltage (V_C) of 35.8V and 38.0V, respectively (assuming a peak pulse current I_{PP} of 35.0A), effectively protecting the ADC from an EOS event. For more details on EOS in ADCs, see [EOS and ESD in ADC](#).
- When possible, use COG (NPO) ceramic capacitors for input filtering. The dielectric used in these capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.
- Input filtering for the ADC inputs and the reference inputs are selected using standard capacitor values and 1% resistor values. For an example design and analysis of these filters, see the [RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices Application Report](#).

Component Selection

- Identify the system components:
 - Given the following specifications are:
 - Input voltage range $\leq \pm 12.0V$
 - Two voltage input channels, and two current input channels
 - Data rate $\leq 10kSPS$
 - 0.05% FS accuracy, or better
 - Optimized for cost
 - Products selected:
 - [ADS125H02](#) is a 24-bit, $\pm 20V$ input, delta-sigma ADC with integrated high-input voltage PGA and voltage reference. This device meets the input voltage range, accuracy, and data rate requirements, and it integrates a precision voltage reference, and GPIOs helping in cost optimization.

- **MUX509** is a differential 4:1, 36V, precision, analog multiplexer. This device enables expanding to 4-channels using a single ADC for cost optimization.
 - Burden resistor: A burden resistor converts the current to a limited voltage to do measurements in the current measurement mode, a 250-Ω resistor was selected given the desired current range measurements (0 to 20mA), and a target burden voltage of 5.0V. Using a precision resistor verifies that the resistor does not become the limiting factor for system accuracy, the following specifications can be used as:
 - Accuracy ≤ 0.1%
 - Temperature coefficient ≤ 20 ppm/°C
 - Power rating ≥ 0.5W
 - Alternative and similar devices are listed in [Design Featured Devices](#).
2. Perform error analysis calculations: A key consideration in the design of an analog input module is the error over the ambient temperature range resulting from the drift of gain, offset, reference voltage, and linearity error. This example shows the results of a Total Unadjusted Error (TUE) analysis that assumes an FS voltage of 10V, and that the initial offset and gain (including reference voltage error) are user calibrated at T_A = 25°C, as well as calibration overtemperature. The following table shows the maximum error, including the drift error of the ADC over the –20°C to 70°C temperature range, before calibration, and after calibration at room temperature, as well as overtemperature.

Maximum Error Before and After Calibration

Specification	Data Sheet Value	Error (ppm)	Error (ppm)
		Including ΔT = 90°C	Assuming Gain and Offset Calibration
Internal VREF initial accuracy (maximum)	0.20%	2000.000	1.325
Internal VREF temperature drift (maximum)	1ppm/°C	90.000	90.000
Internal VREF temperature hysteresis (70 ppm/105°C)	60ppm/°C	60.000	60.000
Quantization noise	172.3nV _{RMS}	0.017	0.017
Noise	53μV _{RMS}	5.300	5.300
INL	0.001%	10.000	10.000
Offset	2500μV	250.000	1.325
Offset temperature drift	2000nV/°C	18.000	18.000
Gain error	0.70%	7000.000	1.325
Gain error temperature drift	4ppm/°C	360.000	360.000
Total error (root sum of squares) [ppm]		7294.124	376.507
Total error (root sum of squares) [%FS]		0.729	0.038

3. Inspecting the data in [Maximum Error Before and After Calibration](#), it is evident that the main contributors to the system total error calculations before any calibration is performed are the initial accuracy of the internal voltage reference, the gain error overtemperature, and the offset voltage, resulting in a total error of 0.729%FS. Assuming gain and offset calibration is performed, reducing the gain, offset, the initial accuracy of the reference to levels in the noise, resulting in the error similar to the ADC noise level, 1.325ppm (assuming average of 16 samples), then the total error can be calculated to be reduced to 0.038%FS. Perform calibration overtemperature to further improve the full-scale accuracy.
4. Calculating PGA gain required: The PGA gain required is determined by the reference voltage and the input voltage range, which is ±10V for the voltage measurements and 5.0V for the current measurements, assuming a burden resistor of 250Ω.

$$\text{Gain}_{\text{Voltage}} = \frac{\pm V_{\text{IN_FSR}}}{V_{\text{REF}}} = \frac{\pm 10\text{V}}{2.5\text{V}} = 0.25\text{V} / \text{V}$$

$$\text{Gain}_{\text{Current}} = \frac{\pm V_{\text{IN_FSR}}}{V_{\text{REF}}} = \frac{5.0\text{V}}{2.5\text{V}} = 0.50\text{V} / \text{V}$$

5. Verify PGA input limitations: As in typical amplifiers the integrated PGA has a maximum allowable input voltage (V_{AINX}), which can be found in the recommended operating conditions table in the [ADS125H02](#) data sheet, and it is determined by the PGA gain, the maximum differential input voltage (V_{IN}), and the minimum value of the high-voltage power supply. Maintain the absolute input voltage (V_{AINX}) within the range as shown in the following equation; otherwise, an incorrect conversion data can result:

$$HV_AVSS + 2.5 + \frac{V_{IN} \times (Gain - 1)}{2} < V_{AINX} < HV_AVDD - 2.5 - \frac{V_{IN} \times (Gain - 1)}{2}$$

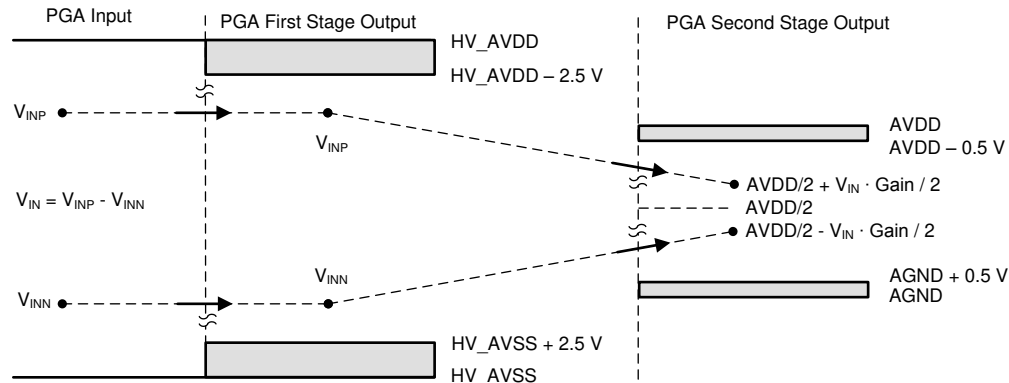
where

- For gain < 1, use value = 1 for gain
- $V_{(AINX)}$ = Input voltage
- $V_{IN} = V_{AINP} - V_{AINN}$ = Maximum expected differential input voltage

In both the voltage and current measurements, since the gain < 1, the absolute input voltage must be:

$$-12.5V < V_{AINX} < 12.5V$$

The following image shows the relationship between the PGA input voltage to the PGA output voltage in attenuation mode. The first PGA stage is configured as a unity-gain follower, the second PGA stage attenuates the differential input and shifts the signal common-mode voltage to $AVDD / 2$ to drive the ADC input.



6. GPIO configuration:

The ADS125H02 device provides four GPIO pins (GPIO0–GPIO4), two GPIOs are available on dedicated pins and two GPIOs are multiplexed functions with an external reference (REFP1 and REFN1). The GPIO input and output levels are referred to AVDD and AGND, so in this case the logic output levels are set to 5.0V. The following bits in registers 3 and 4 are used to control the GPIOs:

- GPIO_CON[3:0] bits set the GPIO connection to the designated pin (1 = connected)
- GPIO_DIR[3:0] bits program the direction of the GPIO as an input (1) or output (0)
- GPIO_DAT[3:0] bits are the data values for the GPIO

In this case, set GPIO_CON[3:0] to '0111', and set GPIO_DIR[3:0] to '1000', while the configuration for GPIO_DAT[3:0] are dependent upon the connected channel. The [MUX509 Truth Table and GPIO_DAT Configuration](#) table shows the configuration of the individual GPIO[x] bits depending on the input channel selected.

MUX509 Truth Table and GPIO_DAT Configuration

EN GPIO2	A1 GPIO1	A0 GPIO0	State
0	1	1	MUX disabled
1	0	0	Channel 1 ON (Voltage)
1	0	1	Channel 2 ON (Voltage)
1	1	0	Channel 3 ON (Current)
1	1	1	Channel 4 ON (Current)

7. Digital filter selection:

Digital low-pass filters are essential to the functionality of a delta-sigma ADC, which relies on oversampling and noise shaping to push quantization noise out of band. There are a variety of options for digital filters available in the ADS125H02 device. When choosing a digital filter, consider the following tradeoffs:

- Slower data rates (higher oversampling ratios) have lower noise bandwidth and are great for noise, but not for data throughput or detection of transient events.
- The built-in PGA monitors are able to assist in detecting transient events that affect the conversion results; therefore, the digital filter is generally able to be run at a slower data rate for better noise performance.
- Higher-order SINC filters have slower settling times when an input step is applied, but provide lower noise bandwidth **and** increased notch width for removing common noise signals, such as power line noise not occurring at exactly 50Hz or 60Hz.
- Digital filter notches occur at intervals of the SINCx filter data rate, so data rates of 50 SPS, 60 SPS or less are recommended for attenuating power line noise.
- The 20 SPS FIR filter is unique from the SINCx filters in that it provides simultaneous rejection of 50- and 60-Hz noise and also settles within a single conversion cycle (like the SINC1 filter).

In this application, TI recommends a low-latency 20SPS using a SINC1 filter, which is shown in the pseudocode example in the following section.

For more information about digital filters in the ADS125H02 device, see the following:

- The *Digital Filter* section of the [ADS125H02](#) data sheet
- [Digital Filter Types in Delta-Sigma ADCs](#) application report

Register Settings

Configuration Register Settings for Voltage and Current Inputs

Register Address	Register Name	Field	Register Value	Description
05h	MODE3	GPIO_DAT[3:0]	See MUX509 Truth Table and GPIO_DAT Configuration	GPIO state (to control the external MUX)
	MODE2	GPIO_DIR[3:0]	1000	GPIO[2:0] outputs, GPIO[3] input
	MODE4	GPIO_CON[3:0]	0111	GPIO[2:0] connected GPIO[3] disconnected
10h	MODE4	MUX[2:0]	000	Internal MUX
10h	MODE4	GAIN[3:0]	0010 or 0011	PGA - Gains for voltage and current measurements, respectively
02h	MODE0	DR[4:0]	00100	Data rate: 20SPS
02h	MODE0	FILTER[2:0]	000	Digital filter: SINC1

Pseudocode Example

The following pseudocode sequence shows the required steps to set up the device and the microcontroller that interfaces to the ADC to take subsequent readings from the ADS125H0x device for both voltage and current measurements. The dedicated $\overline{\text{DRDY}}$ pin indicates the availability of new conversion data. Pseudocode is shown

without the use of the STATUS byte and CRC data verification. Download the [ADS125H02 Example C Code](#) from the [ADS125H02](#) product folder or access it directly with the following link: [ADS125H02 Example C Code](#).

Generic Pseudocode

```

Init:
{
    Configure microcontroller for SPI master, mode 1 (CPOL = 0, CPHA = 1), SCLK freq = 8 MHz
    Configure microcontroller GPIO for /DRDY as a falling edge triggered interrupt input
    Set CS1 low;
    Send 06h 00h A9h 00h;// RESET command to ensure proper reset after power-up
    Set CS1 high;
    // DELAY
    Set CS1 low;
    Send 46h 10h 82h 00h;// WREG to REF: Enable and select the internal 2.5V reference
    Set CS1 high;
    // NOTE: not necessary to issue a WREG to MODE0 command when using the default register values
    Set CS1 low;
    Send 42h 24h 5Ah 00h;// WREG to MODE0: Continuous conversion, low-latency filter, 20 SPS
    Set CS1 high;
    Set CS1 low;
    Send 43h 08h 8Bh 00h;// WREG to MODE1: Continuous conversion, 605us conv. start delay
    Set CS1 high;
    Set CS1 low;
    Send 44h 77h 9Ah 00h;// WREG to MODE2: Enable GPIO outputs on GPIO0, GPIO1, and GPIO2
    Set CS1 high;
    Set channelNumber = 1
    Call Gain_Select()
    Call Channel_Select()
    // (OPTIONAL): For verification read back all register settings
    Call Start_New_Conversion()
}
Loop:
{
    wait for DRDY falling edge interrupt...
    Do you want to switch to the next channel?
    {
        channelNumber = (channelNumber + 1) % 4;
        Call Gain_Select()
        Call Channel_Select()
        Call Start_New_Conversion()
    }
    Call Read_Data()
}
Channel_Select()
{
    // NOTE:
    // A0, A0 and EN are controlled by GPIO0, GPIO1 and GPIO2 respectively
    // STATUS0 byte is always enabled
    Set CS1 low;
    // WREG to MODE3 register to set GPIO pin levels
    If (channelNumber == 1)
        Send 45h 44h 16h 00h;// EN=1; A1=A0=0
    ElseIf (channelNumber == 2)
        Send 45h 45h 11h 00h;// EN=1; A1=0; A0=1
    ElseIf (channelNumber == 3)
        Send 45h 46h 18h 00h;// EN=1; A1=1; A0=0
    ElseIf (channelNumber == 4)
        Send 45h 47h 1Fh 00h;// EN=1; A1=A0=1
    Set CS1 high;
}
Gain_Select()
{
    // NOTE:
    // Using gain of 0.25 v/v for channels 1 & 2
    // Using gain of 0.50 v/v for channels 3 & 4
    // Always select AINP = AIN1 and AINN = AIN0 for analog inputs
    Set CS2 low;
    // WREG to MODE4 register to configure PGA gain
    If (channelNumber <= 2)
        Send 50h 02h D5h 00h;// Gain = 0.25 v/v
    Else
        Send 50h 03h D2h 00h;// Gain = 0.50 v/v
    Set CS2 high;
}
Start_New_Conversion()

```

```

{
    Set CS1 low;
    Send 08h 00h 7Fh 00h;// START command
    Set CS1 high;
}
Read_Data()
{
    Set CS1 low;
    Send 12h 00h AAh 00h 00h 00h 00h 00h;
    Receive FFh 12h 00h AAh [STATUS] [MSB] [MID] [LSB] [CRC]
    Set CS1 high;
    // Cast, concatenate, and sign-extend 24-bit data to signed 32-bit datatype
    signedValue = (((int32_t) [MSB] << 24) + ((int32_t) [MID] << 16) + ((int32_t) [LSB] << 8)) >> 8;
    // Convert ADC value to voltage (LSBsize = 2*VREF/GAIN)
    // NOTE:
    // Using gain of 0.25 V/V for channels 1 & 2
    // Using gain of 0.50 V/V for channels 3 & 4
    VoltageReading = (LSBsize * signedValue);
    If (channelNumber > 2)
        CurrentReading = (VoltageReading / BurdenResistance);
}

```

Design Featured Devices

Design Featured Devices

Device	Key Features	Link	Other Possible Devices
Analog to Digital Converter (ADC) with Integrated PGA and Voltage Reference			
ADS125H02	24-bit, 40kSPS, 2-channel delta-sigma ADC with ± 20 -V input, PGA, IDACs, GPIOs, and VREF	24 bit, 40kSPS, 2-ch delta-sigma ADC with ± 20-V input, PGA, IDACs, GPIOs and VREF	Precision ADCs
ADS125H01	24-bit, 40kSPS, 1-channel delta-sigma ADC with ± 20 -mV to ± 20 -V input	24 bit, 40kSPS, 1-ch delta-sigma ADC with low-noise PGA and ± 20-V input	
Programmable Gain Amplifier (PGA)			
PGA280	4-channel, zero-drift, high voltage, programmable gain amplifier (PGA)	Zero Drift, HV Programmable Gain Amplifier	Analog switches and muxes
PGA281	1-channel, zero-drift, high voltage, programmable gain amplifier (PGA)	Zero-Drift, High Voltage Programmable Gain Amplifier	
Analog Multiplexer			
MUX509	Differential or dual 4:1, 36.0-V, precision analog multiplexer	6.7-pF on-state capacitance, 36V, 4:1, 2-channel analog multiplexer	Analog switches and muxes
MUX36D04	Differential or dual 4:1, 36.0-V, precision analog multiplexer <i>Lower leakage current</i>	1-pA on-state leakage current, 36V, 4:1, 2-channel precision analog multiplexer	
TMUX6104	Single-ended 4:1, ± 16.5 -V, precision analog multiplexer <i>Lowest leakage current, lowest on-capacitance</i>	5-pA on-state leakage current, ± 16.5V, 4:1, 1-channel precision analog multiplexer	
CD4052	Differential or dual 4:1, ± 10.0 -V analog multiplexer <i>Lowest cost</i>	20V, 4:1, 2-channel general-purpose multiplexer	

Power Supply Reference Designs

The ADS125H02 device requires three analog power supplies (high-voltage supplies HV_AVDD and HV_AVSS, and low-voltage analog supply AVDD) and a digital power supply (DVDD). This circuit assumes a bipolar supply (± 15.0 V) for HV_AVDD and HV_AVSS, and a 5.0-V supply. The following table shows there are specifications for three reference designs that can provide the power supplies from a 24.0-V nominal input voltage.

		PMP10532	PMP10516	TIDA-00689
		Schematic Test Results	Schematic Test Results	Schematic Design Guide
V_{IN} range (V)		19.0–30.0V	20.4–28.8V	16.0–32.0V
Input type		DC		
V_{OUT} (V)	Output 1	15.0		
	Output 2	–15.0		
	Output 3	5.00		
I_{OUT(maximum)} (A)	Output 1	0.200	0.200	0.601
	Output 2	0.200	0.060	0.601
	Output 3	1.000	0.100	0.200
P_{OUT(maximum)} (W)	Output 1	3.0	3.0	0.5
	Output 2	3.0	0.9	
	Output 3	5.0	0.5	
Isolation		✓	✓	✓
Total efficiency at V_{IN} = 24V and Maximum I_{OUT}		86.0%	78.8%	44.0%
Footprint		60.0mm × 30.0mm	Approximately 60.0mm × 35.0mm	12.7mm × 40.8mm
Topology		Fly-Buck™	Fly-Buck™ + Linear regulator	Fly-Buck™ + Split rail converter

Trademarks

Fly-Buck™ is a trademark of Texas Instruments.
 All trademarks are the property of their respective owners.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated