Application Note

Discrete DESAT for Opto-Compatible Isolated Gate Driver UCC23513 in Motor Drives

Jerome Shan, Martin Staebler, Roland Bucksch *Systems Engineering Industrial*

ABSTRACT

Reinforced isolated gate drivers are key components in 3-phase inverters for industrial motor drives, and DESAT is a popular approach for overcurrent protection (OCP) or short circuit protection (SCP) in these applications. This application note presents a small form factor, cost-optimized design based on the 6-pin opto-compatible reinforced isolated gate driver UCC23513 with a discrete DESAT implementation using the isolated comparator AMC23C11. This combination achieves a smaller PCB size and lower cost, compared to the 16-pin package smart gate drivers with integrated DESAT protection, and helps to enhance flexibility in applications of compact motor drives. The design also keeps the flexibility to configure the application parameters of the DESAT function.

Table of Contents

List of Figures

Trademarks

PSpice™, C2000™, and LaunchPad™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

1 Introduction

In 3-phase inverters for motor drives, OCP and SCP are critical to protect the system from damage caused by abnormal operating conditions. Shunt-based system level OCP or SCP are often implemented by sensing the current through the negative DC bus or the three low-side switches; especially in many lower power, compact models, where form factor and system cost are critical. These protections are effective for the commonly seen fault patterns of arm shoot-through and phase-to-phase short. However, neither of them can detect an earth ground short when the fault current flows through a high-side switch, as shown in Figure 1-1. A DESAT function on the gate driver can help to protect the power switch against this fault. In fact, device level DESAT protection is effective to all these fault modes in a 3-phase inverter, thus has been widely used in many high power, high performance models.

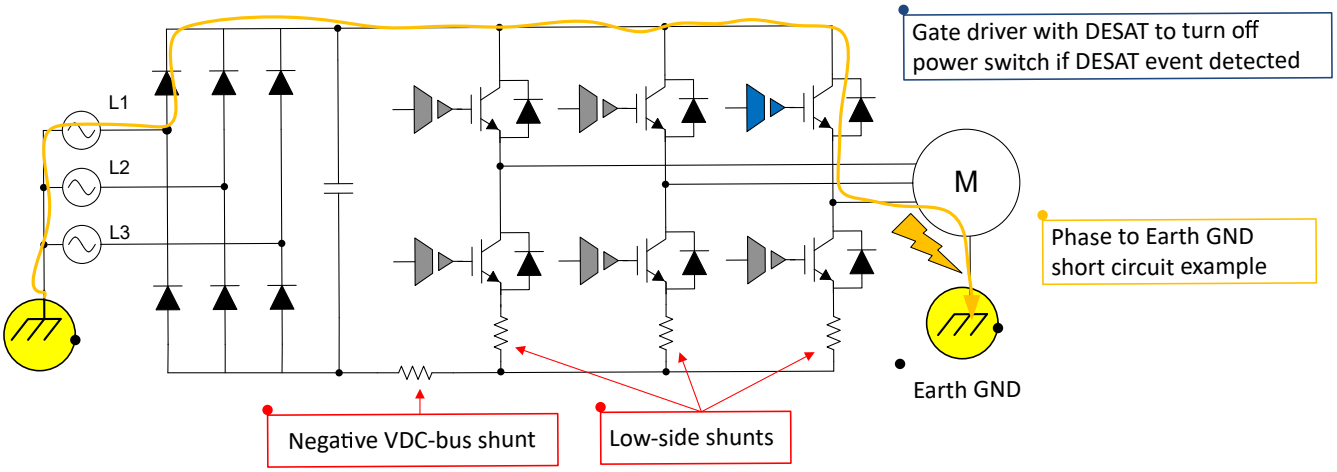

Figure 1-1. Short Circuit Due to Earth Ground Fault in A 3-Phase Inverter

Many industrial motor drives also have a regeneration brake switch to shunt the current to the negative VDC-bus and discharge the bulk capacitor when the voltage goes too high during a regeneration brake operation. Often this brake resistor needs to be installed externally and then connected to the system by a specific terminal on the drive. If a user makes an error in connecting this resistor, or mistakenly used one with a very low resistance, an overcurrent fault can occur once a brake operation is started by the system controller, as shown in Figure 1-2. In this case, a DESAT function on the gate driver can detect the problem and protect the power switch in time.

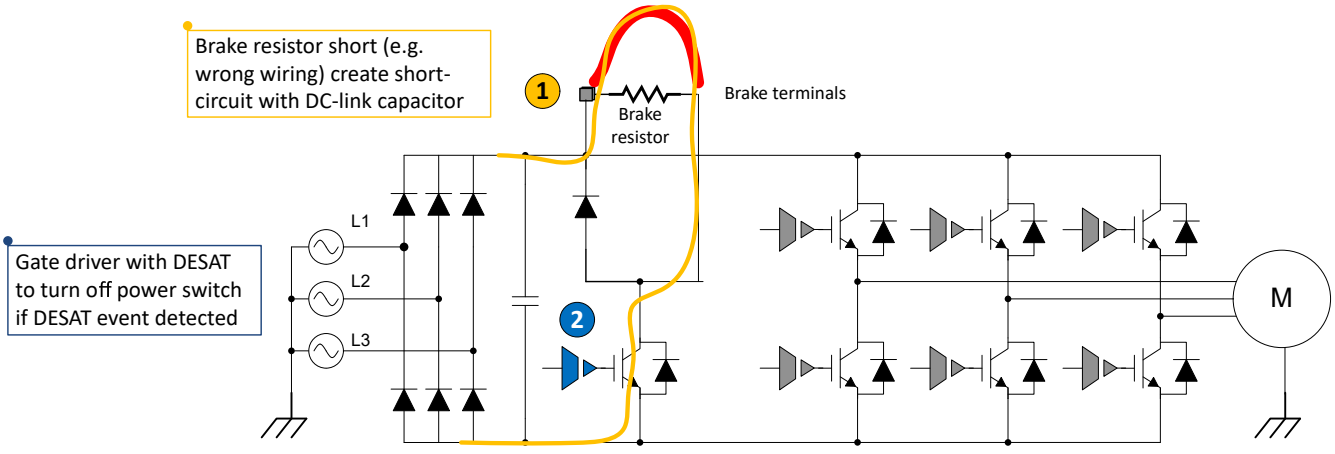

Figure 1-2. Short Circuit Due to Miswiring of External Brake Resistor Terminal

A typical approach to protect the system against these faults uses an isolated smart gate driver with DESAT function, like the UCC21750 reinforced isolated gate driver with CMOS input. As seen in Figure 1-3, a DESAT pin monitors the voltage drop of V_{CE} when the IGBT is turned ON. Once this voltage drop goes up and reaches

the set threshold, which means an over current or short circuit condition is happening, the output of the gate driver will be pulled to low at once and a fault output wii be activated to inform the system controller on the fault.

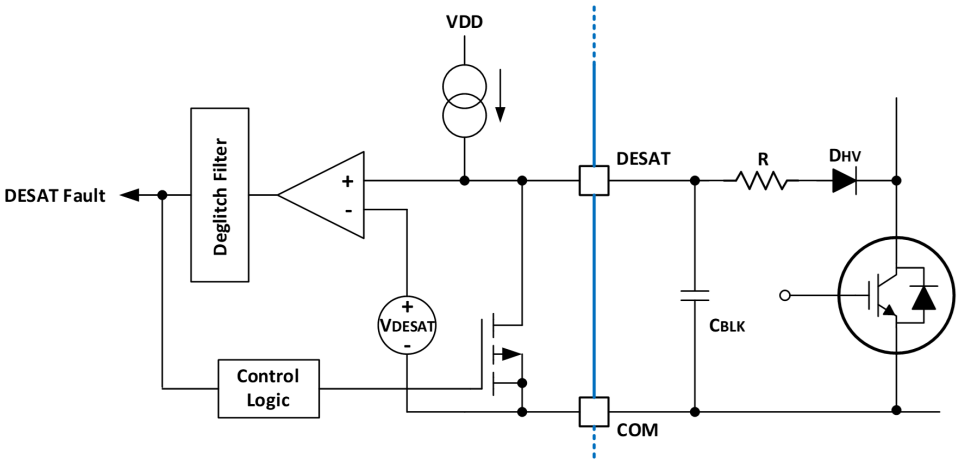

Figure 1-3. UCC21750 With Integrated DESAT Protection

2 System Challenge on Isolated Gate Drivers With Integrated DESAT

Reinforced isolated smart gate drivers with integrated DESAT function are typically offered in a 16-pin SOIC package, which is physically much larger than a compact gate driver without DESAT function in a stretched SO-6 package, as is shown in Figure 2-1. Consider placing six pieces of such devices of a 3-phase inverter on a power inverter PCB, the package length will stack up accordingly. A design using a shorter length compact device can offer an advantage on the PCB size. Even for a regeneration brake power switch, a smaller size gate driver can help to reduce the application layout area significantly. However, such gate drivers sacrifice the overcurrent protection function for application circuit simplicity and cost reasons.

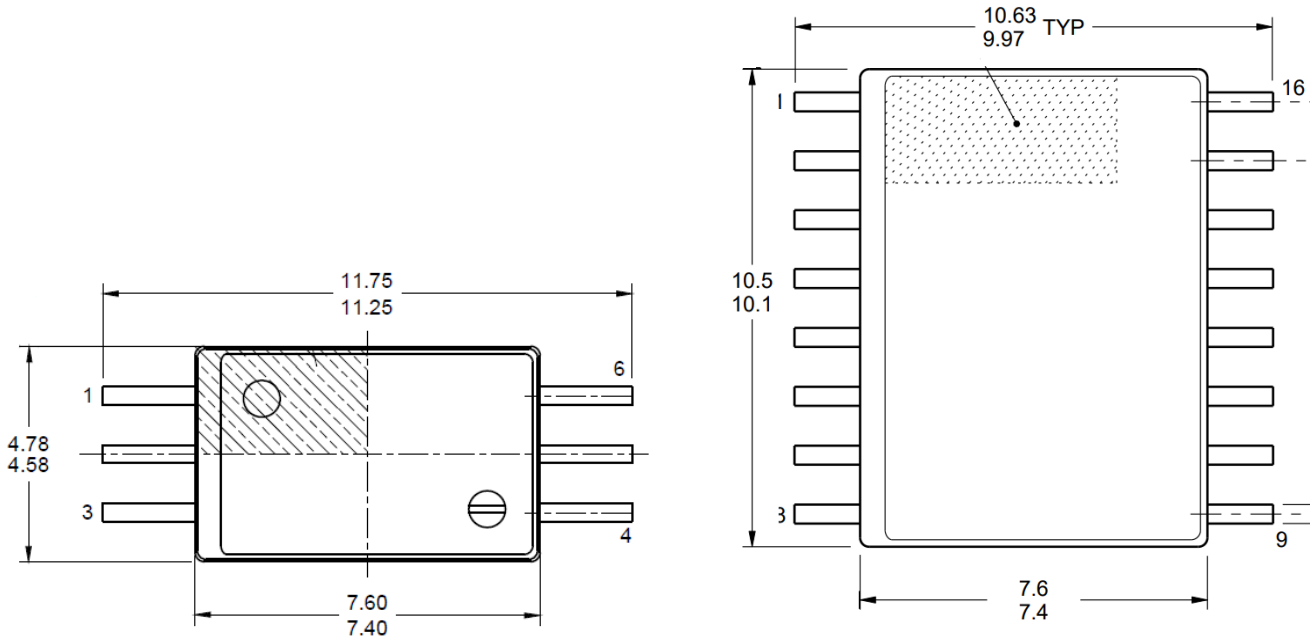

Figure 2-1. Package Size Comparison: SO-6 vs. SOIC-16

An alternative approach is to use the smaller footprint compact gate driver without DESAT and implement the DESAT function discretely using an isolated comparator.

For circuit configurations that only require DESAT function on either the three low-side switches or the three high-side ones, this discrete DESAT design allows all six switches to use a same 6-pin reinforced isolated gate driver; thus avoids mixing simple gate drivers with smart gate drivers in one application system. The external DESAT function can be added to the low-side or high-side gate drivers, respectively. This discrete DESAT implementation adds flexibility to the application design to configure parameters of DESAT voltage, DESAT bias current, DESAT detection blanking time, and DESAT output deglitch filter, thus helps to increase immunity against the PWM switching noise.

3 System Approach With UCC23513 and AMC23C11

The UCC23513 is a 4-A source, 5-A sink, 5.7-kV_{RMS} reinforced isolated, opto-compatible single channel gate driver. The AMC23C11 is a fast response, reinforced isolated comparator with adjustable threshold and latch function. Using the two devices together, we can achieve an external DESAT on the compact gate driver and maintain a small circuit form factor with reinforced isolation.

3.1 System Overview and Key Specification

Figure 3-1 shows a simplified block diagram of the proposed circuit. Here, we use an IGBT as the power switch; and the design is also appropriate for a power MOSFET with some minor changes.

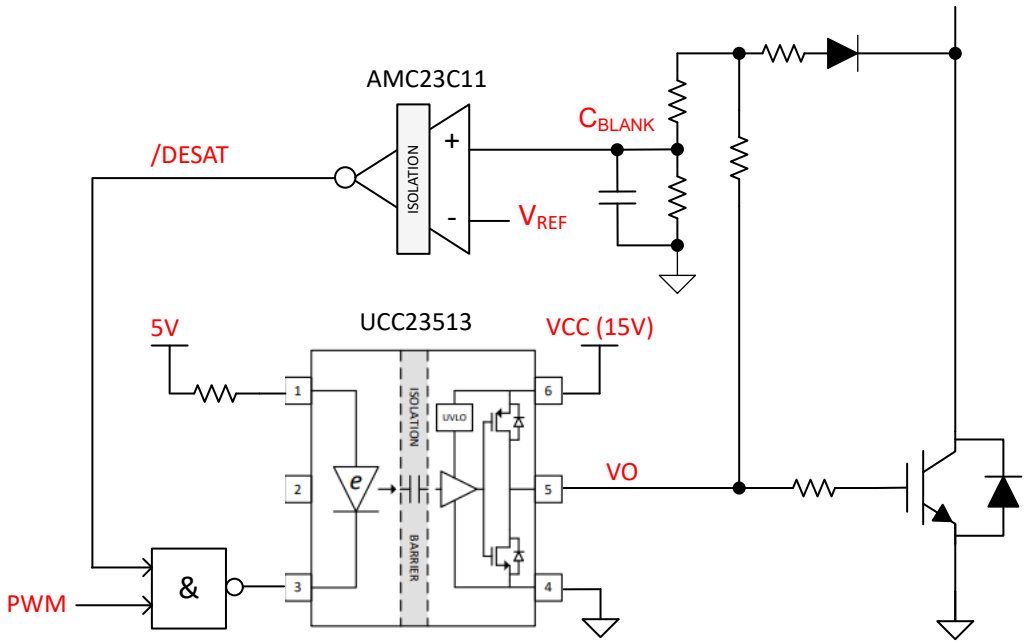

Figure 3-1. Simplified System Block Diagram

A NAND gate is used to realize a function to monitor the V_{CE} only when the PWM input is high. The chip disables the gate driver's input, once the sensed V_{CE} exceeds the DESAT threshold VREF. Table 3-1 shows the key parameters of the application circuit.

Table 3-1. Key System Parameters of the Design

Parameter	Value	Comment
Reinforced isolated gate driver	UCC23513 or UCC23511(1)	6-pin DWY (SO-6) package, see figure 2-1. B version to support 8-V UVLO.
Isolated gate drive supply, VDD	+15 V (IGBT), +12 V (FET)	Unipolar supply
DESAT V_{CE} threshold voltage, $V_{CE(DESAT)}$	8.0 V	Configurable. See section 3.2.2.
DESAT bias current, $i_{BIAS(DESAT)}$	5.5 mA	Configurable. See section 3.2.2.
DESAT blanking filter time constant, t_{BLANK}	0.8 µs	Valid for $V_{CE(SAT)}$=12.5V. Configurable. See equation 8 and table 3-2 in section 3.2.3.
DESAT deglitch filter delay, $t_{DEGLITCH}$	0.2 µs	Configurable. See equation 10 in section 3.2.3.
DESAT latch with reset	Enabled	Can be disabled.
DESAT reaction time(2)	About 1.1 µs to 1.6 µs	By default configuration. Refer to test results.

Table 3-1. Key System Parameters of the Design (continued)

Parameter	Value	Comment
PCB size without connectors	26 mm x 8.4 mm	

Note

(1) UCC23511 is a 1.5-A source, 2-A sink device in same package as UCC23513.

(2) For clear and simple description on the protection process, in this application note, we use 'DESAT reaction time' for the period from the sensed power switch's current reaches to the set trigger level to the point the current begin to drop due to the DESAT protection.

The UCC2351x series can be used to drive power switches of IGBT, SiC, or MOSFET. Both UCC23511 and UCC23513 are offered in a stretched SO-6 package of 7.50 mm x 4.68 mm body size, with greater than 8.5 mm creepage and clearance. Both devices bring significant performance and reliability upgrades over the standard optocoupler based gate drivers while maintaining pin-to-pin compatibility. Their performance advantages include high CMTI, low propagation delay, and small pulse width distortion. The input stage is an emulated diode (ediode) which provides long term reliability and excellent aging characteristics over the traditional LEDs.

The AMC23C11 isolated comparator comes in a 8-pin wide-body SOIC package with a body size of 5.85 mm × 7.50 mm. The device compares the input voltage on the VIN pin against a threshold, adjustable from 20 mV to 2 V, and set by an internal 100-µA reference current and an external resistor. The open-drain output is actively pulled to low when the input voltage VIN is higher than the reference value VREF. When VIN drops below the trip threshold, the device's behavior is determined by the LATCH pin:

- When the LATCH pin is pulled to low, the device is set to transparent mode, allowing the output state to change and follow the input signal with respect to the trip threshold.
- When the LATCH pin is pulled to high, the device is set to latch mode. Once an out-of-range condition is detected, the OUT pin is pulled to low and latched, until the LATCH pin is pulled to low for at least 4 µs to release this latch.

The isolation barrier in AMC23C11 is highly resistant to magnetic interference, and certified to provide a reinforced galvanic isolation of up to 5 kV_{RMS}.

3.2 Schematic Design

Figure 3-2 shows the schematic of a design with a 15-V unipolar supply to drive an IGBT. With some minor changes this design can be fit to a 12-V power supply design for power MOSFETs driving or bipolar power supply applications. See reference design TIDA-00448 for more details.

Resistors R9 through R14 and the high voltage diode D1 are used to sense the actual V_{CE} of the IGBT during the turn-on period and scale it according to the reference voltage VREF of the isolated comparator AMC23C11. R10 and R11 are in parallel to spilit the power dissipation.

The capacitor C14 in parallel to R14 sets a blanking time to avoid false trig during the IGBT turn-on. A 5.1-V Zener diode D2 is added as an option to suppress possible high voltage spikes due to the IGBT switching. Note that the internal capacitance of D2 will be in parallel to C14 and contribute to the blanking time. In our tests we did not assemble this D2. A fast switching diode D1 with low internal capacitance is recommended to avoid false DESAT trigger and minimize the blanking time required.

The low voltage side uses a 3.3-V supply to directly interface the I/O level of popular MCUs, like the C2000™ and the Sitara MCUs. R6 and C11 set a deglitch delay (default 0.2 µs) for the comparator's output, in case of the LATCH is not activated.

3.2.1 Circuit Schematic

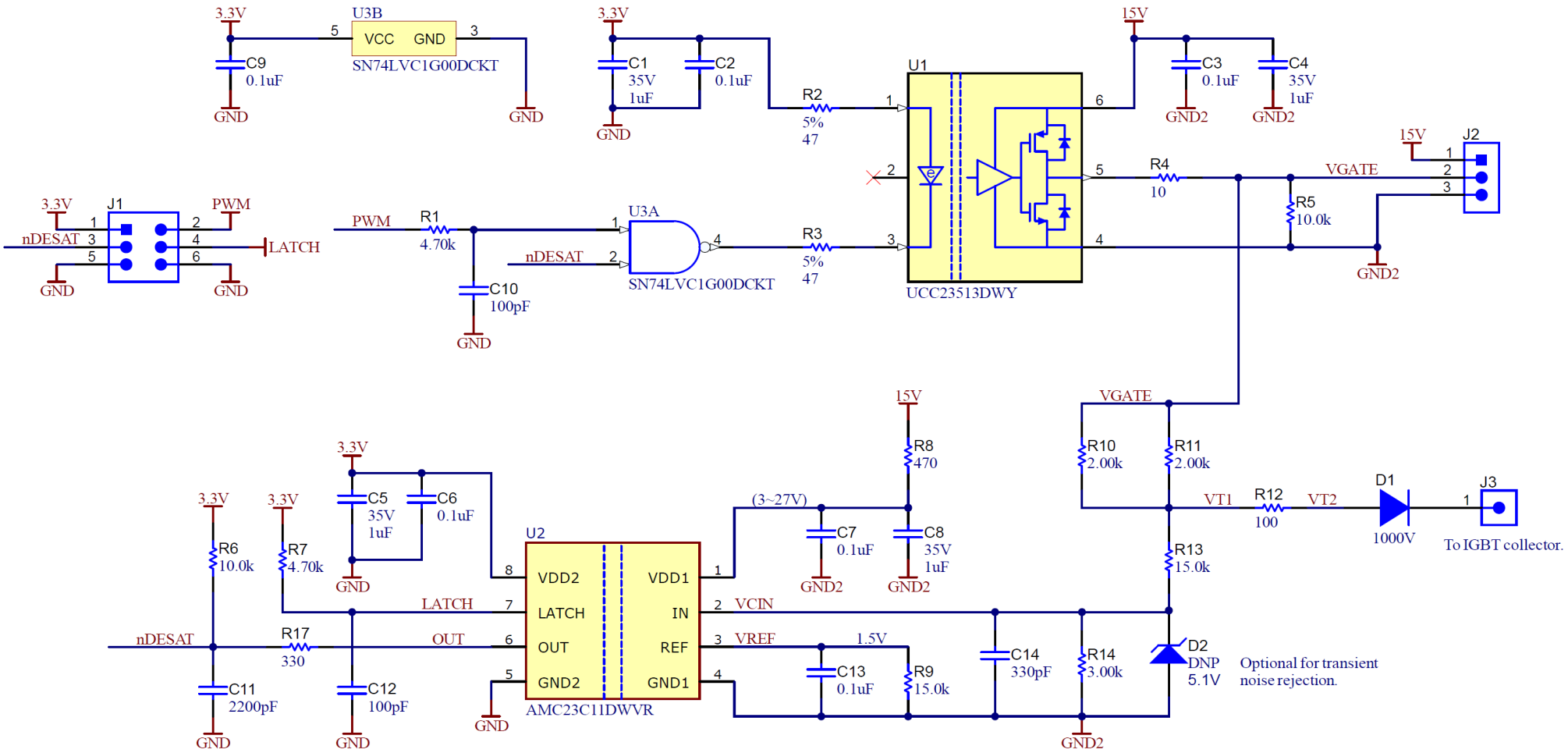

Figure 3-2. Schematic of the Proposed Circuit

3.2.2 Configure $V_{CE(DESAT)}$ Threshold and DESAT Bias Current

Resistors R9 to R14 can be used to adjust the $V_{CE(DESAT)}$ threshold and the DESAT bias current $i_{BIAS(DESAT)}$. The following equations are simplified for a quick estimation on their values for different DESAT threshold and DESAT bias current configurations.

The isolated comparator AMC23C11 has a reference voltage VREF which is set by an internal 100 µA current source and the external resistor R9. The value of R9 is calculated per Equation 1 to set the VREF to 1.5 V in this design. Here 1.5 V is chosen to make the AMC23C11 to operate in the high-hysteresis mode[1].

$$\mathrm{R9} = \frac{VREF}{100\ \mu\mathrm{A}} = 15\ \mathrm{k\Omega} \tag{1}$$

R10 and R11 determine the DESAT bias current and are calculated per Equation 2:

$$\mathrm{R10} = \mathrm{R11} = 2 \times \frac{VDD - V_{CE(DESAT)} - V_{FW(D1)} - R12 \times i_{BIAS(DESAT)}}{i_{BIAS(DESAT)} + i_{R13R14(DESAT)}} \tag{2}$$

Here:

- VDD is the UCC23513's supply voltage; 15 V in this case for IGBT driving;
- $V_{CE(DESAT)}$ is the desired DESAT threshold; 8 V by default in this design;
- $V_{FW(D1)}$ is the forward voltage of the high-voltage diode D1; assumed to be 0.5 V;
- R12 is set to 100 Ω as a common practice[9];
- $i_{R13R14(DESAT)}$ is the current through R13 and R14. Set to 0.5 mA. Lower setting may reduce noise immunity.
- $i_{BIAS(DESAT)}$ is DESAT bias current when the IGBT's V_{CE} reaches $V_{CE(DESAT)}$. Set to 5.5 mA in this design.

So R10 and R11 could be calculated at 2 kΩ for this design.

The power rating of R10 and R11 needs to be selected for normal IGBT operation, where the $V_{CE(DESAT)}$ is significantly smaller. Assuming R12 << R10, the simplified maximum power losses are per Equation 3:

$$P_{R10,\ MAX} = P_{R11,\ MAX} = \frac{\left(VDD - V_{FW(D1)} - R12 \times i_{BIAS(DESAT)} - V_{CE(SAT)}\right)^2}{R10} \times PWM_{DUTY,\ MAX} \tag{3}$$

With the default settings in table 3-1 and a typical $V_{CE(SAT)}$ of 1.5V, the maximum power losses of $P_{R10(MAX)}$ and $P_{R11(MAX)}$ are around 69.8 mW even at 1000% PWM duty cycle.

R13 and R14 are calculated per Equation 4 and Equation 5:

$$\mathrm{R13} = \frac{VREF}{i_{R13R14(DESAT)}} \tag{4}$$

$$\mathrm{R14} = \frac{VDD - \left(i_{BIAS(DESAT)} + i_{R13R14(DESAT)}\right) \times R10 \div 2}{i_{R13R14(DESAT)}} - R13 \tag{5}$$

Applying the parameters' values, we can get R13 of 3 kΩ and R14 of 15 kΩ.

3.2.3 DESAT Blanking Time

The blanking time for DESAT monitoring, the t_{BLANK} , is required to prevent false trig at the turn-on event of the IGBT. Capacitor C14 and resistors of R10 to R14 delay the V_{CE} sensing signal to reach the isolated comparator's input VCIN. The delay is controlled by the charging time of C14 through the equivalent resistance R_{EQ} of the voltage divider R13 and R14:

$$R_{EQ} \approx R13\ //\ R14\ = 3\ \mathrm{k\Omega}\ //\ 15\ \mathrm{k\Omega}\ =\ 2.5\ \mathrm{k\Omega} \tag{6}$$

Choose a C14 of 330 pF, then the time constant of the RC filter is:

$$T_{au} = R_{EQ} \times C14 = 2.5\ \mathrm{k\Omega}\ \times\ 330\ \mathrm{pF}\ =\ 0.82\ \mu\mathrm{s} \tag{7}$$

The actual blanking time depends on the ratio of the configured $V_{CE(DESAT)}$ steady state threshold over the actual $V_{CE(SAT)}$ voltage of the IGBT in an over-current event, and can be approximated per Equation 8.

$$t_{BLANK} = -\ln\left(1 - \frac{V_{CE(DESAT)}}{V_{CE(SAT)}}\right) \times R_{EQ} \times C14 \quad (8)$$

Therefore, it is important to adjust the steady state $V_{CE(DESAT)}$ threshold and the blanking time constant according to the individual IGBT used in the system. Refer to below table for some values with the default settings of the $V_{CE(DESAT)}$ steady state threshold at 8 V:

Table 3-2. Effective Blanking Time With Default $V_{CE(DESAT)}$ Setting

IGBT $V_{CE(SAT)}$ [V]	≥ 14.5	12.5	11	10	9	8.5
t_{BLANK} [µS]	0.7	0.9	1.1	1.4	1.9	2.4

CAUTION

Avoid to configure the steady state threshold $V_{CE(DESAT)}$ too close to the IGBT's actual $V_{CE(SAT)}$ in an over-current condition, since the effective blanking time will be significantly larger than the configured blanking time constant.

3.2.4 DESAT Deglitch Filter

R17 and C11 form a deglitch filter for the nDESAT output signal with a time constant:

$$\tau = 330\,\Omega \times 2200\,\text{pF} = 726\,\text{ns} \quad (9)$$

When a TTL logic IC with a minimum low-level input of 0.8 V is followed, the deglitch time is merely 0.2 µs:

$$t_{DEGLITCH} = -\ln\left(1 - \frac{0.8\,V}{3.3\,V}\right) \times \tau = 202\,\text{ns} \quad (10)$$

Consider the isolated comparator's internal resistance on the OUT pin is in series with R17, the tested deglitch time is about 340 ns to 380 ns in this design. Refer to test results in section 4 for details.

3.3 Reference PCB Layout

A reference layout is made for this circuit with an active area of 26 mm x 8.4 mm on a four-layer PCB.

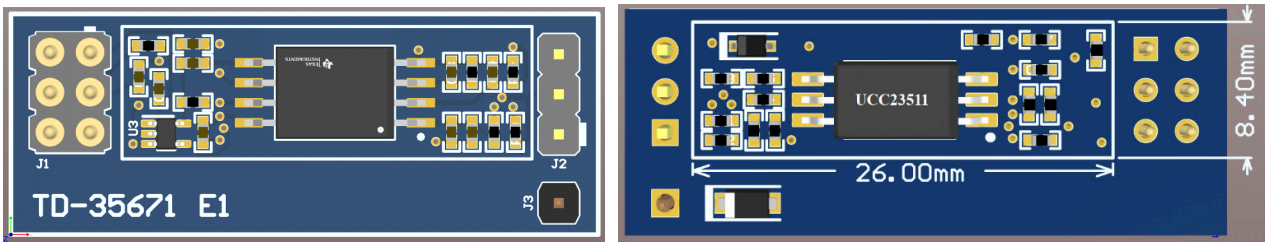

Figure 3-3. Top and Bottom Sides of the Example Layout

With careful layout design placing the gate driver and the comparator on the opposite sides of the PCB, a smaller form factor is achieved, compared to a 16-pin smart gate driver's, taking advantage of their smaller package lengths. In comparison, a typical layout of ISO5451, a smart gate driver with CMOS input in a SOIC 16 package, has an active area of 20.83 mm x 12.95 mm on the PCB[10], as shown in Figure 3-4, which is about 23.5% bigger than the proposed design of UCC23513 and AMC23C11 in Figure 3-3.

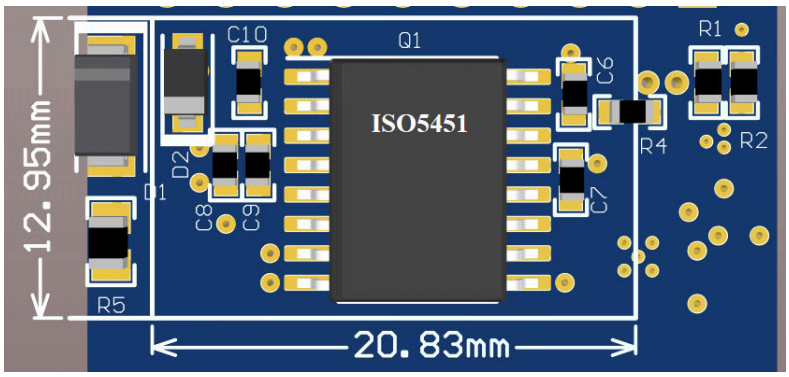

Figure 3-4. Typical Layout of the Smart Gate Driver ISO5451

4 Simulation and Test Results

4.1 Simulation Circuit and Results

Simulations have been made for the circuit to drive a low side IGBT of an active brake circuit in PSpice™ for TI. Figure 4-1 shows the schematic for the simulation.

The simulation uses an AMC23C14's PSpice™ simulation model as the model of AMC23C11 is yet unavailable on ti.com. For the DESAT implementation discussed in this application note, the circuitry connected to the OUT2 (pin7) in the schematic can be ignored, and the AMC23C14 shows the same behavior as the AMC23C11 with the LATCH input (pin7) tied to low.

4.1.1 Simulation Circuit

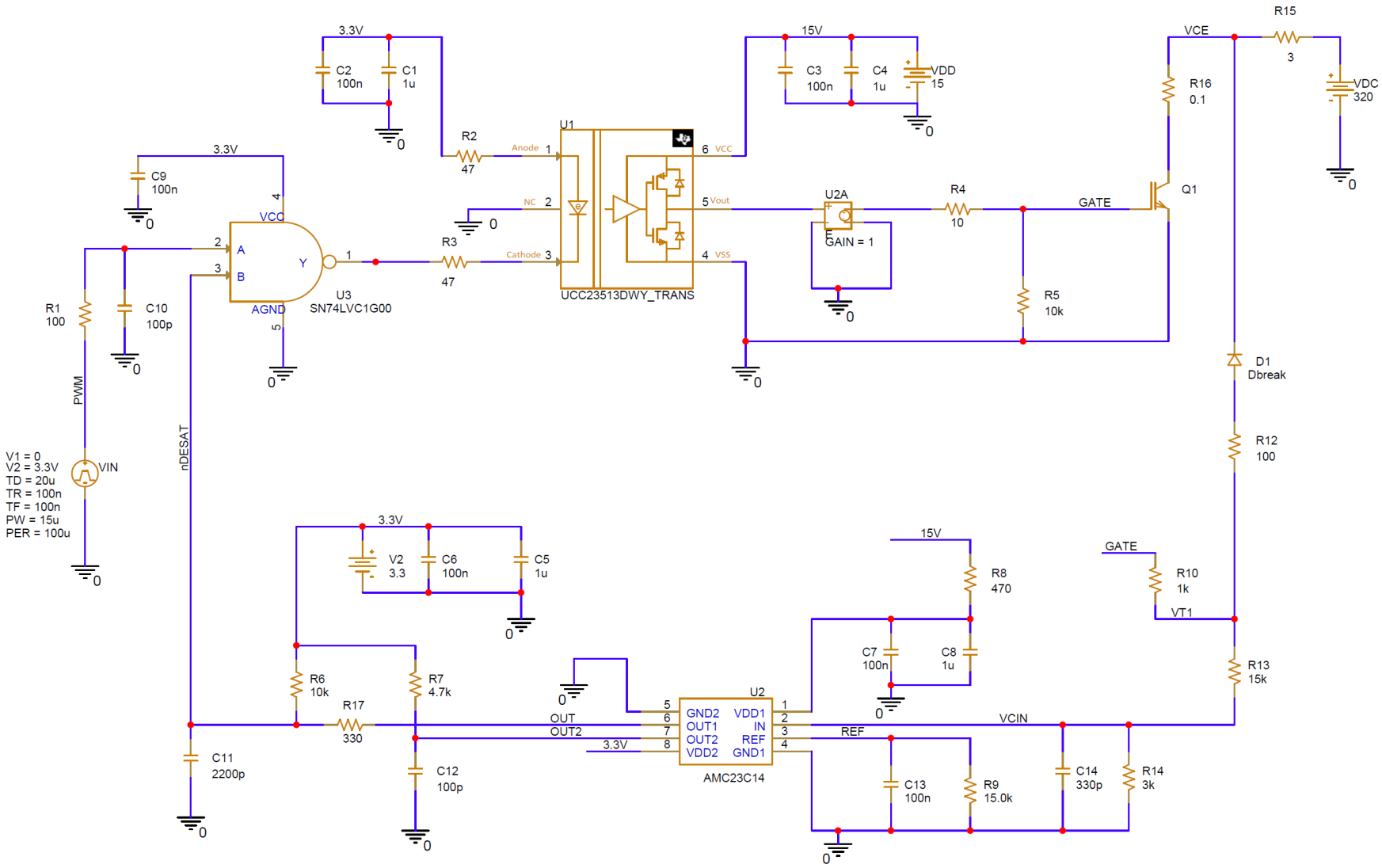

Figure 4-1. Simulation Circuit

4.1.2 Simulation Results

In this simulation, the input PWM signal is set to 10 kHz, 15% duty cycle square waveform. Other conditions are set to a common application situation. Figure 4-2 is a simulation result on a DESAT protection case.

In static state, the PWM input is low, so the NAND gate output is high. UCC23513 has no input current, so the output on the GATE is also low. Thus, the isolated comparator AMC23C11's input voltage of VCIN is pulled to zero; the output OUT and the nDESAT are pulled to high.

When the input PWM signal goes to high, the NAND gate's output will shift to low, as long as the nDESAT is still in high. The UCC23513 then gets the input current and outputs high on the GATE. Then the IGBT U4 turns on and the V_{CE} drops to the $V_{CE(SAT)}$. A sense current flows from GATE through R10, R12 and D1 to the collector of the IGBT U4, makes the VT1 node's voltage follow the IGBT's actual V_{CE} and the VCIN voltage follow the VT1 voltage through the resistor divider of R13 and R14. In case the VCIN does not reach the threshold of VREF, the comparator's output OUT and the filtered output nDESAT will remain at high.

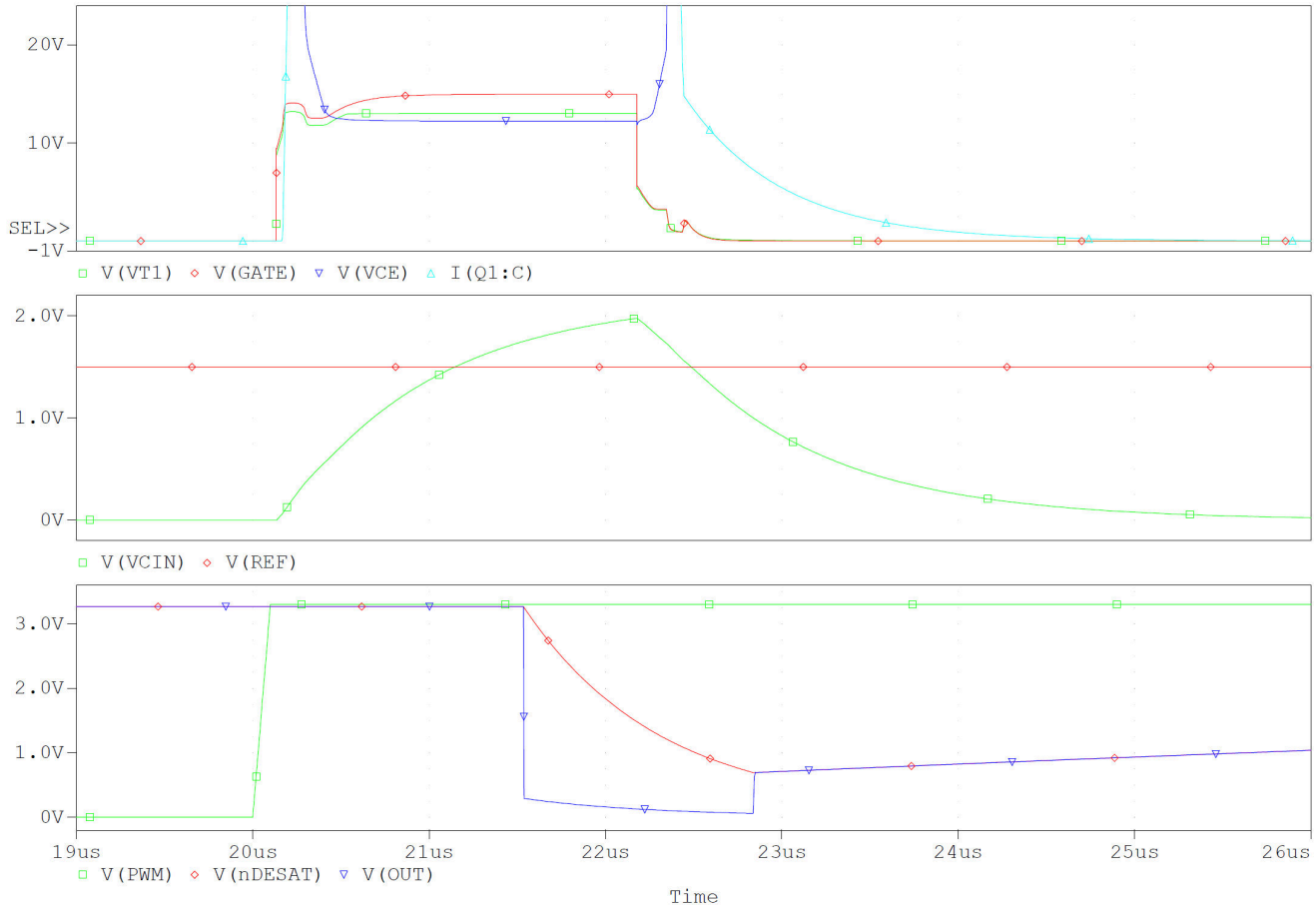

Figure 4-2. Simulation Result of DESAT Triggered

In case of a DESAT triggered process, as shown in the above figure, when the input PWM signal (green trace in the bottom plot) goes to high, the GATE voltage of the IGBT (the red trace in the top plot) will rise up soon after, and the IGBT's V_{CE} sense voltage VT1 (green trace in the top plot) will also rise up. The comparator's input VCIN (the green trace in the middle plot) will then begin to rise up to follow the VT1 voltage in proportional.

Then the IGBT's V_{CE} (blue trace in the top plot) begins to drop. When V_{CE} drops to below the GATE voltage, the VT1 voltage begin to follow the V_{CE}.

Before the VCIN reaches the 1.5 V trigger threshold, set by the VREF (the red line in the middle plot), the comparator's output OUT (the blue trace in the bottom plot) will remain at high. Once VCIN reaches the trigger level, the comparator's OUT will be pulled to low with an internal propagation delay of 240 ns typically. The filtered output of nDESAT (the red trace in the bottom plot) will begin to drop, too.

As an input to the NAND gate U3, once the nDESAT triggers the negative going threshold of U3, the gate driver U1's input current will be cut off and the output GATE will be pulled down. Thus the IGBT will also be turned off and the V_{CE} will rise up soon. This process is the DESAT protection of the circuit.

As the GATE is pulled down, the VT1 will also be pulled down and the VCIN will begin to drop. When VCIN drops to below the threshold of the comparator's input, the OUT will rise up again. This is the case with AMC23C14.

The AMC23C11 behaves exactly the same as the above process when pin 7, the LATCH input, is tied to low. When the LATCH pin is pulled to high, the output low on the comparator's OUT pin will be latched; untill the LATCH pin is pulled to low for at least 4 µs to release the latch state.

4.2 Test Results With 3-Phase IGBT Inverter

Tests have been conducted on a sample board of the proposed circuit on DESAT protection. Two cases were tested, in which the sample board was used as (1) the gate driver of a low-side brake IGBT, and (2) the gate driver of a high-side switch IGBT in a 3-phase motor drive inverter.

4.2.1 Brake IGBT Test

Figure 4-3 shows the platform for the low-side brake IGBT gate driving tests. A C2000™ LaunchPad™ of LAUNCHXL-F28379D has been used as the system controller to generate a series of PWM pulses of 10 kHz with 10% duty cycle, or 10 µs ON time in each 100 µs period, to drive a low-side IGBT. The LaunchPad also generates a high output for the LATCH input of the AMC23C11 and monitors the nDESAT signal with a GPIO.

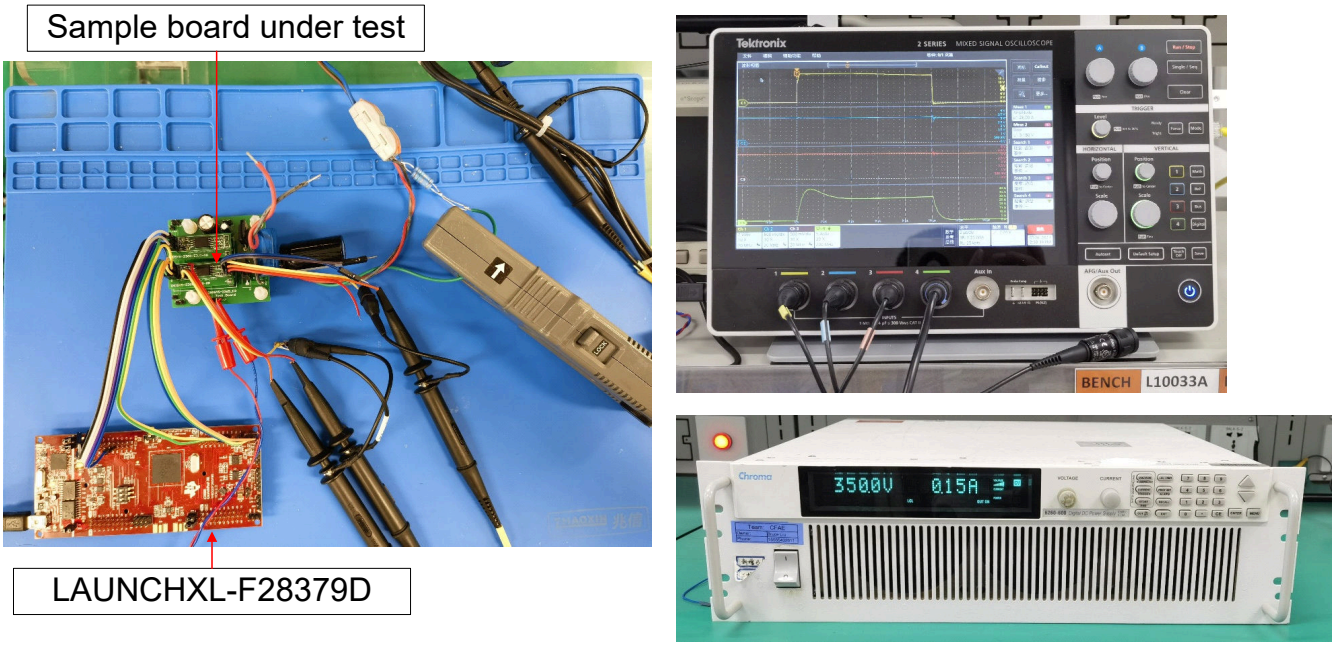

Figure 4-3. Platform for the Low-Side Driving Test

To test on an OCP or SCP situation, a 600-V 10-A discrete IGBT is used and two 1.5-Ω 3-W resistors are put in parallel to emulate a brake resistor. The resistors are inserted between the IGBT collector and the 350-V DC+ rail. The test result is show in Figure 4-4.

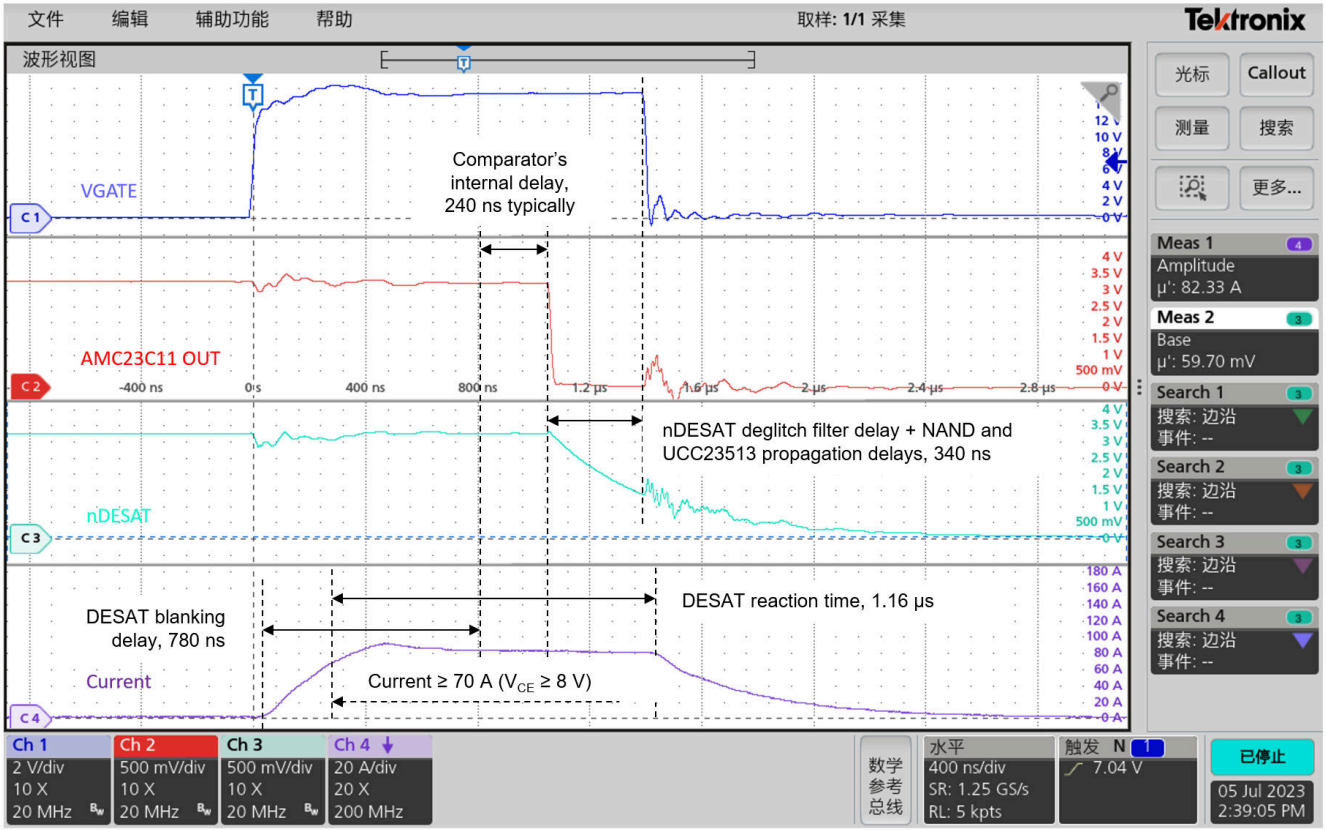

Figure 4-4. Short-Circuit Protection Delays in Low-side Driving Test

In this test, once the IGBT was turned on (t = 0 s), the collector current began to rise up and soon got saturated at around 90 A (t = 480 ns). According to the tested IGBT's data sheet, when the collector current reaches 70 A, the V_{CE} will increase to the 8 V trigger level set for the circuit. DESAT was detected by the isolated comparator AMC23C11 after a blanking time of around 780 ns. Then, after an internal delay of 240 ns typically, the AMC23C11's OUT shifted to low (t = 1.04 µs) and latched (when LATCH is set to high). After another delay by the deglitch filter for nDESAT of about 340 ns, the NAND gate SN74LVC1G00's output shifted to high and cut off the USS23513's input current, made the gate driver pulling the VGATE down (t = 1.44 µs). The DESAT reaction time, from IGBT's the current reached 70 A to the point the current began to drop after the GATE turned to low, was only about 1.16 µs.

4.2.2 Test Results on a 3-Phase Inverter With Phase to Phase Short

Tests on a 3-phase inverter platform of a TI reference design, the TIDA-010025, have been performed to check a phase to phase short circuit condition when driving an ACIM motor. In these tests, the U phase high side IGBT's gate driver was replaced by a sample board of the proposed circuit:

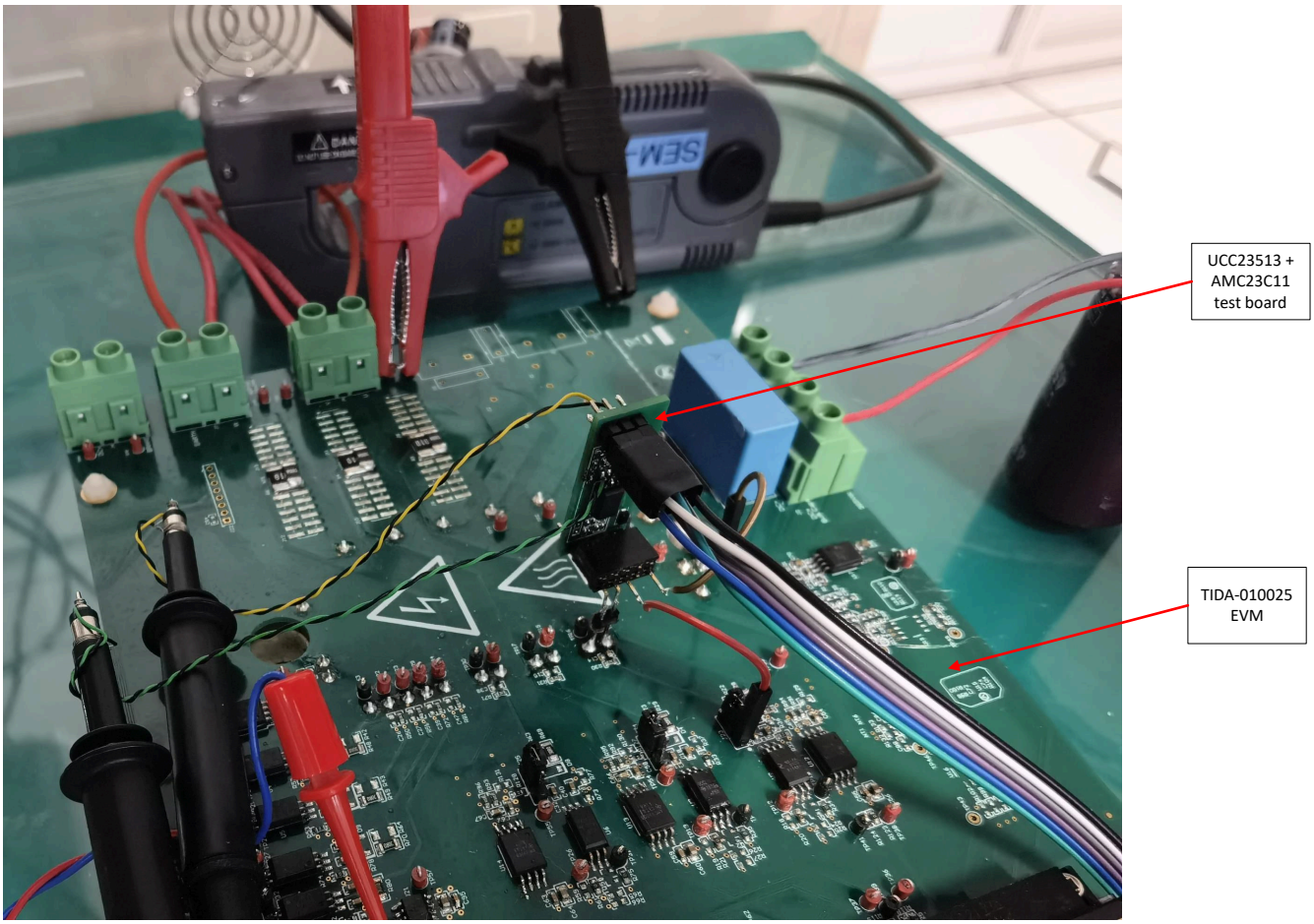

Figure 4-5. Platform for Run Motor Test

The TIDA-010025 reference design has a 1200-V, 25-A PIM power module on the power board, which has integrated six pieces of IGBT with the same ratings in the 3-phase inverter stage. To prepare for the tests, we first removed the original gate driving resistor for the U phase high-side IGBT, then connected the VGATE output, the 15-V power supply, and the VCE sense terminal of the sample board to the power board. To avoid the influence of the reference design's own hardware OCP function, we added a 5 mΩ shunt resistor in parallel to the original 10 mΩ one in all three phases, so that we can triple the OCP trigger level to 72 A. After checked on the output characteristics of the IGBTs, we also made some changes on our sample board for the DESAT threshold to be reached when the $V_{CE(SAT)}$ goes up to 2.5 V, which is corresponding to about 45 A collector current. During these tests, we first run the motor (with no load) to 50 rps, then short the inverter's U and W phases with a circuit breaker connected to the terminals of the power board. Figure 4-6 is a test result waveform.

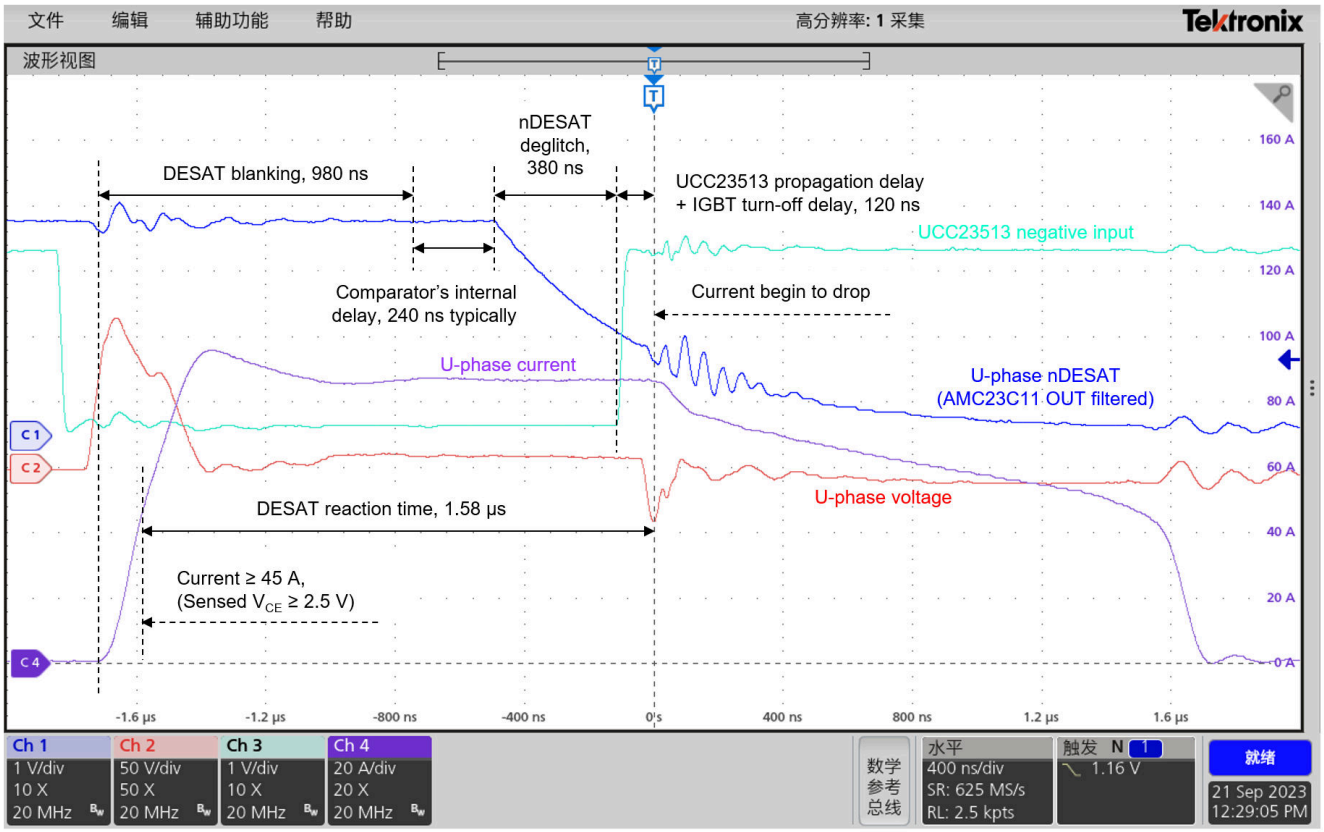

Figure 4-6. Short-Circuit Protection Delays in Run Motor Test

Once the circuit breaker was turned on, the U and W phases got shorted, and the U-phase current began to rise up rapidly. The saturate current soon reached a peak of about 95 A, then dropped a little and got stable at around 86 A. After a blinking time of 980 ns, the AMC23C11 detected the DESAT condition. After another internal propogation delay of 240 ns typically, the output OUT shifted to low. It took about 380 ns for the nDESAT to drop to the NAND gate input's negative going threshold and cut off the UCC23513's input current. The gate driver then took about 120 ns to make the IGBT's current began to drop off. The DESAT reaction time was about 1.58 µs in total.

There are some differences to the results in the low-side driving test. The differences in the two tested IGBTs' characteristics and the application circuits along with the DESAT threshold adjustment have contributed to these variations.

5 Summary

The combination of a compact, isolated simple gate driver with an isolated comparator for DESAT protection has been validated in this application note. The discrete approach reduces the design size compared to a 16-pin smart gate driver with integrated DESAT. This approach also adds flexibility to configure the key parameters for the DESAT function such as threshold, bias current, blanking time, and deglitch filter. The discrete approach also offers a DESAT latch function which can be reset by the MCU too.

This concept can also be expanded to bipolar gate driver supplies, and is equally fitting for both low-side and high-side gate drivers. For more details on these applications, refer to TIDA-00448.

6 References

1. Texas Instruments, AMC23C11: Fast-Response, Reinforced, Isolated Comparator With Adjustable Threshold and Latch Function, data sheet.
2. Texas Instruments, UCC23513: 4-A Source, 5-A Sink, 5.7-kVRMS Opto-Compatible Single-Channel Isolated Gate Driver data sheet.
3. Texas Instruments, UCC23511: 1.5-A Source, 2-A Sink, 5.7-kVRMS Opto-Compatible Single-Channel Isolated Gate Driver data sheet.
4. Texas Instruments, UCC21750: 10-A Source/Sink Reinforced Isolated Single Channel Gate Driver for SiC/IGBT with Active Protection, Isolated Analog Sensing and High-CMTI data sheet.
5. Texas Instruments, AMC23C14: Dual, Fast Response, Reinforced Isolated Window Comparator With Adjustable Threshold data sheet.
6. Texas Instruments, ISO5451: 5.7kVrms, 2.5A/5A single-channel isolated gate driver with active protection features, data sheet.
7. Texas Instruments, PSpice for TI design and Simulation tool.
8. Texas Instruments, UCC21750: How can we adjust the DESAT detection threshold in UCC217xx & ISO5x5x? FAQ.
9. Texas Instruments, TIDA-00448: Flexible High Current IGBT Gate Driver with Reinforced Digital Isolator reference design.
10. Texas Instruments, TIDA-00638: Reference Design for Isolated Gate Driver Power Stage with Active Miller Clamp for Solar Inverters reference design.
11. Texas Instruments, TIDA-010025: Three-phase inverter reference design for 200-480 VAC drives with opto-emulated input gate drivers reference design,

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2023	*	Initial Release

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265