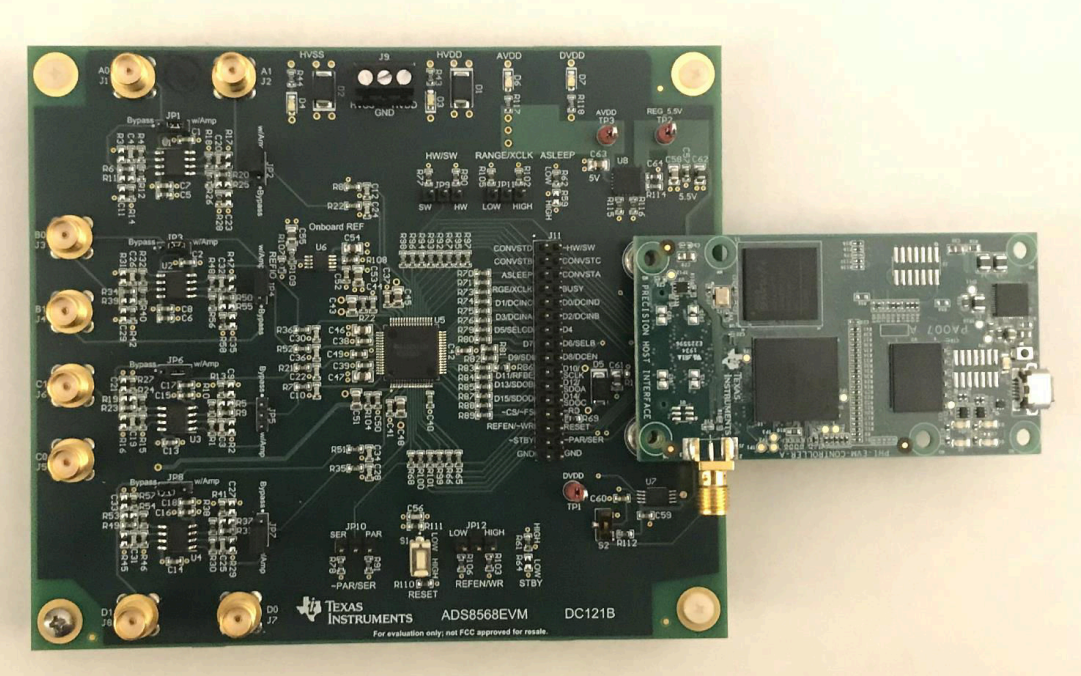
User's Guide

ADS8568EVM-PDK Evaluation Module

ABSTRACT



This user's guide describes the operation and use of the ADS8568 evaluation module (EVM). The ADS8568 is an 8-channel, simultaneous sampling, 16-bit successive approximation (SAR) analog-to-digital converter (ADC). Each input channel on the device can support true bipolar input ranges up to ±12 V. The device includes a programmable internal buffered voltage reverence. The ADC includes a serial SPI interface and a parallel interface for data communication. Configuration of the device is achieved through simple static digital input pins (hardware mode) or through communications to the SPI interface. This user's guide covers circuit description, schematic diagram, and bill of materials for the ADS8568 circuit board.

Table of Contents

List of Figures

List of Tables

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1 EVM Overview

This document describes how to connect the EVM to your computer and test equipment to evaluate device performance and understand device features. The document also describes how to install and use the associated evaluation module software.

1.1 ADS8568EVM-PDK Kit Features

The ADS8568 evaluation module kit includes the following features:

- Hardware and software required for diagnostic testing as well as accurate performance evaluation of the ADS8568 ADC
- Digital and analog interface power with USB power. External power required for high voltage ±15 V supply.
- Easy-to-use evaluation software for 64-bit Microsoft Windows™7, Windows 8, and Windows 10 operating systems.
- PHI controller translates USB (2.0) or higher to parallel, or serial digital communications.

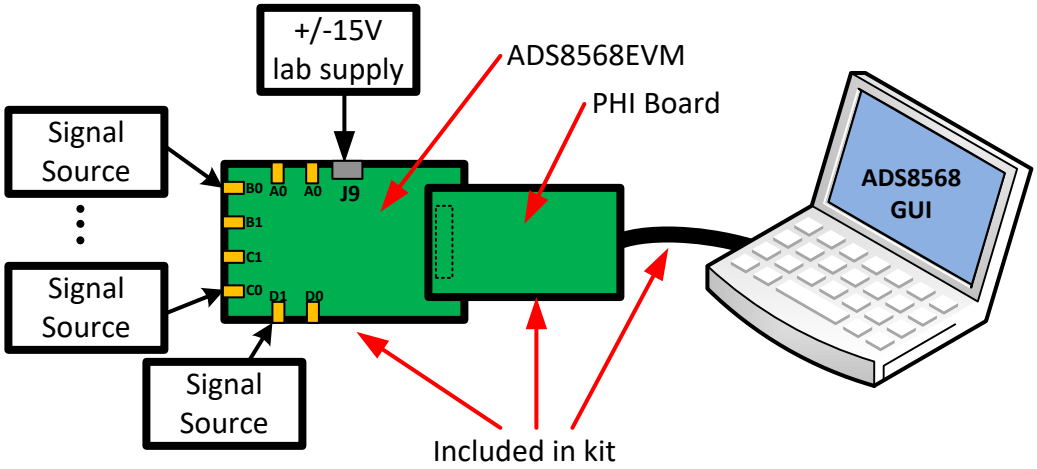

Figure 1-1. System Connection for Evaluation

1.2 ADS8568EVM Board Features

- Eight input channels connected to external single ended signals source applied to SMA connectors or header
- Serial and parallel interface connects to the PHI controller via 60 pin connector (J10)
- High voltage power supplies (HVDD, and HVSS) are not included. Connect common lab supplies via terminal strip J9.
- Low voltage supplies (AVDD, and DVDD) generated using USB power from the PHI controller.
- Integrated or external voltage reference options available.

1.3 Related Documentation From Texas Instruments

Related Documents lists devices that are used in this EVM and may be useful in related designs.

Table 1-1. Related Documents

Device	Literature Number
ADS8568	SBAS543
OPA2211	SBOS377
TPS7A4700	SLVS493
REF6025	SBOS708

2 EVM Analog Interface

2.1 ADC Supply, Input, Voltage Reference, and Digital Connections

Figure 2-1 illustrates the decoupling on AVDD, DVDD, HVDD, HVSS, and the reference IO. The capacitors for decoupling match the recommendations in the ADS8568 data sheet. The layout (see Figure 2-1) uses the shortest possible connections to the decoupling capacitors and connections the ground end to the GND plane using vias. The ADS8568 can use an external or internal voltage reference. This can be selected by changing the position of JP9 to “INT” for internal, or “EXT” for external. Figure 2-1 also illustrates the analog input signal and digital signal connections.

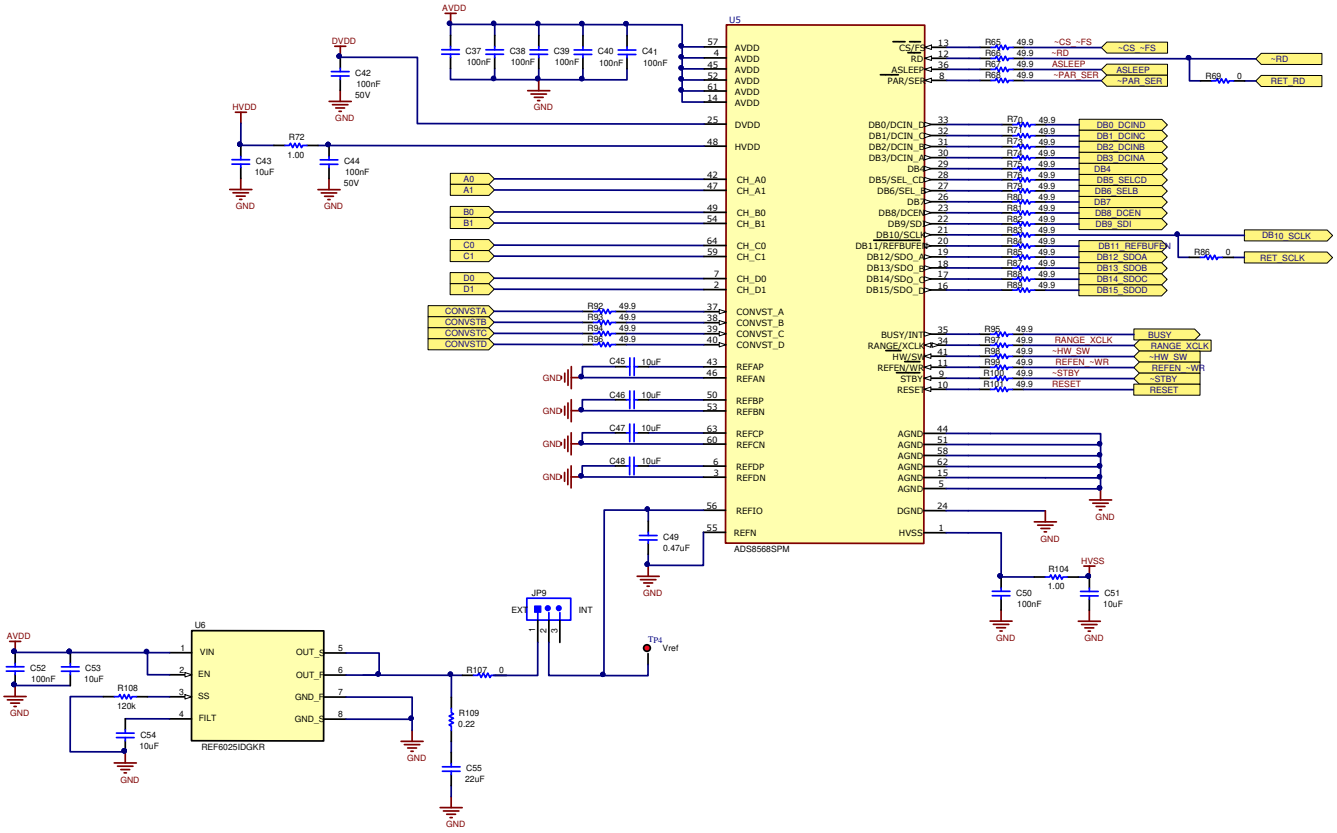

Figure 2-1. ADC Signal and Supply Connection

2.2 ADC Amplifier Drive

Figure 2-2 shows the op amp configuration for each ADC drive input. The default configuration is and inverting configuration. This can be converted to a non-inverting configuration but uninstalling R6, and R14, and installing R11. Also, R11 and C11 can be used to create a low pass filter. The jumper JP1 can be used to completely bypass the amplifier. This diagram only shows one channel but this circuit is repeated 8 times. For other channels, see Appendix A.

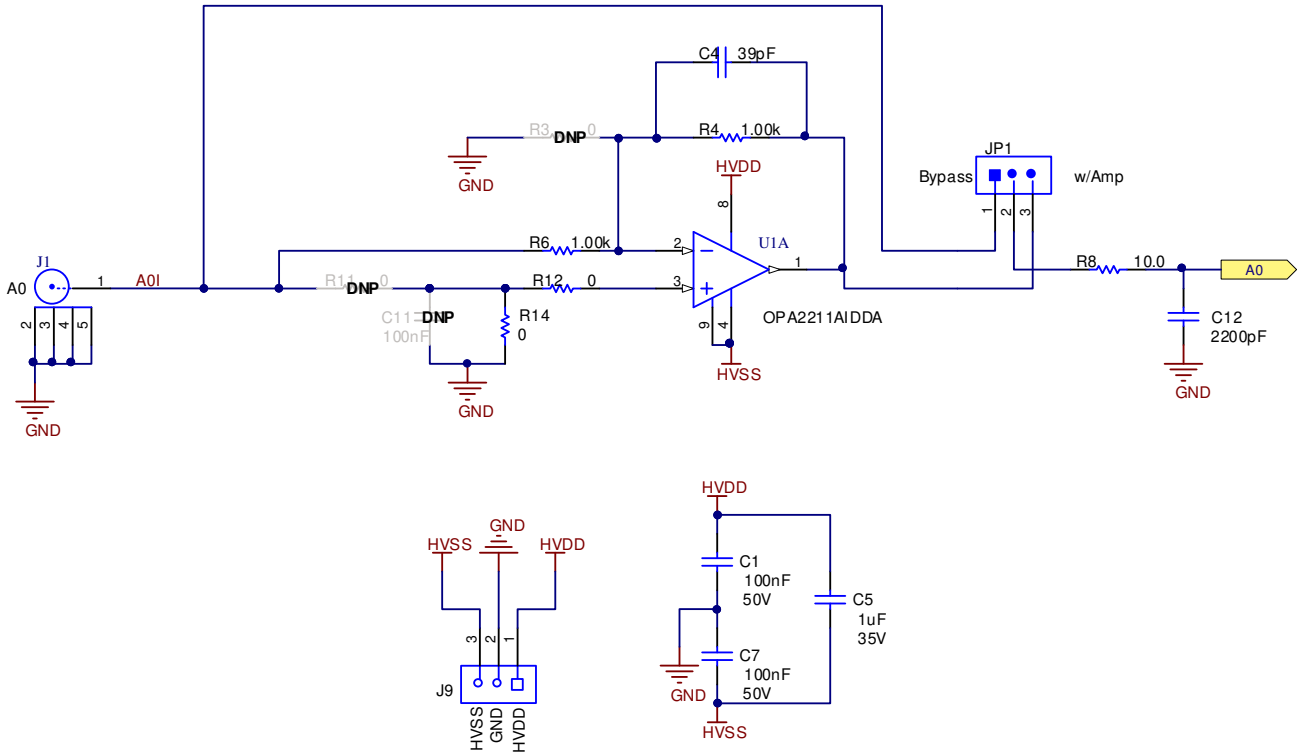

Figure 2-2. Amplifier Drive Circuit

3 Digital Interface

As noted in Section 1, the EVM interfaces with the PHI and communicates with the computer over the USB. There are two devices on the EVM with which the PHI communicates: the ADS8568 ADC (over SPI) and the EEPROM (over I2C). The EEPROM comes pre-programmed with the information required to configure and initialize the ADS8568 platform. When the hardware is initialized, the EEPROM is no longer used.

3.1 Parallel Interface

The parallel interface signals are generated on the PHI controler and connected through J10. Each of these signals has a 47-Ω resistor between the device and the controler to slow down the signal edges in order to minimize signal overshoot. The digital signals can be monatored on J11 test header.

3.2 Serial Interface (SPI)

The ADS8568 ADC uses SPI serial communication in mode 2 (CPOL=1 and CPHA=0). Because the serial clock (SCLK) frequency can be as fast as 45 MHz, the ADS8568EVM offers 47-Ω resistors between the controler and device to aid with signal integrity. Typically, in high-speed SPI communication, fast signal edges can cause overshoot; these 47-Ω resistors slow down the signal edges in order to minimize signal overshoot.

3.3 Connections to PHI connector

Connector J10 is used to connect the PHI digital controller PCB to the ADS8568EVM. This connector has all the digital signals as well as the 5.5V regulated supply and the DVDD supply. The power for the two supplies is from the USB connection. The 5.5V supply is used to generate the AVDD supply. This connector also provides I2C signals that are used on the EEPROM identification circuit.

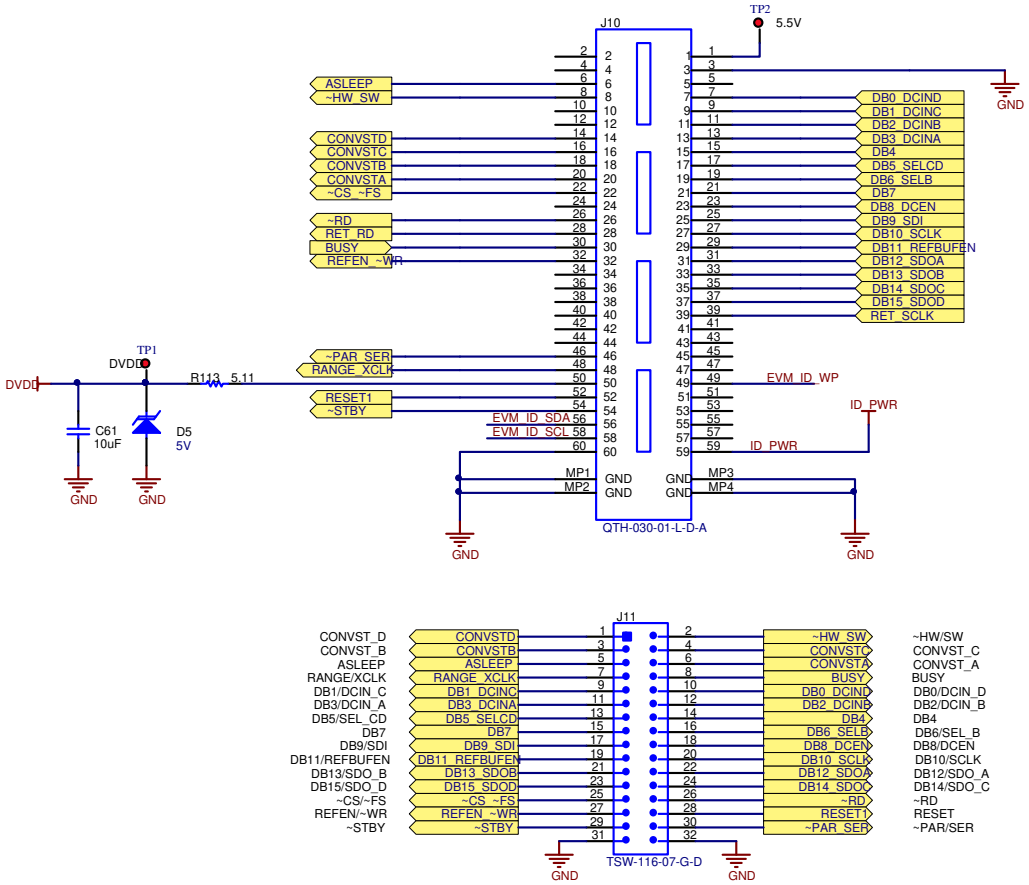

Figure 3-1. PHI to ADS8568EVM connector

3.4 Static Signals for ADS8568

The ADS8568 has several static digital configuration pins. The logic state of the pin will determine the operation of the device. For example, the PAR/SER digital pin will determine if the communication is in parallel or serial mode. These pins are automatically controlled by the PHI digital controller when the GUI is in "hardware mode". The logic level on these pins can be monitored using test points on J11 or as shown in Figure 3-2. Some of these digital control pins also have resistors that can be used to configure the logic levels when the PHI controller is not used. Figure 3-2 shows the static logic configuration. To set a pin to logic high the resistor connected to DVDD is installed. To set an input to logic low the resistor connected to GND needs to be installed. It is important to understand that the configuration of these resistors does not matter when the PHI is used as it will drive the logic level to whatever the GUI setting is. These digital input configuration resistors only matter when the EVM is disconnect from the PHI and used with a different digital controller.

Figure 3-2 also shows the operation of the reset control line. This reset can be initiated by the PHI controller or by the push button switch. Note that RESET is an active high signal so the two reset signals are applied to an OR function so that the device will be reset if either the push button is pressed or the PHI drives the signal active high.

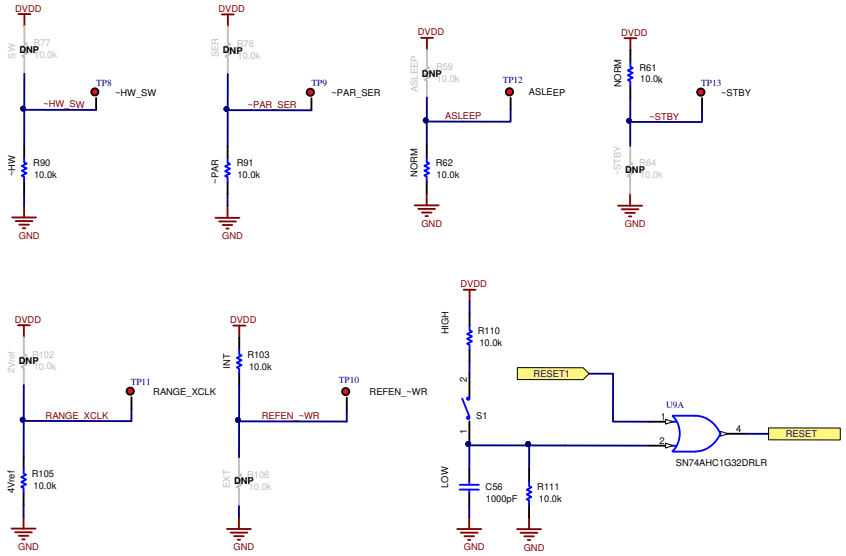

Figure 3-2. Static Digital Input Configuration

3.5 I2C Bus for Onboard EEPROM

The circuit shown in Figure 3-3 is used with our EVM controler (PHI), for EVM identification. This circuit is not required by the ADS8568 for operation. The switch (S2) is a write protect and does not need to be changed for EVM operation.

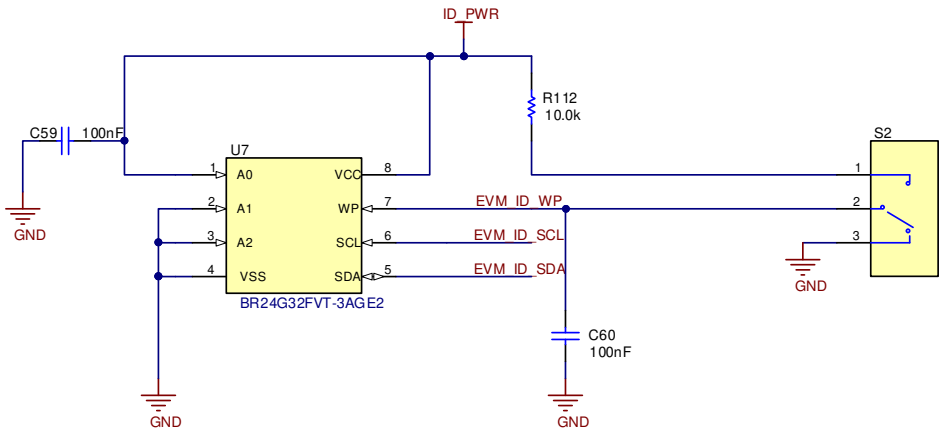

Figure 3-3. EEPROM for EVM ID

4 Power Supplies

The ADS8568EVM has four power supplies: AVDD (5 V), DVDD (3.3 V), HVDD (15 V), and HVSS (-15 V). The two high voltage power supplies require an external ±15 V supply and are connected on a screw terminal strip (J9). The lower voltage supplies (AVDD and DVDD), are generated with the USB power and low dropout regulators (LDO).

4.1 Low Dropout Regulator

U8 is a low dropout regulator (LDO) used to convert the 5.5 V regulated supply from the PHI to a low noise 5 V supply. The input and output of this LDO can be monitored on TP2 and TP3.

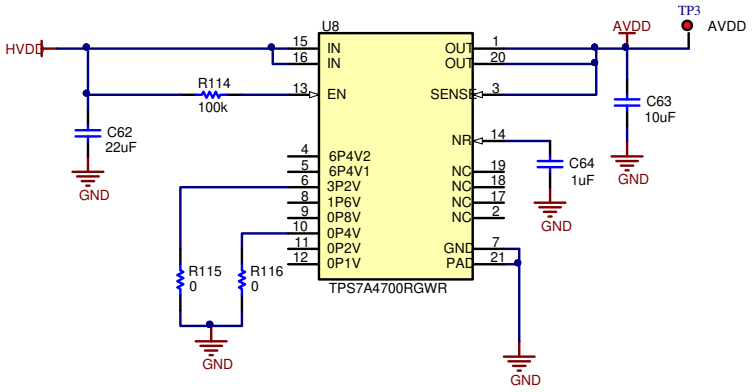

Figure 4-1. Low Dropout Regulator for AVDD (5v Supply)

4.2 Power Connections and LED Indicators

The screw terminal block J9 is used to connect the external high voltage supplies. These supplies are not provided in the evaluation module kit and it is expected that you will use low noise lab supply to provide this power (for example, Keysight E3632a). The high voltage supplies have transient voltage suppressor diodes to help protect the ADC from transients. These supplies are typically connected to +/-15 V. For details on operation, see the ADS8568 data sheet. Figure 4-2 also shows how each supply has an LED monitor for quick verification that power is applied.

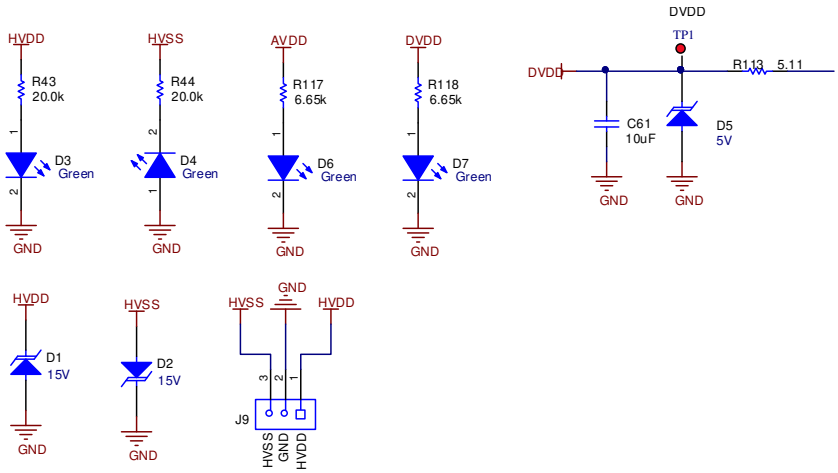

Figure 4-2. Supply Connections and Led Monitors

5 Installing ADS8568EVM Software

Download the latest version of the EVM GUI installer from the Tools and Software folder of the ADS8568EVM and run the GUI installer to install the EVM GUI software on your computer.

CAUTION

Manually disable any anti-virus software running on the computer before downloading the EVM GUI installer onto the local hard disk. Depending on the anti-virus settings, an error message may appear or the installer. The exe file can be deleted.

Accept the license agreements and follow the on-screen instructions shown in Figure 5-1 to complete the installation.

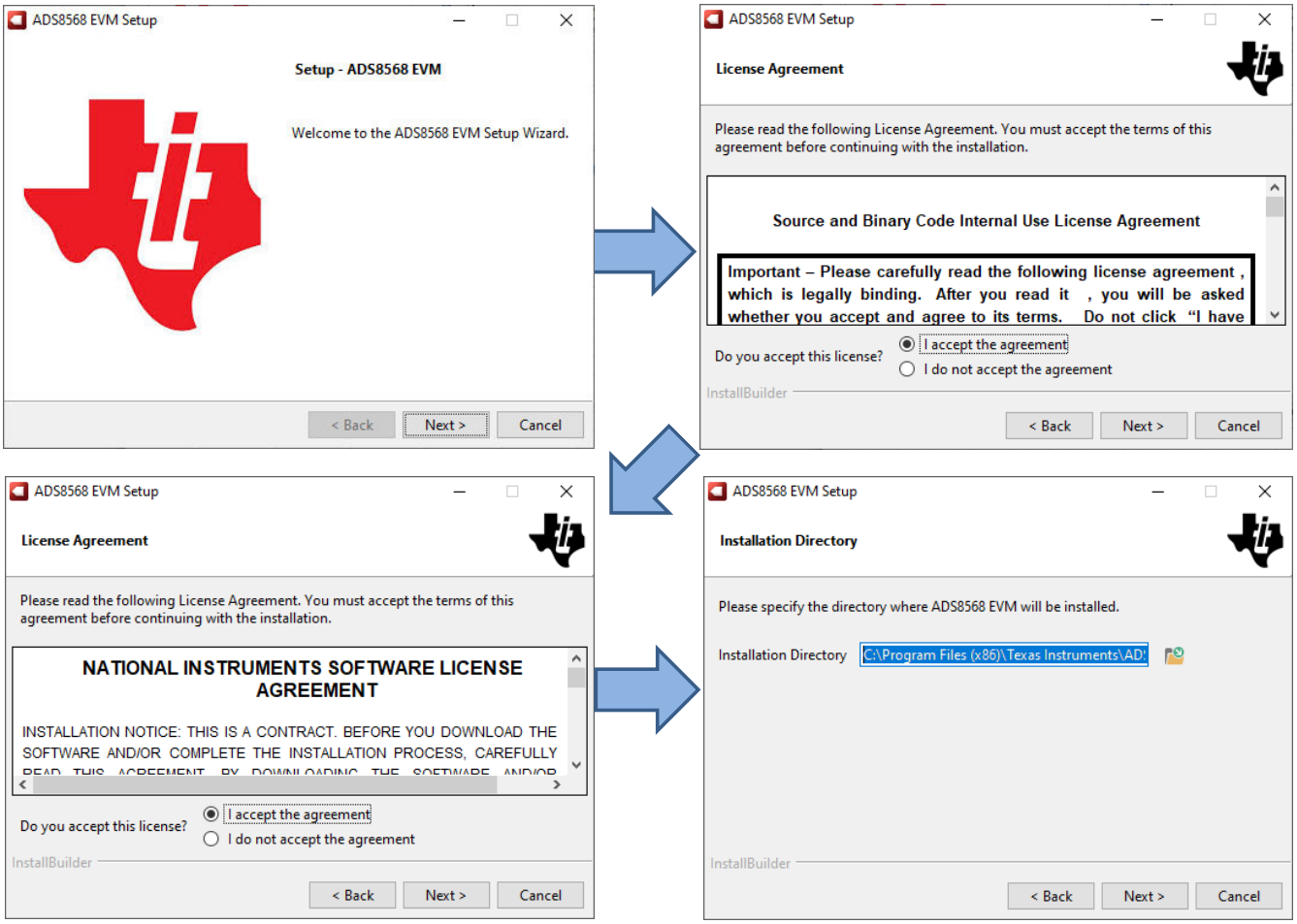

Figure 5-1. ADS8568 Software Installation Prompts

As a part of the ADS8568EVM GUI installation, a prompt with a Device Driver Installation (as shown in Figure 5-2) appears on the screen. Click Next to proceed.

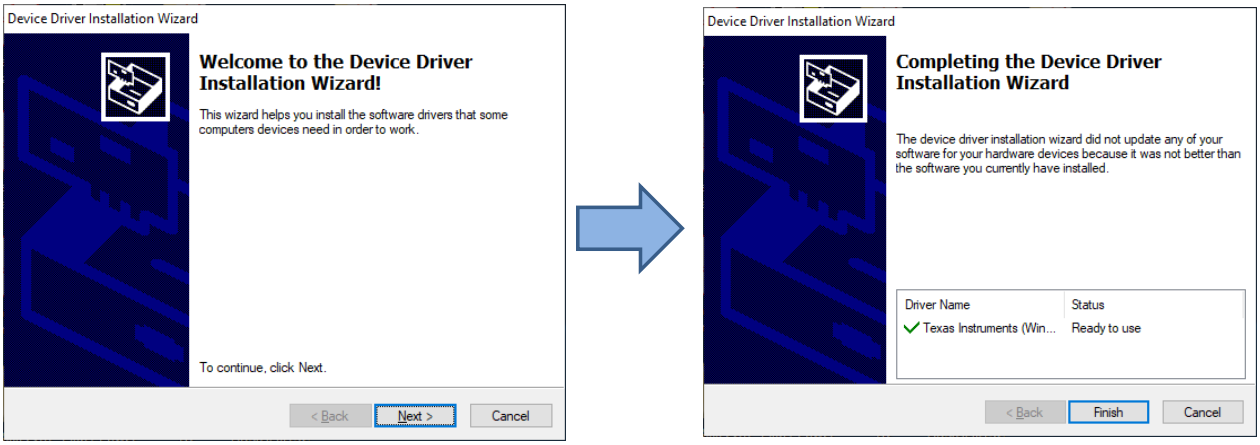

Figure 5-2. Device Driver Installation Wizard Prompts

The ADS8568EVM requires the LabVIEW™ run-time engine and may prompt for the installation of this software, as shown in Figure 5-3, if not already installed.

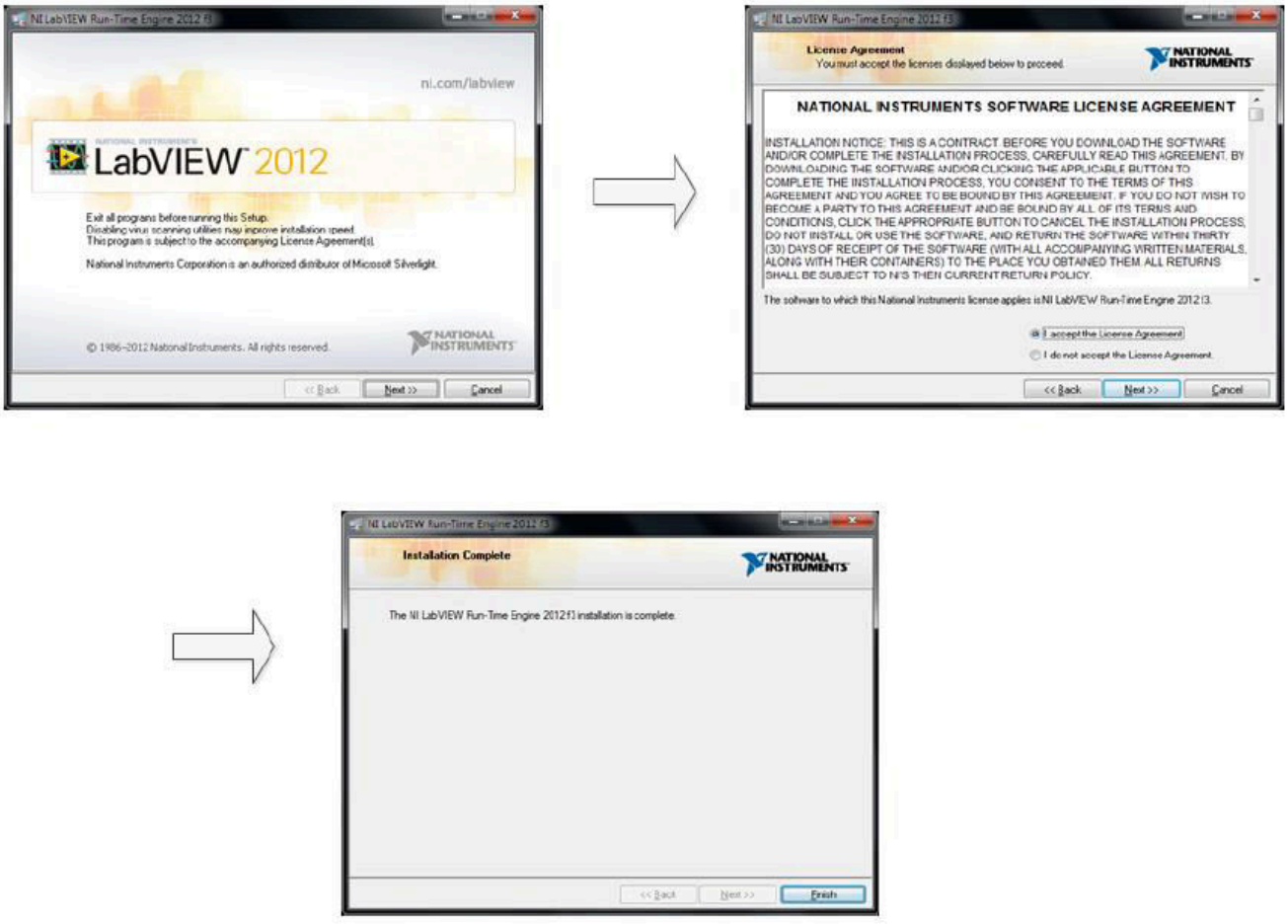

Figure 5-3. LabVIEW Run-Time Engine Installation

Verify that C:\Program Files (x86)\Texas Instruments\ADS8568EVM is as shown in Figure 5-4 after these installations.

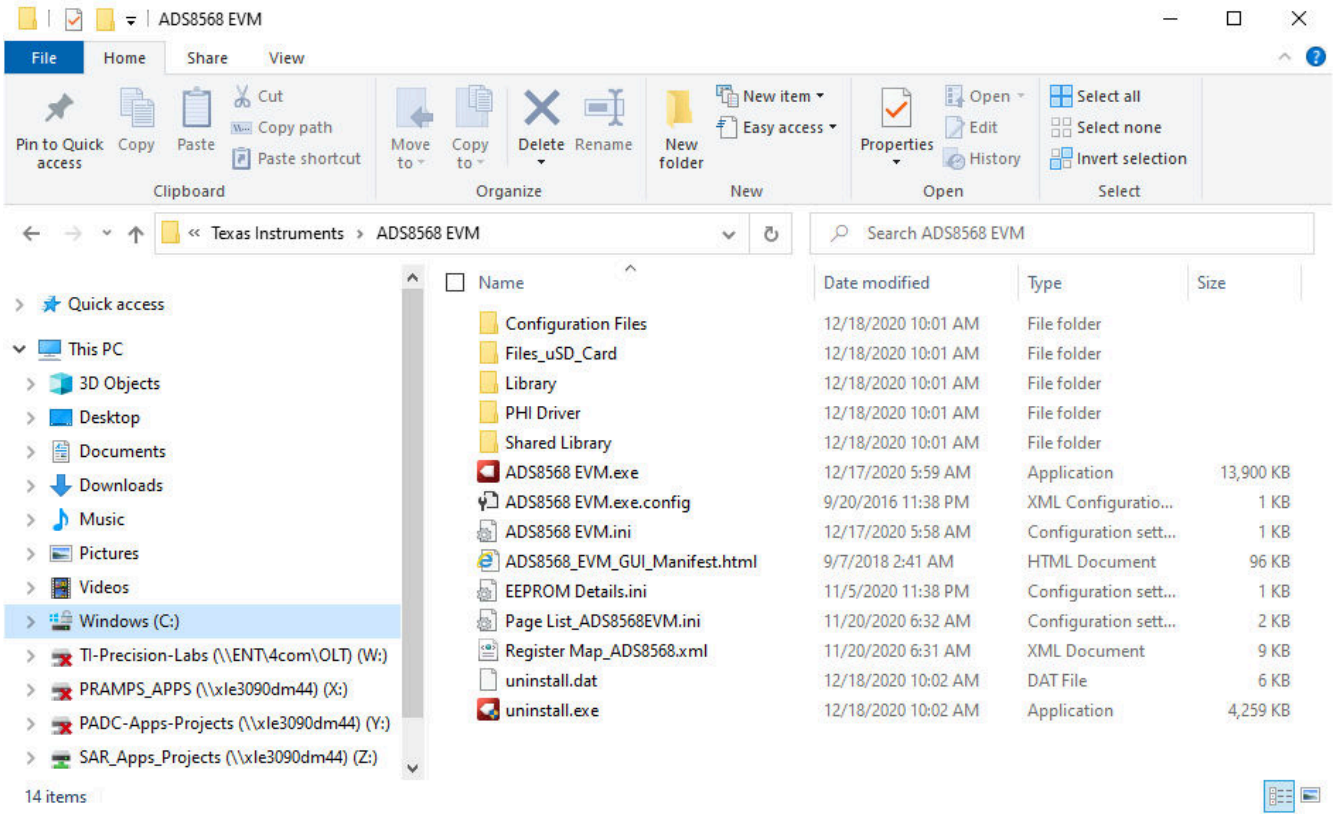

Figure 5-4. ADS8568EVM GUI Folder Post-Installation

6 ADS8568EVM Operation

The following instructions are a step-by-step guide to connecting the ADS8568EVM to the computer and evaluating the performance of the ADS8568:

6.1 Connecting the Hardware and Running the GUI

1. Set the jumpers according to Table 6-1.
2. Physically connect P2 of the PHI to J10 of the ADS8568EVM. Install the screws to assure a robust connection.
3. Connect USB on PHI to the computer first.
   a. LED D5 on the PHI lights up, indicating that the PHI is powered up.
   b. LEDs D1 and D2 on the PHI start blinking to indicate that the PHI is booted up and communicating with the PC; Figure 6-1 shows the resulting LED indicators.
4. Start the software GUI as shown in Figure 6-2. You will notice that the LEDs blink slowly as the FPGA firmware is loaded on the PHI. This will take a few seconds then the AVDD and DVDD power supplies will turn on.
5. Connect the high voltage power supplies (HVDD = +15 V, HVSS = -15 V, and GND).
6. Connect the signal generator. The default input range is ±10 V (or 10Vpk). A common input signal applied is a sinusoidal 1kHz, 9.9Vpk signal with a 0 V offset. Note that this signal is adjusted just below the full scale range to avoid clipping.

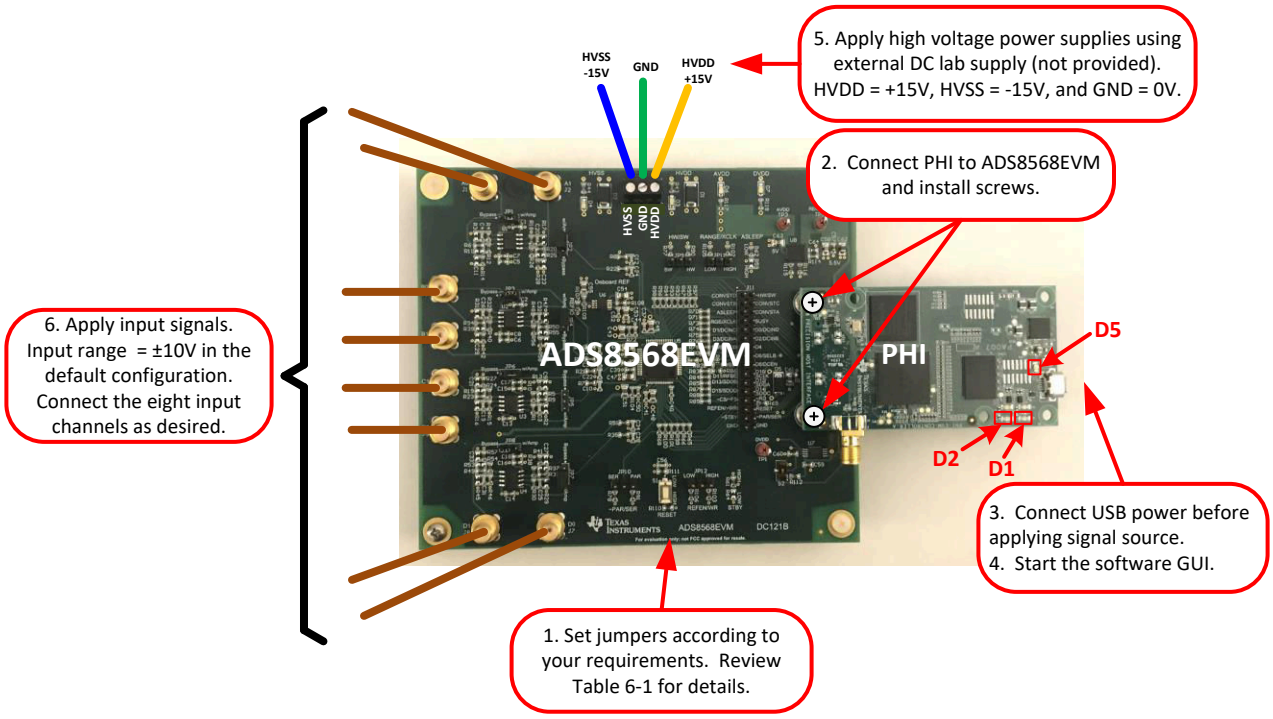

Figure 6-1. ADS8568EVM Hardware Setup and LED Indicators

Figure 6-2 shows how the software can be started on the start menu or using a desktop icon.

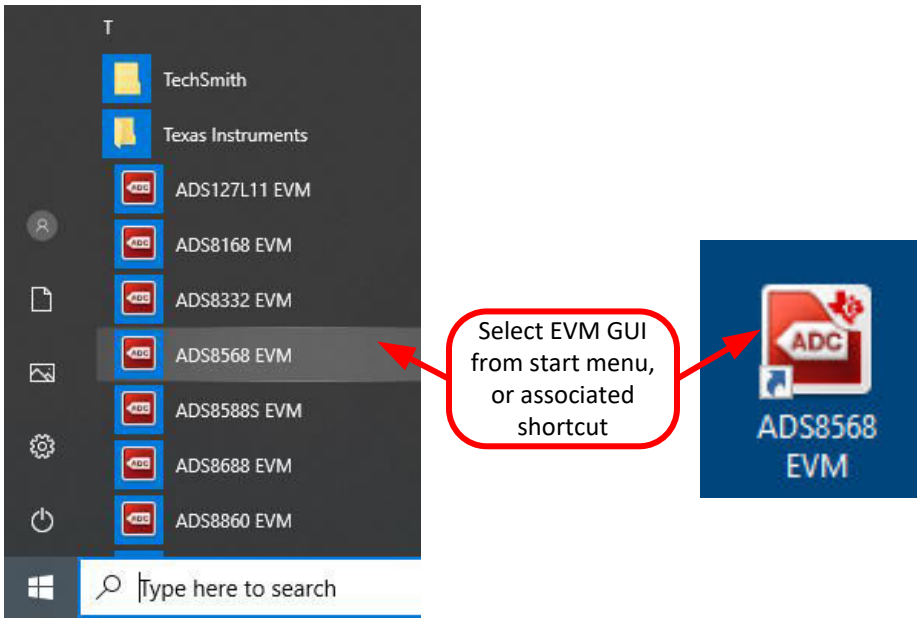

Figure 6-2. Launch the EVM GUI Software

6.2 Jumper Settings for ADS8568EVM

The amplifiers and reference can be configured with jumpers. The amplifier jumpers (JP1-JP8) determine if the amplifier is used or if an external signal is directly connected to the ADC input. JP9 is used to select either the internal reference option or external reference option. Take care to make sure that the GUI configuration for the device reference matches the setting of JP9. The GUI software starts up in the "internal" reference mode, so make sure the JP9 is in the "INT" position.

Table 6-1. Jumper Settings

Jumper	Setting	Default	Function
JP1 to JP8	wAmp / Bypass	wAmp	These eight jumpers determine if the amplifier is used to buffer the inputs signals or if it is bypassed. Choosing wAmp will connect the amplifier between each SMA connector (J1 to J8) and the ADC input. The default amplifier configuration is inverting (Gain = -1V/V). The amplifier gain configuration can be adjusted by soldering and de-soldering different resistors. Choosing the Bypass configuration will connect the SMA connectors directly to the ADC input.
JP9	EXT / INT	INT	This jumper will select internal vs external mode on the voltage reference. Using internal mode will disconnect the external reference. Using external mode will connect the external REF6025 2.5 V reference to the ADC reference input. Take care to make sure that the GUI settings for the voltage reference match this jumpers setting.

6.3 EVM GUI Global Settings for ADC Control

Figure 6-3 shows that the EVM Global controls are located on the right hand side of the GUI. These controls choose the page display, SPI Mode, SCLK frequency, and sampling frequency.

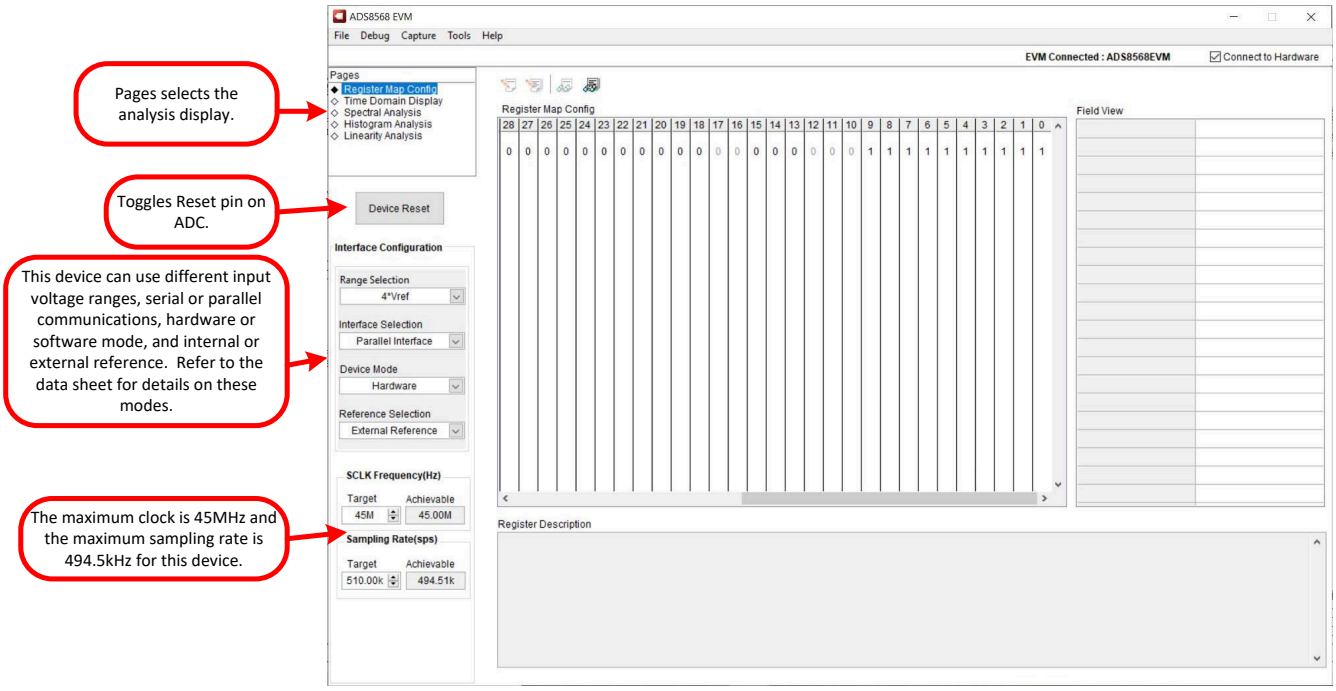

Figure 6-3. Global Settings for ADC Control

6.4 Time Domain Display

The time domain display tool allows visualization of the ADC response to a given input signal. This tool is useful for both studying the behavior and debugging any gross problems with the ADC or drive circuits.

The user can trigger a capture of the data of the selected number of samples from the ADS8568EVM, as per the current interface mode settings indicated in Figure 6-4 by using the Capture button. The sample indices are on the x-axis and there are two y-axes showing the corresponding output codes as well as the equivalent analog voltages based on the specified reference voltage. Switching pages to any of the Analysis tools described in the subsequent sections causes calculations to be performed on the same set of data.

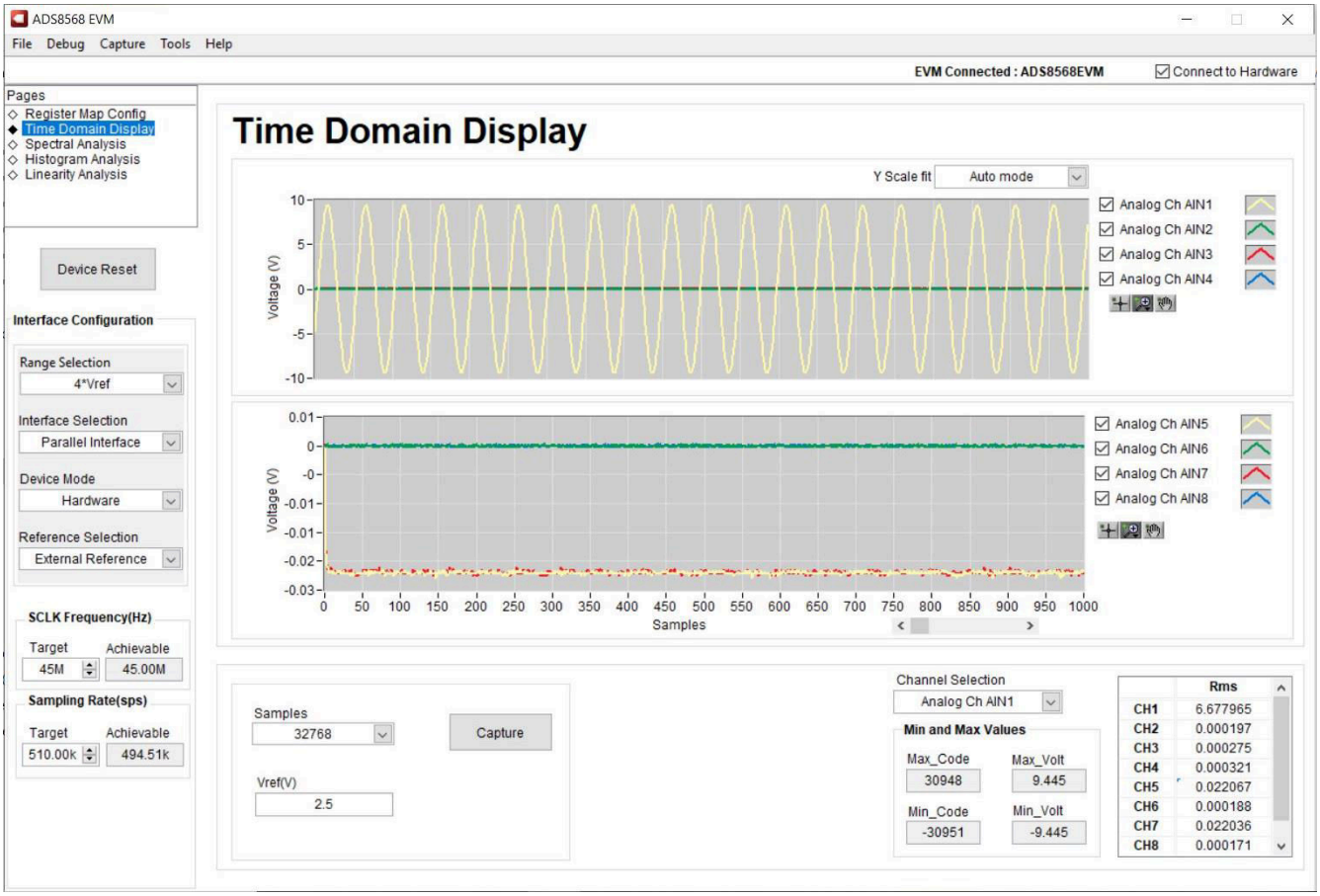

Figure 6-4. Time Domain Display

6.5 Frequency Domain Display

The spectral analysis tool, shown in Figure 6-5, is intended to evaluate the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of the ADS8568 ADC through single-tone sinusoidal signal FFT analysis using the 7-term Blackman-Harris window setting. The FFT tool includes windowing options that are required to mitigate the effects of non-coherent sampling (this discussion is beyond the scope of this document). The 7-Term Blackman Harris window is the default option and has sufficient dynamic range to resolve the frequency components of up to a 24-bit ADC. The None option corresponds to not using a window (or using a rectangular window) and is not recommended.

Figure 6-5. Frequency Domain Display

6.6 Histogram Display

Noise degrades ADC resolution and the histogram tool can be used to estimate effective resolution, which is an indicator of the number of bits of ADC resolution losses resulting from noise generated by the various sources connected to the ADC when measuring a DC signal. The cumulative effect of noise coupling to the ADC output from sources such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC itself is reflected in the standard deviation of the ADC output code histogram that is obtained by performing multiple conversions of a DC input applied to a given channel. As shown in Figure 6-6, the histogram corresponding to a DC input is displayed on clicking the Capture button.

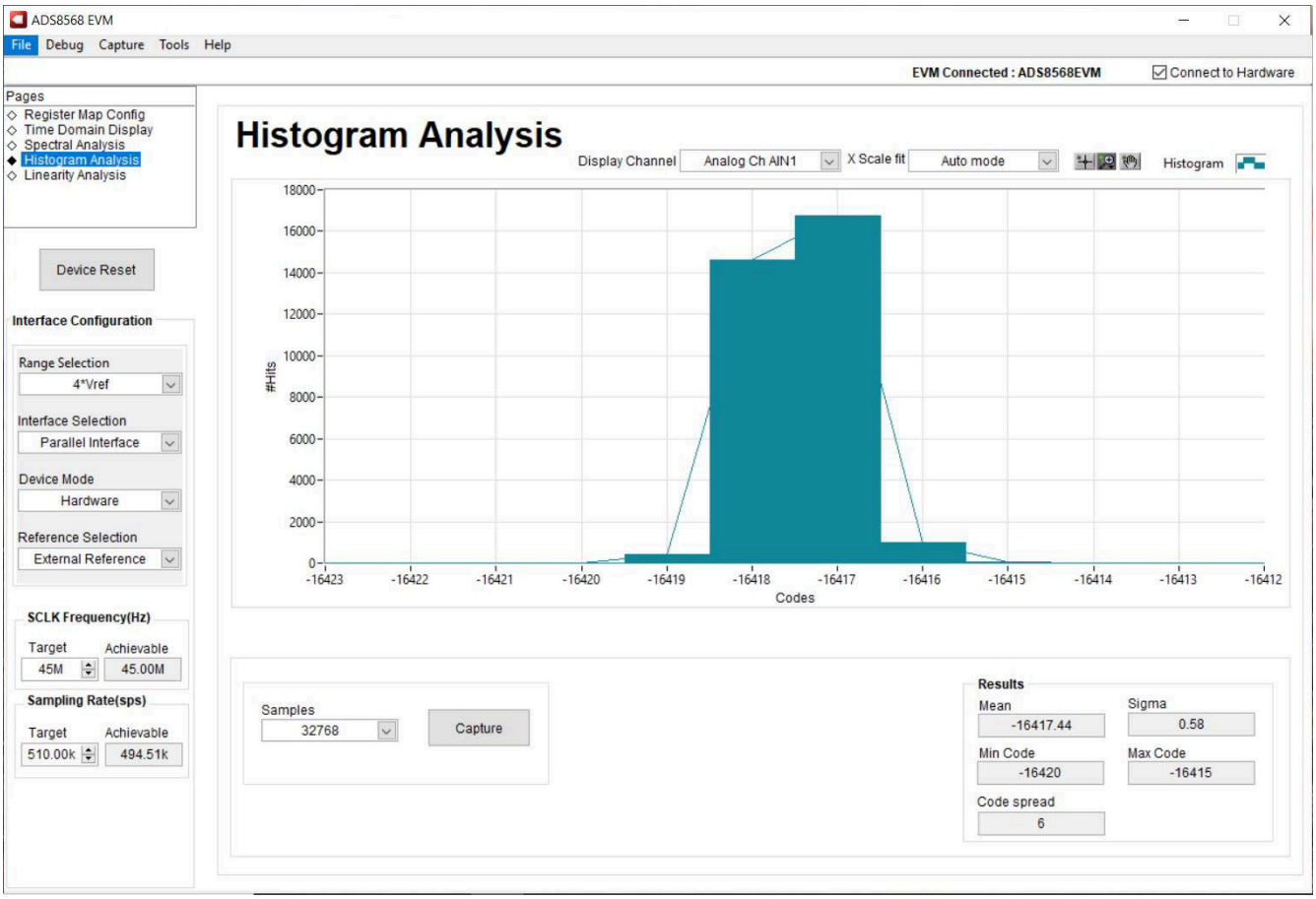

Figure 6-6. Histogram Display

7 Modifying Hardware and Using Software to Evaluate ADS8548 and ADS8528

The ADS8568 is part of a family of related devices. This EVM hardware and software will support the entire family as all the devices are pin-for-pin compatable. The ADS8548 is the 14 bit version of the device, and the ADS8528 is the 12 bit version of the device. The procedure below shows how to modify the hardware and software to evaluate the other devices in this family.

1. Desolder the ADS8568 device an replace it with the device you want to evaluate.
2. Enable the EEPROM for writing. This is done by changing switch S2 to the top position using tweezers. For details, see Figure 7-1.
3. Connect EVM and start GUI as described in Connecting the Hardware and Running the GUI.
4. Use the "Tools" menu to "Load EEPROM" according to the device that is currently installed. When this procedure is successfully completed, you will see the status bar at the top of the software update according to the device installed on the hardware. For details, see Figure 7-2.

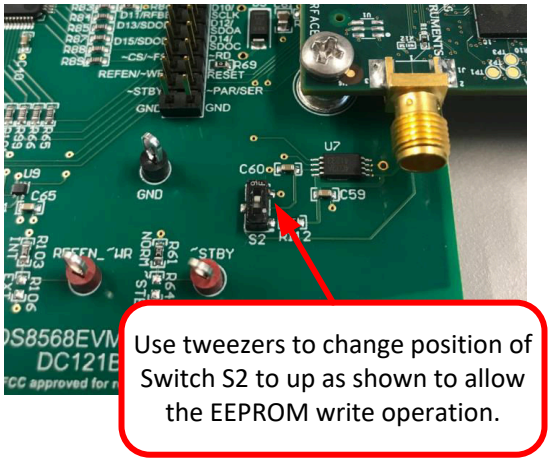

Figure 7-1. Enable EEPROM for Writing

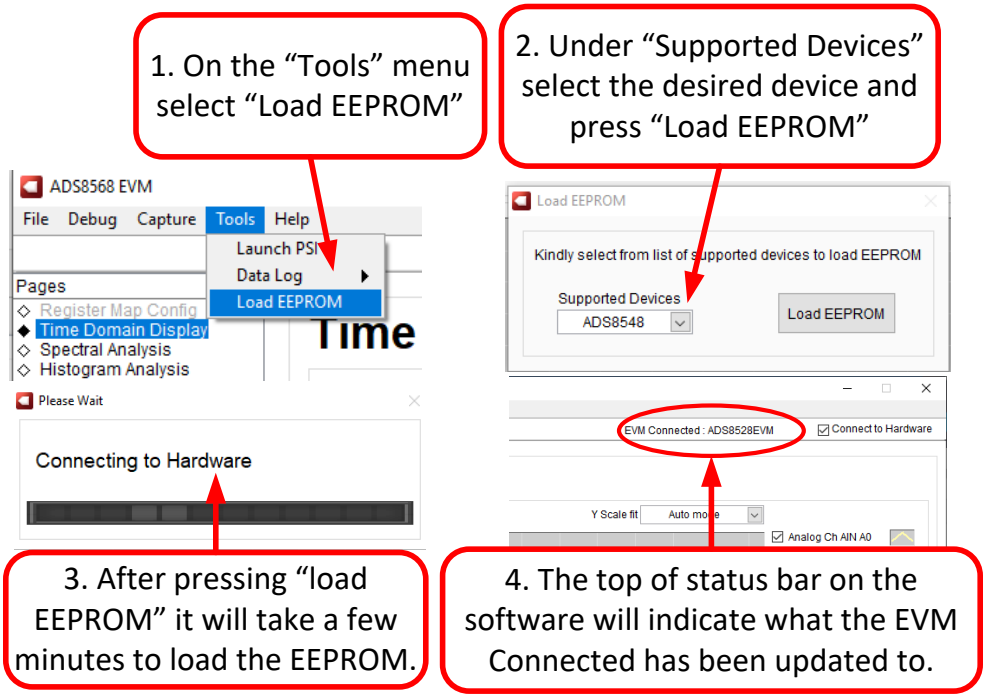

Figure 7-2. Configure EEPROM and Software for New Device

A Bill of Materials, Layout, and Schematic

Schematics for the ADS8568EVM are appended to this user's guide. The bill of materials is provided in Bill of Materials. Layout shows the PCB layouts for the ADS8568EVM.

A.1 Bill of Materials

Designator	Qty	Value	Description	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board	DC121	Any
C1, C2, C7, C8, C13, C14, C17, C18, C37, C38, C39, C40, C41, C42, C44, C50, C52, C59, C60, C65	20	0.1 µF	CAP, CERM, 0.1 µF, 50 V, ± 10%, X7R, 0603	C0603C104K5RACTU	Kemet
C3, C4, C19, C20, C25, C26, C31, C32	8	39 pF	CAP, CERM, 39 pF, 50 V, ± 5%, C0G/NP0, 0603	CGA3E2C0G1H390J080AA	TDK Corporation
C5, C6, C15, C16, C64	5	1 µF	CAP, CERM, 1 µF, 35 V, ± 10%, X5R, 0603	GMK107BJ105KA-T	Taiyo Yuden
C10, C12, C22, C24, C28, C30, C34, C36	8	2200 pF	CAP, CERM, 2200 pF, 50 V, ± 5%, C0G/NP0, 0603	GRM1885C1H222JA01D	MuRata
C43, C45, C46, C47, C48, C51, C53, C54, C61, C63	10	10uF	CAP, CERM, 10 µF, 35 V, ± 10%, X5R, 0805	C2012X5R1V106K125AC	TDK
C49	1	0.47 µF	CAP, CERM, 0.47 µF, 50 V, ± 10%, X5R, 0603	C1608X5R1H474K080AB	TDK
C55, C62	2	22 µF	CAP, CERM, 22 uF, 35 V, +/- 20%, X5R, 0805	C2012X5R1V226M125AC	TDK
C56	1	1000 pF	CAP, CERM, 1000 pF, 50 V, ± 10%, C0G/NP0, 0603	06035A102KAT2A	AVX
D1, D2	2	15 V	Diode, TVS, Uni, 15 V, 24.4 Vc, SMB	SMBJ15A-13-F	Diodes Inc.
D3, D4, D6, D7	4	Green	LED, Green, SMD	APT2012LZGCK	Kingbright
D5	1	5 V	Diode, TVS, Uni, 5 V, 9.2 Vc, 400 W, 43.5 A, SMA	SMAJ5.0A	Littelfuse
H1, H2, H3, H4	4		Hex Standoff Threaded #4-40 Aluminum 0.250" (6.35mm) 1/4"	1891	Keystone
H5, H6, H7, H8	4		MACHINE SCREW PAN PHILLIPS 4-40	PMSSS 440 0025 PH	B&F Fastener Supply
H9, H10	2		ROUND STANDOFF M3 STEEL 5MM	9774050360R	Wurth Elektronik
H11, H12	2		Machine Screw Pan PHILLIPS M3	RM3X4MM 2701	APM HEXSEAL
H13	1		Cable, USB-A to micro USB-B, 1 m - Kitting item	102-1092-BL-00100	CnC Tech
H14	1		PHI-EVM Controller Kitting item Edge# 6591636	PA007	Texas Instruments
J1, J2, J3, J4, J5, J6, J7, J8	8		Connector, SMA, TH	142-0701-201	Cinch Connectivity
J9	1		Terminal Block, 3.5 mm, 3x1, Tin, TH	0393570003	Molex
J10	1		Header(Shrouded), 19.7 mil, 30x2, Gold, SMT	QTH-030-01-L-D-A	Samtec
J11	1		Header, 100 mil, 16x2, Gold, TH	TSW-116-07-G-D	Samtec
JP1, JP2, JP3, JP4, JP5, JP6, JP7, JP8, JP9	9		Header, 100 mil, 3x1, Gold, TH	TSW-103-07-G-S	Samtec
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	THT-14-423-10	Brady

Designator	Qty	Value	Description	Part Number	Manufacturer
R2, R4, R5, R6, R16, R18, R19, R20, R30, R32, R33, R34, R46, R48, R49, R50	16	1.00k	RES, 1.00 k, 1%, 0.1 W, 0603	RC0603FR-071KL	Yageo
R7, R8, R21, R22, R35, R36, R51, R52	8	10.0	RES, 10.0, 1%, 0.1 W, 0603	RC0603FR-0710RL	Yageo
R10, R12, R13, R14, R24, R26, R27, R28, R38, R40, R41, R42, R54, R56, R57, R58, R69, R86, R107, R115, R116	21	0	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	RMCF0603ZT0R00	Stackpole Electronics Inc
R43, R44	2	20.0k	RES, 20.0 k, 1%, 0.1 W, 0603	RC0603FR-0720KL	Yageo
R61, R62, R90, R91, R103, R105, R110, R111, R112	9	10.0k	RES, 10.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	RMCF0603FT10K0	Stackpole Electronics Inc
R65, R66, R67, R68, R70, R71, R73, R74, R75, R76, R79, R80, R81, R82, R83, R84, R85, R87, R88, R89, R92, R93, R94, R95, R96, R97, R98, R99, R100, R101	30	49.9	RES, 49.9, 1%, 0.1 W, 0603	RC0603FR-0749R9L	Yageo
R72, R104	2	1.00	RES, 1.00, 1%, 0.1 W, 0603	RC0603FR-071RL	Yageo
R108	1	120k	RES, 120 k, 1%, 0.1 W, 0603	RC0603FR-07120KL	Yageo
R109	1	0.22	RES, 0.22, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	ERJ-3RQFR22V	Panasonic
R113	1	5.11	RES, 5.11, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06035R11FKEA	Vishay-Dale
R114	1	100k	RES, 100 k, 1%, 0.1 W, 0603	RC0603FR-07100KL	Yageo
R117, R118	2	6.65k	RES, 6.65 k, 1%, 0.1 W, 0603	RC0603FR-076K65L	Yageo
S1	1		Switch, Tactile, SPST-NO, 0.05A, 12V, SMD	EVQPNF04M	Panasonic
S2	1		Switch, Slide, SPDT 100 mA, SMT	CAS-120TA	Copal Electronics
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8, SH-J9	9	1x2	Shunt, 100 mil, Flash Gold, Black	SPC02SYAN	Sullins Connector Solutions
TP1, TP2, TP3, TP4, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13	12		Test Point, Multipurpose, Red, TH	5010	Keystone
TP5, TP14	2		Test Point, Multipurpose, Black, TH	5011	Keystone
U1, U2, U3, U4	4		1.1 nV/rtHz Noise, Low Power, Precision Operational Amplifier, 4.5 to 36 V, -40 to 125 degC, 8-pin SOP (DDA8), Green (RoHS & no Sb/Br)	OPA2211AIDDA	Texas Instruments
U5	1		Analog to Digital Converters - ADC 16B,8Ch,Sim Sampling Bipolar Inp ADC	ADS8568SPM	Texas Instruments
U6	1		5ppm/C High-Precision Voltage Reference with Integrated High-Bandwidth Buffer, DGK0008A (VSSOP-8)	REF6025IDGKR	Texas Instruments
U7	1		I2C BUS EEPROM (2-Wire), TSSOP-B8	BR24G32FVT-3AGE2	Rohm
U8	1		36V, 1A, 4.17µVRMS, RF Low-Dropout (LDO) Voltage Regulator, RGW0020A (VQFN-20)	TPS7A4700RGWR	Texas Instruments

Designator	Qty	Value	Description	Part Number	Manufacturer
U9	1		Single 2-Input Positive-OR Gate, DRL0005A, LARGE T&R	SN74AHC1G32DRLR	Texas Instruments
C9, C11, C21, C23, C27, C29, C33, C35	0	0.1uF	CAP, CERM, 0.1 µF, 50 V, ± 10%, X7R, 0603	GRM188R71H104KA93D	MuRata
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A
R1, R3, R9, R11, R15, R17, R23, R25, R29, R31, R37, R39, R45, R47, R53, R55	0	0	RES, 0, 5%, 0.1 W, 0603	RC0603JR-070RL	Yageo
R59, R64	0	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	RC0603FR-0710KL	Yageo
R77, R78, R102, R106	0	10.0k	RES, 10.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	RMCF0603FT10K0	Stackpole Electronics Inc

A.2 Layout

Top and Bottom Layer ADS8568EVM shows the top and bottom layers. All signals are on top and bottom.

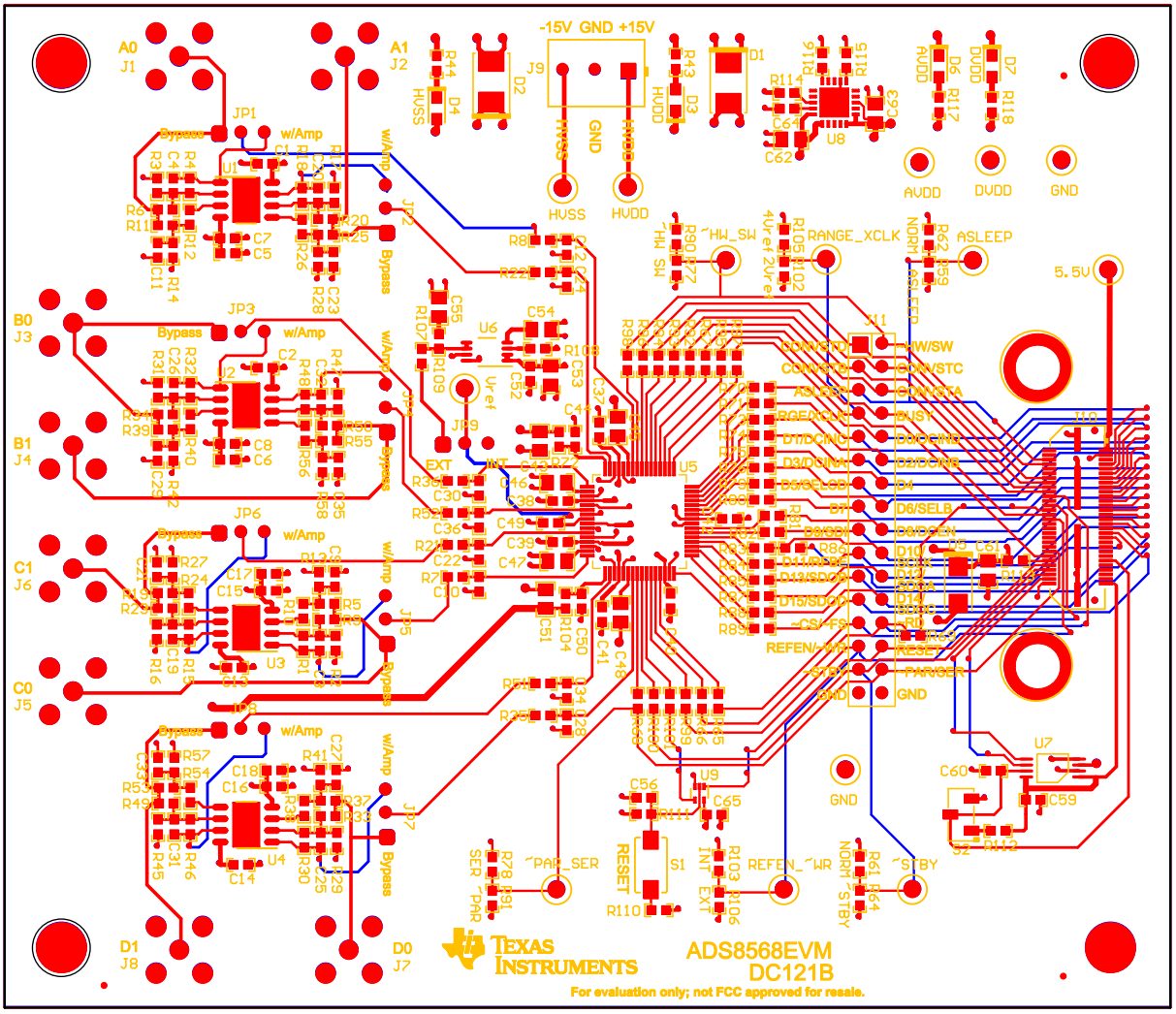

Figure A-1. Top and Bottom Layer ADS8568EVM

Inner Power Layer shows all power supply connections (AVDD, DVDD, HVDD, and HVSS).

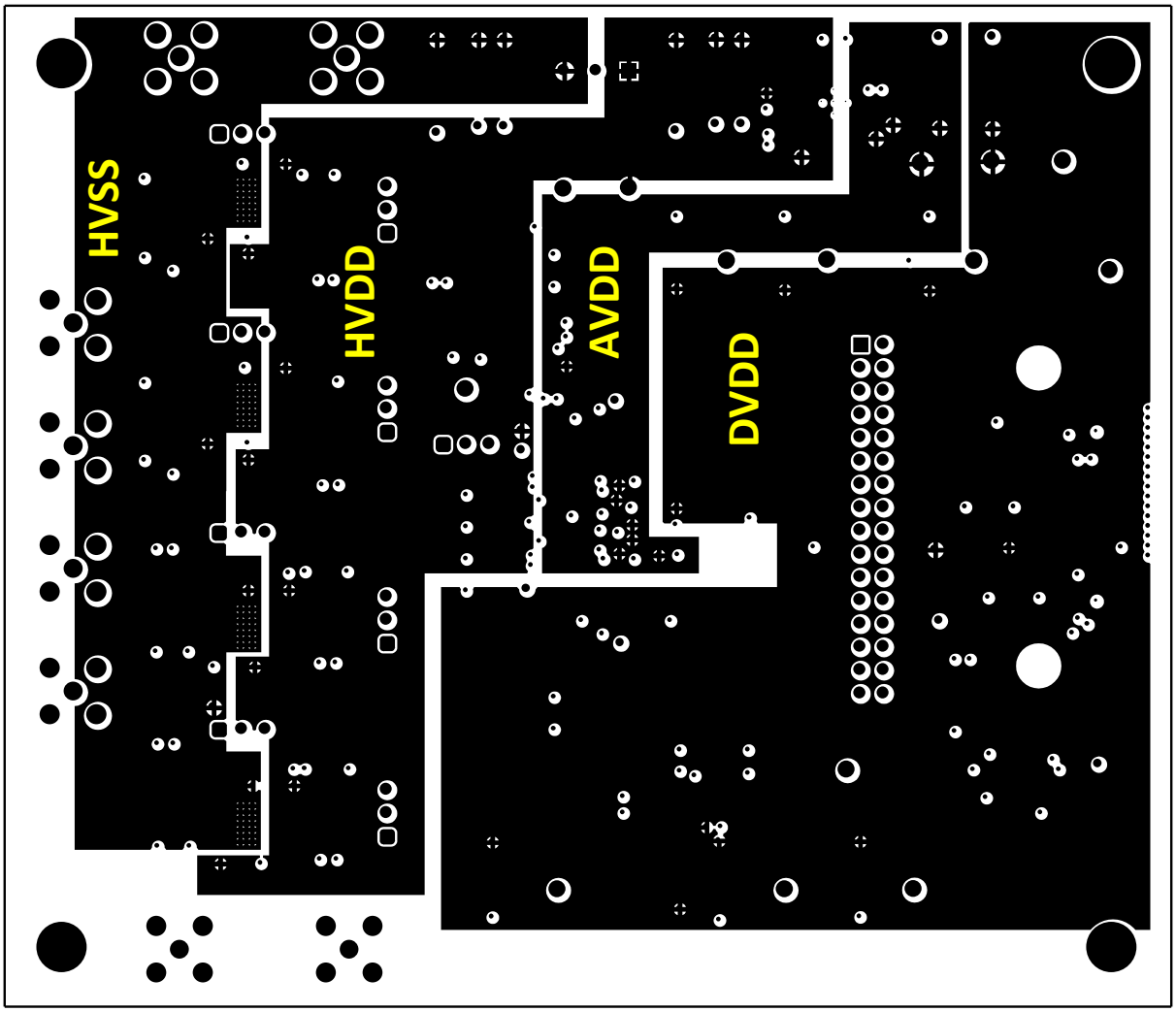

Figure A-2. Inner Power Layer

Inner Ground Layer shows the internal ground layer. All GND connections are to this layer using vias.

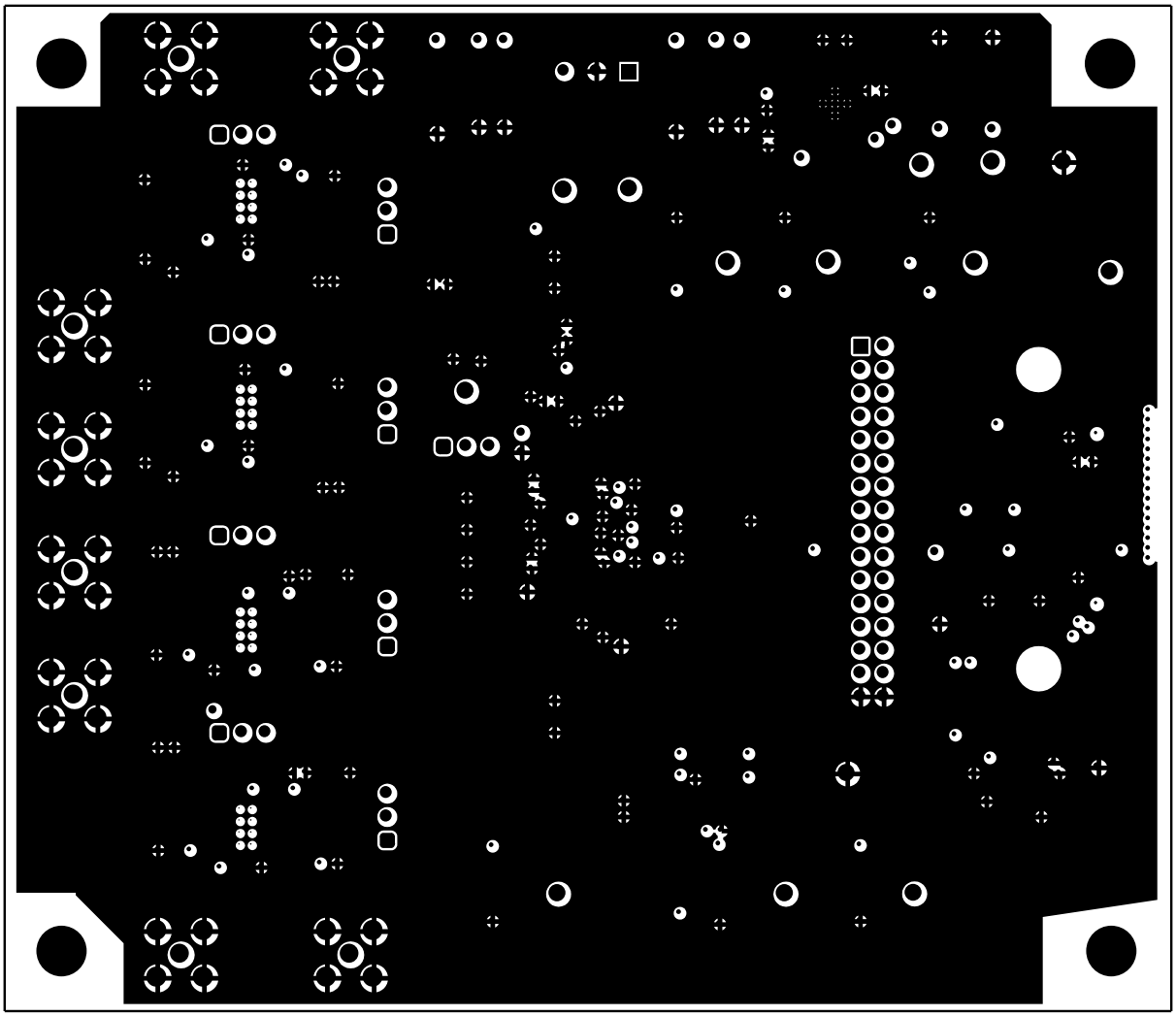

Figure A-3. Inner Ground Layer

A.3 Schematic

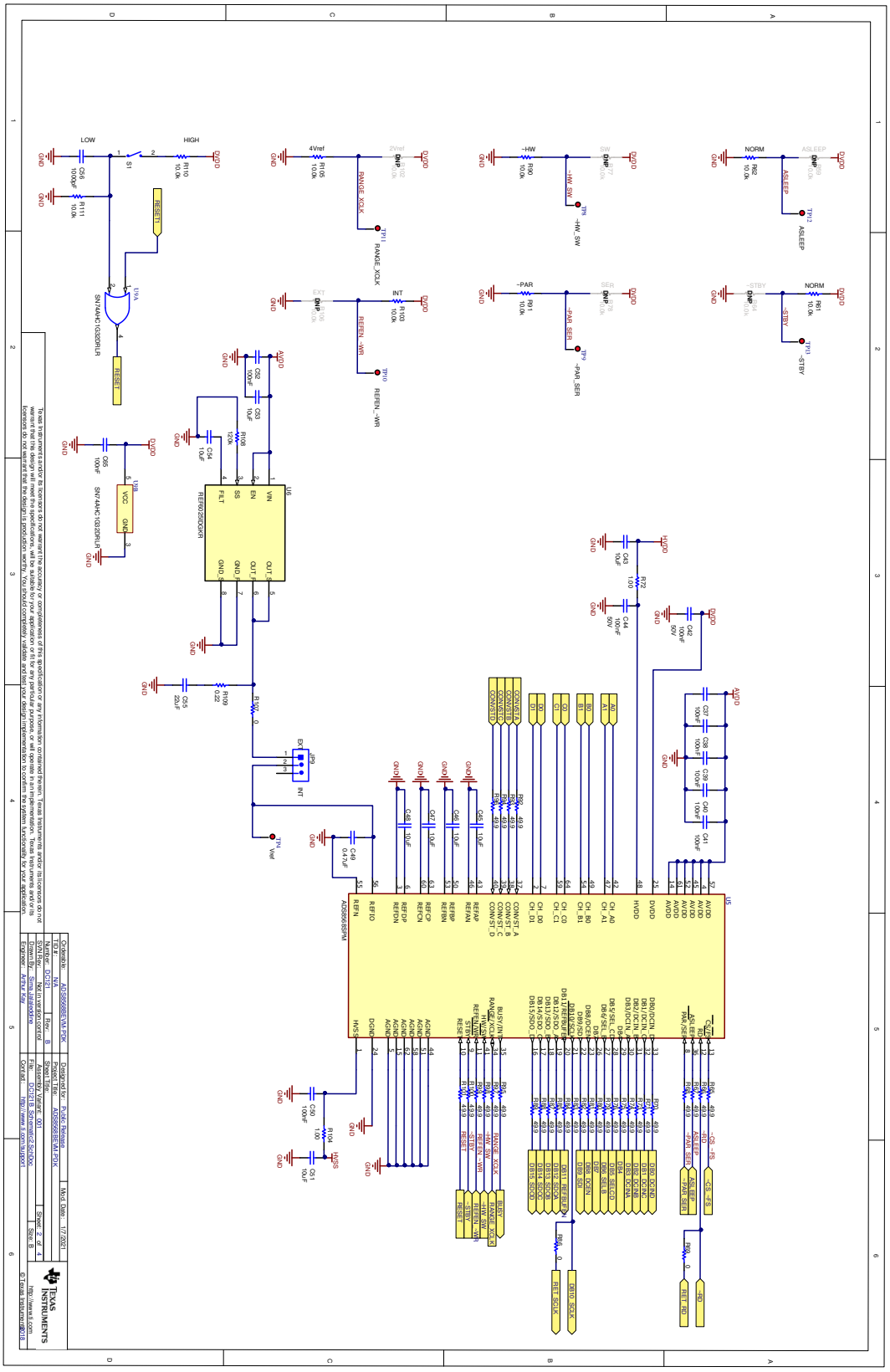

Figure A-4. ADC schematic

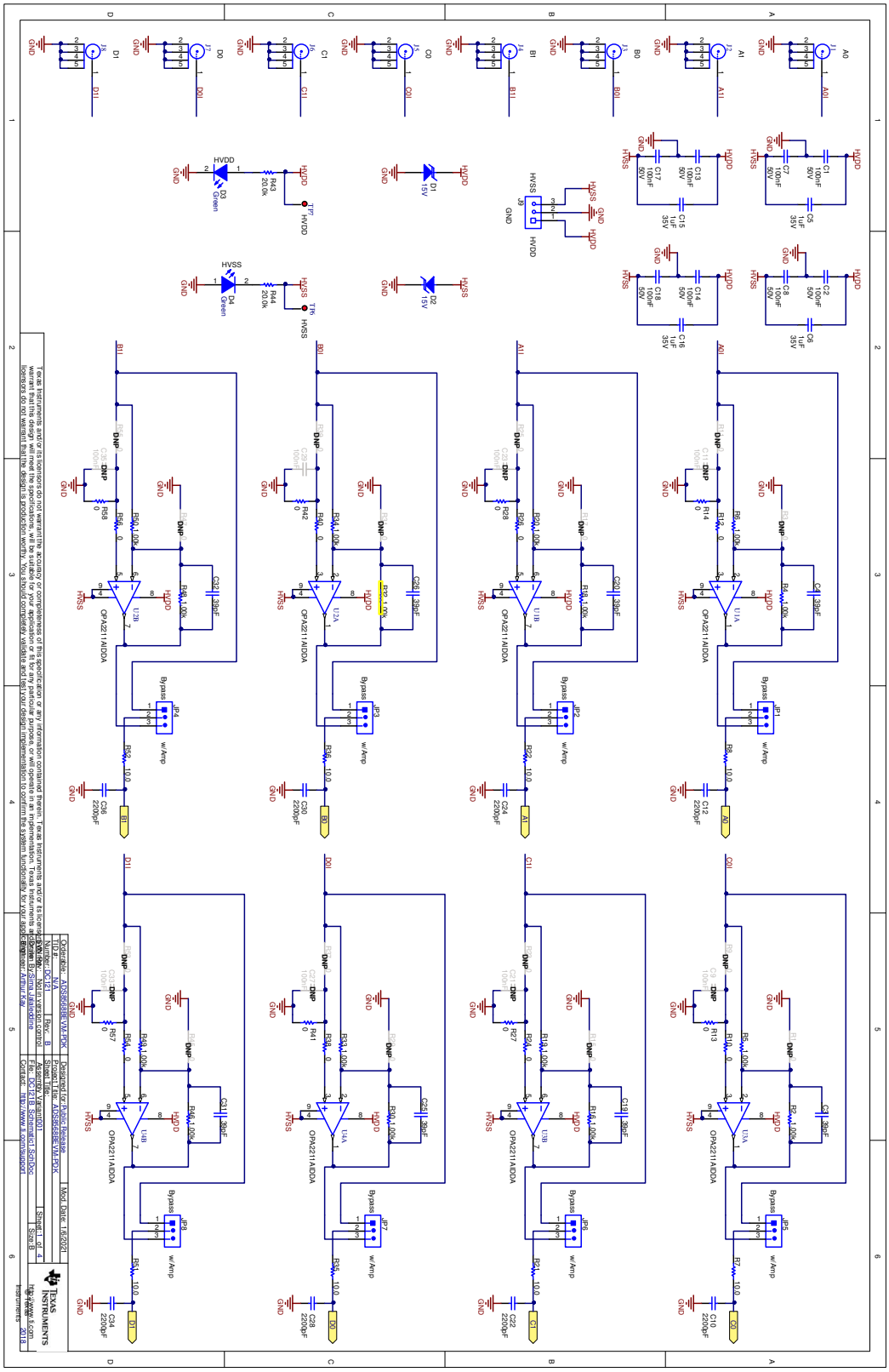

Figure A-5. ADC Drive Schematic

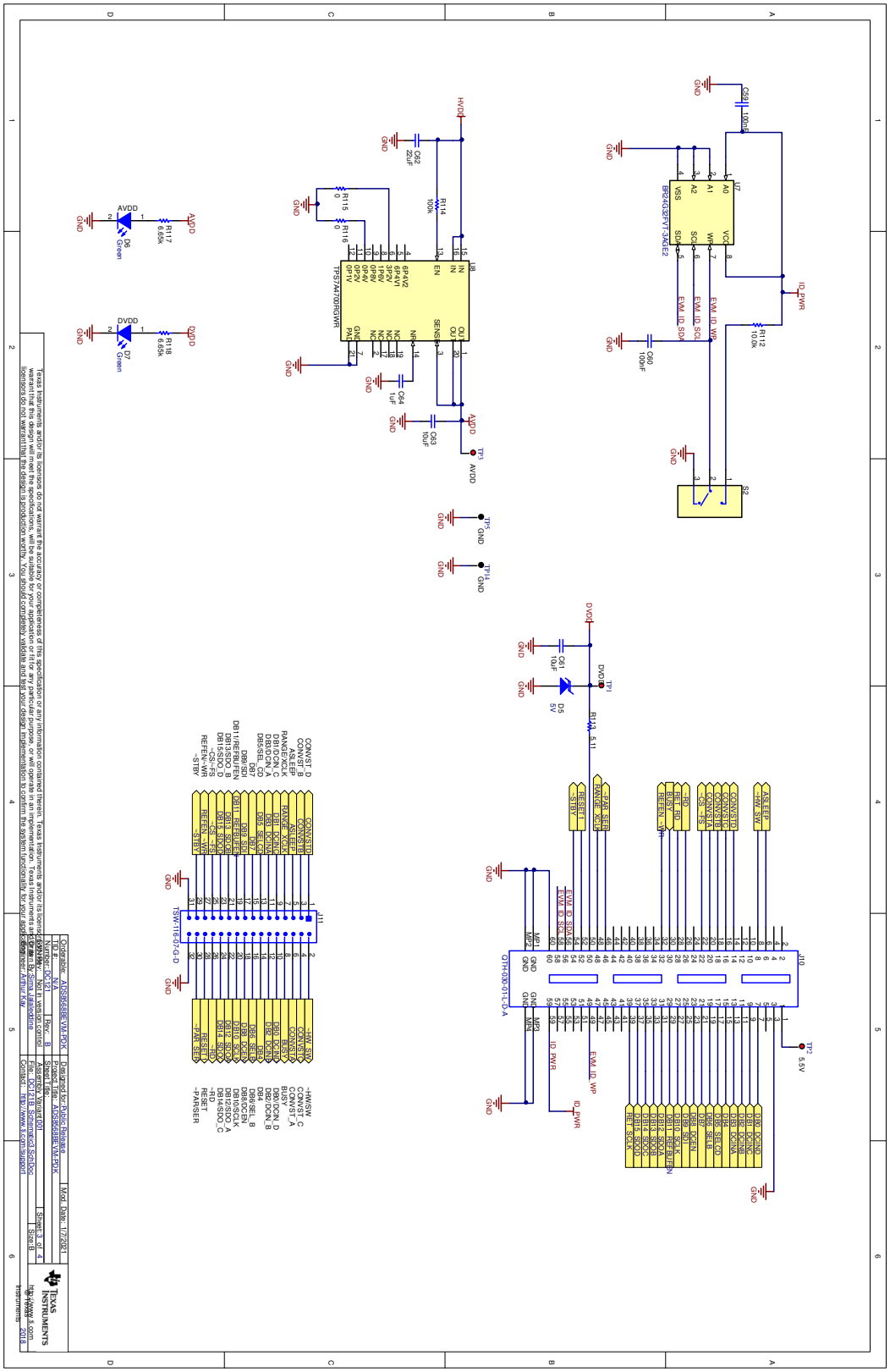

Figure A-6. Power and PHI Connections schmatic

B Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (February 2020) to Revision E (May 2021)	Page
• Added *Evaluation Module* to document title	0
• Corrected spelling in *Abstract* section	1

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