

EVM User's Guide: ADS1282V2EVM-PDK

ADS1282EVM-PDK Evaluation Module



Description

The ADS1282EVM is a platform for evaluating the performance of the ADS1282, a high performance, 2-channel, 31-bit, delta-sigma ADC. The ADS1282 board includes the ADS1282 and all the peripheral analog circuits and components required to extract optimum performance from the ADC. The evaluation kit includes the ADS1282EVM board and the precision host interface (PHI) controller board that enables the accompanying computer software to communicate with the ADC over Universal Serial Bus (USB) for data capture, configuration, and analysis.

Get Started

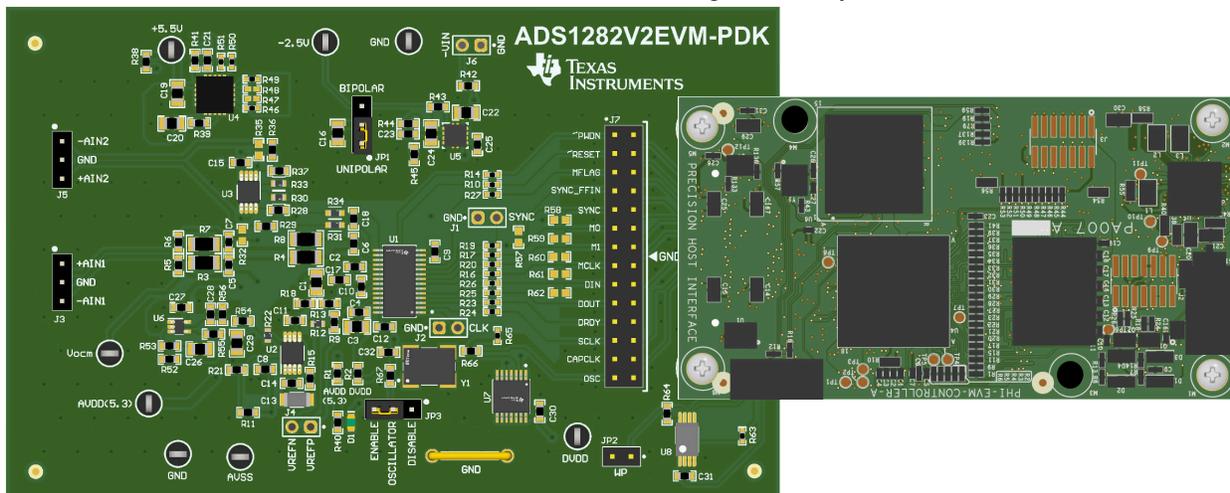
1. Order ADS1282EVM-PDK from ti.com
2. Download and install the [ADS1282EVM-PDK-GUI](#) software
3. Connect the ADS1282EVM to the computer with the included USB cable
4. Launch the ADS1282EVM GUI from the start menu
5. Refer to the [ADS1282 data sheet](#) for IC details
6. Visit the [E2E forums](#) for support and questions

Features

- High resolution: 130dB SNR (250SPS)
- High accuracy: THD: -122 dB, INL: 0.5ppm
- Low-noise PGA
- Two-channel input mux
- Inherently-stable modulator with fast responding overrange detection
- Flexible digital filter:
 - Sinc + FIR + IIR (selectable)
 - Linear or minimum phase response
 - Programmable high-pass filter
 - Selectable FIR data rates: 250SPS to 4kSPS
- Filter bypass option
- Low power consumption: 25mW
 - Shutdown: 10 μ W
- Offset and gain calibration engine
- SYNC input
- Analog supply:
 - Unipolar (+5V) or bipolar (± 2.5 V)
- Digital supply: 1.8V to 3.3V

Applications

- Energy exploration
- Seismic monitoring
- High-accuracy instrumentation



1 Evaluation Module Overview

1.1 Introduction

The ADS1282 is a high-performance, single-chip, delta-sigma analog-to-digital converter (ADC) with an integrated, low-noise programmable gain amplifier (PGA) and two-channel input multiplexer (mux). The ADS1282 is an excellent choice for the demanding needs of energy exploration and seismic monitoring environments. The PHI board primarily serves three functions:

- Provides a communication interface from the EVM to the computer through a USB port
- Provides the digital input and output signals necessary to communicate with the ADS1282
- Supplies power to all active circuitry on the ADS1282EVM board

This user's guide describes the characteristics, operation, and use of the ADS1282 evaluation module (EVM). The ADS1282EVM enables the evaluation of the device through a USB interface. This user's guide includes complete circuit descriptions, schematic diagrams, and a bill of materials. Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the ADS1282EVM.

1.2 Performance Development Kit Contents

The ADS1282EVM Performance Development Kit (PDK) includes the following features (Figure 1-1):

- Hardware and software required for diagnostic testing as well as accurate performance evaluation of the ADS1282.
- The PHI controller, which provides a convenient communication interface to the ADS1282 over USB 2.0 (or higher).
- Easy-to-use evaluation software for 64-bit Microsoft® Windows®.
- Windows 10 or 11 operating systems.
- The software suite includes graphical tools for data capture, histogram analysis, spectral analysis, and custom configuration of the ADS1282. This suite also has a provision for exporting data to a text file for post-processing.

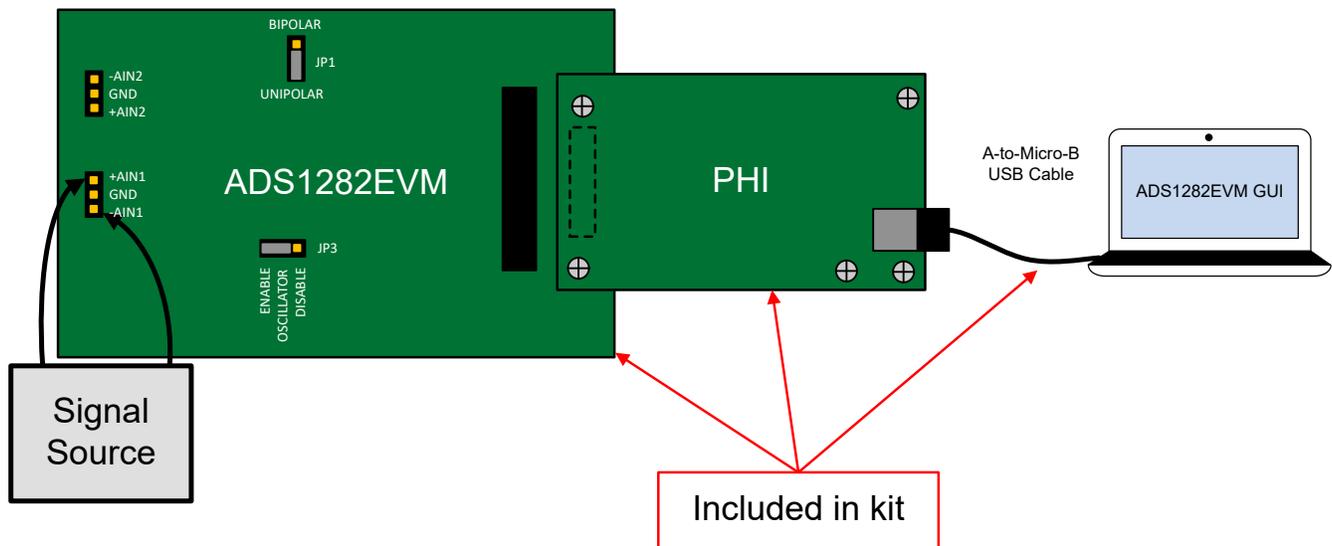


Figure 1-1. System Connection for Evaluation

1.3 Specifications

The following specifications are applicable to the ADS1282EVM board and the PHI board.

Table 1-1. ADS1282EVM-PDK Specifications

PARAMETER	CONDITIONS	VALUE
Temperature	Recommended operating free-air temperature range, T_A	$15^{\circ}\text{C} \leq T_A \leq 35^{\circ}\text{C}$
Power supply input range (bipolar)	Recommended voltage range for J6 (-Vin) to GND	$-5\text{V} \leq -V_{in} \leq -3\text{V}$
Analog input voltage	Absolute input voltage to GND (unipolar)	$0.7\text{V} \leq A_{INP} \leq 4.05\text{V}$
		$0.7\text{V} \leq A_{INN} \leq 4.05\text{V}$
	Absolute input voltage to GND (bipolar)	$-1.8\text{V} \leq A_{INP} \leq 1.55\text{V}$
		$-1.8\text{V} \leq A_{INN} \leq 1.55\text{V}$
External clock	Recommended frequency range (f_{CLK})	1MHz to 4.096MHz

1.4 Device Information

Please refer to [ADS1282 data sheet](#) for complete specifications.

Table 1-2. ADS1282 Specifications

DEVICE SPECIFICATION	VALUE
Package size	9.7mm x 6.4mm
Operating temperature range	-40°C to 85°C
AVSS to DGND supply voltage	-2.6V to 0V
AVDD to AVSS supply voltage	4.75V to 5.25V
DVDD to DGND supply voltage	1.65V to 3.6V
Reference input voltage ($V_{REF} = V_{REFP} - V_{REFN}$)	0.5V to $(AVDD - AVSS) + 0.2\text{V}$

2 Hardware

The ADS1282EVM is designed for easy interfacing with analog sources. This section covers the details of the front-end circuit, including jumper configurations for different input ranges and clock sources, as well as board connectors for signal sources.

2.1 EVM Analog Input Options

Connect differential analog input signals to pins +AINx and -AINx (x denoting channels 1 and 2) of headers J3 and J5. Enable single-ended inputs for channel 1 by connecting -AIN1 to system ground (short pins 2-3 of header J3) and apply the signal to pin 1 of header J3. For channel 2, connect -AIN2 to system ground (short pins 1-2 of header J5) and apply the signal to pin 3 of header J5.

Each of the differential input pairs accepts up to a $5V_{PP}$ differential signal, with an offset (common-mode) voltage from 0V up to +2.5V. The REF6050 provides the EVM default 5V reference voltage. Refer to Figure 2-1 for details.

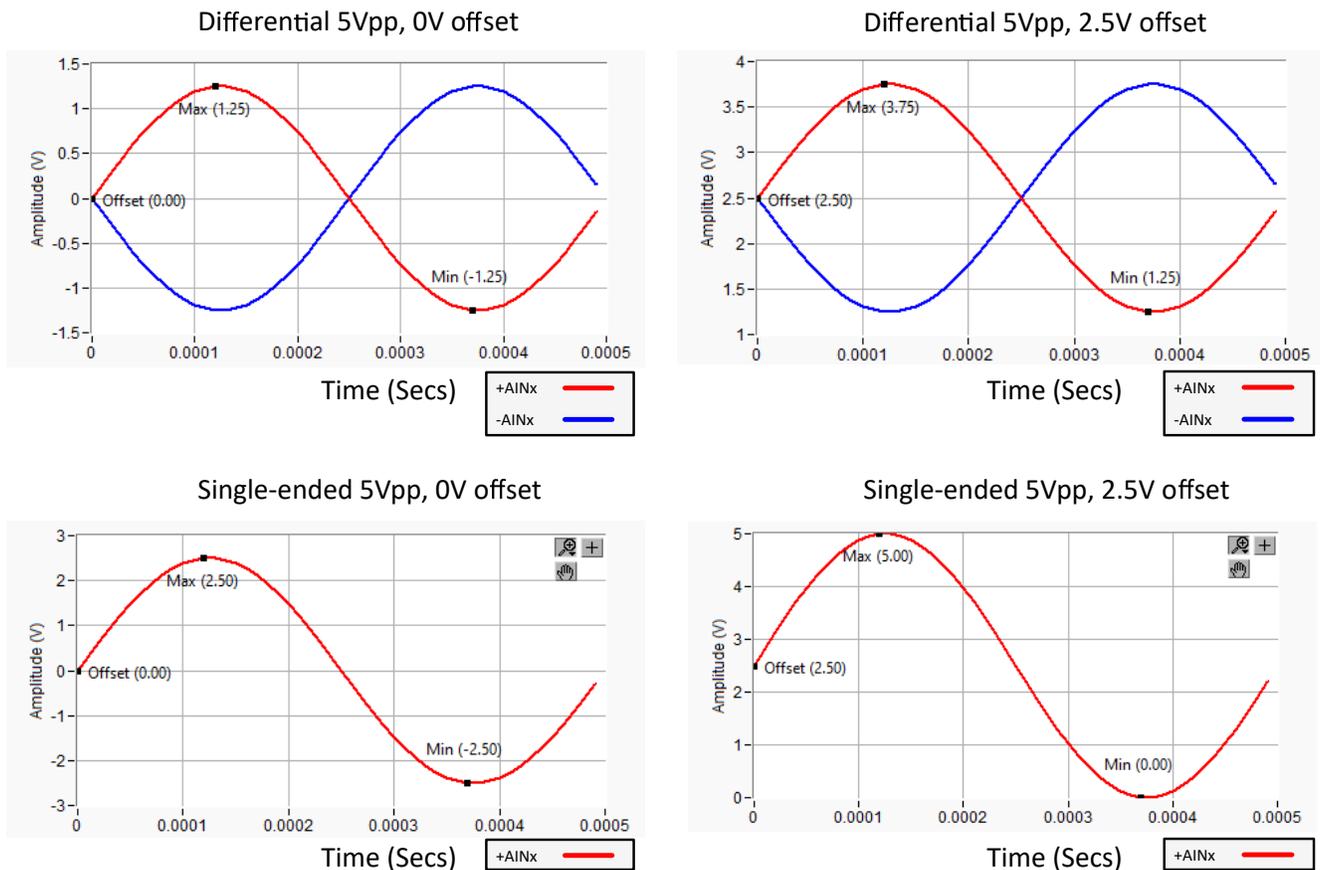


Figure 2-1. Maximum Input Signal Range ($V_{REF} = 5V$)

2.2 Common-Mode Amplifier

Figure 2-2 shows the OPA379 op-amp circuit used to generate the common-mode voltage that the ADS1282 requires from the input signals. The circuit output, V_{ocm} , provides a voltage that is mid-scale with respect to the selected input range of the ADS1282. In unipolar mode, V_{ocm} is +2.5V relative to ground. In bipolar mode, V_{ocm} is 0V relative to ground.

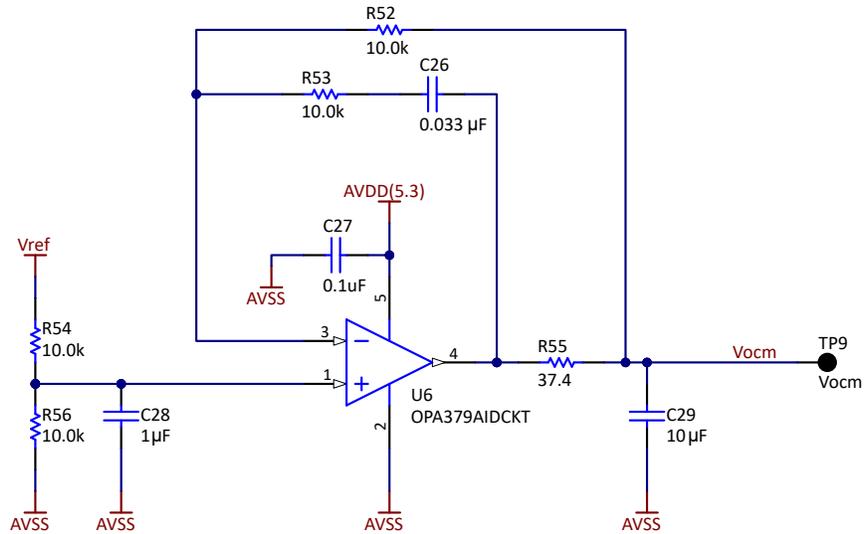


Figure 2-2. Common-Mode Amplifier

2.3 Analog Input 1 Circuit

Figure 2-3 shows the front-end circuit to ADC input channel 1. V_{ocm} supplies a DC shift to the differential inputs connected to header J3. In unipolar mode, differential-output sources with a common-mode voltage equal to ground (0V) are given a +2.5V DC shift. The DC shift raises the input signal common-mode voltage by the same amount (2.5V), and the signal at the inputs to the ADS1282 has a common-mode voltage close to mid-scale of the unipolar input range (0-5V). The mid-scale common-mode voltage makes analog input channel 1 best for bipolar differential signals centered around a 0V common-mode voltage.

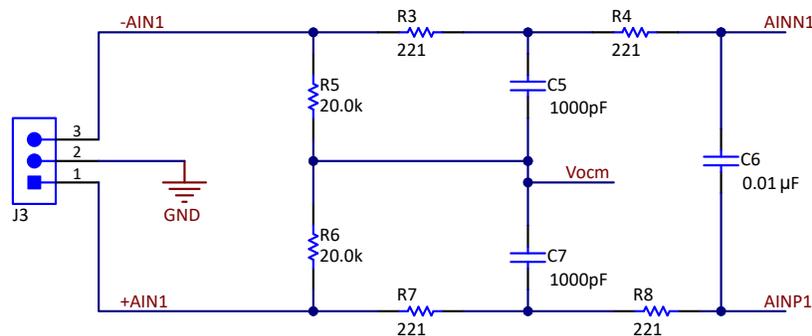


Figure 2-3. Analog Input 1 Circuit

2.4 Analog Input 2 Amplifier

Figure 2-4 shows the fully differential amplifier circuit (THS4551) that drives ADC input channel 2. This amplifier circuit provides flexibility for different input configurations, including single-ended and differential inputs. Additionally, the circuit enables signals with different common-mode voltages to easily interface with the ADS1282.

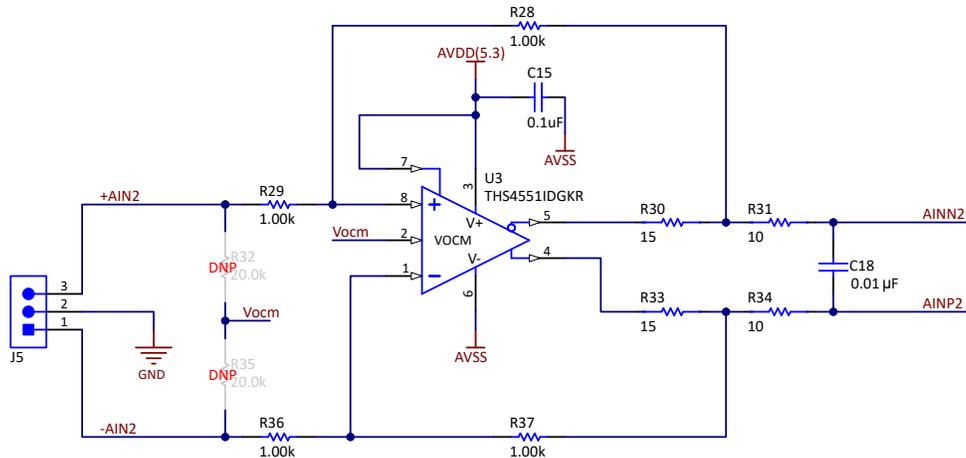


Figure 2-4. Analog Input 2 Amplifier

2.5 Voltage Reference

Figure 2-5 shows the REF6050 voltage reference circuit. By default, the REF6050 connects to the ADS1282 through the 0Ω resistors R12 and R18. The REF6050 integrates a low output impedance buffer necessary for precision ADCs to maintain a steady reference voltage during the conversion process.

Use an external reference source in place of the REF6050 by removing R12 and R18, and installing header J4. The positive terminal of the voltage reference connects to header J4 pin 1, and the negative terminal to header J4 pin 2. The pins of header J4 can also be used as test points for the onboard REF6050. Use resistors R9 and R13 (not shown) as optional filter resistors when using an external voltage reference. Remove resistor R11 to disable the voltage output of the REF6050 voltage reference.

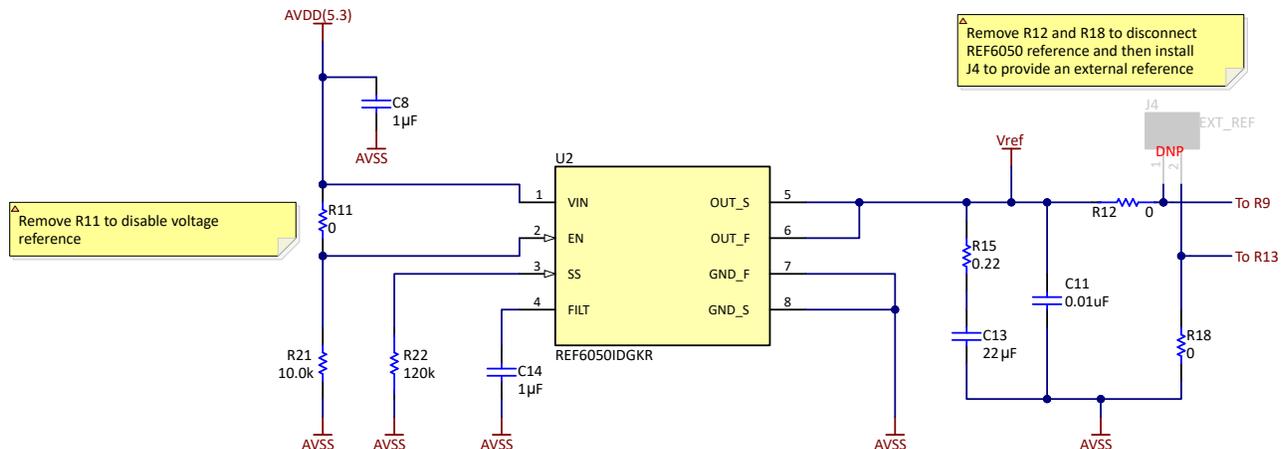


Figure 2-5. Onboard Voltage Reference

2.6 ADC Connections and Decoupling

Figure 2-6 shows all connections to the ADS1282 data converter (U1). Each power supply connection has a pair of 10 μ F and a 1 μ F decoupling capacitors. Make sure these capacitors are physically close to the device and have a good connection to the AVSS plane. The supply connections also have a series 0 Ω resistor. These resistors facilitate current measurement for the ADC. Each digital pin has a 49.9 Ω series resistor. These resistors smooth the edges of the digital signals to provide minimal overshoot and ringing.

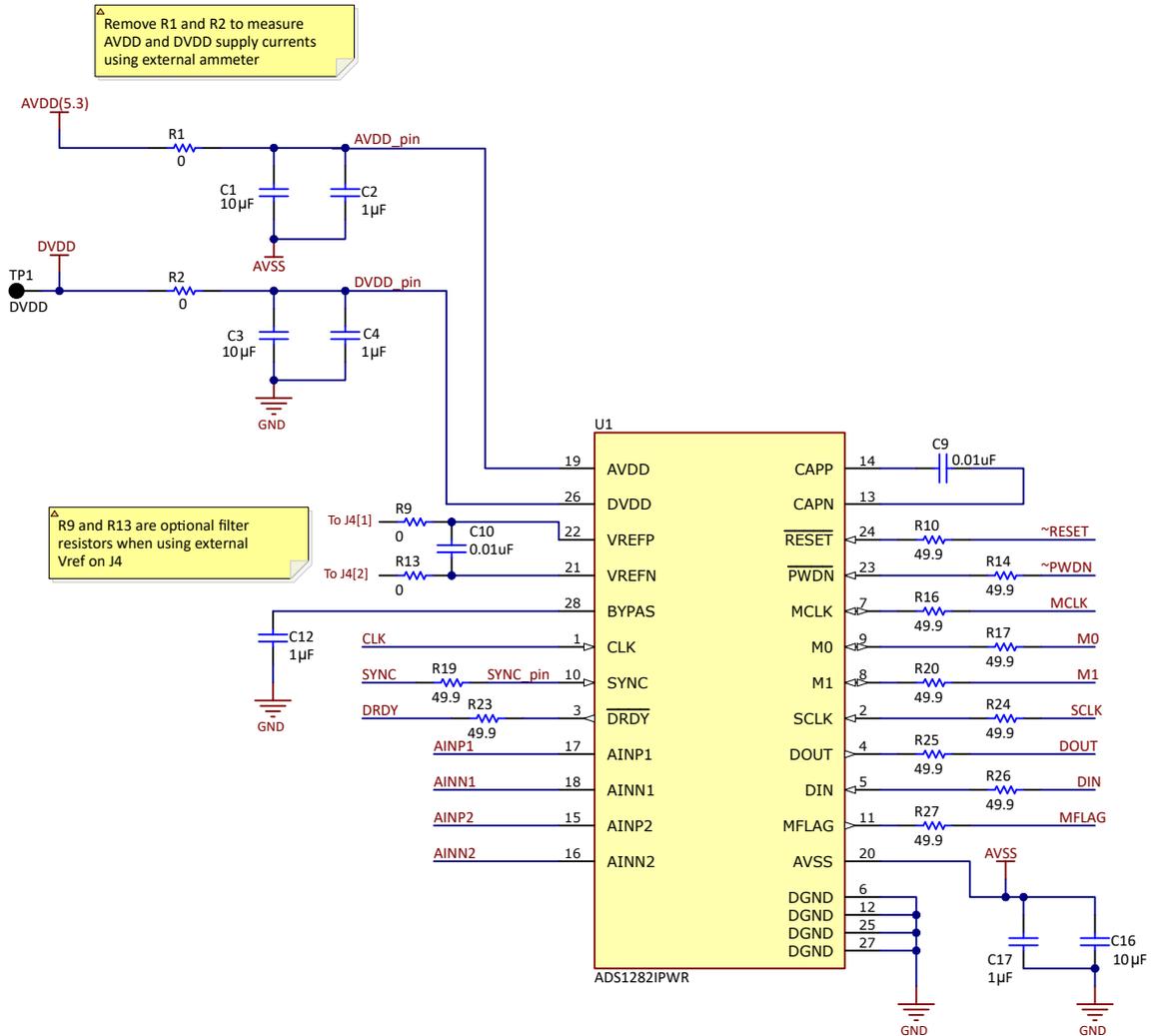


Figure 2-6. Connections and Decoupling

2.7 Power Supplies

By default, the PHI powers the ADS1282EVM circuitry from the computer power supply through USB without requiring an external power supply.

The EVM supports two different power configurations: unipolar, where the ADS1282 AVDD supply is set to 5V and AVSS is connected to GND; and bipolar operation, where AVDD is set to +2.5V and AVSS is set to -2.5V.

Unipolar operation mode does not require an external power supply, as the ADS1282EVM receives power for all the onboard circuitry directly from the PHI through USB.

Optionally, enable bipolar operation of the ADS1282EVM by using an external power supply. To do so, install header J6 and provide a voltage from -5V to -3V to pin 2 of header J6 (-VIN) while grounding pin 1 of header J6 (GND). Then, switch the shunt position on jumper JP1 to short pins 1-2 together.

Figure 2-7 shows the connection options for the external power supply that is required for bipolar EVM operation.

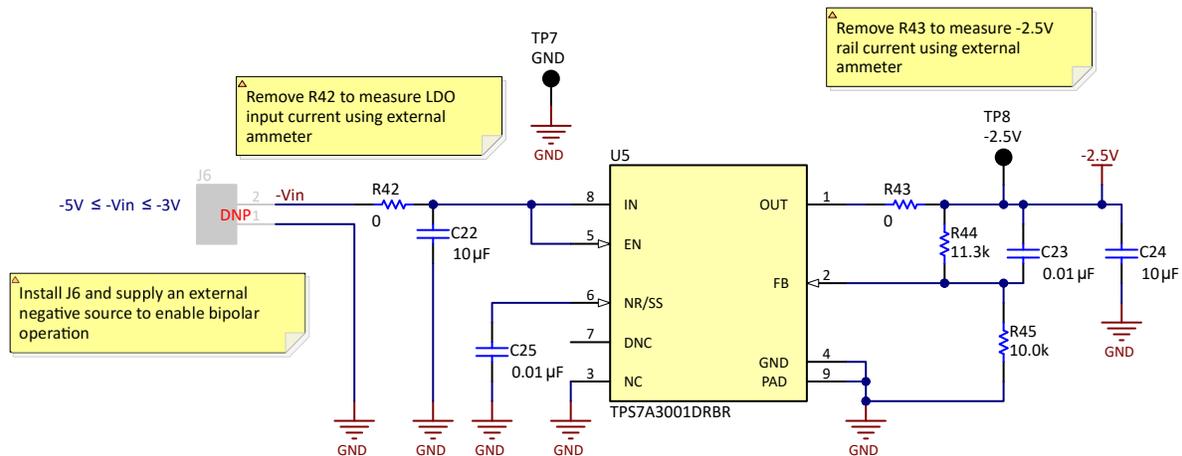


Figure 2-7. External Power Supply Connection

2.8 Low Dropout Regulators (LDO)

Figure 2-8 shows how the ADS1282 5.3V AVDD and -2.5V AVSS supplies are generated. The PHI provides power for AVDD. The user must apply an external power supply to generate the -2.5V rail for AVSS.

The TPS7A47-Q1 LDO regulates AVDD to 5.3V. The 5.3V LDO output is used for the AVDD connections and can be reprogrammed to different output voltages using R46, R47, R48, R49, R50, and R51. See Section 5.1 for possible configurations.

The TPS7A30 LDO generates the -2.5V rail for AVSS. This LDO is only supplied by external power on header J6. By default, AVSS is connected to GND with a shunt on jumper JP1, position 1-2. If AVSS is set to -2.5V for bipolar operation, connect an external negative supply to J6 and move the shunt on jumper JP2 to position 2-3. In this configuration, the voltage level for AVDD does not need to be changed. The 5.3V LDO is referenced to AVSS, so setting AVSS = -2.5V also changes AVDD to 2.8V with respect to GND.

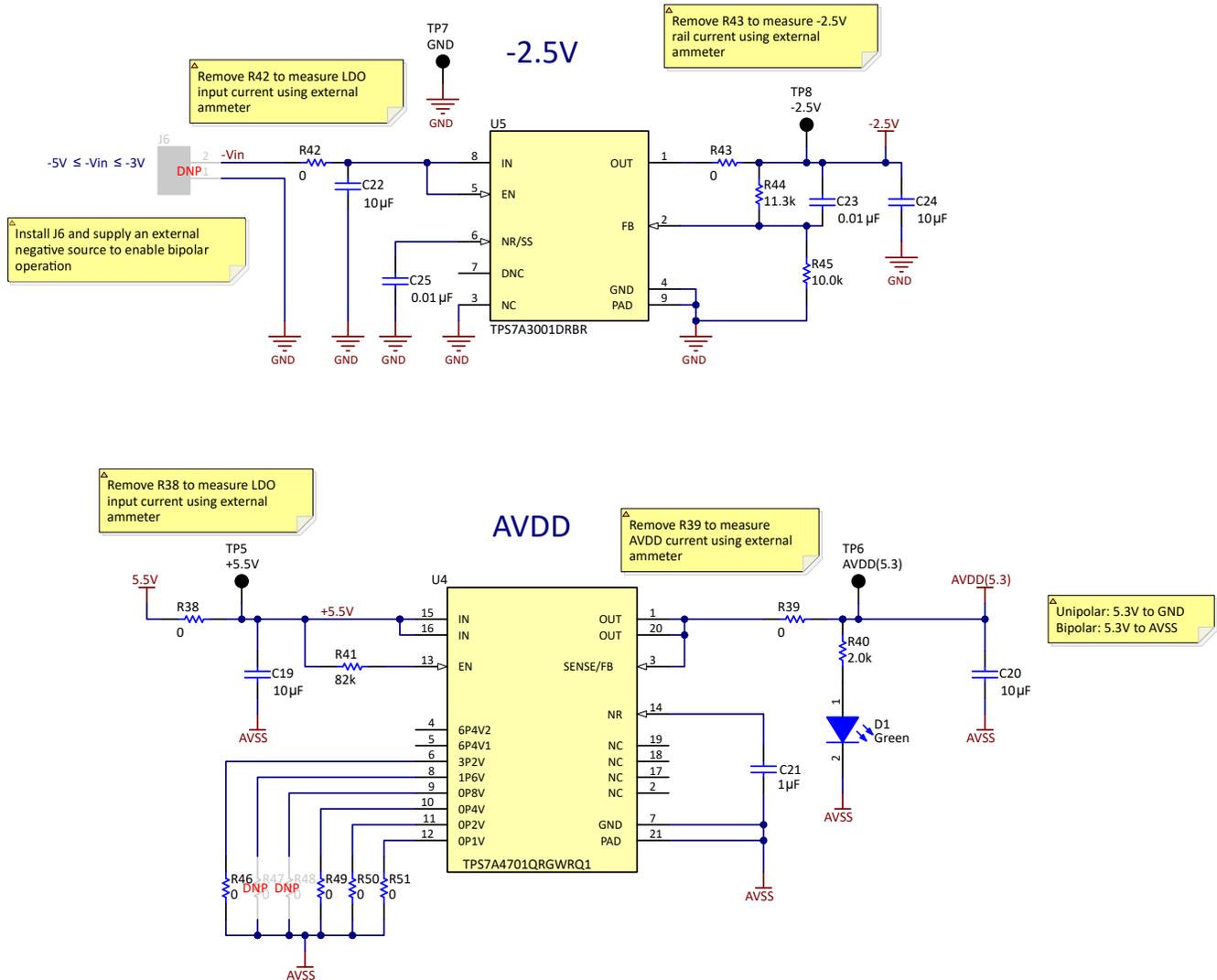


Figure 2-8. LDO Regulators: -2.5V (top), 5.3V (bottom)

2.11 Serial Interface

Figure 2-11 shows the digital connections between the ADS1282 and the PHI. The ADS1282 uses SPI serial communication in mode 0 (CPOL = 0, CPHA = 0) to configure the internal registers. The signal bank (J7) provides test points for the ADS1282EVM digital signals.

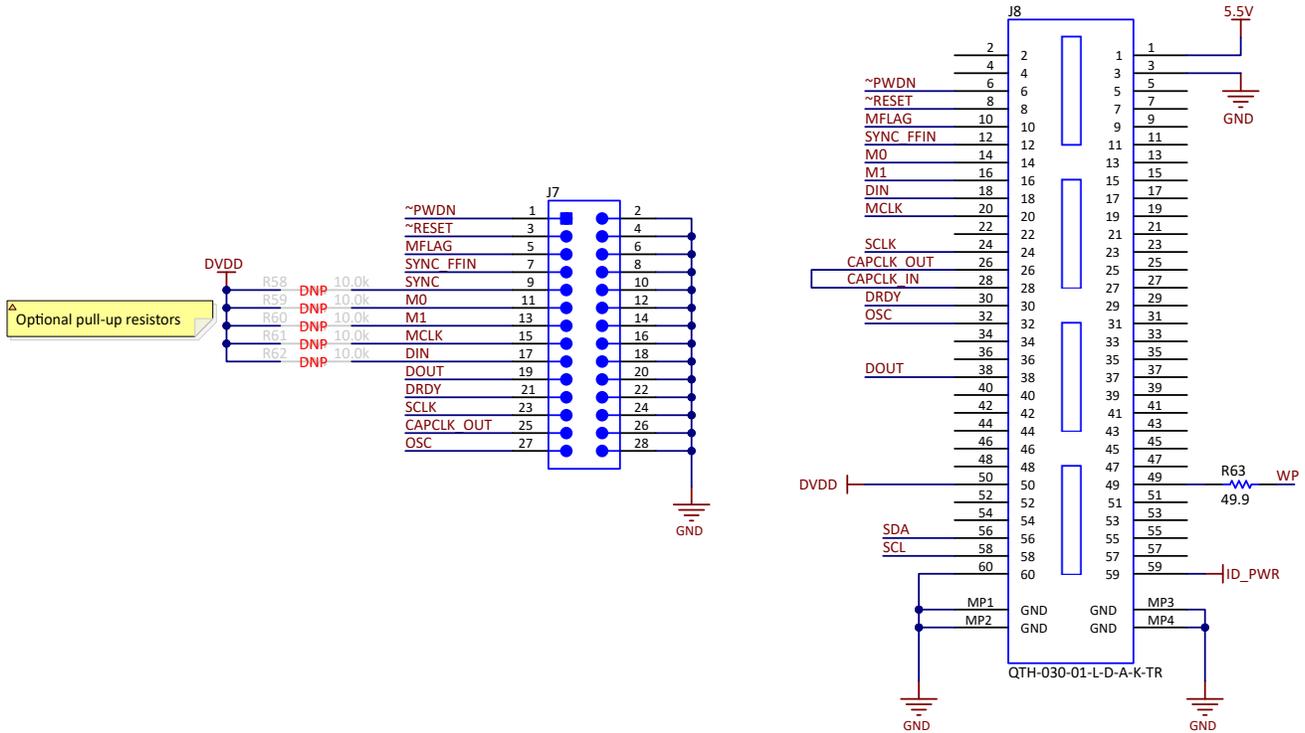


Figure 2-11. Connections to Digital Signals on PHI and Test Points

2.12 EEPROM

Figure 2-12 shows the EEPROM circuit the PHI uses to identify the EVM at power up. The EEPROM communicates with the PHI over an I2C bus that is not shared with the ADS1282. This circuit is not required by the ADS1282 for operation and is powered down when not used by the PHI.

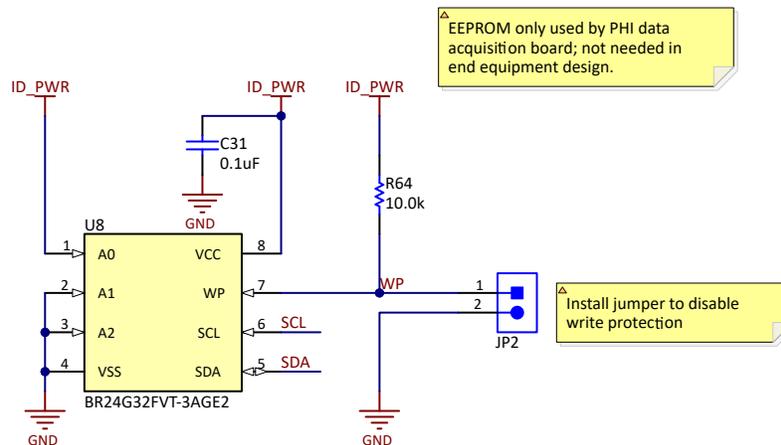


Figure 2-12. EEPROM for EVM ID

3 Software

3.1 Software Description

The ADS1282EVM-PDK-GUI software suite includes graphical tools for data capture, register configuration, time domain analysis, histogram analysis, and spectral analysis. This suite also has a provision for exporting data to a text file for post-processing.

3.2 ADS1282 EVM Software Installation

Download the latest version of the EVM GUI installer from the Tools and Software folder of the [ADS1282EVM](#) and run the GUI installer to install the EVM GUI software on your computer.

As shown in [Figure 3-1](#), accept the license agreement and follow the on-screen instructions to complete the installation. If the LabVIEW™ run-time engine has not already been installed, then a prompt to accept this license agreement appears.

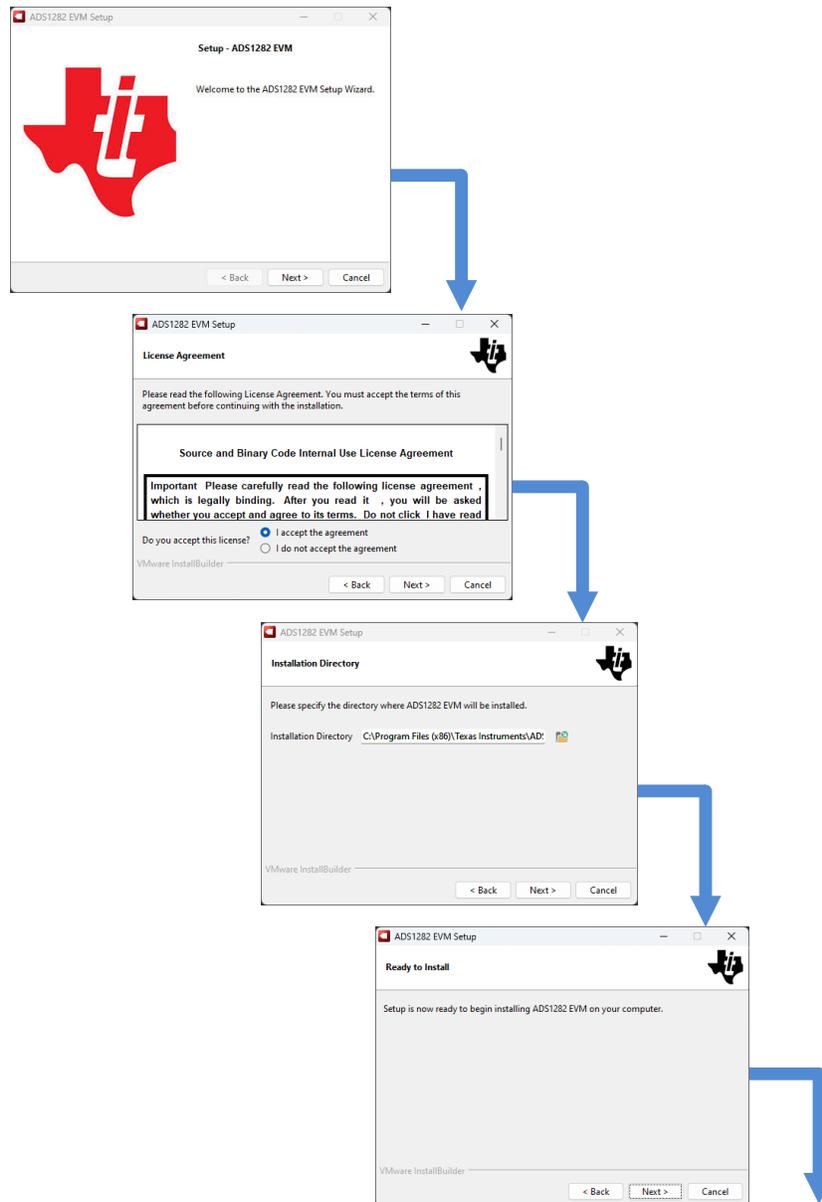


Figure 3-1. Software Installation and Prompts (1)

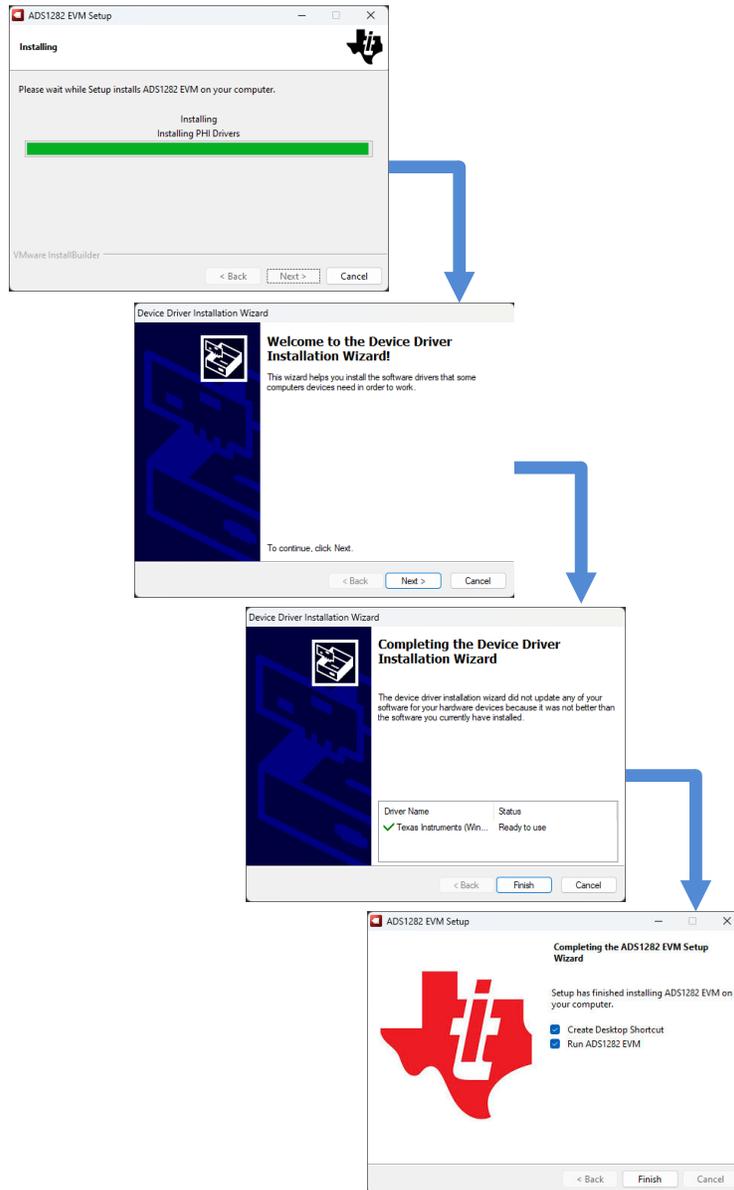


Figure 3-2. Software Installation and Prompts (2)

4 Implementation Results

4.1 EVM Operation

4.1.1 Evaluation Setup

Connect the EVM as shown in [Figure 4-1](#) after installing the software:

1. Physically connect P2 of the PHI to J8 of the ADS1282EVM. Install the included screws to provide a robust connection.
2. Connect the USB connector on the PHI to the computer.
 - a. LED D5 on the PHI lights up, indicating that the PHI is powered up.
 - b. LEDs D1 and D2 on the PHI start blinking to indicate that the PHI is booted up and communicating with the PC; [Figure 4-1](#) shows the resulting LED indicators.
3. Start the software GUI as shown in [Figure 4-2](#). Notice that the LEDs blink slowly when the FPGA firmware is loaded on the PHI. This loading takes a few seconds. LED D1 on the ADS1282EVM illuminates once a connection has been established.
4. Connect the differential signal generator to the ADS1282EVM inputs. The full-scale input range is $\pm 2.5V$ differential with a common mode from 0V to 2.5V. A typical input signal is a $4.8V_{PP}$ sinusoidal wave. This signal is adjusted just below the full-scale range to avoid clipping.
5. Verify the default jumper positions of the ADS1282EVM. Jumper JP1 is placed in the UNIPOLAR position (pins 1-2) by default. Jumper JP3 is placed in the ENABLE position (pins 2-3) by default.

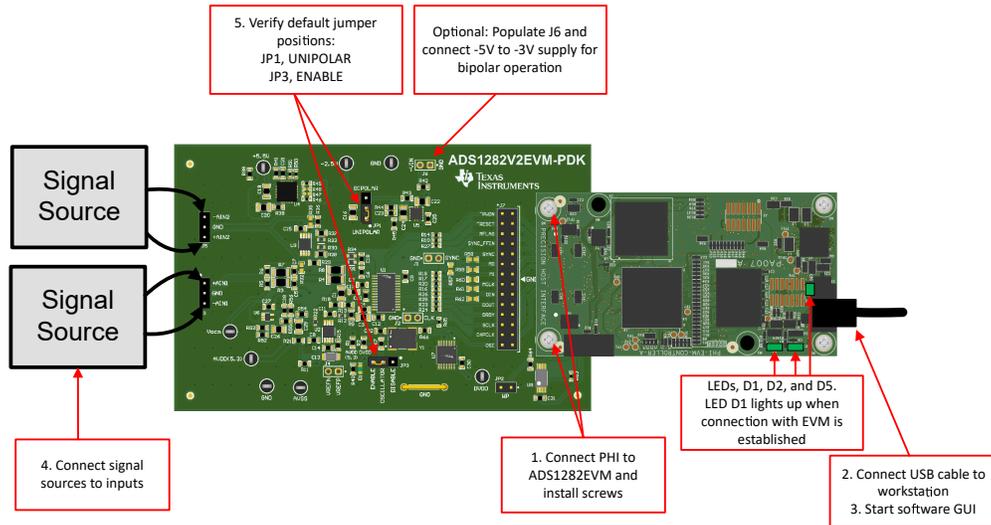


Figure 4-1. Connecting the Hardware to the ADS1282EVM

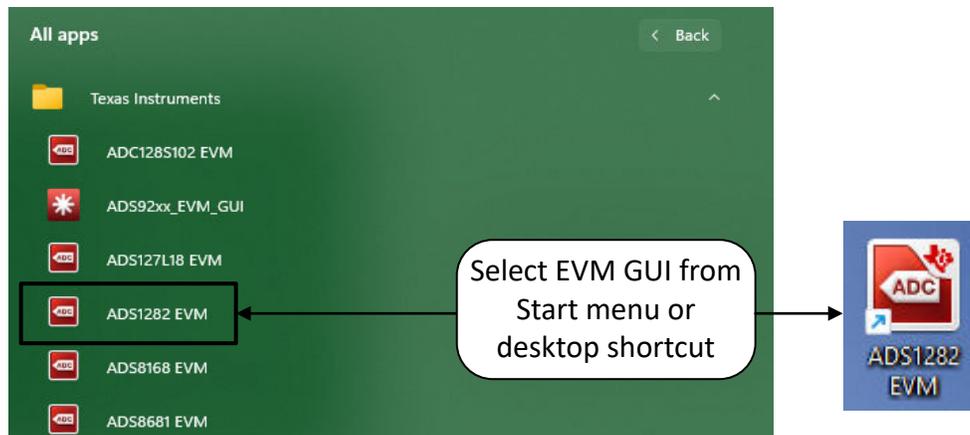
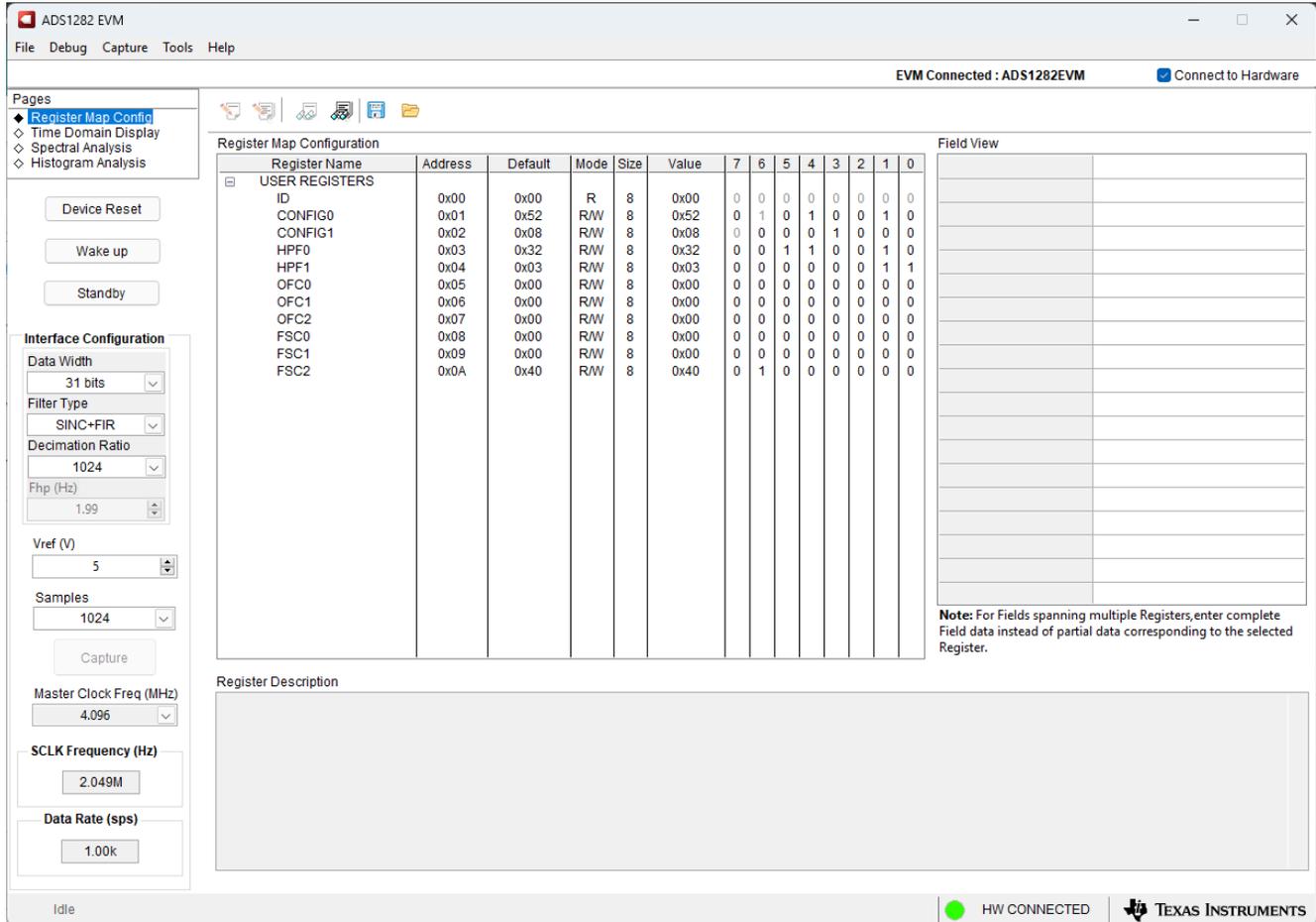


Figure 4-2. Launch the ADS1282EVM GUI Software

4.1.2 EVM Register Settings

Figure 4-3 shows the ADC register settings. Modify the registers to enable different device modes (such as filter settings and power settings). Access this page by selecting the Register Configurations under Pages on the left side of the GUI.



The screenshot shows the 'Register Map Configuration' page in the ADS1282 EVM GUI. The interface includes a sidebar with navigation options like 'Register Map Configuration', 'Time Domain Display', 'Spectral Analysis', and 'Histogram Analysis'. Below these are buttons for 'Device Reset', 'Wake up', and 'Standby'. The 'Interface Configuration' section on the left contains dropdown menus for 'Data Width' (31 bits), 'Filter Type' (SINC+FIR), 'Decimation Ratio' (1024), and 'Fhp (Hz)' (1.99). It also has input fields for 'Vref (V)' (5), 'Samples' (1024), 'Master Clock Freq (MHz)' (4.096), 'SCLK Frequency (Hz)' (2.049M), and 'Data Rate (sps)' (1.00k). A 'Capture' button is located below the 'Samples' field.

The main area displays a table for 'Register Map Configuration' with columns for Register Name, Address, Default, Mode, Size, Value, and bit fields 7 through 0. Below the table is a 'Field View' section and a 'Register Description' area.

Register Name	Address	Default	Mode	Size	Value	7	6	5	4	3	2	1	0
USER REGISTERS													
ID	0x00	0x00	R	8	0x00	0	0	0	0	0	0	0	0
CONFIG0	0x01	0x52	R/W	8	0x52	0	1	0	1	0	0	1	0
CONFIG1	0x02	0x08	R/W	8	0x08	0	0	0	0	1	0	0	0
HPF0	0x03	0x32	R/W	8	0x32	0	0	1	1	0	0	1	0
HPF1	0x04	0x03	R/W	8	0x03	0	0	0	0	0	0	1	1
OFC0	0x05	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0
OFC1	0x06	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0
OFC2	0x07	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0
FSC0	0x08	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0
FSC1	0x09	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0
FSC2	0x0A	0x40	R/W	8	0x40	0	1	0	0	0	0	0	0

Note: For Fields spanning multiple Registers, enter complete Field data instead of partial data corresponding to the selected Register.

Figure 4-3. EVM Register Configuration

4.1.2.1 Channel Configuration

Figure 4-4 shows how the MUX field of the CONFIG1 register can be used to switch between channels 1 and 2. Options available for this field are AINP1_AINN1, AINP1_AINN2, INT_SHORT, PARALLEL, and EXT_SHORT_AINN2. The Register Description section at the bottom of the Register Map Config page describes each option.

The screenshot displays the ADS1282 EVM software interface. The main window is titled "Register Map Configuration" and shows a table of registers. The CONFIG1 register is highlighted, with its address (0x02), default value (0x08), and current value (0x08) visible. The MUX field is selected, and a dropdown menu is open, showing options: AINP1_AINN1, AINP2_AINN2, INT_SHORT, PARALLEL, and EXT_SHORT_AINN2. The Register Description section at the bottom provides details for MUX[6:4] and CHOP[3:3].

Register Name	Address	Default	Mode	Size	Value	7	6	5	4	3	2	1	0
USER REGISTERS													
ID	0x00	0x00	R	8	0x00	0	0	0	0	0	0	0	0
CONFIG0	0x01	0x52	R/W	8	0x52	0	1	0	1	0	0	1	0
CONFIG1	0x02	0x08	R/W	8	0x08	1	0	0	0	1	0	0	0
HPF0	0x03	0x32	R/W	8	0x32	0	0	1	1	0	0	1	0
HPF1	0x04	0x03	R/W	8	0x03	0	0	0	0	0	0	1	1
OFC0	0x05	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0
OFC1	0x06	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0
OFC2	0x07	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0
FSC0	0x08	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0
FSC1	0x09	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0
FSC2	0x0A	0x40	R/W	8	0x40	0	1	0	0	0	0	0	0

Register Description

RESERVED_2[7:7]
Reserved

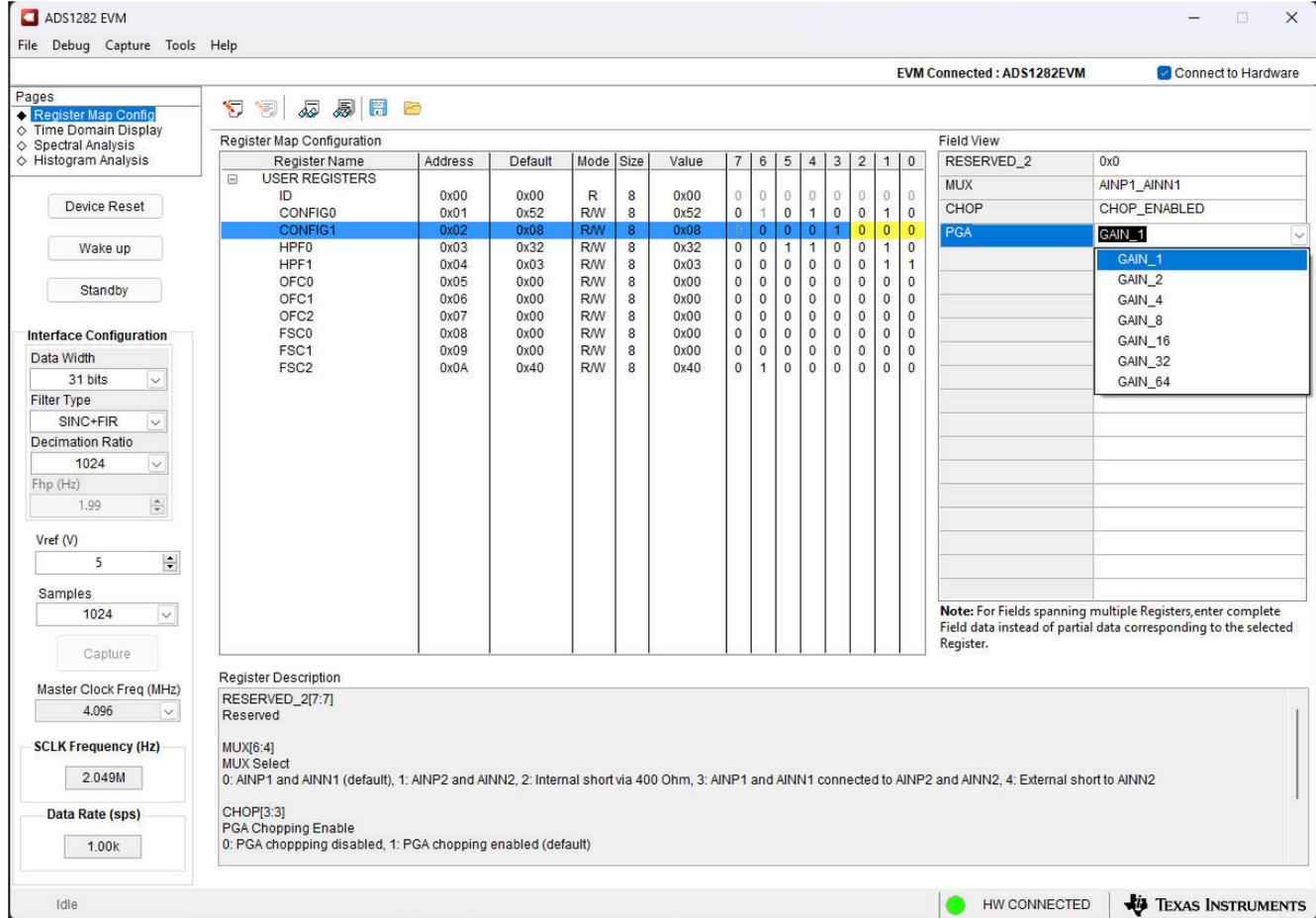
MUX[6:4]
MUX Select
0: AINP1 and AINN1 (default), 1: AINP2 and AINN2, 2: Internal short via 400 Ohm, 3: AINP1 and AINN1 connected to AINP2 and AINN2, 4: External short to AINN2

CHOP[3:3]
PGA Chopping Enable
0: PGA chopping disabled, 1: PGA chopping enabled (default)

Figure 4-4. Channel Selection

4.1.2.2 PGA Gain Selection

Figure 4-5 shows how the ADS1282 internal PGA gain can be configured within the PGA field of the CONFIG1 register. Gain options available are 1, 2, 4, 8, 16, 32, and 64. This setting is useful for providing dynamic range to small signals relative to the full-scale input range of the ADS1282.



The screenshot shows the ADS1282 EVM software interface. The main window displays the Register Map Configuration table, which lists various registers and their bit fields. The CONFIG1 register is highlighted, and its bit fields are shown in a grid. The PGA field is selected, and a dropdown menu is open, showing the available gain options: GAIN_1, GAIN_2, GAIN_4, GAIN_8, GAIN_16, GAIN_32, and GAIN_64. The GAIN_1 option is currently selected.

Register Name	Address	Default	Mode	Size	Value	7	6	5	4	3	2	1	0
USER REGISTERS													
ID	0x00	0x00	R	8	0x00	0	0	0	0	0	0	0	0
CONFIG0	0x01	0x52	R/W	8	0x52	0	1	0	1	0	0	1	0
CONFIG1	0x02	0x08	R/W	8	0x08	0	0	0	0	1	0	0	0
HPF0	0x03	0x32	R/W	8	0x32	0	0	1	1	0	0	1	0
HPF1	0x04	0x03	R/W	8	0x03	0	0	0	0	0	0	1	1
OFC0	0x05	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0
OFC1	0x06	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0
OFC2	0x07	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0
FSC0	0x08	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0
FSC1	0x09	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0
FSC2	0x0A	0x40	R/W	8	0x40	0	1	0	0	0	0	0	0

Field View

RESERVED_2	0x0
MUX	AINP1_AINN1
CHOP	CHOP_ENABLED
PGA	GAIN_1
	GAIN_1
	GAIN_2
	GAIN_4
	GAIN_8
	GAIN_16
	GAIN_32
	GAIN_64

Note: For Fields spanning multiple Registers, enter complete Field data instead of partial data corresponding to the selected Register.

Register Description

RESERVED_2[7:7]
Reserved

MUX[6:4]
MUX Select
0: AINP1 and AINN1 (default), 1: AINP2 and AINN2, 2: Internal short via 400 Ohm, 3: AINP1 and AINN1 connected to AINP2 and AINN2, 4: External short to AINN2

CHOP[3:3]
PGA Chopping Enable
0: PGA chopping disabled, 1: PGA chopping enabled (default)

Figure 4-5. PGA Gain Selection

4.1.2.3 Data Rate Configuration

Figure 4-6 shows how to select the data output rate of the ADS1282. The device supports data output speeds of up to 400 samples per second. Other options available are 250 SPS, 500 SPS, 1000 SPS, 2000 SPS, and 4000 SPS.

The screenshot shows the ADS1282 EVM software interface. The main window is titled "Register Map Configuration" and displays a table of registers. The "CONFIG0" register is selected, and its "DR" field is set to "4000 SPS". The interface also includes a "Field View" section on the right, which shows the bit fields of the selected register. The "DR" field is highlighted, and a dropdown menu is open, showing the available data rate options: 250 SPS, 500 SPS, 1000 SPS, 2000 SPS, and 4000 SPS. The "4000 SPS" option is selected.

Register Name	Address	Default	Mode	Size	Value	7	6	5	4	3	2	1	0
USER REGISTERS													
ID	0x00	0x00	R	8	0x00	0	0	0	0	0	0	0	0
CONFIG0	0x01	0x52	R/W	8	0x62	0	0	1	0	0	0	1	0
CONFIG1	0x02	0x08	R/W	8	0x08	0	0	0	0	1	0	0	0
HPF0	0x03	0x32	R/W	8	0x32	0	0	1	1	0	0	1	0
HPF1	0x04	0x03	R/W	8	0x03	0	0	0	0	0	0	1	1
OFC0	0x05	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0
OFC1	0x06	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0
OFC2	0x07	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0
FSC0	0x08	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0
FSC1	0x09	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0
FSC2	0x0A	0x40	R/W	8	0x40	0	1	0	0	0	0	0	0

Field View

SYNC	PULSE_SYNC
RESERVED_1	0x1
DR	4000 SPS
PHASE	250 SPS
FILTER	500 SPS
	1000 SPS
	2000 SPS
	4000 SPS

Note: For Fields spanning multiple Registers, enter complete Field data instead of partial data corresponding to the selected Register.

Register Description

SYNC[7:7]
Synchronization mode
0: Pulse SYNC mode (default), 1: Continuous SYNC mode

RESERVED_1[6:6]
Reserved

DR[5:3]
Data Rate Select
0: 250 SPS, 1: 500 SPS, 2: 1000 SPS (default), 3: 2000 SPS, 4: 4000 SPS

Figure 4-6. Data Rate Configuration

4.1.3 Time Domain Display

The time domain display tool allows visualization of the ADC response to a given input signal. Use this tool to study the behavior and debug any gross problems with the ADC or drive circuits. Trigger a capture of the data of the selected number of samples from the ADS1282EVM, as per the current interface mode settings indicated in Figure 4-7 by using the *Capture* button. The sample indices on the x-axis and the y-axis show the corresponding equivalent analog voltages based on the specified reference voltage. Switching pages to any of the analysis tools described in the subsequent sections causes calculations to be performed on the same set of data.

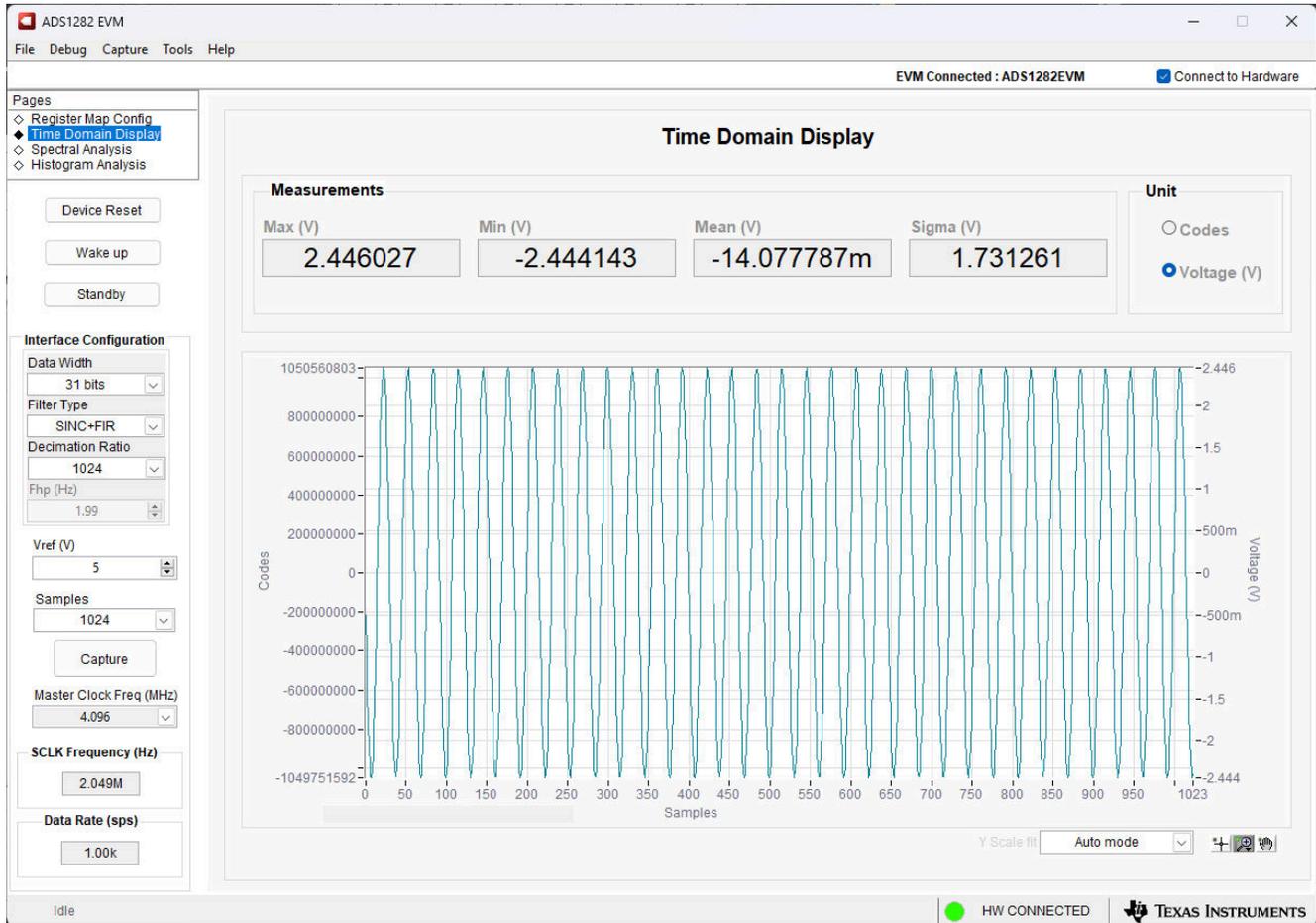


Figure 4-7. Time Domain Display

4.1.4 Spectral Analysis Display

The spectral analysis tool, shown in Figure 4-8, is intended to evaluate the dynamic performance (SNR, THD, THD+N, SFDR, and Dynamic Range) of the ADS1282 through single-tone sinusoidal signal FFT analysis using the 7-term Blackman-Harris window setting. The FFT tool includes windowing options that are required to mitigate the effects of non-coherent sampling (this discussion is beyond the scope of this document). The option to use no window is not recommended in evaluating the performance of the ADS1282.

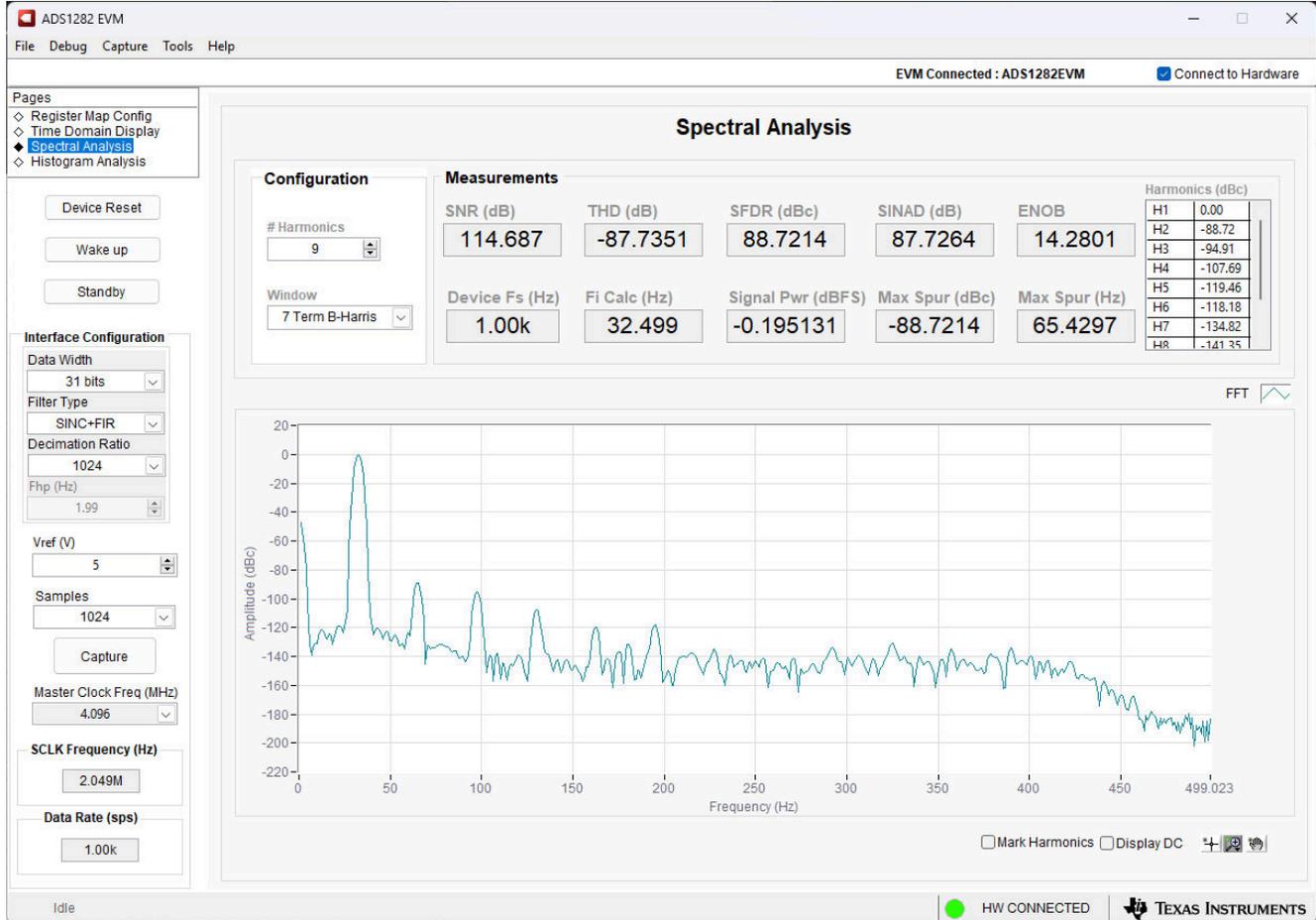


Figure 4-8. Frequency Domain Display

4.1.5 Histogram Analysis Display

Noise degrades ADC resolution and the histogram tool can be used to estimate effective resolution. The cumulative effect of noise coupled to the ADC output comes from sources such as the input drive circuits, reference drive circuit, ADC power supply, and the ADC. Cumulative noise is reflected in the standard deviation of the ADC output code histogram that is obtained by performing multiple conversions of a DC input applied to a given channel. Figure 4-9 shows the histogram corresponding to a DC input displayed by clicking the *Capture* button.

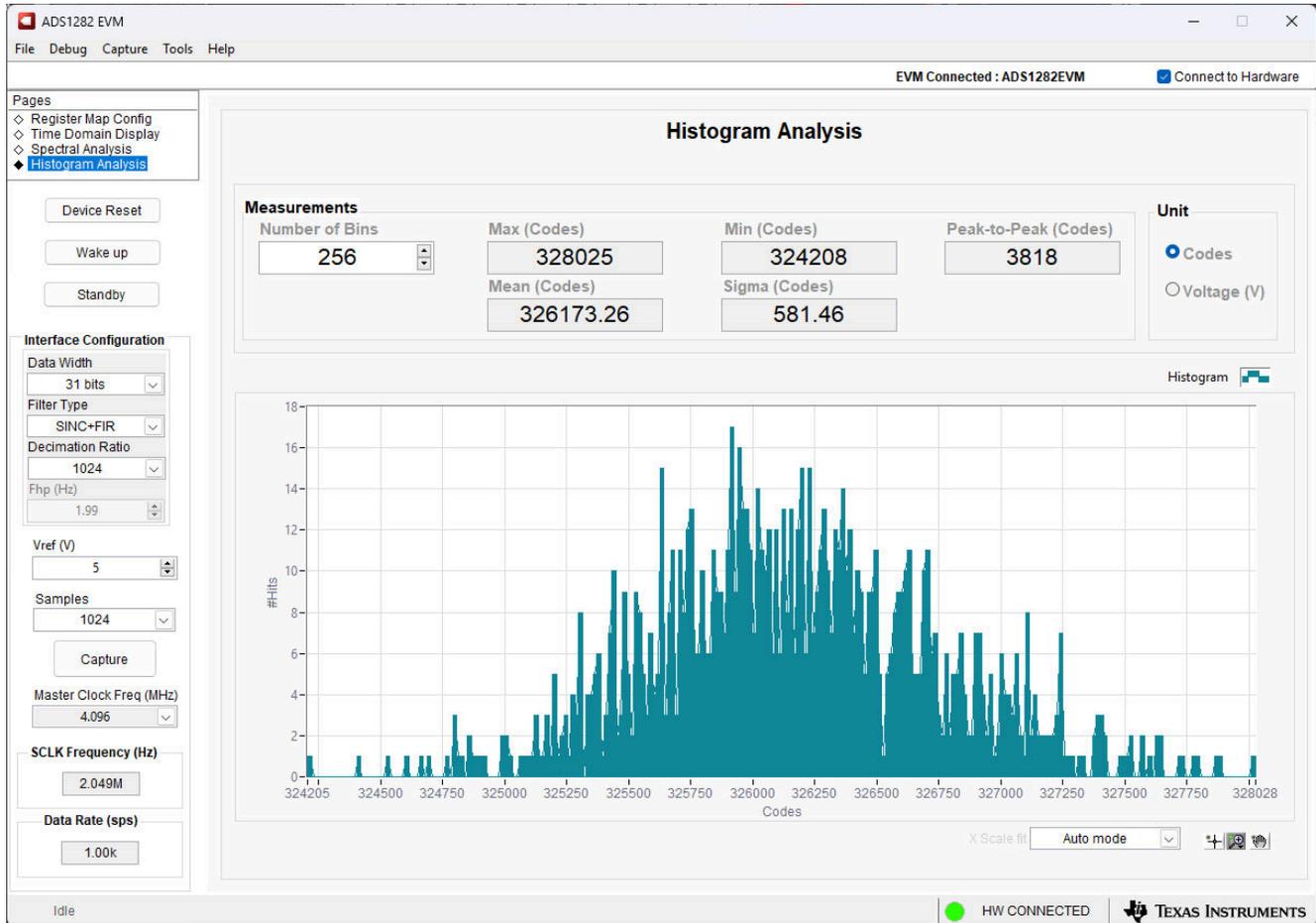


Figure 4-9. Histogram Display

5 Hardware Design Files

This section contains the ADS1282EVM schematics, PCB layouts, and bill of materials (BOM).

5.1 Schematics

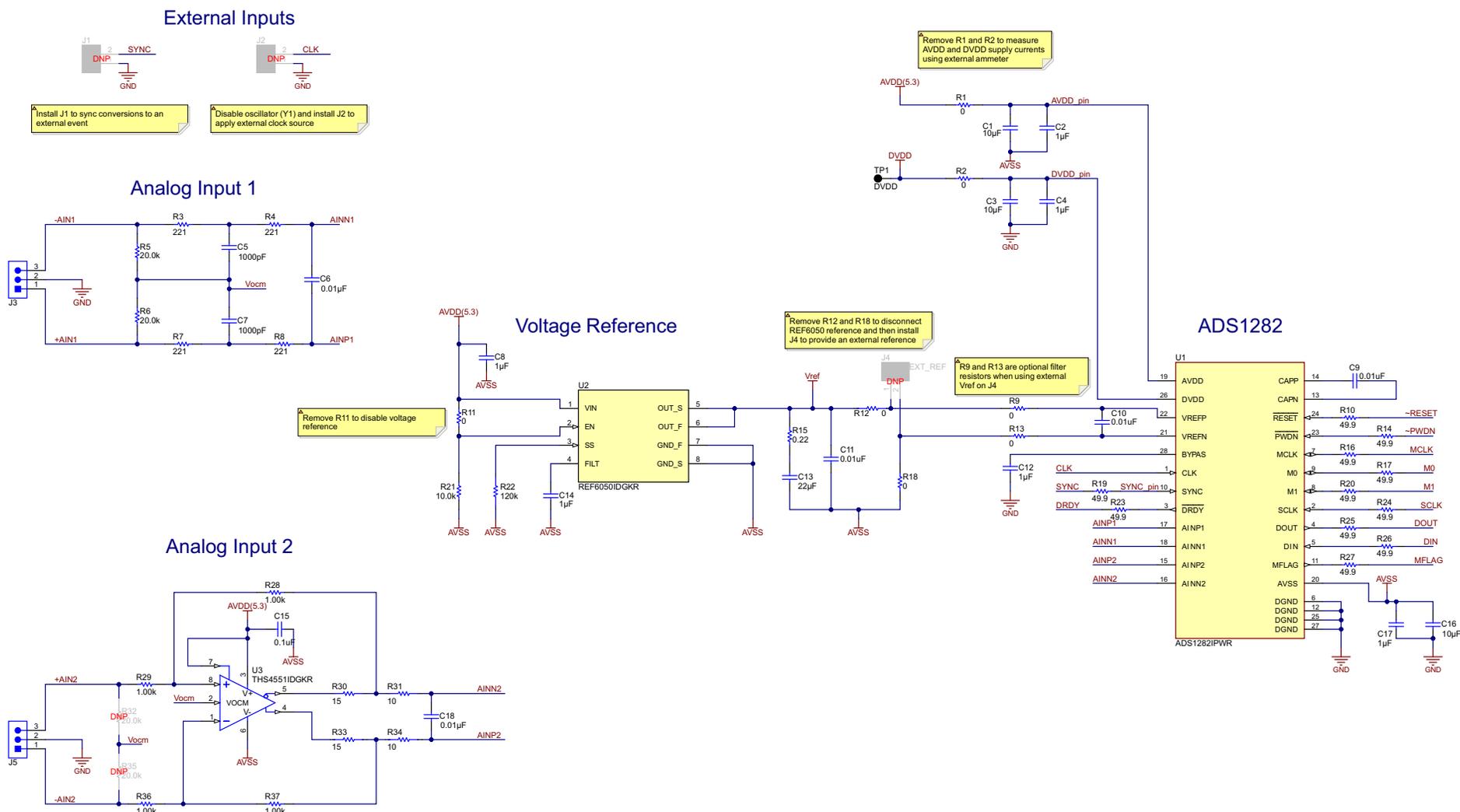
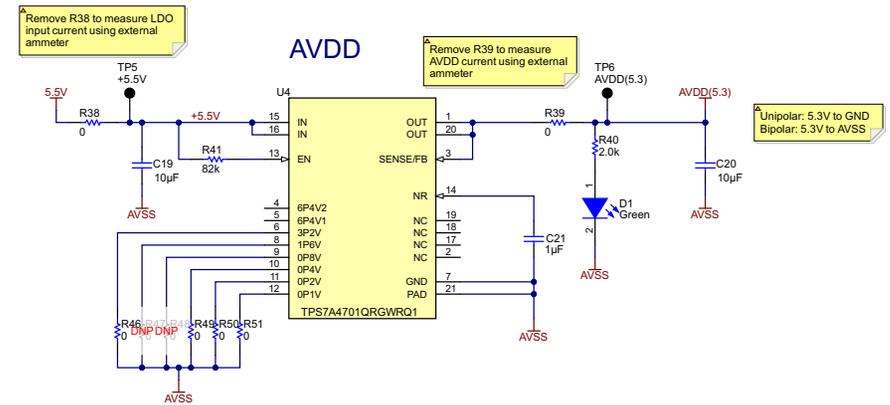
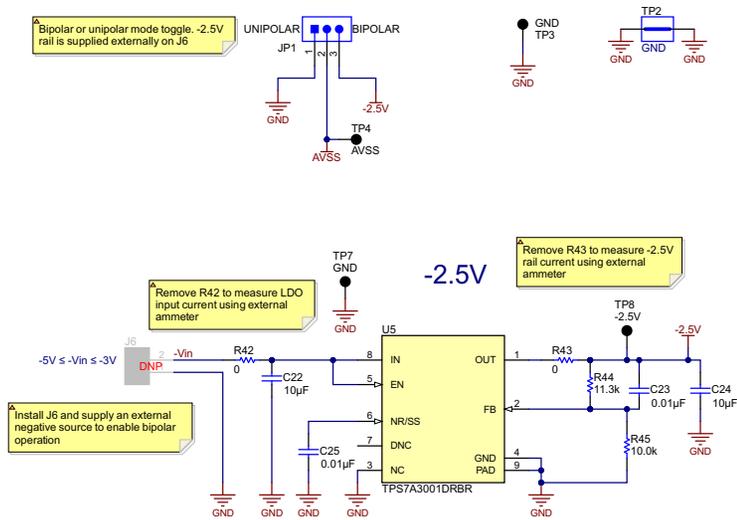
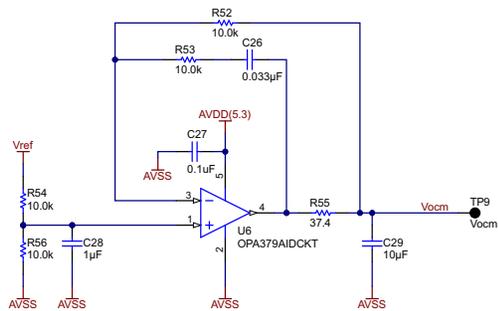


Figure 5-1. ADS1282EVM Analog Inputs & Reference Schematic

AVSS Select and Testpoints



Common Mode



Programmable LDO Configurations						
Vout (V)	3P2V	1P6V	0P8V	0P4V	0P2V	0P1V
2.5	-	-	INSTALLED	-	INSTALLED	INSTALLED
3.0	-	INSTALLED	-	-	-	-
3.3	-	INSTALLED	-	-	INSTALLED	INSTALLED
4.5	-	INSTALLED	INSTALLED	INSTALLED	INSTALLED	INSTALLED
5.0	INSTALLED	-	-	INSTALLED	-	-
5.3	INSTALLED	-	-	INSTALLED	INSTALLED	INSTALLED

INSTALLED = Solder 0-Ohm jumper to GND/AVSS
VOUT = 1.4V + Σ (all grounded pins)

Figure 5-2. ADS1282EVM Power Schematic

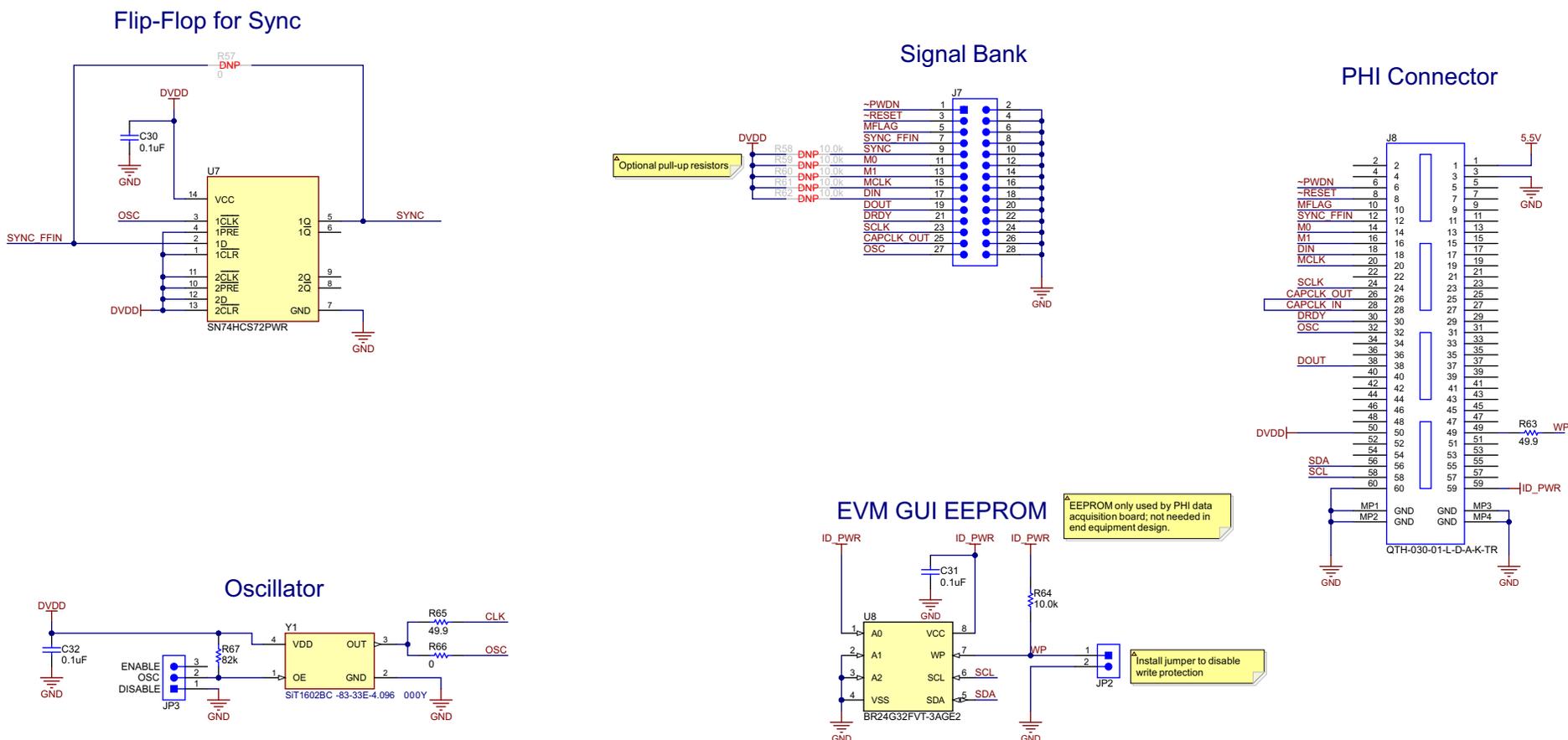


Figure 5-3. ADS1282EVM Digital Interface & Clocking Schematic

5.2 PCB Layouts

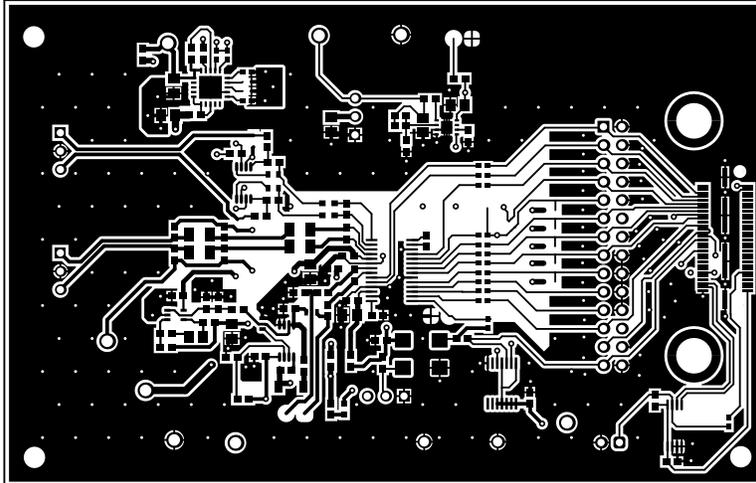


Figure 5-4. PCB Layout for the ADS1282EVM (Top Layer)

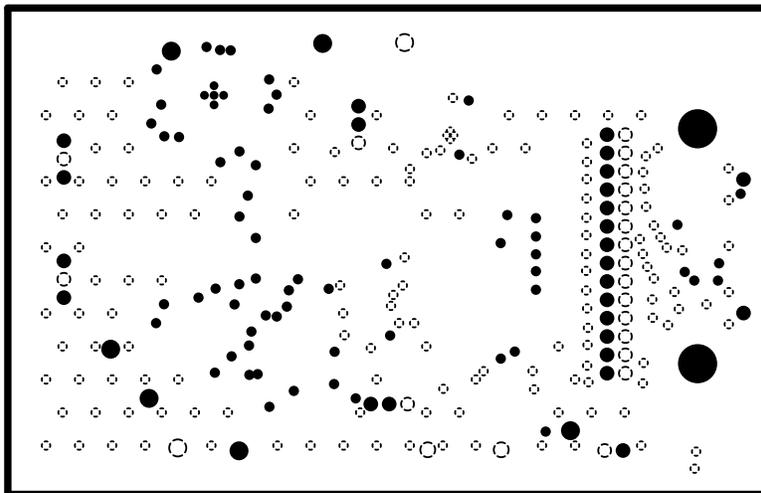


Figure 5-5. PCB Layout for the ADS1282EVM (Internal GND Plane)

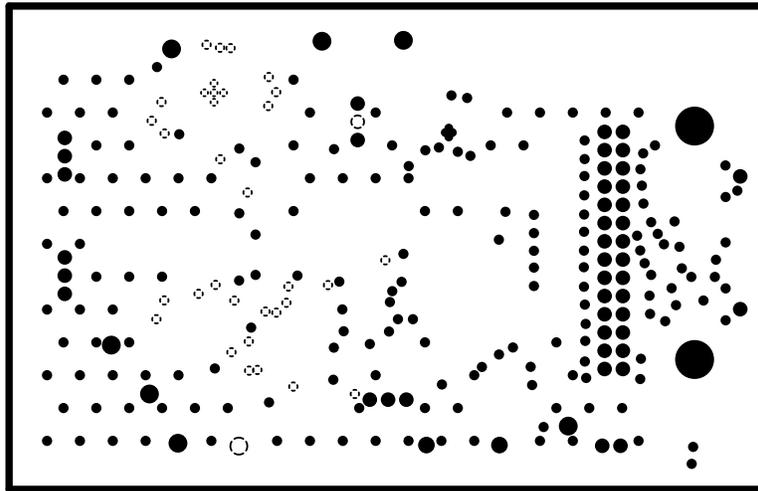


Figure 5-6. PCB Layout for the ADS1282EVM (Internal AVSS Plane)

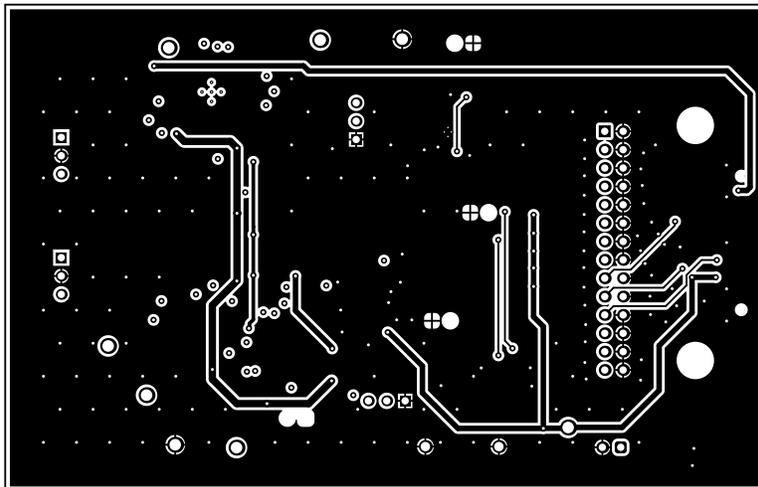


Figure 5-7. PCB Layout for the ADS1282EVM (Bottom Layer)

5.3 Bill of Materials (BOM)

Table 5-1. Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		ADS1282V2EVM	Any
C1, C3, C16, C19, C20, C22, C24	7	10uF	CAP, CERM, 10µF, 25V, +/- 10%, X5R, 0805	0805	CC0805KKX5R8BB106	Yageo
C2, C4, C8, C12, C14, C17, C21, C28	8		CAP, 1uF, 25V, ±10%, X7R, 0603	0603	CL10B105KA8NNNC	Samsung
C5, C7	2	1000pF	CAP, CERM, 1000pF, 50V, +/- 5%, C0G/NP0, 0603	0603	C0603C102J5GACTU	Kemet
C6, C18, C23, C25	4	0.01uF	CAP, CERM, 0.01µF, 25V, +/- 1%, C0G/NP0, 0603	0603	C0603C103F3GACTU	Kemet
C9, C10, C11	3	0.01uF	CAP, CERM, 0.01uF, 25V, +/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0603	0603	C0603C103J3GCAUTO	Kemet
C13	1	22uF	CAP, CERM, 22µF, 16V, +/- 20%, X5R, AEC-Q200 Grade 3, 1206	1206	CL31A226MOHNNNE	Samsung Electro-Mechanics
C15, C27, C30, C31, C32	5	0.1uF	CAP, CERM, 0.1uF, 25V, +/- 5%, X7R, 0603	0603	C0603C104J3RACTU	Kemet
C26	1	0.033uF	CAP, CERM, 0.033µF, 50V, +/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0805	0805	CGA4J2C0G1H333J125AA	TDK
C29	1	10uF	CAP, CERM, 10µF, 10V, +/- 10%, X7R, 0805	0805	GRM21BR71A106KA73L	MuRata
D1	1	Green	LED, Green, SMD	0603 LED	SM0603GCL	Bivar
H1, H2	2		Machine Screw Pan PHILLIPS M3		RM3X4MM 2701	APM HEXSEAL
H3, H4, H5, H6	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M
H7, H8	2		ROUND STANDOFF M3 STEEL 5MM	ROUND STANDOFF M3 STEEL 5MM	9774050360R	Wurth Elektronik
J3, J5, JP1, JP3	4		Header, 100mil, 3x1, Tin, TH	Header, 3 PIN, 100mil, Tin	PEC03SAAN	Sullins Connector Solutions
J7	1		Header, 100mil, 14x2, Gold, TH	14x2 Header	TSW-114-07-G-D	Samtec
J8	1		Header(Shrouded), 19.7mil, 30x2, Gold, SMT	Header (Shrouded), 19.7mil, 30x2, SMT	QTH-030-01-L-D-A-K-TR	Samtec
JP2	1		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec

Table 5-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
R1, R2, R9, R11, R13, R18, R38, R39, R42, R43, R66	11	0	RES, 0, 5%, 0.1 W, 0603	0603	RC0603JR-070RL	Yageo
R3, R4, R7, R8	4	221	RES, 221, 1%, 0.25 W, AEC-Q200 Grade 0, 1206	1206	CRCW1206221RFKEA	Vishay-Dale
R5, R6	2	20.0k	RES, 20.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0720KL	Yageo
R10, R14, R16, R17, R19, R20, R23, R24, R25, R26, R27, R63, R65	13	49.9	RES, 49.9, 1%, 0.063 W, 0402	0402	RC0402FR-0749R9L	Yageo America
R12	1	0	CRCW Thick Film Commodity Chip Resistor Jumper 0603 Size 0 Ohm 0.1 W 2-Pin SMD Paper T/R	0603	CRCW06030000Z0EBC	Vishay
R15	1	0.22	RES, 0.22, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3RQFR22V	Panasonic
R21, R45, R52, R53, R54, R56, R64	7	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0710KL	Yageo
R22	1	120k	Res Thick Film 0603 120K Ohm 1% 0.1W(1/10W) ±100ppm/C Pad SMD T/R	0603	CRCW0603120KFKEAC	Vishay Dale
R28, R29, R36, R37	4	1.00k	RES, 1.00 k, 1%, 0.1 W, 0603	0603	RC0603FR-071KL	Yageo
R30, R33	2	15	Res Thick Film 0603 15 Ohm 1% 0.1W(1/10W) ±100ppm/C Pad SMD Automotive T/R	0603	RMCF0603FT15R0	Stackpole
R31, R34	2	10	10 Ohms ±0.5% 0.1W, 1/10W Chip Resistor 0603 (1608 Metric) - Thin Film	0603	RT0603DRD0710RL	Yageo
R40	1	2.0k	RES, 2.0 k, 5%, 0.1 W, 0603	0603	RC0603JR-072KL	Yageo
R41, R67	2	82k	RES, 82 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060382K0JNEA	Vishay-Dale
R44	1	11.3k	RES, 11.3 k, 1%, 0.1 W, 0603	0603	RC0603FR-0711K3L	Yageo
R46, R49, R50, R51	4	0	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	RK73Z1ETTP	KOA Speer
R55	1	37.4	RES, 37.4, 1%, 0.1 W, 0603	0603	RC0603FR-0737R4L	Yageo
SH-J1, SH-J2	2	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec

Table 5-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
TP1, TP3, TP4, TP5, TP6, TP7, TP8, TP9	8		Test Point, Multipurpose, Black, TH	Black Multipurpose Test point	5011	Keystone Electronics
TP2	1		1mm Uninsulated Shorting Plug, 10.16mm spacing, TH	Shorting Plug, 10.16mm spacing, TH	D3082-05	Harwin
U1	1		Ultra-High-Resolution, 4kSPS, 2-Ch Delta-Sigma ADC With PGA for Seismic and Energy Exploration	TSSOP-28	ADS1282IPWR	Texas Instruments
U2	1		5ppm/C High-Precision Voltage Reference with Integrated High-Bandwidth Buffer, DGK0008A (VSSOP-8)	DGK0008A	REF6050IDGKR	Texas Instruments
U3	1		Low Noise, Precision, 150MHz, Fully Differential Amplifier, DGK0008A (VSSOP-8)	DGK0008A	THS4551IDGKR	Texas Instruments
U4	1		Automotive 35V, 1A, 4.2µVRMS, RF Low-Dropout (LDO) Voltage Regulator, RGW0020A (VQFN-20)	RGW0020A	TPS7A4701QRGWRQ1	Texas Instruments
U5	1		Vin -3V to -36V, -200mA, Ultra-Low-Noise, High-PSRR, Low-Dropout (LDO) Linear Regulator, DRB0008A (VSON-8)	DRB0008A	TPS7A3001DRBR	Texas Instruments
U6	1		2.9uA, 90kHz Rail-to-Rail I/O Operational Amplifier, 1.8V to 5.5V, -40 to 125 degC, 5-pin SOT23 (DCK5), Green (RoHS & no Sb/Br)	DCK0005A	OPA379AIDCKT	Texas Instruments
U7	1		Flip Flop 2 Element D-Type 2 Bit Negative Edge 14-TSSOP (0.173", 4.40mm Width)	TSSOP14	SN74HCS72PWR	Texas Instruments
U8	1		I2C BUS EEPROM (2-Wire), TSSOP-B8	TSSOP-8	BR24G32FVT-3AGE2	Rohm
Y1	1		4.096MHz XO (Standard) HCMOS, LVC MOS Oscillator 3.3V Enable/Disable 4-SMD, No Lead	SMD4	SiT1602BC-83-33E-4.096000Y	SiTime
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
J1, J2, J4, J6	0		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec
R32, R35	0	20.0k	RES, 20.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0720KL	Yageo
R47, R48	0	0	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	RK73Z1ETTP	KOA Speer

Table 5-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
R57	0	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
R58, R59, R60, R61, R62	0	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0710KL	Yageo

6 Additional Information

6.1 Trademarks

LabVIEW™ is a trademark of National Instruments.

Microsoft® and Windows® are registered trademarks of Microsoft Corporation.

All trademarks are the property of their respective owners.

7 Related Documentation

7.1 Supplemental Content

[Table 7-1](#) shows the related documentation from Texas Instruments.

Table 7-1. Related Documentation

Document	Literature Number
ADS1282 product data sheet	SBAS418
THS4551 product data sheet	SBOS778
REF6050 product data sheet	SBOS708
TPS7A30 product data sheet	SBVS125
OPA379 product data sheet	SBOS347
TPS7A4701 product data sheet	SBVS204
SN74HCS72 product data sheet	SCLS801

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1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an "EVM" or "EVMs") to the User ("User") in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.
 - 1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM ("Software") shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software
 - 1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.
2. *Limited Warranty and Related Remedies/Disclaimers:*
 - 2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.
 - 2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.
 - 2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI's recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI's recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI's instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGRADATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 Regulatory Notices:

3.1 United States

3.1.1 Notice applicable to EVMs not FCC-Approved:

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

3.3 Japan

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

<https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html>

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。技術適合証明を受けていないものご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。日本テキサス・イ

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西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。 <https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html>

3.4 European Union

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive):*

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

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- 4 *EVM Use Restrictions and Warnings:*
 - 4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.
 - 4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.
 - 4.3 *Safety-Related Warnings and Restrictions:*
 - 4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.
 - 4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.
 - 4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.
 5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.
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