Functional Safety Information

INA381-Q1 Functional Safety, FIT Rate, Failure Mode Distribution and Pin FMA

1 Overview

This document contains information for the INA381-Q1 (VSSOP-10 package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

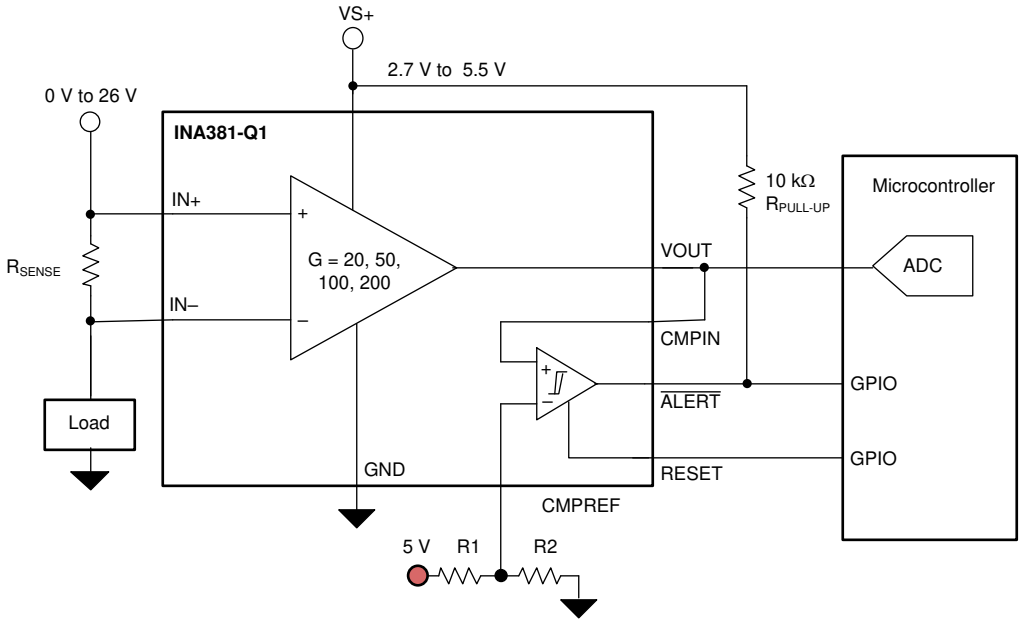

Figure 1-1. Functional Block Diagram

The INA381-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for the INA381-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	6
Die FIT Rate	2
Package FIT Rate	4

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 10 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	BICMOS Op Amp, Comparators, Voltage Monitors	8 FIT	45°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the INA381-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT open (Hi-Z)	15%
VOUT to GND	15%
VOUT to VS	15%
VOUT functional, not in specification	40%
ALERT false trip, failure to trip	15%

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the INA381-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to Supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the INA381-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the INA381-Q1 data sheet.

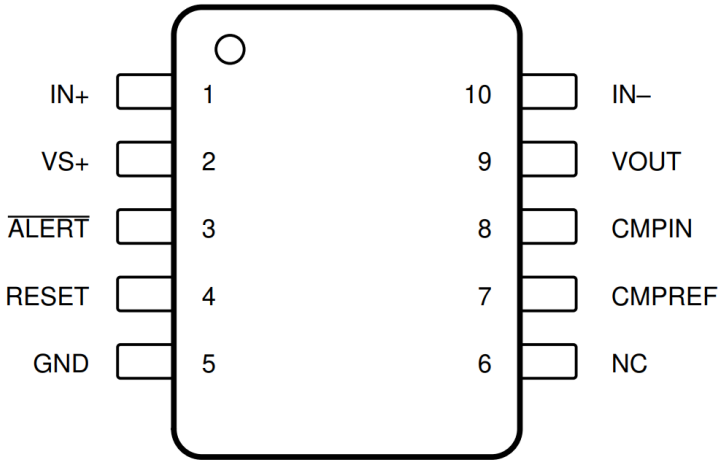

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- T_A = -40°C to +125°C
- V_S = 5 V
- V_{IN+} = 12 V
- CMPREF = 2 V.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN_+	1	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to ground. In low side configuration, input pins are shorted.	B
VS_+	2	Power supply shorted to ground	B
$\overline{\text{ALERT}}$	3	$\overline{\text{ALERT}}$ output is stuck low	B
RESET	4	If intended connection is not GND, functionality will be affected.	D if RESET=GND by design; B otherwise
GND	5	Normal Operation	D
NC	6	Normal Operation	D

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
CMPREF	7	$\overline{\text{ALERT}}$ output is stuck low	B
CMPIN	8	$\overline{\text{ALERT}}$ output is stuck high	B
VOUT	9	Output shorts to ground. When left in this configuration for a long time, under high supplies self heating could cause dice junction temperature to exceed 150 degrees Celsius.	B
IN_-	10	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to ground. In low side configuration, normal operation	B for High side or D for low side

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN_+	1	Differential input voltage is not well defined	B
VS_+	2	No power supply to device. Device may be biased through inputs. Output will be close to GND.	B
$\overline{\text{ALERT}}$	3	Pin can be left open if not needed	D if $\overline{\text{ALERT}}$=open by design; B otherwise
RESET	4	Comparator mode is not defined	B
GND	5	GND is floating. Output will be incorrect as it is no longer referenced to GND.	B
NC	6	Normal Operation	D
CMPREF	7	Comparator threshold is not defined.	B
CMPIN	8	Comparator input is not defined	B
VOUT	9	Output can be left open, there is no effect on the IC.	B
IN_-	10	Differential input voltage is not well defined.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
IN_+	1	VS_+	In high-side configuration, a short from the bus supply to VS will occur. High current will flow from bus supply to VS or vice versa. Device could be damaged.	A for High side or B for low side
VS_+	2	$\overline{\text{ALERT}}$	$\overline{\text{ALERT}}$ is stuck high or unpredictable.	B
$\overline{\text{ALERT}}$	3	RESET	$\overline{\text{ALERT}}$ is unpredictable.	B
RESET	4	GND	If intended connection is not GND, functionality will be affected.	D if RESET=GND by design; B otherwise
GND	5	NC	Normal Operation.	D
NC	6	CMPREF	Normal Operation.	D
CMPREF	7	CMPIN	Comparator input pins are shorted.	B
CMPIN	8	VOUT	Normal Operation.	D
VOUT	9	IN_-	In high-side configuration, a short from the bus supply to VOUT will occur. Device could be damaged . In low side configuration, power supply is shorted to GND.	A for High side or B for low side
IN_-	10	IN_+	Input differential voltage=0V.	C

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN_+	1	In high-side configuration, a short from the bus supply to VS will occur. High current will flow from bus supply to VS or vice versa. Device could be damaged.	A for High side or B for low side
VS_+	2	Normal operation	D
$\overline{\text{ALERT}}$	3	$\overline{\text{ALERT}}$ is stuck high or unpredictable.	B
RESET	4	If intended connection is not VS, functionality will be affected.	D if RESET=VS by design; B otherwise
GND	5	Power supply shorted to GND	B
NC	6	Normal operation	D
CMPREF	7	$\overline{\text{ALERT}}$ is stuck high.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
CMPIN	8	$\overline{\text{ALERT}}$ is stuck low.	B
VOUT	9	Output shorts to supply. When left in this configuration for a long time, under high supplies self heating could cause dice junction temperature to exceed 150 degrees Celsius.	B
IN_	10	In high-side configuration, a short from the bus supply to VS will occur. High current will flow from bus supply to VS or vice versa. Device could be damaged.	A for High side or B for low side

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2020) to Revision A (September 2020) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1
- Added *Pin Failure Mode Analysis (Pin FMA)* section..... 4

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