User's Guide

TPS7A21EVM-059 Evaluation Module

ABSTRACT

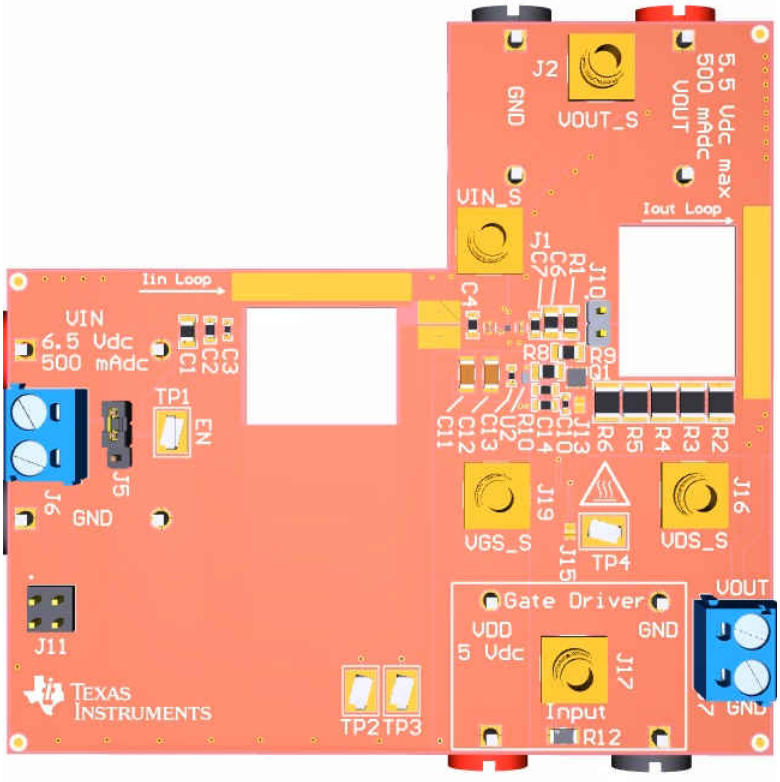

Figure 1-1. TPS7A21EVM-059 Evaluation Module

This user's guide describes the operational use of the TPS7A21EVM-059 evaluation module (EVM) as a reference design for engineering demonstration and evaluation of the TPS7A21 low-dropout linear regulator (LDO). Included in this user's guide are setup and operating instructions, thermal and layout guidelines, a printed-circuit board (PCB) layout, a schematic diagram, and a bill of materials (BOM).

Throughout this document, the terms *evaluation board*, *evaluation module*, and *EVM* are synonymous with the TPS7A21EVM-059.

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1 Trademarks

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2 Introduction

The Texas Instruments TPS7A21EVM-059 evaluation module (EVM) helps designers evaluate the operation and performance of the TPS7A21 LDO voltage regulator. As shown in Table 2-1, the TPS7A21EVM-059 contains one TPS7A21 LDO voltage regulator in the DSBGA package. An optional load transient circuit is also included to assist the user with high-speed load transient testing. An input current loop is included that allows fast measurements of the input current.

Table 2-1. Device Information

EVM ORDERABLE NUMBER	V_{OUT}	PART NAME	PACKAGE
TPS7A21EVM-059	3.3 V	TPS7A2133PYWDJ	4-pin DSBGA

3 Setup

This section describes the jumpers and connectors on the EVM, and how to properly connect, set up, and use the TPS7A21EVM-059. Section 3.1 and Section 3.3 describe the test setup and operation for the TPS7A21 LDO. Section 3.2 and Section 3.4 describe the test setup and operation of the optional load transient circuit.

3.1 LDO Input/Output Connector Descriptions

3.1.1 VIN and GND

VIN and GND are the connection terminals for the input supply. The VIN terminal is the positive connection, and the GND terminal is the negative (that is, ground) connection.

3.1.2 VOUT and GND

VOUT and GND are the connection terminals for the output load. The VOUT terminal is the positive connection, and the GND terminal is the negative (that is, ground) connection.

3.1.3 EN

EN is a 3-pin header used to enable or disable the TPS7A21.

The center pin of the 3-pin header is tied to the TPS7A21 EN input. When the 2-pin shunt is placed across the top two pins of the header, VIN is shorted to EN, and the TPS7A21 is enabled. When the 2-pin shunt is placed across the bottom two pins of the header, GND is shorted to EN, and the TPS7A21 is disabled. Alternatively, the 3-pin header can remain floating. The TPS7A21 includes an internal smart enable pulldown resistor, which ties the EN pin to GND through an internal 500-kΩ resistor. If the 3-pin header is floating, the TPS7A21 remains disabled.

When driving the EN terminal with an off-board supply or signal generator, the applied voltage must be kept between 0 V and 6.5 V.

3.2 Optional Load Transient Input/Output Connector Descriptions

3.2.1 VDD and GND

VDD and GND are the connection terminals for the input supply of the load transient circuit. The VDD terminal is the positive connection, and the GND terminal is the negative (that is, ground) connection.

3.2.2 J10

J10 is an optional connection for the user to make measurements or apply loads to the output of the LDO.

3.2.3 J12

J12 is an optional connection to insert a damping circuit across the load transient MOSFET drain to source voltage.

3.2.4 J13

J13 is an optional connection to insert capacitance or additional load across the drain to source of the load transient MOSFET.

3.2.5 J16

J16 is a high-frequency kelvin connection that allows accurate measurements of the load transient MOSFET drain to source voltage.

3.2.6 J17

J17 is the connection for the function generator to drive the gate driver device. J17 is terminated by the 50-Ω resistor, R12.

3.2.7 J19

J19 is a high-frequency kelvin connection that allows accurate measurements of the load transient MOSFET gate to source voltage.

3.2.8 TP2 and TP3

TP2 and TP3 allow the user to measure the gate drive resistance R8 when power is turned off to the EVM.

3.2.9 TP4

TP4 is the enable pin to enable the gate driver device. Tie this pin to GND to enable the gate driver.

3.3 TPS7A21 LDO Operation

The TPS7A21EVM-059 evaluation module contains the TPS7A21 LDO with input and output capacitors installed. These three components provide the minimum required solution size, as illustrated by the white boxes in Figure 1-1. Additional pads are available to test the LDO with additional input and output capacitors beyond what is already installed on the EVM. The TPS7A21 LDO can be enabled or disabled by using the J5 3-pin header.

1. Place a 2-pin shunt across the header to tie VIN to EN to enable the device.
2. Place a 2-pin shunt across the header to tie GND to EN, or leave the 3-pin header floating to disable the device.

Alternatively, by connecting an external function generator to TP1 (EN) and a nearby GND post (J6), the user can enable or disable the TPS7A21 LDO after VIN is applied. Figure 3-1 shows the result of the TPS7A21EVM-059 during turn on. The blue trace is the enable voltage, and the red trace is the output voltage.

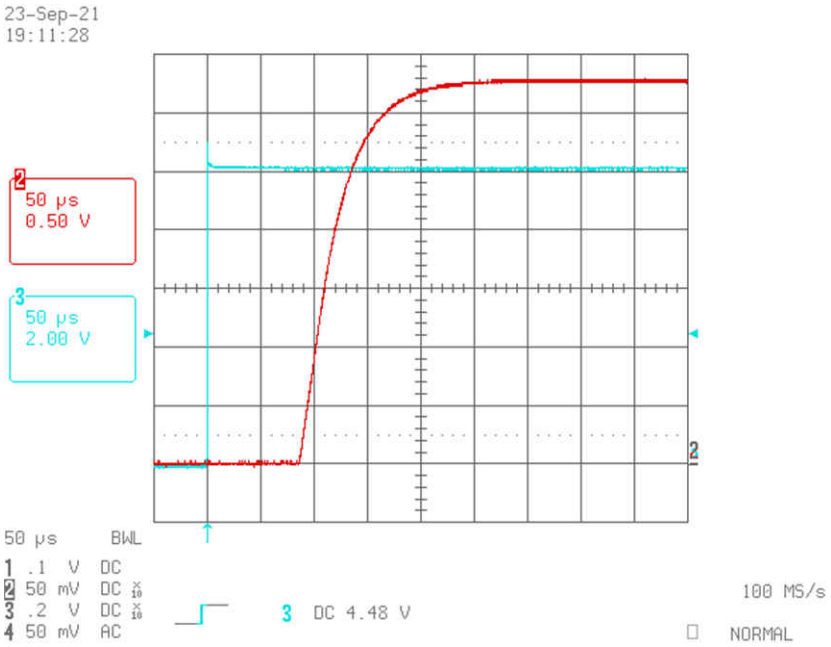

Figure 3-1. TPS7A21EVM-059 Turn On

If desired, a current probe can be inserted in the EVM as shown in Figure 3-2 to measure the input and output current. The slots were sized to fit most current probes, such as the LeCroy™ AP015 or CP031 current probes.

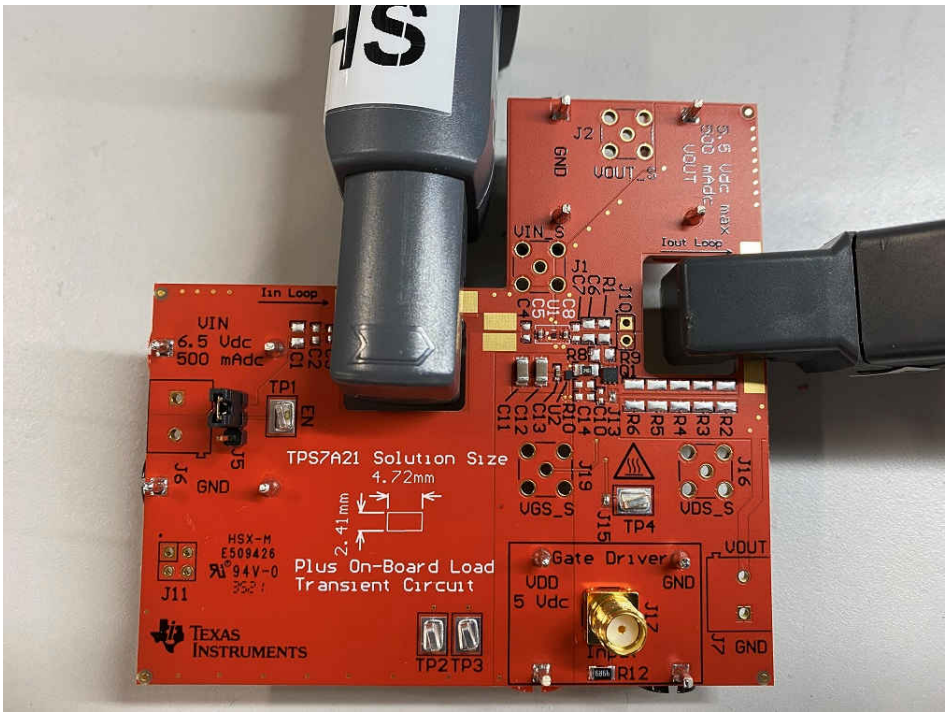

Figure 3-2. TPS7A21EVM-059 With Current Probes Attached

The user has two options for providing a DC load on the output of the TPS7A21. J7 can be used to place a DC load that flows through the current sense path on the output of the LDO. Alternatively, the J4 (VOUT) and J9 (GND) banana connectors can be used for external measurements and loading; however, the IOUT loop does not sense current flowing through these connectors. In cases where very fast transient tests are performed, ringing may be observed on VIN or VOUT as a result of the parasitic inductance within the PCB of the EVM. A strip of wire placed on the exposed copper in the current path can reduce this ringing. Select the correct size of additional wire to fill the volume of the current probe. For most current probes, a 10 AWG wire can be used.

WARNING

The sensors of some current probes are tied to GND and cannot come into contact with energized conductors. See the user manual of your current probe for details. If your current probe has this limitation, use a thin strip of electrical or Kapton® tape to isolate the current sense path from the current probe.

Optional kelvin sense points are provided using the SMA connectors J1 (VIN) and J2 (VOUT).

3.4 Optional Load Transient Circuit Operation

The TPS7A21EVM-059 evaluation module contains an optional high-performance load transient circuit to allow efficient testing of the TPS7A21 LDO load transient performance. To use the optional load transient circuit, install the correct components in accordance with the application. Modify the input and output capacitance connected to the TPS7A21 LDO to match the expected operating conditions. Determine the desired peak current to test, and modify the parallel resistor combination of R2, R3, R4, R5, and R6 as shown:

$$I_{Peak} = \frac{V_{OUT}}{R_2 \| R_3 \| R_4 \| R_5 \| R_6} \quad (1)$$

The slew rate of the load step can be adjusted by C9, R7, and R8. In this section, only R8 is adjusted to set the slew rate. For a 0-mA to 500-mA load step, use Table 3-1 to select a value of R8 that results in the desired rise or fall time.

Table 3-1. Suggested Ramp Rate Resistor Values

R8	Rise Time	Fall Time
54.9 kΩ	6 µs	10 µs
27.4 kΩ	3 µs	5 µs
13.6 kΩ	1.5 µs	2.8 µs
6.81 kΩ	750 ns	1.5 µs
3.4 kΩ	500 ns	750 ns
1.69 kΩ	200 ns	500 ns
845 Ω	100 ns	200 ns
422 Ω	50 ns	100 ns
210 Ω	30 ns	50 ns
105 Ω	20 ns	30 ns

After the EVM is modified (if needed), connect a power supply to banana connectors J14 (VDD) and J18 (GND) with a 5-V DC supply and a 1-A DC current limit. As shown in Figure 3-3, the TPS7A21 transient response is very fast and the output voltage recovers in well under 1 ms after the initial load transient. Therefore, use a load transient pulse duration limit of 1 ms to prevent excessive heating of the pulsed resistors (R2, R3, R4, R5, and R6). Configure a function generator for the 50-Ω output, in a 0-V DC to 5-V DC square pulse. If necessary, burst mode can be configured in the function generator for repetitive, low duty cycle, load transient testing.

A 3.4-kΩ resistor is installed on the EVM at R8. This resistor provides approximately 1 A/µs slew rate from 0 mA to 500 mA. Figure 3-3 provides example test data with R8 = 3.4 kΩ. The red trace is the output voltage and the blue trace is the output current. J7 provides 1 mA of DC load current and R2, R3, R4, R5, and R6 provide 499 mA of pulsed load. The resulting test data shows a 1-mA to 500-mA load step on VOUT of the LDO, with only a 1-µF capacitor on the output of the LDO.

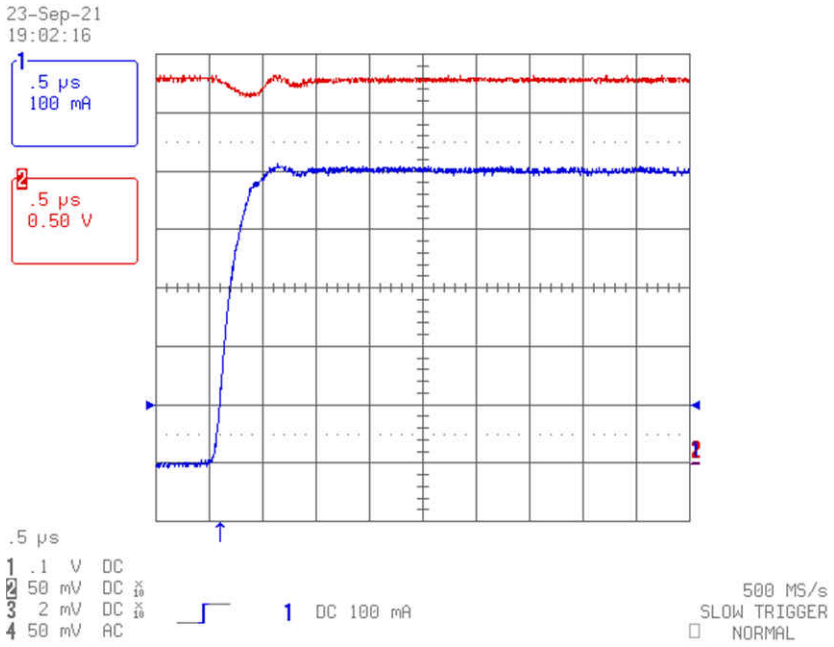

Figure 3-3. TPS7A21EVM-059 Load Transient Results

4 Board Layout

Figure 4-1 through Figure 4-6 show the board layout for the TPS7A21EVM-059 PCB.

The TPS7A21EVM-059 dissipates power, which may cause some components to experience an increase in temperature. The TPS7A21 LDO, LMG1020YFFR gate driver, and pulsed resistors R2, R3, R4, R5, and R6 are most at risk of raising to a high junction temperature during normal operation.

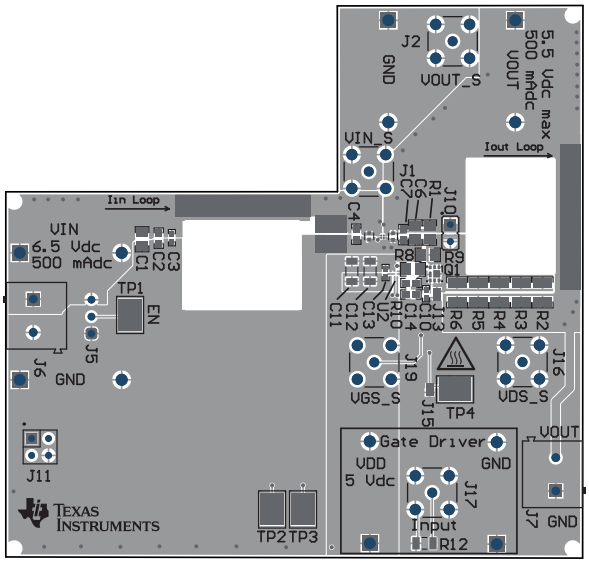

Figure 4-1. Top Assembly Layer and Silk Screen

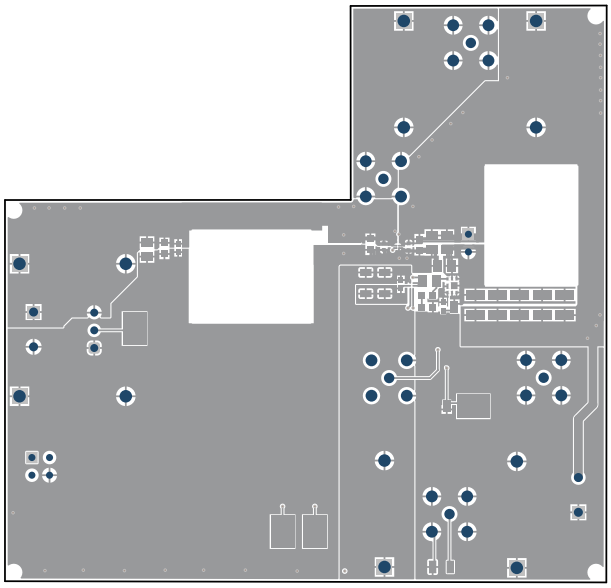

Figure 4-2. Top Layer Routing

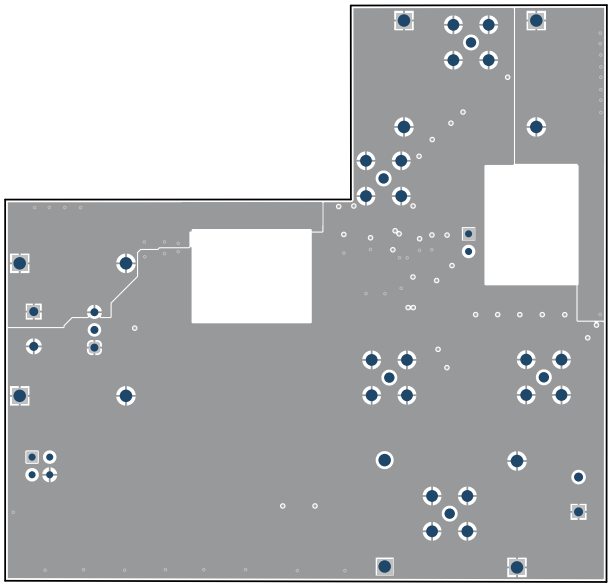

Figure 4-3. Layer 2

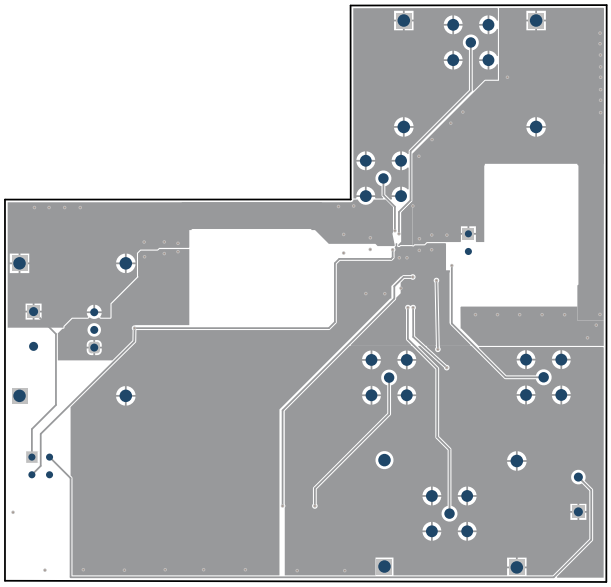

Figure 4-4. Layer 3

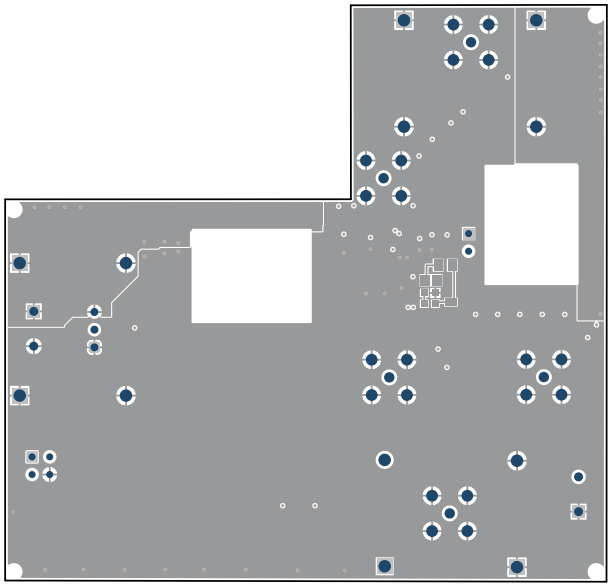

Figure 4-5. Bottom Layer Routing

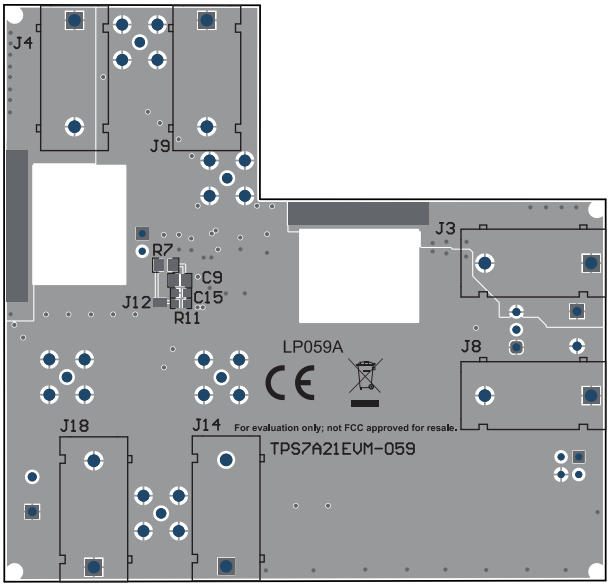

Figure 4-6. Bottom Assembly Layer and Silk Screen

5 TPS7A21 EVM Schematic

Figure 5-1 shows a schematic for the TPS7A21EVM-059.

Revision History				
Rev	ECN #	Approved Date	Approved by	Notes
N/A	N/A	N/A	N/A	N/A

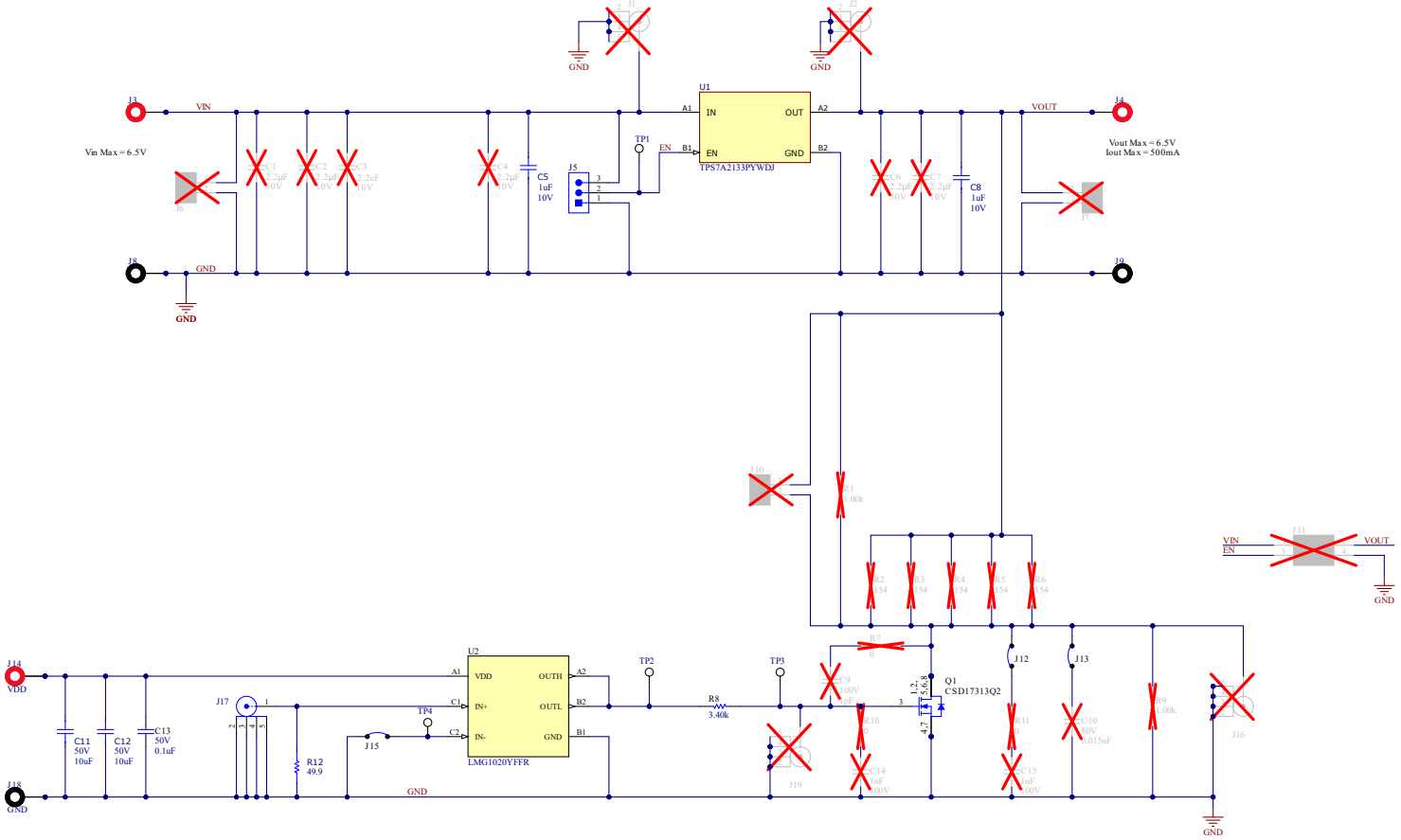

Figure 5-1. Schematic

6 Bill of Materials

Table 6-1 shows the bill of materials for the TPS7A21EVM-059.

Table 6-1. Bill of Materials

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
!PCB1	1		Printed Circuit Board		LP059	Any		
C5, C8	2	1µF	1µF ±10% 10V Ceramic Capacitor X7R 0402 (1005 Metric)	402	GMC04X7R105K10NT	Cal-Chip Electronics		
C11, C12	2	10µF	10 µF ±10% 50V Ceramic Capacitor X7R 1206 (3216 Metric)	1206	GMC31X7R106K50NT	Cal-Chip Electronics		
C13	1	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0402	402	C1005X7R1H104K050BB	TDK		
FID1, FID2, FID3, FID4, FID8	5		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A		
J3, J4, J14	3		Standard Banana Jack, insulated, 10A, red	571-0500	571-0500	DEM Manufacturing		
J5	1		Header, 2.54 mm, 3x1, Gold, TH	Header, 2.54mm, 3x1, TH	61300311121	Wurth Elektronik		
J8, J9, J18	3		Standard Banana Jack, insulated, 10A, black	571-0100	571-0100	DEM Manufacturing		
J12, J13, J15	3		Jumper, SMT	shorting jumper, SMT	JMP-36-30X40SMT	Any		
J17	1		SMA Straight Jack, Gold, 50 Ohm, TH	SMA Straight Jack, TH	901-144-8RFX	Amphenol RF		
Q1	1	30V	MOSFET, N-CH, 30 V, 5 A, DQK0006C (WSON-6)	DQK0006C	CSD17313Q2	Texas Instruments		None
R8	1	3.40k	RES, 3.40 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	805	ERJ-6ENF3401V	Panasonic		
R12	1	49.9	RES Thick Film, 49.9Ω, 1%, 0.75W, 100ppm/°C, 1206	1206	CRCW120649R9FKEAHP	Vishay Dale		
SH-J1	1	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec	969102-0000-DA	3M
TP1, TP2, TP3, TP4	4		Test Point, Compact, SMT	Testpoint_Keystone_Compact	5016	Keystone		
U1	1		500-mA, Ultra-Low-Noise, Low-IQ High-PSRR LDO	PowerWCSP4	TPS7A2133PYWDJ	Texas Instruments		
U2	1		5V, 7A/5A Low Side GaN Driver With 60MHz/1ns Speed, YFF0006AEAE (DSBGA-6)	YFF0006AEAE	LMG1020YFFR	Texas Instruments	LMG1020YFFT	Texas Instruments
C1, C6	0	2.2uF	CAP, CERM, 2.2 uF, 50 V, +/- 20%, X7R, 0805	805	C2012X7R1H225M125AC	TDK		
C2, C4, C7	0	2.2uF	CAP, CERM, 2.2 uF, 10 V, +/- 10%, X7R, 0603	603	C1608X7R1A225K080AC	TDK		
C3	0	2.2uF	CAP, CERM, 2.2 uF, 10 V, +/- 10%, X7S, 0402	402	C1005X7S1A225K050BC	TDK		

Table 6-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
C9	0	1pF	CAP, CERM, 1 pF, 100 V, +/- 5%, C0G/NP0, 0805	805	GQM2195C2A1R0CB01D	MuRata		
C10	0	0.015uF	CAP, CERM, 0.015 uF, 50 V, +/- 10%, X7R, 0402	402	GRM155R71H153KA12D	MuRata		
C14, C15	0	1000pF	CAP, CERM, 1000 pF, 100 V, +/- 5%, X7R, 0603	603	06031C102JAT2A	AVX		
FID5, FID6, FID7	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A		
J1, J2, J16, J19	0		SMA Straight Jack, Gold, 50 Ohm, TH	SMA Straight Jack, TH	901-144-8RFX	Amphenol RF		
J6, J7	0		Terminal Block, 5 mm, 2x1, Tin, TH	Terminal Block, 5 mm, 2x1, TH	691 101 710 002	Wurth Elektronik		
J10	0		Header, 100mil, 2x1, Gold, TH	Sullins 100mil, 1x2, 230 mil above insulator	PBC02SAAN	Sullins Connector Solutions		
J11	0		Header, 100mil, 2x2, Gold, TH	2x2 Header	TSW-102-07-G-D	Samtec		
R1, R9	0	1.00k	RES, 1.00 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	805	ERJ-6ENF1001V	Panasonic		
R2, R3, R4, R5, R6	0	154	RES, 154, 1%, 0.5 W, 1210	1210	RC1210FR-07154RL	Yageo		
R7	0	0	RES, 0, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	805	ERJ-6GEY0R00V	Panasonic		
R10, R11	0	0	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	603	RMCF0603ZT0R00	Stackpole Electronics Inc		

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