Application Report
SCAA057 – August 2002

PCB Layout Guidelines for CDCLVP110

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ABSTRACT

This application note describes various electrical and thermal performance considerations for TI's CDCLVP110. In addition, it provides recommendations for PCB layout as well as optimizing power consumption in a real system application. Finally, it shows examples of how to estimate the worst case chip temperature.

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1 Introduction

As clock and data transmission approaches the gigabit range, modern processes and small geometries are needed to fulfill such requirements. The CDCLVP110 is built in the SiGe process. Small feature sizes result in a small die size. As the die area gets smaller the thermal resistance from junction to the ambient increases. Optimizing the PCB layout provides the high-frequency performance required for 3.5-GHz operation and also helps to sink heat from the chip to the ambient.

2 Optimizing the PCB Layout for the CDVLP110

2.1 PCB Layout Considerations for Electrical Performance

Generally, an RF-type PCB layout is required in high-speed systems with clock speeds up to 3.5 GHz and typical rise and fall times of 150 ps. Impedance matching over 50-Ω transmission lines is best achieved using ground planes. Also, a V_{CC} plane is recommended for a low-impedance power supply connection. This can be realized as a split plane, having the device power supply (V_{CC}) and the termination voltage (V_{CC} - 2 V) wired in one layer. The best clock signal integrity and fast transition times can be achieved by using high frequency laminates in the signal layers. The termination resistors for the CLK0/CLK0z (CLK1/CLK1z) input pairs should be placed as close as possible to the CDCLVP110 device leads. The Qn/Qnz outputs are best terminated at the end of the 50-Ω transmission lines, which are close to the input pins of the receiver, driven by the LVP110. Figure 1 shows one routing example for CLK0, CLK0z, and one example for Q4, Q4z. To avoid impedance discontinuity, vias should not be placed in the clock signal lines and the high-speed signal routing should be done on the component side (top or bottom layer). This is different from standard PCB layout recommendations of having high-speed signal wires in the inner layers or embedded between two ground layers for EMI reduction. However, the differential signaling here cancels out this effect. A combination of 100-nF (C2 and C4 in Figure 1) decoupling capacitors and low-inductance multilayer ceramic chip capacitors of 100 pF (C1, C3, and C5 in Figure 1) with class 1 dielectric type (like NPO or COG) are recommended.

2.2 PCB Layout Considerations for Thermal Performance

TI's CDCLVP110 devices were characterized from –40°C to 85°C. This device passed the operating live test at 155°C ambient temperature (chip temperature about 180°C) and at 240h with no failures. Assuming a typical application ambient temperature of 55°C and applying the Arrhenius equation would result in a theoretical acceleration factor of 325. This is as if the device were continuously powered for 78,000 hrs (calculated with 0.7eV activation energy). For reliability reasons, it is recommended to keep the chip temperature as low as possible. As a rule of thumb, the average chip temperature over the lifetime should not exceed 110°C.

The junction to ambient thermal resistance (θ_{JA}) worst case values in the *package thermal impedance* table of the CDCLVP110 data sheet, literature number SCAS681 were generated by modeling with a JESD51-7 high K board, two signal and two plane layers (2s2p). These values can only be used for rough estimates of the chip temperature. Since the external resistances of the surrounding air, PCB etc. are in series with the package resistance, factors external to the package affect the junction temperature significantly. The JESD51-7 is an agreed standard for PCB layout to compare different package types. The thermal resistance in the application may be similar but it can differ. Figure 1 shows a PCB layout example optimized to give best electrical and thermal performance. The thermal resistance of the lead frame (copper) is significantly lower than that of the plastic. The five leads specified for V_{CC} connection have the additional advantage of transferring heat away from the chip. With the help of thermal vias in the PCB, heat is drawn from the device through the power and ground planes through special edge connectors and dissipated into the ambient surroundings. Using 0,3 mm Ø vias to connect to V_{CC}, ground (V_{EE}), and Vterm gives connections with both low impedance and low thermal resistance. In addition, the traces on the top and bottom layers can be used for heat transfer if they are exposed (not covered by the solder mask). If required, the copper area beneath the device can be exposed and the use of thermal grease could further reduce the θ_{JA}. This might be an alternative in systems where the use of a fan is not possible. In systems where airflow is readily available, not only θ_{JA} is reduced but the ambient temperature is also lowered.

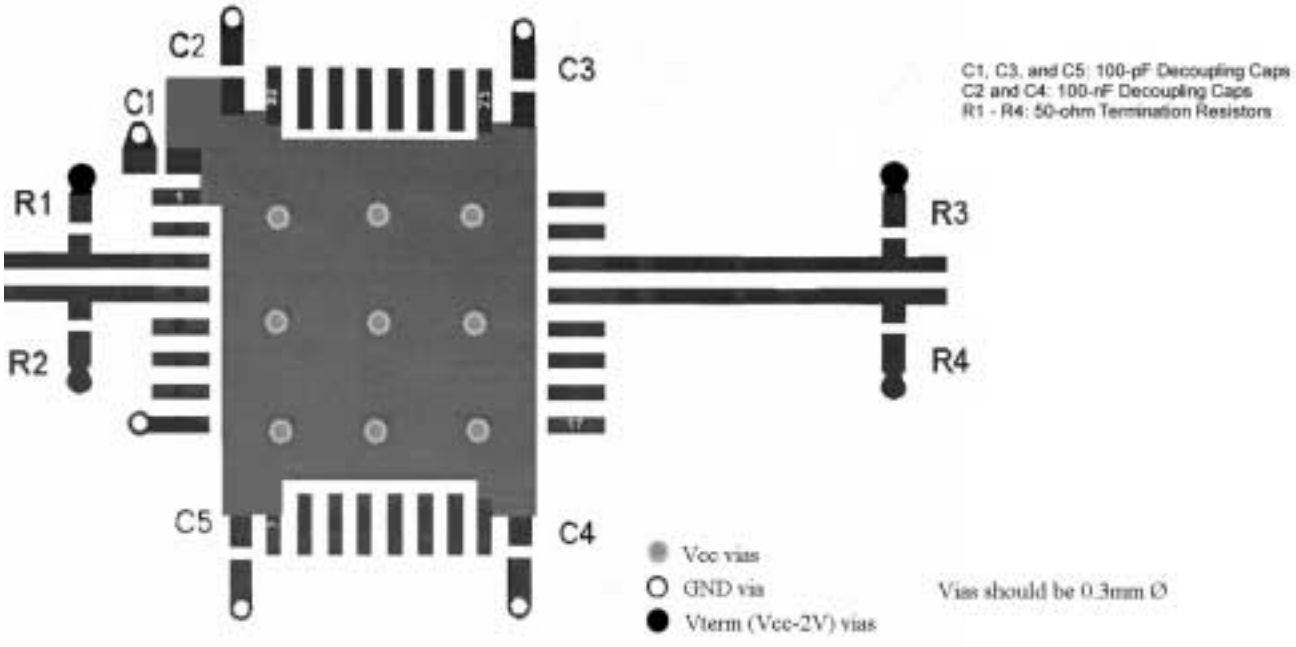

Figure 1. PCB Layout Proposal

3 Power Consumption and Chip Temperature

Estimating the chip temperature is a difficult task with all the external factors mentioned in Section 2.1 having an influence. The classical method by merely using the worst case: package data, power consumption, and environmental temperature results in a much too pessimistic picture.

Example 1: Max Power Consumption and Worst Case Chip Temperature

Data sheet limits:

1. Internal: I_{DD} max 85 mA
2. Output + internal: I_{DD} max 380 mA
3. Delta (output w/o internal): 380 mA – 85 mA = 295 mA or ~15 mA per output (20 outputs)

P_{int} = 3.8 V x 85 mA = 323 mW

All outputs are terminated with 50 Ω to V_{CC} - 2 V

$P_{outputs}$ = (295 mA x 2 V) – 20(15 mA)^2 x 50 Ω

$P_{outputs}$ = 590 mW – 225 mW = 365 mW

P_{Device} = 323 mW + 365 mW = 688 mW (worst case)

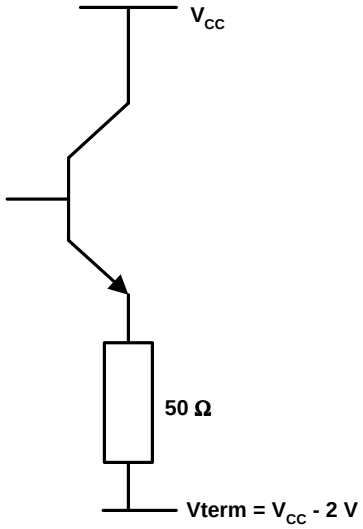

Figure 2. Output Stage and Termination Schematic

Worst case θ_{JA} (with no air flow): 78°C /W

Delta T = 0.688 W x 78°C / W = 53.6°C

Therefore, the chip temperature is maximum 54°C above the ambient temperature.

Example 2: Typical Power Consumption at 3.3-V V_{CC}:

Internal: I_{DD} = 60 mA

Typical V_{OL}/V_{OH} relative to Vterm: 0.5 V / 0.9 V

Average I_{Load} = 0.7 V/50 Ω = 14 mA per output

P_{int} =3.3 V x 60 mA ~ 200 mW

Poutputs = 20(14 mA x 2 V) – 20(14 mA)^2 x 50 Ω

Poutputs = 560 mW – 196 mW ~ 360 mW

PDevice = 200 mW + 360 mW = 560 mW

Delta T = 0.56 W x 78°C/W = 44°C above T_A at still air

Delta T = 0.56 W x 68°C/W = 38°C above T_A at 500 LFM air flow

3.1 How Can the Device Power Consumption Be Reduced?

In applications where not all 10 output pairs are needed, unused outputs should be left open and not terminated with 50 Ω. The above calculation examples show that the power savings would be in the range of 36-mW device internal plus 20 mW on the termination resistors (device external) per differential output pair. Running the system at 2.5 V reduces the internal (without the output transistors) power dissipation to typical 2.5 V x 56 mA ~ 140 mW. Compared to a typical of 200 mW (Example 2) in a 3.3-V system the device power consumption is around 60 mW lower.

4 Summary

Under worst-case conditions (Example 1), the maximum chip temperature is 54°C above T_A. As long as the ambient temperature in the application is below 60°C, no special PCB layout or airflow is required. In a 3.3-V environment (Example 2), T_J is about 40°C above T_A so that a temperature of 70°C over the lifetime of the device is possible. In a system where T_A is continuously at 85°C and the use of a fan is not possible, applying PCB layout proposals described in Section 2.2 to reduce θ_{JA} and the chip temperature by 5°C to 10°C is required. Reducing the power consumption in the device as described in Section 2.1 is another recommended alternative to consider.

5 References

1. *Filtering Techniques: Isolating Analog and Digital Power Supplies in TI's PLL-Based CDC Devices,* Texas Instruments literature number SCAA048
2. *How Not to Decouple High-Speed OP-Amps*, Texas Instruments literature number SLOA069.
3. *Package Thermal Characterization Methodologies*, Texas Instruments literature number SZZA003.
4. *Thermal Derating Curves for Logic-Products Packages*, Texas Instruments literature number SZZA013A.
5. *EIA/JEDEC STANDARD, JESD51-7: High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*

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