User's Guide

TDP1204 EVM User's Guide

ABSTRACT

How to use and configure the TDP1204 EVM along with recommendations for system hardware implementation is described in this document. These recommendations are only guidelines and it is the designer's responsibility to consider all system characteristics and requirements. Engineers should refer to the data sheet for technical details such as device operation, terminal description, and so forth.

Table of Contents

1 Overview 2
1.1 What is the TDP1204 EVM? 2
1.2 What is Included in the TDP1204 EVM? 2
1.3 What Does the EVM Look Like? 2
2 Hardware Configuration 3
2.1 Power 3
2.2 Enable or Reset 3
2.3 Configuration Jumpers 3
2.4 Rx EQ Configuration 4
2.5 HPD Snoop Option 5
2.6 Local I2C Access 5
3 Quick Start Guide 5
4 Schematics 6

Trademarks

All trademarks are the property of their respective owners.

Copyright © 2022 Texas Instruments Incorporated

1 Overview

1.1 What is the TDP1204 EVM?

The TDP1204 EVM is a PCB created to help for customers evaluate the TDP1204 for video applications with HDMI interfaces. This EVM can also be used as a hardware reference design for implementations of the TDP1204. PCB design or layout files can be provided upon request to provide PCB design illustrations of the routing or placement rules with a TDP1204 component.

1.2 What is Included in the TDP1204 EVM?

The major components of the EVM are as below:

- TDP1204 device
- Standard HDMI source connector (receptacle)
- Standard HDMI sink connector (receptacle)
- DC power regulators
- I2C programming interface for external I2C host connections
- USB interface
- Headers for configurating various TDP1204 features

1.3 What Does the EVM Look Like?

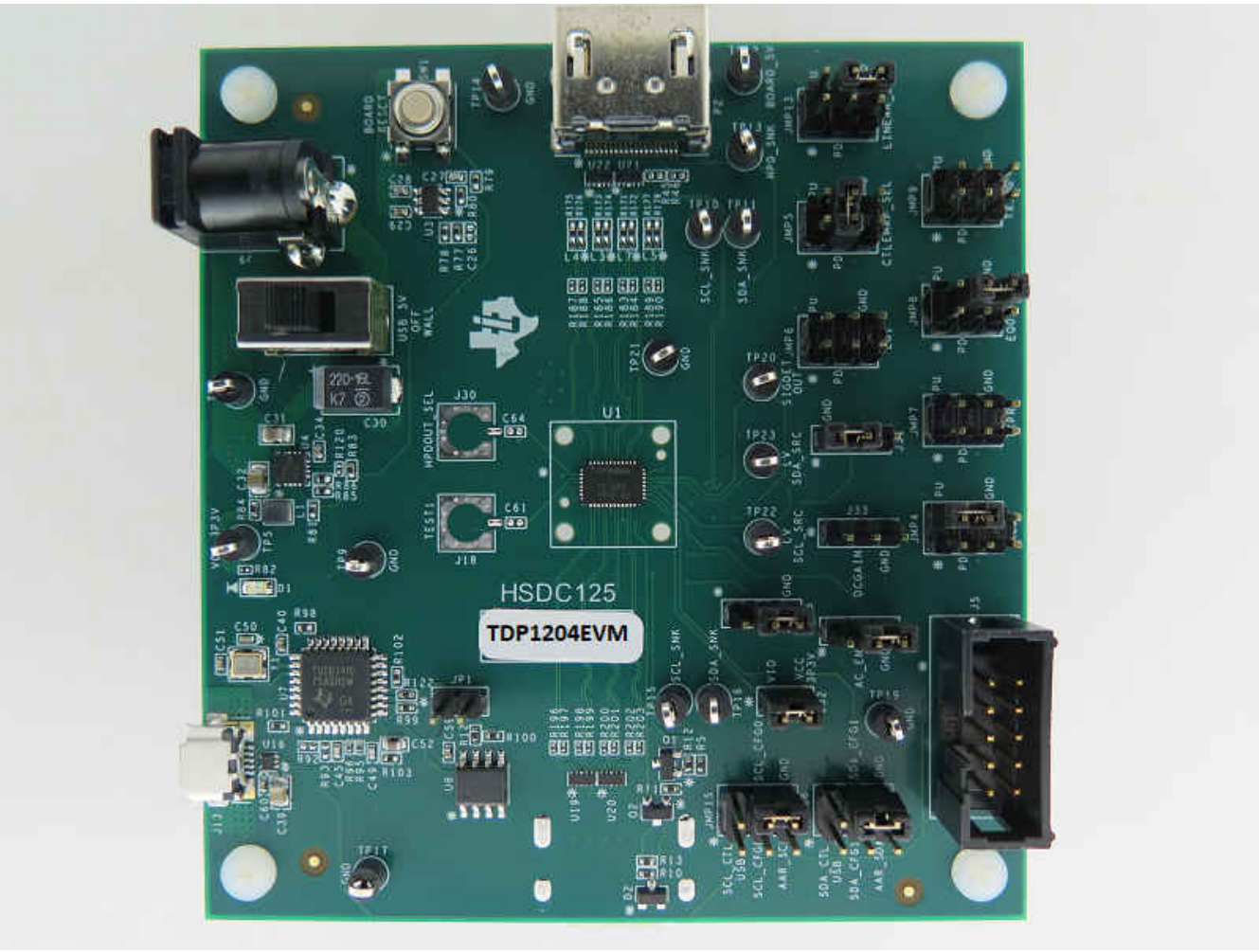


Figure 1-1. EVM Board

Copyright © 2022 Texas Instruments Incorporated

2 Hardware Configuration

2.1 Power

A DC barrel jack (J9) to accept a 5-V wall power adapter is provided on the EVM. The DC barrel jack (CUI Inc. PJ-202AH) has an inner diameter of 2.1 mm and an outer diameter of 5.5 mm. The tip of the +5 V power supply must be positive. A +5 V power supply of at least 1.5 amps that meets the above requirements can be used to power the TDP1204 EVM. Power is provided to the EVM when SW2 is set to position 1.

Alternately, it is possible to power the EVM by connecting a USB Micro cable from a host to the J13 USB Micro B connector and setting SW2 to position 3.

Note

Limit VBUS voltage and voltage from barrel jack to no more than 6 V.

2.2 Enable or Reset

There are three device enable or reset options to use with the EVM.

1. Supervisor circuitry option. This is the default configuration on the EVM. The enable (EN) signal is held low until the power good (REG_PG) from the 3.3 V voltage regulator reaches a stable high voltage level then released high.
2. RC timing option. C26 external capacitor and internal resistor are used ton control the EN pin ramp time after device is powered on. C26 is a DNI (*Do Not Install* option) by default. C26 needs to be installed and R77 needs to be uninstalled to enable this option.
3. External control option. A push button (SW1) is provided to manual control of the EN pin.

2.3 Configuration Jumpers

Multiple jumpers are provided on the EVM for configuration of TDP1204 and also for probe points.

The following is a list of 4-level jumpers which are used to configure the TDP1204: JMP4, JMP5, JMP6, JMP7, JMP8, JMP9, and JMP13. The jumper position to select between the different levels is detailed in Table 2-1.

Note

4-level pins are sampled after the rising edge of EN pin. Therefore, a change in any 4-level pin state will not be applied until after EN pin is toggled from low to high.

Table 2-1. 4-Level Configuration Jumper Settings

Jumper Position	4-level State
Short 4 to 6	0
Short 3 to 4	R
Open	F
Short 2 to 4	1

Table 2-2. Jumpers

Jumper	Default Position	Description
JMP4	Short 4 to 6	**MODE.** Default is pin-strap mode. If I2C mode is desired, leave this jumper open or no-connect. Refer to data sheet for more details.
JMP5	Short 2 to 4	**CTLEMAP_SEL.** Refer to data sheet for details on different CTLEMAP options.
JMP6	Open	**EQ1.** In pin-strap mode, this jumper along with JMP8 (EQ0) will select the EQ value for the receiver. The EQ may need to be tuned based on quality of HDMI cable used. Refer to data sheet for details on EQ options.
JMP7	Open	**TXPRE.** Refer to data sheet for details.
JMP8	Short 4 to 6	**EQ0/ADDR.** In pin-strap mode, this jumper along with JMP6 (EQ1) will select the EQ value for the receiver. The EQ may need to be tuned based on quality of HDMI cable used. Refer to data sheet for details.
JMP9	Open	**TXSWG.** Refer to data sheet for details.
JMP13	Short 4 to 6	**LINEAR_EN.** Refer to data sheet for details.

Copyright © 2022 Texas Instruments Incorporated

Table 2-2. Jumpers (continued)

Jumper	Default Position	Description
JMP15	Short 4 to 6	**SCL and CFG0.** **Short 1 to 3:** I2C clock from TUSB3410 (U7). **Short 3 to 5:** I2C clock from Aardvark connector (J5). **Short 2 to 4:** CFG0 pulled up to VIO (3.3 V). Refer to data sheet for details on CFG0. **Short 4 to 6:** CFG0 pull-down to GND. Refer to data sheet for details on CFG0.
JMP16	Short 4 to 6	**SDA and CFG1.** **Short 1 to 3:** I2C data from TUSB3410 (U7). **Short 3 to 5:** I2C data from Aardvark connector (J5). **Short 2 to 4:** CFG1 pulled up to VIO (3.3 V). Refer to data sheet for details on CFG1. **Short 4 to 6:** CFG1 pull-down to GND. Refer to data sheet for details on CFG1.
J25	Short 2 to 3	**HPDOUT_SEL.** **Short 1 to 2:** HPD_OUT is open drain. **Short 2 to 3:** HPD_OUT is push-pull.
J27	Short 2 to 3	**AC_EN** **Short 1 to 2:** OUT_D[2:0] and OUT_CLK is AC-coupled. Make sure R171, R172, R173, R174, R175, R176, R177, and R178 are populated with 100 nF capacitor or make sure AC capacitor is external to EVM board. **Short 2 to 3:** OUT_D[2:0] and OUT_CLK is DC-coupled. Make sure R171, R172, R173, R174, R175, R176, R177, and R178 are populated with 0-Ω resistor.
J31	Short 2 to 3	**DDC Level Shifter enable/disable** **Short 1 to 2:** Discrete DDC level shifter (U23) disabled. **Short 2 to 3:** Discrete DDC level shifter (U23) enabled.
J32	Short 1 to 2	**VIO Voltage.** **Short 1 to 2:** VIO connected to board 3.3 V. **OPEN:** VIO is from an external supply.

2.4 Rx EQ Configuration

There are sixteen EQ settings with 0 being the lowest and Fh being the highest. Refer to data sheet for specific EQ value.

Table 2-3. Rx Equalization Control

Register(s): CLK_EQ, D0_EQ, D1_EQ, D2_EQ Equalization Setting #	EQ1 PIN Level	EQ0 PIN Level	EQ Gain
0	0	0	Lowest EQ setting.
1	0	R	
2	0	F	
3	0	1	
4	R	0	
5	R	R	
6	R	F	
7	R	1	
8	F	0	
9	F	R	
10	F	F	
11	F	1	
12	1	0	
13	1	R	
14	1	F	
15	1	1	Highest EQ setting

Copyright © 2022 Texas Instruments Incorporated

2.5 HPD Snoop Option

To accommodate systems that do not properly resend DDC commands after HPD goes low, we have implemented an HPD snoop mode on the TDP1204 EVM. This mode allows the HPD line to be routed around the TDP1204, but remain connected to the TDP1204 on the sink side to allow the TDP1204 to snoop its state.

- Populate R131, no populate R129 for HPD on.
- No populate R131, populate R129 for HPD snoop-only

2.6 Local I2C Access

Access to TDP1204s local I2C signals is provided through the J5 connector. The TDP1204 supports either 1.2 V, 1.8 V and 3.3 V LVCMOS levels. The TDP1204 VIO pin is used to select which voltage level is used for the following 2-level control pins: LV_DDC_SDA, LV_DDC_SCL, SCL/CFG0, and SDA/CFG1. It is important that the I2C signalling levels meet the TDP1204 LVCMOS levels when I2C interface is accessed through the connector.

A standalone external I2C host can be connected through J5 for debug and control purposes. An example of an external I2C Host controller is the Total Phase Aardvark I2C/SPI Host Adapter (Total Phase Part#: TP240141). Sample scripts for this I2C host controller are provided by request.

The target I2C address for the TDP1204 can be modified by the EVM jumper JMP8. Please refer to the TDP1204 ADR/EQ pin setting and its corresponding I2C address. Refer to TDP1204 data sheet for the 7-bit I2C target address options.

Table 2-4. Aardvark I2C (J5) Pinout

J5 pin #	Description	J5 pin #	Description
1	SCL_CTL	2	GND
3	SDA_CTL	4	NC
5	NC	6	NC
7	NC	8	NC
9	NC	10	GND

3 Quick Start Guide

The instructions below assume the EVM is configured for pin-strap mode and is powered from barrel jack.

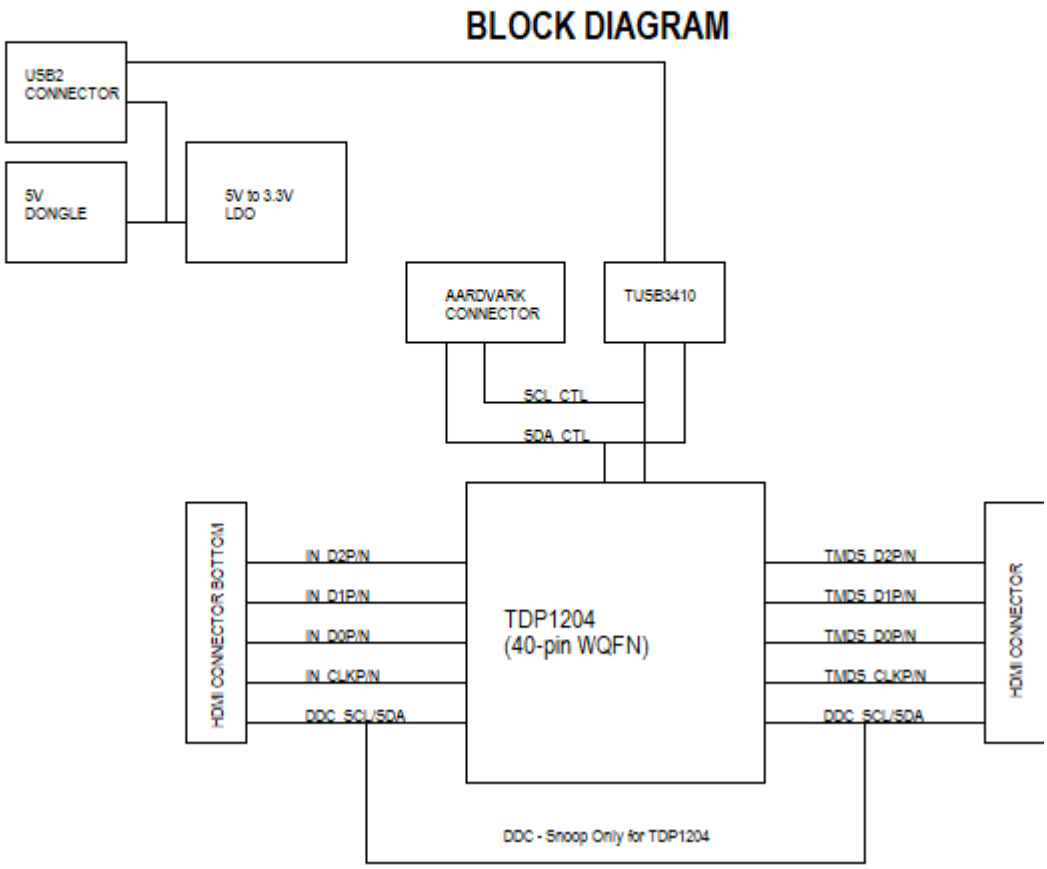
1. Insertion +5 V DC Power source into barrel jack. Turn on SW2.
2. If using external I2C configuration instead of pin-straps, please configure TDP1204 at this step.
3. Insert a HDMI source using a standard HDMI cable into P1 (HDMI receptacle).
4. Insert a HDMI video sink into P2 (HDMI receptacle) using a standard HDMI cable.
5. Video output on HDMI sink should be observed.

Copyright © 2022 Texas Instruments Incorporated

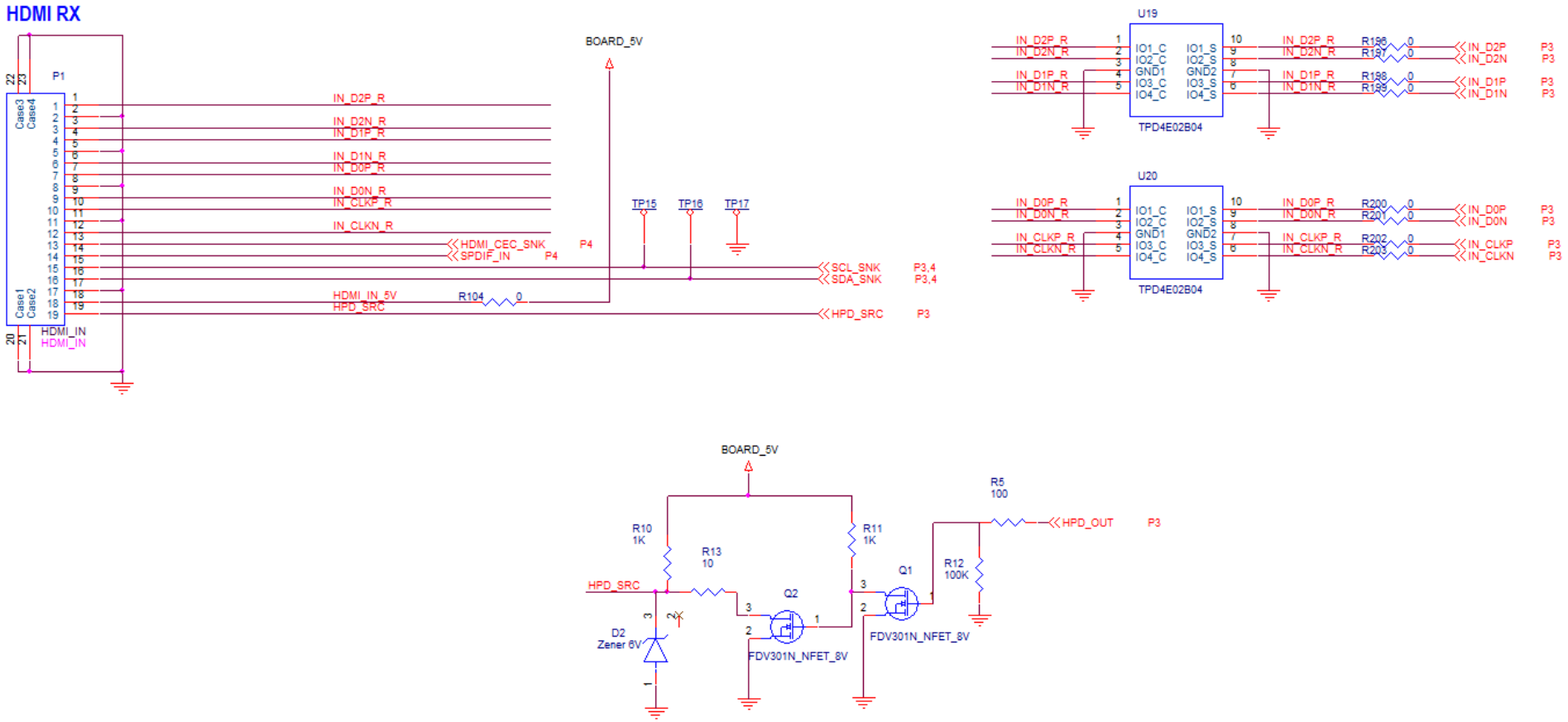
4 Schematics

NOTES:

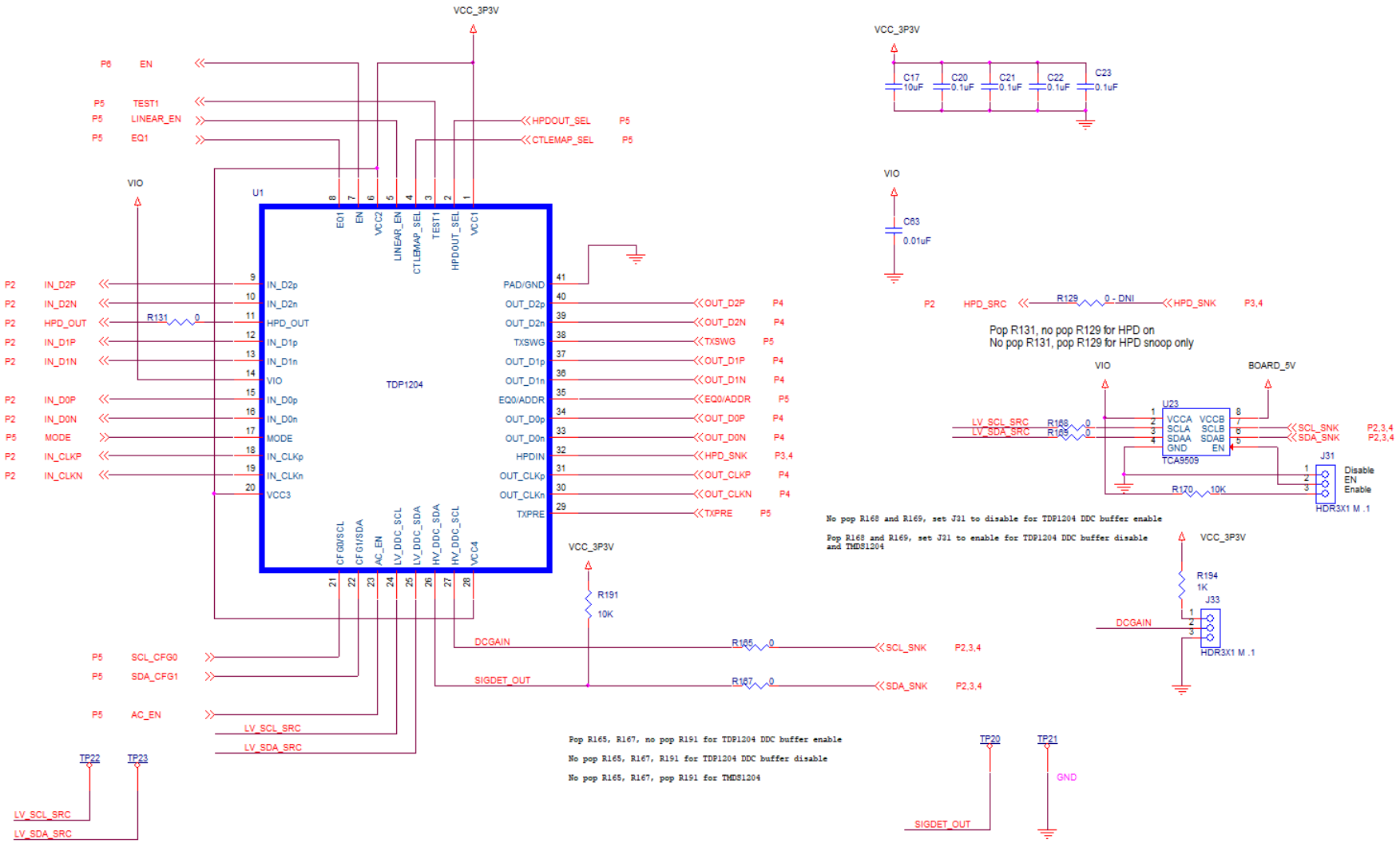
- 100-ohm differential impedance for HDMI differential pairs.



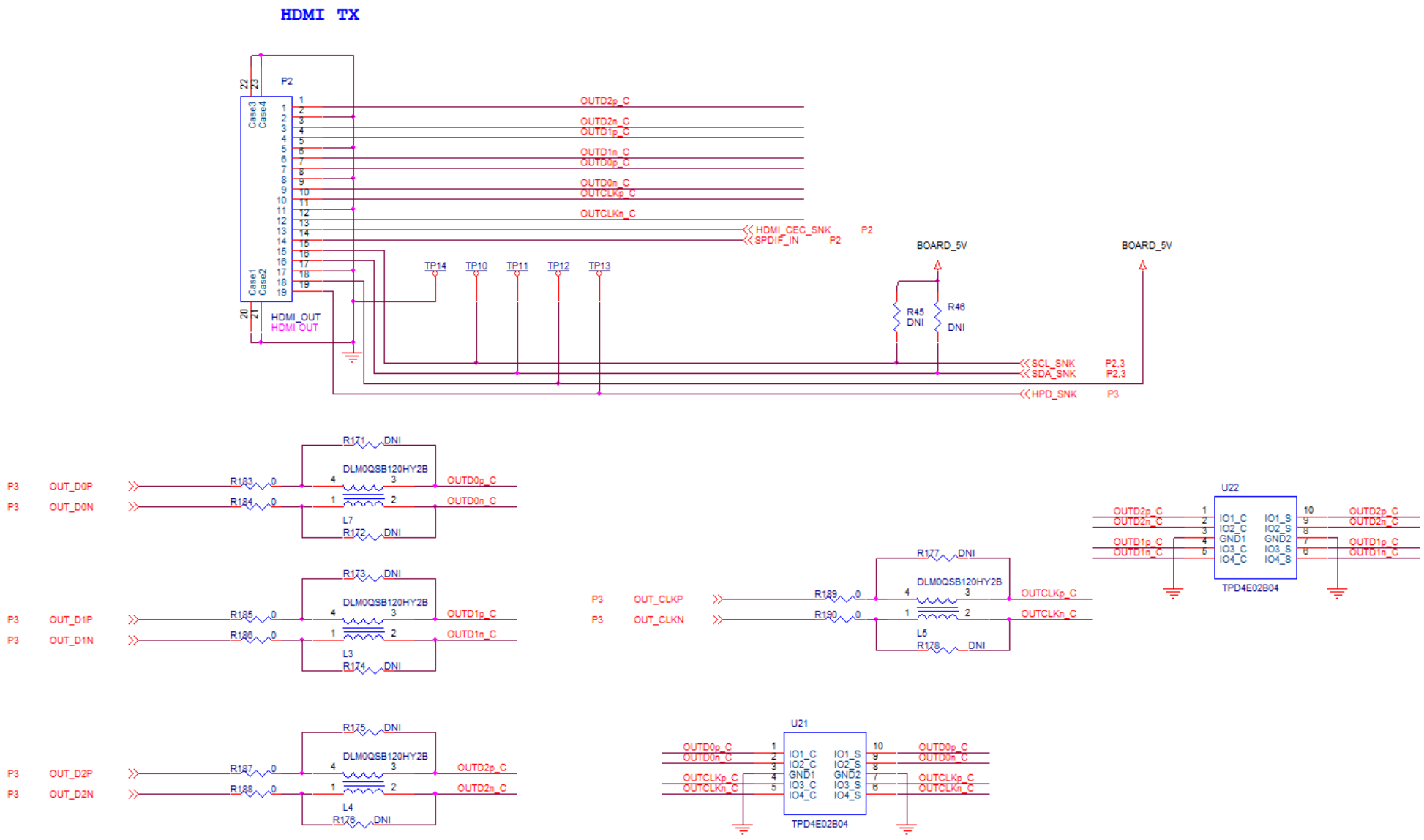
Copyright © 2022 Texas Instruments Incorporated



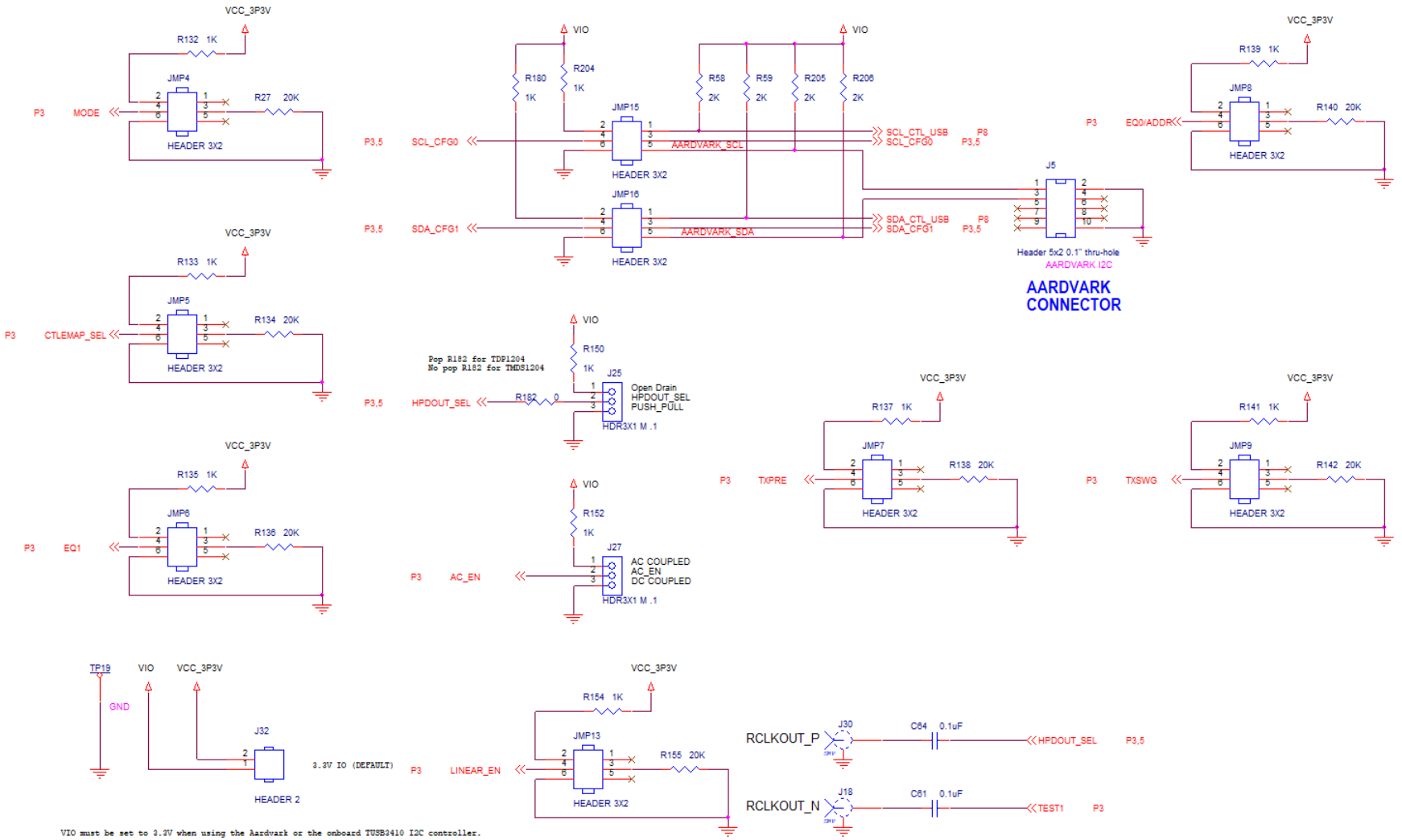
Copyright © 2022 Texas Instruments Incorporated



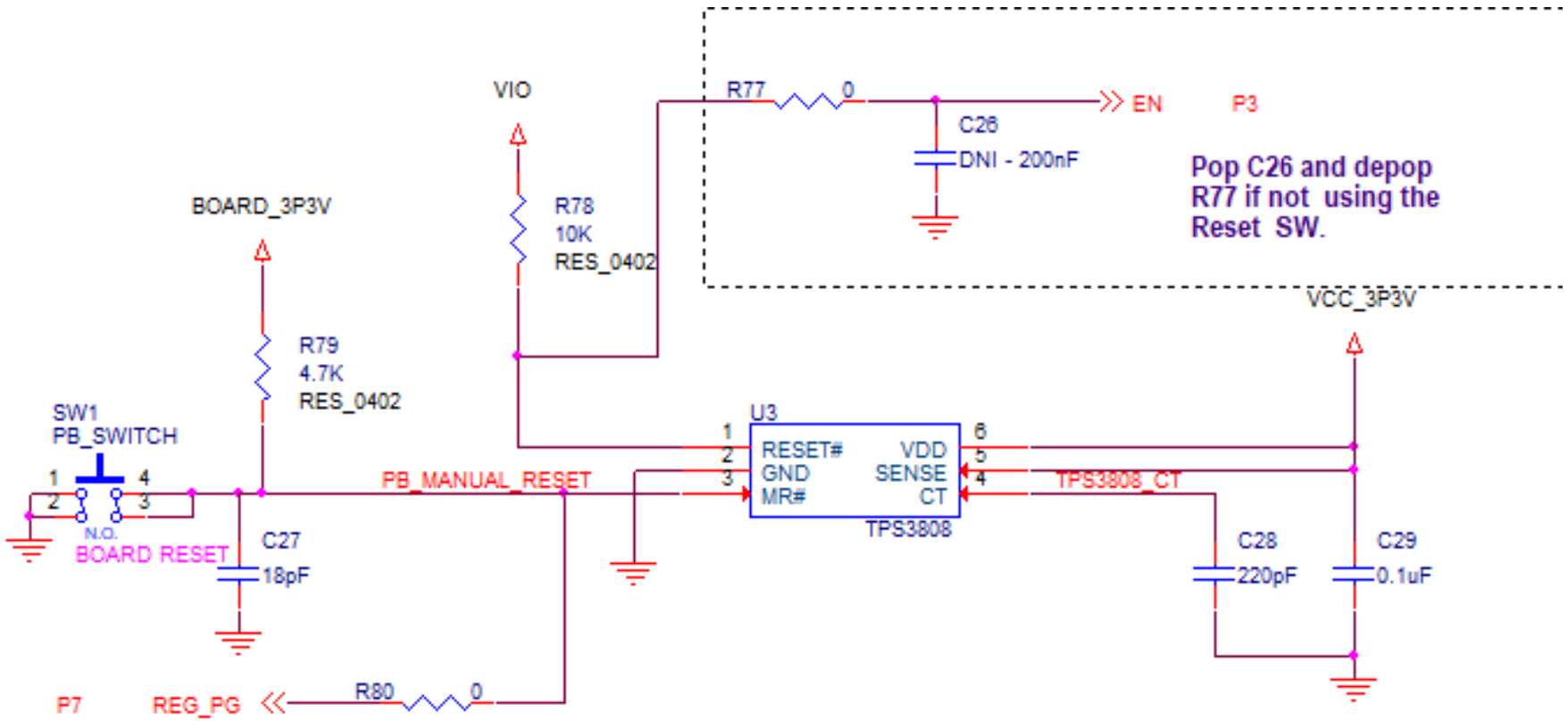
Copyright © 2022 Texas Instruments Incorporated



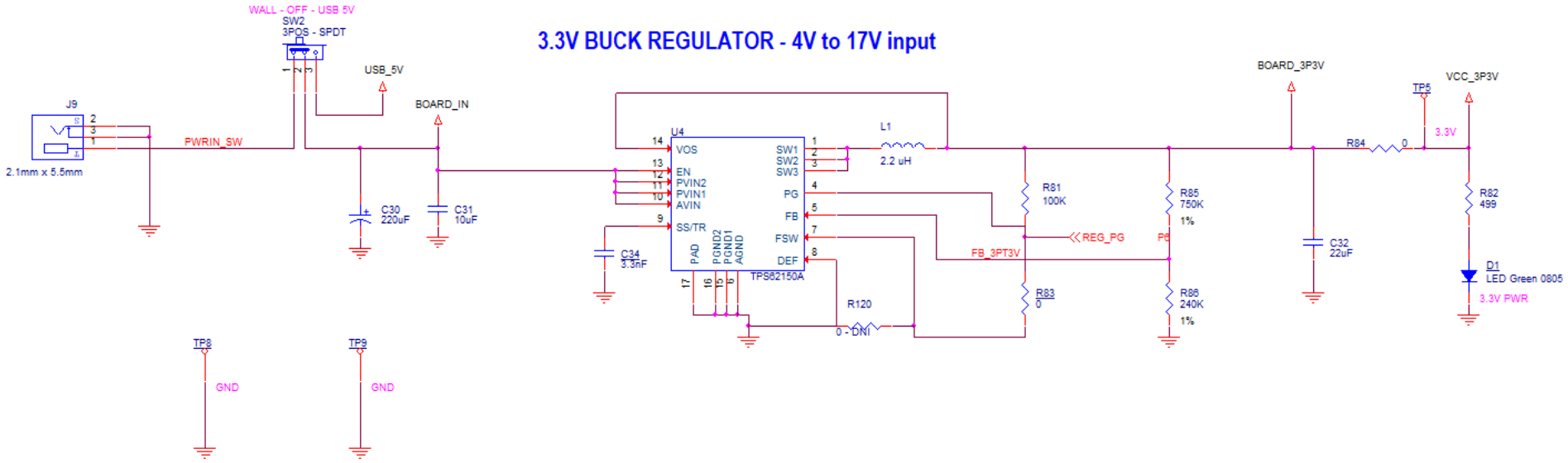
Copyright © 2022 Texas Instruments Incorporated



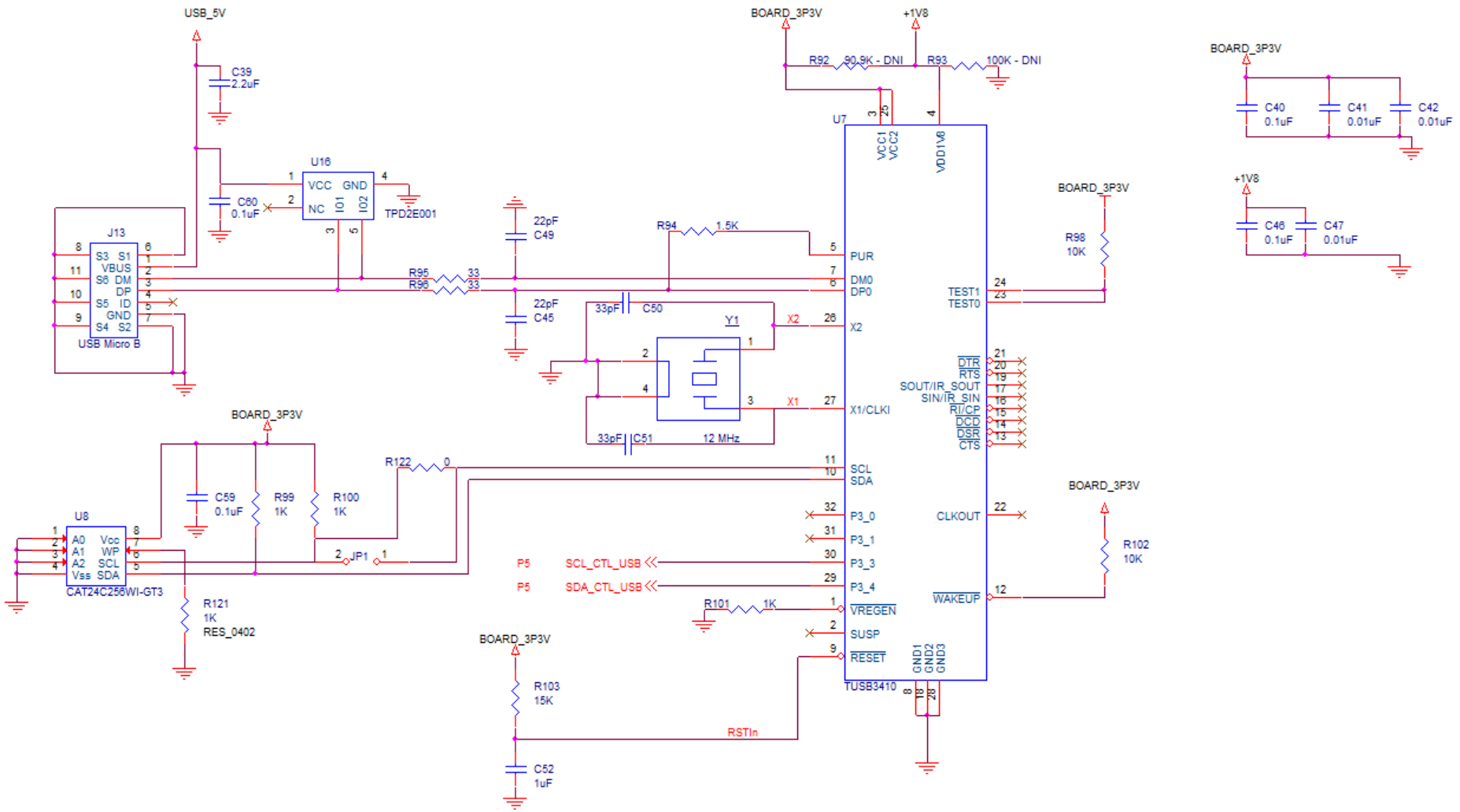
Copyright © 2022 Texas Instruments Incorporated



Copyright © 2022 Texas Instruments Incorporated



Copyright © 2022 Texas Instruments Incorporated



Copyright © 2022 Texas Instruments Incorporated

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated