Application of the SN74SSTVF16857 in Planar PC2700 (DDR-333) RDIMMs

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ABSTRACT

The high-capacity memory modules used in servers and workstations present a complex load to the memory controller used in these high-reliability, high-performance systems. To meet the demands of stable functionality over a broad spectrum of operating environments and system timing needs, and to support data integrity, these dual in-line memory modules (DIMMs) require the use of registers in the address and control signal paths. These registered DIMMs (RDIMMs) come in various configurations, depending on the system requirements. The JEDEC-standard SSTV16857 used on many double-data-rate (DDR) planar RDIMMs is production tested using the JEDEC-defined test load. The test load is a lumped resistor-capacitor (RC) network, which differs significantly from the distributed RDIMM load. Consequently, Texas Instruments (TI) developed the SN74SSTVF16857 device, whose outputs are optimized and designed to drive a planar RDIMM load. The SN74SSTVF16857 outputs have edge-control circuitry to minimize switching noise in the unterminated RDIMM environment, making it over 600 ps faster than the JEDEC-standard SSTV16857 device in PC2700 RDIMM (DDR-333) applications during simultaneous switching. This application report discusses the characteristics, applications, and performance of the SN74SSTVF16857 in a planar PC2700 RDIMM. The information in this report and the SN74SSTVF16857 data sheet should enable a memory-module designer to successfully design a planar PC2700 RDIMM.

Keywords: 1U, 2.5 V, buffer, DDR, DDR-333, DIMM, RDIMM, low profile, PC1600, PC2100, PC2700, planar RDIMM, power consumption, register, SSTL_2, SSTV, SSTV16857, SSTVF16857

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1 Introduction

The increasing demand for more memory capacity and bandwidth in high-performance servers, workstation computer systems, and networking equipment has lead to the development of the JEDEC standard for double-data-rate (DDR) synchronous dynamic-random-access-memory (SDRAM) based, 184-pin, registered dual in-line memory modules (RDIMMs). To meet the demands of stable functionality over the broad spectrum of operating environments and system timing needs and to support data integrity, the loads presented by the large number of SDRAMs on the RDIMMs require the use of registers in the address and control-signal paths. Texas Instruments (TI) offers a variety of registers to support planar and stacked DDR RDIMMs.

The SN74SSTV32867 and SN74SSTV32877 are 26-bit input to 26-bit output devices. Both devices are offered in the 96-ball GKE LFBGA package and are single-chip solutions for PC1600 (DDR-200) and PC2100 (DDR-266) planar RDIMMs. The SN74SSTV32867 has output edge-control circuitry to minimize switching noise in an unterminated RDIMM load, while the SN74SSTV32877 has SSTL_2 Class II specified outputs and the output-enable function to disable the outputs (high-impedance state).

The SN74SSTV16857 and SN74SSTVF16857 are 14-bit input to 14-bit output devices. Both devices are offered in the 48-pin TSSOP package and are dual-chip solutions (two registers per RDIMM) for PC1600 and PC2100 planar RDIMMs. The SN74SSTVF16857 has output edge-control circuitry to minimize switching noise in an unterminated RDIMM load. In addition, the SN74SSTVF16857 is a dual-chip solution for PC2700 (DDR-333) planar RDIMMs.

The SN74SSTV16859, SN74SSTVF16859, SN74SSTV32852 and SN74SSTVF32852 are register solutions for stacked DDR RDIMMs. The SN74SSTV16859 and SN74SSTVF16859 are 13-bit input to 26-bit output devices packaged in a 64-pin TSSOP package. Two SN74SSTV16859 or two SN74SSTVF16859 devices are required to drive 36 SDRAMs on a two-rank ×4 SDRAMs PC1600 or PC2100 RDIMM. The SN74SSTVF16859 has output edge-control circuitry to minimize switching noise in an unterminated RDIMM load. In addition, the SN74SSTVF16859 is a dual-chip solution for PC2700 (DDR-333) stacked RDIMMs.

The SN74SSTV32852 and SN74SSTVF32852 are 24-bit input to 48-bit output devices packaged in a 114-ball GKF LFBGA package. One SN74SSTV32852 or one SN74SSTVF32852 device is required to drive 36 SDRAMs on a two-rank ×4 SDRAMs PC1600 or PC2100 RDIMM. The SN74SSTV32852 is most suitable for low-profile (1U) PC2100 RDIMM designs.[1] The SN74SSTVF32852 has output edge-control circuitry to minimize switching noise in an unterminated RDIMM load. In addition, the SN74SSTVF32852 is a single-chip solution for PC2700 (DDR-333) stacked RDIMMs.

The selection of a register component is integral to the execution of a successful RDIMM design. This application report focuses only on the logic solutions that Texas Instruments has available for the planar PC2700 RDIMMs that provide improved performance, cost savings, and design optimization. The report discusses the characteristics, applications, and performance of the SN74SSTVF16857 in a planar RDIMM at DDR-333 speed.

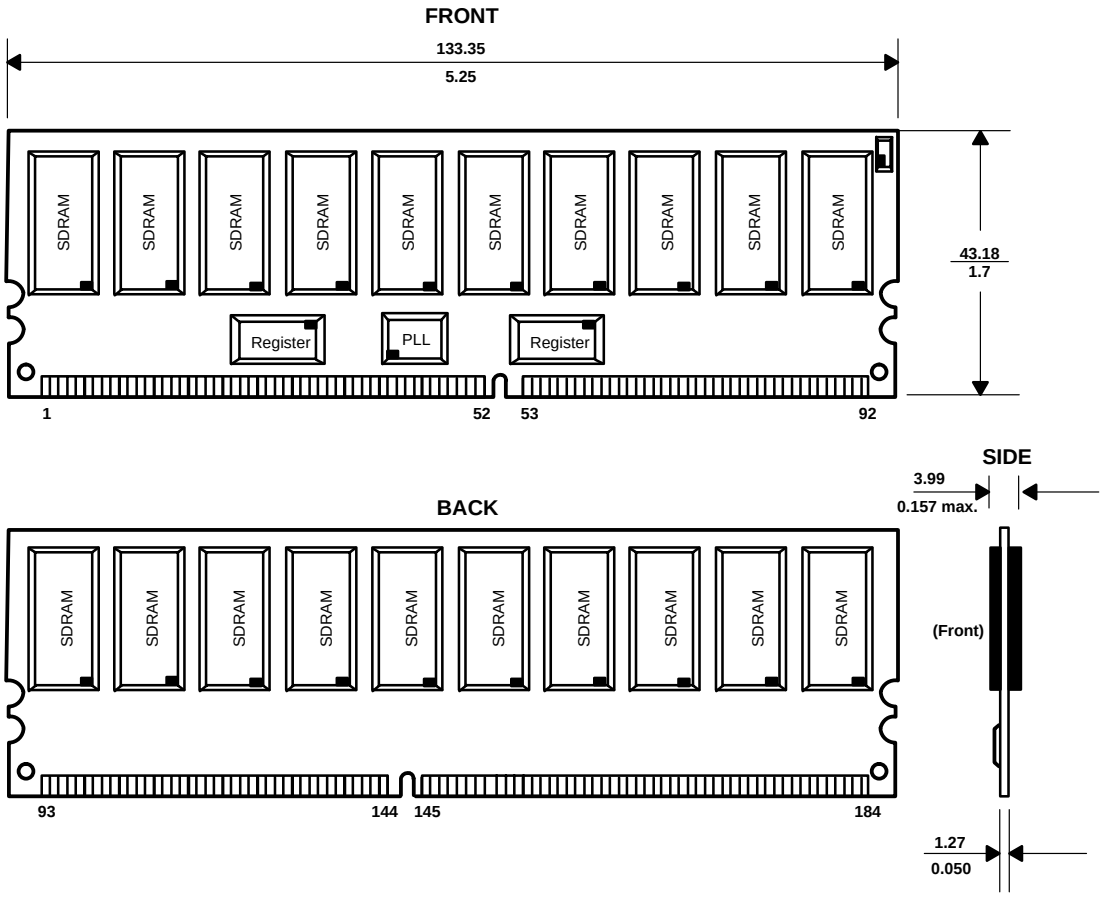
2 DDR RDIMM Overview

DDR RDIMMs provide twice the data-bus bandwidth of previous-generation single-data-rate (SDR) memory modules. Data transfer in DDR systems is done at twice the rate at which commands or addresses may be clocked into the DDR SDRAM device. Commands and addresses are entered into the SDRAM device only on the crossing of the rising edge of the clock (CK) signal and falling edge of the complementary clock ($\overline{CK}$) signal. However, data is exchanged on the crossing of both the rising and falling edges of the CK signal (and $\overline{CK}$ signal).

Differential signaling was added to the DDR system to improve signal integrity, decrease timing variations, and improve noise immunity within the system. In addition to the differential clocks and data being transmitted on both clock edges, the use of SSTL_2 signaling techniques, addition of delay locked loops (DLL) to reduce access time uncertainty, addition of data strobes to improve data capture timing, and the reduction of input capacitances at the DDR SDRAM and register devices enhances signal integrity, timing, and noise immunity.

Further, the 184-pin DDR RDIMMs have a reset ($\overline{RESET}$) feature and an input-clocks-detect feature to facilitate controlled power up and to minimize power consumption during low power mode. When $\overline{RESET}$ is low, the register's differential input receivers are disabled, and undriven (floating) data and reference voltage (V_{REF}) inputs are allowed for the register. In addition, when $\overline{RESET}$ is low, all register outputs are forced low. These enhancements permit the modules to power up with the SDRAM outputs in the high-impendance state (eliminating the risk of high current dissipations and/or dotted I/Os), and result in the powering down of module support devices when the module is in self-refresh mode.

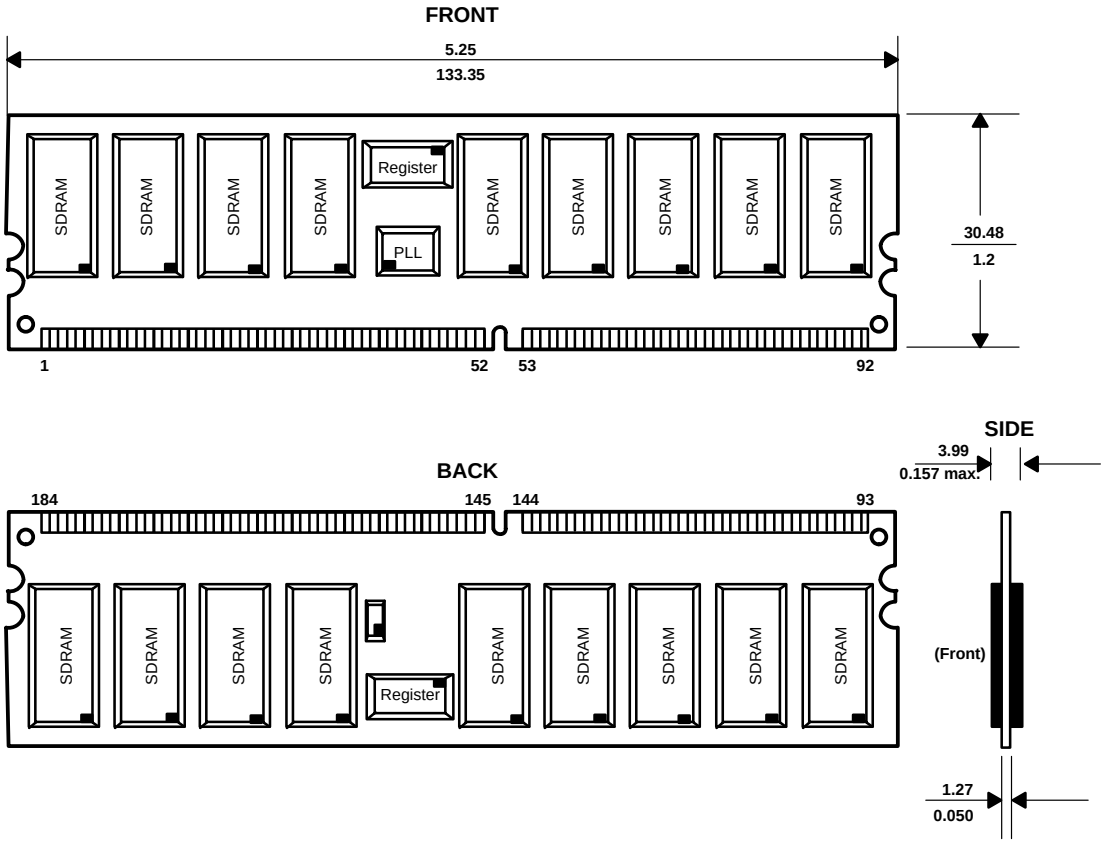
RDIMMs come in many configurations, depending on the system requirements. Figure 1 shows an example of a JEDEC-standard Raw Card version B registered DDR DIMM. The four types of integrated circuits (IC) on the module are the DDR SDRAMs (18 devices per module), the SSTV16857 registers (two devices per module), a CDCV857-type phase-locked-loop (PLL) clock driver (one device per module), and a serial-presence-detect (SPD) EEPROM (one device per module).



NOTES: A. All dimensions are typical, unless otherwise stated. millimeters / inches
B. All dimensions are for reference only. Refer to JEDEC Publication 95 MO-206 for detailed dimensions.

Figure 1. JEDEC-Standard Raw Card Version B Component Placement

The JEDEC-standard Raw Card version B is a 1.7-inch-height RDIMM. However, the current trend is to migrate to a module that has a maximum height of 1.2 inch to accommodate applications in 1U (1.75-inch tall) form-factor systems (high-performance servers and networking equipment). Consequently, the 1.7-inch Raw Card version B RDIMM has been redesigned to the 1.2-inch Raw Card version M RDIMM. Figure 2 shows a diagram of an example JEDEC-standard Raw Card version M registered DDR DIMM. The Raw Card version M RDIMM can support the same memory density as the Raw Card version B RDIMM.



millimeters
inches

NOTES: A. All dimensions are typical, unless otherwise stated.
B. All dimensions are for reference only. Refer to JEDEC Publication 95 MO-206 for detailed dimensions.

Figure 2. JEDEC-Standard Raw Card Version M Component Placement

For mechanical diagrams, component placements, and additional information of other JEDEC-standard Raw Cards, refer to the *PC2100 and PC1600 DDR SDRAM Registered DIMM Design Specification.*[2] The data presented in this application report were collected from the *PC2100 and PC1600 DDR SDRAM Registered DIMM Design Specification.*[2]

The JEDEC-standard Raw Card versions A, B, L, and M are planar registered DDR DIMMs. Raw Card versions A and L RDIMMs can support one rank of ×8 SDRAMs, for a maximum of nine memory ICs per memory module. In this application, using the SSTV16857-type register, each register output drives nine SDRAM loads. Also, Raw Card versions A and L RDIMMs can support two ranks of ×8 SDRAMs, for a maximum of 18 memory ICs per memory module. In this application, using the SSTV16857-type register, each register output drives 18 SDRAM loads. Raw Card versions A and L RDIMMs require the use of two 14-bit input to 14-bit output registers to drive a 20-bit address/command bus (for one rank of ×8 SDRAMs) or a 22-bit address/command bus (for two ranks of ×8 SDRAMs).

Similarly, Raw Card versions B and M RDIMMs require the use of two 14-bit input to 14-bit output SSTV16857-type registers. The RDIMMs can support one rank of ×4 SDRAMs (18 memory ICs per memory module). In these applications, each SSTV16857-type register output drives 18 SDRAM loads. Raw Card versions B and M RDIMMs require the use of two 14-bit input to 14-bit output registers to drive a 20-bit address/command bus (for one rank of ×4 SDRAMs).

The JEDEC-standard Raw Card versions C and N are stacked registered DDR DIMMs, organized as two ranks of ×4 SDRAMs (36 memory IC per memory module). The RDIMMs require a one-input to two-output-type register and each register output drives 18 SDRAM loads. In the Raw Card version C RDIMM application, each SSTV16859 register output drives 18 SDRAM loads. Raw Card version C RDIMM requires the use of two 13-bit input to 26-bit output registers to drive a 22-bit address/command bus (for two ranks of ×4 SDRAMs). On the other hand, in the Raw Card version N RDIMM application, each SSTV32852 register output drives 18 SDRAM loads. The Raw Card version N RDIMM requires the use of one 24-bit input to 48-bit output register to drive a 23-bit address/command bus (for two ranks of ×4 SDRAMs).

The scope of this application report is limited to the application of planar RDIMMs (Raw Card versions A, B, L, and M) and an evaluation of the performance of the SN74SSTVF16857 in these RDIMM applications at DDR-333 speed.

At DDR-333 speed, the clock frequency is 166.67 MHz. However, the rate for transferring data to or from the SDRAM is 333-million transfers per second (double the clock frequency). Therefore, an 8-byte-wide data bus has a bandwidth (the amount of data it can move each second) of 2,666 MB/s (333-million transfers per second ×8 bytes). Consequently, PC2700 is used to refer to RDIMMs with DDR-333 SDRAMs and is used in systems with a 333-Mbit/s data-rate memory data bus.

3 Register Solution for Planar PC2700 RDIMMs

The JEDEC-standard register for planar RDIMM applications is the SSTV16857. Figure 3 shows the function table, pinout, and logic diagram of the SSTV16857.

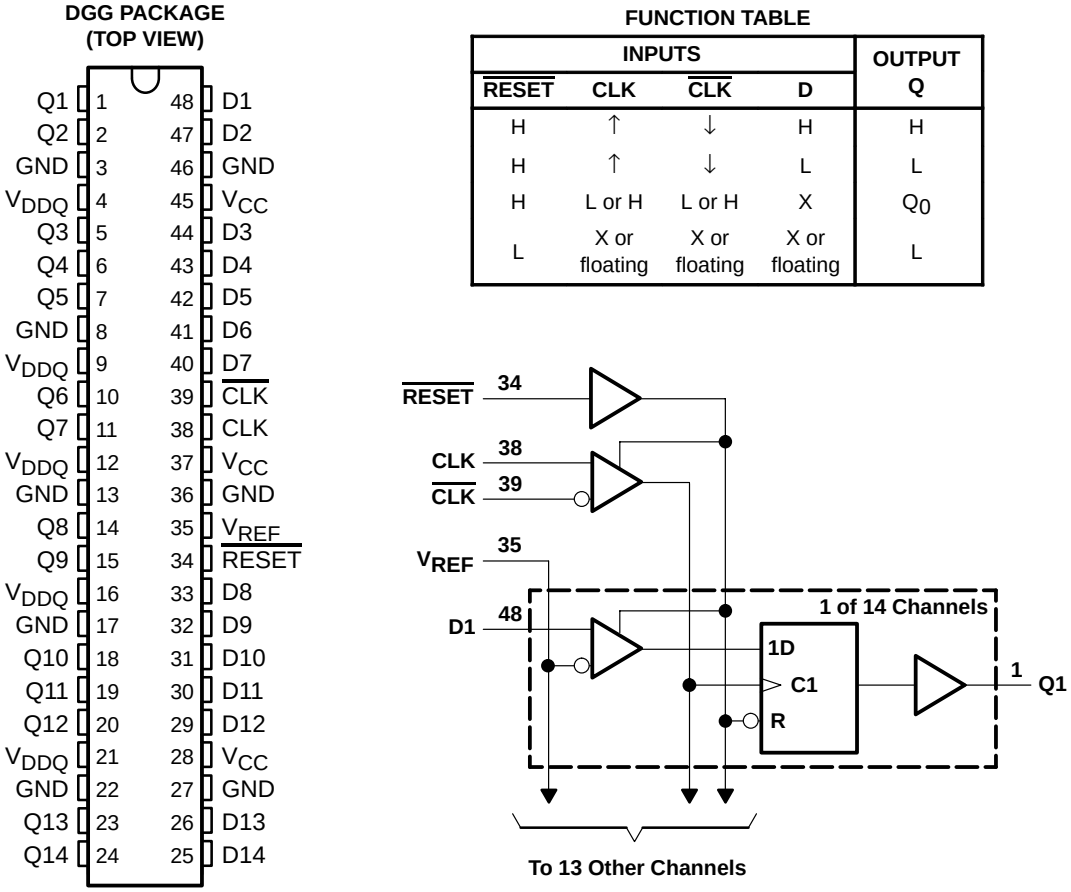


Figure 3. Function Table, Pinout, and Logic Diagram of the SSTV16857

The SSTV16857 is characterized and specified using the JEDEC-defined test load (see Appendix A). However, the test load is a lumped resistor-capacitor (RC) network, which differs significantly from the distributed RDIMM load. While the JEDEC-defined test load is a terminated one, the actual RDIMM application load is unterminated. Consequently, TI developed the SN74SSTVF16857 device, with outputs optimized and designed to drive a planar RDIMM load.

The SN74SSTVF16857 is package, pinout, and functionally compatible with the JEDEC-standard SSTV16857. The principal design differences between the two devices are:

- The SSTVF16857 has edge-control output circuitry, while the SSTV16857 has standard SSTL_2 totem-pole output drivers.
- The SSTVF16857 is designed for the required (less) SSTL_2 Class I drive strength needed for the unterminated RDIMM environment, while the SSTV16857 is designed for the SSTL_2 Class II drive strength. The JEDEC specification for SSTL_2 defines the input and output specifications and ac test conditions for devices that are designed to operate in the SSTL_2 logic switching range, nominally 0 V to 2.5 V. The output is defined for a terminated load. According to the JEDEC specification, there are two different classes of SSTL_2, Class I and Class II. Currently, conventional SSTV devices operate using Class II. The SSTVF16857 device employs SSTL_2, Class I. Class I and Class II devices must meet their respective electrical characteristics as defined in the JEDEC standard for *Stub Series Teriminated Logic for 2.5 V (SSTL_2).*[3] These characteristics are summarized in Table 1.
- The SSTVF16857 has improved maximum propagation delay, with no change to the minimum propagation delay, compared to the SSTV16857.

Table 1. Electrical Characteristics for SSTL_2, Class I and Class II Drivers

Parameter		Class I Driver			Class II Driver			Unit
Output supply voltage, V_{DDQ}		2.3	2.5	2.7	2.3	2.5	2.7	V
High-level output	Minimum output current, I_{OH}	–8.1	–8.1	–8.1	–16.2	–16.2	–16.2	mA
	High-level output voltage, V_{OH}	1.74	1.84	1.94	1.94	2.05	2.15	V
Low-level output	Minimum output current, I_{OL}	8.1	8.1	8.1	16.2	16.2	16.2	mA
	Low-level output voltage, V_{OL}	0.56	0.66	0.76	0.36	0.46	0.55	V

The design differences listed above between the SSTV16857 and SSTVF16857 allow the SSTVF16857 to perform better than the SSTV16857 in a planar DDR RDIMM application.

First, the SSTVF16857 outputs have edge-control circuitry to slow down and control the edges of the output signals from the register to the SDRAMs. This results in less undershoot and overshoot of the signal at the SDRAM inputs and minimizes simultaneous-switching noise in the unterminated DDR RDIMM environment. Further, the edge-control circuitry in the SSTVF16857 balances the output high-to-low and output low-to-high edges for better signal integrity and improved eye diagram.

Second, the SSTVF16857 has SSTL_2 Class I drivers needed for the unterminated RDIMM environment, while the SSTV16857 has SSTL_2 Class II drivers. The memory components present an unterminated load to the register and a typical RDIMM could have up to 18 memory loads per output. The SSTVF16857 register is specified with an 8-mA output drive, rather than the 16-mA drive of conventional SSTV products. The 16-mA drive current is too much current for an unterminated load and results in unnecessary ringing on the outputs. Therefore, TI deliberately designed the SN74SSTVF16857 with SSTL_2 Class I outputs that do not exhibit this kind of ringing in the actual application. The result is superior signal integrity.

Further, because the SSTVF16857 outputs are SSTL_2 Class I specified, they drive less current than the SSTV16857 into the net from the register output to the SDRAM input. Consequently, the change in the output drive current with respect to time (dI_O/dt) is reduced for the SSTVF16857 device. This results in lowered output-inductance effects, less output-signal switching noise, and reduced propagation delay push-out due to simultaneous switching, which allows for additional timing margin in the RDIMM system.

The dynamic operating current (I_{CCD} – at each data input) refers to the dynamic current consumed by the device due to the switching of each data input (hence, affecting outputs) and is specified as μA/clock MHz/D input. Although the SN74SSTVF16857 is designed on basically the same process technology as the SN74SSTV16857, the power saving is realized because the SN74SSTVF16857 is a weaker SSTL_2, Class I driver instead of Class II. The SN74SSTVF16857 is 2-μA/Clock MHz/D Input lower than the SN74SSTV16857. This saving adds up when considering that this is a 14-bit device operating at 167 MHz. For additional information on power consumption calculations, refer to the TI application report, *Low-Power Support Using Texas Instruments SN74SSTV16857 and SN74SSTV16859 DDR-DIMM Registers.*[4]

Last, the SSTVF16857 has improved maximum propagation delay over the SSTV16857, while maintaining the same minimum propagation delay. The SSTVF16857 is over 600 ps faster than the JEDEC-standard SSTV16857 device in PC2700 RDIMM (DDR-333) applications, during simultaneous switching. In addition to lowering the maximum propagation delays, the SN74SSTVF16857 maintains the minimum propagation delay. This allows the SN74SSTVF16857 to be backward compatible to PC1600 and PC2100 systems. Therefore, the SN74SSTVF16857 is a true drop-in replacement for the SSTV16857.

In conclusion, Table 2 shows a data-sheet comparison between the SSTV16857 and SSTVF16857.

Table 2. Data-Sheet Comparison between SSTV16857 and SSTVF16857

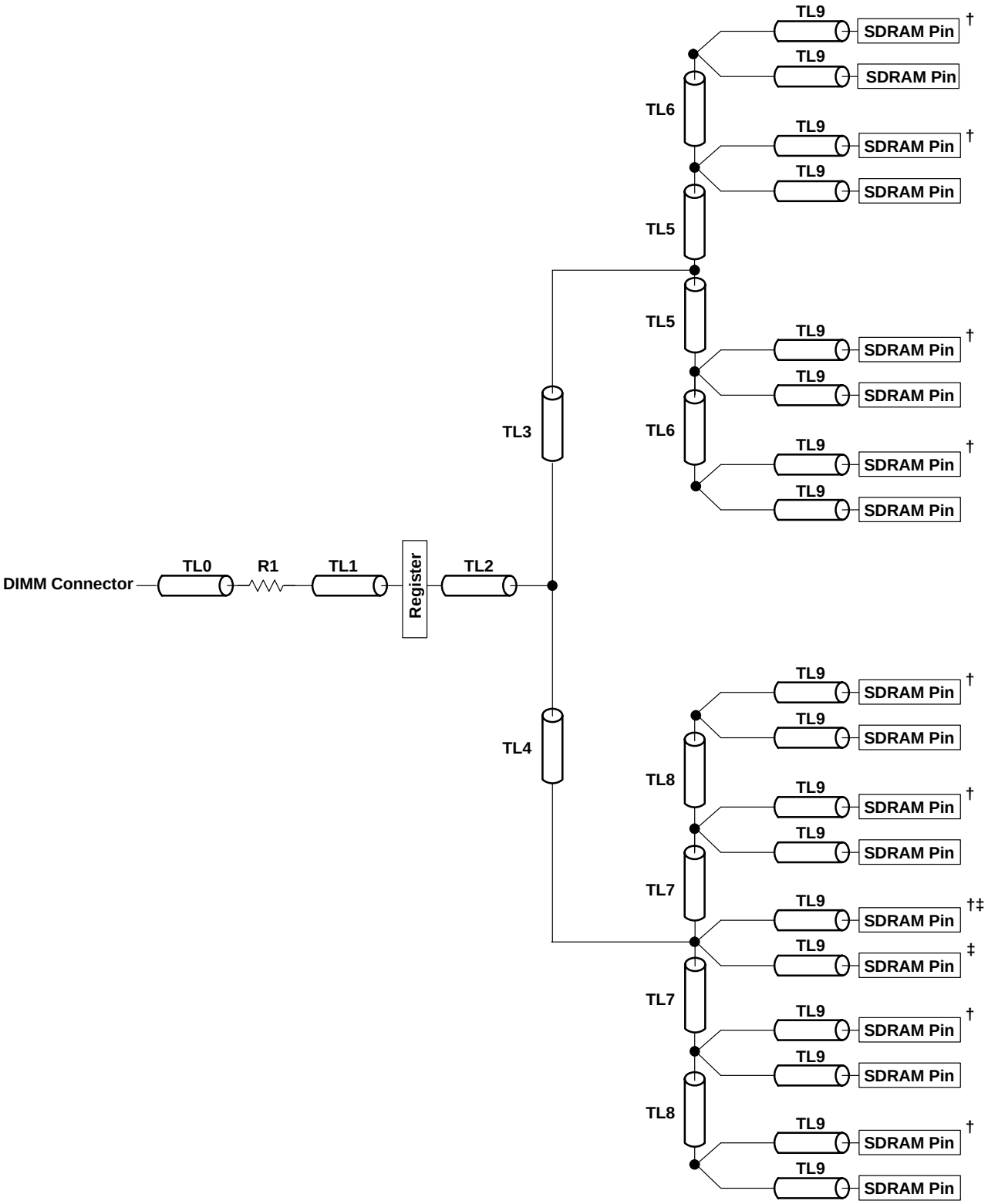
Feature/Parameter	SSTV16857	SSTVF16857
Inputs	SSTL_2	SSTL_2
Outputs	SSTL_2 Class II	SSTL_2 Class I
V_{OH} at 2.3-V V_{CC} (min)	1.95 V (I_{OH} = –16 mA)	1.95 V (I_{OH} = –8 mA)
V_{OL} at 2.3-V V_{CC} (max)	0.35 V (I_{OL} = 16 mA)	0.35 V (I_{OL} = 8 mA)
I_{CC} – Standby (max)	10 μA	10 μA
I_{CC} – Static operating (typ)	8 mA	8 mA
I_{CCD} – Clock only (typ)	28 μA/MHz	28 μA/MHz
I_{CCD} – per each data input (typ)	9-μA/Clock MHz/D Input	7-μA/Clock MHz/D Input
t_{pd} (min)	1.1 ns	1.1 ns
t_{pd} (max)	2.8 ns	2.5 ns

To achieve DDR-333 speeds for planar RDIMM applications, the SN74SSTVF16857 drives 18 loads per output, while closing timings at 167 MHz. The JEDEC-standard SSTV16857 is specified for a maximum propagation delay of 2.8 ns. This is too slow to close timings on an 18-load PC2700 RDIMM application. Therefore, the SN74SSTVF16857 was not only specifically designed into the RDIMM load, but the maximum propagation delay also was decreased to 2.5 ns. The combination of decreased simultaneous switching effects, faster t_{pd}, and improved signal integrity allows the SN74SSTVF16857 to achieve PC2700 speeds without making changes to the PC1600 and PC2100 Raw Card versions A, B, L, or M discussed in this application report.

4 Application Information

The SN74SSTVF16857 is intended for use in PC1600, PC2100, and PC2700 planar DDR SDRAM RDIMMs. In these applications, Raw Card versions A and L RDIMMs with one rank of ×8 SDRAMs presents the lightest load for the register outputs. Raw Card versions A and L RDIMMs, with two ranks of ×8 SDRAMs and the Raw Card versions B and M RDIMMs with one rank of ×4 SDRAMs, presents the heaviest load for the register outputs. Therefore, an evaluation of the register's operation in the Raw Card version L RDIMM (one rank of ×8 SDRAMs) and the Raw Card version M RDIMM reveals a broad range of performance for the register.

The SN74SSTVF16857 and SN74SSTV16857 were simulated in the Raw Card version L RDIMM (one rank of ×8 SDRAMs) and Raw Card version M RDIMM (one rank of ×4 SDRAMs) and the performances were evaluated. Figure 4 shows a typical address net structure for Raw Card versions L and M, into which the registers were simulated. The timing measurements include the net delay from the output of the register to the input of the SDRAM.



† These SDRAM loads will be removed in the single bank of ×8-based DIMM designs.
‡ ×64 based DIMMs. Raw Card version M will remove the two center SDRAMs of the bottom block.

Figure 4. Routing for Address/Command Net Structures (Raw Card Versions L and M)

Table 3 shows the results from simulating the SSTV16857 and SSTVF16857 into the one rank of ×8 SDRAMs Raw Card version L RDIMM application load. The simulation results are for single-bit switching, using the strong register models. The results indicate that the rising and falling edges from the SSTVF16857 device are more balanced than that for the SSTV16857 device.

Table 3. Simulation Results Into Raw Card Version L (9 Loads) Application Loads

Parameter		SSTV16857	SSTVF16857	Unit
t_{PLH}	Measured from the crossing of CLK going high and $\overline{CLK}$ going low at the register clock inputs to the transitioning of the register output signal at the SDRAM input	2.43	1.98	ns
t_{PHL}		2.26	2.09	ns

From the simulation evaluation, the SSTVF16857 is 340 ps faster (worst-case high-to-low and low-to-high) in the one rank of ×8 SDRAMs Raw Card version L RDIMM application than the SSTV16857 device, during single-bit switching.

Table 4 shows the results from simulating the SSTV16857 and SSTVF16857 into the Raw Card version M RDIMM application load. The simulation results are for simultaneous switching, using the weak register models. Even into the heavier Raw Card version M load, the results indicate that the rising and falling edges from the SSTVF16857 device are more balanced than that for the SSTV16857 device.

Table 4. Simulation Results Into Raw Card M (18 Loads) Application Loads

Parameter		SSTV16857	SSTVF16857	Unit
t_{PLH} (SS)	Measured from the crossing of CLK going high and $\overline{CLK}$ going low at the register clock inputs to the transitioning of the register output signal at the SDRAM input	4.8	4.01	ns
t_{PHL} (SS)		3.73	4.16	ns

From the simulation evaluation, the SSTVF16857 is 640 ps faster (worst case high-to-low and low-to-high) in the Raw Card version M RDIMM application than the SSTV16857 device, during simultaneous switching.

The speed advantage achieved with the SN74SSTVF16857 allows the device to be used in PC2700 RDIMM applications. Table 5 describes a post-register timing budget for a typical DDR PC2700 RDIMM. This method measures time from the crossing of the rising edge of CLK and the falling edge of $\overline{CLK}$ at the register clock inputs to the command/address bus signal switching at the SDRAM input. The t_{pdm} values include the timing into the post-register RDIMM net and the SDRAM load. Therefore, $t_{NETDELAY}$ is not included in the calculation. For the setup case, the t_{pdm} number includes the simultaneous-switching effect. Hence, t_{SS} also is not included in the calculation.

Table 5. PC2700 Timing Budget Analysis With the SSTV16857 and SSTVF16857

Symbol	Parameter	Time (ns)			
		SSTV16857		SSTVF16857	
		Setup	Hold	Setup	Hold
t_{CLK}	Clock cycle time	6	N/A	6	N/A
t_{pdm}†	Maximum time for the signal to exit the register	–4.8	2.26	–4.16	1.98
$t_{NETDELAY}$	Maximum time for the signal to propagate from the register to any SDRAM. The switching point for a rising edge is $V_{REF} \pm 100$ mV.	Included in simulation	Included in simulation	Included in simulation	Included in simulation
t_{REG}	Shift in the register clock in relationship to the SDRAM. The input clocks to the registers and the SDRAM are intended to track, but some error is likely.	–0.1	–0.1	–0.1	–0.1
t_{IS}	Setup time required for the SDRAM inputs	–1.1	N/A	–1.1	N/A
t_{IH}	Hold time required for the SDRAM inputs	N/A	–1.1	N/A	–1.1
t_{skew}	Clock jitter and skew on the RDIMM	–0.275	–0.2	–0.275	–0.2
t_{SS}	Simultaneous switching effect	Included in simulation	N/A	Included in simulation	N/A
t_{xTALK}	Crosstalk adder	–0.1	N/A	–0.1	N/A
Margin		**–0.375**	**0.86**	**0.265**	**0.58**

† Measured from the crossing of the rising edge of CLK and the falling edge of $\overline{CLK}$ at the register clock inputs to the signal switching at the SDRAM input.

Accordingly, Table 5 shows that the SSTV16857 does not meet the PC2700 application timing requirements. With the SSTV16857, the timing budget has a negative setup time. However, the SSTVF16857 meets and exceeds the PC2700 application requirements, with a margin of 265 ps (setup) and 580 ps (hold).

In addition to meeting the timing requirements, memory-module designers often are concerned with the performance of a register and the signal integrity of the output signal at the input of the receiving device when the register's outputs are switched simultaneously. The most common method of assessing this is by observing the impact on a single output when multiple outputs are switched.

The SN74SSTVF16857 was evaluated in the Raw Card version B DDR RDIMM (18 loads), and the results were compared with another DDR register for planar RDIMM applications. On the Raw Card version B DDR RDIMM, the SSTV16857 (designated U11) is wired as shown in Figure 5. Only 11 of the 14 data input pins (D1–D10 and D12) can be switched in the application. The other three inputs (D11, D13, and D14) are hardwired to GND. Therefore, an evaluation of the simultaneous-switching signal-integrity effect and the register's performance in the RDIMM application is with a maximum of 11 outputs switching simultaneously.

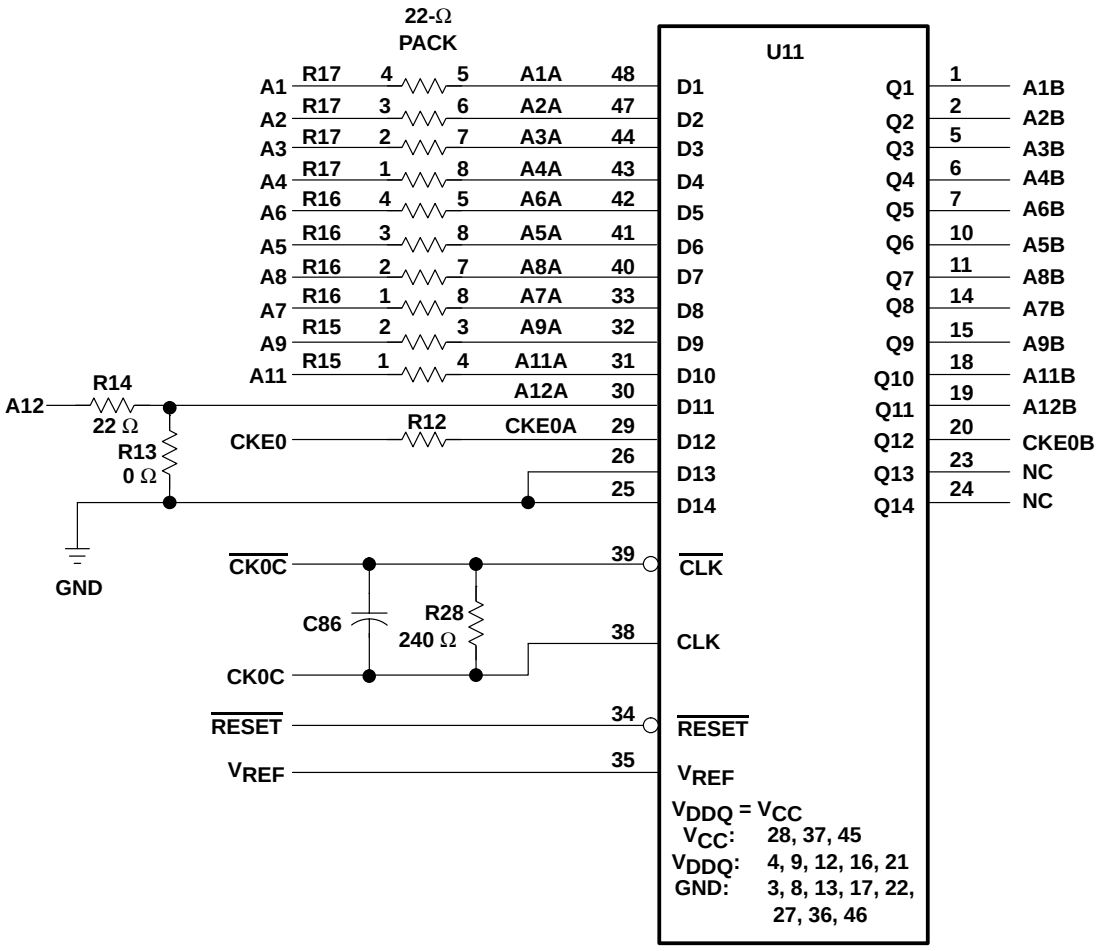


Figure 5. SSTV16857 (U11) as Connected on the Raw Card Version B DDR RDIMM

In the evaluation, three different scenarios were tested.

In the first case, only the A2 (D2 input) signal to the register was switched, and the corresponding A2B (Q2 output) signal from the register was captured at the receiving input of the SDRAM. This assessment was done on two Raw Card version B DDR RDIMMs (18 loads) at DDR-266 speed. One of the two RDIMMs was populated with the SN74SSTVF16857 register and the other RDIMM was populated with a competitor's SSTV16857 register. The results of the registers' output signals, measured at the SDRAM input pin, are shown in Figure 6. The CLK and $\overline{\text{CLK}}$ signals measured at the respective inputs of the register also are shown.

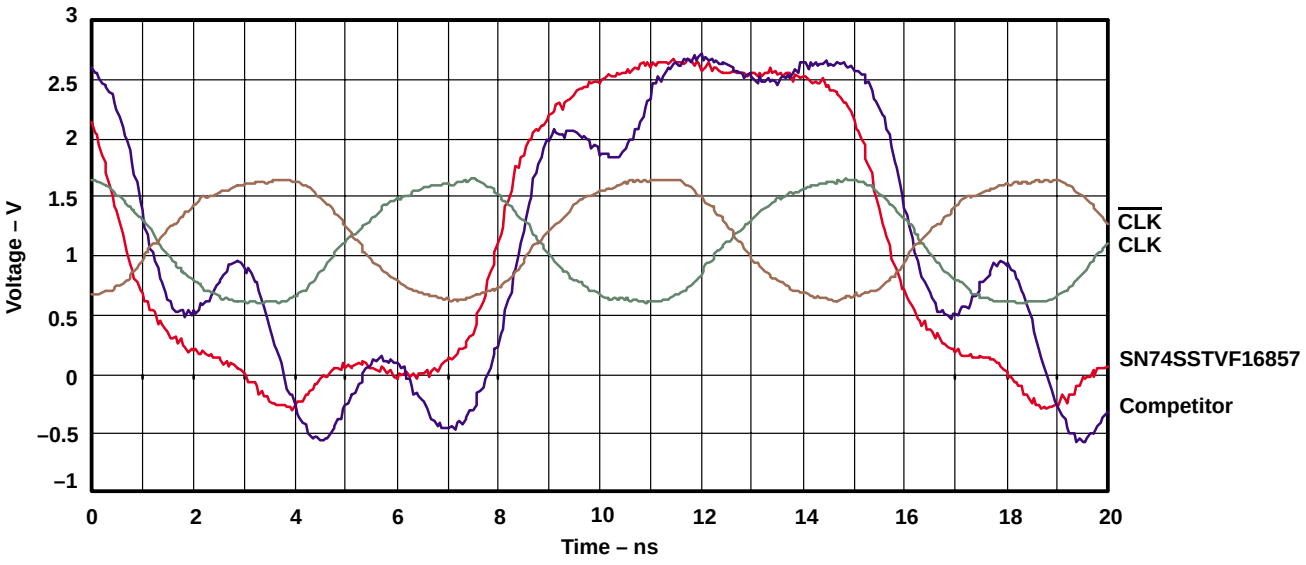


Figure 6. Single-Bit (Q2 Output) Switching Results on Raw Card Version B RDIMM

The results of the test reveals that the Raw Card version B RDIMM, with the SN74SSTVF16857 register, has a single-bit switching propagation delay of 2.85 ns when measured from the crossing of the rising edge of CLK and the falling edge of $\overline{\text{CLK}}$ at the register clock inputs, to the command/address bus signal switching at the SDRAM input. In addition, the SN74SSTVF16857 register is 450 ps faster than the competitor's device in the Raw Card version B RDIMM application, during single-bit switching. Further, the competitor's device exhibits nonmonotonic switching behaviors during the low-to-high and high-to-low transitions, while the SN74SSTVF16857 has no signal reversal during the low-to-high and high-to-low transitions.

In the second evaluation case, 11 of the register's data inputs (D1–D10 and D12) were switched (L to H to L) simultaneously and one of the register's data output signals (A2B) was captured at the receiving input of the SDRAM.

The assessment was done on two Raw Card version B DDR RDIMMs (18 loads) at DDR-333 speed. One of the two RDIMMs was populated with the SN74SSTVF16857 register and the other RDIMM was populated with one other competitor's SSTV16857 register. Results are shown on Figure 7. The CLK and $\overline{\text{CLK}}$ signals measured at the respective inputs of the register also are shown.

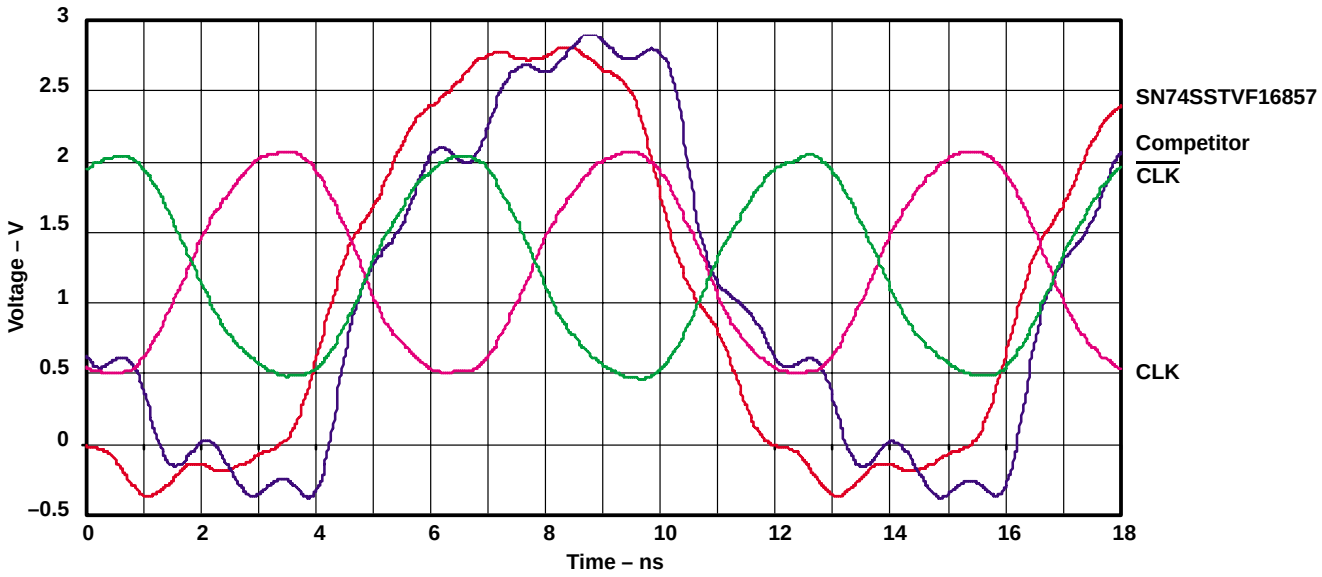


Figure 7. Q2 Output Switching In-Phase (Synchronously) With Ten Other Outputs

In the third evaluation case, ten of the register's data inputs (D1, D3–D10 and D12) were switched simultaneously (L to H to L), and one of the register's data inputs (D2) was switched complementarily (H to L to H) to the other ten switching data inputs. Also, during the third test case, one of the register's data output signals (A2B, which is the corresponding data output signal to the complementary D2 input) was captured at the receiving input of the SDRAM.

The assessment was done on two Raw Card version B DDR RDIMMs (18 loads) at DDR-333 speed. One of the two RDIMMs was populated with the SN74SSTVF16857 register and the other RDIMM was populated with one other competitor's SSTV16857 register. The results are shown in Figure 8. The CLK and $\overline{\text{CLK}}$ signals measured at the respective inputs of the register also are shown.

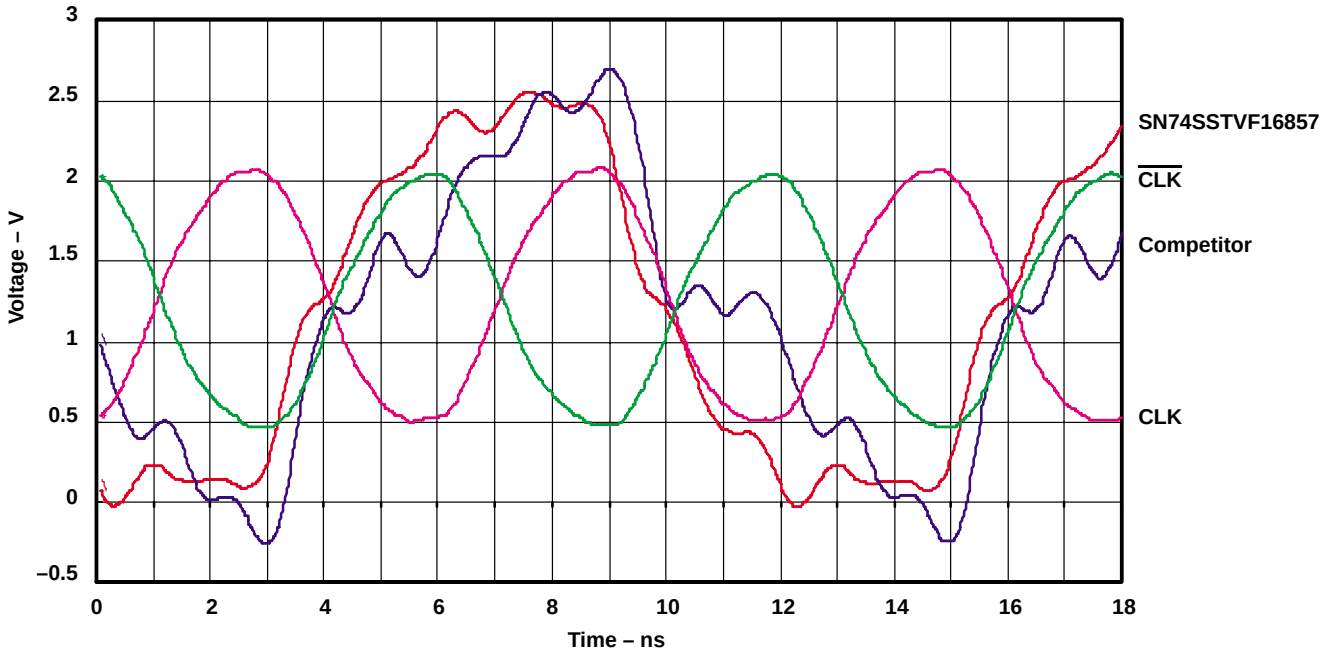


Figure 8. Q2 Output Switching Out-of-Phase (Complementarily) with Ten Other Outputs

The simultaneous-switching results reveal that the SN74SSTVF16857 has more balanced high-to-low and low-to-high edges and superior signal integrity performance than the competitor's offering. While the competitor's device exhibits nonmonotonic switching behaviors at the threshold voltage, during low-to-high and high-to-low transition, the SN74SSTVF16857 has no signal reversal at the threshold region. In addition, the SN74SSTVF16857 is faster than the competitor's device, and the SN74SSTVF16857 minimizes signal-integrity concerns and reduces the need for excess settling time of the output waveform.

5 Features and Benefits

Table 6 summarizes the features and benefits of the SN74SSTVF16857.

Table 6. Features and Benefits of SN74SSTVF16857 Devices

FEATURES	BENEFITS
Improved propagation delay	Provides significant improvements for PC2700 RDIMMs operating at DDR-333 speeds. Over 600-ps faster (simultaneous switching) than the JEDEC-standard SSTV16857
Maintained the same minimum propagation delay as the SSTV16857	Allows backward compatibility to PC1600 and PC2100 RDIMMs
Balanced rising and falling edges on the outputs	Allows for easier system tuning and improved eye pattern at SDRAM receivers
Output edge-control circuitry	Minimizes switching noise in unterminated RDIMM load and provides superior signal integrity for robust memory-module systems
SSTL_2 Class I output drives	Realizes power savings. The SN74SSTVF16857 is 2-μA/Clock MHz/D input in I_{CCD} lower than the SSTV16857, typically.
Pin-to-pin compatible with the SSTV16857	Allows for drop-in replacement for the SSTV16857
Cost	Even though the SN74SSTVF16857 performs better than the SSTV16857 in RDIMM applications, the SN74SSTVF16857 device is cost comparable to the SN74SSTV16857 product.

6 Conclusion

The SN74SSTVF16857 14-bit registered buffer with SSTL_2 inputs and outputs provides simple cost-effective register solutions for PC1600, PC2100, and PC2700 planar RDIMM applications. The SN74SSTVF16857 outputs feature edge-control circuitry to minimize switching noise in the unterminated RDIMM environment, making it over 600 ps faster than the JEDEC-standard SSTV16857 device in PC2700 RDIMM (DDR-333) applications, during simultaneous switching. The characteristics, applications, and performance of the SN74SSTVF16857 in a planar PC2700 RDIMM are discussed in this application report.

7 Frequently Asked Questions (FAQs)

Question 1: *What are SSTVF devices?*

Answer: The SSTVF series of RDIMM register components are enhanced and improved for PC2700 RDIMMs operating at DDR-333 speeds.

Question 2: *How do I get copies of the SN74SSTVF16857 data sheets and samples?*

Answer: The SN74SSTVF16857 data sheets can be obtained by accessing http://logic.ti.com. Samples of the SN74SSTVF16857 device can be obtained by contacting your local TI sales representative.

Question 3: *How do I get copies of SN74SSTVF16857 HSPICE and IBIS models?*

Answer: The HSPICE and IBIS models for SN74SSTVF16857 device can be obtained by accessing http://logic.ti.com.

Question 4: *What are the advantages of using the SN74SSTVF16857 devices?*

Answer: The advantages of using the SN74SSTVF16857 device include:

- Improved propagation delay enables significant improvements for PC2700 RDIMMs operating at DDR-333 speeds. The SN74SSTVF16857 is over 600 ps faster (simultaneous switching) than the JEDEC-standard SSTV16857.
- Maintaining the same minimum propagation delay with the SSTV16857 allows the SN74SSTVF16857 to be backward compatible to PC1600 and PC2100 RDIMMs.
- Balanced rising and falling edges on the outputs allow easier system tuning and improved eye pattern at the SDRAM receivers.
- Improved output edge-control circuitry minimizes switching noise in an unterminated RDIMM load and provides superior signal integrity for robust memory module systems.
- SSTL_2 Class I output drive realizes power savings. The SN74SSTVF16857 is 2-μA/Clock MHz/D input in I_{CCD} lower than the SSTV16857, typically.
- Pin-to-pin compatibility with the SSTV16857 enhances the SN74SSTVF16857 for use as a drop-in replacement for the SSTV16857.

Question 5: *What do PC100, PC133, PC600, PC700, PC800, PC1600, PC2100, and PC2700 stand for?*

Answer: To qualify as PC100, PC133, PC600, etc., a memory module must meet industry standards for use in a particular type of system.

In SDR modules, the numbers that come after the PC refer to the speed of the system's memory data bus. In DDR modules, the numbers that come after the PC refer to the total bandwidth of the module. Here is a short summary of each type:

PC100 DIMM is SDR SDRAM designed for use in systems with a 100-MHz memory data-bus clock speed. It is used in many Pentium™ II, Pentium III, AMD K6-III™, AMD Athlon™, AMD Duron™, and Power Mac G4 systems.

PC133 DIMM is SDR SDRAM designed for use in systems with a 133-MHz memory data-bus clock speed. It is used in many Pentium III B, some Pentium IV, AMD Athlon, and Power Mac G4 systems.

PC600, PC700, and PC800 DIMMs are Rambus™ memory operating at 600-MHz, 700-MHz, and 800-MHz frequencies, respectively. It is used in some Pentium III systems, installed one module at a time, and many Pentium IV systems in identical matched pairs within the same Rambus memory channel.

PC1600 DIMM is DDR designed with DDR-200 SDRAMs and is used in systems with a 200-Mbit/s data rate (100-MHz clock speed) memory data bus. The 1600 refers to the module's bandwidth (the amount of data it can move each second), which is 1.6 Gbyte/s. PC1600 is used primarily in AMD Athlon systems and some Pentium III and Pentium IV systems.

PC2100 DIMM is DDR designed with DDR-266 SDRAMs and is used in systems with a 266-Mbit/s data rate (133-MHz clock speed) memory data bus. The 2100 refers to the module's bandwidth (the amount of data it can move each second), which is 2.1 Gbyte/s. PC2100 is used primarily in AMD Athlon systems and some Pentium III and Pentium IV systems.

PC2700 DIMM is DDR designed with DDR-333 SDRAMs and is used in systems with a 333-Mbit/s data rate (167-MHz clock speed) memory data bus. The 2700 refers to the module's bandwidth (the amount of data it can move each second), which is 2.7 Gbyte/s. PC2700 is used primarily in AMD Athlon systems and some Pentium III & Pentium IV systems.

8 References

1. *Application of the SN74SSTV32852 in Stacked, Low-Profile (1U) PC-1600/2100 DIMMs*, application report, literature number SCEA025.
2. JEDEC, *PC2100 and PC1600 DDR SDRAM Registered DIMM Design Specification, (JEDEC Standard No. 21-C) Revision 1.3*, January 2002.
3. JEDEC, *Stub Series Terminated Logic for 2.5 V (SSTL_2),* JESD8-9B, May 2002.
4. *Low-Power Support Using Texas Instruments SN74SSTV16857 and SN74SSTV16859 DDR-DIMM Registers*, application report, literature number SCEA020.

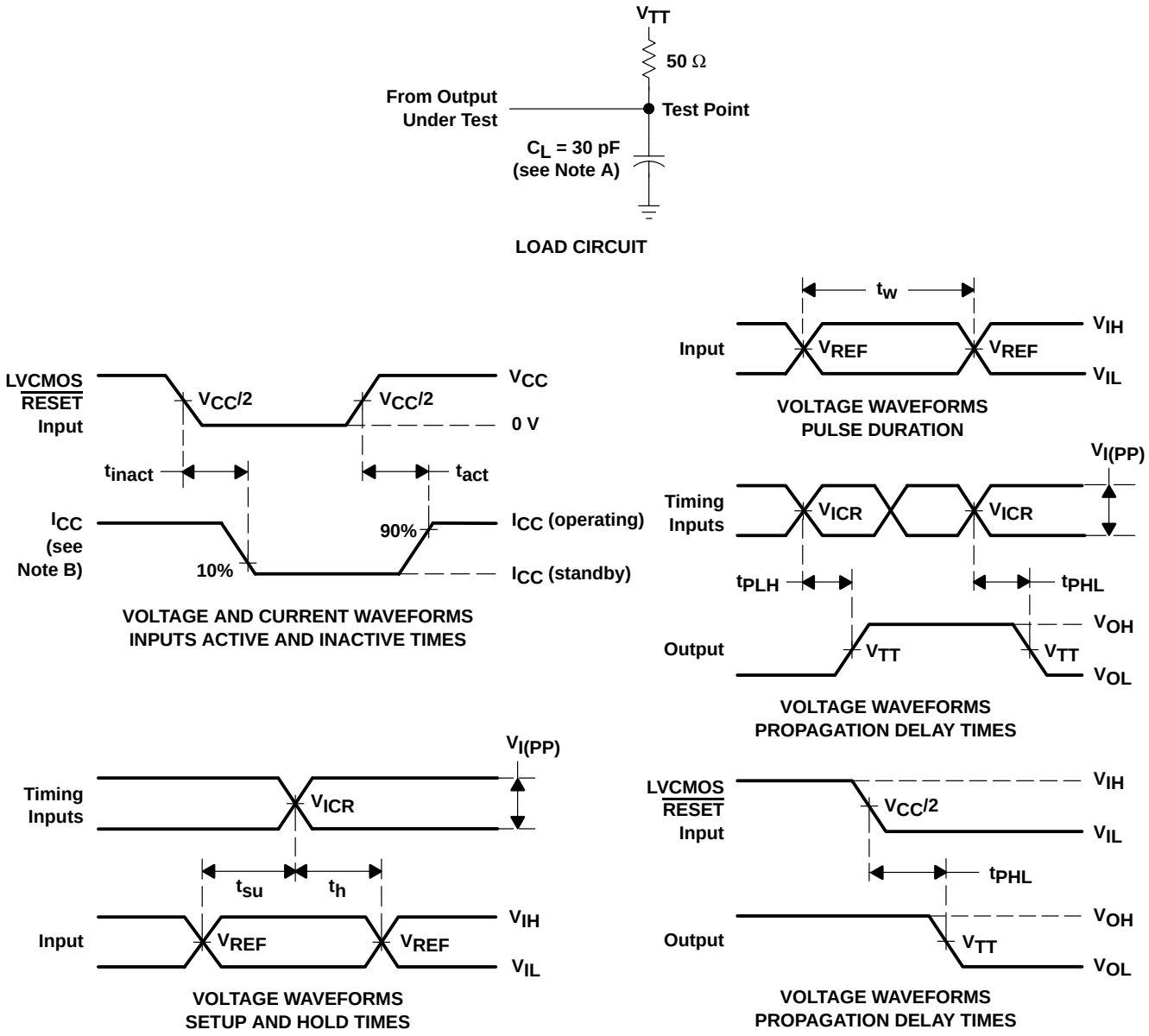
9 Glossary

1U	Low profile–1 unit of telecommunication equipment rack height
CK	Positive line of the differential pair of clock input signals that drives into the DIMM
$\overline{CK}$	Negative line of the differential pair of clock input signals that drives into the DIMM
CLK	Positive line of the differential pair of clock input signals that drives into the register (all register data inputs are sampled on the rising edge of their associated clocks)
$\overline{CLK}$	Negative line of the differential pair of clock input signals that drives into the register
DDR	Double data rate
DDR-200	A speed grade for DDR SDRAM devices. The nominal operating (clock) frequency of such devices is 100 MHz. Therefore, although the devices operate over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 100-MHz clock frequency. The corresponding nominal data rate is 200 MHz.
DDR-266	A speed grade for DDR SDRAM devices. The nominal operating (clock) frequency of such devices is 133 MHz. Therefore, although the devices operate over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 133-MHz clock frequency. The corresponding nominal data rate is 266 MHz.
DDR-333	A speed grade for DDR SDRAM devices. The nominal operating (clock) frequency of such devices is 166.7 MHz. Therefore, although the devices operate over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 166.7-MHz clock frequency. The corresponding nominal data rate is 333 MHz.
DIMM	Dual in-line memory module
DLL	Delay locked loop
EEPROM	Electrically erasable programmable read-only memory
IBIS	I/O buffer information specification (http://www.eigroup.org/ibis)
IC	Integrated circuit
I_{CC}	Power-supply current consumption
I_{CCD}	Dynamic power-supply current consumption
JEDEC	Joint Electron Device Engineering Council (http://www.jedec.org)
LFBGA	Low-profile fine-pitch ball grid array

PC1600	JEDEC standard DIMMs using DDR-200 SDRAM devices
PC2100	JEDEC standard DIMMs using DDR-266 SDRAM devices
PC2700	JEDEC standard DIMMs using DDR-333 SDRAM devices
PLL	Phase lock loop, also know as zero-delay clock buffer
rank	A DIMM rank is the external physical bank of SDRAMs on the DIMM, formally referred to as a bank. Not to be confused with the SDRAM internal memory bank, the external physical bank is now referred to as a rank. While the SDRAM memory bank is selected using the bank address (BA0, BA1) signals on the DIMM, the DIMM rank is selected using the chip-select ($\overline{CS0}$, $\overline{CS1}$) signals on the DIMM.
RC	Resistor-capacitor network
RDIMM	Registered dual in-line memory module
SDR	Single data rate
SDRAM	Synchronous dynamic random-access memory (JEDEC-standard memory IC)
SSTVF16857	JEDEC-standard 2.5-V 14-bit to 14-bit registered buffer with SSTL_2 inputs and outputs for DDR RDIMM applications
SPD	Serial presence detect EEPROM
SPICE	Simulation program with integrated circuit emphasis
SSTL_2	2.5-V stub series-terminated logic, JEDEC-specified power-supply and interface-level standard
t_f	Fall time. The time interval between two reference points (20% and 80%, unless otherwise specified) on a waveform that is changing from the defined high level to the defined low level
TI	Texas Instruments (http://www.ti.com)
TSSOP	Thin shrink small-outline package
t_{pd}	Propagation delay time. The time between the specified reference points on the input and output voltage waveforms, with the output changing from one defined level (high or low) to the other defined level (t_{pd} = t_{PHL} or t_{PLH})
t_{pdm}	Maximum propagation delay time for the signal to exit the register, measured from the timing input reference to the output signal at the SDRAM input.
t_{PHL}	Propagation delay time, high-to-low level output. The time between the specified reference points on the input and output voltage waveforms, with the output changing from the defined high level to the defined low level.

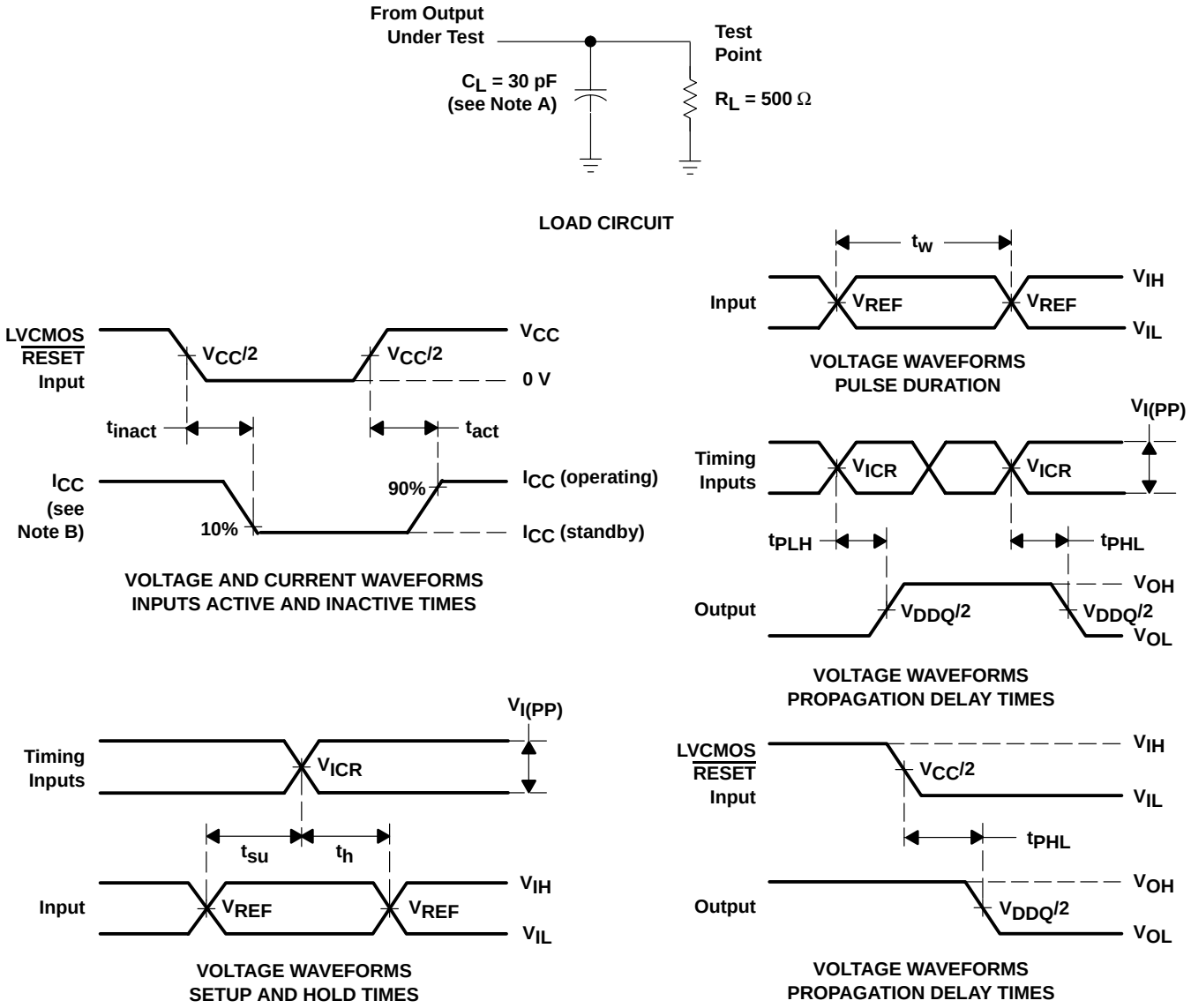
t_{PLH}	Propagation delay time, low-to-high level output. The time between the specified reference points on the input and output voltage waveforms, with the output changing from the defined low level to the defined high level
t_r	Rise time. The time interval between two reference points (20% and 80%, unless otherwise specified) on a waveform that is changing from the defined low level to the defined high level
V_{OH}	High-level output voltage. The voltage at an output terminal with input conditions applied that, according to product specification, establishes a high level at the output.
V_{OL}	Low-level output voltage. The voltage at an output terminal with input conditions applied that, according to product specification, establishes a low level at the output.

Appendix A. Parameter Measurement Information



NOTES: A. C_L includes probe and jig capacitance.
B. I_{CC} tested with clock and data inputs held at V_{CC} or GND, and I_O = 0 mA.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, input slew rate = 1 V/ns ±20% (unless otherwise noted).
D. The outputs are measured one at a time with one transition per measurement.
E. $V_{TT} = V_{REF} = V_{DDQ}/2$
F. $V_{IH} = V_{REF}$ + 310 mV (ac voltage levels) for differential inputs. $V_{IH} = V_{CC}$ for LVCMOS input.
G. $V_{IL} = V_{REF}$ – 310 mV (ac voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 9. SSTV16857 Load Circuit and Voltage Waveforms



NOTES:
A. C_L includes probe and jig capacitance.
B. I_{CC} tested with clock and data inputs held at V_{CC} or GND, and I_O = 0 mA.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, input slew rate = 1 V/ns ±20% (unless otherwise noted).
D. The outputs are measured one at a time with one transition per measurement.
E. $V_{REF} = V_{DDQ}/2$
F. $V_{IH} = V_{REF}$ + 310 mV (ac voltage levels) for differential inputs. $V_{IH} = V_{CC}$ for LVCMOS input.
G. $V_{IL} = V_{REF}$ – 310 mV (ac voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 10. SSTVF16857 Load Circuit and Voltage Waveforms

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