Application Report
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Common Risks of Discrete FET Voltage Translation and Advantages of TI's Integrated 2N7001T Level Shifter

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ABSTRACT

Discrete Field Effect transistors (FET) are commonly considered for level translation. This application note provides an overview of the common discrete push-pull level shifter implementations and the potential drawbacks. Finally, the 2N7001T solution from TI is discussed to show how the discrete level shifter implementation drawbacks are overcome.

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Trademarks

1 Introduction

Texas Instruments' voltage translation devices can be categorized into three major families: unidirectional, direction-controlled bidirectional, and the auto-bidirectional.

Unidirectional translators are designed to facilitate a one-way communication between a host and a peripheral device. Popular related devices include SN74AUP1T34, SN74LV1T34, SN74AUP1T57, SN74AVC2T244, and the new 2N7001T solution.

Direction controlled translators contain one or more direction control pins that allow the directional flow of the data lines to be manually configured. Popular device families include LVC, AVC, and the newly released AXC.

Auto-bidirectional translators are designed for communication interfaces with bidirectional data lines, and do not require any additional external control signals to manage the direction flow of data. Common device families for auto-bidirectional translators include TXS, TXB, and LSF.

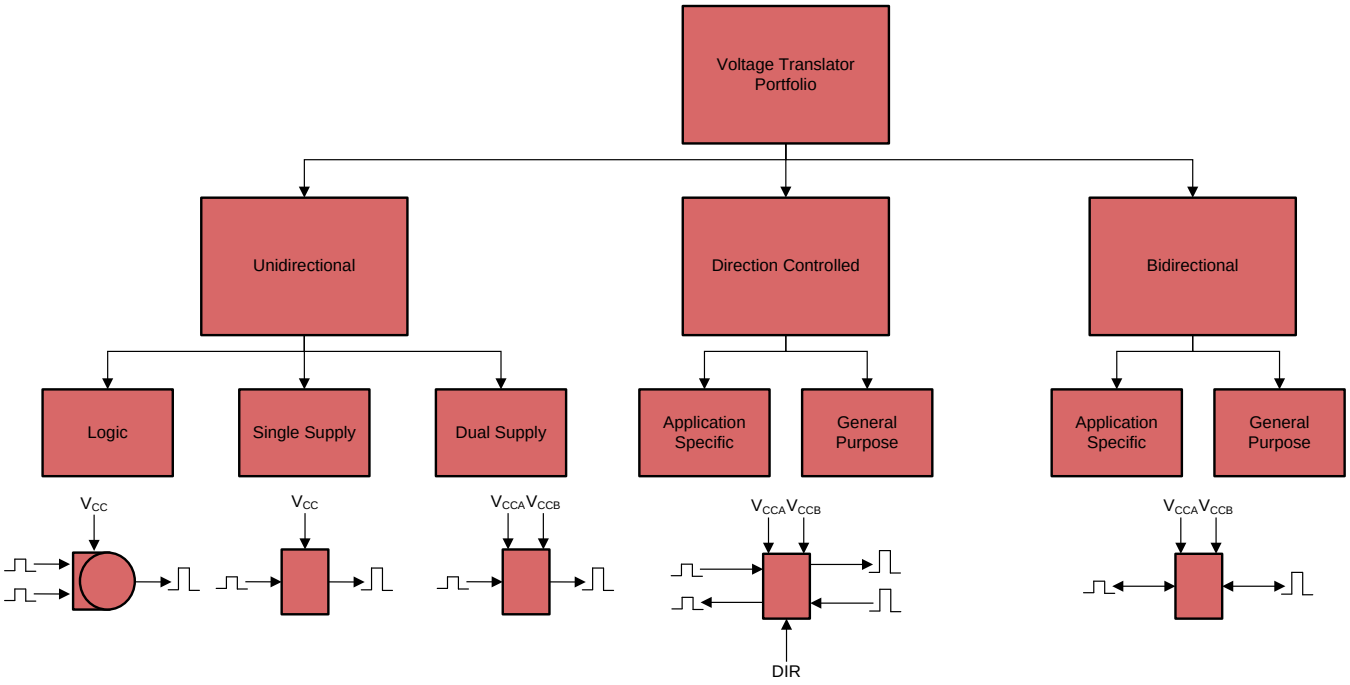

Figure 1. Texas Instruments Voltage Translation Portfolio

2 2N7001T: Unidirectional Level Shifter

Figure 2 shows TI's 2N7001T device which is a low-power single channel unidirectional level shifter with configurable dual power supply rails that operate from 1.65 V to 3.6 V. The device is fully specified for I_{off} partial power-down applications. The device provides ESD (electrostatic discharge) protection on all the pins along with an ambient temperature support range from –40°C to +125°C .

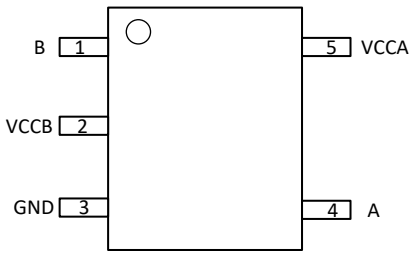

Figure 2. 2N7001T DCK Package

3 Discrete Implementation Comparison

3.1 NMOS Implementation

Figure 3 shows the discrete level shifter implementation using NFET (N-channel Field Effect Transistor) and two resistors. Table 1 lists the common design considerations for the NMOS solution.

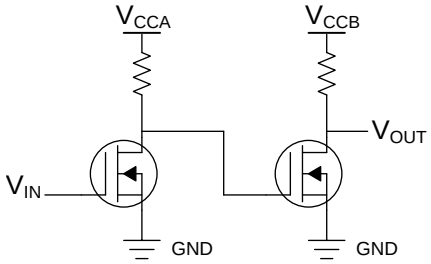

Figure 3. NMOS Solution

Table 1. Design Considerations For NMOS Solution vs 2N7001T

DESIGN CONSIDERATIONS	NMOS SOLUTION	2N7001T
Speed	Higher speed requires lower PU resistors. This increases current consumption.	No speed vs power trade off; Higher data rate is supported because of the active drive structure.
Power Consumption	Lower power requires higher pull-up resistors resulting in lower speed.	No power vs speed trade-off; Low-power and low leakage is due to dual supplies and push-pull structure.
Ease of Use	Multiple components increase both the debugging time and probability of failure.	A single component reduces the probability of failure and reduces the debugging time.
Solution Size	Solution size is larger than TI Solution.	The solution size is compact, and it is easy to debug. Leaded (DCK) and non-leaded packages (DPW) are available.
Vcc isolation	No Vcc isolation. When the power supply is at 0V, the IO pins are not in Hi-Z.	Turning off either supply places the IO pins in high impedance (Hi-Z). This results in power savings.
ESD protection	There is no built-in ESD protection.	The ESD ratings are 2-kV HBM and 1-kV CDM.
Rise/Fall time	The rising edges are slow due to the RC charging time.	The rise and fall time is fast because of the push pull structure. Hence, the systems downstream does not have issues with slow rising edges. For more information, see the *Solving CMOS Transition Rate Issues* white paper.
Power sequencing	Supply sequencing may be required. Glitches may occur while power sequencing.	Supply sequencing is not required. Glitches may occur while power sequencing.
Fab and Assembly	Multiple components increase the manufacturing time and cost.	A single component reduces the manufacturing time and cost.

An example for the rise time analysis, a simulation of NMOS structure using an open drain buffer, and the 2N7001T device was done as shown in Figure 4. The open drain output with a pull-up resistor of 1-kOhm driving a 30-pF cap load resulted in a rise time of about 73ns as shown in Figure 5. Using the 2N7001T to drive the same 30-pF cap load, resulted in 2.3ns rise time as shown in Figure 6. The application note *Implications of Slow Floating CMOS* explains the effects of slow rising edge inputs to a CMOS system.

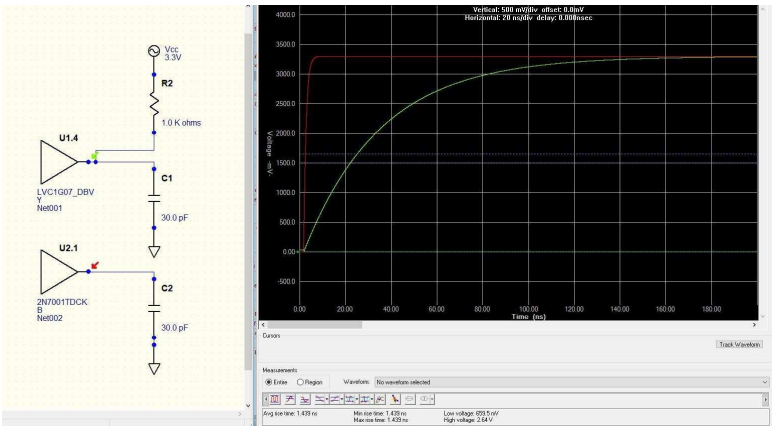

Figure 4. HyperLynx Simulation of Open drain buffer and 2N7001T

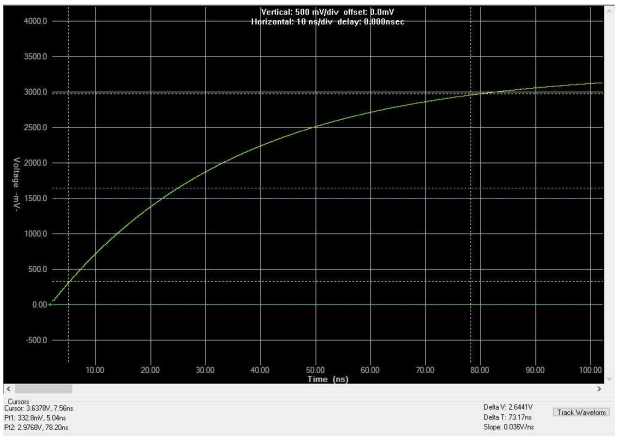

Figure 5. 73ns Rise time for an Open Drain buffer

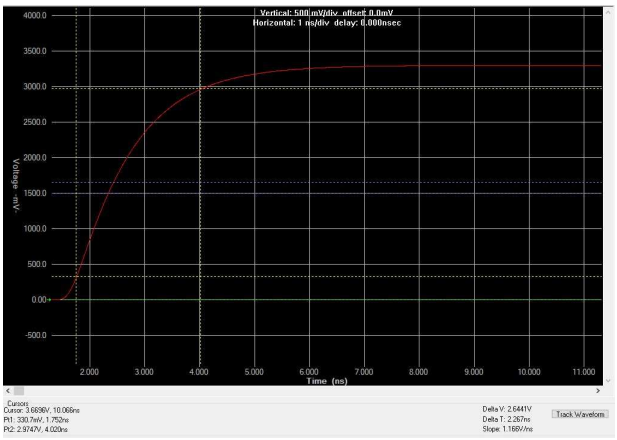

Figure 6. 2.2ns Rise time for 2N7001T

3.2 BJT Implementation

BJT (Bipolar Junction Transistor) based discrete implementation uses NPN transistors, and the accompanying resistor network for level translation as shown in theFigure 7. Table 2 lists the common design considerations for the BJT solution.

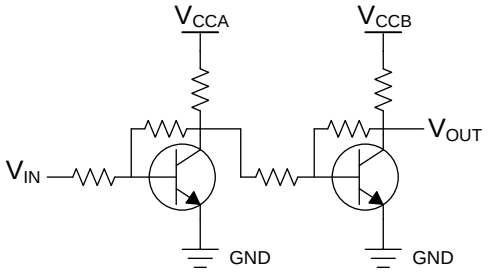

Figure 7. BJT Solution

Table 2. Design Considerations For BJT Solution vs 2N7001T

DESIGN CONSIDERATIONS	BJT SOLUTION	2N7001T
Speed	The speed is higher compared to CMOS. However, speed is limited by the pull-up resistors.	The speed is fast because of the active drive structure.
Power Consumption	With the BJT solution, the leakage current is very high.	Low-power and low leakage is due to dual supplies and push-pull structure.
Ease of Use	Multiple components increase both the debugging time and probability of failure.	A single component reduces the probability of failure and reduces the debugging time.
Solution Size	Solution size is larger than TI Solution.	The solution size is compact, and it is easy to debug. Leaded (DCK) and non-leaded packages (DPW) are available.
Vcc isolation	No Vcc isolation. When the power supply is at 0V, the IO pins are not in Hi-Z.	Turning off either supply places the IO pins in high impedance (Hi-Z). This results in power savings.
ESD protection	There is no built-in ESD protection.	The ESD ratings are 2-kV HBM and 1-kV CDM.
Rise/Fall time	The rising edges are slow due to the RC charging time.	Fast rising and falling edges because of the push pull structure. Hence, the systems downstream does not have issues with slow rising edges. For more information, see the *Solving CMOS Transition Rate Issues* white paper.
Power sequencing	Supply sequencing maybe required. Glitches may occur while power sequencing.	Supply sequencing is not required. Glitches may occur while power sequencing.
Fab and Assembly	Multiple components increase the manufacturing time and cost.	A single component reduces the manufacturing time and cost.

3.3 Push-Pull Implementation

Figure 8 shows a push-pull implementation using the NFET (N-channel Field Effect Transistor) and PFET (P-channel Field Effect Transistor) along with the pull-up resistor network. Table 3 lists the common design considerations for the push-pull solution.

Figure 9 shows the solution size comparison between the push-pull solution and using the 2N7001T solution.

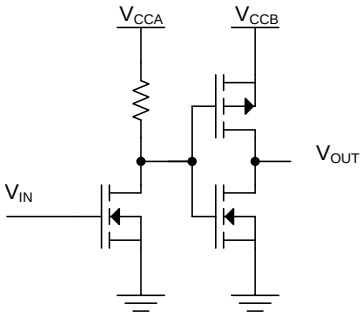

Figure 8. Push-Pull Solution

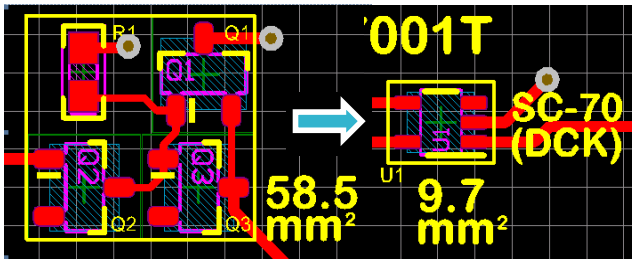

Figure 9. Size Comparison of 2N7001T vs Push-Pull Solution

Table 3. Design Considerations For Push-Pull Solution vs 2N7001T

DESIGN CONSIDERATIONS	PUSH-PULL SOLUTION	2N7001T
Speed	Speed vs power trade off; higher speed requires lower PU resistors. This increases current consumption.	The speed is fast because of the active drive structure.
Power Consumption	Power vs speed trade-off; lower power requires higher pull-up resistors resulting in lower speed.	Low-power and low leakage is due to dual supplies and push-pull structure.
Ease of Use	Multiple components increase both the debugging time and probability of failure.	A single component reduces the probability of failure and reduces the debugging time.
Solution Size	Solution size is larger than TI Solution.	The solution size is compact, and it is easy to debug. Leaded (DCK) and non-leaded packages (DPW) are available.
Vcc isolation	No Vcc isolation. When the power supply is at 0V, the IO pins are not in Hi-Z.	Turning off either supply places the IO pins in high impedance (Hi-Z). This results in power savings.
ESD protection	There is no built-in ESD protection.	The ESD ratings are 2-kV HBM and 1-kV CDM.
Rise/Fall time	Overall, the rise and fall time is quicker. However, due to the pull-up resistor in the initial stage, there may be a large propagation delay (tpd) and other related issues due to a slow rise time.	The rise and fall time is fast because of the push pull structure. Hence, the systems downstream does not have issues with slow rising edges. For more information, see the *Implications of Slow Floating CMOS* application note.
Power sequencing	Supply sequencing may be required. Glitches may occur while power sequencing.	Supply sequencing is not required. Glitches may occur while power sequencing.
Fab and Assembly	Multiple components increase the manufacturing time and cost.	A single component reduces the manufacturing time and cost.

4 Additional Resources

- Texas Instruments, 2N7001TEVM user's guide
- Texas Instruments, 2N7001T sample page
- Texas Instruments, *Introducing the 2N7001T* video
- Texas Instruments, *Implications of Slow Floating CMOS Inputs* application report
- Texas Instruments,*Solving CMOS transition rate issues with Schmitt trigger* white paper

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