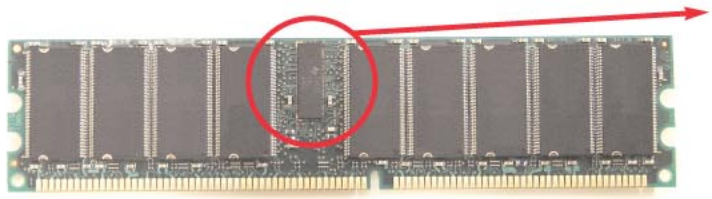
2Q 2002

PC-1600/2100 Stacked Registered DIMM Module



SN74SSTV32852
24:48 Bit Registered Buffer

- Designed for 2.5-V operation
- SSTL_2 compatible I/O's
- Differential Clock Inputs(CLK&/CLK)
- LVCMOS switching levels on /RESET input
- /RESET input disables differential input receivers, resets all registers, and forces all outputs low.
- Pinout optimizes DIMM PCB layout
- Only one device per DIMM is required
- Designed specifically for 1U low-profile DIMM applications
- Samples available
- Production Released

PLL Clock Driver

NAME	CDCV857B	R-DIMM
CDCV857B	+/- 50 ps static phase offset	DDR-333
CDCV857/A	+/- 75 ps static phase offset	DDR 200/266

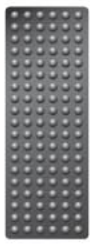
Registered Memory Buffers

NAME	Device Description	R-DIMM
SN74SSTV16857 SN74SSTVF16857	14-Bit Registered Buffer With SSTL_2 Inputs and Outputs	PC-1600/2100/2700
SN74SSTV16859	13-Bit to 26-Bit Registered Buffer with SSTL_2 Inputs and Outputs	PC-1600/2100/2700 Stacked R-DIMM
SN74SSTV32852	24-Bit to 48-Bit Registered Buffer with SSTL_2 Inputs and Outputs	PC-2400/2700 Stacked R-DIMM
SN74SSTV32867	26-Bit Registered Buffer with SSTL_2 Inputs and LVCMOS Outputs	PC-2400/2700
SN74SSTV32877	26-Bit Registered Buffer with SSTL_2 Inputs and Outputs	PC-2400/2700

SSTV16859MLF

128 mm² of total board space is required

Over 31% Space Savings

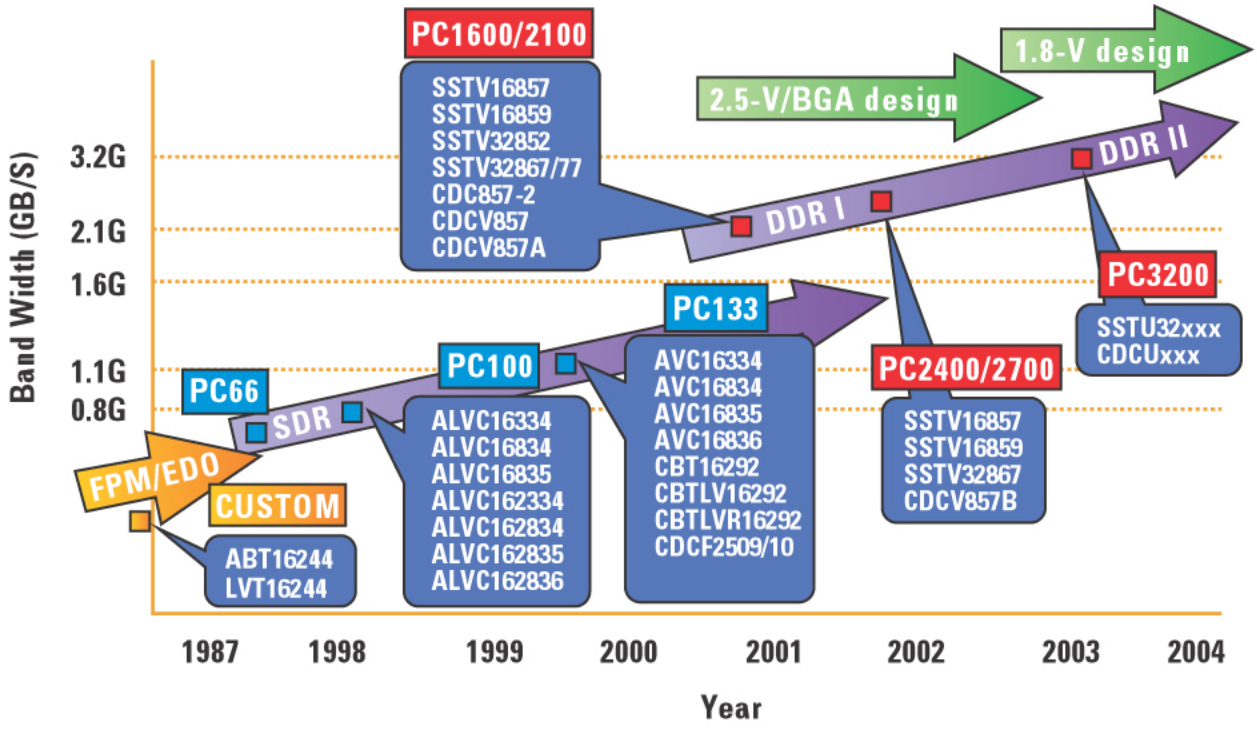


SSTV32852
Only 88 mm² is required

Recommended Registered Buffers

DIMM Configuration	133 MHz PC1600/2100JEDEC 1.7"TSOP DRAMs	133 MHz PC1600/2100 1U Low ProfileTSOP DRAMs	167 MHz PC2700 1U Low Profile BGA DRAMs
1 Bank x8 9 SDRAMs	Raw Card A 2 x SSTV16857 48-pin TSSOP 9 Loads/Output	Raw Card L 2 x SSTV16857 48-pin TSSOP 9 Loads/Output	Raw Card A 2 x SSTV16857 48-pin TSSOP 9 Loads/Output
2 Banks x 8 (18 SDRAMs) 1 Bank x 4 (18 SDRAMs)	Raw Card A/B 2 x SSTV1685748-pin TSSOP 18 Loads/Output	Raw Card L/M 2 x SSTV1685748-pin TSSOP 18 Loads/Output	Raw Card B/C 2 x SSTV16859 64-pin TSSOP 9 Loads/Output
2 Banks x 4 (36 SDRAMs)	Raw Card C 2 x SSTV16859 64-pin TSSOP 18 Loads/Output	Raw Card N 1 x SSTV32852 114-ball LFBGA 18 Loads/Output	Raw Card D In Development

Logic Roadmap for High-Speed Memory Interface



For more information about logic, go to: www.ti.com/sc/logic

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