FIFO Surface-Mount Packages for PCMCIA Applications

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Introduction

As today's applications become more complex and integrated, there is a continuing need to reduce board space without sacrificing functionality. This need has never been greater than for Personal Computer Memory Card International Association (PCMCIA) cards. The appeal for PC card adapters in large area network (LAN) is due to the small form factor and performance. PCMCIA card designers face the challenge of reducing current half-size boards (typically 4.5 in $\times$ 8 in) such as those used in present desktop systems, to the size of a credit card.

With the emergence of notebook computers, personal data assistants (PDAs), and wireless communications, designers are turning to PCMCIA cards to meet the growing demand for more flexibility. This trend has driven the chip-set manufacturers to reduce the number of add-on features normally designed into desktop computers to fit the board confines of portable systems. PCMCIA cards provide an alternative: standard add-on features in a miniature-portable format. Until the introduction and standardization of PCMCIA cards, portable systems were left virtually unconnected to other systems and peripherals. Many of the PCMCIA designs provide the needed interconnectedness between systems by performing input/output (I/O) data functions. Typical I/O adapters found today are EtherNet, faxes, SCSI, and modems, to name a few.

As bus widths and data speeds increase, so does the chance of data bottlenecks and latency. Specialty memories such as FIFOs are required for either rate matching or clock partitioning from data buses and processors. Until now, many designers either had to compromise performance or increase device count due to the lack of PCMCIA-compliant FIFO packaging. Texas Instruments (TI) has met the challenge of reduced board area and increased integration with their advanced FIFO memories. TI offers 9-, 18-, and 36-bit high-performance FIFO memories in the PCMCIA-compatible thin quad flat package (TQFP).

PCMCIA

PCMCIA was founded in 1989 to define and set PC-card standards. In today's market, there are three widely accepted standards: Type I, ratified in June 1990; Type II, ratified in September 1991; and Type III, which is pending. PCMCIA cards all share a common length and width, differing only in their height (see Figure 1).

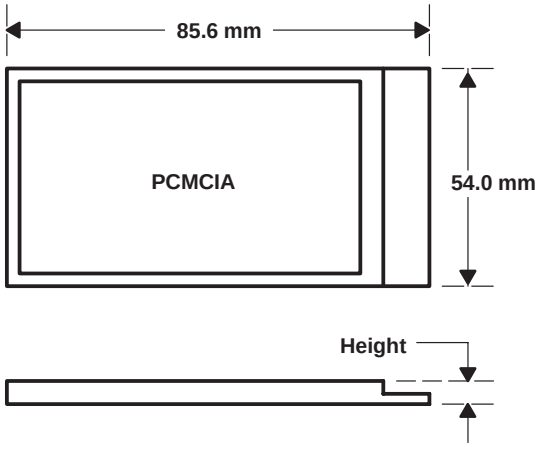
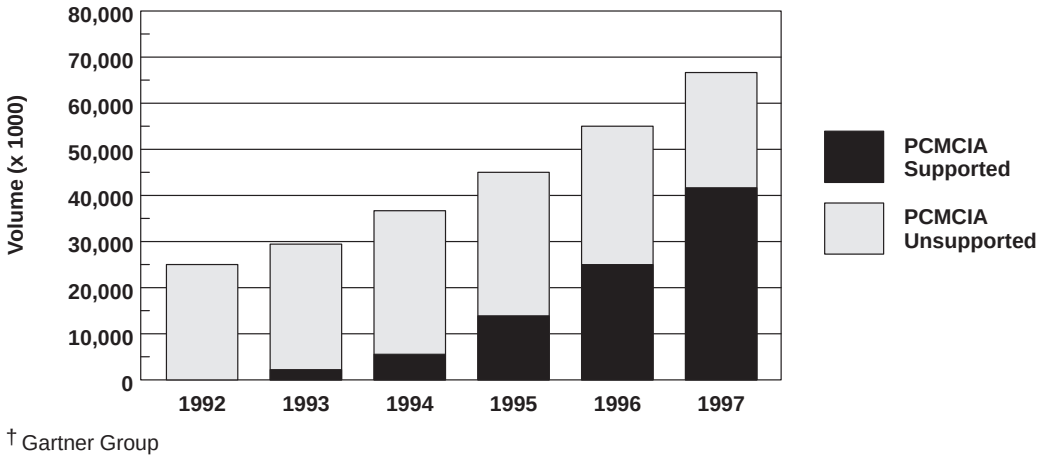


Figure 1. PCMCIA Card Dimensions

Due to the increased popularity of PCs (i.e., laptops, notebooks, and PDAs), a demand for the same functionality as found in larger PC counterparts has arisen. To keep pace with the growing market demand, portable-computer manufacturers have begun to support PCMCIA card ports on nearly all new designs (see Figure 2).



† Gartner Group

Figure 2. Portable Computers Supporting PCMCIA Cards†

In the past, PCMCIA cards were seen as a way to easily upgrade system memory without adding storage overhead to the already compact chip sets. Today, PCs are replacing hardwired-desktop networked systems as the main computing unit. The need to provide for system interconnection and data communications has targeted new PCMCIA designs for LAN, fax, and modem-adapter cards. These applications typically are found in Type II PCMCIA cards. Other designs such as subminiature disk drives and wireless radio frequency communication adapters typically found in Type III PCMCIA cards (see Table 1).

Table 1. PCMCIA Card Applications

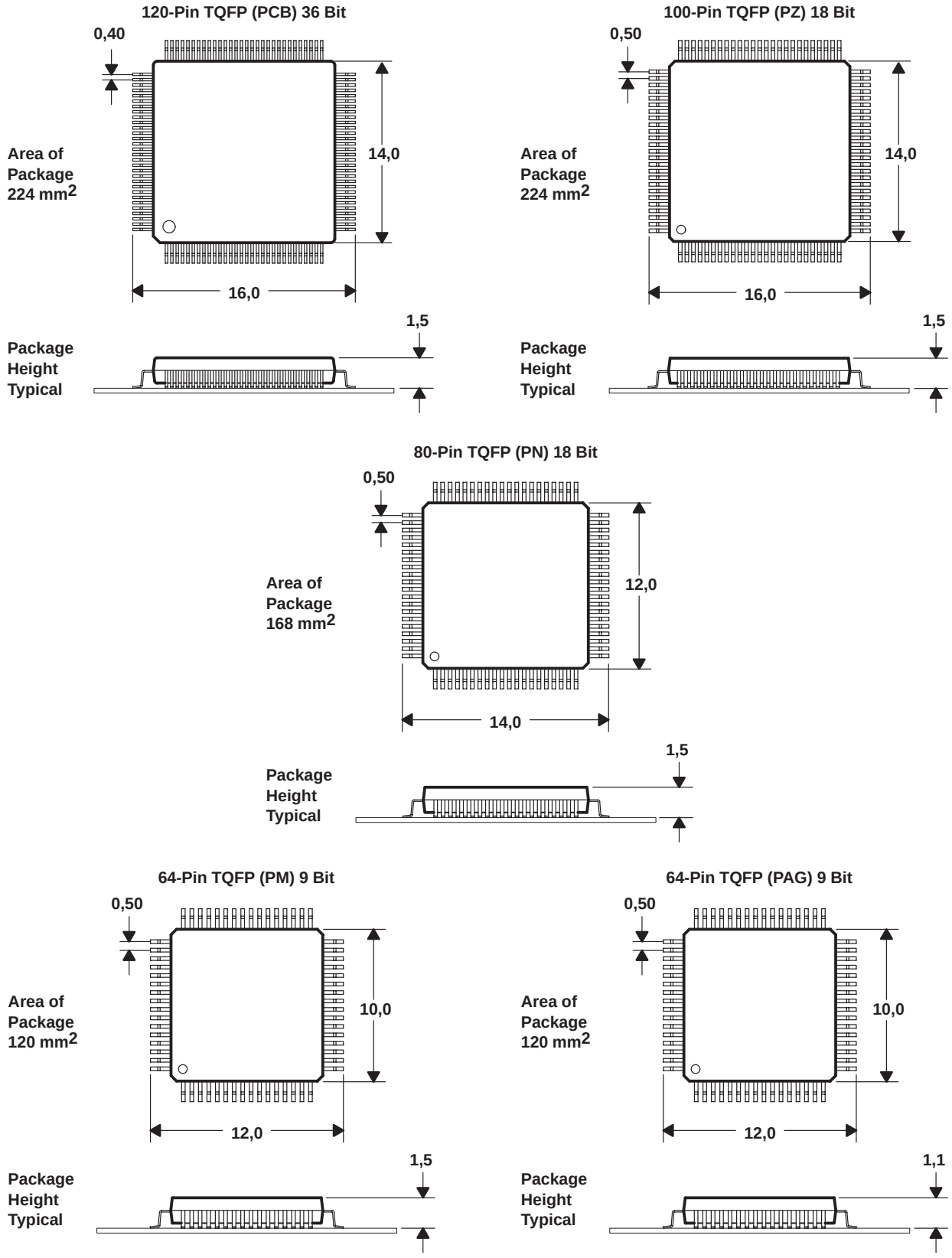
TYPE	HEIGHT	APPLICATION
I PC	3.3 mm	Memory devices: Flash, DRAM, OTP, and high-speed add-ons
II PC	5 mm	I/O devices: Fax, modems, and LAN adapters
III PC	10.5 mm	Wireless devices: RF-communications devices and submini disk drives

Type I cards are focused mainly for plug-in memory. Type II and Type III cards are gaining ground in many new applications. Type II cards are used mainly for I/O applications such as those listed in Table 1. The growing acceptance of PCMCIA cards for I/O interface has caused manufacturers of DSPs, CODECs, bus-interface devices, and ASICs to begin producing PCMCIA-compliant devices. For example, TI's Rio Grande chip set for PCI features ports to support two PCMCIA cards.

There is a demand for these features in a portable package the size of a PCMCIA card and an even greater demand for devices in PCMCIA-compatible packages. These devices must provide the needed features, consume less power, and require less critical board space.

Packaging

The primary obstacle facing many designers is obtaining packages small enough to incorporate into their PCMCIA designs. To shrink a current adapter-card design and have it fit into the small form factor of a PCMCIA card requires all components, not just the printed circuit board, to be reduced in size. To ensure functionality is not lost, many designers implement multilayered boards to help increase integration. Some boards have ten layers and measure only 0.03 in thick. Multilayered boards are only part of the solution; both active and passive components must be dual-side mounted for maximum chip count and overall integration. To ensure the entire board fits into a PCMCIA form requires specialized packaging from the device manufacturers. Since FIFOs play a key role in the functionality of many of these designs, TI has utilized board-space-saving TQFP packaging across 9-, 18-, and 36-bit FIFO product lines (see Figure 3).



NOTE: Dimensions are in millimeters.

Figure 3. FIFO Package Dimensions

TQFP packaging not only reduces critical board area and height; it also offers increased performance and reliability due to TI's advanced CMOS and BiCMOS processing. There are a number of players in the FIFO market today that employ either plastic-leaded chip carrier (PLCC) or leadless chip carrier (LCC) packages as the smallest option for any organization. Due to the larger size of these older packages, many designers that otherwise would have chosen a FIFO for a design have been forced to design without FIFOs in their PCMCIA designs, incurring higher integration cost and increased board space. By comparing total package area by FIFO organization, it is obvious that TI offers the smallest package option for each of the popular FIFO organizations (see Figure 4).

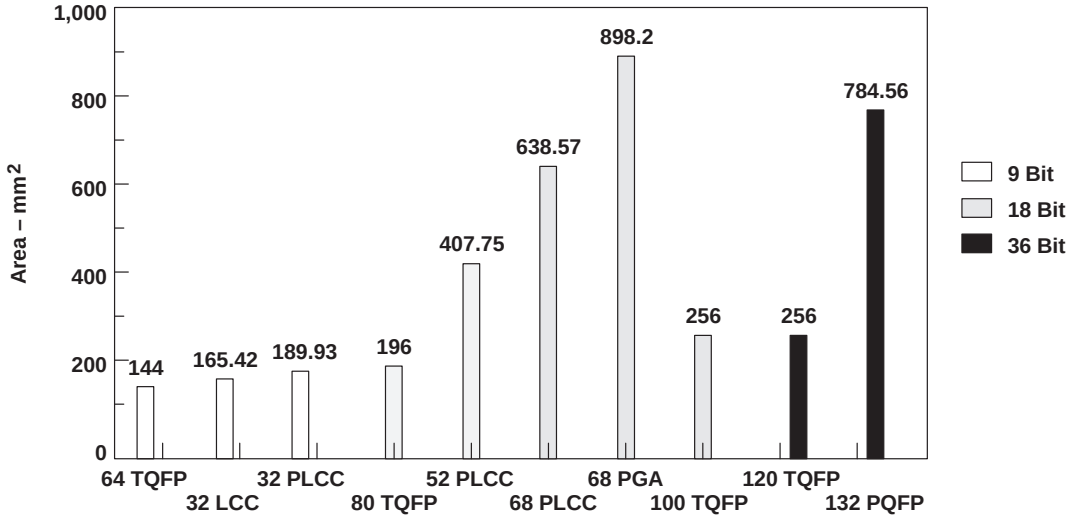


Figure 4. Area Versus Package Option

The board-space savings are even more dramatic when considering cascaded multiple 9-bit FIFOs in 32-pin PLCC packages to construct an 18- or 36-bit FIFO solution. TI's 9-, 18-, and 36-bit FIFOs offered in the TQFP packages not only eliminate the need to cascade devices, but reduce board space. An example of this board-space savings is the conventional 18-bit package, the 68-pin PLCC. TI's 18-bit FIFOs in the 80-pin TQFP reduce board space by 80%. The 68-pin PLCC has a nominal package height of 4.38 mm versus 1.5 mm for all of TI's TQFP packages. This is better shown by Figure 5 , which illustrates two TQFP packages with a nominal height of 3 mm. An additional 0.5 mm for PC board thickness makes the total height 3.5 mm. This is not only 20% thinner than PLCC, but also meets PCMCIA Type II specification.

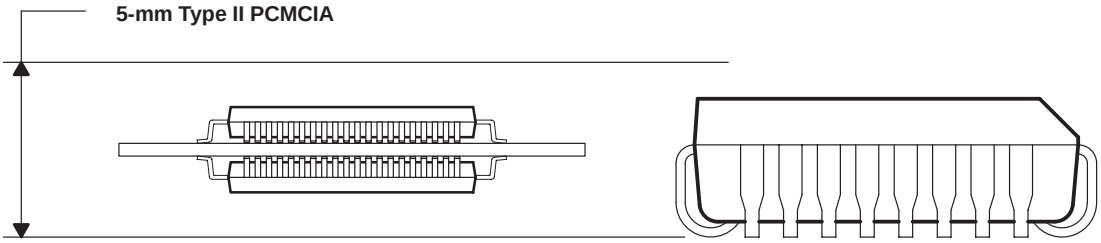


Figure 5. TQFP Package Height

Figure 6 shows a comparison of FIFO surface-mount packages versus the PCMCIA Type II specification. Packages below the reference line meet the Type II specifications. Those packages above the reference line exceed the maximum height requirements. All values are calculated based on double-side mounting (two packages) and do not include the PC board thickness (nominally 0.5 mm). Only the TQFP and 9-bit 32 LCC packages pass the Type II PCMCIA specifications.

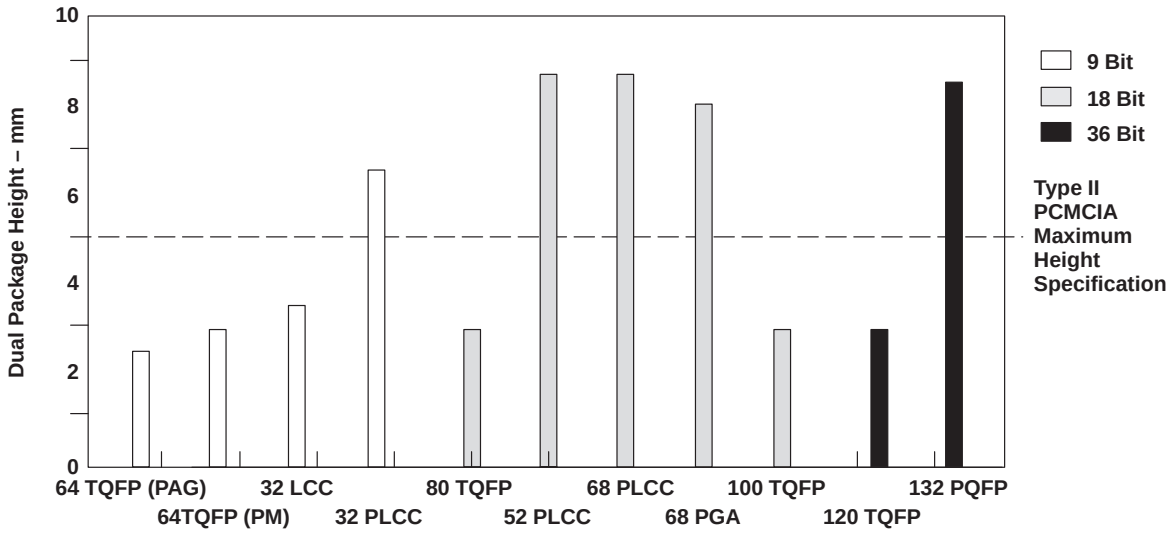


Figure 6. Type II PCMCIA Package Height Versus Dual Package Solutions†

† Board thickness is not included.

Although the LCC package may physically fit the requirements for PCMCIA cards, it does not permit optimum system design, since so much of the board area is occupied by one device. TI FIFOs available in TQFP packages allow a designer to choose the architecture and features that best meet the design criteria and dramatically reduce critical board space.

Another critical point to consider in PCMCIA design is package dimensioning and tolerances. As previously stated, the nominal values specified for a package may appear to meet PCMCIA card specification. However, due to different techniques involved in the mold processes of different packages, designers must carefully review all specifications given in the mechanical drawings for each package. In the case of the 32-pin LCC, the height tolerance varies greatly from a minimum of 1.27 mm to a maximum of 2.2 mm, a variance of 57% (see Figure 7).

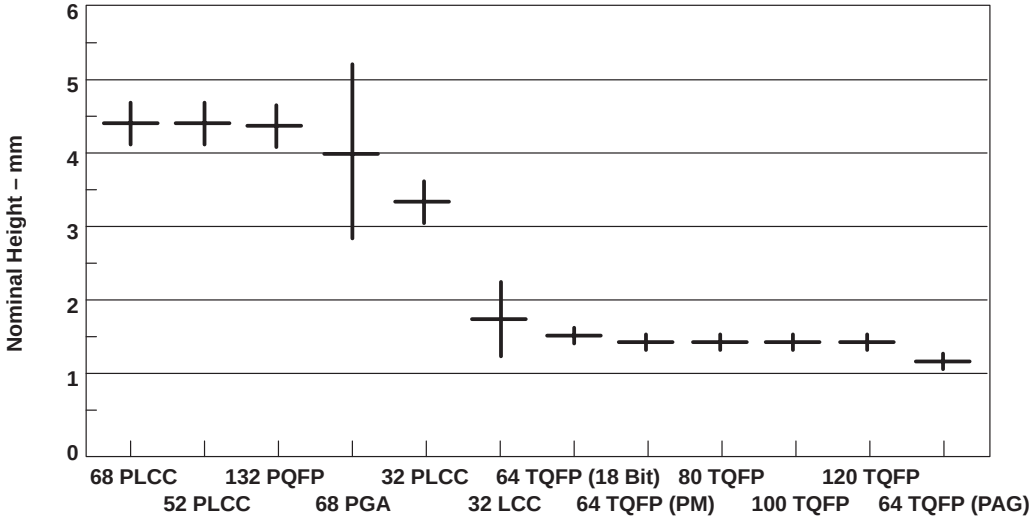


Figure 7. Typical Package Height Versus Height Variance

Figure 7 shows that TI's TQFP packages hold the tightest mechanical tolerances for all dimensions, ensuring the package clearance desired never varies by more than 0.05 mm from the nominal value. Tight control on package height is critical because clearance of a full circuit board is very tight to begin with, without factoring in variations in circuit board, solder thickness, and the PCMCIA card. TI's control of the TQFP package dimensions allows mechanical conformity without package inspection and sorting.

Power

The PCMCIA card specifications have forced all aspects of devices to be reduced in size. Equal to the need for smaller packaging is the need for reduced device power consumption. Since PCMCIA cards are closed systems, cooling fans are size restricted. Designers must carefully review device power consumption because PCMCIA cards are used primarily with portable systems that are battery powered. Reducing power consumption is especially critical to increased system battery life.

FIFO power consumption depends on several factors. Most of the power consumed by a FIFO is used in charging the CMOS circuit while performing reads and writes, sometimes referred to as duty cycle. The speed at which a FIFO operates affects the amount of power consumed. As speed increases, so does the frequency of reads and writes. To assist designers in calculating power, TI provides an I_{CC} versus frequency plot for each FIFO in the Sept. 1994 High-Performance FIFO Memories data book (literature number SCAD003B). Because the duty cycle and clock frequency at which a FIFO is operated depend on the design, TI has implemented a unique circuit feature on its advanced FIFOs, i.e., dynamic-sense amplifiers. Dynamic-sense amplifiers draw power only during a read or write operation; otherwise, they are idle, drawing less than 400 μA. Conventional FIFOs implement static-sense amplifiers that draw power even when the device is idle (approximately 50 mA). TI's dynamic-sense amplifiers are designed to optimize maximum performance without any degradation of propagation delay times. Figure 8 is a comparison of TI's 9-, 18-, and 36-bit clocked FIFOs with several conventional synchronous 9-bit FIFOs. The synchronous 9-bit FIFOs all draw more than 50 μA when idle. As system speed increases, so does the amount of power consumed. As speeds approach 60 MHz, the 9-bit synchronous FIFO draws more power than TI's clocked 36-bit FIFOs.

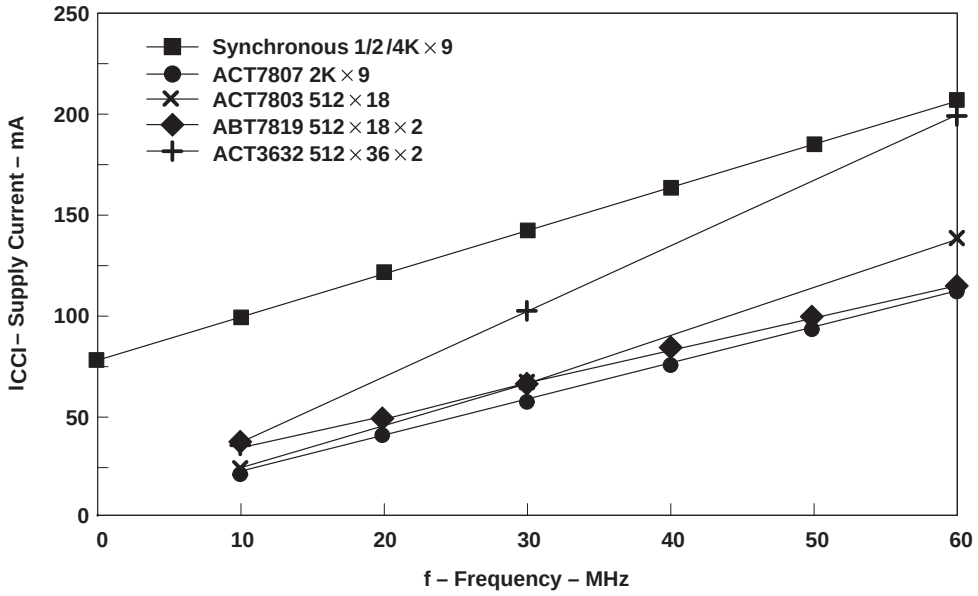


Figure 8. Active I_{CC} Versus Frequency

Using the following equation, an accurate power calculation can be made for any FIFO device.

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_{pd} \times V_{CC}^2 \times f_i) + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

Where:

I_{CC} = power-down supply current maximum
N = number of inputs driven by a TTL device
ΔI_{CC} = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
C_{pd} = power dissipation capacitance
C_L = output capacitance load
f_i = data input frequency
f_o = data output frequency

The power consumption of a single 9-bit device is an important consideration, since many designs require 18- or 36-bit FIFO solutions. Since power consumption is primarily a factor of the number of outputs switching, reducing power consumption with wider-word-width FIFOs is critical [for example, the total power consumption of a 1K × 36 FIFO when constructed by cascading four 1K × 9 FIFOs (see Figure 9)]. TI's single-chip solution, the SN74ACT3641, not only saves 65% board space, but reduces power consumption by 78% when operating at 60 MHz.

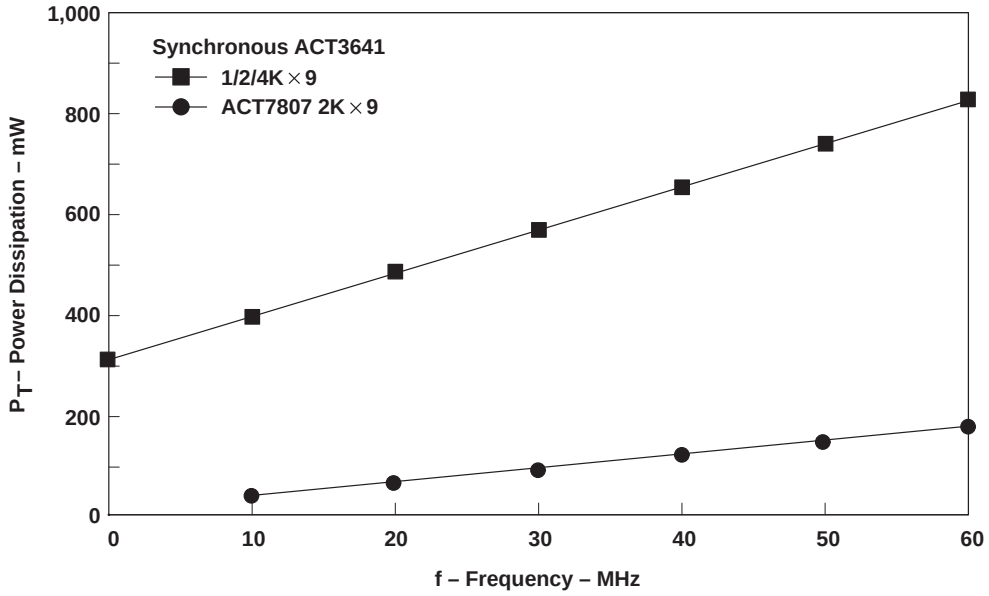


Figure 9. Multiple 9-Bit Solution Versus Single 36-Bit FIFO

Thermal Resistance

As with any small package, thermal considerations must be taken into account. Any heat generated by a device must be dissipated to ensure proper operation. The heat dissipation of a package is measured in terms of thermal resistance (R_Θ). $R_{\Theta JA}$ is defined as the thermal resistance from the die junction to ambient air. Figure 10 shows a listing of all TI's surface-mount packages and their associated $R_{\Theta JA}$ values. The listed values are measured in still air, which is a better representation of the true operating conditions of a FIFO in a PCMCIA card. The 120-pin TQFP is an example of TI's new thermally enhanced packaging (TEP) technology. The 120-pin TQFP has a heat spreader mounted to the top of the package and the die is mounted underneath in a dead-bug fashion. The 120-pin TQFP has the same $R_{\Theta JA}$ characteristics as the larger 132-pin PQFP and is 67% smaller. The heat dissipation similarities between the two packages are due to the addition of a heat spreader built into the 120-pin TQFP.

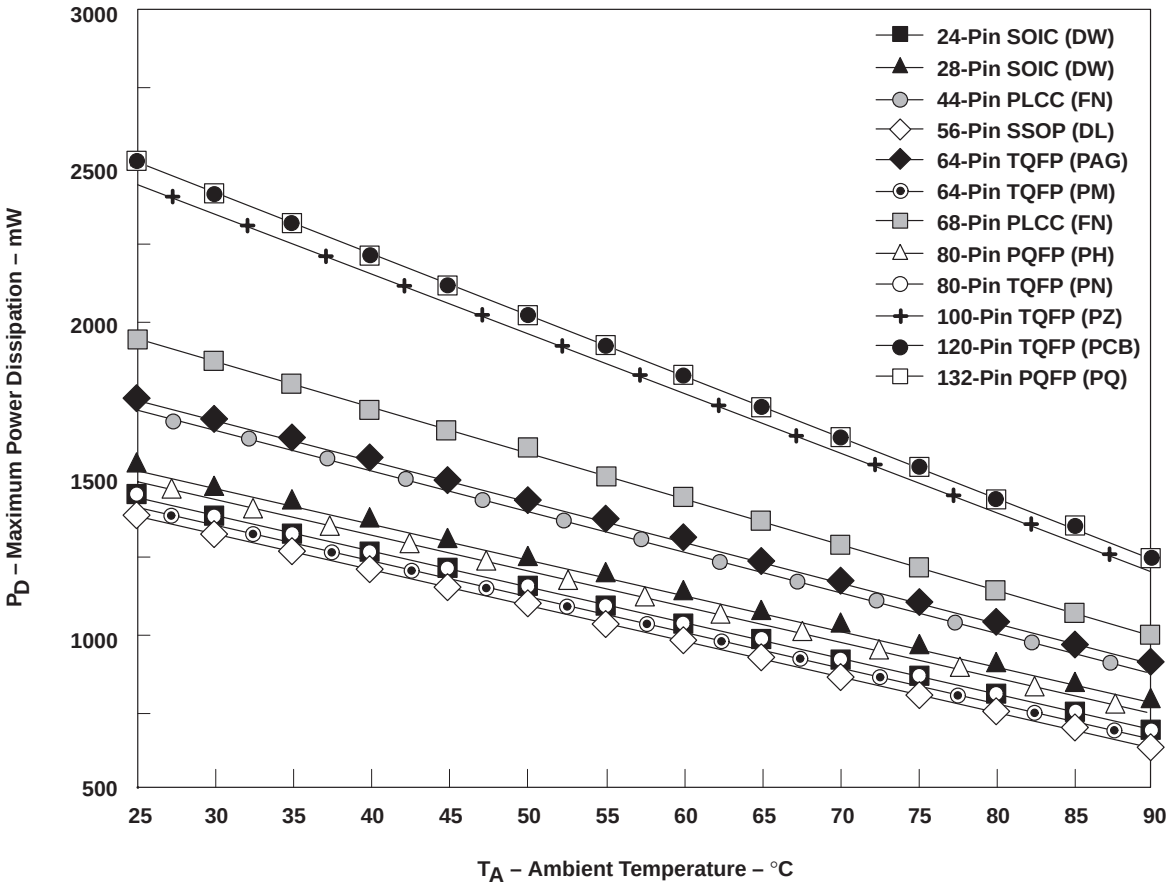


Figure 10. $R_{\Theta JA}$ for FIFO Packages in Still Air

The $R_{\Theta JA}$ characteristics in Figure 10 are measured in still air (no laminar flow), which best represents the conditions of a closed PCMCIA card. The $R_{\Theta JA}$ values are calculated using the following equation:

$$R_{\Theta JA} = \frac{T_J - T_A}{\text{power}}$$

Effective heat dissipation is needed as power increases to reduce junction temperature of the die. The increased temperature can cause drift and even device failure, which dramatically decreases mean time between failure (MTBF). TI has improved device reliability by combining decreased power and effective packaging.

Conclusion

As the demand for PCMCIA card continues, so does the demand for lower power and more space-saving packages. TI has met both demands with TQFP packages for their advanced CMOS and BiCMOS FIFOs. The TQFP package dramatically reduces board space over conventional packaging and eliminates the need to cascade multiple FIFOs to create 18- and 36-bit FIFO solutions. The implementation of dynamic-sense amplifiers on all advanced FIFOs reduces power consumption and; therefore, improves system reliability and provides longer battery life for portable systems.