



# ***Design Considerations for Logic Products***

*Application Book*  
Volume 3

***December 2000***

***Logic Products***

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**Application  
Book  
Volume 3**

# **Design Considerations for Logic Products**

*December  
2000*



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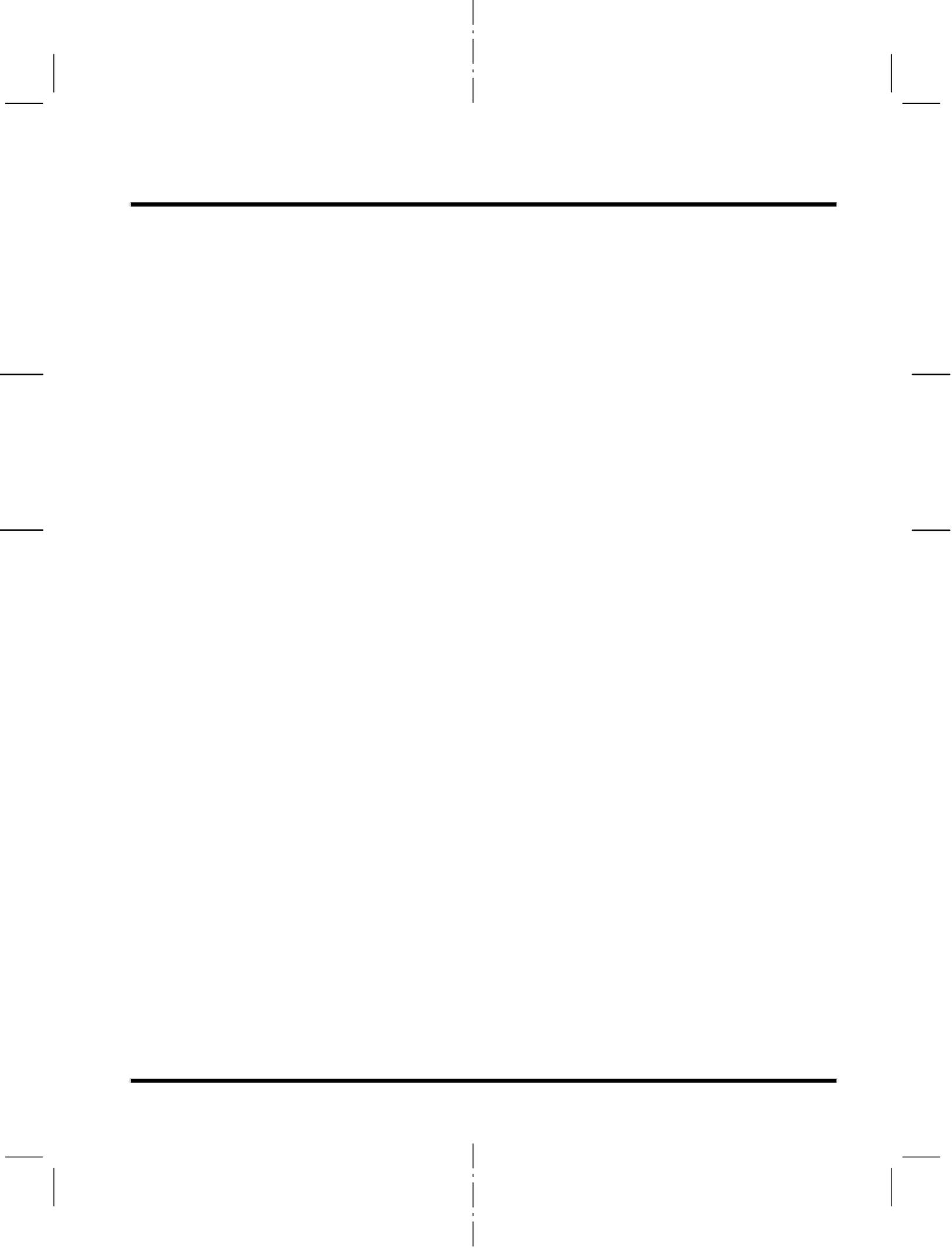
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# Appendix A

# ***Design Considerations for Logic Products Application Book***

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## INTRODUCTION

This collection of application reports and articles provides the design engineer with a valuable technical reference for Texas Instruments' products. It contains application reports written or revised between August 1999 and August 2000. This book is divided into three sections, each focusing on different aspects of design decisions. An index is included to make it easy to find the information.

Section 1, *General Design Considerations*, includes discussions of using digital integrated circuits with 5-, 3.3-, and 2.5-V power supplies, migration to lower voltages, voltage translation, and other considerations when designing with TI logic devices.

Section 2, *Device-Specific Design Aspects*, focuses on features specific to a device or family of devices, including CBT in flexible voltage-level translation, the new CBTK active-clamp feature, AHC/AHCT123A monostable multivibrators, and the Advanced Low-Voltage Technology (ALVT) family.

Section 3, *Packaging*, gives an overview of electrical and thermal parameters, logic-device marking guidelines, and packing methodology to help you select the best advanced-logic-device package for your design.

For more information on these and other TI products, please contact your local TI representative, authorized distributor, the TI technical support hotline at 972-644-5580, or visit the TI logic home page at <http://www.ti.com/sc/logic>. Application reports published in previous volumes of the *Design Considerations for Logic Products* Application Book (see Appendix A) also are available through links on the TI logic home page.

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SZZA008  
September 1999



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## Abstract

This application report presents a comprehensive collection of the input and output characteristic curves of integrated circuits from various 5-V logic families. These curves go beyond the information given in data sheets by providing additional details regarding the characteristics of the components. This knowledge is particularly useful when, for example, a decision must be made as to which circuit should be used in a bus system, or when the waveforms that can be expected in a transmission system need to be predicted by using a Bergeron chart. These oscillograms are of great assistance when generating models for simulation programs, which analyze the dynamic behavior of the integrated circuits in a particular environment.

## 1 Introduction

The parameters given in the data sheets of integrated circuits can give only a very limited indication of their actual behavior in a system. Generally, data sheets give only information regarding the behavior over the input and output voltage range of 0 to 5 V. Even the output currents specified over this range only provide an incomplete picture of the actual performance that can be expected.

But, often the behavior outside the normal operating conditions is of interest. This is, for example, the situation when the characteristic curves are used to predict the signal waveforms resulting from line reflections.

With the input/output (I/O) characteristics, use of the Bergeron method, and knowledge of the load resistor, the amplitude of the line reflections can be determined.

This application report contains the input and output characteristics of integrated logic circuits, operating at  $V_{CC} = 5$  V.

Many modern logic families are specified for operation at different supply voltages. For example, the AHC logic can be used at 5-V, 3.3-V, or even at 2.5-V supply voltage.

Since three supply voltages are currently used, it is necessary to provide I/O characteristics at these different voltage levels. This report deals exclusively with devices operated at  $V_{CC} = 5$  V.

Two other application reports regarding this topic are available:

- *Input and Output Characteristics of Digital Integrated Circuits at 3.3-V Supply Voltage*, literature number SZZA010
- *Input and Output Characteristics of Digital Integrated Circuits at 2.5-V Supply Voltage*, literature number SZZA012

In view of the wide range of integrated circuits available, it is necessary to limit this information to typical characteristics only.

In Sections 2 and 3 of this report, the input and output characteristics of the following circuits are representative of other components that behave similarly in circuits:

- '00 The characteristic curves of this NAND gate are representative of all logic circuits having normal drive capability, such as gates, flip-flops, counters, multiplexers, etc.
- '40 For a range of applications, gates are available in several logic families having increased drive capability. Such components can supply about three times the output current, when compared with the normal drive capability of the logic circuits mentioned above.
- '1004 A special group of driver circuits introduced into the ALS and AS family for applications require a very large output current. These components play a particularly significant role in clock-distribution systems.
- '240 The output characteristics of these bus-interface circuits are of particular importance when choosing a circuit family for a specific system requirement. As mentioned elsewhere in this report, the available output current has a decisive influence on the distortion of signals on bus lines.
- '25240 The incident wave switching (IWS) driver was developed to meet the requirements imposed by fast bus systems and applications with exceptionally low-resistance lines. Because these components play a very significant role in applications of this kind, their characteristic curves also have been included.

Table 1 gives an overview of the input and output characteristics, which are shown in Figures 1 through 77 in the remaining sections of this application report.

Because input characteristics depend exclusively on the technology used, rather than on the logical function of the device, only one representation per logic family is shown (gate function '00 or driver function '240) in the input-characteristics section.

**Table 1. Representatives of the Different Logic Families**

FAMILY	TYPE				
	'00	'40	'240/'244	'1004	'25240
SN74	√	√			
SN74LS	√	√	√		
SN74S	√	√	√		
SN74ALS	√	√	√	√	
SN74AS	√		√	√	
SN74F	√	√	√		
SN74HC	√		√		
SN74AHC	√		√		
SN74AC	√		√		
SN74BCT			√		√
SN74ABT†			√		√†
SN74ABTE†			√†		
SN74LV	√		√		

† For the ABT/ABTE families, the measurements were taken using the bidirectional devices SN74ABT25245 and SN74ABTE16245.

Section 4 contains the calculation of line reflections using the Bergeron method, based on the SN74AHC240 device. Measurement results, demonstrating different switching behaviors of the various logic families, are given in Section 5. For these measurements, the devices under test were loaded with a 1.3-m-long coaxial cable having a characteristic impedance of 50 Ω. The end of the cable was not connected, i.e., open circuit. These waveforms provide good insight into the dynamic behavior of the components.

## 2 Input Characteristics

In the positive range, the high impedance of the input stage of the logic circuit determines the input characteristics of logic circuits (see Figures 1 through 12).

For bipolar circuits, a base-emitter current, which flows into the input circuitry, is needed. Therefore, the input resistance for bipolar logic devices is in the range of several kilohms. Negative voltage peaks are limited by a protection diode.

CMOS and BiCMOS circuits have CMOS inputs. The CMOS input stages are exclusively controlled by the applied voltage, so there is no current flowing into the input stage. Therefore, the input impedance of CMOS and BiCMOS devices is much higher and is in the range of megohms. Again, negative voltage peaks are limited by a protection diode.

The input stages of some CMOS logic families (SN74HC, SN74AC) also have an input protection diode, that is connected to  $V_{CC}$ . This diode limits the positive input voltage to maximum  $V_{CC} + 0.7$  V.

The bus-hold circuit is a special input circuit that is an option for many ABT devices. Inputs of devices that have the bus-hold circuit hold the last valid logic state. This feature is suitable where an input remains undefined, e.g., during a high-impedance state on the bus. Using the bus-hold circuit eliminates the need for pullup or pulldown resistors.

Devices with the bus-hold circuit are designated by an H in their nomenclature, for example, SN74ABTH245.

A more detailed application report, *Bus-Hold Circuits*, literature number SZDAE15, is available from Texas Instruments (TI™).

Additional application reports and other related literature are listed in Section 7, *References*.

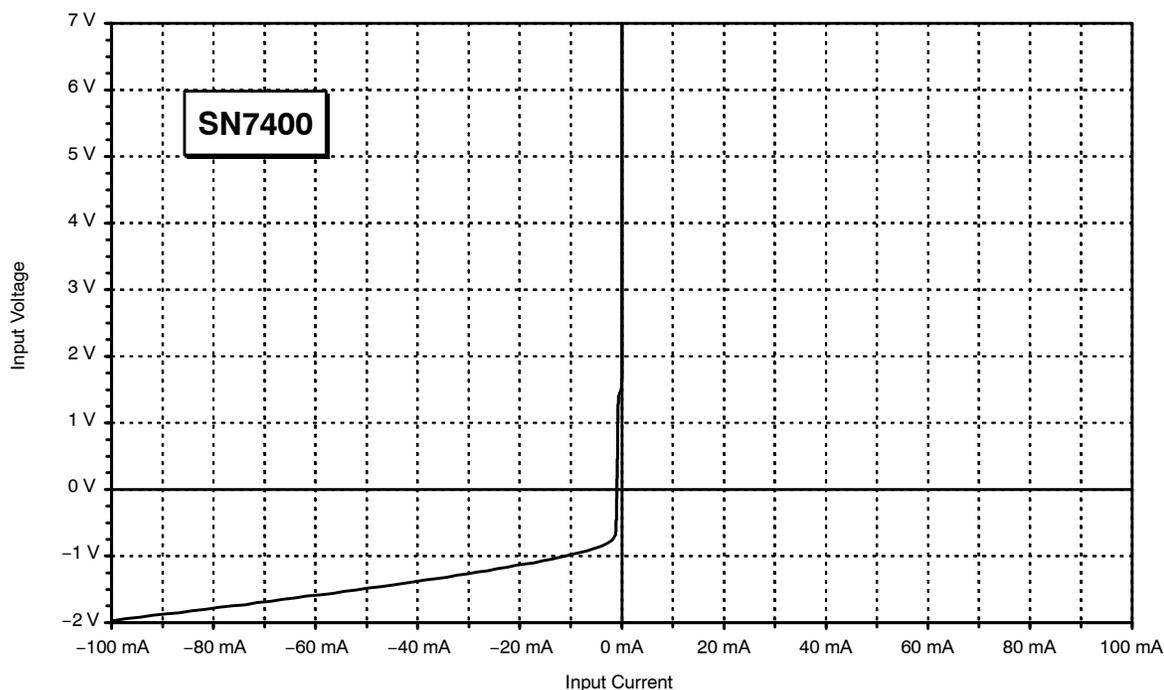
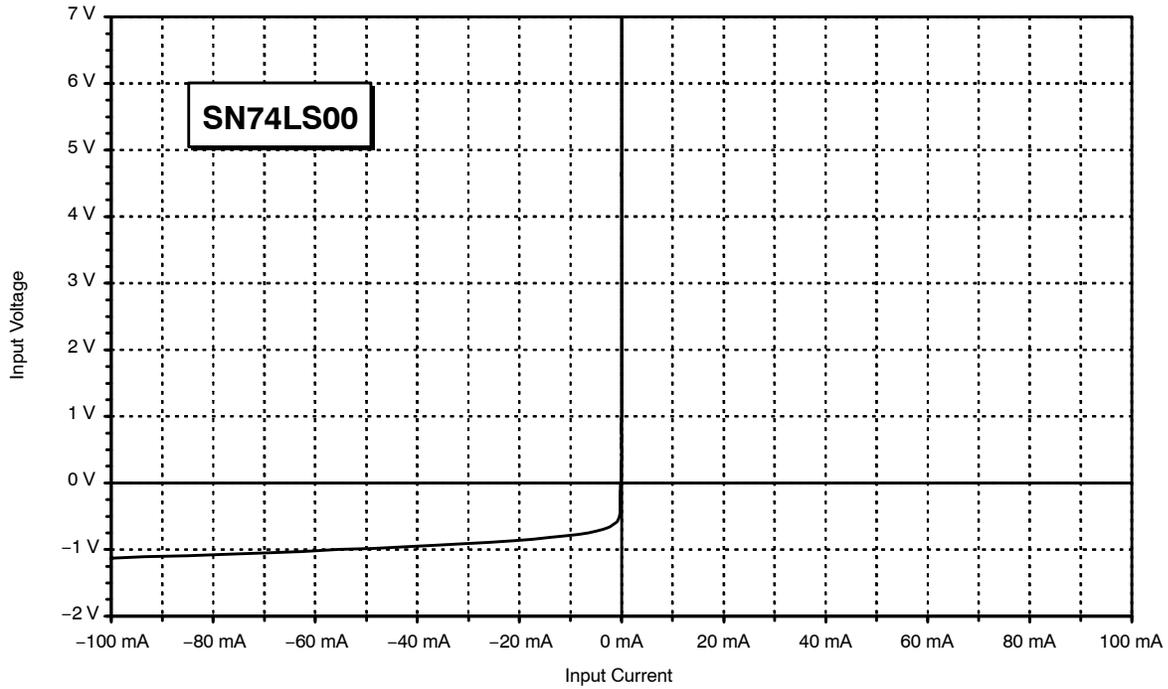
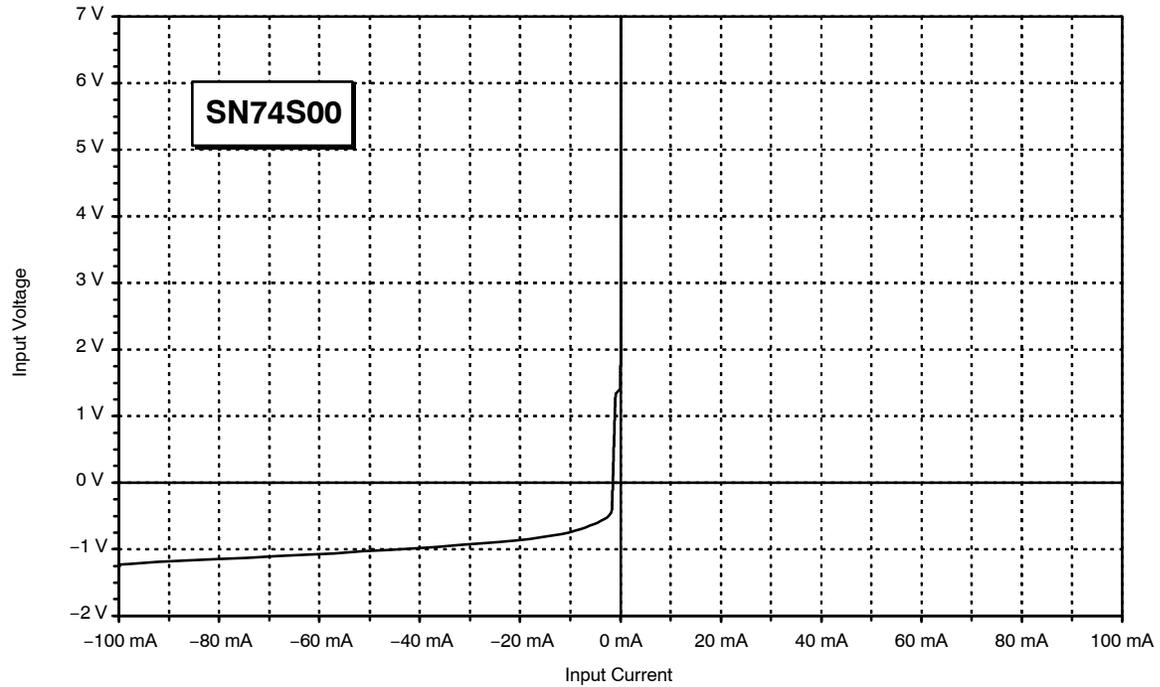


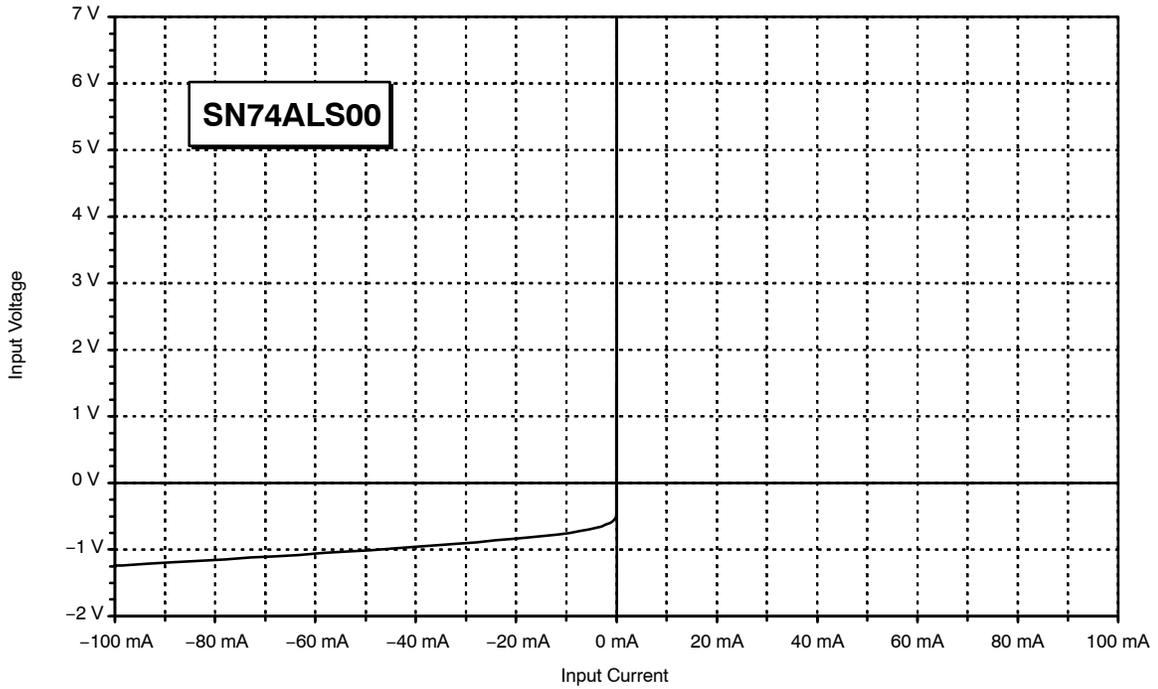
Figure 1. Input Characteristic of the SN74xxx Series



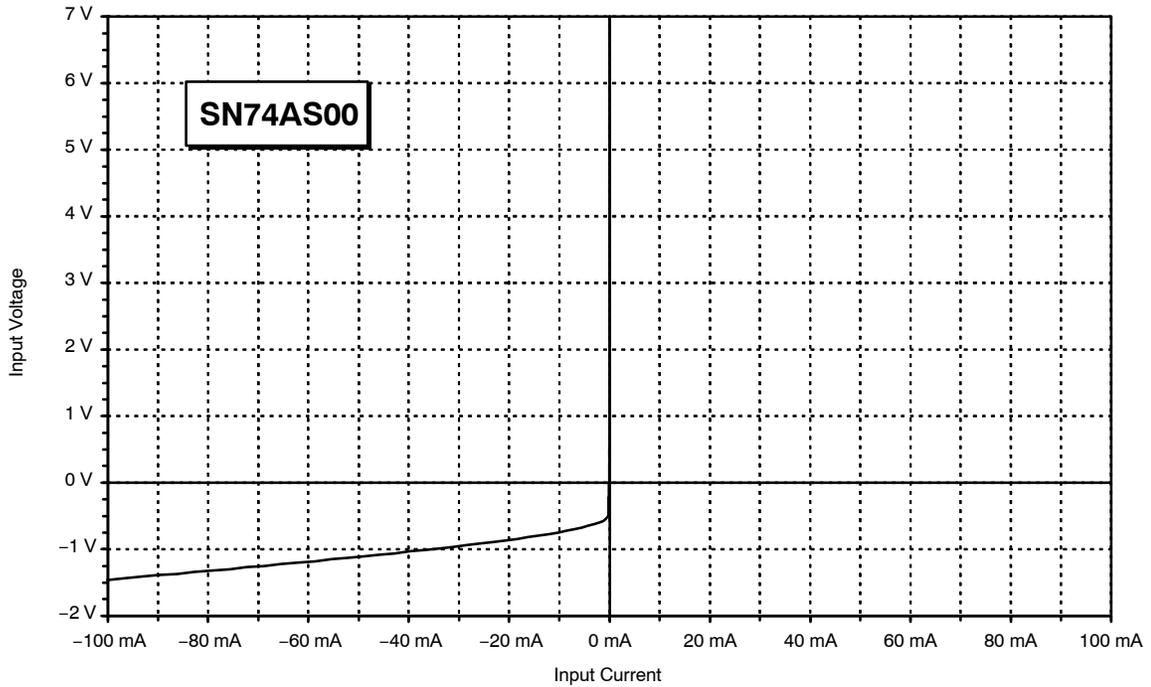
**Figure 2. Input Characteristic of the SN74LSxxx Series**



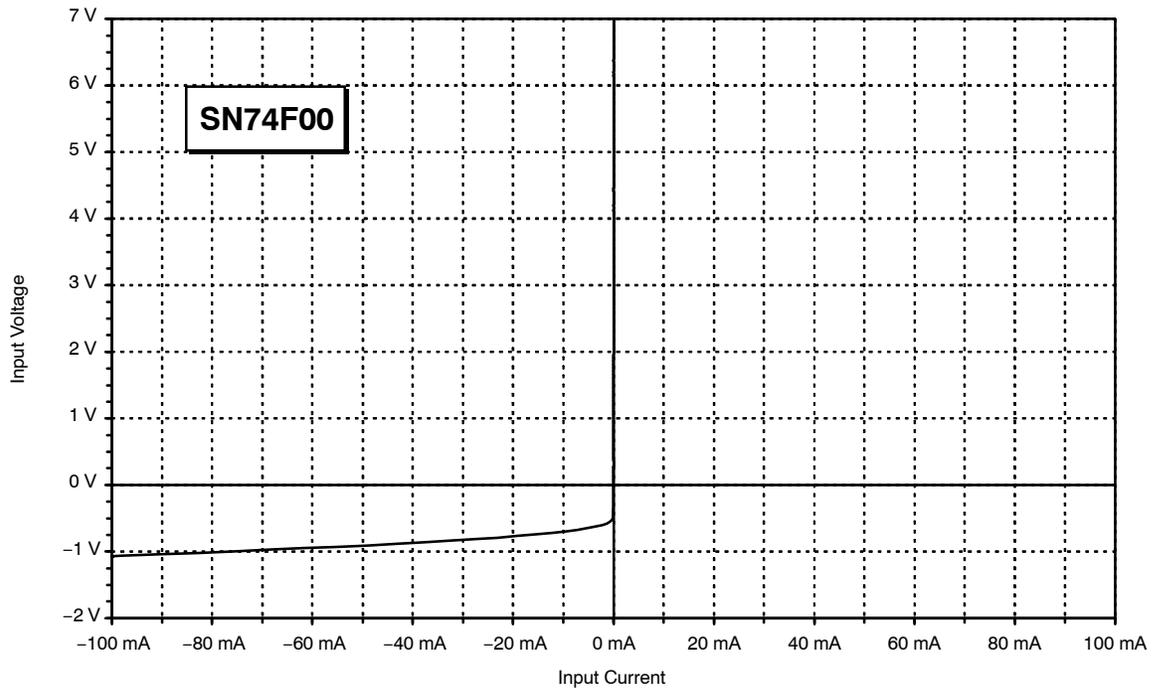
**Figure 3. Input Characteristic of the SN74Sxxx Series**



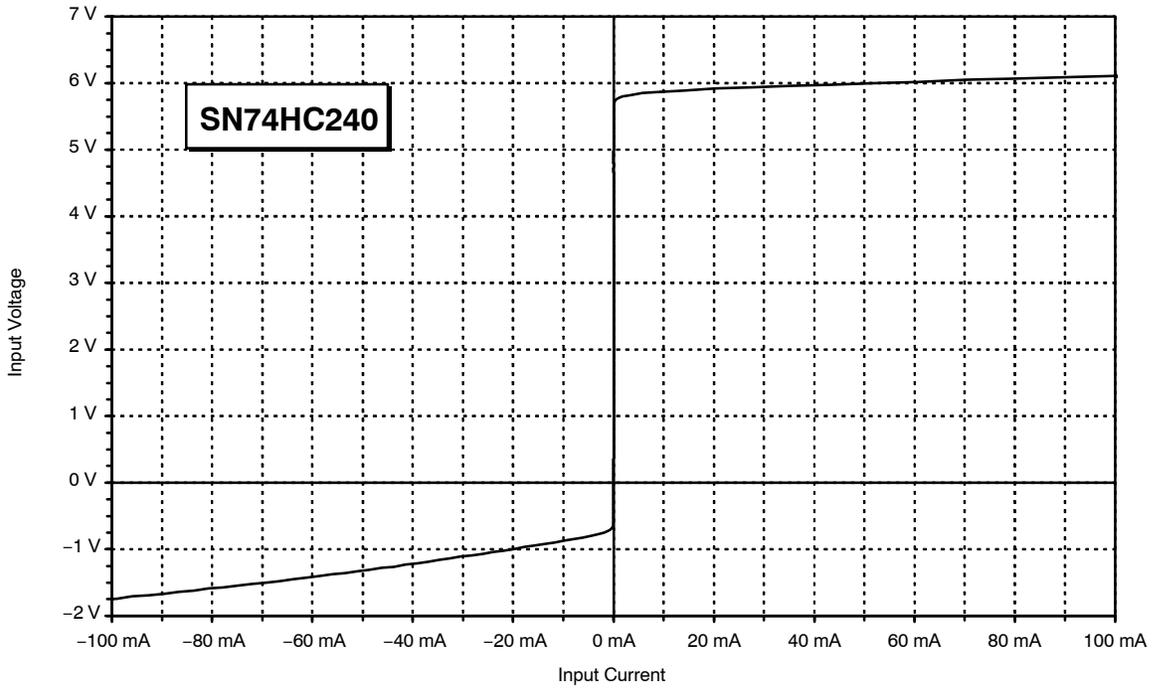
**Figure 4. Input Characteristic of the SN74ALSxxx Series**



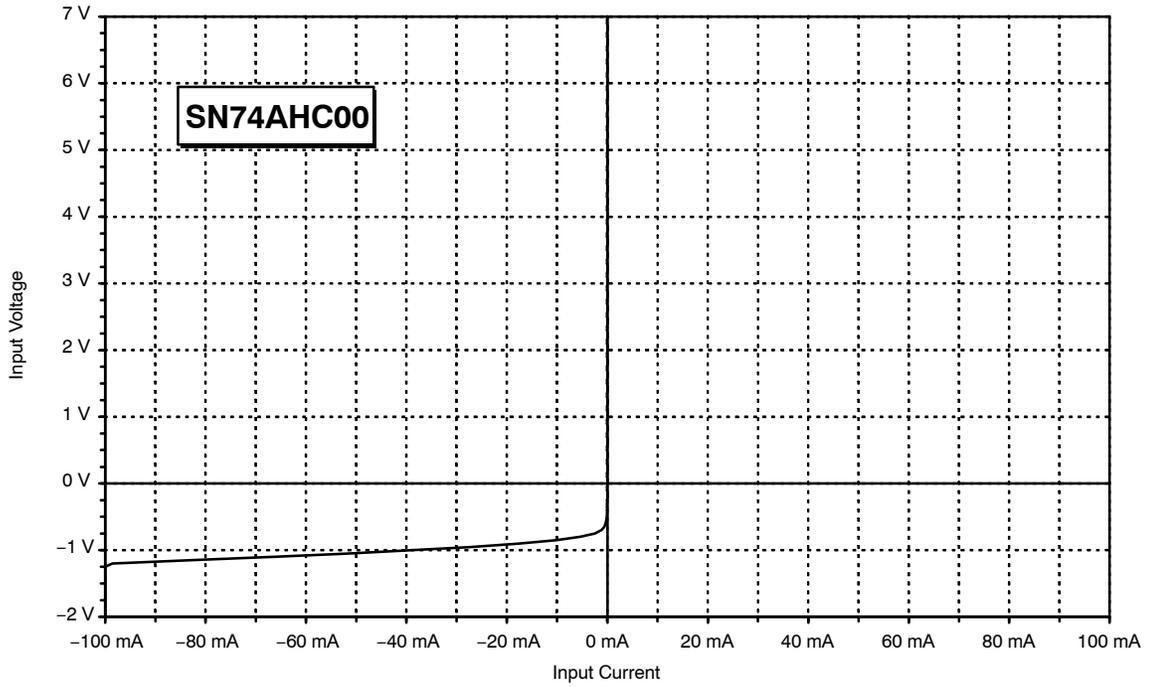
**Figure 5. Input Characteristic of the SN74ASxxx Series**



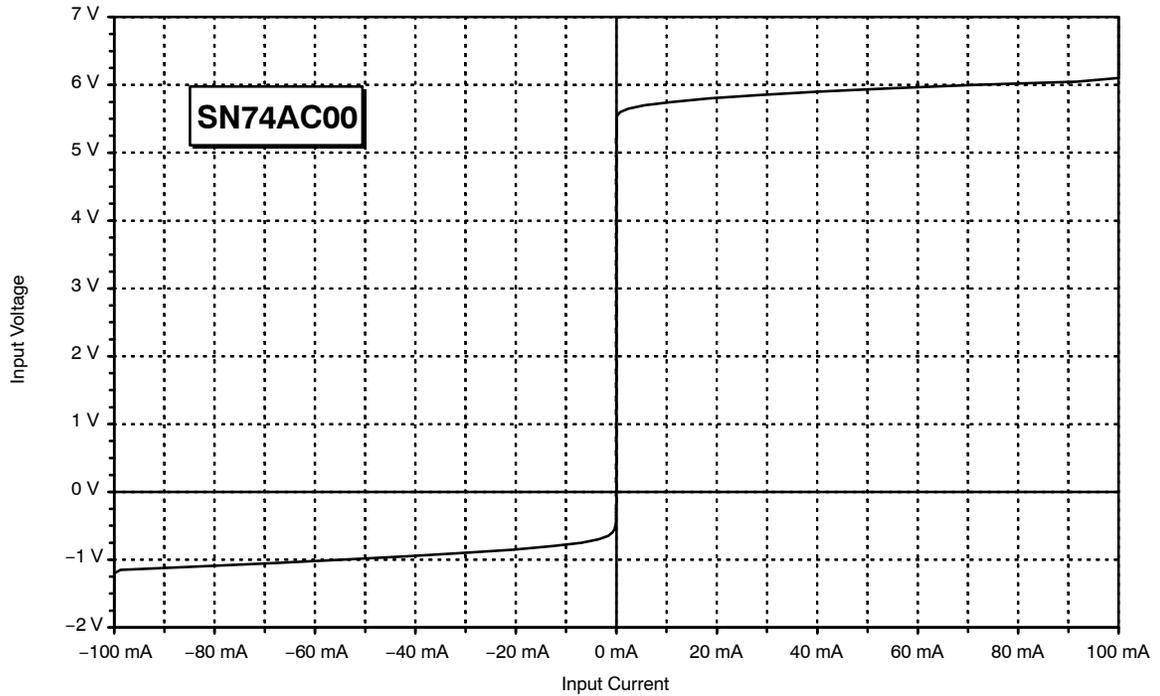
**Figure 6. Input Characteristic of the SN74Fxxx Series**



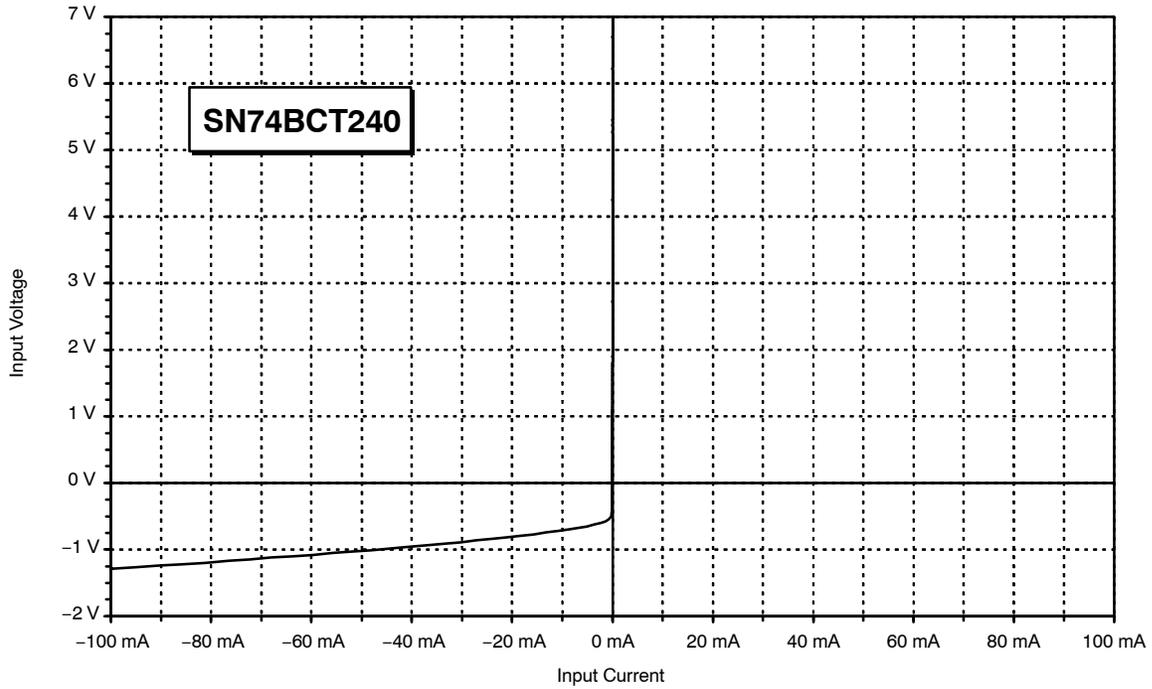
**Figure 7. Input Characteristic of the SN74HCxxx Series**



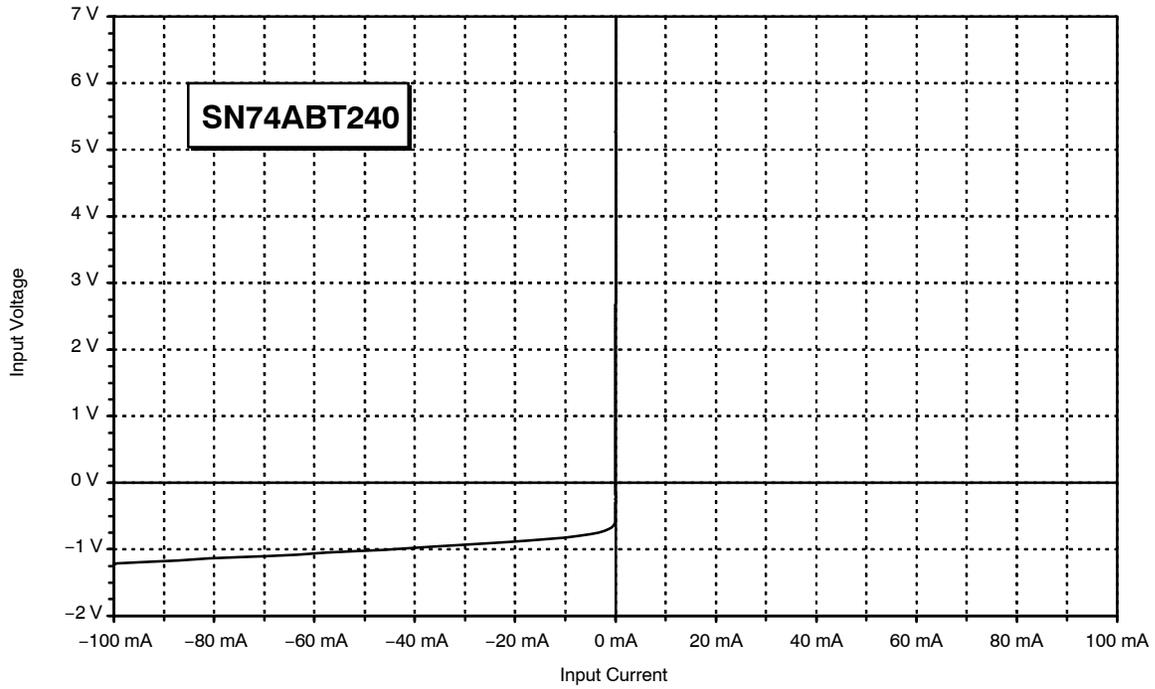
**Figure 8. Input Characteristic of the SN74AHCxxx Series**



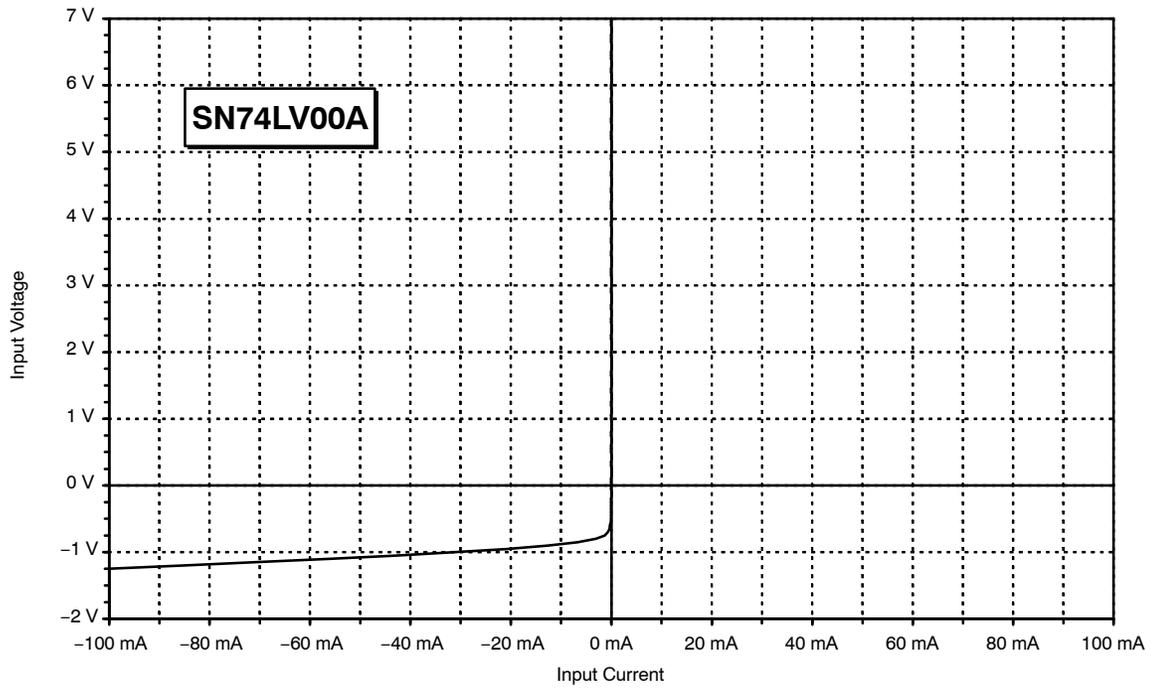
**Figure 9. Input Characteristic of the SN74ACxxx Series**



**Figure 10. Input Characteristic of the SN74BCTxxx Series**



**Figure 11. Input Characteristic of the SN74ABTxxx Series**



**Figure 12. Input Characteristic of the SN74LVxxx Series**

### 3 Output Characteristics

The output stage of a logic circuit in the high state behaves like a voltage source with an open circuit voltage of 5 V for CMOS logic, and 3.6 V for TTL and BiCMOS logic (see Figures 13 through 43). The internal resistance for the high state is inversely proportional to the drive capability of the device. The value of the internal resistance for the standard logic families is in the range of 30  $\Omega$  to 40  $\Omega$ . The internal resistance of the IWS driver is lower than 5  $\Omega$ .

In the low state, for positive voltages, the output resistance is based on the internal resistance of the conducting transistor, i.e., collector-emitter for bipolar and BiCMOS technologies and drain-source resistance for CMOS technologies. Again, negative voltage peaks are limited by a protection diode.

The output stages of some CMOS logic families (SN74HC, SN74AC) also have an input protection diode, which is connected to  $V_{CC}$ . This diode limits the positive input voltage to maximum  $V_{CC} + 0.7$  V.

TI offers driver options in the ABT family with integrated series resistors rated at about 25  $\Omega$ .

Using the damping resistors at the output stage, the effective output impedance of the driver is about 30  $\Omega$ . If the value of the line impedance also is about 30  $\Omega$ , no line reflections will be observed at the output of the device. In this case, the beginning of the line is terminated perfectly.

This option is especially beneficial for memory applications. In those applications, overshoots and undershoots may cause malfunctions. In point-to-point applications, nearly ideal signal shapes can be achieved. The 2 following the alphabetical part of the device number indicates the series damping resistor, for example, SN74ABT2245.

Further information on the topic of series damping resistors is given in the TI application report, *Bus-Interface Devices With Output-Damping Resistors or Reduced-Drive Outputs*, literature number SCBA012A.

More application reports and other related literature are listed in Section 7, *References*.

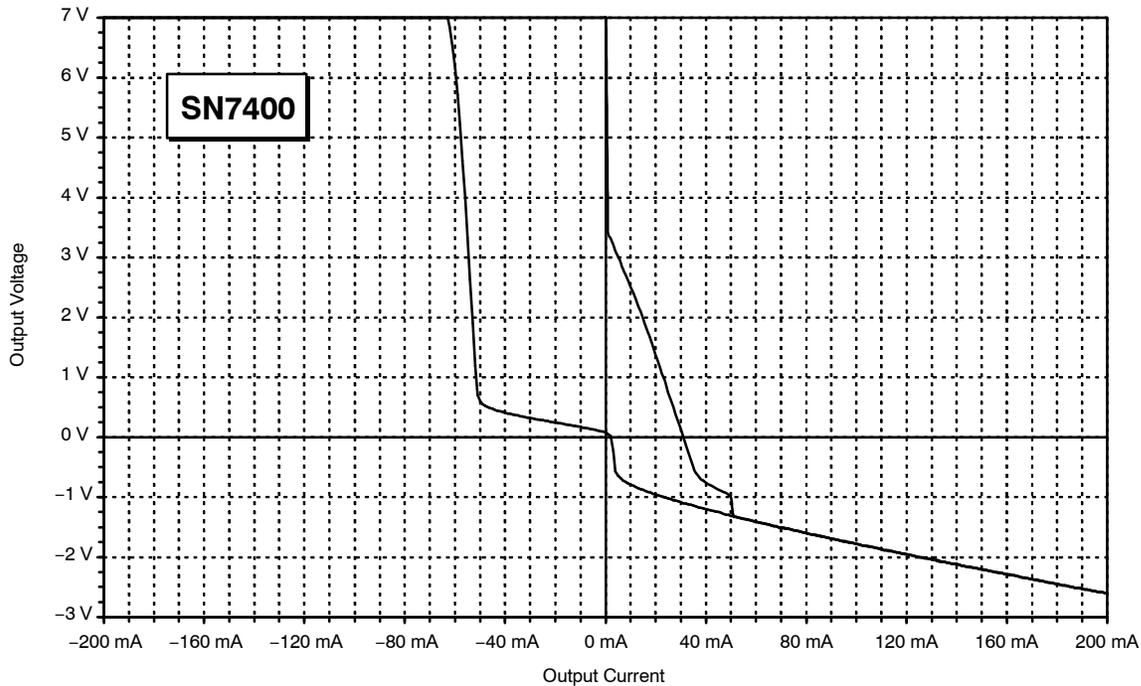
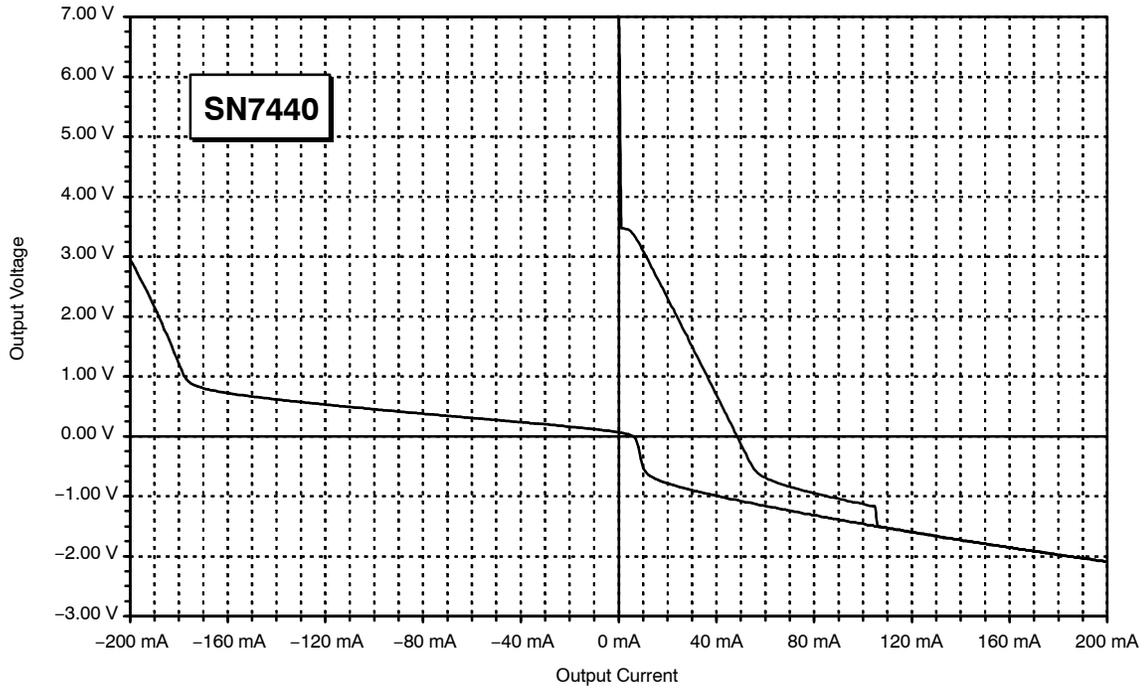
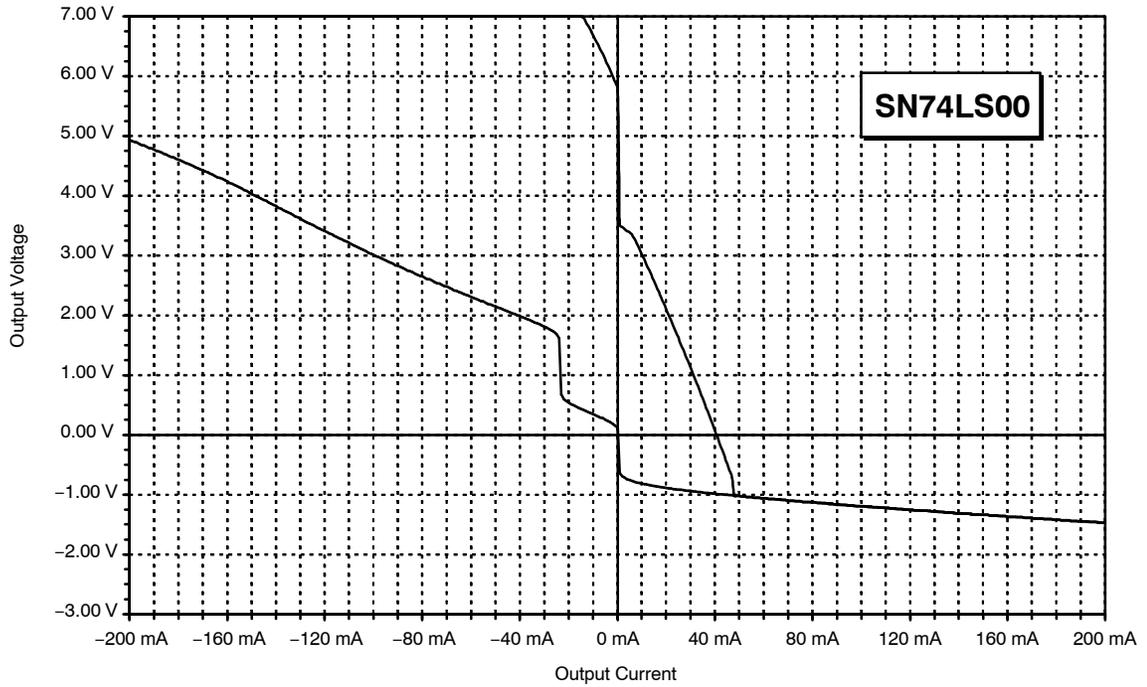


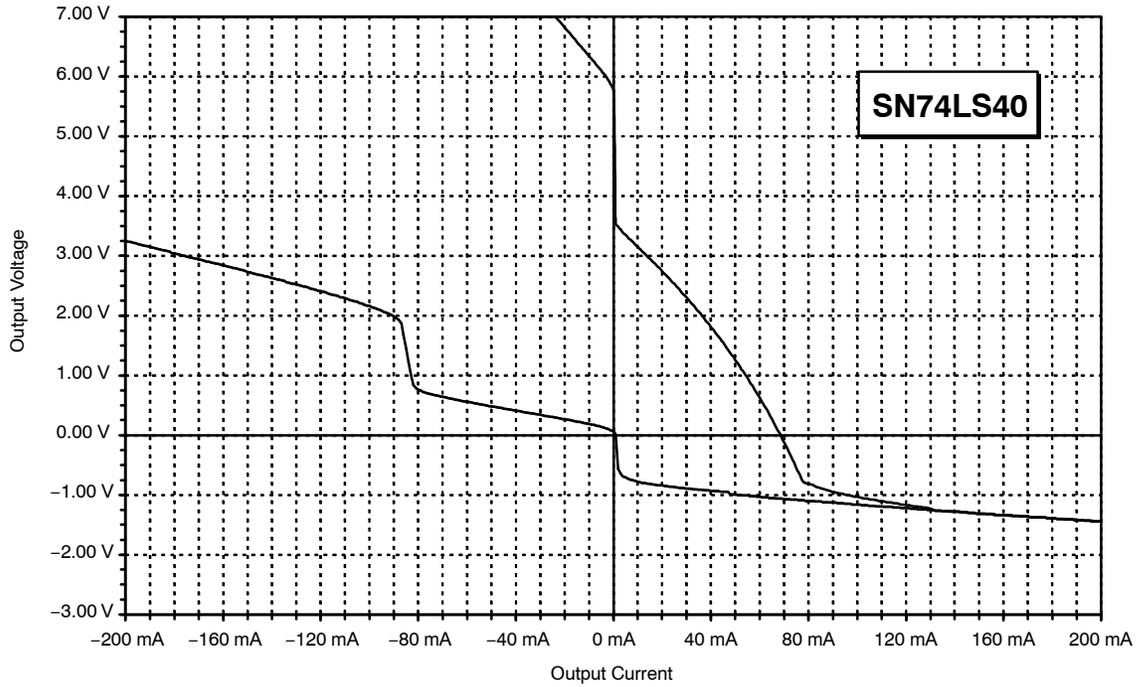
Figure 13. Output Characteristic of the SN7400



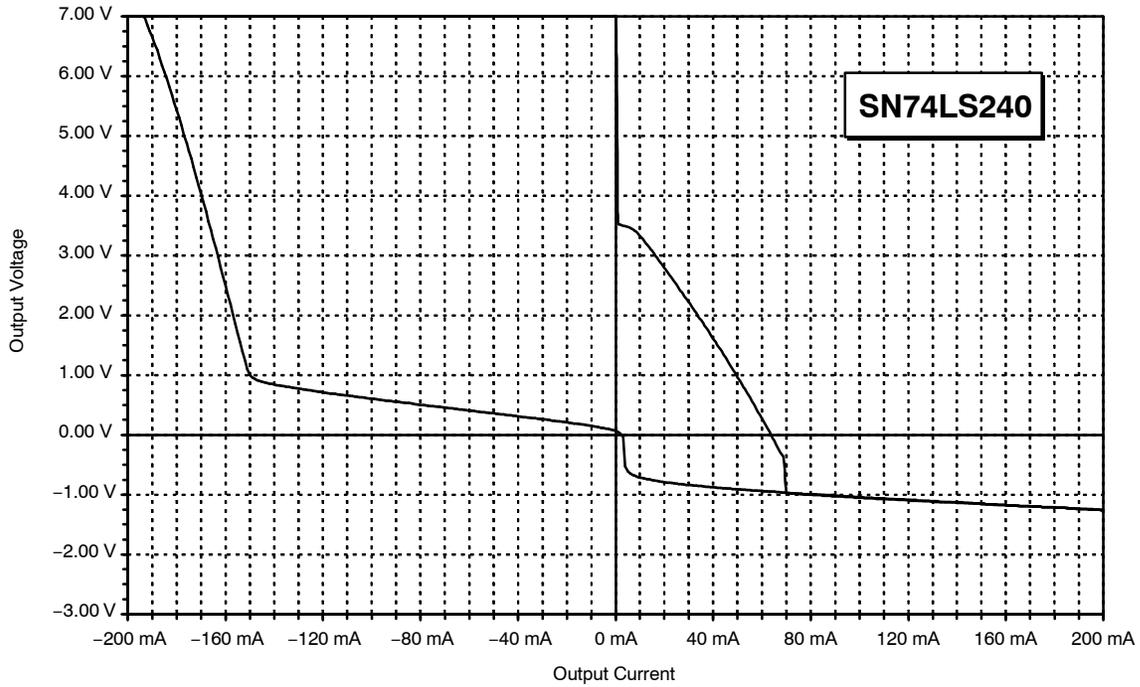
**Figure 14. Output Characteristic of the SN7440**



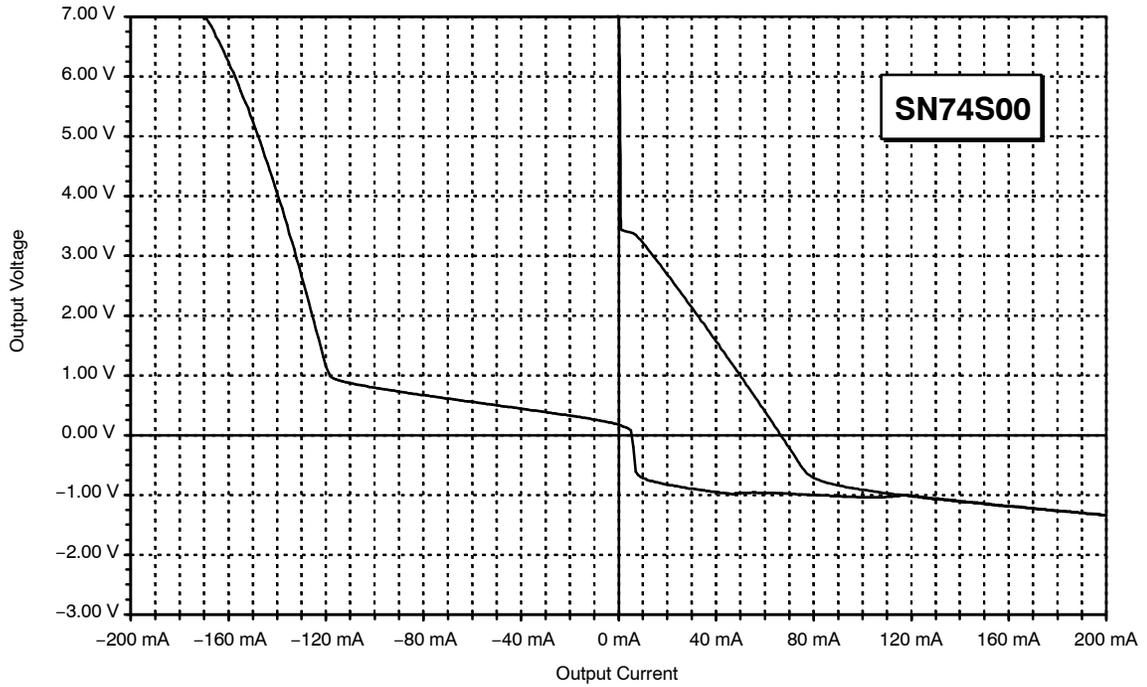
**Figure 15. Output Characteristic of the SN74LS00**



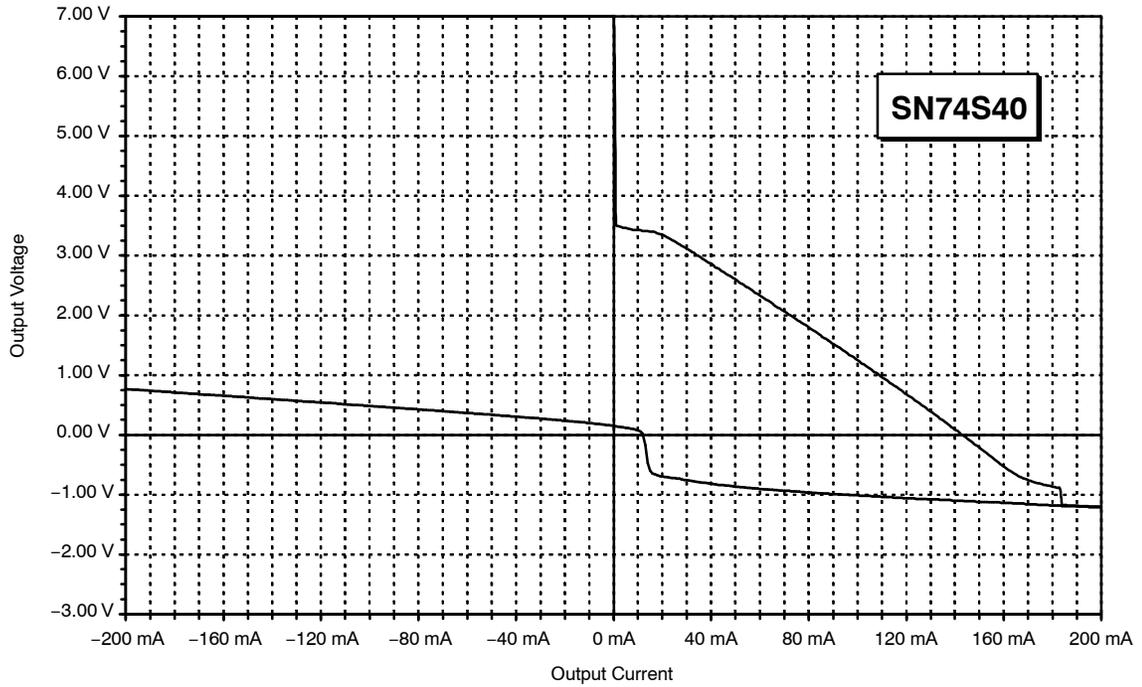
**Figure 16. Output Characteristic of the SN74LS40**



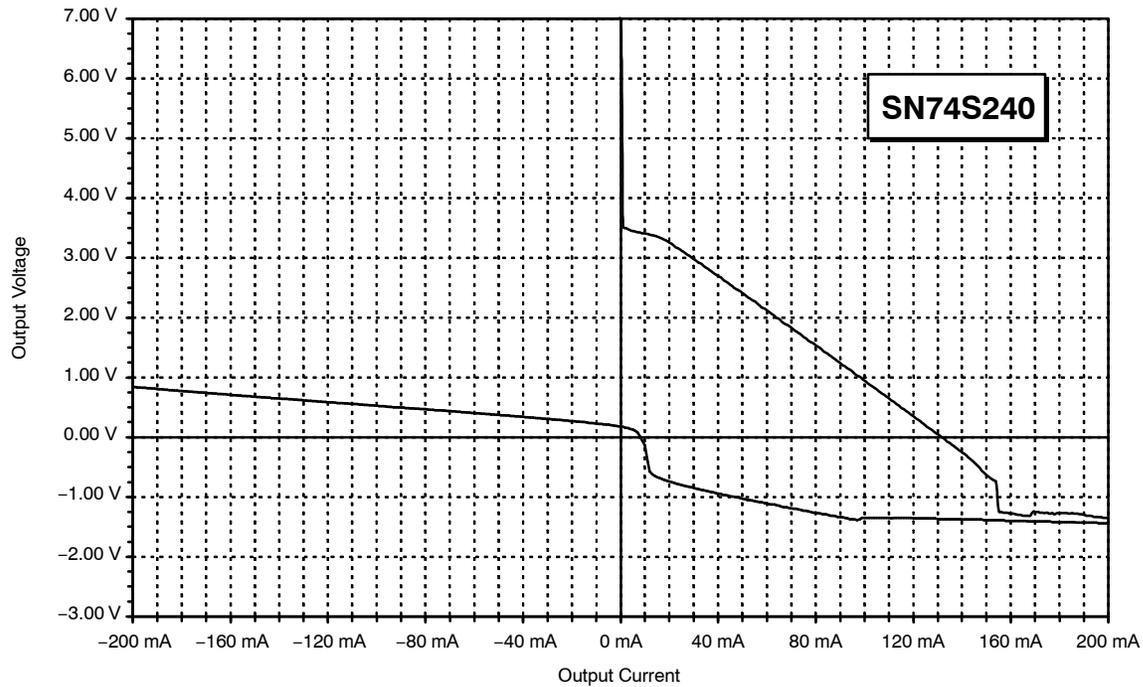
**Figure 17. Output Characteristic of the SN74LS240**



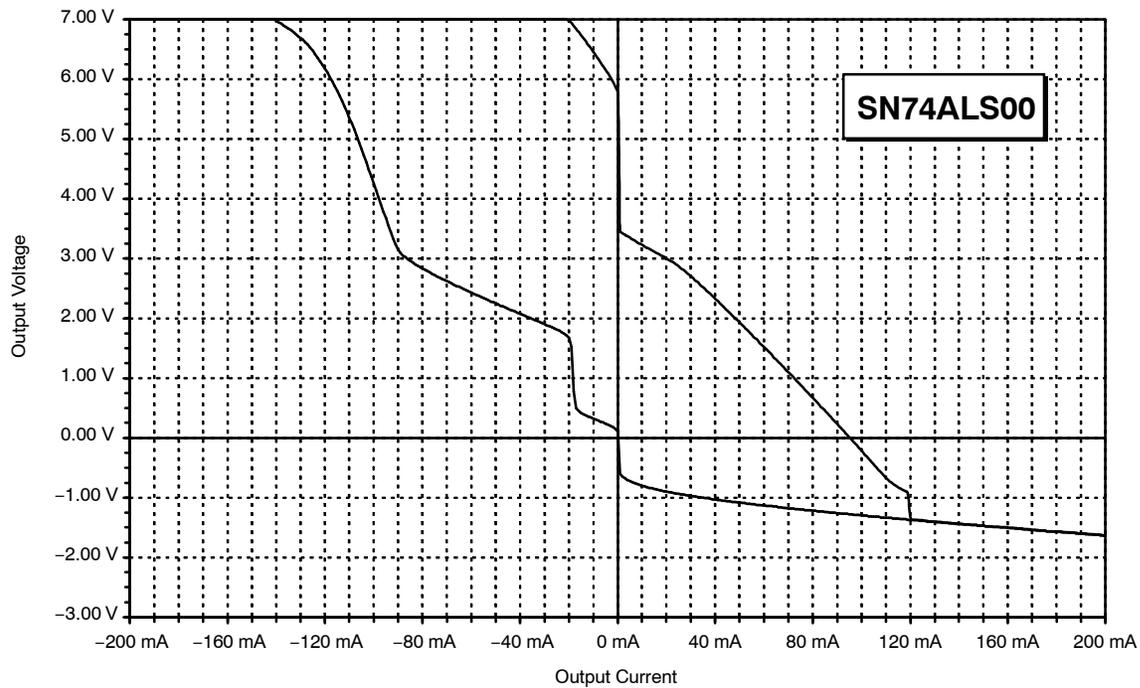
**Figure 18. Output Characteristic of the SN74S00**



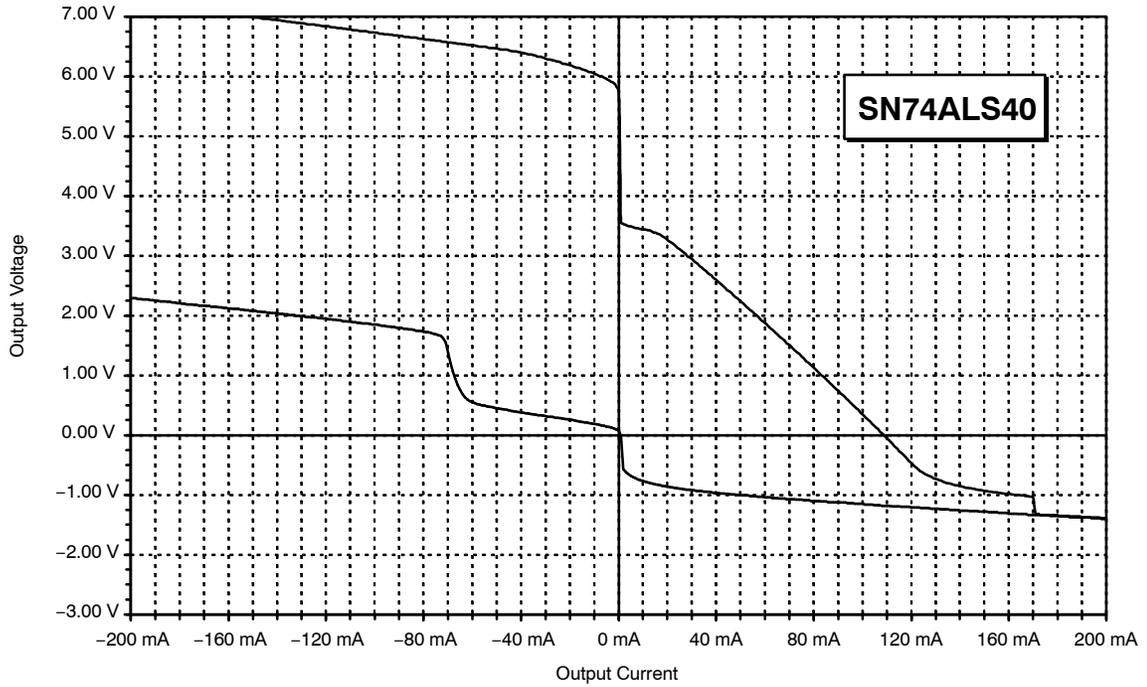
**Figure 19. Output Characteristic of the SN74S40**



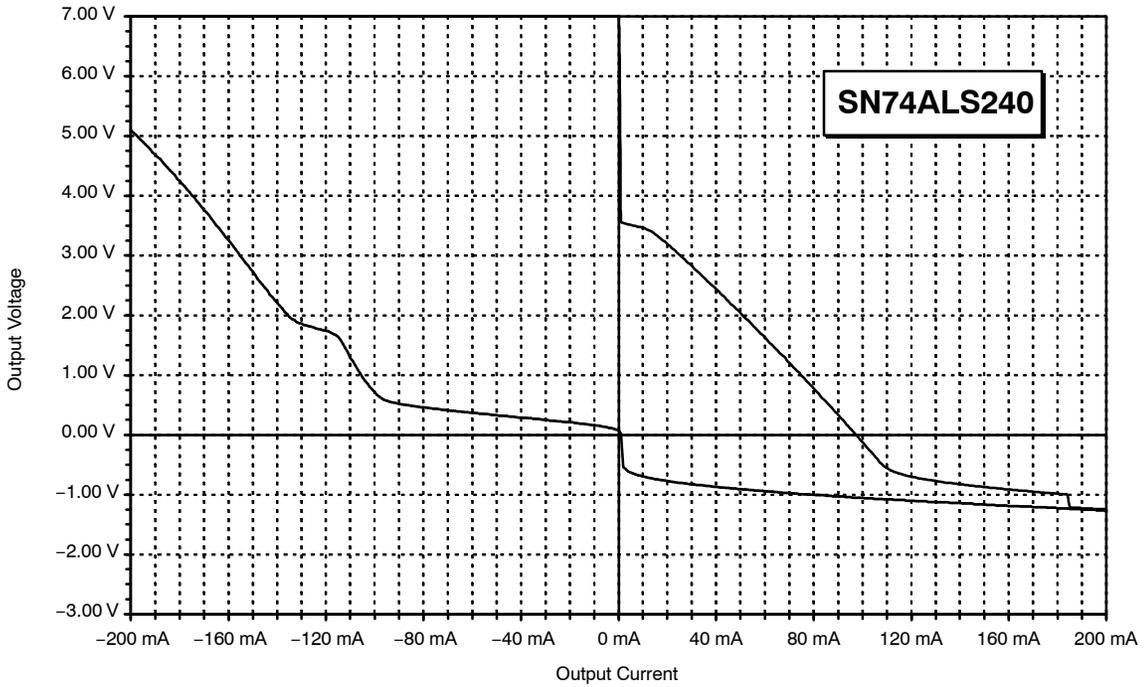
**Figure 20. Output Characteristic of the SN74S240**



**Figure 21. Output Characteristic of the SN74ALS00**



**Figure 22. Output Characteristic of the SN74ALS40**



**Figure 23. Output Characteristic of the SN74ALS240**

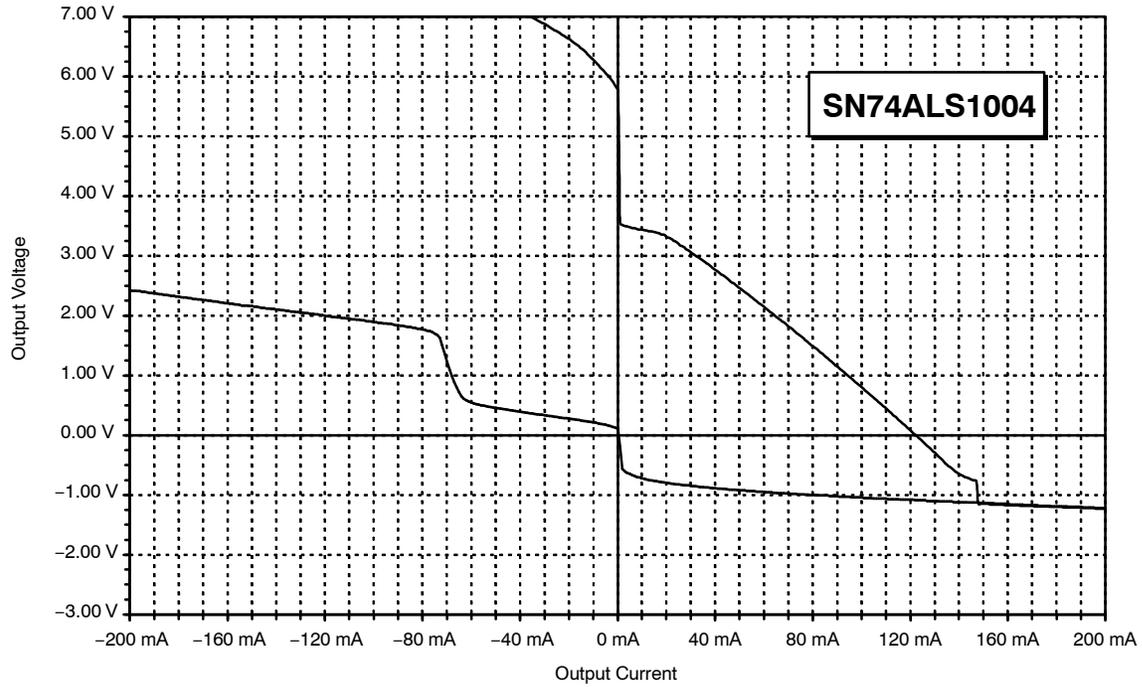


Figure 24. Output Characteristic of the SN74ALS1004

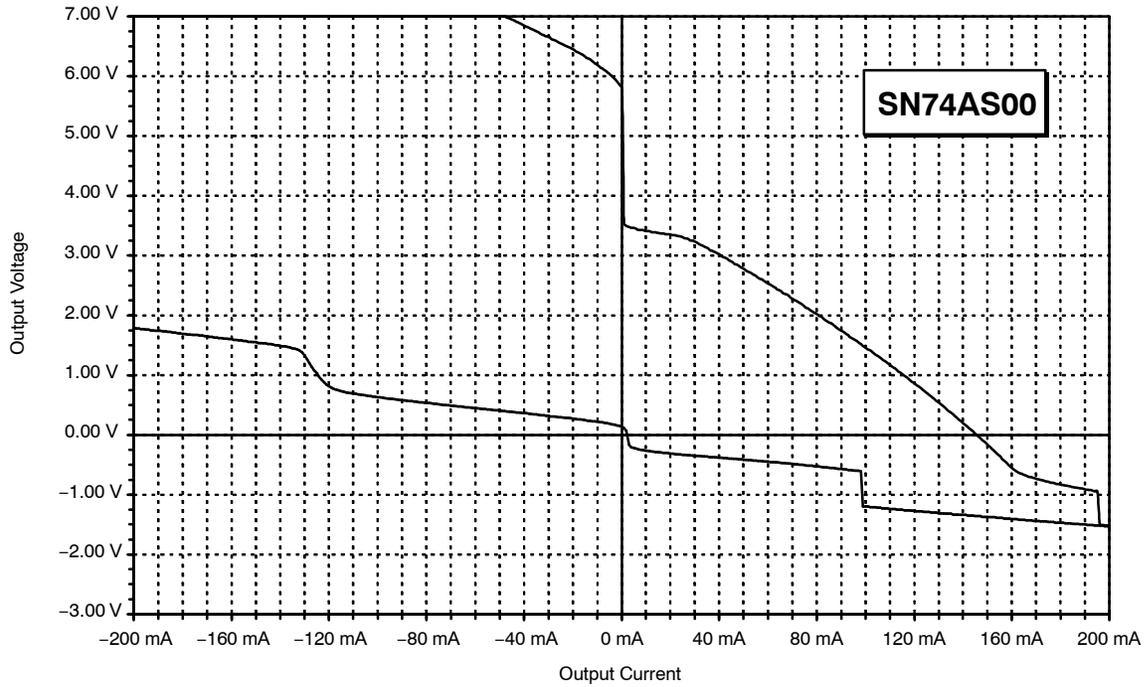
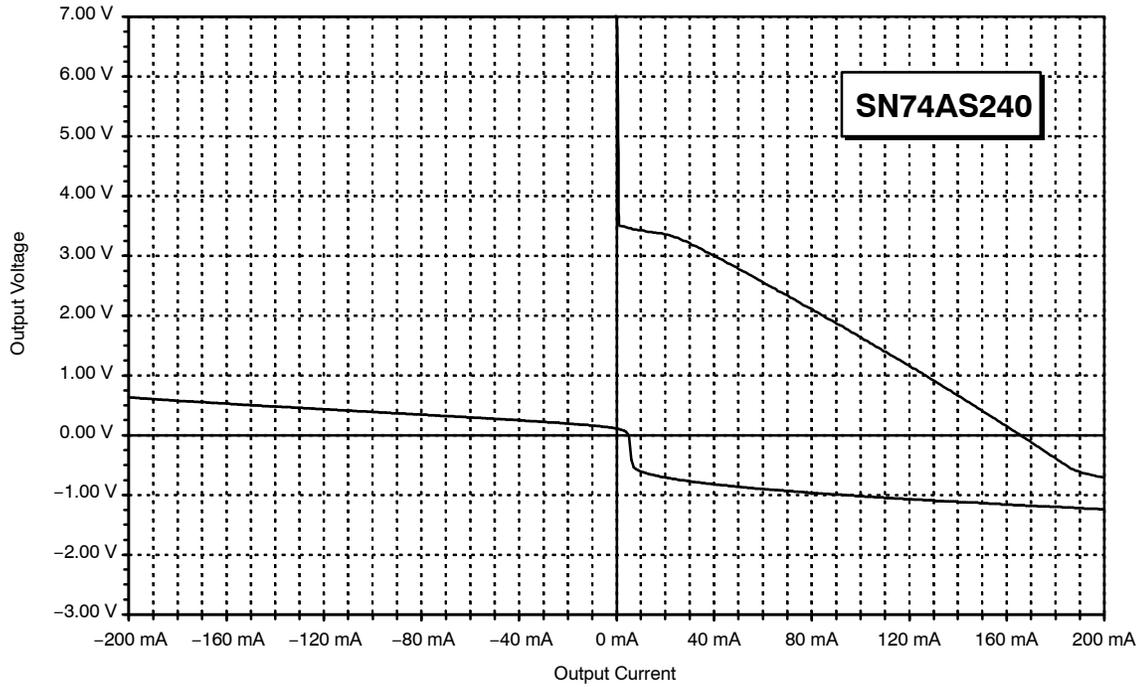
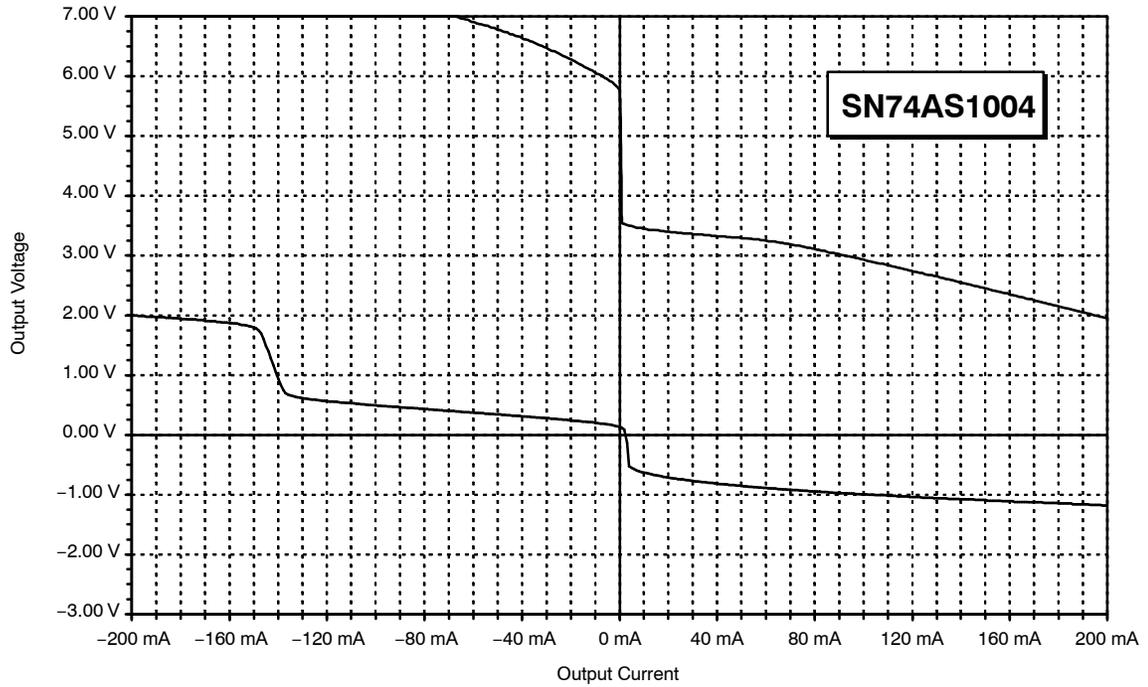


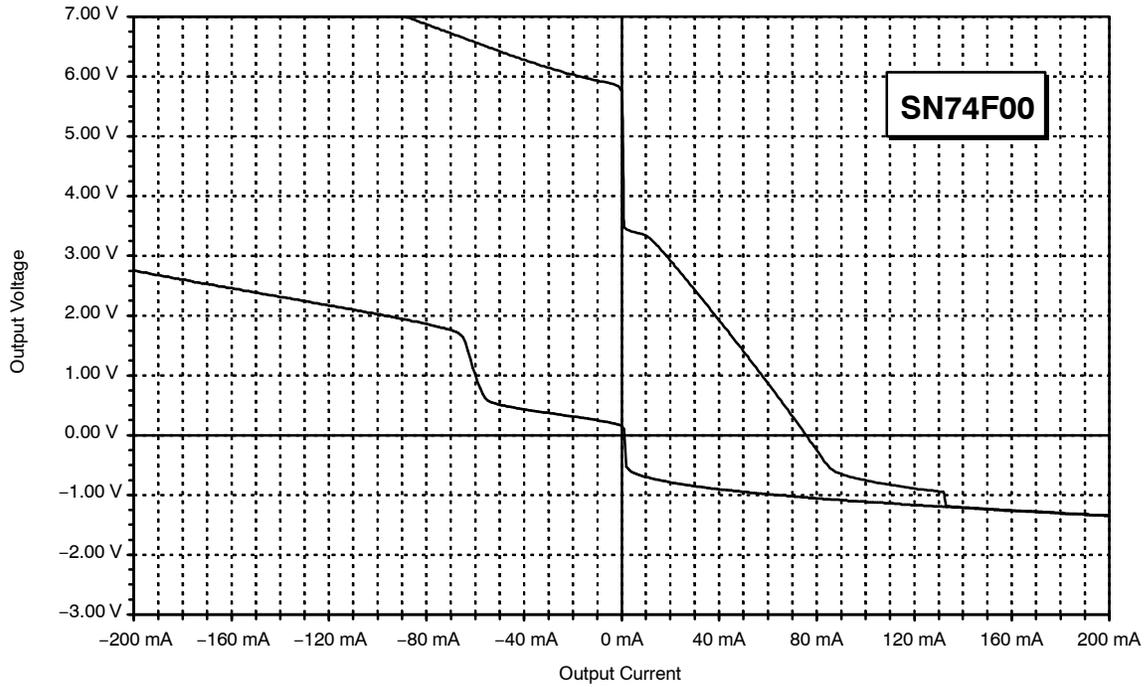
Figure 25. Output Characteristic of the SN74AS00



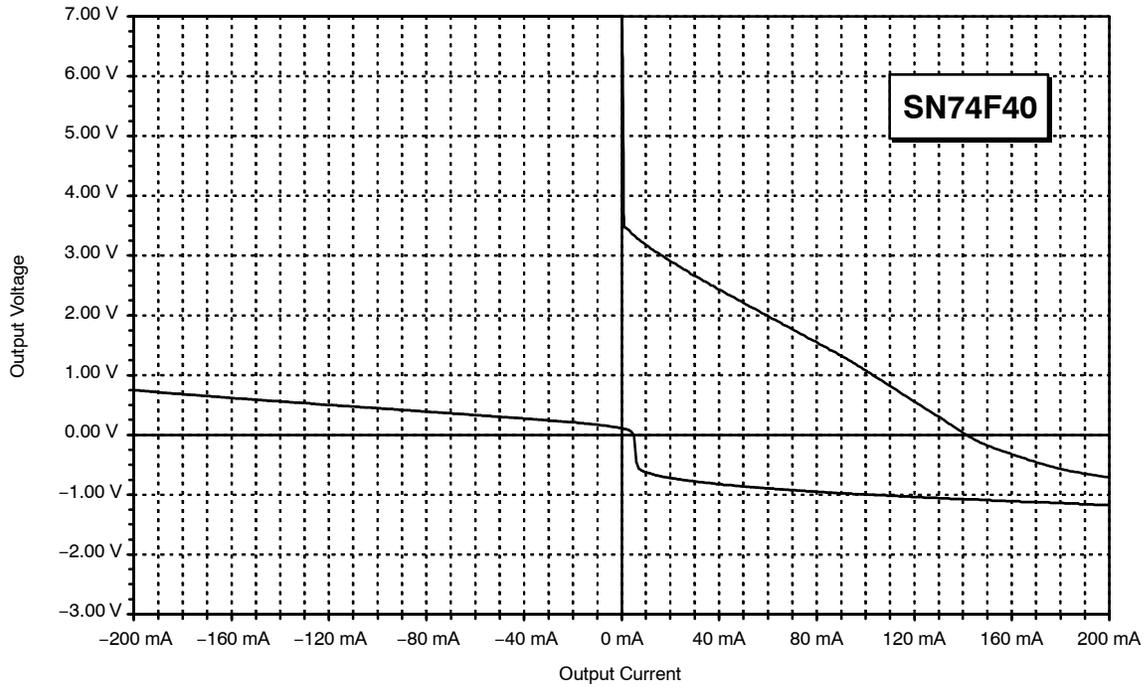
**Figure 26. Output Characteristic of the SN74AS240**



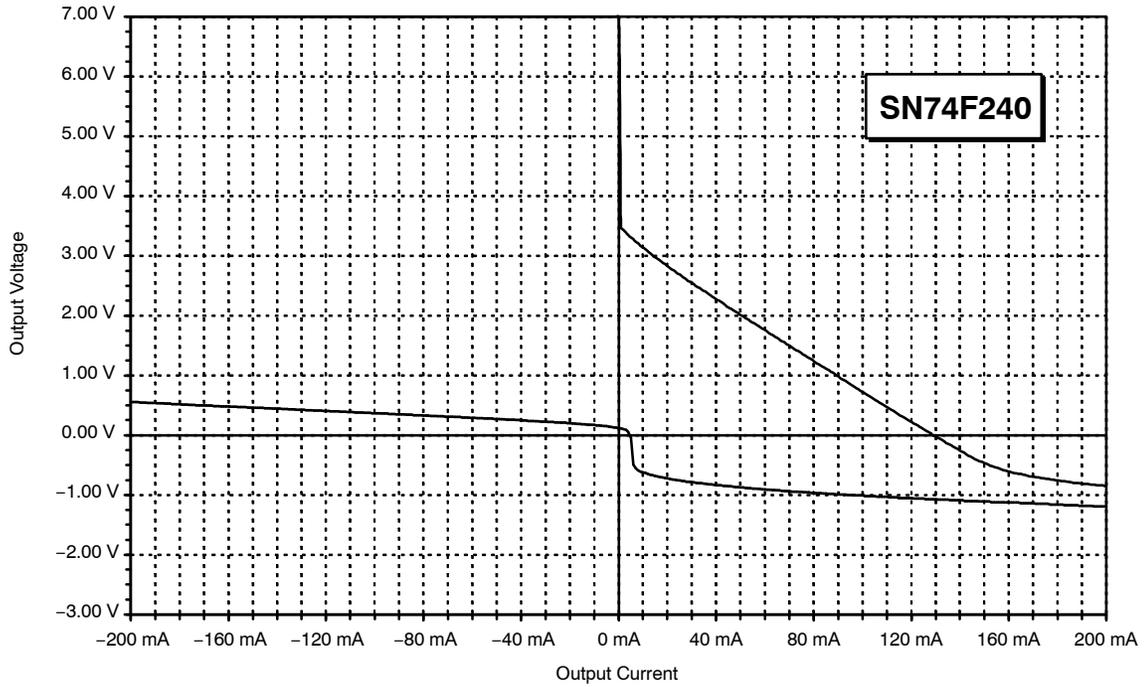
**Figure 27. Output Characteristic of the SN74AS1004**



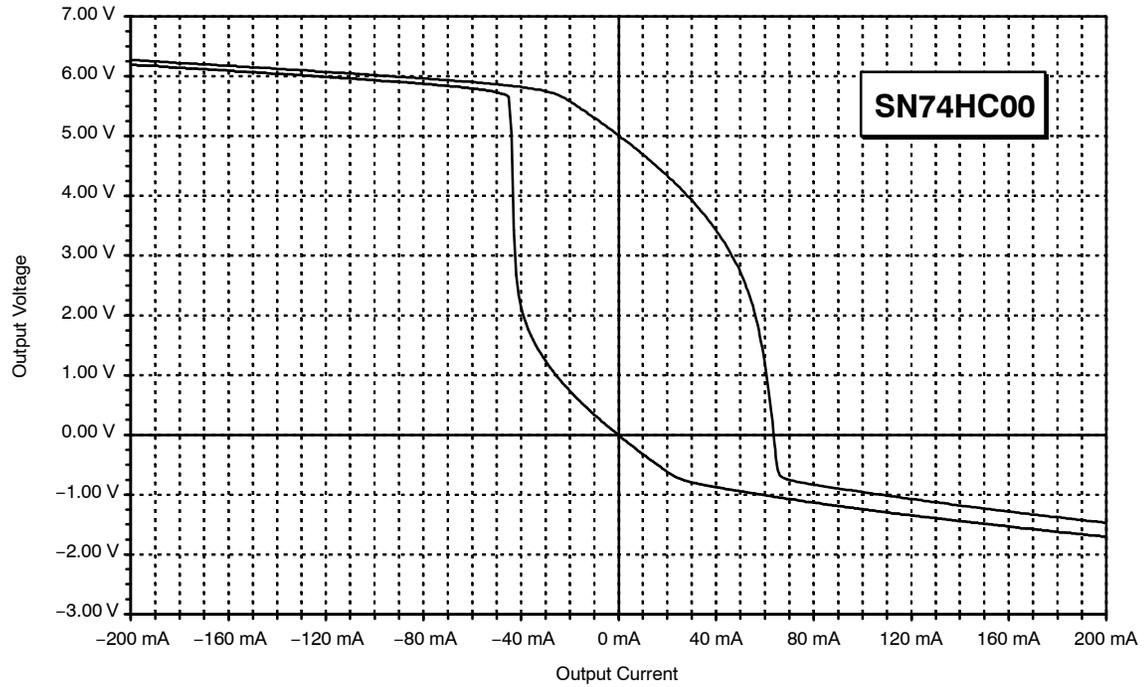
**Figure 28. Output Characteristic of the SN74F00**



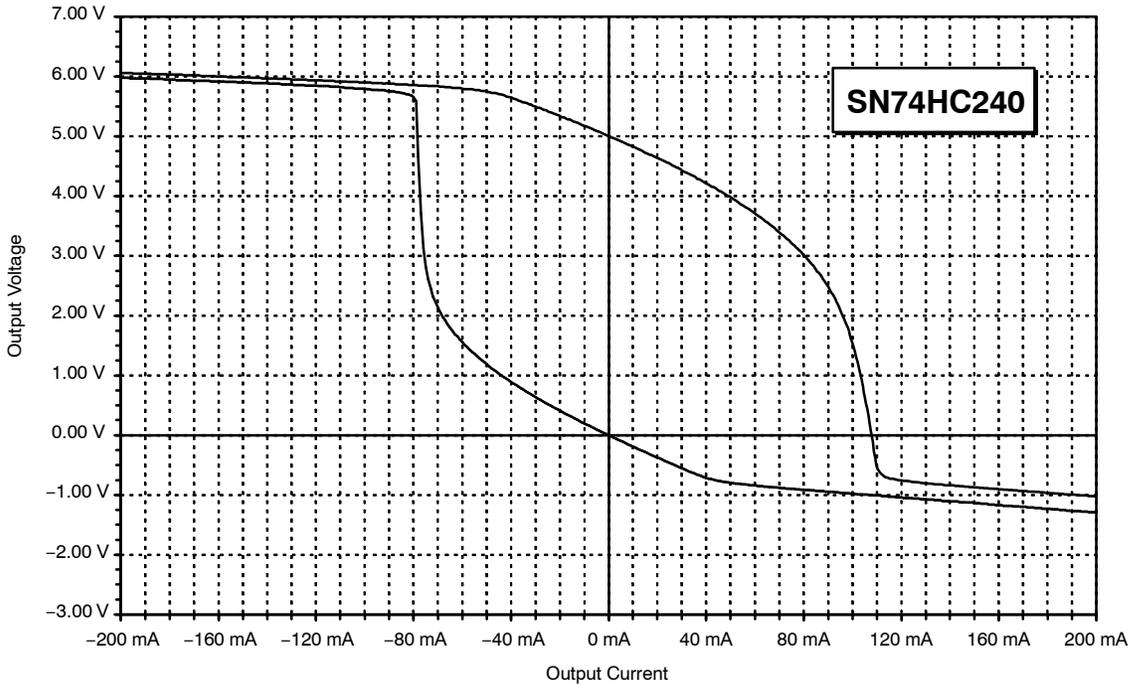
**Figure 29. Output Characteristic of the SN74F40**



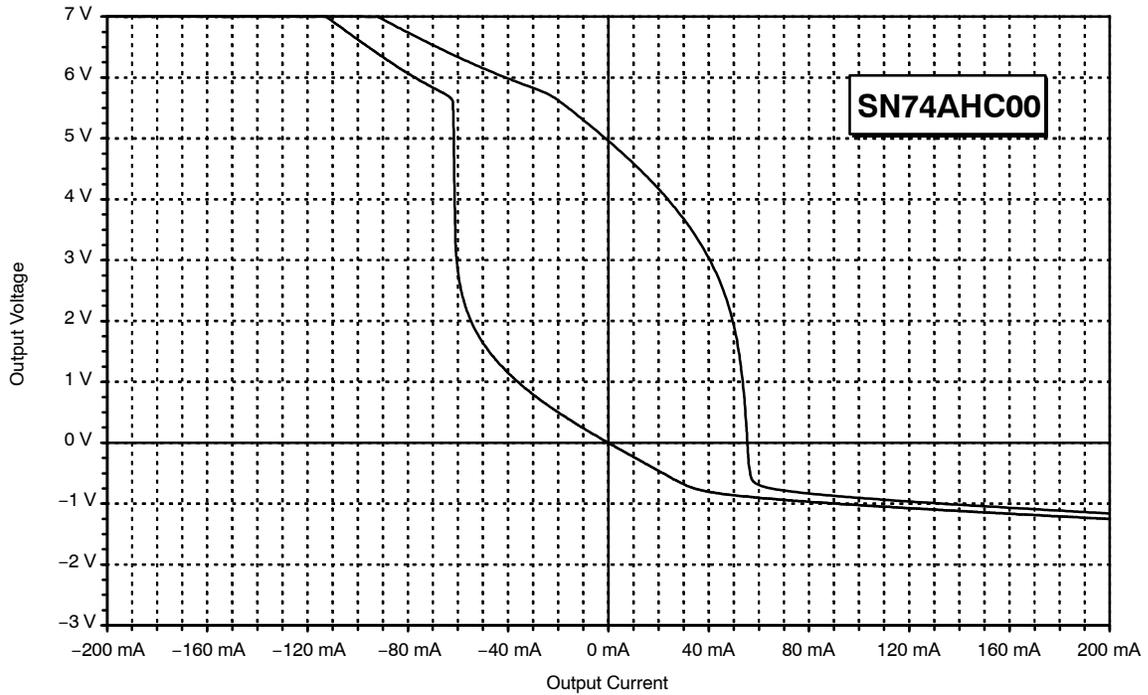
**Figure 30. Output Characteristic of the SN74F240**



**Figure 31. Output Characteristic of the SN74HC00**



**Figure 32. Output Characteristic of the SN74HC240**



**Figure 33. Output Characteristic of the SN74AHC00**

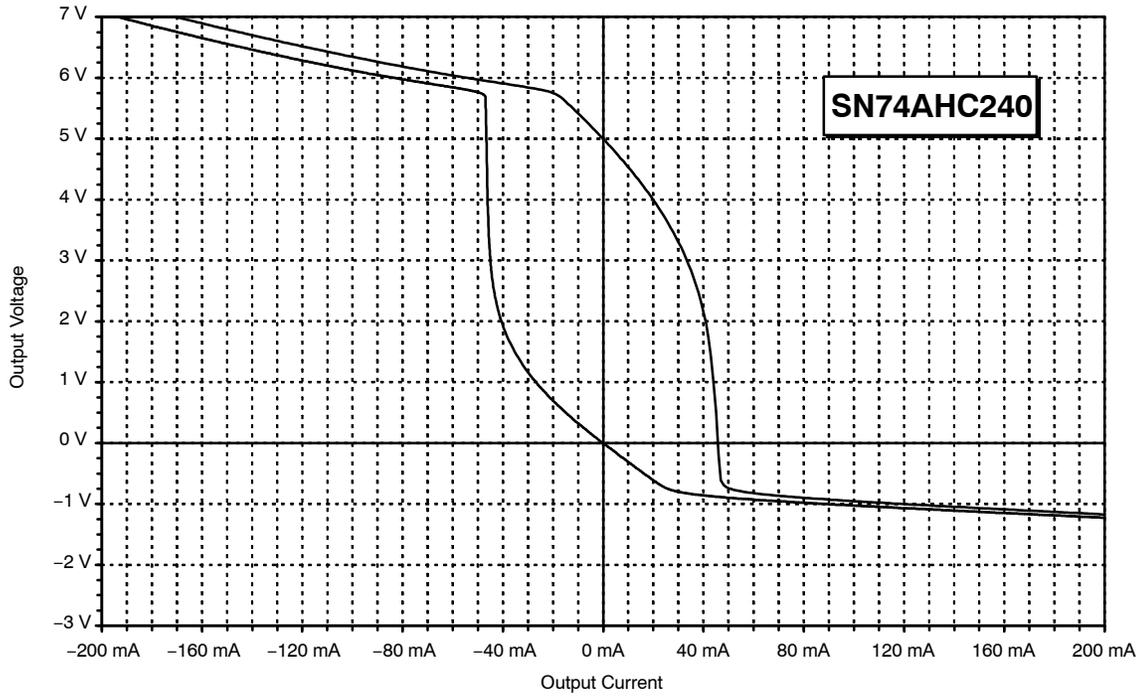


Figure 34. Output Characteristic of the SN74AHC240

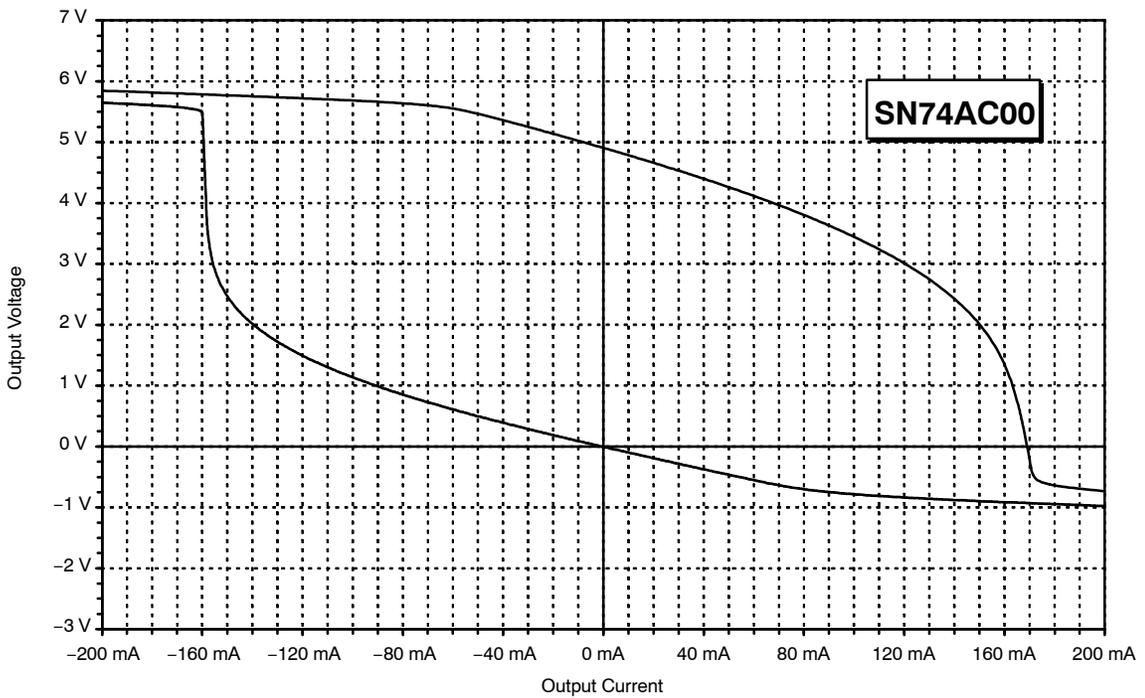
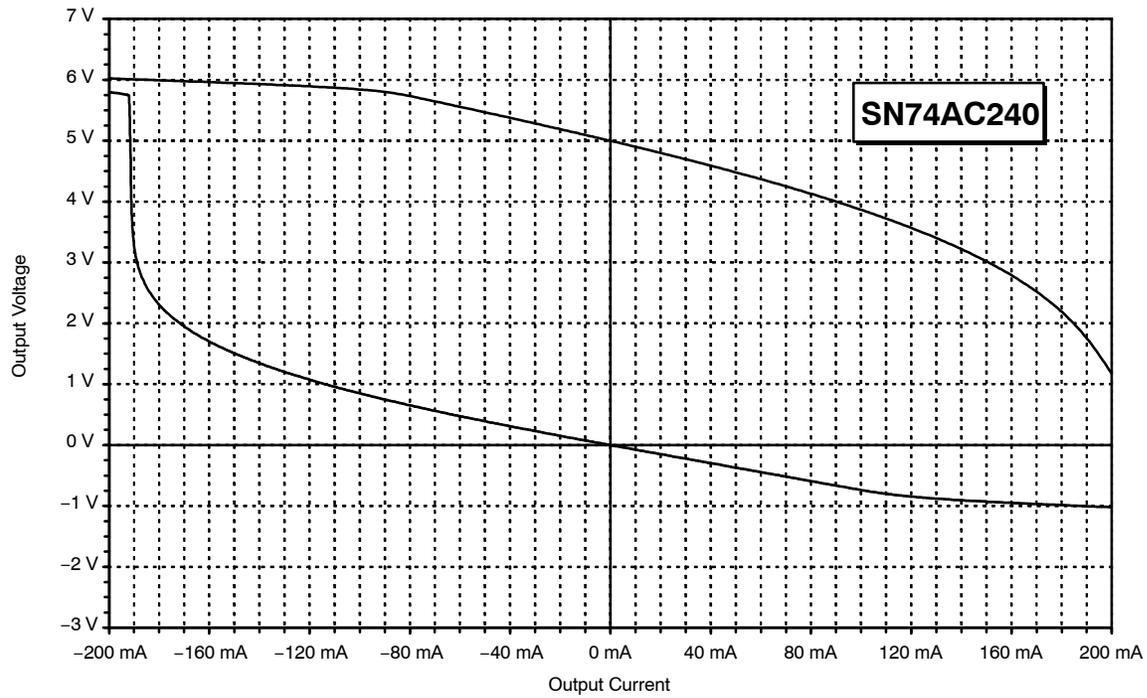
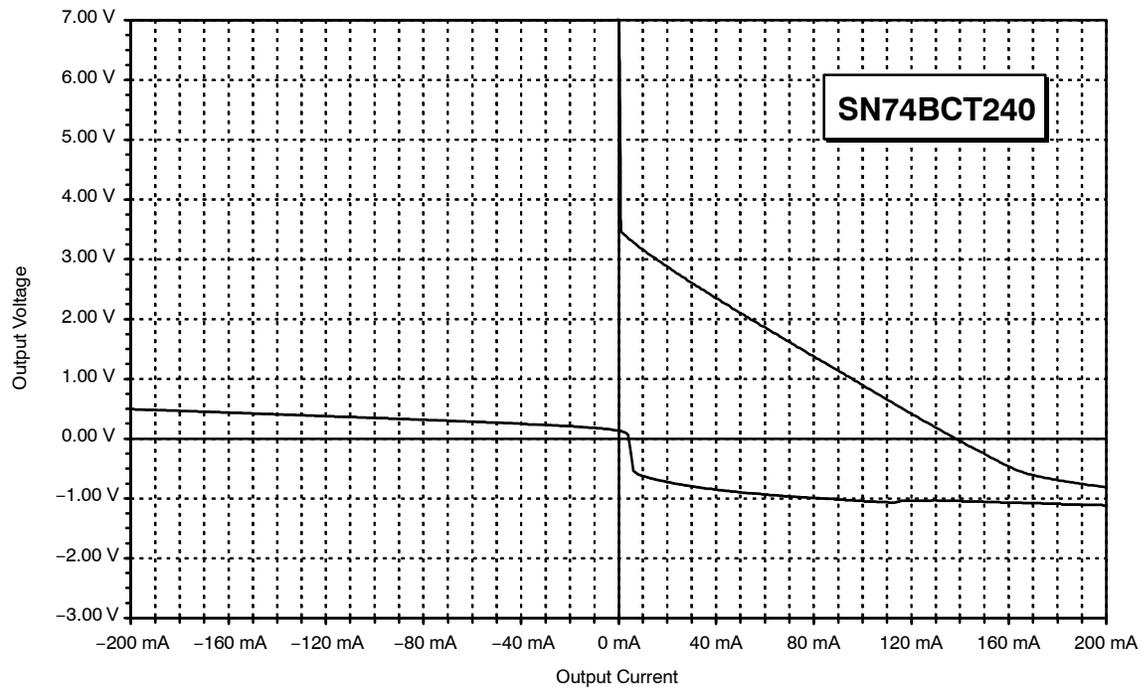


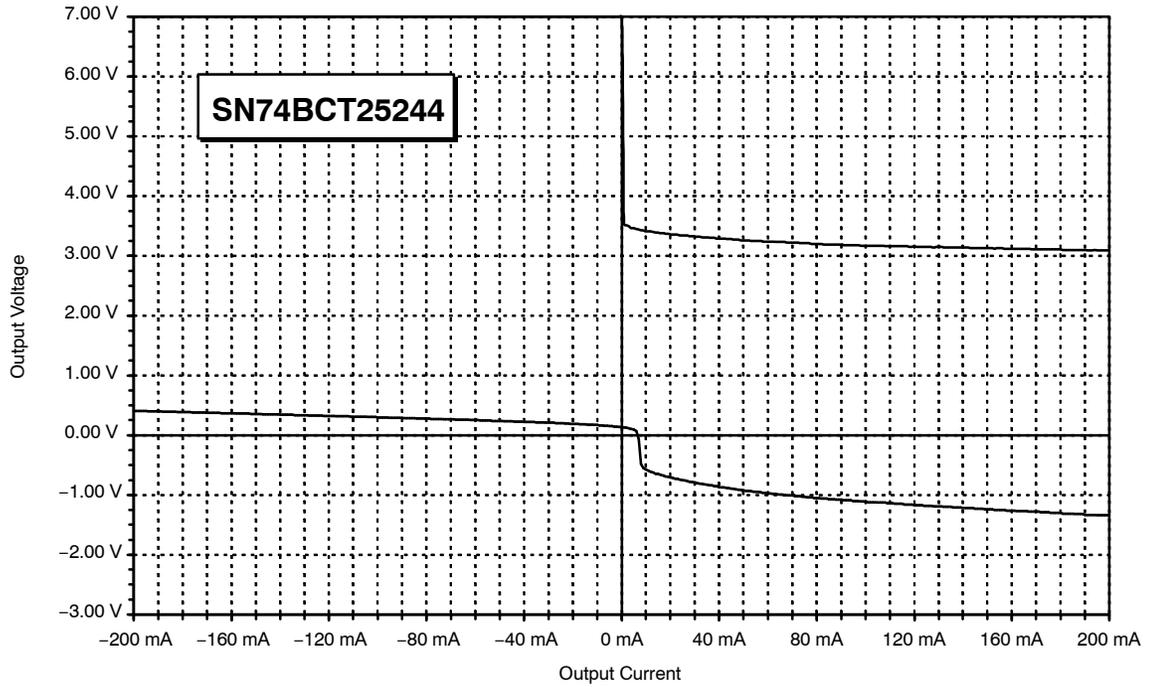
Figure 35. Output Characteristic of the SN74AC00



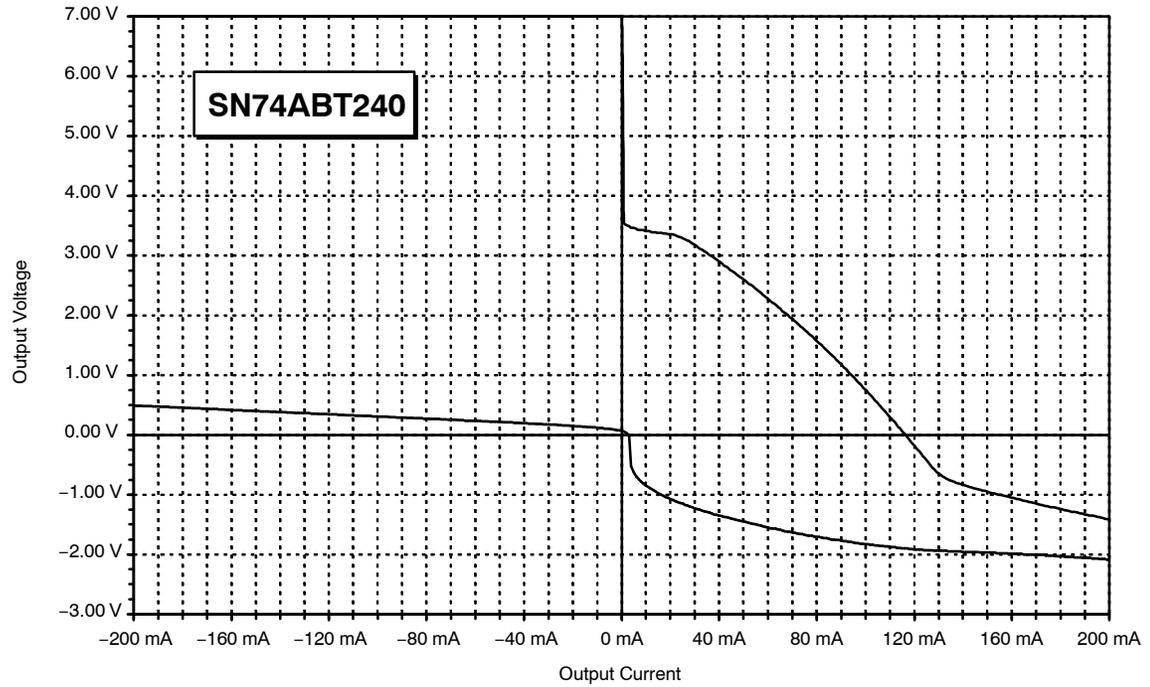
**Figure 36. Output Characteristic of the SN74AC240**



**Figure 37. Output Characteristic of the SN74BCT240**



**Figure 38. Output Characteristic of the SN74BCT25244**



**Figure 39. Output Characteristic of the SN74ABT240**

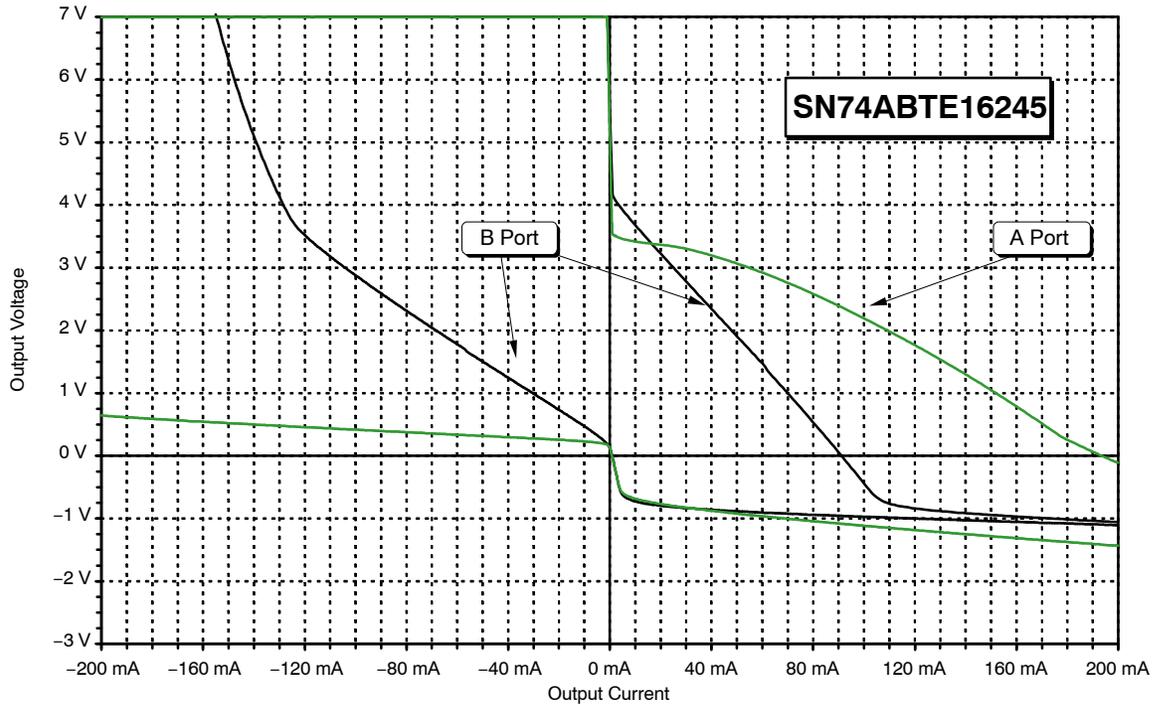


Figure 40. Output Characteristic of the SN74ABTE16245

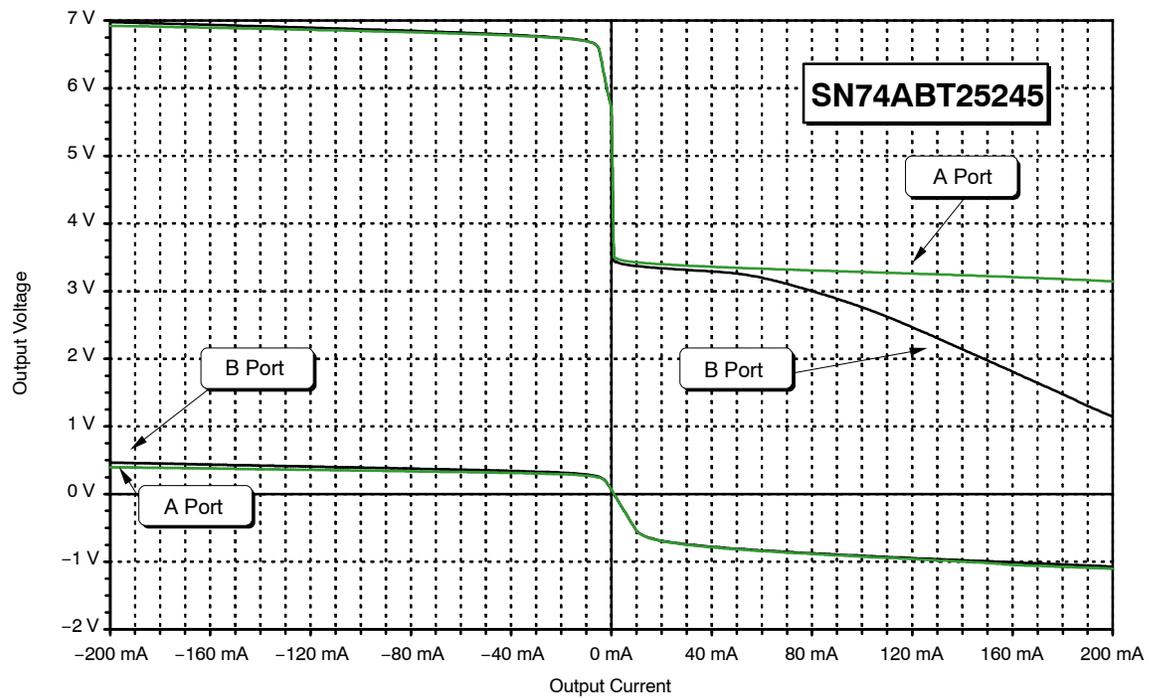


Figure 41. Output Characteristic of the SN74ABT25245

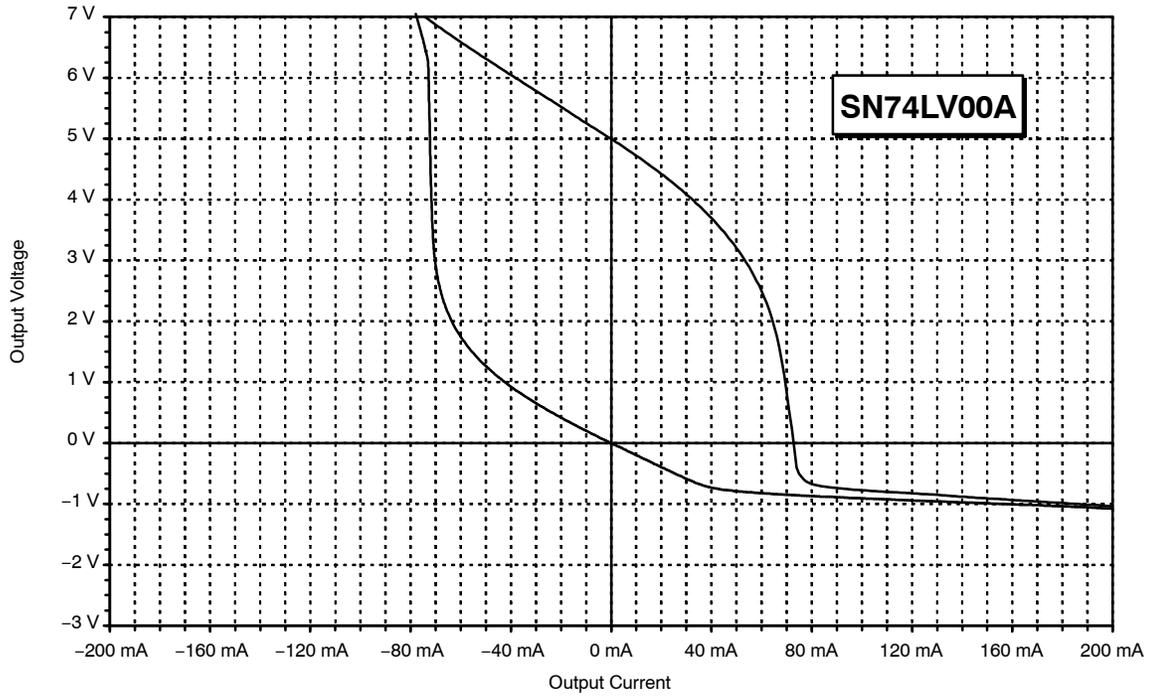


Figure 42. Output Characteristic of the SN74LV00A

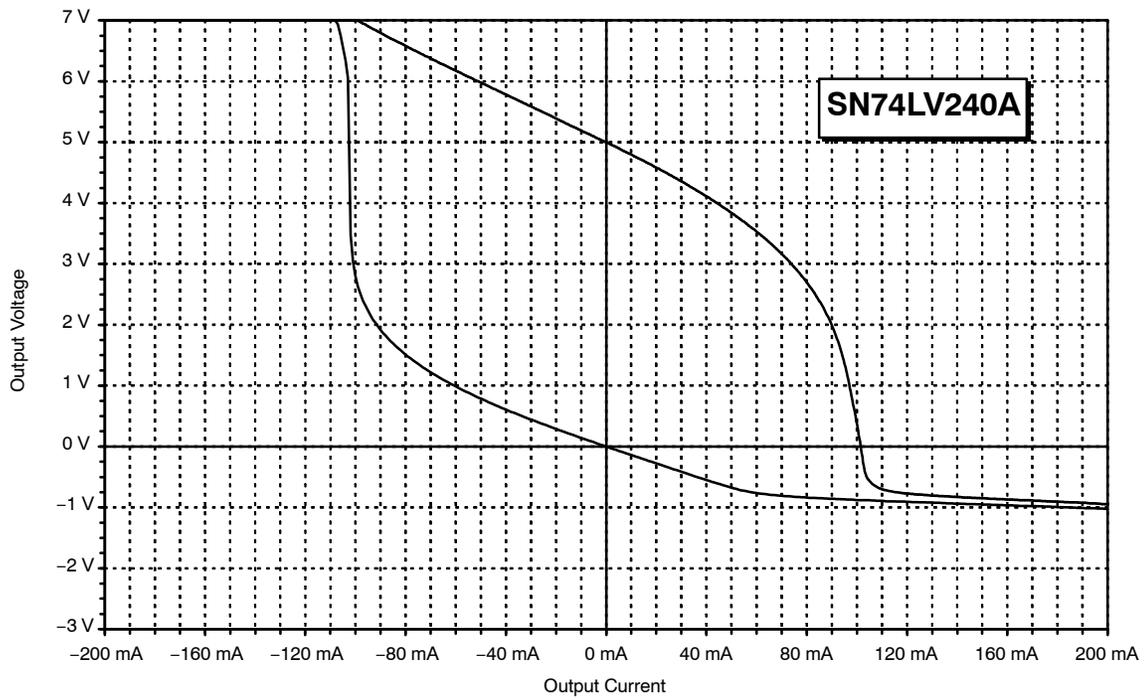


Figure 43. Output Characteristic of the SN74LV240A

## 4 Bergeron Method Applied to the SN74AHC240

The input and output characteristics, shown in Section 1, *Introduction*, and Section 3, *Output Characteristics*, can be used to determine the signal reflections within a certain application using a graphical procedure known as the Bergeron method.

The prerequisite to using the Bergeron method is that the lines must exceed a certain length. There is a simple rule:

*If the rise time or the fall time of a signal is shorter than twice the propagation delay on the line, the line theories must be applied.*

Practically, this means that for a line with a signal propagation time of 5 ns/m and a signal with a rising or falling edge of 2 ns, starting with a line length that exceeds 20 cm [ $2 \text{ ns} / (5 \text{ ns/m} \times 2)$ ], the line theory must be applied.

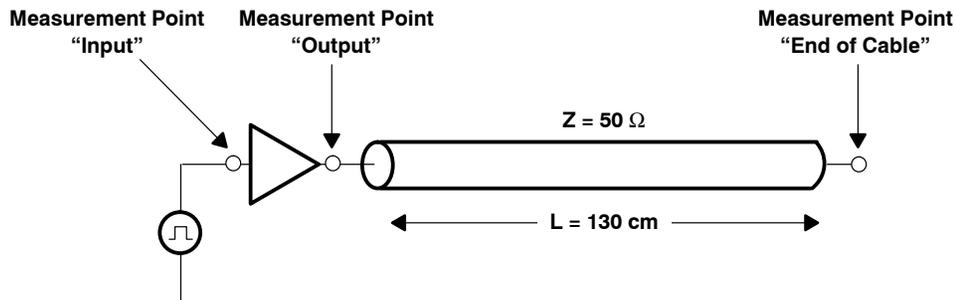
For a bus line, the signal propagation delay increases to 25 ns/m, so that, in this case, the line theory must be applied for a line that exceeds 4 cm [ $2 \text{ ns} / (25 \text{ ns/m} \times 2)$ ].

In the example, the SN74AHC240 device was tested. The Bergeron method was used to determine the signal shape in advance. The measurement setup is shown in Figure 44.

Practically, this means, that for a line with a signal propagation of 5 ns/m and a signal with a rising or falling edge of 2 ns, starting with a line length that exceeds 20 cm [ $2 \text{ ns} / (5 \text{ ns/m} \times 2)$ ], the line theory must be applied.

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In the example, the SN74AHC240 device was tested. The Bergeron method was used to determine the signal shape in advance. The measurement setup is shown in Figure 44.



**Figure 44. Measurement Setup for the Bergeron Method**

The first step in doing the graphical solution using the Bergeron method is to draw the output and load characteristics in a voltage-versus-current diagram:

- Output characteristic of the device SN74AHC240
- Load characteristic at the end of the line

The output characteristic is taken directly from Figure 45. The load characteristic equals the Y-axis for the investigated case, because no resistor is connected to the end of the line ( $R_L = \infty$ ).

The intersection between the load characteristic and the output characteristic represents the steady states and the current and voltage values at the line start and the end of the line at the time  $t < 0$ , respectively.

## 4.1 Voltage Value at the Output of the Driver

For the low-to-high transition, a straight line is drawn, starting at the intersection of the output low characteristic and the load characteristic. For the high-to-low transition, the straight line starts at the cross point of output high characteristic and the load characteristic.

The line impedance,  $Z_O$ , determines the steepness of this line. In the example, the line impedance is  $50 \Omega$ .

The intersection of this straight line and the output characteristics gives the voltage and current values at the beginning of the line at the time  $t = 0$ .

## 4.2 Voltage Value at End of the Line

Now, a straight line with the steepness  $-Z_O$  is drawn through this point. The intersection between this line and the load characteristic gives the voltage values at the end of the line after one propagation delay time of the line, that is after time  $t = 1$ .

Afterwards, the procedure will be repeated, applying straight lines to the output characteristic and the load characteristic.

The steepness of the straight line is:

- $Z_O$  from the output characteristic to the load characteristic and
- $-Z_O$  from the load characteristic to the output characteristic.

In this way, the current/voltage values are determined:

- at the end of the line, at the times  $t = 1, 3, 5 \dots$
- at the beginning of the line, at the times  $t = 2, 4, 6 \dots$

The Bergeron diagram is shown in Figure 45. The related diagram, which shows the line reflections, is shown in Figure 46.

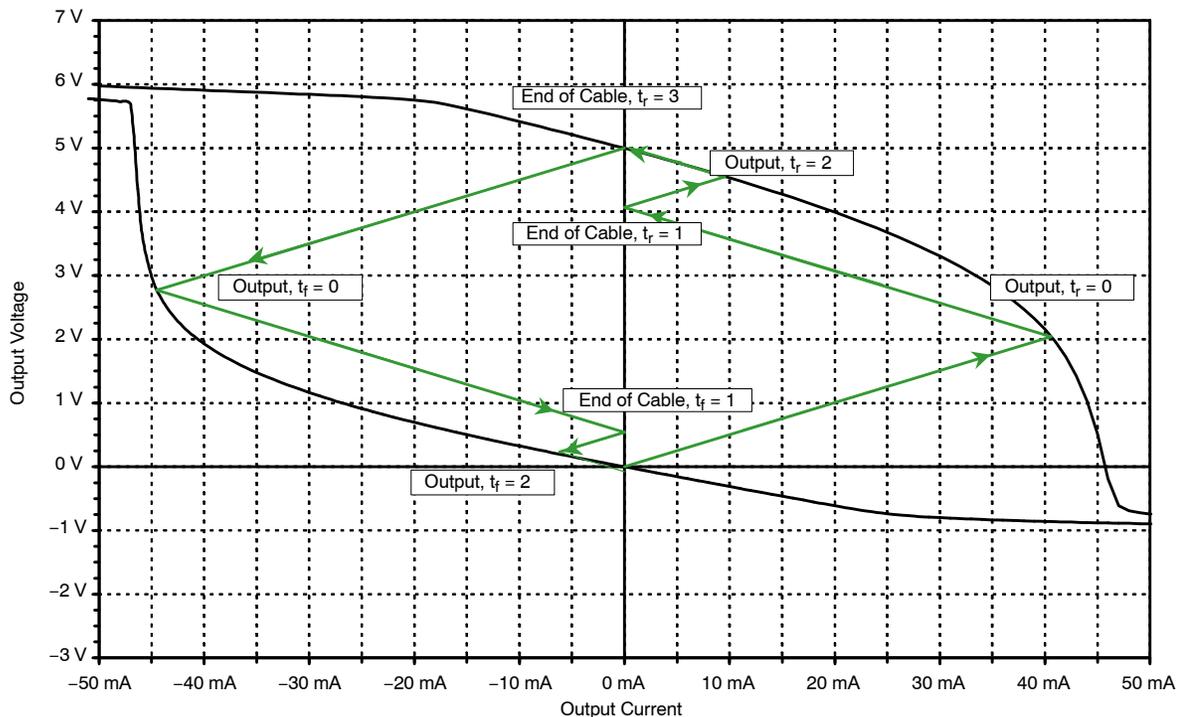
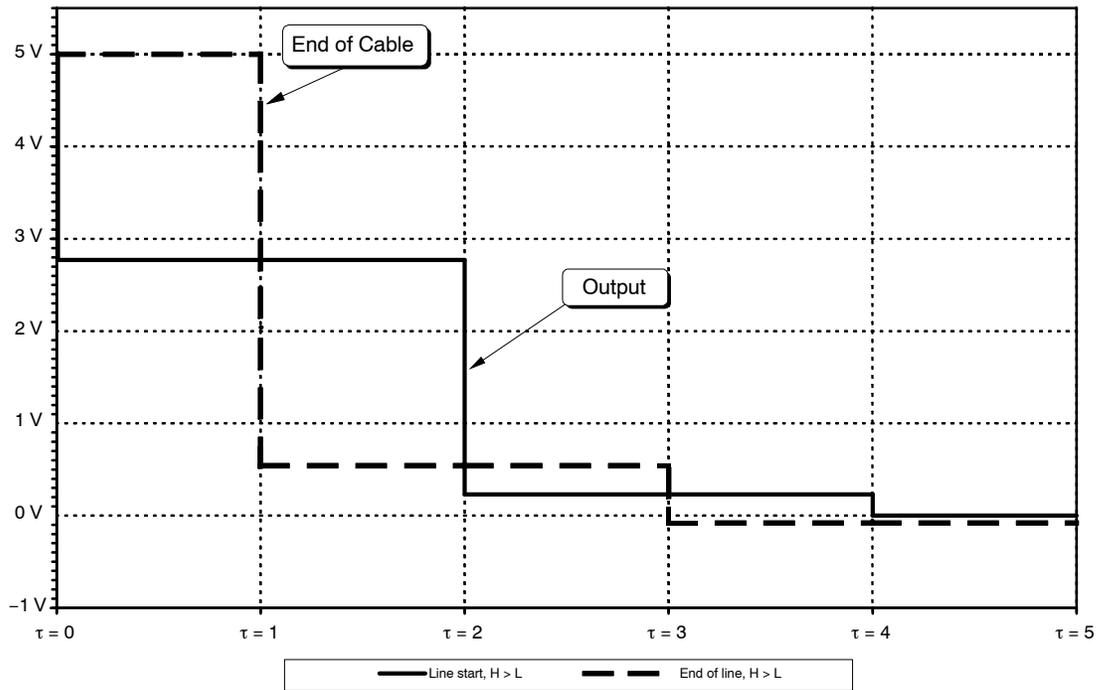
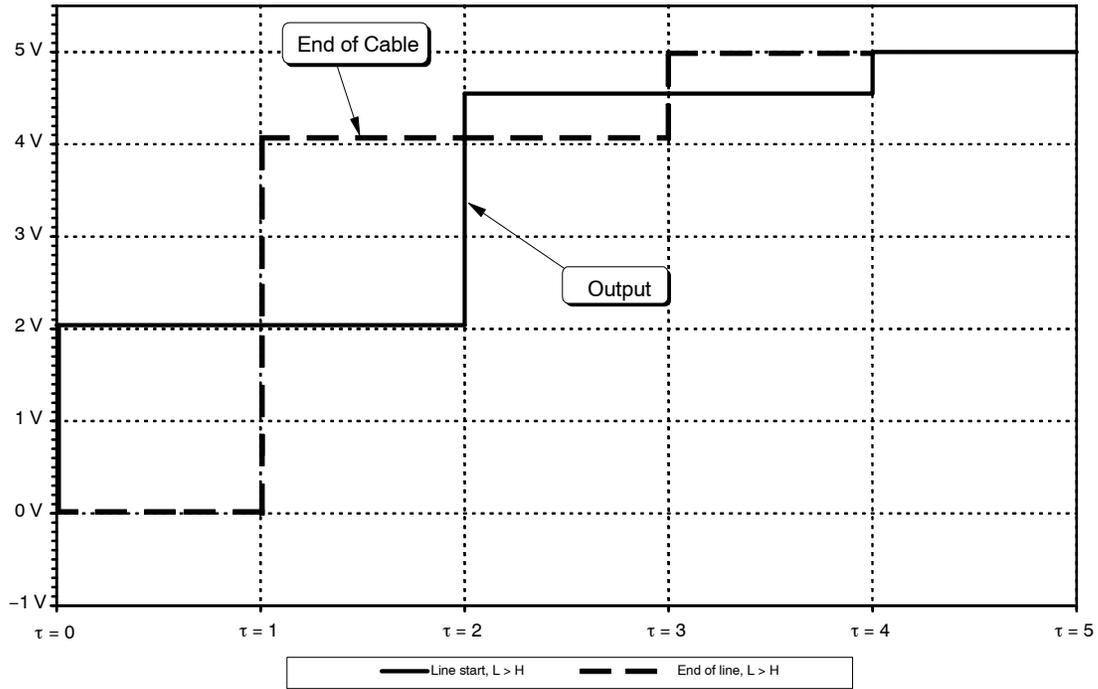
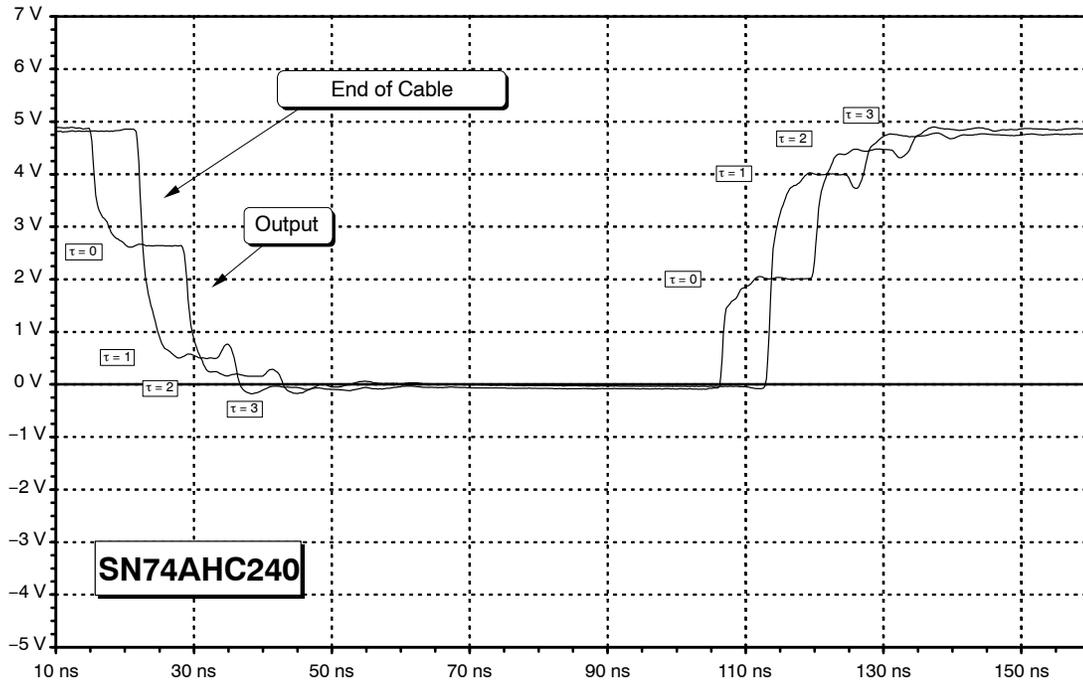


Figure 45. Bergeron Diagram for the SN74AHC240



**Figure 46. Diagram of Line Reflections for the SN74AHC240**

Figure 47 shows the line-reflection measurement results for the SN74AHC240.

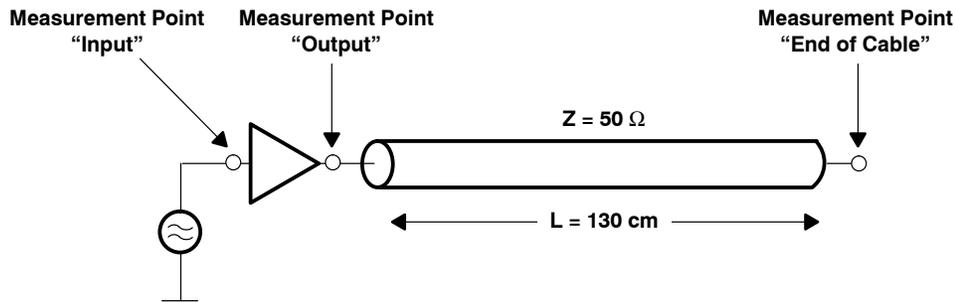


**Figure 47. Signal Shape of the SN74AHC240**

The calculated values using the Bergeron procedure match very well with the measurement of the signal shapes. The TI application report, *The Bergeron Method: A Graphic Method for Determining Line Reflections in Transient Phenomena*, literature number SDYA014, describes the graphic procedure in more detail.

## 5 Output Waveforms

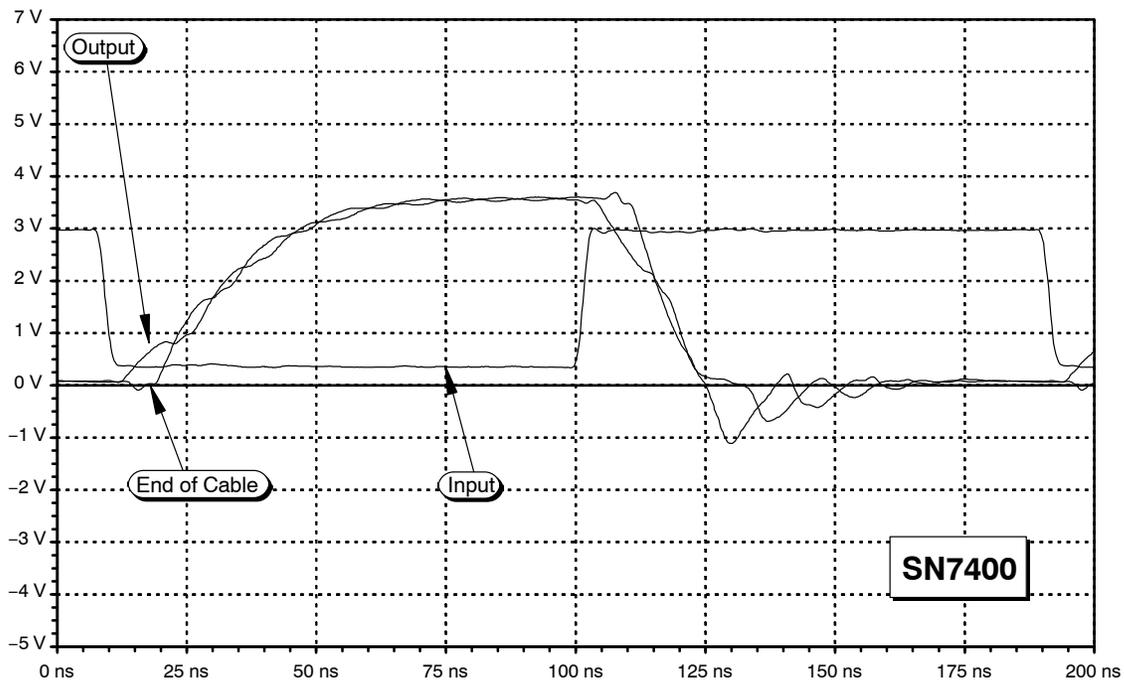
The measurement setup shown in Figure 48 is used to obtain the voltage waveforms of typical output stages (see Figures 49 through 77).



**Figure 48. Measurement Setup for the Bergeron Method**

For these measurements, the devices under test were loaded with a 1.3-m-long coaxial cable having a characteristic impedance of  $50\ \Omega$ . The end of the line was not connected, i.e., open circuit.

These waveforms provide good insight into the dynamic behavior of the components. In particular, the oscillograms provide information regarding drive capability with a low-resistance load, together with an indication of the line reflections that can be expected.



**Figure 49. Output Waveforms of the SN7400**

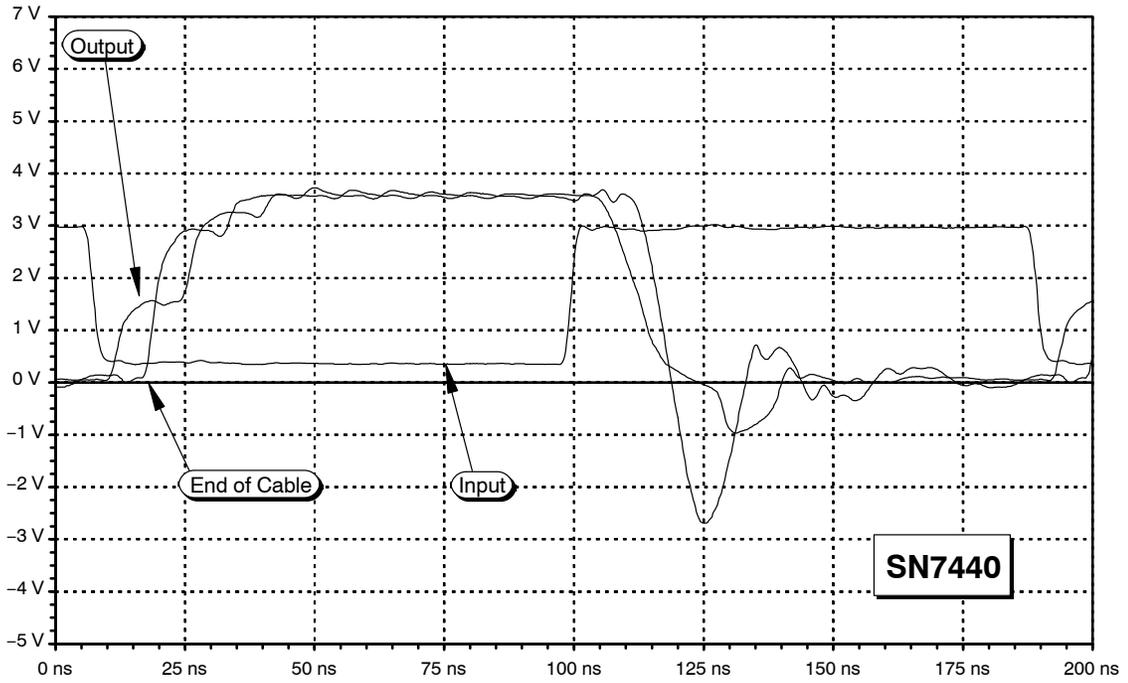


Figure 50. Output Waveforms of the SN7440

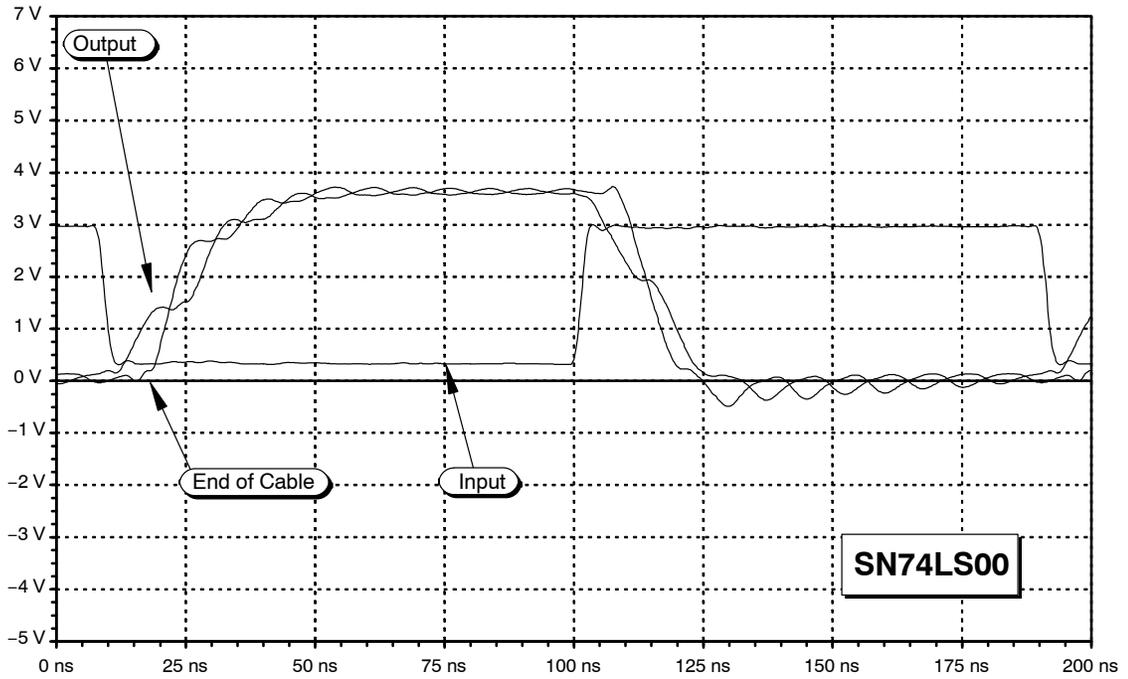


Figure 51. Output Waveforms of the SN74LS00

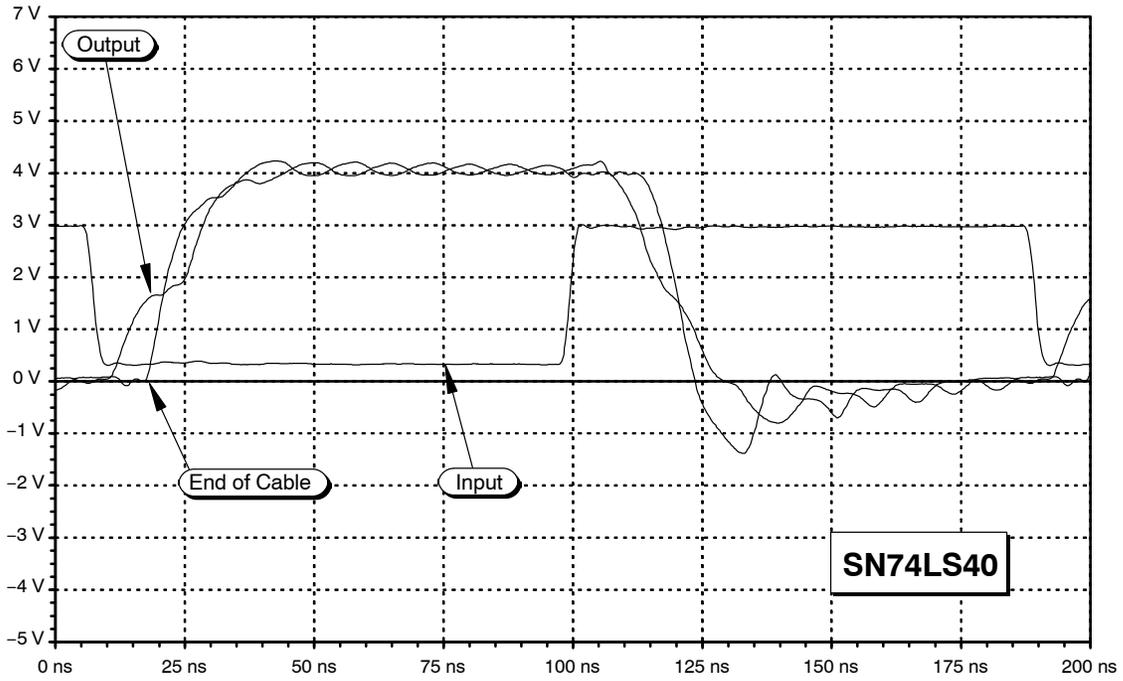


Figure 52. Output Waveforms of the SN74LS40

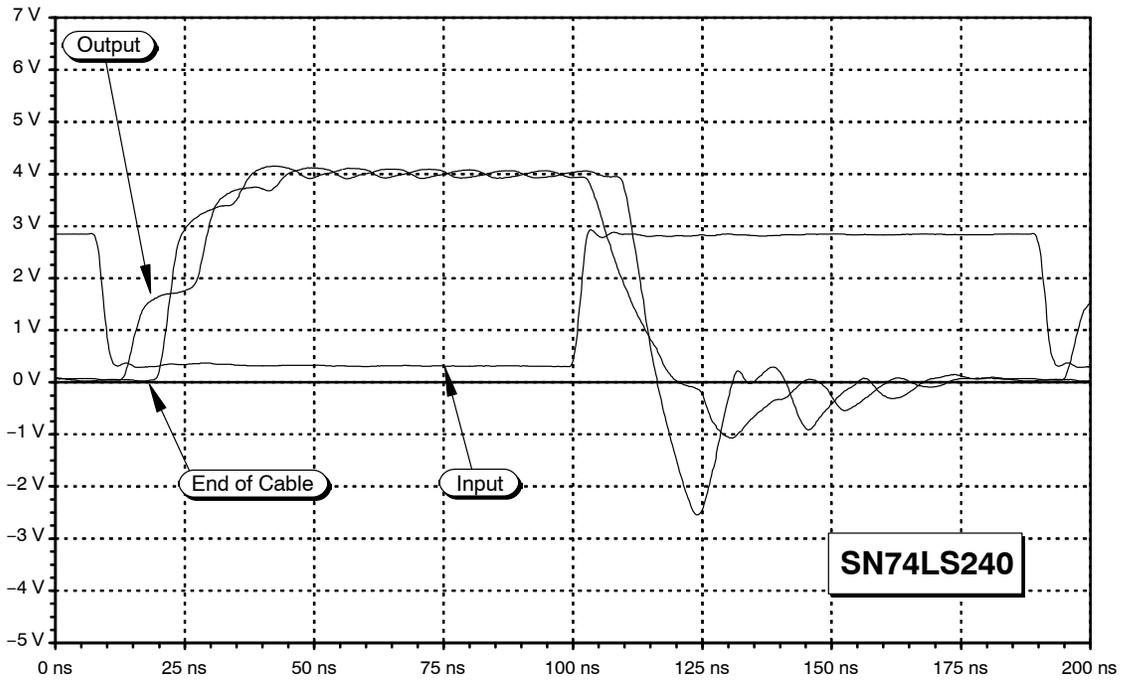
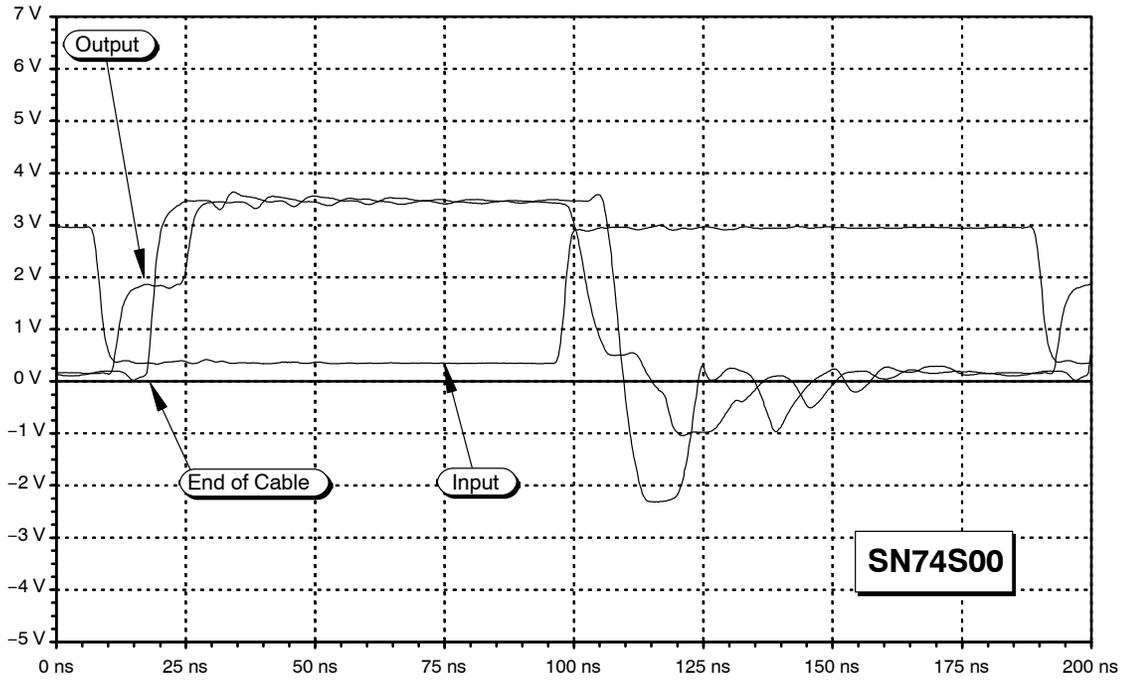
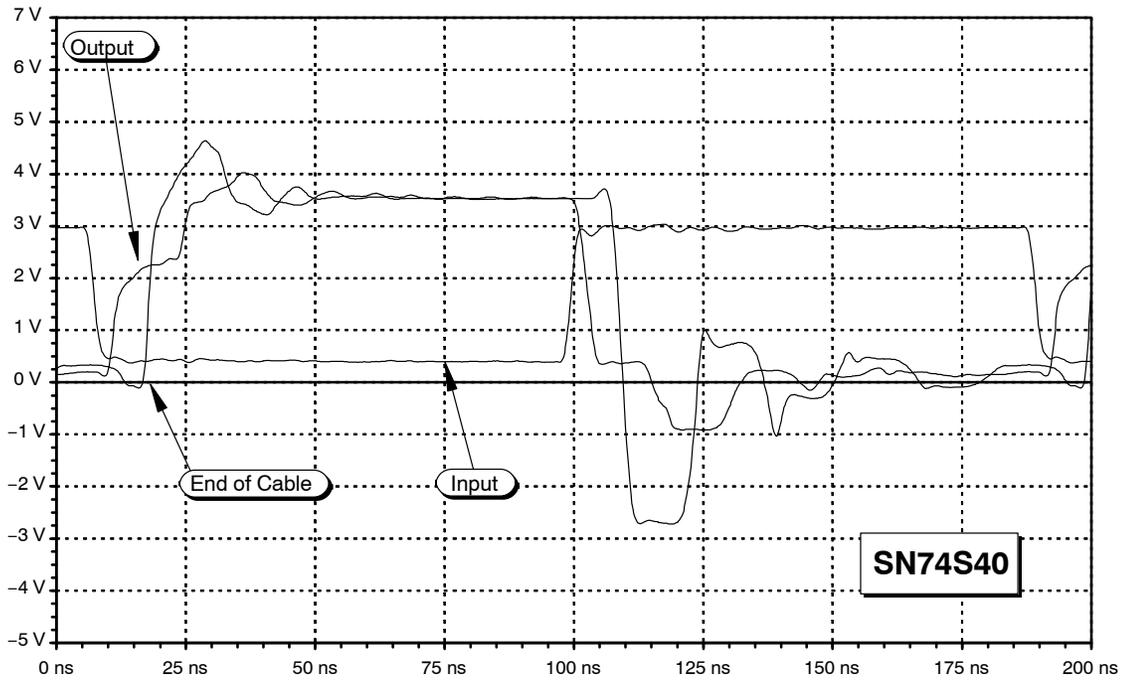


Figure 53. Output Waveforms of the SN74LS240



**Figure 54. Output Waveforms of the SN74S00**



**Figure 55. Output Waveforms of the SN74S40**

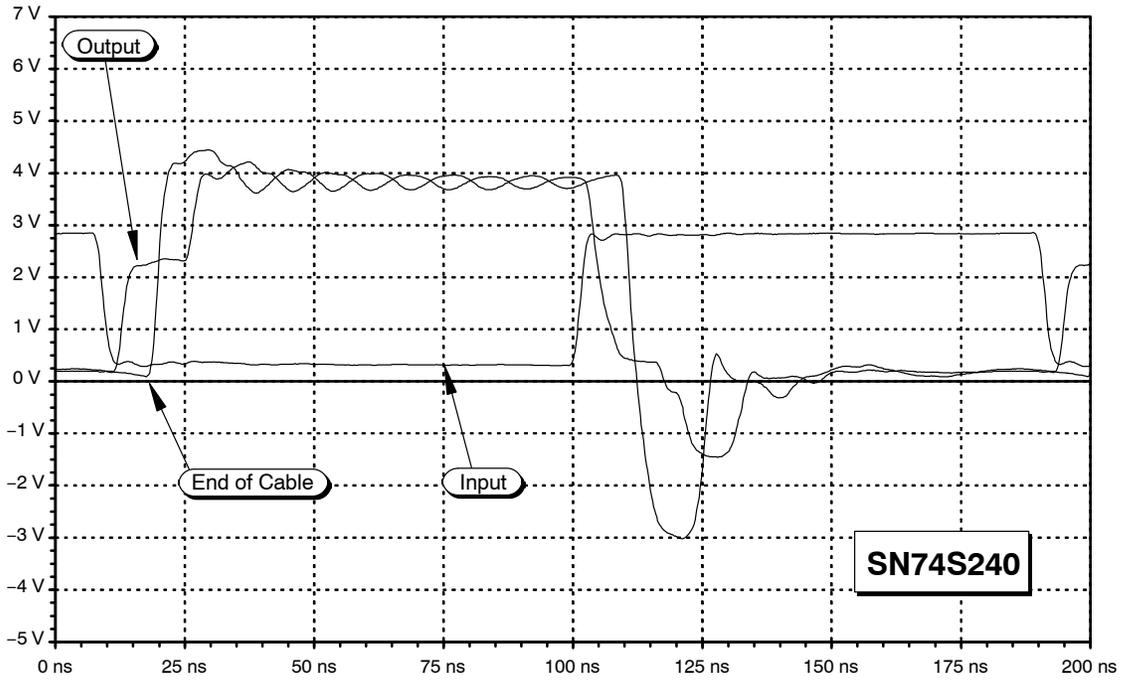


Figure 56. Output Waveforms of the SN74S240

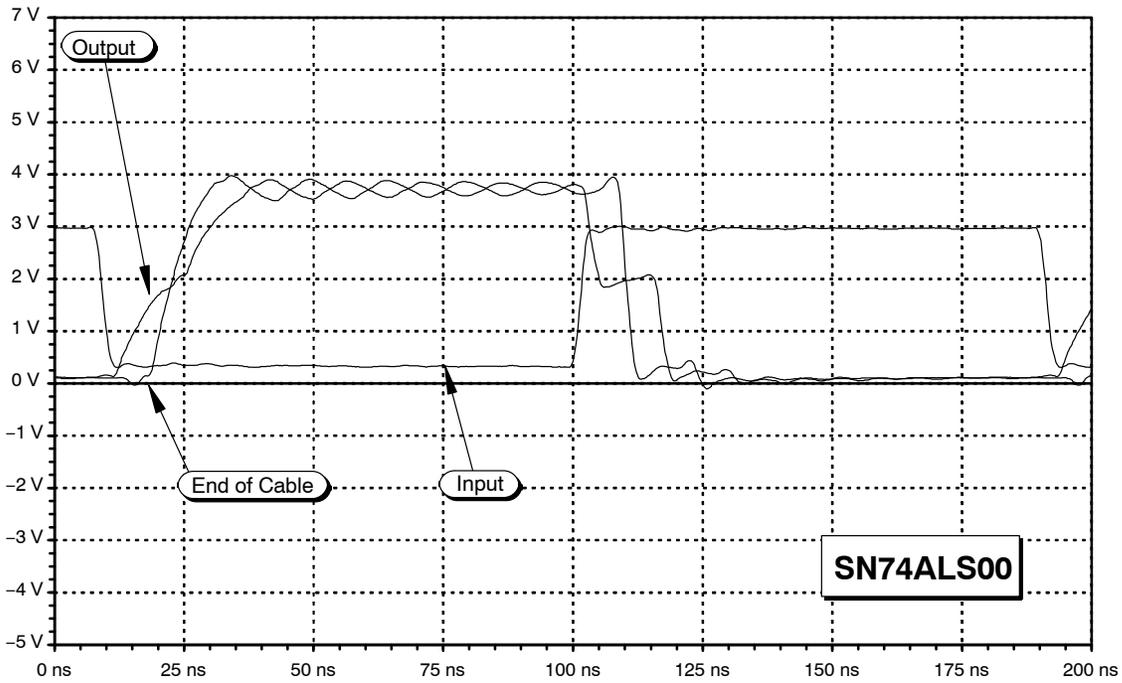


Figure 57. Output Waveforms of the SN74ALS00

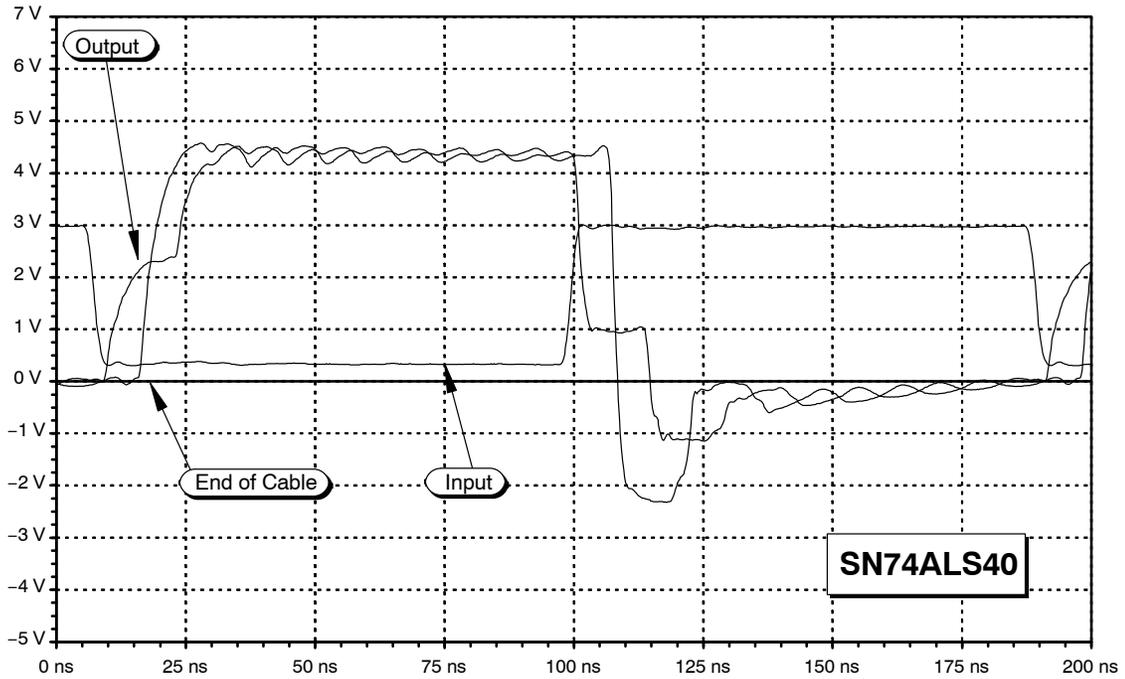


Figure 58. Output Waveforms of the SN74ALS40

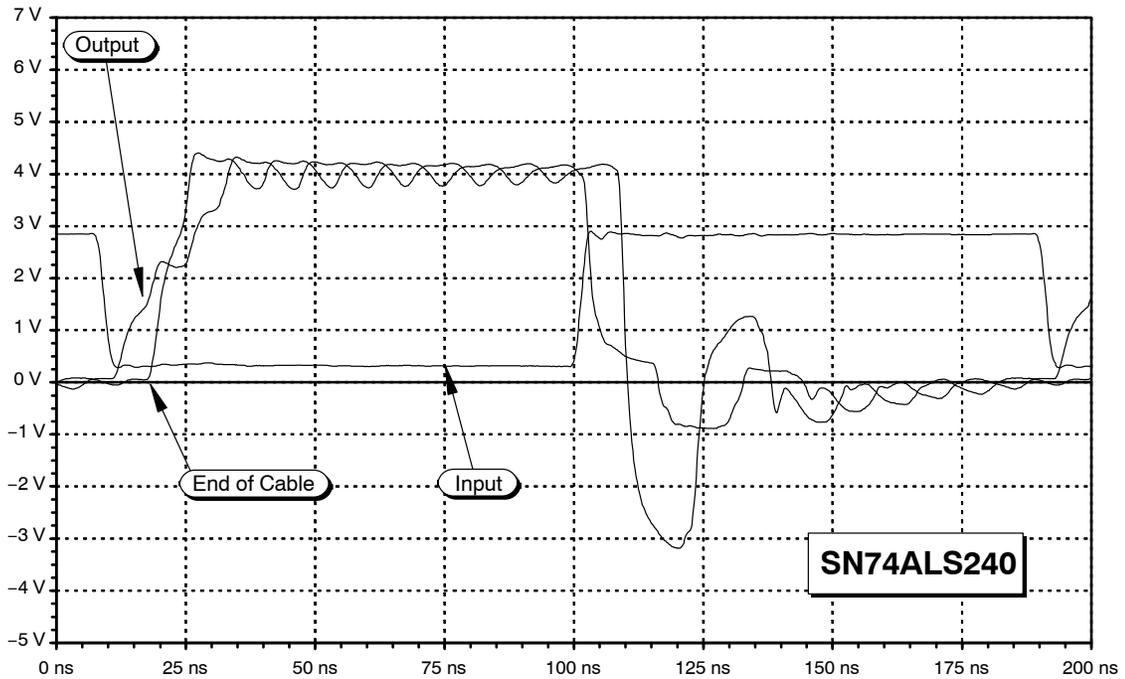


Figure 59. Output Waveforms of the SN74ALS240

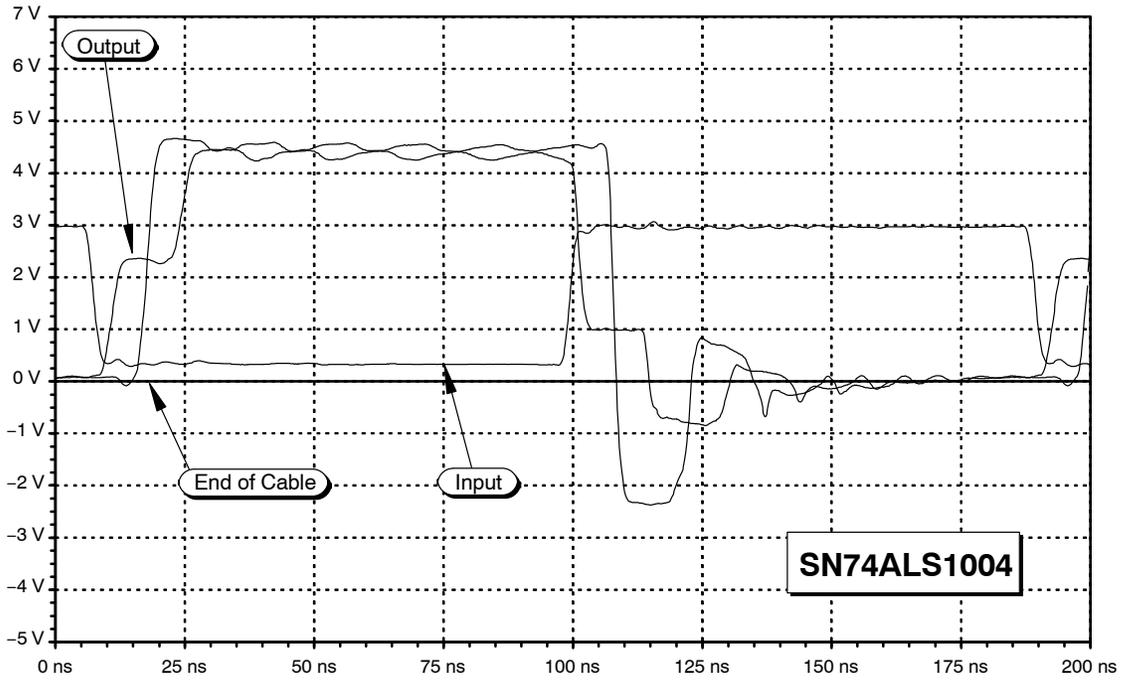


Figure 60. Output Waveforms of the SN74ALS104

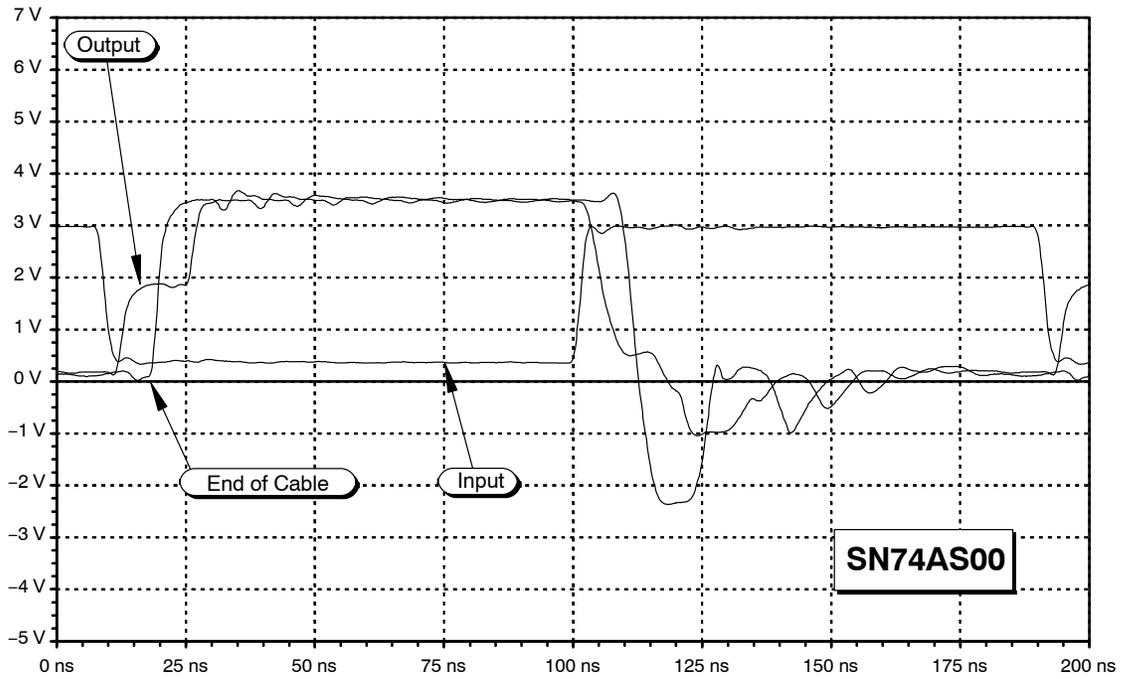
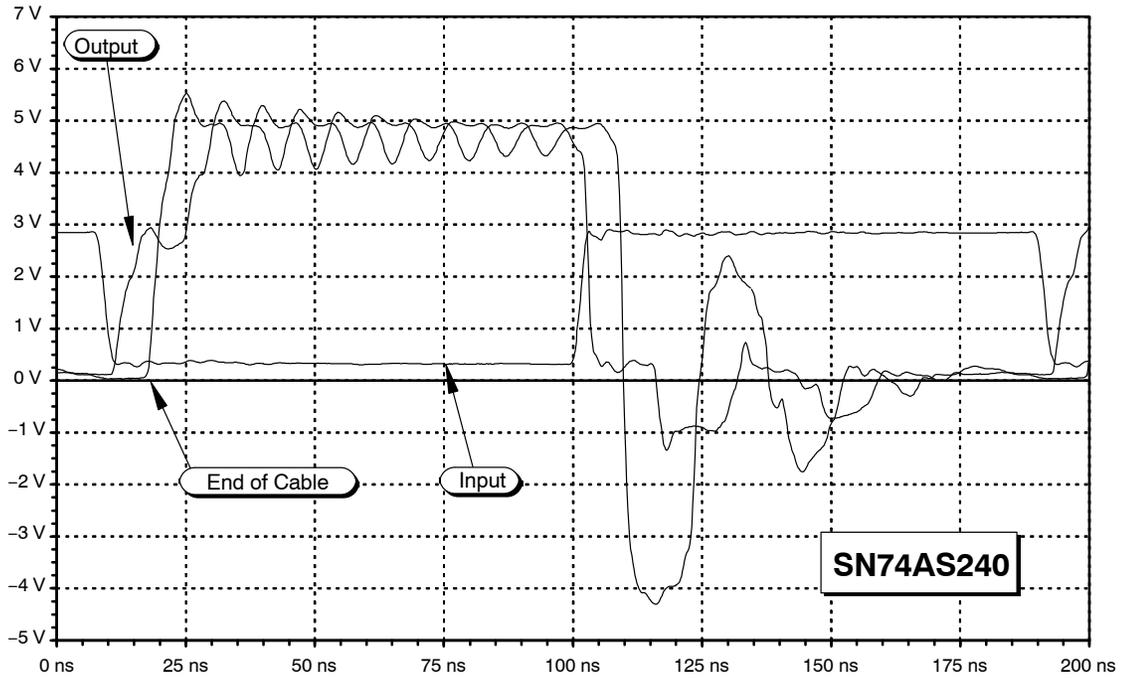
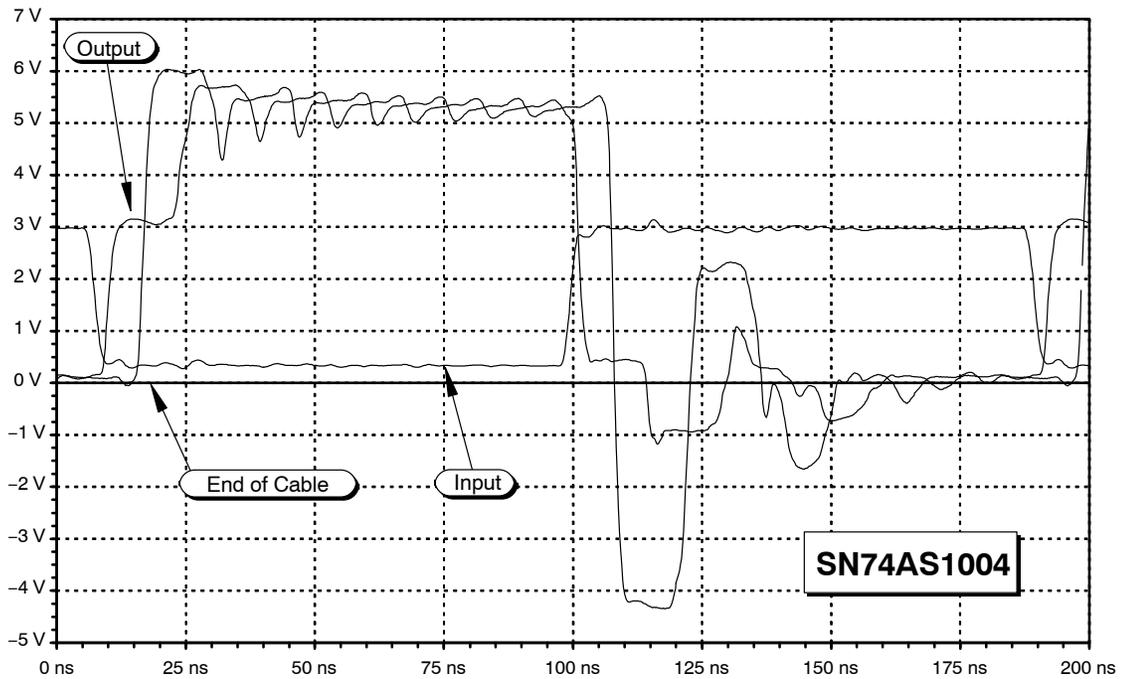


Figure 61. Output Waveforms of the SN74AS00



**Figure 62. Output Waveforms of the SN74AS240**



**Figure 63. Output Waveforms of the SN74AS1004**

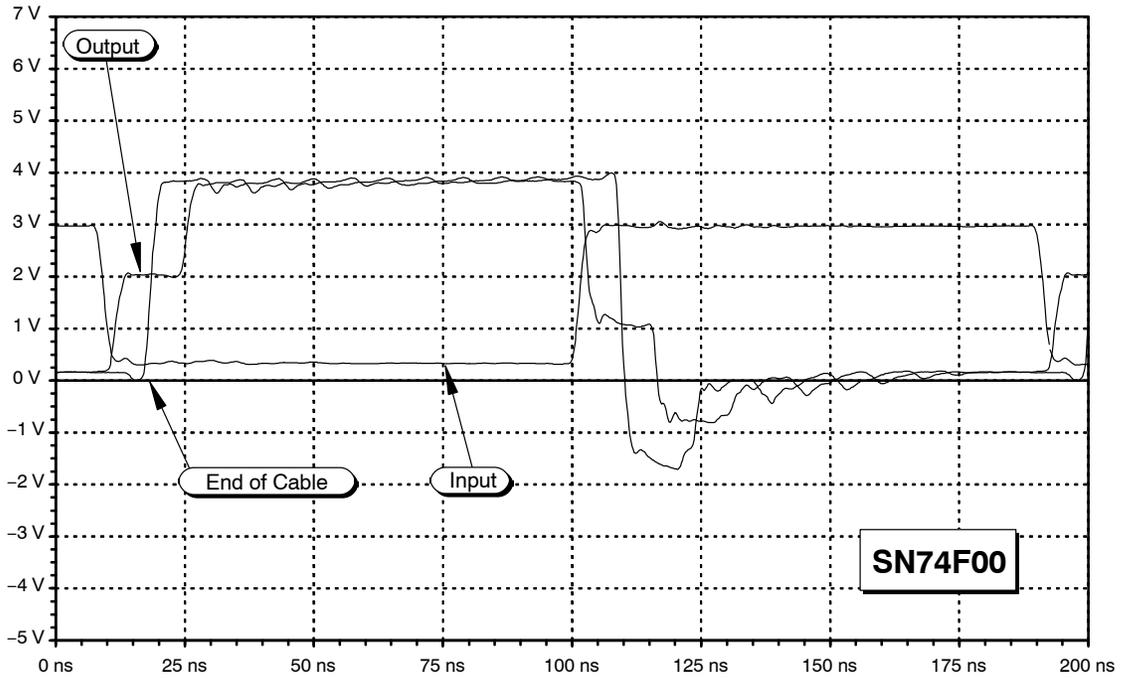


Figure 64. Output Waveforms of the SN74F00

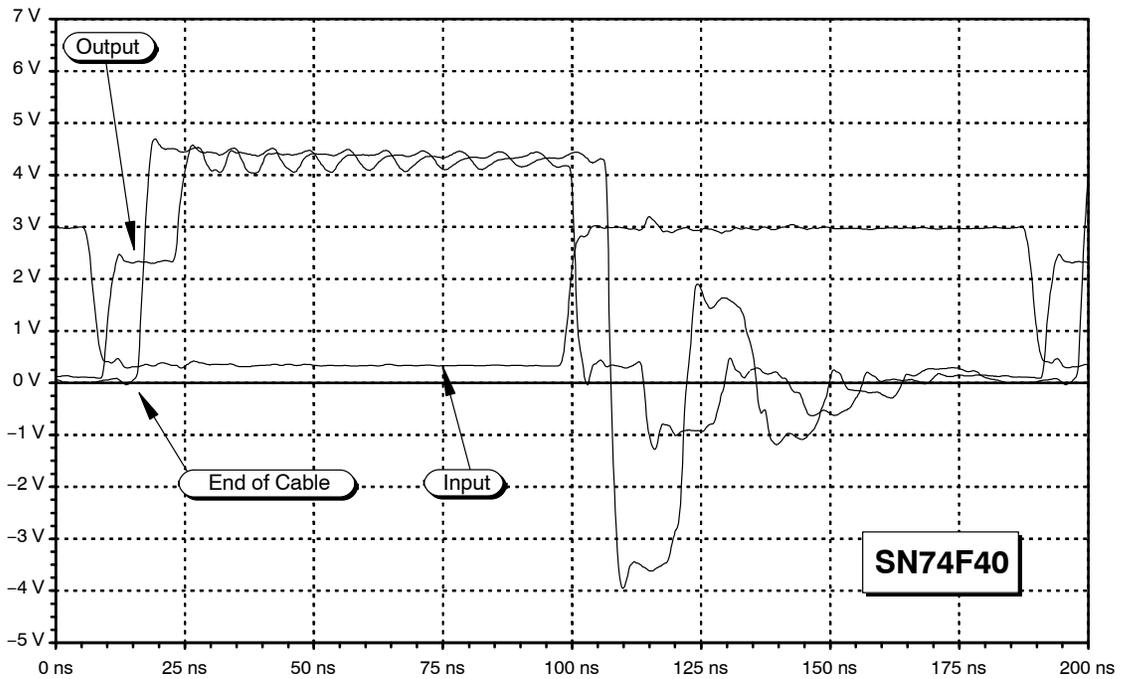


Figure 65. Output Waveforms of the SN74F40

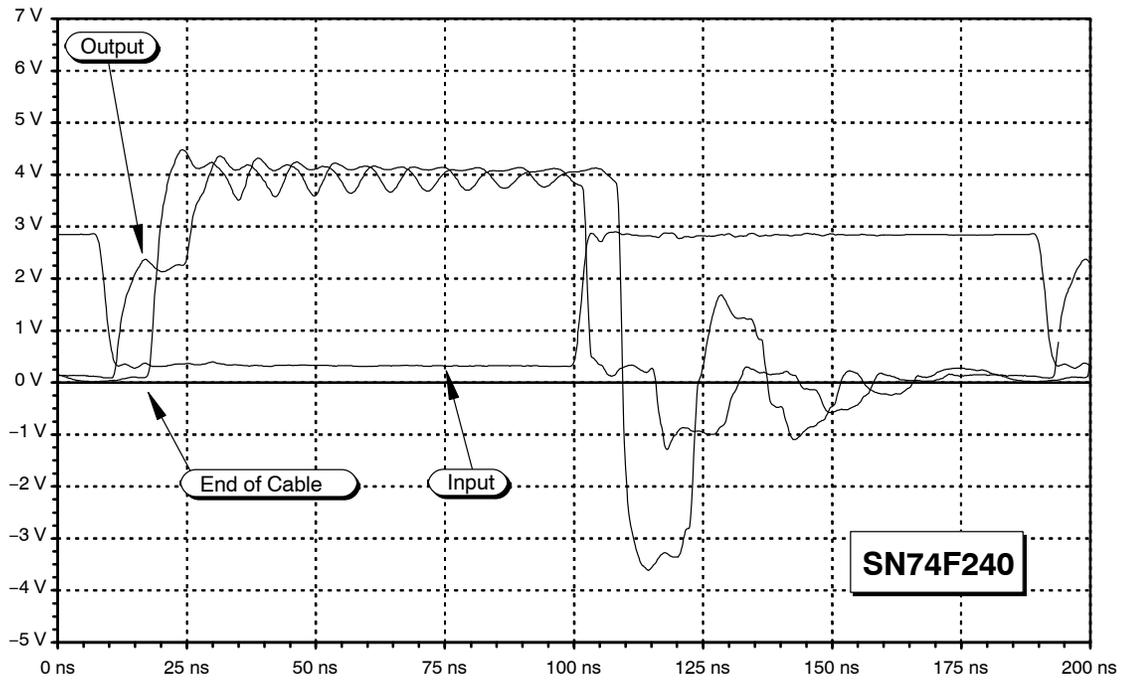


Figure 66. Output Waveforms of the SN74F240

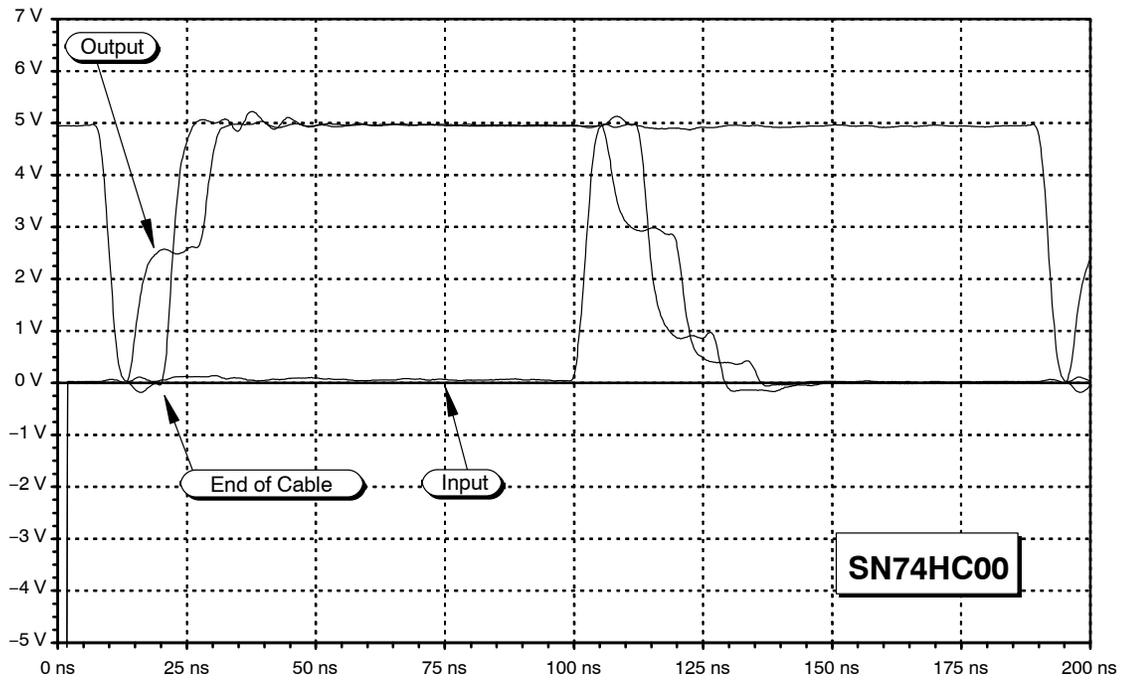


Figure 67. Output Waveforms of the SN74HC00

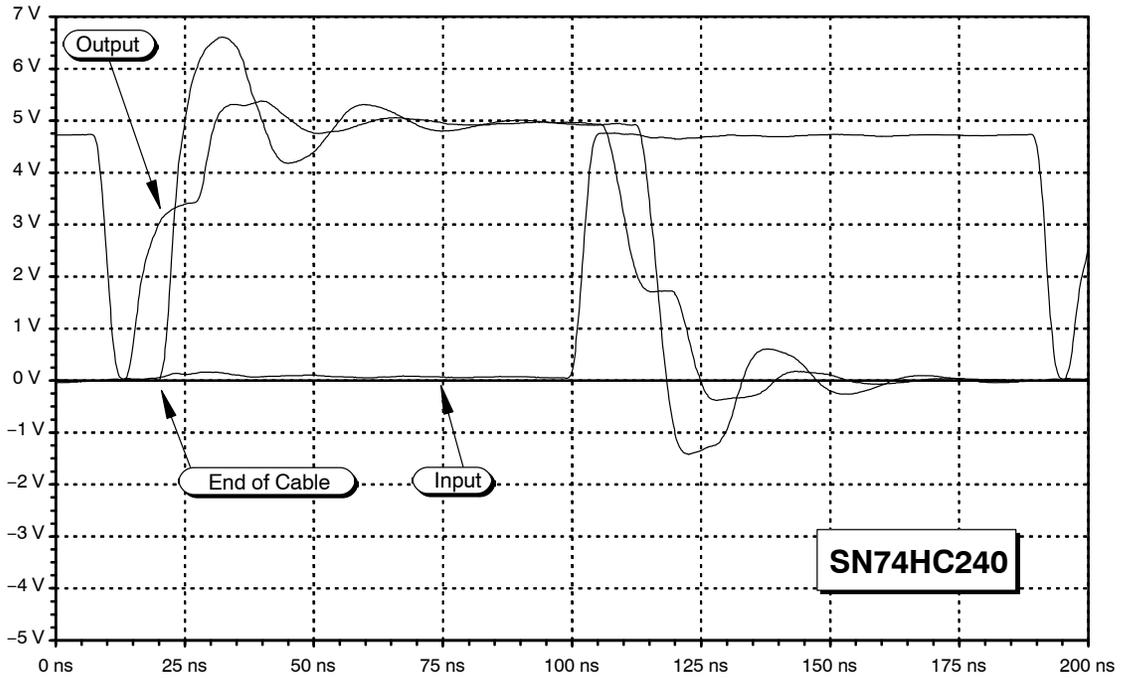


Figure 68. Output Waveforms of the SN74HC240

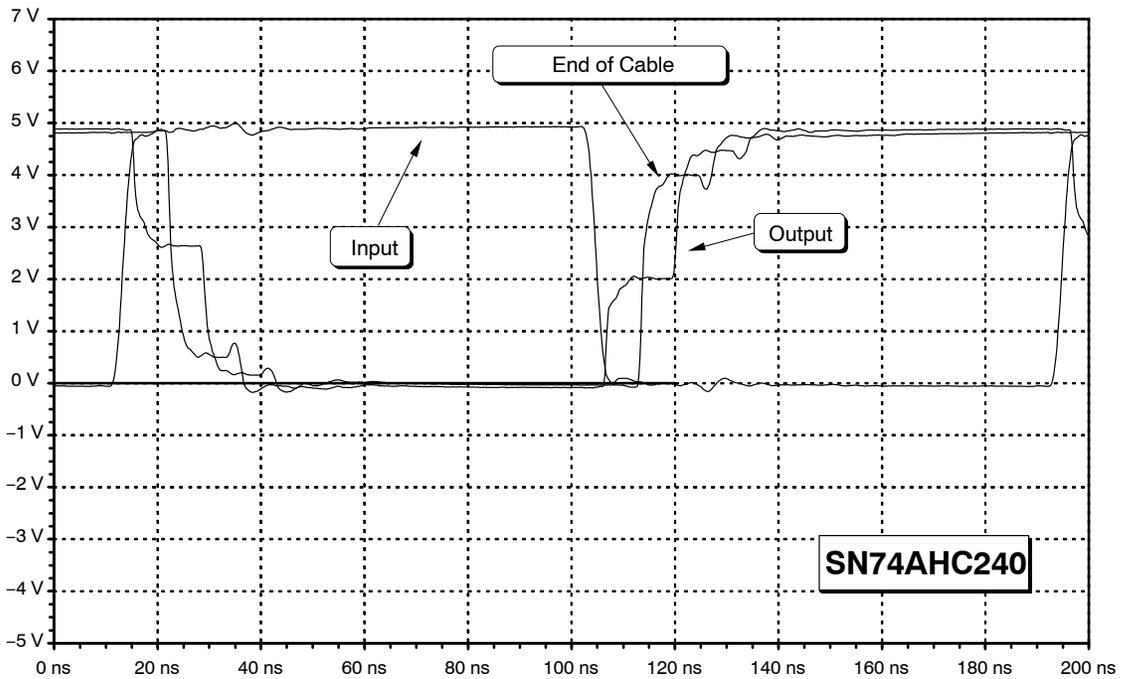


Figure 69. Output Waveforms of the SN74AHC240

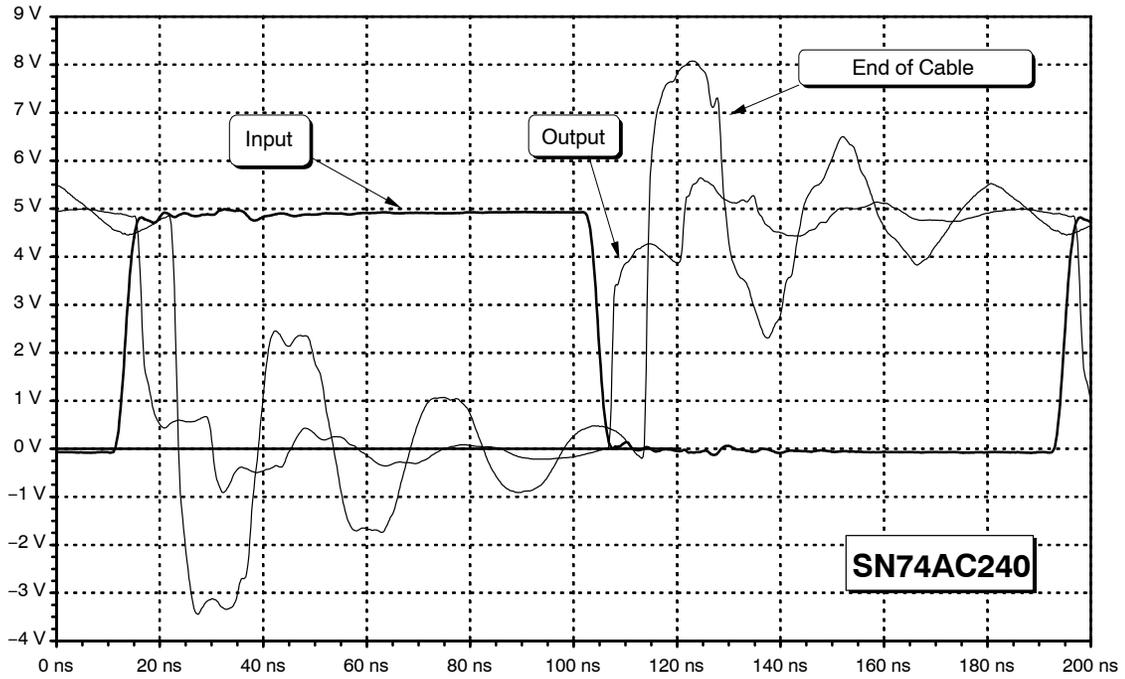


Figure 70. Output Waveforms of the SN74AC240

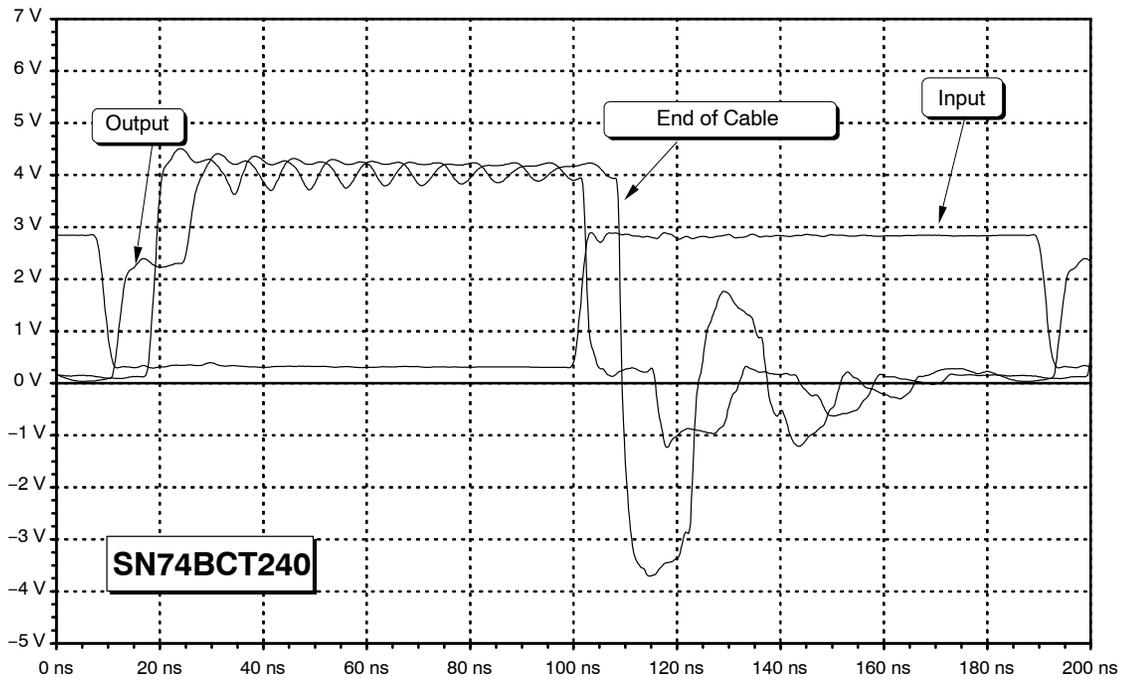
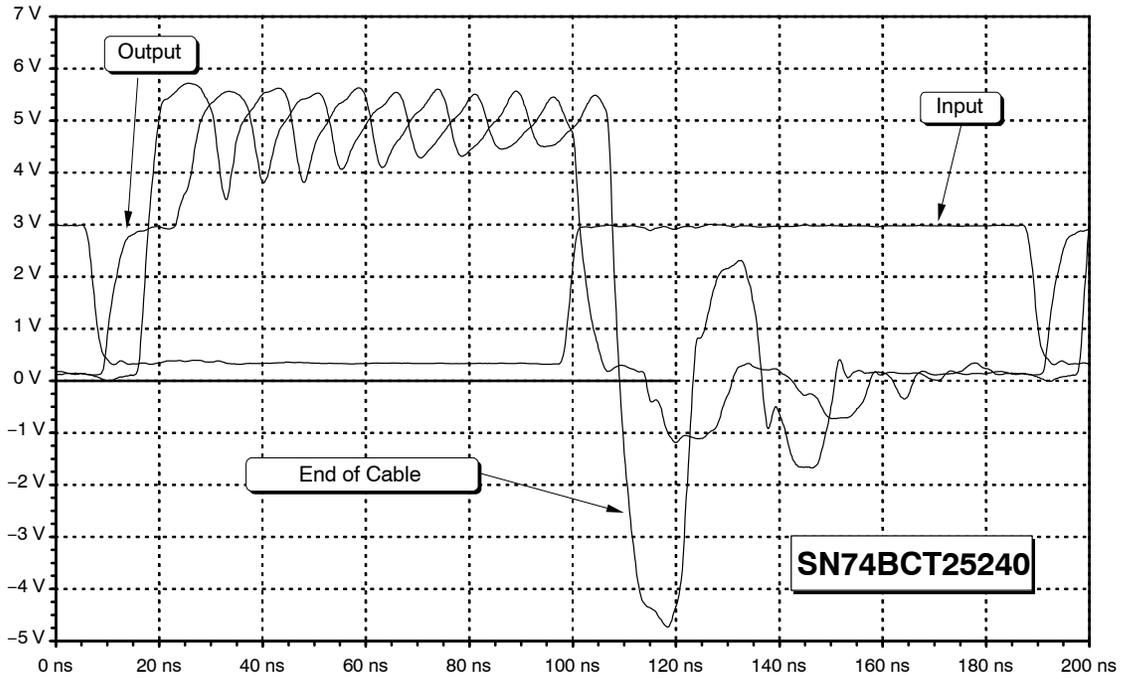
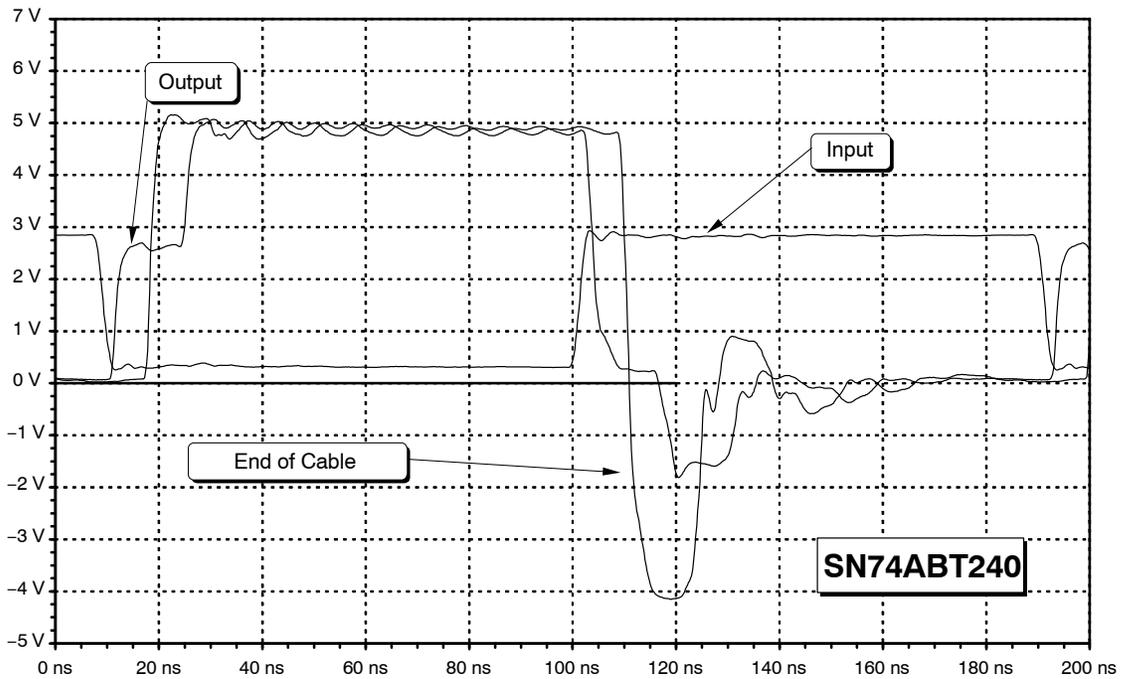


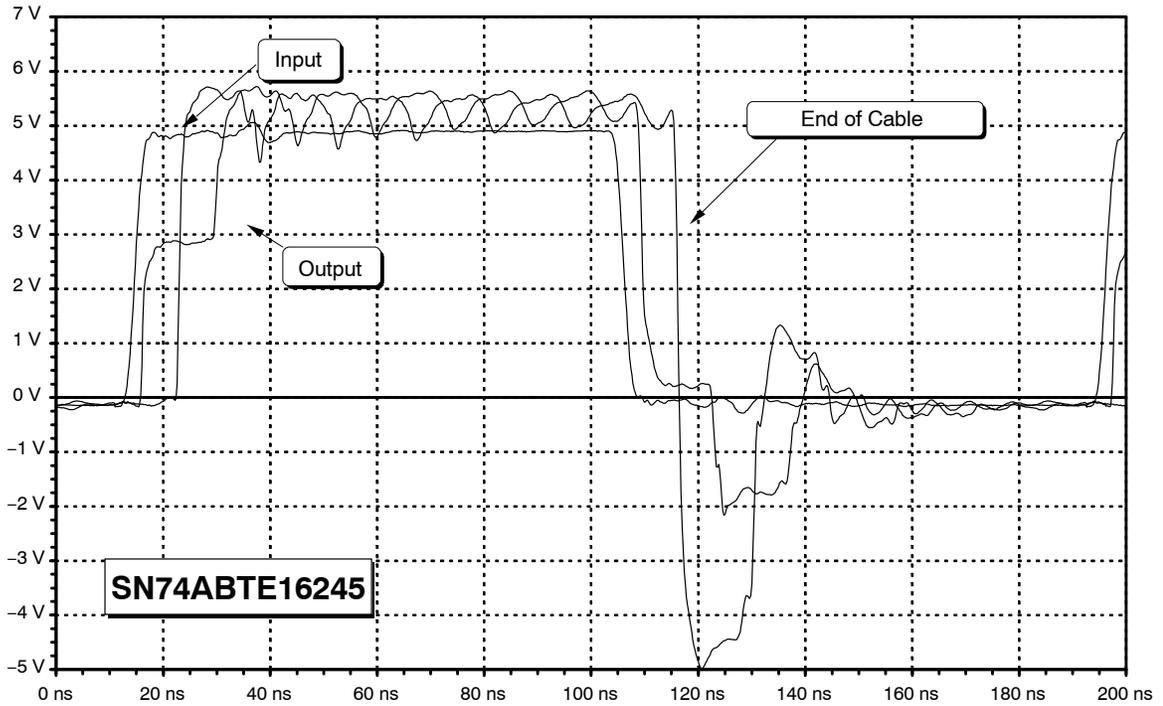
Figure 71. Output Waveforms of the SN74BCT240



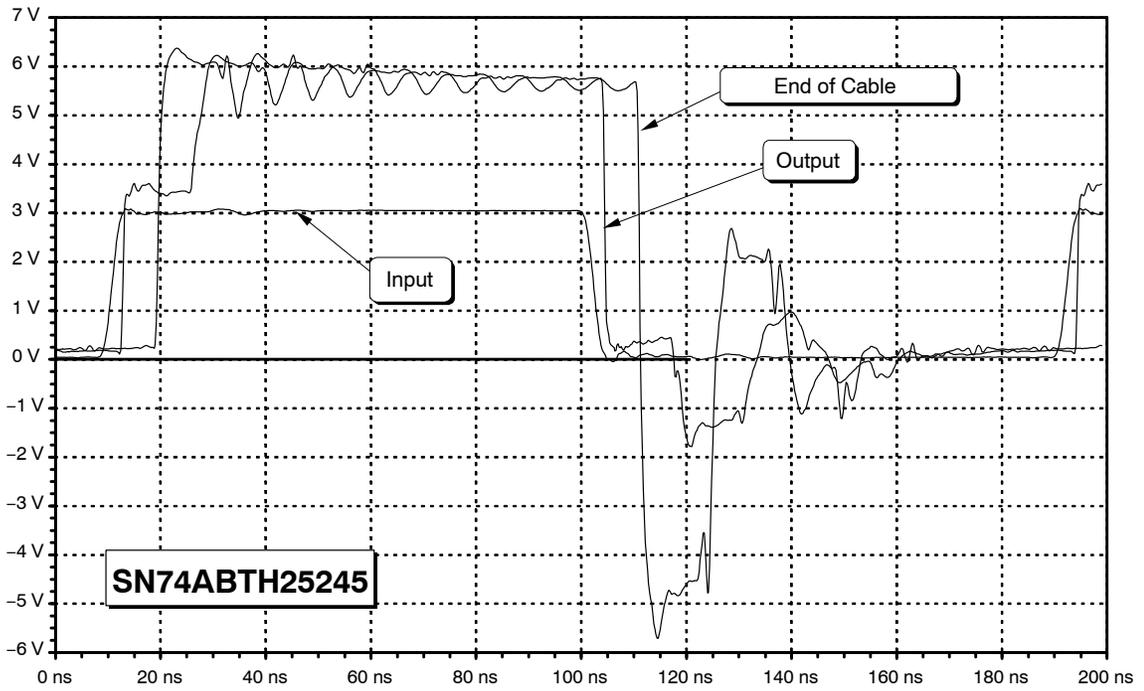
**Figure 72. Output Waveforms of the SN74BCT2524**



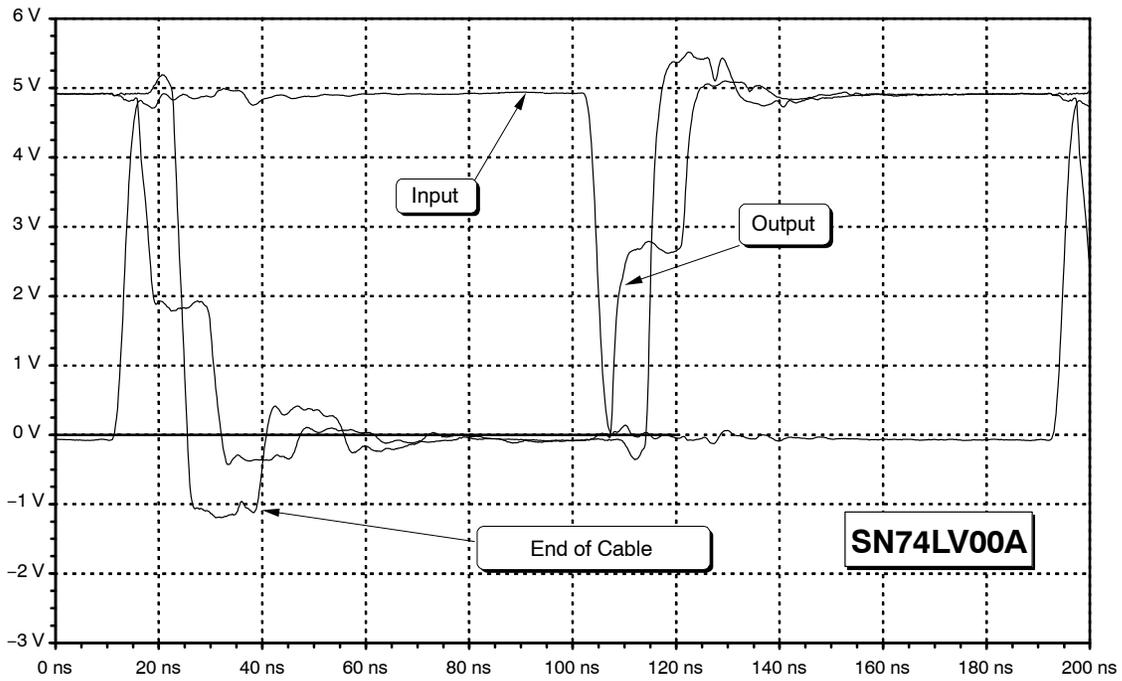
**Figure 73. Output Waveforms of the SN74ABT240**



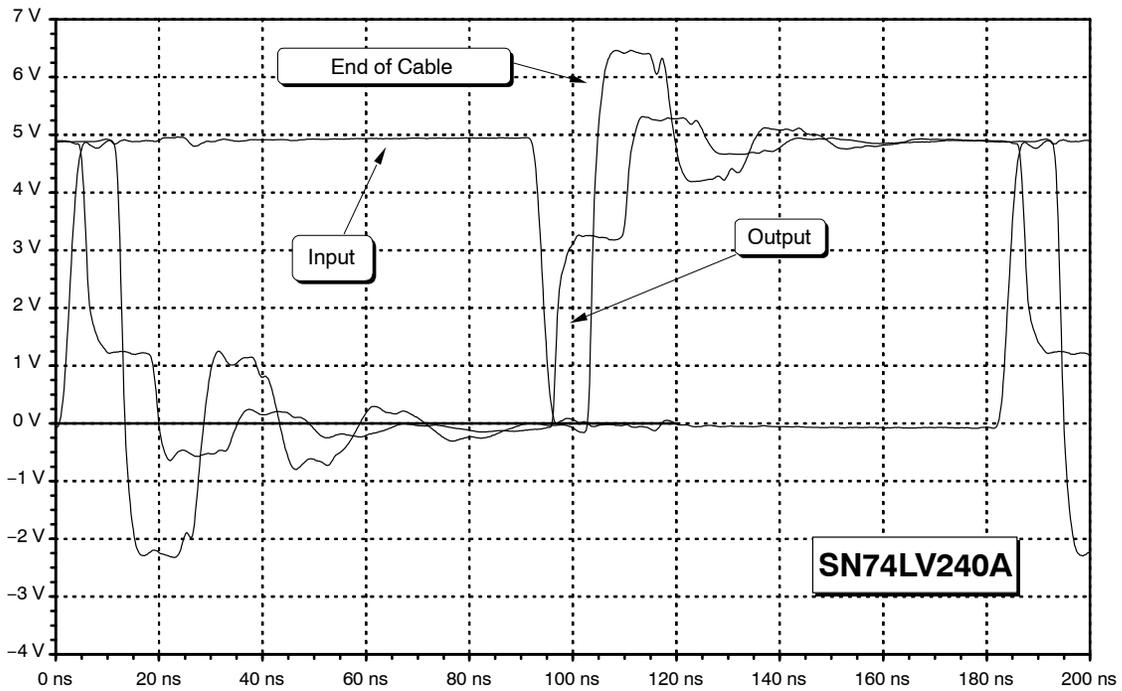
**Figure 74. Output Waveforms of the SN74ABTE16245**



**Figure 75. Output Waveforms of the SN74ABTH25245**



**Figure 76. Output Waveforms of the SN74LV00A**



**Figure 77. Output Waveforms of the SN74LV240A**

## 6 Abbreviations and Glossary

### A

SN74AC	Advanced CMOS
SN74ABT	Advanced BiCMOS Technology
SN74AHC	Advanced High-Speed CMOS
SN74ALS	Advanced Low-Power Schottky
SN74AS	Advanced Schottky

### B

SN74BCT	BiCMOS Technology
BiCMOS	Combination of Bipolar and CMOS process (CMOS input structure, bipolar output structure)

### G

GND	Ground
-----	--------

### H

HC	High-speed CMOS
----	-----------------

### I

I/O	Input/Output
-----	--------------

### L

SN74LS	Low-power Schottky
SN74LV	Low-Voltage CMOS, originally designed for $V_{CC} = 3.3\text{-V}$ , also specified at 5 V

### R

$R_L$	Load resistor
-------	---------------

**S**

SN74S Schottky  
SPICE Simulation Program with Integrated Circuit Emphasis

**T**

TTL 5-V, Transistor-Transistor Logic

**V**

V<sub>CC</sub> Supply voltage

## 7 References

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- Advanced CMOS Logic*, Data Book, 1996, literature number SCADE02.
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- AHC/AHCT Logic Advanced High-Speed CMOS*, Data Book, 1997, literature number SCLD003A.
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- The Bergeron Method: A Graphic Method for Determining Line Reflections in Transient Phenomena*, October 1996, literature number SDYA014.
- Bus-Interface Devices With Output-Damping Resistors or Reduced-Drive Outputs*, August 1997, literature number SCBA012A.
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- Electromagnetic Emission from Logic Circuits*, November 1998, literature number SZZA007.
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- Input and Output Characteristics of Digital Integrated Circuits at 2.5-V Supply Voltage*, literature number SZZA012.

### 7.2 Internet Information Sources

TI Semiconductor Home Page

<http://www.ti.com/sc>

TI Distributors

<http://www.ti.com/sc/docs/distmenu.htm>

TI Logic Home Page

<http://www.ti.com/sc/docs/asl/lit/lit.htm>

TI Logic Literature

<http://www.ti.com/sc/docs/asl/lit/lit.htm>

TI Product Information and Document Search

<http://www.ti.com/sc/docs/msp/download.htm>

## 8 Acknowledgment

The author of this document is Peter Forstner. Revisions were made by Johannes Huchzermeier.



# ***Input and Output Characteristics of Digital Integrated Circuits at 3.3-V Supply Voltage***

SZZA010  
September 1999



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## Abstract

This application report contains a comprehensive collection of the input- and output-characteristic curves of integrated circuits from various 3.3-V logic families. These curves go beyond the information given in data sheets by providing additional details regarding the characteristics of the components. This knowledge is particularly useful when, for example, a decision must be made as to which circuit should be used in a bus system, or when the waveforms that can be expected in a transmission system must be predicted using a Bergeron chart. These oscillograms are of great assistance when generating models for simulation programs that analyze the dynamic behavior of the integrated circuits in a particular environment.

## 1 Introduction

The parameters given in the data sheets of integrated circuits can give only a very limited indication of their behavior in a system. Generally, data sheets give only information regarding the behavior over the input and output (I/O) voltage range of 0 to 3.3 V. Even the output currents specified over this range provide an incomplete picture of in-system performance.

Behavior of integrated circuits outside the usually accepted operating conditions often is of interest. This is, for example, the situation when the characteristic curves need to be used to predict the signal waveforms resulting from line reflections.

Along with the I/O characteristics, use of the Bergeron method, and knowledge of the load resistor, the amplitude of the line reflections can be determined.

Many modern logic families are specified at different voltage nodes, for example the AHC logic, and can be used at 5-V, 3.3-V, or even at 2.5-V supply voltage.

Since three main voltage nodes currently are used, it is necessary to provide I/O-characteristics at these different voltage levels. This report deals exclusively with devices operated at 3.3-V supply voltage.

Two other application reports regarding this topic are available:

- *Input and Output Characteristics of Digital Integrated Circuits at 5-V Supply Voltage*, literature number SZZA008
- *Input and Output Characteristics of Digital Integrated Circuits at 2.5-V Supply Voltage*, literature number SZZA012

In view of the wide range of integrated circuits that are available, it has been necessary to limit this information to typical characteristics only. In the second and third sections of this application report, the input and output characteristics of the following circuits have been shown as being representative of other components that behave similarly in circuit:

- '00 The characteristic curves of this NAND gate are given as representative of all logic circuits having normal drive capability, such as gates, flip-flops, counters, multiplexers, etc.
- '240/'244 The output characteristics of these bus-interface circuits are of particular importance when a decision must be made as to which circuit family should be used for a specific system requirement. The available output current has a decisive influence on the distortion of signals on bus lines.
- '16240/'16244 The output characteristics of these bus-interface devices correspond with the '240/'244 functions regarding the electrical behavior. However, these devices support 16 drivers within one package. This meets the market requirements, because modern designs are based on wider buses, using 16 bits, 32 bits, or more bits on the backplanes. Further, the noise behavior of the Widebus™ shows a significant improvement versus the standard octal packages.

Representatives of the different logic families (see Table 1) give an overview of the input and output characteristics, which are presented in sections 2 and 3.

**Table 1. Representatives of the Different Logic Families**

FAMILY	TYPE		
	'00	'240/'244	'16244
SN74AHC	√	√	
SN74AC	√	√	
SN74LV	√	√	
SN74LVC	√	√	
SN74ALVC			√
SN74ALB			√
SN74ALVT			√
SN74LVT		√	

Because the input characteristics depend exclusively on the technology used, not on the logical function of the device, only one representative per logic family is shown (gate function '00 or driver function '240) in the input-characteristics section.

Section 4 of this application report presents the calculation of line reflections using the Bergeron method. The calculation is done with the SN74ALVTH16244.

Measurement results demonstrating different switching behaviors of the various logic families are given in Section 5. For these measurements, the devices under test were loaded with a 1.3-m-long coaxial cable having a characteristic impedance of 50 Ω; the end of the line was not connected, i.e., open circuit. These waveforms provide good insight into the dynamic behavior of the devices.

## 2 Input Characteristics

The high impedance of the input stage of the logic circuit determines the input characteristics of logic circuits in the positive range.

In contrast to the 5-V logic families, all of the 3.3-V families have CMOS input stages. The technologies used are based on the CMOS or the BiCMOS manufacturing process. In both cases, CMOS input stages are used. CMOS input stages are controlled exclusively by the applied voltage, so there is no current flowing into the input stage. Therefore, the input impedance of CMOS and BiCMOS devices is in the megaohm range. Negative voltage peaks are limited by a protection diode.

The input stages of some CMOS and BiCMOS logic families (SN74AC, SN74ALB) also have an input protection diode connected to  $V_{CC}$ . This diode limits the positive input voltage to maximum  $V_{CC} + 0.7$  V, but prohibits their use in mixed-voltage systems.

The bus-hold circuit represents a special input circuit that is implemented in the input stages of the LVT and ALVT logic families and is optionally available for the LVC and ALVC family devices.

Inputs of components that have the bus-hold circuit hold the last valid logic state. This feature is suitable in the case where an input stays undefined, e.g., during a high-impedance state on the bus. Using the bus-hold circuit eliminates the need for pullup or pulldown resistors.

Devices with the bus-hold circuit are designated by the 'H' in their part numbers, for example, SN74LVTH245.

A more detailed application report, *Bus-Hold Circuits*, literature number SDZAE15, is available from Texas Instruments (TI™).

A list of application reports and other literature is given in Section 7.

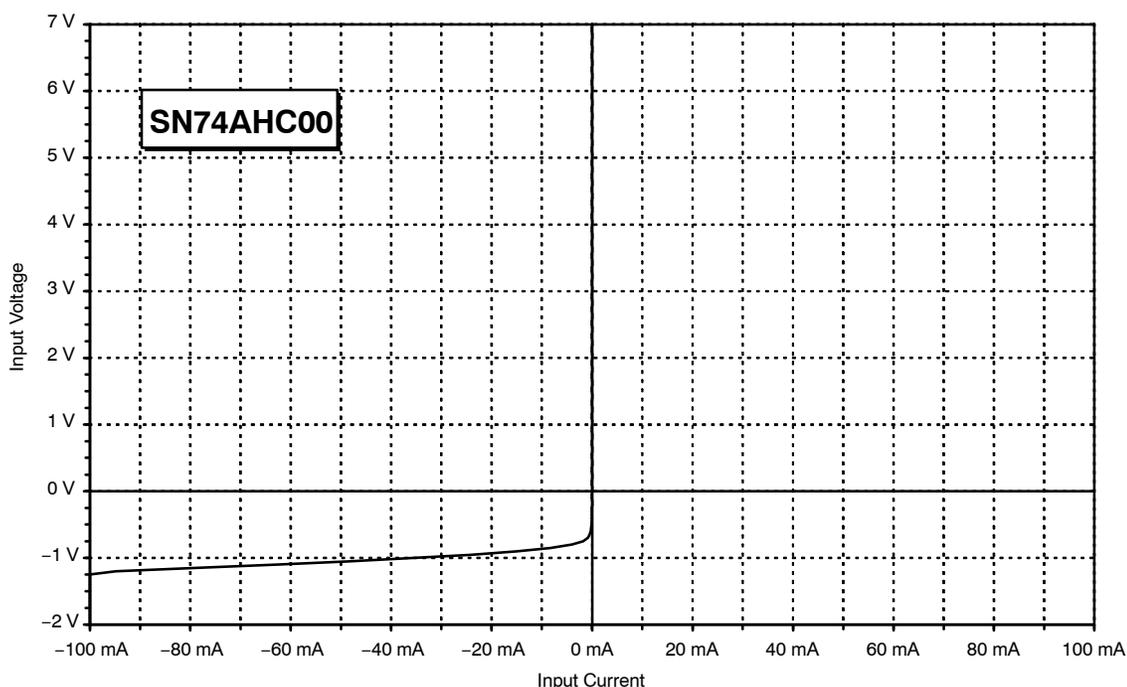
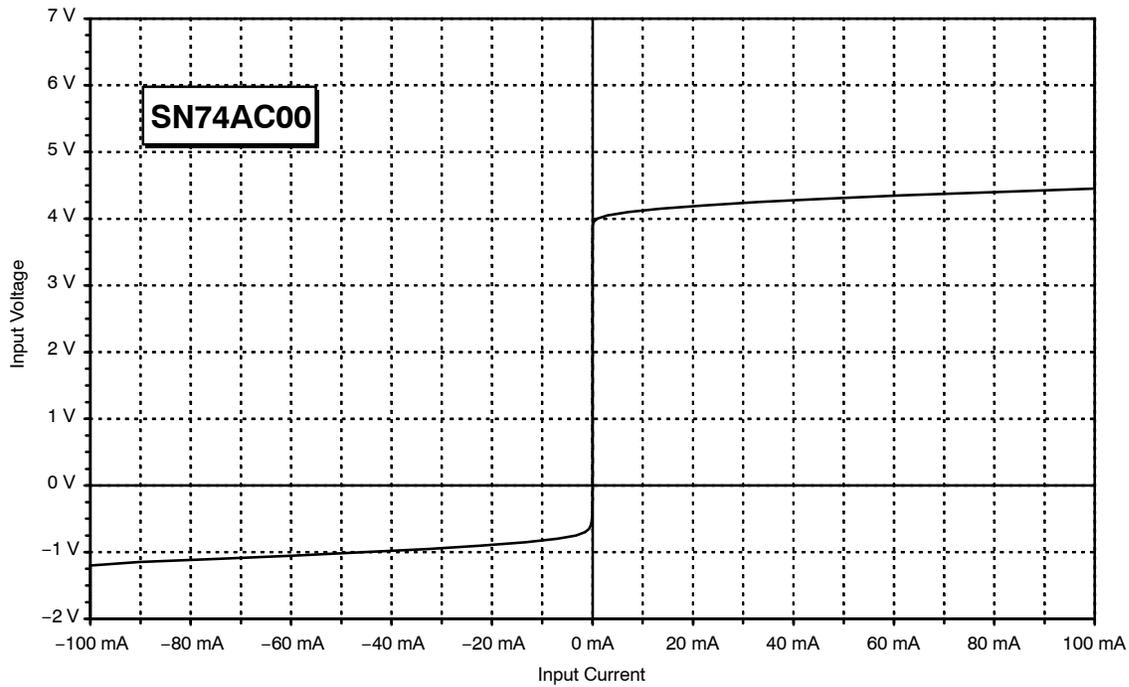
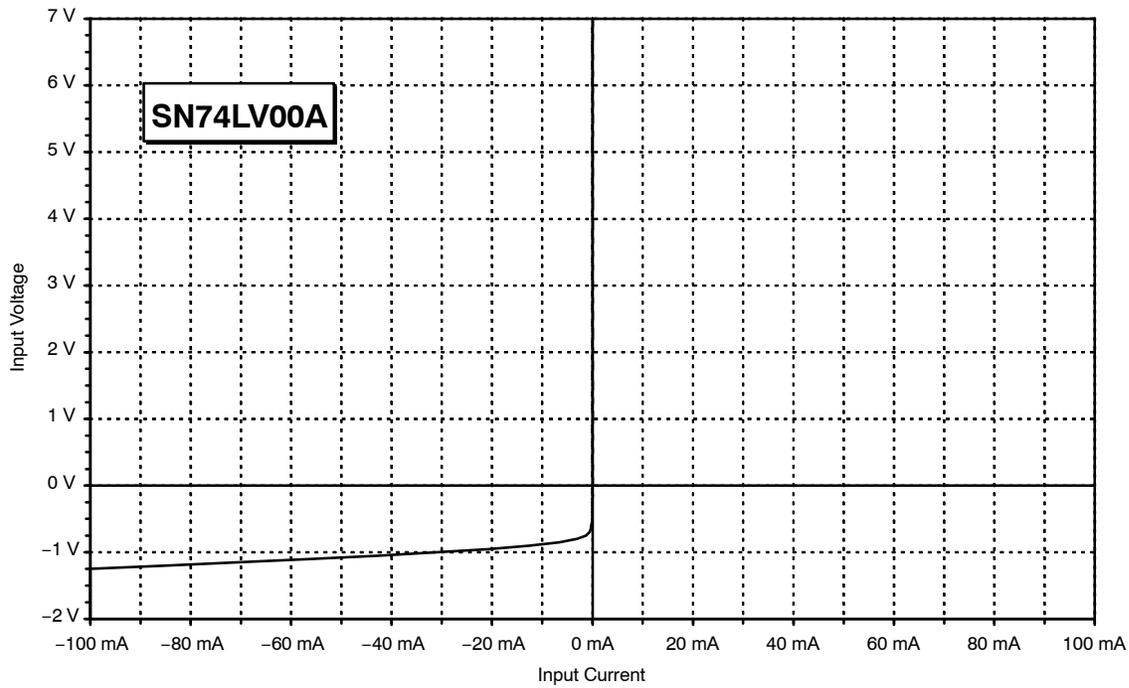


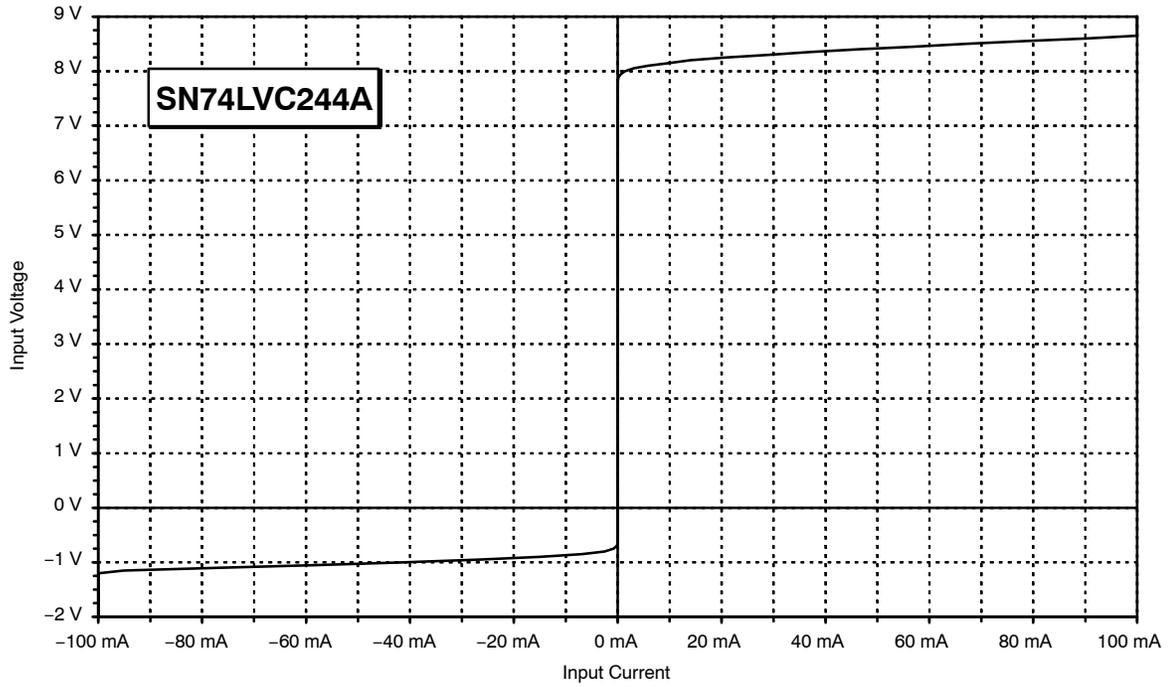
Figure 1. Input Characteristic of the SN74AHCxxx Series



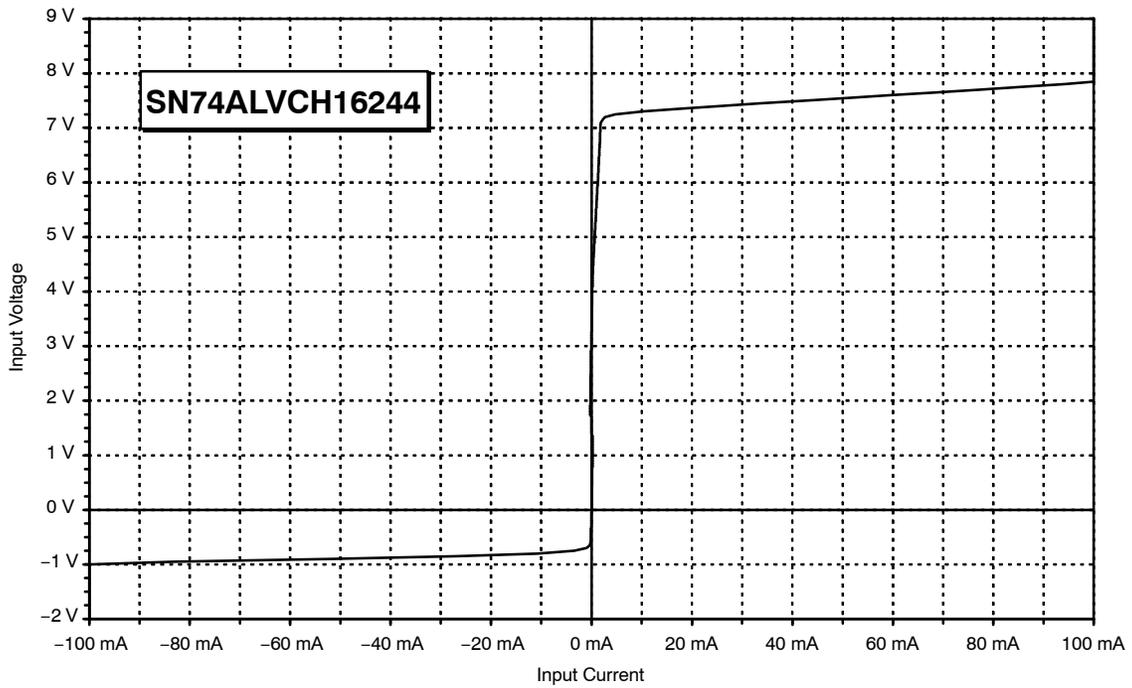
**Figure 2. Input Characteristic of the SN74ACxxx Series**



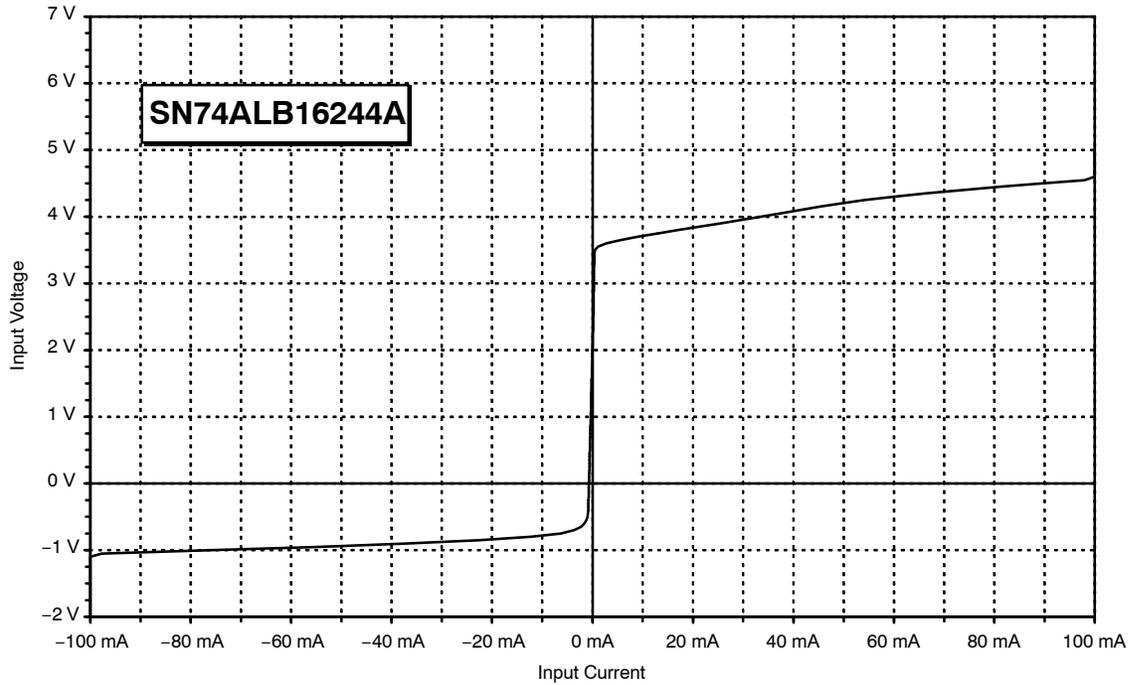
**Figure 3. Input Characteristic of the SN74LVxxx Series**



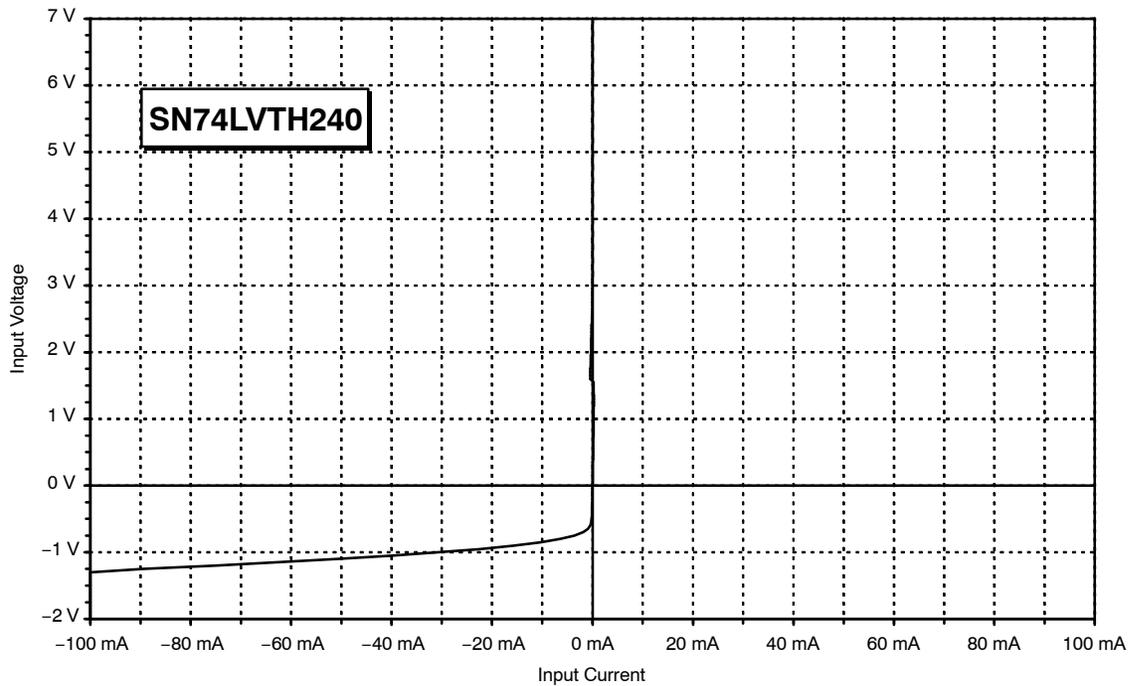
**Figure 4. Input Characteristic of the SN74LVCxxx Series**



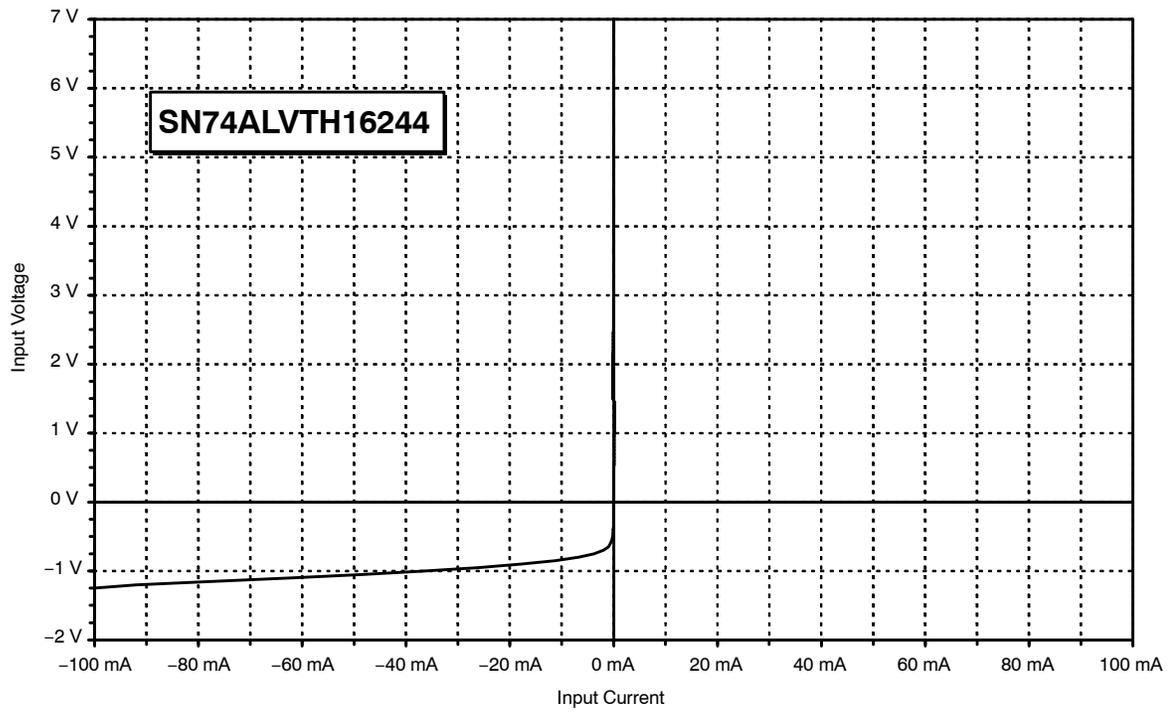
**Figure 5. Input Characteristic of the SN74ALVCxxx Series**



**Figure 6. Input Characteristic of the SN74ALBxxx Series**



**Figure 7. Input Characteristic of the SN74LVTHxxx Series**



**Figure 8. Input Characteristic of the SN74ALVTHxxx Series**

### 3 Output Characteristics

The output stage of a logic circuit in the high-impedance state behaves like a voltage source with an open-circuit voltage of  $V_{CC}$  for CMOS logic and low voltage for BiCMOS logic. The internal resistance for the high-impedance state is inversely proportional to the drive capability of the device. The value of the internal resistance for the standard logic families is in the range of  $30\ \Omega$  to  $40\ \Omega$ .

In the low state for positive voltages, the output resistance is based on the internal resistance of the conducting transistor, i.e., collector-emitter for BiCMOS technologies and drain-source resistance for CMOS technologies. Negative voltage peaks are limited by a protection diode. The output stages of some CMOS logic families (SN74AHC, SN74AC) also have an output protection diode, which is connected to  $V_{CC}$ . This diode limits the positive output voltage to maximum  $V_{CC} + 0.7\ \text{V}$ .

#### 3.1 Series Damping Resistors (SN74XXX2xxx, SN74XXXR2xxx)

In the LVC, ALVC, LVT and ALVT families, TI offers driver options with integrated series resistors of about  $25\ \Omega$ .

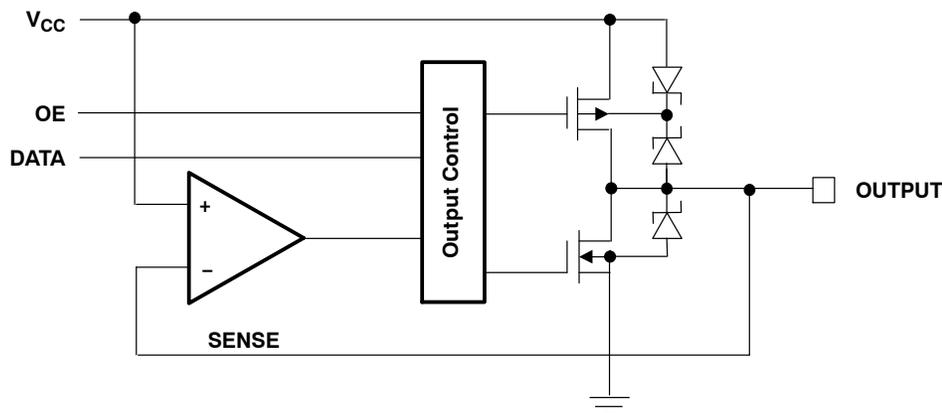
Using the damping resistors at the output stage, the effective output impedance of the driver is about  $50\ \Omega$ . If the value of the line impedance also is about  $50\ \Omega$ , no line reflections are observed at the output of the device. In this case, the beginning of the line is terminated perfectly. This option is especially beneficial for memory applications in which overshoots and undershoots might cause a malfunction. In point-to-point applications, nearly ideal signal shapes can be achieved. The “2” in the device part number indicates the presence of a series damping resistor. The “R” in combination with the “2” indicates series damping resistors on both ports of bidirectional devices, for example, the SN74LVC2245A and LVTH162374.

Further information about series damping resistors is given in the TI application report, *Bus-Interface Devices With Output Damping Resistors or Reduced-Drive Outputs*, literature number SCBA012.

A list of available application reports and other literature is in Section 7.

#### 3.2 Automatic High-Impedance State (Auto3-state) Output of the ALVT Family

The auto3-state function, which is implemented in the output stages of the ALVT family, represents a specialty. The principle is shown in Figure 9.



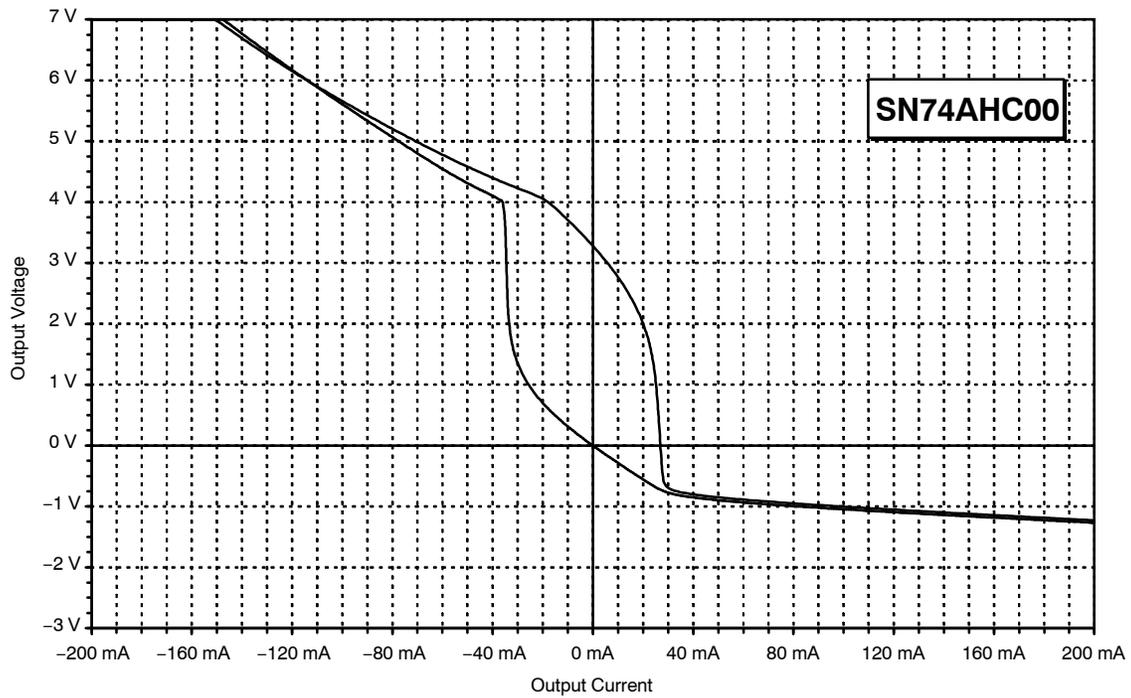
**Figure 9. Simplified Output Stage of ALVT Devices**

Assume that the output is in the active-high state and a comparator monitors the voltage at the output and compares it with the supply voltage. If the voltage that is applied externally to the output exceeds the supply voltage, the output stage is switched to the high-impedance-state. In this case, the logic levels applied to the data and control input pins of the device are irrelevant.

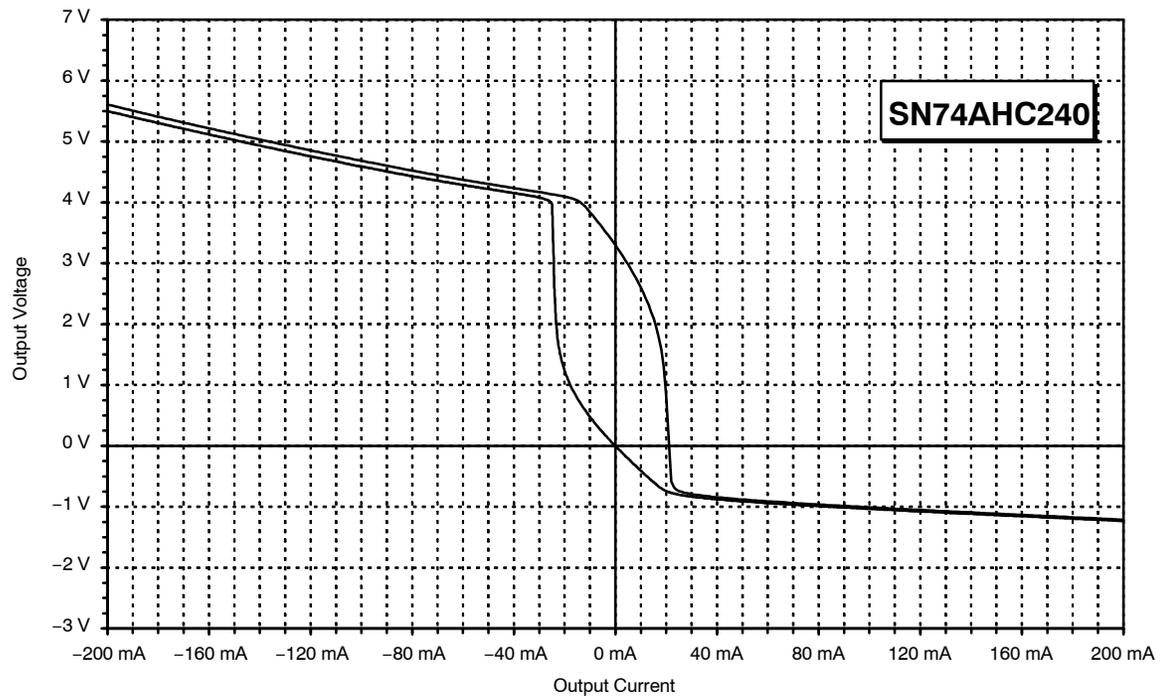
A current of about 30 mA is needed to trigger the auto3-state circuit, such that bus contentions are prevented, but switching noise does not trigger the protective circuit. However, this also implies that the auto3-state cannot be implemented by using a simple pullup resistor.

Current can flow into the output only in the case of an active high. If the output is set to high impedance by the OE control pin, no current flows.

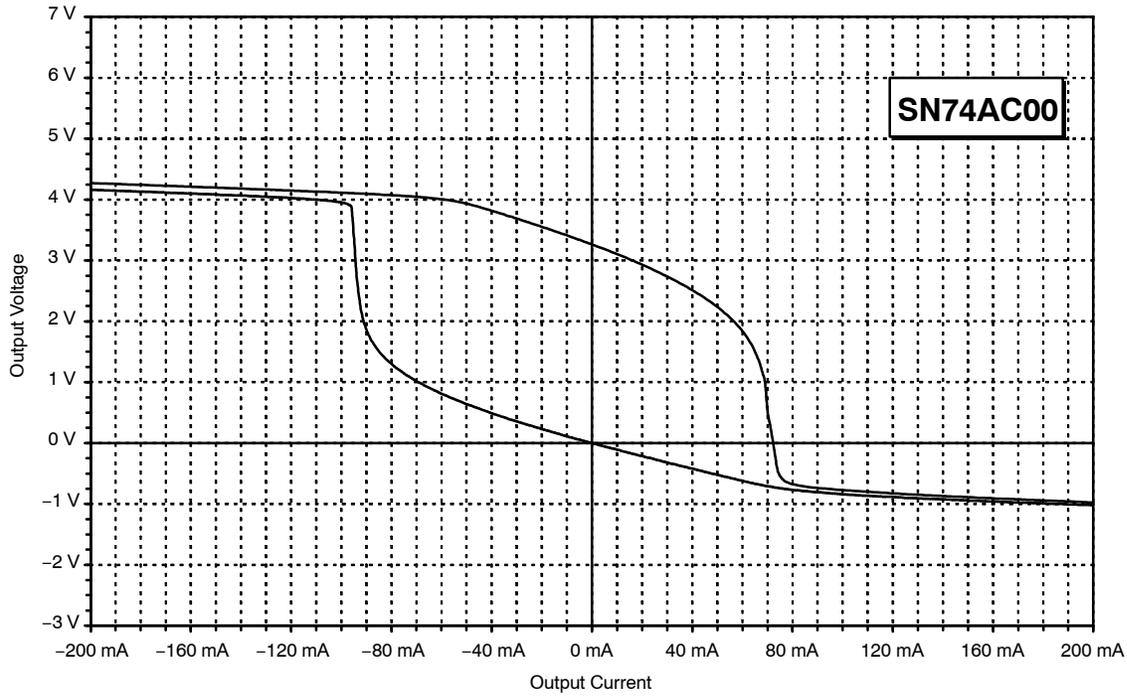
The series opposed Schottky diodes always connect the back gate of the pullup transistor of the output stage to the higher voltage that is either  $V_{CC}$  or the voltage that can be applied externally to the output. In this way, current flow from the output to  $V_{CC}$  is suppressed.



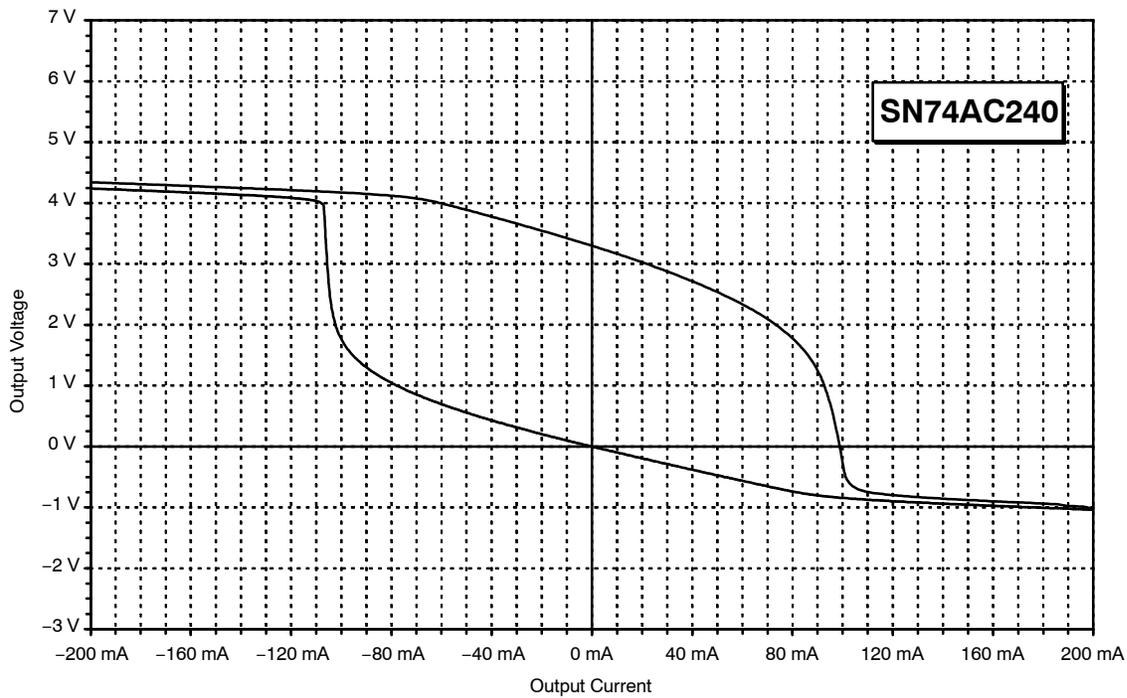
**Figure 10. Output Characteristics of the SN74AHC00**



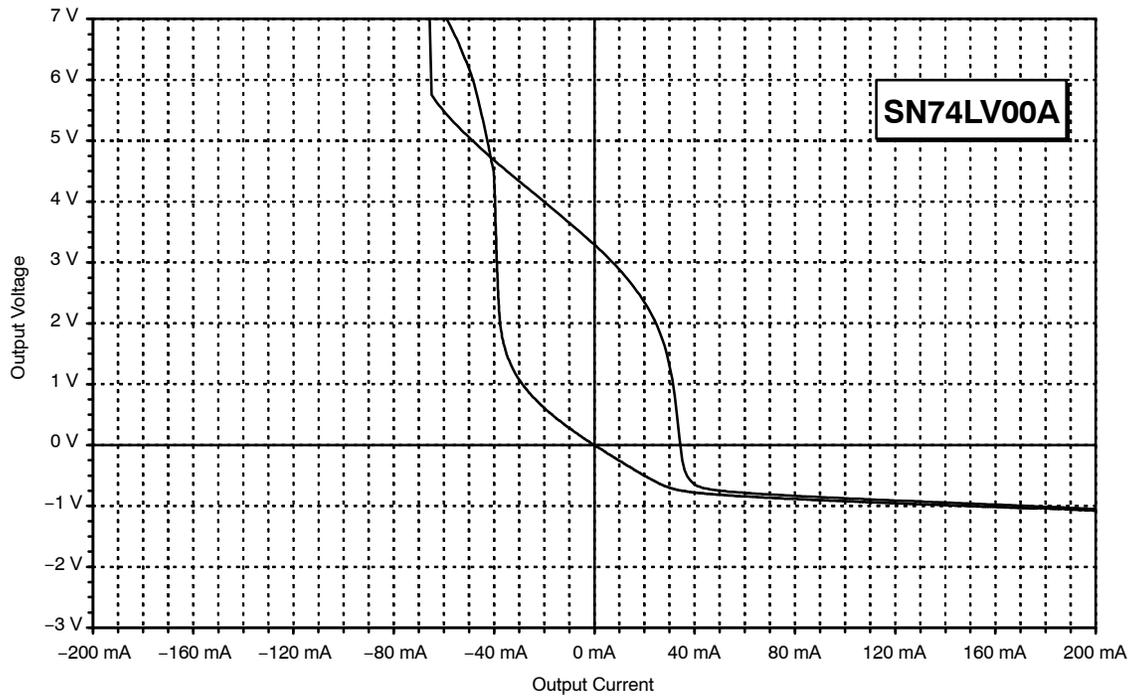
**Figure 11. Output Characteristics of the SN74AHC240**



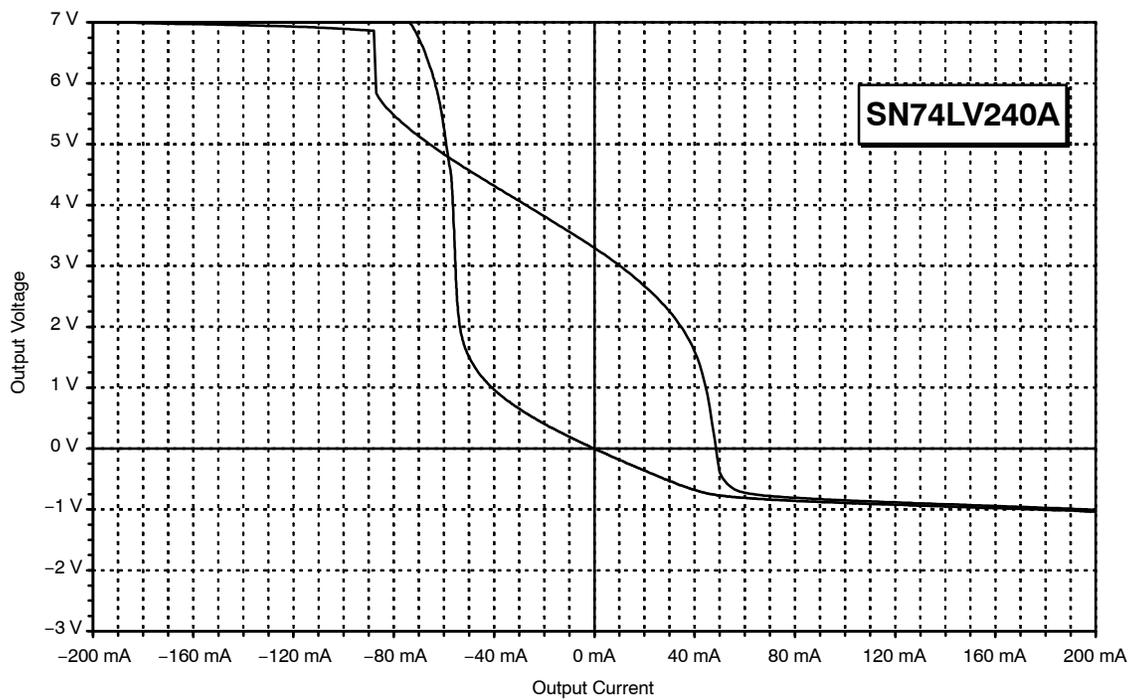
**Figure 12. Output Characteristics of the SN74AC00**



**Figure 13. Output Characteristics of the SN74AC240**



**Figure 14. Output Characteristics of the SN74LV00A**



**Figure 15. Output Characteristics of the SN74LV240A**

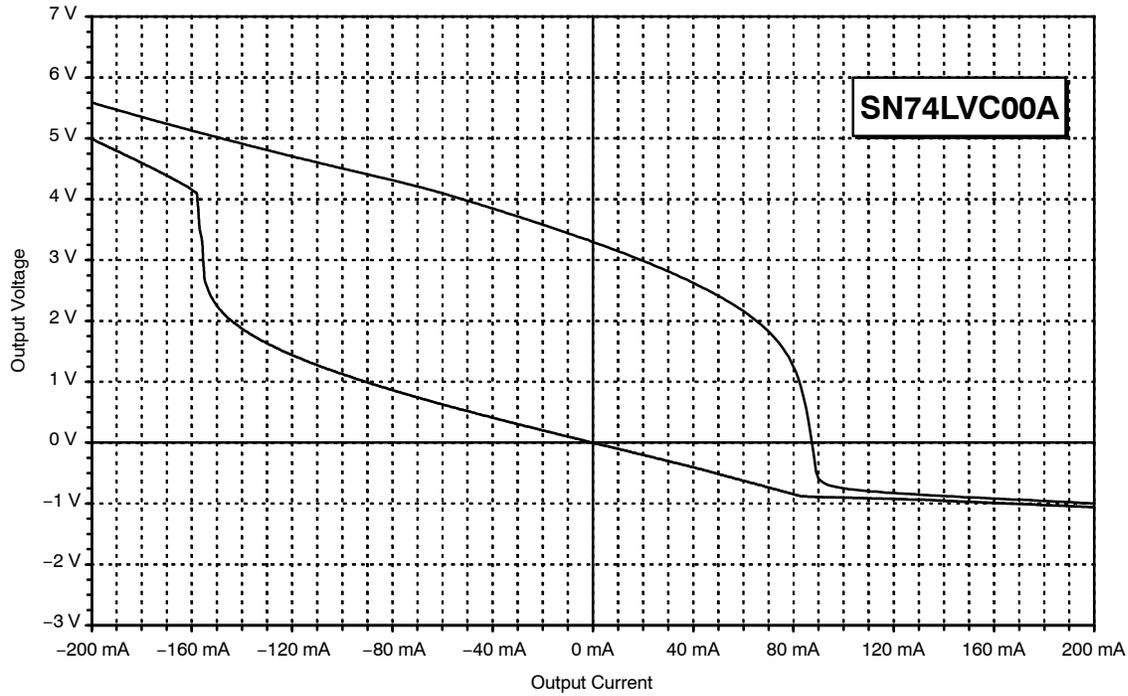


Figure 16. Output Characteristics of the SN74LVC00A

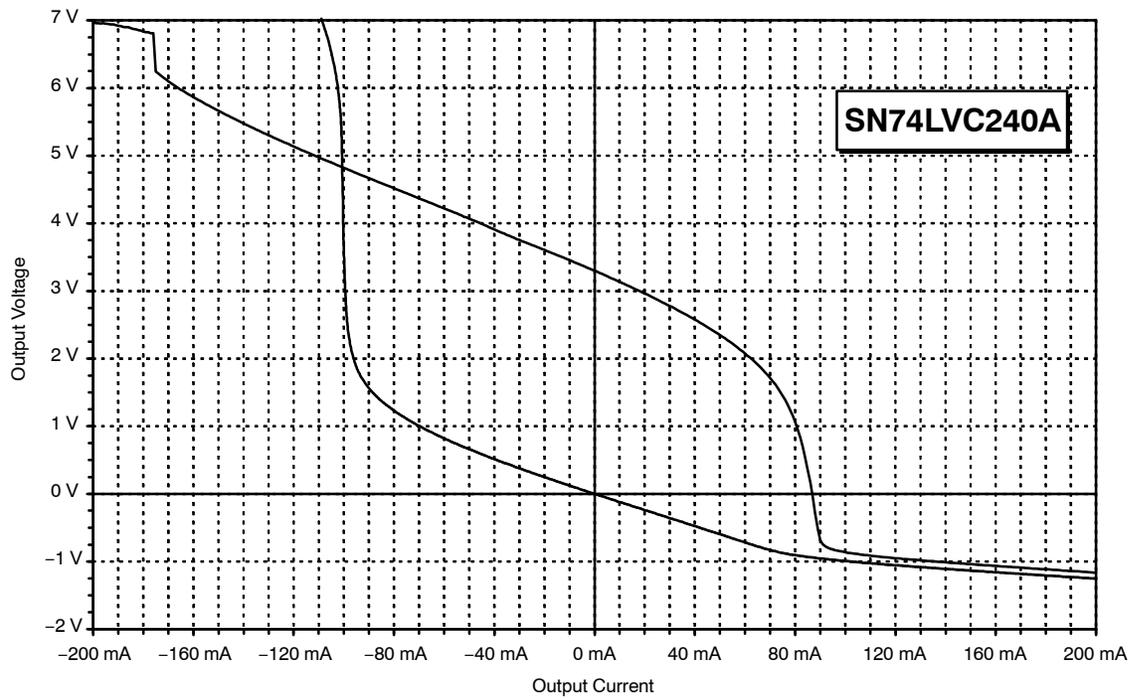
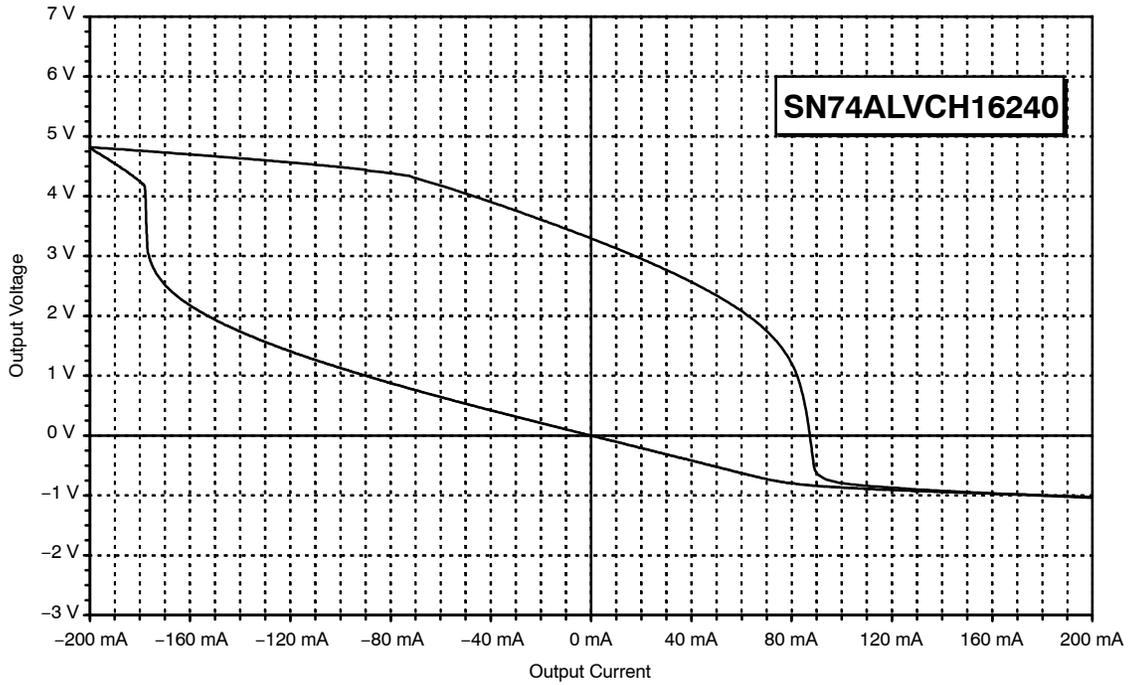
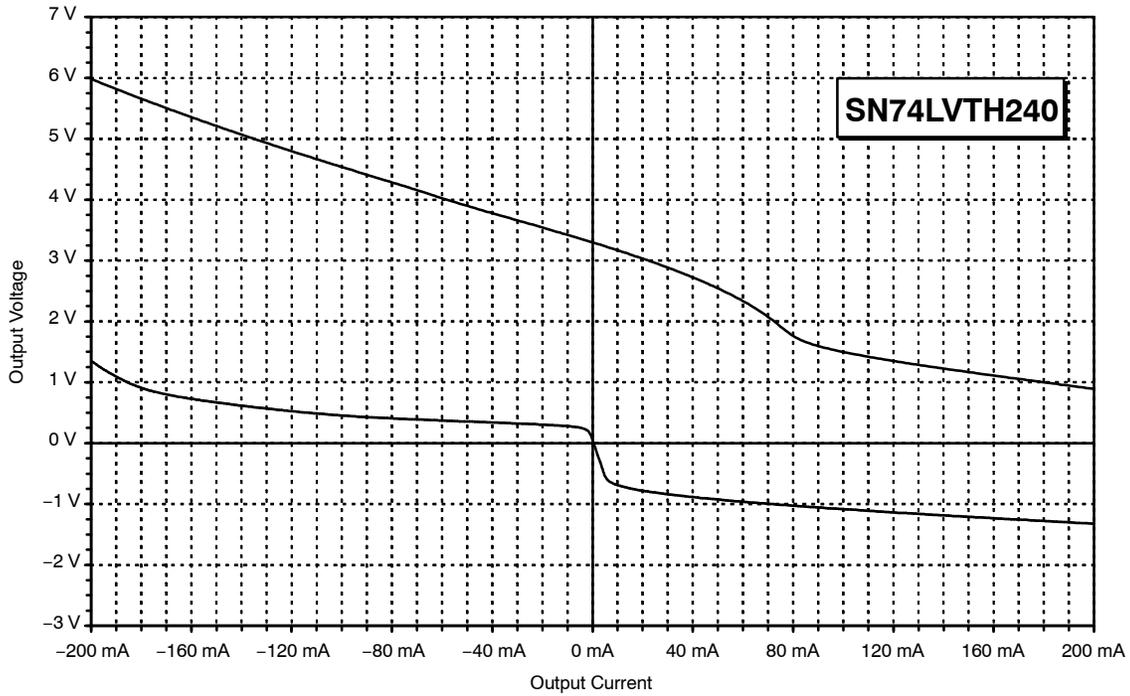


Figure 17. Output Characteristics of the SN74LVC240A



**Figure 18. Output Characteristics of the SN74ALVCH16240**



**Figure 19. Output Characteristics of the SN74LVTH240**

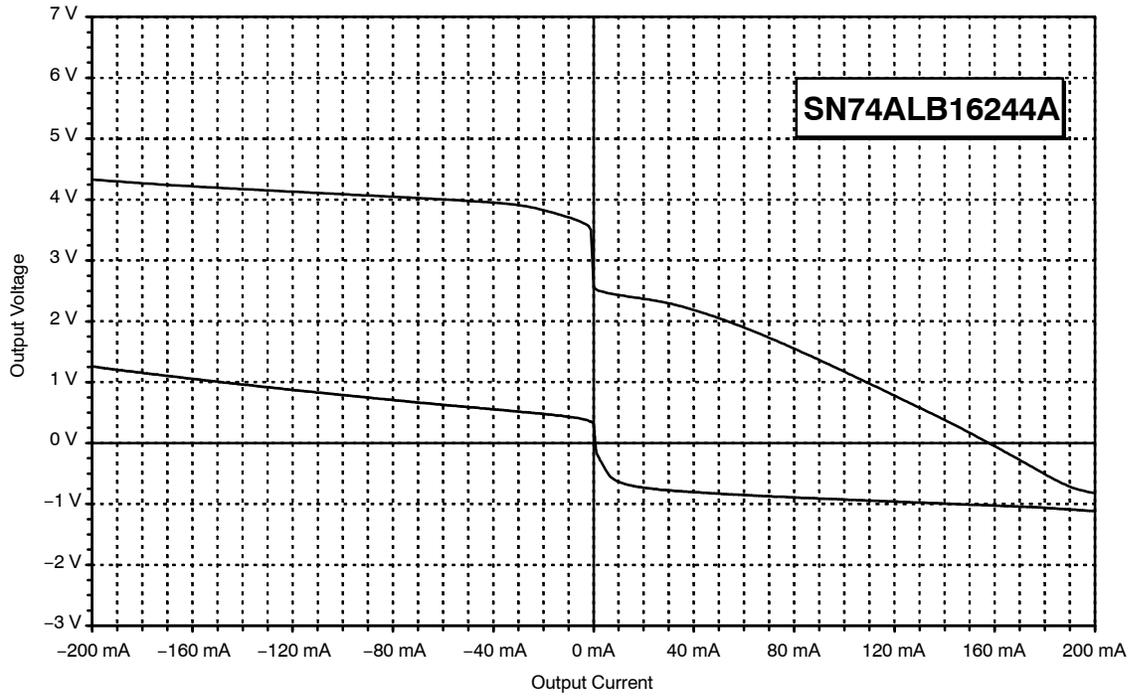


Figure 20. Output Characteristics of the SN74ALB16244A

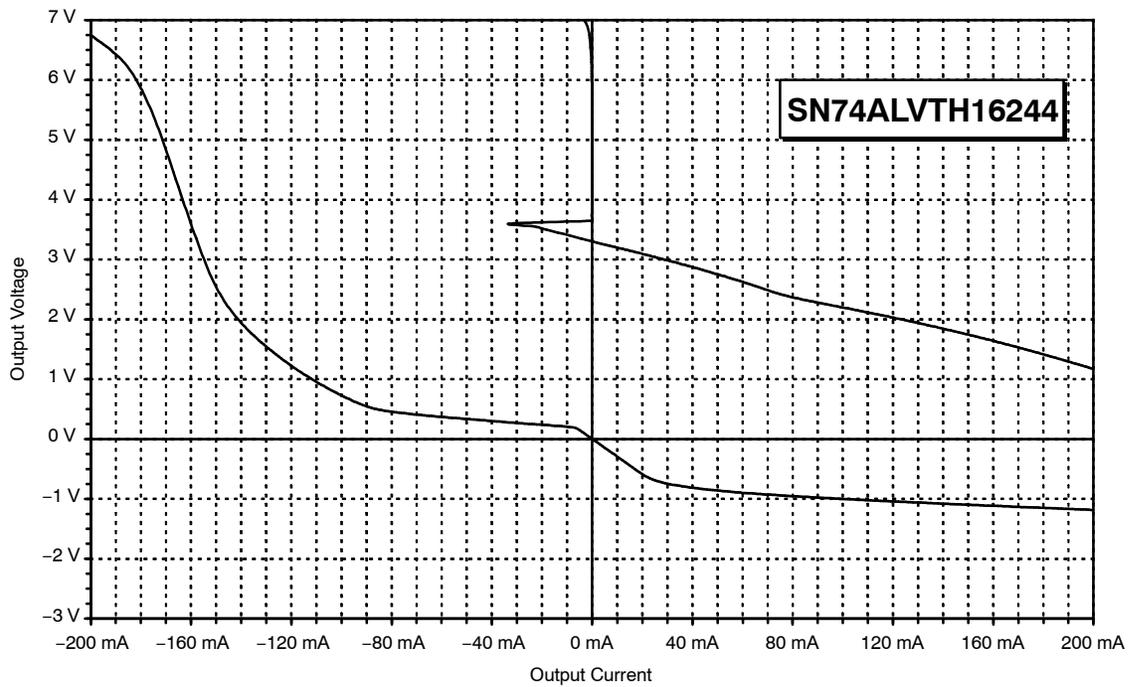


Figure 21. Output Characteristics of the SN74ALVTH16244

## 4 Bergeron Method Applied to the SN74ALVTH16244

The input and output characteristics, shown in Sections 2 and 3, can be used to determine the signal reflections within a certain application by using a graphical procedure known as the Bergeron method.

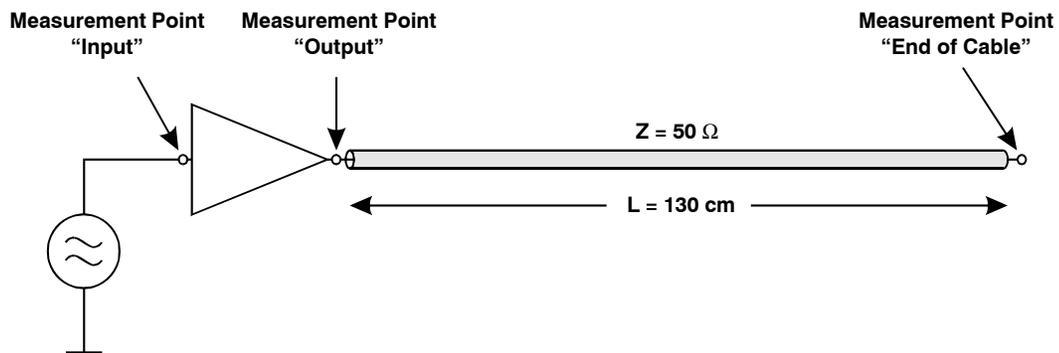
The prerequisite for the use of the Bergeron method is that the lines exceed a certain length:

*If the rise time or the fall time of a signal is shorter than twice the propagation delay on the line, the line theory must be applied.*

Practically, for a line with a signal propagation of 5 ns/m and a signal with a rising or falling edge of 2 ns, starting with a line length that exceeds 20 cm [ $2 \text{ ns} / (5 \text{ ns/m} \times 2)$ ], the line theory must be applied.

For a bus line, the signal propagation delay increases to 25 ns/m, so that, in this case, the line theory has to be applied for a line length that exceeds 4 cm [ $2 \text{ ns} / (25 \text{ ns/m} \times 2)$ ].

The SN74ALVTH16244 device was tested, using the measurement setup shown in Figure 22. The Bergeron method was used to determine the signal shape in advance.



**Figure 22. Measurement Setup for the Bergeron Method**

The first step in the graphical solution using the Bergeron method is to draw the following characteristics in a voltage-versus-current diagram:

- Output characteristics of the SN74ALVTH16244 device
- Load characteristic at the end of the line

The output characteristics are taken directly from Figure 21. The load characteristic equals the Y-axis for the investigated case because no resistor is connected to the end of the line ( $R_L = \infty$ ).

The intersection between the load characteristic and the output characteristic represents the steady states, the current and voltage values at the line start, and the end of the line at the time  $t < 0$ , respectively.

### 4.1 Voltage Value at the Output of the Driver

For the low-to-high transition, draw a straight line, starting at the intersection of the output-low characteristic and the load characteristic. For the high-to-low transition, start the straight line at the cross point of *output-high* characteristic and the load characteristic.

The line impedance,  $Z_O$ , determines the steepness of this line. In the example, the line impedance is  $50 \Omega$ .

The intersection of this straight line and the output characteristics equals the voltage and current values at the beginning of the line at the time  $\tau = 0$ .

## 4.2 Voltage Value at End of the Line

Now, a straight line with the steepness  $-Z_O$  is drawn through this point. The intersection between this line and the load characteristics results in the voltage values at the end of the line after one propagation delay time of the line, that is after  $\tau = 1$ .

Afterward, the procedure is repeated, applying straight lines to the output characteristics and the load characteristics.

The steepness of the straight line is:

- $-Z_O$  from the output characteristics to the load characteristics
- $Z_O$  from the load characteristic to the output characteristics

In this way, current and voltage values are obtained:

- at the end of the line, at the times  $\tau = 1, 3, 5 \dots$
- at the line start, at the times  $\tau = 2, 4, 6 \dots$

The Bergeron diagram is shown in Figure 23. The related diagram (see Figure 24) shows the line reflections.

The precalculated values using the Bergeron procedure match very well with the measured signal shapes. Another TI application report, *The Bergeron Method: A Graphic Method for Determining Line Reflections in Transient Phenomena*, literature number SDYA014, describes the graphic procedure in more detail

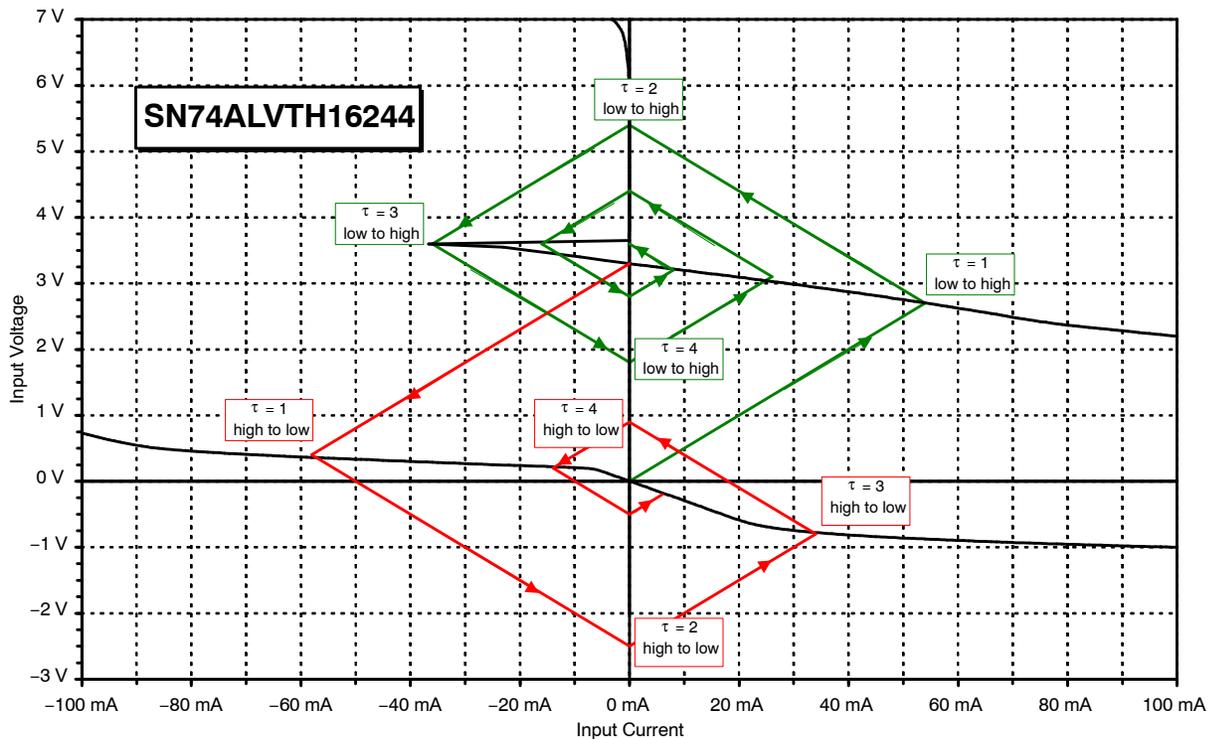


Figure 23. Bergeron Diagram for the SN74ALVTH16244

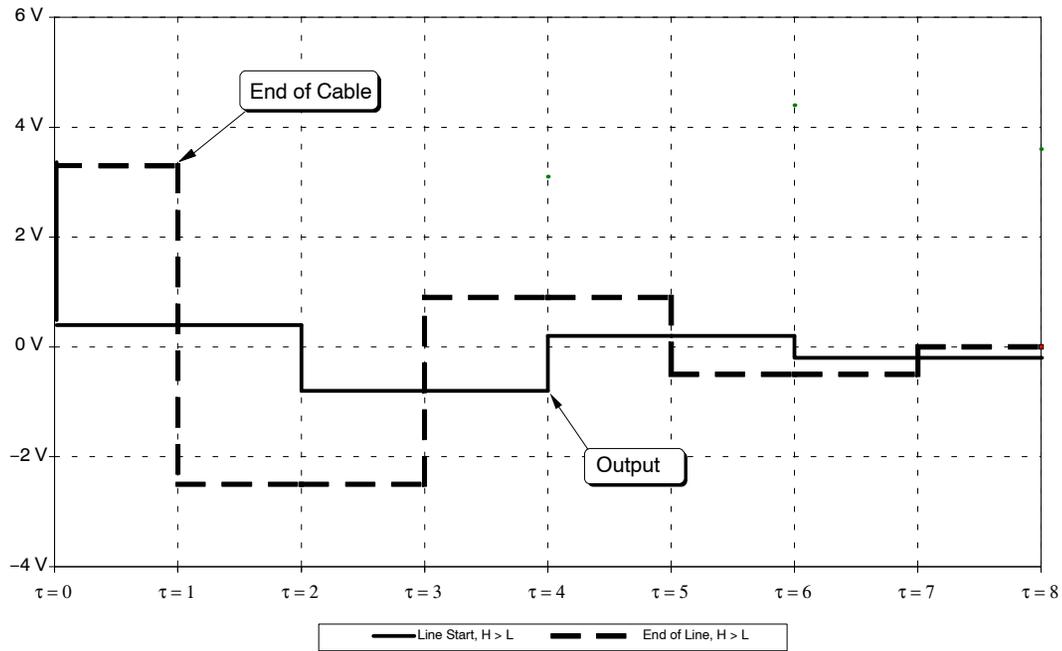
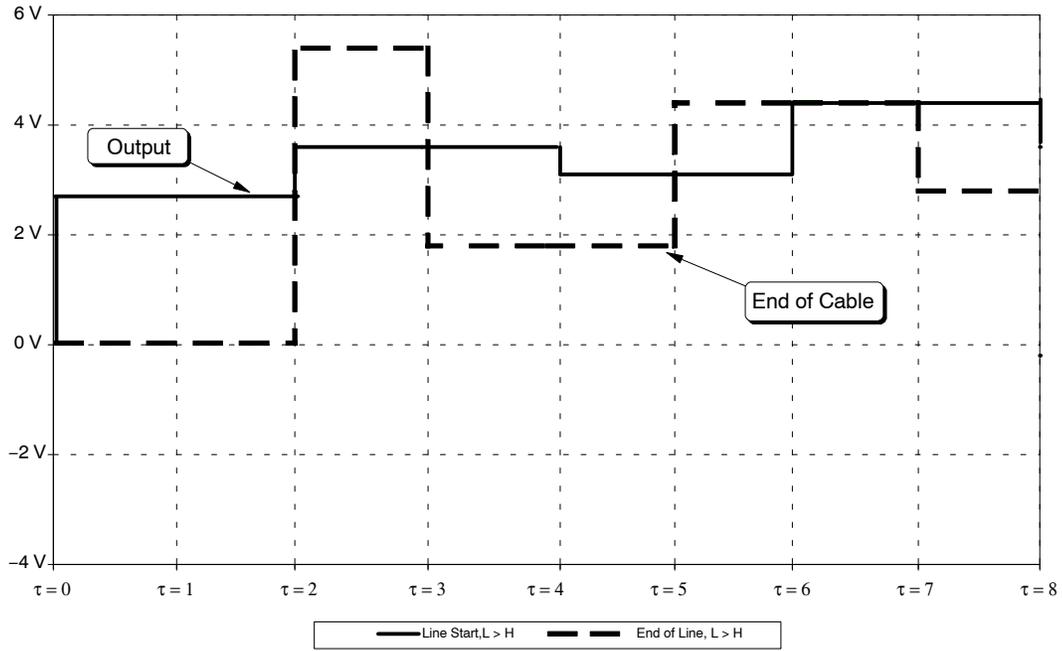


Figure 24. Diagram of Line Reflections for the SN74ALVTH16244

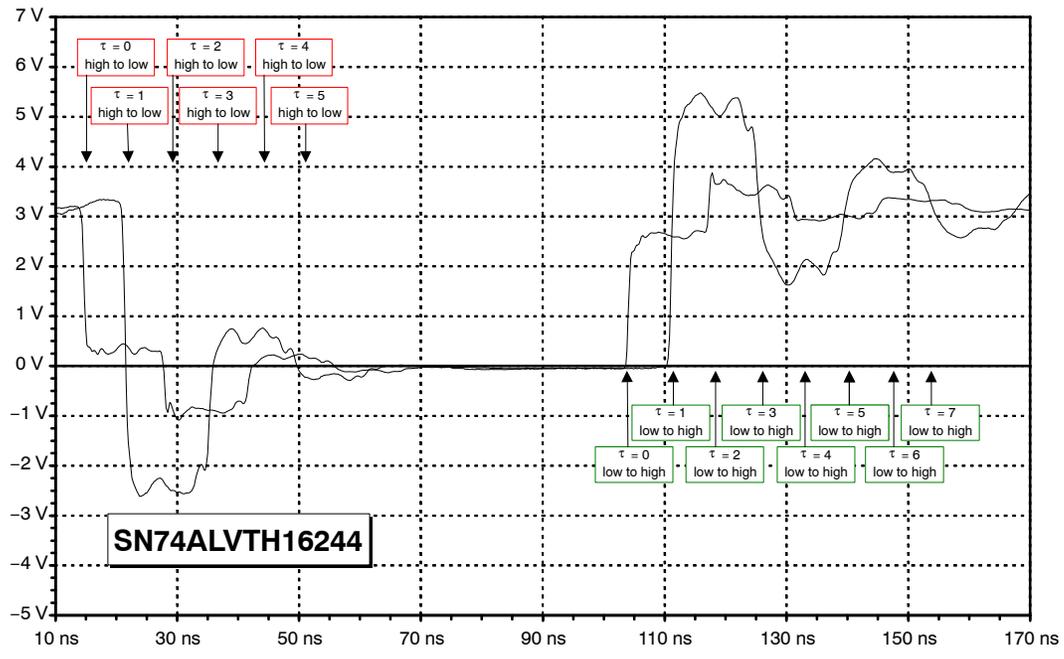


Figure 25. Signal Shape of the SN74ALVTH16244

## 5 Output Waveforms

The following measurements demonstrate the voltage waveforms of typical output stages. The measurement setup is shown in Figure 22.

For these measurements, the devices under test were loaded with a 1.3-m coaxial cable having a characteristic impedance of  $50\ \Omega$ ; the end of the line was not connected, i.e., open circuit.

These waveforms provide good insight into the dynamic behavior of the devices. In particular, the oscillograms provide information regarding drive capability with a low-resistance load, together with an indication of the line reflections that can be expected.

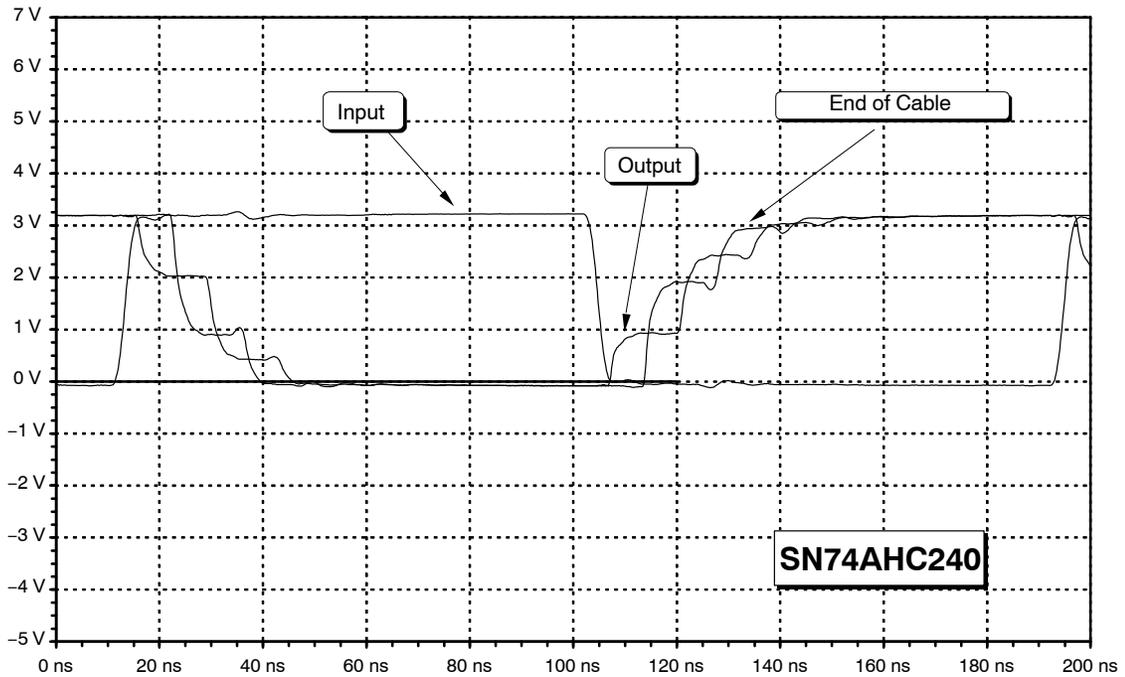


Figure 26. Output Waveforms of the SN74AHC240

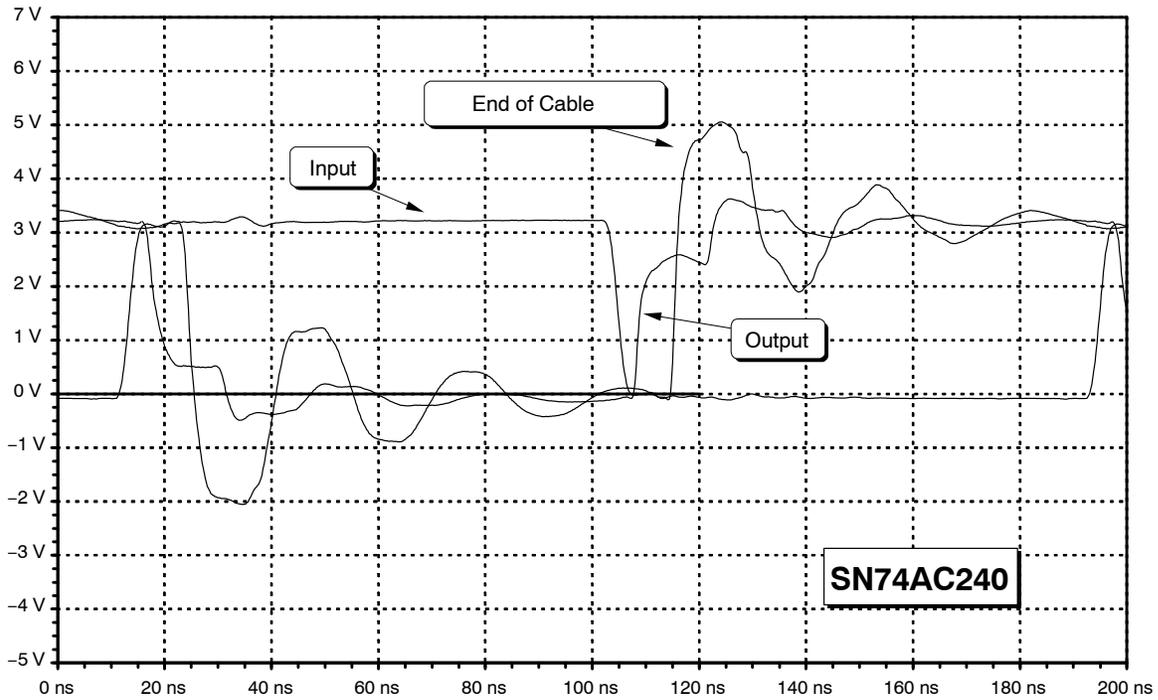


Figure 27. Output Waveforms of the SN74AC240

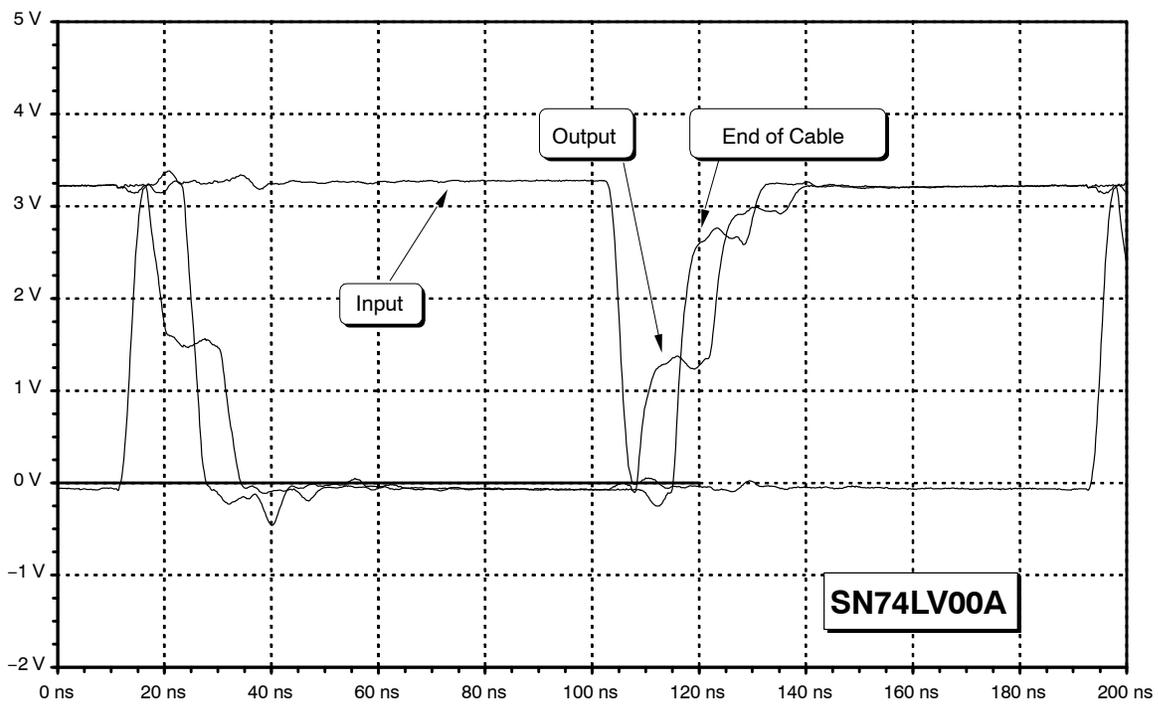


Figure 28. Output Waveforms of the SN74LV00A

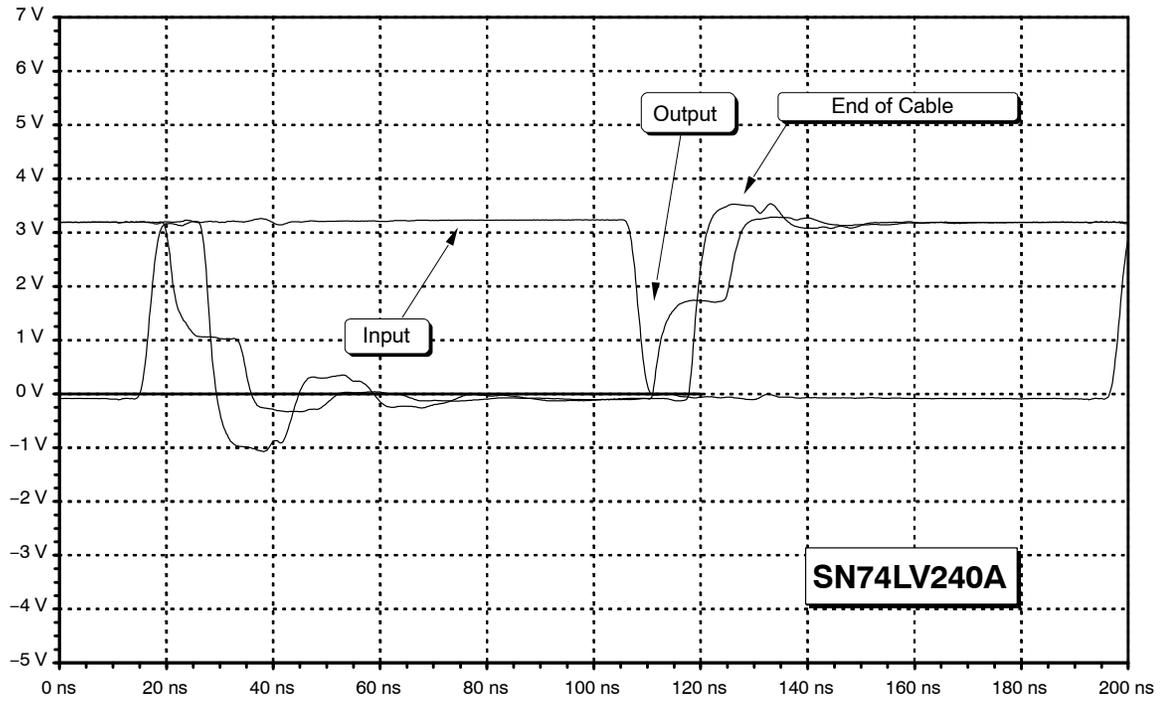


Figure 29. Output Waveforms of the SN74LV240A

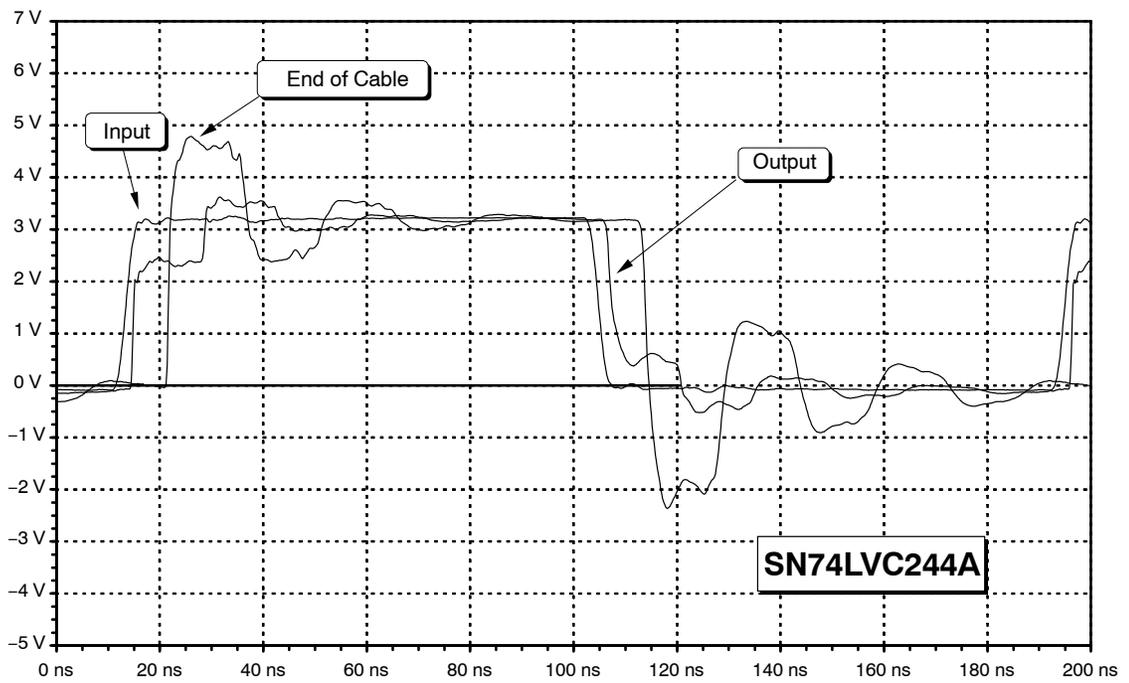
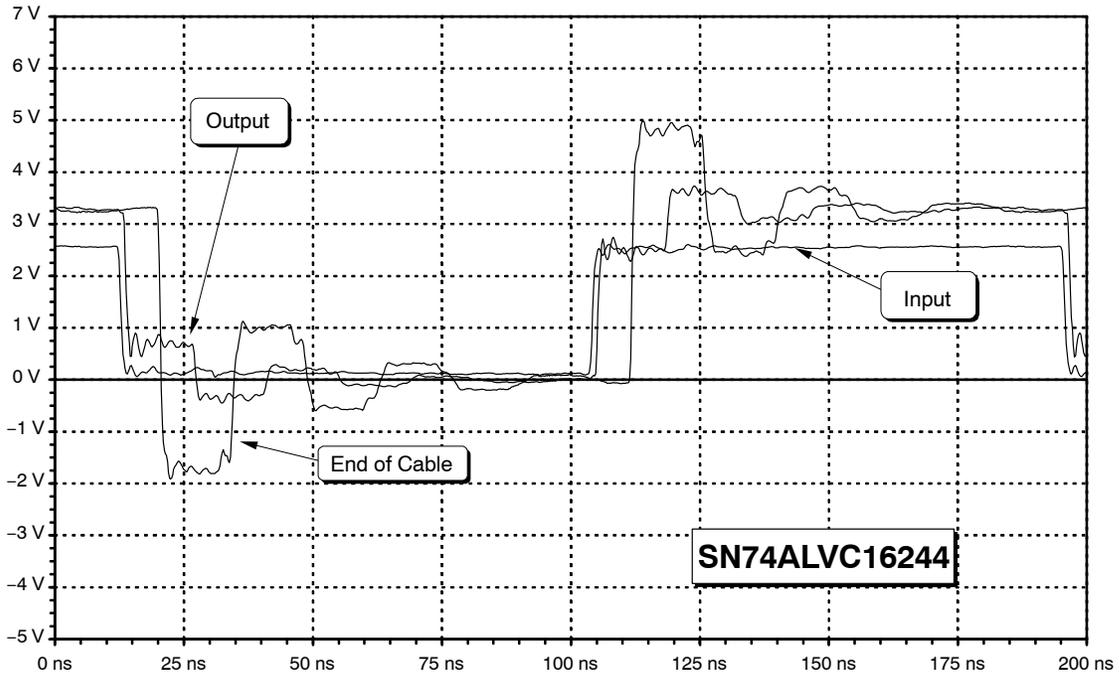
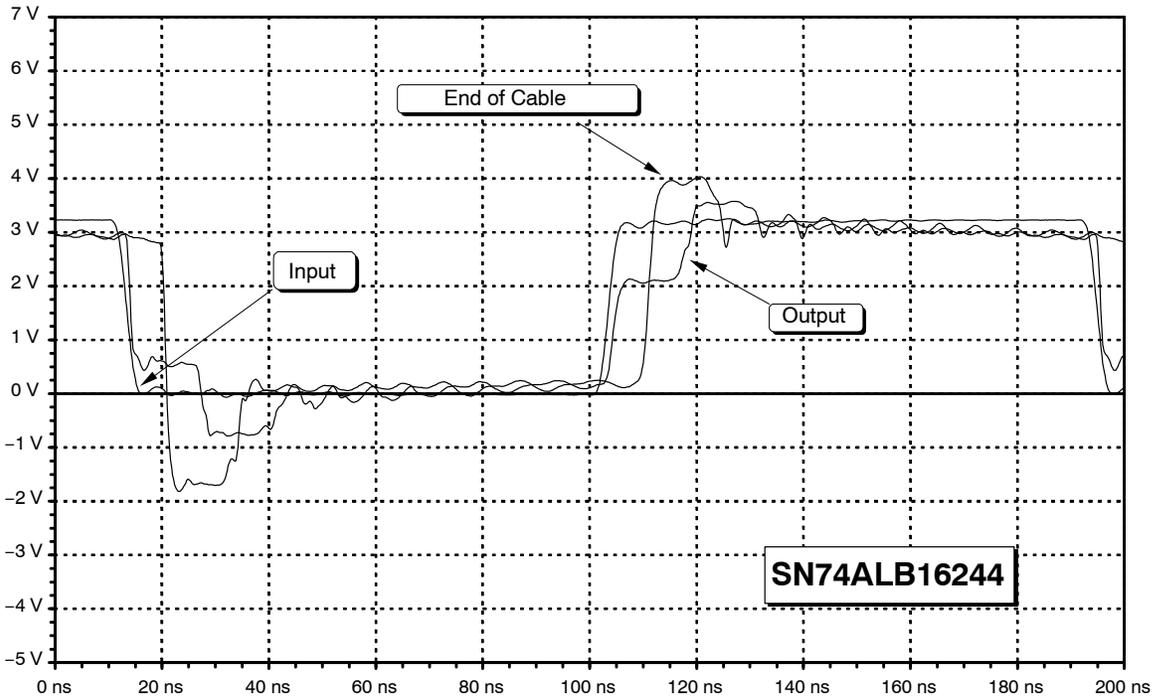


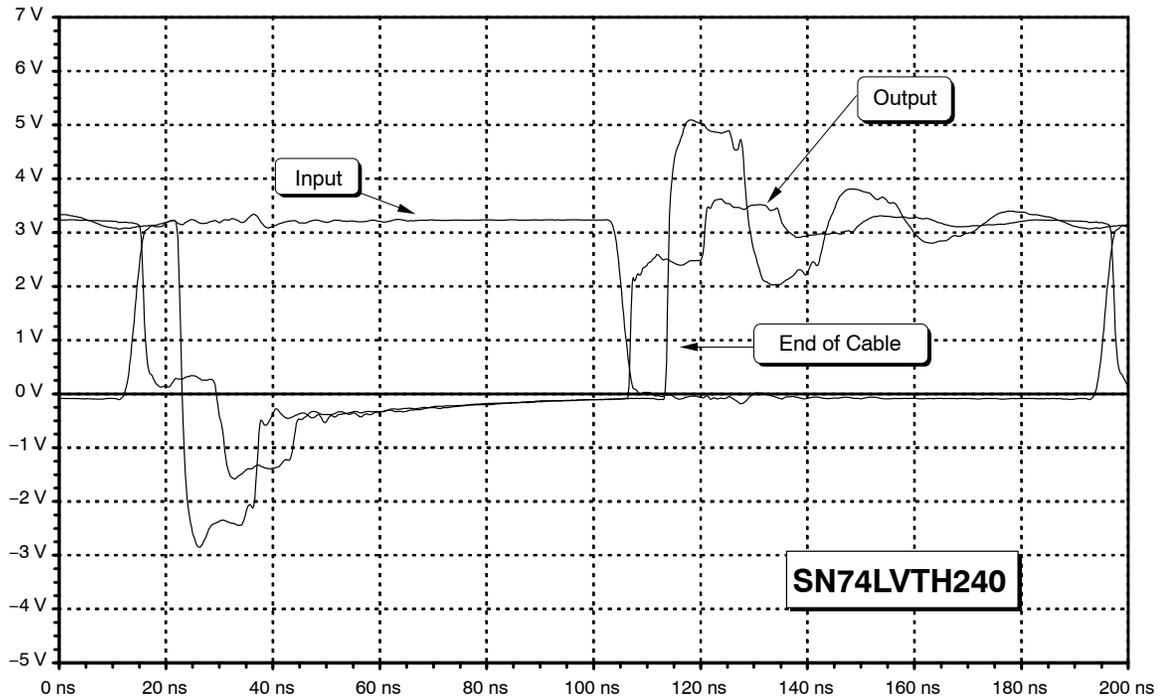
Figure 30. Output Waveforms of the SN74LVC244A



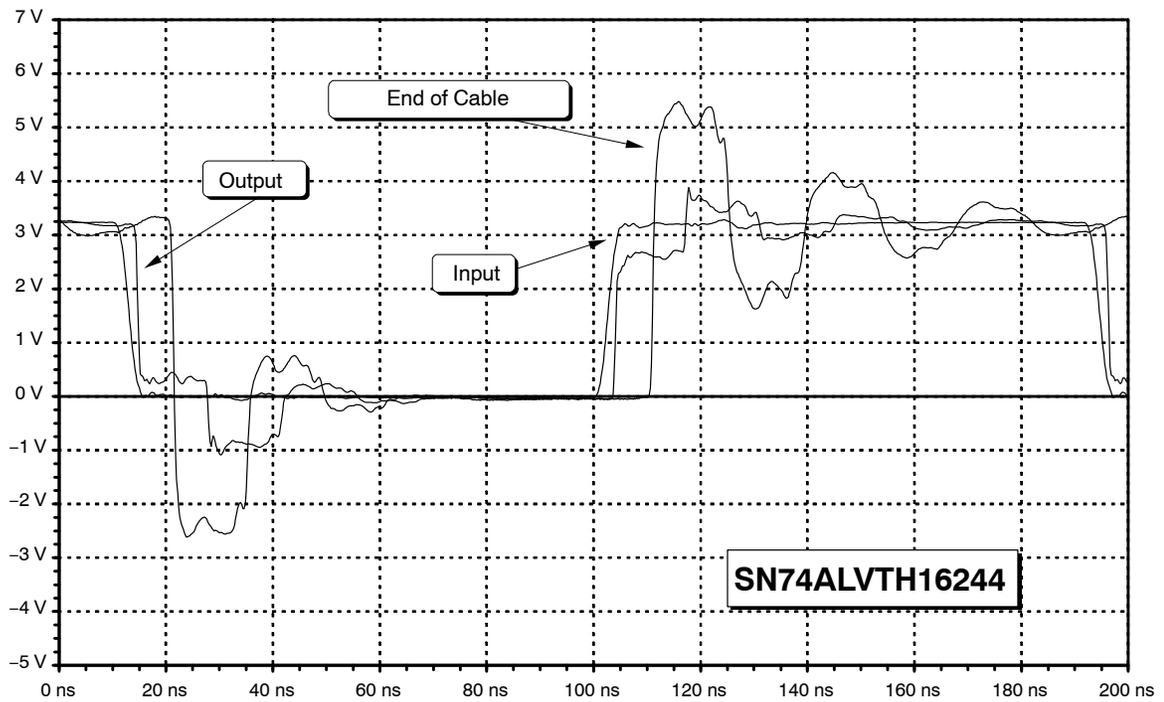
**Figure 31. Output Waveforms of the SN74ALVC16244**



**Figure 32. Output Waveforms of the SN74ALB16244**



**Figure 33. Output Waveforms of the SN74LVTH240**



**Figure 34. Output Waveforms of the SN74ALVTH16244**

## 6 Abbreviations and Glossary

5-V tolerance      Logic devices with 5-V tolerance allow 5-V CMOS logic levels at their inputs and outputs in the high-impedance state.

### A

Auto3-state      Devices tolerate a higher voltage level at the outputs during active high state at the output. Also called overvoltage protection.

SN74ALVC      Advanced Low-Voltage CMOS devices

SN74ALVT      Advanced Low-Voltage Technology devices

SN74AC      Advanced CMOS devices

SN74AHC      Advanced High-speed CMOS devices

### B

BiCMOS      Combination of bipolar and CMOS processes (CMOS input structure, bipolar output structure)

### G

GND      Ground

### I

I/O      Input/Output

### L

SN74LV      Low-Voltage CMOS devices, originally designed for  $V_{CC} = 3.3$  V; also specified at 5 V

SN74LVLC      Low-Voltage CMOS devices

SN74LVLT      Low-Voltage Technology devices with overvoltage protection (see auto3-state)

### R

$R_L$       Load resistor

### S

SN74S      Schottky devices

SPICE      Simulation Program with Integrated Circuit Emphasis

**T**

TTL level      Transistor-Transistor Logic level

**V**

V<sub>CC</sub>      Supply voltage

## 7 References

### 7.1 Documents Published by TI

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- Advanced CMOS Logic*, Data Book, 1996, literature number SCADE02.
- Logic Selection Guide and Data Book*, CD-ROM, April 1998, literature number SCBC001B.
- AHC/AHCT Logic Advanced High-Speed CMOS*, Data Book, 1997, literature number SCLD003A.
- Design Considerations for Logic Products*, Application Book, 1997, literature number SDYA002.
- Digital Design Seminar*, Reference Manual, 1998, literature number SDYDE01B.
- Designing With Logic*, March 1997, literature number SDYA009.
- The Bergeron Method: A Graphic Method for Determining Line Reflections in Transient Phenomena*, October 1996, literature number SDYA014.
- Bus-Interface Devices With Output Damping Resistors or Reduced Drive Outputs*, August 1997, literature number SCBA012A.
- Live Insertion*, October 1996, literature number SDYA012.
- Thin Very Small-Outline Package (TVSOP)*, March 1997, literature number SCBA009C.
- Low-Voltage Logic Families*, April 1997, literature number SCVAE01A.
- Bus-Hold Circuit*, July 1992, literature number SDZAE15.
- Electromagnetic Emission from Logic Circuits*, November 1998, literature number SZZA007.
- PCB Design Guidelines for Reduced EMI*, November 1998, literature number SZZA009.
- Input and Output Characteristics of Digital Integrated Circuits at 2.5-V Supply Voltage*, literature number SZZA012.
- Input and Output Characteristics of Digital Integrated Circuits at 5-V Supply Voltage*, literature number SZZA008.

### 7.2 Internet Information Sources

TI Semiconductor Home Page

<http://www.ti.com/sc>

TI Distributors

<http://www.ti.com/sc/docs/distmenu.htm>

TI Logic Home Page

<http://www.ti.com/sc/docs/asl/home.htm>

TI Logic Literature

<http://www.ti.com/sc/docs/asl/lit/lit.htm>

TI Product Information and Document Search

<http://www.ti.com/sc/docs/msp/download.htm>

## 8 Acknowledgment

The author of this document is Peter Forstner. Revisions were made by Johannes Huchzermeier.

# ***Input and Output Characteristics of Digital Integrated Circuits at 2.5-V Supply Voltage***

SZZA012  
January 2000



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## Abstract

This application report contains a comprehensive collection of the input- and output-characteristic curves of integrated circuits from various 2.5-V logic families. These curves go beyond the information given in data sheets by providing additional details regarding the characteristics of the devices. This knowledge is particularly useful, for example, when choosing a device for use in a bus system, or when the waveforms expected in a transmission system must be predicted using a Bergeron chart. These oscillograms assist in generating models for simulation programs that analyze the dynamic behavior of the devices in a particular environment.

## 1 Introduction

For a long time, a 5-V supply voltage was standard for the design of new systems. However, with the reduction of the supply voltage, system power consumption can be reduced directly, as shown by the general formula for power consumption:

$$P_{\text{STAT}} = V_{\text{CC}} \times I_{\text{CC}} \quad (1)$$

Compared to a 5-V system, 3.3-V systems save about one-third and 2.5-V systems save about one-half of the consumed energy. However, with the reduction of the supply voltage, drive capability of the logic circuit also is reduced.

The parameters in the data sheet give only a very limited indication of a device's behavior in a system. For example, data sheets generally give only information regarding the behavior over the input and output (I/O) voltage range of 0 to 5 V, 3.3 V, and 2.5 V. The output currents specified over this range provide an incomplete picture of in-system performance.

Behavior of the device outside the usually accepted operating conditions is often of interest. For example, this is true when the characteristic curves are needed to predict signal waveforms resulting from line reflections.

By using the I/O characteristics and the Bergeron method, along with a knowledge of the load resistance, the amplitude of the line reflections can be determined.

This report presents I/O characteristics of integrated logic circuits that operate at  $V_{\text{CC}} = 2.5$  V, mainly those that originally were designed for 3.3-V  $V_{\text{CC}}$ . However, many modern logic families are specified at multiple supply voltages. For example, AHC logic can be used at 5-V, 3.3-V, or 2.5-V supply voltage. Because three main voltages are used, I/O characteristics are provided for each voltage level. This application report deals exclusively with devices operated at 2.5 V.

Two other application reports regarding this topic are available:

- *Input and Output Characteristics of Digital Integrated Circuits at 5-V Supply Voltage*, literature number SZZA008
- *Input and Output Characteristics of Digital Integrated Circuits at 3.3-V Supply Voltage*, literature number SZZA010

With the wide range of devices available, information in this application report is limited to typical characteristics. In Sections 2 and 3, the I/O characteristics of the following devices are shown as being representative of other components that behave similarly in operating circuits:

- '00                    The characteristic curves of this NAND gate are representative of all logic devices having normal drive capability, such as gates, flip-flops, counters, multiplexers, etc.
- '240/'244            The output characteristics of these bus-interface devices are of particular importance in deciding which family should be used for a specific system requirement. As mentioned elsewhere in this application report, the available output current has a decisive influence on the distortion of signals on bus lines.
- '16240/'16244      The output characteristics of these bus-interface devices correspond with the '240/'244 functions regarding the electrical behavior. However, these devices have 16 drivers within one package. This feature meets the market requirements, because modern designs are based on wider buses using 16 bits, 32 bits, or more bits on the backplanes. Further, the noise behavior of Widebus™ devices shows a significant improvement over the standard octal packages.

Table 1 lists representatives of the different logic families and gives an overview of I/O characteristics presented in Sections 2 and 3.

**Table 1. Representatives of the Different Logic Families**

FAMILY	TYPE		
	'00	'240/'244	'16244
SN74AHC	√	√	
SN74AC	√	√	
SN74LV	√	√	
SN74LVC	√	√	
SN74ALVC			√
SN74ALB			√
SN74ALVT			√
SN74LVT		√	

Because the input characteristics depend exclusively on the technology used, not on the logical function of the device, only one representative per logic family is shown (gate function '00 or driver function '240) in Section 2.

Section 4 shows how to calculate line reflections using the Bergeron method and data from the SN74ALVCH16240 device.

Measurement results demonstrating different switching behaviors of the various logic families are given in Section 5. For these measurements, the devices under test were loaded with a 1.3-m-long coaxial cable having a characteristic impedance of 50 Ω; the end of the line was not connected, i.e., open circuit. These waveforms provide good insight into the dynamic behavior of the devices.

Texas Instruments (TI™) offers the advanced very low-voltage CMOS (AVC) logic family as an optimized solution for the next low-voltage node with 2.5-V supply voltage. The TI application report, *AVC Logic Family Technology and Applications*, literature number SCEA006A, discusses the features and benefits of 2.5-V logic.

## 2 Input Characteristics

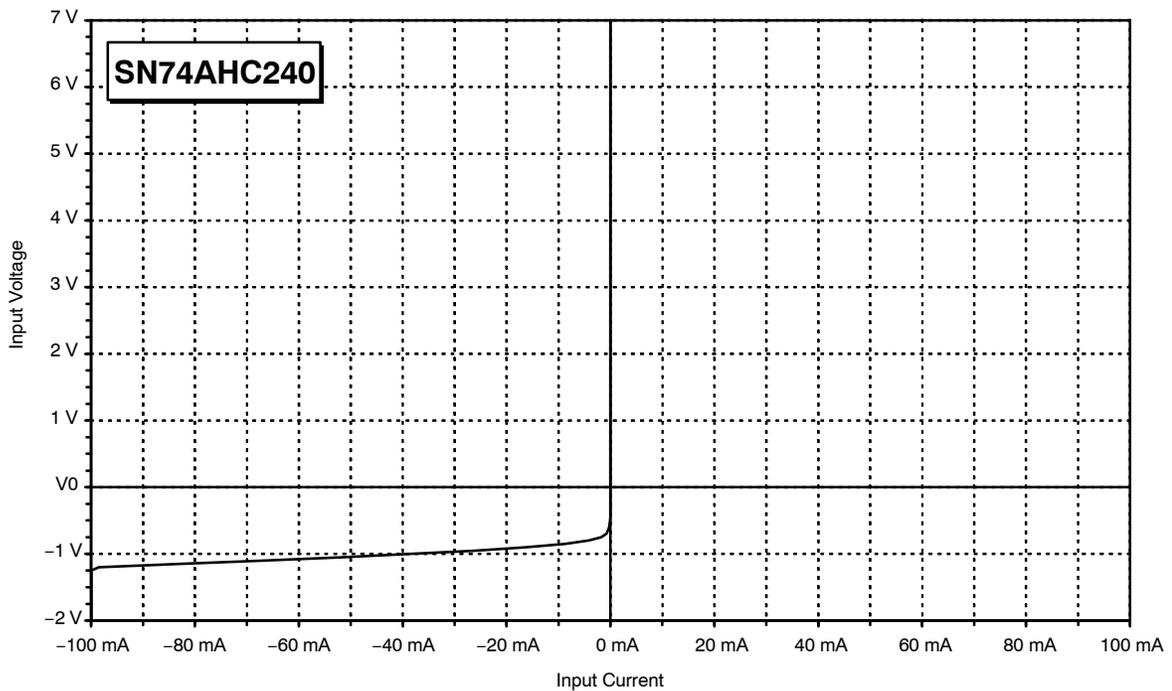
The high impedance of the input stage of the logic circuit determines the input characteristics of logic circuits in the positive range (see Figures 1 through 5).

All logic families that are discussed in this report have CMOS input stages and use technologies based either on the CMOS or BiCMOS manufacturing process. In both cases, CMOS input stages are used. CMOS input stages are controlled exclusively by the applied voltage so there is no current flowing into the input stage. Therefore, the input impedance of CMOS and BiCMOS devices is in the megohm range. Negative-voltage peaks are limited by a protection diode.

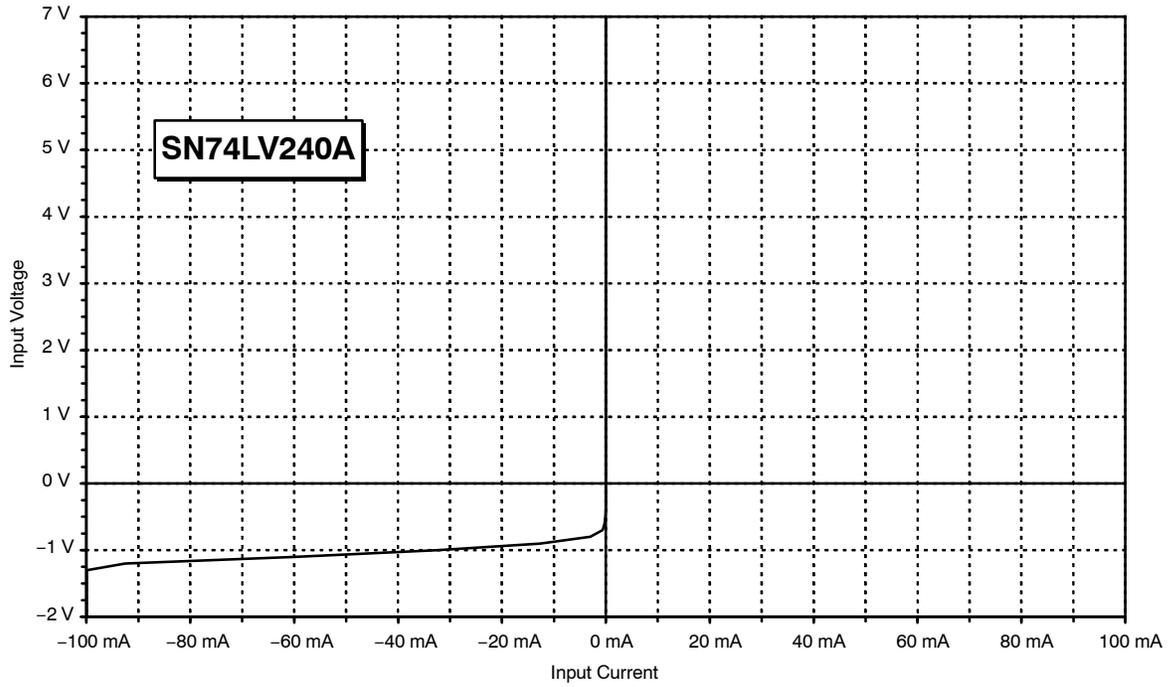
The bus-hold circuit represents a special circuit in the input stages of the LVT and ALVT logic families and, optionally, is available in the LVC and ALVC devices. Inputs of devices that have the bus-hold circuit hold the last valid logic state. This feature is useful if an input stays undefined, for example, during a high-impedance state on the bus. Using the bus-hold circuit eliminates the need for pullup or pulldown resistors. Devices with the bus-hold circuit have H in their part number, for example, SN74LVTH245.

A more detailed application report, *Bus-Hold Circuits*, literature number SDZAE15, is available from TI.

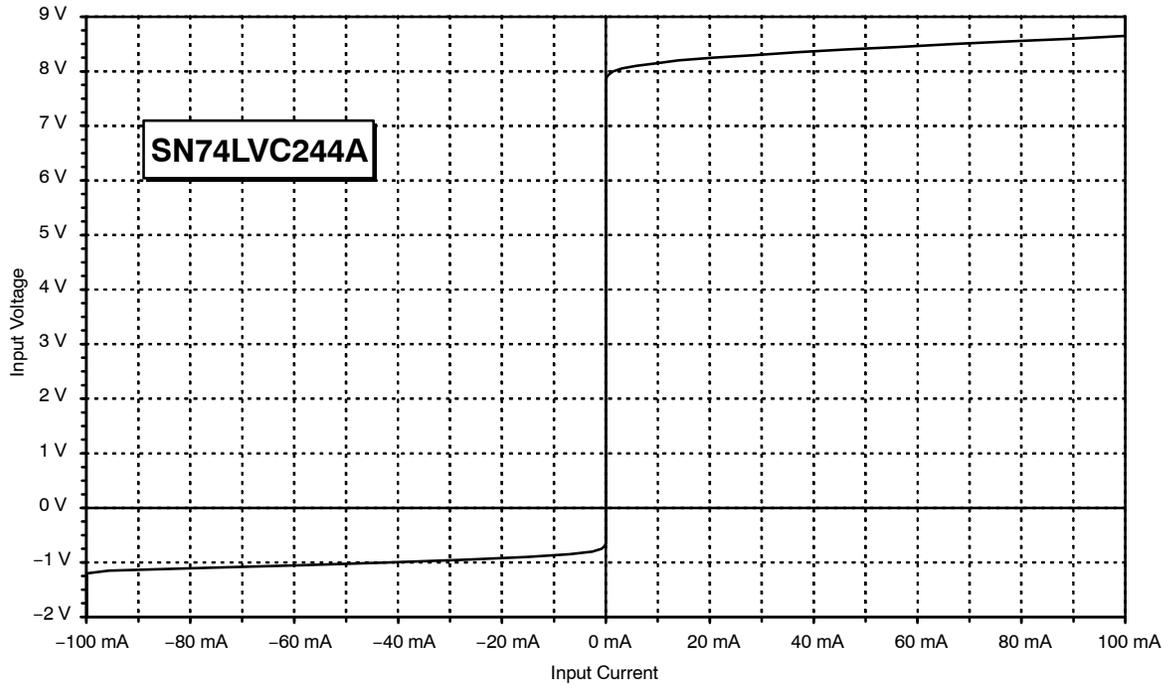
Other application reports and literature are listed in Section 7.



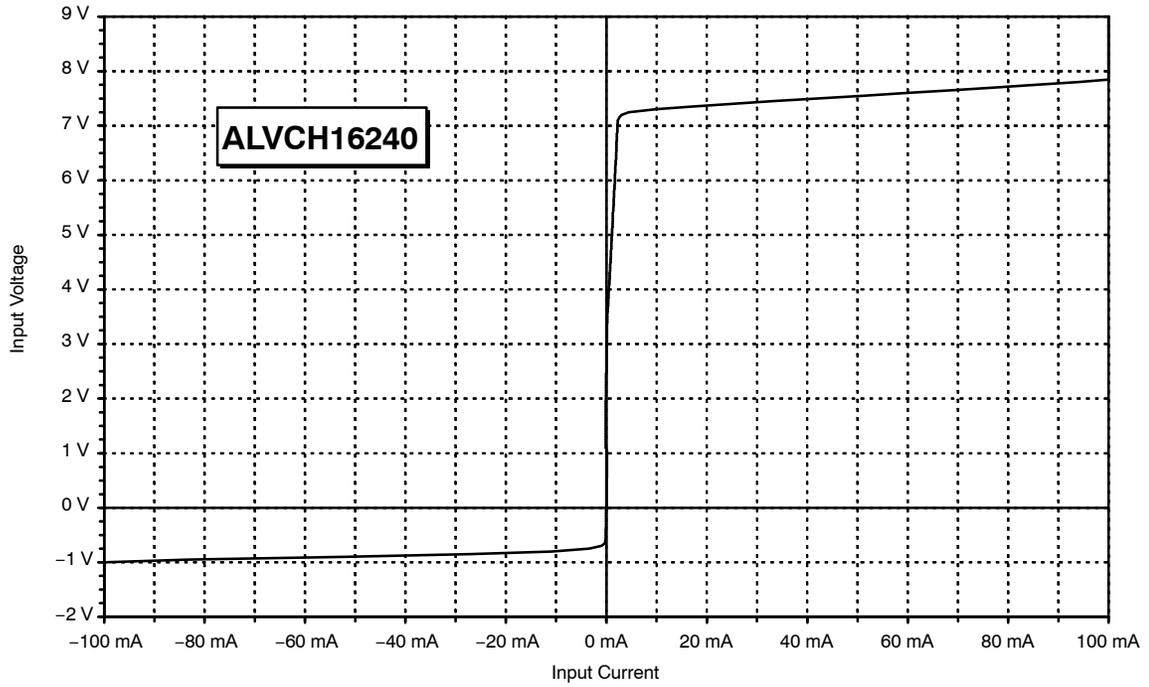
**Figure 1. Input Characteristic of the SN74AHCxxx Series**



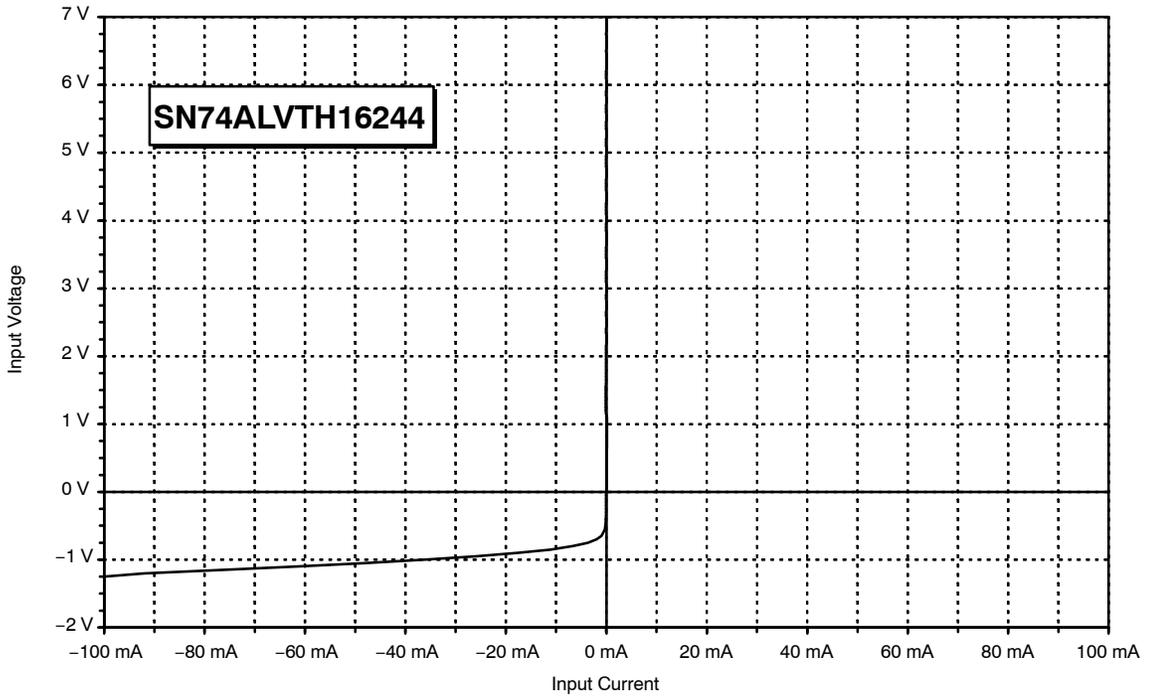
**Figure 2. Input Characteristic of the SN74LVxxx Series**



**Figure 3. Input Characteristic of the SN74LVCxxx Series**



**Figure 4. Input Characteristic of the SN74ALVCHxxx Series**



**Figure 5. Input Characteristic of the SN74ALVTHxxx Series**

### 3 Output Characteristics

The output stage of a logic device in the high logic state behaves like a voltage source with an open-circuit voltage of  $V_{CC}$  for CMOS logic, low-voltage BiCMOS logic, respectively. The internal resistance for the high state is inversely proportional to the drive capability of the device. The internal resistance for standard logic families is  $15\ \Omega$  to  $60\ \Omega$ .

In the low logic state for positive voltages, the output resistance is based on the internal resistance of the conducting transistor, i. e., collector-emitter for BiCMOS technologies and drain-source resistance for CMOS technologies. Negative-voltage peaks are again limited by a protective diode. The output stages of some CMOS logic families (e.g., SN74AHC) also have an output protective diode that is connected to  $V_{CC}$ . This diode limits the positive output voltage to  $V_{CC} + 0.7\ \text{V}$ .

#### 3.1 Series Damping Resistors (SN74XXX2xxx, SN74XXXR2xxx Devices)

In the LVC, ALVC, LVT, and ALVT families, TI offers driver options with integrated series resistors of about  $25\ \Omega$ .

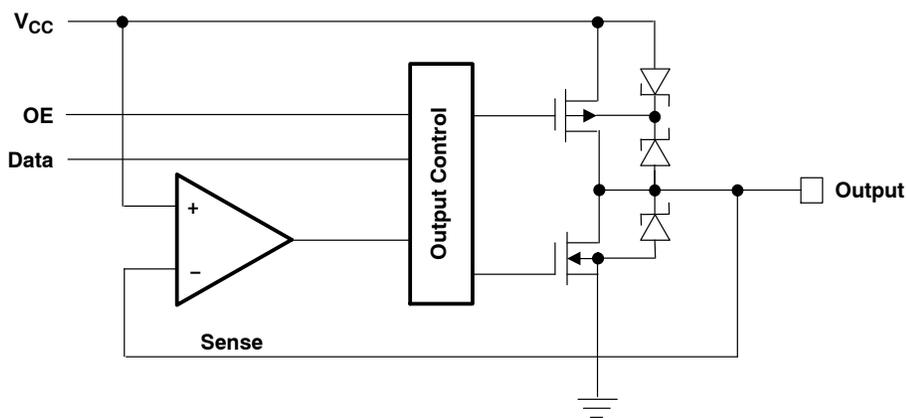
With damping resistors in the output stage, the effective output impedance of the driver is about  $50\ \Omega$ . If the value of the line impedance is also in the range of  $50\ \Omega$ , no line reflections are observed at the output of the device. In this case, the beginning of the line is terminated perfectly. This option is especially beneficial in memory applications where overshoots and undershoots can cause malfunctions. In point-to-point applications, near-ideal signal shapes can be achieved. The 2 in the part number indicates the series damping resistor on the output port, for example, SN74ALVCH162244. The R indicates series damping resistors on both ports of bidirectional devices, for example, the SN74ALVCHR16245.

Further information about series damping resistors is given in the TI application report, *Bus-Interface Devices With Output Damping Resistors or Reduced-Drive Outputs*, literature number SCBA012.

Other application reports and literature is listed in Section 7.

#### 3.2 Auto3-State Output of the ALVT Family

The auto3-state function, which is implemented in the output stages of the ALVT family, represents a specialty. The principle is shown in Figure 6. Output characteristics of representative devices are shown in Figures 7 through 14.



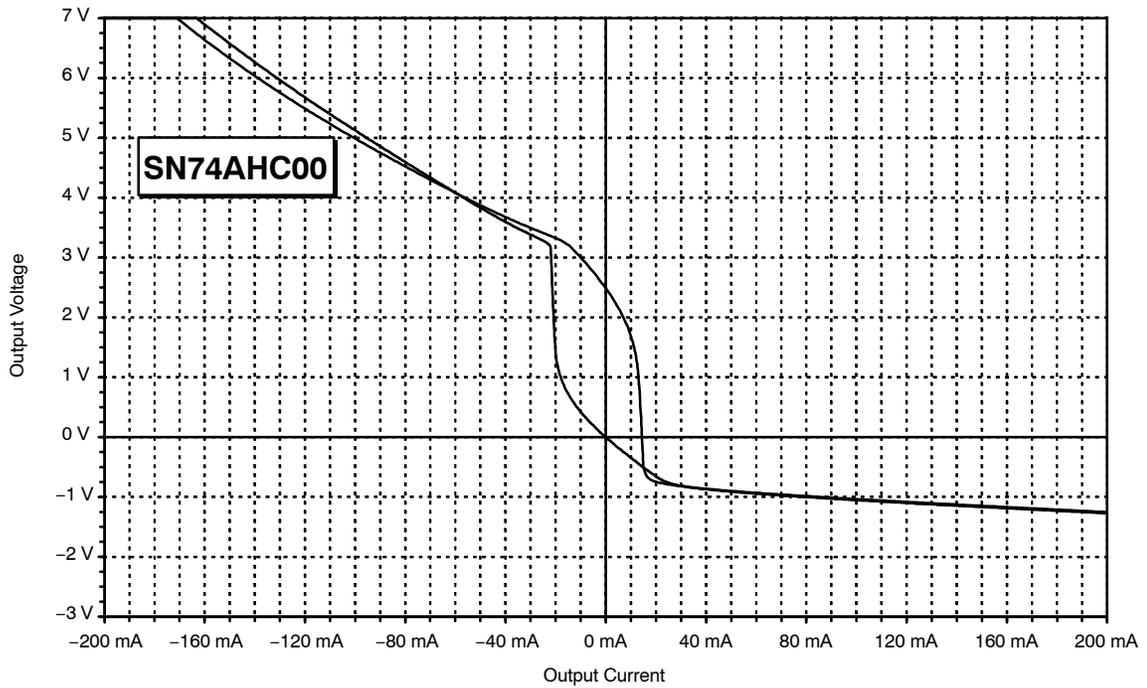
**Figure 6. Simplified Auto3-State Output Stage of ALVT Devices**

Assume that the output is in the active-high state and a comparator monitors the voltage at the output and compares it with the supply voltage. If the voltage that is applied externally to the output exceeds the supply voltage, the output stage is switched to the high-impedance state. In this case, the logic levels applied to the data and control input pins of the device are irrelevant.

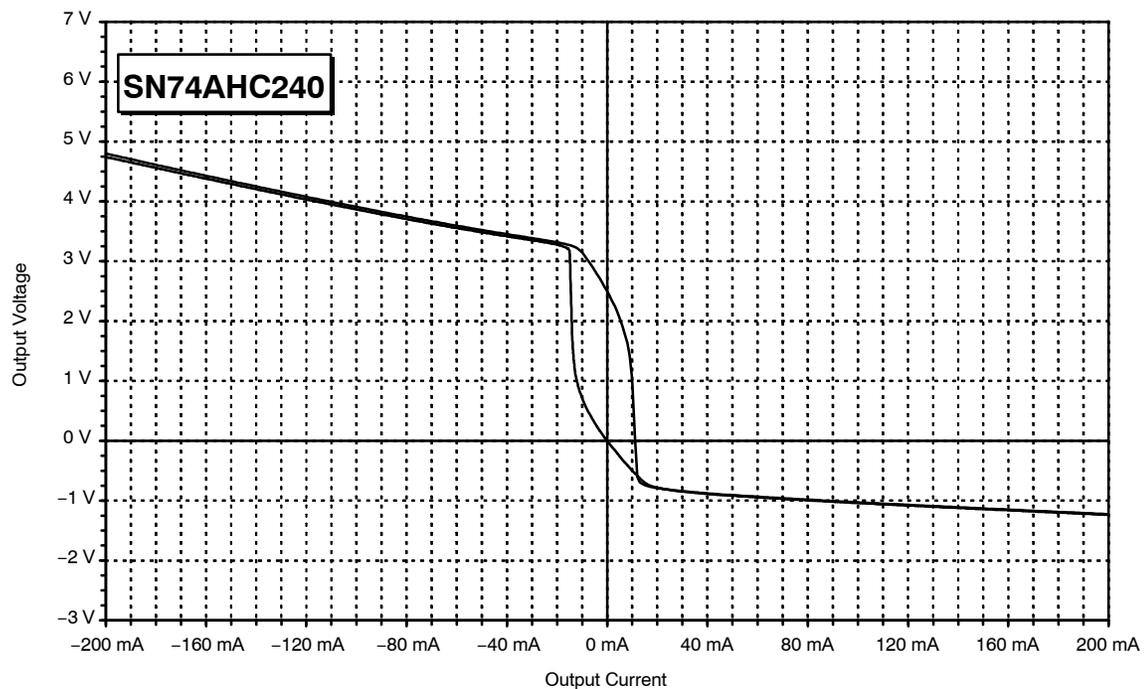
A current of about  $30\ \text{mA}$  is needed to trigger the auto3-state circuit so that bus contentions are prevented, but switching noise does not trigger the protective circuit. However, this also implies that the auto3-state cannot be implemented by using a simple pullup resistor.

Current can flow into the output only in the case of an active high. If the output is set to high impedance by the OE control pin, no current flows.

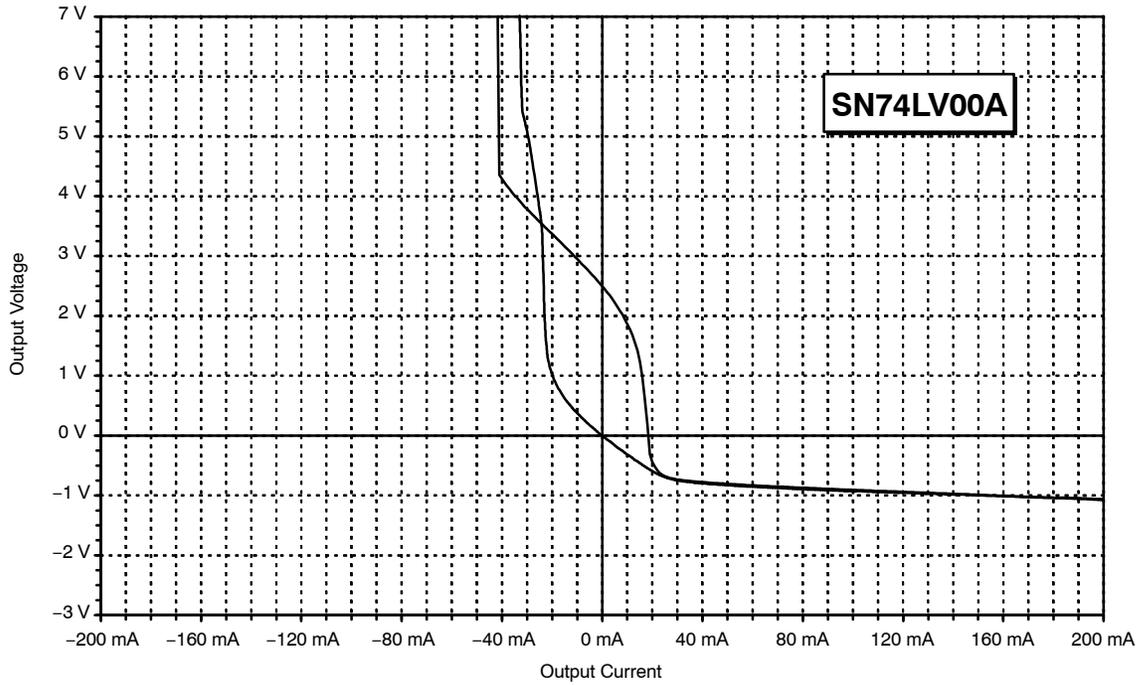
The series-opposed Schottky diodes always connect the back gate of the pullup transistor of the output stage to the higher voltage that is either  $V_{CC}$  or the voltage that can be applied externally to the output. In this way, current flow from the output to  $V_{CC}$  is suppressed.



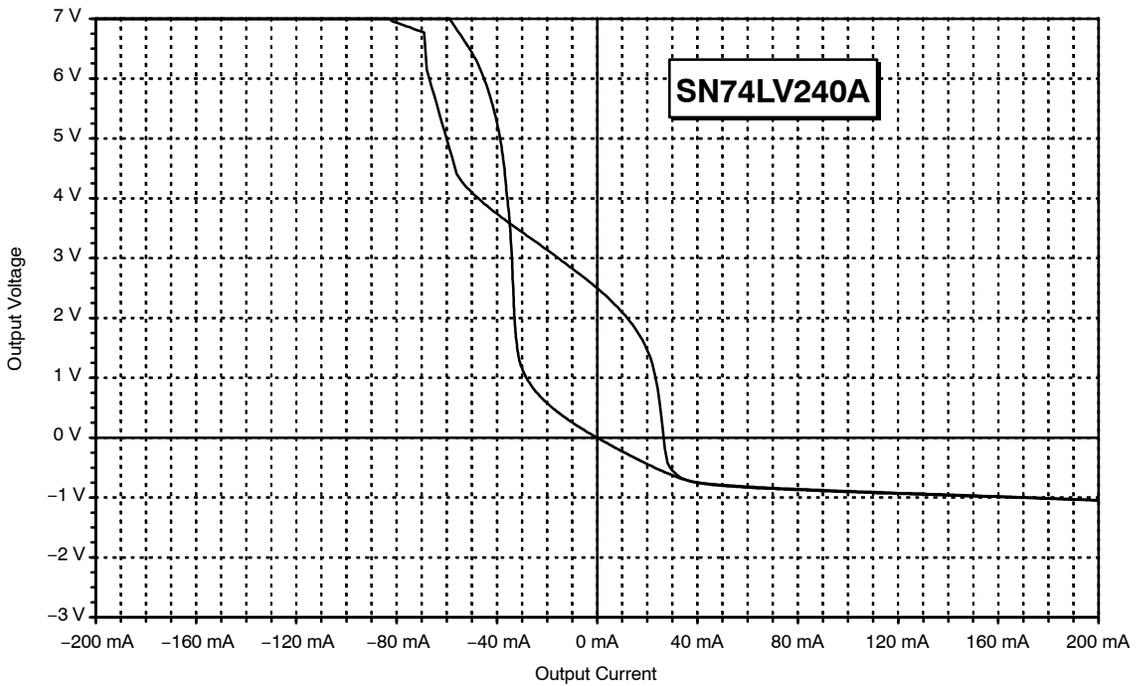
**Figure 7. Output Characteristics of the SN74AHC00**



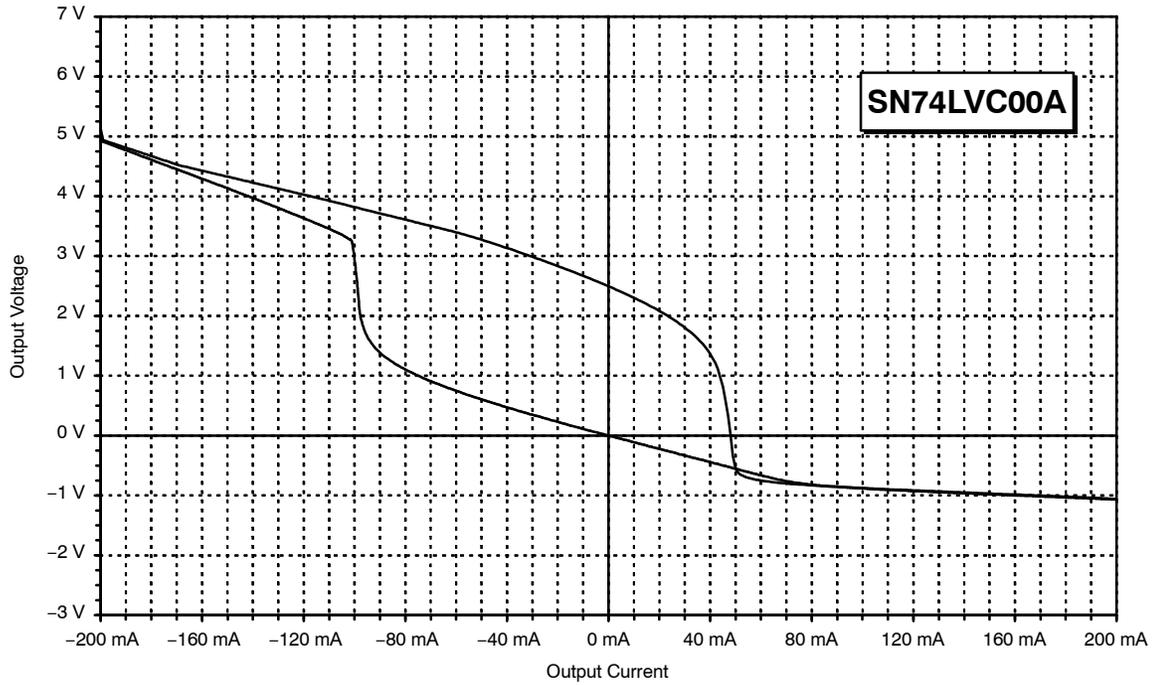
**Figure 8. Output Characteristics of the SN74AHC240**



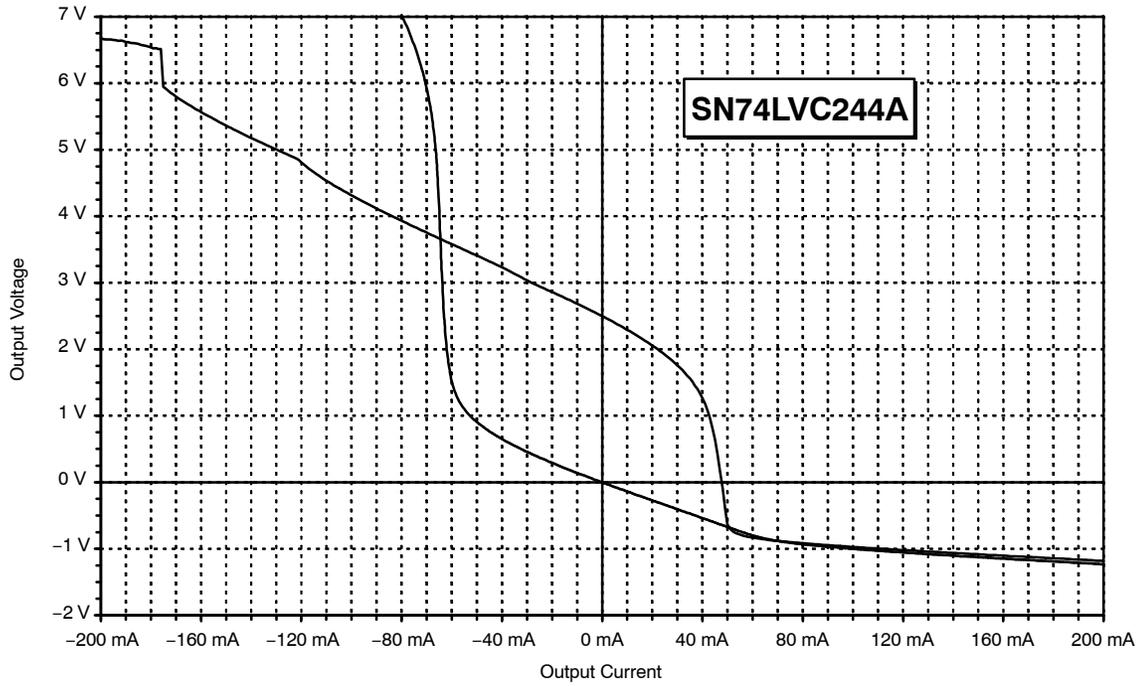
**Figure 9. Output Characteristics of the SN74LV00A**



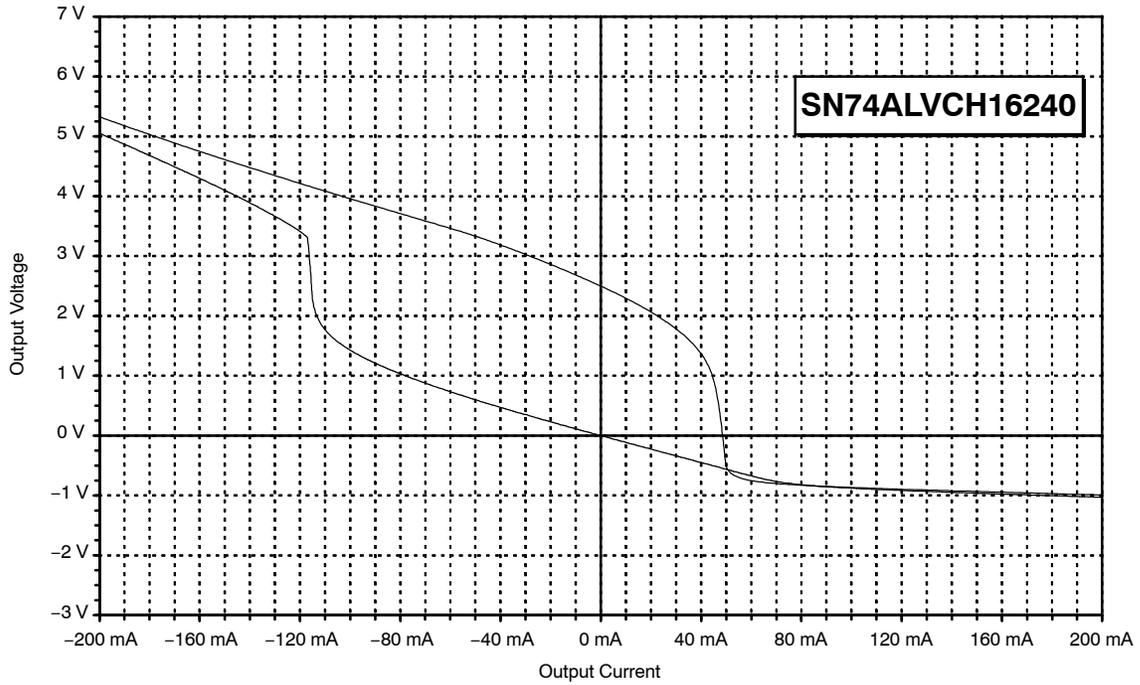
**Figure 10. Output Characteristics of the SN74LV240A**



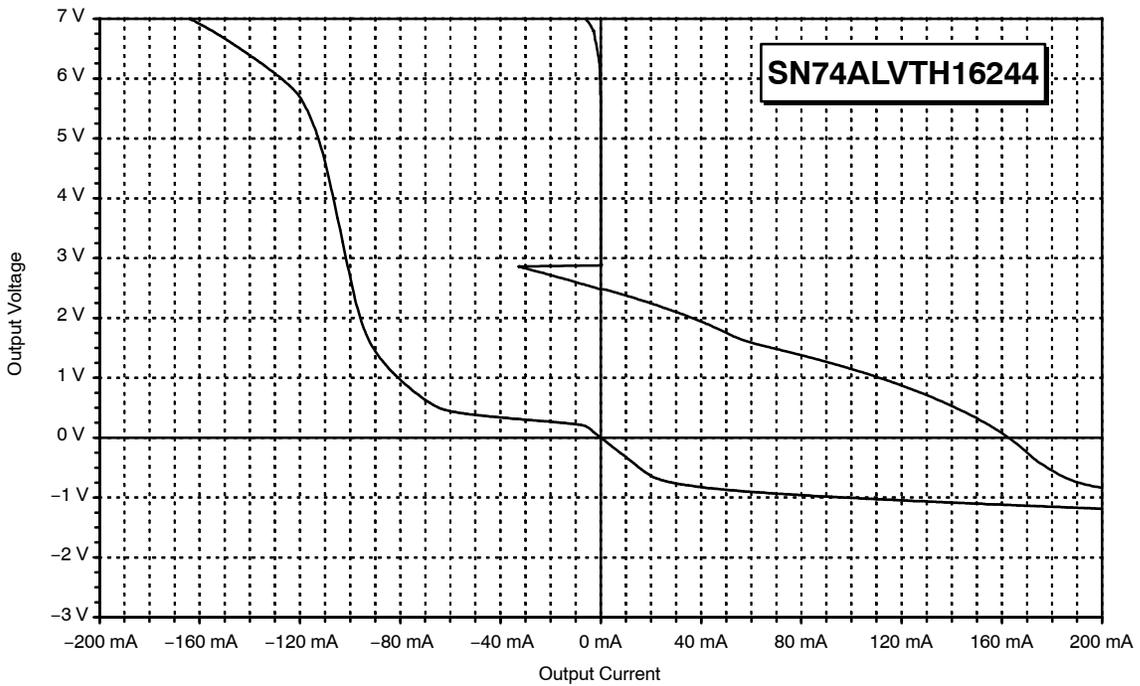
**Figure 11. Output Characteristics of the SN74LVC00A**



**Figure 12. Output Characteristics of the SN74LVC244A**



**Figure 13. Output Characteristics of the SN74ALVCH16240**



**Figure 14. Output Characteristics of the SN74ALVTH16244**

## 4 Bergeron Method Applied to the SN74ALVCH16240

The input and output characteristics, shown in Sections 2 and 3, can be used to determine the signal reflections within a certain application by using a graphical procedure known as the Bergeron method.

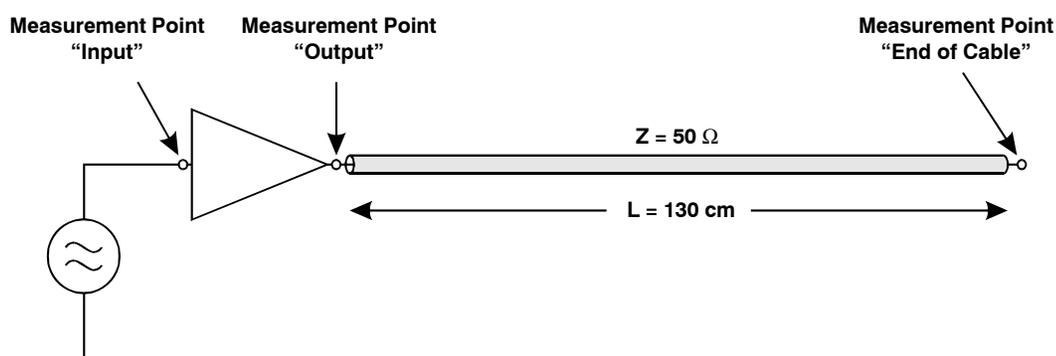
The prerequisite for the use of the Bergeron method is that the lines exceed a certain length:

*If the rise time or the fall time of a signal is shorter than twice the propagation delay on the line, the line theory must be applied.*

In practice, for a line with a signal propagation of 5 ns/m and a signal with a rising or falling edge of 2 ns, starting with a line length that exceeds 20 cm [ $2 \text{ ns} / (5 \text{ ns/m} \times 2)$ ], the line theory must be applied.

For a bus line, the signal propagation delay increases to 25 ns/m, so that, in this case, the line theory must be applied for a line length that exceeds 4 cm [ $2 \text{ ns} / (25 \text{ ns/m} \times 2)$ ].

The SN74ALVCH16240 device was tested, using the measurement setup shown in Figure 15. The Bergeron method was used to predict the signal shape.



**Figure 15. Measurement Setup for the Bergeron Method**

The first step in the graphical solution using the Bergeron method is to draw the following characteristics in a voltage-versus-current diagram:

- Output characteristics of the SN74ALVCH16240 device
- Load characteristic at the end of the line

The output characteristics are taken directly from Figure 13. The load characteristic equals the Y axis for the investigated case because no resistor is connected to the end of the line ( $R_L = \infty$ ).

The intersection between the load characteristic and the output characteristic represents the steady states, the current and voltage values at the line start, and the end of the line at the time  $t < 0$ , respectively.

### 4.1 Voltage Value at the Output of the Driver

For the low-to-high transition, draw a straight line, starting at the intersection of the output-low characteristic and the load characteristic. For the high-to-low transition, start the straight line at the cross point of *output-high* characteristic and the load characteristic.

The line impedance,  $Z_O$ , determines the steepness of this line. In the example, the line impedance is  $50 \Omega$ .

The intersection of this straight line and the output characteristics equals the voltage and current values at the beginning of the line at the time  $\tau = 0$ .

## 4.2 Voltage Value at the End of the Line

Now, a straight line with the steepness  $-Z_O$  is drawn through this point. The intersection between this line and the load characteristics results in the voltage values at the end of the line after one propagation delay time of the line, that is, after  $\tau = 1$ .

Afterward, the procedure is repeated, applying straight lines to the output characteristics and the load characteristics.

The steepness of the straight line is:

- $-Z_O$  from the output characteristics to the load characteristics
- $Z_O$  from the load characteristics to the output characteristics

In this way, current and voltage values are obtained:

- At the end of the line, at the times  $\tau = 1, 3, 5 \dots$
- At the line start, at the times  $\tau = 2, 4, 6 \dots$

The Bergeron diagram is shown in Figure 16. The related diagram (see Figure 17) shows the line reflections.

The calculated values of the Bergeron procedure match very well with the measured signal shapes. Another TI application report, *The Bergeron Method: A Graphic Method for Determining Line Reflections in Transient Phenomena*, literature number SDYA014, describes the graphic procedure in more detail

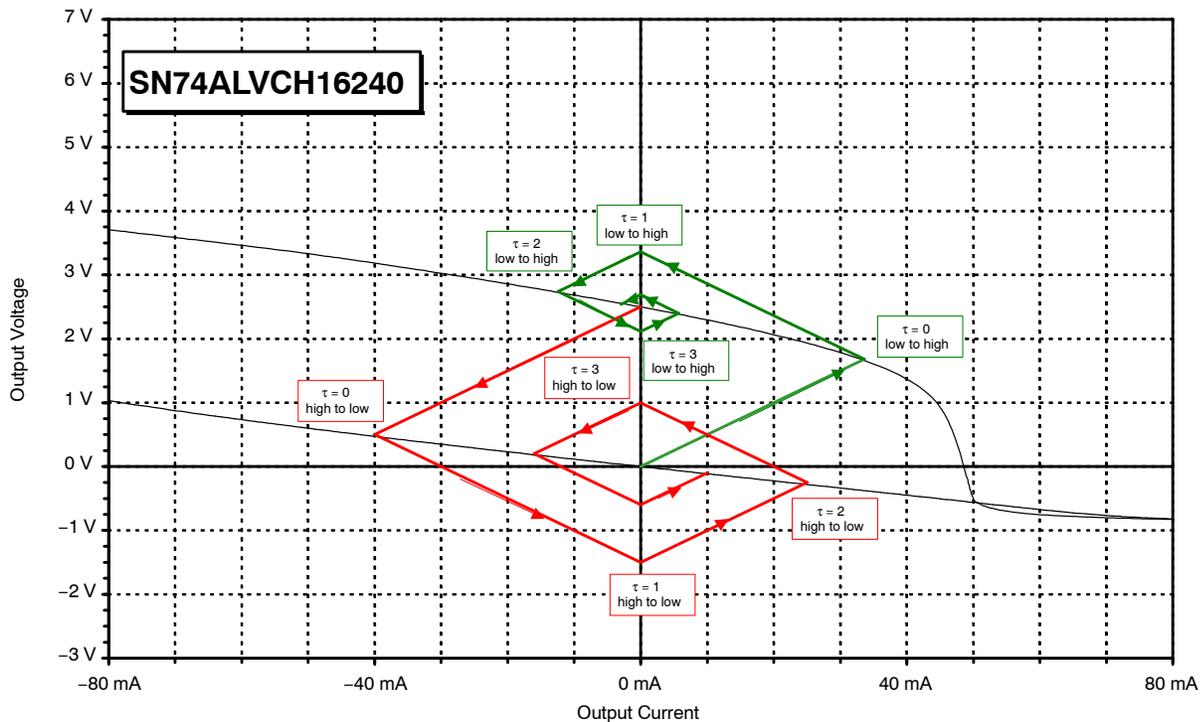
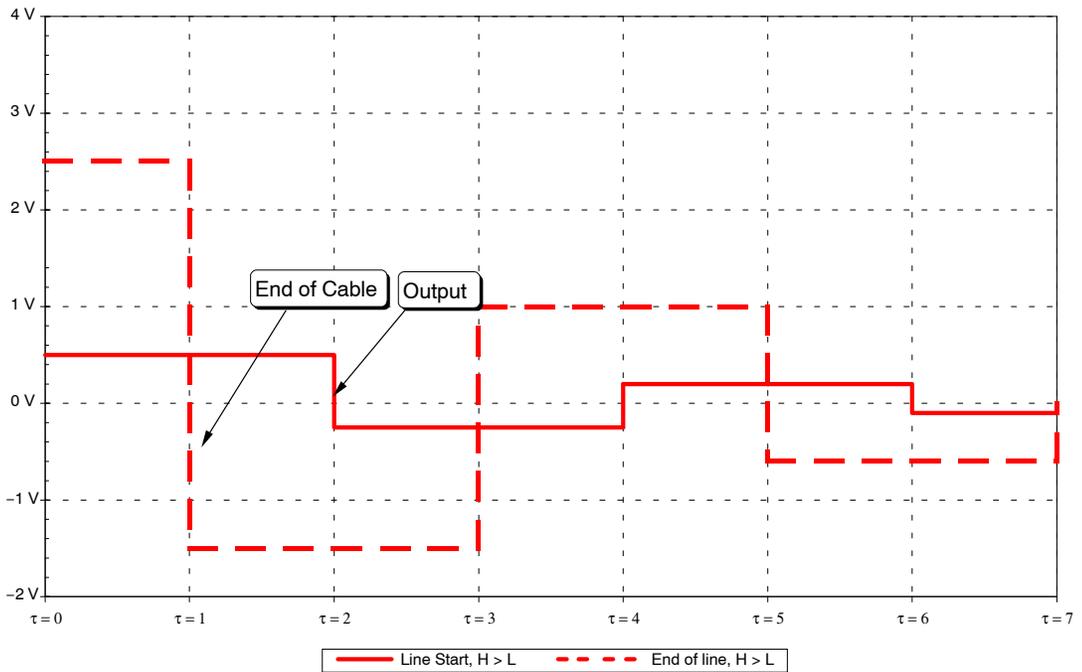
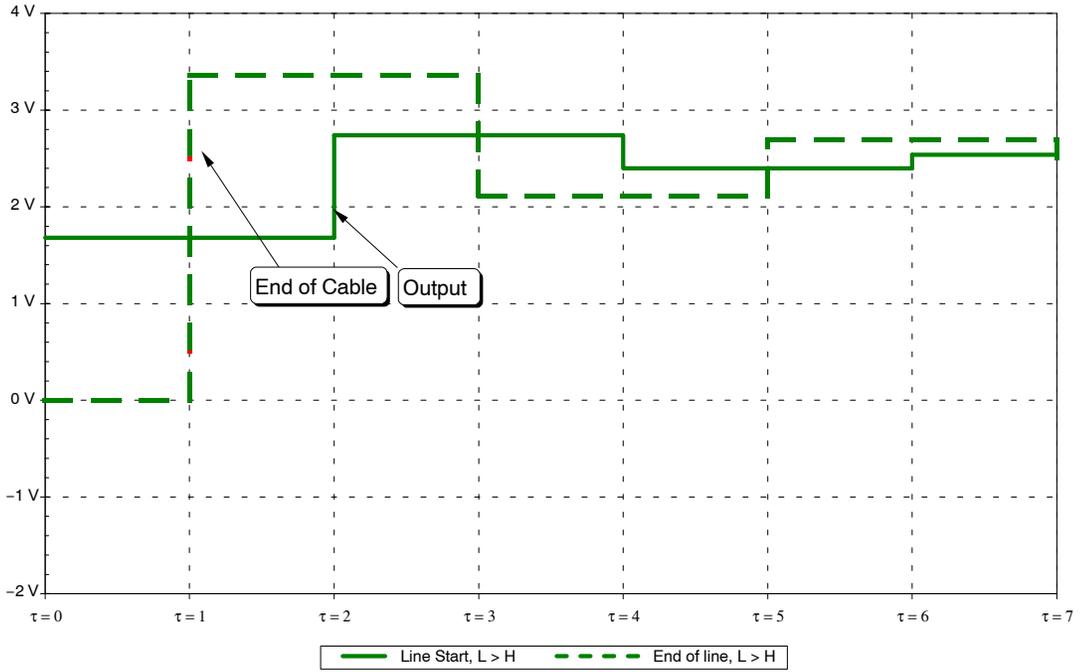


Figure 16. Bergeron Diagram for the SN74ALVCH16240



**Figure 17. Diagram of Line Reflections for the SN74ALVCH16240**

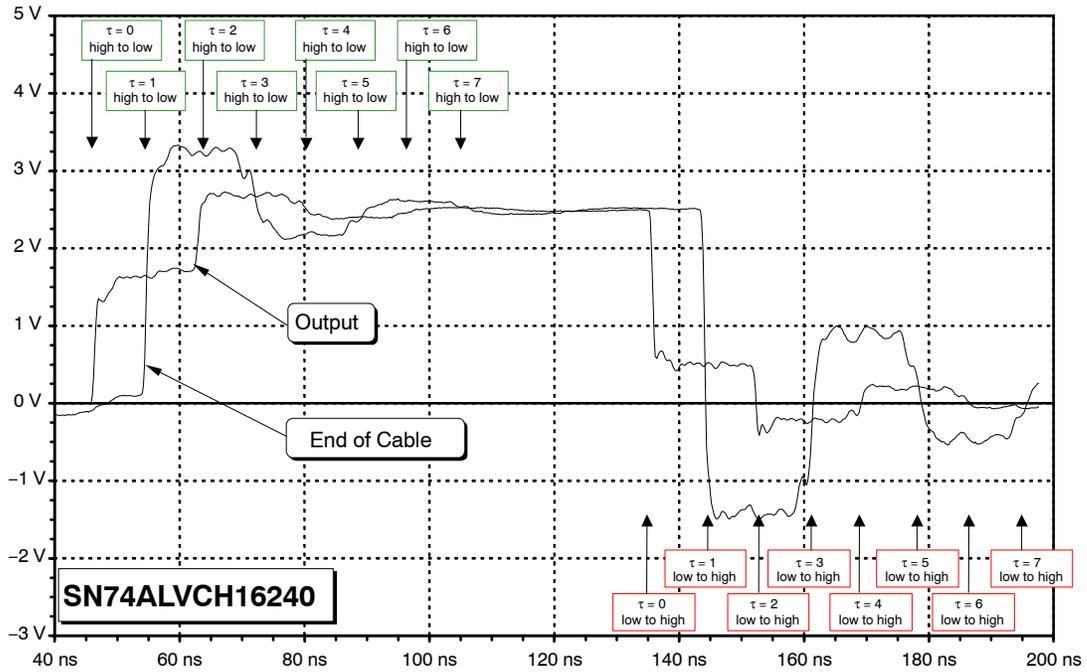
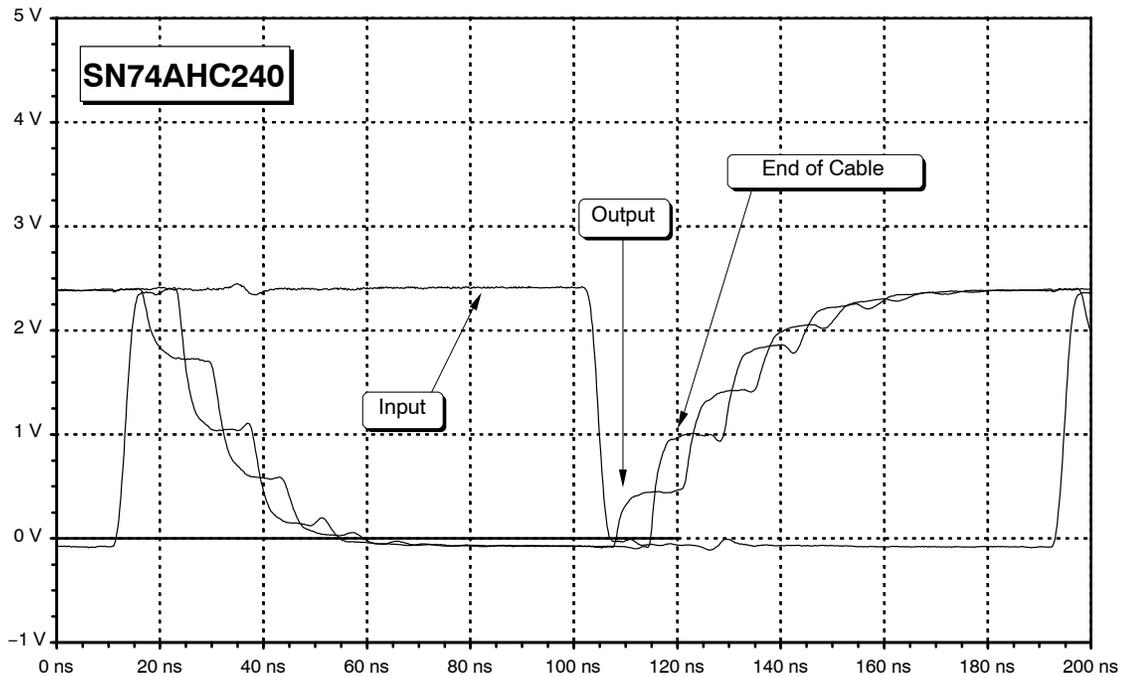


Figure 18. Signal Shape of the SN74ALVCH16240

## 5 Output Waveforms

Figures 19 through 25 show the measured voltage waveforms of typical output stages. Figure 15 shows the measurement setup. For these measurements, the devices under test were loaded with a 1.3-m coaxial cable having a characteristic impedance of  $50\ \Omega$ ; the end of the line was not connected, i.e., open circuit.

These waveforms provide good insight into the dynamic behavior of the devices. In particular, the oscillograms provide information regarding drive capability with a low-resistance load, together with an indication of the line reflections that can be expected.



**Figure 19. Output Waveforms of the SN74AHC240**

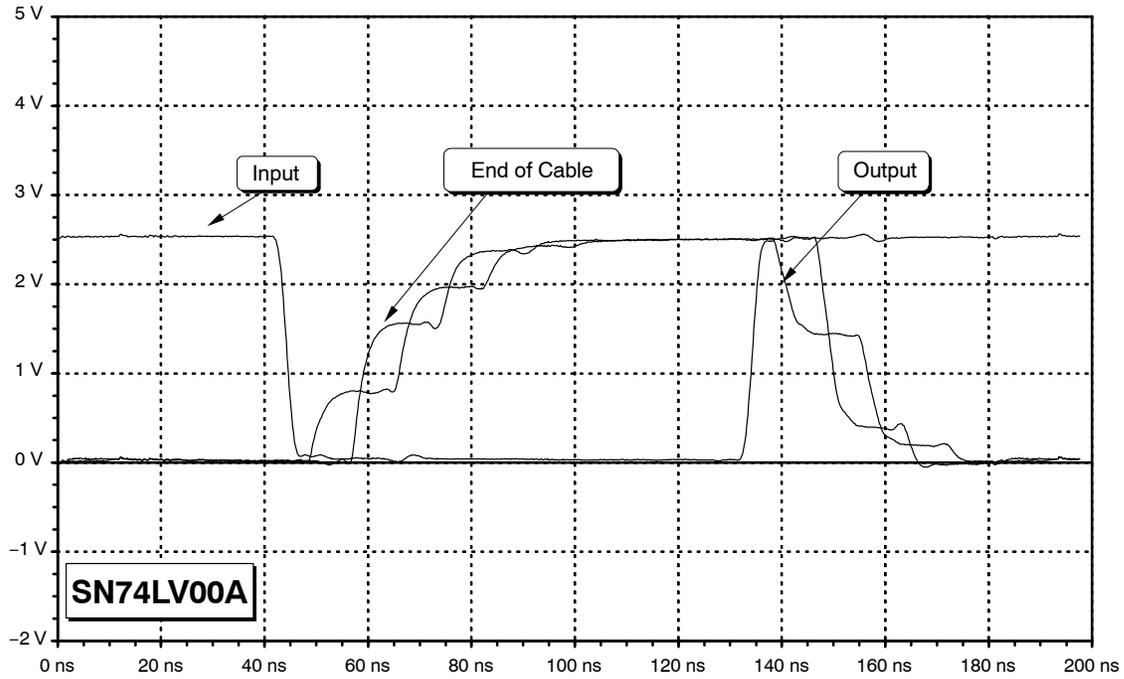


Figure 20. Output Waveforms of the SN74LV00A

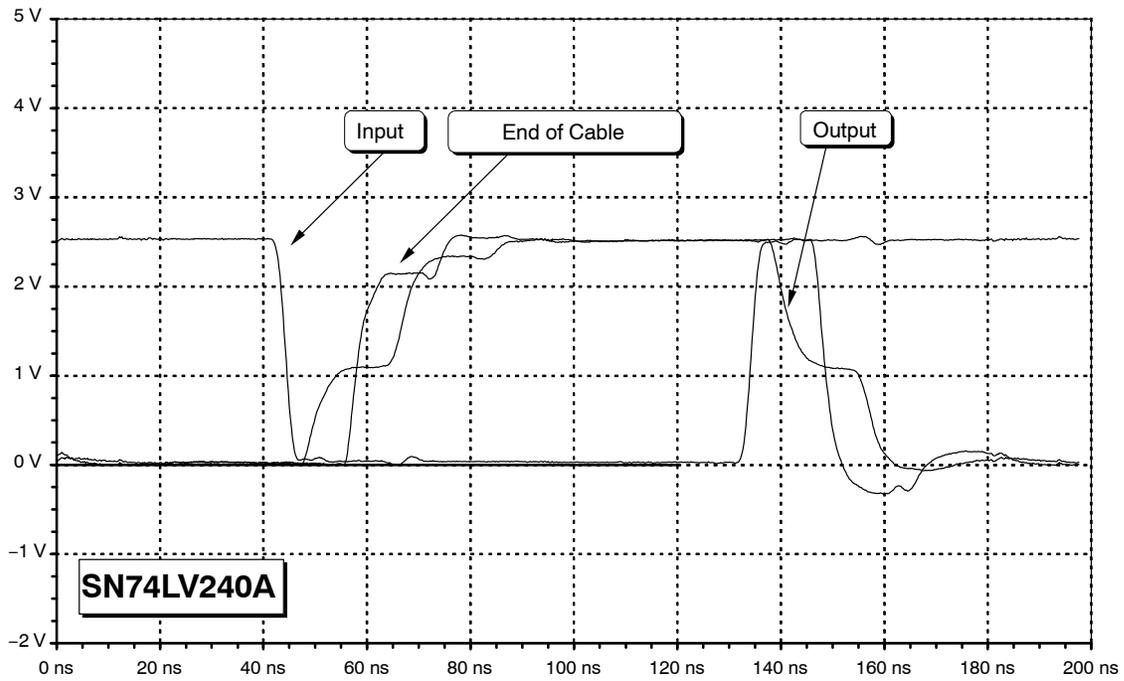


Figure 21. Output Waveforms of the SN74LV240A

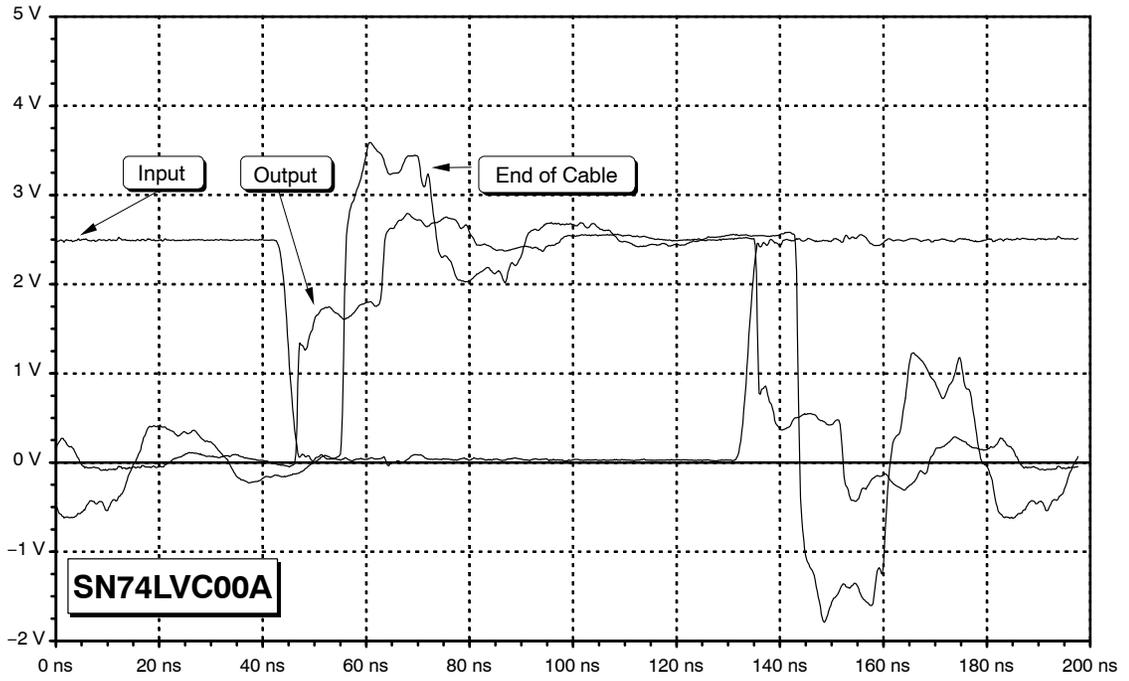


Figure 22. Output Waveforms of the SN74LVC00A

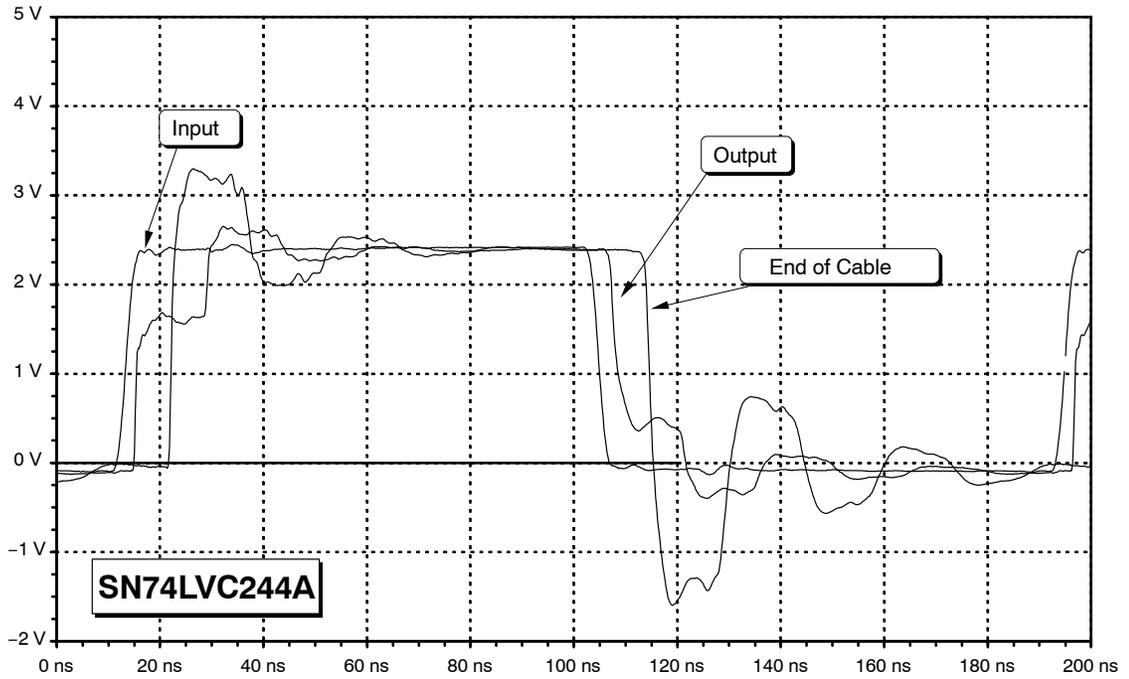


Figure 23. Output Waveforms of the SN74LVC244A

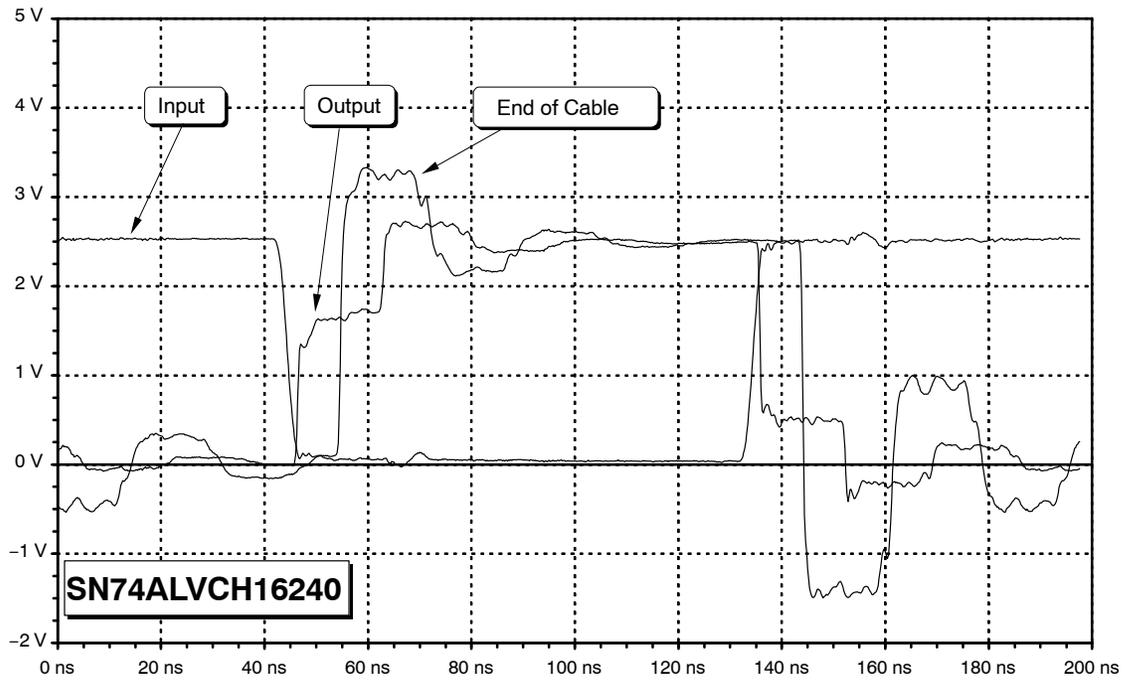


Figure 24. Output Waveforms of the SN74ALVCH16240

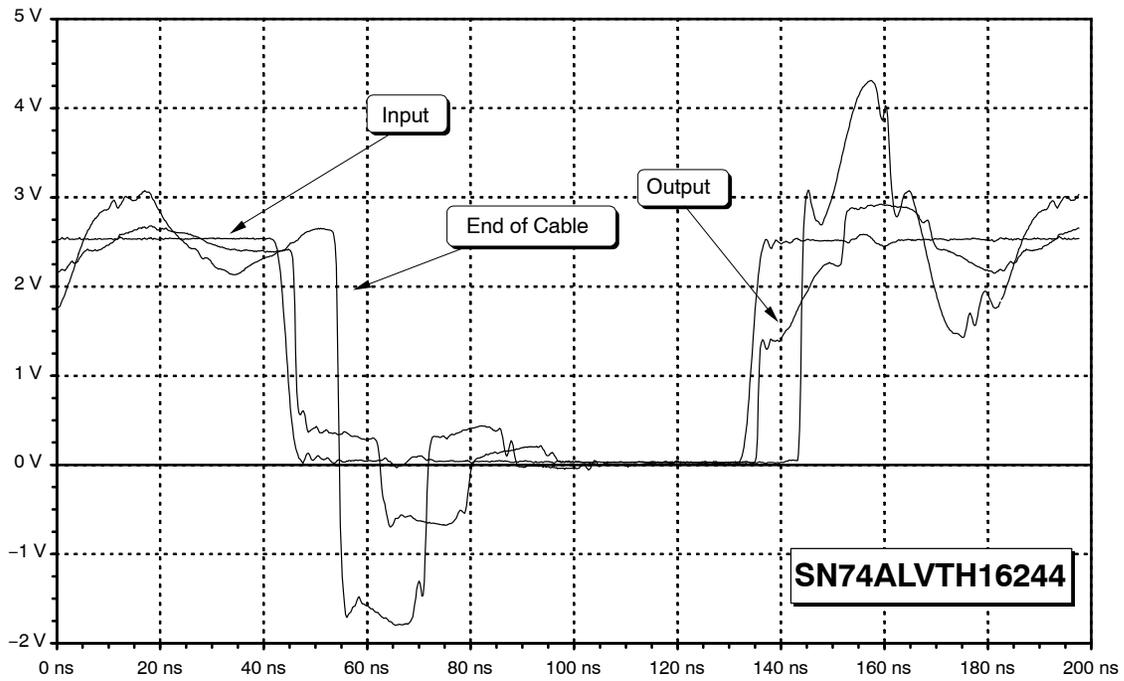


Figure 25. Output Waveforms of the SN74ALVTH16244

## 6 Abbreviations and Glossary

SN74ABT	Advanced BiCMOS Technology devices
SN74AC	Advanced CMOS devices
SN74AHC	Advanced High-speed CMOS devices
SN74ALS	Advanced Low-power Schottky devices
SN74AS	Advanced Schottky devices
SN74ALVC	Advanced Low-Voltage CMOS devices
SN74ALVT	Advanced Low-Voltage Technology devices
SN74AVC	Advanced Very low-voltage CMOS devices
Auto3-state	During active-high state at the output, devices with auto3-state tolerate a higher voltage level at the outputs (also called overvoltage protection).
SN74BCT	BiCMOS Technology devices
BiCMOS	Combination of bipolar and CMOS process (CMOS input structure and bipolar output structure)
Bus hold	Input circuitry that holds the last valid logic state applied to it before entering a nondefined state on the bus, until a new valid logic state is driven actively.
3-/5-V tolerance	Logic devices with 5-V (3.3-V) tolerance tolerate 5-V (3.3-V) CMOS logic levels at their input and output in the high-impedance state while supplied with 2.5-V.
GND	Ground
I/O	Input/Output
SN74LS	Low-power Schottky devices
SN74LV	Low-Voltage CMOS devices, originally designed for $V_{CC} = 3.3\text{-V}$ , also specified at 5 V
SN74LVC	Low-Voltage CMOS devices
SN74LVT	Low-Voltage Technology devices
Overvoltage protection	See auto3-state and 3-/5-V tolerance
$R_L$	Load resistor
SN74S	Schottky devices

Series resistor    A resistor in the output stage of a bus driver. With this resistor, the effective output impedance of the driver is shifted to about 50  $\Omega$ , making an optimum line adaptation.

SPICE            Simulation Program with Integrated Circuit Emphasis

TTL-level       Transistor-Transistor Logic level

V<sub>CC</sub>            Supply voltage

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<http://www.ti.com/sc>

TI Distributors

<http://www.ti.com/sc/docs/distmenu.htm>

TI Logic Home Page

<http://www.ti.com/sc/docs/asl/home.htm>

TI Logic Literature

<http://www.ti.com/sc/docs/asl/lit/lit.htm>

TI Product Information and Document Search

<http://www.ti.com/sc/docs/msp/download.htm>

## 8 Acknowledgment

The author of this application report is Johannes Huchzermeier.



# ***Benefits and Issues on Migration of 5-V and 3.3-V Logic to Lower-Voltage Supplies***

SDAA011A  
September 1999



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## Abstract

In the last few years, the trend toward reducing supply voltage ( $V_{CC}$ ) has continued, as reflected in an additional specification of 2.5-V  $V_{CC}$  for the AVC, ALVT, ALVC, LVC, LV, and the CBTLV families.

In this application report, the different logic levels at  $V_{CC}$  of 5 V, 3.3 V, 2.5 V, and 1.8 V are compared. Within the report, the possibilities for migration from 5-V logic and 3.3-V logic families to 2.5-V  $V_{CC}$  are shown, and the implications of the reduced supply voltage are discussed. Data is provided that shows the influence of reduced  $V_{CC}$  on power consumption, drive capability, and propagation delay time for the logic families.

Further, the requirements for an overvoltage tolerance (5-V/3.3-V input and output) is discussed, as well as interfacing opportunities in a mixed-mode environment in which two different supply voltages are used.

This application report is intended to be used as a designer's guide to component selection and usage at supply voltages below 3.3-V. The data in this document is typical data taken under typical laboratory conditions (25°C) and 2.5-V or 1.8-V, except where otherwise noted. The data is intended as a design guideline only.

## Background

The use of 5-V  $V_{CC}$  has long been the standard for both core and memory logic. However, with the increase in complexity and the functionality of application-specific integrated circuits (ASICs), central processing units (CPUs), microprocessors, and digital signal processors (DSPs), it has become necessary to reduce the structure size of these elements.

Using modern manufacturing processes that produce smaller structures, the thickness of the gate oxide of each single transistor has become more sensitive to electrostatic field strength. Because the field strength is proportional to the supply voltage, the direct result is that supply voltage must be reduced for a reliable operation.

In other words, making electronic devices more complex, without enlarging the overall size of the chip area, requires reducing the structure size, which also requires reducing  $V_{CC}$ .

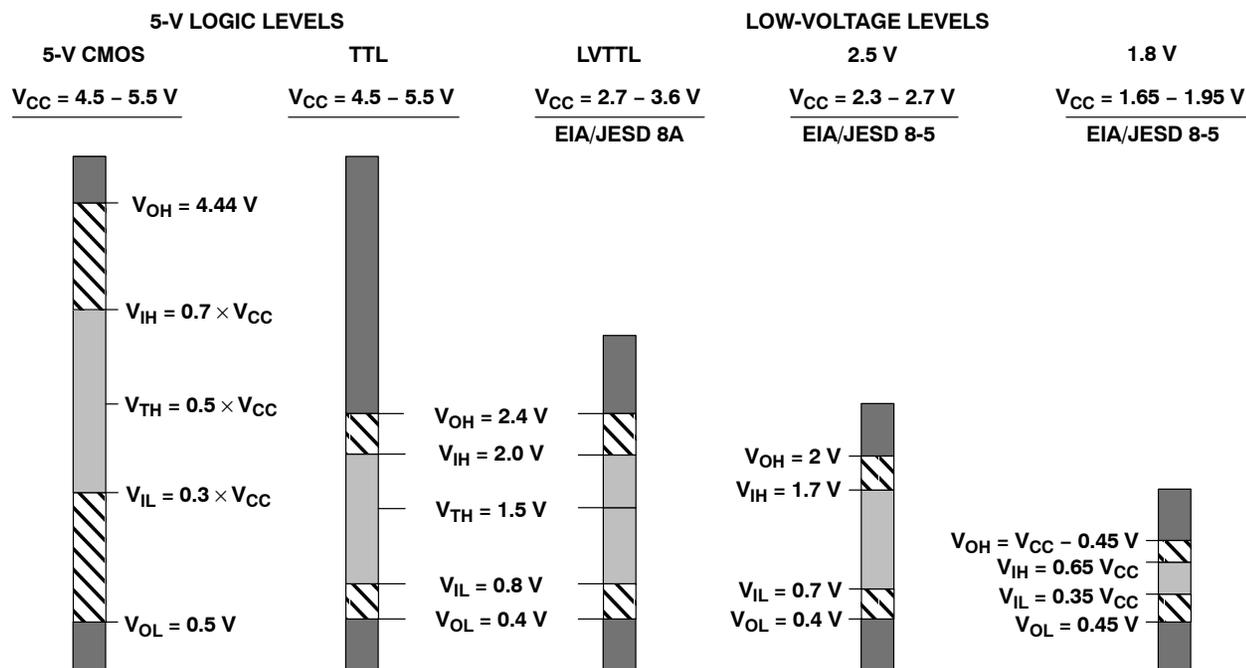
The limit for reliable operation at less than 5-V  $V_{CC}$  is reached at a structure size of 0.6 micron, and the use of a 0.35-micron manufacturing process requires 2.5-V  $V_{CC}$  for proper operation.

Moreover, power consumption always is a concern for new system designs. A reduction in supply voltage produces an exponential decrease in power consumption; therefore, the trend is to reduce power-supply voltage. To meet these requirements, many modern logic families are specified at different voltage nodes, which enables designers to use them at 3.3-V  $V_{CC}$  and at 2.5-V  $V_{CC}$ .

This application report investigates the possibilities for migration of 5-V and 3.3-V logic to 2.5-V logic, and discusses the implications.

## Input- and Output-Level Specifications at Different Supply Voltages

For each  $V_{CC}$  a standard is defined, with commonly agreed-upon levels of input and output levels. Figure 1 shows the appropriate switching levels for 5-V, 3.3-V, and 2.5-V that have passed the JEDEC committee. Additionally, the 1.8-V level specification, as given in the data sheets of the SN74LVCxxxA and SN74AVCxxx devices, is shown.



**Figure 1. 5-V, 3.3-V, and 2.5-V Switching-Level Comparison**

Table 1 contains additional information regarding the various logic families, including manufacturing process, the optimal power supply, and the  $V_{CC}$  at which the logic families are functional.

The AHC family is included in this overview. Although the AHC family was targeted for the 5-V  $V_{CC}$ , after its market introduction, this family also was specified for operation at 3.3 V  $V_{CC}$ .

The low-voltage logic families (SN74LVxxxA, SN74LVCxxxA, SN74ALVCHxxx) also have been characterized at 2.5-V  $V_{CC}$ , to meet the trend of reduced supply voltages.

The AVC family is the optimal solution for 2.5-V  $V_{CC}$ , and also is fully characterized at 1.8-V and 3.3-V  $V_{CC}$ .

The data sheets for the LVC family show switching characteristics at 1.8-V  $V_{CC}$ .

**Table 1. Operational Supply Voltages of Different Logic Families**

LOGIC FAMILY	MANUFACTURING PROCESS	OPTIMAL POWER-SUPPLY LEVEL	OPERATIONAL AT $V_{CC} = 3.3 \text{ V}$	OPERATIONAL AT $V_{CC} = 2.5 \text{ V}$	OPERATIONAL AT $V_{CC} = 1.8 \text{ V}$
AHC	CMOS	5 V	Fully specified	Yes, down to 2 V	Not specified
ALVC	CMOS	3.3 V	Fully specified	Fully specified	Planned
ALVT	BiCMOS	3.3 V	Fully specified	Fully specified	Not specified
AVC	CMOS	2.5 V	Fully specified	Fully specified	Fully specified
CBTLV	CMOS	3.3 V	Fully specified	Fully specified	Not specified
LVxxxA	CMOS	3.3 V	Fully specified	Fully specified	Not specified
LVCxxxA	CMOS	3.3 V	Fully specified	Fully specified	Fully specified

The CMOS process indicates that both the input and the output structures comprise pure CMOS circuitry, whereas, the BiCMOS process indicates that both bipolar and CMOS transistors are implemented in the data or control input circuitry and/or output circuitry.

## Power-Consumption Considerations

With the reduction of the supply voltage, a proportional power saving results. This section provides comparisons of the power consumption of logic families at different voltage levels.

The total power consumption of an integrated circuit is the sum of quiescent power dissipation, or static power consumption, (see Equation 1) and dynamic power consumption (see Equation 2). Dynamic power consumption consists of two parts:

- The average power dissipation caused by current spikes (see Equation 3). This is the power consumption that is caused by the internal circuitry of the logic device.
- The power dissipation caused by driving an externally connected load (see Equation 4).

$$\text{Static power consumption:} \quad P_{\text{STAT}} = V_{\text{CC}} \times I_{\text{CC}} \quad (1)$$

$$\text{Dynamic power consumption:} \quad P_{\text{DYN}} = P_{\text{T}} + P_{\text{L}} \quad (2)$$

$$\text{Transient power consumption:} \quad P_{\text{T}} = V_{\text{CC}}^2 \times C_{\text{PD}} \times f_{\text{I}} \times N_{\text{SW}} \quad (3)$$

$$\text{Capacitive-load power consumption:} \quad P_{\text{T}} = V_{\text{CC}}^2 \times C_{\text{L}} \times f_{\text{OI}} \times N_{\text{SW}} \quad (4)$$

Where:

- $V_{\text{CC}}$  = supply voltage
- $C_{\text{L}}$  = load capacitance
- $C_{\text{PD}}$  = dynamic power-dissipation capacitance
- $f_{\text{I}}$  = input-signal frequency
- $f_{\text{O}}$  = output-signal frequency
- $I_{\text{CC}}$  = supply current
- $N_{\text{SW}}$  = number of outputs switching

A reduction of  $V_{\text{CC}}$  directly results in a power savings. The relation in the static power consumption is linear (assuming that static  $I_{\text{CC}}$  is independent of  $V_{\text{CC}}$ ), while the term  $V_{\text{CC}}$  is included as a squared factor within the dynamic power consumption formulas (see Equation 3 and Equation 4).

Using equations 1 through 4, a 3.3-V  $V_{\text{CC}}$  system theoretically saves between 33% for the static considerations (see Equation 1) and up to 57% for the dynamic case, when compared to 5-V systems. With a 2.5-V  $V_{\text{CC}}$ , the system's power consumption decreases to between 50% (static) and 75% (dynamic), respectively, compared to the 5-V system.

The data sheets of the logic families do not show all information about power consumption. One parameter that is shown for power consumption is the supply current ( $I_{\text{CC}}$ ). However, in some cases, this parameter is given at only one supply voltage. The parameter  $I_{\text{CC}}$  is given in the table of electrical characteristics (recommended operation conditions) shown for the SN74LV245A in Table 2.

**Table 2. LV245A Supply Current Parameter ( $I_{\text{CC}}$ )**

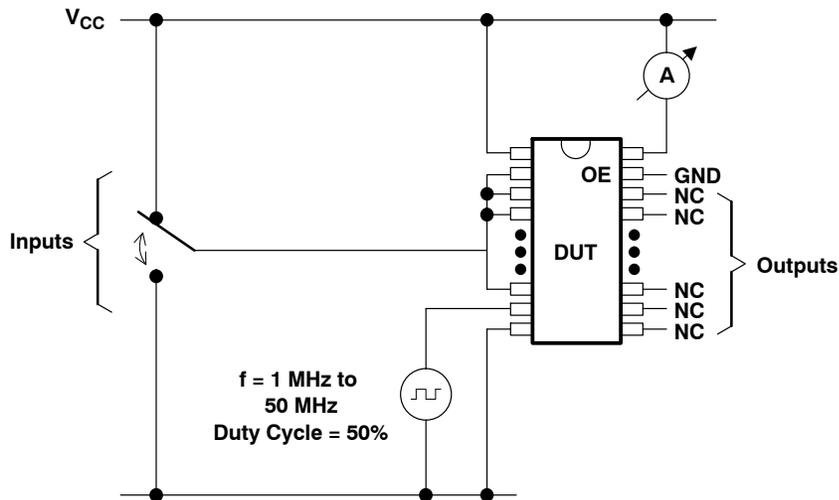
TEST CONDITIONS		$V_{\text{CC}}$	MIN	MAX	UNIT
$I_{\text{CC}}$	$V_{\text{I}} = V_{\text{CC}}$ or GND, $I_{\text{O}} = 0$	5.5 V		20	$\mu\text{A}$

However, as previously mentioned, this parameter indicates the power consumption for static states only, either for the case that the input is statically set to  $V_{\text{CC}}$  or set to GND.

Another parameter that indicates the power consumption indirectly is the power-dissipation capacitance ( $C_{pd}$ ) that is given, for example, for the AVC family at three supply voltages. With this parameter, the transient power consumption can be calculated using Equation 3.

For a more comprehensive overview of Texas Instruments logic families, measurements of the dynamic power consumption at different supply voltages have been taken. The logic families investigated were AHC, ALVT, ALVC, LVC, LV, and AVC.

The measurement setup is shown in Figure 2. For the measurement of dynamic power consumption, all but one input of the device under test (DUT) were set to a static high-state or low-state logic value. One input is connected to a signal generator. The applied signal is a square wave with a duty cycle of 50% and switches between the supply voltage of the DUT and GND. The frequency of the signal was varied between 1 MHz and 50 MHz and the supply current ( $I_{CC}$ ) was measured within that range. The outputs of the DUT are not connected, so that only the device's internal power consumption, not the external load, is measured.



**Figure 2. Power Consumption vs Frequency Measurement Setup**

Figures 3 through 5 show the measurement results for 3.3-V, 2.5-V, and 1.8-V  $V_{CC}$ . The LVC and the AVC families have a specification for the 1.8-V  $V_{CC}$ , but the other logic families do not. However, the test samples of all investigated logic families showed full functionality at 1.8-V  $V_{CC}$ . For comparison, the power consumption has been measured at 1.8-V also.

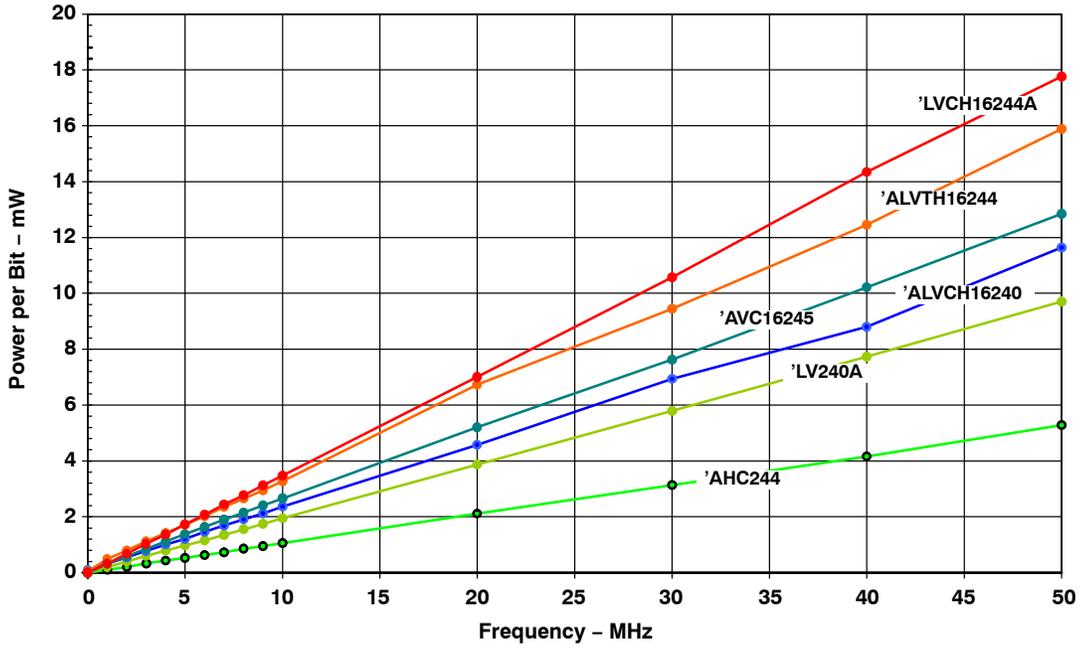


Figure 3. Power Consumption at 3.3-V V<sub>CC</sub>

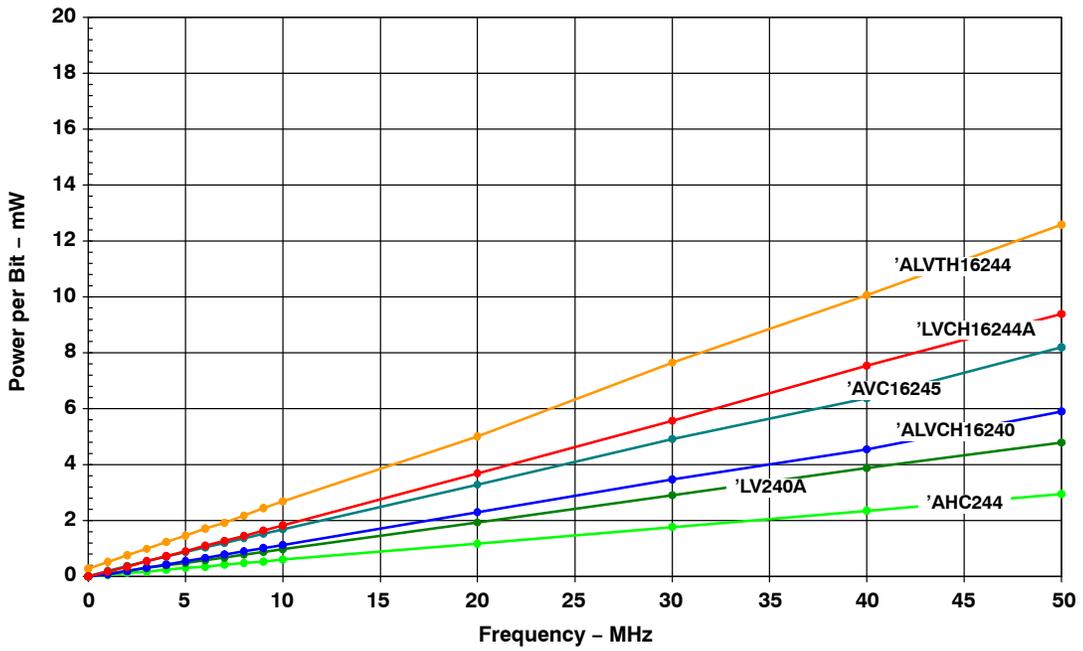


Figure 4. Power Consumption at 2.5-V V<sub>CC</sub>

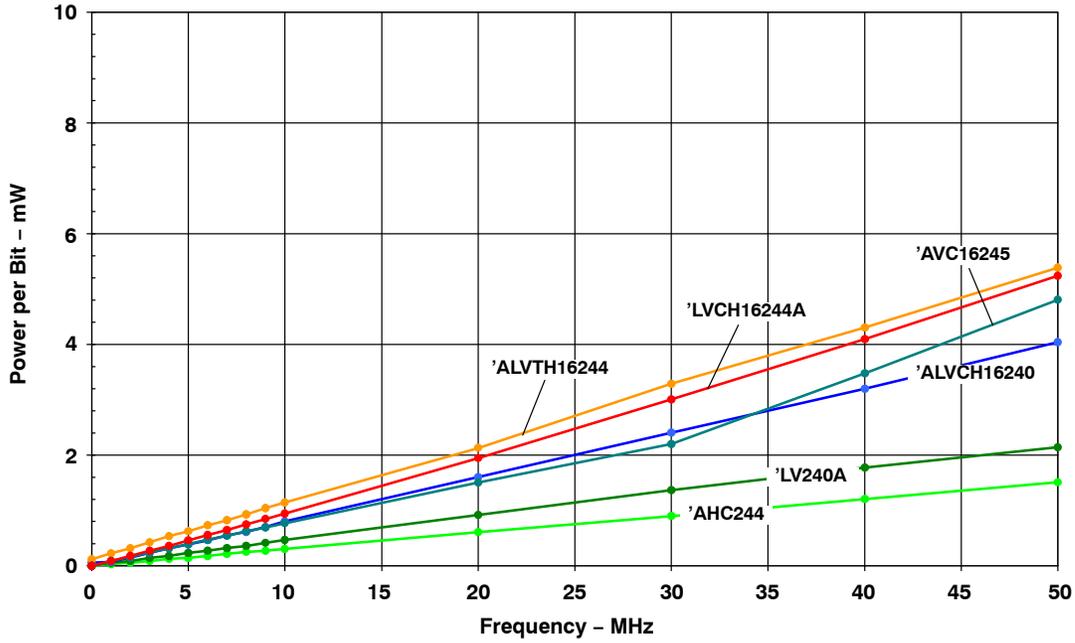


Figure 5. Power Consumption at 1.8-V V<sub>CC</sub>

Figure 6 shows the relative power consumption of the tested logic devices compared to 3.3-V V<sub>CC</sub>.

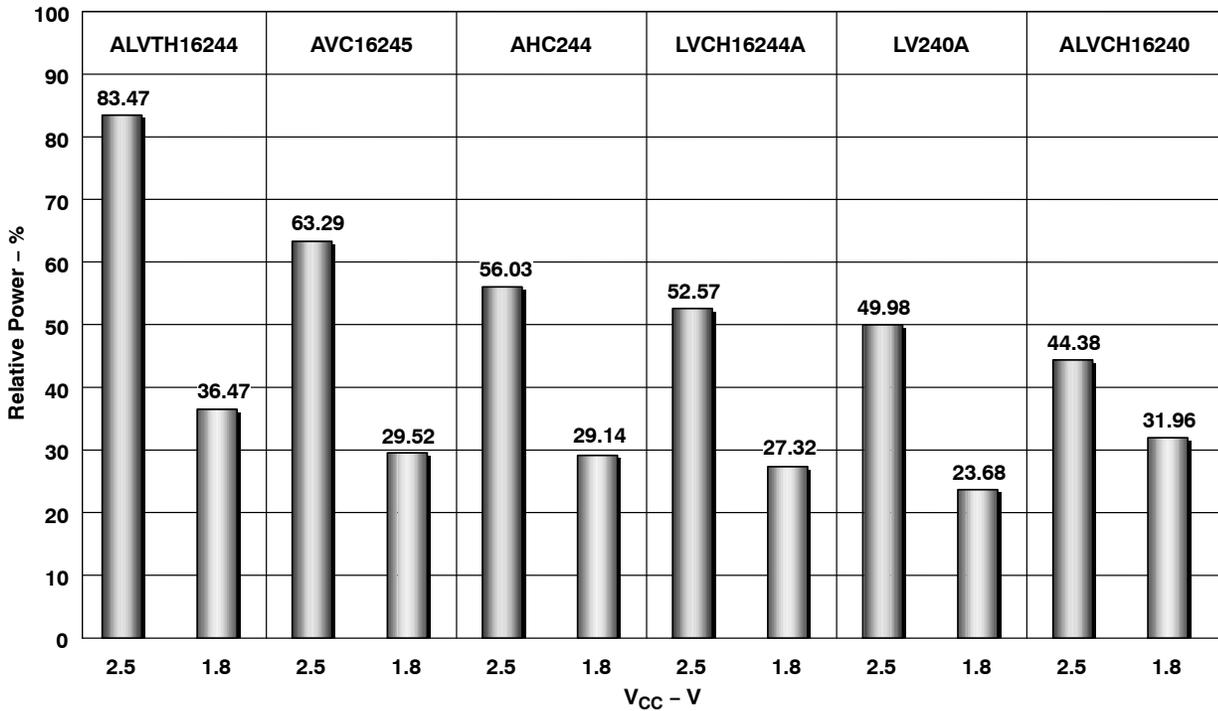


Figure 6. Relative Power Consumption at 2.5-V and 1.8-V V<sub>CC</sub> Compared to 3.3-V V<sub>CC</sub>

## Output Characteristics at Less Than 3.3-V $V_{CC}$

### Standard Logic Families

With the reduction of the supply voltage there is also a reduction of the drive capability of the logic circuit.

The output stage of a logic circuit in the high state behaves like a voltage source with an open-circuit voltage of  $V_{CC}$  for CMOS logic, and low-voltage BiCMOS logic, respectively.

In the low state, for positive voltages, the output resistance is based on the internal resistance of the conducting transistor, i.e., collector-emitter for BiCMOS technologies and drain-source resistance for CMOS technologies.

Negative voltage peaks at the inputs are limited by protection diodes. Output stages of the CMOS logic family SN74AHCxxx also have output protection diodes that connect output stages and  $V_{CC}$ . This diode limits the positive output voltage to  $V_{CC} + 0.5$  V.

The available output current depends on  $V_{CC}$ , which determines the gate source voltage of the output transistors. At a supply voltage below about 1 V (less than the turn-on voltage of the MOS transistors) the output stays in the off state. With increasing supply voltage, output current increases also.

The LVC family has the dc characteristics shown in Table 3. The drive capability of this device decreases with decreasing supply voltage.

**Table 3. LVCH245A Output Drive Parameters ( $V_{OH}$  and  $V_{OL}$ )**

PARAMETER	TEST CONDITIONS	$V_{CC}$	MIN	MAX	UNIT
$V_{OH}$	$I_{OH} = -100 \mu A$	1.65 to 3.6 V	$V_{CC} - 0.2$		V
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2		
	$I_{OH} = -8 \text{ mA}$	2.30 V	1.7		
	$I_{OH} = -12 \text{ mA}$	2.70 V	2.2		
	$I_{OH} = -12 \text{ mA}$	3.00 V	2.4		
	$I_{OH} = -24 \text{ mA}$	3.00 V	2.2		
$V_{OL}$	$I_{OL} = 100 \mu A$	1.65 to 3.6 V		0.2	V
	$I_{OL} = 4 \text{ mA}$	1.65 V		0.45	
	$I_{OL} = 8 \text{ mA}$	2.30 V		0.7	
	$I_{OL} = 12 \text{ mA}$	2.70 V		0.4	
	$I_{OL} = 24 \text{ mA}$	3.00 V		0.55	

Figure 7 illustrates values of  $I_{OL}$  and  $I_{OH}$  and the corresponding values of  $V_{OL}$  and  $V_{OH}$  for a typical LVC device. The output characteristics of the LVC device were taken at 3.3-V, 2.5-V, and 1.8-V  $V_{CC}$ . The drive capability decreases significantly with reduced supply voltage. The same trend can be observed for all logic families.

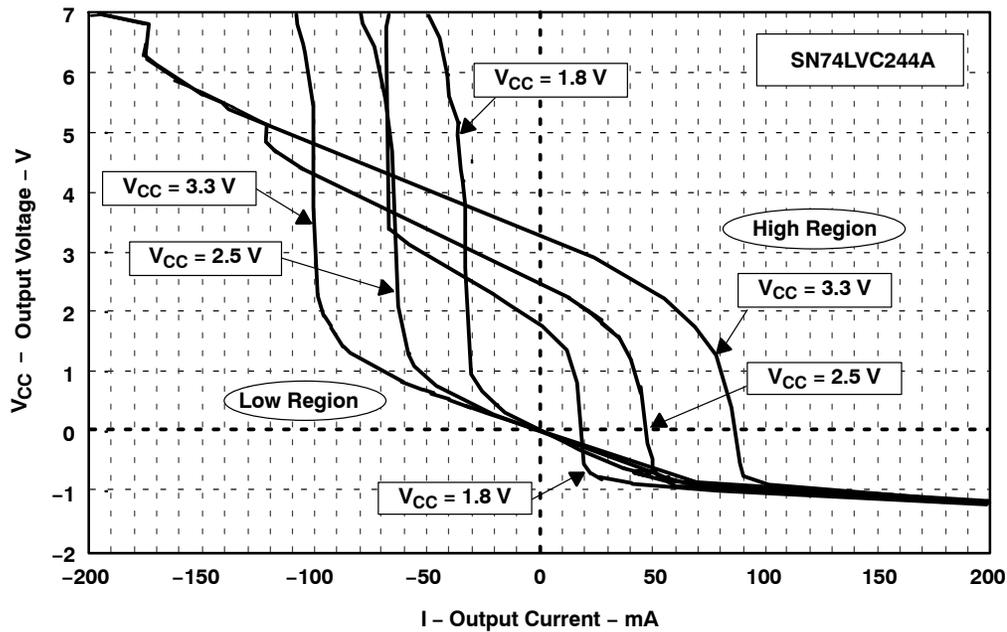


Figure 7. Output Characteristics of the LVC244 at Different Supply Voltages

Table 4 shows a comparison of the output-current specifications of the logic families discussed in this report. All families have full 3.3-V and 2.5-V specifications. LV and the AHC have additional 5.5-V drive specifications. The AVC and LVC families show full specifications regarding the high-level and low-level output voltage and output current in the data sheets at  $V_{CC} = 1.8\text{ V}$ .

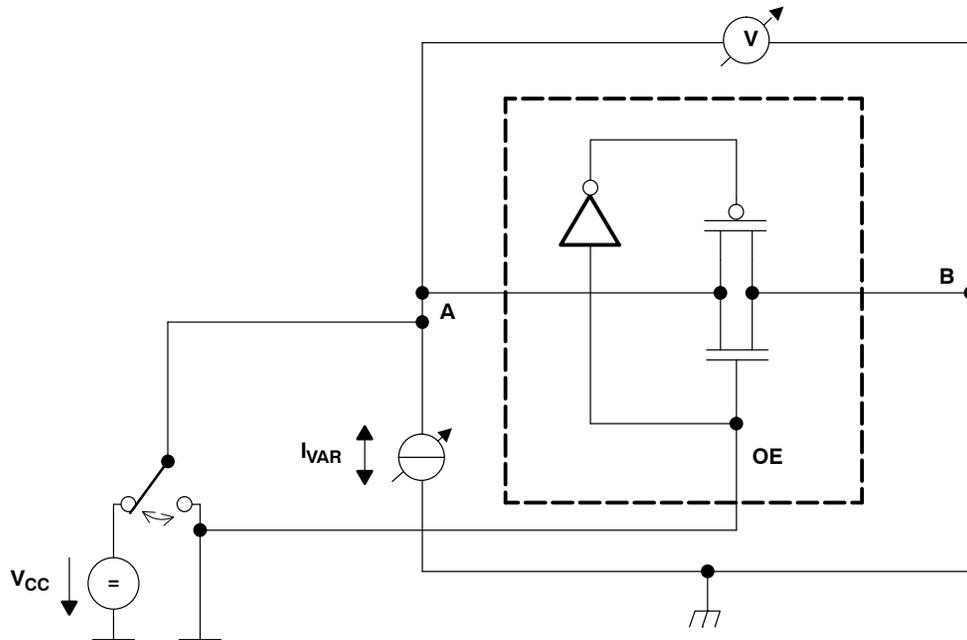
**Table 4. Output-Current Specifications as Shown in the Data Sheet**

LOGIC FAMILY	$V_{CC}$	MINIMUM		MAXIMUM		SPECIFIED IN DATA SHEET
		$V_{OH}$	$I_{OH}$	$V_{OL}$	$I_{OL}$	
AHC	2 V	1.9 V	-50 $\mu\text{A}$	0.1 V	50 $\mu\text{A}$	No switching characteristic
	2.30 V					N/A
	3.00 V	2.48 V	-4 mA	0.44 V	4 mA	Yes
	4.5 V	3.8 V	-8 mA	0.44 V	8 mA	5-V specification
LV	2 V-5.5 V	$V_{CC}-0.1\text{ V}$	-50 $\mu\text{A}$	0.1 V	50 $\mu\text{A}$	Yes
	2.30 V	2 V	-2 mA	0.40 V	2 mA	Yes
	3.00 V	2.48 V	-8 mA	0.44 V	8 mA	Yes
	4.5 V	3.8 V	-16 mA	0.55 V	16 mA	5-V specification
LVC	1.65	1.2 V	-4 mA	0.45 V	4 mA	Yes
	2.30 V	1.7 V	-8 mA	0.70 V	8 mA	Yes
	2.70 V	2.2 V	-12 mA	0.40 V	12 mA	Yes
	3.00 V	2.2 V	-24 mA	0.55 V	24 mA	Yes
ALVC	1.65					Planned
	2.30 V	2 V	-6 mA	0.40 V	6 mA	Yes
	2.70 V	2.2 V	-12 mA	0.40 V	12 mA	Yes
	3.00 V	2 V	-24 mA	0.55 V	24 mA	Yes
ALVT	1.65					
	2.30 V	1.8 V	-8 mA	0.50 V	-24 mA	Yes
	3.00 V	2 V	-32 mA	0.55 V	-64 mA	Yes
AVC	1.65	1.2 V	-4mA	0.45 V	4 mA	Yes
	2.30 V	1.75 V	-8 mA	0.55 V	8 mA	Yes
	3.00 V	2.3 V	-12 mA	0.7 V	12 mA	Yes

## Crossbar Technology (CBT)/Crossbar Technology Low Voltage (CBTLV)

The CBT families (SN74CBTxxx and SN74CBTLVxxx) are FET switches that do not have their own drive capability. They are a good solution in systems that require bus isolation and bus exchanging. The impedance of CBT devices varies with the amount of current flowing from the drain to the source. The data sheets reflect this with the parameter  $r_{on}$ .

Figure 8 shows the  $r_{on}$  measurement setup. Measurements were taken at 3.3-V, 2.5-V, and 1.8-V  $V_{CC}$  to show the influence of  $V_{CC}$  on  $r_{on}$  of the CBTLV3245A. The output was enabled by connection to GND.



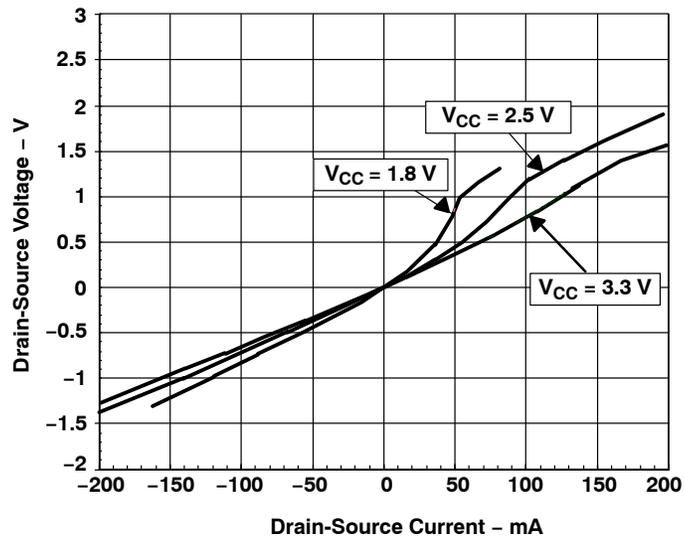
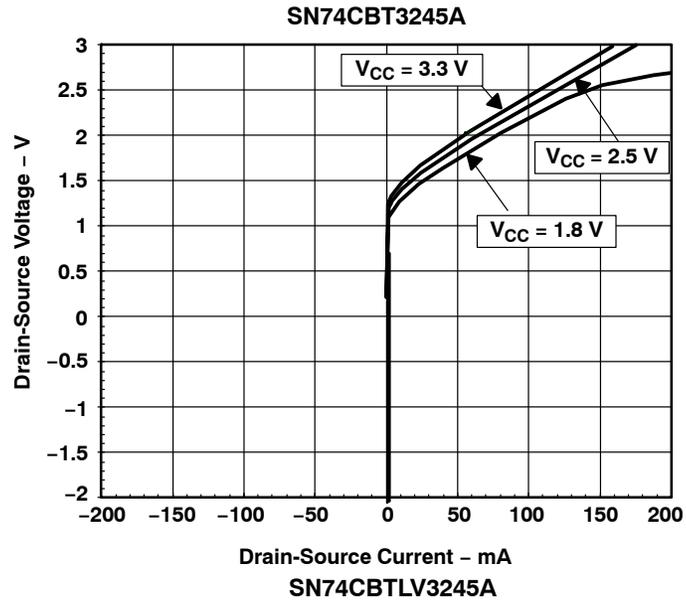
**Figure 8. Setup for Measuring  $r_{on}$  of the CBTLV3245A**

Input A was connected to  $V_{CC}$  to measure  $r_{on}$  in the high state. To measure  $r_{on}$  in the low state, input A was connected to GND of the supply voltage.

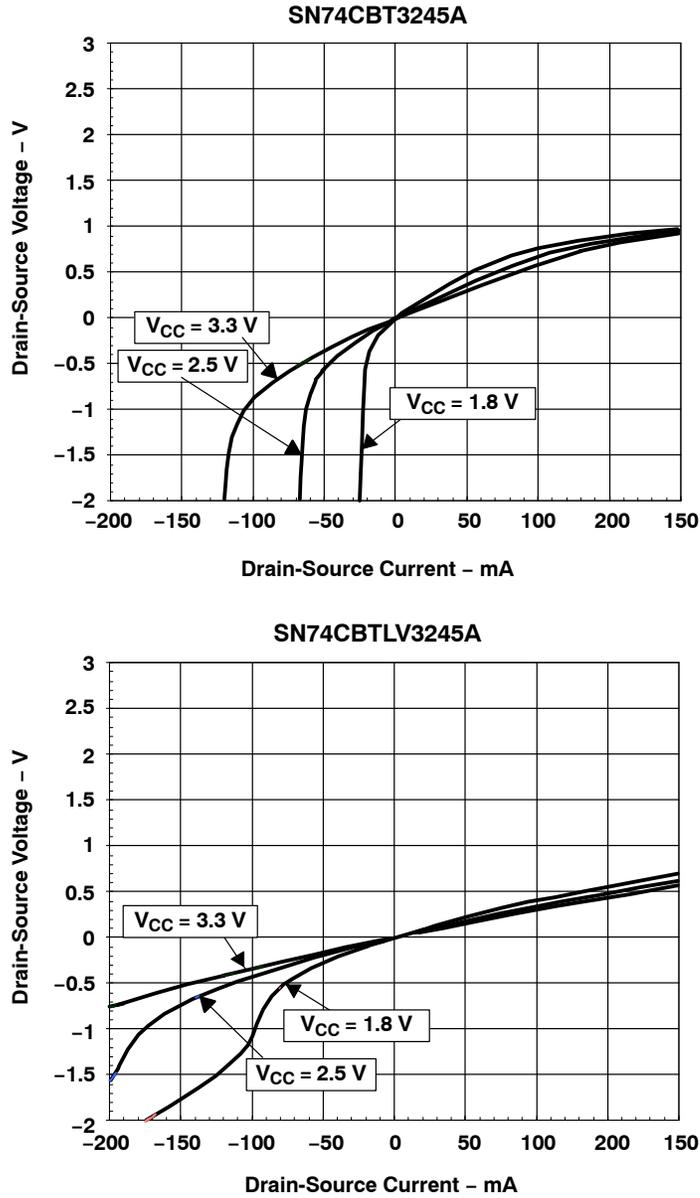
Also, input A was connected to a variable-current source that was swept from  $-200$  mA to  $200$  mA. The voltage was measured over the drain-source of the CBTLV3245A between point A and point B.

Figures 9 and 10 show the measurement results. The linearity of  $r_{on}$  of the CBTLV3245A is best at 5.5-V  $V_{CC}$  with  $r_{on}$  (high state) of  $10\ \Omega$  to  $20\ \Omega$  and  $r_{on}$  (low state) of  $4\ \Omega$  to  $7\ \Omega$ .

The linearity of  $r_{on}$  for the CBTLV3245A is best at 3.3-V  $V_{CC}$  with  $r_{on}$  (high state) of  $6\ \Omega$  to  $10\ \Omega$  and  $r_{on}$  (low state) of  $2\ \Omega$  to  $5\ \Omega$ .



**Figure 9. High-State  $r_{on}$  of CBT3245A and CBTLV3245A at Different Supply Voltages**



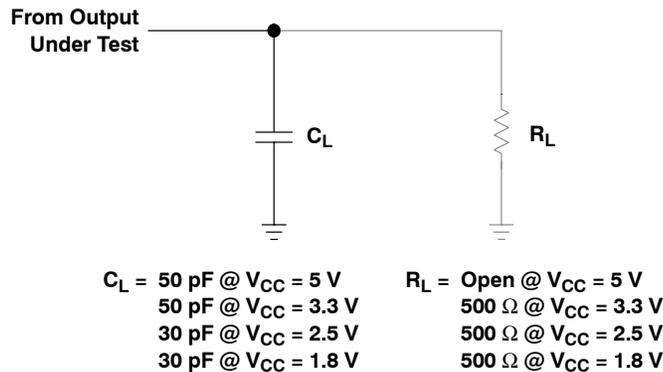
**Figure 10. Low-State  $r_{on}$  of CBT3245A and CBTLV3245A at Different Supply Voltages**

The linearity of  $r_{on}$  (drain-source) of the FET degrades with decreasing supply voltage. The CBT device conducts only if the drain-source voltage is more than approximately 1 V. The CBTLV devices are operational below this voltage because the P-channel FET is switched in parallel with the n-channel transistor and exhibits transmission-gate behavior. The  $r_{on}$  (high state) varies, depending on the conducted current and the supply voltage. The resistance values can be derived from Figures 9 and 10.

## Propagation Delay Time at Different Supply Voltages

Decreasing a system's supply voltage from 5 V to 3.3 V, or lower, slows its speed (increases propagation time). This section contains a comprehensive collection of measurements that shows this effect. The data sheets show that the measurement setup for the propagation delay depends on the supply voltage of the device under test (DUT).

However, not only is the supply voltage reduced, but the measurement setup for the propagation delay time is different. Figure 11 shows the test condition for the measurements of the high-to-low and low-to-high propagation delay times at 5-V, 3.3-V, 2.5-V, and 1.8-V  $V_{CC}$ .

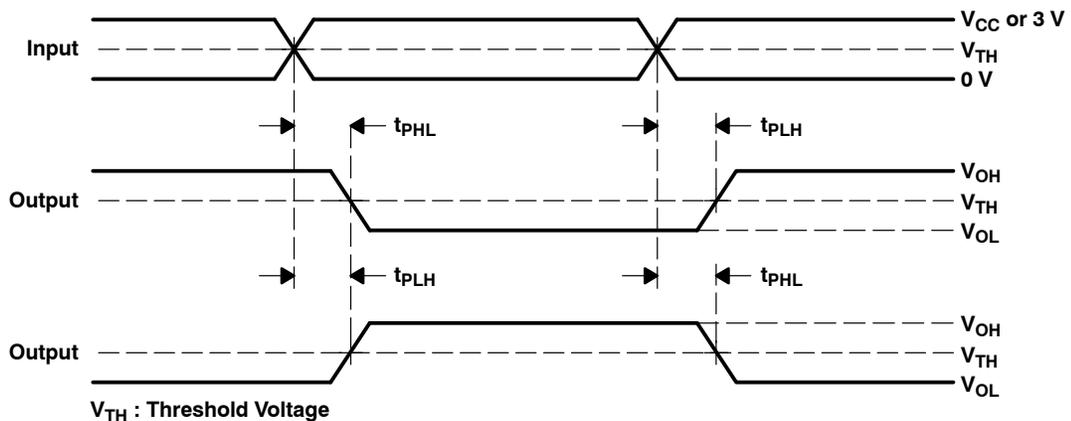


**Figure 11. Test Conditions for Measuring Propagation Delay Time**

While at 5-V  $V_{CC}$ , a 50-pF capacitor is the only load to the device's output, at 3.3-V  $V_{CC}$  a 500- $\Omega$  resistor ( $R_L$ ) is in parallel with the capacitor for the measurement. At 2.5-V  $V_{CC}$  the value of the capacitor is reduced to 30 pF, and the value of the resistor in parallel is 500  $\Omega$ .

Figure 12 shows voltage waveforms. All input pulses are supplied by a generator having the following characteristics: signal frequency = 1 MHz,  $t_p, t_f \leq 2.5 \text{ ns}$ . One output is measured at a time, with one transition per measurement.

For ALVTH at 3.3-V  $V_{CC}$ , the input signal was switched between 3.0 V and 0 V. In this case, the threshold voltage is 1.5 V. For all other measurements the input signal was switched between  $V_{CC}$  and GND and the threshold voltage chosen was  $V_{CC}/2$ .



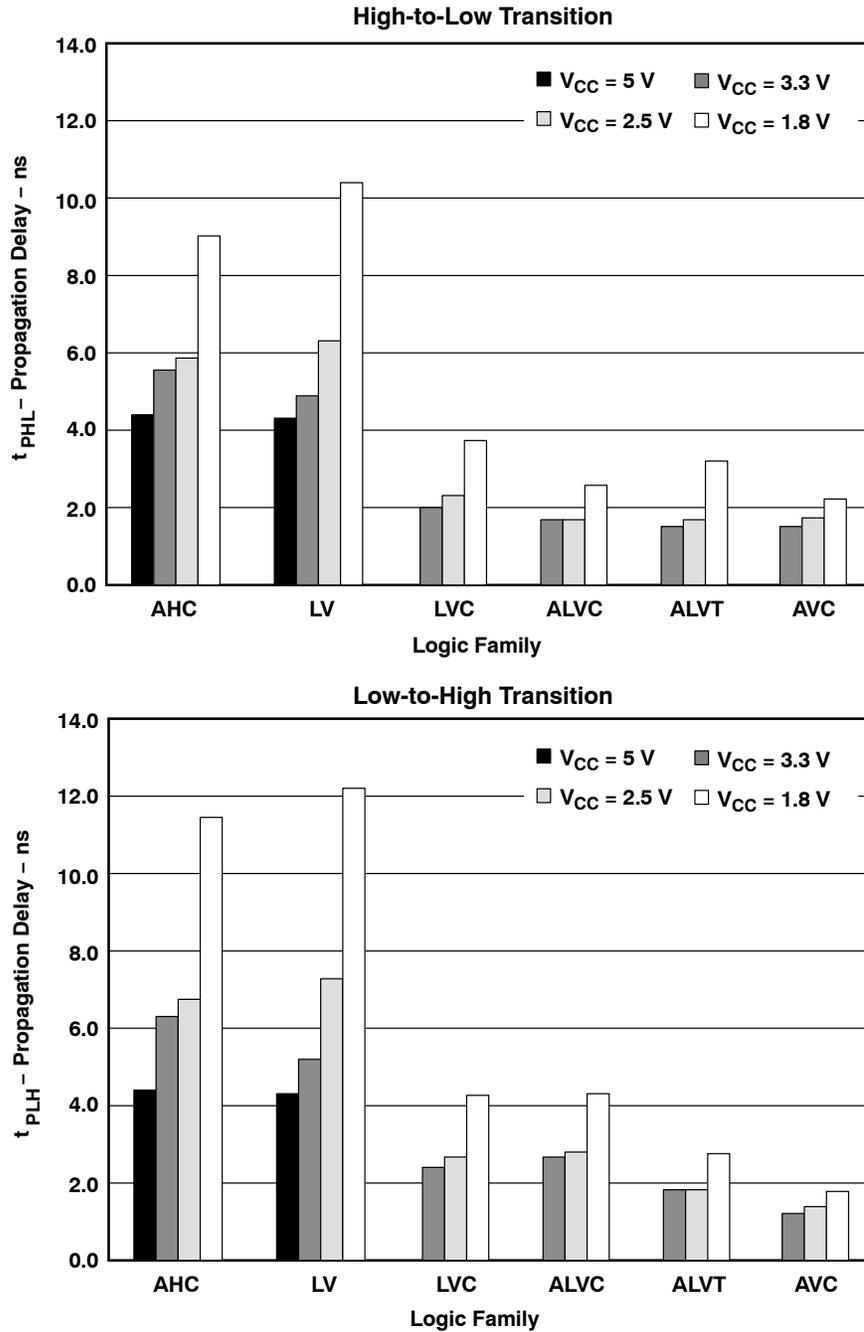
**Figure 12. Propagation Delay Times of Inverting and Noninverting Outputs**

Table 5 shows the results of the propagation delay time measurements. In Figure 13, the results are shown graphically for easier comparison.

**Table 5. Typical Propagation Delays at Different Supply Voltages**

SUPPLY VOLTAGE	LOAD CONDITION	t <sub>pd</sub>	AHC244	LV240A	LVCH16244A	ALVCH16244	ALVTH16244	AVC16244	UNIT
5 V	C <sub>L</sub> = 50 pF	t <sub>PLH</sub>	4.4	4.3	N/A	N/A	N/A	N/A	ns
		t <sub>PHL</sub>	4.4	4.3	N/A	N/A	N/A	N/A	ns
3.3 V	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω	t <sub>PLH</sub>	6.2	5.2	2.4	2.6	1.9	1.2 <sup>†</sup>	ns
		t <sub>PHL</sub>	5.5	4.9	2.0	1.7	1.5	1.6 <sup>†</sup>	ns
2.5 V	C <sub>L</sub> = 30 pF, R <sub>L</sub> = 500 Ω	t <sub>PLH</sub>	6.8	7.2	2.6	2.7	1.9	1.4	ns
		t <sub>PHL</sub>	5.9	6.4	2.4	1.7	1.7	1.8	ns
1.8 V	C <sub>L</sub> = 30 pF, R <sub>L</sub> = 500 Ω	t <sub>PLH</sub>	11.4	12.1	4.2	4.3	2.7	1.9	ns
		t <sub>PHL</sub>	9.0	10.5	3.8	2.7	3.2	2.2	ns

<sup>†</sup> Measured with C<sub>L</sub> = 30 pF



**Figure 13. Typical Propagation Delays at Different Supply Voltages**

With the AVC family, TI offers an optimized solution for the next low-voltage node of 2.5-V V<sub>CC</sub>. This logic family is the fastest family in this comparison. Even when supplied with 1.8 V, the propagation delay time of the DUT is slightly less than 2 ns.

An application report, *AVC Logic Family Technology and Applications*, literature number SCES06, discussing the features and benefits of this 2.5-V logic, is available from TI.

## Interfacing Between Different Voltage Levels

Regarding the term compatibility, possible interactions between logic devices that are supplied from different power-supply voltages must be considered. It is necessary to distinguish correctly between the terms tolerance, interfacing or translating, and level shifting. The input and output specifications are important for this discussion.

### Input-Overvoltage Tolerance

A logic device is input-overvoltage tolerant if its input can withstand the presence of a higher voltage without being damaged. For example, the input-overvoltage tolerance is called 5-V tolerance if the device is powered from a 3.3-V, 2.5-V, or 1.8-V  $V_{CC}$  source and can accept a voltage level of 5 V at the inputs.

The input overvoltage tolerance is presented in the data sheet under the *recommended operating conditions* topic. The parameter is called  $V_I$  (input voltage). The LVC specification is shown as an example in Table 6.

**Table 6. Extract of Recommended Operating Conditions for the LVCH245A**

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	1.65	3.6	V
$V_I$	Input voltage	0	5.5	V

In this case, the input voltage ( $V_I$ ) exceeds  $V_{CC}$ . This also implies that the device is tolerant of higher input voltage levels at every supply voltage between 1.65 V and 3.6 V. Table 7 shows the input overvoltage tolerance of the logic devices at the different supply voltages.

**Table 7. Input-Overvoltage Tolerance of Different Logic Families**

VOLTAGE ( $V_I$ ) APPLIED TO INPUT	FAMILY AND SUPPLY VOLTAGE			
	ALVT, LVC, LVT, LV, AHC $V_{CC} = 3\text{ V TO }3.6\text{ V}$	ALVT, LVC, LV, AHC $V_{CC} = 2.3\text{ V TO }2.7\text{ V}$	LVC, LV, AHC $V_{CC} = 2\text{ V}$	LVC $V_{CC} = 1.65\text{ V}$
5 V	5-V tolerant	5-V tolerant	5-V tolerant	5-V tolerant
3.3 V		3.3-V tolerant	3.3-V tolerant	3.3-V tolerant
2.5 V			2.5-V tolerant	2.5-V tolerant

AVC logic has 3.3-V input-overvoltage tolerance with 2.5-V  $V_{CC}$  or 1.8-V  $V_{CC}$  and 2.5-V  $V_{CC}$  input-overvoltage tolerance with 1.8-V  $V_{CC}$ .

### Output-Overvoltage Tolerance

A logic device is output-overvoltage tolerant if it can withstand the presence of a higher voltage during the high-impedance state at the output without being damaged.

The output-overvoltage tolerance is in the data sheet in the recommended operating conditions table as the parameter  $V_O$ . An example specification for the SN74LV245A is shown in Table 8.

**Table 8. Extract of Recommended Operating Conditions for the LV245A**

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2	3.6	V
$V_O$	Output voltage	High or low state		V
		0	$V_{CC}$	
		3-state		
		0	5.5	

During the logic high state, the device's output must not be connected to a higher voltage than  $V_{CC}$ ; otherwise, the pullup transistor of the output stage will begin operation in reverse mode and a significant current could flow into the output of the device. This will prohibit a higher voltage logic level than  $V_{CC}$  and, under worst case conditions, damage the logic device.

Table 9 summarizes the output-overvoltage tolerance during the high-impedance state.

**Table 9. Output-Overvoltage Tolerance of Different Logic Families**

APPLIED VOLTAGE DURING THE HIGH-IMPEDANCE STATE	FAMILY AND SUPPLY VOLTAGE			
	ALVT, LVC, LVT, LV $V_{CC} = 3\text{ V TO }3.6\text{ V}$	ALVT, LVC, LV $V_{CC} = 2.3\text{ V TO }2.7\text{ V}$	LVC, LV $V_{CC} = 2\text{ V}$	LVC $V_{CC} = 1.65\text{ V TO }1.95\text{ V}$
5 V	5-V tolerant	5-V tolerant	5-V tolerant	5-V tolerant
3.3 V		3.3-V tolerant	3.3-V tolerant	3.3-V tolerant
2.5 V			2.5-V tolerant	2.5-V tolerant

The LVT logic family is 5-V overvoltage tolerant (inputs and outputs) at 3.3-V  $V_{CC}$ . The ALVT, LVC, and LV families are 5-V overvoltage tolerant (inputs and outputs) at 3.3-V and 2.5-V  $V_{CC}$ . The LVC family also is 5-V overvoltage tolerant (inputs and outputs) at 1.8 V  $V_{CC}$ .

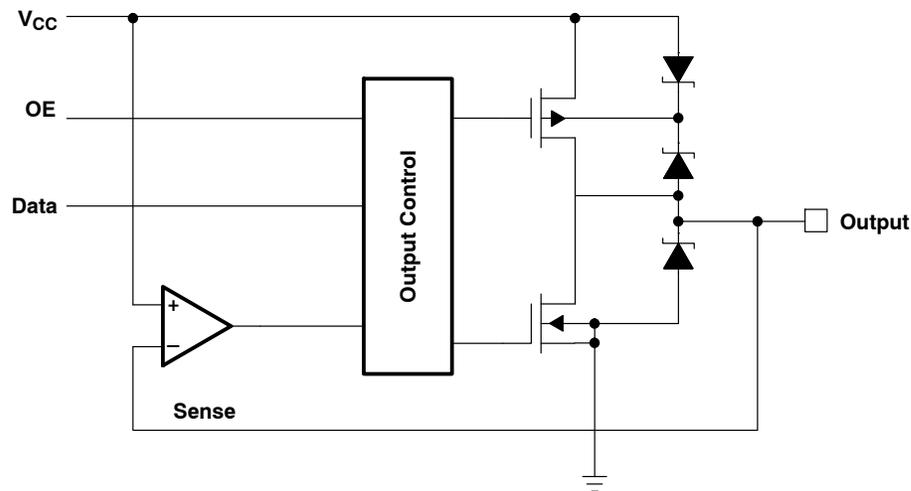
The AVC family is 3.3-V output-overvoltage tolerant at 2.5-V and lower  $V_{CC}$ .

The specification of the ALVC logic family shows the maximum value of  $V_{CC}$  for the input and the output voltages that can be applied to the device inputs and outputs.

The AHC family is tolerant of higher voltages only at the input. At the output, AHC devices have clamping diodes to  $V_{CC}$  such that an overvoltage applied to the output results in a current that flows through the clamping diode within the device to the internal  $V_{CC}$  connection.

### Auto3-State Output of the ALVT Family

The auto3-state function that is implemented in the output of the ALVT family represents a specialty. The principle is shown in Figure 14.



**Figure 14. Simplified Auto3-state Output Stage of the ALVT Family**

Assume that the output is in the active high state and a comparator monitors the voltage at the output and compares it with the supply voltage. If the voltage that is applied externally to the output exceeds the supply voltage, the output stage is switched to the high-impedance state. In this case, the logic levels that are applied to the data and control input pins of the device are irrelevant.

A current of about 30 mA is needed to reach  $V_{CC} + 0.6\text{ V}$  to trigger the auto3-state circuit, so that bus contentions are prevented, but switching noise will not trigger the auto3-state circuit. However, this also implies that the auto3-state cannot be achieved by the use of a simple pullup resistor.

It should be emphasized that a current can flow into the output only in the case of an active high. If the output is set to high impedance by the output enable (OE) control, no current will flow.

The series-opposed Schottky diodes always connect the back gate of the pullup transistor of the output stage to the higher voltage of  $V_{CC}$  or the voltage that is applied externally to the output. In this way, current flow from the output to  $V_{CC}$  is suppressed.

ALVTH logic has full overvoltage tolerance.

### Translation Between Different Logic Levels

All of the logic families mentioned in this report can be operated and will function at 2.5-V and 3.3-V  $V_{CC}$ . The question is, how do they interact when one device is supplied with 2.5-V  $V_{CC}$  and the other with 3.3-V  $V_{CC}$ .

The overview of the different-level specifications from Figure 1 shows that the signal transfer from a 3.3 V  $V_{CC}$  (or higher supply voltage) logic to a 2.5-V  $V_{CC}$  logic will work perfectly if the 2.5-V part has overvoltage tolerance.

$V_{OL}$  (3.3 V) = 0.4 V is lower than  $V_{IL}$  (2.5 V) = 0.7 V, having a noise margin of 300 mV, and  $V_{OH}$  (3.3 mV) = 2.4 V is greater than  $V_{IH}$  (2.5 V) = 1.7 V, resulting in a noise margin of 700 mV.

However, signal transfers in the opposite direction, from a 2.5-V logic to a 3.3-V (or higher supply voltage) logic is more critical. The low-level noise margin with  $V_{OL}$  (2.5 V) = 0.4 V and  $V_{IL}$  (3.3 V) = 0.7 V equals 300 mV. But the high-level definitions show that  $V_{OH}$  (2.5 V) = 2.0 V equals the input high limit of the 3.3-V  $V_{CC}$  logic  $V_{IH}$  (3.3 V) = 2.0 V (Figure 1, 5-V, 3.3-V, and 2.5 V  $V_{CC}$  switching-level comparison). In this case, the interface does not have any noise margin.

Therefore, 2.5-V  $V_{CC}$  devices should not be used to drive 3.3-V  $V_{CC}$  devices.

Table 10 gives an overview of the output-level compatibility of different logic families at 5-V, 3.3-V, 2.5-V, and 1.8-V  $V_{CC}$ .

**Table 10. Output-Level Compatibility of Logic Families at Different Supply Voltages**

LOGIC FAMILIES	SUPPLY VOLTAGE	CAN GENERATE 5-V LEVELS <sup>†</sup>	CAN GENERATE 3.3-V LEVELS <sup>†</sup>	CAN GENERATE 2.5-V LEVELS <sup>†</sup>	CAN GENERATE 1.8-V LEVELS <sup>†</sup>
AHC, LV	5 V	Yes	Yes <sup>‡</sup>	Yes <sup>‡</sup>	Yes <sup>‡</sup>
AHC, LV, LVC, ALVC, ALVT, AVC	3.3 V	TTL levels only	Yes	Yes <sup>§</sup>	Yes <sup>§</sup>
AHC, LV, LVC, ALVC, ALVT, AVC	2.5 V	TTL levels, but no noise margin for $V_{OH}$	No noise margin for $V_{OH}$	Yes	Yes <sup>¶</sup>
LVC, AVC	1.8 V	No <sup>#</sup>	No <sup>#</sup>	No <sup>#</sup>	Yes

<sup>†</sup> Output voltage levels exceed required input threshold voltage of the subsequent input stage at the given supply voltage.

<sup>‡</sup> Receiver logic needs 5-V input tolerance.

<sup>§</sup> Receiver logic needs 3.3-V input tolerance.

<sup>¶</sup> Receiver logic needs 2.5-V input tolerance.

<sup>#</sup>  $V_{OH}$ ,  $V_{OL}$  don't match,  $V_{OL}$ ,  $V_{IL}$  don't match

Table 10 shows that there is a need for level-shifting devices for the interface between 5-V (CMOS) and 3.3-V  $V_{CC}$ , as well as for the translation between 2.5-V and 3.3-V  $V_{CC}$  devices.

A logic-high level at the output of the 3.3-V  $V_{CC}$  device cannot reach the required input high level of the successive 5-V CMOS input stage. Interfacing the output of the 2.5-V  $V_{CC}$  to the successive 3.3-V  $V_{CC}$  device is possible; however, in this case, there is no noise margin.

### 5-V to 3.3-V Level Shifters

Level shifters were developed for interfacing 5-V  $V_{CC}$  CMOS and 3.3-V  $V_{CC}$  logic. The SN74LVC4245A and SN74ALVC164245 establish a connection between 3.3-V  $V_{CC}$  and 5-V  $V_{CC}$  systems. These noninverting bus transceivers use two separate power-supply rails. The voltage ranges are defined as  $V_{CCA} = 4.5\text{ V to }5.5\text{ V}$  and  $V_{CCB} = 2.7\text{ to }3.6\text{ V}$ . The pin layout was designed such that they are directly replaceable by the standard devices SN74xxx245 and SN74xxx16245.

Furthermore, the SN74LVCC4245A is available for the 3.3-V to 5-V CMOS interfacing. The A-port  $V_{CCA}$  is dedicated to accepting a 5-V supply level, and the configurable B port, which is designed to track  $V_{CCB}$ , accepts voltages from 3 V to 5 V. This allows for translation from a 3.3-V  $V_{CC}$  to a 5-V  $V_{CC}$  environment, and vice versa. The LVCC4245A allows the voltage-source pin and I/O pin on the B port to float when  $V_{CCA}$  is supplied, such that there will be no disturbances on the A port if  $V_{CCB}$  and B-port I/O pins are not connected. The device will not operate until  $V_{CCA}$  and  $V_{CCB}$  are applied. This allows buffering data to and from PCMCIA sockets, permitting PCMCIA cards to be inserted and removed during operation.

Figure 15 shows the pinouts of the SN74ALVCH164245 and the SN74LVC4245A/LVCC4245A.

### 2.5-V to 3.3-V/5-V SN74LVCC3245A Level Shifter

The SN74LVCC3245A level shifter gives more flexibility for level shifting. The A-port  $V_{CCA}$  is specified for the supply-voltage range of  $V_{CCA} = 2.3\text{ V to }3.6\text{ V}$  and  $V_{CCB} = 3\text{ V to }5.5\text{ V}$ . This allows for translation from a 2.5-V or 3.3-V environment to 3.3-V or 5-V logic levels, and vice versa. The SN74LVCC3245A is an appropriate solution for all interfacing applications from 2.5-V or 3.3-V logic levels to 3.3-V and/or 5-V CMOS.

The LVCC3245A, like the LVCC4245A, allows the  $V_{CCB}$  voltage-source pin and I/O pin on the B port to float when outputs are disabled. This allows buffering data to and from PCMCIA sockets that permit PCMCIA cards to be inserted and removed during operation.

The pinout of the SN74LVCC3245A is shown in Figure 15.

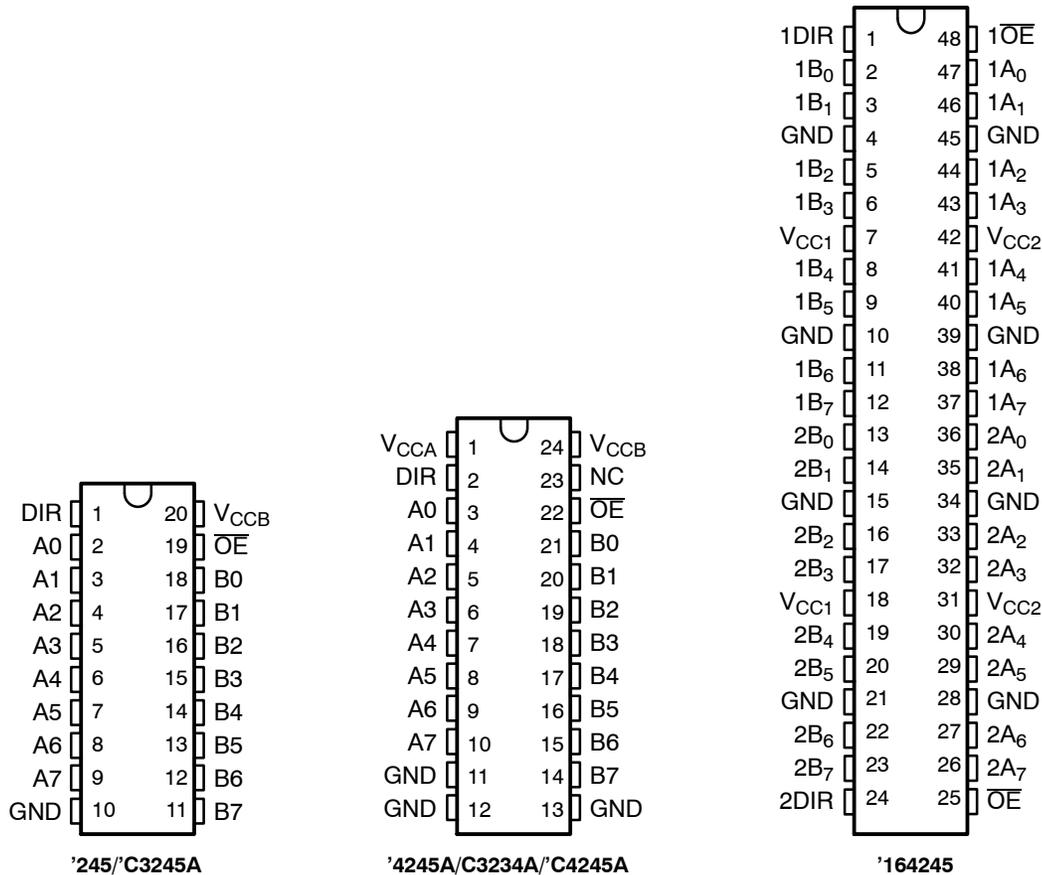
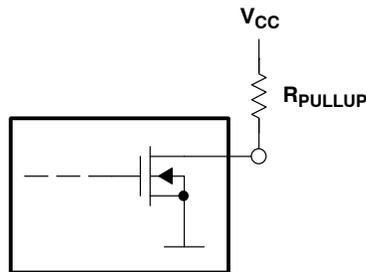


Figure 15. Pinouts of the LVCC3245A, LVCC4245A, LVC4245A, and ALVC164245

### Open-Drain Drivers for Level Shifting

Another option for interfacing different logic levels is the use of open-drain devices. An open-drain output includes a pulldown transistor with the drain connect left open. An external connection via a pullup resistor is necessary. If the output transistor sinks current at the output, a logic-low state results. If the transistor is turned off, the logic-high state is forced by the pullup resistor, which is connected to  $V_{CC}$ .

Figure 16 shows the principle of an open-drain output interface. The value of  $R_{PULLUP}$  can be calculated from current requirements of inputs of the connected receivers, and  $R_{PULLUP}$  must be high enough to limit current into the conducting transistor.



**Figure 16. Open-Drain Output Principle**

Table 11 shows the maximum voltage values that can be applied to the inputs and outputs of the available open-drain devices.

**Table 11. Output-Overvoltage Tolerance at Open-Drain Drivers**

	MAXIMUM VOLTAGE AT INPUT	MAXIMUM VOLTAGE AT OUTPUT
SN74AHC05	5.5 V	$V_{CC}$
SN74LV05	5.5 V	$V_{CC}$
SN74LVC06A	5.5 V	5.5 V
SN74LVC07A	5.5 V	5.5 V

Table 12 gives the level-shifting options for the SN74LVC07A between the different logic levels. The level shifting is possible because the pullup resistor effectively connects the output of the device to any required  $V_{CC}$ . Therefore, the correct switching level is provided to the input of the successive logic device. However, the maximum parameter values of the device, i.e., I/O voltages and current, must not be exceeded.

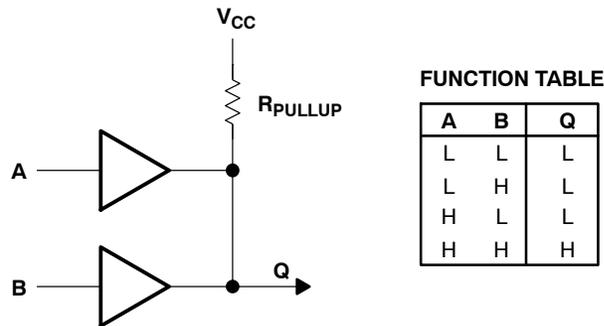
**Table 12. Level Shifting Using the SN74LVC07A**

SUPPLY VOLTAGE $V_{CC1}$	LVC07A UNDERSTANDS	PULLUP RESISTOR CAN BE CONNECTED TO	LEVEL CONVERSION RANGE
1.8 V	1.8-V levels	1.8 V, 2.5 V, 3.3 V, and 5 V	1.8 V to 1.8 V to 5.5 V
2.5 V	2.5-V levels	1.8 V, 2.5 V, 3.3 V, and 5 V	2.5 V to 1.8 V to 5.5 V
3.3 V	3.3-V levels	1.8 V, 2.5 V, 3.3 V, and 5 V	3.3 V to 1.8 V to 5.5 V
5 V	5-V levels	1.8 V, 2.5 V, 3.3 V, and 5 V	5 V to 1.8 V to 5.5 V

## Wired Links

Another benefit from open-drain devices is that additional logic functionality can be built into a system without the need for additional gate devices. An active-low wired-OR and an active-high wired-AND can be implemented.

Figure 17 shows a wired connection and the resulting function table.



**Figure 17. Wired Links Using Open-Drain Connections**

The output (Q) is high when all inputs are high, resulting in an AND function in the case of a high-active-logic definition, and resulting in an OR function in the case of a low-active-logic definition. Those phantom links on the output side can be used to reduce component count. This kind of application is useful because a gate with n inputs can be implemented without extra active components.

## Summary

The trend toward lower supply voltages continues unabated because the complexity of integrated circuits such as ASIC, CPU, and DSP requires continual reduction in structure size.

With the LV, LVC, ALVC, ALVT, AVC, and CBTLV logic families, TI offers options that are solutions for 2.5-V  $V_{CC}$  systems.

The measurement data shows that the propagation delay time of today's 3.3-V logic families varies at  $V_{CC} = 2.5$  V from below the 2-ns range (AVC, ALVT) to 7 ns (LV). The drive capability ( $I_{OH}/I_{OL}$ ) of the devices, which were investigated at 2.5-V, varies between  $\pm 2$  mA (LV) and  $-8$  mA/24 mA (ALVT). Consequently, a suitable logic family for most of the 2.5-V applications already is available.

At 1.8-V  $V_{CC}$  the devices show good performance as well, although the SN74LVCxxxA and SN74AVC logic families are fully specified at this  $V_{CC}$  only.

All investigated samples are fully operational at 1.8 V. The migration from 3.3-V  $V_{CC}$  to 1.8-V  $V_{CC}$  can result in power savings up to 76 percent.

The logic families ALVT, LVC, and LV show full overvoltage I/O tolerance at 1.8-V, 2.5-V and 3.3-V  $V_{CC}$ .

Options on bidirectional interfacing of different logic levels are given, with the level shifters that enable bidirectional level shifting from 2.5 V to 5.5 V.

Another option enabling even more flexibility is the open-drain driver, SN74LVC07A, that interfaces 1.8-V up to 5.5-V logic levels.

## Acknowledgment

The author of this report is Johannes Huchzermeier.

## Glossary

### A

ABT	Advanced BiCMOS Technology
AC	Advanced CMOS
AHC	Advanced High-Speed CMOS
ALS	Advanced Low-Power Schottky
ALVC	Advanced Low-Voltage CMOS
ALVT	Advanced Low-Voltage Technology
AS	Advanced Schottky
Auto3-state	During the active-high state at the output, devices with auto3-state tolerate a higher voltage level at the outputs. This is also called overvoltage protection.
AVC	Advanced Very Low-Voltage CMOS

### B

BCT	BiCMOS Technology
BiCMOS	Combination of Bipolar and CMOS processes: CMOS input structure and bipolar output structure
Bus hold	Input circuitry that holds the last valid logic state that was applied to it before entering a nondefined state on the bus until a new valid logic state is driven actively.

### D

DUT	Device under test
-----	-------------------

### G

GND	Ground
-----	--------

### I

$I_{CC}$	Supply current
I/O	Input/Output

## L

LS	Low-Power Schottky
LV	Low-Voltage CMOS, originally designed for $V_{CC} = 3.3\text{-V}$ , also specified at 5 V
LVC	Low-Voltage CMOS
LVT	Low-Voltage Technology

## O

Overvoltage protection    See auto3-state and 3-/5-V tolerance

## R

$R_L$	Load resistor
$R_{PULLUP}$	Resistor that is used for open-drain devices to ensure a logic-high level on the signal line
ROC	Recommended operating conditions

## S

Series resistor	A resistor that is implemented on the output stage of a bus driver. With this resistor, the effective output impedance of the driver is shifted to a value of about $50\ \Omega$ , which is an optimum line termination.
S	Schottky
SPICE	Simulation Program with Integrated Circuit Emphasis

## T

3-/5-V tolerance	Logic devices with 5-V (3.3-V) tolerance tolerate 5-V (3.3-V) CMOS logic levels at their input and output during the high-impedance state, while supplied with 2.5-V
TTL-level	Transistor-transistor logic levels

## V

$V_{CC}$	Supply voltage
----------	----------------

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***Voltage Translation  
(5 V, 3.3 V, 2.5 V, 1.8 V),  
Switching Standards, and  
Bus Contention***

SCYA006  
September 1999



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## Abstract

Voltage translation is required because many analog devices operate at 5-V  $V_{CC}$ , but most digital products operate at 3.3-V  $V_{CC}$ , or lower. Interfaces between devices must consider issues such as driver and receiver switching compatibility and bus contention. Texas Instruments (TI™) offers a variety of products that provide translation among 5-V, 3-V, 2.5-V, and 1.8-V devices.

## Introduction

In today's applications there are many mixed-voltage designs that require voltage translation between different levels. Many analog products still operate at 5-V  $V_{CC}$ , whereas, most digital products have migrated to 3.3-V  $V_{CC}$ , or lower. TI's logic devices are ideal for these types of situations. This application report explains how to utilize TI logic products for both CMOS and TTL voltage translations.

### Switching Compatibility Between Drivers and Receivers

To have switching compatibility between a driver and a receiver, the output of the driver must be compliant with the input of the receiver. To establish a low signal at the receiver,  $V_{OL}$  of the driver should be less than or equal to  $V_{IL}$  of the receiver. To establish a high signal at the receiver,  $V_{OH}$  of the driver should be greater than or equal to  $V_{IH}$  of the receiver (see Figure 1).

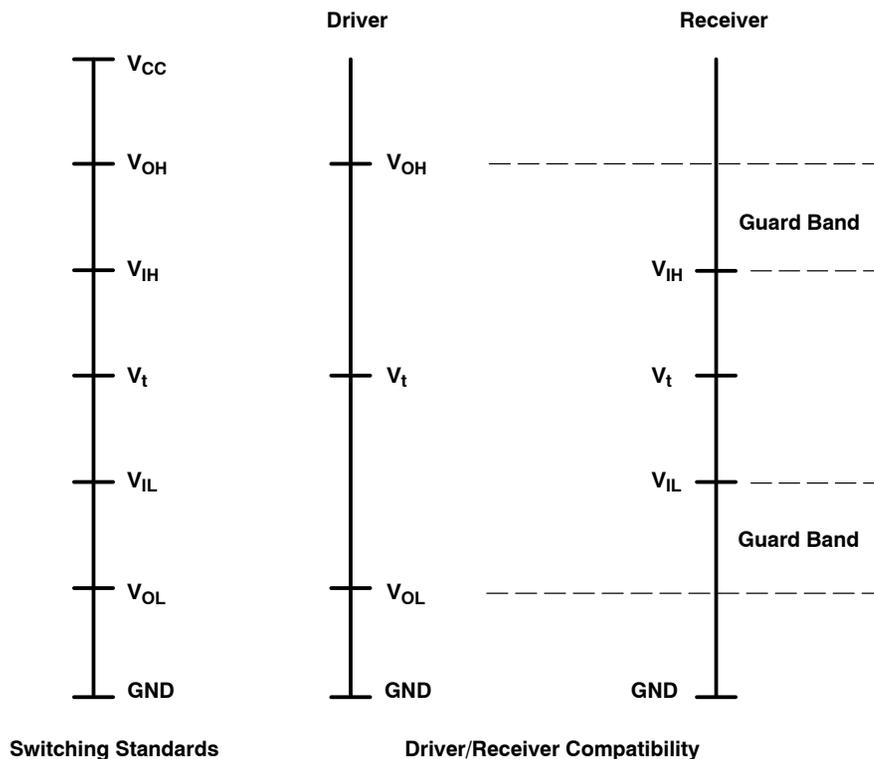
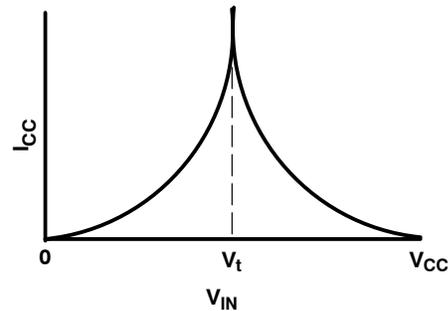


Figure 1. Switching Standards

The guard band is the difference between the  $V_{OH}$  of the driver and the  $V_{IH}$  of the receiver and the difference between the  $V_{OL}$  of the driver and the  $V_{IL}$  of the receiver.

The threshold voltage ( $V_t$ ) is the transition voltage where both the PMOS and NMOS transistors of the input stage may be turned on at the same time. At this level there is no valid signal level, and the device is unstable.

For CMOS devices, when both transistors are fully and/or partially turned on, there is a low-resistance current path from  $V_{CC}$  to ground that results in high power dissipation. When switching from low to high or high to low, the voltage passes through the threshold; however, it is not recommended that the input voltage of the receiver remains at the threshold region. This may cause a high surge of current drain that can damage the input and destroy the device (see Figure 2). A good practice is to keep the signal levels at the recommended operating conditions (above  $V_{IH}$  or below  $V_{IL}$  of the receiver).

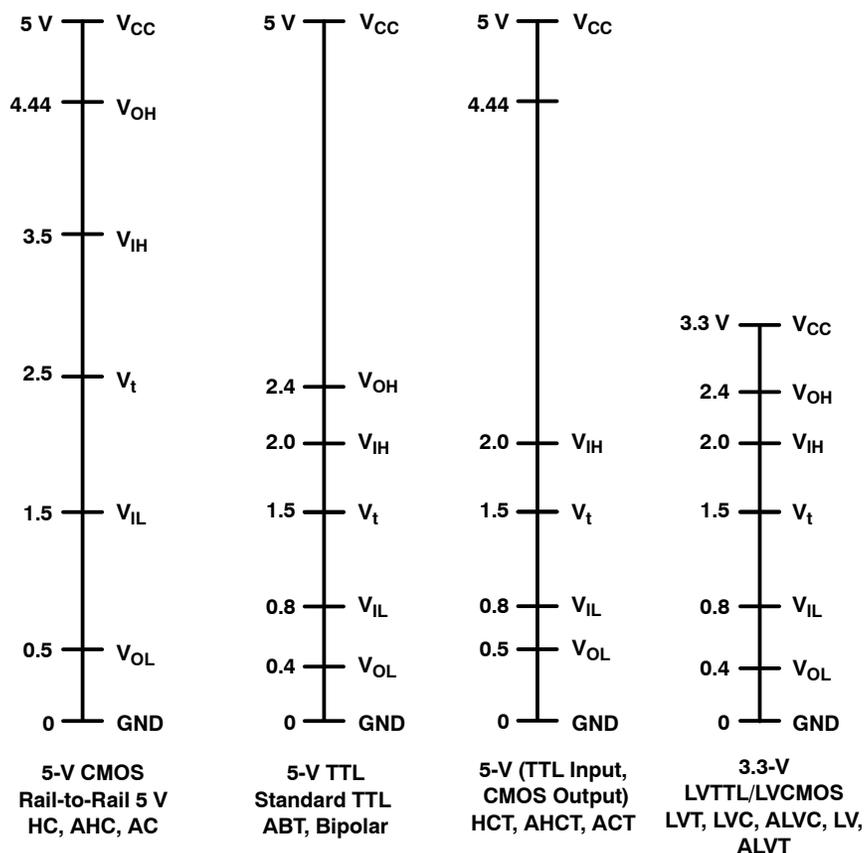


**Figure 2.  $V_{IN}$  vs  $I_{CC}$**

As shown in Figure 2, the current consumption is the lowest at  $V_{IN}$  equal to 0 V or  $V_{CC}$ , and highest at the threshold voltage ( $V_t$ ). Therefore, the power dissipation is lower when input voltages are at  $V_{CC}$  or ground. Refer to  $I_{CC}$  and  $\Delta I_{CC}$  specification in the data sheet.

## Product Families and Switching Standards

Figure 3 shows the switching standards for TI logic families.



**Figure 3. Comparison of Switching Standards**

Frequently asked questions about switching standards are:

***Do 3.3-V LVTTTL and 3.3-V LVCMOS have the same switching standards?***

Yes, 3.3-V LVTTTL and 3.3-V LVCMOS have the same switching standards.

***Which switching standards are compatible?***

5-V TTL and 3.3-V (LVTTTL and LVCMOS) have the same switching standards for V<sub>OL</sub>, V<sub>IL</sub>, V<sub>IH</sub>, and V<sub>OH</sub>. The only difference is V<sub>CC</sub>.

***Is 5-V CMOS compatible with 5-V TTL or 3.3-V LVTTTL/LVCMOS?***

In most cases, no, because V<sub>IH</sub> for 5-V CMOS is 3.5 V. The exceptions are the HCT, AHCT, and ACT devices, which have TTL-input and CMOS-output compatibility.

***Where do TI logic families fit in?***

5-V CMOS inputs and outputs:	HC, AHC, and AC
5-V TTL inputs and outputs:	ABT and bipolar
5-V TTL inputs and 5-V CMOS outputs:	AHCT, HCT, and ACT
3.3-V CMOS and LVTTTL:	LVC, ALVC, LV, LVT, ALVT, AVC, and AHC

## Unidirectional Voltage Translations

### Voltage Translation From 3.3-V LVTTTL/LVCMOS to 5-V TTL

Because all TI 3.3-V logic devices are output compatible with 5-V TTL, this voltage translation can be done with TI 3.3-V families, such as LVT, LVC, ALVC, LV, ALVT, AHC, HC, and AVC (see Figure 4).

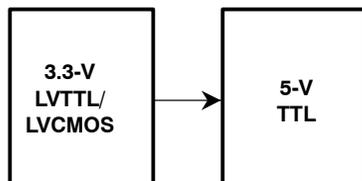


Figure 4. 3.3-V LVTTTL/LVCMOS to 5-V TTL

### Voltage Translation From 5-V TTL to 3.3-V LVTTTL/LVCMOS

Because the 5-V TTL and 3.3-V LVTTTL/LVCMOS switching standards are compatible, except for the  $V_{CC}$ , this translation can be done with TI 3.3-V logic families that have 5-V tolerant inputs, such as LVC, AHC, LVT, and ALVT. These logic families do not have a diode to  $V_{CC}$ , which was formerly used for electrostatic-discharge (ESD) protection (see Figure 5).

The diode to  $V_{CC}$  results in a current conduction at  $3.3\text{ V} + 0.5 V_{be}$ . The resulting effects from the diode are:

- Clamping the driving signal at 3.3 V plus the diode drop
- Pulling the 3.3-V supply to a higher voltage (which may violate the data-sheet specification)
- Powering up a device that was intended to be powered down

Therefore, TI's 5-V-tolerant low-voltage families do not have this diode to  $V_{CC}$  and can be used in this voltage translation. They have other methods for ESD protection.

TI's CBTD or CBT with an external diode also can be used for 5-V TTL to 3.3-V LVTTTL/LVCMOS translation.

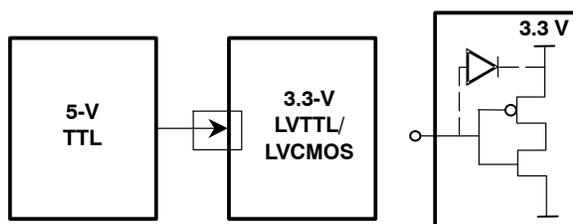


Figure 5. 5-V TTL to 3.3-V LVTTTL/LVCMOS

### Voltage Translation From 5-V CMOS to 3.3-V LVTTTL/LVCMOS

This voltage translation can be done if the TI 3.3-V logic device is 5-V tolerant on the inputs, such as LVC, AHC, LVT, and ALVT (see Figure 6).

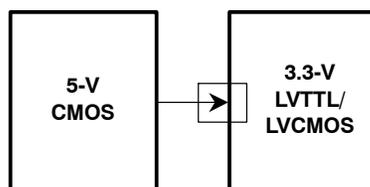


Figure 6. 5-V CMOS to 3.3-V LVTTTL/LVCMOS

### Voltage Translation From 3.3-V LVTTTL/LVCMOS to 5-V CMOS

The 5-V CMOS  $V_{IH}$  is 3.5 V, which is above the  $V_{OH}$  of the 3.3-V devices. Therefore, a standard 3.3-V device cannot achieve this type of translation. TI has split-rail transceivers that have two voltage supplies, one on the A port and one on the B port, that allow for translation from 3.3-V LVTTTL/LVCMOS to 5-V CMOS devices. The 8-bit LVCC3245A and LVCC4245A transceivers have configurable rails on the B port. The LVCC3245A A port can operate between 2.3-V and 3.6-V  $V_{CC}$ . The configurable B port can operate between 3-V and 5.5-V  $V_{CC}$ . The LVCC4245A A port operates between 4.5-V and 5.5-V  $V_{CC}$ , and the configurable B port operates between 2.7-V and 5.5-V  $V_{CC}$ . TI also offers 16-bit SN74ALVC164245 transceivers in which the A port has a 5-V  $V_{CC}$  and the B port has a 3.3-V  $V_{CC}$  (see Figure 7).

TI also has 5-V logic families (AHCT, HCT, and ACT) that have TTL inputs and CMOS outputs. Therefore, these devices can interface 3.3-V outputs to 5-V CMOS inputs (see Figure 7).

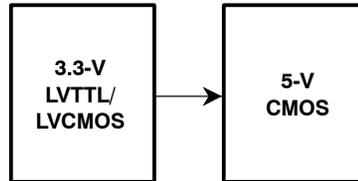
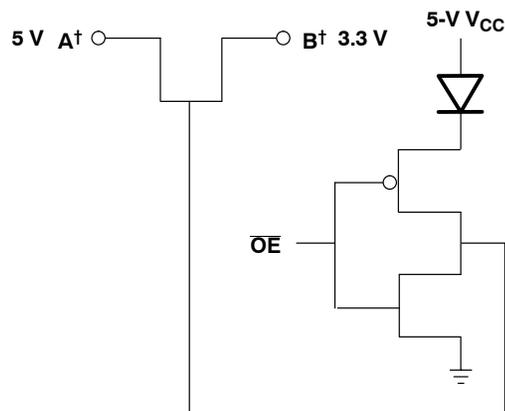


Figure 7. 3.3-V LVTTTL/LVCMOS to 5-V CMOS

### Bidirectional Voltage Translation

#### Voltage Translation From 3.3 V to 5-V TTL and From 5-V TTL to 3.3 V Using CBT or CBTD

This type of bidirectional translation (from A to B or B to A) can be done with TI's SN74CBT bus switches, using an external diode, or SN74CBTD bus switches that have the diode integrated internally. This method is suitable for voltage translation and bus-isolation applications. For example, with TI's 5-V  $V_{CC}$  SN74CBTD3384 bus switch (see Figure 8), the conditions are such that there are no pulldown resistors, and there is a minimal current passing through the FET.



† A can be 3.3 V, and B can be 5 V.

Figure 8. CBTD Bus Switch

The diode drop between  $V_{CC}$  and the PMOS gate is 0.7 V, which brings the voltage at the source to 4.3 V. With a 5-V input on the A side, the  $V_{gs}$  drop across the N channel is approximately 1.0 V, hence, the B side is translated to about 3.3 V. The typical  $V_{CC}$  vs  $V_{OH}$  graph is shown in Figure 9 and is provided in the data sheets for various temperatures and currents. In this example, the maximum voltage that can pass from B to A is 3.3 V. If a voltage less than 3.3 V is applied at B, the same voltage results on the A side. If a voltage greater than 3.3 V is applied at B, it is limited to 3.3 V on the A side. The  $V_{IH}$  min for 5-V TTL is 2.0 V. Therefore, as long as the voltage at B complies with 5-V TTL switching standards, this device can translate in both directions. Utilizing a bus switch for voltage translations also has the advantage of very fast propagation delay time.

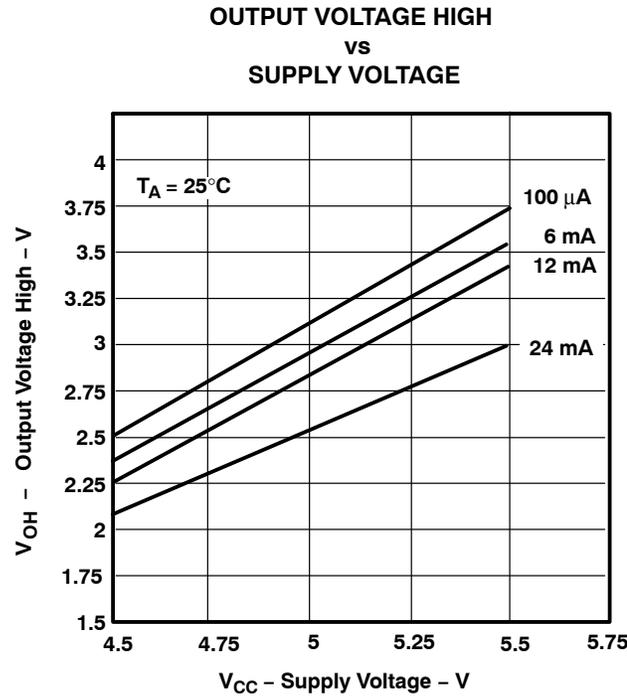


Figure 9. Typical  $V_{OH}$  vs  $V_{CC}$

### Voltage Translation From 3.3 V to 5-V TTL and 5-V TTL to 3.3 V Using TI 5-V-Tolerant Transceivers

TI's low-voltage logic transceivers that are 5-V input and output tolerant, such as LVT, ALVT, and most LVC devices, can be used for bidirectional voltage translation between 3 V and 5-V TTL when buffering is required, and added delay is not critical to the application (see Figure 10). Output tolerance is specified as output voltage ( $V_O$ ) or as the voltage range applied to any output in the high-impedance or power-off state (refer to the absolute maximum ratings in the data sheet for more information).

See the *Bus Contention* section of this application report.

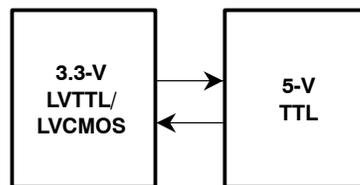


Figure 10. Translation Between 3.3 V and 5-V TTL

### Voltage Translation From 3.3-V LVTTTL/LVCMOS to 5-V CMOS and From 5-V CMOS to 3.3 V

Because 5-V CMOS switching standards have a  $V_{IH(min)}$  of 3.5 V, TI split-rail devices, SN74LVCC4245A, SN74LVCC3245/A, and SN74ALVC164245 transceivers are the method of bidirectional voltage translation between 3.3-V and 5-V CMOS (see Figure 11).

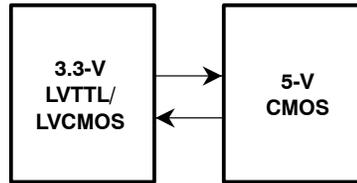


Figure 11. Translation Between 3.3-V and 5-V CMOS

### Voltage Translation Between 3.3 V, 2.5 V, and 1.8 V

The switching standards allow for voltage translation between 2.5 V and 3.3 V. Voltage translation between 3.3 V and 2.5 V also is permissible if the 2.5-V device is 3.3-V input tolerant. Voltage translation between 1.8 V and 3.3 V is not possible because the 3.3-V  $V_{IH min}$  is 2.0 V, which is not in range for a 1.8-V  $V_{CC}$  device. Voltage translation from 1.8 V to 2.5 V also is not possible because the  $V_{IH min}$  for a 2.5-V  $V_{CC}$  device is 1.7 V (see Figure 12).

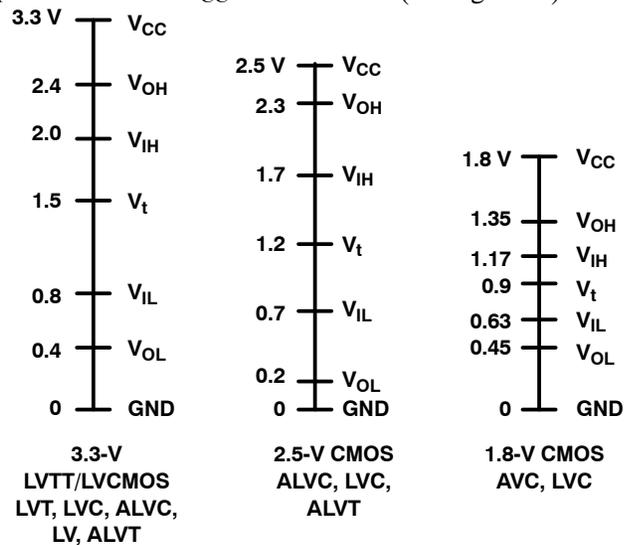
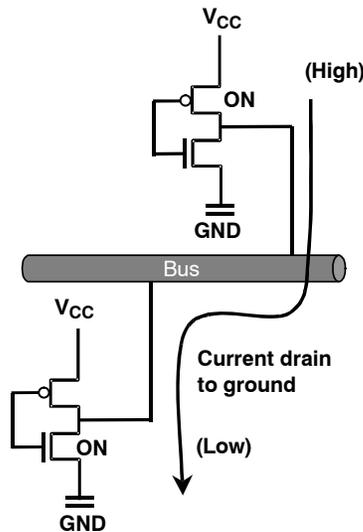


Figure 12. Comparison of Low-Voltage Switching Standards

## Bus Contention

TI data sheets specify the maximum continuous current through a single output or through  $V_{CC}$  and GND. These values are absolute maximum ratings, which are stress ratings, not recommended operating conditions. These specifications most likely are exceeded when bus contention occurs.

Figure 13 shows a bus-contention situation between two devices driving the same bus. One has low-level output and the other has high-level output. This happens when drivers that have different enable and disable delays get on and off the same bus. This produces a short between the drivers, creating a current surge that may damage the devices. Typically, logic devices cannot withstand these high-current shorts that usually exceed the absolute maximum ratings of the device.

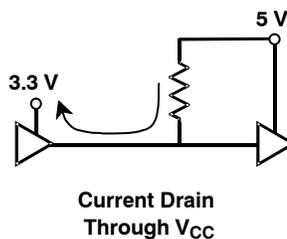


**Figure 13. Bus Contention**

If  $V_{CC} = 5\text{ V}$  and the resistance through the p and n channels of the transistors is about  $10\ \Omega$  per output:

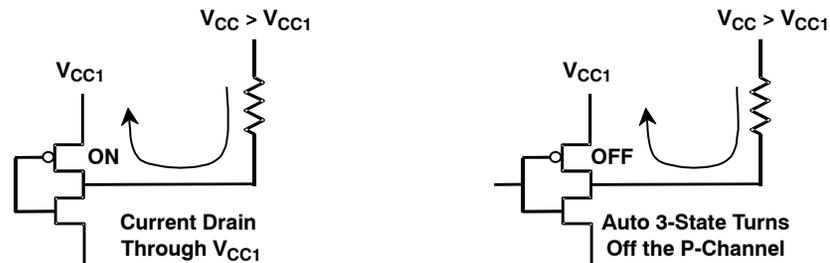
$$I = \frac{V}{R} = \frac{5\text{ V}}{10\ \Omega} = 0.5\text{ A per output} \quad (1)$$

Another high-current situation that may damage the device occurs when a 3.3-V device is at a high level and the output is pulled up to a higher voltage, such as 5 V (see Figure 14). Properly sizing the pullup resistor is very important. Using a pullup resistor of proper value limits the current to an allowable level. The device will not be damaged; however, there will be additional power dissipation from the current path through the 3.3-V device to  $V_{CC}$ .



**Figure 14. 3.3-V Driver Pulled to a Higher  $V_{CC}$**

The ALVT family has the auto3-state feature that automatically turns off the p-channel of the logic device to stop the current flow to  $V_{CC}$  (see Figure 15). This feature is specified in the absolute maximum ratings table of the ALVT data sheet as the voltage range applied to any output in the high state (-0.5 V to 7 V).



**Figure 15. Auto3-State**

### **Conclusion**

Voltage translation from 5 V to 3 V, 3 V to 2.5 V, and vice versa, can be done with a wide variety of TI logic products. 3.3-V and 2.5-V logic can translate to 1.8 V, if the 1.8-V device is 2.5-V and 3.3-V tolerant. However, due to switching standards, 1.8-V logic currently cannot be translated upward to 2.5 V and 3.3 V with the existing families. Newer families are being developed to handle voltage translations of these levels.

### **Acknowledgment**

The authors of this application report are Susan Feodorov and Ramzi Ammar.

## Glossary

### A

ABT	Advanced BiCMOS technology
AC/ACT	Advanced CMOS logic
AHC/AHCT	Advanced high-speed CMOS logic
ALVC	Advanced low-voltage CMOS technology
ALVT	Advanced low-voltage BiCMOS technology

### C

CBT	Crossbar technology
CMOS	Complementary metal-oxide semiconductor

### L

LS	Low-power Schottky logic
LV	Low-voltage CMOS technology
LVC	Low-voltage CMOS technology
LVCMOS	Low-voltage CMOS
LVT	Low-voltage BiCMOS technology
LVTTTL	Low-voltage TTL (3.3-V power supply and interface levels)

### V

$V_{CC}$	Supply voltage
$V_{IH}$	High-level input voltage
$V_{IL}$	Low-level input voltage
$V_{IN}$	Input voltage
$V_{OH}$	High-level output voltage
$V_{OL}$	Low-level output voltage
$V_{OLP}$	Low-level output voltage peak
$V_{OLV}$	Low-level output voltage valley
$V_t$	Threshold voltage

# ***PCB Design Guidelines For Reduced EMI***

SZZA009  
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## ABSTRACT

General layout guidelines for printed circuit boards (PCB), which exist in relatively obscure documents, are summarized. Some guidelines apply specifically to microcontrollers; however, the guidelines are intended to be general, and apply to virtually all modern CMOS integrated circuits. This document covers most known and published layout techniques as applied in a low-noise, unshielded environment. Efforts have been made to target two-layer boards, and the maximum acceptable noise level is assumed to be 30 dB, or greater, more stringent than FCC Part 15. This level seems to be the upper limit of acceptable noise in European and U.S. automotive markets.

This document does not always explain the why's of a given technique because it is intended only as a reference document, not a teaching aid. The reader is cautioned against making the assumption that although on a prior design a given technique was not applied and the unit had acceptable performance, that the technique is not useful. Over time, as IC devices increase in speed and density, every method to isolate and reduce noise will be required.

## 1 Background

### 1.1 RF Sources

Design guidelines to be discussed concern radio-frequency (RF) noise from the microcomputer. This noise is generated inside the device and is coupled out in many different possible ways. The noise is present on all outputs, inputs, power supply, and ground at all times. Potentially, every pin on the microcomputer can be a problem.

The biggest problem is noise from the integrated-circuit (IC) input/output (I/O) pins. Because the area covered by traces connected to them on the PCB form a large antenna. These pins also connect to both internal and external cables. The noise from clock switching within the IC appears as “glitches” on a static output. The glitch is caused by the common impedance of the output pin and the clock drivers, that is, the shared pins that supply each power and ground. The synchronous nature of most devices causes all current-switching events to occur at the same time, making a large noise spike containing RF energy.

The second most-important contributor is the power-supply system, which includes the voltage regulation and the bypassing capacitors at both the regulator and at the microcomputer. These circuits are the source of all the RF energy in the system, as they feed the clocked circuits inside the IC with the current required for switching.

The third noise source is the oscillator circuit, where the oscillator swings rail to rail. In addition to the fundamental frequency, harmonics are introduced on the output side because the output buffer is digital, which squares the sine wave. Also, any noise caused by internal operations, such as the clock buffers, appears on the output. If proper separation is maintained between the crystal and its tank circuits from other components and traces on the PCB, and the loop areas are kept small, there should be no problems with this noise source. But it has been shown that if ICs or passive components, such as the main  $V_{\text{Batt}}$  series inductor, are placed close to the crystal, harmonics of the crystal can couple and propagate.

The primary focus in this application report is on the first and second previously described noise sources. The way to deal with the third noise source has been addressed. Also, critical information is disclosed on board zoning (floor planning) and shielding.

### 1.2 Surface-Mount Devices vs Through-Hole Components

Surface-mount devices (SMD) are better than leaded devices in dealing with RF energy because of the reduced inductances and closer component placements available. The latter is possible due to the reduced physical dimensions of SMDs. This is critical to two-layer board design, where maximum effectiveness from noise-control components is needed. Generally, leaded capacitors all go self-resonant (become more inductive than capacitive) at about 80 MHz. Because noise above 80 MHz needs to be controlled, serious questions should be asked if a design is to be executed only with through-hole components.

### 1.3 Static Pins vs Active Pins vs Inputs

As mentioned previously, all lines have noise from the processor, to some degree. The total noise from a pin depends on how much noise the microcomputer provides it and its function in the system. For example, an output pin has the noise from the microcomputer's power rails and the noise capacitively coupled from adjacent pins and the substrate. If the pin's function is the system clock, that too is noise. Even if the pin were static at a one or zero level, one would still have to contend with noise from inside the chip.

In the case of an I/O pin in the input mode, the capacitance of the unused output transistors transfers noise from both power rails to the pin. The amount of noise is based on the impedance of whatever is connected to the pin. The higher the impedance, the more noise comes out of the microcomputer. That is why unused inputs should be tied to the lowest-impedance rail: ground, by direct short, if possible.

With respect to switching output signals, basically, only worry about signals that make an edge transition at a rate greater than 50 kHz (see Figure 1). If a pin changes its state at a rate of less than once per 100 instructions, this is acceptable because the contribution from switching is negligible. If the pin toggles, and toggles back on the next instruction, and remains static for 100 instructions, it, too, is acceptable because it contains the same amount of energy as in the previous example.

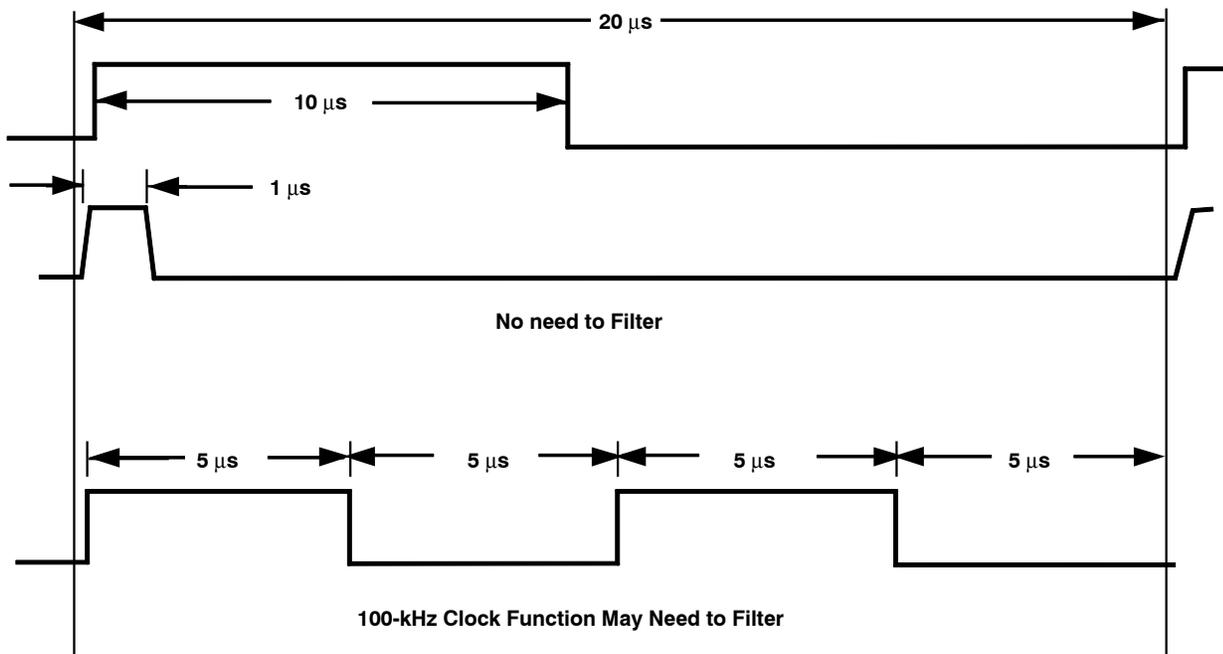
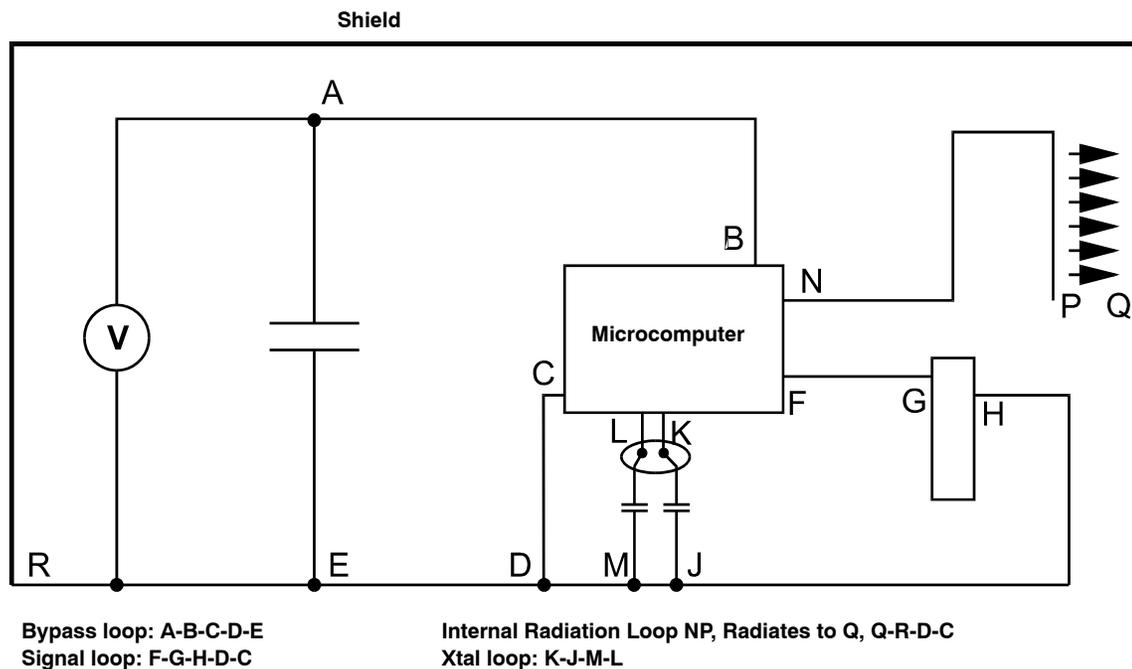


Figure 1. Signals Below 50 kHz Are Not EMI Concerns

## 1.4 Basic Loops

Every edge transition that is sent from the microcomputer to another chip is a current pulse. The current pulse goes to the receiving device, exits through that device's ground pin, then returns via the ground traces, to the ground pin of the microcomputer (see Figure 2). The pulse does not exit the ground lead of the receiving device and return to the battery, but travels in a loop to where it originates. Loops exist everywhere. Any noise voltage and its associated current travels the path(s) of lowest impedance back to the place where it was generated. This is a very powerful concept, because it allows you to mitigate noise propagation by controlling the shape and impedance of the return path.

A loop can be a signal and its return path, the bypassing loop between power and ground and the active devices inside the microcomputer, the oscillator crystal and its driver in the microcomputer, as well as the loop from the power supply or voltage regulator to the bypassing capacitors. Other more difficult loops are actually ambient field loops. For example, the crystal itself radiates energy that can be coupled into a wire running nearby. Then, the wire contains noise that tries to get back to the crystal loop. That may involve a very long and convoluted path, which serves as another antenna for noise from the crystal.



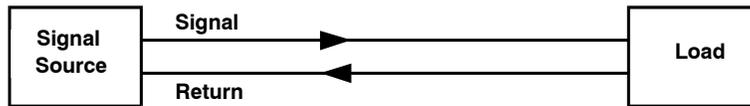
**Figure 2. Examples of Loops**

### 1.4.1 Proportionality of Loops and Dipoles

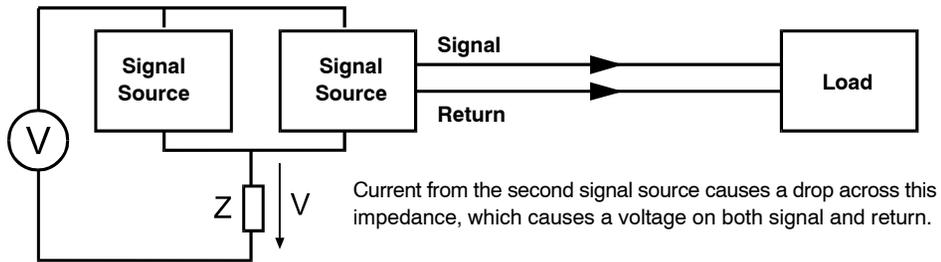
Loops and dipoles are antennas. Their radiating efficiency increases up to  $1/4$  wavelength ( $\lambda$ ) of the frequency of interest. Geometrically, that means, in the case of a loop, that the larger the laid-out area of the loop, the stronger the radiation until one or both legs of the loop reach  $1/4$  wavelength. In the dipole, the longer the antenna, the more radiation, until the length of the antenna reaches  $1/4$  wavelength. At 1 MHz,  $1/4 \lambda = 75$  m. At 300 MHz,  $1/4 \lambda = 25$  cm, or about 10 inches.

### 1.5 Differential vs Common Mode

Differential-mode noise is the noise of a signal as it travels down its trace to the receiving device, then back along the return path (see Figure 3). There is a differential voltage between the two wires. This is the type of noise that every signal must make in order to do its job. Make sure there is no more noise than needed to get the job done, in terms of both frequency content (rise and fall times) and the magnitude of the current. In common mode, a voltage travels down both the signal and return lines at the same time. There is no differential between the signal and its return. The voltage is caused by an impedance that is common to both the signal and the return. *Common impedance noise is the most common source of noise in most microcomputer-based systems that are not using external memories.*



Differential-mode noise is the "noise" voltage when a signal travels to its lead and returns. An output switching is an example of differential-mode noise.



Common-mode noise is the noise voltage that travels down both the signal and return caused by a voltage drop across a shared impedance. Ground bounce on outputs is an example of common-mode noise.

**Figure 3. Differential-Mode vs Common-Mode Noise**

## 2 Board Layout

### 2.1 Grounds and Power

The only non-dc current that should flow in the power routing of the PCB is the current required to replenish the bypassing capacitor. High-frequency current used inside the microcomputer that is switched on the input clock edges should come from the bypassing capacitors, not from the power supply.

#### 2.1.1 Inductance

Inductance increases with increasing length, and decreases (at a slower rate) with increasing width of the conductor. In power routing, the inductance makes voltage drops that radiate and propagate.

Because it is not desirable for any trace to radiate RF energy, any trace carrying RF energy should be as low an inductance as possible:

- On a two-layer board, for both power and ground, the length-to-width ratio should not exceed 3:1 for any traces between the IC and the voltage source.
- Power and ground should be run directly over each other, which reduces impedance and minimizes loop area.

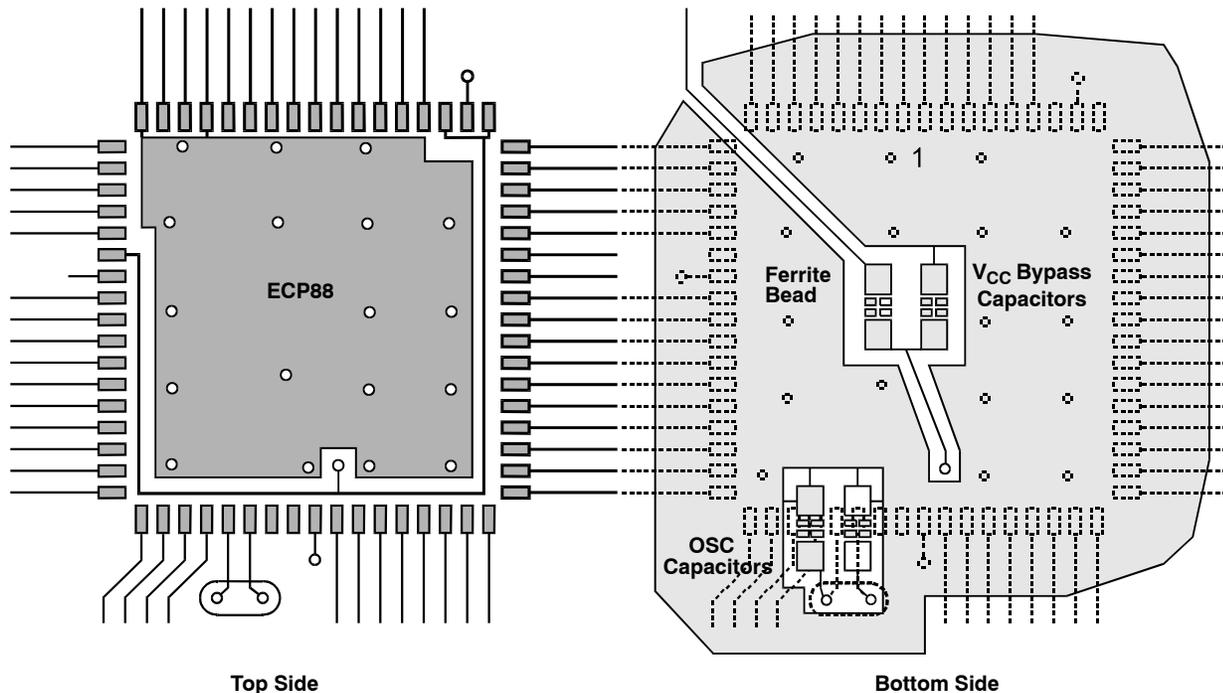
#### 2.1.2 Two-Layer vs Four-Layer Boards

A two-layer board can achieve 95% of the effectiveness of a four-layer board by emulating what makes a four-layer board better:

- Make an extra effort to route ground underneath power.
- Grid power and ground, but be careful not to create unneeded common impedance connections or to violate an intended isolation, such as between high-power and digital grounds. See section 2.2.3, *Gridding to Create Planes*.
- Route returns for direct connections to the processor I/Os directly under the signal trace. Gridding is a space-effective way of doing this. See section 2.2.3, *Gridding to Create Planes*.
- Under the microcomputer, build a solid plane for ground that bypassing components and the oscillator loop can be tied to. Tie this ground to the ground pin and the power-supply bypass capacitor. This is called a microcomputer ground, which is discussed in section 2.1.3.

#### 2.1.3 Microcomputer Grounds in One- and Two-Layer Designs

A microcomputer ground is a ground area on the bottom layer underneath the microcomputer that becomes a ground island for the noise made by the microcomputer. This area should extend about 1/4 inch outside the outline of the device and tie to the microprocessor ground. Ground connections for the power-supply bypassing capacitors and any bypassing capacitors on the pins also should tie to this ground. Additionally, the ground area should extend out and around the through holes for the oscillator leads, and the bypass capacitors tied in to provide the smallest possible loop area when viewed from the top. See Figure 4 for an example.



**Figure 4. Microcomputer Ground**

The topside traces are shown in dotted line form on the bottom side diagram for alignment purposes. Notice how the oscillator capacitors lay back over the traces between the device and the crystal. This eliminates loop area. The same is true for the placement of the ferrite bead and  $V_{CC}$  bypass capacitor, being centrally located with the main power lead running almost directly under the lead finger for the ground.

#### 2.1.4 Signal Return Grounds

As mentioned previously in section 1.4, a loop is made by a signal, and the ground return path from the receiver device back to the signal source. Signal return paths present the most difficult design problem in PCB layout.

It would be difficult to route a ground return underneath each trace connected to a signal pin on the microcomputer. But, this is exactly what the ground plane of a four-layer board does. No matter where the traces run, there is always a ground return path running underneath it.

The closest approximation to having a ground plane in a two-layer board comes from gridding the ground, as described in section 2.2.3. As stated previously, radiation from the signal traces is the primary concern. Reducing the loop area by routing the return for the signal underneath the signal trace is most effective way of dealing with this problem. Therefore, creating a ground grid is the most important thing to do (after floor planning) in laying out the PCB.

#### 2.1.5 Analog vs Digital vs High Power

Digital ground and power carry the RF energy that needs to be contained, so it is best to isolate it from any other power and ground, either analog, high power, or other unrelated trace. If noise from the microcomputer or any other circuit gets on an isolated ground, it can be returned by careful placement of a small RF capacitor in the 470 – 1000 pF range. Choosing the location of the capacitor is by trial and error, and is best done in the screen room.

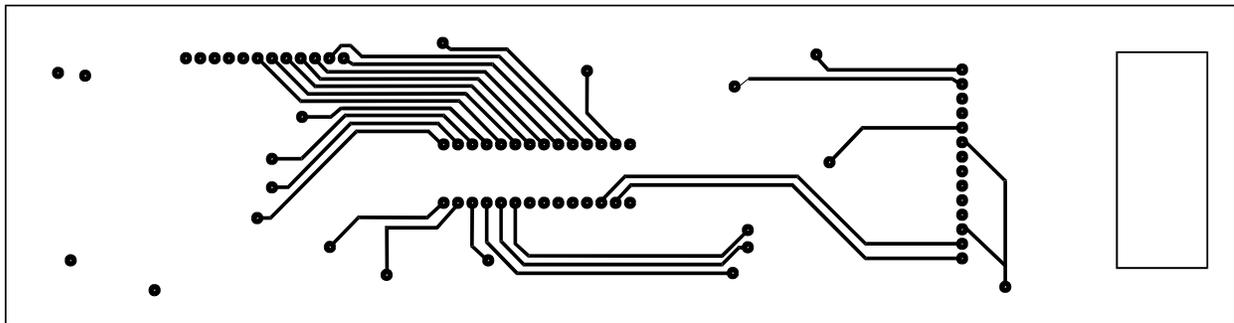
#### 2.1.6 Analog Power-Supply Pins and Analog Reference Voltages

The reference voltage of an analog-to-digital (A/D) converter integrated into a microcomputer does supply a very small amount of clocked current; however, it is not enough to be concerned about from a noise-emissions standpoint. Most applications have the analog  $V_{SS}/V_{CC}$  tied to the digital  $V_{SS1}/V_{CC1}$  pins, which does not change significantly the noise characteristics of the A/D nor the radiated emissions, provided the power distribution is built to guidelines in sections 2.1.1 through 2.1.4.

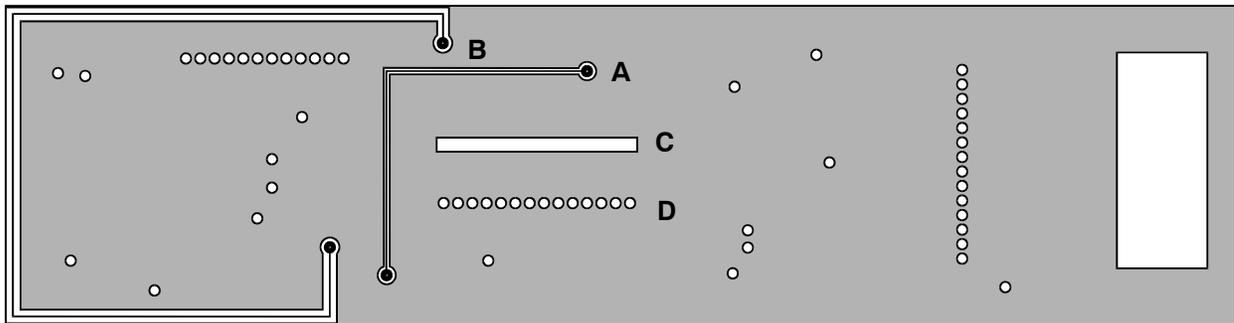
### 2.1.7 Power Plane Do's and Don'ts for Four-Layer Boards

The reasons for reduced noise from four-layer boards were mentioned in section 2.1.2. The following guidelines should maintain the advantages gained in the four-layer board.

- Pay utmost attention to how the holes and cutouts in the planes are done. They break up the plane and, therefore, cause increases in loop areas (see A and B in Figure 5).
- Avoid buried traces in the ground plane. If you have to use them, put them in the +V plane.
- When making through holes for 100-mil-center-spacing leads in the plane, place a small trace between each pin. Breaking up the plane with a row of holes is much better than having a long slot (see C and D in Figure 5).
- When splitting up the ground plane to make, for example, a digital and power ground, make sure that the signals connected to the microcomputer are still located entirely over the digital ground. Extending signal traces beyond the power ground hurts because the power ground does not work to reduce the loop area for digital noise signals.



Ground Plane



- |  |  |
|--|--|
| <p><b>A</b> POOR – Buried trace cuts ground plane into two parts</p> <p><b>B</b> BETTER – Buried trace around the perimeter<br/>Best solution is no trace at all in the ground plane</p> | <p><b>C</b> POOR – Slot formed by 100-mil spacing cuts up ground plane and focuses slot antenna radiation into that connection</p> <p><b>D</b> BETTER – Ground plane extends between 100-mil centers</p> |
|--|--|

**Figure 5. Layout Considerations**

## 2.2 Power Distribution for Two-Layer Boards

### 2.2.1 Single-Point vs Multipoint Distribution

In a true single-point power-distribution system, each active component has its own separate power and ground, and these traces would remain separate until they meet at a single reference point. In multipoint systems, the connections are made in a daisy-chain fashion, so there are multiple 0-V reference points. It is clear that multipoint systems have the potential for common impedance coupling. While implementing a single-point system may be impossible, a combination of single point for devices generating RF and multipoint for everything else serves to reduce noise. The best scheme possible has a single point that ties together the regulator ground, microcomputer ground, battery negative, and chassis or shield (see Figure 6).

### 2.2.2 Star Distribution

Star distribution is much like single point. It looks like all points reference the same fixed point, which is located centrally, by about the same length of traces. Additionally, that same reference point may be attached, via a large single trace, to its source, which is not centrally located. Therefore, the major differences to single point are:

- The single reference point on a star can be a longer trace, instead of a point
- The point where the separate traces begin is near the center of the board, and each trace goes in its own direction, with the resulting trace length equal to that of all the others.
- The star is best applied to something like a system clock in a high-speed computer board. The signal originates on the edge connector and proceeds to the center of the board, where it then splits and goes to each place it is needed. Since it effectively originates at the center of the board, the delay in the signal from one area of the board to another is minimal. The name star sometimes is used to refer to single point, making the above clarification necessary.

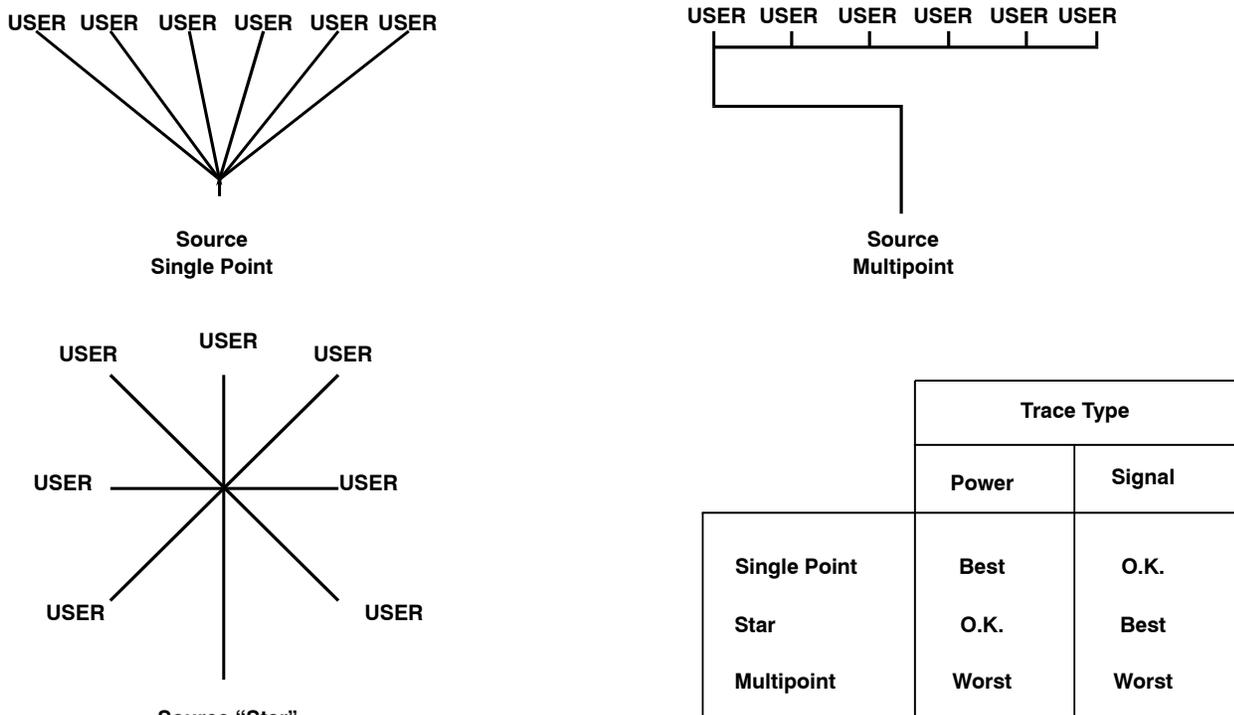


Figure 6. Power Distribution

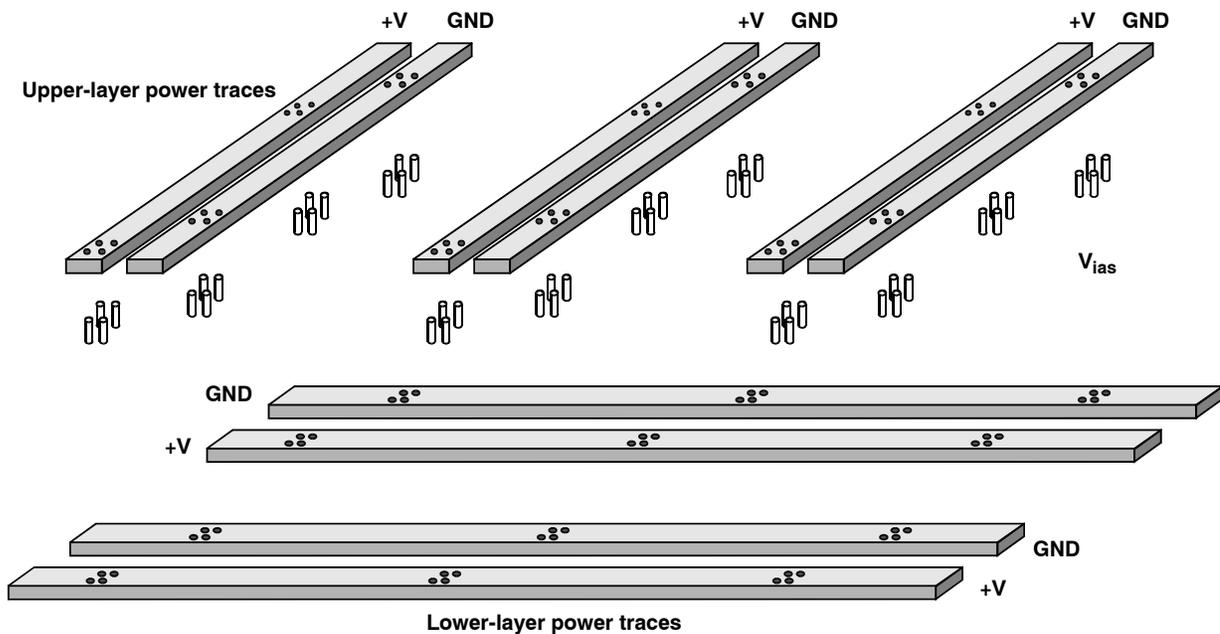
### 2.2.3 Gridding to Create Planes

Gridding is the most critical design technique for two-layer boards. Much like a power utility grid, gridding is a network of orthogonal connections between traces carrying ground. It effectively creates a ground plane, which provides the same noise reduction as on four-layer boards. It serves two purposes:

- Emulates the ground plane of a four-layer board by providing a ground return path under each of the signal traces
- Lowers the impedance between the microcomputer and the voltage regulation

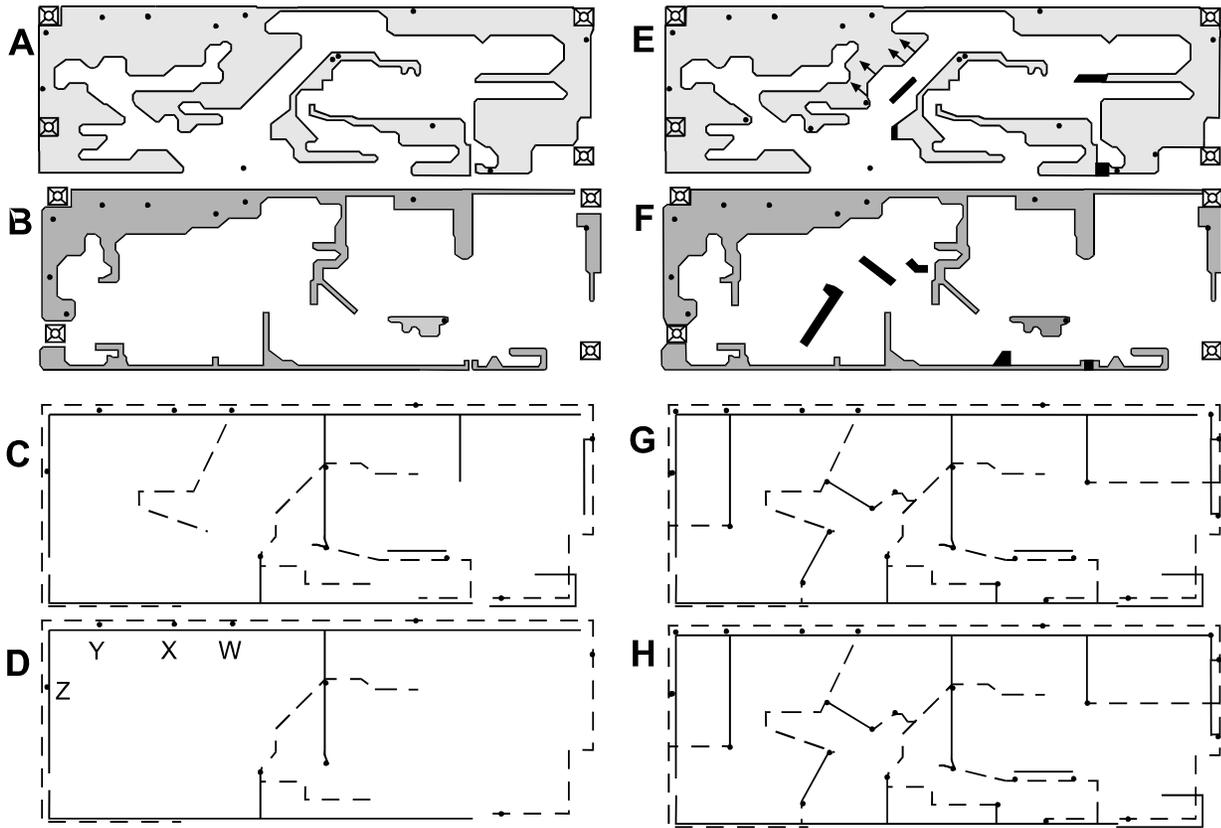
Gridding is done by expanding any ground traces and using ground-fill patterns to create a network of connections to ground across the PCB. For example, a PCB has most of the topside traces running vertically and most of the bottom traces running horizontally (see Figure 7). This already is working against having the return run directly under signal. First, every ground trace is expanded to fill up as much of the empty PCB space as possible. Then, all the remaining empty space is filled with ground. Place through holes where top-side traces cross bottom-side traces. Then do the same to the ground-fill patterns. Ground-fill patterns make a better contribution to the grid if they are tied to ground at both ends. A ground-fill-pattern geometry connected at only one point is just a ground shield, but if connected at two or more points, it becomes a conductor, and, therefore, becomes a contributor in the grid.

- Grid as much as possible on a two-layer board. Look for places where small changes in the layout would allow another connection to be made in the grid.
- Use as many through holes as can physically fit.
- Lines do not have to be orthogonal, or of the same width.



**Figure 7. Gridding Power Traces on Two-Layer Boards**

An example of gridding ground only to achieve the effect of a ground plane is shown in Figure 8. Note how the changes made in order to implement this were minor, indicating how a small effort can have a large payback.



**Figure 8. Gridding of Ground Fills and Traces to Form a Ground Plane**

In the example in Figure 8, A and B represent the top and bottom sides, respectively, of a simple two-layer board. The +V traces and all interconnects have been deleted, leaving only the ground fill and ground traces, along with the vias between the front and back. Figure 8C is a simple stick diagram of the ground routing for the board. Each stick, or leg, represents the path of the ground conductor, as if the conductor has been shrunk down to a minimum-width trace. The top-side traces are represented by the dashed line, and the bottom-side traces by the solid line. It is easy to see in this diagram that most traces are dead ends. Most traces are connected at only one end. In Figure 8D, most of the single-ended traces have been removed. The result is a sparsely connected pattern that represents how ground is routed over the entire board. Excluding points W, X, Y, and Z in Figure 8D, there is only one path between any two points anywhere on the routing.

In Figures 8E, 8F, 8G, and 8H, the design has been modified very slightly, to achieve a gridded ground. In Figures 8E and 8F, the addition of some traces, shown in solid black, and slightly moving some geometries, as indicated by the arrows, has created an extensive network of interconnections that creates the desired grid. This is shown by the stick diagram of ground in Figure 8G. Closing the gaps around the mounting holes also contributes to the network. No longer are whole traces connected at only one end. Now, they connect at both ends, and form a more complete conductor. Figure 8H shows the density of the grid, which contrasts to the openness of Figure 8D. Also, notice how, in Figure 8H, no traces are dropped because they connect only at one end. Only one trace has this problem, and it is part of a geometry already connected in three other locations. This interconnected network is the goal of gridding ground. The result is nearly as effective as an actual ground plane.

## 2.2.4 Bypassing and Ferrite Beads

Bypassing between the +V and ground at the microcomputer is critical because the intent is for the capacitance to supply the current used in the device for switching. If the current is not available in the bypassing loop, because of too much inductance, the laws of physics say that the current should come to the lowest impedance, which then is from the leads connecting to the power supply. The distributed capacitance of the power routing becomes the source for the higher frequencies. Thus, the ferrite bead blocks the sourcing of RF current from the power line connection, forcing the microcomputer to live off the current available inside the ferrite bead.

It is of the utmost importance to realize, and always keep in mind, that the power-routing purpose is only to replenish the charge in the bypassing capacitor, and that the bypassing capacitor should supply all currents at or above the oscillator frequency. Keeping RF off the power distribution traces is accomplished using these measures (see Figure 9):

- Use a ferrite bead and a bypassing capacitor ( $0.1\ \mu\text{F}$  or  $0.01\ \mu\text{F}$ ), placing the capacitors inside the ferrite bead. Place a  $1000\text{-pF}$  capacitor outside the ferrite bead, creating a PI filter. The ground connection for this capacitor should be the microground. However, if there is a lot of noise on this point, the capacitor could couple that noise back onto the +V line.
- The ferrite bead is used only on +V, not on ground. If a through-hole ferrite bead is used, it is mounted with the exposed lead connected to +V.
- Apply the 3:1 length-to-width rule for traces in the bypassing loop, to minimize impedance in this high-frequency path.
- Make the bypassing loops as small as possible in area and length. When tying the bypass capacitors for the oscillator or +V supply, try to extend the microcomputer ground rather than running a trace. Try to run any trace back over (or under) any other segment of the loop to reduce the radiating area when viewed from the top of the board.
- It is acceptable and beneficial to use ferrite beads and the same bypassing values on four-layer boards. The  $1000\text{-pF}$  capacitor may not be needed on four-layer boards, but it should be drawn in the initial design, and deleted later if screen-room testing shows that it is not needed.

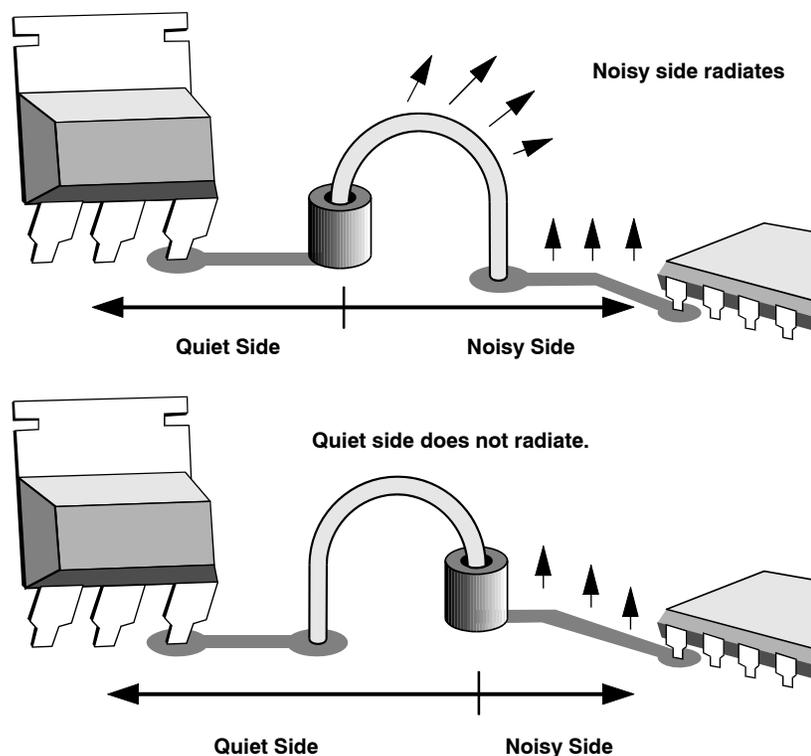


Figure 9. Ferrite-Bead Placement Closest to the Noise Source

### 2.2.5 Keeping Noise Close to the Chip

The following applies to pins that are used for simple digital I/O, not for pins used in the memory-expansion bus. The goal here is not so much to reduce the noise of the edge switching, but to mute the noise of the clock glitches when the pin is static.

Noise on the pins is coupled internal to the device through many paths that can change as the pin function changes. For example, the input pin in a keyboard scan has capacitively coupled noise from both the substrate and the power rails. Also, because it is high impedance, any ambient fields couple efficiently. When the key is pushed, the pin has a new set of noise sources because the signal line's impedance has changed. Thus, it is difficult to effectively develop a matrix of all possibilities; therefore, the following is recommended:

- Put a 50 –100- $\Omega$  resistor in series with every output pin, and 35 – 50- $\Omega$  resistor on every input pin. If the system design calls for higher series resistance, use that value. Higher resistances are better for outputs, but usually do not improve characteristics of inputs. Place the resistor as close as possible to the microcomputer, overlapping the microcomputer ground if possible.
- Bypass any pin on the microcomputer to ground using a 1000-pF capacitor, provided the edge rate needed for the signal line is not faster than 100 ns. On outputs and pins that the system uses for both input and output, ground for the capacitor should be the microcomputer ground. The other end of the capacitor should be tied to the receiver side, not the microcomputer side, of the series resistor. Placing the capacitor inside the resistor makes the load seen by the microcomputer look like a short when it switches, which is not desirable. If adding the capacitor has to be traded off against placing the series resistor, because of space limitations, place only the resistor.
- On pins used for input only, place the capacitor inside, on the microcomputer side, of the resistor to reduce the loop area. Then, high frequencies originating in the microcomputer on the pin see less impedance to ground through the capacitor than through the resistor.
- Resets and interrupts are special functions, thus care must be taken not to reduce functionality.
- Do not apply any of the above remedies to oscillator pins. If proper spacing between the oscillator components and other unrelated components and traces is maintained, there should not be a need for oscillator signal conditioning.
- Unused pins should be configured as inputs and tied directly to the microcomputer ground. It is recommended that the watchdog be enabled to correct the unlikely event in which a device is disturbed, loses its program counter, and executes code to make the input become an output with a high level.

These rules take up space and add components, and so are not well accepted in production. The goal is to implement all rules on all I/O pins, but if that is not possible, then rank order the candidates least likely to cause noise and remove the application of these rules one pin at a time.

Filtering priorities from most needed to least needed are:

- Signals leaving the enclosure (see section 3.3, *Cables and Bypassing to the Shield*)
- Signals leaving the PCB to other boards inside the enclosure
- Signals staying on the PCB with high-impedance loads (i.e., driving another MOS input or open circuit)
- Pins of parallel I/O port designed to support high-speed data transfer, e.g., between the microcomputer and an external memory, need filtering over the remaining I/O pins, because of their faster rise and fall times.

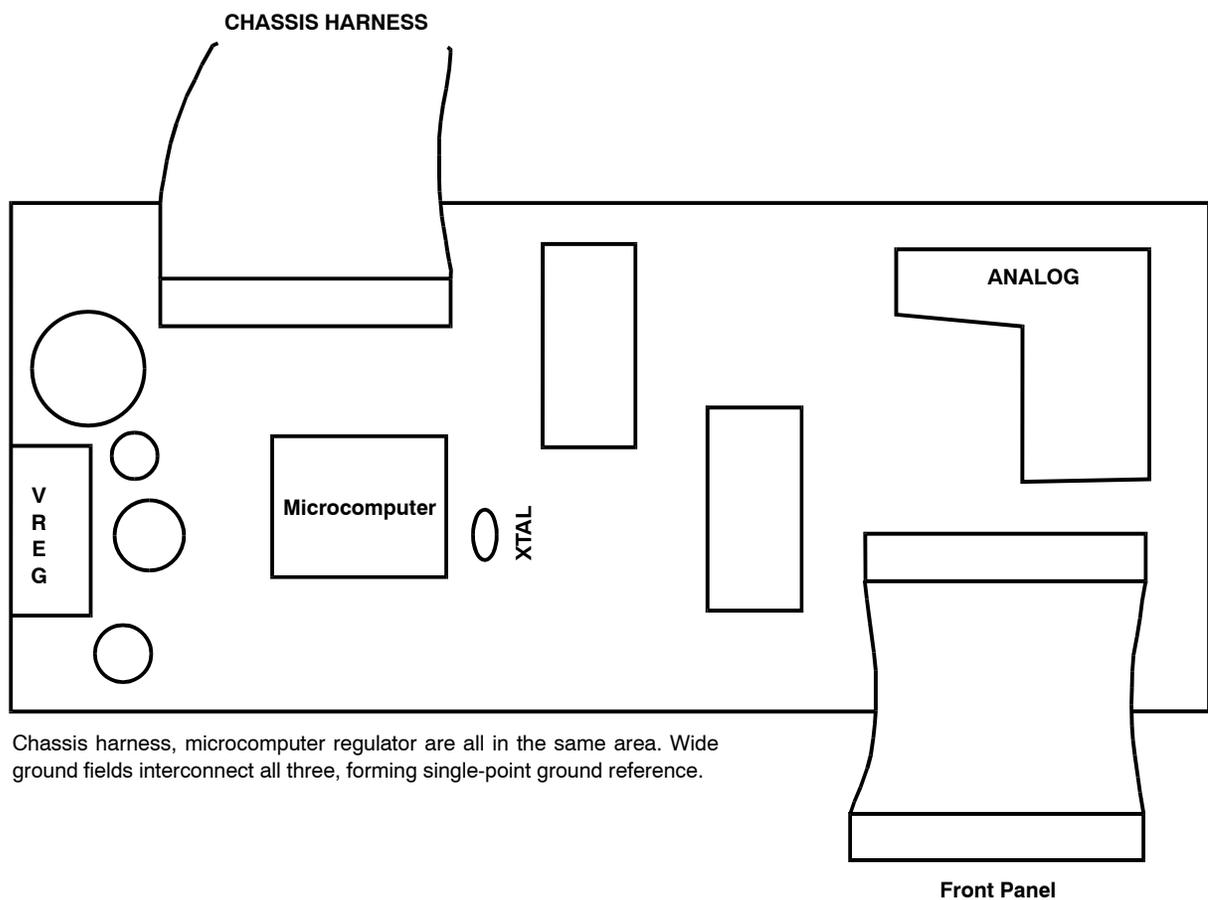
When the design is complete and first prototypes are built, an hour or two in the screen room removing each of the filtering components one at a time, identifies which are or are not needed to get the desired EMI level.

## 2.3 Board Zoning

Board zoning has the same basic meaning as board floor planning, which is the process of defining the general location of components on the blank PCB before drawing in any traces. Board zoning goes a little bit further in that it includes the process of placing like functions on a board in the same general area, as opposed to mixing them together (see Figure 10). High-speed logic, including micros, are placed close to the power supply, with slower components located farther away, and analog components even farther still. With this arrangement, the high-speed logic has less chance to pollute other signal traces. It is especially important that oscillator tank loops be located away from analog circuits, low-speed signals, and connectors. This applies both to the board, and the space inside the box containing the board. Do not design in cable assemblies that fold over the oscillator or the microcomputer after final assembly, because they can pick up noise and carry it elsewhere.

In prioritizing component placement, the most important things to do in PCB design are:

- Locate the microcomputer next to the voltage regulator, and the voltage regulator next to where  $V_{\text{Batt}}$  enters the board.
- Built a gridded or solid ground between the three (forming a single-point ground), and tie the shield at that point.



Chassis harness, microcomputer regulator are all in the same area. Wide ground fields interconnect all three, forming single-point ground reference.

Figure 10. Board Zoning

## 2.4 Signal Traces

### 2.4.1 Capacitive and Inductive Crosstalk

Capacitive and inductive crosstalk occur between traces that run parallel for even a short distance. In capacitive coupling, a rising edge on the source causes a rising edge on the victim. In inductive coupling, the voltage change on the victim is in the opposite direction as the changing edge on the source. Most instances of crosstalk are capacitive. The amount of noise on the victim is proportional to the parallel distance, the frequency, the amplitude of the voltage swing on the source, and the impedance of the victim, and inversely proportional to the separation distance. Measures that reduce crosstalk are:

- Keeping RF-noise-carrying traces that are connected to the microcomputer away from other signals so they do not pick up noise.
- Signals that may become victims of noise should have their return ground run underneath them, which serves to reduce their impedance, thus reducing the noise voltage and any radiating area.
- Never run noisy traces on the outside edge of the board.
- If possible, group a number of noisy traces together surrounded by ground traces.
- Keep non-noisy traces away from areas on the board where they could pick up noise, such as connectors, oscillator circuits, relays, and relay drivers.

Most EMI-related crosstalk problems center around the crystal, when the victim is located too close. No unrelated components should be closer than 1 inch to the crystal.

### 2.4.2 Antenna Factor Length Rules

Normally, for Federal Communication Commission (FCC) limits, trace length becomes important when it is greater than 1/10 of the wavelength. For military standard limits, that number becomes 1/20 to 1/30 of the wavelength. For automotive and consumer two-layer boards, 1/50 of the wavelength begins to be critical, particularly in unshielded applications. That says traces longer than 4 inches can be a problem for FM-band noise. In these cases, some form of termination is recommended to prevent ringing.

### 2.4.3 Series Termination, Transmission Lines

The main purpose of termination is to provide critical damping to achieve the highest possible data transmission rates with the least-possible overshoot. When applied to most microcontroller systems, however, the focus changes to taking out as much total differential-mode noise as possible while allowing system functionality. Below is a table of different methods of termination and the main characteristics of each method.

**Table 1. Termination Characteristics**

	PARALLEL	THEVENIN	SERIES	AC	ACTIVE
Power dissipation	high	high	low	medium	medium
Number of components	1	2	1	2	1
Adds delay	no	no	yes	no	no

Note that CMOS is an under-damped technology, which means that you always have to be on guard for ringing and overshoot. Use some form of termination if any of the following conditions are present:

- A signal trace is more than 1 foot long.
- A signal goes to a cable that leaves the shielded enclosure.
- Any ringing is present.

Series resistance is an inexpensive solution to termination and ringing problems, and is the preferred method for microcomputer-based systems where minimizing the differential-mode noise is also a concern.

## 2.4.4 Impedance Matching at Inputs

The input to a CMOS device looks like a series inductance of about 5 – 40 nH, which leads to about 5 pF in parallel, with about 5 M $\Omega$  to the grounded substrate (see Figure 11). This is a very high impedance, and can lead to lots of ringing and other noise if the device driving the input is not matched in some fashion to the higher impedance. This is the complement of the situation of section 2.4.3, where attention is paid to the microcomputer's output because of the under-damped nature of the load it drives. Here, the microcomputer is the under-damped load, and ringing and overshoot are real possibilities. More than likely, some form of termination will be required, and again, the series resistance is the most likely solution. Resistance placed at the driver increases the output impedance, as seen by the trace and the input pin, thus matching the high impedance of the input.

If the input is connected to an open trace, such as the open line to a switch, a pullup or pulldown resistor is recommended. While this increases the amount of current switched when the input is activated, it reduces the impedance at all other times. This reduces the trace's chances of being a victim of coupled noise.

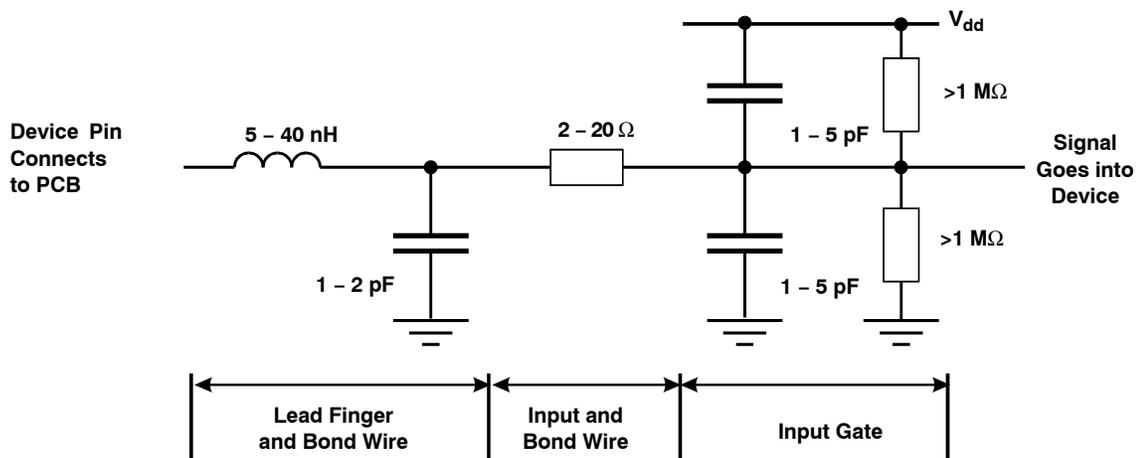


Figure 11. MOS Buffer Simplified Schematic

## 2.5 Cables and Connectors

A well-designed two-layer board, and most four-layer boards, have minimal radiation. The problem at the system level is the radiation due to cables interconnecting the PCB with any off-board support function, other processor, or display and keypad PCBs. Because usually there is only one ground wire between boards, that one inductive wire has to return all of the RF energy carried onto the second PCB by the other wires. If there is any impedance in the single ground wire, a portion of the RF energy does not return to the microcomputer's PCB via the ground wire, but rather through a radiated path. The energy radiates off the second board and couple back to the first, but, during the process, that radiation also can add noise in other locations in the system, as well as become direct radiation measured in the screen room. The key corrective action is to ensure the conducted path for the return has a very low RF impedance.

### 2.5.1 Differential-Mode and Common-Mode Noise

Common-mode noise is a big problem in cables, but the fault does not lie in the cable, it lies in the connections on the board that the signals and returns tie to that form the common impedance. Common-mode noise is corrected either at the source, by reducing the impedance of the common node, or reduced by placing a ferrite bead around the entire cable.

Differential-mode noise (the useful noise of an edge transition) should first be reduced to the maximum (slowest) allowable rise and fall times and should occur at only the minimum needed frequency. The noise radiated is due to the loop of the signal and its return. This loop is minimized by having as many returns as possible and by twisting each signal and return pair. The latter causes field cancellation at some distance away, in the same manner as routing power over ground.

### 2.5.2 Crosstalk Model

Crosstalk in a cable is the same as in the PCB. Noise is coupled from the source onto quiet victim signals. Therefore, run clocking or other high-speed wires twisted with their own separate return. Crosstalk is a problem in cables over 2-meters long, and can be a problem in cables as short as 6 inches.

### 2.5.3 Number of Returns

It is common practice in the computer industry to have at least one ground for every nine other signal lines in a cable or harness. With higher speeds, this ratio is moving toward 1:5. These higher speeds are not limited to data rates, but also to harmonic content. Use these guidelines in designing signal and return lines:

- The best practice is to have one ground return for each signal in the cable, as a twisted pair.
- Never run less than one ground return for every nine signal lines, even if it is just the jumper cable to the front-panel display in a completely sealed metal box.
- If the cable is over one foot long, it should have one ground return line for four signal lines.
- When possible, there should be a solid metal bracket, used as a mechanical brace, soldered between the two boards, to serve as a mounting bracket and as a robust RF ground return.

### 2.5.4 I/O Recommendations for Off-PCB Signals

The PCB should have a large ground area tied to the enclosure shield that serves as the ground for the bypassing capacitors on each of the wires entering or leaving the enclosure. These capacitors provide final filtering of microcomputer noise, but also are intended to filter to the shield any noise picked up on the cable outside the box. See section 3.3, *Cables and Bypassing to the Shield*.

### 2.5.5 Keeping Noise and Electrostatic Discharge (ESD) Out

Noise and ESD incident on the cable are intended to pass through the bypass capacitor at the cable on the PCB and out to the shield (chassis). Therefore, the ground from the capacitor to shield should be wide (3:1) and bonded securely to the shield, preferably by two or more screws. The bypass capacitor value should be less than 1000 pF, so the effective series resistance (ESR) is minimum in the 50 – 500-MHz range. Lead length of axial devices would be a factor in the ESR, so surface-mount components are preferred.

## 2.6 Other Layout Issues

### 2.6.1 Front-Panel PCB with Keypad and Display in Automotive and Consumer Applications

In multi-PCB applications, a front-panel PCB, which carries the display and the keyboard, is part of the shielding enclosure. It also can be a source of emissions. The goal here is to make the ground return for the noise of the microcomputer, and to create an effective extension of the shield over the front of the box. This can be done by defining all lines on one side of the board to run one way, and the other side to run at 90 degrees (see Figure 12). Then, interspersed among the signals for keyboard and matrix, are the lines that make up two separate gridded ground planes: one that serves as the ground return and one that serves as part of the shield. The latter should securely contact the chassis at each corner and every two inches along the edge. The return ground plane should tie to the microcomputer's ground plane, preferably using something heavy, like soldered-in metal braces. This prevents the impedance between the controller and the front-panel PCB from being a major problem.

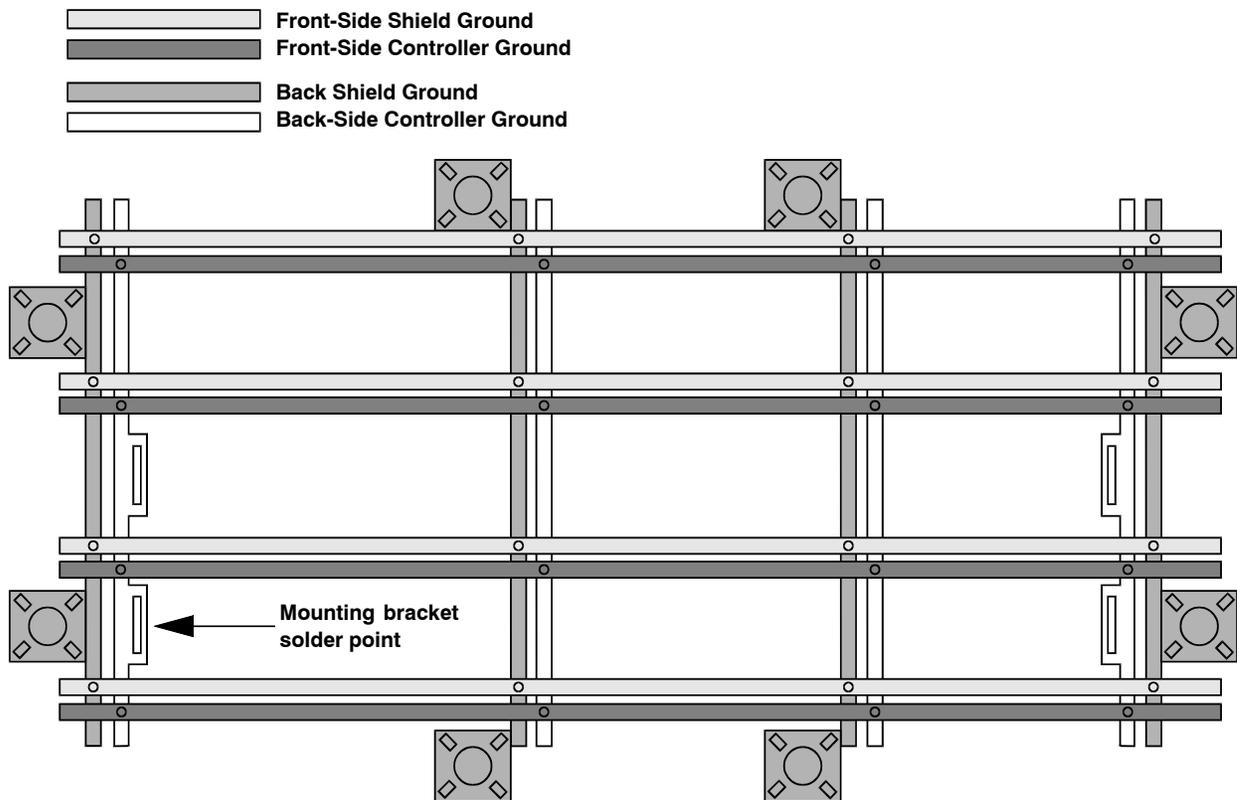


Figure 12. Front-Panel Gridding to Form Two Ground Planes

### 2.6.2 Layout for Susceptibility

Susceptibility (called immunity in Europe) occurs as incident electric or magnetic fields couple onto signal traces. Because the coupled signal is alternating current, the sine wave is superimposed on voltage already present on the trace. At the input to a microcomputer, that voltage is rectified, and causes a dc offset voltage on the pin. When this dc voltage gets large enough to shift the input away from the switching-point voltage, the intended switching function is no longer seen by the microcomputer. If the input is the oscillator, the device suddenly has no clocks. If the input is reset, the device may go into reset and stay there until the disturbing field is removed.

The physics of susceptibility are the same as for emissions, only applied in reverse. Large loop areas pick up more signal, just as they would radiate more signal. Therefore, the things you do to keep a signal immune from radiation are the same as those to keep it from radiating.

The most important pins for immunity are those that affect program control: the oscillator, reset, interrupts, and any input pins used for program branching. Apply the same rules as for reducing radiation from these pins. *By far, most susceptibility problems are associated with the loop defined by the oscillator pins, the crystal, the crystal bypass capacitors, and the path between the bypass-capacitor ground connection and the ground of the microcomputer.*

Also, be careful of ground bounce (common impedance coupling) of circuits that may generate these more critical signals. If the ground path has high impedance, it may cause the driving circuit's reference voltage to shift, causing that input to the microcomputer (RESET, OSC) to be outside the switching range of the microcomputer.

### 2.6.3 Autorouters

Autorouters for PCBs do not take any noise reduction actions; therefore, care should be taken in their use. Power and ground routing, as well as signals that impact susceptibility, should be laid out by hand. Any signal with clocked data, such as low address bits in a memory expansion bus, should be next. Only signals with switching rates below 50 kHz can be left safely to the autorouter. Even then, every signal should be checked for EMI issues. Routing near the crystal, and the crystal and tank circuit itself, should be checked. Finally, the ground traces should be gridded.

## **3 Shielding**

### **3.1 How It Works**

When an incident electric field traveling in the air hits a metal surface, the metal causes the penetrating field strength to decrease. The metal causes the field to be replaced with conduction currents that flow in the metal close to the surface. A very small (exponential decay) amount of the field does pass through, but for emissions, this is never a problem. The metal chassis serves as a shield. The fields from all the radiating surfaces inside it are blocked and kept inside the box, with the only noise coming from the cables or wires that enter or exit the box and from holes or slots made in the box.

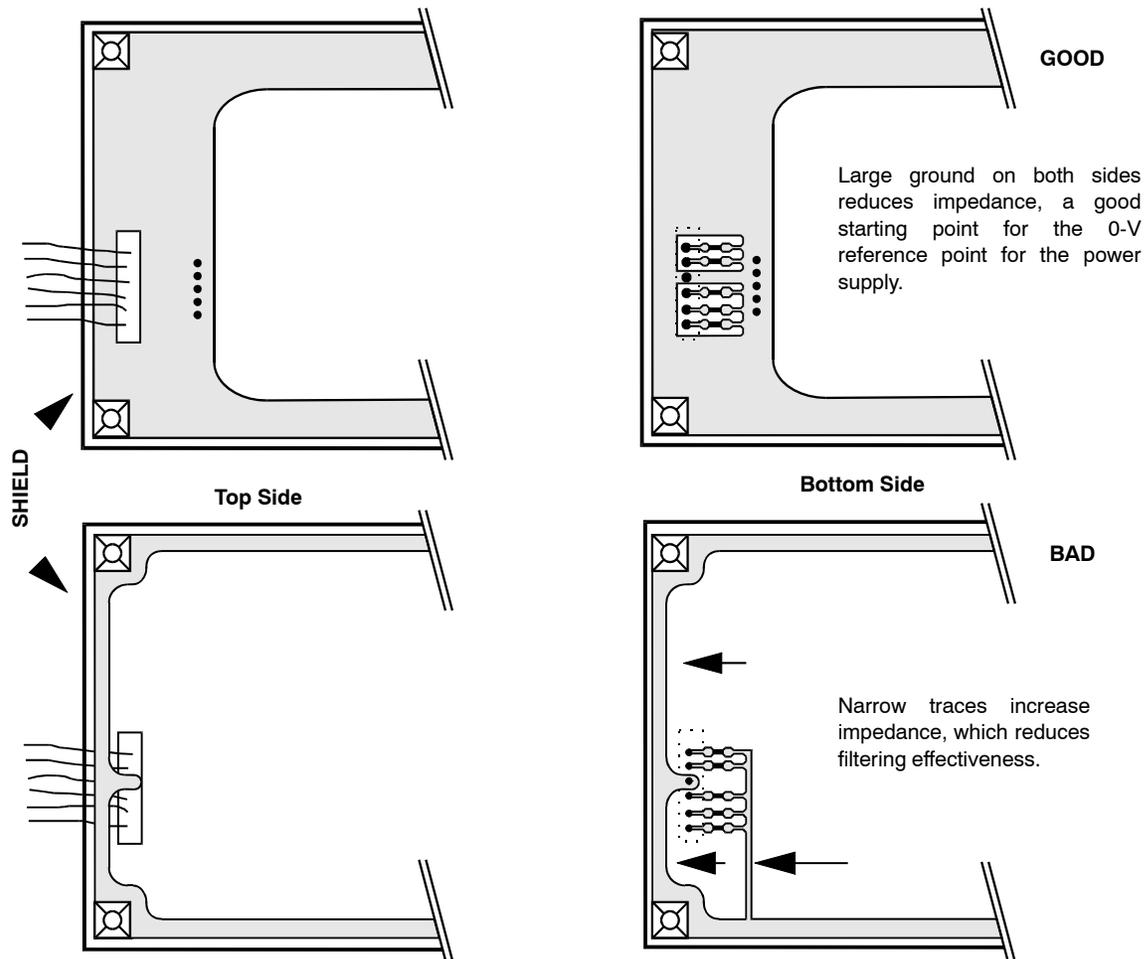
If a metal enclosure is to be used, its shielding effect should be utilized. However, it is always better to reduce the noise inside the box than to rely on the shielding effectiveness.

### **3.2 Grounding the Shield**

The shield has the difficult job of providing a terminating or conducting surface for direct ESD hits, ambient fields, and internal fields, as well as noise carried on the cables entering and exiting the chassis. To do this well, the shield should be thought of as an RF conducting plane, with the least number of breaks and impedance's between the source of the RF currents and the ground reference point. The ground reference point should be the single point, as mentioned earlier, that ties together the regulator ground, the microcomputer ground, and battery negative.

### **3.3 Cables and Bypassing to the Shield**

The PCB should have a large separate ground area tied to the enclosure shield which serves as the ground for the I/O bypassing capacitors (see Figure 13). These capacitors provide final filtering of system noise, but also are intended to filter noise picked up on the cable outside the box. The value of the capacitor should be below 1000 pF, more likely about 470 pF. The connection to the chassis is an RF path requiring 3:1 length to width.



**Figure 13. Mounting Filter Capacitors for External I/Os**

### 3.4 Slot Antennas: Cooling Slots and Seams

Slot antennas are formed by long thin gaps in the shielding material, such as at the seams between the two pieces of the box, and at the front-panel interface. These slots are very effective radiators. It is important that some form of contact assurance be used, such as dimpling, or using alternating fingers, to insure contact between the two surfaces. No slot should be more than 4 inches long. Cooling slots should not be used. For emissions reasons, only small round holes should be used if ventilation is needed.

## 4 Summary

The design of systems that generate low electromagnetic interference is not a mystery, but requires application of well-known engineering techniques. The design begins with the selection of semiconductor components that produce low electromagnetic radiation. However, in many cases, other criteria, such as the required performance of the semiconductor component, may be in contradiction with low interference. The main task is the design of a PCB that eliminates antennas that can radiate electromagnetic energy. Even if this can be achieved sometimes, large loops of signal and corresponding ground-return lines that carry high frequencies must be avoided. Therefore, a careful positioning of the integrated circuits is essential to achieve short interconnect lines.

In the next step, a close ground grid is placed over the printed circuit board. This grid ensures that return lines are close to the signal lines, thus keeping the effective antenna area small. A ground plane in a multilayer board provides this feature. By using this technique, low electromagnetic emission can be achieved with low design effort. However, some cost-sensitive applications allow two-layer PCBs only. Nevertheless, in this case, careful layout provides nearly the same performance as a multilayer board.

Finally, filtering of critical lines, such as the supply line, ensures that high-frequency currents do not leave the PCB.

By applying the rules presented in this report, shielding of the total system is not required. Experience and careful work by the design engineer are much more effective than sophisticated computer-aided design tools.

## 5 References

1. *Printed-Circuit-Board Layout for Improved Electromagnetic Compatibility*, October 1996, Application Report, literature number SDYA011.
2. *Electromagnetic Emission from Logic Circuits*, November 1998, Application Report, literature number SZZA007.
3. Texas Instruments Internet Web Page at <http://www.ti.com>



# ***Electromagnetic Emission From Logic Circuits***

SZZA007  
November 1999



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## Abstract

As a result of new legal requirements covering the electromagnetic compatibility of electronic equipment, users must now address this issue at system conception and when choosing components. This application report is intended to give the development engineer insight into a method of making the measurements that establish those properties of integrated circuits that primarily determine their electromagnetic compatibility. The report concludes with an examination of the results obtained with a variety of logic circuits.

## 1 Introduction

The electromagnetic compatibility of equipment and systems has taken on additional significance now that economic community (EC) regulations require the manufacturers of equipment to declare their compliance with electromagnetic compatibility requirements. One aspect of compatibility covers the interference immunity of the equipment, that is, the extent to which electromagnetic fields generated by external sources may influence the operation of the equipment. In this area, there has been intensive research over many years, and comprehensive literature is available to the design engineer that should answer any questions. The situation is very different with regard to the radiation of electromagnetic fields. Even though the obligation to label equipment as compliant specifically addresses this point, the legal situation basically has not changed, because the appropriate regulations covering radiation have been in force for several decades.

Manufacturers of semiconductors increasingly are being asked about the electromagnetic compatibility of components. Corresponding regulations basically concern only equipment and installations, but not the components they contain. Therefore, the engineer developing a piece of equipment is required to take appropriate measures to ensure compatibility. The manufacturer of semiconductors often can provide only limited help. Measures can, for example, be implemented by protective circuitry integrated into components, which should ensure that the components are not destroyed by an electrostatic discharge. Additional measures can reduce high-frequency interference generated by the components. Two parameters, in this case, are of considerable significance:

- Rise and fall times of signals at the output of the integrated circuit. The steepness of these edges determines, to a large extent, the energy radiated from the signal lines.
- High-frequency current flowing in the supply voltage of the integrated circuits that is the result of load changes inside the circuits

After a discussion of some general aspects of this problem, the measurement results obtained with a variety of logic circuits is shown. Generally, logic circuits cannot be considered to be model examples of low-interference components. Because of their applications in computers and similar equipment, particular care is taken during the development of such integrated circuits to achieve short propagation delay times, which produce rapidly rising and falling signal edges. Interference generated by these components is considered important only to the extent that, in a large system, they should not interfere with each other.

## 2 Propagation of Interference Generated by Integrated Circuits

Electrical energy is radiated by antennas that effectively are created by the conductors within and outside the integrated circuit.

The field strength, E, at a particular distance, r, from an antenna, A (see Figure 1), can be calculated:

$$E = k \times I \times A \times \frac{1}{r} \times \sin \vartheta \quad (1)$$

Where:

- E = Field strength
- I = Current
- A = Area of the antenna
- r = Distance to the antenna
- $\vartheta$  = Angle to the plane of antenna
- k = Antenna constant

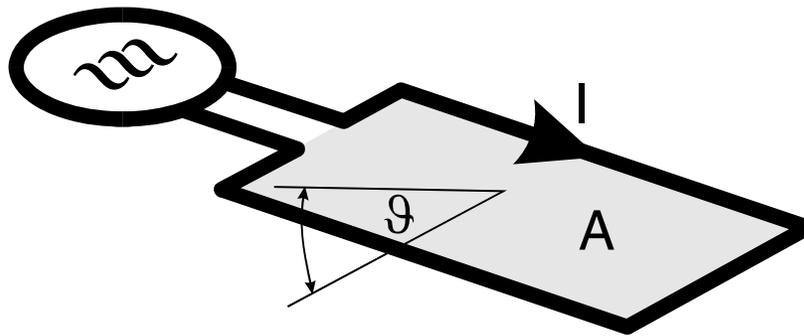


Figure 1. Radiation From an Antenna

In addition to the current that flows, the area of the antenna plays a major role in the field strength generated. In an integrated circuit, this area is bounded by the signal lines within and outside the component, as well as the associated return lines. In this context, connections to the supply voltage should not be overlooked because they conduct significant charging and discharging currents at every switching cycle. The area of the antenna that is formed by the conductors within the integrated circuit can, because of its small size, be disregarded in the frequency range below 1 GHz. The current loops, which are critical for the significant radiation, are shown in Figure 2.

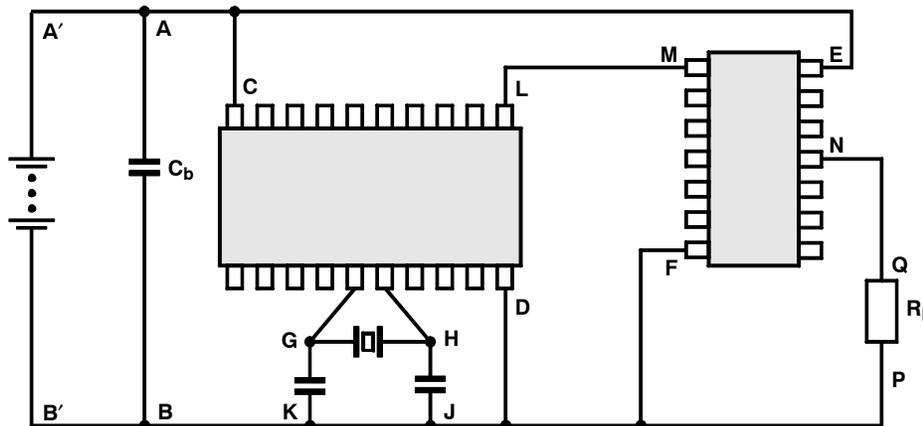


Figure 2. Current Loops on a Circuit Board

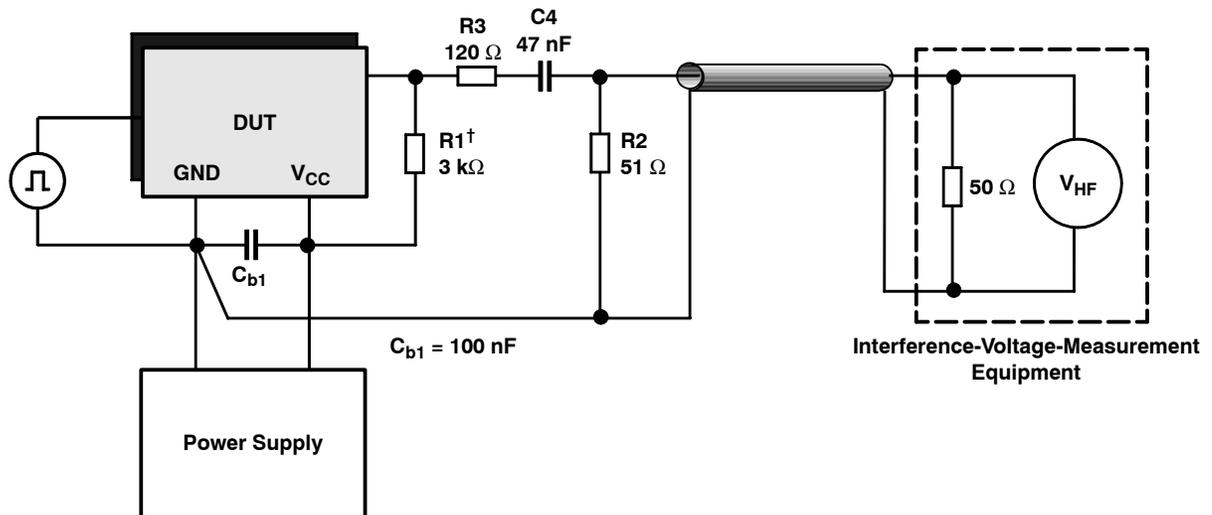
The signal line L-M, together with the associated return path F-D, forms one of the more important loops. The area that is enclosed by this loop operates as an antenna, and radiates high-frequency energy. An additional loop is formed by the positive supply lines A-C and A'-C, and the associated ground lines B-D and B'-D. Because blocking capacitors have only limited ability to equalize current changes in the circuit<sup>1</sup>, the design engineer must consider all supply lines as far as the power supply and, possibly, beyond to the mains transformer and mains power lines. In most cases, the power lines are the longest and, therefore, enclose the largest areas. The currents flowing there have a major influence on the electromagnetic compatibility of a system.

### 3 Measurement of Interference Generated by Integrated Circuits

The design engineer needs components that, as far as possible, generate little electromagnetic interference. Therefore, a measurement procedure that provides results with which the user can compare components from different manufacturers is necessary. As previously mentioned, the connections in a system behave as an antenna that radiates high-frequency interference. For this reason, the measurement procedure<sup>2</sup> developed by a working group from the Deutsche Elektrotechnische Kommission, or German Electrotechnical Commission (DKE), proposes measuring two parameters:

- Spectrum of the output signals of the integrated circuit. These signals are conducted into (and, to some extent, out of) the system over lines that may be long. Therefore, they make a significant contribution to the interference generated by the circuit.
- Spectrum of the supply current of the integrated circuit. Alternating currents of significant magnitude that result from load changes at the output of the circuit, and also from switching processes within the component, flow along the supply-voltage connections. The supply lines also are taken out of the system. The length, i.e., large antenna area, of these lines makes the interference generated from the supply lines increasingly evident.

Figure 3 shows the setup for measuring the spectrum of the output signal of the circuit under examination. In this arrangement, the circuit is driven in a manner typical of its normal operation. The measurement results were obtained by examining bus-interface circuits. These components do not have their own clock generator; therefore, a generator having a frequency of  $f = 1$  MHz controls the device under test (DUT). The integrated circuit is loaded at its output with an equivalent approximate  $150\text{-}\Omega$  resistance. This value is in accordance with the characteristic impedance of lines in the cable harnesses in vehicles. In many cases, this load does not represent the situation in the user's circuit. However, the arrangement chosen does allow for a comparative measurement of various circuits, for example, different logic families. The load resistance consists of a voltage divider, R2 and R3, and the input resistance of the interference-voltage-measuring equipment connected by a coaxial cable. To avoid excessive direct currents at the output of the DUT, an additional capacitor, C4, is provided in the output circuit. With circuits that have an open-collector output, an additional pullup resistor, R1, must be included.

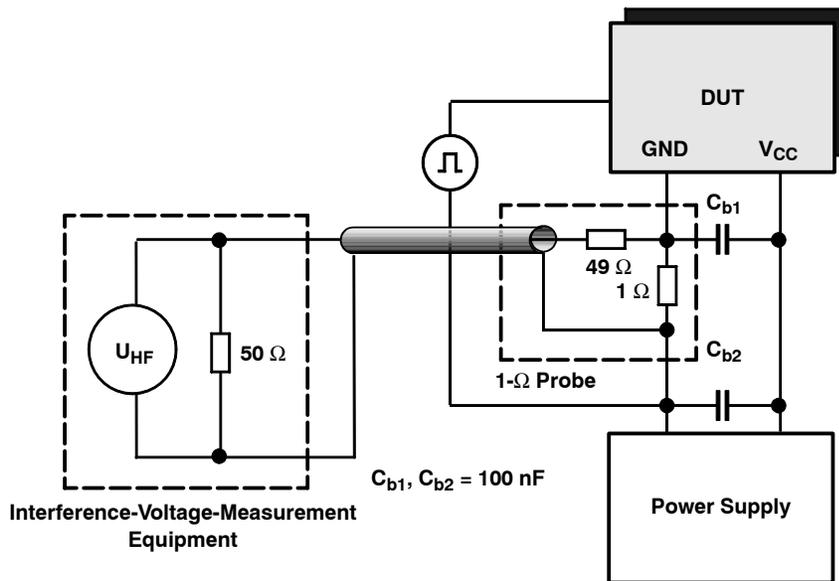


† For devices with open-collector (open-drain) outputs only

**Figure 3. Measurement of the Frequency Spectrum Generated at the Output of a Circuit**

As mentioned previously, the supply-voltage connections of an integrated circuit are a supreme source of high-frequency interference voltages and currents. Because of the switching processes that occur inside the devices, these currents often are greater than currents in the load to which they are connected.

Supply currents can be measured in various ways. One method is to use one of the well-known clamp-on current probes, which must have sufficient bandwidth. Apart from the high cost of such current probes, their mechanical dimensions are a disadvantage. At very high frequencies that must be measured precisely, the comparatively long connection lines and, hence, high inductances that result, make it almost impossible to obtain meaningful measurements. With fast digital circuits, large inductances in the connection lines put into question the function of the device under test or, at least, affect it negatively. Therefore, when the measurement specification was developed, the decision was made to measure the supply current by means of the voltage drop across a  $1\text{-}\Omega$  resistor inserted in the ground connection to the device being tested. For this purpose, a special test probe with an input resistance of  $1\text{-}\Omega$  was developed (see Figure 4). The measured voltage drop is then taken via a  $49\text{-}\Omega$  resistor and a coaxial cable to the interference-voltage-measuring equipment. Tests have shown that an arrangement such as this can be used successfully at frequencies above  $1\text{ GHz}$ .



**Figure 4. Measurement of the Supply Current**

The measurement procedure described herein preferably should measure currents and voltages delivered by the integrated circuit to the lines that follow it and, thus, radiated from the antennas that the lines form. All currents that flow only between the integrated circuit and the closely adjacent blocking capacitor can, therefore, be ignored. If the antenna area remains sufficiently small, significant radiation is not expected. For this reason, when developing the measurement setup, steps should be taken to reduce the interference caused by the device that is being tested. Of particular importance are the blocking capacitors, which must be used with logic circuits to ensure reliable operation of the circuit. As shown in Figure 4, the current of interest is measured only after the capacitor  $C_{b1}$ .

## 4 Measurement of Digital Signals and Current Spikes

### 4.1 Equipment

The equipment listed below was used to obtain the results discussed in the following sections:

- Spectrum Analyzer (Rhode & Schwarz Type FSEA), with the following settings:
  - Frequency range = 1–500 MHz
  - Resolution bandwidth = 10 kHz
  - Video bandwidth = 10 kHz
- Oscilloscope (Tektronix Type TDS744)
- AC Performance Test Board<sup>3</sup>
- 1- $\Omega$  Test Probe (Elditest Electronic Type GE4010)

### 4.2 Spectrum of Digital Signals

When measuring the frequency spectrum of the output signals of the integrated circuits, together with the spectrum of the supply current, the basic waveforms shown in Figure 5 are found. The frequency  $f_1$  is determined by the repetition frequency of the signal that is being measured. For these measurements, the bus-interface circuits were controlled at their inputs with a frequency of 1 MHz. This frequency was chosen at random. In contrast with microprocessors, which are usually driven at a specific clock frequency, the operating frequency used for logic circuits depends mainly on their particular application. The clock frequency of the processor higher up in the hierarchy of the system obviously also plays a part in such cases. The location of the component in the application is equally important. Thus, high frequencies are found on the system bus with backplane wiring. In the peripheral applications of a system, the operating frequencies usually are one or two orders of magnitude lower.

Above the frequency  $f_1$ , the amplitude of the harmonics reduces at 20 dB/decade up to a frequency  $f_2$ , which is determined by the rise and fall time,  $t_r$ , of the measured signal. The following relationship then applies:

$$f_2 = \frac{1}{\pi \times t_r} \quad (2)$$

Above the frequency  $f_2$ , the amplitude of the harmonics reduces at 40 dB/decade and produces the waveform shown in Figure 5.

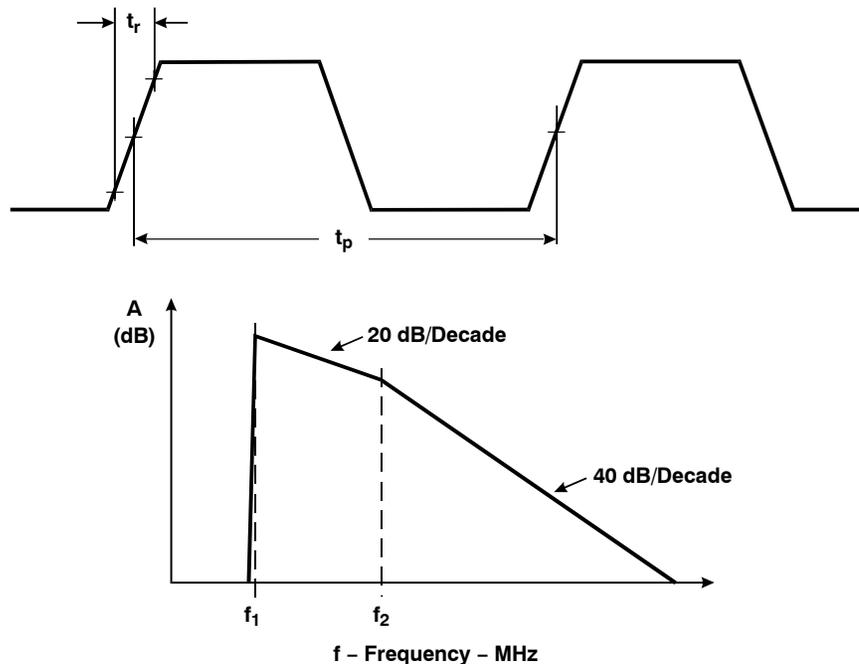


Figure 5. Spectrum of a Digital Signal

During the development of a circuit intended to generate the lowest possible level of electromagnetic interference, and when choosing the integrated circuits to be used, attention must be paid to the following parameters:

- Amplitude of the output signal. A 30% reduction in the amplitude of the signal also reduces by 3 dB the amplitude of the harmonics that are generated. A logical and sensible step is, where possible, to change the circuit supply voltage from 5 V to 3 V.
- Rise time of the signal. With circuits having slow edges, the frequency  $f_2$  also is correspondingly reduced. This also results in a reduction of the harmonic interference that is generated. However, the design engineer is usually under certain constraints. A circuit that generates an output signal with slow edges also has a longer delay time. That is, 50% of the rise/fall time of the output signal is manifested as additional delay time. However, this situation gives rise to the general requirement that only those circuits should be used that are fast enough for the application in question, and not to use any components that are too fast. Apart from the higher cost of the latter, the extra expense for the screening is an additional factor to consider.
- Current spikes generated when switching push-pull (totem pole) outputs are an additional potential source of interference. For this reason, the frequency spectrum of the supply current is discussed. With the logic circuits under consideration, the result must be correctly interpreted relative to the application. At low loading levels, such as those presented by connections with a length of only a few centimeters, the contribution resulting from the current spikes predominates. With low-resistance loads, such as the 150  $\Omega$  used in the measurement setup or actual bus lines, this part can, to a large extent, be neglected. In such cases, the currents in supply lines that result from the charging and discharging of capacitive reactances instead become significant.

### 4.3 Spectrum of the Output Signal

The waveform in Figure 5 indicates the measurement results that can be expected.

The output of a CMOS circuit can, with some simplification, be represented as an ideal voltage source,  $V_{CC}$ , and an internal resistance,  $R_O$  (see Figure 6). This output resistor is then connected either to the supply voltage  $V_{CC}$  (output high) or to ground (output low). An output voltage,  $V_{out}$ , results, which depends on the load. The voltage is measured according to Figure 3 at the output of the voltage divider  $R_3/R_2$ ; this being connected (via a coaxial cable) to the interference-voltage-measuring equipment having an input resistance of  $R_m$ . The following expression applies for the voltage,  $V_m$ , which subsequently appears at the measuring equipment:

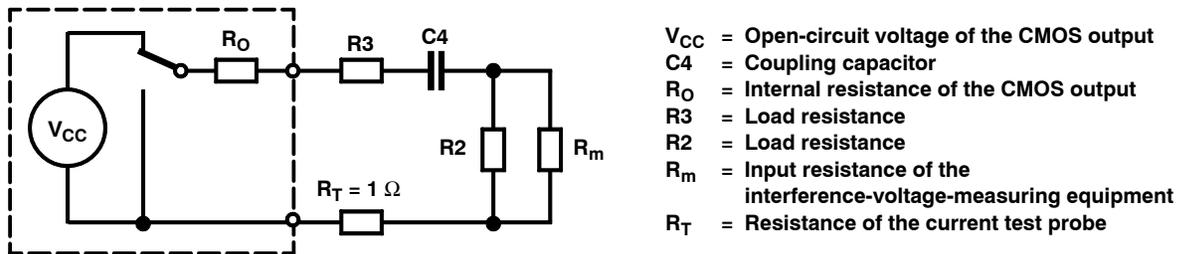


Figure 6. Equivalent Circuit of a CMOS Output Stage When Loaded by a Test Circuit

$$V_m = V_{CC} \times \frac{\frac{R_2 \times R_m}{R_2 + R_m}}{R_O + R_3 + \frac{R_2 \times R_m}{R_2 + R_m}} \quad (3)$$

In this case, the resistance of the probe ( $R_T$ ) is 1  $\Omega$ , and the impedance of coupling capacitor  $C_4$  can be disregarded. Assuming  $R_m = R_2 = 50 \Omega$ , the expression is simplified to:

$$V_m = V_{CC} \times \frac{R_2}{2 \times (R_O + R_3) + R_2} \quad (4)$$

The voltage  $V_m$ , which is to be measured, has a square waveform that is made up of an infinite number of sine-wave voltages with the following relationship:

$$V_m = V_{mpp} \left( \sin \omega t + \frac{\sin 3\omega t}{3} + \frac{\sin 5\omega t}{5} + \frac{\sin 7\omega t}{7} \Lambda \right) \quad (5)$$

Where:

$V_{mpp}$  = peak-to-peak voltage of the signal (with CMOS circuits, is the same as  $V_{CC}$ )

Because the interference-voltage-measuring equipment, for example, a spectrum analyzer, measures effective values, the above result must be corrected appropriately. The result is that the value of the voltage of the fundamental of the signal,  $V_{meff}$ , read from the interference-voltage-measuring equipment, is:

$$V_{meff} = 5 \text{ V} \times \frac{50 \Omega}{[2 \times (10 \Omega + 120 \Omega) + 50 \Omega] \times 2 \times \sqrt{2}} = 0.285 \text{ V} \quad (6)$$

The interference voltage is measured over a frequency range of several hundred megahertz; in this case, from 1 MHz to 500 MHz. The range of values of the measured voltages is also correspondingly large. To improve the readability of the curves, a logarithmic representation is used. The unit of measurement commonly used here is dB $\mu$ V. The value of  $V_{meff}$  must be converted using:

$$A = 20 \times \log \frac{V_{meff}}{1 \mu\text{V}} \quad (7)$$

For this example, the following value applies for the amplitude of the fundamental ( $f = 1 \text{ MHz}$ ):

$$A_{(1 \text{ MHz})} = 20 \times \log \frac{V_{meff(1 \text{ MHz})}}{1 \mu\text{V}} = 20 \times \log \frac{0.285 \text{ V}}{1 \mu\text{V}} = 109 \text{ dB}\mu\text{V} \quad (8)$$

The cutoff frequency,  $f_2$ , must be determined. The waveform at the output of an AC circuit is shown in Figure 7. The spectrum of the output signal of an AC circuit is shown in Figure 8.

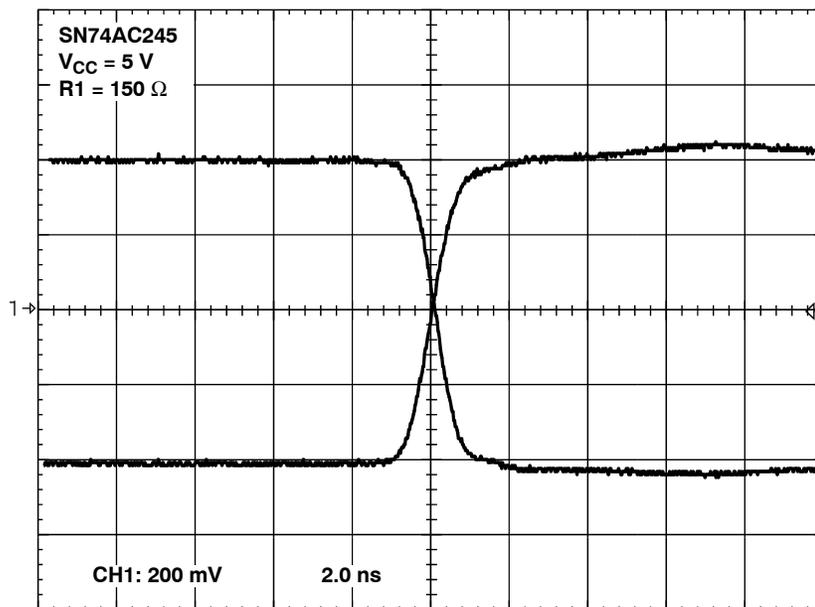
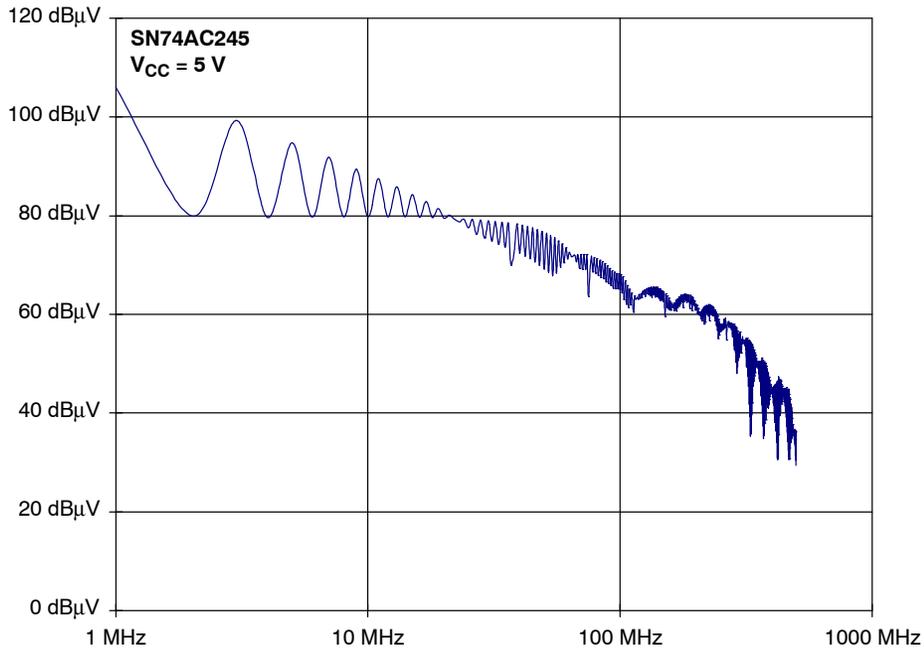


Figure 7. SN74AC245 Waveform at the Output of the Circuit ( $R1 = 150 \Omega$ )



**Figure 8. Spectrum of the Output Signal of an AC Circuit**

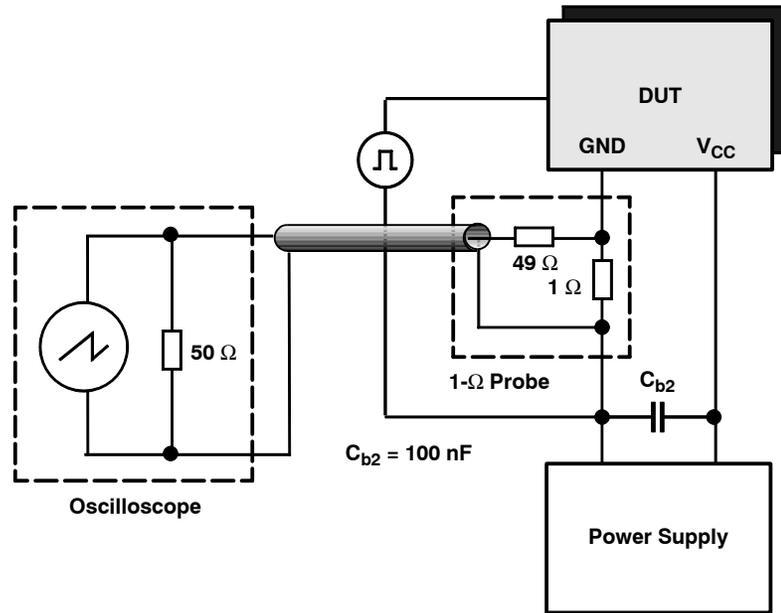
The rise and fall times of the signals at the outputs are about 1.5 ns:

$$f_2 = \frac{1}{t_{r/f} \times \pi} = \frac{1}{1.5 \text{ ns} \times \pi} = 200 \text{ MHz} \quad (9)$$

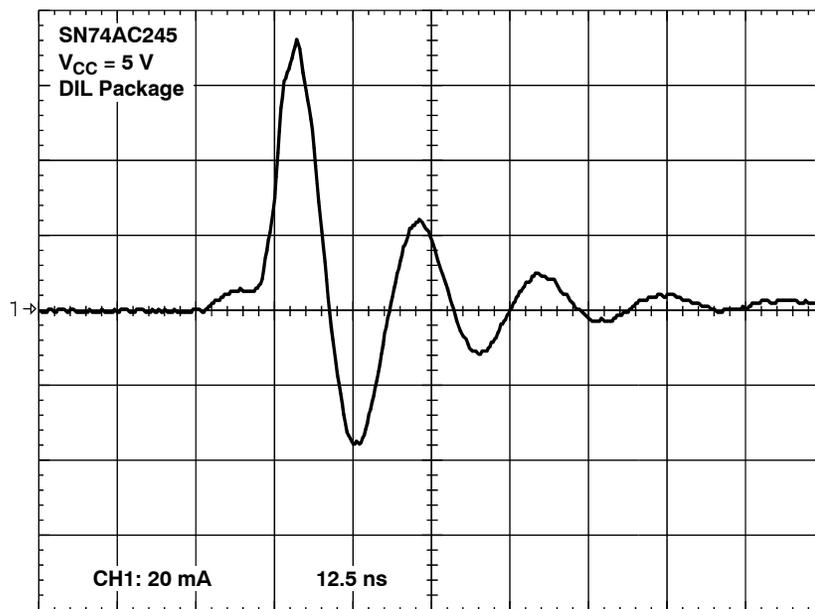
Up to  $f_2 = 200 \text{ MHz}$ , the amplitudes of the harmonics decrease at 20 dB/decade. Above this frequency, the attenuation is as expected, 40 dB/decade.

#### 4.4 Measurement of the Spectrum of the Supply Current

The frequency spectrum of the supply current can be determined in a similar way. The current in the ground connection depends on the switching processes occurring inside the integrated circuit and it depends on the load connected to the output of the circuit. The former contribution cannot be predicted without a detailed knowledge of the inside of the circuit, and must, therefore, be determined by measurements. The major contribution is from the so-called current spikes that result when switching the output from one state to the other. During the transition from one state to the other, both output transistors of the push-pull stage simultaneously are conducting for several nanoseconds. This results in an increased supply current. The amplitude of the current spikes can be determined by a setup as shown in Figure 9, very similar to that shown in Figure 4. However, the blocking capacitor  $C_{b1}$  shown in Figure 4, which would be parallel to the device being tested, is not included. As shown in Figures 10, 11, and 12, this capacitor greatly affects the amplitude and the waveform of these current spikes.



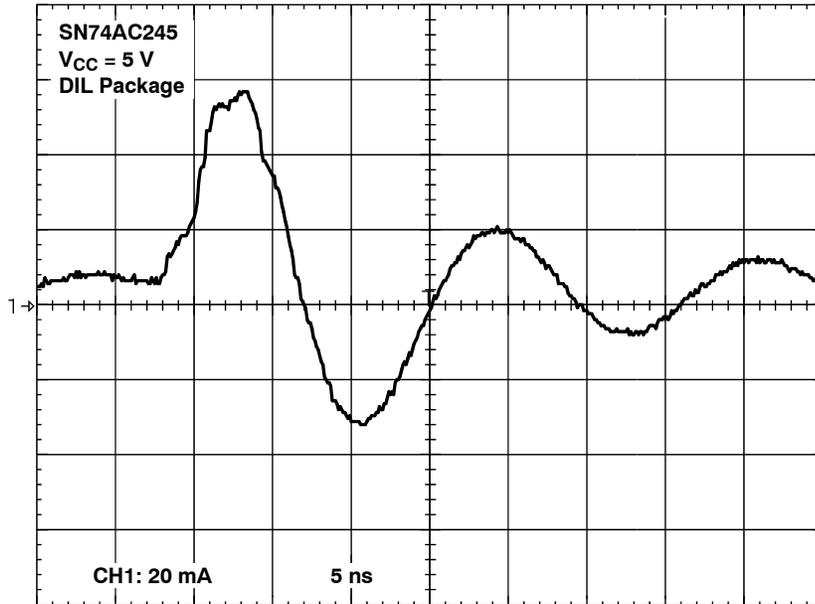
**Figure 9. Test Circuit for Determination of Current Spikes**



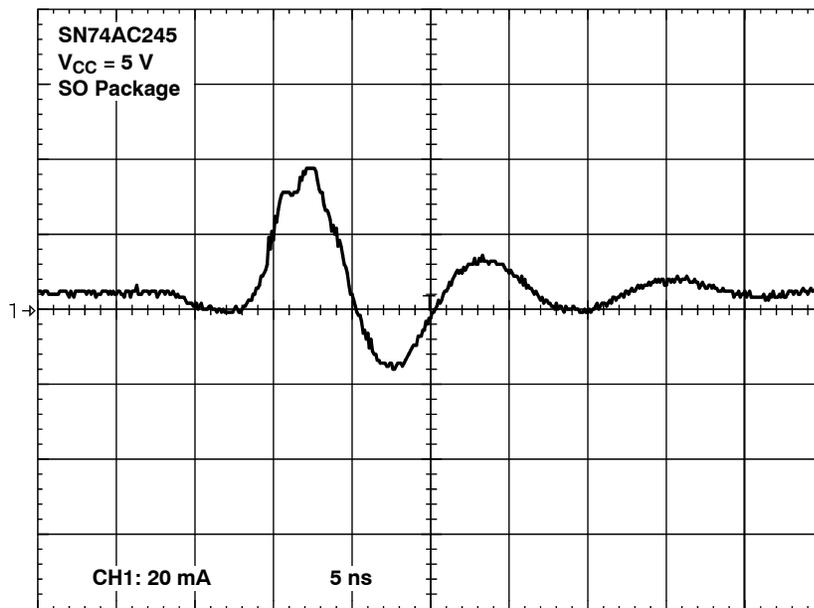
**Figure 10. SN74AC245 Current Spikes With Unloaded Output (DIL package)**

With the AC circuits being measured, the amplitude of the peak current is 70 mA (see Figure 10). Measurements have shown that the waveform and its amplitude are largely independent of the package type (DIL or SO) in which the semiconductor chip is encapsulated.

In practical applications, a blocking capacitor ( $C_{b1}$  in Figure 4) is found very close to the integrated circuit. One of its main jobs is to provide the energy required when switching over the load at the output. It also has a considerable influence on the amplitude of the high-frequency interference generated by the integrated circuit. The package construction of the integrated circuit plays an important part. With the smaller SO packages having correspondingly lower inductances, a current amplitude can be measured, which is about 30% lower than with the same chip in a DIL package. The lower inductances result naturally in a higher resonant frequency of the damped oscillations, as shown in Figures 11 and 12.

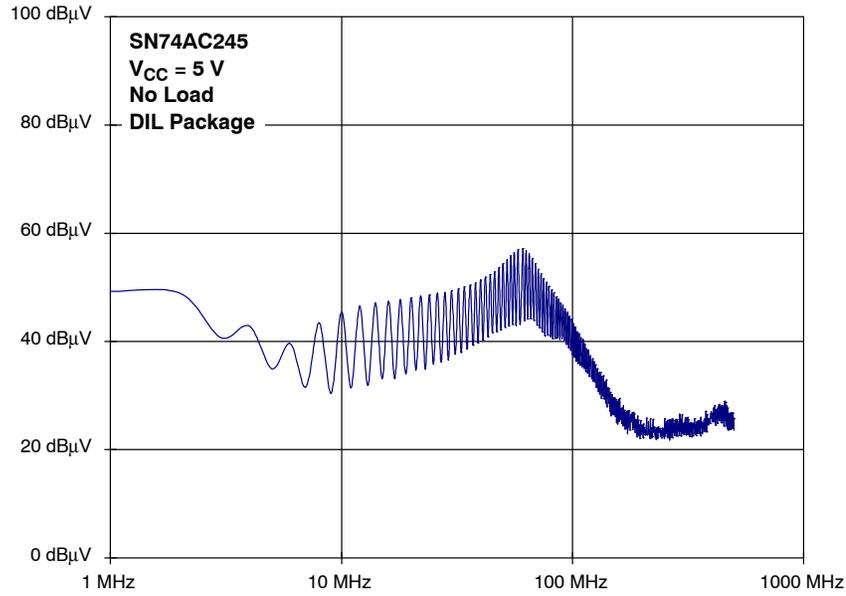


**Figure 11. Supply Current Spikes of an Unloaded AC Circuit (DIL package)**

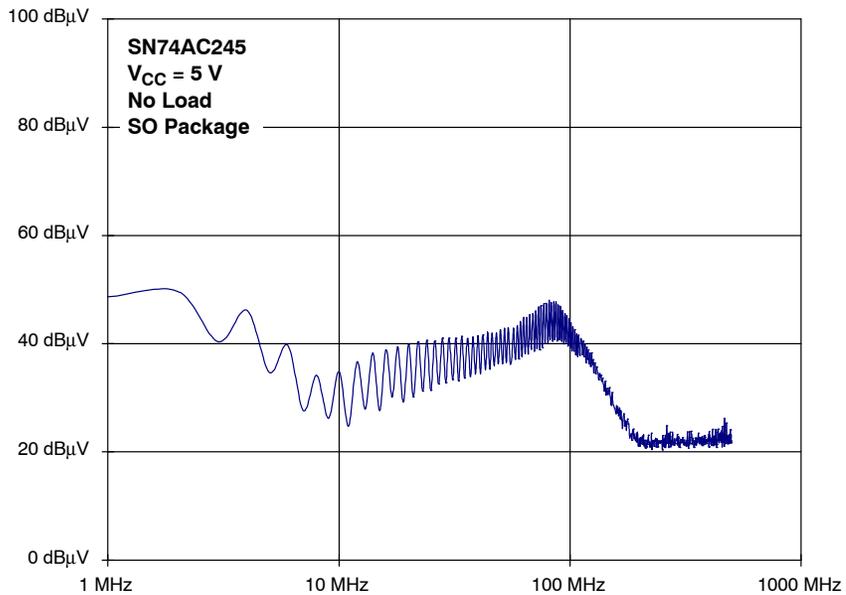


**Figure 12. Supply Current Spikes of an Unloaded AC Circuit (SO package)**

The differences in the behavior of packages become evident when measurements are made of the frequency spectrum of the currents, as previously discussed. With the chip in an SO package, the maximum value of the amplitude of the harmonics is at a frequency about 20 MHz higher than that in a DIL package. At the same time, the amplitude measured with SO packages is about 10 dB lower (see Figures 13 and 14).

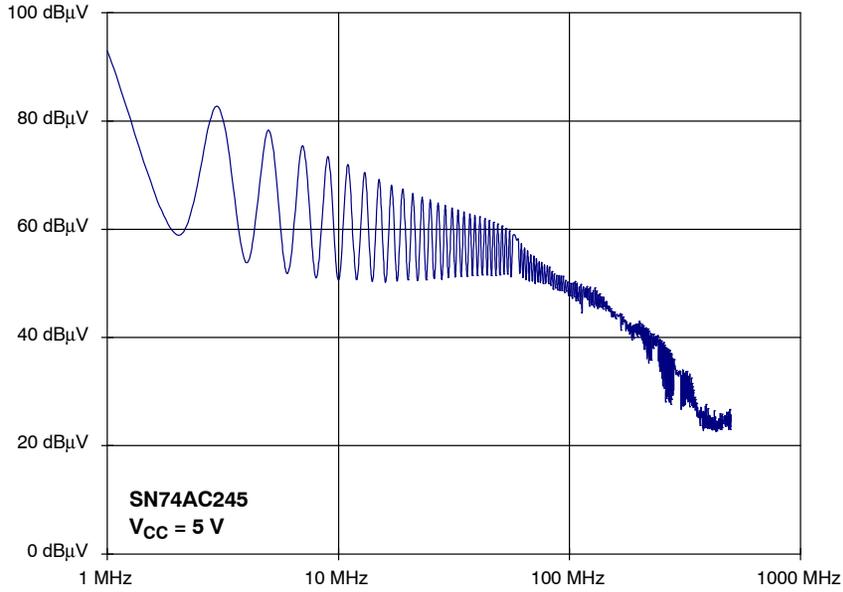


**Figure 13. Frequency Spectrum of the Supply Current of an Unloaded AC Circuit (DIL package)**



**Figure 14. Frequency Spectrum of the Supply Current of an Unloaded AC Circuit (SO package)**

In practical applications, the currents resulting from the load connected to the outputs outweigh the effects just described. Figure 15 shows the spectrum of the sum of the currents flowing in the ground line of an AC circuit. This, and all subsequent measurements, were made with integrated circuits in the DIL package. In this case, all eight outputs of the component switch simultaneously. A load consisting of  $R = 150 \Omega$  and  $C = 0.047 \mu\text{F}$  in series was connected to the outputs.



**Figure 15. Frequency Spectrum of the Supply Current of a Loaded AC Circuit**

The measurement results can be checked mathematically. The spectrum of the output signal was measured across a load resistance  $R_3 // R_m = 25 \Omega$ . For this measurement, the same load current also flows through the  $1\text{-}\Omega$  test probe. The resulting voltage drop,  $V_{\text{meff(GND)}}$ , is proportional to the ratio of the values of the resistors and must be multiplied by the number of simultaneously switching outputs. In addition, the voltage divider in the  $1\text{-}\Omega$  probe divides the measured voltage by a factor of 2. The result is:

$$V_{\text{meff(GND)}} = V_{\text{meff}} \times \frac{1 \Omega}{25 \Omega} \times \frac{n}{2} \quad (10)$$

If the voltage ratio  $(1/25) \times (n/2)$  is now calculated in dB as a unit of measurement, the required ratio  $A_{\text{(GND)}}$  is:

$$A_{\text{(GND)}} = 20 \times \log\left(\frac{1}{25} \times \frac{8}{2}\right) = -15.9 \text{ dB} \quad (11)$$

For low frequencies, the spectrum of the supply current can be determined directly from the frequency spectrum of the output signal. The current spikes become evident only at higher frequencies. The frequency spectrum of the supply current with loaded and unloaded outputs is shown in Section 5.

## 5 Measurement Results

### 5.1 SN74ABT245 Measurement Results

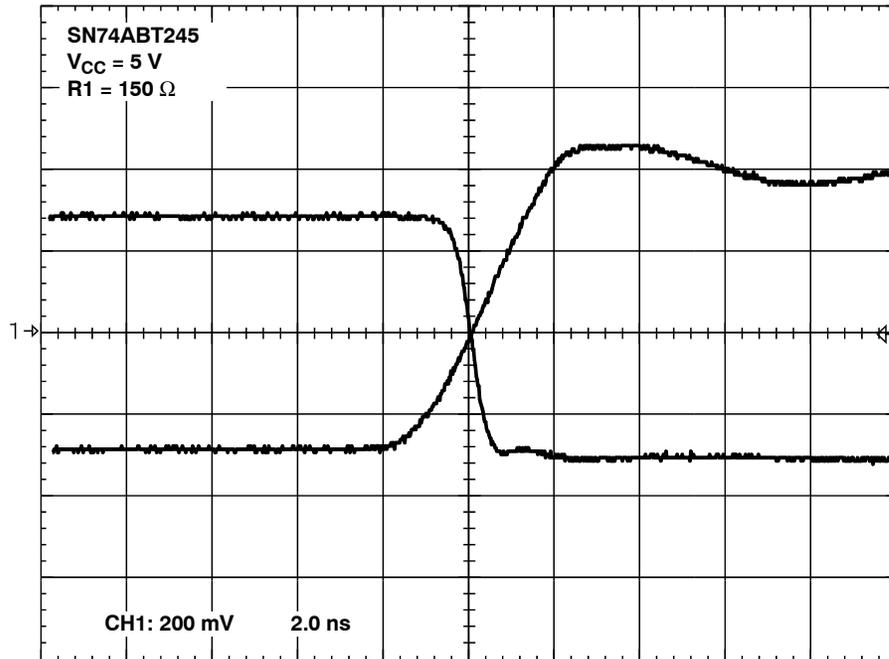


Figure 16. SN74ABT245 Waveform at the Output

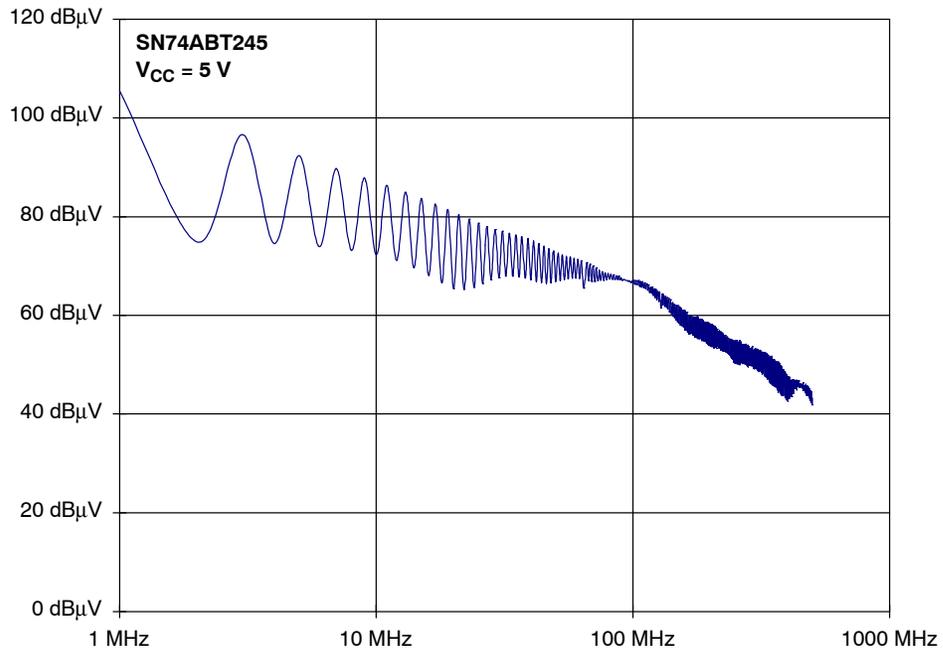
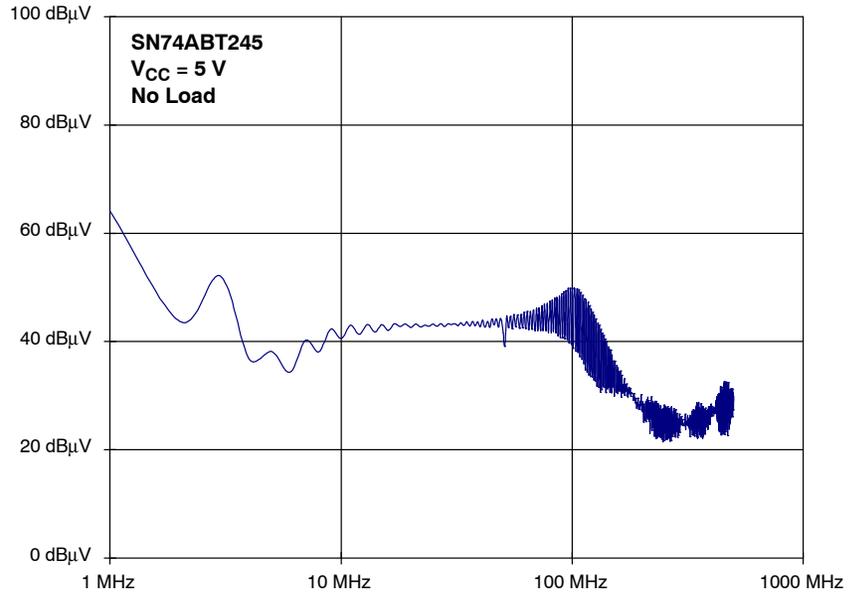
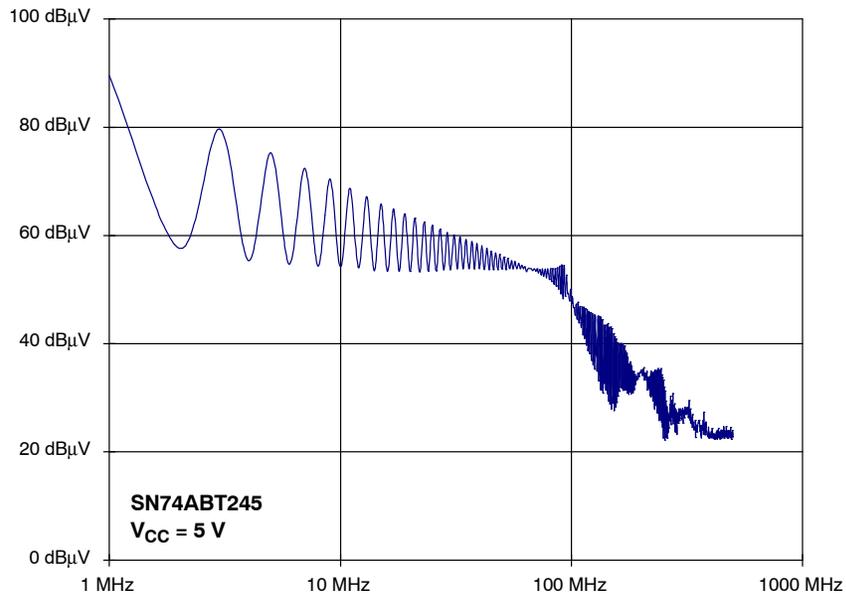


Figure 17. SN74ABT245 Spectrum of the Output Signal



**Figure 18. SN74ABT245 Spectrum of the Supply Current (output unloaded)**



**Figure 19. SN74ABT245 Spectrum of the Supply Current (output loaded)**

## 5.2 SN74ABT2245 Measurement Results

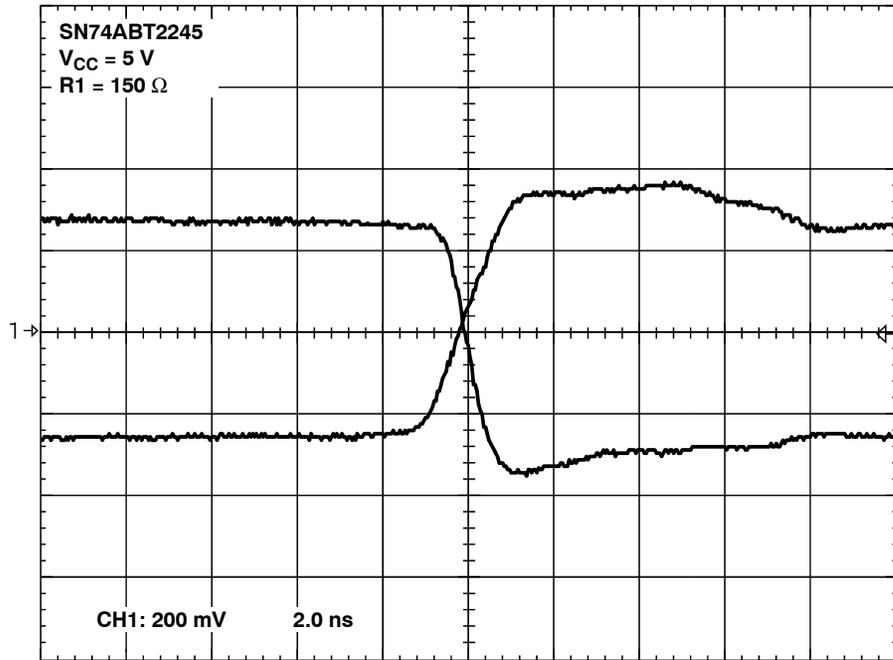


Figure 20. SN74ABT2245 Waveform at the Output

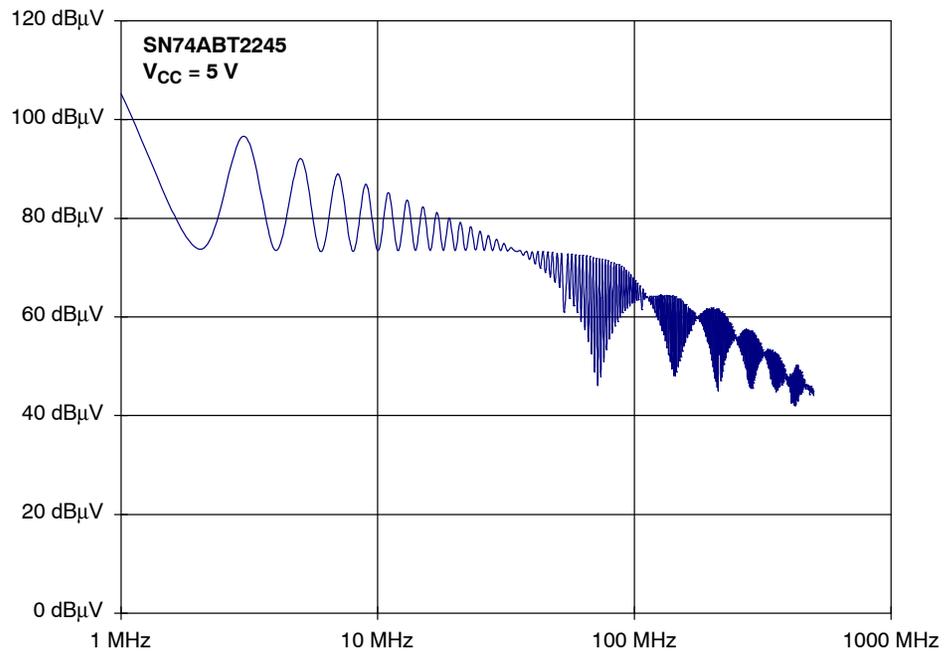
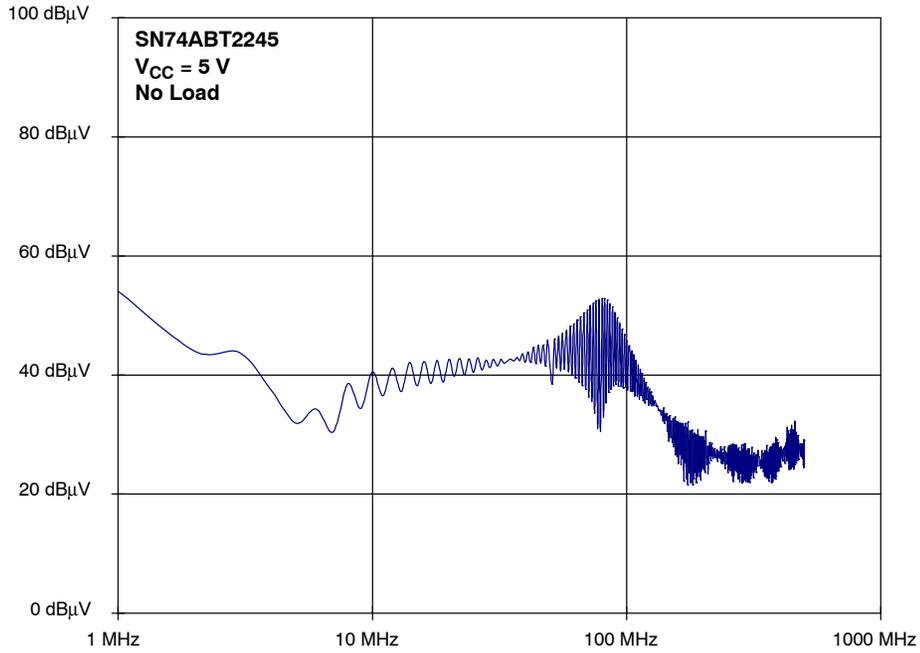
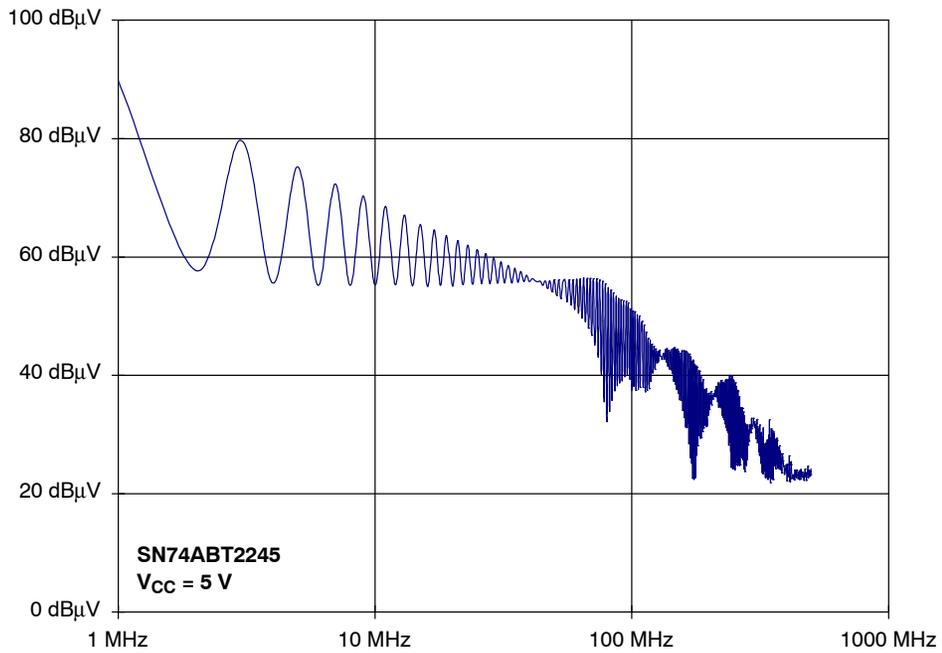


Figure 21. SN74ABT2245 Spectrum of the Output Signal



**Figure 22. SN74ABT2245 Spectrum of the Supply Current (output unloaded)**



**Figure 23. SN74ABT2245 Spectrum of the Supply Current (output loaded)**

### 5.3 SN74AC245 Measurement Results ( $V_{CC} = 5\text{ V}$ )

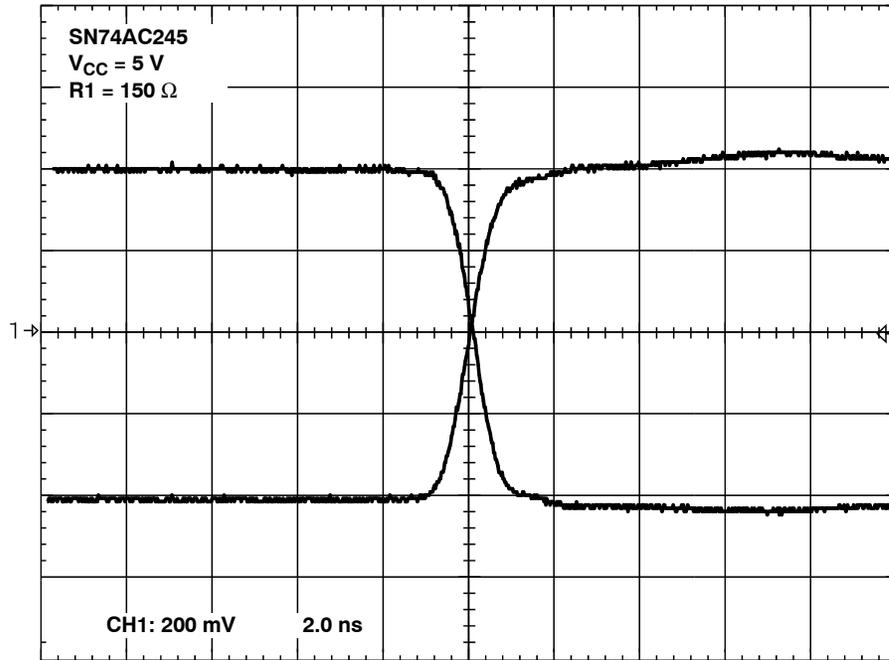


Figure 24. SN74AC245 Waveform at the Output

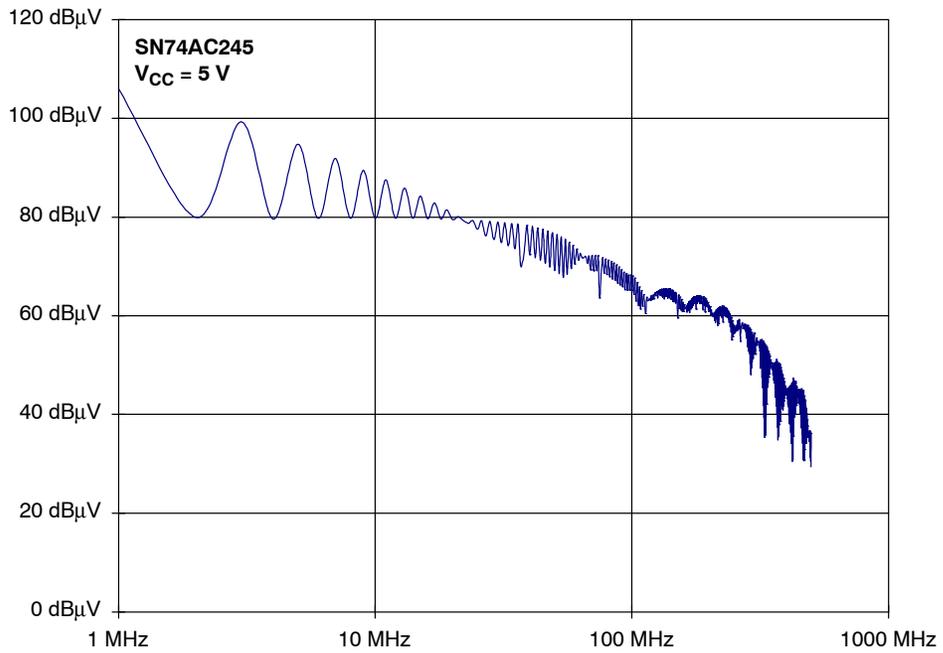
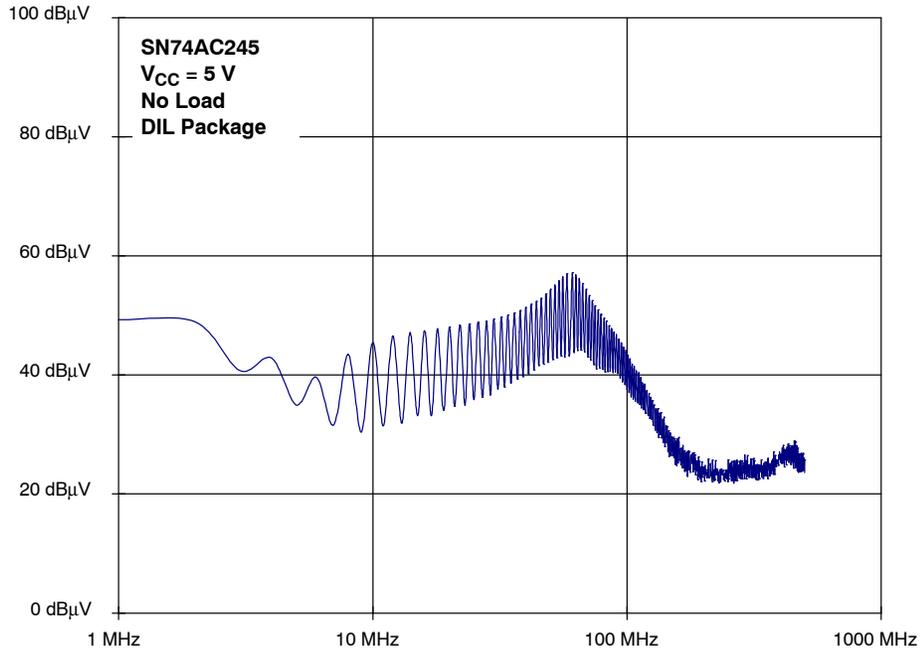
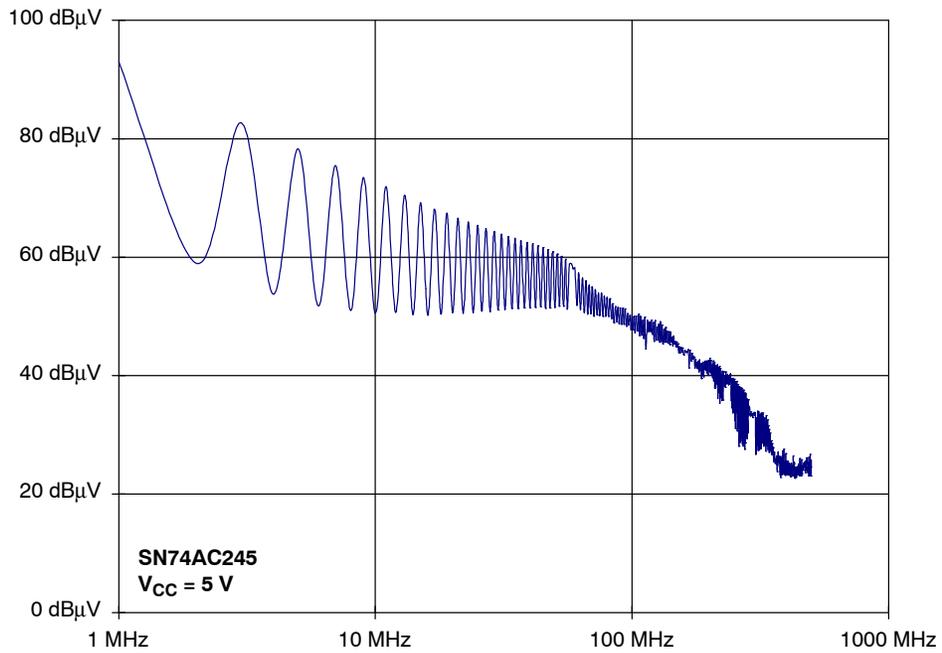


Figure 25. SN74AC245 Spectrum of the Output Signal



**Figure 26. SN74AC245 Spectrum of the Supply Current (output unloaded)**



**Figure 27. SN74AC245 Spectrum of the Supply Current (output loaded)**

### 5.4 SN74AC245 Measurement Results ( $V_{CC} = 3.3\text{ V}$ )

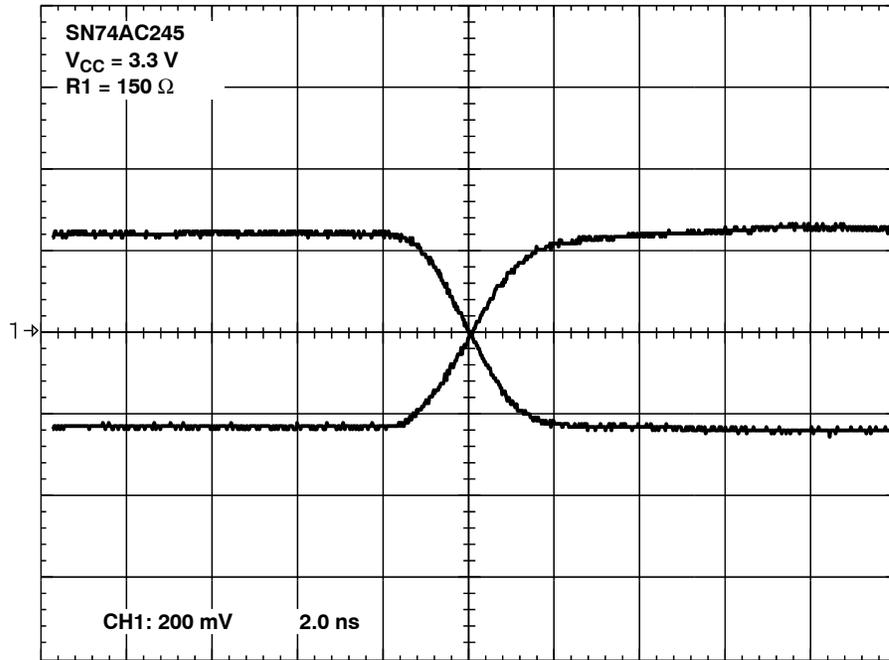


Figure 28. SN74AC245 Waveform at the Output

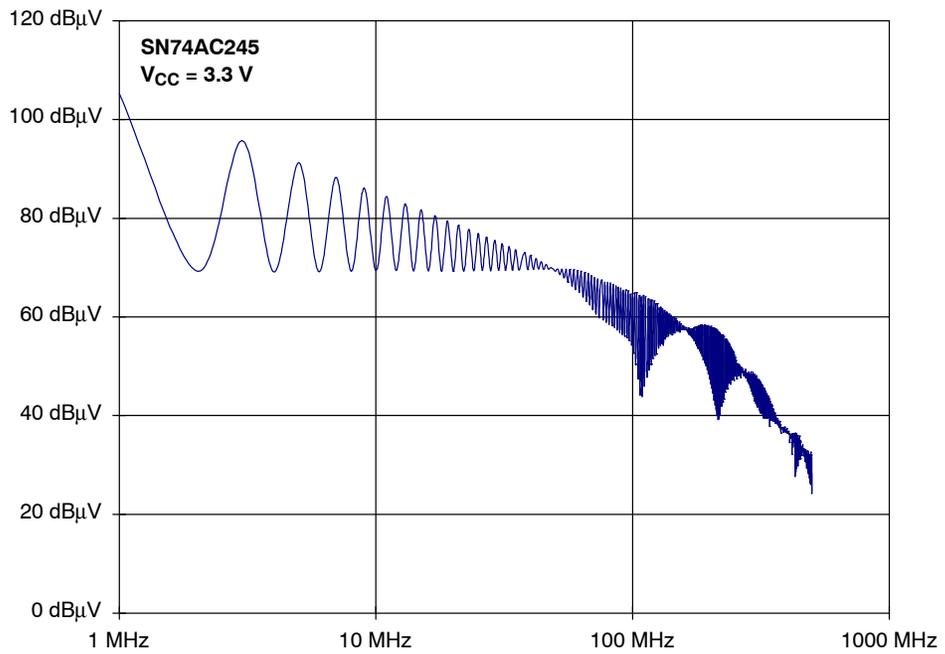
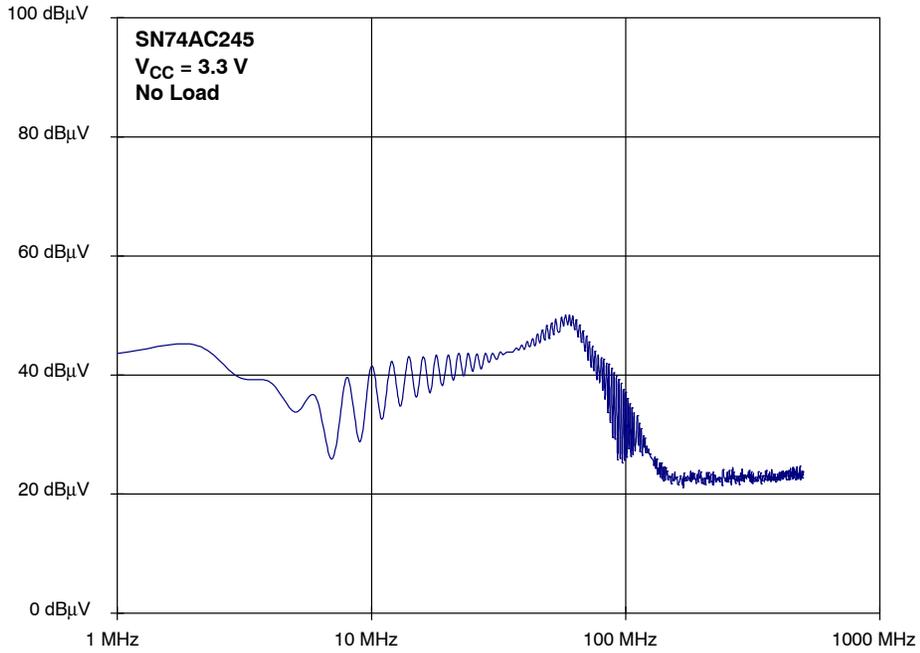
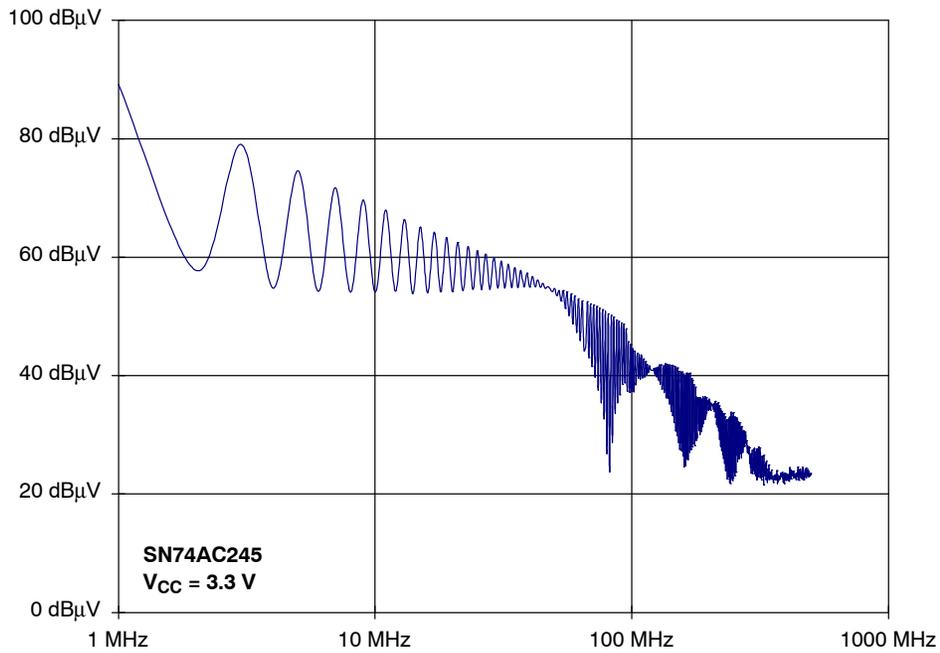


Figure 29. SN74AC245 Spectrum of the Output Signal



**Figure 30. SN74AC245 Spectrum of the Supply Current (output unloaded)**



**Figure 31. SN74AC245 Spectrum of the Supply Current (output loaded)**

### 5.5 SN74AHC245 Measurement Results ( $V_{CC} = 5\text{ V}$ )

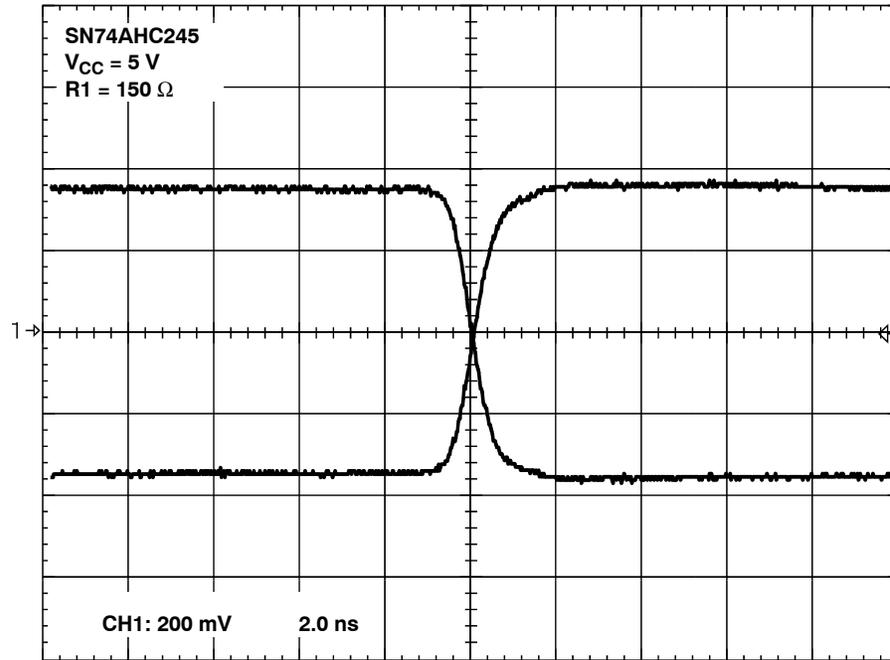


Figure 32. SN74AHC245 Waveform at the Output

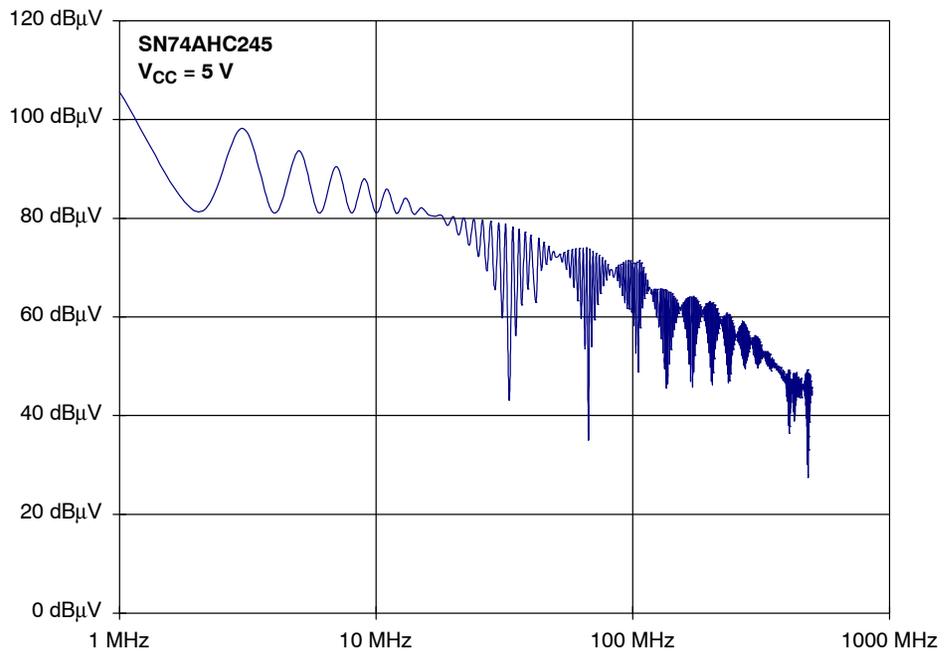
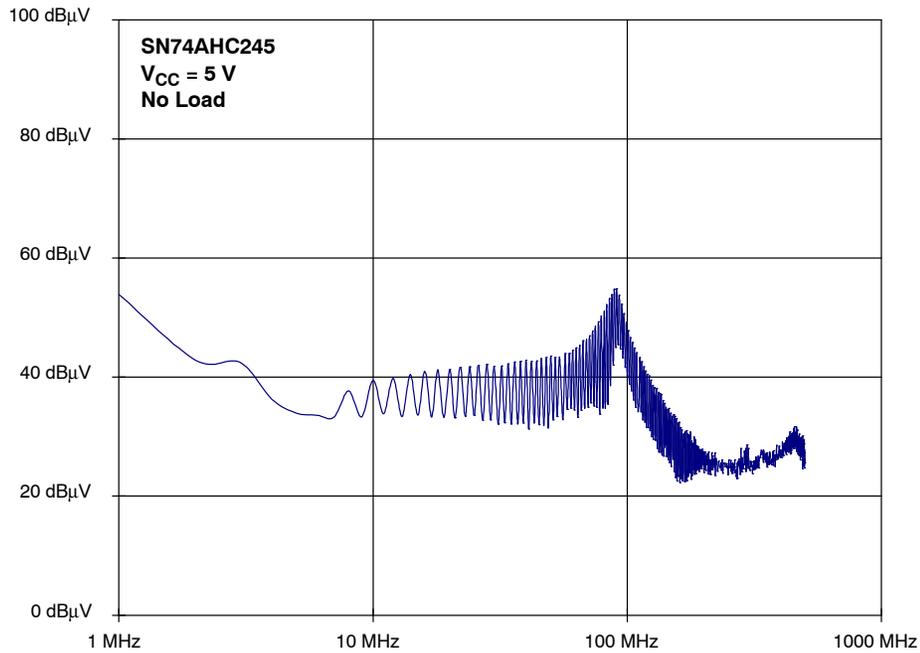
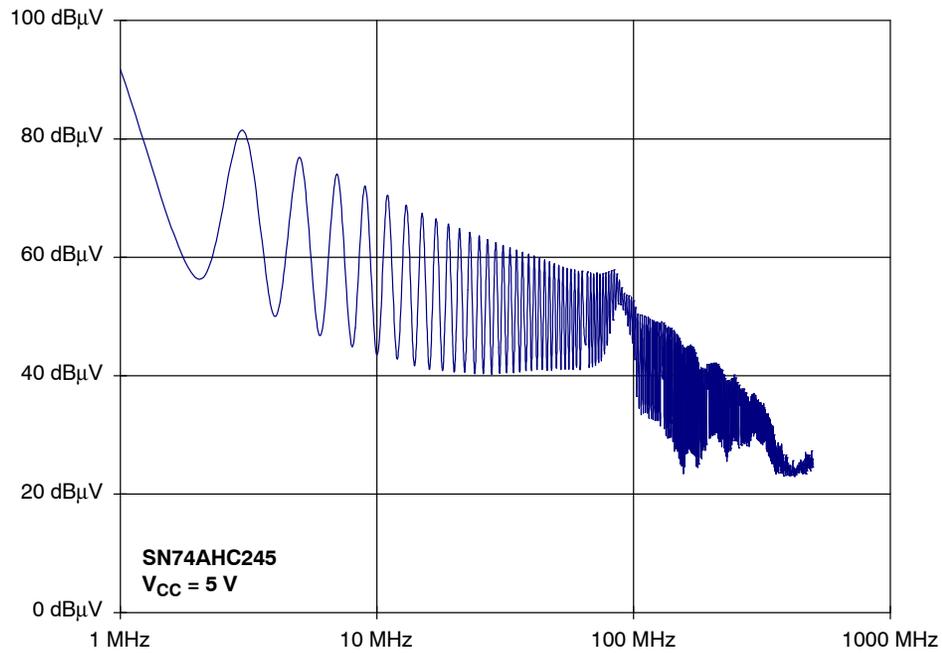


Figure 33. SN74AHC245 Spectrum of the Output Signal



**Figure 34. SN74AHC245 Spectrum of the Supply Current (output unloaded)**



**Figure 35. SN74AHC245 Spectrum of the Supply Current (output loaded)**

### 5.6 SN74AHC245 Measurement Results ( $V_{CC} = 3.3\text{ V}$ )

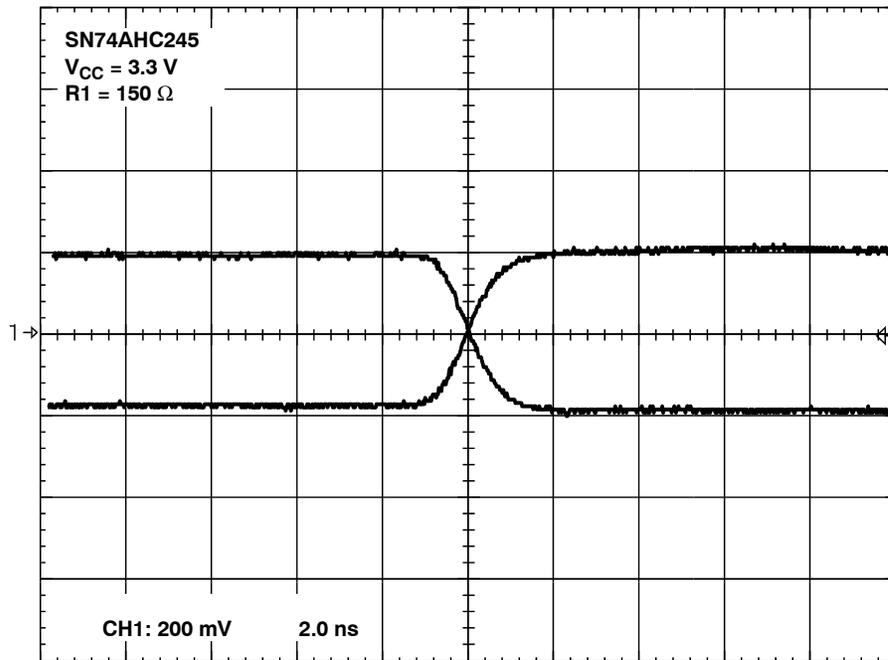


Figure 36. SN74AHC245 Waveform at the Output

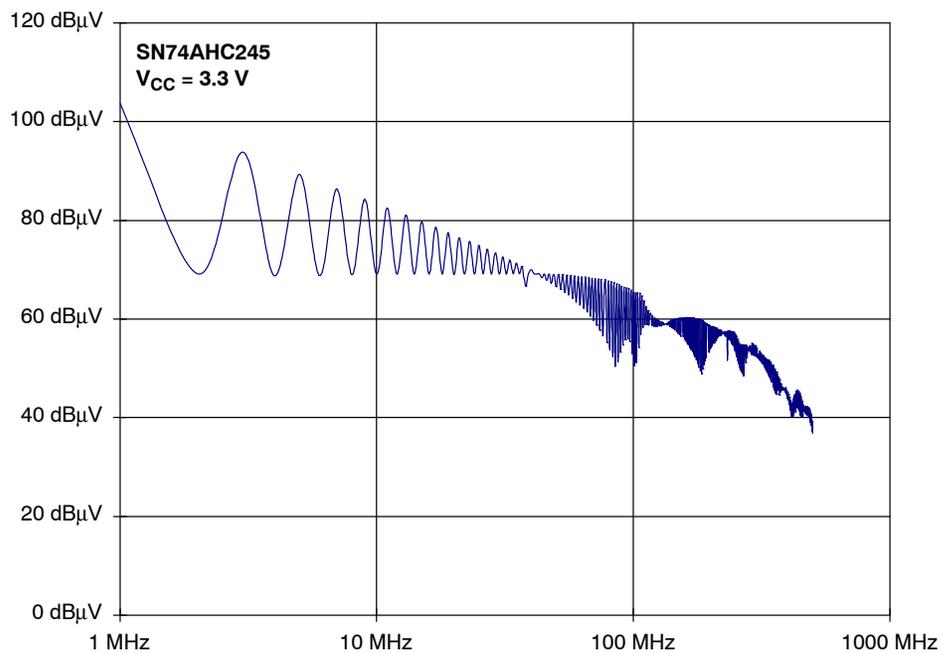
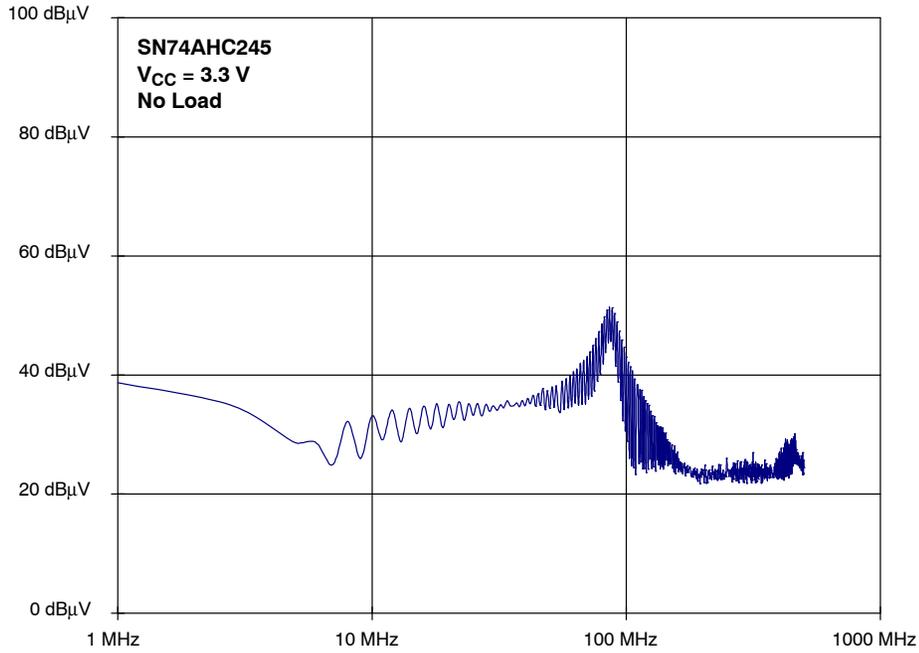
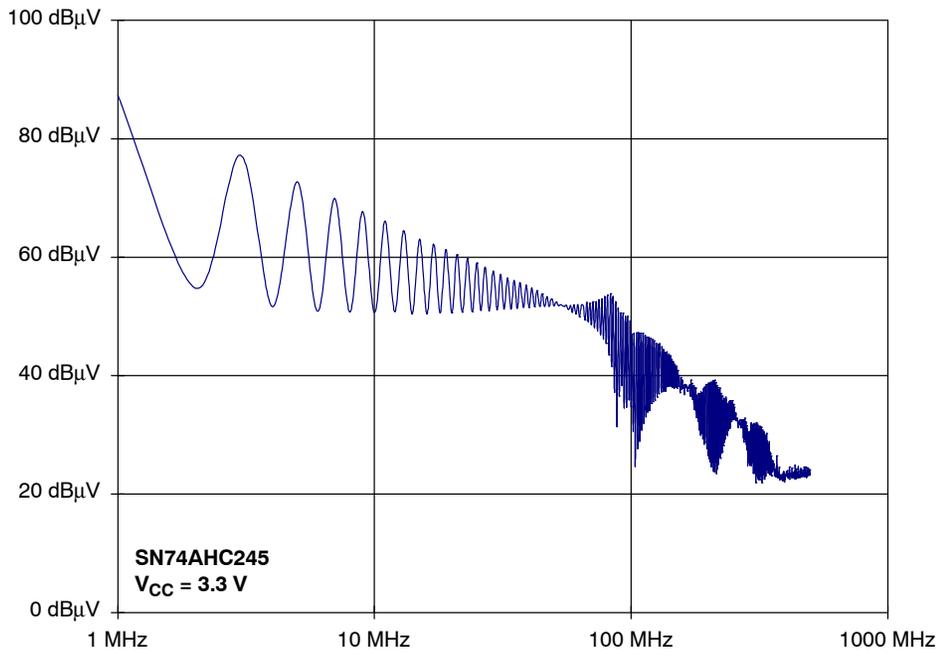


Figure 37. SN74AHC245 Spectrum of the Output Signal



**Figure 38. SN74AHC245 Spectrum of the Supply Current (output unloaded)**



**Figure 39. SN74AHC245 Spectrum of the Supply Current (output loaded)**

## 5.7 SN74ALS245 Measurement Results

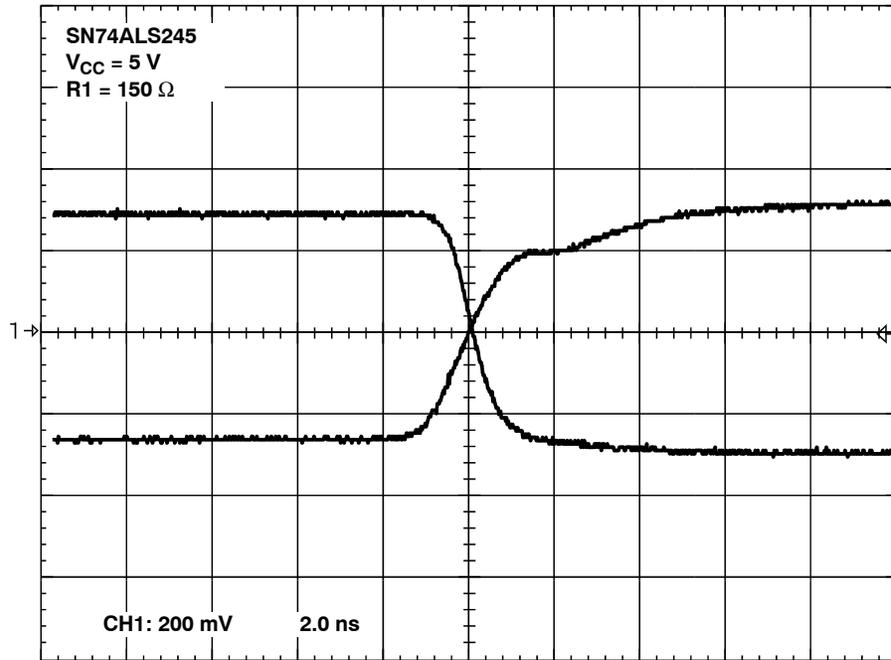


Figure 40. SN74ALS245 Waveform at the Output

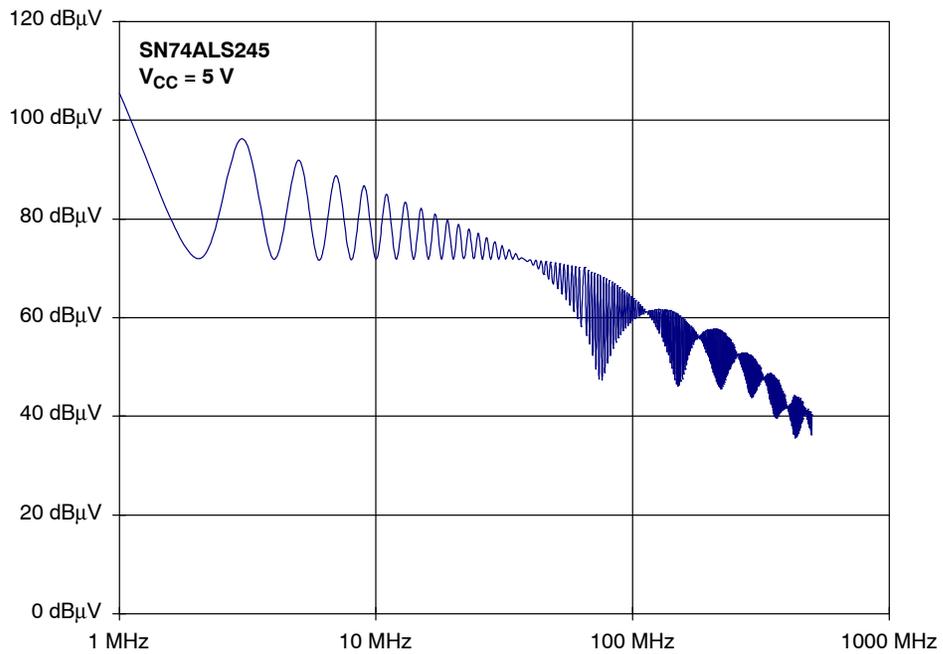
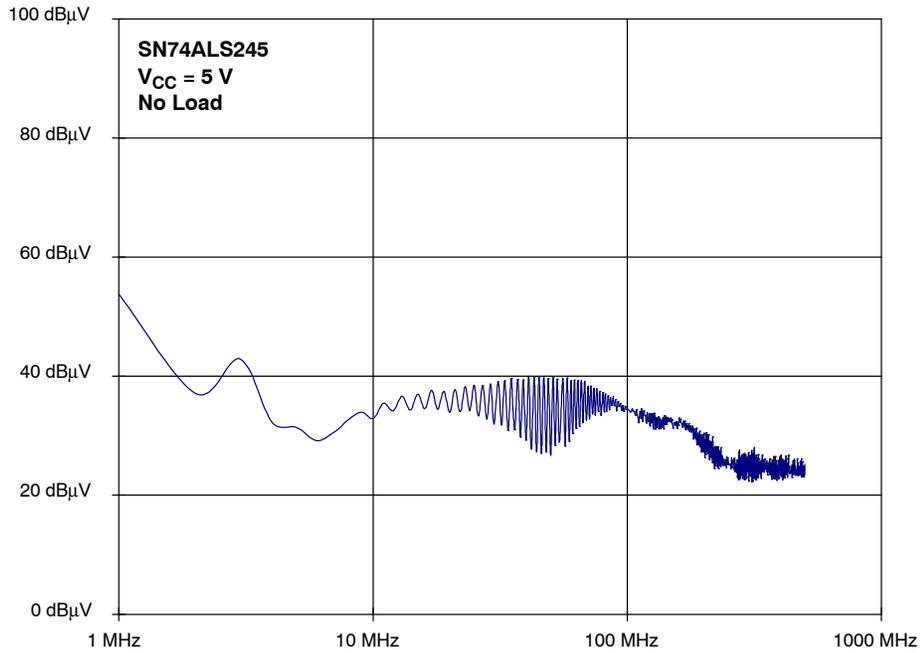
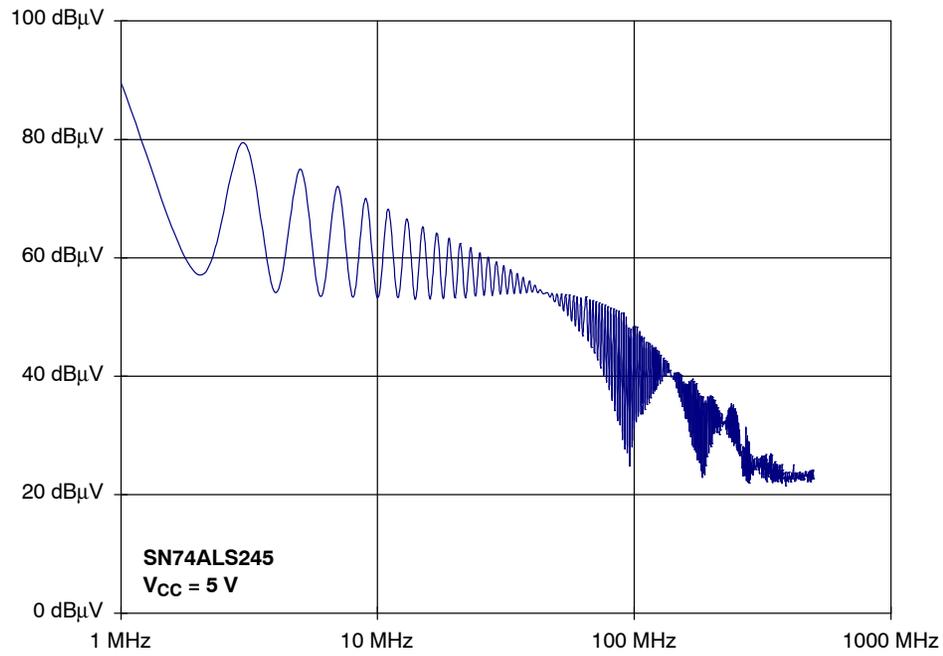


Figure 41. SN74ALS245 Spectrum of the Output Signal



**Figure 42. SN74ALS245 Spectrum of the Supply Current (output unloaded)**



**Figure 43. SN74ALS245 Spectrum of the Supply Current (output loaded)**

## 5.8 SN74AS245 Measurement Results

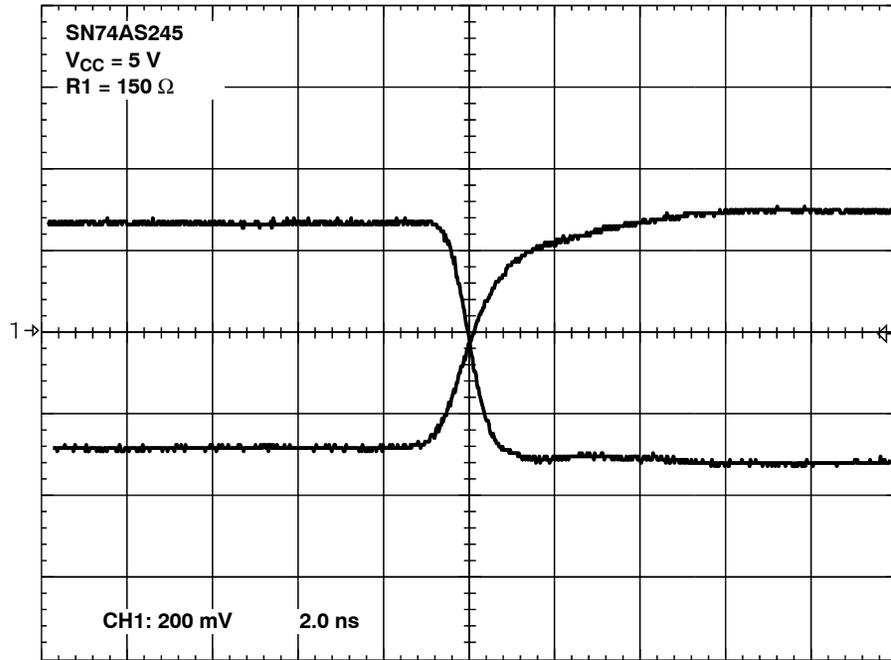


Figure 44. SN74AS245 Waveform at the Output

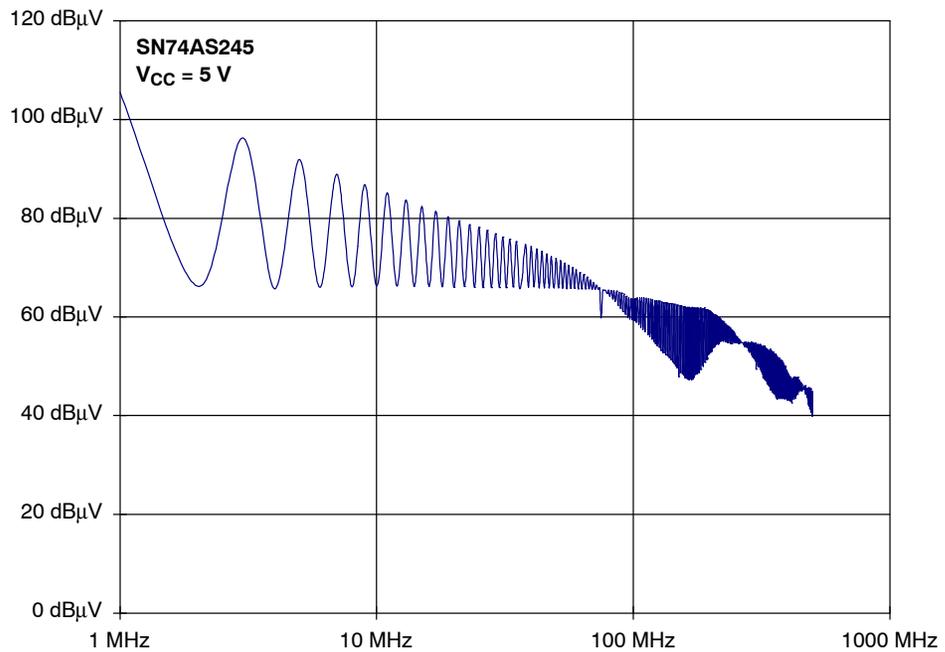
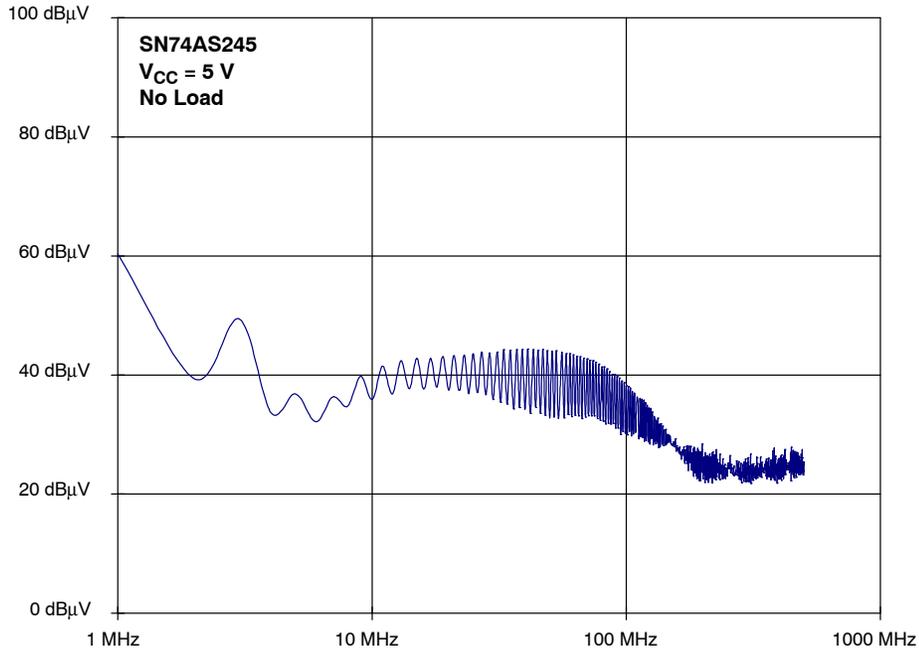
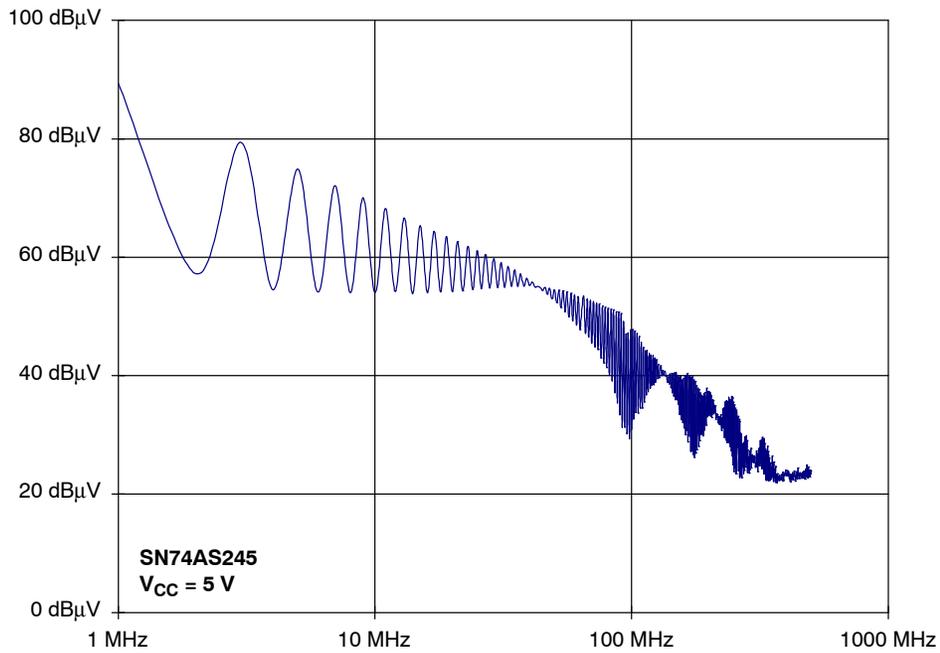


Figure 45. SN74AS245 Spectrum of the Output Signal



**Figure 46. SN74AS245 Spectrum of the Supply Current (output unloaded)**



**Figure 47. SN74AS245 Spectrum of the Supply Current (output loaded)**

## 5.9 SN74BCT245 Measurement Results

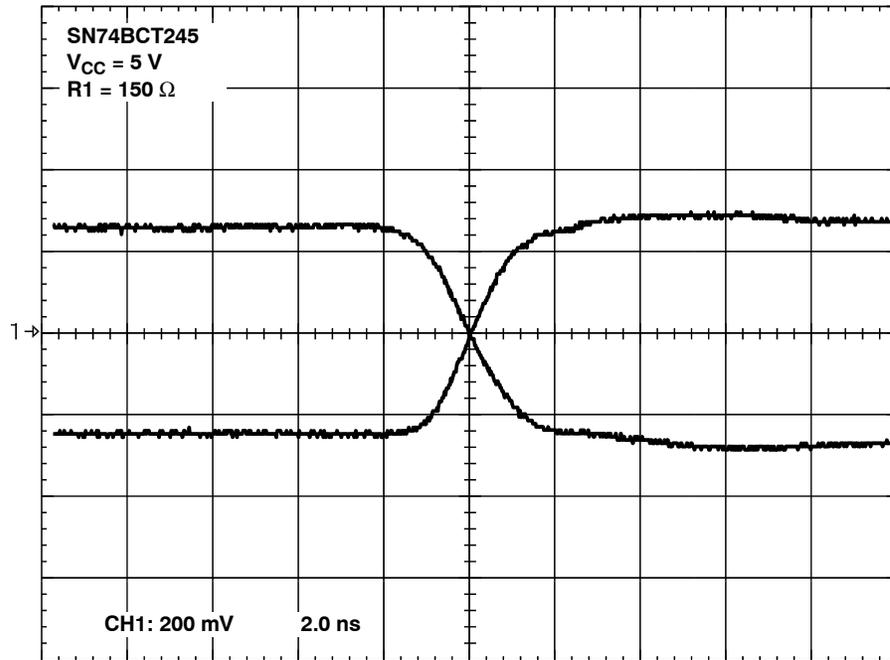


Figure 48. SN74BCT245 Waveform at the Output

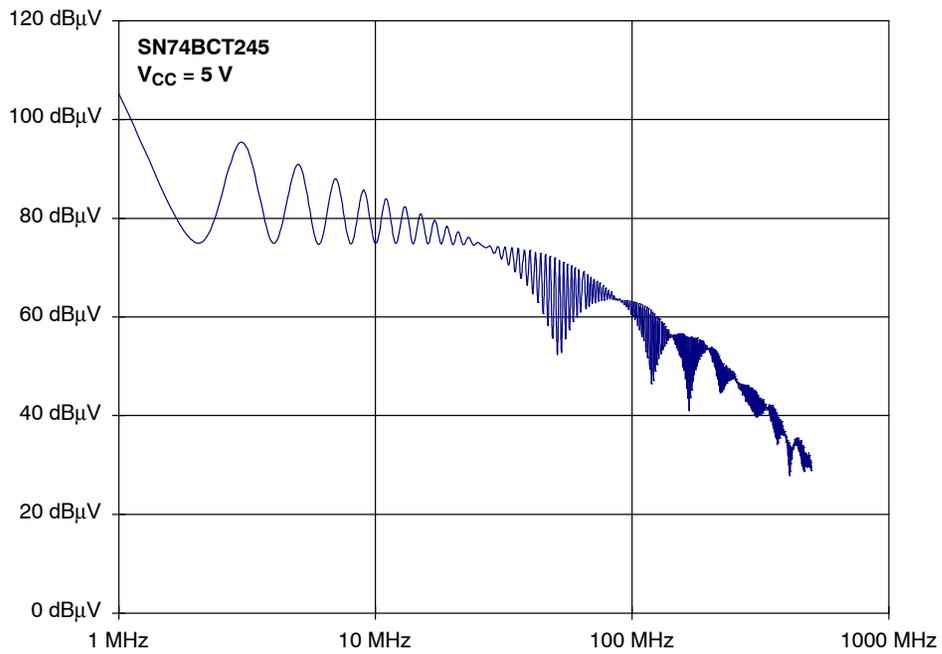
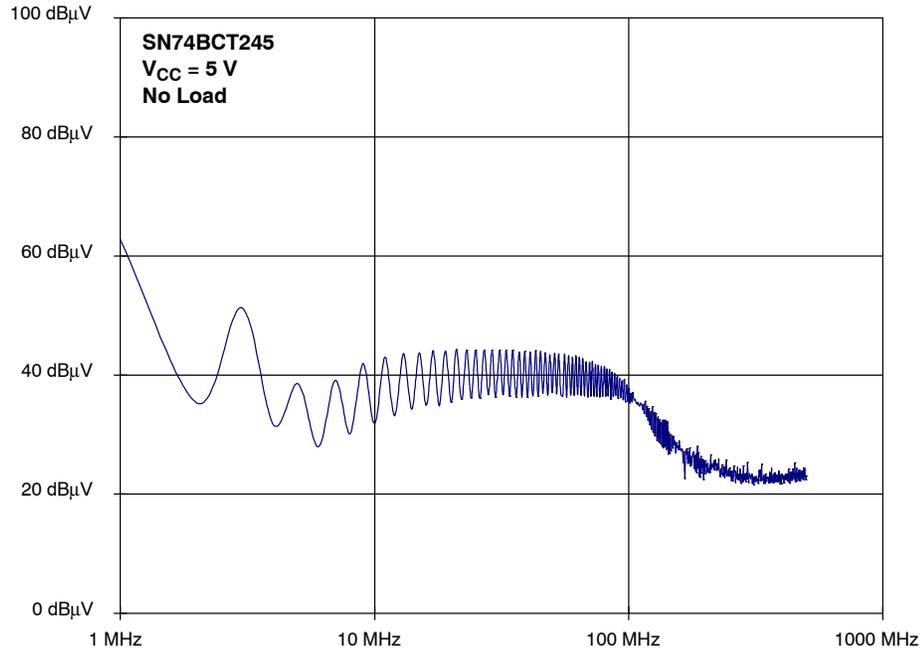
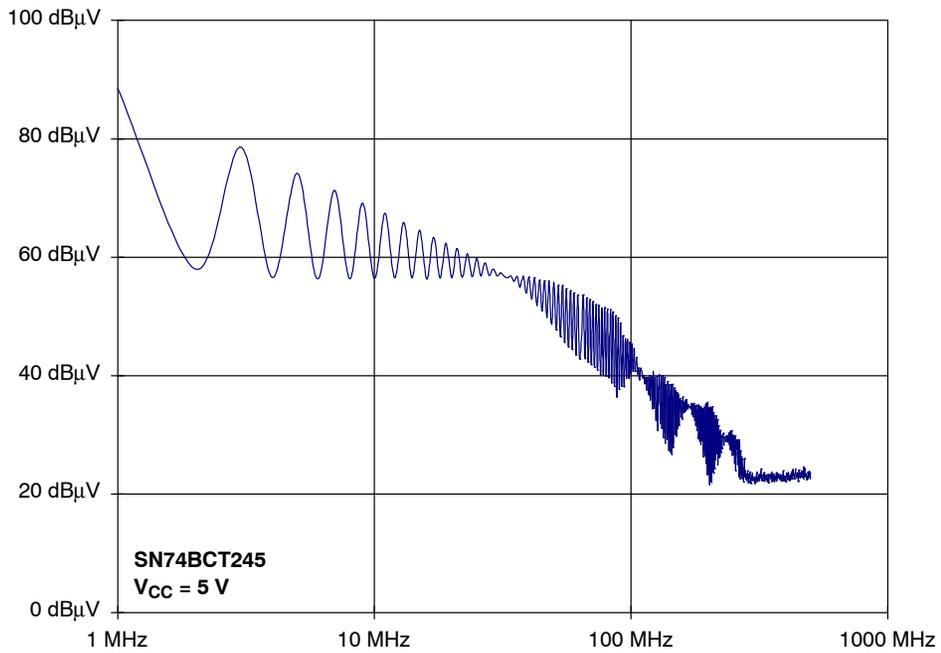


Figure 49. SN74BCT245 Spectrum of the Output Signal



**Figure 50. SN74BCT245 Spectrum of the Supply Current (output unloaded)**



**Figure 51. SN74BCT245 Spectrum of the Supply Current (output loaded)**

## 5.10 SN74F245 Measurement Results

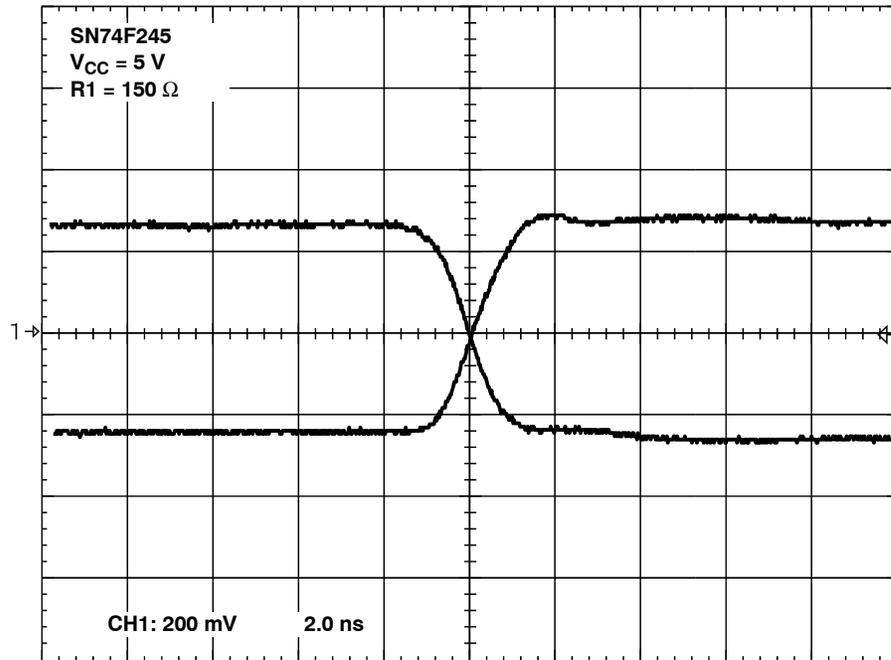


Figure 52. SN74F245 Waveform at the Output

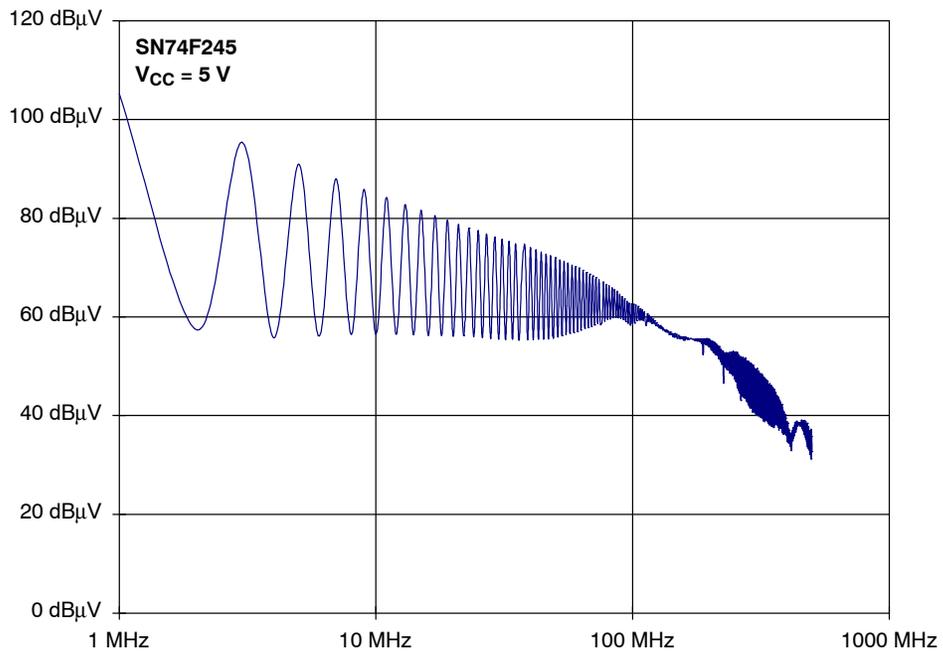
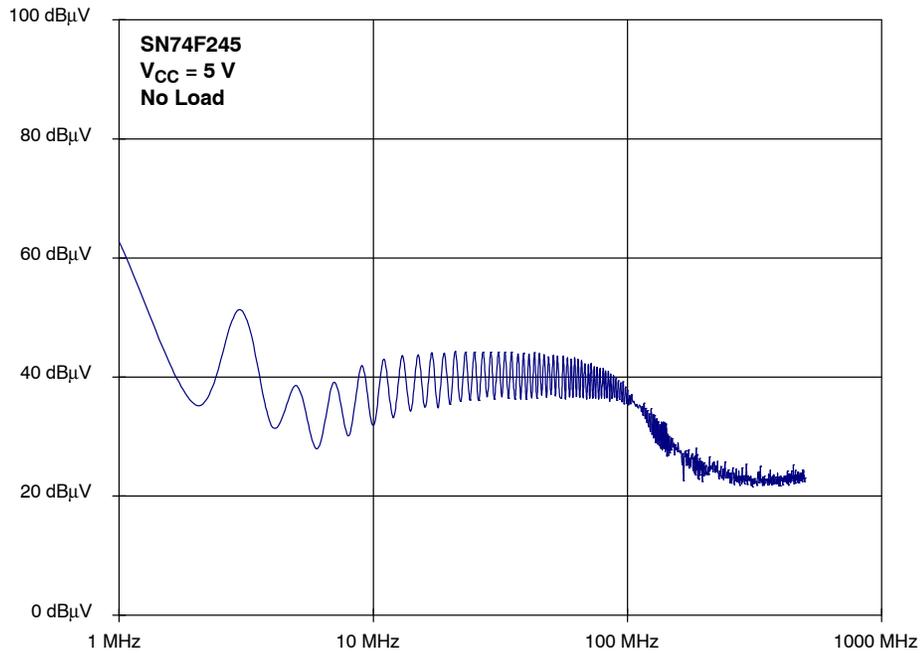
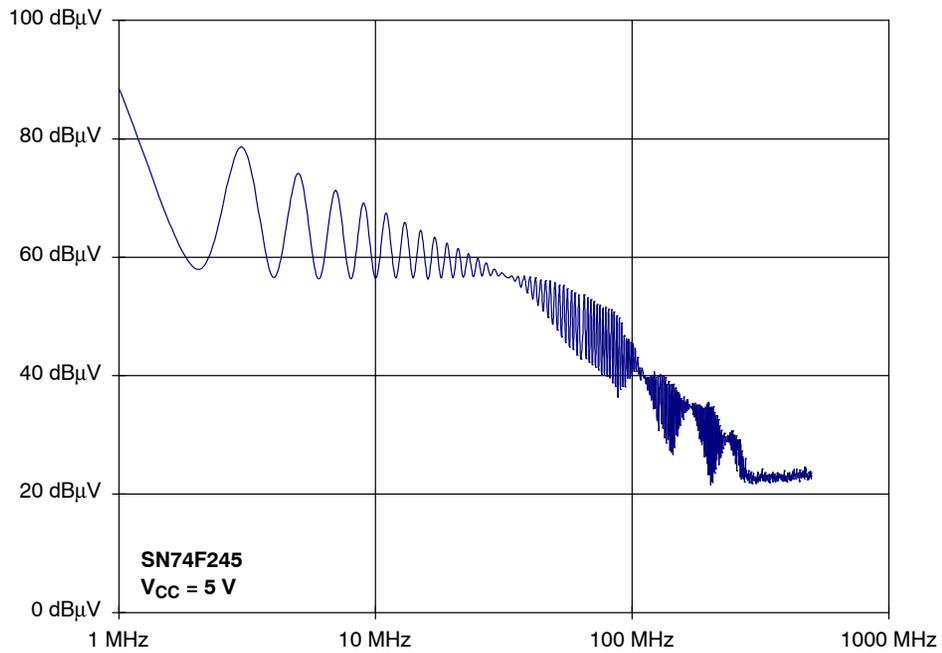


Figure 53. SN74F245 Spectrum of the Output Signal



**Figure 54. SN74F245 Spectrum of the Supply Current (output unloaded)**



**Figure 55. SN74F245 Spectrum of the Supply Current (output loaded)**

### 5.11 SN74HC245 Measurement Results

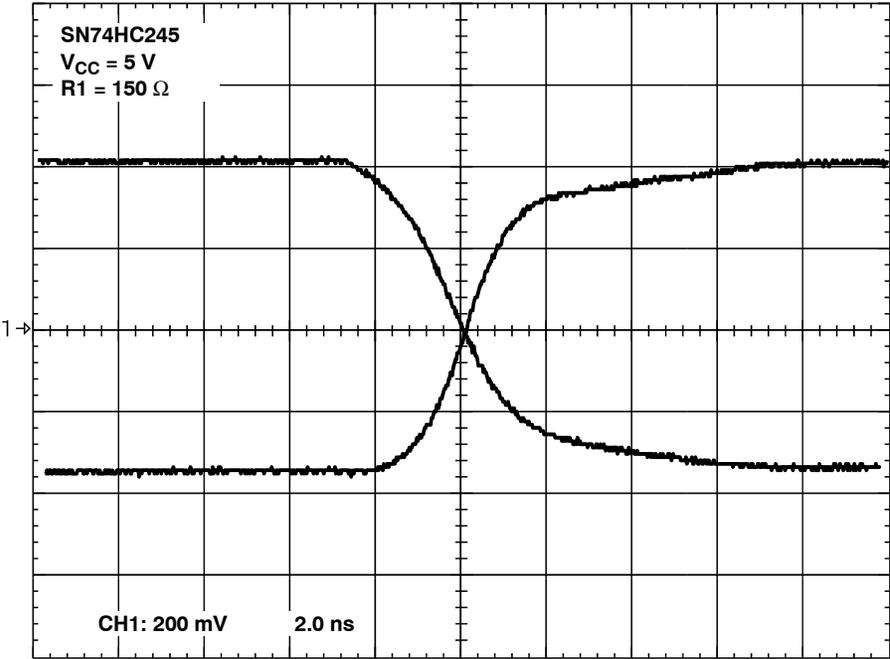


Figure 56. SN74HC245 Waveform at the Output

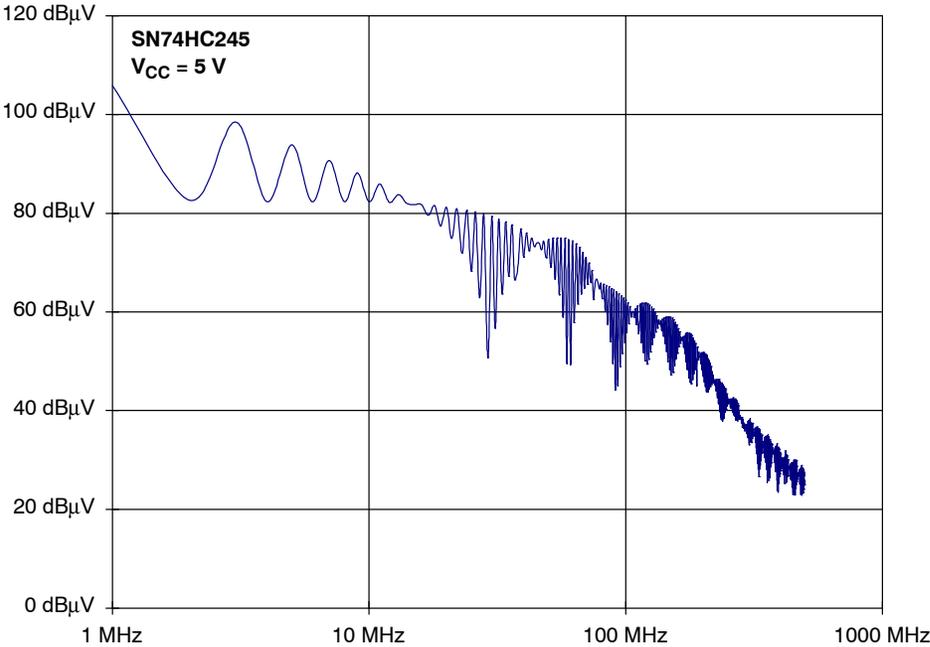
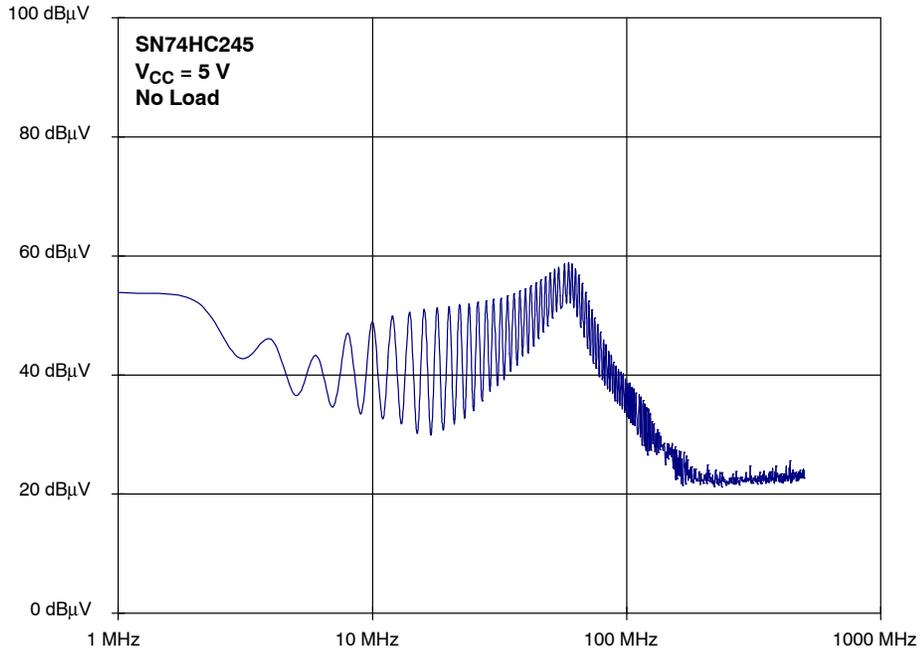
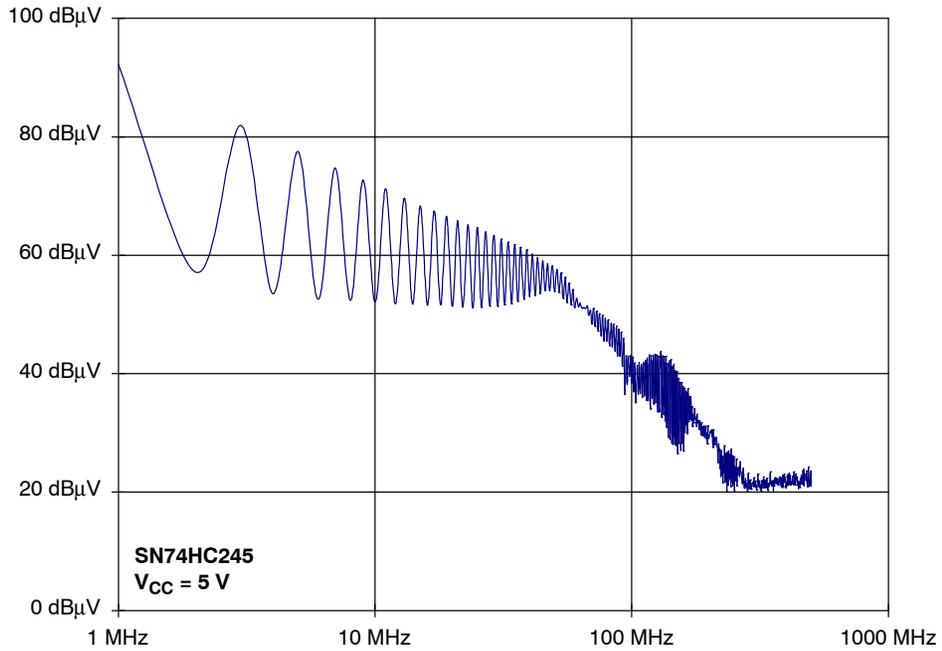


Figure 57. SN74HC245 Spectrum of the Output Signal



**Figure 58. SN74HC245 Spectrum of the Supply Current (output unloaded)**



**Figure 59. SN74HC245 Spectrum of the Supply Current (output loaded)**

## 5.12 SN74LS245 Measurement Results

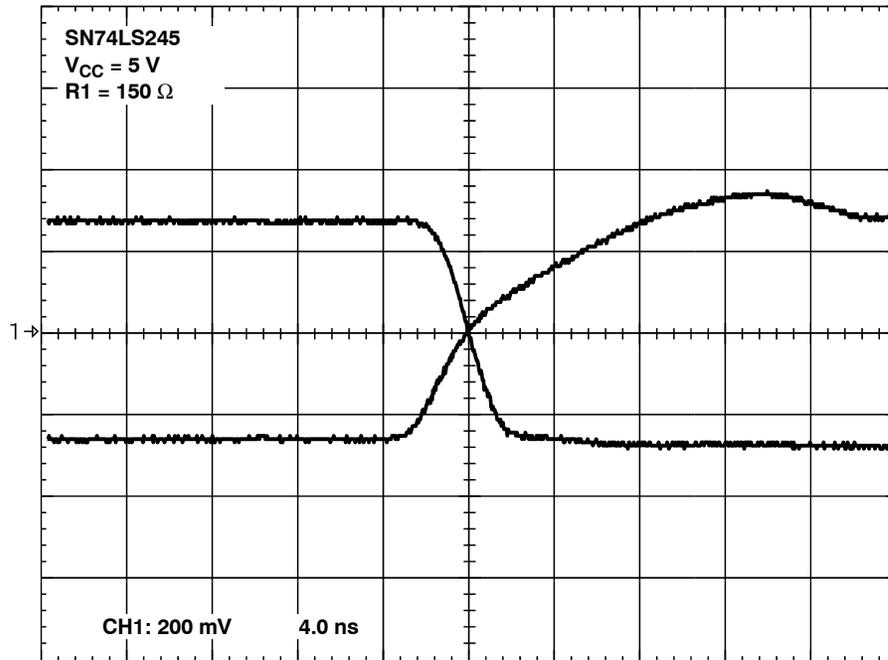


Figure 60. SN74LS245 Waveform at the Output

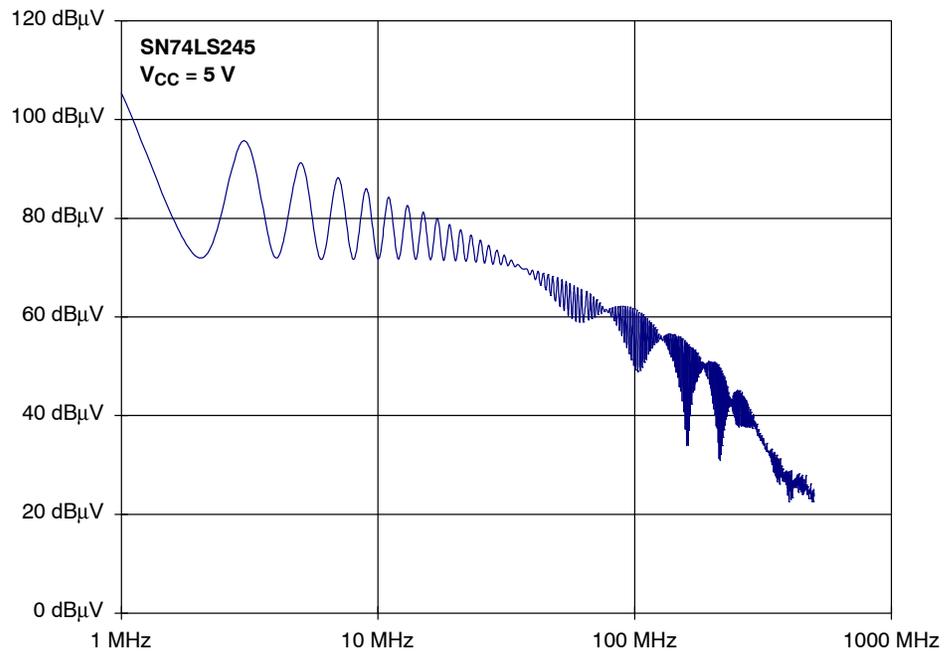
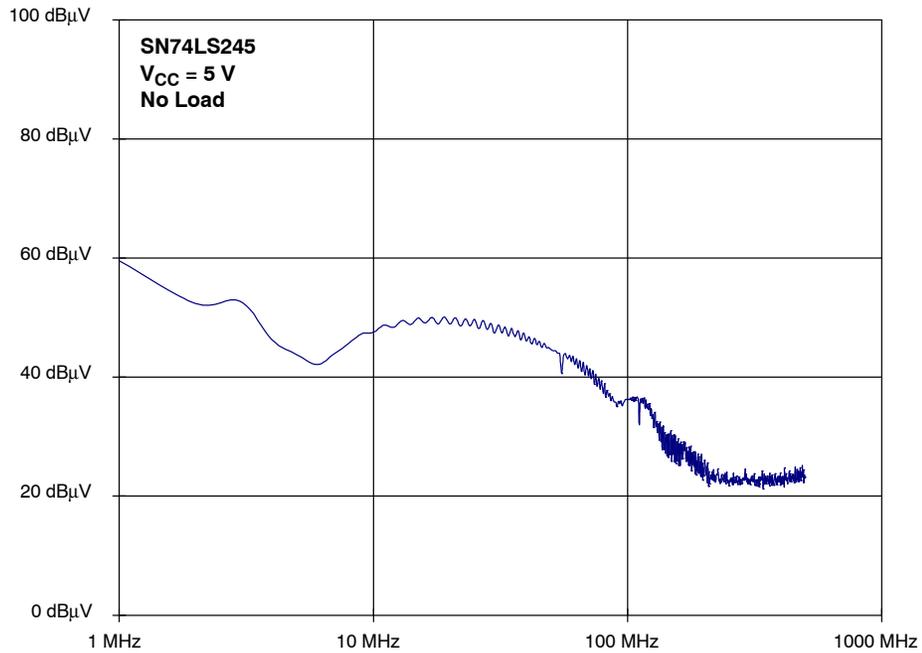
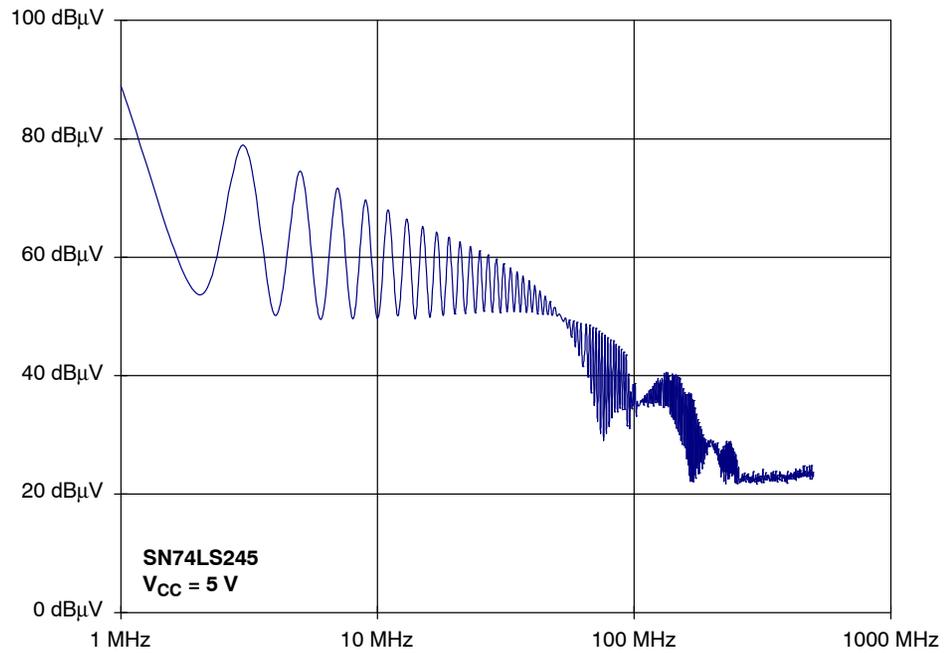


Figure 61. SN74LS245 Spectrum of the Output Signal



**Figure 62. SN74LS245 Spectrum of the Supply Current (output unloaded)**



**Figure 63. SN74LS245 Spectrum of the Supply Current (output loaded)**

## 6 Conclusion

This application report shows the extent to which the measurement method proposed by a working group in the DKE can determine the electromagnetic interference generated by integrated circuits. As previously demonstrated, there is good agreement between the results of measurements and the calculated theoretical values. However, because of the relatively simple structures of logic circuits, a realistic prediction of their electromagnetic compatibility can be made using only a few known parameters, such as signal amplitude and rise time. The situation is very different with highly integrated circuits, such as microprocessors or other VLSI semiconductors. Without a detailed examination of their behavior, the complex structures of these components make it impossible to reliably predict their electromagnetic compatibility. However, the measurement procedure used provides useful assistance in predicting the electromagnetic emission of the module or equipment, which can be done during the planning phase of a new development.

The logic circuits that have been examined are not good examples of components having outstanding electromagnetic compatibility. They have been conceived for applications where short delay times in the signal paths are of importance and, in most cases, have high drive capability at the outputs. Therefore, when developing these components, the intention usually is to achieve steep switching edges because these directly determine signal delay times. With modern logic circuits, the rise and fall times are about 1 ns to 2 ns. Shorter times no longer can be tolerated with the signal swings of 3 V to 5 V, which are common today, because the interference generated by the circuit itself would be of the same order as that which would no longer permit reliable operation of the system. The steep edges inevitably give rise to high interference amplitude in the upper frequency range, and correspondingly high currents in the integrated-circuit connections, which function as antennas.

Nevertheless, equipment with adequate electromagnetic compatibility can be designed using such components. The design engineer must observe certain basic rules when choosing the components to avoid problems later. From the many families of integrated circuits available, those with speeds (maximum clock frequency, required delay time) that are just able to achieve system requirements should be chosen. Every increase in performance often must be at the expense of costly changes to suppress interference. From this point of view, the older (and, thus, slower) bipolar logic families, such as advanced low-power Schottky TTL, and MOS families such as high-speed CMOS, have advantages. Also, bipolar circuits offer advantages because of their approximately 30% smaller signal-level swing. Another way to improve electromagnetic compatibility is to lower supply voltages. For this purpose, the new CMOS families are ideal because they feature excellent performance, even at a reduced supply voltage. The smaller currents, which result from the lower voltage swing, reduce the undesired radiation of high frequencies. Finally, careful layout of printed circuit boards<sup>1</sup> and, possibly, the use of filters in critical parts of the circuit are proven methods of achieving electromagnetic compatibility of a system.

## 7 References

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1. *PCB Design Guidelines for Reduced EMI*, literature number SZZA009.
2. *Fachverband Bauelemente der Elektrotechnik im Zentralverband der Elektrotechnik und Elektronikindustrie: Messung der EME von integrierten Schaltungen* (Expert Association for Electrotechnical Components in the Central Association of the Electrotechnical and Electronic Industry: The Measurement of the Electromagnetic Sensitivity of Integrated Circuits).
3. *Timing Measurement With Fast Logic Circuits*, literature number SDYA015; also obtainable at [http://www.ti.sc.docs.psheets/app\\_digital\\_logic.htm](http://www.ti.sc.docs.psheets/app_digital_logic.htm)
4. *Logic Selection Guide and Data Book*, CD-ROM, literature number SCBC001.
5. *Digital Design Seminar*, literature number SDYDE01A.

### 7.2 Internet

Texas Instruments web page at <http://www.ti.com>

## 8 Acknowledgments

The author of this application report is Eilhard Haseloff.

# **Latch-Up, ESD, and Other Phenomena**

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*Eilhard Haseloff*
*Standard Linear & Logic*

## **ABSTRACT**

The engineer designing an electronic system often needs to know the behavior of its components under operating conditions that are outside those usually described in the data sheets. Thus, although the latch-up effect is no longer a problem with modern CMOS circuits, a closer look at this phenomenon makes it easier for the engineer to assess realistically the risks that may arise under specific – perhaps extreme – operating conditions. The electromagnetic compatibility of integrated circuits, as well as their sensitivity and immunity to these effects, plays a significant role. Under particular operating conditions, parasitic transistors in integrated circuits can jeopardize the correct function of a component. This application report discusses latch-up, electrostatic discharge (ESD), and other phenomena, and their relationships, thereby providing designers information needed to assure the functional security of the system, even under extreme operating and environmental conditions.

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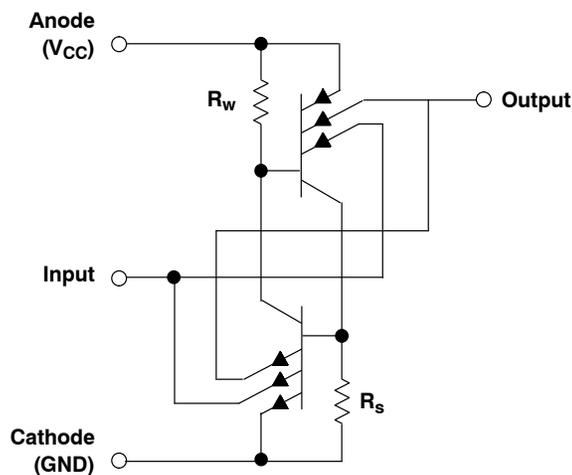
## 1 Introduction

When a customer buys an integrated circuit – a gate or an operational amplifier – from a semiconductor manufacturer, it contains considerably more transistors and diodes than are necessary for the basic function. The additional components, such as the clamping diodes on the inputs and outputs of logic circuits, are required to ensure reliable operation under particular conditions. These components limit the overshoots and undershoots resulting from line reflections and, thus, reduce signal distortion. Also, protection circuits, which are intended to protect the component from destruction as a result of electrostatic discharge, are provided.

In addition to these intentionally integrated additional components, an integrated circuit also contains a number of transistors and diodes that inevitably result from the construction and manufacture of the semiconductor circuit. These components are called parasitic transistors and diodes. Under normal operating conditions, as specified in the data sheets, such parasitic components have no influence on the function of the circuit. However, in particular situations, these parts of the circuit suddenly and unexpectedly can become active, and threaten the correct operation of the complete system. Therefore, the development engineer who uses integrated circuits also must be acquainted with the behavior of parasitic components. Only then can a circuit be designed with the necessary protective precautions that ensure reliable operation under required environmental conditions. Parasitic effects are discussed in the following sections to help design engineers understand these phenomena and, if necessary, take suitable precautions to prevent undesirable behavior by the integrated circuit.



In this example, the N-doped regions for source and drain of the N-channel transistor and the cathodes of the clamping diodes have been diffused into a P-doped substrate. The substrate is connected to the most negative point in the circuit, usually the ground connection (GND). In normal operation, the N-doped regions have a voltage that is more positive than the ground connection. In this way, these P-N junctions are blocking. The substrate now forms the base of a parasitic npn transistor, while all N-doped regions – that is, the drain and source of the N-channel transistor and cathode of the clamping diodes – function as emitters. The collector belonging to this transistor forms the well in which the complementary P-channel transistor is located. The latter, with its connections, forms a parasitic pnp transistor. The npn and pnp transistors form a thyristor, as shown in Figure 2. The anode and cathode of this thyristor are connected to the supply voltage of the integrated circuit, while all other points – inputs and outputs – function as the gate of the thyristor. As long as the voltages on the latter connections stay more positive than the ground connection and more negative than  $V_{CC}$ , correct operation occurs. The base-emitter diodes are blocking.



**Figure 2. Parasitic Thyristor in a CMOS Circuit**

A parasitic thyristor of this kind in an integrated circuit can be triggered in various ways:

- If there is a voltage at the input or output of a circuit that is more positive than the supply voltage, or more negative than the ground connection (or, to be precise, more negative than the connection to the substrate), current flows into the gate of the thyristor. If the amplitude and duration of the current are sufficient, the thyristor is triggered. The transit frequency of the parasitic transistors is only about 1 MHz. For this reason, overvoltages and undervoltages with durations of only a few nanoseconds, such as result from line reflections along the connections on circuit boards, usually are not able to trigger the thyristor. With lines of several meters in length and overshoots of correspondingly longer duration, the probability that the thyristor might be triggered must be taken into account. This applies also at the interfaces between a circuit and the outside world; unacceptable overvoltages also often occur at this point.
- An electrostatic discharge can trigger the parasitic thyristor. Even if the electrostatic discharges have a duration of only a few tens of nanoseconds, when this happens, the complete chip may be flooded with charge carriers, which then flow away slowly, resulting in the triggering of the thyristor.

- The parasitic thyristor can be triggered by a rapid rise of the supply voltage. This effect often was observed in earlier generations of CMOS circuits.
- Additionally, the thyristor might be triggered by a high supply voltage – far higher than the value given in data sheets. In this case, the supply voltage must be increased up to the breakdown voltage of the transistors. When in breakdown, the current in the parasitic transistors, which should be blocking, increases in an avalanche process, so that activation of the thyristor must be anticipated.
- Also, latch-up can be initiated by ionizing radiation. This is important with components that operate close to a source of high-energy radiation.

After the triggering of the thyristor, various reactions can be observed:

- The parasitic thyristor triggers very rapidly and enters a very low-resistance state. The source of the supply voltage is short circuited as a result of the circuit that has been affected. A very high current flows, which, in a very short time, leads to destruction of the component. The thyristor can be switched off again only by switching off the supply voltage. Therefore, the recommendation in the literature is that a resistor should be placed in series with the supply voltage connection to the integrated circuit. If the thyristor does trigger, this resistor limits the current to a value that no longer poses any danger to the device. If possible, the resistor should limit the current to a value below the holding current of the thyristor such that, after the end of the conditions that led to its being triggered, the thyristor automatically switches off.
- The thyristor triggers in the manner previously described, but, in this case, the thyristor has a comparatively high forward resistance. The result is that only the supply current increases, but this increase usually is quite large. Because of the high power dissipation in the circuit, the component can be damaged. The thyristor usually switches off only after the supply voltage has been switched off.
- In some cases, the thyristor has a very high resistance. The high forward resistance limits the current to values below the holding current of this thyristor. In this case, the supply current increases. The supply current sinks to normal values when the trigger current at the gate of the thyristor (as a result of an overvoltage at the input or output of the integrated circuit) is switched off.

## 2.2 Precautions to Be Taken Against Latch-Up

Semiconductor manufacturers have worked to avoid latch-up of CMOS circuits, and various precautions can be implemented. First, the conflicting components can be located as far as possible from each other. This reduces the current gain of the parasitic transistors, and the triggering sensitivity of the thyristors is reduced. However, these precautions achieve only limited success because, for reasons of space and cost, the distance between the conflicting components can be increased only to a certain limit. On the other hand, the continuous process of reduction in the geometries of semiconductor circuits works in the opposite direction. Therefore, other remedies that combat latch-up are necessary, including surrounding the critical parts of the circuit with guard rings (see Figure 3).

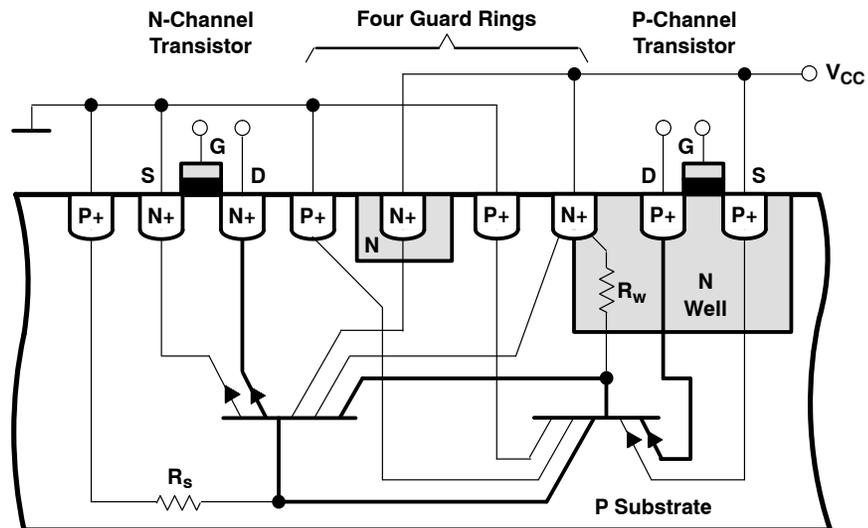
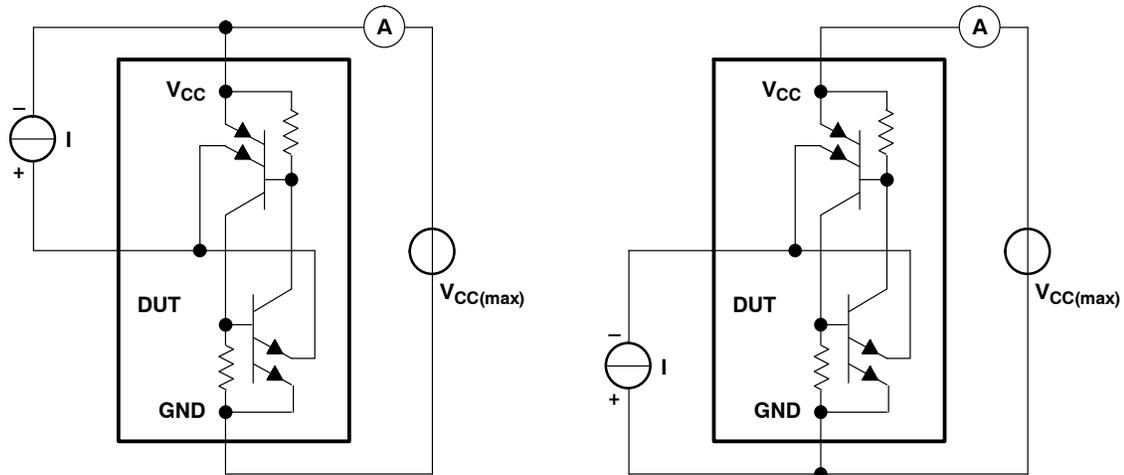


Figure 3. Guard Rings in a CMOS Circuit

These guard rings form additional collectors for the parasitic transistors. Such collectors are connected either to the positive or negative supply-voltage connection of the integrated circuit. These additional collectors are placed considerably closer to the base-emitter region of the transistor in question than the corresponding connections of the complementary transistor. As a result, the charge carriers injected into one of the two transistors is diverted largely via these auxiliary collectors to the positive or negative supply-voltage connection. These precautions do not completely eliminate the questionable thyristor. However, the thyristor's sensitivity is reduced to such an extent that, under normal operating conditions, there should be little risk of triggering the thyristor.

## 2.3 Latch-Up Test

After designing an integrated circuit, the first samples of the new device are subjected to intensive testing. All relevant parameters are measured – many more than those included in the data sheets. The latch-up sensitivity of CMOS and BiCMOS circuits also is examined, using the test circuit shown in Figure 4. The maximum permissible supply voltage is applied to the circuit, then current is injected for a certain duration into each input and output. During this test, the supply current of the device under test must not rise.



**Figure 4. Latch-Up Test Circuit**

Measurement conditions are different for various types of circuits. For example, logic circuits of the SN54/74 families are subjected to a current of 300 mA to 500 mA for 10  $\mu$ s at an ambient temperature of 125°C. These test conditions should comprehend the worst-case operating conditions. The parasitic transistors in the integrated circuit are bipolar components. The current gain of such devices increases with temperature and, thus, also the sensitivity of the thyristor that is to be tested. A test pulse duration of 10  $\mu$ s should ensure that the questionable thyristor is triggered, if this is possible. As previously mentioned, the transit frequency of the parasitic transistors is very low. Thus, significantly shorter pulses cannot provoke a reaction from the circuit. The amplitude of the current is used to assess the worst-case conditions under which the circuit can be operated. Overshoots and undershoots caused by line reflections can – in theory – give rise to currents of up to 100 mA in the clamping diodes (see Section 4.3). At the interfaces to the outside world, under certain circumstances, even higher currents can occur. Additional investigations have shown that, at room temperature, currents of 1 A to 2 A typically are needed to cause latch-up. The test conditions described are potentially destructive, meaning that devices tested in this way must not be delivered to customers. The high current density during this test might permanently damage the device.

At final test, LinCMOS devices are tested individually for latch-up sensitivity. To avoid damage to the components, a current of only 100 mA is injected into the device under test. Because analog components, such as operational amplifiers, usually operate in a considerably higher-resistance environment compared to digital circuits, these test conditions are sufficient to cover conditions likely to occur in practice.

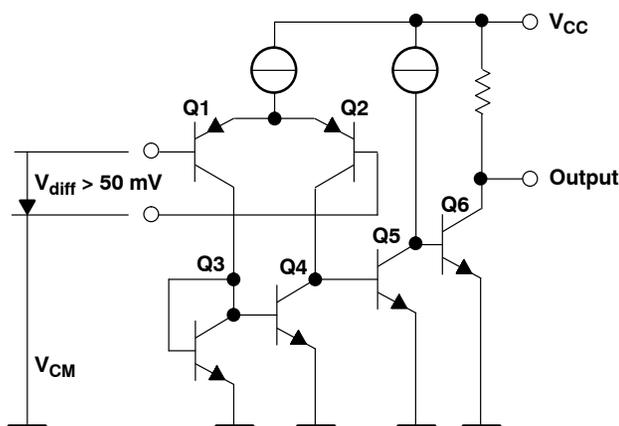
The characteristics of modern CMOS and BiCMOS circuits described here meet practically all the requirements, with respect to insensitivity to latch-up, that are likely to occur in practice. Only in a very few cases would the development engineer need to take additional precautions.

## 2.4 Pseudolatch-Up

In addition to the essential meaning of latch-up, as described previously, this term also is used commonly for a number of other phenomena, even though, in such cases, latch-up in its classical sense is not involved. Because, in certain applications, effects of the other phenomena also can cause serious problems, they are discussed in more detail in the following sections.

### 2.4.1 Pseudolatch-Up With Analog Circuits

If a voltage that is applied to the inputs of an operational amplifier or comparator lies outside the range given in the data sheet for common-mode operation, the input stage of the circuit may be put into a state that results in unpredictable behavior. See Figure 5 and the following paragraph for a discussion of this behavior.

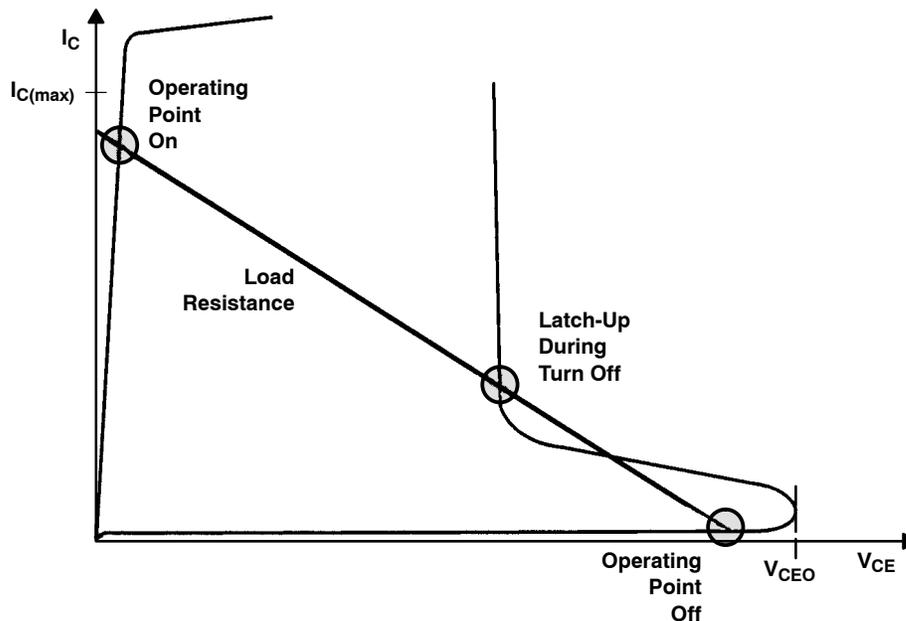


**Figure 5. Simplified Circuit of a Differential Amplifier**

The initial assumption is that the difference in voltage between the two inputs is  $V_{diff} = 50 \text{ mV}$ , whereby the voltage on the base of transistor Q1 is more positive than that on the base of transistor Q2. It also is assumed that the two voltages are within the permissible common-mode range ( $0.3 \text{ V} \leq V_{CM} \leq V_{CC} - 1 \text{ V}$ ). Under these conditions, transistors Q1, Q3, and Q4 are blocking, Q2 and Q5 are conducting, and output transistor Q6 is blocking. Consequently, a voltage level at the output is reached that corresponds to the supply voltage,  $V_{CC}$ . If the common-mode voltage,  $V_{CM}$ , is raised by more than approximately  $V_{CC} - 1 \text{ V}$ , the base-emitter voltage available to transistor Q2 is no longer sufficient to cause a base current to flow. Because the current flow in transistor Q2 is interrupted, Q5 also switches off. Output transistor Q6 becomes conducting, and a voltage level at its collector is reached that no longer conforms to the required potential difference at the input of the amplifier. This sudden and unexpected behavior of the circuit sometimes is called latch-up, even when this effect has nothing to do with the phenomenon described in Section 2.1. A defined state of the circuit again is reached at the instant when the voltage at the inputs returns to a value within the recommended range of input voltage. However, with certain complex operational amplifiers, the internal circuitry might become latched under the input conditions described in this paragraph. In this case, a reduction of the input voltage no longer results in the correct operation of the circuit; on the contrary, the supply voltage first must be switched off to reactivate the amplifier. However, this is not the basic phenomenon of latch-up.

## 2.4.2 Pseudolatch-Up With Bipolar Transistors

Another phenomenon, also called latch-up, occurs with bipolar transistors, particularly with output transistors carrying high currents. Figure 6 shows the output characteristics of a bipolar transistor in which the load resistor also is represented. The data sheet for the transistor includes, among other characteristics, the maximum collector current  $I_{C(max)}$  and the breakdown voltage  $V_{CEO}$  of the transistor. These two figures can be assumed to define the limits of the permissible safe operating area of the transistor.



**Figure 6. Output Characteristics With Load Resistor**

A detailed analysis of the breakdown characteristics of the transistor reveals that, when the transistor is in breakdown, the breakdown voltage decreases with increasing collector current. If a low resistance is drawn in on the diagram, this intersects the corresponding output characteristics, not only at the desired on and off points, but also at a third intersection of the breakdown characteristics with the load resistance. This is not critical when the transistor is switched on fast, although, in this case, the breakdown characteristics are exceeded briefly. During this transition, the transistor acquires an increasingly low resistance; therefore, the working on point is defined reliably. The behavior is very different when the transistor is switched off because it travels along the load resistance line in the direction of off. During this journey, the transistor intersects the breakdown characteristics as it becomes increasingly resistive. At this point, the transistor hangs up: the term commonly used is, again, latch-up. A considerable collector current flows while there is a high collector-emitter voltage. The result is high power dissipation which, in turn, causes a high chip temperature and results in accelerated aging (and even destruction) of the component.

It often is difficult to detect this situation with commonly used measurement techniques. If contact is made to a point connected to the collector using the test probe of a voltmeter, or with the probe of an oscilloscope, which usually has a much lower capacitance, the effect mentioned above no longer can be observed. When there is capacitive loading, the switch-off curve no longer is a straight-line resistance characteristic but, instead, is a hyperbola. The capacitance at the output first prevents a rise of the collector voltage, while the collector current already is falling. As a result, the critical point is avoided.

This kind of latch-up can be avoided effectively only by choosing transistors that have sufficient reserve in the breakdown region. Texas Instruments frequently specifies in data sheets of interface circuits a latch-up-free region in which the output transistor can be operated without danger to the device. For example, with the power drivers in the SN75471 family, the data sheet gives a maximum collector voltage in a blocking state (off-state output voltage) of  $V_O = 70 \text{ V}$ . This value corresponds approximately to the voltage  $V_{CEO}$  in Figure 6. Because of the behavior in breakdown of the transistor described above, latch-up-free operation is specified only with an output voltage of  $V_{CE(max)} = 55 \text{ V}$  and a collector current of  $I_{C(max)} = 300 \text{ mA}$ .

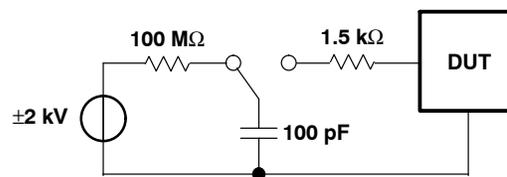
### 3 Electrostatic Discharges

Electrostatic discharges constitute a danger for integrated circuits that never should be underestimated<sup>1</sup>. Electrostatic charging can occur as a result of friction, as well as for other reasons. When two nonconducting materials rub together, then are separated, opposite electrostatic charges remain on both. These charges attempt to equalize each other. A common example of the generation of such charges is when one walks with well-insulated shoes on a carpet that is electrically nonconducting, causing the body to become charged. If a conducting object is touched, for example, a water pipe or a piece of equipment connected to a ground line, the body is discharged. The energy stored in the human body is injected into the object that is touched, and is converted primarily into heat. The power dissipation that arises in such cases can destroy sensitive electronic circuits.

Even though the semiconductor industry has increased efforts to protect components against destruction as a result of electrostatic discharges, usually it is not possible to provide adequate protection in every conceivable situation. Test circuits have been developed to test sensitivity to electrostatic discharges by simulating various scenarios. These test circuits are analyzed in more detail in the following paragraphs. These should provide the design engineer with insight into the reliability of these tests and the effectiveness of the individual protection circuits, providing the criteria to decide, in individual cases, whether additional precautions are necessary.

#### 3.1 Human-Body Model

The human-body model is described in MIL-STD-883B. The test is a simulation, in which the energy stored in a human body is discharged into an integrated circuit. The body is charged as a result of friction, for example. Figure 7 shows the test circuit. In this circuit, a capacitor ( $C = 100 \text{ pF}$ ) is charged through a high-value resistor to  $\pm 2000 \text{ V}$ , then discharged through a  $1.5\text{-k}\Omega$  resistor into the device under test.



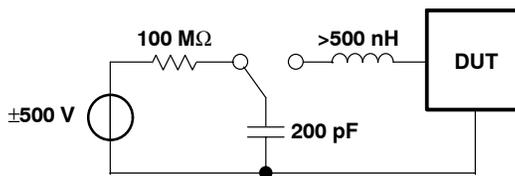
**Figure 7. Human-Body Model Test Circuit**

The  $100\text{-pF}$  capacitor simulates the capacitance of the human body. However, the actual capacitance of the human body is between  $150 \text{ pF}$  and  $500 \text{ pF}$ , depending on size and contact area (shoe size). Also, the  $1.5\text{-k}\Omega$  value of the discharge resistor must be considered. The internal resistance of the human body ranges from a few kilohms to a few hundred kilohms, depending on various factors, which include the humidity of the skin. However, if the discharge takes place through a metallic object, such as a screwdriver, the discharge resistor can be assumed to be a few tens of ohms. For these reasons, the corresponding Standard IEC 802-2 prescribes a test circuit with a capacitance of  $150 \text{ pF}$  which, in practice, is more realistic and a lower value of discharge resistor ( $R = 330 \Omega$ ). This standard is, however, concerned with a test specification for equipment that is not directly applicable to integrated circuits. Using a value of  $2000 \text{ V}$  also is questionable because, when a discharge causes a tingling in the tips of the fingers, the body has been charged to at least  $4000 \text{ V}$ .

The energy of about 0.4  $\mu\text{W}$ s that must be dissipated in the actual protection circuit is comparatively small. The major part of the energy stored in the capacitor is converted into heat in the discharge resistor. A considerably more-important parameter in the test, according to this method, is the rise time of the current during the discharge. Standard IEC 802-2 prescribes a rise time of about 0.7 ns at the actual location of the discharge. This value is of interest because, with a fast discharge, at the first instant only a small part of the protection circuit conducts. Only during the subsequent phase (a matter of nanoseconds) does the current spread over the complete conducting region of the protection circuit. Therefore, during the first moments of the discharge, the danger of a partial overload of the protection circuit exists. A similar effect can be observed with thyristors and triacs. With such components, the rate of current rise after triggering must be limited because, at first, only a small area of the semiconductor near the trigger electrode is conducting. A high current density can result in the destruction of the component. This effect is, however, in many cases responsible for the fact that, even with discharges from considerably higher voltages, the destruction of the circuit does not necessarily occur. The point at which the discharge occurs usually is not at the connections to the integrated circuit, but, instead, to the cabinet of the equipment or to the contact of a plug. Between this point and the endangered integrated circuit there is a length of conductor that has significant inductance. This inductance slows the rate of rise of the current, and helps ensure that the discharge current is spread evenly over the complete protection circuit.

### 3.2 Machine Model

The test using the machine model simulates the situation in machinery or other equipment that contains electronic components or modules. The casing of such equipment is constructed largely of metal, but often contains plastic bearings or other parts having a wide variety of shapes and sizes. When individual parts of the machine are in motion, these plastic bearings can generate electrostatic charges. Figure 8 shows the test circuit. In this test, a  $C = 200\text{-pF}$  capacitor is charged to  $\pm 500\text{ V}$ , then discharged, without a series resistor, into the device under test.



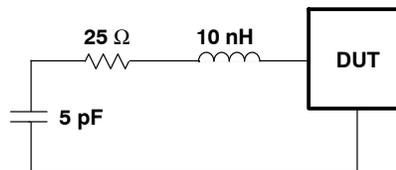
**Figure 8. Machine-Model Test Circuit**

Because the charged metal parts have a very low electrical resistance in this test circuit, no series resistor is used to limit the current. Therefore, the peak current in the device under test is significantly higher than in the previously described human-body test circuit. Whereas, in the human-body test circuit, extremely short rise times are required, as a result of the extremely low inductance of the construction used, considerably higher inductances of 500 nH are specified in the discharge circuit of the machine model. As a result, the rise time of the current and, consequently, its amplitude, are limited. Therefore, the problem of the partial overload of the protection circuit of the device under test is reduced significantly. The energy of 4  $\mu\text{W}$ s to be dissipated is considerably higher than in the machine-model test.

Because of the high energy used in this test, integrated circuits usually cannot be tested with voltages of 500 V without damaging the device under test. As a guideline, assume that components that survive, without damage, the human-body model test with a voltage of up to 2000 V, also are not damaged by a machine-model test using voltages of up to  $\pm 200$  V.

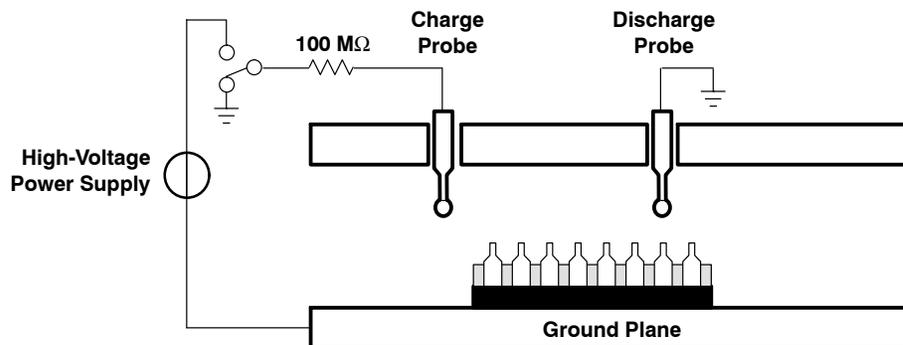
### 3.3 Charged-Device Model

Despite the informative tests conducted according to the methods described in the previous sections, in practice, damage due to electrostatic discharges also can occur during the processing of integrated circuits. It has not been possible to reproduce the profile of failures observed during processing by using normal test equipment. Intensive investigations show that electrostatic charging, and consequent discharging, of the device are responsible for the damage. Charging occurs when the integrated circuit slides along plastic transport rails before being inserted into circuit boards, and the discharge occurs when the component lands on the circuit board. Similarly, damage to the component can occur after it has been tested, when it slides from the test station onto the transport rail, and is damaged by the electrostatic charging that occurs. During testing, the integrated circuit was without fault, but it was damaged immediately afterward. Because the device package is small, the capacitances are only a few picofarads, but the inductances also are extremely low (see Figure 9).



**Figure 9. Equivalent Circuit of Discharge of the Charged-Device Model**

Therefore, in this case, still shorter rise times ( $< 200$  ps) of the current can be expected. Because the protection circuit is only partially conducting, damage to the circuit can result. The simplified test setup is shown in Figure 10.



**Figure 10. Charged-Device Model Test Setup**

The device under test is placed on its back on a metal plate. In this way, the largest possible capacitance of the circuit to the environment is attained. The circuit is charged with a moveable charging test probe and discharged with a second test probe.

Investigations have shown that integrated circuits in this test that survive charging up to 1000 V and subsequent discharging without damage, can be processed without problems in assembly machinery if the usual precautions to prevent electrostatic charging are taken. There is no correlation between the results of the human-body and charged-device model tests. Components that survive the human-body model test without damage do not necessarily behave in the same way in a charged-device test. Conversely, a successful charged-device model test gives no indication of results when a component is tested according to the human-body model.

### 3.4 Charged-Cable Model

The three test methods discussed previously have their justifications, but they do not cover all situations that might arise. A typical problem that occurs with the use of electronic equipment is related to inserting connectors attached to cables. If a user walks on a nonconducting floor with the plug on the end of a 10-m cable in their hand, the person's body and the cable become charged. When the plug is inserted in the socket of a piece of equipment, the capacitance of the cable is discharged. The capacitance of a 10-m cable is about 1000 pF, producing a charging voltage of up to 1000 V. The 500  $\mu$ Ws of energy, which must be tolerated by the integrated circuit, is many times larger than in the tests described previously. The discharge current, which is determined by the line impedance of the cable (typically 100  $\Omega$ ), is about 10 A. This current flows for a time corresponding to two signal-propagation times, namely, 100 ns. However, because of the comparatively high inductances of the connector and the line connected to it within the equipment in question, no exceptionally steep current-pulse edges arise. The problem of the partial conduction of the protection circuits is, to a large extent, eliminated. Therefore, it is possible to integrate protection circuits that survive such conditions without damage. The differential line driver and receiver interface device SN75LBC184 is a good example of a design that protects against damage due to electrostatic discharges.

### 3.5 ESD-Protection Circuits

ESD-protection circuits were first integrated into CMOS devices. The thin and, therefore, very vulnerable gate oxide of the MOS transistor makes protection against destruction as a result of electrostatic discharges essential. The protective precaution that was taken initially, and which is still the best method, is the integration of clamping diodes, which limit the dangerous voltages and conduct excess currents into regions of the circuit that are safe. The safe regions consist primarily of the supply-voltage connections. In the simplest case, the protection circuits consist of diodes that are oriented to be blocking in normal operation, and are situated between the connection to the component to be protected and the supply voltage lines (see Figure 11).

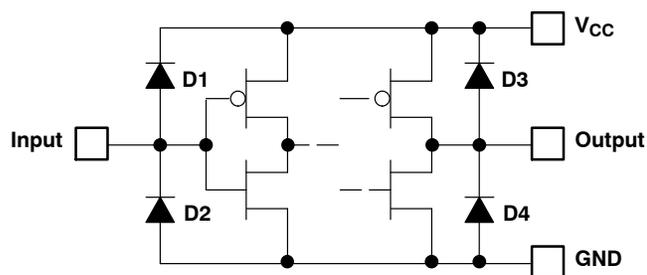
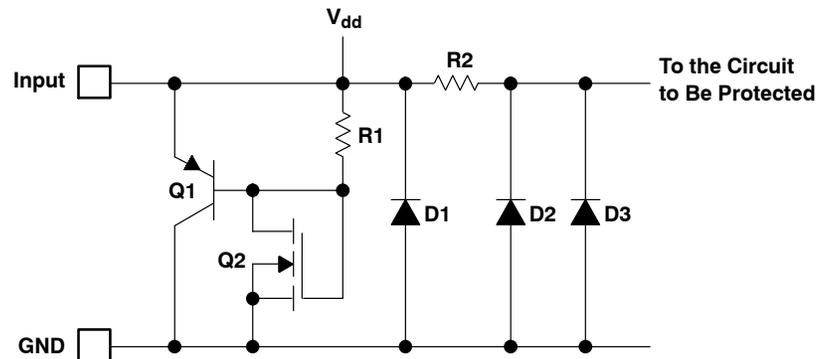


Figure 11. ESD-Protection Circuits Using Diodes

To tolerate even higher energy levels, and to protect the more sensitive parts of a circuit, two-stage protection circuits frequently are used at the inputs (see Figure 12). With this arrangement, the so-called coarse protection should conduct away the higher energy levels. In the example shown, the protective circuit against negative voltages consists of diode D1. Positive voltages are first limited by transistor Q1, which begins to conduct as soon as the input voltage ( $V_{in} > V_{dd} + 0.7\text{ V}$ ) allows current to flow through resistor R1. If the input voltage increases further, at about 22 V to 26 V, the thick-oxide MOS field-effect transistor Q2 conducts. Q2 provides additional base current to the base of transistor Q1. In this way, the energy in the interfering pulse is conducted away reliably. The fine protection circuitry, which should protect the next device (primarily the gate oxide of the transistors) from excessive voltages, consists of resistor R2 and Zener diode D3.



**Figure 12. Two-Stage ESD-Protection Circuits**

It is not practical to show all kinds of ESD-protection circuits that have been developed for every conceivable circuit configuration. The design of these parts of the circuit depends primarily on the application in which a device is used. Operational amplifiers that have, among other features, very high-resistance input circuits, use different protective circuits than, for example, interface devices for data-communications systems. In such interfaces, robustness of the device is an important characteristic.

### 3.6 Potentialities and Limitations of Protection Circuits

During design of the circuitry intended to protect an integrated circuit against destruction as a result of electrostatic discharges, the engineer must consider a number of conflicting requirements. The rate of thermal conduction in silicon is only  $1\ \mu\text{m}/\mu\text{s}$ . Therefore, the protection circuit must, at first, be able to withstand the total energy. Only later is the generated heat conducted to the surrounding circuit. By using data based on the charged-cable model, the approximate area necessary for a protection circuit that can withstand this stress should be calculated.

The formula for the temperature increase of a body, in this case the active protection circuit, is:

$$\Delta T = \left( \frac{1}{V \times C_s} \right) E \quad (1)$$

Where:

$\Delta T$  = Temperature increase

$V$  = Volume of the body to be heated

$C_s$  = Thermal capacitance of silicon = 1.89 Ws/(cm<sup>3</sup> × K)

$E$  = Injected energy

Assuming that, following a discharge, a temperature increase ( $\Delta T$ ) of 150 K is permissible, and an energy ( $E$ ) of 500  $\mu$ Ws is injected, thus:

$$150 \text{ K} = \left( \frac{1}{V \times 1.89 \text{ Ws}/(\text{cm}^3 \times \text{K})} \right) 500 \mu\text{Ws} \quad (2)$$

Therefore, the necessary volume of the protection circuit is:

$$V = \frac{500 \mu\text{Ws}}{150 \text{ K} \times 1.89 \text{ Ws}/(\text{cm}^3 \times \text{K})} = 1.76 \times 10^{-3} \text{ mm}^3 \quad (3)$$

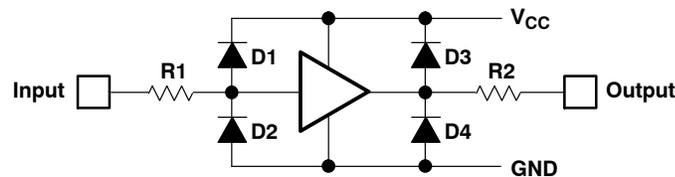
The injected energy is converted into heat in the very thin depletion layer of the protection circuit. If a thickness ( $D$ ) of 2  $\mu$ m for the depletion layer is assumed, the necessary area ( $A$ ) of this part of the circuit is:

$$A = \frac{V}{D} = \frac{1.76 \times 10^{-3} \text{ mm}^3}{2 \mu\text{m}} = 0.88 \text{ mm}^2 \quad (4)$$

Such areas can be implemented in integrated circuits. However, when the total area of an integrated circuit is only a few square millimeters, this part of the circuit has a significant influence on the cost of the component. Also, large-area protection circuits significantly influence the characteristics of an integrated circuit. The protection circuits increase significantly the input capacitance of the circuit, and cause an increase in the leakage current of the input circuit. Input leakage current is an important consideration, especially for operational amplifiers, in which extremely high-resistance inputs are required. Therefore, the ESD-protection circuit characteristic could be a disadvantage for the intended implementation of a device.

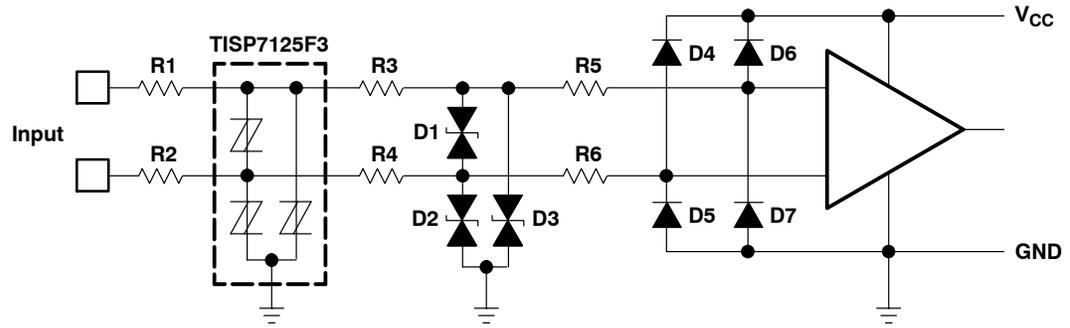
### 3.7 External Protection Circuits

Despite all the care semiconductor manufacturers take in the development of protection circuits, not every conceivable situation that might arise in practice can be addressed. Users might need to take additional precautions using circuit-design techniques similar to those already discussed. In the example shown in Figure 13, excessive voltages at inputs and outputs are limited by additional diodes D1 through D4. These diodes should have a low forward voltage, even at high currents. If required by the application, this may extend into the range of several amperes. Series resistors R1 and R2 should limit the currents. Usually, there is no difficulty in choosing a suitable resistor for the input circuit. Resistor values of 1 k $\Omega$  to 10 k $\Omega$  usually are appropriate. In practice, it usually is adequate to use only a high-value resistor, without additional diodes. Together with the input capacitance of the subsequent circuit, the resistor provides a low-pass circuit that sufficiently slows down the fast rise times that can occur with electrostatic discharges. The choice of a suitable resistor at the outputs of the circuit to be protected can be more difficult. An important characteristic of outputs is that they have a low resistance because they are intended to drive heavy loads, for example, long lines. In this case, matching the output resistance to the line impedance is usually a sufficient protective precaution, this being commonly necessary for other reasons. The resulting value of the resistor lies in the range of only 33  $\Omega$  to 200  $\Omega$ . A resistor of this kind also protects a circuit sufficiently against the kind of disturbances that arise with the charged-cable model.



**Figure 13. Protection Circuits for Integrated Circuits**

The nuclear electromagnetic pulse (NEMP) was considered to be of particular significance at the time of the Cold War, under the threat of the nuclear conflict that might have occurred. As a result of the Compton effect, a nuclear explosion high above the surface of the earth (up to 80 km) would give rise to an electromagnetic pulse that could destroy electrical and electronic installations within a radius of hundreds of kilometers. However, comparatively trivial events also are able to cause similar damage on a local basis. Events of this kind include lightning strikes during a storm (LEMP, or lightning electromagnetic pulse). In close proximity to a lightning strike, voltages of several thousands of volts and currents of many hundred amperes can be induced into nearby conductors. Electronic equipment that should operate in such an environment must be protected from destruction by suitable precautions. Equipment in this category includes telecommunication and data-transmission installations, together with measuring equipment which, because of the functions it performs, may be particularly threatened by phenomena of this nature. It is obvious that the protection circuits previously described are inadequate under these conditions. For applications of this kind, special voltage limiters that can cope with currents and voltages of the magnitude previously mentioned have been developed. Figure 14 shows an example of the protection circuit for the input of an operational amplifier.



**Figure 14. Protection Circuit for Extreme Requirements**

Three-stage protection circuits are suitable for applications of this kind. The first limiting stage, consisting of the voltage limiter TISP7125F3, drains away currents on the order of several hundreds of amperes. In the second limiter stage, voltage-limiting diodes D1 through D3 (transient-voltage suppressors) lead off currents in the range of amperes. The third stage of the protection circuit is formed by the diodes D4 through D7. In most cases, at this point, the ESD-protection circuits already included in the integrated circuits are adequate. With the circuit concept shown in Figure 14, the input of the differential amplifier is protected against both unipolar and differential interference. In the mechanical construction of the system circuit, care must be taken in choosing suitable grounding points, so that currents caused by the interference are kept away from the circuit to be protected. The high current-carrying capacity of the conductors allows the use of low values for resistors R1 through R6. Therefore, this circuit concept also is suitable for protecting outputs.

## 4 Parasitic Transistors in Integrated Circuits

Because the parasitic transistors in CMOS integrated circuits form thyristors, they might be responsible for latch-up of the circuit. Bipolar and MOS circuits also contain additional parasitic transistors which, although not endangering the device, can affect the correct functioning of the circuit. Figure 15 shows a simplified representation of the relationships in a bipolar integrated circuit. A P-doped substrate, which is connected with the most-negative polarity of the voltage supply (GND) to the circuit, contains the N-doped collector of the npn transistor. In this region, the P-doped base and the N-doped emitter are diffused in, one after the other. Beside this transistor is a clamping diode that consists of the N-doped cathode in the P-doped substrate (anode). In addition to these intended components, an unwanted parasitic npn transistor is created, as shown in Figure 15.

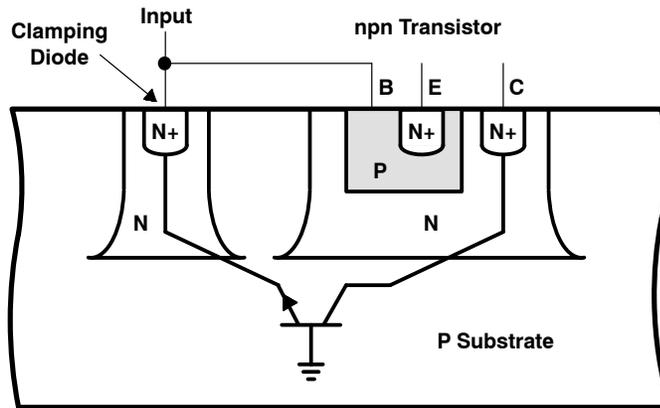


Figure 15. Parasitic Transistors in Bipolar Circuits

Figure 16 shows the complete input circuit, including the parasitic transistor. If a voltage ( $\approx -0.7$  V) is applied to the input of this circuit that brings this transistor into a conducting state, an unwanted current flows from the input into the collector circuit of the input transistor.

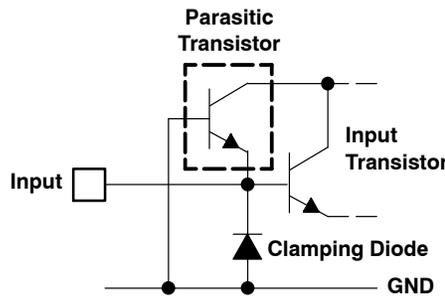
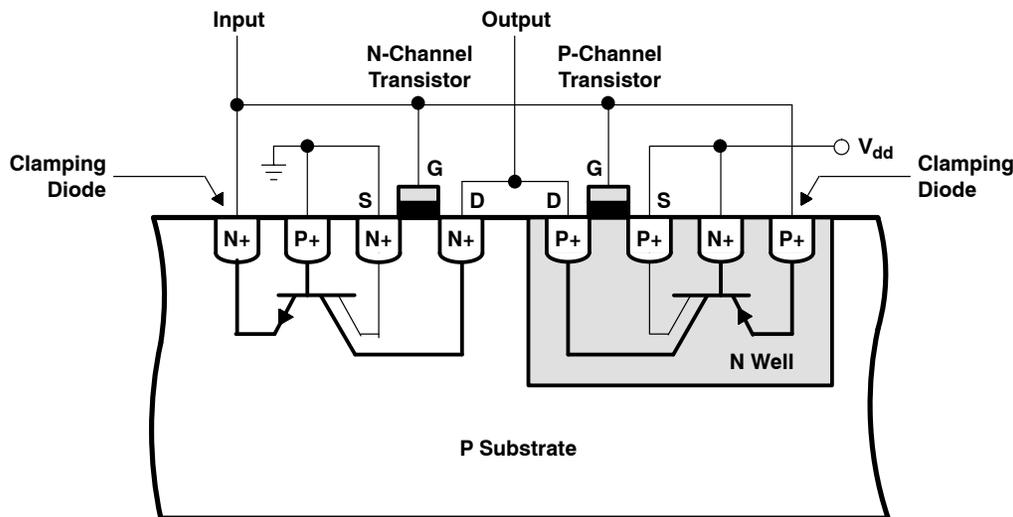


Figure 16. Input Circuit With Parasitic Transistor

The parasitic transistors in CMOS circuits are responsible for the potential latch-up effect that can occur with these components. However, far below the trigger threshold of the parasitic thyristors, the individual parasitic transistors begin to have undesirable effects on the behavior of the integrated circuit. Figure 17 shows the inside a CMOS circuit. A simplified input stage is shown in which the clamping diode, with the P-doped substrate and the N-doped region of an adjacent N-channel MOS transistor, forms a parasitic npn transistor. In this case also, negative voltages at the inputs of the circuit can result in unpredictable behavior by the component. With complementary MOS circuits, parasitic pnp transistors also are in the complementary part of the circuit, and these become active if the input voltage becomes more positive than the supply voltage by an amount equal to their base-emitter forward voltages.



**Figure 17. Parasitic Transistors in CMOS Circuits**

If the input and output voltages are more positive than the ground connection (GND) and more negative than the positive supply voltage connection ( $V_{CC}$  or  $V_{dd}$ ) to the circuit, as recommended in the data sheet, the parasitic transistors remain switched off. The proper operation of the circuit can be ensured. However, if a voltage that lies outside the previously stated limits is applied to the input of a circuit, the parasitic transistors switch on. Under these circumstances, the correct function of the circuit cannot be ensured. The parasitic transistors shown are only a few of the many in an integrated circuit. Under the conditions described previously, it is easy to provoke any number of undesirable reactions in an integrated circuit.

With analog circuits in particular, this behavior quickly can lead to serious malfunction of the circuit. Usually, analog circuits are constructed to have very high resistance. As a result, even the smallest currents are able to have an adverse influence on, for example, the apparent offset voltage of a differential amplifier. The only effective way to avoid these effects consists of keeping the input and output voltages of a circuit within a range that prevents unwanted switching on of the parasitic transistors. With analog integrated circuits, the data sheets, therefore, specify a range of input voltage:

$$-0.3 \text{ V} \leq V_{in} \leq V_{CC} + 0.3 \text{ V} \quad (5)$$

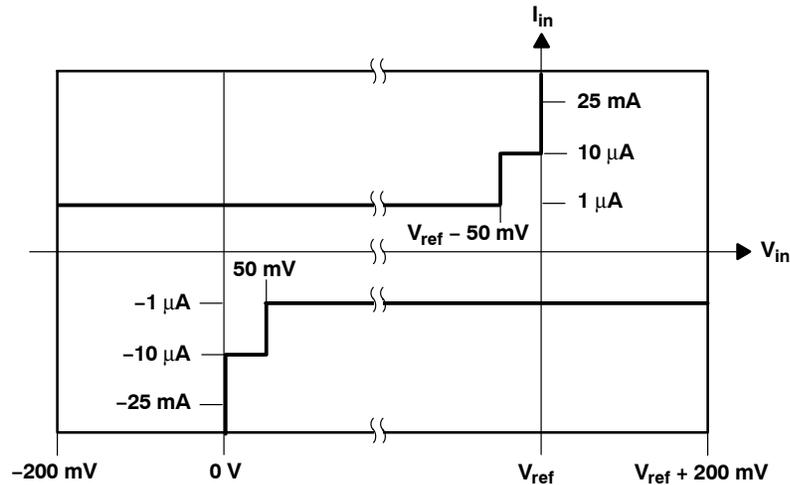
This specification accounts for the fact that the base-emitter diode of a transistor becomes conducting with voltages applied that are significantly less than 0.7 V. However, the base-emitter voltage of a transistor reduces with increasing temperature; therefore, the voltage limits must be considerably narrower.

The semiconductor manufacturer is limited in reducing the influence of the parasitic transistors. Sensitivity can be reduced by situating critical parts of a circuit as far as possible from each other. This results in reduced current gain of the parasitic transistors and, thus, sensitivity of the component. The integration of the guard rings described previously is an additional technique to improve the behavior of the circuit under abnormal operating conditions. However, as already shown, this does not eliminate the parasitic transistors; only their current gain is reduced and, therefore, also the probability that the component could show undesirable behavior under certain conditions.

#### 4.1 Precautions to Protect Analog Circuits

Usually, within a system, it is simple to maintain the required voltage limits, ensuring the correct functioning of the integrated circuits. However, the relationships at the interfaces of the equipment to the outside world often are unpredictable. At these interfaces, significant interference voltages must be expected and, in some cases, may far exceed the limits discussed previously. Nevertheless, correct operation of the equipment must be ensured. The precautions mentioned previously, which should help prevent occurrences, such as destruction resulting from an electrostatic discharge, usually are ineffective at this point. The precautions limit the input and output voltages of the component in question to the extent that damage can be prevented with certainty. However, these protection circuits depend largely on the limiting properties of diodes; therefore, they are unable to prevent an interfering voltage from being generated at the inputs or outputs of the circuit that, briefly, exceeds the required limits. In such a case, attention should be paid less to the interference at the input of an integrated circuit; the output of this channel does, in such a case, show an incorrect result. It is more important to prevent other elements in the component, for example, in a double operational amplifier, from functioning incorrectly. Thus, taking additional precautions is prudent.

The use of silicon diodes is inadvisable because of their high forward voltage ( $V_f = 0.7 \text{ V}$ ); also, Schottky diodes ( $V_f = 0.4 \text{ V}$ ) cannot be used because of their comparatively high forward voltage. Germanium diodes are the most suitable from the point of view of forward voltage ( $V_f = 0.3 \text{ V}$ ), but must be excluded because of their limited temperature range ( $T_{\max} = 90^\circ\text{C}$ ) and because they are difficult to obtain. To support applications of this kind, Texas Instruments has made available a special limiter circuit<sup>2</sup> (TL7726). In the TL7726 integrated circuit, the limiting function no longer is performed with simple diodes, but by transistors. By appropriately feeding the bases of these transistors, negative input voltages are limited to values  $> -0.2 \text{ V}$ . Positive input voltages are limited to a value that is  $< 0.2 \text{ V}$  more positive than the reference voltage connection ( $V_{\text{ref}}$ ) of this integrated circuit. This connection usually is made to the supply voltage connection of the circuit to be protected. Figure 18 shows the characteristics of this limiter, which is at an extremely high resistance within the working range of the circuit to be protected. Thus, the input current of the limiter, with an input voltage  $50 \text{ mV} \leq V_{\text{in}} \leq V_{\text{ref}} - 50 \text{ mV}$ , is less than  $1 \mu\text{A}$ . However, if the input voltage exceeds the value of the reference voltage or goes below ground potential, larger currents also are reliably diverted.



**Figure 18. Characteristics of Voltage Limiter TL7726**

The operation of this voltage limiter can be explained simply. The voltage limiter is connected in parallel with the inputs of the component to be protected (see Figure 19). In addition, a resistor ( $R_s$ ) must be inserted in each input line to limit the input current to an acceptable value. There is usually no difficulty choosing a suitable resistor; the high input resistance of modern operational amplifiers and analog-to-digital (A/D) converters simplifies the choice of an appropriate component. However, the limiter circuit has a comparatively high input capacitance which, together with the series input resistance  $R_s$ , influences the upper frequency limit of the complete circuit. In addition, digital-to-analog (D/A) converters, which contain a capacitor network in the conversion part of their circuitry, contribute an additional comparatively high input capacitance. This increases still further the low-pass characteristics of the protection circuit. The TL7726 limiter tolerates high peak currents of short duration, making possible the use of low-ohmic-value input resistors.

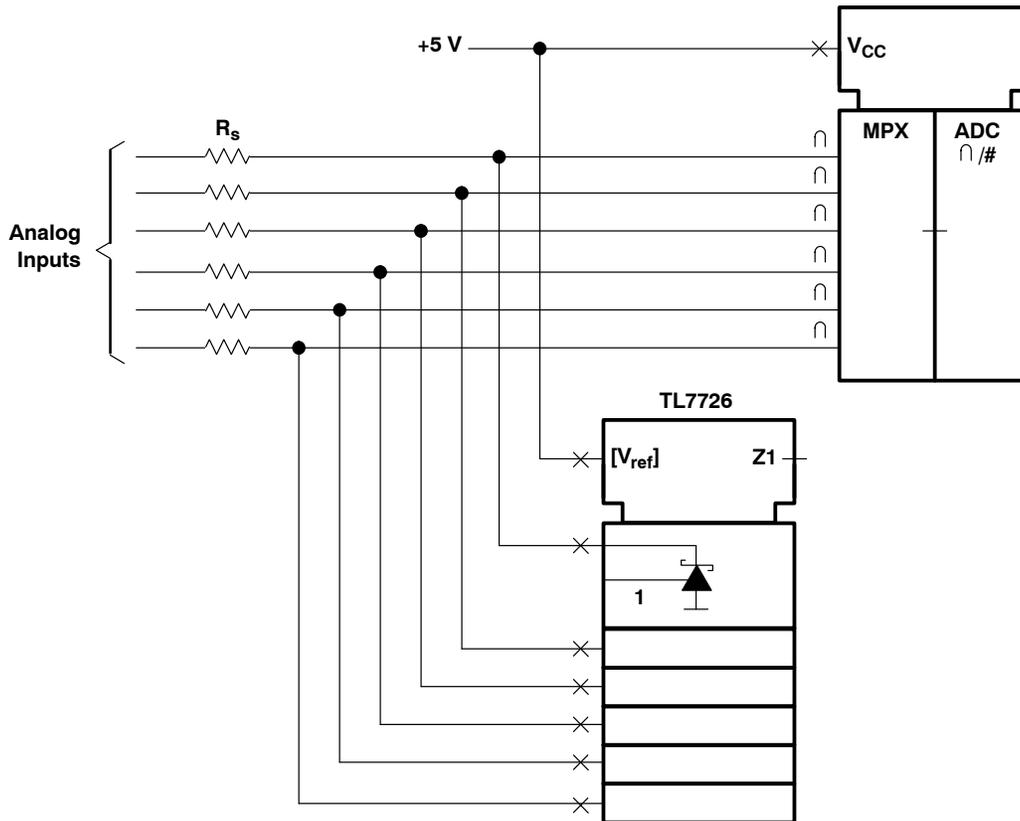


Figure 19. A/D Converter With Limitation of the Input Voltage

### 4.2 High-Frequency Effects

Analog circuits usually have limited bandwidth. Thus, the transit frequencies ( $f_T$ ) of operational amplifiers are only a few megahertz. From this point of view, a disturbance to the operation of these components as a result of high-frequency signals should be unlikely. In practice, cases can arise of a disturbance to the circuit as a result of interfering signals, the frequency of which might be several hundred MHz. On closer examination, the component has not been disturbed directly by the high-frequency radiation. Instead, the high-frequency interfering signal that is received by the connection lines that operate as an antenna is rectified by the nonlinear P-N junctions in the semiconductor. These junctions include, for example, the diodes in the protection circuits of the integrated circuits that are affected (see Figure 20). The nonlinear input characteristic of an amplifier can cause it to function as a rectifier for high-frequency voltages or currents as a result of the audion effect. The dc voltage generated at this point can shift the working point of a circuit significantly, putting the correct operation of the circuit into question.

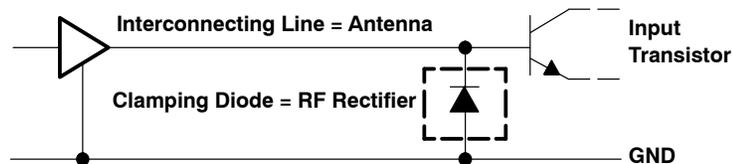


Figure 20. Rectification of High-Frequency Interference Signals

Precautions to counter the effects described here include all possible methods for high-frequency decoupling of critical parts of the circuit. These precautions comprise adequate screening of the sensitive parts of the circuit. Insertion of low-pass filters in sensitive input lines to attenuate high-frequency signals also can be effective.

### 4.3 Behavior of Logic Circuits

Parasitic transistors also are found in logic circuits, but the danger of a possible malfunction of the component as a result of unintentional switching on of a parasitic transistor is significantly less than with analog circuits. It is not that the parasitic transistors are less sensitive, rather, the high noise margin that is common to all digital circuits is advantageous. Whereas, with analog circuits, even the smallest currents that circulate in the substrate of the circuit can cause serious errors in the output signal, with logic circuits, considerably higher currents are necessary to produce an incorrect logic level. In addition, semiconductor manufacturers take additional precautions in the form of additional guard rings to exclude, as far as possible, the influence of parasitic transistors on the inputs and on the outputs of these devices.

Reflections that occur at the ends of lines that have not been terminated correctly cause overshoots and undershoots at the inputs and outputs of logic circuits. Figure 21 shows the waveforms at the beginning and end of an open-circuit line having a characteristic impedance of  $Z_o = 50 \Omega$ , which is controlled by an SN74LVT244 device<sup>3</sup>. Because the end of the line is not terminated correctly, large overshoots and undershoots occur at this point. In theory, the amplitude would be double the voltage at the beginning of the line. As Figure 21 shows, reflections produce such overshoots and undershoots at the beginning of the line.

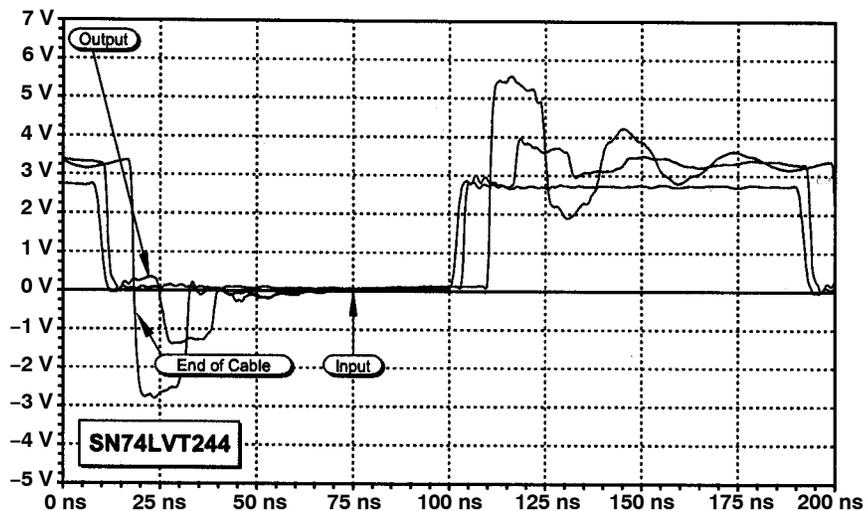


Figure 21. Waveforms on an Open-Circuit Line

In practice, clamping diodes limit the overshoots and undershoots in the integrated circuits to which they are connected. These diodes must be able to pass relatively high currents without compromising the function of the component. The amplitude of current  $I_D$  in the clamping diode can be calculated using equation 6.

$$I_D = \frac{2 \times V_{CC} \times \frac{Z_o}{R_o + Z_o} - (V_{CC} + V_{fD})}{Z_o + R_{fD}} \quad (6)$$

Where:

- $V_{CC}$  = Supply voltage
- $Z_o$  = Characteristic impedance of the line
- $R_o$  = Internal resistance of the line driver
- $V_{fD}$  = Forward voltage of the clamping diode ( $\approx 0.7$  V)
- $R_{fD}$  = Differential resistance of the clamping diode

Without introducing any serious error, it can be assumed that  $R_o \ll Z_o$ , and  $R_{fD} \ll Z_o$ . This simplifies equation 6 to:

$$I_D = \frac{V_{CC} - V_{fD}}{Z_o} \quad (7)$$

With a supply voltage of  $V_{CC} = 3.3$  V and a characteristic impedance of  $Z_o = 30 \Omega$ , which are found in typical bus systems, the result is:

$$I_D \approx \frac{3.3 \text{ V} - 0.7 \text{ V}}{30 \Omega} \approx 80 \text{ mA} \quad (8)$$

Integrated-circuit design engineers lay out the clamping diodes, and the guard rings that surround them, so that currents that flow in the clamping diodes (and thus, inevitably, also in the substrate of the circuit) can be calculated to have approximate values of the magnitude in equation 8 and cause no malfunction of the circuit. This assumes that a switch-on duration of the current of only a maximum of 100 ns with a duty cycle  $< 10\%$  is permitted. This limitation does not affect the logic circuits, because the overshoots and undershoots exist for only a fraction of the period of the wanted signals. The limitation of the switch-on time also makes it possible to keep the area needed for the necessary guard rings within acceptable limits. Because the transit frequency of the parasitic transistors is only about 1 MHz, shorter pulses in the range of nanoseconds are unable to switch on these parasitic transistors. During testing, without powerful pulse generators, a direct-current test usually is performed. A current of  $I_D = 3$  mA is injected into the clamping diodes for a duration of  $t_d = 10 \mu\text{s}$  to  $20 \mu\text{s}$ . Extensive investigations show that, with 3 mA/10  $\mu\text{s}$ , this test correlates sufficiently accurately to the assumed operating conditions of 80 mA/100 ns.

## 5 Summary

An adequate understanding of both the characteristics and the limitations of integrated circuits is necessary to develop a system that operates reliably under the required conditions. The information given in semiconductor device data sheets often is insufficient to answer all questions. This application report discusses relevant problems not covered in the data sheets, such as the latch-up effect in CMOS circuits. That semiconductor manufacturers take extensive precautions to prevent these problems arising in integrated circuits is reason enough for the design engineer to become acquainted with them. Care was taken in preparing this application report to differentiate between the latch-up effect and other phenomena, which arise for completely different reasons, but are called latch-up. The situation is different with the immunity of integrated circuits to electrostatic discharges. Many test methods have been developed to realistically test the robustness of devices. However, all of these tests can provide an answer only under particular operating conditions. Therefore, users must use data from the manufacturer to reach conclusions about the suitability of components in a specific situation and to take additional precautions as necessary.

The existence of so-called parasitic transistors in semiconductor devices can cause operational problems of which users should be aware. The basic cause of these problems has been examined in detail, together with the possible manifestation of parasitic transistors in actual circuits. The discussion on parasitic transistors concluded with several precautions in system design that can be taken to solve the latch-up problem.

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Additional information on this subject:

4. Texas Instruments, *Digital Design Seminar Manual*, literature number SDYDE01A.
5. Texas Instruments, *Data Transmission Seminar Manual*, literature number SLLDE01C.
6. Texas Instruments, *Linear Design Seminar Manual*, literature number SLYDE05.
7. Texas Instruments, *Logic Application Reports and Product Selection CD-ROM*, literature number SDZE01A.
8. Texas Instruments Internet site: <http://www.ti.com>

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# ***Flexible Voltage-Level Translation With CBT Family Devices***

SCDA006  
July 1999



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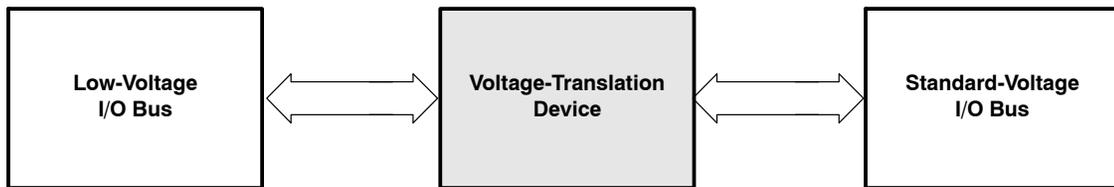
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## Abstract

Voltage translation between buses with incompatible logic levels can be accomplished using Texas Instruments (TI™) translation-voltage clamps (TVC) or standard crossbar technology (CBT) devices. CBT devices in this application offer flexibility in designs, protection of circuits that are sensitive to high-state voltage-level overshoots, and cost efficiency.

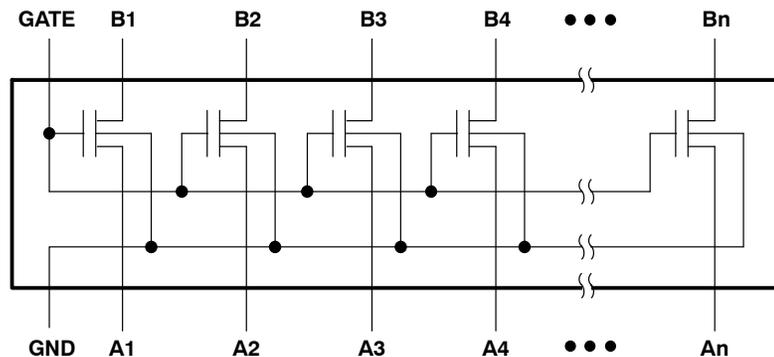
## Introduction

In designing electronics systems, proper interfaces between buses with incompatible logic levels must be provided. Voltage-level translation is necessary to allow the interconnection with flexibility to provide a future migration path to lower-voltage input/output (I/O) levels (see Figure 1). TI offers I/O voltage translation solutions with two device families.



**Figure 1. Flexible Voltage-Translation Application**

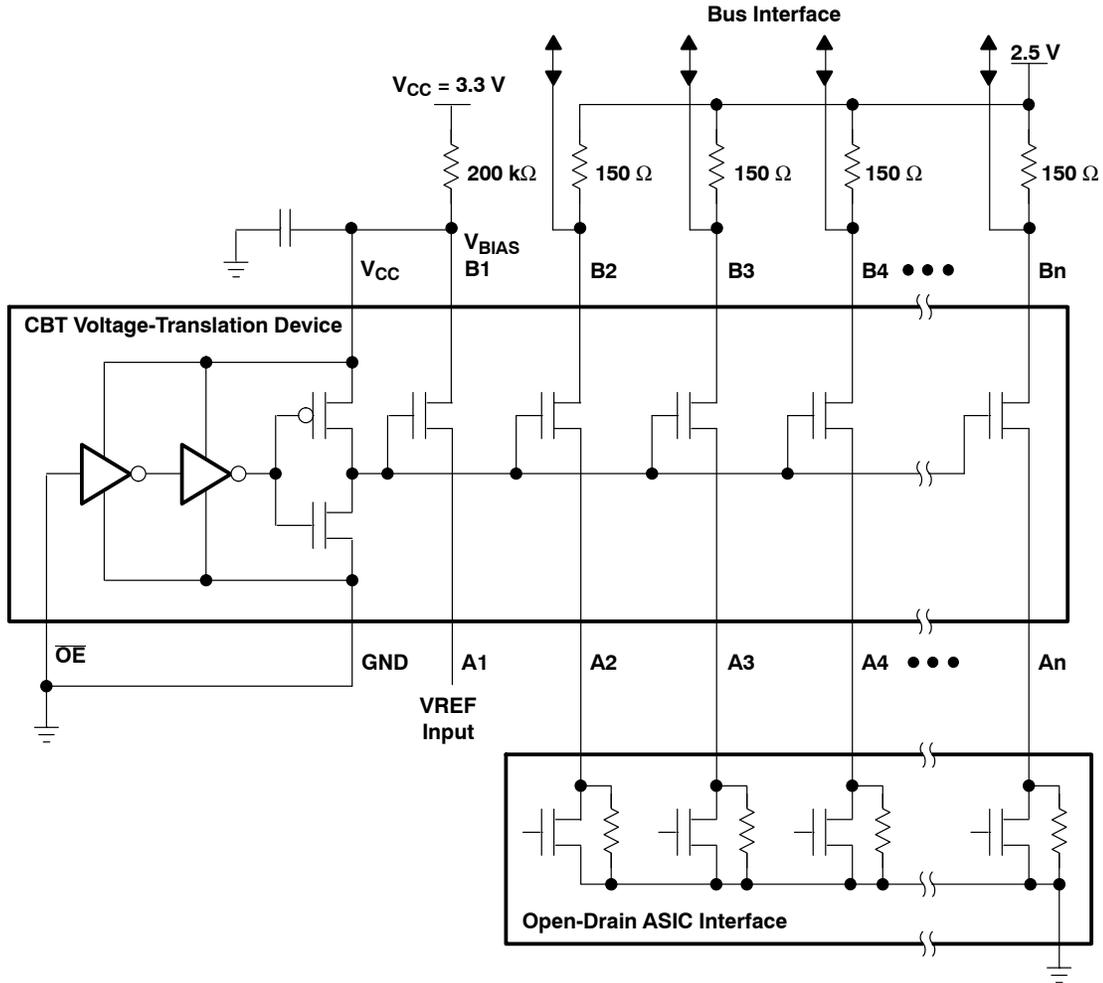
One possible solution for flexible voltage translation is the TI translation-voltage clamp (TVC) family that has been designed specifically for protecting sensitive I/Os (see Figure 2). The information in the data sheet for each TVC-family device describes the I/O protection application of the TVC family and should enable the design engineer to successfully implement an I/O protection circuit utilizing the TI TVC solution.



**Figure 2. Simplified Schematic of a Typical TVC-Family Device**

A comparable solution, allowing cost-effective and flexible voltage translation implemented with standard crossbar technology (CBT) family devices is described in this application report.





**Figure 4. Typical Application of CBT as a Voltage-Translation Device**

### Conclusion

TI offers a line of CBT devices, including standard, Widebus™, dual-bit, and single-bit functions. The flexibility of CBT enables a low-voltage migration path for advanced designs to align with existing industry standards. The TI CBT family provides the designer with a solution for voltage-level translation and protection of circuits with I/Os that are sensitive to high-state-voltage-level overshoots.

### Acknowledgment

The authors of this application report are Thomas V. McCaughey, Stephen M. Nolan, and John D. Pietrzak.



# **Texas Instruments Solution for Undershoot Protection for Bus Switches**

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## **ABSTRACT**

Three solutions for undershoot protection (Schottky diode, charge pump, and active clamp) are discussed. Their advantages and disadvantages are presented, as well as a comparison of significant characteristics of each solution. Laboratory test data confirm the superior performance of the TI device with the active-clamp undershoot-protection feature.

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## Introduction

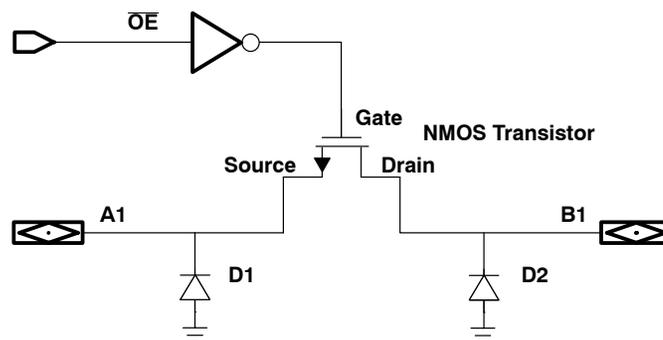
The TI™ CBT/CBTLV bus-switch family has become an indispensable solution in high-performance personal-computer (PC), data-communications, and consumer applications. In some applications, due to various system design techniques, undershoot events occur. This undershoot forces the switch on, intermittently, over a short time interval. When a bus switch is disabled, an input undershoot that exceeds its threshold voltage  $V_T$  can turn on the pass transistor. This unwanted condition causes severe data errors on the outputs.

TI has a new, active-clamp undershoot-protection feature in the bus-switch family, designated K, i.e., CBTK. This application report discusses various options for undershoot protection, including their advantages and disadvantages. Laboratory test results demonstrate the superior performance of the new CBTK devices with the undershoot-protection feature.

## Background

### What Happens to the Bus Switches When Undershoot Occurs

The bus switch consists of a large, but simple, NMOS transistor that passes data. Figure 1 illustrates a simple bus switch. The gate of the NMOS transistor is controlled by an enable signal. When the gate voltage is low, the switch is off.

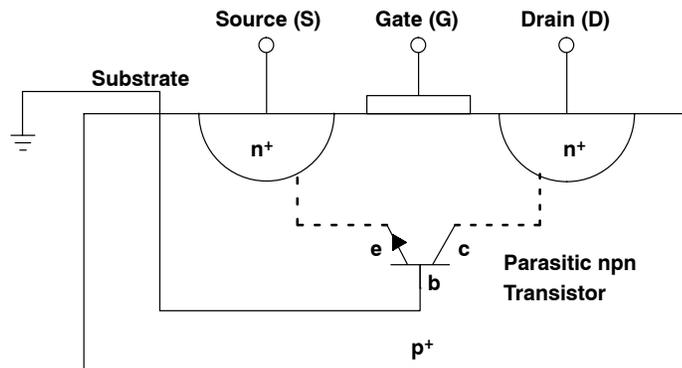


**Figure 1. Basic NMOS-Transistor Bus Switch**

When the gate voltage is high, the switch is on. The threshold voltage  $V_T$  of an NMOS transistor is approximately +650 mV. When  $V_{GS}$  (gate-source voltage,  $V_G - V_S$ ) is greater than  $V_T$ , the switch is turned on. In the enabled state, undershoot is not a problem. But, when the switch is disabled, a negative voltage on the bus could turn on the switch, causing a data error.

Two different situations can exist when undershoot occurs. The first situation occurs when the source node voltage ( $V_S$ ) becomes lower than the gate voltage ( $V_G$ ). Any undershoot on the source node ( $V_S$ ) greater than or equal to +650 mV creates a positive  $V_{GS}$ , which is greater than  $V_T$ . This turns on the switch, and the two buses are no longer isolated. Corruption of data is inevitable.

In the second situation, a parasitic npn transistor is formed in the NMOS transistor during manufacturing. Figure 2 shows the cross-sectional view of an NMOS transistor. The emitter is the n<sup>+</sup> source/drain implant, the base is the p-type substrate, and the collector is the n<sup>+</sup> source/drain implant. When undershoot below ground occurs on the source node, because the substrate is at 0 V, a positive  $V_{be}$  is created on the parasitic npn transistor and causes the transistor to conduct. With  $\beta$  of approximately 10, a small amount of base current generates enough collector current to establish a continuous flow from collector to emitter, i.e., from drain to source. So the switch is on again, instead of being off, creating a major data error.



**Figure 2. Cross-Sectional View of an NMOS Transistor**

## Undershoot Event Cases

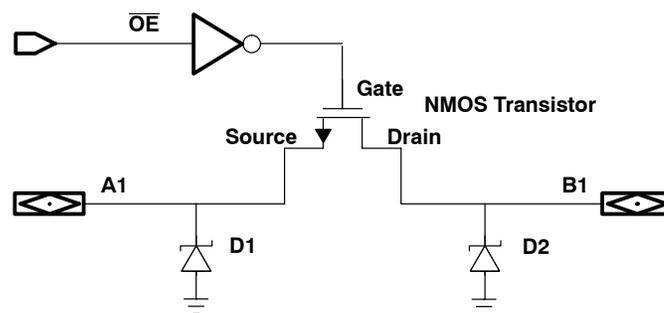
Termination is an important consideration in signal integrity. Usually, undershoot occurs when a bus is not terminated or is poorly terminated. Signals with very fast edge rates also can degrade signal quality by generating undershoots. Good transmission-line designs can resolve these issues, but some systems, such as a PCI bus, are designed to have a reflected wave. To achieve very high speed using low power, the PCI bus is not terminated. Reflections are not eliminated, by design, but reflections are expected. These reflections can cause severe undershoot conditions that force the bus switch to function improperly.

## Techniques for Undershoot Protection

Three main techniques provide undershoot protection: Schottky-diode solution (CBTS), charge-pump solution (none), and active-clamp solution (CBTK). TI, as a world leader in bus-switch technology, designed the CBTK devices to solve undershoot problems. This active clamp feature offers excellent protection against high-current undershoot events. The comparisons in the following paragraphs prove CBTK to be the best solution for undershoot protection.

### Schottky-Diode Solution

Figure 3 shows the basic NMOS crossbar switch with Schottky diodes. The n-channel pass-transistor source and drain are connected to two different buses. The gate of the pass transistor is controlled by the  $\overline{OE}$  signal that is generated from the output-enable circuit. When the gate voltage is high, the switch is closed. When the gate voltage is low, the switch is open. The undershoot event does not affect performance of the switch when the switch is on. But, if undershoots occur when the bus switch is off, passing unwanted data can cause a data error. To prevent this, two Schottky diodes are connected from the source and drain to ground. When one of the buses has negative voltage that exceeds the forward turnon voltage of the Schottky diode, the diode turns on and clamps the source or drain voltage of the NMOS switch, keeping the buses isolated.



**Figure 3. Basic NMOS Switch With Schottky-Diode Clamps**

A Schottky diode clamp has the following advantages and disadvantages:

- Advantages
  - Low power requirement
  - Some undershoot protection
  - Bidirectional, both ports protected
- Disadvantages
  - Slow to react to undershoot voltages with fast edge rates. This could cause the n-channel pass transistor to turn on and affect the buses.
  - No effect on the parasitic npn transistor. Because the parasitic transistor's base is the substrate that is at ground, the undershoot turns on the transistor and a large current corrupts the data.
  - Significant addition of input/output capacitance

## Charge-Pump Solution

In this implementation, a charge pump with a negative voltage controls the substrate voltage and the gate voltage of the transistor. During an undershoot event, the charge pump keeps the gate voltage and the substrate voltage negative, so both of them are off.

The advantages and disadvantages of the charge pump are:

- Advantages
  - Excellent undershoot protection
  - Lower input/output capacitance
  - Low  $I_{off}$
  - Bidirectional, both ports protected
- Disadvantages
  - Significantly high  $I_{CC}$
  - Higher cost due to chip size increase for the charge-pump circuit

## Active-Clamp Solution

This technology integrates an active-clamp undershoot-protection circuit on both ports. In the active-clamp circuit, a bias generator sets a voltage slightly above ground, which allows the active-clamp pullup voltage to turn on during an undershoot event. This clamp counteracts the undershoot voltage and limits  $V_{GS}$ ,  $V_{GD}$  of the n-channel, and  $V_{be}$  of the parasitic npn transistor. Figure 4 shows the basic NMOS switch with active-clamp pullup circuits.

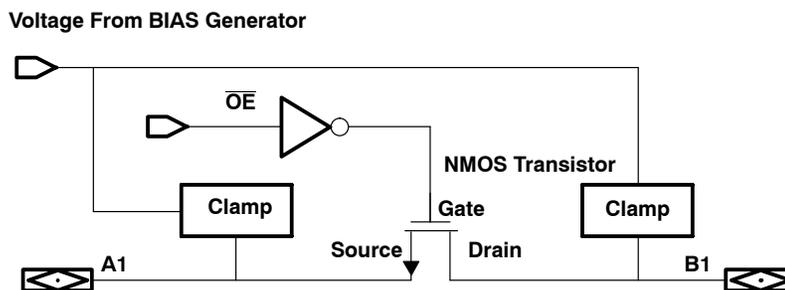


Figure 4. Basic NMOS Switch With Active-Clamp Pullup Circuits

Advantages and one disadvantage of the active-clamp solution are:

- Advantages
  - Excellent undershoot protection
  - Capacitance is low. Minimal capacitance is added.
  - Overvoltage-tolerant I/Os
  - Faster enable/disable switching speed than the Schottky solution
  - Less power required
  - Low  $I_{off}$
  - Both ports protected
- Disadvantage
  - Chip-size increased

Table 1 provides a comparison of significant characteristics of these three undershoot-protection technologies. Different techniques of undershoot protection provide varying degrees of protection with different tradeoffs.

The comparison in Table 1 indicates that the Schottky-diode solution handles only minimal-undershoot events.

The charge-pump solution provides excellent undershoot protection, but has high  $I_{CC}$  and high power consumption. Therefore, it is not ideal for mobile and power-consumption-sensitive applications.

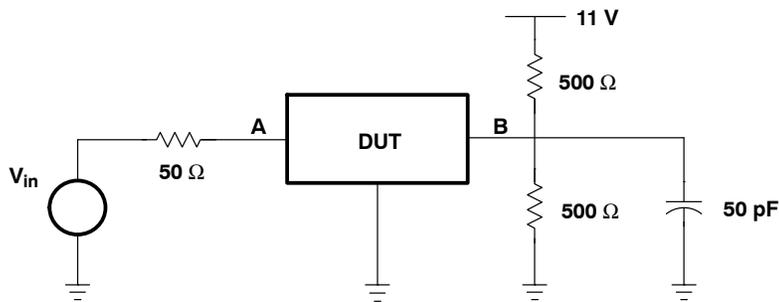
The active-clamp solution provides excellent undershoot protection and consumes less power. Moreover, it is overvoltage tolerant, which allows compatible operation in mixed-voltage systems.

**Table 1. Comparisons of Undershoot-Protection Technologies**

CHARACTERISTICS	SCHOTTKY DIODE (CBTS)	CHARGE PUMP	ACTIVE CLAMP (CBTK)
Undershoot protection	Good. Protection on both ports slows to react with fast edge rates. No effect on parasitic transistor.	Excellent protection on both ports	Excellent protection on both ports
$I_{CC}$	Low ( $\leq 10 \mu A$ )	Very high ( $> 100 \mu A$ )	Low ( $\leq 20 \mu A$ )
Capacitance	High (9 pF)	Low (5 pF)	Low (5 pF)
$I_{off}$	No $I_{off}$ specification	Low (10 $\mu A$ )	Low (10 $\mu A$ )
Overvoltage tolerance	No	No	Yes

## Laboratory Comparison of Various Device Options

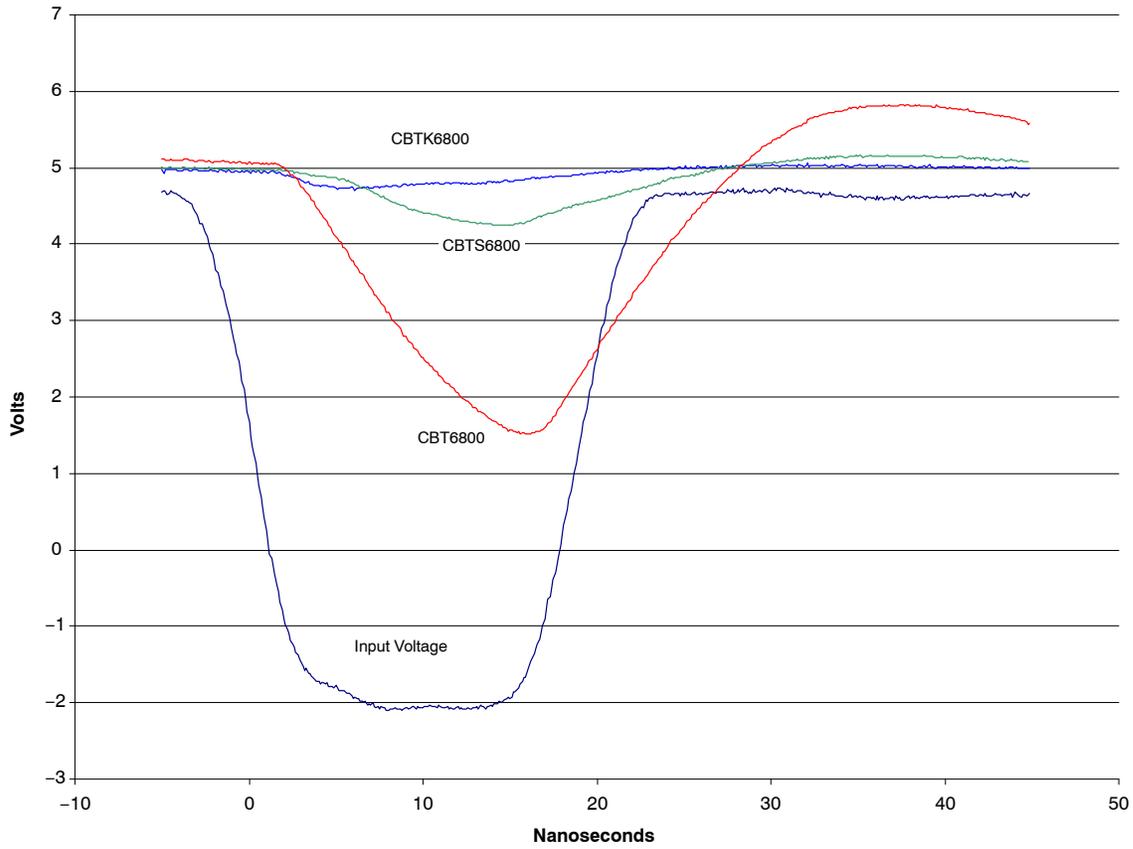
Laboratory testing demonstrated the excellent undershoot-handling capability of the active-clamp circuit (CBTK). Figure 5 shows the test setup. Three devices (CBT6800, CBTS6800, and CBTK6800) were tested with one output switching. A valid high logic level is established on port B by charging a load capacitor on port B to 5.5 V. The bus switch was disabled and an input with an undershoot of  $-2$  V and 20-ns pulse duration was applied. The output of each device was recorded. The standard CBT6800 device turned on as soon as the undershoot event occurred and the capacitor discharged. The Schottky-diode version (CBTS6800) turned on slowly and discharged the capacitor. In contrast, the CBTK effectively clamped the undershoot and maintained excellent signal integrity on port B.



**Figure 5. Test Setup for the Undershoot Test**

Figure 6 shows the output waveforms from the test. The active-clamp solution performance is much superior compared to the standard product without the clamping feature. The CBTS offers minimal protection. TI provides bus switches with Schottky diodes (CBTS) and active-clamp undershoot-protection (CBTK) features.

Due to an undesirably high  $I_{CC}$ , the charge-pump solution is not offered by TI.



**Figure 6. Output Waveforms During Testing of Undershoot Protection of Different Crossbar-Switch Solutions**

## Conclusion

Systems migrating to lower voltages and improved speeds require bus switches that can prevent unwanted undershoots. Good design techniques can solve problems associated with transmission lines, but systems with an intentionally reflected wave have undershoots.

The TI active-clamp solution provides excellent undershoot protection, while consuming less power, a desirable feature in today's power-hungry applications. Combined with low power consumption and overvoltage tolerance, the CBTK device is the ultimate solution for undershoot events. TI, as a leading supplier of bus switches, offers innovative functions from multiplexers to simple FET switches in a variety of bit widths. The active-clamp feature, implemented across the majority of functions in 5-V and 3.3-V devices, provides greater flexibility in designing systems.

## Glossary

$\beta$ (beta)	( $I_c/I_b$ ) Gain factor of a bipolar junction transistor
CBT	Crossbar technology
CBTLV	Low-voltage crossbar technology
CBTK	Crossbar technology with active-clamp undershoot protection
CBTS	Crossbar technology with Schottky-diode undershoot protection
$I_{CC}$	Supply current
$I_{off}$	Input/output power-off leakage current
NMOS	N-channel metal-oxide semiconductor
PC	Personal computer
$V_{be}$	Difference between base voltage and emitter voltage
$V_G$	Gate voltage
$V_S$	Source voltage
$V_{GS}$	Difference between gate voltage and source voltage
$V_{GD}$	Difference between gate voltage and drain voltage
$V_T$	Threshold voltage



# ***Designing With the SN74AHC123A and SN74AHCT123A***

SCLA014  
October 1999



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## Abstract

This application report is designed to answer any questions that the user may have on the operation of the SN74AHC123A. It also covers the most frequently asked questions and includes detailed instructions on how to calculate the external components required to make the device function correctly. Several circuits using this device also are included to show the versatility of operations that can be performed using this part.

## Introduction

The SN74AHC123A and SN74AHCT123A are dual, retriggerable, monostable multivibrators (see Appendix A) that have similar functions. The SN74AHCT123A has TTL inputs and CMOS outputs. The SN74AHC123A has CMOS inputs and outputs. These devices require external resistors and capacitors for proper operation, and the resulting RC time constant determines the output pulse duration. These devices are capable of very-long-duration output pulses by retriggering the inputs at appropriate times. An input clear can be used to decrease the output pulse duration. This application report discusses the following points:

- Rules for operation, which include the output pulse duration, its calculation, and retriggering data
- Setup of the device in relation to its external components and the variation from unit to unit
- Applications

## Features

Features of these devices are:

- Retriggerable
- Edge triggered from active-high or active-low logic inputs
- Inputs are TTL-voltage compatible for the SN74AHCT123A.
- $V_{CC}$  range of the SN74AHC123A is 2 V to 5.5 V.
- $V_{CC}$  range of the SN74AHCT123A is 4.5 V to 5.5 V.
- Clear ( $\overline{CLR}$ ) input overrides the other inputs ( $\overline{A}$  and B).
- When inputs  $\overline{A}$  and B have pulses applied to them, the signal that occurs first determines the pulse that triggers the output.
- Three inputs ( $\overline{A}$ , B, and  $\overline{CLR}$ ) have Schmitt triggers with sufficient hysteresis to handle slow input transition rates with jitter-free triggering at the output.

Figure 1 illustrates the logic diagram for both devices. Each multivibrator has two inputs, one that is active low and the other that is active high, allowing leading- and trailing-edge triggering. The output pulse duration can be increased by retriggering the input signal in use. The retrigger pulses at the input must occur after a certain period to be recognized and acted upon by the device. If the input retrigger pulse follows the initial input pulse after  $0.30 \times$  the initial output pulse duration, the output is retriggered.  $\overline{CLR}$  terminates the output pulse at any time.

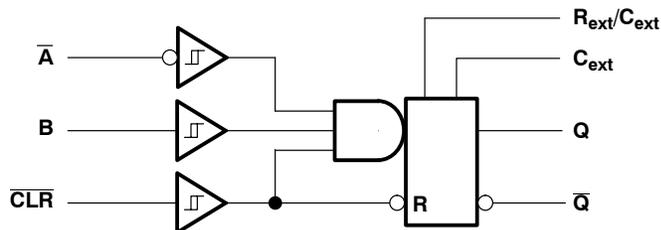


Figure 1. SN74AHC123A and SN74AHCT123A Logic Diagram for Each Multivibrator

**Table 1. Function Table for the SN74AHC123A and SN74AHCT123A**

INPUTS			OUTPUTS	
CLR	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L <sup>†</sup>	H <sup>†</sup>
X	X	L	L <sup>†</sup>	H <sup>†</sup>
H	L	↑		
H	↓	H		
↑	L	H		

<sup>†</sup> These outputs are based on the assumption that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the setup.

## Rules for Operation

Proper use depends on observing these rules of operation:

- Minimum value of external resistance ( $R_T$ ) is 250  $\Omega$ .
- External capacitance ( $C_T$ ) can have any value.
- Input voltage range is from 0 V to 5.5 V.
- SN74AHC123A  $V_{CC}$  must be 2 V to 5.5 V, and SN74AHCT123A  $V_{CC}$  must be 4.5 V to 5.5 V.
- SN74AHC123A and SN74AHCT123A  $T_A$  can be between  $-40^\circ\text{C}$  and  $85^\circ\text{C}$ .
- A switching diode on one side of the capacitor is not needed for the timing scheme.
- Required connections of  $R_T$  and  $C_T$  for the proper operation of the devices, are shown in Figure 2.  $C_T$  can be grounded at the  $C_{ext}$  terminal.

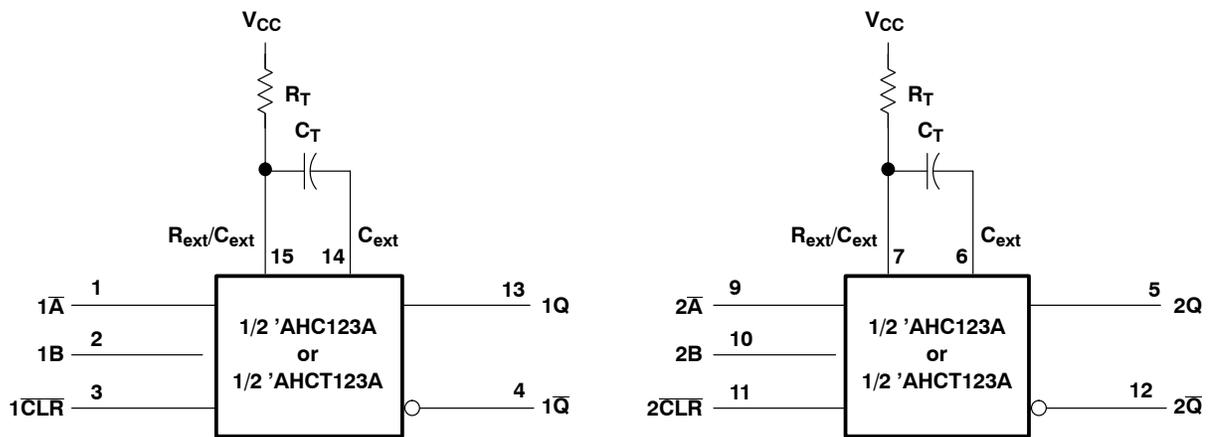


Figure 2. Timing Component Connections

### Output Pulse Duration

The output pulse duration ( $t_w$ ) for both devices is determined primarily by the values of  $C_T$  and  $R_T$ . The timing components are connected as shown in Figure 2.

The definition of the output pulse duration is shown in equation 1.

$$t_w = K \times R_T \times C_T \quad (1)$$

Where:

$t_w$  = pulse duration in ns

$K$  = multiplier factor

$R_T$  = external timing resistance in  $k\Omega$

$C_T$  = external capacitance in pF

If:

$C_T$  is  $\geq 1000$  pF,  $K = 1.0$

$C_T$  is  $< 1000$  pF,  $K$  can be determined from Figure 3

The minimum output pulse duration, using the minimum value of external resistance (250  $\Omega$ ) and a minimum value of external capacitance (open air), is approximately 290 ns.

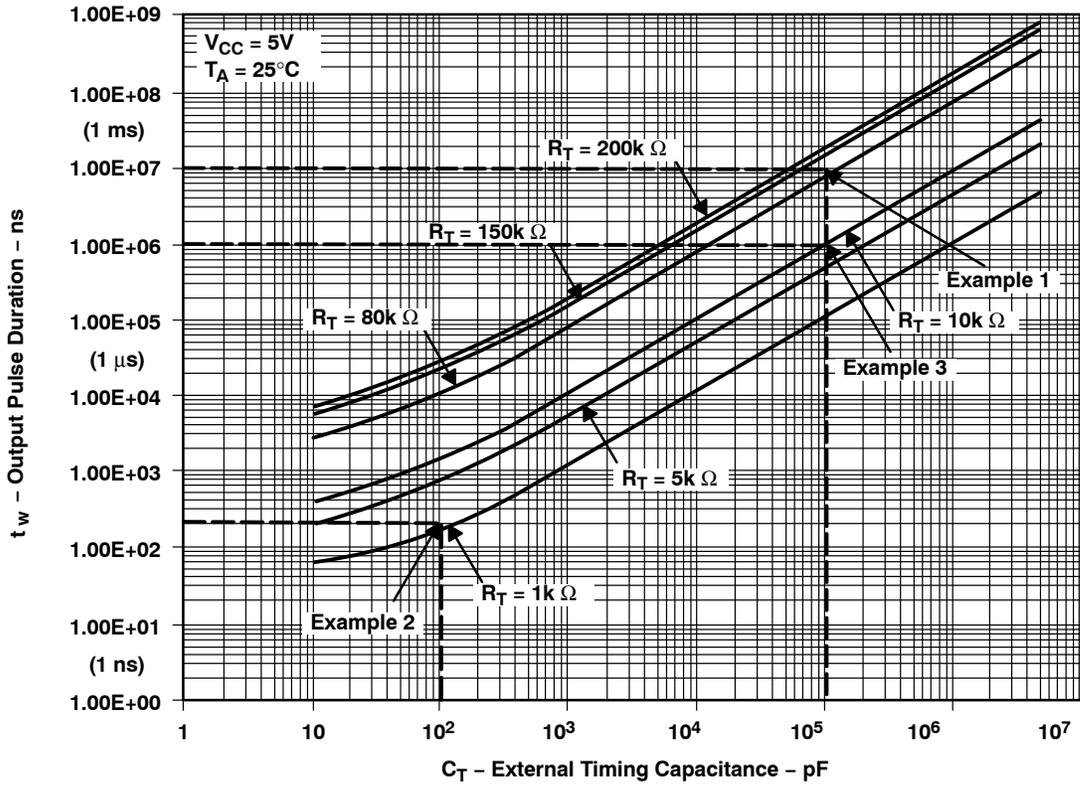


Figure 3. Output Pulse Duration vs External Timing Capacitance

**Calculations**

Equation 1 and Figure 3 can be used to determine values for output pulse duration and external resistance and capacitance values for the SN74AHC123A and SN74AHCT123A.

Equation 1 and Figures 3 and 4 can be used to solve the following problems.

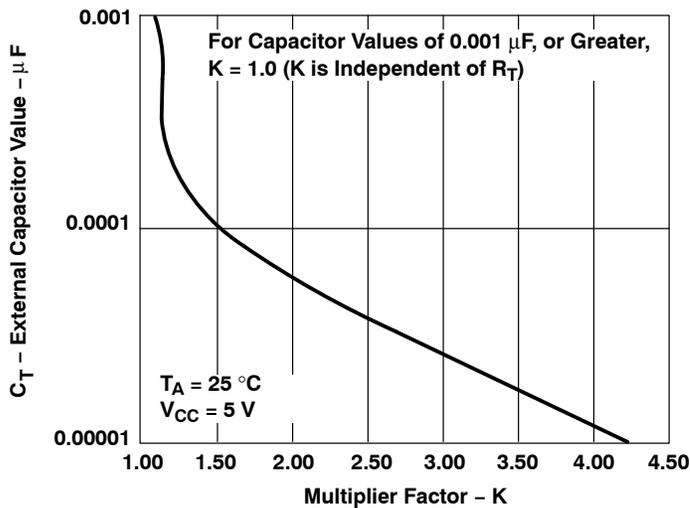


Figure 4. External Capacitance vs Multiplier Factor

- Pulse duration for a given external resistance and capacitance

For example, if an 80-k $\Omega$  resistor and a 100-nF capacitor are used, the pulse duration is obtained by following the  $R_T = 80\text{-k}\Omega$  curve to the line indicating that  $C_T = 100\text{ nF}$ . The y (vertical) coordinate of this point gives the value of the pulse duration, which is approximately  $8 \times 10^6\text{ ns}$  (8 ms).

The pulse duration ( $t_w$ ) for an external resistance of 80 k $\Omega$  and a capacitor of 100 nF is:

$$t_w = 1.0 \times 80\text{ k}\Omega \times 1 \times 10^5\text{ pF} = 8 \times 10^6\text{ ns} = 8\text{ ms} \quad (2)$$

$(K = 1.0\text{ because } C_T\text{ is greater than } 1000\text{ pF})$

This value was obtained graphically in Figure 3.

- Required external resistance for a given pulse duration and external capacitance

If a pulse duration of 200 ns is desired and a timing capacitance of 100 pF is used, the resistance needed is found where the horizontal line of 200 ns on the  $t_w$  axis intersects 100 pF on the  $C_T$  axis. This point may be along one of the curves and, in this case, the point is slightly above the  $R_T = 1\text{-k}\Omega$  curve. So the required resistance is approximately 1.3 k $\Omega$ .

The required external resistance ( $R_T$ ) that produces a pulse duration of 200 ns with a 100-pF external capacitor is:

$$R_T = \frac{t_w}{K \times C_T} = \frac{200\text{ ns}}{1.5 \times 100\text{ pF}} = 1.3\text{ k}\Omega \quad (3)$$

Because  $C_T < 1000\text{ pF}$ , use Figure 4 to find the value of K. Follow the  $t_w = 100\text{-pF}$  horizontal line from the vertical axis to the curve, then drop a vertical line to the  $C_T$  axis. The intersection on the  $C_T$  axis gives the K value; in this case,  $K = 1.5$ .

This value of  $R_T$  is approximately equal to the value of  $R_T$  as given in Figure 3.

- Required external capacitance for a certain pulse duration and external resistance

For example, if  $C_T = 10\text{ k}\Omega$  and a pulse duration of  $1 \times 10^6\text{ ns}$  is desired, the timing capacitance required can be obtained by finding the point where  $t_w = 1 \times 10^6\text{ ns}$  (from the vertical axis) intersects the 10-k $\Omega$  curve. This point is then dropped vertically, to cross the horizontal axis at  $C_T = 1 \times 10^5\text{ pF}$  (100 nF).

The external capacitance ( $C_T$ ) that produces an output pulse duration of  $1 \times 10^6\text{ ns}$ , with a timing resistance of 10 k $\Omega$ , is:

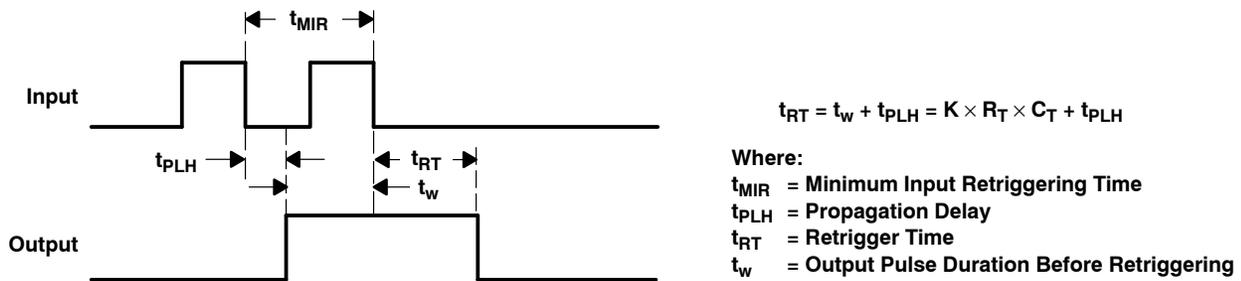
$$C_T = \frac{t_w}{K \times R_T} = \frac{1 \times 10^6\text{ ns}}{1.0 \times 10\text{ k}\Omega} = 1 \times 10^5\text{ pF} = 100\text{ nF} \quad (4)$$

The value of capacitance is unknown; therefore, the explanation following equation 1 cannot be used directly to find a value for K. Figure 4 must be studied to determine a value for K. Using Figure 3, the maximum value for a 1000-pF capacitor and 200 k $\Omega$  resistor is about  $2 \times 10^5\text{ ns}$ , which is much lower than the desired output pulse duration of  $1 \times 10^6\text{ ns}$  for this application. It can be concluded that the external capacitance is larger than 1000 pF and  $K = 1.0$ .

The value of  $C_T$  here is the same as that in Figure 3.

## Retriggering Data

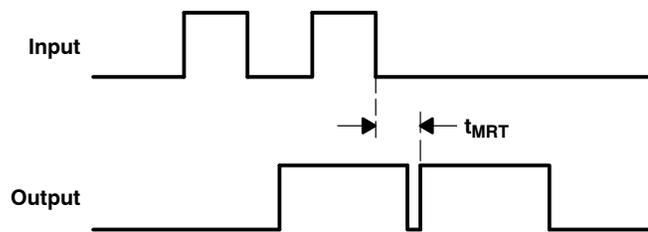
The retrigger pulse duration is calculated as shown in Figure 5.



**Figure 5. Retrigger Pulse Duration**

$t_{MIR}$  is the minimum time required after the initial signal before retriggering the input. After  $t_{MIR}$ , the device retriggers the output. Experimentally, it also can be shown that, to retrigger the output pulse, the two adjacent input signals should be  $t_{MIR}$  apart, where  $t_{MIR} = 0.30 \times t_w$ .

The minimum value from the end of the input pulse to the beginning of the retriggered output should be approximately 15 ns to ensure a retriggered output. This is illustrated in Figure 6.



$t_{MRT}$  = Minimum Time Between the End of the Second Input Pulse and the Beginning of the Retriggered Output  
 $t_{MRT} = 15 \text{ ns}$

**Figure 6. Input/Output Requirements**

### Variation in Output Pulse Duration Due to Temperature and $V_{CC}$ Levels

Figure 7 shows the percentage variation in the output pulse duration due to temperature and  $V_{CC}$  of the devices. All points on the graph are plotted relative to  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 5\text{ V}$  (which is assumed to be 0% variation). For example, according to Figure 7, at a temperature of  $40^\circ\text{C}$  and a  $V_{CC}$  level of 4 V, the value of the output pulse duration differs by 2% from the reading at  $V_{CC} = 5\text{ V}$  and  $T_A = 25^\circ\text{C}$ .

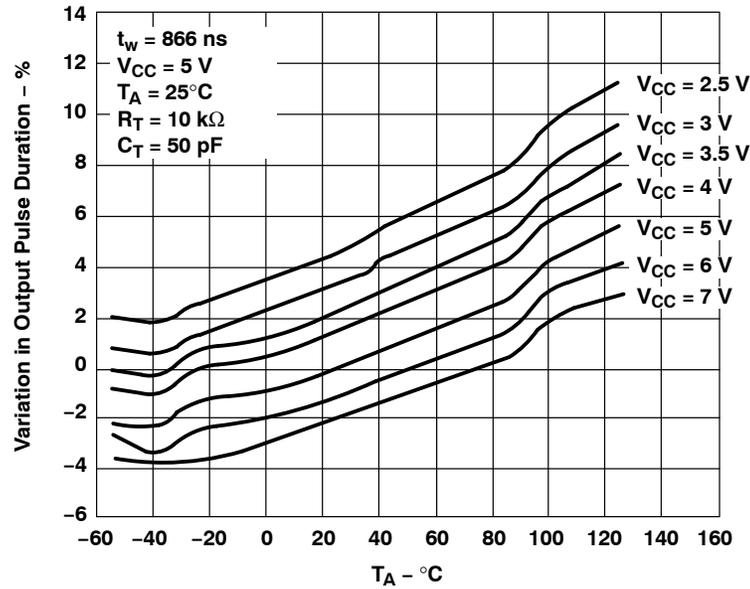


Figure 7. Variations in Output Pulse Duration for Various Temperatures and  $V_{CC}$  Levels

## Special Considerations

### Setup Guidelines<sup>1</sup>

Because the SN74AHC123A and SN74AHCT123A monostable multivibrators are half analog and half digital and are inherently more sensitive to noise on the analog portion (timing leads) than standard digital circuits, they should not be located near noise-producing sources or transient-carrying conductors. Liberal power-supply bypassing is recommended for greater reliability and repeatability. Also, a monostable multivibrators should not be used as a solution for asynchronous systems; synchronous design techniques always provide better performance. For time delays over 1.5 seconds or timing capacitors over 100  $\mu\text{F}$ , it usually is better to use a free-running astable multivibrator and two inexpensive decade counters (such as a 7490A) to generate the equivalent of a long-delay one-shot multivibrator. Astable oscillators made with monostable building blocks have stabilities approaching 5 parts in 100, and should not be used if system timing is critical. Crystal oscillators provide better stability.

In all one-shot multivibrator applications, follow these guidelines:

- Use good high-frequency 0.1- $\mu\text{F}$  (ceramic disk) capacitors, located 1 to 2 inches from the monostable package, to bypass  $V_{CC}$  to ground.
- Keep timing components ( $R_T$ ,  $C_T$ ) close to the package and away from high-transient-voltage or current-carrying conductors.
- Keep the Q output trace away from the  $\overline{\text{CLR}}$  lead; when the one-shot multivibrator times out, the negative-going edge may cause the  $\overline{\text{CLR}}$  lead to be pulled down, restarting the cycle. If this happens, constantly high ( $Q = H$ ,  $\overline{Q} = L$ ) outputs with 50-ns low spikes occur at the repetition rate determined by  $R_T$  and  $C_T$ . If sufficient trace isolation cannot be obtained, a 50-pF capacitor, bypassing the  $\overline{\text{CLR}}$  lead to ground, usually eliminates the problem.
- Beware of using the diode or transistor protective arrangement when retriggerable operation is required; the second output pulse may be shorter due to excess charge left on the capacitor. This may result in early timeout and apparent failure of retriggerable operation. Use a capacitor that is able to withstand 1 V in reverse and meet the leakage-current requirements of the particular one-shot multivibrator.
- Remember that the timing equation associated with each device has a prediction accuracy.

### Distribution of Units

Figure 8 shows the variation in the output pulse duration for a random sample of both devices. The average pulse width of the output is 856 ns, with a standard deviation of 3.5 ns. The median has the same value as the mean. There also is a high frequency of finding units with an average output pulse duration. A unit with the median-value pulse duration was tested to obtain the plots in Figures 3, 4, 7, and 8.

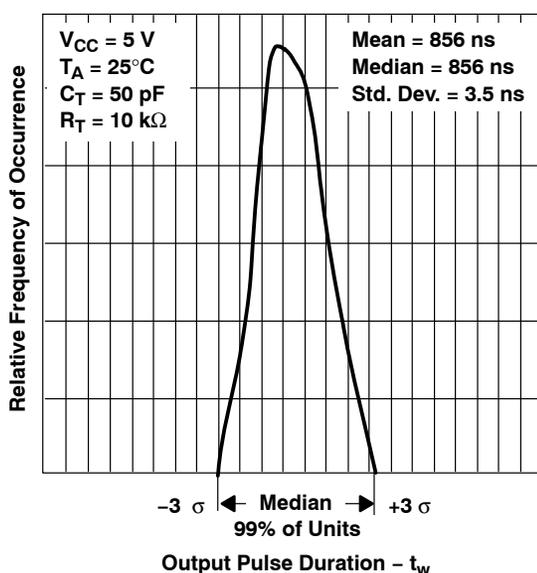
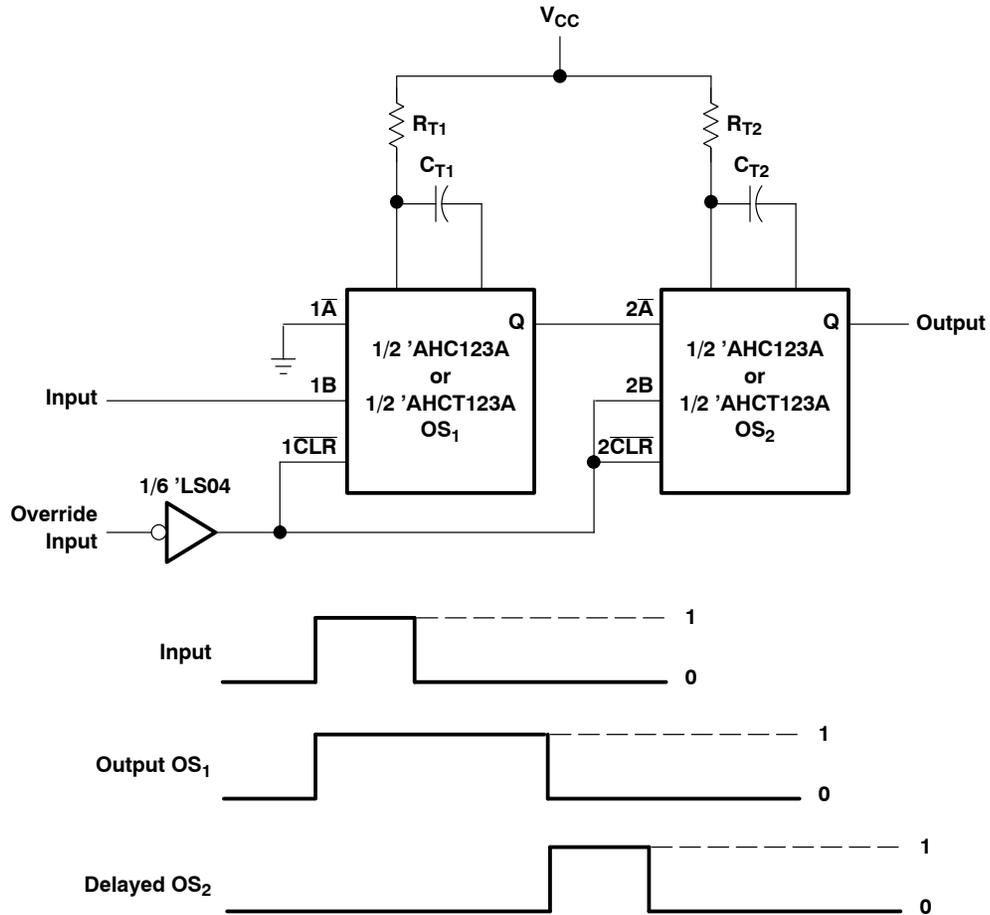


Figure 8. Distribution of Units vs Output Pulse Duration

## Applications

### Delayed-Pulse Generator With Override<sup>1</sup>

In Figure 9, the value of the delay time depends on the values of  $R_{T1}$  and  $C_{T1}$  in the first one-shot multivibrator ( $OS_1$ ). The second one-shot multivibrator ( $OS_2$ ) determines the output pulse duration that is defined by the values of  $R_{T2}$  and  $C_{T2}$ . A positive rising pulse into the override circuit can terminate the output pulse at any time.



**Figure 9. Delayed-Pulse Generator With Override**

## Missing-Pulse Generator<sup>1</sup>

The external resistance ( $R_{T1}$ ) and the external capacitance ( $C_{T1}$ ) determine the pulse duration of  $OS_1$ . This pulse duration is set to be greater than one-half of the incoming frequency. A transition from low to high logic on the incoming pulse sets the output of  $OS_1$  to a high logic level. The output of  $OS_1$  remains high as long as the input pulse consistently switches from high to low to high logic at regular intervals. This implies that the one-shot multivibrator is being retriggered. If there is a missing pulse in the pulse train of the input, the output of  $OS_1$  falls to a low logic level and the output of  $OS_2$  rises to a high level (see Figure 10).

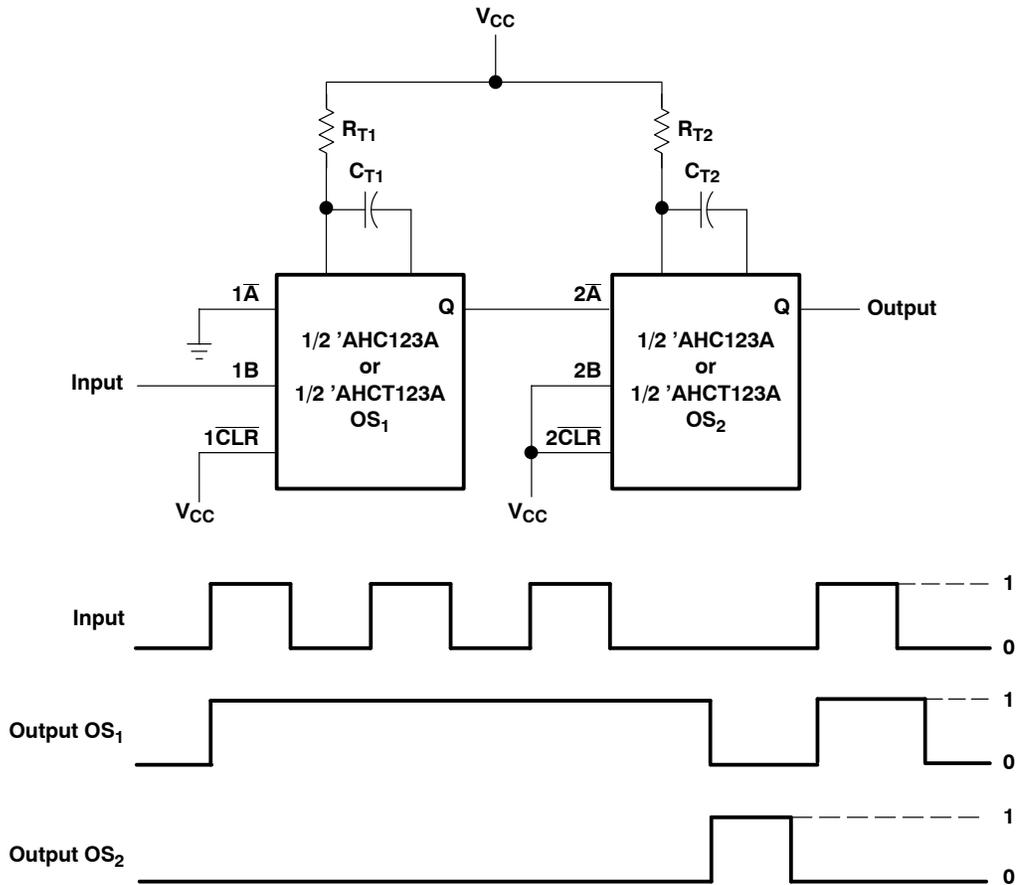


Figure 10. Missing-Pulse Detector

### Low-Power Pulse Generator<sup>1</sup>

In Figure 11, the first one-shot multivibrator (OS<sub>1</sub>) is responsible for the output frequency of the generator. The external resistance (R<sub>T1</sub>) and the external capacitance (C<sub>T1</sub>) determine the frequency. The OS<sub>2</sub> configuration gives rise to the output pulse duration, which is determined by R<sub>T2</sub> and C<sub>T2</sub>.

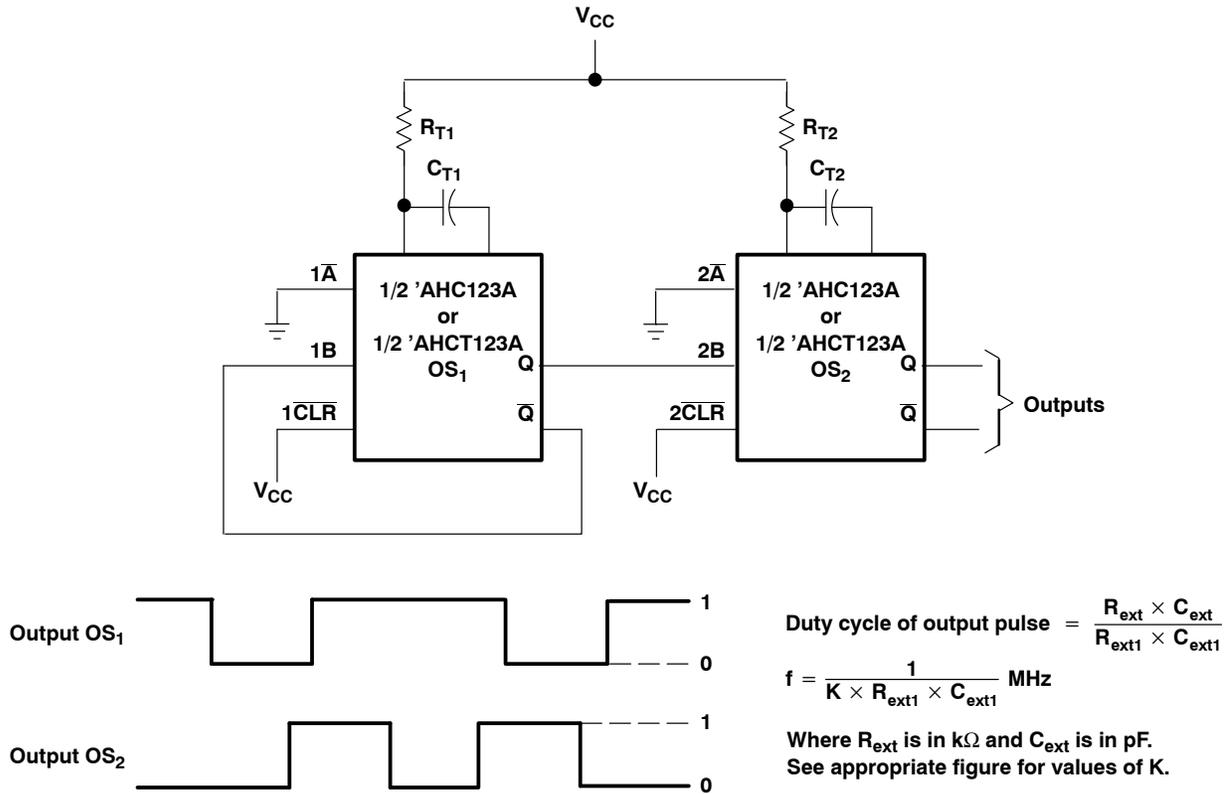


Figure 11. Low-Power Pulse Generator

### Negative- or Positive-Edge-Triggered One-Shot Multivibrator<sup>1</sup>

The circuit in Figure 12 is arranged such that a negative-going input pulse causes a low-to-high-to-low pulse on OS<sub>1</sub>. A positive-going input pulse causes a low-to-high-to-low pulse on OS<sub>2</sub>. The outputs of OS<sub>1</sub> and OS<sub>2</sub> are connected to an OR gate that outputs a pulse when OS<sub>1</sub> or OS<sub>2</sub> switches. The circuit in Figure 12 also can be used as a frequency doubler.

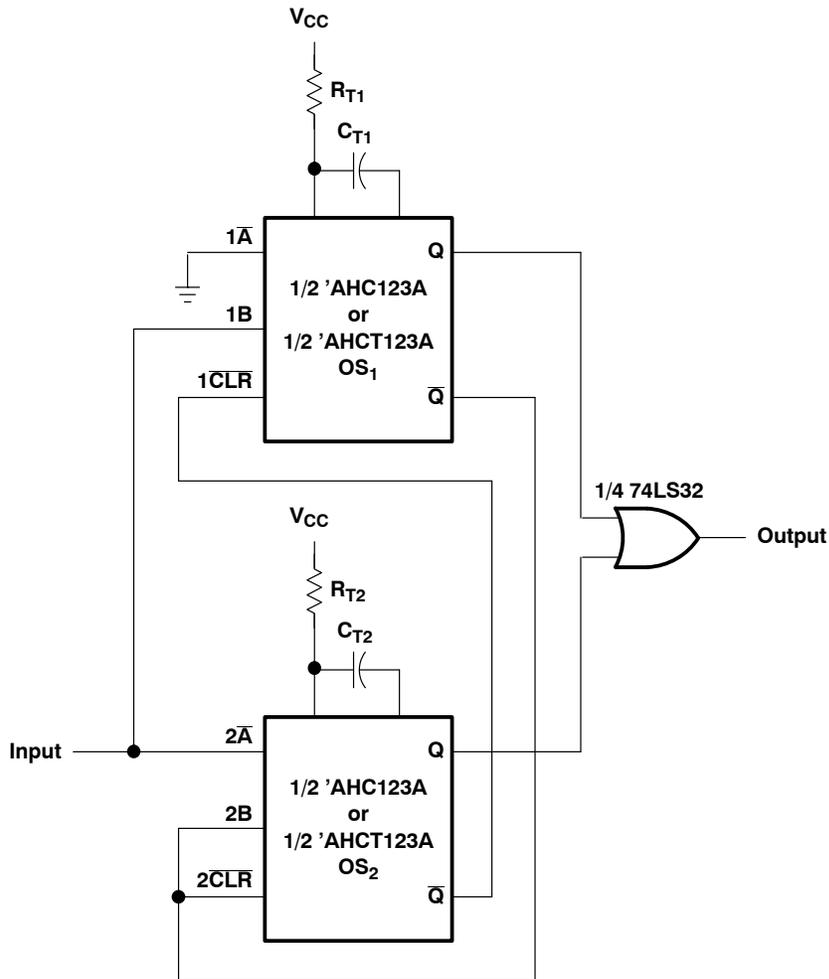


Figure 12. Negative- or Positive-Edge-Triggered One-Shot Multivibrator

### Pulse-Duration Detector<sup>1</sup>

Figure 13 shows a circuit using the AHC/AHCT123A chip, which generates an output pulse ( $t_3$ ) if the trigger pulse duration ( $t_2$ ) is wider than the programmed output pulse duration ( $t_w = K \times R_T \times C_T$ ). It functions as follows:

The A input of the AHC/AHCT123A is approximately  $V_{CC}$  and the transistor  $Q_1$  usually is off. The Q output of the AHC/AHCT123A normally is low and the output of  $Q_2$  is off (the output normally is low because no pullup exists). A trigger of duration  $t_1$  applied at the input is differentiated by the  $R_1C_1$  combination and  $Q_1$  is turned on. The result of that momentary condition at the base of  $Q_1$  is a negative-going pulse at point 1 (the A input of the AHC/AHCT123A), which triggers AHC/AHCT123A. The AHC/AHCT123A remains on for the time  $t_w = K \times R_T \times C_T$ , which is waveform  $t_2$ .  $Q_2$  on the output of the device is turned on for a time equal to  $t_2$  and, after this time, turns off. If the input pulse is still high after this, it appears at the output. The circuit output pulse duration,  $t_3$ , equals the input pulse duration, minus the pulse duration of the AHC/AHCT123A.

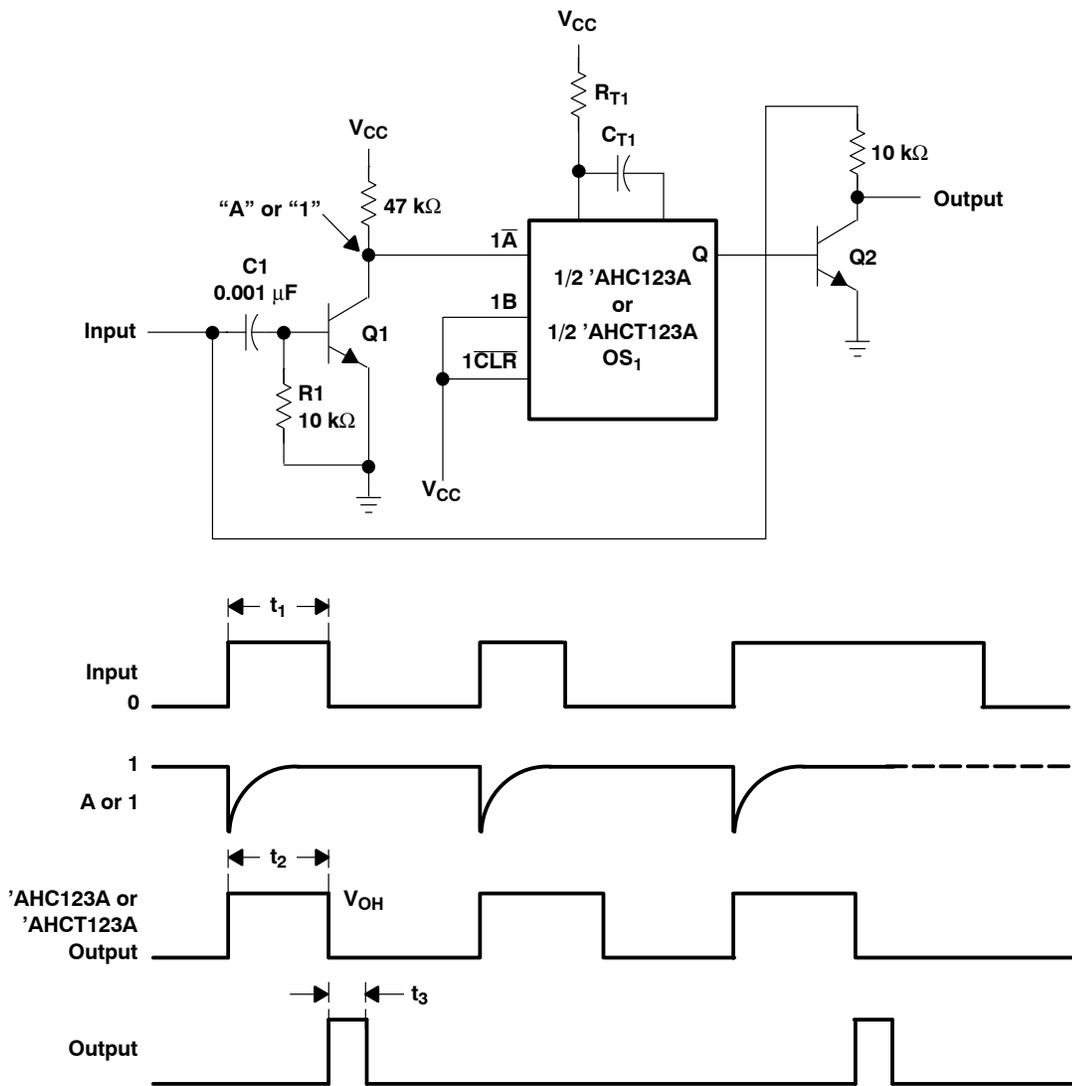


Figure 13. Pulse-Duration Detector

## Frequency Discriminator<sup>1</sup>

$R_{T1}$  and  $C_{T1}$  in Figure 14 form a resistor-capacitor integration network that produces an output voltage proportional to the frequency. This plot is linear and is valid over a limited range.

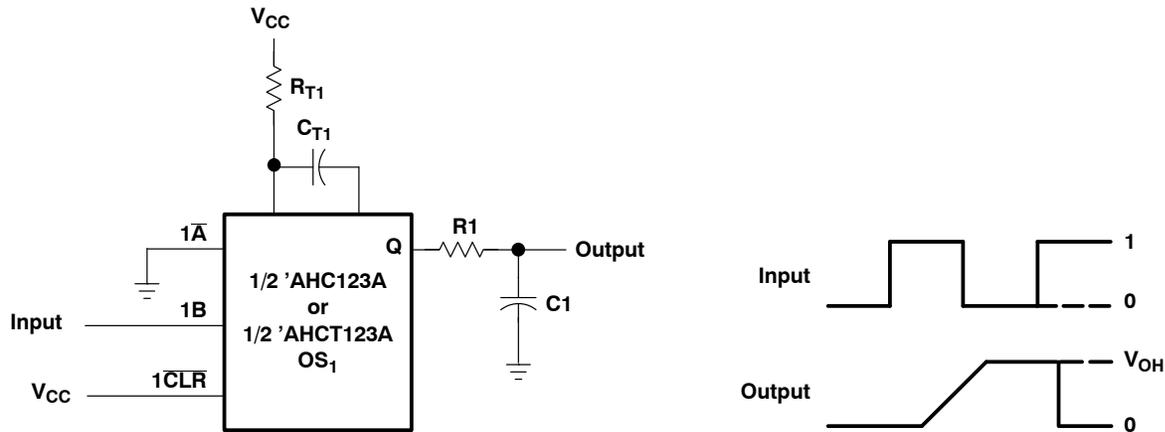


Figure 14. Frequency-Discriminator Circuit

## Conclusion

The SN74AHC123A and SN74AHCT123A function similarly. Both devices require external resistors and capacitors for proper operation, and these timing units can be used to determine the output pulse duration. These devices can be retriggered to create very long output pulses. If the input signal is triggered and the time length to the previous input signal is less than  $0.30 \times$  initial output pulse duration in seconds, the output duration remains unchanged. A clear input can be used at any time to terminate the output pulse. The output pulse duration also varies according to the temperature of operation and the  $V_{CC}$  of the device.

There are several applications in which these dual retriggerable monostable multivibrators can be used. In all cases, it is essential that the setup guidelines be followed to promote the safety and reliability of the devices.

## Acknowledgments

The authors of this application report are Sujatha Garimella, Dennis Wade, Clif Dugan, and Gerry Balmer. The authors wish to thank Arnie Ruiz, Joe Costa, Jim Stein, Dave Long, Imran Sohrab, Bryan Lammers, Mark Frimann, Keith Henderson, Terence Ndofor, and Hari Garimella for their assistance with this application report.

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1. Clif Dugan, *Designing with the SN54/74LS123*, Texas Instruments Incorporated, Dallas, TX, 1990.
2. Walter H. Buchsbaum, Sc.D., *Encyclopedia of Integrated Circuits: A Practical Handbook of Essential Reference Data*, Prentice-Hall Incorporated, Englewood Cliffs, NJ, 1981.

Information from the following web sites also was used in this application report:

<http://www.sh-gpl.ti.com/mirrors/>  
<http://www-s.ti.com/sc/psheets/schs142/schs142.pdf>  
<http://www-s.ti.com/sc/psheets/sdls043/sdls043.pdf>  
<http://www-s.ti.com/sc/psheets/scls420a/scls420a.pdf>  
<http://www-s.ti.com/sc/psheets/scls352b/scls352b.pdf>

## Appendix A

### One-Shot Monostable Multivibrator<sup>†</sup>

Multivibrators are a form of flip-flop circuit in which an RC time constant is used to determine the rate of change of state (toggling). In the monostable or one-shot multivibrator (MV), an external trigger signal starts the change of state of this MV, and the external RC time constant determines the time required from the beginning to the end of this one-shot oscillation.

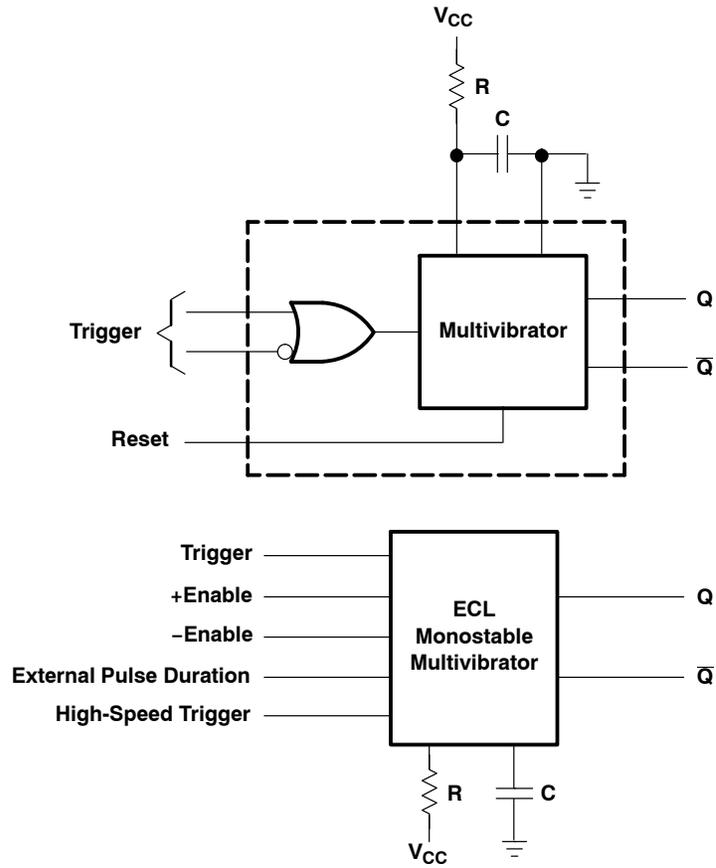
A basic monostable MV is shown in Figure A–1. The key elements are the two trigger inputs, the reset input, and the values of the external RC time constant. The OR circuit that triggers the MV has a small circle on one of its inputs, indicating that it can accept either a positive- or a negative-edge trigger. The edge-triggering ability is produced because this particular OR circuit is combined with a Schmitt-trigger effect. In some ICs, this type of circuit has a hysteresis characteristic and is referred to as a transmission gate.

The operation of the monostable MV requires that it first be reset so that the Q output is 0 and the  $\bar{Q}$  output is 1. When either a positive or a negative trigger signal is entered, Q immediately changes to 1 and  $\bar{Q}$  to 0. After a period of time, determined by the RC time constant, the MV returns to its original state, having generated one pulse. When the reset signal occurs, the MV returns to the original state where Q is at 0. In retriggerable monostable MVs, any trigger signal that occurs during the period when Q is at 1 prolongs the duration of the pulse beyond the time determined by the RC time constant.

The function block of a typical emitter-coupled logic (ECL) monostable MV is illustrated in Figure A–1, which shows some of the various features that are available in monostable MV ICs. Trigger signals are applied to the trigger input, and the external +enable or –enable signals determine whether the MV accepts positive- or negative-going edges. Internal Schmitt-trigger circuits make the trigger input insensitive to rise and fall times. Although there is an external RC time constant, there also is an input for external pulse-width control. With an external resistor, a control voltage can be used to vary the pulse width. When a control current is used, the resistor is not required. In addition, this ECL IC has a special high-speed-trigger input that bypasses the internal Schmitt-trigger circuits and permits a very rapid response.

Monostable MVs that can be triggered multiple times within a given time period to increase the pulse duration according to a fixed ratio are available. Other monostable MVs include a preset feature that can be combined with retriggering to generate specific-pulse waveforms.

<sup>†</sup>Walter H. Buchsbaum, Sc.D., wrote Appendix A and provided Figure A–1 (see *Encyclopedia of Integrated Circuits: A Practical Handbook of Essential Reference Data*).



**Figure A-1. One-Shot Monostable Multivibrator and Function Block Diagram**

# ***Advanced Low-Voltage Technology***

SCEA015  
July 1999



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## Abstract

ALVT, the advanced low-voltage logic family, offers high-performance BiCMOS devices that are functional at 3.3-V and 2.5-V  $V_{CC}$  and have low propagation delay, low static-power consumption, and 64 mA current drive. Other features include 5-V tolerance; auto3-state; bus hold; partial power down, hot insertion, and live insertion; and excellent simultaneous-switching and output-skew performance.

## Introduction

Texas Instruments (TI™) ALVT (advanced low-voltage logic) family is the next-generation low-voltage technology that has been optimized for customer applications. This application report includes ALVT characterization information to aid design engineers in more accurately designing their digital logic systems. The focus is on the family's features and benefits, product characteristics, and design guidelines. The state-of-the-art features that have been available in the 5-V Advanced BiCMOS technology, are now available with the ALVT, the higher performance low-voltage technology that is fabricated using state-of-the-art 0.65-micron BiCMOS technology for bus-interface functions. This application report is intended to be used as a designer's guide for component selection and usage. The ALVT family is functional at 3.3-V and 2.5-V  $V_{CC}$  and is 5-V tolerant at 3.3-V  $V_{CC}$ . ALVT provides superior performance, with 2.5-ns propagation delay, current drive of 64 mA, and static power consumption of 0.1 mA.

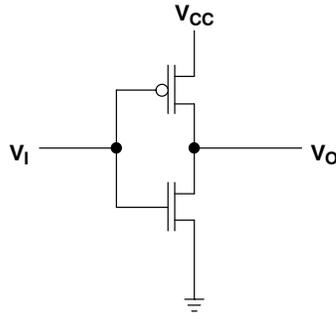
## Customer Applications for ALVT

The ALVT family was created to drive lower impedances in backplane applications. Several key issues are important in backplane applications, including topics such as live insertion; power-up 3-state; 5-V tolerance; signal integrity, including ground bounce; bus hold; and bus contention.

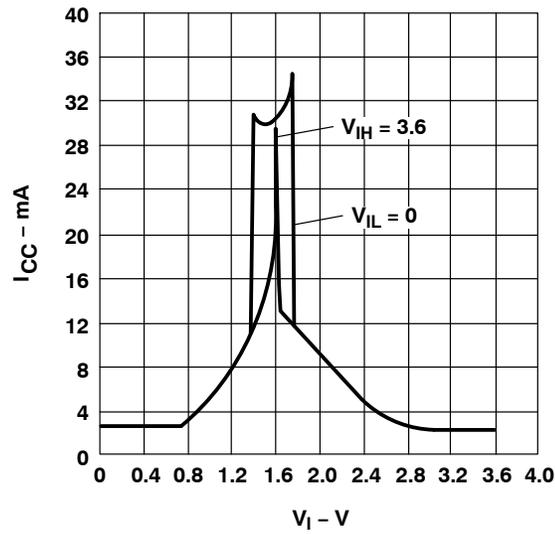
The ALVT family can operate at a  $V_{CC}$  from 2.5 V to 3.3 V. It is 30% faster than the LVT family and is one of the fastest families in 5-V and the 3.3-V ranges. The ALVT family is initially targeted for the Widebus™ (16-bit) devices and features damping-resistor versions that minimize undershoot in bus-driving applications.

## Input Characteristics

ALVT has a CMOS input structure (see Figure 1). The input is an inverter consisting of a p-channel to  $V_{CC}$  and an n-channel to GND. When a low voltage level is applied to the input, the p-channel transistor is on, and the n-channel transistor is off, resulting in current flowing from  $V_{CC}$ , pulling the  $V_{out}$  node (at the input stage) to a high state. When a high level is applied, the n-channel transistor is on, the p-channel transistor is off, and the current flows to GND, pulling the  $V_{out}$  node (at the input stage) to a low state. However, there is a state at the input transition when the n-channel and the p-channel transistors are turned on simultaneously, generating a current path between  $V_{CC}$  and GND. This could damage the transistors, depending on the length of time the signal lies in the threshold region, which is 0.8 V to 2 V ( $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ). The supply current can increase to 35 mA per input, peaking at approximately 1.5-V  $V_I$  (at 3.6-V  $V_{CC}$ ) (see Figure 2).



**Figure 1. ALVT Input Structure**



**Figure 2.  $I_{CC}$  vs  $V_{IN}$  for ALVTH16244**

ALVT devices function at 2.5-V and 3.3-V  $V_{CC}$ , and the corresponding input-high and input-low levels are shown in Table 1.

**Table 1. ALVT Functions at 2.5 V and 3.3 V**

VOLTAGE LEVELS	2.5-V $V_{CC}$	3.3-V $V_{CC}$
$V_{IH}$ (min)	1.7 V	2.0 V
$V_{IL}$ (max)	0.7 V	0.8 V

## Output Characteristics

Figure 3 shows the simplified output circuit of a typical ALVT device. The Schottky diode (D1) is used to block the reverse current in certain power-down applications. The MOS transistors at the output allow rail-to-rail switching, while the bipolar transistors provide current switching and high-drive capability. The NMOS transistor (M2) is responsible for the low level and provides edge-rate control in the high-to-low transition. The circuit for the 5-V tolerance and the auto3-state are connected as shown in Figure 3.

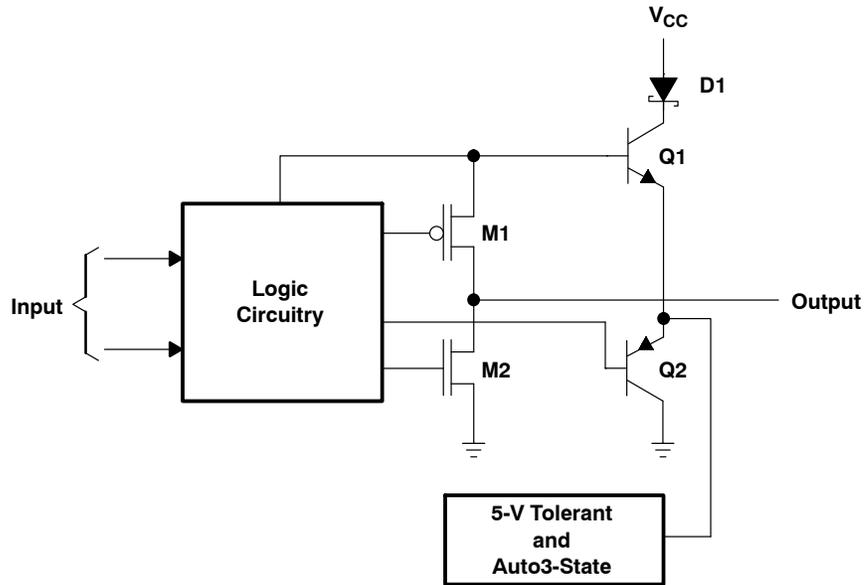


Figure 3. ALVT Output Circuit

Figure 4 illustrates values of  $I_{OH}$  and  $I_{OL}$  and the corresponding values of  $V_{OH}$  and  $V_{OL}$  for the ALVTH16244 device.

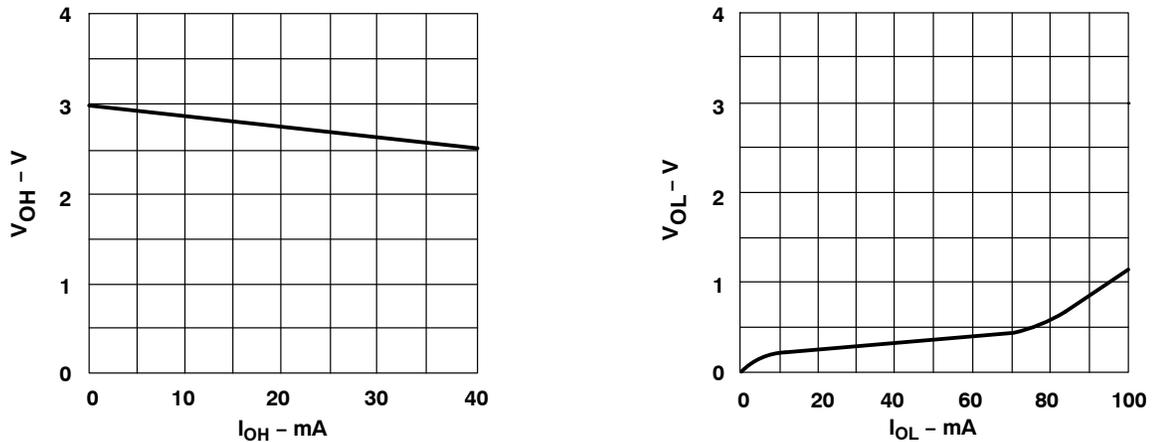


Figure 4. Output Drive for ALVTH16244

## 5-V Tolerance

Any 5-V TTL or CMOS device can drive the 5-V tolerant inputs of the ALVT device. A device without the 5-V tolerant capability at the inputs would require a dual-level  $V_{CC}$  shifter to avoid current flow between the 5-V supply and the 3-V supply. The devices in the TI portfolio that a designer can use to perform the level shifting include the ALVC164245, LVC4245A, LVCC4245, and LVCC3245.

The 5-V-tolerant outputs help establish a connection between the device and any 5-V TTL bus. A non-5-V-tolerant output would require a dual  $V_{CC}$  level shifter to drive the output.

The 5-V tolerance at the inputs is implemented by not including a diode to  $V_{CC}$  in the input circuitry, making the inputs 5-V tolerant. The output 5-V tolerance is achieved by including a blocking diode between the backgate and the source to block the parasitic diode current as shown in Figure 5. P1 and D2 clamp the gate and backgate to the output after the output rises over  $V_{CC}$ , preventing turnon of the output PMOS.

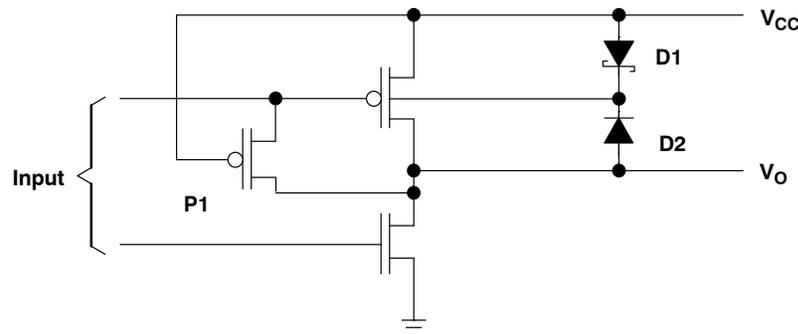


Figure 5. 5-V-Tolerant Output

## Auto3-State

The auto3-state feature in the ALVT is demonstrated in Figure 6. This feature is not the same as the power-up 3-state feature. Auto3-state provides short-circuit current limiting (approximately 40 mA) at approximately  $V_O = V_{CC} + 0.5$  V. As the outputs are swept above  $V_{CC} + 0.5$  V, the outputs are in the 3-state condition, preventing bus contention in cases where the bus is driven to a higher voltage by a competing driver. The output overvoltage protection is illustrated in Figure 6 by a simple comparator circuit that compares the output voltage to  $V_{CC}$  and limits the current by turning off the PMOS transistor when the output is approximately 0.5 V greater than  $V_{CC}$ . This helps protect the PMOS transistor in the active-high state. The output current in this case is represented by  $I_{ex}$  and is specified in the data sheet at 125  $\mu$ A, for  $V_O = 5.5$ .

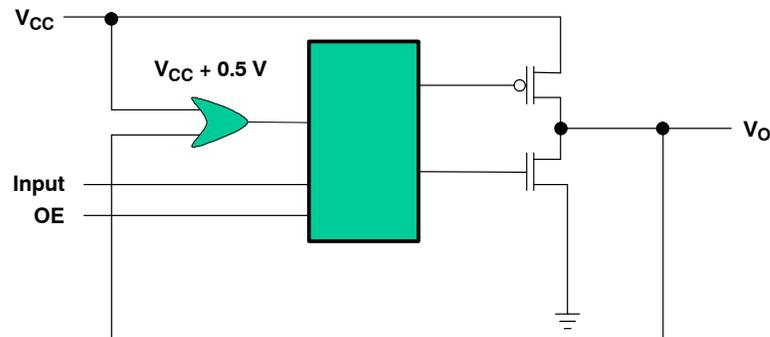
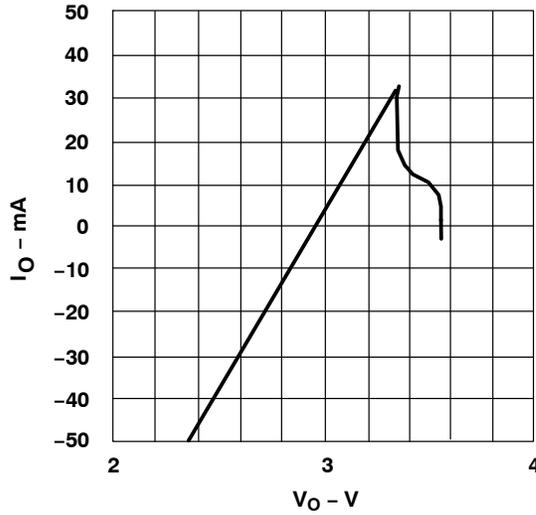


Figure 6. Auto3-State Circuitry

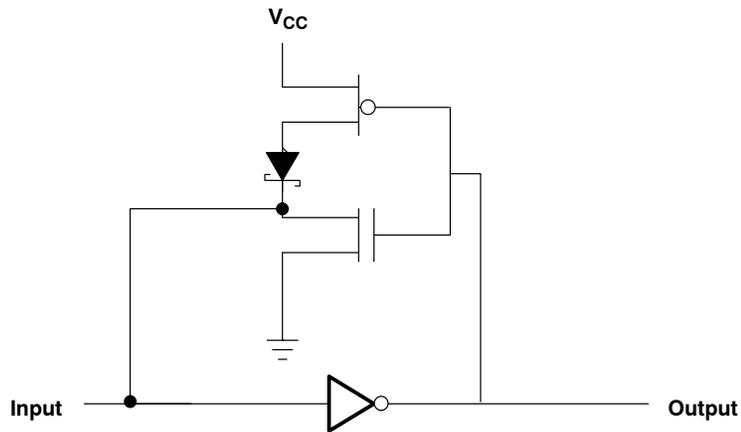
Figure 7 shows the V-I curve at the outputs for the condition where the output is pulled above  $V_{CC}$  (3.0 V) for the ALVTH16244. If  $V_O$  is greater than  $V_{CC}$ , the current sinks into the output PMOS transistor until the comparator senses the difference in the output voltage and shuts off the transistor. The maximum current sinking into the PMOS transistor is 45 mA.



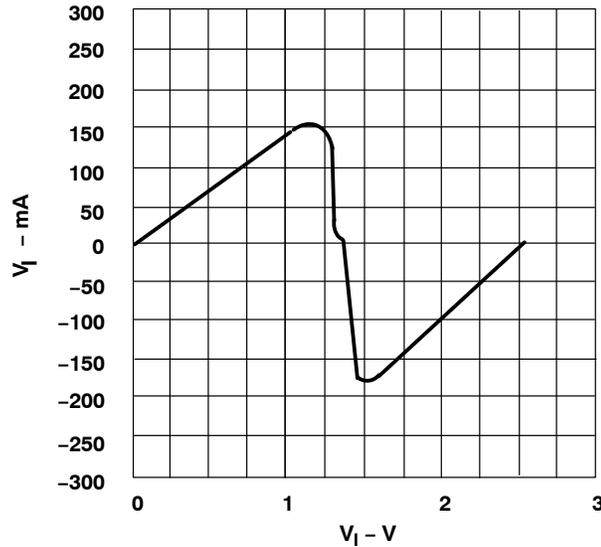
**Figure 7. Auto3-State Implementation for ALVTH16244**

**Bus Hold**

All devices in the ALVT family have bus-hold circuits. The bus-hold circuit is an internal feedback circuit that keeps the unused input pins from floating and eliminates the need for external pullup resistors. This feature is implemented in ALVT devices by using input transistors that act either as pullups or pulldowns (see Figure 8), allowing the inputs of the CMOS transistors to be left open. The circuit also shows a Schottky diode between the input and the PMOS transistor that blocks the input current if the device is connected to a 5-V signal when the device is powered off. Figure 9 shows the bus-hold characteristic for the ALVTH16244.



**Figure 8. Bus-Hold Circuitry**

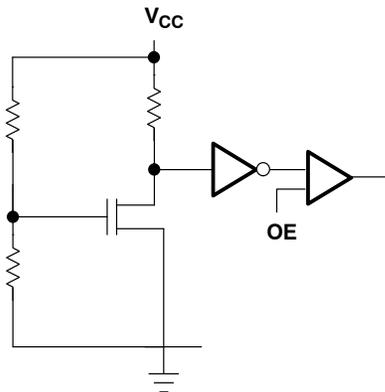


**Figure 9. Bus-Hold Current With  $V_{CC} = 3\text{ V}$  and  $V_I$  Sweep From 0 V to 3 V**

### Partial Power Down, Hot Insertion, and Live Insertion

A device that is hot-insertable prevents driver conflicts as the card is being inserted or removed from a loaded backplane. Both  $I_{off}$  and power-up 3-state (PU3S) circuitry are needed for hot insertion. The ALVT family has these features, which are used for both partial-power-down and hot-insertion applications. The power-up 3-state feature, as shown by the power-up control circuit in Figure 10, maintains the output in a 3-state condition when  $V_{CC}$  is lower than 1.2 V. The high-impedance state at the output prevents any current sinking into the device to prevent damage in hot-insertion applications. The internal circuitry consists of a transistor that turns off if  $V_{CC}$  is lower than 1.2 V. This keeps the output at 3-state while  $V_{CC}$  is lower than 1.2 V. This is important for applications where the device is connected to an operating backplane, which results in a device being powered up from 0 to  $V_{CC}$ . After  $V_{CC}$  passes 1.2 V, the transistor turns on, which, in combination with the external OE signal, activates the device.

The ALVT devices feature the  $I_{off}$  specification and include the PU3S circuitry. For a glitch-free live insertion to the data bus an additional precaution must be taken. Typically, board I/Os must be precharged. This can be implemented internally or externally to the bus-interface device. A power-sequencing scheme with the ground, precharge circuitry ( $V_{CCBias}$ ),  $V_{CC}$  and I/O must be followed to facilitate live insertion. ALVT devices do not include this feature with internal precharging circuitry. If live insertion is required, external precharging circuitry is required.



**Figure 10. Power-Up Control Circuit**

Figure 11 shows the output of the ALVTH16244 as  $V_{CC}$  is powered up or powered down between 0 and 3.6 V. In this example, the output has a 3.0-V force when it is in 3-state and remains in 3-state well outside the data-sheet specification of  $V_{CC} \leq 1.2\text{ V}$ . The power-up 3-state currents are specified as  $I_{OZPU}$  and  $I_{OZPD}$  in the data sheet.

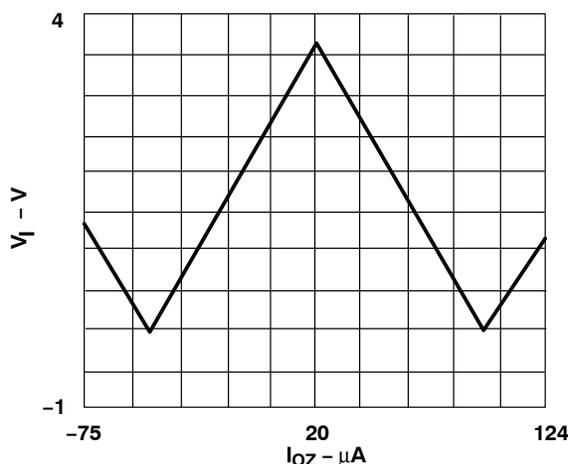


Figure 11. Power-Up/Power-Down Test With  $V_o = \text{High}$ , ALVTH16244

### Interfacing Between 3 V and 5 V

With the trend toward lower voltages, it is extremely important for inputs and outputs to be compatible with mixed-mode operations. As lower-voltage ASICs, processors, and memories come into existence, it becomes important to operate in these mixed-mode voltage applications. In today's market, there is a mix of both 5-V and 3-V systems, with subsequent migration to 2.5 V and, eventually to 1.8 V. The 3-V I/O pins must tolerate both 3 V and 5 V at the inputs and the outputs. Table 2 summarizes the mixed-mode operating capability of the ALVT family.

Table 2. ALVT Mixed-Mode Operation

FEATURES	ALVT
Drive 5-V TTL levels	Yes
Drive 5-V CMOS levels	No
5 V on inputs/control pins	Yes
5 V on outputs	Yes (when in 3-state and active high)

Inputs of ALVT devices are designed without the diode, making them 5-V tolerant. The Schottky diode at the outputs prevents the current from flowing from the output transistor. The auto3-state feature, explained previously, also protects the internal circuit of the device, making the outputs 5-V tolerant.

### Signal Integrity

A designer is concerned about the performance of the device when the outputs are switching. The most common method of assessing this behavior is by observing the impact on one unswitched signal output, when multiple outputs are switching.

### Simultaneous Switching and Ground Bounce

Simultaneous switching is a method used to measure the magnitude of noise a device produces while switching. The method of measuring simultaneous-switching noise (ground bounce) consists of holding one output low and switching all other outputs from the high state to the low state. Mutual inductance causes transient current to flow through the package and into the output pin that is being held low. This results in a rise in voltage and the output begins to ring. The peak of this ringing is called  $V_{OLP}$  (output low peak voltage) and is the most common and critical measure of ground bounce due to the relatively small noise margin between a valid output low state and beginning of the threshold region of 0.8 V.  $V_{OLV}$  (output low valley voltage) is the lowest point that the output that is being held low reaches. ALVT devices are optimized for ground-bounce performance, and can be measured with respect to GND or  $V_{CC}$ . When measuring with respect to GND,  $V_{OLP}$  is the impact of one quiet, logic-low output when all other outputs are switched from high to low.

In a similar fashion, two other measurements of simultaneous switching exist. In this scenario, a single output is held high and all other outputs are switched from the low state to the high state. Mutual inductance occurs and results in the output voltage dipping from its logic high state and ringing. The valley of this phenomenon is called output high valley voltage ( $V_{OHV}$ ) and the peak is called output high peak voltage ( $V_{OHP}$ ).

Simultaneous switching performance is extremely important. If the value of  $V_{OLP}$  goes above 0.8 V, the threshold region is entered and the device could switch from the low state to the high state. Conversely, if the value of  $V_{OHV}$  drops below 2 V, the device could switch from the high state to the low state. For this reason, simultaneous-switching values always are monitored closely when designing, testing, and implementing devices.

Figures 12 and 13 show the  $V_{OHV}$  and  $V_{OLP}$  levels for the ALVTH16244 for high-to-low and low-to-high transitions.

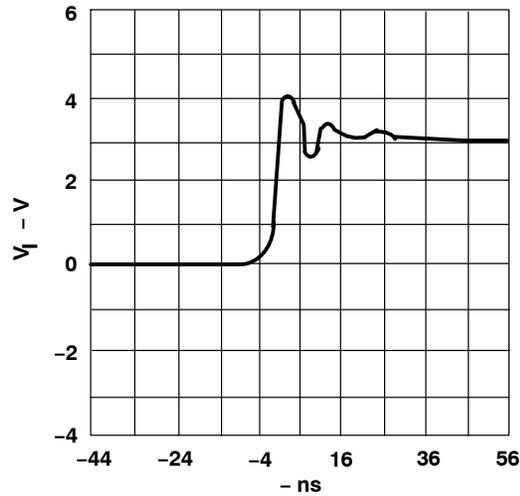


Figure 12.  $V_{OHV}$

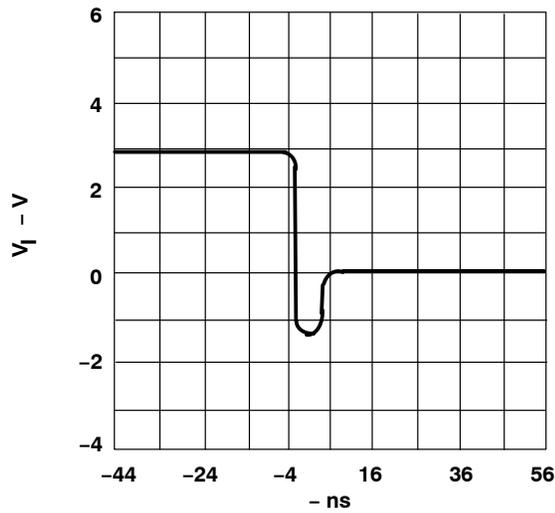


Figure 13.  $V_{OLP}$

The technique used to reduce the impact of simultaneous switching on a device is to increase the number of power and GND pins. This reduces the mutual inductances between the signals.

### Propagation Delay, Load, and Number of Outputs Switching

The ALVT family has been characterized for faster speeds and has a typical propagation-delay time of 2.5 ns. Propagation delay is an important parameter because it is a direct indication of the speed of the device and can be a primary parameter in determining whether or not a given logic family is suitable for a particular application.

The standard load for testing the ALVT family is 50 pF and 500 ohms. In most applications in which the ALVT families can be used, the load is 50 pF, but they are also commonly used in systems that require up to 100-pF loads. Figure 14 shows propagation-delay time versus load capacitance for the TI ALVTH16244. As the load increases, an increase in propagation delay occurs.

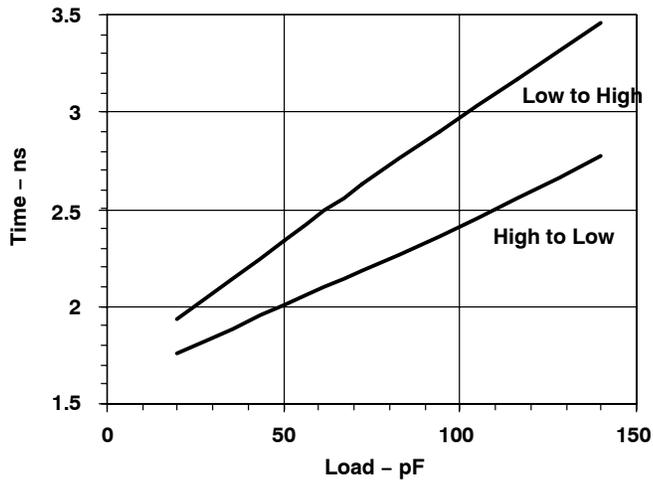


Figure 14.  $t_{pd}$  vs  $C_L$

Figure 15 shows the results of single outputs switching, 4 outputs switching, 8 outputs switching, and 16 outputs switching at one specific load. Additionally, a distinction is made between whether the output is switching from a low-to-high state or from a high-to-low state.

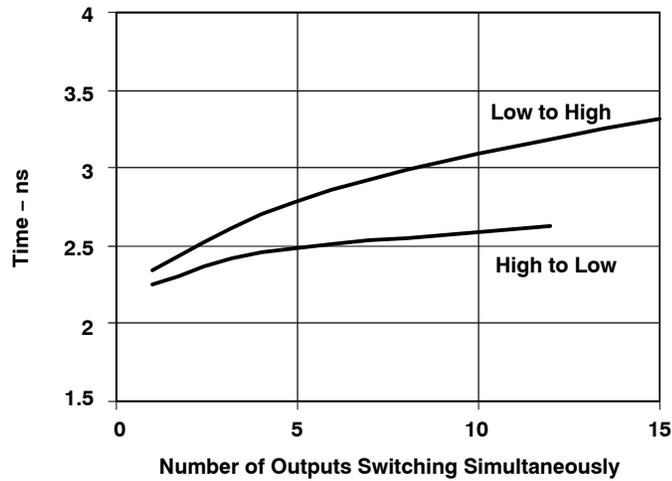


Figure 15.  $t_{pd}$  vs Simultaneous Switching,  $V_{CC} = 3.3$  V and 50 pF

## Supply Current Versus Frequency

The supply current ( $I_{CC}$ ) is critical because it is an indication of the amount of power consumed by the device. A small value for  $I_{CC}$  is desirable because  $I_{CC}$  is a factor in the dynamic power dissipated by the device. Reducing the amount of power consumed yields many benefits, including less heat generated, which eventually increases the reliability of a system. This could also enhance the performance because lower stress gradients are present on the device and the integrity of the signal is improved due to the reduction of ground bounce and signal noise.

Figures 16 and 17 illustrate the relationship of  $I_{CC}$  to frequency for the TI ALVTH16244. The data were taken at 25°C for single-output and all-outputs switching.

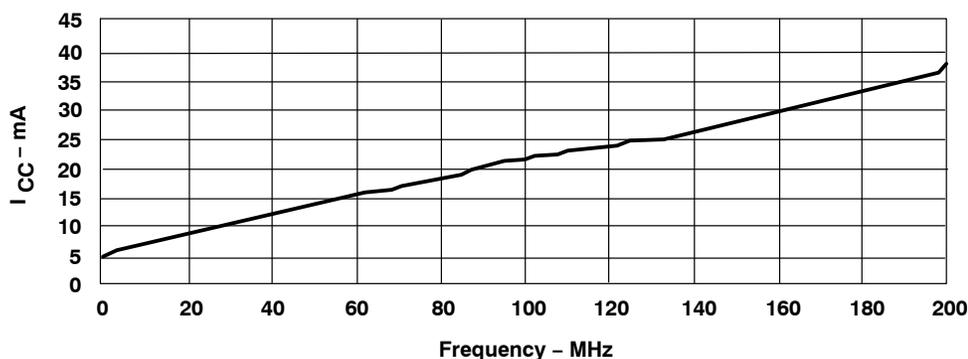


Figure 16.  $I_{CC}$  vs Frequency (Single-Output Switching Enabled)

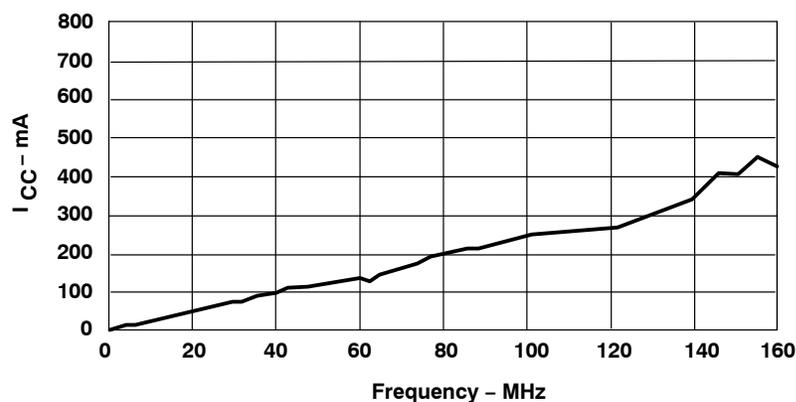


Figure 17.  $I_{CC}$  vs Frequency (16 Outputs Switching)

## Output-to-Output Skew

This feature is important in an application in which clock distribution and high-speed data buffering are an issue, mostly found in backplane applications. Output-to-output skew indicates the variance in the output switching times. If an application has a requirement for a minimum amount of skew, this is probably the parameter with which the engineer is concerned. When conducting this test, the inputs were tied together and switched and the difference in the outputs was subsequently computed; for comparison purposes, competitors have labeled this value  $t_{sko}$ . For the ALVTH16244, observed  $t_{sko}$  is  $\leq 250$  ps (typical).

## Packaging Availability and Nomenclature

The ALVT family is available in the SSOP (DL), TSSOP (DGG), and the TVSOP (DGV) packages. For order entry, the device part number is limited to 18 alphanumeric characters; therefore, the package designation for DGG (TSSOP) is shortened to G, and DGV (TVSOP) is shortened to V, as shown in the data sheets.

## **Summary**

The ALVT family is optimized for high-performance applications. With the high-drive capability and the low propagation delays, along with low power dissipation and good signal integrity, this family is useful for high-end telecom and networking end equipments. The advanced features, such as auto3-state and the 5-V-tolerant I/Os, make the family compatible with mixed-mode environments.

## **Acknowledgment**

The authors of this application report are Shankar Balasubramaniam, Shaun Pugh, Ernest Cox, and Gary Abbe. The authors acknowledge the assistance provided by Rob Wilson and Mac McCaughey.



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# **Comparison of Electrical and Thermal Parameters of Widebus™ SMD SSOP, TSSOP, TVSOP, and LFBGA Packages**

Johannes Huchzermeier

Standard Linear and Logic

## **ABSTRACT**

The trend toward 16- and 32-bit-wide bus systems, in conjunction with continuing advances in surface-mount technology during the 1980s and 1990s, led to the development of ever-smaller packages combined with increased integrated-circuit performance. The improvement in the electrical characteristics of the packages also made possible development of smaller-footprint packages for Widebus™ circuits. In the mid-1980s, Texas Instruments produced Widebus™ devices with improved electrical characteristics and expanded data width, supporting up to 20 bits in a single package.

Now, Texas Instruments is launching the low-profile, fine-pitch, ball grid array (LFBGA). The LFBGA is the first ball grid array package (BGA) for logic components, featuring improved signal characteristics, as well as increased integration.

With new designs that support up to 36 bits in a single package, doubling of component density on the printed circuit board using Widebus packages has been achieved.

The purpose of this report is to familiarize designers with the advantages of this package option by comparing the mechanical data, electrical characteristics, and thermal parameters of four packages: 48-pin SSOP (Shrink Small-Outline Package), 48-pin TSSOP (Thin Shrink Small-Outline Package), 48-pin TVSOP (Thin Very Small-Outline Package), and 96-pin LFBGA (Low-profile Fine-pitch Ball Grid Array), using the 244-function (unidirectional) buffer/driver of the LVC logic family.

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## Introduction

The introduction of surface-mount technology at the beginning of the 1980s led to a major reduction in the component space needed on the circuit board. Users exploited this advantage either by reducing the space needed for a given system or by increasing system performance, while using the same amount of space. The steadily increasing integration of electrical circuitry also created pressure for advances in the miniaturization of packages. Standard components, such as bus drivers, also were produced in ever-smaller space-saving packages.

During the same period, the transition from 8-bit processors to 16- and 32-bit processors occurred. The associated enlargement of data and address buses tended to counteract the space advantage that had been gained because two or four modules now had to be used in place of a single bus driver.

In order to satisfy the user's need for more compact equipment, Texas Instruments (TI™) developed new packages suitable for surface-mount technology:

- SSOP (Shrink Small-Outline Package) doubles the number of bits within one package, while requiring no more space than the usual 8-bit SOP (Small Outline Package) modules
- TSSOP (Thin Shrink Small-Outline Package) represents a significant space saving over the SSOP package, and also is suitable for use in PCMCIA plug-in boards due its reduced package height
- TVSOP (Thin Very Small-Outline Package) permits a further space saving of up to 38% compared to the TSSOP package

Also, emphasis was placed on important factors, such as the speed of the new functions, while striving to keep interference voltages as low as possible.

However, miniaturization of package types to 0.4 mm pin-to-pin distance, reached the limit for reliable manufacturing processes, and led to the development of ball grid arrays.

The LFBGA (Low-profile Fine-pitch Ball Grid Array) package represents the ideal solution because it combines minimal space requirements with low package parasitics and a high level of functional density.

This report compares the dimensions, electrical characteristics, and thermal parameters of four packages:

SSOP	(Shrink Small-Outline Package) for Widebus	48-pin DL
TSSOP	(Thin Shrink Small-Outline Package) for Widebus	48-pin DGG
TVSOP	(Thin Very Small-Outline Package) for Widebus	48-pin DGV
LFBGA	(Low-profile Fine-pitch Ball Grid Array)	96-ball GKE

In addition to package names and the number of external connections, each package type is designated by a clearly defined abbreviation (e.g., DL, DGG, DGV, and GKE), which is used when ordering a component.

The influence of package type on electrical characteristics is investigated in this application report, using measurements on the unidirectional buffer components SN74LVH16244A and SN74LVCH32244A.

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## Package Parameters

The increasing speed of integrated circuits makes the electrical characteristics of the package even more important.

In addition to the inevitable parasitic capacitances of the leads within a package, their inductance is the major factor determining the behavior of fast digital circuits, limiting ranges of applications in some cases.

Furthermore, with reduced distances between pins, the pins' coupling factors are increasingly important.

Supply-voltage connections should have low inductance values. For all signal lines a good package should show the lowest possible values for the following electrical variables:

- Capacitance of a pin against ground
- Inductance of the pins
- The pins' mutual-coupling factors.

The pins' mutual-coupling factors can be determined, using the general-transformer equation.

$$k = \frac{M}{\sqrt{L_1 \times L_2}} \quad (1)$$

Where:

- M = coupling inductance
- L<sub>1</sub> and L<sub>2</sub> = respective self-inductance of the pin connections
- k = the inductive coupling factor

The three electrical variables of a package are determined by:

- Line length of the pins in the package
- Distance between the lines
- Length of the bonding wires.

For purposes of comparison, note that large dual in-line packages, PDIPs (plastic dual in-line packages), for example, have significantly longer leads than SSOP, TSSOP, TVSOP, or LFBGA packages.

A long lead produces high inductance and high coupling factors. Also, the large surfaces resulting from the long line result in higher capacitance. With small package types, such as the TSSOP, the inductance and capacitance of the leads is significantly less. However, the coupling-factor advantage gained by the short leads is partially offset by the minimal distance between the leads, thereby increasing the coupling factor.



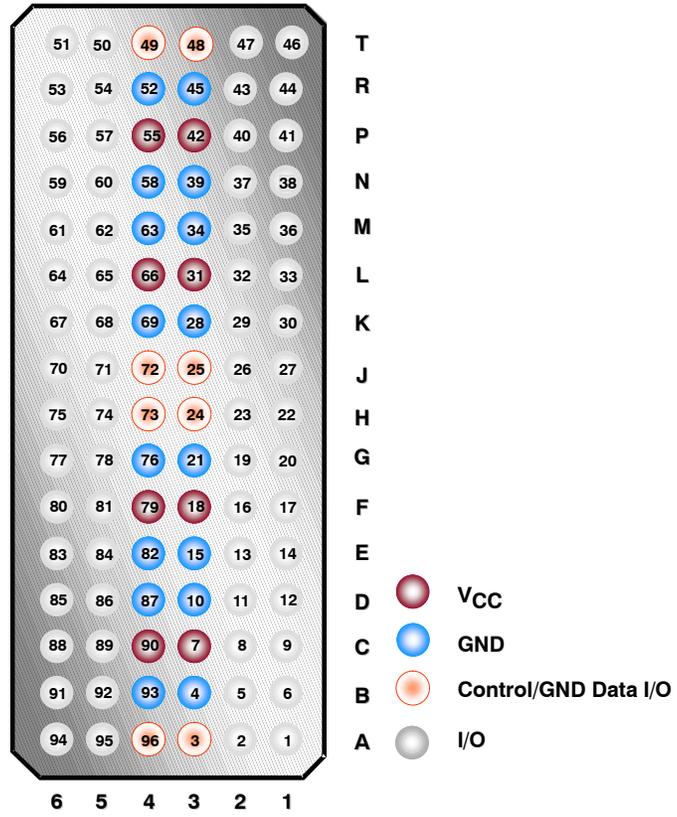


Figure 2. 32-Bit Package for 96-Ball Low-Profile Fine-Pitch Ball Grid Arrays

**Table 1. SSOP 48-Pin Capacitance, Inductance, and Coupling-Factor (k) Package Parameters**

Pin	Capacitance Pin to GND (pF)	Inductance Die to Pin (nH)	Coupling Factor (k)			Pin	Capacitance Pin to GND (pF)	Inductance Die to Pin (nH)	Coupling Factor (k)		
			Pin	Pin	Factor				Pin	Pin	Factor
1	0.44	7.97	1	2	0.48	48	0.44	7.97	48	1	0.06
2	0.24	7.30	2	3	0.49	47	0.24	7.30	47	48	0.48
3	0.20	6.76	3	4	0.49	46	0.20	6.76	46	47	0.49
4	0.18	6.27	4	5	0.48	45	0.18	6.27	45	46	0.49
5	0.16	5.86	5	6	0.46	44	0.16	5.86	44	45	0.48
6	0.16	5.80	6	7	0.46	43	0.16	5.80	43	44	0.46
7	0.18	5.66	7	8	0.47	42	0.18	5.66	42	43	0.46
8	0.12	5.50	8	9	0.47	41	0.12	5.50	41	42	0.47
9	0.10	5.30	9	10	0.48	40	0.10	5.30	40	41	0.47
10	0.08	5.19	10	11	0.48	39	0.08	5.19	39	40	0.48
11	0.07	5.08	11	12	0.44	38	0.07	5.08	38	39	0.48
12	0.21	5.86	12	13	0.54	37	0.21	5.86	37	38	0.44
13	0.21	5.86	13	14	0.44	36	0.21	5.86	36	37	0.54
14	0.07	5.08	14	15	0.48	35	0.07	5.08	35	36	0.44
15	0.08	5.19	15	16	0.48	34	0.08	5.19	34	35	0.48
16	0.10	5.30	16	17	0.47	33	0.10	5.30	33	34	0.48
17	0.12	5.50	17	18	0.47	32	0.12	5.50	32	33	0.47
18	0.18	5.66	18	19	0.46	31	0.18	5.66	31	32	0.47
19	0.16	5.80	19	20	0.46	30	0.16	5.80	30	31	0.46
20	0.16	5.86	20	21	0.48	29	0.16	5.86	29	30	0.46
21	0.18	6.27	21	22	0.49	28	0.18	6.27	28	29	0.48
22	0.20	6.76	22	23	0.49	27	0.20	6.76	27	28	0.49
23	0.24	7.30	23	24	0.48	26	0.24	7.30	26	27	0.49
24	0.44	7.97	24	25	0.06	25	0.44	7.97	25	26	0.48

**Table 2. TSSOP 48-Pin Capacitance, Inductance, and Coupling-Factor (k) Package Parameters**

Pin	Capacitance Pin to GND (pF)	Inductance Die to Pin (nH)	Coupling Factor (k)			Pin	Capacitance Pin to GND (pF)	Inductance Die to Pin (nH)	Coupling Factor (k)		
			Pin	Pin	Factor				Pin	Pin	Factor
1	0.41	3.92	1	2	0.39	48	0.40	3.99	48	1	0.03
2	0.22	3.63	2	3	0.38	47	0.22	3.63	47	48	0.4
3	0.19	3.37	3	4	0.36	46	0.19	3.31	46	47	0.39
4	0.18	3.02	4	5	0.35	45	0.17	3.06	45	46	0.37
5	0.19	2.99	5	6	0.34	44	0.17	2.91	44	45	0.35
6	0.20	2.81	6	7	0.31	43	0.18	2.80	43	44	0.34
7	0.12	2.71	7	8	0.32	42	0.16	2.69	42	43	0.34
8	0.12	2.70	8	9	0.33	41	0.11	2.58	41	42	0.33
9	0.10	2.59	9	10	0.35	40	0.10	2.52	40	41	0.34
10	0.09	2.54	10	11	0.35	39	0.09	2.45	39	40	0.35
11	0.08	2.46	11	12	0.36	38	0.08	2.37	38	39	0.34
12	0.08	2.43	12	13	0.35	37	0.08	2.37	37	38	0.36
13	0.08	2.42	13	14	0.35	36	0.08	2.37	36	37	0.35
14	0.08	2.45	14	15	0.35	35	0.08	2.38	35	36	0.36
15	0.09	2.50	15	16	0.35	34	0.09	2.44	34	35	0.36
16	0.10	2.55	16	17	0.34	33	0.10	2.51	33	34	0.34
17	0.11	2.62	17	18	0.33	32	0.11	2.57	32	33	0.34
18	0.15	2.69	18	19	0.33	31	0.16	2.69	31	32	0.33
19	0.18	2.83	19	20	0.34	30	0.18	2.78	30	31	0.33
20	0.17	2.98	20	21	0.35	29	0.17	2.87	29	30	0.33
21	0.17	3.06	21	22	0.37	28	0.17	2.98	28	29	0.35
22	0.19	3.34	22	23	0.39	27	0.19	3.26	27	28	0.37
23	0.22	3.66	23	24	0.39	26	0.22	3.55	26	27	0.39
24	0.40	3.96	24	25	0.03	25	0.40	3.89	25	26	0.4

**Table 3. TVSOP 48-Pin Capacitance, Inductance, and Coupling-Factor (k) Package Parameters**

Pin	Capacitance Pin to GND (pF)	Inductance Die to Pin (nH)	Coupling Factor (k)			Pin	Capacitance Pin to GND (pF)	Inductance Die to Pin (nH)	Coupling Factor (k)		
			Pin	Pin	Factor				Pin	Pin	Factor
1	0.30	4.02	1	2	0.38	48	0.30	4.01	48	1	0.13
2	0.18	3.72	2	3	0.39	47	0.18	3.72	47	48	0.38
3	0.14	3.46	3	4	0.39	46	0.14	3.44	46	47	0.39
4	0.12	3.21	4	5	0.4	45	0.12	3.20	45	46	0.39
5	0.12	2.93	5	6	0.42	44	0.12	2.93	44	45	0.4
6	0.12	2.80	6	7	0.38	43	0.12	2.80	43	44	0.42
7	0.08	2.68	7	8	0.4	42	0.08	2.67	42	43	0.37
8	0.07	2.58	8	9	0.4	41	0.07	2.56	41	42	0.39
9	0.06	2.51	9	10	0.41	40	0.06	2.47	40	41	0.39
10	0.06	2.40	10	11	0.42	39	0.06	2.43	39	40	0.41
11	0.05	2.40	11	12	0.41	38	0.05	2.39	38	39	0.41
12	0.05	2.40	12	13	0.42	37	0.05	2.38	37	38	0.41
13	0.05	2.43	13	14	0.42	36	0.05	2.42	36	37	0.42
14	0.05	2.46	14	15	0.42	35	0.05	2.47	35	36	0.42
15	0.06	2.59	15	16	0.41	34	0.06	2.55	34	35	0.41
16	0.06	2.65	16	17	0.4	33	0.06	2.64	33	34	0.4
17	0.07	2.79	17	18	0.39	32	0.07	2.78	32	33	0.4
18	0.08	2.96	18	19	0.39	31	0.08	2.88	31	32	0.39
19	0.12	3.21	19	20	0.41	30	0.11	3.23	30	31	0.37
20	0.12	3.49	20	21	0.39	29	0.12	3.52	29	30	0.42
21	0.12	3.49	21	22	0.39	28	0.12	3.52	28	29	0.4
22	0.14	3.74	22	23	0.38	27	0.14	3.70	27	28	0.38
23	0.18	3.99	23	24	0.38	26	0.18	3.93	26	27	0.39
24	0.30	4.31	24	25	0.12	25	0.30	4.29	25	26	0.38

**Table 4. LFBGA 96-Ball Package Parameters (Balls 1 – 48) (Balls 49 – 96 Analog)**

Ball	Capacitance Ball to GND (pF)	Inductance Ball to Die (nH)	Ball Number and Coupling															
			[Diagram]		[Diagram]		[Diagram]		[Diagram]		[Diagram]		[Diagram]		[Diagram]		[Diagram]	
1	0.14	2.87																
2	0.06	1.65							2	0.25	5	0.08	6	0.06				
3	0.07	1.76							3	0.29	4	0.17	5	0.17	6	0.09	1	0.25
4	0.12	2.83	2	0.17	3	0.25	96		96		93		4	0.25	5	0.19	2	0.29
5	0.05	1.74	1	0.08	2	0.17	3	0.19	4	0.25	7	0.16	8	0.16	9	0.09	6	0.29
6	0.05	1.77			1	0.06	2	0.09	5	0.29	8	0.18	9	0.17				
7	0.11	2.75	5	0.16	4	0.15	93		90		87		10	0.16	11	0.19	8	0.26
8	0.05	1.66	6	0.18	5	0.16	4	0.08	7	0.26	10	0.18	11	0.19	12	0.10	9	0.29
9	0.05	1.75			6	0.17	5	0.09	8	0.29	11	0.22	12	0.17				
10	0.12	2.66	8	0.18	7	0.16	90		87		82		15	0.08	13	0.11	11	0.29
11	0.05	1.62	9	0.22	8	0.19	7	0.19	10	0.29	15	0.07	13	0.19	14	0.11	12	0.24
12	0.05	1.70			9	0.17	8	0.10	11	0.24	13	0.29	14	0.24				
13	0.06	1.91	12	0.29	11	0.19	10	0.11	15	0.15	18	0.06	16	0.16	17	0.10	14	0.29
14	0.05	1.73			12	0.24	11	0.11	13	0.29	16	0.18	17	0.18				
15	0.11	2.63	11	0.07	10	0.08	87		82		79		18	0.15	16	0.32	13	0.15
16	0.05	1.86	14	0.18	13	0.16	15	0.32	18	0.15	21	0.06	19	0.16	20	0.09	17	0.30
17	0.05	1.70			14	0.18	13	0.10	16	0.30	19	0.16	20	0.16				
18	0.11	2.67	13	0.06	15	0.15	82		79		76		21	0.15	19	0.32	16	0.15
19	0.05	1.91	17	0.16	16	0.16	18	0.32	21	0.16	24	0.06	23	0.12	22	0.11	20	0.30
20	0.05	1.68			17	0.16	16	0.09	19	0.30	23	0.12	22	0.20				
21	0.10	2.68	16	0.06	18	0.15	79		76		73		24	0.14	23	0.17	19	0.16
22	0.05	1.72			20	0.20	19	0.11	23	0.33	26	0.06	27	0.08				
23	0.05	1.60	20	0.12	19	0.12	21	0.17	24	0.21	25	0.09	26	0.11	27	0.06	22	0.33
24	0.10	2.85	19	0.06	21	0.14	76		73		72		25	0.32	26	0.09	23	0.21
25	0.10	2.85	23	0.09	24	0.32	73		72		69		28	0.14	29	0.07	26	0.21
26	0.05	1.60	22	0.06	23	0.11	24	0.09	25	0.32	28	0.17	29	0.15	30	0.09	27	0.33
27	0.05	1.72			22	0.08	23	0.06	26	0.33	29	0.16	30	0.15				
28	0.11	2.68	26	0.17	25	0.14	72		69		66		31	0.15	32	0.07	29	0.21
29	0.05	1.74	27	0.16	26	0.15	25	0.07	28	0.21	31	0.19	32	0.16	33	0.10	30	0.32
30	0.05	1.70			27	0.15	26	0.09	29	0.32	32	0.17	33	0.16				
31	0.10	2.68	29	0.19	28	0.15	69		66		63		34	0.15	35	0.08	32	0.21
32	0.05	1.76	30	0.17	29	0.16	28	0.07	31	0.21	34	0.19	35	0.17	36	0.10	33	0.31
33	0.05	1.70			30	0.16	29	0.10	32	0.31	35	0.19	36	0.17				
34	0.10	2.63	32	0.19	31	0.15	66		63		58		39	0.05	37	0.10	35	0.22
35	0.05	1.79	33	0.19	32	0.17	31	0.08	34	0.22	39	0.09	37	0.23	38	0.10	36	0.30
36	0.05	1.75			33	0.17	32	0.10	35	0.17	37	0.30	38	0.13				
37	0.05	1.76	36	0.30	35	0.17	34	0.10	39	0.18	42	0.06	40	0.17	41	0.10	38	0.21
38	0.11	2.60			36	0.13	35	0.10	37	0.21	40	0.19	41	0.12				
39	0.05	1.68	35	0.09	34	0.05	63		58		55		42	0.11	40	0.33	37	0.18

**Table 4. LFBGA 96-Ball Package Parameters (Balls 1 – 48) (Balls 49 – 96 Analog) (Continued)**

Ball	Capacitance Ball to GND (pF)	Inductance Ball to Die (nH)	Ball Number and Coupling															
			38		37		39		42		45		43		44		41	
																		
40	0.05	1.81	38	0.19	37	0.17	39	0.33	42	0.17	45	0.06	43	0.17	44	0.09	41	0.28
41	0.05	1.66			38	0.12	37	0.10	40	0.28	43	0.18	44	0.15				
42	0.11	2.75	37	0.06	39	0.11	58		55		52		45	0.15	43	0.25	40	0.17
43	0.05	1.84	41	0.18	40	0.17	42	0.25	45	0.17	48	0.06	47	0.13	46	0.13	44	0.28
44	0.06	1.85			41	0.15	40	0.09	43	0.28	47	0.13	46	0.25				
45	0.11	2.83	40	0.06	42	0.15	55		52		49		48	0.16	47	0.16	43	0.17
46	0.06	1.75			44	0.25	43	0.13	47	0.28								
47	0.06	1.66	44	0.13	43	0.13	45	0.16	48	0.25							46	0.28
48	0.14	2.87	43	0.06	45	0.16	52		49									

Table 5 gives the maximum and minimum values of capacitance and inductance and the maximum value for the mutual coupling of two pins from Tables 1 through 4.

**Table 5. Comparison of Capacitance, Inductance, and Coupling-Factor (k) Package Parameters**

	Capacitance Pin to GND (pF)		Inductance Die to Pin (nH)	Coupling Factor (k) Pin to Pin (nH)
	MAX	MIN		
SSOP 48 pin	MAX	0.443	7.970	0.54
	MIN	0.074	5.080	
	DELTA	0.369	2.890	
TSSOP 48 pin	MAX	0.410	3.990	0.40
	MIN	0.077	2.370	
	DELTA	0.333	1.620	
TVSOP 48 pin	MAX	0.296	4.310	0.42
	MIN	0.048	2.380	
	DELTA	0.248	1.930	
LFBGA 96 ball	MAX	0.145	2.866	0.42
	MIN	0.046	1.597	
	DELTA	0.099	1.269	

The lower the parasitic parameters for a package are, the better the electrical quality of the package. In this comparison, the SSOP package showed the highest values for all parameters and the largest difference between maximum and minimum values. The SSOP maximum value is 180% higher than the value for the LFBGA 96-ball packages, and the difference between its maximum and minimum values is more than twice as great as for the LFBGA 96-ball package.

A comparison of the LFBGA 96-ball package with the dual in-line Widebus package types also demonstrates the superiority of the ball grid array package over the dual in-line Widebus package. The effects of lead inductance are examined in greater detail in the *Electrical Characteristics* section.

## Electrical Characteristics

If one or more outputs switch, current flowing through the output lines leads to voltage drops, particularly to the inductance ( $L_P$ ) of the lines of the supply voltage ( $V_{CC}$ ) and GND. This voltage drop ( $U_{LP}$ ) can be calculated using equation 2:

$$U_{LP} = -L_P \frac{\Delta i}{\Delta t} \quad (2)$$

$U_{LP}$  is superimposed within the circuit on the supply-voltage pins and ground pins and also is directly superimposed on the potential of the outputs, which do not switch. Because the amplitude of the interference is dependent on the current, it increases with increasing numbers of simultaneously switching outputs. Simultaneous switching interference is interference caused by the simultaneous switching of several outputs. There are various methods of reducing the amplitude of the interference.

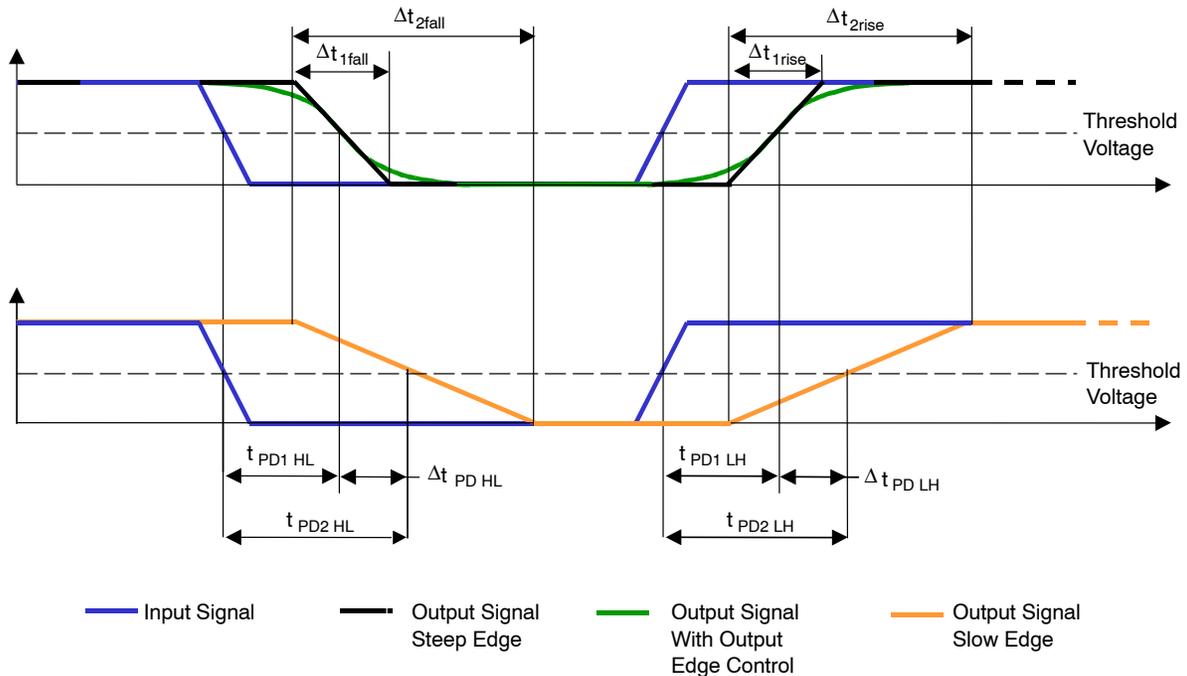
First, the output current [ $\Delta i$  in equation (2)], i.e., the current drive capability, which influences the amplitude of the interference, can be limited. However, this solution is not applicable in many packages because a large current is needed to drive low-impedance lines.

The second option is to reduce the slew rate at the start of switching, or, in other words, to increase the switching duration ( $\Delta t$ ) in equation 2.

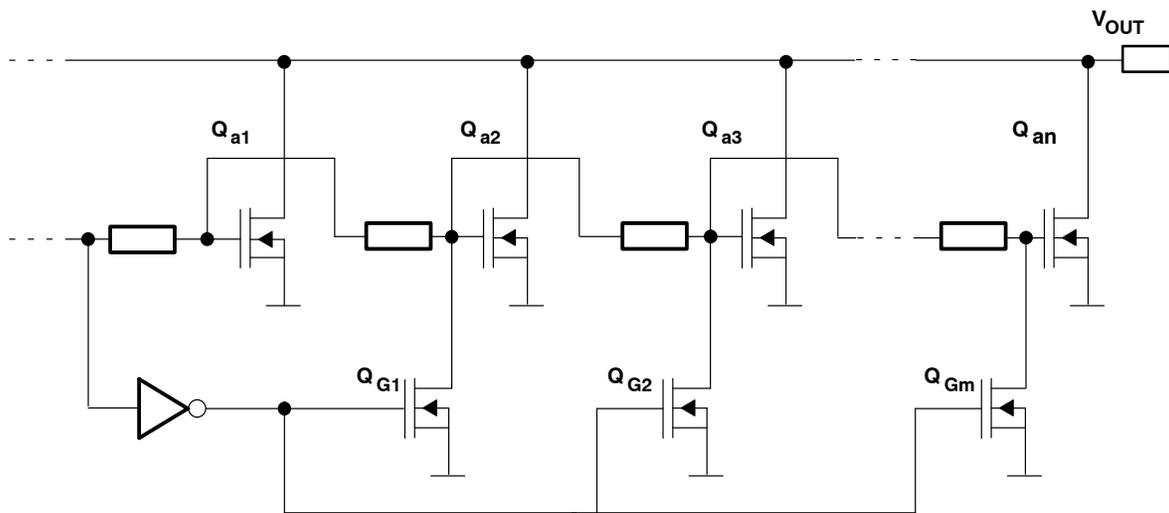
However, because the propagation delay time is measured at the threshold voltage, which is one-half the supply voltage with CMOS or 1.5 V with bipolar technology, the propagation delay time increases proportionately with a steeper output signal edge. Therefore, this solution also is of very limited use.

To reduce signal slew-rate (see Figure 3), TI uses a switching technique known as Output Edge Control (OEC™) in the output stages of modern logic circuits (see Figure 4).

OEC is a trademark of Texas Instruments Incorporated.



**Figure 3. Influence of Slew Rate on Propagation Delay Time and the Principle Behind OEC**



**Figure 4. Basic Structure of the OEC Output Stage**

The output stage, as a whole, is divided into several mini-output stages whose drain and source connections are each switched in parallel. The gates of these transistors are triggered in a delayed fashion. The resistance of these transistors before the gates, together with the input capacitance of the transistors (Miller capacitance), creates a signal delay line. When a signal is applied to this arrangement, the whole transistor does not switch on at once, rather the individual part transistors conduct one after the other. Thus, the closing of the circuit is delayed so that, on output, there is a transition rise time or fall time of about 2 ns. When switching off, the gates of the output transistors are switched off without delay via transistors  $Q_{G1}$  to  $Q_{Gm}$  to limit the current spikes occurring when switching from push-pull output stages. However, any further delaying of edges by this method is not possible.

The measures cited thus far are not sufficient to adequately damp the interference mentioned above. Accordingly, the inductance of the supply-voltage lead ( $L_P$ ) must be reduced. The distance of the silicon from the pin connections and, therefore, the inductance, is determined decisively by the length of the lead. Therefore, the best solution is to reduce the size of the package as much as possible. In the case of modern logic circuits, with a propagation delay time of less than 6 ns, a reduction of the inductance in the supply leads results in an increase in speed because the braking effect of lead inductance is reduced.

In Widebus packages, additional grounding and supply connections are inserted along the whole width of the circuit, an arrangement known as staggered pinout. This does increase the number of pins, but the main advantage is that the interference voltages that can arise due to crosstalk between two neighboring connections are significantly reduced. Additionally, this distribution of supply connections results in a significant reduction in lead inductance.

## Simultaneous-Switching Behavior

Figure 5 shows the simultaneous-switching measurement setup and the position of the outputs examined.

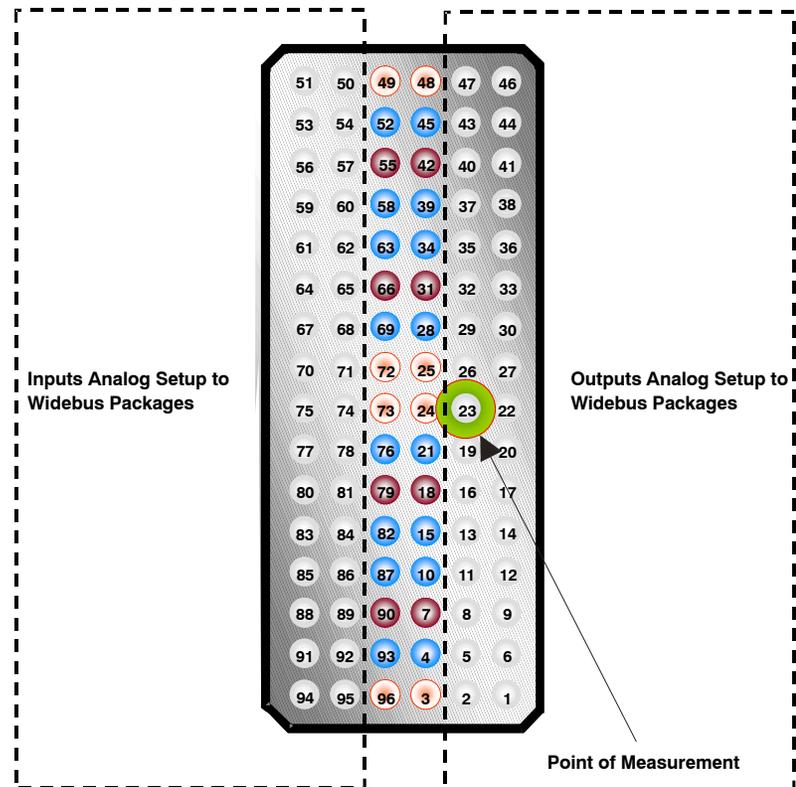
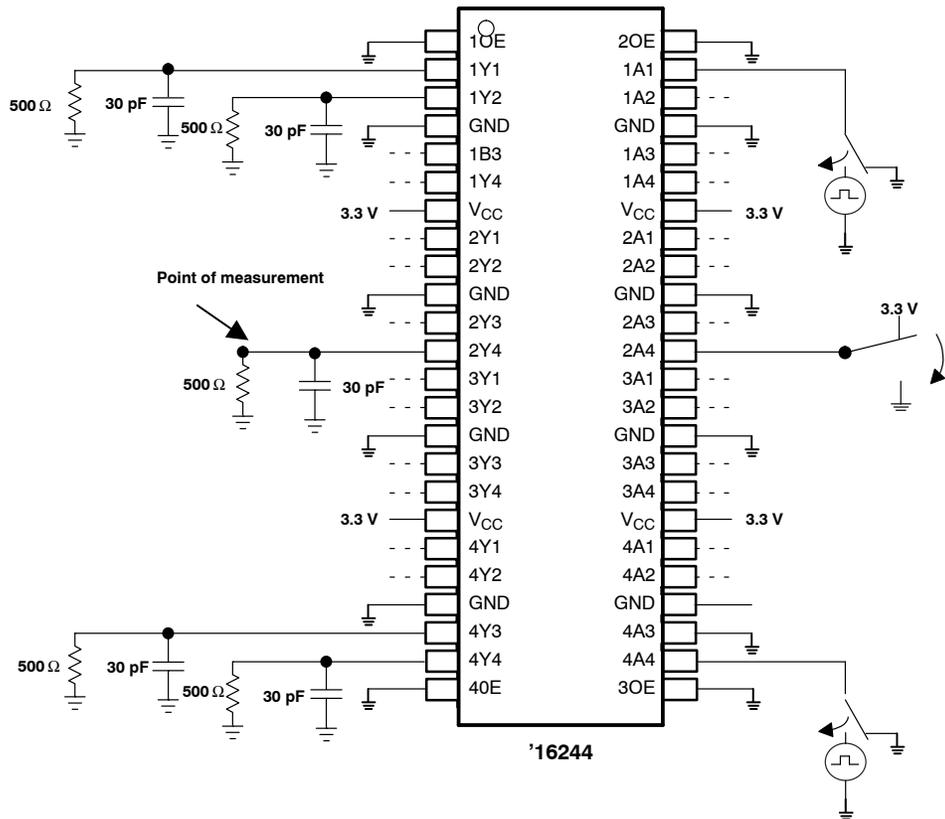


Figure 5. Simultaneous-Switching Measurement Setup

For this measurement procedure, one input is connected to a fixed low (L) state, or high (H) state, while all other inputs are switched simultaneously. The outputs of the connecting driver react to the changes in the various inputs with a certain delay, while the nonswitched output should maintain a constant low state (or high state).

However, three factors lead to a reaction by the nonconnected input:

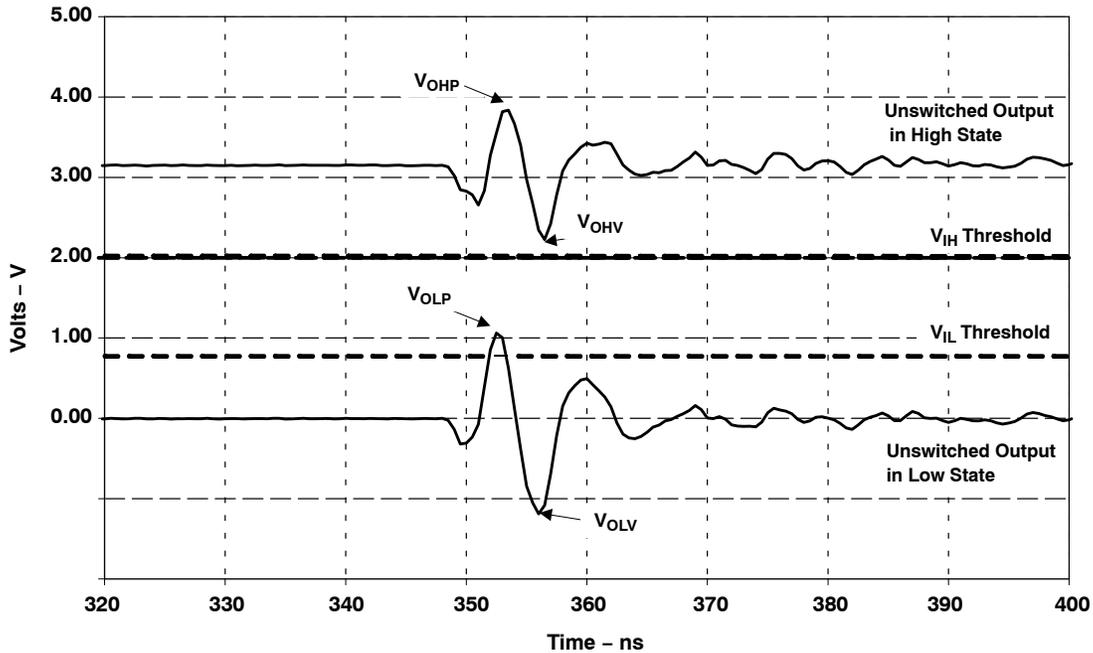
- Crosstalk between neighboring pins
- A brief notch in the supply voltage, not measurable from outside, caused by the inductance of the  $V_{CC}$  lead
- A brief increase in the grounding level, not measurable from outside, caused by the ground lead

The worst case possible for the measurement procedure is when the distance to the GND and supply pins is greatest. Accordingly, for the Widebus package, measurements are made at pin 37 (2A2) and for the LFBGA at ball 23 (4A4).

Figure 6 sets out the parameters and definitions of significance for this measurement procedure. Points on the curves are defined as:

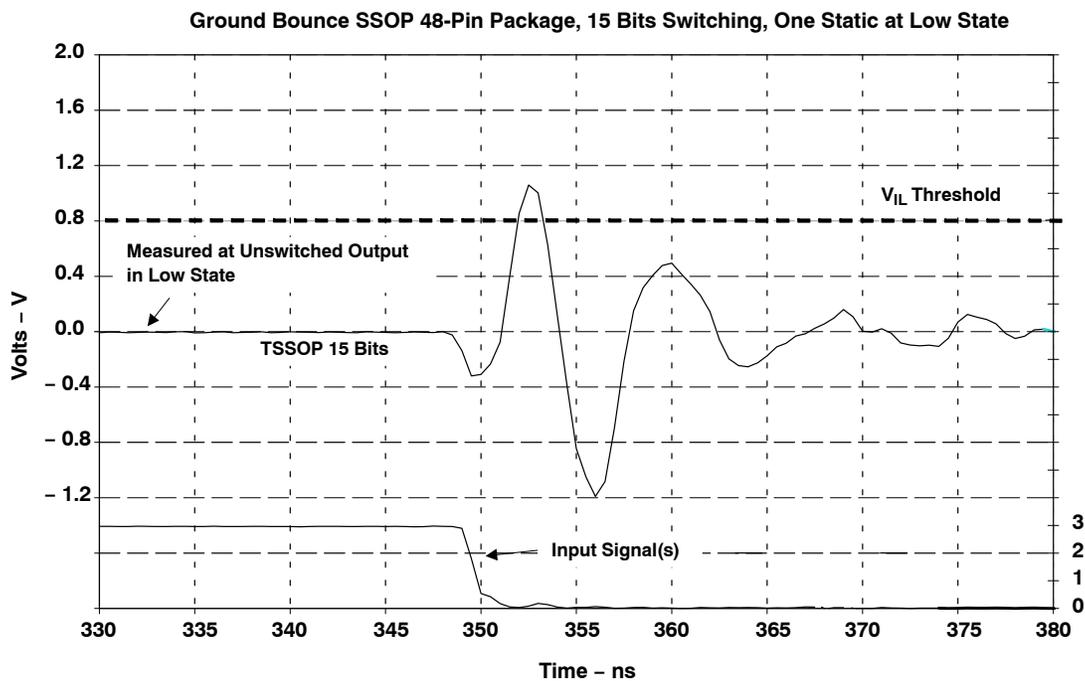
$V_{OHP}$ (voltage output high peak):	High bounce: peak output-voltage value during a static high at the nonswitched output
$V_{OHV}$ (voltage output high valley):	High bounce: minimum output-voltage value during a static high at the nonswitched output
$V_{OLP}$ (voltage output low peak):	Ground bounce: peak output-voltage value during a static low at the nonswitched output
$V_{OLV}$ (voltage output low valley):	Ground bounce: minimum output-voltage value during a static low at the nonswitched output

The critical parameters are  $V_{OLP}$  and  $V_{OHV}$  because, in the worst case, they could exceed the switching thresholds  $V_{IH}$  and  $V_{IL}$ .



**Figure 6. Simultaneous-Switching Parameter**

The ground- and high-bounce measurements for the simultaneous switching of several outputs are given in Figures 7 through 14 for the package types investigated in this report.



**Figure 7. Measured Simultaneous-Switching Ground Bounce, SSOP 48-Pin Package**

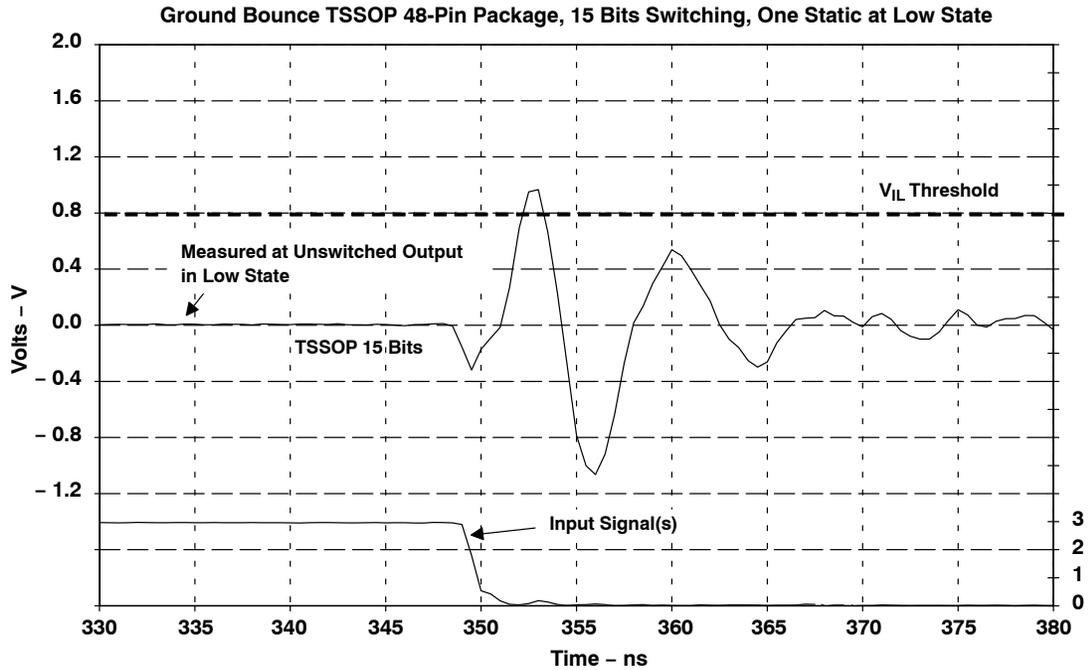


Figure 8. Measured Simultaneous-Switching Ground Bounce, TSSOP 48-Pin Package

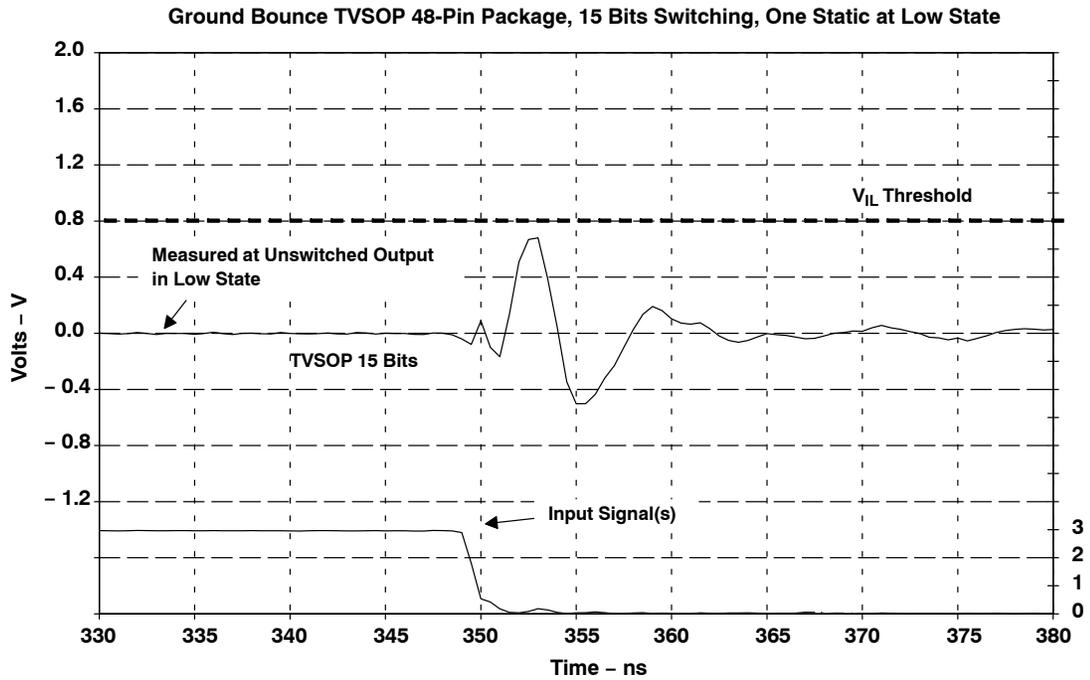


Figure 9. Measured Simultaneous-Switching Ground Bounce, TVSOP 48-Pin Package

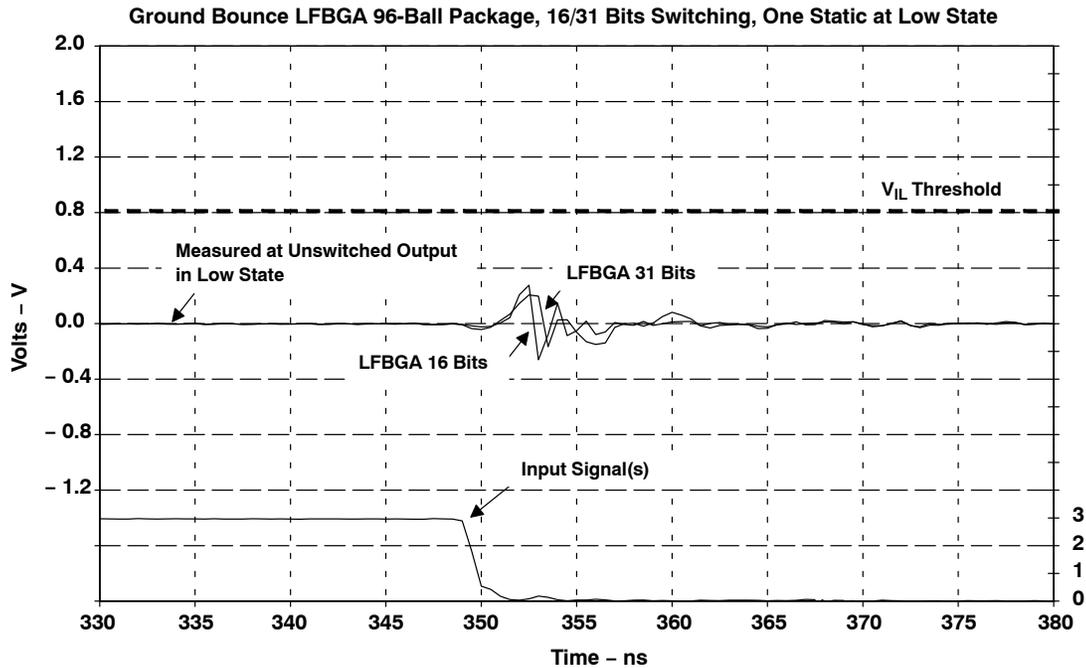


Figure 10. Measured Simultaneous-Switching Ground Bounce, LFBGA 96 Ball

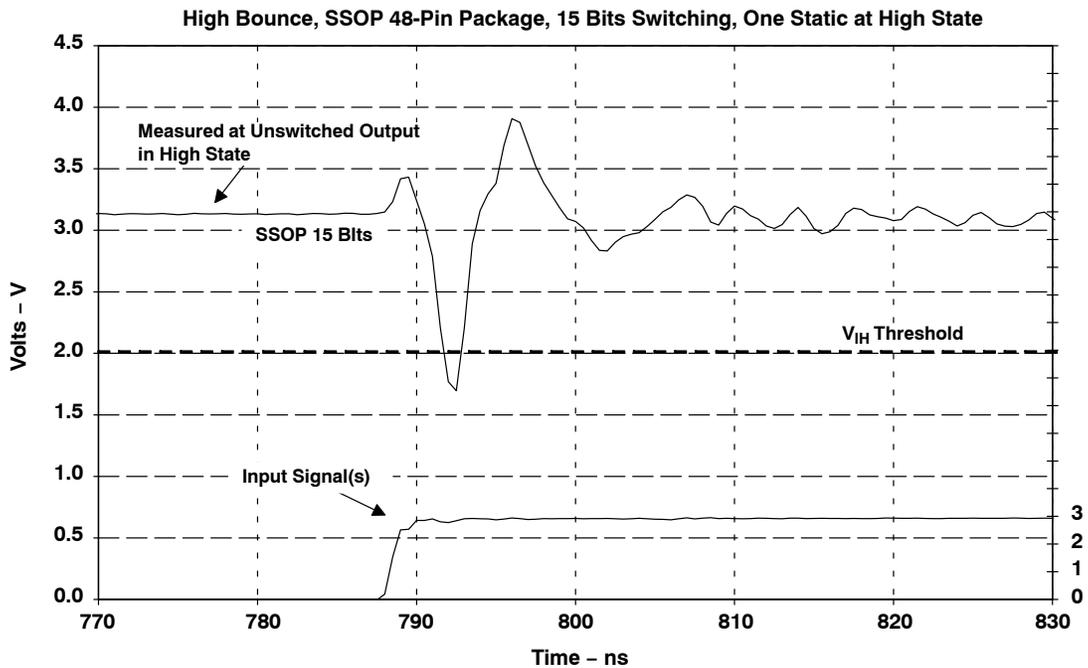


Figure 11. Measured Simultaneous-Switching High Bounce, SSOP 48-Pin Package

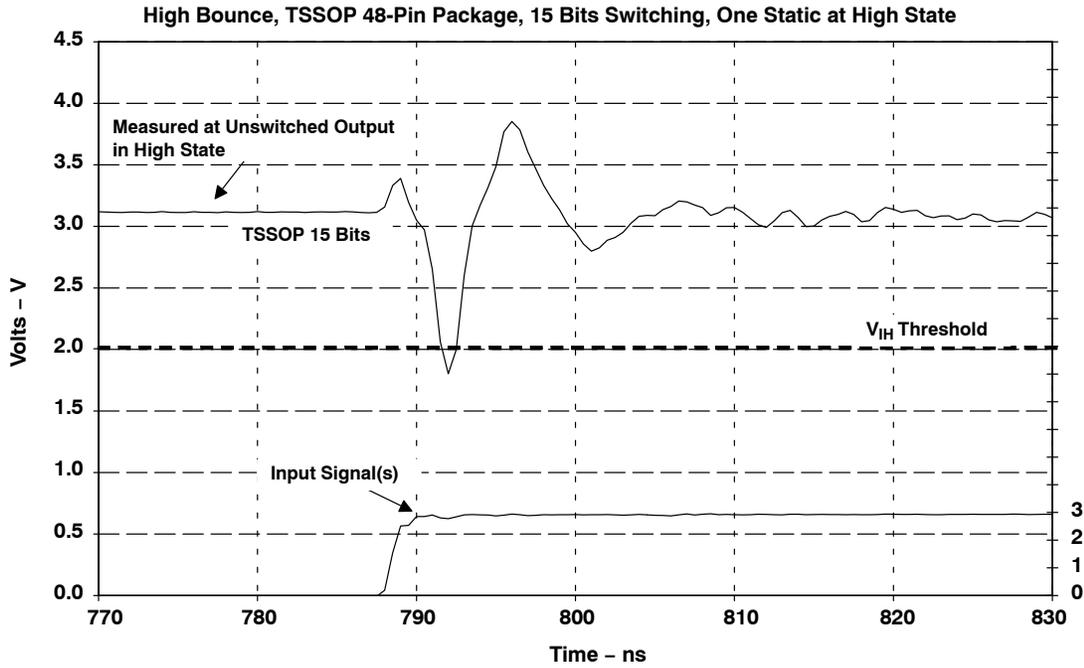


Figure 12. Measured Simultaneous-Switching High Bounce, TSSOP 48-Pin Package

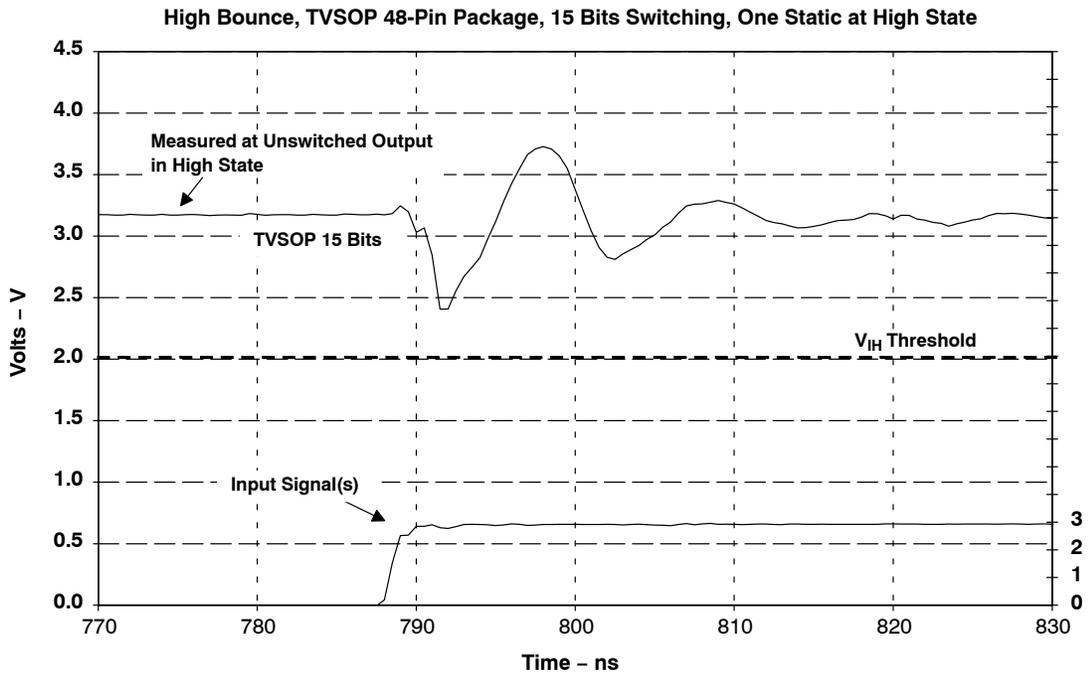
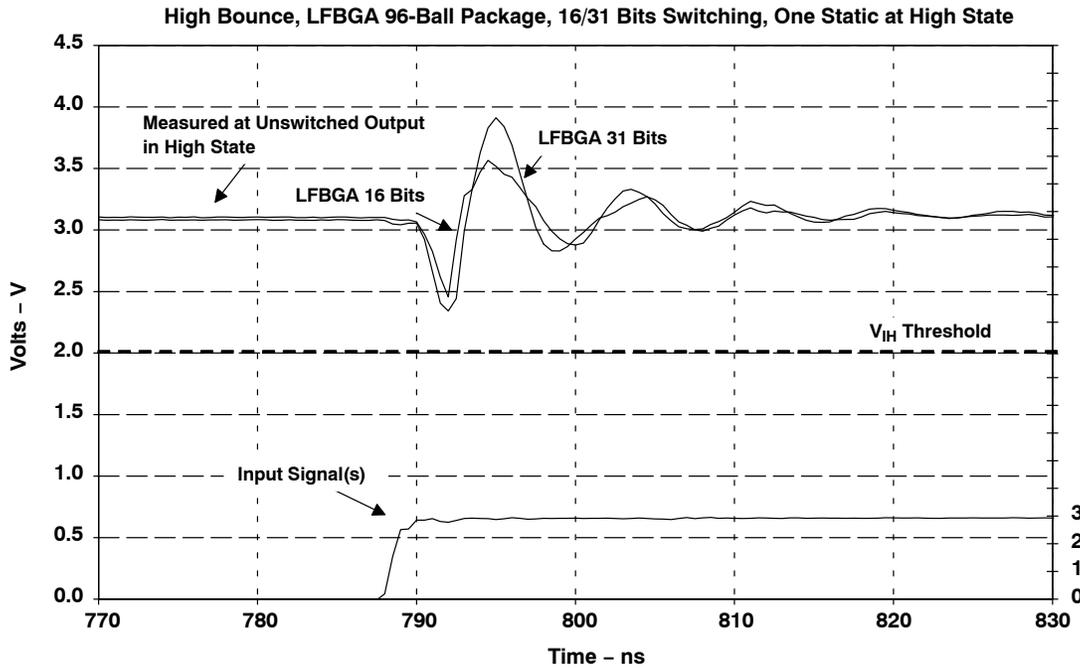
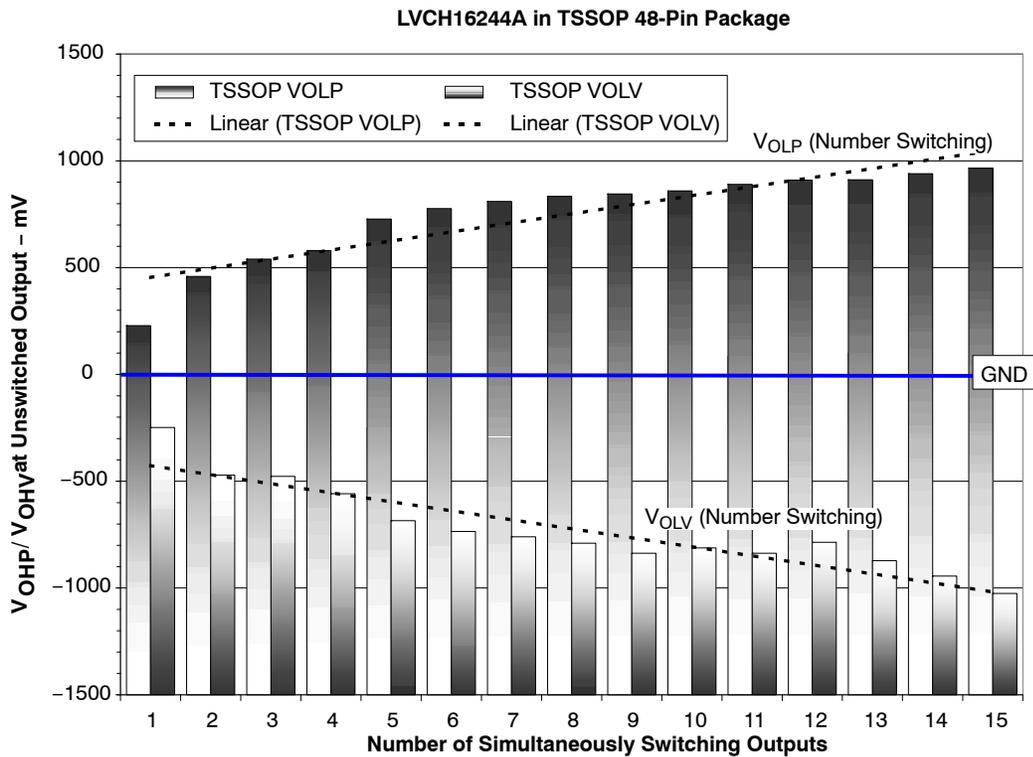
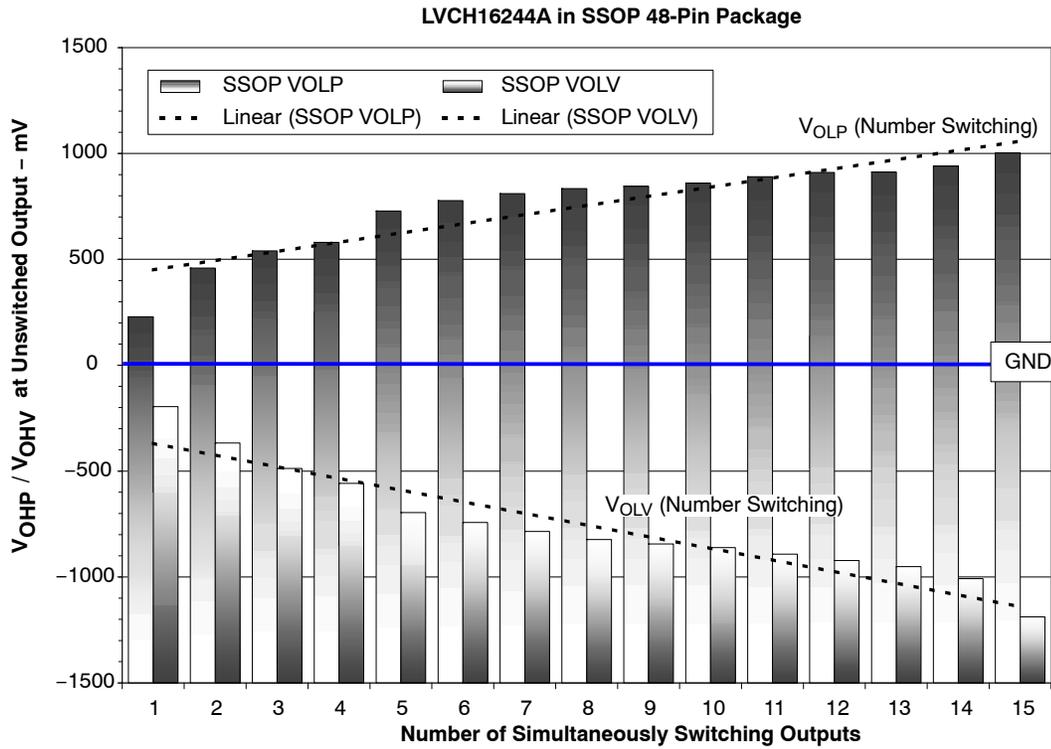


Figure 13. Measured Simultaneous-Switching High Bounce, TVSOP 48-Pin Package

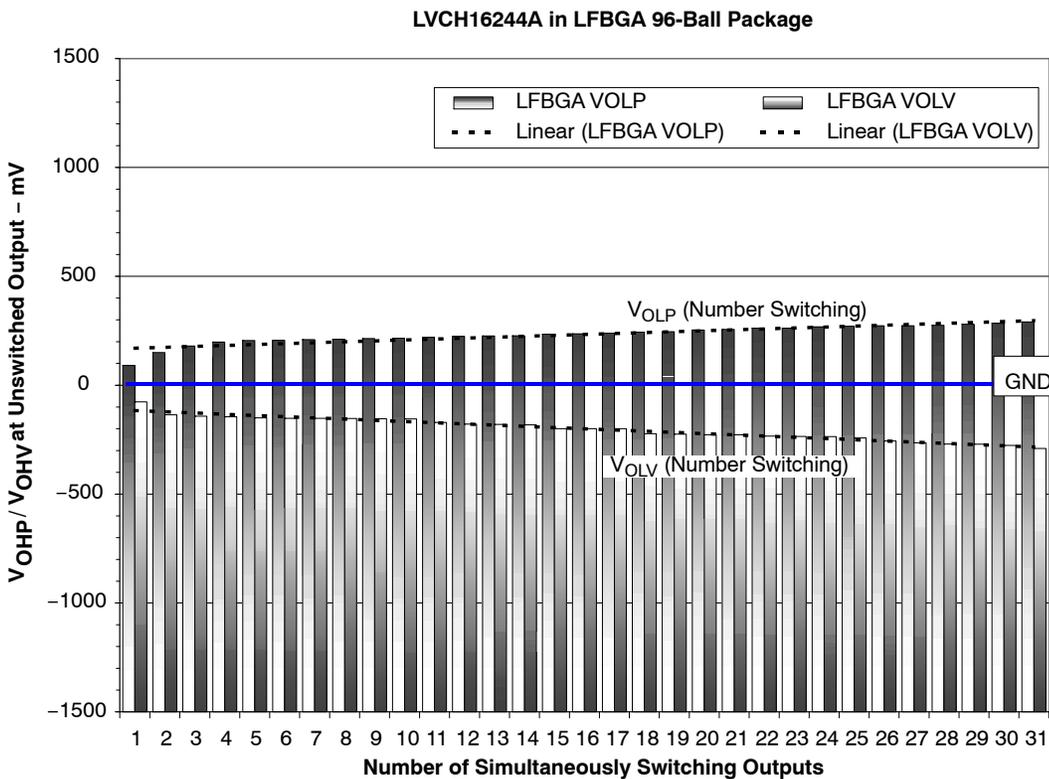
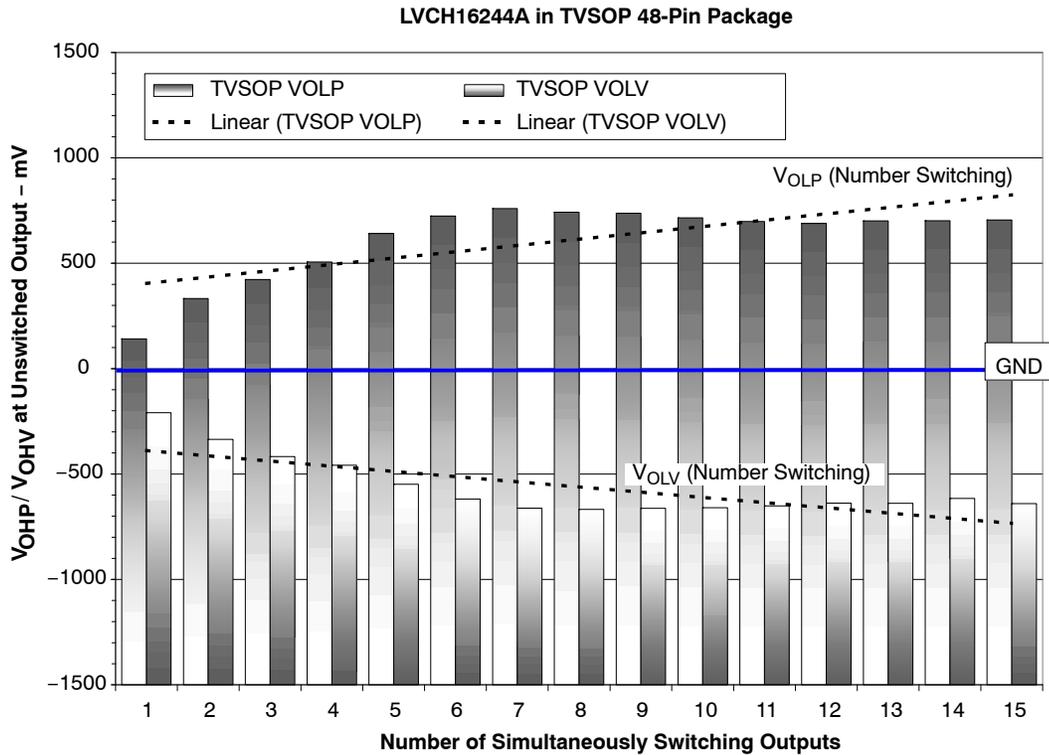


**Figure 14. Measured Simultaneous-Switching High Bounce, LFBGA 96 Ball**

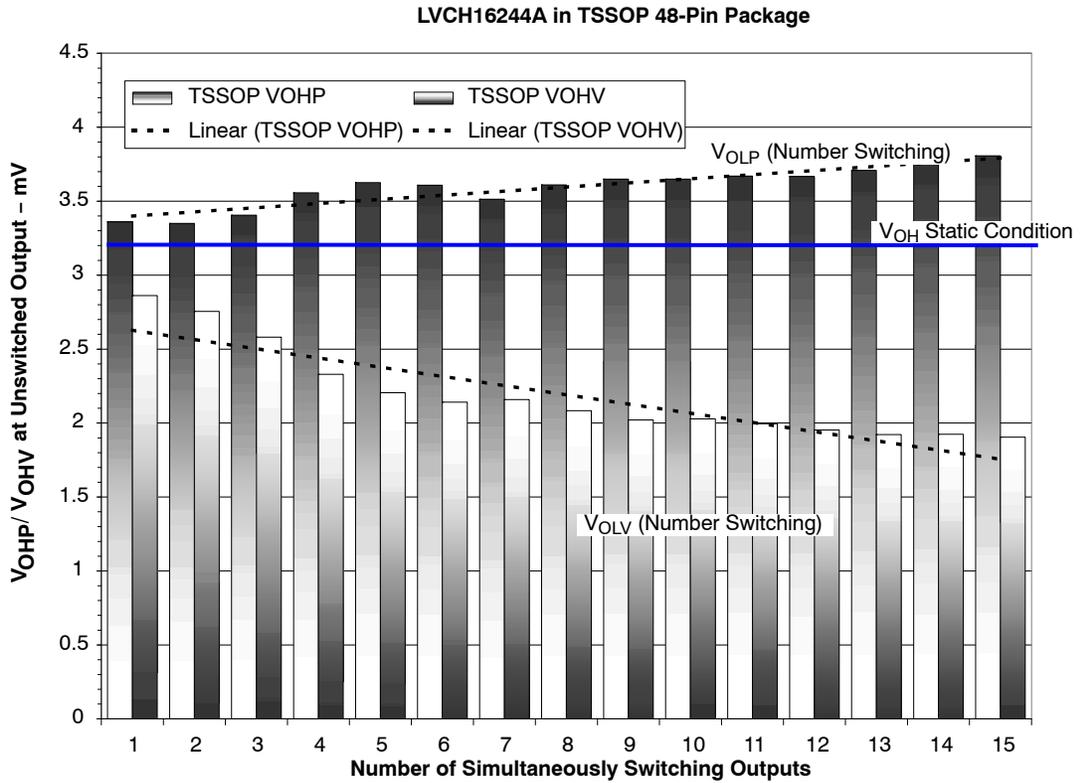
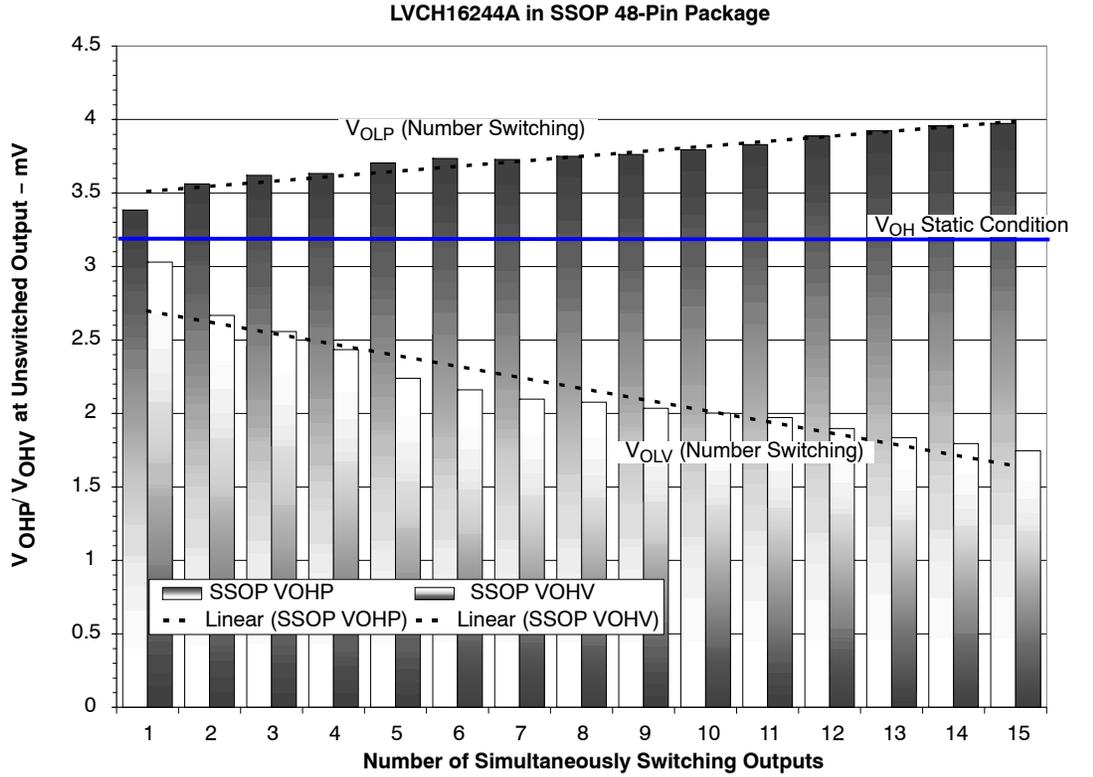
The results shown in Figures 7 through 14 examine only the case in which all outputs but one are connected. It is also of interest to know the relationship between the number of simultaneously switching outputs and the level of interference. These results are shown in Figures 15 through 18. The dotted lines show the linearized increase in the ground/high bounce relative to the number of connected outputs.



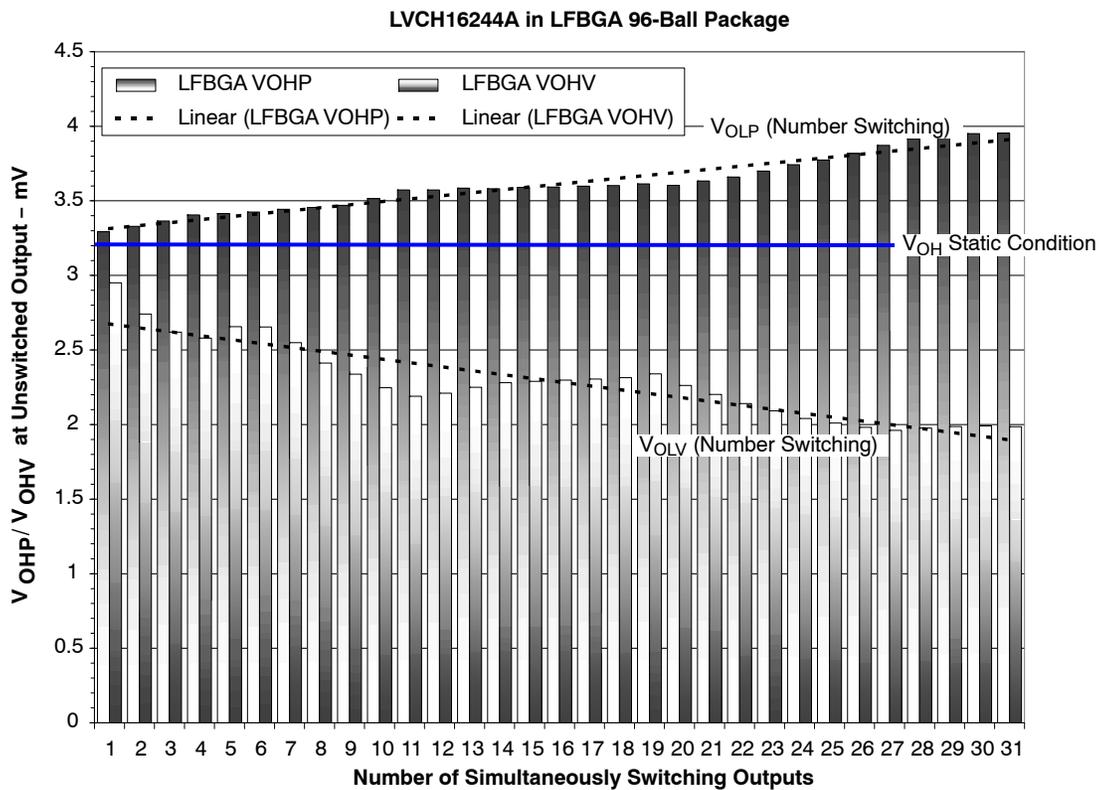
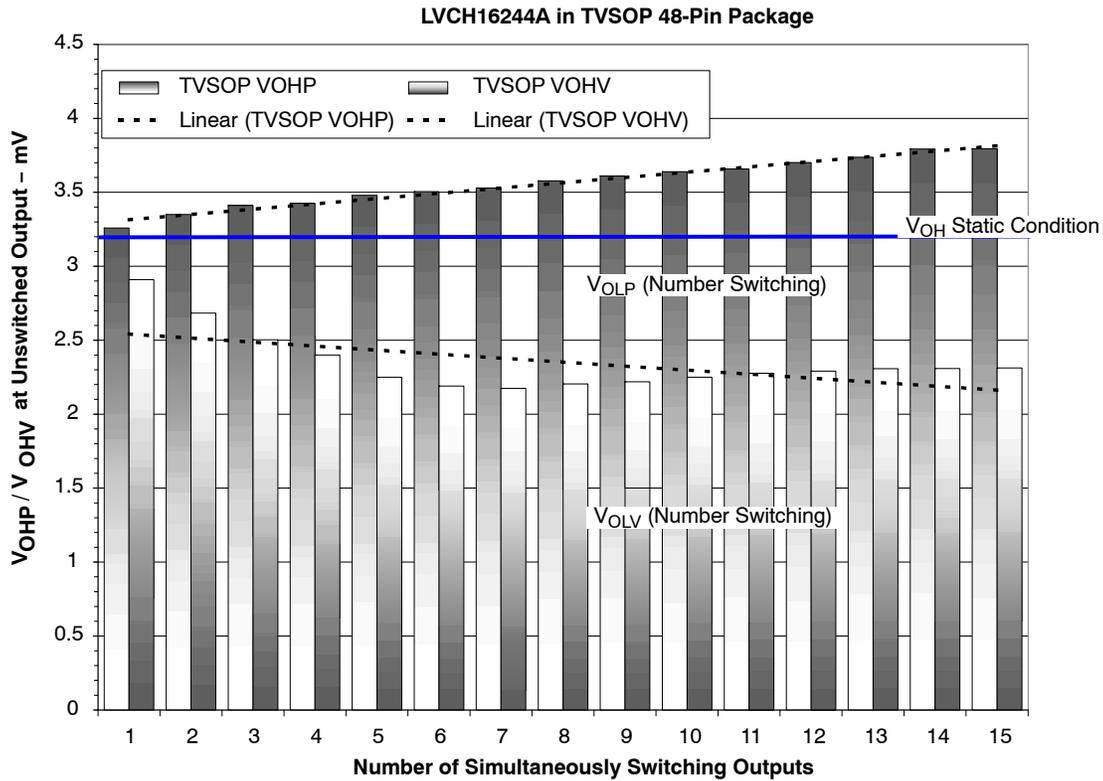
**Figure 15. Simultaneous-Switching Ground Bounce, SSOP 48 Pin (top), TSSOP 48 Pin (bottom)**



**Figure 16. Simultaneous-Switching Ground Bounce, TVSOP 48 Pin (top), LFBGA 96 Ball (bottom)**



**Figure 17. Simultaneous-Switching Ground Bounce, SSOP 48 Pin (top), TSSOP 48 Pin (bottom)**



**Figure 18. Simultaneous-Switching High Bounce, TVSOP 48-Pin (top), LFBGA 96 Ball (bottom)**

The ground- and high-bounce interference voltages produced by simultaneous switching must not exceed the threshold voltage range for the subsequent input stage (1.4 V to 1.5 V). All the package types investigated meet this requirement for the investigated logic functions SN74LVCH16244A and SN74LVCH32244A. Although the components in the SSOP and TSSOP packages slightly exceed the input voltage threshold for the relevant logic states, switching of the subsequent stage is not expected because the typical threshold voltage of 1.5 V is not reached under any circumstances.

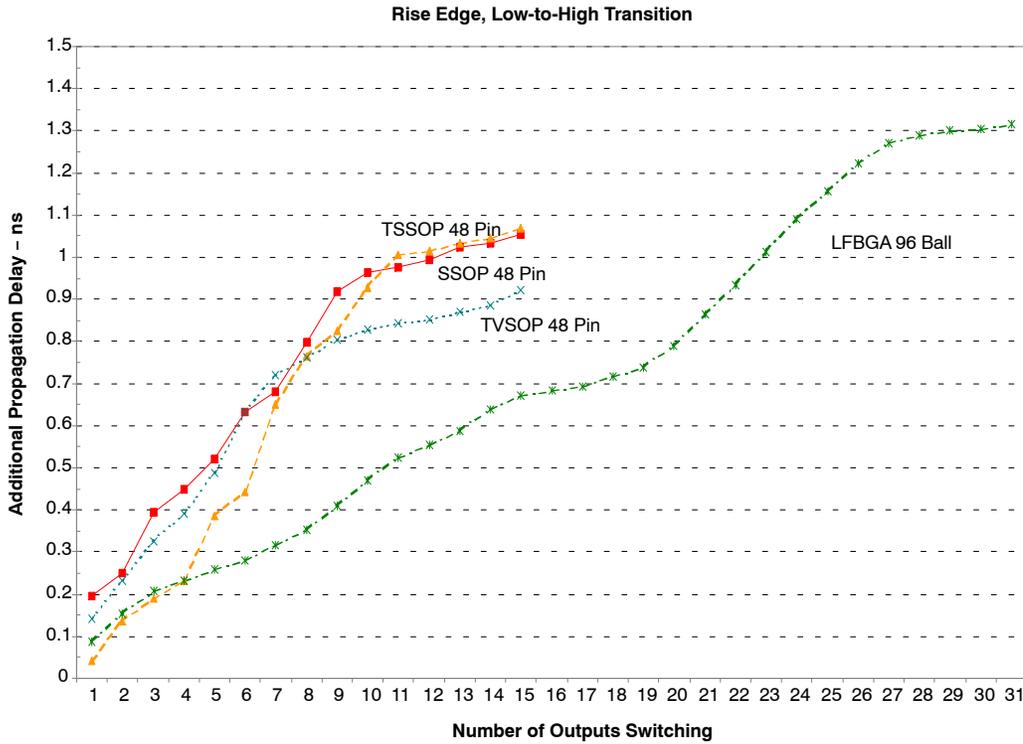
The best result obtained in this investigation was for the ball grid array package. The positive effect of the favorable ball arrangement with additional GND balls is evident.

A small part of the differences measured could be due to component spread rather than being exclusively the result of the package being measured.

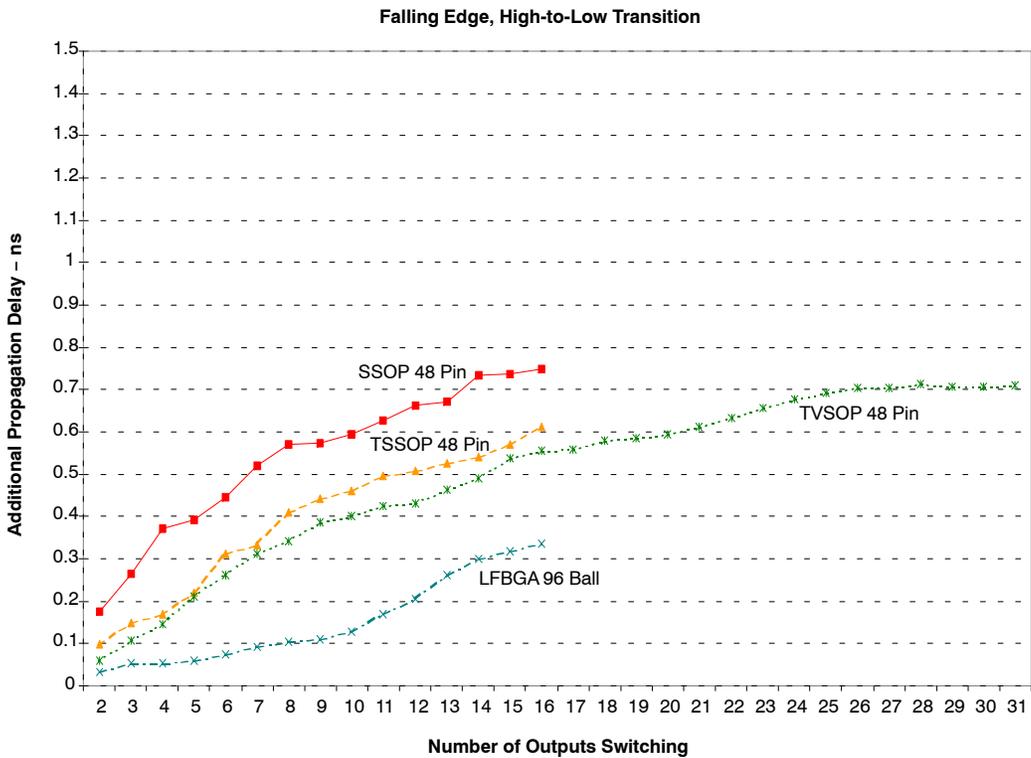
The process technology involved also has a decisive effect on the interference level. However, the results here give an idea of the general tendencies that apply to other logic families as well.

### **Increase in Propagation Delay Time**

The package type also influences the increase in propagation delay that occurs when several outputs switch simultaneously. The inductance of the supply and ground leads is the decisive factor. To measure this behavior for various packages, the relation between propagation delay and the number of outputs switching was measured. (see Figures 19 and 20). In all cases, the devices measured were from the LVC family operated at a supply voltage of 3.3 V and whose outputs were, in accordance with the data sheet, loaded with 30 pF and 500  $\Omega$ : SN74LVCH16244A for the Widebus package and SN74LVCH32244A for the LFBGA 96-pin package.



**Figure 19. Rising-Edge Propagation Delay Time Relative to the Number of Simultaneously Switching Outputs for the SSOP, TSSOP, TVSOP, and LFBGA Packages**



**Figure 20. Falling-Edge Propagation Delay Time Relative to the Number of Simultaneously Switching Outputs for the SSOP, TSSOP, TVSOP, and LFBGA Packages**

In Figures 19 and 20, the Y-axis shows the increase in propagation delay time and the X-axis shows the number of outputs switching. The representation of the increase in propagation delay time was selected in order to eliminate fluctuations in absolute switching speed that occur as a result of variations in component tolerances. Because the absolute increase in propagation delay time for the rising edges is 0.3 ns to 0.8 ns (for the falling edge, 0.9 ns to 1.3 ns), the measurements are at the upper limits of achievable measurement accuracy, the given measurement setup, and the measuring instruments used. This is the reason for the nonlinearities of the data curves.

The SSOP package produced the worst results for all tests, while the TVSOP 48-pin gave the best values for a Widebus package.

Again, the LFBGA package performed well.

## Thermal Properties

When developing a digital system, the thermal behavior of the package must be taken into account.

The small size of surface-mounted devices means that the dissipation of the heat arising from power loss becomes increasingly critical as components become smaller.

The thermal resistance of packages relative to airflow is given in Table 6. The maximum power consumption curves in relation to the ambient temperature for the package types investigated in this report are given in Figures 21 through 24.

**Table 6. Comparison of the Thermal Resistance ( $R_{\theta JA}$ ) of Different Packages**

Package	Thermal Resistance at Various Airflows			
	0 m/s	0.83 m/s	1.38 m/s	2.78 m/s
SSOP 48 pin	93.5	69.9	63.8	57.1
TSSOP 48 pin	89.1	78.5	75.1	69.4
TVSOP 48 pin	92.9	80.9	77.1	71
LFBGA 96 ball	40	37.5	37	35.7

In equation 3, the chip temperature is derived from the thermal resistance, the component's overall power loss, and the ambient temperature.

$$T_J = R_{QJA} \times P_{TOT} + T_A \quad (3)$$

Where:

- $T_J$  = chip temperature (J = junction)
- $R_{QJA}$  = thermal resistance of the chip (junction) at the ambient air temperature
- $P_{TOT}$  = component's overall power loss
- $T_A$  = ambient temperature

The total power consumption ( $P_{TOT}$ ) of a circuit is determined mainly by:

- Circuit standby power consumption ( $P_{Stat}$ )
- Power consumption ( $P_S$ ) caused by the current spike that occurs when switching an output
- Power consumption ( $P_L$ ) necessary for the transition from one logic state to the other of the capacitive load connected at the output.

The equation for calculating  $P_{TOT}$  is:

$$P_{TOT} = P_{Stat} + P_S + P_L \quad (4)$$

Where:

- $P_{Stat}$  = static power consumption
- $P_S$  = dynamic power consumption caused by current spikes
- $P_L$  = dynamic power consumption caused by capacitance load

The static share ( $P_{Stat}$ ) of the power consumption, which is caused by the component itself, can be calculated from the parameters  $I_{CCL}$ ,  $I_{CCH}$ , and  $I_{CCZ}$ , given in the specification sheet, the supply voltage, and the relationship of active high, low, and high impedance. Equation 6 gives the amount of static power consumption. However, this power consumption does not depend on the number of switched outputs, but on the share of the signal.

The dynamic share of the power consumption depends on the factor's line impedance and length; the output load of the input and output rates; the duty cycle from active high, low, and high impedance; and the amplitude and duration of current peaks at the moment of switching. The definition of share is given in equation 5:

$$\text{share}_{\text{high}(\text{low}; Z)} = \frac{T_{\text{high}(\text{low}; Z)}}{T_{\text{high}} + T_{\text{low}} + T_Z} \quad (5)$$

Where:

$T_{\text{high,low,Z}}$  = average amount of time within a signal period

$$P_{Stat} = \sum_{k=1}^n \frac{V_{CC}(\text{share}(k)_{\text{high}} \times I_{CCH} + \text{share}_{\text{low}}(k) \times I_{CCL} + \text{share}_Z(k) \times I_{CCZ})}{n} \quad (6)$$

Where:

$V_{CC}$  = supply voltage

$I_{CCL}$ ,  $\text{share}_{\text{low}}(k)$  = current consumption for static low at output, average percentage share of the  $k^{\text{th}}$  output

$I_{CCH}$ ,  $\text{share}_{\text{high}}(k)$  = current consumption for static high at output, average percentage share of the  $k^{\text{th}}$  output

$I_{CCZ}$ ,  $\text{share}_Z(k)$  = current consumption for high-impedance state at output, average percentage share of the  $k^{\text{th}}$  output

$k$  = number of the switched output of the circuit

$n$  = number of inputs in the circuit

The power consumption caused by the current spikes can be calculated using equation 7:

$$P_S = \sum_{k=1}^n V_{CC} \times I_s \times t_s \times f \times k \quad (7)$$

Where:

$I_s$  = amplitude of current spikes

$t_s$  = duration of current spikes

$f$  = clock rate (repetition rate)

$k$  = number of the switched outputs of the circuit

$n$  = number of switched outputs

The technology involved is a major factor in the amplitude of current spikes. With bipolar output stages, the amplitude of current spikes is less. They are more clearly revealed by the rising signal edges.

Power consumption ( $P_L$ ) is caused by external loads at the outputs of the circuit. This power is taken up by the circuit for the transition from one logic state to the other, and can be calculated by equation 8:

$$P_L = \sum_{k=1}^n V_{CC} \frac{V_{swing} \times C_L(k) \times f(k)}{2} \quad (8)$$

Where:

- $C_L(k)$  = capacitive load connected to the  $k^{\text{th}}$  output
- $V_{swing}$  = signal swing  $V_{OH} - V_{OL}$
- $f(k)$  = frequency applied to the  $k^{\text{th}}$  input

In addition to the power consumption shares mentioned above, additional power consumption can result from bus conflicts. A bus conflict occurs when two drivers on a line simultaneously create different logic levels. This problem can be avoided when designing a circuit by using proper timing arrangements.

Power consumption and chip temperature can be calculated, using the LVTH16244A as an example.

The SN74LVTH16244A 16-bit driver, with  $V_{CC} = 3.6$  V, runs at a clock speed of 33 MHz. All of the outputs are switched. The symmetrical driver output load in the static case is 1 M $\Omega$ . The overall capacitive load totals 90 pF per output. On average, each output delivers logical high, low, and high-impedance one-third of the time. The current spikes at the moment of switching reach values of 20 mA in the LVT family. The duration of the current spike is 5 ns, and there are no bus conflicts.

Because the assigned load conditions and frequency are the same for all inputs and outputs, equations 5 through 8 are simplified. The summation and the control variables  $n$  and  $k$  are eliminated from equation 6. The factor 16 is added in equations 7 and 8 to reflect 16 inputs and outputs.

On the basis of the data-sheet values for the supply current ( $I_{CC}$ ) in the high, low, and high-impedance state, for the component SN74LVTH16244A:

- $I_{CCH/Z} = 190$   $\mu$ A (for  $V_{CC} = 3.6$  V,  $I_O = 0$ ,  $V_I = V_{CC}$  or GND, outputs high or high impedance)
- $I_{CCL} = 5$  mA (for  $V_{CC} = 3.6$  V,  $I_O = 0$ ,  $V_I = V_{CC}$  or GND, outputs low)

$P_{Stat}$  is derived for one-third low, one-third high, and one-third high impedance of the driver as follows:

$$P_{Stat} = 3.6 \text{ V} \times \left( \frac{5 \text{ mA}}{3} + \frac{0.19 \text{ mA}}{3} + \frac{0.19 \text{ mA}}{3} \right) = 6.46 \text{ mW} \quad (9)$$

These values also give the dynamic share in accordance with equations 7 and 8, and result in equation 10.

$$P_{dyn} = 16 \times (P_s + P_L) \quad (10)$$

With the given values, equation 10 results in

$$P_{\text{dyn}} = 16 \times \left( 3.6 \text{ V} \times 20 \text{ mA} \times 5 \text{ ns} \times 33 \text{ MHz} + 3.6 \text{ V} \frac{3.6 \text{ V} \times 90 \text{ pF} \times 33 \text{ MHz}}{2} \right) \quad (11)$$

$$= 0.19 \text{ W} + 0.308 \text{ W} = 0.498 \text{ W}$$

The overall result in this case is:

$$P_{\text{TOT}} = 6.46 \text{ mW} + 0.498 \text{ W} = \sim 0.5 \text{ W} \quad (12)$$

The temperature on the silicon can be determined from the thermal resistance ( $R_{\text{QJA}}$ ) of the package, and the ambient temperature, with the aid of equation 3.  $R_{\text{QJA}}$  corresponds to the capacity to dissipate heat to the ambient environment. Four package options are available:

SSOP:  $R_{\text{QJA}} = 89^\circ\text{C/W}$

TSSOP:  $R_{\text{QJA}} = 93^\circ\text{C/W}$

TVSOP:  $R_{\text{QJA}} = 94^\circ\text{C/W}$

LFBGA:  $R_{\text{QJA}} = 40^\circ\text{C/W}$

The thermal resistance given in each case is without any additional cooling measures. For the packages investigated, the following chip temperatures ( $T_{\text{J}}$ ) are derived at an ambient temperature of  $25^\circ\text{C}$ , and without additional cooling:

SSOP package:  $T_{\text{J}} = 89^\circ\text{C/W} \times 0.5 \text{ W} + 25^\circ\text{C} = 69.5^\circ\text{C}$

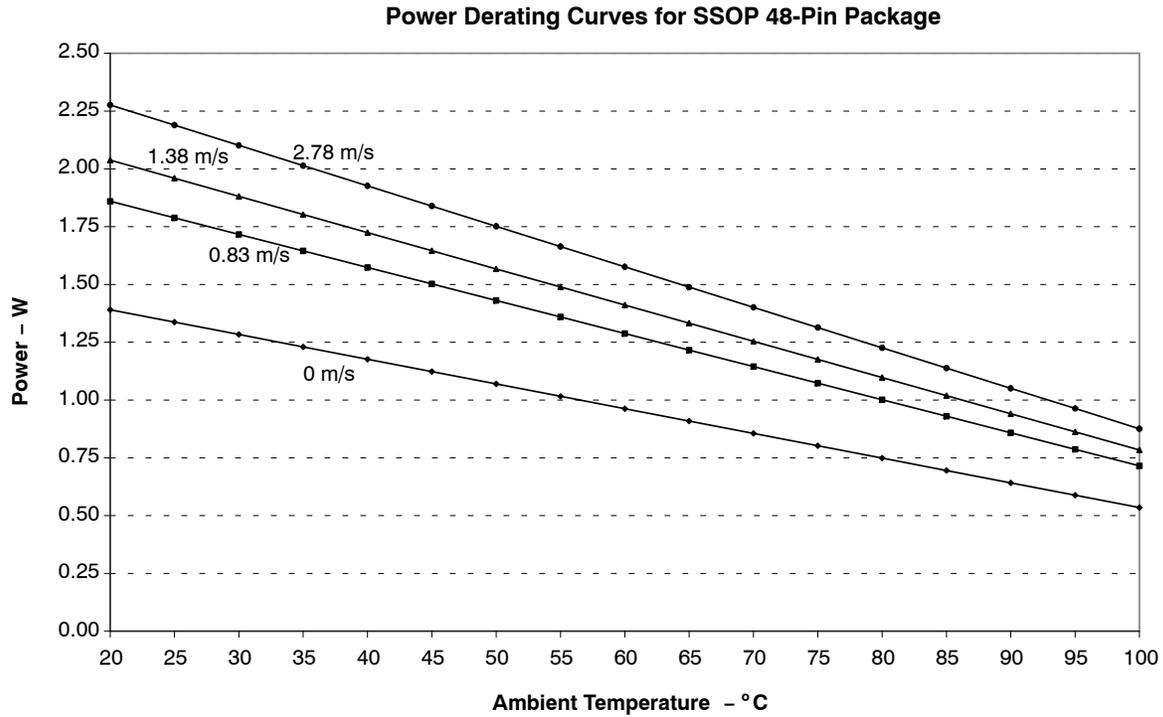
TSSOP package:  $T_{\text{J}} = 93^\circ\text{C/W} \times 0.5 \text{ W} + 25^\circ\text{C} = 71.5^\circ\text{C}$

TVSOP package:  $T_{\text{J}} = 94^\circ\text{C/W} \times 0.5 \text{ W} + 25^\circ\text{C} = 72.0^\circ\text{C}$

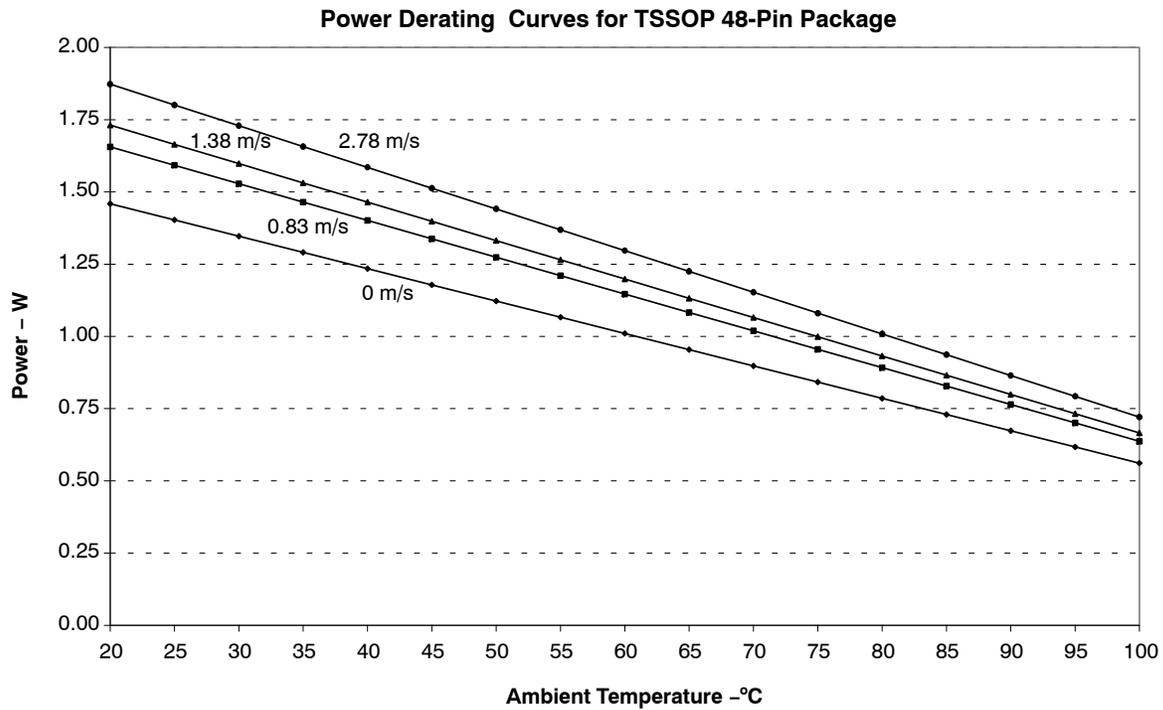
LFBGA 96 package:  $T_{\text{J}} = 40^\circ\text{C/W} \times 0.5 \text{ W} + 25^\circ\text{C} = 45.0^\circ\text{C}$

If the temperature rises further as a result of greater output loads, leading to chip temperatures in excess of  $150^\circ\text{C}$ , additional cooling devices or fans must be used to dissipate the excess heat.

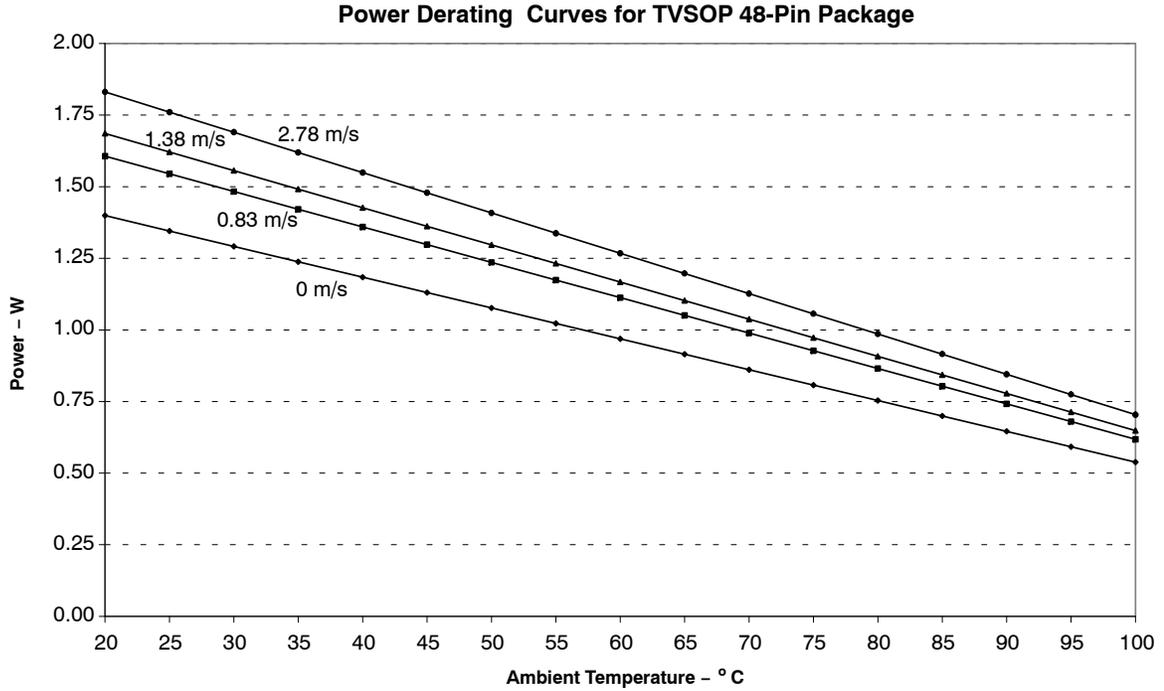
Figures 21 through 24 show the characteristic curves for power consumption relative to ambient temperature. In all cases, an upper limit value for the chip temperature of  $150^\circ\text{C}$  is assumed. Airflow ranges from 0 m/s to 2.78 m/s. An airflow of 0 m/s relates to an application using no additional cooling measures, while 2.78 m/s is for a system application using a cooling fan.



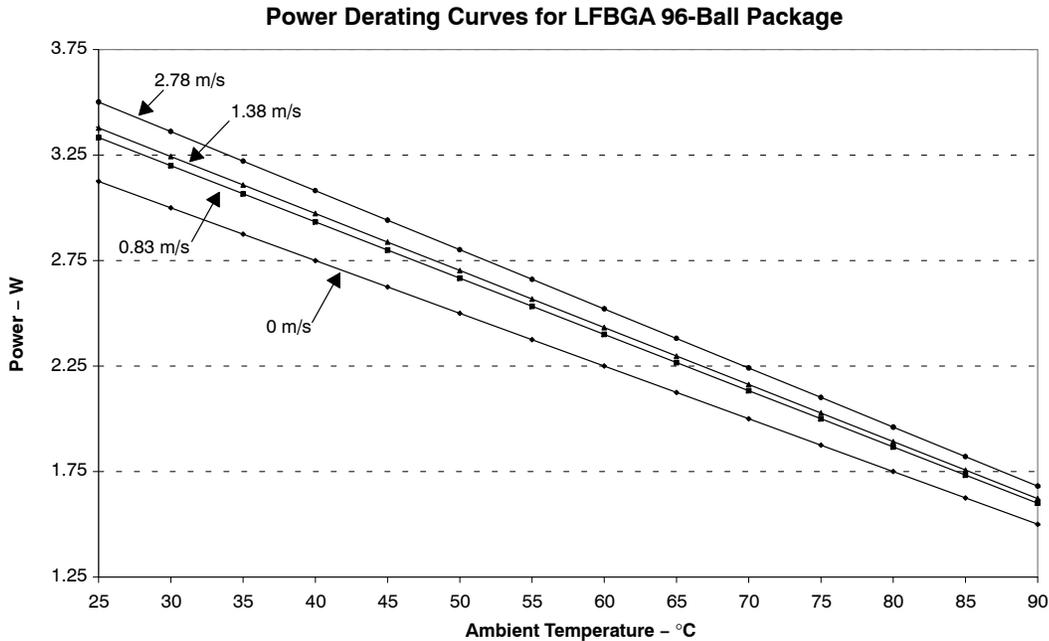
**Figure 21. Maximum Power Consumption Relative to Ambient Temperature,  $T_J = 150^\circ\text{C}$ , SSOP 48-Pin Package**



**Figure 22. Maximum Power Consumption Relative to Ambient Temperature,  $T_J = 150^\circ\text{C}$ , TSSOP 48-Pin Package**



**Figure 23. Maximum Power Consumption Relative to Ambient Temperature,  $T_J = 150^\circ\text{C}$ , TVSOP 48-Pin Package**



**Figure 24. Maximum Power Consumption Relative to Ambient Temperature,  $T_J = 150^\circ\text{C}$ , LFBGA 96 Ball**

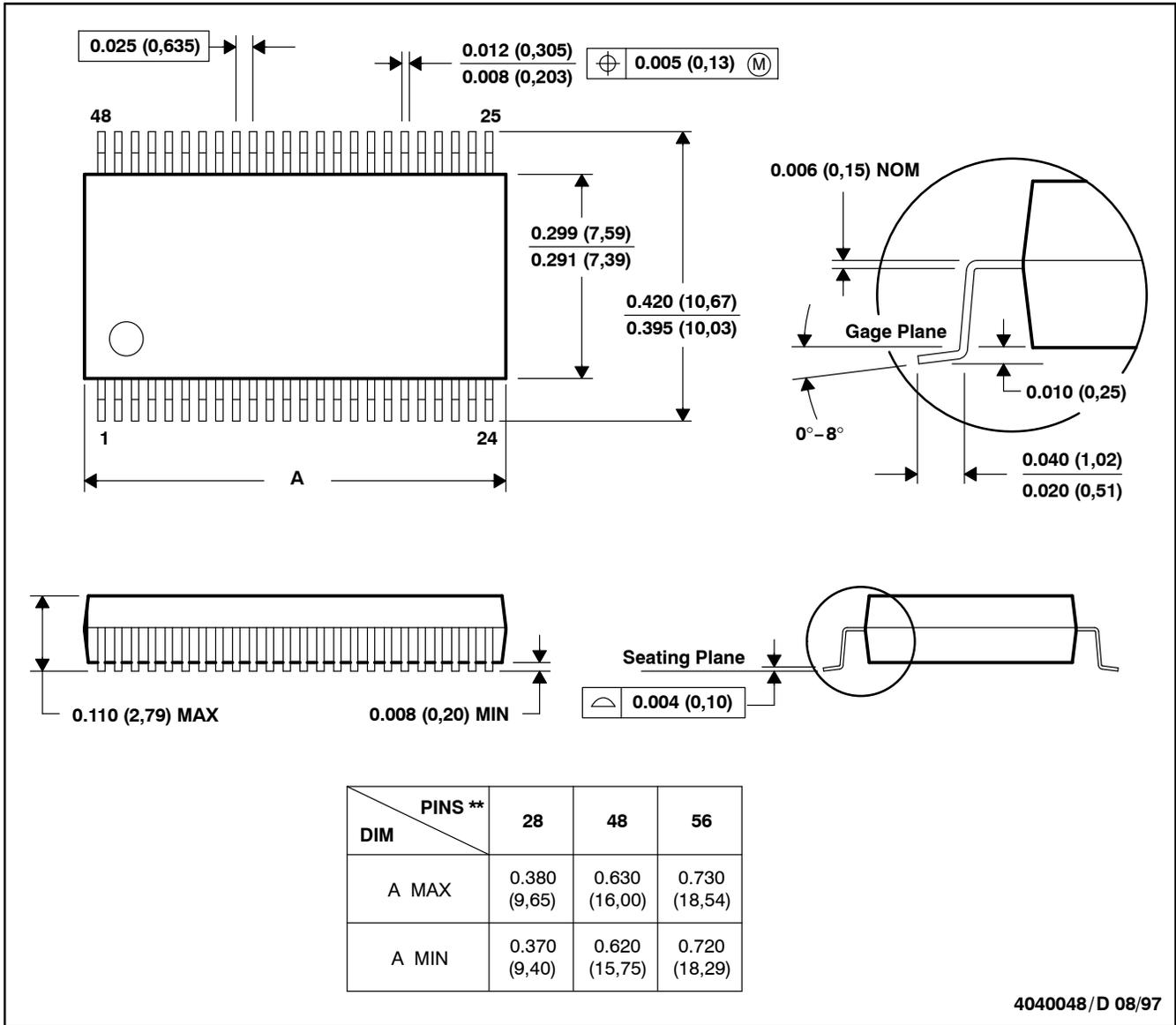
Although the LFBGA 96-pin package is the smallest, in this comparison it showed the lowest heat resistance. Table 6 shows that the LFBGA 96-pin package dissipates heat more effectively by a factor of more than two, compared to any of the other packages investigated. This leads to the added advantage that many systems do not require additional cooling provisions.

# Package Dimensions and Size Comparison

Dimensions of the packages discussed in this report are provided in Figures 25 through 28.

**DL (R-PDSO-G\*\*)**  
48 PINS SHOWN

**PLASTIC SMALL-OUTLINE PACKAGE**



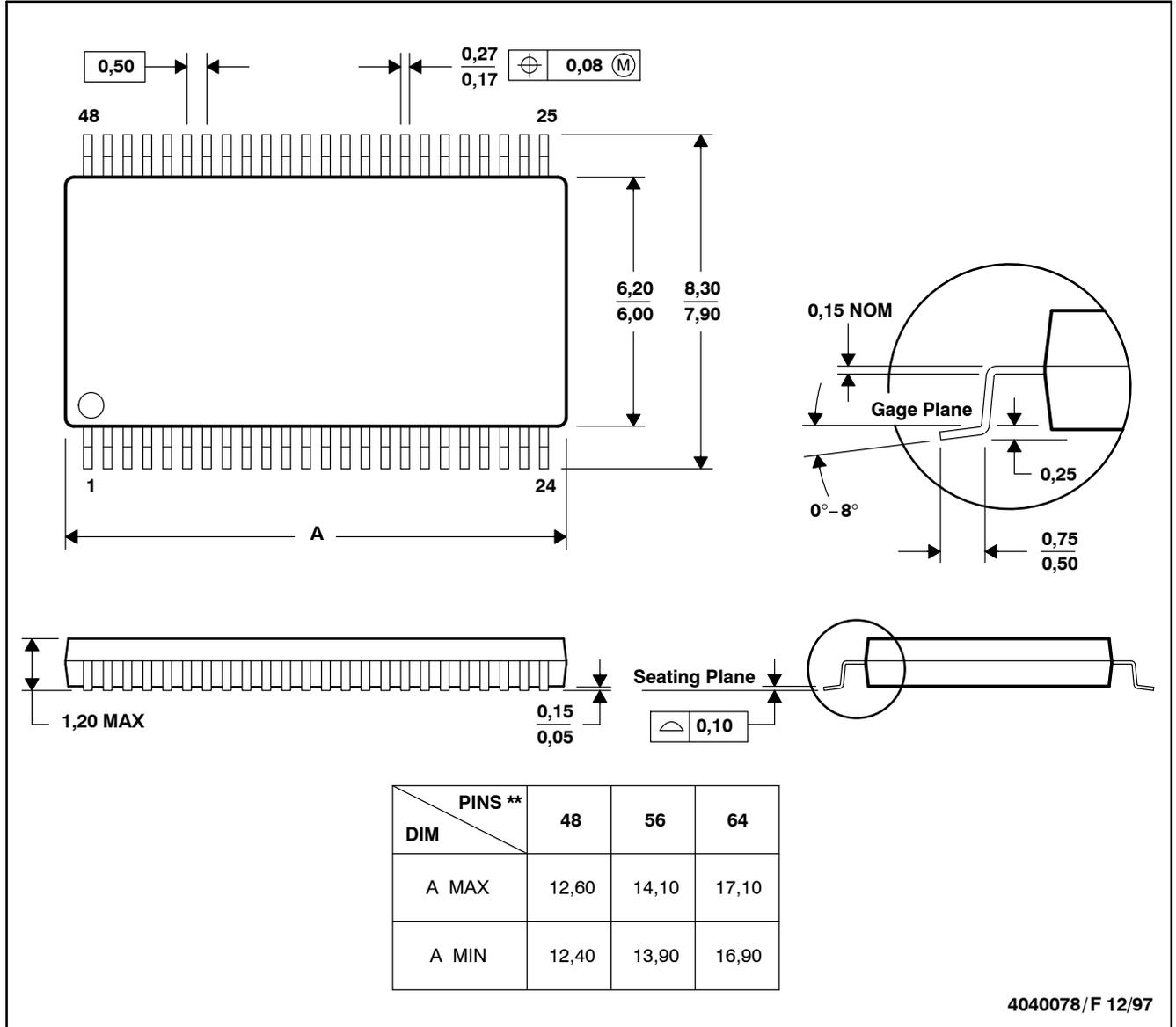
- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118

**Figure 25. Dimensions of the SSOP 28-, 48-, and 56-Pin Packages**

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



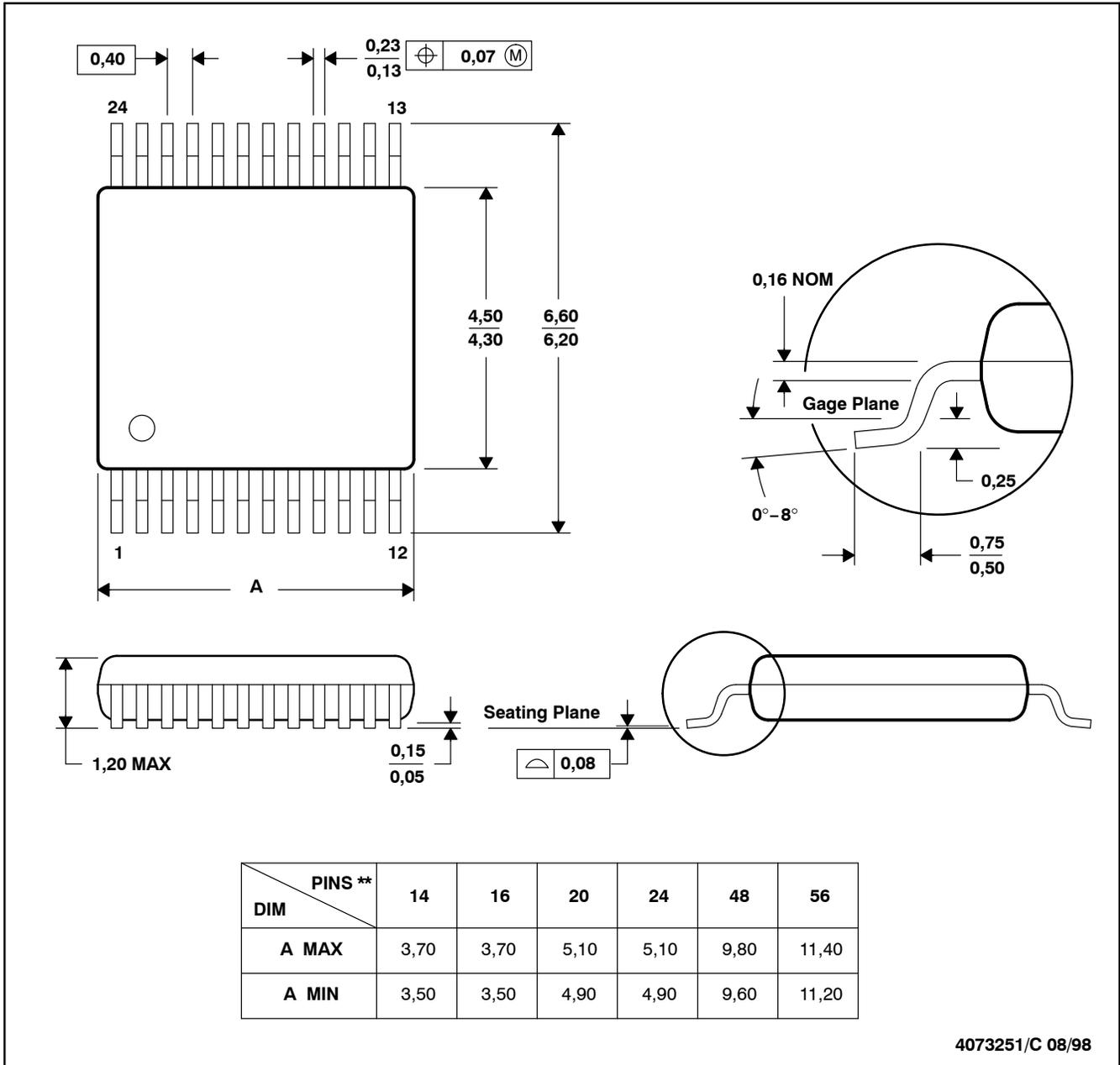
- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

Figure 26. Dimensions of the TSSOP 48-, 56-, and 64-Pin Packages

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

24 PINS SHOWN

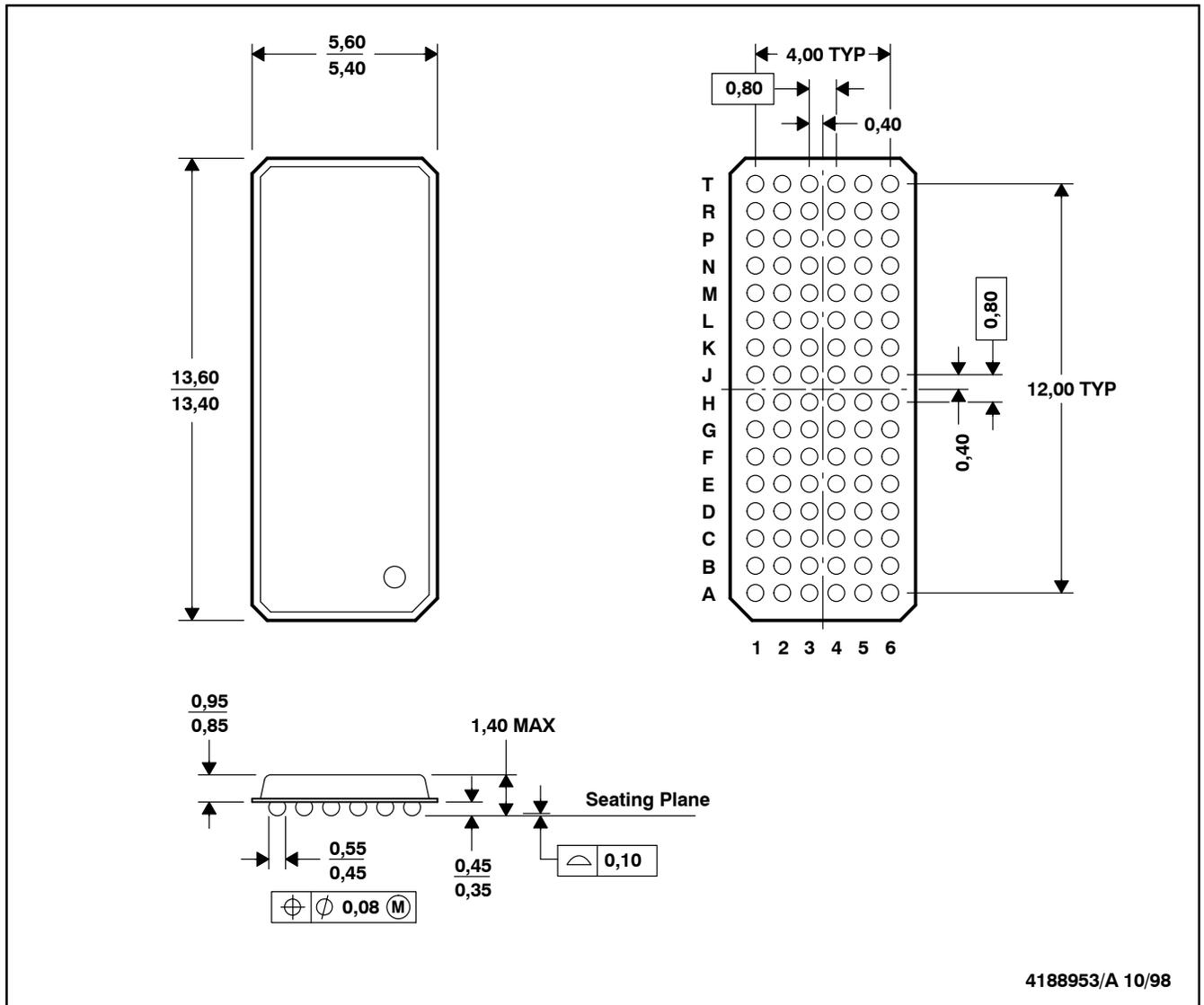


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

Figure 27. Dimensions of the TVSOP 48-, 56-, and 64-Pin Packages

GKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. MicroStar BGA™ configuration

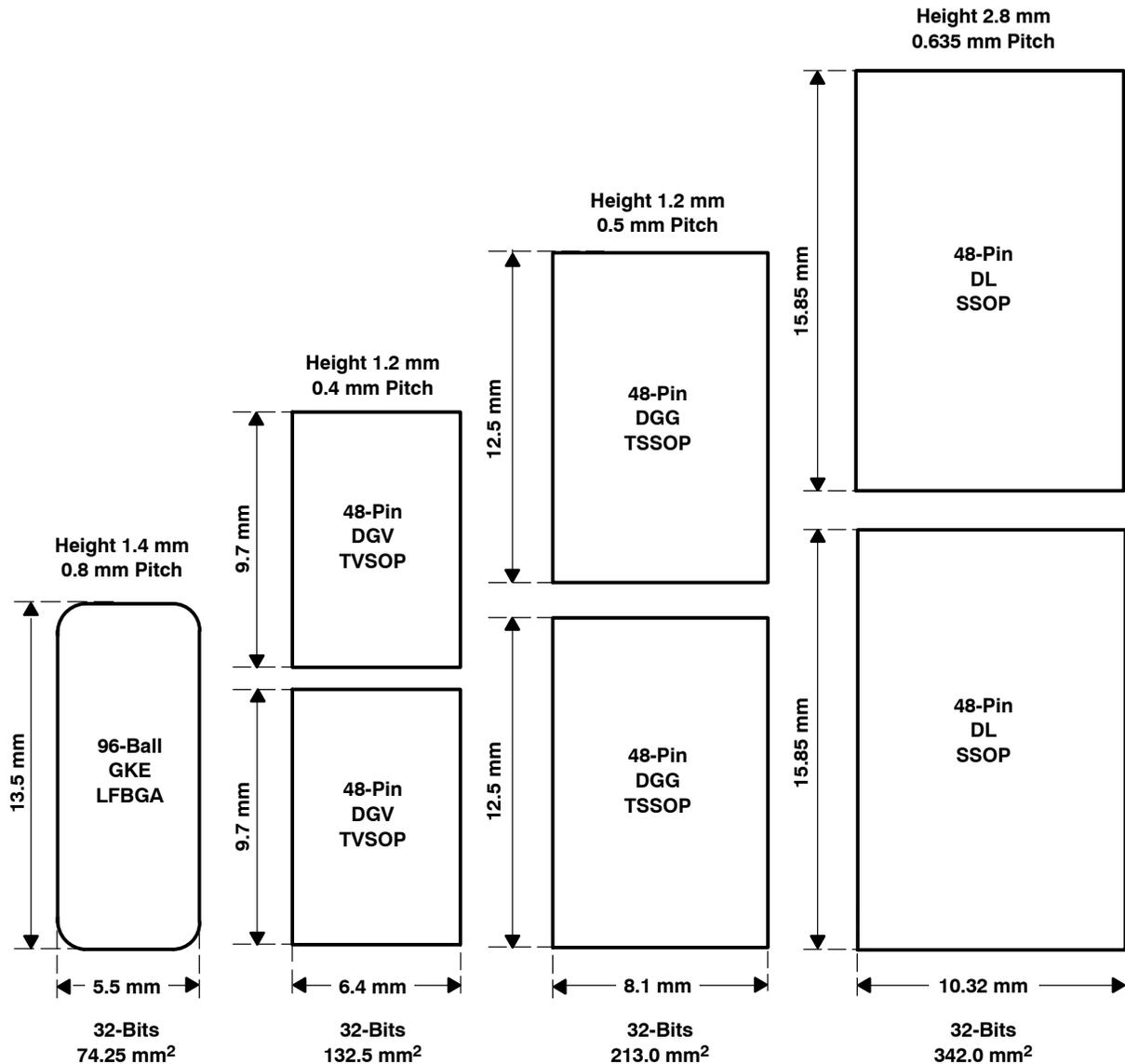
Figure 28. Dimensions of the LFBGA 96-Ball Package

MicroStar BGA is a trademark of Texas Instruments Incorporated.

Figure 29 shows the amount of space needed for a 32-bit interface using the package types discussed in this report. The LFBGA 96-ball package requires the least amount of space.

Creating the interface using two SSOP packages requires 4.5 times as much space.

The low-profile, fine-pitch, 96-ball grid array package requires 2.32 mm<sup>2</sup> per bit, while the TVSOP package requires almost twice as much space at 4.14 mm<sup>2</sup> per bit. The space required using the TSSOP package is 6.65 mm<sup>2</sup> per bit, and for the SSOP package the space is 10.69 mm<sup>2</sup> per bit.



**Figure 29. Space Needed for a 32-Bit Interface Using Various Packages Options**

## Summary

The trend toward 32-bit, or wider, bus systems reflects the need to increase the data rate in modern computer systems, and there is a corresponding demand for bus drivers supporting wider data formats.

To meet these requirements, TI has introduced the Widebus devices and low-profile fine-pitch ball grid array package.

Optimizing the voltage supply via staggered pinning for the Widebus packages ensures extremely low interference voltages, even during simultaneous switching of several outputs (simultaneous-switching interference). Additionally, Widebus packages allow the very high speeds that can be achieved with modern semiconductor technology to be fully exploited at the system level as well.

The TVSOP package is the smallest Widebus package. It gives the best results among the Widebus dual in-line packages for the ground-bounce and simultaneous-switching parameters of several outputs. The additional delay caused by simultaneously switching outputs also was the smallest with this package. However, the TVSOP package currently is still relatively difficult to process due to its very small pin-to-pin spacing of 0.4 mm.

The LFBGA package features another improvement: terminals are in the form of balls, leading to a further reduction in parasitic inductance.

In addition to the circuit-board space advantages it affords, the LFBGA package achieves a marked improvement in signal quality for all measurements as a result of its low package parasitics and, particularly, its minimal inductance.

The LFBGA package also demonstrates good heat resistance. A  $\theta_{JA}$  of 40°C/W represents at least twice the heat dissipation efficiency of any of the other Widebus packages investigated for this report.

## Acknowledgment

The author of this application report is Johannes Huchzermeier.

## Glossary

AC	Advanced CMOS
ABT	Advanced BiCMOS Technology
AHC	Advanced High-Speed CMOS
ALVC	Advanced Low-Voltage CMOS
ALVT	Advanced Low-Voltage Technology
ALS	Advanced Low-Power Schottky
AS	Advanced Schottky
AVC	Advanced Very-Low-Voltage CMOS
Auto3-state	Devices with Auto3-state tolerate a higher voltage level at the outputs during active-high state at the output. (also called overvoltage protection)
BCT	BiCMOS technology
BiCMOS	Combination of the bipolar and CMOS manufacturing processes, with CMOS input structure and bipolar output structure
Bonding wire	Wire connecting the chip and the pin
Bus hold	An input circuit that holds the last valid state before the onset of the undefined state on the bus until a new valid logic state ensues
Coupling factor	Reciprocal inductive coupling between two neighboring pins on the basis of the transformer equation
GND	Ground (UK = Earth)
HC	High-speed CMOS
I/O	Input/Output
Leadframe	Metal mask to which the chip is attached, with the pins leading outward.
LFBGA	Low-profile fine-pitch ball grid array
LS	Low-Power Schottky
LVC	Low-Voltage CMOS
LV	Low-Voltage CMOS, originally designed for 3.3-V $V_{CC}$ , but also usable with a 5-V $V_{CC}$

LVT	Low-voltage technology
OEC™ the	Output Edge Control, a procedure patented by Texas Instruments that reduces the output-signal slew rate.
R <sub>Load</sub>	Load resistance
S	Schottky
SPICE	Simulation Program with Integrated Circuit Emphasis
SSOP	Shrink Small-Outline Package
TSSOP	Thin Shrink Small-Outline Package
TVSOP	Thin Very Small-Outline Package
TTL	5-V Logic, Transistor-Transistor Logic
V <sub>CC</sub>	Supply voltage

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# ***Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs***

SZZA017A  
September 1999



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## Abstract

In an effort to standardize integrated-circuit (IC) package thermal-measurement methods, JEDEC has released standards for test-board designs. Typical thermal metrics reported are package thermal resistance from junction to ambient ( $\theta_{JA}$ ), and package thermal resistance from junction-to-case ( $\theta_{JC}$ ). Recent data generated by Texas Instruments (TI™) linear and logic package designers includes  $\theta_{JA}$  and  $\theta_{JC}$  measured, or modeled, on both a JEDEC low-thermal-conductivity (low K) PCB design and a JEDEC high-thermal-conductivity (high K) PCB design. A study showed good correlation between modeled results and data taken in a laboratory. A web page provides the new thermal data for TI packages. An additional feature of this web page allows the user to plot derating curves for each package, using the thermal data provided.

## Introduction

Users of ICs need to know the thermal-dissipation performance of the plastic packages used to encapsulate the ICs. Package thermal-resistance data allows the user to compare performance of different IC suppliers, as well as determine the limits of a package in a specific end-use environment. Thermal metrics, such as  $\theta_{JA}$  and  $\theta_{JC}$ , are used to compare thermal performance of plastic IC packages. The thermal conductivity of all materials of the IC package and the test-board influence the thermal-resistance values reported by semiconductor manufacturers. Recent advancements in reporting of thermal data include standardized test-board designs. Prior to development of these standard test-board designs, IC manufacturers used their own PCB designs to generate thermal data; therefore, comparison of package thermal data between suppliers was not meaningful.

## Background

Thermal resistance is the resistance of the package to heat dissipation and is inversely related to the thermal conductivity of the package. The source of heat in a plastic IC package is the chip. All electrical circuits dissipate some power in the form of heat. This heat is conducted through the package into the ambient environment, and, in the process, the temperature of the die ( $T_J$ ) rises above ambient. The thermal conductivity of the silicon chip, die-attach epoxy, copper leadframe, and mold compound all affect the rate at which the heat is dissipated. The geometry of the package and of the printed circuit board (PCB) greatly influence how quickly the heat is transferred to the PCB and away from the chip.

The most commonly used thermal metrics for IC packages are thermal impedance measured, or modeled, from the chip junction to the ambient air surrounding the package ( $\theta_{JA}$ ) and thermal impedance measured, or modeled, from the chip junction to the case ( $\theta_{JC}$ ).

Figure 1 is a thermal representation of a typical IC plastic package, with the silicon chip and the thermal metrics identified.

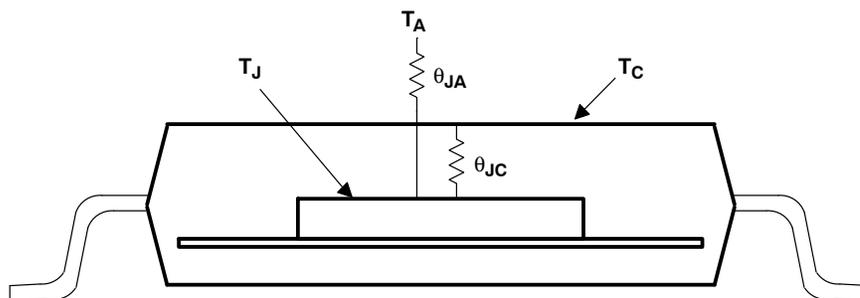


Figure 1. IC Package Thermal Metrics

Mathematically,  $\theta_{JA}$  is defined as:

$$\theta_{JA} = (T_J - T_A)/P \quad (1)$$

Where:

$T_J$  = junction temperature of the chip

$T_A$  = ambient temperature

$P$  = power to the chip

$\theta_{JA}$  is measured using the following steps:<sup>1</sup>

1. IC package containing a test chip is mounted on a test board.
2. Temperature-sensing component of the test chip is calibrated.
3. Package/test-board system is placed in a still-air environment.
4. Known power is dissipated in the test chip.
5. After steady state is reached, the junction temperature is measured.
6. The difference in measured ambient temperature compared to the measured junction temperature is calculated and is divided by the dissipated power.

Mathematically,  $\theta_{JC}$  is defined as:

$$\theta_{JC} = (T_J - T_C)/P \quad (2)$$

Where:

$T_J$  = junction temperature of the chip

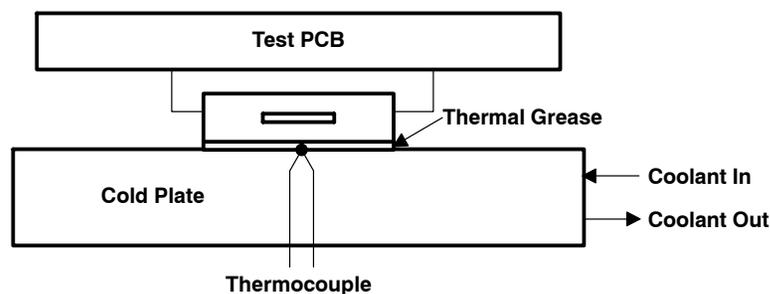
$T_C$  = package case temperature

$P$  = power to the chip

Measurement of  $\theta_{JC}$  is formalized in industry standards. Summarized, the procedure is:

1. IC package containing a test chip is mounted on a test board.
2. The package, in a “dead bug” configuration, is pressure fitted to a copper cold plate (a copper block with circulating constant-temperature fluid).
3. Silicone thermal grease provides thermal coupling between the cold plate and the package.
4. Power is applied to the device.
5. Junction temperature of the test chip is measured.
6. Temperature of the package surface in contact with the cold plate is measured by a thermocouple pressed against this surface.
7.  $\theta_{JC}$  is calculated by dividing the measured temperature difference by the dissipated power.

Figure 2 is a schematic representation of the laboratory method used to measure  $\theta_{JC}$ .



**Figure 2.  $\theta_{JC}$  Laboratory Measurement Method**

$\theta_{JA}$  values are the most subject to interpretation. Factors that can greatly influence the measurement and calculation of  $\theta_{JA}$  are:

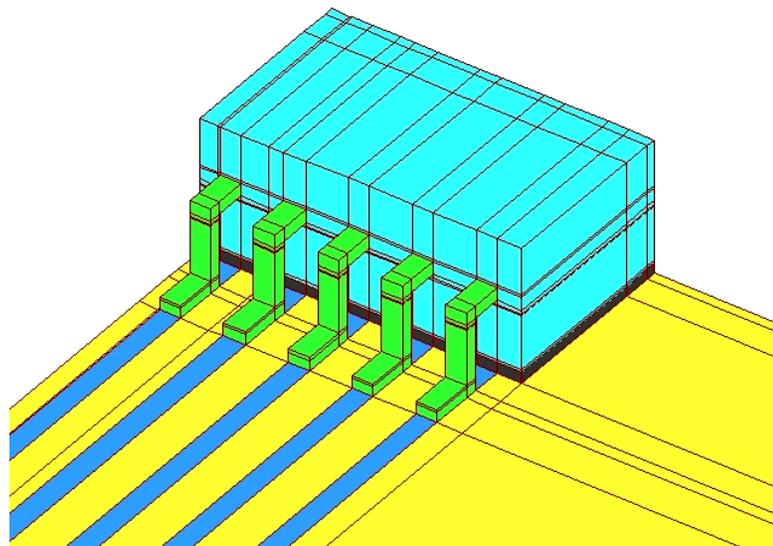
- Whether or not the device is mounted to a PCB
- PCB trace size, composition, thickness, geometry
- Orientation of the device (horizontal or vertical)
- Volume of the ambient air surrounding the device under test, and airflow
- Whether or not other surfaces are in close proximity to the device being tested

To eliminate the test-board design as a variable in data reported by IC manufacturers, thermal test-board design standards have been developed and released.<sup>2,3</sup> In August 1996, the Electronics Industries Association (EIA) released *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*, EIA/JESD 51-3. In February 1999, the EIA released *Test Board With Two Internal Solid Copper Planes for Leaded Surface Mount Packages*, EIA/JESD 51-7. These standards describe guidelines with parameters for thermal-test-board design for low effective thermal conductivity (one signal layer in the trace fanout area) and for PCB designs with high effective thermal conductivity (one power and one ground plane). The specified parameters include the area of the test board, the amount of copper traces on the test board, and the resulting trace fanout area, each important to the heat-sinking characteristics of the PCB. Prior to release of these standards, thermal-impedance data for similar packages varied widely within the industry due to the use of different test-board designs. As the industry adopts this standard design methodology, thermal-impedance variations from test-board design should be minimized. The critical factors of these test-board designs are shown in Table 1.

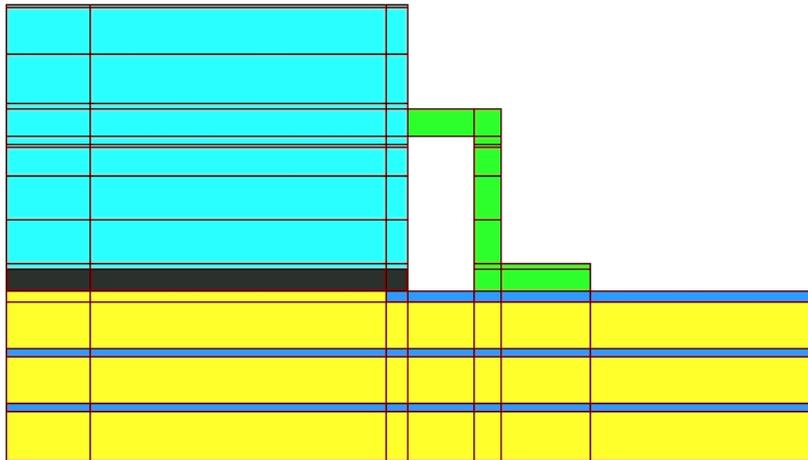
**Table 1. Critical PCB Design Factors for JEDEC 1s and 2s2p Test Boards**

TEST BOARD DESIGN	JEDEC LOW-K 1s (inch)	JEDEC HIGH-K 2s2p (inch)
Trace thickness	0.0028	0.0028
Trace length	0.98	0.98
PCB thickness	0.062	0.062
PCB width	4	4
PCB length	4.5	4.5
Power/ground-plane thickness	No internal copper planes	0.0014 (2 planes)

Figure 3 is an orthogonal view of a one-quarter package model for the 20-pin small-outline integrated-circuit (SOIC) package. Note the traces on the PCB extending out from the leads. Figure 4 is a cross section of the same package on a JEDEC 2s2p (high K) PCB. Note the two internal copper planes embedded in the circuit board and the trace layer on the top surface of the PCB.



**Figure 3. One-Quarter Package Model of 20-Pin SOIC Package**



**Figure 4. Cross Section of 20-Pin SOIC Package on 2s2p PCB**

### Correlation Study

TI uses test boards designed to JESD 51-3 and JESD 51-7 for thermal-impedance measurements. The parameters outlined in these standards also are used to set up thermal models. TI uses the thermal-model program ThermCAL, a finite-difference thermal-modeling tool. Previous data generated using the low-K PCB designs showed the models to be accurate to within 10% of measured data.<sup>4</sup>

Nine TI packages were tested using a JEDEC high-K test-board design and compared to ThermCAL model results for the same packages. Laboratory-measured thermal data and modeled results are shown in Table 2.

**Table 2. Correlation Study Results Using JEDEC High-K PCB Design**

PACKAGE PIN COUNT AND DESIGNATOR	DIE SIZE (mils)	$\theta_{JA}$ ( $^{\circ}\text{C}/\text{W}$ )		DIFFERENCE (%)	$\theta_{JC}$ ( $^{\circ}\text{C}/\text{W}$ )	
		MEASURED	MODELED		MEASURED	MODELED
8 PW	62 × 62	149.4	151.8	1.6	48.7	50.1
16 PW	62 × 62	108.4	99.5	-8.2	36.4	31.1
24 PW	62 × 62	87.9	79.0	-10.1	31.2	26.9
48 DGG	120 × 120	70.0	63.3	-9.6	18.2	16.4
56 DGG	120 × 120	63.8	56.4	-11.6	16.4	14.6
64 DGG	120 × 120	55.4	53.0	-4.3	10.8	12.6
64 PAG	240 × 240	42.3	39.3	-7.1	3.7	5.5
80 PN	240 × 240	44.1	41.9	-5.0	7.6	9.6
100 PZ	240 × 240	40.8	38.1	-6.6	7.8	8.1

This comparison shows modeled  $\theta_{JA}$  data is accurate to within 10% of measured data for most cases when using the ThermCAL software. On average (all nine packages) the difference between measured data and modeled data was 6.9%.

After accuracy of the model results was established, other linear and logic packages were modeled using the JEDEC high-K test board.  $\theta_{JA}$  and  $\theta_{JC}$  data for all packages can be viewed at:

<http://www.ti.com/sc/docs/products/logic/package/thrmdata.htm>

Also included on this web page are copies of the JEDEC standards and related application reports. Within the thermal data page for any specific-package family (SOIC, for example) a derating curve can be viewed. This is an additional feature provided for the user.

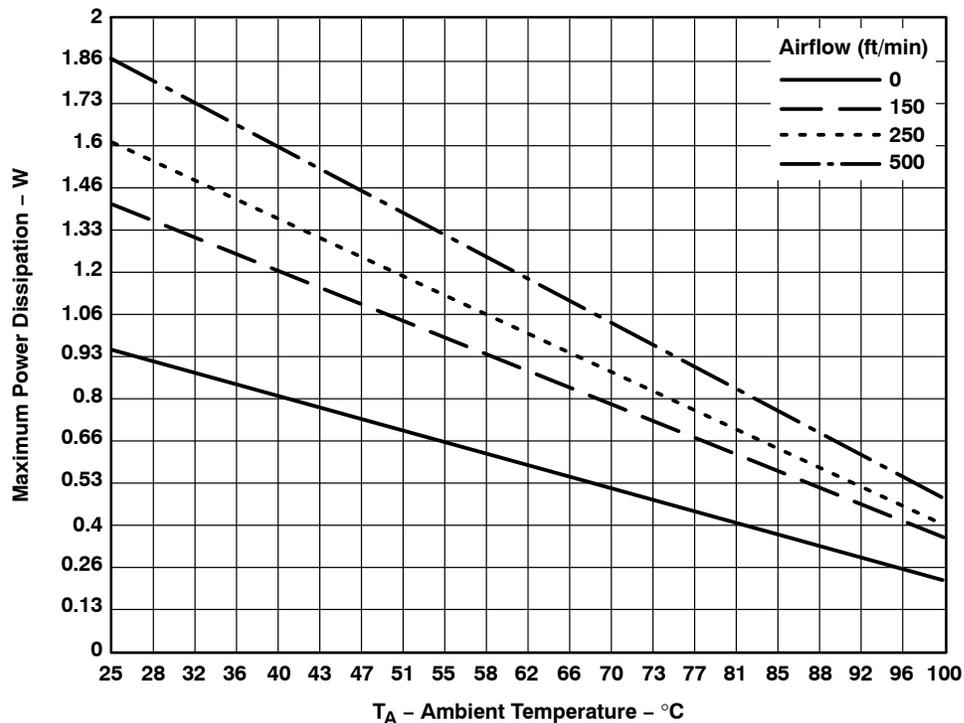
## Derating Curves

When a device reaches a state of thermal equilibrium, the electrical power delivered is equal to the thermal heat dissipated, which is transferred to the surroundings. The maximum allowable power consumption ( $P$ ) at a given ambient temperature ( $T_A$ ) is computed using the maximum junction temperature for the chip ( $T_J$ ) and the thermal resistance of the package ( $\theta_{JA}$ ) as shown in equation 3:

$$P = (T_J - T_A)/\theta_{JA} \quad (3)$$

Over time, heat destroys semiconductors. Therefore, manufacturers usually specify a maximum junction temperature ( $T_J \text{ max}$ ). If the junction temperature goes above this value, irreversible damage occurs. Typically, the IC user knows the ambient temperature of the operating environment ( $T_A$ ), the thermal resistance of the IC package ( $\theta_{JA}$ ) provided by the supplier, and a specified maximum junction temperature. Equation 3 can be used to determine the maximum power that can be applied to the particular package under the specified test conditions.

By varying the ambient temperature at a given airflow in equation 3, a derating curve can be developed for each package. By using the thermal resistance value of the package at different airflows, a derating curve can be developed for each airflow. A typical set of derating curves for the 16-pin SOIC (DW) package is shown in Figure 5. The data for the 16-pin DW package ( $\theta_{JA}$ ) used to calculate the curves was generated using a JEDEC 1s (low K) PCB design.



**Figure 5. Derating Curves for 16-Pin DW SOIC Package**

As an example, the 16-pin DW package has a  $\theta_{JA}$  of  $104.6^\circ\text{C}/\text{W}$  at zero airflow. The maximum power that the package can withstand at  $T_A = 25^\circ\text{C}$  and  $T_J = 125^\circ\text{C}$  is:

$$P = (125^\circ\text{C} - 25^\circ\text{C})/104^\circ\text{C}/\text{W} = 0.956 \text{ W} \quad (4)$$

$\theta_{JA}$  was derived using a JEDEC low-K PCB.

For a given package, these derating curves allow the designer to see the effect of rising ambient temperature and changes in airflow on the maximum power allowed. By accessing the web page, the user can view the derating curves for each package. The program uses the  $\theta_{JA}$  data shown to display the maximum power dissipation (y-axis) of the package over a range of ambient temperatures (x-axis). This maximum power dissipation of the package is equivalent to the maximum allowable consumption of the IC device. The user can vary the junction temperature and ambient temperature range used in the calculation of maximum power dissipation.

## Conclusion

An improvement of 30% to 45% is seen in the thermal resistance values of TI packages when tested on a high-K board versus a low-K board. The high-K design has two copper planes embedded in the PCB. Because the high-K design is more representative of many end-user PCB designs, this new thermal data gives a more accurate representation of the performance of the package in use. TI thermal data is now easily accessible to external customers via the TI external web page.

## Acknowledgment

The authors of this application report are Douglas W. Romm and Ray H. Purdom.

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# **Standard Linear & Logic Semiconductor Marking Guidelines**

---

*James Huckabee and Cles Troxtell*

*Standard Linear & Logic*

## **ABSTRACT**

The Texas Instruments (TI™) Standard Linear & Logic (SLL) business group uses complex methods to assign device topside marking. These methods ensure that correct component identification is applied at each factory location. End users of the standard components often need to peruse many TI and industry publications to understand the markings. This application report combines topside-marking guidelines and package-outline examples in one document.

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## Introduction

This application report describes the guidelines used by SLL to mark semiconductor packages. This document provides customers the answers to the most frequently asked questions and allows them to review the rules used in marking TI devices. Internet web addresses of available tools also are provided.

## Background

The marking of microcircuits originates in military specifications. MIL-M-38510 defines general rules for marking devices used in most military applications. Some of the requirements of MIL-M-38510 are package index identifier, part identification, chip identification code, manufacturer's identification code, manufacturer's designation, country of origin, device type, device class, drawing designator, case outline, and many others. TI marking specifications are based on some of the same requirements.

## Standards for Topside Marking of Semiconductor Components

Commercial marking specifications are an outgrowth of the military applications. The marking placed on each component provides important information about how and where the device was manufactured and about the materials used in the manufacturing process.

TI defines marking requirements in its internal specification system for each unique device. The assignment of specific device marking is defined by technology namerules, the specific electronic function, and the assigned package namerules. The standard component-identification requirements are defined in TI quality-system specifications. The quality requirements for the component, as marked, are defined in the specific package family quality specifications.

TI standard marking contains the following items:

- TI logo
- Lot trace code (LTC)
- Device name (or abbreviation or code)
- Pin 1 identifier (if not a mechanical feature of the package)

The TI logo is used as the company identifier for most marking applications. In some cases, due to component size, TI is used in place of the TI logo. Some components are so small that no company identifier is used.

The LTC is used in TI marking if space permits, and contains the following information:

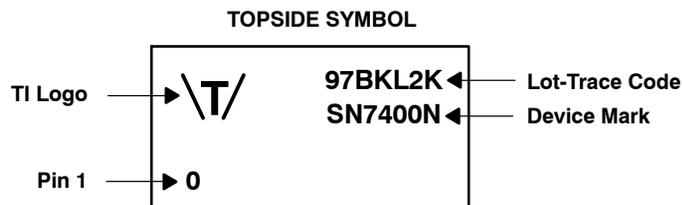
- Date of manufacture by year (Y) and month (M) the lot started in assembly
- Specific assembly-lot code (LLLL) (sequential alphanumeric identification assigned when the lot started in assembly)

For some assembly subcontractors, the assembly-lot code characters are ZLLL. The Z *always* is the leading character and is reserved to ensure that only specific subcontractors use it. The remaining characters (LLL) are assigned and used by the specific subcontractor for lot-genealogy purpose.

- Site of manufacture code (S)

The LTC provides a means of tracing an individual marked component to the assembly site, the assembly-lot number, the wafer-fabrication site, and the specific wafer-fabrication lot number.

The LTC for each manufacturing lot is generated when the lot starts assembly, and is printed as part of the marking diagram on the specific-lot factory traveler. Figure 1 illustrates a typical traveler marking diagram.



**Figure 1. Typical Text Printed on the Lot Traveler**

## Package Technology Marking Restrictions

The demand for smaller and lighter systems applications, coupled with the increasing complexity of electronic technologies and functions, has produced an antagonistic relationship between the technology device identifiers and the available surface area on the devices for marking. While device names have more characters, typically, the package is shrinking. Figure 2 is an example of standard marking for the SN7400N device.



**Figure 2. Standard Marking**

Recent technology names are more complex. It is not uncommon for device names to exceed 20 characters. If the number of characters in the device name exceeds the maximum characters allowed on a single line for the particular package, the device name must be abbreviated or coded. Figure 3 shows the result if a device name is too long. The SN74ALVCHR162269A DGGR is shortened by omitting the prefix (SN74) and the suffix (DGGR) to allow an abbreviated mark, but the technology and function can be identified easily.



**Figure 3. Typical Abbreviated Device Marking**

If the package is even smaller, the package marking is coded. Figure 4 shows a typical coded marking.



**Figure 4. Coded Marking**

In this example, the LTC is shortened to only the year and month of manufacture. The device name is coded in very short form. If possible, the code contains some of the technology characters.

Using coded symbology also can complicate lot genealogy. If a problem is discovered involving *one* device produced in this year and month, and lot identification is not evident, *all* lots of this device type produced during this month are quarantined.

## Typical Applications of Each Marking Format

SLL uses three standard marking formats, which are the preferred formats for all standard catalog devices. Use of these standard formats is encouraged, even if customers require special content.

Format 1 – Standard two-line marking

Format 2 – Standard three-line marking

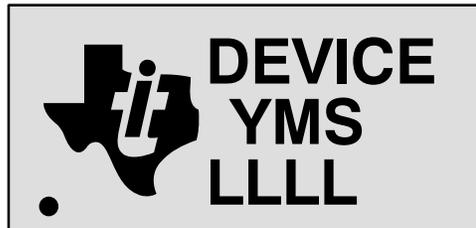
Format 3 – Two-line marking for very small packages

Format 1 (see Figure 5) is the preferred format for all marking and is used on all packages where space is not a limiting factor. Key features of this format are that it allows the use of the full TI logo, the full LTC, and the full device name as ordered. Lot genealogy can be traced to a single assembly lot at a single site, and the component is marked with the actual device name as ordered by the customer.



**Figure 5. Generic Marking Standard, Format 1**

Format 2 (see Figure 6) is used on packages that are too small for Format 1. This format allows use of the full LTC and maintains the lot-genealogy capability of Format 1. The device name can be abbreviated or coded, depending on the technology/function and package used.



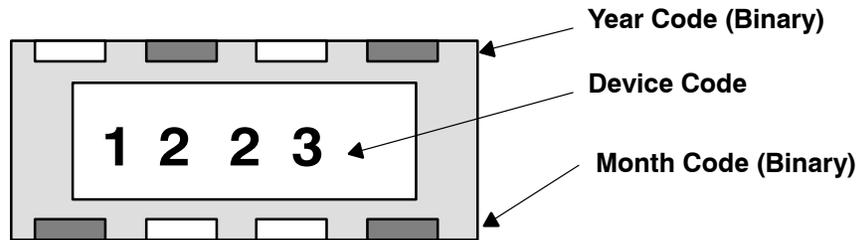
**Figure 6. Generic Marking Standard, Format 2**

Format 3 (see Figure 7) is used only on smaller packages where neither Format 1 or Format 2 is feasible. This format loses the full LTC and decreases lot-genealogy capability (from the individual component) to *all* lots of a device type in a specific year and month.



**Figure 7. Generic Marking Standard, Format 3**

Additional special formats are used on very small packages, such as SOT/TO. The format is tailored to the specific package. Figure 8 shows one special format, for the DBV package.



**Figure 8. Generic Special Marking Format for the DBV Package**

In this example, the year and month are binary codes along the edges of the device (year is 5 for 1995, and month is 9 for September).

The device code is four characters where:

Character 1 = Technology code

Characters 2 and 3 = Device function code (two characters)

Character 3 = Wafer fabrication and assembly site (combination) code.

## Device Marking Assignment

SLL has defined naming rules (namerules) that determine the marking applied to a specific standard catalog device. There are three namerules for each technology: A, B, and C. Standard pin/package configurations have a unique namerule and format assigned.

An example of a device/technology namerule for an SN74ABT device is:

NAMERULE A	NAMERULE B	NAMERULE C
SN74ABT***	ABT***	AB***

The asterisks are wild-card characters for the specific device function.

Device namerule A uses the entire device name, including any prefixes and the package designator:

DEVICE NAME	MARKING
SN74ABT245N	SN74ABT245N

The N package is assigned to namerule A and format 1.

Device namerule B omits the prefix and package designator from the device name:

DEVICE NAME	MARKING
SN74ABT245DW	ABT245

The 20-pin DW package is assigned to namerule B, format 1.

Device namerule C codes the device name:

DEVICE NAME	MARKING
SN74ABT245PWR	AB245

The 20-pin PW package is assigned to namerule C, format 2.

Device revisions are included as a part of the device marking, for example:

NAMERULE	DEVICE NAME	MARKING
A	SN74ABT245AN	SN74ABT245AN
B	SN74ABT245ADW	ABT245A
C	SN74ABT245APWR	AB245A

Namerule C needs further explanation. Device functions with three numbers (e.g., 245 in the examples above) also apply to device functions with fewer than three numbers.

For example, for namerule set SN74HCT\*\*\* HCT\*\*\* HT\*\*\*  
an SN74HCT**04**PWR device is marked HT**04**.

Conversely, device namerules with three numbers *do not necessarily apply* to device names with *more than three numbers*.

For example, for namerule set SN74ABT\*\*\* ABT\*\*\* AB\*\*\*  
an SN74ABT**245**PWR device is marked AB**245**.

However, a device such as SN74ABT2245PWR *is not* marked AB2245.

A different namerule applies to SN74ABT2\*\*\* devices.

For example, for namerule set SN74ABT2\*\*\* ABT2\*\*\* AA\*\*\*  
the SN74ABT2245PWR is marked **AA245**.

Some packages, because of their very small size, have special namerules and formats. The SOT packages (DBV, DCK, and PK) are examples of these special assignments. Each special namerule has a separate listing of the rules for the specific technology, package, and function combinations.

## Web Address of Marking Guidelines

The main home page of the SLL marking guidelines is:

<http://www.ti.com/sc/docs/products/logic/package/symindex.html>

It contains links to various marking web pages and gives a brief explanation of how to determine the correct marking for a particular device.

For example, to find the device name marking for the SN74ABT245N device, from the Package Namerule Assignments table, find 20 PIN PDIP (N) and the corresponding NAMERULE A. In the Device Namerules table, look in the A column to find the device technology (e.g., SN74ABT\*\*\*), and see that this device uses the entire device name and the package code (N). Therefore, the device name marking on the device is: SN74ABT245N.

The following address displays the package namerule and format assignments by pin and package:

<http://www.ti.com/sc/docs/products/logic/package/pkrule.html>

The following address displays the device/technology namerule definitions. Namerules A, B, and C for each defined technology are displayed in alphabetical order:

<http://www.ti.com/sc/docs/products/logic/package/namerule.html>

The following address displays the special namerule and format defined for the 5-pin DBV package. Additional information that can be accessed is an explanation of the binary date code used on the DBV package.

<http://www.ti.com/sc/docs/products/logic/package/5pinsym.html>

The following links allow a search to determine either the device name or device marking:

[http://www1.sh.sc.ti.com/pkg/SYMBOL/symbol\\_search.html](http://www1.sh.sc.ti.com/pkg/SYMBOL/symbol_search.html) (TI internal access)

[http://www.shvp.sc.ti.com/cgi-bin/pkg/symbol\\_search](http://www.shvp.sc.ti.com/cgi-bin/pkg/symbol_search) (external access)

From these two web pages, a search for the package mark or device name can be initiated. Figures 9 and 10 show the search inputs and results. The inputs must be exact and complete. For example, the device name must include the TI device package code (DW) and packaging code (R).

The screenshot shows the Texas Instruments website navigation bar with the following elements:

- Navigation menu: Semiconductor, Standard Linear & Logic, Assembly & Packaging, Search, Feedback, Internal Web.
- Search bar: SLL Pkg/Assy Home [Go]

**Package Marking Search**

Device Name:

Package Mark:

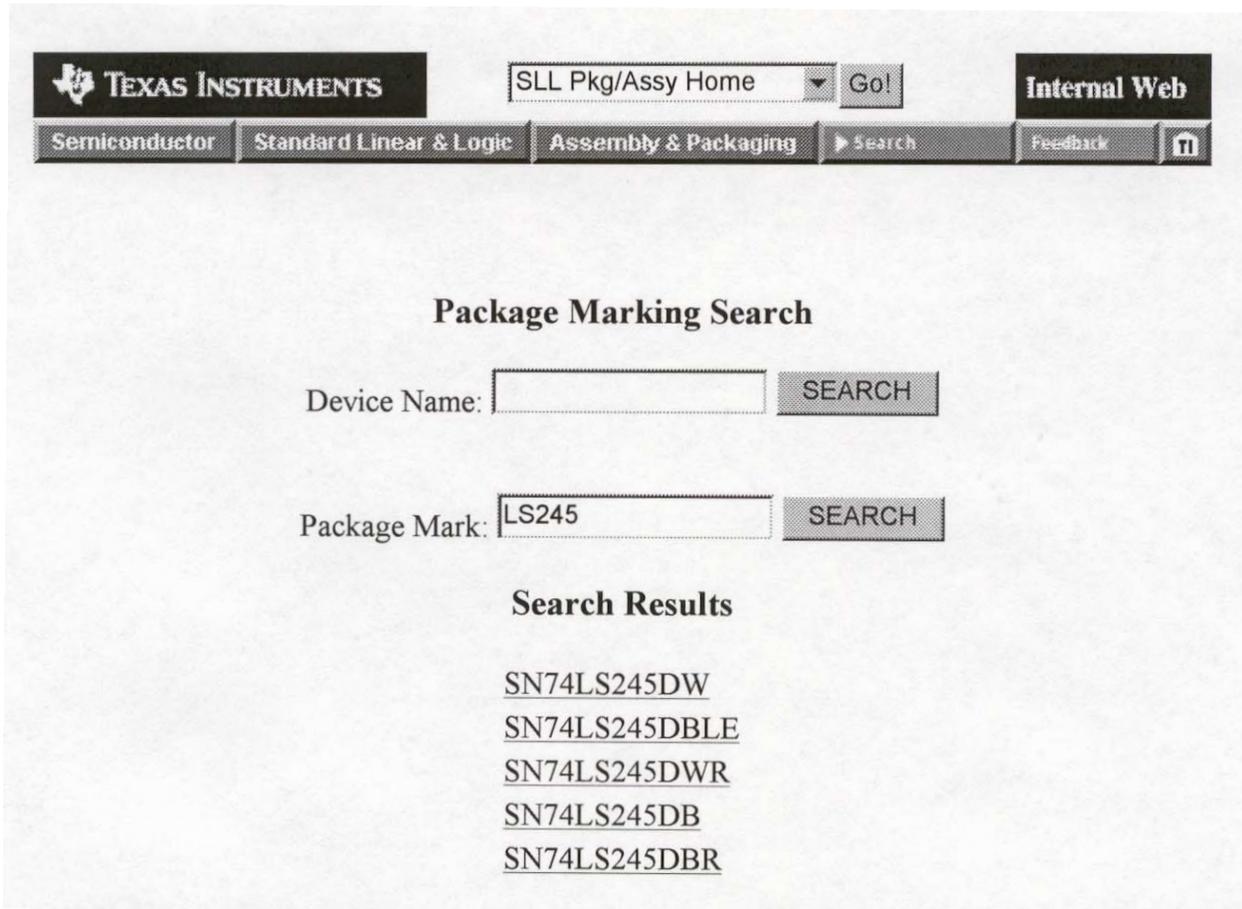
**Search Results**

**DEVICE NAME: SN74LS245DWR**  
**INTERNAL DEVICE NAME: SN74LS245DWR**  
**DEVICE DESCRIPTION: OCTAL BUS TRANSCEIVER**  
**DEVICE STATUS: ACTIVE (OBSOLETED)**  
**PIN/PKG: 20/DW**  
**T-symbol: DW**  
**Mark assigned at: CUST1**  
**Actual Topside Mark: LS245**

The diagram shows a physical package marking with the following details:

- Topside marking: YML111S, LS245
- Package type: 20-pin DW package

Figure 9. Search for Package Mark and Results



The screenshot shows the Texas Instruments website interface. At the top, there is a navigation bar with the Texas Instruments logo on the left, a dropdown menu set to "SLL Pkg/Assy Home" with a "Go!" button, and an "Internal Web" button on the right. Below this is a secondary navigation bar with buttons for "Semiconductor", "Standard Linear & Logic", "Assembly & Packaging", "Search", "Feedback", and a home icon. The main content area is titled "Package Marking Search". It contains two search fields: "Device Name:" with an empty input box and a "SEARCH" button, and "Package Mark:" with the input "LS245" and a "SEARCH" button. Below the search fields, the heading "Search Results" is followed by a list of five device part numbers: SN74LS245DW, SN74LS245DBLE, SN74LS245DWR, SN74LS245DB, and SN74LS245DBR.

**Figure 10. Search for Device Name and Results**

## Conclusion

The SLL marking assignments provide unique identification to each device. The advent of more complex technologies, and the corresponding lengthening of the technology name, is stressing the capability to assign intuitive marking. This, in turn, requires more marking assignments to be coded. Coded marking requires more details to be available to customers to ensure that the correct product is purchased for customers' applications. The marking on the device package is the link to the component's complete identification and its process history.

## Glossary

SLL	Standard Linear & Logic, a TI strategic business entity
Marking	The characters physically marked on the topside of each device
Pin/Pkg	The number of pins on a particular package
Namerule	A set of marking guidelines for a specific technology that defines the marking for specific devices in specific package outlines

## References

1. MIL-M-38510                      Marking historical requirements



# **Semiconductor Packing Methodology**

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*Cles Troxtell, Bobby O'Donley, Ray Purdom, and Edgar Zuniga*

*Standard Linear and Logic*

## **ABSTRACT**

The Texas Instruments (TI™) Semiconductor Group uses three packing methodologies to prepare semiconductor devices for shipment to end users. The methods employed are linked to the device level for shipping configuration keys. End users of the devices often need to peruse many TI and industry publications to understand the shipping configurations. This application report documents TI's three main shipping methods and typical dimensions for end users to review.

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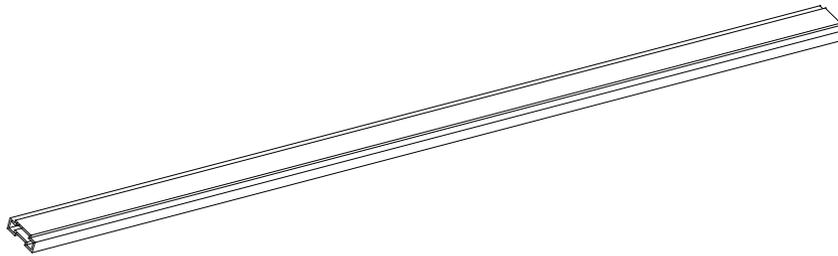
## Introduction

This application report describes in detail the methods used by the TI Standard Linear and Logic (SLL) business unit to pack semiconductor devices (components). This report provides customers the answers to the most frequently asked questions and allows them to review the different methods used to pack our products.

## Background

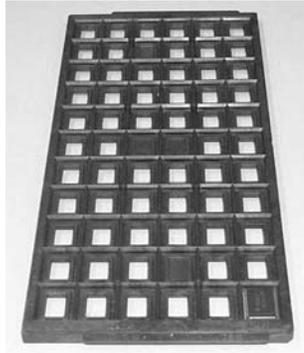
TI ships product in three basic configurations: magazines, trays, and tape and reel. Brief definitions of each packing configuration are:

- **Stick Magazines** – The stick magazine (also called shipping tube) was developed in the early days of the integrated circuit (IC) industry. The magazine is used to transport and store electronic components between the manufacturer and the customer and for use in the manufacturing plant. Magazines also are used to feed components to automatic-placement machines for surface and through-hole board mounting. Multiple stick magazines are placed in next-level intermediate containers (boxes and bags) in standard packing quantities. A typical stick-magazine is shown in Figure 1.



**Figure 1. Single-Stick-Magazine Shipping Tube**

- **Trays** – The IC shipping tray contains the components during component-assembly operations, during transport and storage from the component manufacturing plant to the customer's board-assembly site, and for feeding components to automatic-placement machines for surface mounting on board assemblies. The tray is designed for components that have leads on four sides (QFP and TQFP packages) and require component lead isolation during shipping, handling, or processing. Trays are stacked and bound together to form standard packing configurations. SLL uses only standard JEDEC tray configurations. A typical JEDEC tray is shown in Figure 2.



**Figure 2. JEDEC Tray**

- **Tape and Reel** – The tape-and-reel configuration is used for transport and storage from the manufacturer of the electronic components to the customer, and for use in the customer manufacturing plant. The configuration is designed for feeding components to automatic-placement machines for surface mounting on board assemblies. The configuration can be used for all SMT packages and provides component lead isolation during shipping, handling, and processing. The complete configuration consists of a carrier tape with sequential individual cavities that hold individual components, and cover tape sealed onto the carrier tape to prevent the component from exiting the cavity. In most cases, single reels of components are inserted into intermediate boxes prior to shipping. A typical loaded reel is shown in Figure 3.



**Figure 3. Reel With Carrier Tape**

## Typical Applications of Each Packing Method

### Stick Magazine (Shipping Tubes) – Primary Component Container

Magazines are constructed of rigid clear or translucent polyvinylchloride (PVC) material.

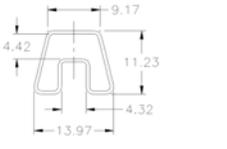
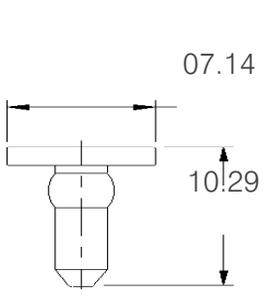
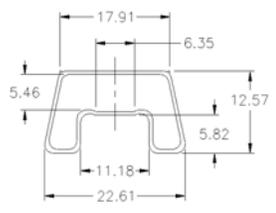
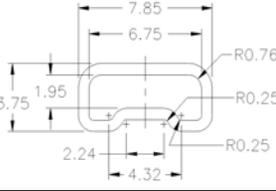
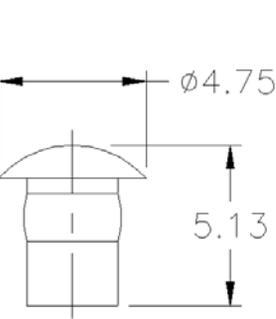
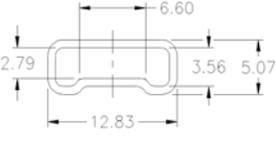
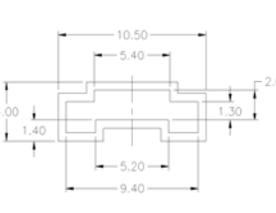
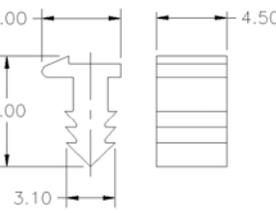
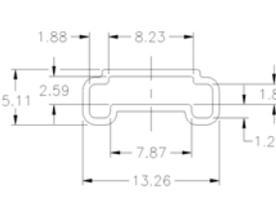
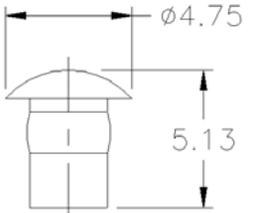
Magazines are extruded in applicable standard outlines that meet current industry standards, and protect components during shipping and handling. The magazine dimensions provide proper component location and orientation for industry-standard automated-assembly equipment.

Magazines are packed and shipped in multiples of the single-magazine quantity. Multiple magazines are loaded into intermediate containers (bags and boxes) to form standard quantities for ease of handling and order simplification. Typical intermediate-level packing quantities for magazines vary by pin count and package type. Figure 4 shows an intermediate packing for PDIP packages. Magazine packing quantities are included in Table 1.



**Figure 4. Intermediate Packing for PDIP Packages**

**Table 1. Magazine**

Package Type	Pin Count Package Designator	Quantity Per Magazine	Container Standard Quantity	Sectional Shape (mm)	Magazine Length (mm)	Wall Thickness (mm)	Pin or Plug Shape and Dimensions (mm)
PDIP (300 mil)	8 P 14 N 16 N 20 N 24 NT 28 NT	50 25 25 20 15 10	1000 1000 1000 1000 750 500		506.1	0.58	
PDIP (600 mil)	24 N	15	750		507.0	0.56	
SOP (JEDEC, narrow body)	8 D 14 D 16 D	75 50 40	1500 1000 1000		507.0	0.55	
SOP (JEDEC, wide body)	16 DW 20 DW 24 DW 28 DW	40 25 25 20	1000 1000 1000 1000		507.0	0.76	
SOP (EIAJ)	8 PS 14 NS 16 NS 20 NS 24NS	80 50 50 40 34	1040 1000 1000 1000 1020		530.0	0.55	
SSOP (narrow body, pitch ≤1 mm)	28 DB 30 DB 38 DB	50 50 40	1000 1000 1000				
SSOP (wide body, pitch ≤1 mm)	28 DL 48 DL 56 DL	40 25 20	1000 1000 1000		473.7	0.64	



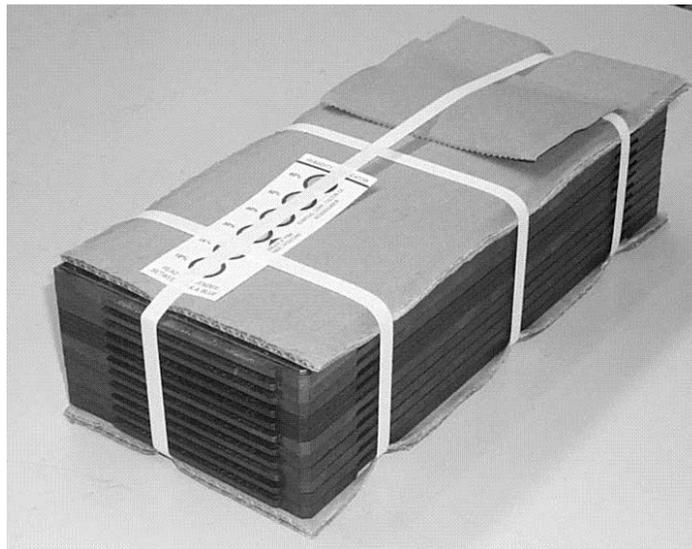
## Trays – Primary Component Container

Trays are constructed of carbon-powder or fiber materials that are selected based on the maximum temperature rating of the specific tray. TI trays that are designed for use on components requiring exposure to high temperatures (moisture-sensitive components) have temperature ratings of 150°C or more.

Trays are molded into rectangular JEDEC standard outlines containing matrices of uniformly spaced pockets. The pocket cradles the component for protection during shipping and handling. The spacing provides exact component locations for standard industry automated-assembly equipment used for pick-and-place in board-assembly processes.

Trays are packed and shipped in multiples of the single-tray quantity. Trays are stacked and bound together for rigidity. An empty cover tray is applied to the top of the loaded and stacked trays. Typical tray stack configurations are five full trays and one cover tray (5+1) and ten full trays and one cover tray (10+1). A typical 10+1 tray stack is shown in Figure 5.

Customers can receive units in single or multiple stacks, depending on individual requirements.



**Figure 5. Example of Trays Stacked and Bound**

Components are arranged in the trays to match standard industry norms. TI standard orientation is to place pin 1 at the tray chamfered corner (see Figure 6).



**Figure 6. JEDEC Tray With Properly Arranged Units**

Standard packing quantities vary by package size. Table 2 lists SLL packages and their standard quantities.

**Table 2. SLL Packages and Standard Quantities**

PACKAGE TYPE	PACKAGE	PINS	QUANTITY PER TRAY	MATRIX	CONTAINER STANDARD QUANTITY
TQFP	PM	64	160	8 × 20	800
	PN	80	119	7 × 17	495
	PCA	100	90	6 × 15	450
	PZ	100	90	6 × 15	450
QFP	RC	52	96	6 × 16	480

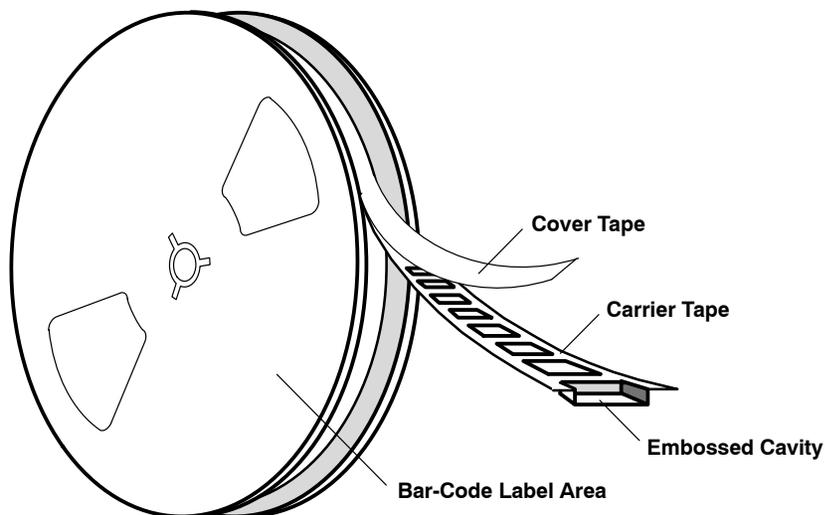
## Tape and Reel – Primary Component Container

The tape-and-reel configuration, as shipped by TI, meets current industry standards. EIA-481-1, EIA-481-2, and EIA-481-3 apply to the embossed configurations. EIA-468-B applies to the radial-lead-device configurations.

### ***Embossed Tape and Reel***

Most components ordered by customers are delivered in the embossed tape-and-reel configuration. This configuration consists of a carrier tape with a cover tape sealed to the carrier tape (see Figure 7). This composite tape, loaded with the components, is wound onto a reel. The reel is placed in a corrugated shipping box for transport and delivery.

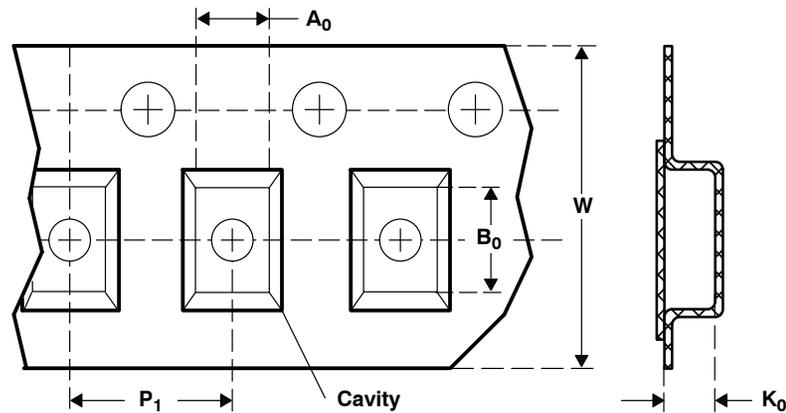
The three components of this packing configuration are the carrier tape, the cover tape, and the reel. A description of each component is provided in the following paragraphs.



**Figure 7. Tape-and-Reel Packing**

## Carrier Tape

Figure 8 shows the basic outline and dimension labels of the carrier tape. Typically, the carrier tape is constructed from a polystyrene (PS) or PS-laminate film. The unformed film thickness is 0.2 mm to 0.4 mm, depending on the size and weight of the component carried by the tape.



**Figure 8. Carrier-Tape Dimensions**

Carrier tape design is defined largely by the component length, width, and thickness.

These component dimensions are the basis for the common industry dimension variables for carrier tape:

- $A_0$  = Dimension designed to accommodate the component width
- $B_0$  = Dimension designed to accommodate the component length
- $K_0$  = Dimension designed to accommodate the component thickness. For cavities with bottom pedestals, a  $K_1$  dimension is specified to identify the required pedestal height.
- $W$  = Dimension defining overall width of the carrier tape. This must conform to accepted Industry norms (8/12/16/24/32/44/56 mm).
- $P_1$  = Dimension defining the pitch between successive cavity centers. This dimension must conform to industry norms (4-mm increments).

Table 3 gives the basic dimensions for SLL packages shipped in the tape-and-reel configuration. The table also shows shipping quantities and moisture-sensitivity requirements.

**Table 3. Tape-and-Reel Packing Configurations**

FAMILY	PACKAGE	PINS	QUANTITY	REEL DIAMETER (mm)	A <sub>0</sub> (mm)	B <sub>0</sub> (mm)	K <sub>0</sub> (mm)	K <sub>1</sub> (mm)	P <sub>1</sub> (mm)	W (mm)	DRY PACKED
SOIC	DR	8	2500	330	6.4	5.2	2.1	N/A	8	12	No
		14	2500	330	6.5	9	2.1	N/A	8	16	
		16	2500	330	6.5	10.3	2.1	N/A	8	16	
	DWR	16	2000	330	11.1	10.85	2.65	2.35	12	16	
		20	2000	330	11.1	13.35	2.7	2.35	12	24	
		24	2000	330	11.1	15.9	2.7	2.35	12	24	
		28	1000	330	11.35	18.67	3.1	2.44	16	32	
TSSOP	PWR	8	2000	330	7	3.6	1.6	1.2	8	12	No
		14	2000	330	7	5.6	1.6	1.2	8	12	
		16	2000	330	7	5.6	1.6	1.2	8	12	
		20	2000	330	6.95	7.1	1.6	1.2	8	16	
		24	2000	330	6.95	8.3	1.6	1.2	8	16	
	DGGR	48	2000	330	8.6	15.8	1.8	1.3	12	24	Yes
		56	2000	330	8.6	15.8	1.8	1.3	12	24	
		64	2000	330	8.4	17.3	1.7	1.2	12	24	
SOP	PSR	8	2000	330	8.2	6.6	2.5	2.1	12	16	No
	NSR	14	2000	330	8.2	10.5	2.5	2.1	12	16	
		16	2000	330	8.2	10.5	2.5	2.1	12	16	
		20	2000	330	8.2	13	2.5	2.1	12	24	
		24	2000	330	8.2	15.7	2.5	2.1	12	24	
SSOP	DBR	14	2000	330	8.2	6.6	2.5	2.1	12	16	No
		16	2000	330	8.2	6.6	2.5	2.1	12	16	
		20	2000	330	8.2	7.5	2.5	2.1	12	16	
		24	2000	330	8.2	8.8	2.5	2.1	12	16	
		28	2000	330	8.2	10.5	2.5	2.1	12	16	
		30	2000	330	8.2	10.5	2.5	2.1	12	16	
		38	2000	330	8.2	13	2.5	2.1	12	24	
	DL	28	1000	330	11.35	9.78	3.1	2.44	12	24	
		48	1000	330	11.35	16.2	3.1	2.44	16	32	
		56	1000	330	11.35	18.67	3.1	2.44	16	32	
	DBQR	16	2500	330	6.4	5.2	2.1	N/A	8	16	
		20	2500	330	6.5	10.3	2.1	N/A	8	16	
		24	2500	330	6.5	10.3	2.1	N/A	8	16	

**Table 3. Tape-and-Reel Packing Configurations (Continued)**

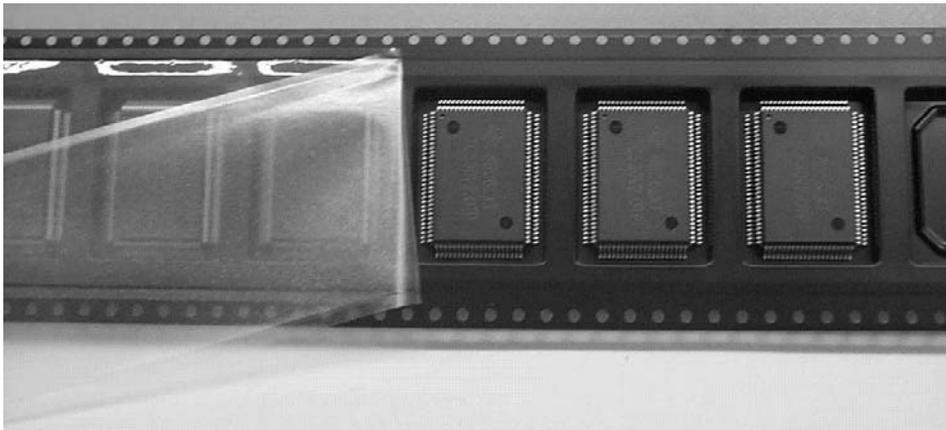
FAMILY	PACKAGE	PINS	QUANTITY	REEL DIAMETER (mm)	A <sub>0</sub> (mm)	B <sub>0</sub> (mm)	K <sub>0</sub> (mm)	K <sub>1</sub> (mm)	P <sub>1</sub> (mm)	W (mm)	DRY PACKED
TVSOP	DGVR	14	2000	330	6.8	4	1.6	1.2	8	12	No
		16	2000	330	6.8	4	1.6	1.2	8	12	
		20	2000	330	7	5.6	1.6	1.2	8	12	
		24	2000	330	7	5.6	1.6	1.2	8	12	
		48	2000	330	6.8	10.1	1.6	1.2	12	24	
		56	2000	330	6.8	11.7	1.6	1.2	12	24	
	DBBR	80	2000	330	8.4	17.3	1.7	1.2	12	24	
TQFP	PMR	64	1000	330	12.5	12.5	1.9	1.6	16	24	Yes
PowerFLEX™	KTPR	2	3000	330	6.5	10	2.45	2.2	8	16	No
	KTER	3	2000	330	9.8	11	2.45	2.2	12	24	
	KTGR	54	2000	330	9.8	11	2.45	2.2	12	24	
PLCC	FNR	20	1000	330	10.3	10.3	4.9	3.8	12	16	No
		28	750	330	13	13	4.9	3.7	16	24	
		44	500	330	18	18	5.7	4.1	24	32	Yes
MicroStar BGA™	GKER	96	1000	330	5.7	13.7	2	1.2	8	24	Yes
	GKFR	114	1000	330	5.7	16.2	2	1.2	8	24	
SOT	PKR	3	1000	330	4.85	4.52	2.3	1.85	8	12	No
	DCKR	5	3000	178	2.24	2.34	1.22	N/A	4	8	
	DBVR	5	3000	178	3.15	3.2	1.4	N/A	4	8	
TO-92	LPR	3	2000	360	N/A	N/A	N/A	N/1	13	18	No

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## Cover Tape

Typically, the cover tape is a PET film or film laminate, with adhesive applied to the underside of the film. Most applications use a heat-and pressure-sensitive adhesive to ensure a positive consistent seal to the carrier tape. The film thickness, including adhesive, is 50 to 65 microns.

A typical rectangular QFP package in the component pocket with the cover tape sealed, but partially peeled back, is shown in Figure 9. The package is properly oriented in the tape cavity.



**Figure 9. Rectangular QFP Package Properly Oriented in Carrier Tape**

Component orientation in the carrier-tape pocket is governed by EIA-783, which states that orientation rules shall be followed, sequentially, until no other variation is possible (see Figure 10):

1. The largest axis of the component outline shall be perpendicular to the tape length.
2. The edge of the package containing termination 1 shall be oriented toward the round sprocket holes.
3. For the components where rule 1 and rule 2 do not establish a unique orientation, termination 1 shall be in quadrant 1 (see Figure 11).

Typical TI component orientation is shown in Figure 12.

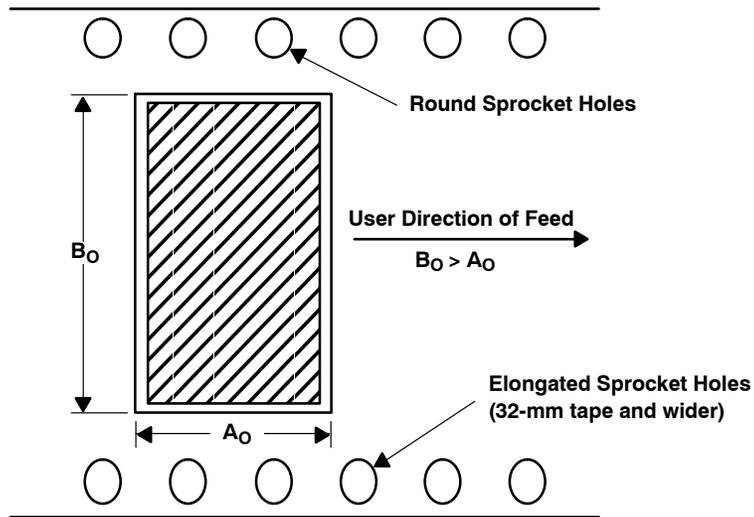


Figure 10. EIA-783 Guideline, Rules 1 and 2

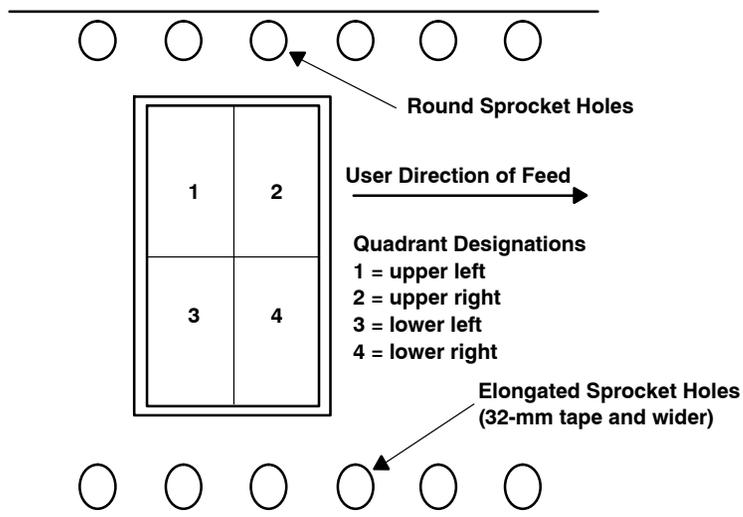
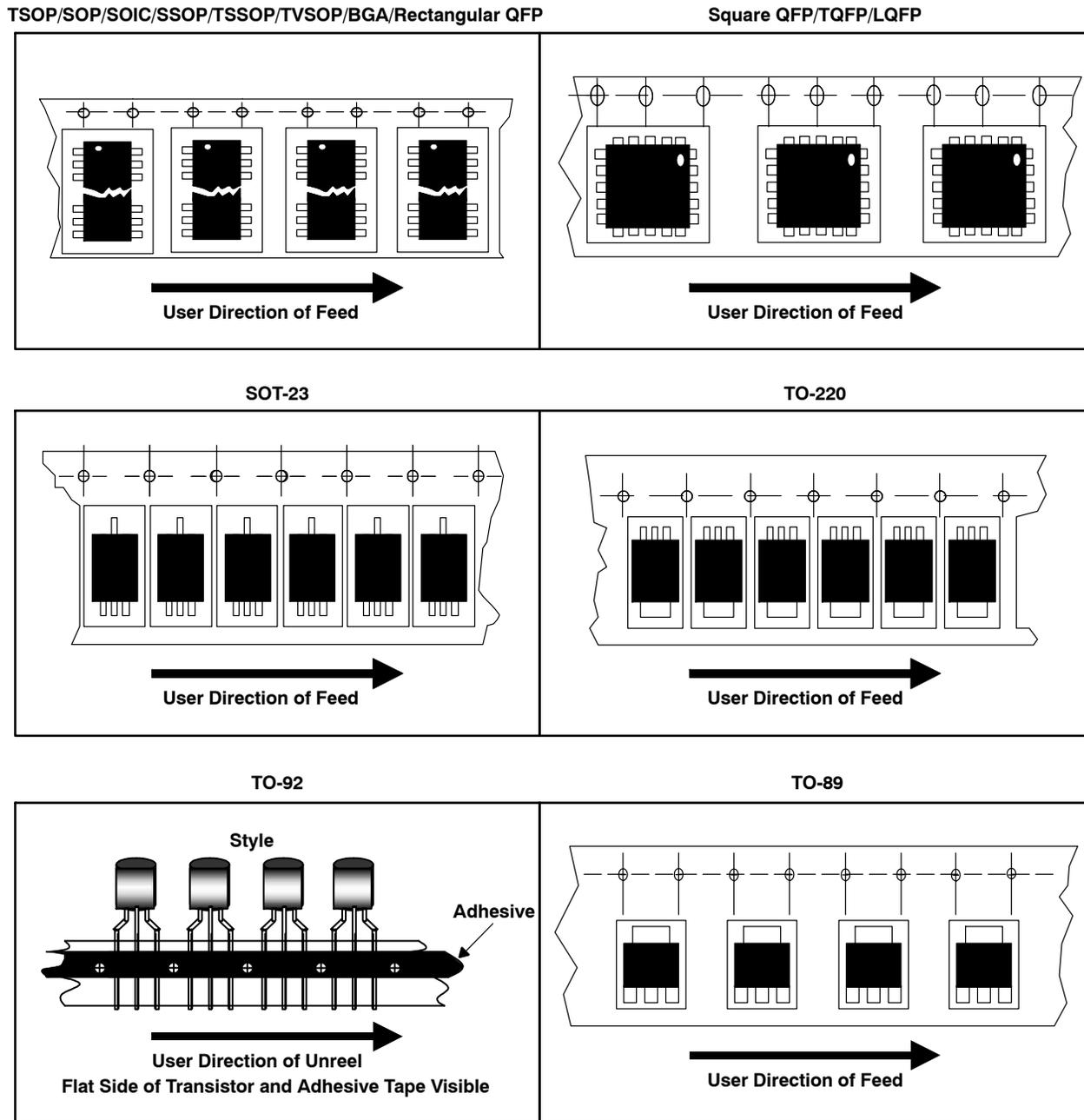


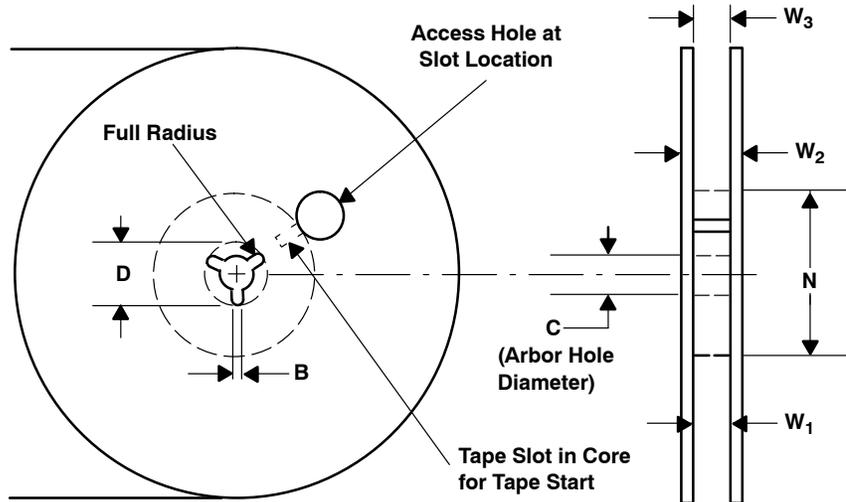
Figure 11. EIA-783 Guideline, Rule 3



**Figure 12. Typical TI Component Orientations for Tape-and-Reel Packing**

**Reels**

The reels that contain the sealed carrier tape are constructed of polystyrene (PS) material. The reels can be constructed of one, two, or three parts. Typically, they are blue, but other colors are acceptable. The reels are recyclable, and TI participates in environmentally responsible recycling programs. Customers can receive new or recycled reels. In all cases, recycled reels are required to conform to drawing specifications. Reel dimensions are within the EIA-481-1, EIA-481-2, and EIA-481-3 standards as shown in Figure 13.



**Figure 13. Typical Reel Outline as Defined by EIA-481-x**

Examples of tape-and-reel intermediate-level packing are shown in Figures 14 and 15.



**Figure 14. Loaded Reel (Not Moisture Sensitive)**



**Figure 15. Standard Box Containing Loaded Reel**

## Moisture Sensitivity

Plastic IC packages absorb moisture from the surrounding environment. This is a typical characteristic of the materials used in the construction of plastic packages (mold compound and die attach). The moisture inside the package increases or decreases to reach the relative humidity (RH) of the surrounding environment. Weight gain/loss analysis is used to determine the time that it takes for a package to reach moisture saturation or the time required for removing it. This information is used to specify maximum exposure times and minimum dry-baking times for a particular package.

Moisture inside the package turns into steam when the package is exposed to the vapor phase/infrared reflow and/or wave-soldering processes that are common in the fabrication of printed circuit boards (PCB). The resulting steam and vapor pressure can cause cracking of the package, a phenomenon called popcorning.

## Testing for Moisture Sensitivity

The sensitivity of a package to moisture-induced damage depends on many factors, including room temperature, relative humidity (RH), and the construction of the package. Surface-mount packages are more susceptible to moisture-induced damage than their through-hole counterparts because surface-mount packages normally are exposed to higher solder temperatures. Through-hole parts are usually larger and, therefore, are stronger mechanically.

TI surface-mount products are tested for moisture sensitivity using the procedures outlined on EIA/JEDEC A112-A and EIA/JEDEC A113-B. JEDEC levels 1 through 6 define relative levels of moisture sensitivity. Level 1 denotes a package that is not moisture sensitive. Any package denoted level 2, or higher, requires removal of moisture by baking or under vacuum, followed by dry packing to protect it during shipment. Shipping containers are labeled according to the product moisture-sensitivity classification (see *Moisture Labeling*). Dry packing and labeling procedures are discussed in the following paragraphs.

SLL packages have been tested and classified according to their sensitivity to moisture-induced damage. The classification of each surface-mount-technology (SMT) package is listed in Table 4.

**Table 4. Moisture-Sensitivity Classification for SMT Products**

PACKAGE TYPE	LEVEL 1†	LEVEL 2†	LEVEL 3†	LEVEL 4†
PLCC	PN		FN (44/68)	
TO/SOT	DCK (5) DBV (5) LP (3) KC (3/5) KV (5)			
SOP (EIAJ)	PS (8) NS (14/16/20)			
SOIC	D (8/14/16) DW (16/20/24/28)			
SSOP	DBQ (16/20/24) DB (14/16/20/24) DB (28/30/38) DL (28/48/56)			
TSSOP	DCT (8) PW (8/14/16) PW (20) DGG (64)	PW (24)	DGG (48/56)	
TVSOP	DGV (14/16) DGV (20/24/48/56) DBB (80)			
QFP		RC (52)	PH (80)	
TQFP		PAG (64) PZ (100) PCA (100) PN 80)		PM (64)
HSIP	PK (3)			
PowerFlex	KTP (2) KTE (3) KTG (5)			
MicroStar BGA			GKE (96) GKF (114)	

† Pin count is shown in parentheses.

NOTE: Some device types in these packages might have different moisture-sensitivity levels than those shown in this table. To date, no device package uses level 5 or 6.

TI through-hole packages have not been tested according to JESD 22-A112-A or JESD 22-A113-A standards. Due to the nature of the through-hole PCB soldering process, the component package is shielded from the solder wave by the PCB and is not subjected to the higher reflow temperatures experienced by surface-mount components.

TI through-hole packages are not classified as moisture sensitive.

## Dry-Packing Process

If a package has been determined to be moisture sensitive (level 2 or higher), it must be dry packaged. Normally, in this process packages are baked for 24 hours at  $125^{\circ}\text{C} \pm 5^{\circ}\text{C}$ . Baking time could vary, depending on the package type.

## Dry Packing

Dry packing consists of baking the packages to reduce moisture to a level not to exceed 0.05% by weight. Then, the units are placed in a moisture-barrier bag, along with desiccant, to keep the moisture inside the bag to a level  $<20\%$  RH. Each product is labeled as moisture sensitive, outlining the necessary precautions for handling the product. Table 5 shows the floor life for the different package moisture-sensitivity levels.

**Table 5. Floor Life for Different Package Moisture-Sensitivity Levels**

LEVEL	FLOOR LIFE			SOAK TIME		
	CONDITIONS		TIME	TIME (HOURS)	CONDITIONS	
	TEMPERATURE ( $^{\circ}\text{C}$ )	RH (%)			TEMPERATURE ( $^{\circ}\text{C}$ )	RH (%)
1	$\leq 30$	90	Unlimited	168	85	85
2	$\leq 30$	60	1 year	168	85	60
				$X + Y = Z$ (see Note)		
3	$\leq 30$	60	168 hours	$24 + 168 = 192$	30	60
4	$\leq 30$	60	72 hours	$24 + 72 = 96$	30	60
5	$\leq 30$	60	24 hours	$24 + 24 = 48$	30	60
6	$\leq 30$	60	6 hours	$0 + 6 = 6$	30	60

NOTE: X = time between bake and dry bake at the manufacturing site

Y = floor life of package after removal from dry-pack bag

Z = total soak time

The X values are default values. If the actual time exceeds this value, use the actual time and adjust the soak time.

## Typical Packing Method

The typical packing method requires the following materials:

- Magazines (plastic tubes), trays, tape and reel
- Desiccant
- Moisture-barrier bag
- Labels [moisture-sensitive identification (MSID) label, dry-pack caution label]
- Humidity-indicator card

Examples of tray and tape-and-reel dry pack are shown in Figures 16 and 17.



**Figure 16. Tray Box and Sealed Moisture-Barrier Bag (Top),  
Opened Bag and Tray Stack (Bottom)**



**Figure 17. Dry-Packed Tape-and-Reel Configuration**

**Moisture-Sensitivity Labeling**

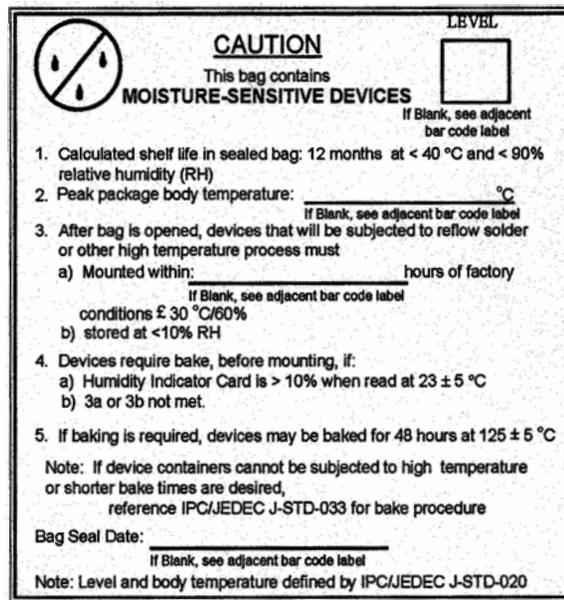
Primary and intermediate containers containing moisture-sensitive packages are labeled as shown in Figures 18 and 19.



**Figure 18. MSID Label**

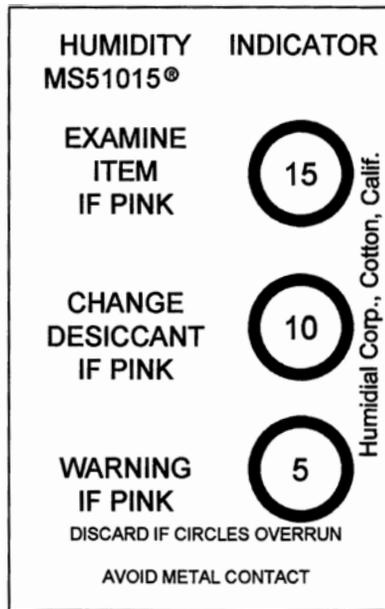
The MSID label is applied to the outside of the intermediate container near the TI barcode label. The presence of this label indicates that moisture-sensitive packages are inside.

The moisture-sensitivity caution label in Figure 19 is applied to the reel (for tape-and-reel configurations) and to the outside of the sealed moisture-barrier bag. This label contains detailed information specific to the device (moisture-sensitivity level, floor life, etc.).



**Figure 19. Moisture-Sensitivity Caution Label (Levels 2a Through 5a)**

The humidity-indicator card shown in Figure 20 is placed inside the sealed moisture-barrier bag. This card can verify that the product has been stored and shipped in a low-humidity environment.



**Figure 20. Humidity-Indicator Card**

***Environmental***

TI strives to optimize the packing density of each configuration to minimize the volume of packing material entering the industrial waste stream. Where possible, TI uses pure materials such as PS/PVC for ease of disposal. Cellulose material suppliers are encouraged to incorporate recycled material to reduce their consumption of virgin material. Typical packing materials used and their respective recycling code assignments are listed in Table 6.

**Table 6. Packing-Material Environmental Coding**

PACKING MATERIAL	COMPOSITION	RECYCLING CODE
Magazines	PVC	3
End pins/plugs	PVC	3
Trays	PAS/ABS/PPE	7 (other)
Reel	PS	6
Carrier tape	PS	6
Cover tape	PET-Laminate	7 (other)
Drypack bag	PET-Laminate	7 (other)
Boxes	Kraft corrugated	N/A

## Conclusion

TI continually reviews packing configurations to ensure alignment with current industry trends and requirements. TI strives to ensure that customers receive products that are easily introduced into their respective assembly processes, while minimizing the customer's requirement for storage space, equipment setups/loading, and volume of material entering an industrial waste stream.

It is important that TI's customers be familiar with TI's available packing configurations. This report summarizes the packing configurations in a format that makes this information easier to disseminate.

## Glossary

Carrier tape	Continuous formed embossed tape that is the primary container for components shipped in the tape-and-reel configuration
Cover tape	Clear or transparent tape applied to the carrier tape to seal the component(s) inside the individual tape compartments
Desiccant	Moisture-adsorbing material placed inside sealed dry-pack bags to adsorb internal bag moisture
Dry-pack bag	Moisture-barrier bag with WVTR (water-vapor transmission rate) of less than 0.000365 grams per 100 square inches surface area per 24 hours
EIA	Electronics Industries Alliance
End pins	Pins that are inserted in holes near each end of a magazine to prevent the components from exiting the magazine
End plugs	Similar to end pins, but the plug is inserted in each open end of the magazine
Humidity-indicator card	Card that can verify that humidity levels in sealed dry-packed bags have not exceeded specified limits. The card changes color to indicate different humidity levels.
Intermediate container	Container(s) that are filled with loaded primary-level containers
JEDEC	Joint Electron Device Engineering Council
Magazine (stick magazine or shipping tubes)	Usually, extruded PVC shaped for individual component requirements
PDIP paper bag	Intermediate container used for most PDIP products
Primary container	Container used for the first level of packing
Reel	Industry-standard reel used to collect and feed the loaded and sealed carrier tape
Reel box (pizza box)	Intermediate container for the fully loaded reel, carrier tape, and cover tape
Termination	Describes the ends of the package pins
Tray	Primary container used for QFP/TQFP/BGA devices, e.g., standard JEDEC outlines used as defined by package outlines
Tray box	Intermediate container for stacked and bound tray packs

## Acknowledgment

The authors of this article are Bobby O'Donley, Ray Purdom, Cles Troxtell, and Edgar Zuniga.

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## References

1. EIA-481 Standards – Excerpts used to assure complete alignment
2. EIA-783 – Component Orientation
3. JEDEC – Moisture Sensitivity Testing Procedures: EIA/JEDEC A112-A, EIA/JEDEC A113-B

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