Application Report

TLIN2021A-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for the TLIN2021A-Q1 which is a local interconnect network (LIN) transceiver in 8-pin SOIC (D), 8-pin SOT23 (DDF) and 8-pin VSON (DRB) packages to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

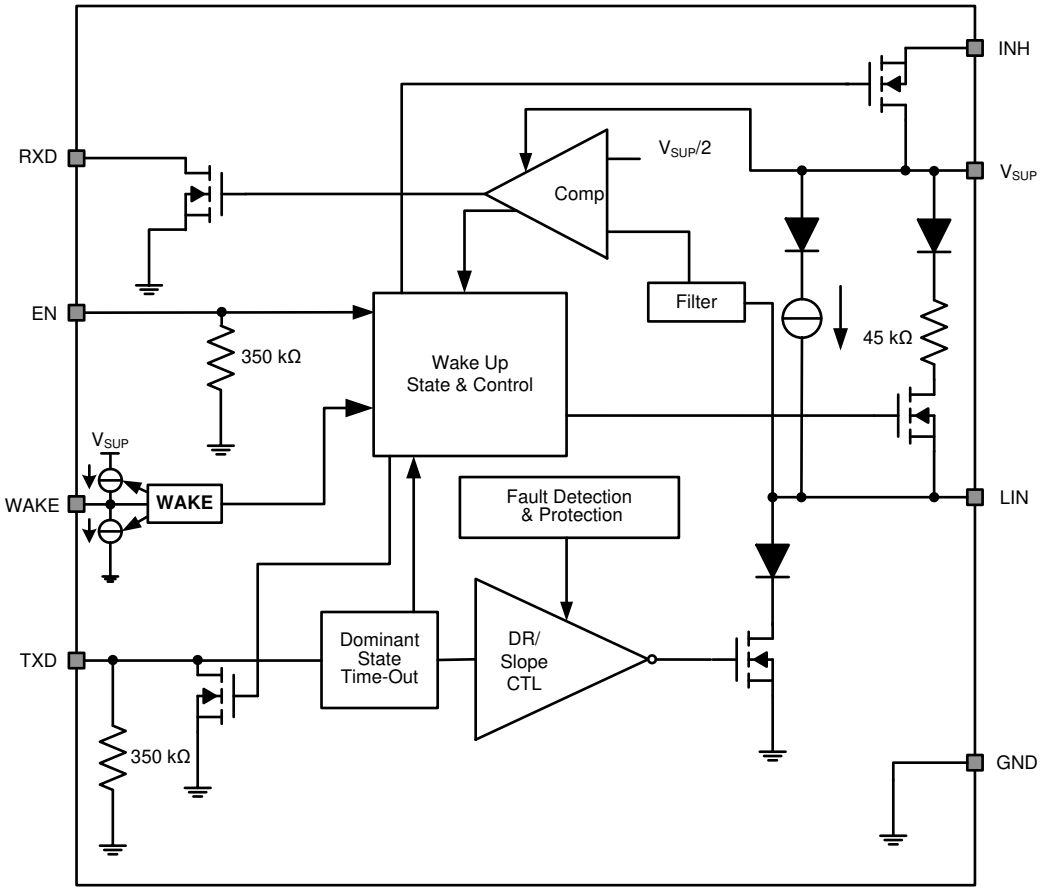

Figure 1-1. Functional Block Diagram

TLIN2021A-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for the TLIN2021A-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours) (DDF)	FIT (Failures Per 10^9 Hours) (DRB)	FIT (Failures Per 10^9 Hours) (D)
Total Component FIT Rate	6	7	13
Die FIT Rate	4	3	5
Package FIT Rate	2	4	8

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 150 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TLIN2021A-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
LIN Transmitter failure	43%
LIN Receiver failure	4%
High Voltage I/O failure	13%
Digital logic + I/O buffers failure	10%
Global power management + state control failure	30%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TLIN2021A-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TLIN2021A-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TLIN2021A-Q1 data sheet.

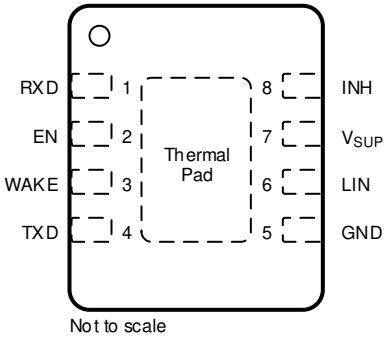

Figure 4-1. DRB Pin Diagram

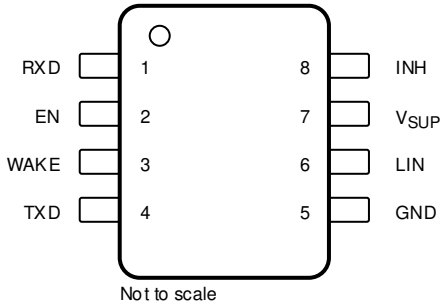

Figure 4-2. D and DDF Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- All conditions within the recommended operating conditions

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
RXD	1	RXD biased dominant, no communication from LIN bus to MCU possible	B
EN	2	Device may only operate in Standby Mode after power-on. If short occures in Normal mode, the part would be forced to enter sleep mode and could disable LIN communication	B
WAKE	3	WAKE pin biased to ground and no local wake up possible	B
TXD	4	TXD biased dominant, no communication from MCU to LIN bus possible	B
GND	5	None	D
LIN	6	LIN biased dominant, no LIN communication possible	B
VSUP	7	Device is unpowered and will not function	B
INH	8	INH biased to GND, will not be able to enable system power if used in this manner	B

Note

DRB package includes a thermal pad

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
RXD	1	No communication from LIN bus to MCU possible	B
EN	2	Biased low due to internal pull-down so device in standby mode	B
WAKE	3	No local wake up possible	B
TXD	4	No communication from MCU to LIN bus possible	B
GND	5	Device is unpowered and will not function	B
LIN	6	No LIN communication possible	B
VSUP	7	Device is unpowered and will not function	B
INH	8	Will not be able to enable system power if used in this manner	B

Note

DRB package includes a thermal pad

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
RXD	1	EN	Device will go into sleep mode when a dominant bit is received on the LIN bus, disabling communication	B
EN	2	WAKE	Absolute maximum voltage on EN pin may be exceeded causing damage to EN pin	A
WAKE	3	TXD	Absolute maximum voltage on EN pin may be exceeded causing damage to TXD pin	A
GND	5	LIN	LIN biased dominant, no LIN communication possible	B
LIN	6	VSUP	LIN biased recessive, no LIN communication possible	B
VSUP	7	INH	INH biased high, will not be able to turn off system power if used in this manner	B

Note

The DRB package includes a thermal pad. There is a chance the thermal pad is soldered down and could short to any pin on device. What the thermal pad is soldered to determines the behavior. Example: if soldered to a ground plane then the adjacent pins would behave as if shorted to ground.

Table 4-5. Pin FMA for Device Pins Short-Circuited to VSUP supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
RXD	1	Absolute maximum voltage violation, transceiver may be damaged	A
EN	2	Absolute maximum voltage violation, transceiver may be damaged	A
WAKE	3	WAKE pin biased high and no local wake up possible	B
TXD	4	Absolute maximum voltage violation, transceiver may be damaged	A
GND	5	Device is unpowered and will not function	A
LIN	6	LIN biased recessive, no LIN communication possible	B
VSUP	7	None	D
INH	8	INH biased high, will not be able to turn off system power if used in this manner	B

Note

DRB package includes a thermal pad

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