

# TPS6292xx-Q1 Functional Safety FIT Rate and Pin FMA



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## 1 Overview

This document contains information for TPS6292xx-Q1 (SOT-583 package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

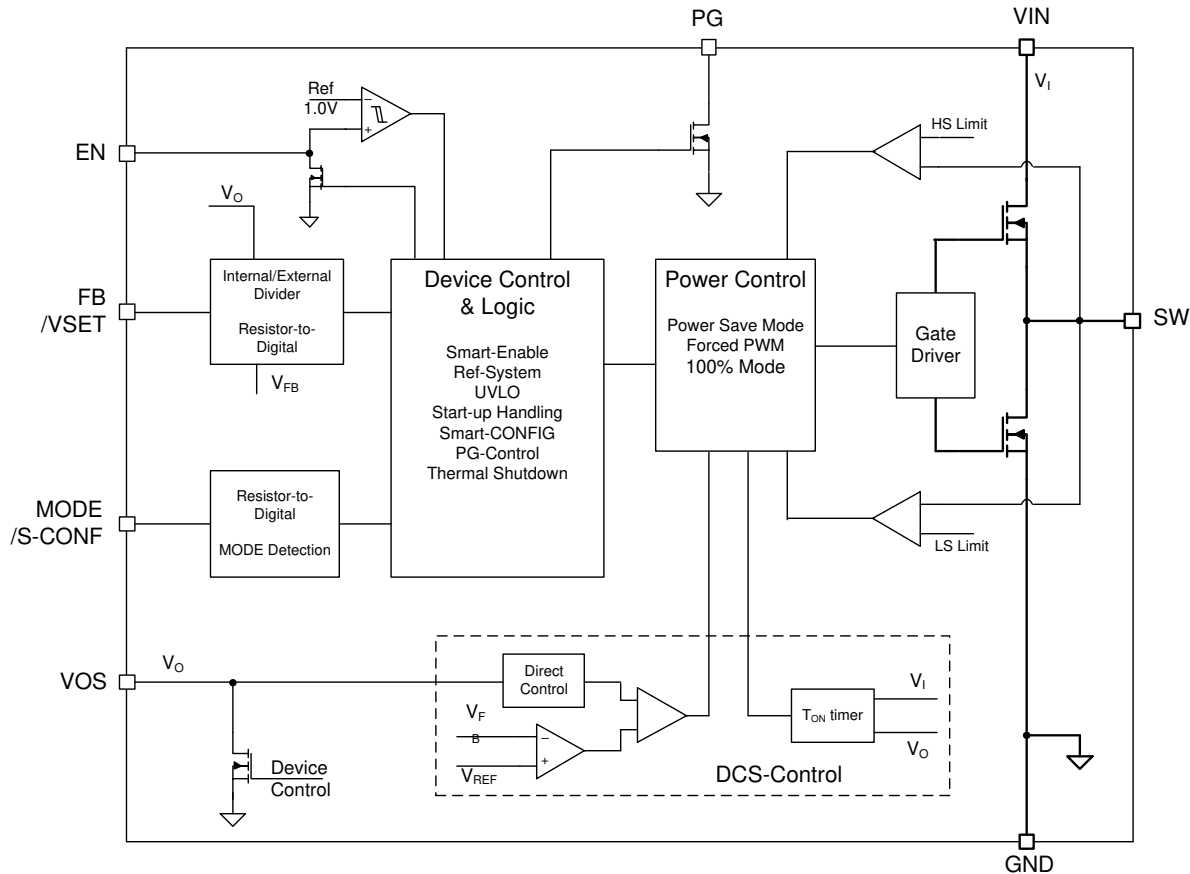


Figure 1-1. Functional Block Diagram

TPS6292xx-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

## 2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TPS6292xx-Q1 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 <sup>9</sup> Hours)
Total Component FIT Rate	5
Die FIT Rate	3
Package FIT Rate	2

The failure rate and mission profile information in [Table 2-1](#) comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Automotive Control
- Power dissipation: 400 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2T**

Table	Category	Reference FIT Rate	Reference Virtual T <sub>j</sub>
5	CMOS, BICMOS Digital, analog/ mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T<sub>j</sub> (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

### 3 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS6292xx-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

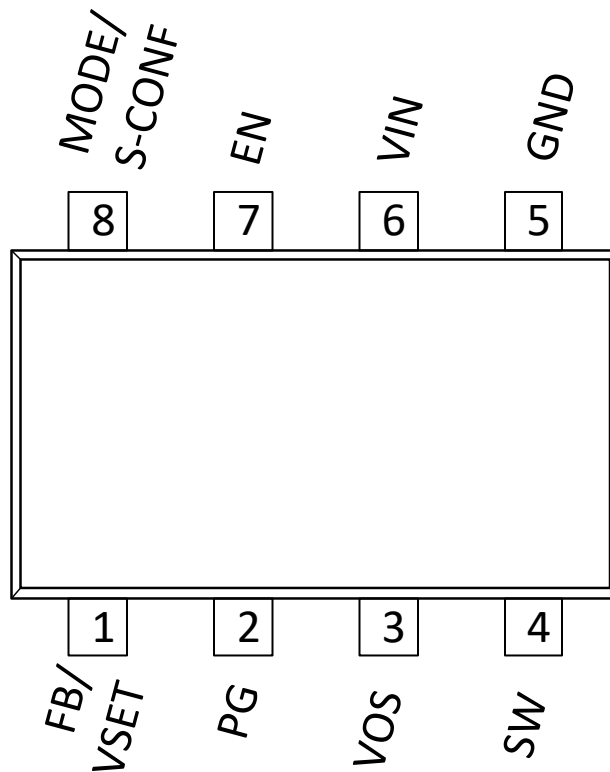
- Pin short-circuited to Ground (see [Table 3-2](#))
- Pin open-circuited (see [Table 3-3](#))
- Pin short-circuited to an adjacent pin (see [Table 3-4](#))
- Pin short-circuited to VIN (see [Table 3-5](#))

[Table 3-2](#) through [Table 3-5](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 3-1](#).

**Table 3-1. TI Classification of Failure Effects**

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

[Figure 3-1](#) shows the TPS6292xx-Q1 pin diagram. For a detailed description of the device pins please refer to the 'Pin Configuration and Functions' section in the TPS6292xx-Q1 datasheet.



**Figure 3-1. Pin Diagram**

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device is operating in one of the two typical application configurations show in [Figure 3-2](#) or [Figure 3-3](#).

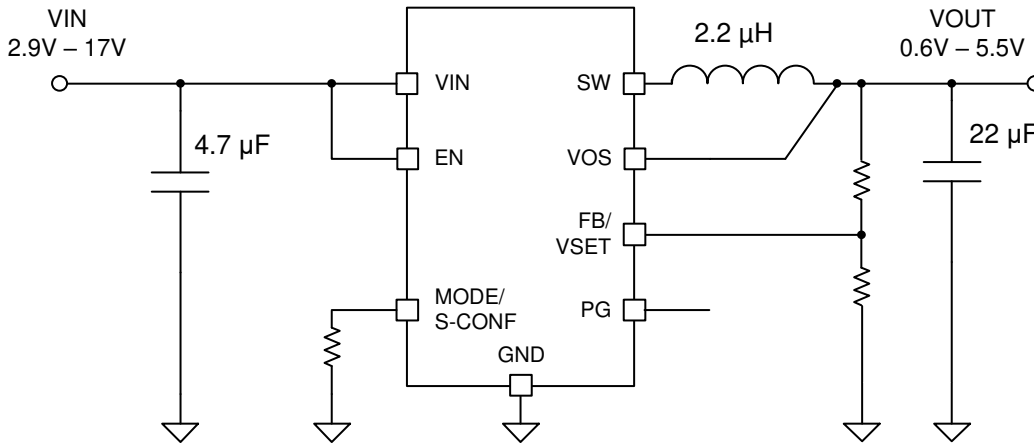


Figure 3-2. Adjustable  $V_O$  Operation Schematic

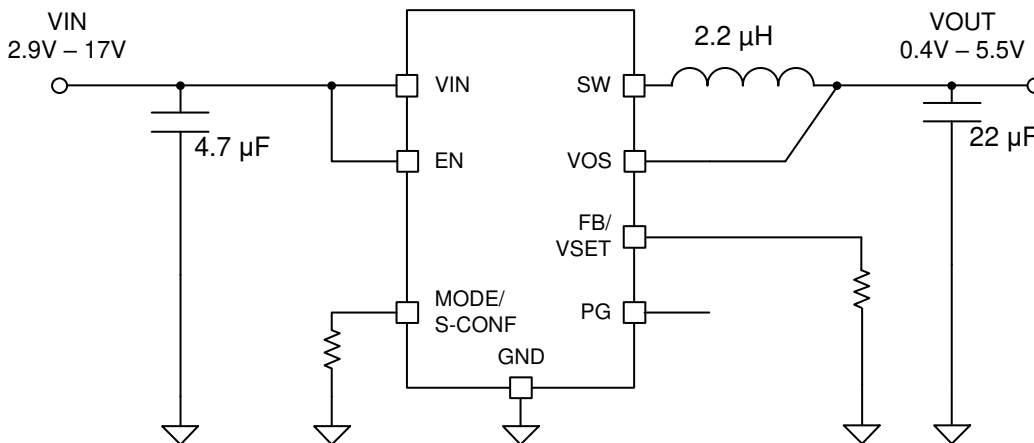


Figure 3-3. Set-able  $V_O$  Operation Schematic

Table 3-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Application Configuration	Description of Potential Failure Effect(s)	Failure Effect Class
FB/VSET	1	External FB <sup>(3)</sup>	Loss of output voltage regulation. Output voltage will go to $V_{in}$ . Possible device damage. <sup>(2)</sup> Abs Max voltage may be exceeded.	A
		Internal FB <sup>(4)</sup>	Device will regulate output voltage to 1.2V	D
PG	2		Loss of PG functionality	C
VOS	3		Loss of output voltage	B
SW	4		Possible device damage	A
GND	5		Intended pin connection	D
VIN	6		Device does not power on	B
EN	7		Device does not power on	B
MODE/S-CONF	8	External FB <sup>(3)</sup>	Part will run in 2.5MHz APFM with AEE mode <sup>(5)</sup>	C <sup>(5)</sup>
		Internal FB <sup>(4)</sup>	Loss of output voltage regulation. Output voltage will go to $V_{in}$ <sup>(5)</sup> . Possible device damage. <sup>(2)</sup> Abs Max voltage may be exceeded.	A <sup>(5)</sup>

**Table 3-3. Pin FMA for Device Pins Open-Circuited**

Pin Name	Pin No.	Application Configuration	Description of Potential Failure Effect(s)	Failure Effect Class
FB/VSET	1	External FB <sup>(3)</sup>	Loss of output voltage regulation. Output voltage may go to Vin Possible device damage. <sup>(2)</sup> Abs Max voltage may be exceeded.	A
		Internal FB <sup>(4)</sup>	Device will regulate output voltage to 3.3V	D
PG	2		Loss of PG functionality	C
VOS	3	External FB <sup>(3)</sup>	Open loop operation. Undetermined output voltage behavior	B
		Internal FB <sup>(4)</sup>	Loss of output voltage regulation. Output voltage may go to Vin Possible device damage. <sup>(2)</sup> Abs Max may be exceeded.	A
SW	4		Loss of output voltage regulation	B
GND	5		Potential device damage	A
VIN	6		Device does not power on	B
EN	7		Device does not power on	B
MODE/S-CONF	8	External FB <sup>(3)</sup>	Part will run in 2.5MHz APFM with AEE mode <sup>(5)</sup>	C <sup>(5)</sup>
		Internal FB <sup>(4)</sup>	Loss of output voltage regulation. Output voltage will go to Vin <sup>(5)</sup> Possible device damage. <sup>(2)</sup> Abs Max voltage may be exceeded.	A <sup>(5)</sup>

**Table 3-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

Pin Name	Pin No.	Shorted to	Application Configuration	Description of Potential Failure Effect(s)	Failure Effect Class
FB/VSET	1	PG		Loss of output voltage regulation. Possible device damage <sup>(1)</sup> . Abs Max voltage may be exceeded if PG is connected to Vin through a resistor.	A
PG	2	VOS		Loss of output voltage regulation. Possible device damage <sup>(1)</sup> . Abs Max voltage may be exceeded if PG is connected to Vin through a resistor.	A
VOS	3	SW		Loss of output voltage regulation. Possible device damage <sup>(1)</sup> . Abs Max voltage may be exceeded.	A
GND	5	VIN		Device not functional	B
VIN	6	EN		Device cannot be disabled	B
EN	7	MODE/S_CONF	External FB <sup>(3)</sup>	Part will run in 2.5MHz FPFM mode	C
			Internal FB <sup>(4)</sup>	Loss of output voltage regulation. Output voltage will go to Vin <sup>(5)</sup> Possible device damage. <sup>(2)</sup> Abs Max voltage may be exceeded.	A

**Table 3-5. Pin FMA for Device Pins Short-Circuited to VIN**

Pin Name	Pin No.	Application Configuration	Description of Potential Failure Effect(s)	Failure Effect Class
FB/VSET	1		Possible device damage <sup>(1)</sup> . Abs Max volatge may be exceeded.	A
PG	2		Potential device damage. Abs Max current rating for pin	A
VOS	3		Possible device damage <sup>(1)</sup> . Abs Max volatge may be exceeded.	A
SW	4		Possible device damage. <sup>(2)</sup> Abs Max voltage may be exceeded.	A
GND	5		Device not functional	B
VIN	6		Intended pin connection	D
EN	7		Device cannot be disabled	B
MODE/S-CONF	8	External FB <sup>(3)</sup>	Part will run in 2.5MHz FPFM mode <sup>(5)</sup>	C <sup>(5)</sup>
		Internal FB <sup>(4)</sup>	Loss of output voltage regulation. Output voltage will go to Vin <sup>(5)</sup> Possible device damage. <sup>(2)</sup> Abs Max voltage may be exceeded.	A <sup>(5)</sup>

- (1) Damage will occur if Vin is greater than the 6-V Absolute Maximum Rating for the pin
- (2) Damage will occur if Vin is greater than the 6-V Absolute Maximum Rating for the VOS pin.
- (3) Applies to a typical application schematic as show in [Figure 3-2](#)
- (4) Applies to a typical application schematic as show in [Figure 3-3](#)
- (5) Assumes Pin FMA condition occurs prior to device being enabled. If Pin FMA conditon occurs after device is operating, the part will continue operating as previously configured.

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