Functional Safety Information

LM63460-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for LM63460-Q1 (VQFN-FCRLF (22) package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

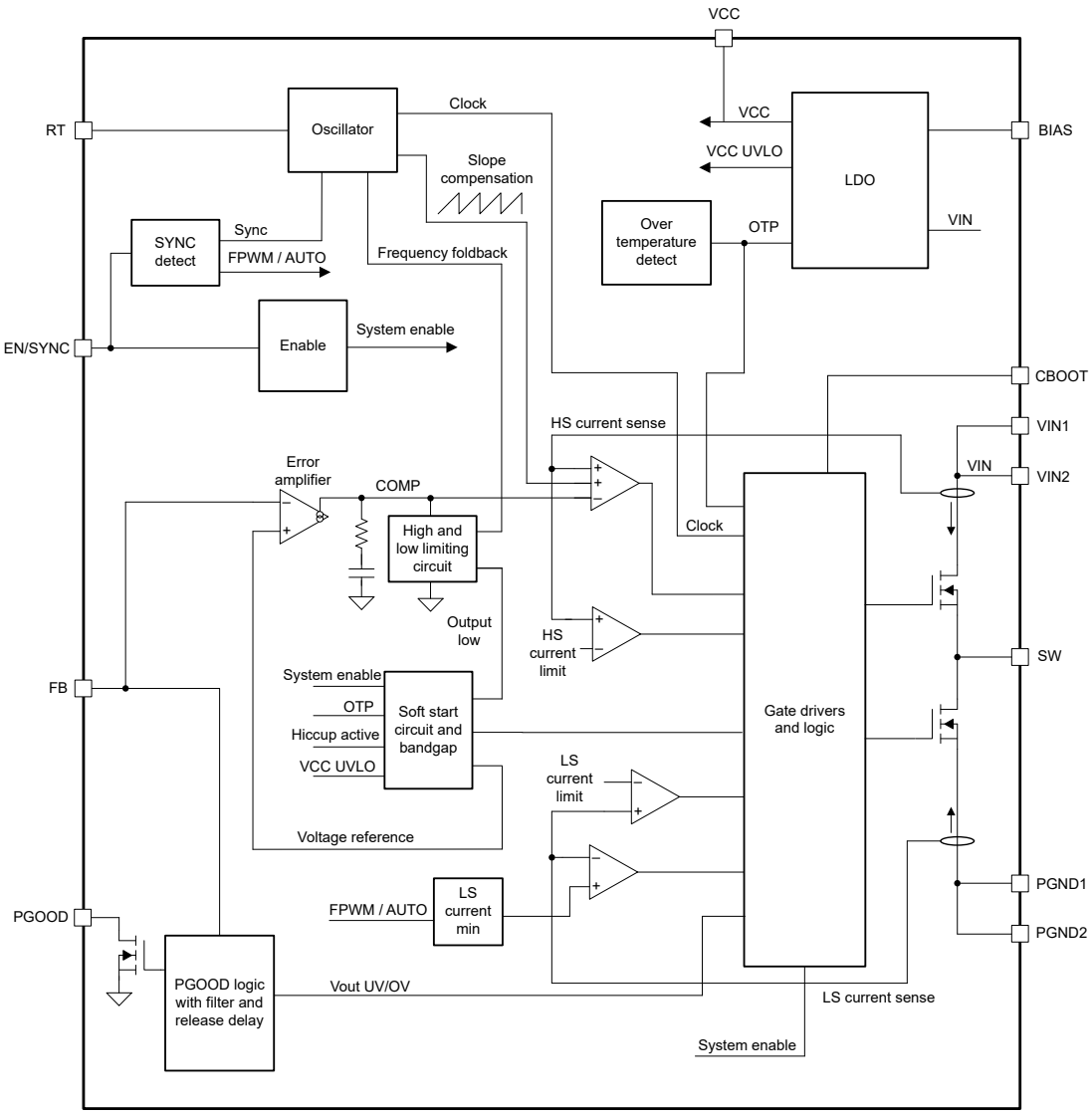

Figure 1-1. Functional Block Diagram

LM63460-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

ADVANCE INFORMATION for preproduction products; subject to change without notice.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for LM63460-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	16
Die FIT Rate	6
Package FIT Rate	10

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 700 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS / BiCMOS analog / mixed signal, less than 50 V supply	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the LM63460-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution
SW no output	45%
SW output not in specification – voltage or timing	40%
SW power FET stuck on	5%
PGOOD false trip, fails to trip	5%
Short circuit any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the LM63460-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the LM63460-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the LM63460-Q1 data sheet.

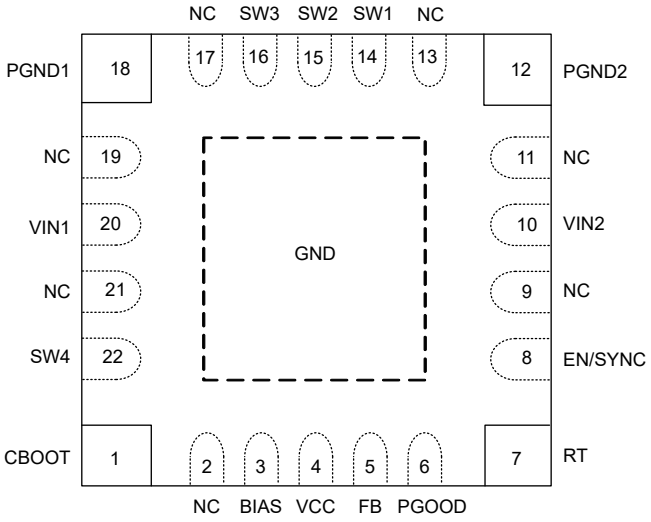

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Application circuit, as per the LM63460-Q1 data sheet is used.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
CBOOT	1	V_{OUT} = 0 V	B
NC	2	No effect	D
BIAS	3	Normal operation. Chip power now from VIN causes decreased efficiency.	C
VCC	4	V_{OUT} = 0 V	B
FB	5	V_{OUT} >> than programmed output voltage	B
PGOOD	6	PGOOD is not valid signal. No other changes to chip performance. V_{OUT} is in regulation.	C
RT	7	V_{OUT} = 0 V	B
EN/SYNC	8	V_{OUT} = 0 V	B
NC	9	No effect	D
VIN2	10	V_{OUT} = 0 V	B
NC	11	No effect	D
PGND2	12	No effect	D
NC	13	No effect	D
SW1	14	Damage to HS FET	A
SW2	15	Damage to HS FET	A
SW3	16	Damage to HS FET	A
NC	17	No effect	D
PGND1	18	No effect	D
NC	19	No effect	D
VIN1	20	V_{OUT} = 0 V	B
NC	21	No effect	D
SW4	22	Damage to HS FET	A
GND	DAP	No effect	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
CBOOT	1	V_{OUT} = 0 V	B
NC	2	No effect	D
BIAS	3	Normal operation. Chip power now from VIN causes decreased efficiency.	C
VCC	4	VCC output will be unstable and can increase above 5.5-V rating of the VCC pin.	A
FB	5	V_{OUT} >> than programmed output voltage	B
PGOOD	6	PGOOD is not valid signal. V_{OUT} is in regulation.	C
RT	7	V_{OUT} = 0 V	B
EN/SYNC	8	Unpredictable operation	B
NC	9	No effect	D
VIN2	10	V_{OUT} normal. Current loop will be affected, potentially affecting noise/jitter/EMI/ reliability.	C
NC	11	No effect	D
PGND2	12	V_{OUT} normal. Current loop will be affected, potentially affecting noise/jitter/EMI/ reliability.	C
NC	13	No effect	D
SW1	14	No effect. Two SW pins are sufficient.	D
SW2	15	No effect. Two SW pins are sufficient.	D
SW3	16	No effect. Two SW pins are sufficient.	D
NC	17	No effect	D
PGND1	18	V_{OUT} normal. Current loop will be affected, potentially affecting noise/jitter/EMI/ reliability.	C
NC	19	No effect	D

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VIN1	20	V_{OUT} normal. Current loop will be affected, potentially affecting noise/jitter/EMI/ reliability.	C
NC	21	No effect	D
SW4	22	V_{OUT} = 0 V, SW4 needed for CBOOT	B
GND	DAP	Load regulation is degraded and thermal impedance is impacted.	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
CBOOT	1	NC	No effect	D
NC	2	BIAS	No effect	D
BIAS	3	VCC	VCC ESD clamp damaged if BIAS > 5 V	A
VCC	4	FB	V_{OUT} = 0 V	B
FB	5	PGOOD	V_{OUT} can become >> than programmed output voltage	B
PGOOD	6	RT	V_{OUT} = 0 V	B
RT	7	EN/SYNC	V_{OUT} = 0 V	B
EN/SYNC	8	NC	No effect	D
NC	9	VIN2	No effect	D
VIN2	10	NC	No effect	D
NC	11	PGND2	No effect	D
PGND2	12	NC	No effect	D
NC	13	SW1	No effect	D
SW1	14	SW2	No effect	D
SW2	15	SW3	No effect	D
SW3	16	NC	No effect	D
NC	17	PGND1	No effect	D
PGND1	18	NC	No effect	D
NC	19	VIN1	No effect	D
VIN1	20	NC	No effect	D
NC	21	SW4	No effect	D
SW4	22	CBOOT	V_{OUT} = 0 V	B
GND	DAP	Any	Other pin is shorted to ground; see Table 4-2.	

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
CBOOT	1	VOUT = 0 V. CBOOT ESD clamp will run current to destruction.	A
NC	2	No effect	D
BIAS	3	If VIN exceeds 16 V, damage will occur. If VIN is below 16 V, normal operation	A
VCC	4	If VIN exceeds 5.5 V, damage will occur.	A
FB	5	V_{OUT} = 0 V	B
PGOOD	6	V_{OUT} = 0 V. PGOOD ESD clamp will run current to destruction.	A
RT	7	V_{OUT} = 0 V	B
EN/SYNC	8	V_{OUT} normal	D
NC	9	No effect	D
VIN2	10	No effect	D
NC	11	No effect	D
PGND2	12	V_{OUT} = 0 V	B
NC	13	No effect	D
SW1	14	Damage to LS FET	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SW2	15	Damage to LS FET	A
SW3	16	Damage to LS FET	A
NC	17	No effect	D
PGND1	18	V_{OUT} = 0 V	B
NC	19	No effect	D
VIN1	20	No effect	D
NC	21	No effect	D
SW4	22	Damage to LS FET	A
GND	DAP	V_{OUT} = 0 V	B

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265