Functional Safety Information

TPS1HTC30-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for the TPS1HTC30-Q1 (HTSSOP package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

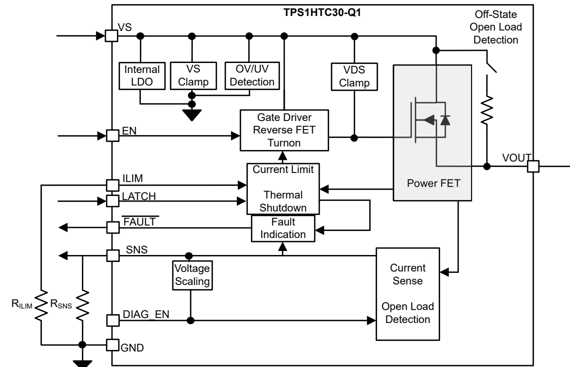

Figure 1-1. Functional Block Diagram

The TPS1HTC30-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

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2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TPS1HTC30-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	11
Die FIT rate	3
Package FIT rate	8

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 750 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS1HTC30-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT open (HiZ)	20
VOUT stuck on (VS)	10
VOUT functional, not in specification voltage or timing	50
Diagnostics not in specification	10
Protection function fails to trip	10

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4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS1HTC30-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VS (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TPS1HTC30-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS1HTC30-Q1 data sheet.

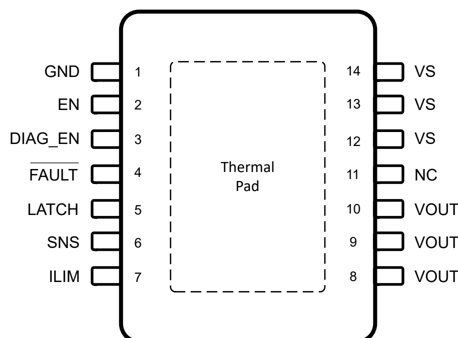

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Follows data sheet recommendation for operating conditions, external components selection, and PCB layout

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	Resistor, diode network is bypassed if present	B
EN	2	Shutdown of corresponding channel	B
DIAG_EN	3	Diagnostics are disabled	B
FAULT	4	Status being reported can be erroneous	B
LATCH	5	Device defaults to auto-retry mode when encountering thermal fault	B
SNS	6	Sense current not valid from SNS pin	B
ILIM	7	Device defaults to internal open current limit	C
NC	11	No effect	D
VOUT	8,9,10	Current limit of device engages	B
VS	12,13,14	Device has no input supply and therefore does not function	B

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Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	Loss of ground detection engages and device shuts off	B
EN	2	Corresponding channel is shutdown and EN is pulled down internally	B
DIAG_EN	3	Internally pulled down. Diagnostics are disabled.	B
$\overline{\text{FAULT}}$	4	Fault signal not reported	B
LATCH	13	Internally pulled down. Device defaults to auto-retry mode when encountering thermal fault	B
SNS	10	Version B only. Correct sense current cannot be read.	B
ILIM	11	Device defaults to internal current limit	C
NC	11	No effect	D
VOUT	8,9,10	No effect. If configured, open load detection triggers	B
VS	12,13,14	Device has no input supply and therefore does not function	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	EN	Channel is disabled	B
EN	2	DIAG_EN	EN signal affects DIAG_EN signal and vice versa	B
DIAG_EN	3	$\overline{\text{FAULT}}$	Fault reporting is erroneous. Diagnostics are enabled if $\overline{\text{FAULT}}$ is pulled high.	B
$\overline{\text{FAULT}}$	4	LATCH	Fault reporting is erroneous. Device is in auto-retry mode if $\overline{\text{FAULT}}$ is pulled high.	B
LATCH	5	SNS	Current sensing output is erroneous. Device is in auto-retry or latched off depending on the output of the SNS pin.	B
SNS	6	ILIM	Current limit and current sensing output is incorrect	B
VOUT	10	NC	No effect	D
NC	11	VS	No effect	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply (VS)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	Supply power is bypassed and device does not turn on	B
EN	2	Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell	A
DIAG_EN	3	Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell	A
$\overline{\text{FAULT}}$	4	Version B only. Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell.	A
LATCH	5	Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell	A
SNS	6	Version B only. Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell	A
ILIM	7	Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell	A
NC	11	No effect	D
VOUT	8,9,10	Output is pulled to supply voltage. Short-to-battery detection is triggered if configured.	B

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