Fact Sheet

Military Semiconductor Products

HIGHLIGHTS

The SMJ320C40 is the world's first digital signal processor (DSP) designed for parallel processing and represents the fourth generation of digital signal processors from Texas Instruments. The on-chip parallel processing capabilities of this DSP make the immense floating-point performance required by many applications achievable and cost effective.

PERFORMANCE

Released — 40 MHz (40 MFLOPS) / 5% power supply (GF, HFH, TAB packages & KGD)
— 50 MHz (50 MFLOPS) / 5% power supply (GF, HFH, TAB packages & KGD)
— 60 MHz (60 MFLOPS) / 5% power supply / -55°C to 100°C (GF, HFH, TAB packages)

Maximum Clock Cycle Time is 242.5 ns (4.1 MHz). This is necessary due to the use of dynamic nodes.

TECHNOLOGY

0.72 micron double metal EPIC™ G1ZSE CMOS

PACKAGING

GF — 325-pin ceramic staggered pin grid array, cavity down. Weight: 31 grams
$R_{\theta JA}$ — 15.6°C/W, $R_{\theta JC}$ — 2.3°C/W

HFH — 352-lead ceramic quad flat pack with 0.5 mm lead pitch. This cavity up package has a nonconductive tie bar (NCTB), gold finish leads. Weight: 30 grams
$R_{\theta JA}$ — 28.7°C/W, $R_{\theta JC}$ — 1.28°C/W

TAB — 324-pad JEDEC standard TAB frame (48 mm), polyimide encapsulant option, solder-dipped

KGD — Known Good Die are warranted to the datasheet at temperature and speed, and specifically suited to MCM applications. KGD has the same reliability level as a test and processed packaged part.

$R_{\theta JA}$.........Thermal resistance of a package without a path for heat dissipation. This is specified at a zero linear feet per minute air flow.

$R_{\theta JC}$.........Thermal resistance of a package assuming an infinite path for heat dissipation

DIE SIZE (Approximate)

496 x 480 active area

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SMD RELEASES MATRIX

Device Name	Package	Speed	DSCC SMD
SMJ320C40GFM40	325-pin staggered CPGA	40 MHz	5962-9466902QXA
SMJ320C40GFM50	325-pin staggered CPGA	50 MHz	5962-9466903QXA
SMJ320C40GFS60	325-pin staggered CPGA	60 MHz	5962-9466904QXA
SMJ320C40HFHM40	352-lead CQFP (NCTB)	40 MHz	5962-9466902QYC
SMJ320C40HFHM50	352-lead CQFP (NCTB)	50 MHz	5962-9466903QYC
SMJ320C40HFHS60	352-lead CQFP (NCTB)	60 MHz	5962-9466904QYC
SMJ320C40KGDM40CT	Known Good Die	40 MHz	5962-9466902Q9B
SMJ320C40KGDM50CT	Known Good Die	50 MHz	5962-9466903Q9B
SMJ320C40TABM40/10	325-lead OLB/ILB TAB frame	40 MHz	5962-9466902QUA
SMJ320C40TABM50/10	325-lead OLB/ILB TAB frame	50 MHz	5962-9466903QUA
SMJ320C40TABS60/10	325-lead OLB/ILB TAB frame	60 MHz	5962-9466904QUA

POWER DISSIPATION

S TEMP = -55°C to 100°C

Typical I_{CC}:	350 mA
Minimum I_{CC}:	130 mA
Reference:	"Calculation of TMS320C40 Power Dissipation Application Report" - Literature No. SPRA032

TEST VECTORS

The SMJ320C40 has >500,000 test vectors. The actual test vectors are TI proprietary information.

TOOLS SUPPORT

Part Number	Description
TMDS3240130PC	Code Composer Studio™ is the DSP industry's first fully integrated development environment (IDE) with DSP-specific functionality. With its familiar MS-Visual C++™ like environment, Code Composer lets you edit, build, debug, profile and manage projects from a single unified environment. Other unique features include graphical signal analysis, injection/extraction of data signals via file I/O, multi-processor debugging, automated testing and customization via a C-interpretive scripting language and much more. OS requirements = Windows™ / PC.
C4X-ADA-XX	Translates Ada source code into 320C3X assembly source code. OS requirements = UNIX™ & VMS Call (800) 477-8924, Ext. 5801
TDMS3243850-02	C3X/C4X PC Assembler/Linker—The assembler.converts assembly language to machine language. The linker combines object modules into a single executable object file, performs relocation and resolves external references. OS = Windows
TMDS3243855-02	C Compiler/Assembler/Linker—Translates C source code into 320C4X assembly source code and performs assembler/linker functions. OS = MS-DOS
TMDS324355508	C3X/4X UNIX C Compiler/Assembler/Linker. OS = UNIX

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TOOLS SUPPORT (continued)

TMDS3240640   UNIX OS Software debugger tool that simulates the operation of the 320C4X. Note: For Windows-based systems, the debugger function is provided in the Code Composer IDE.

TMDS3243551-09   SunOS™/OpenWin™ C4X UNIX Simulator. Note: For Windows-based systems, the simulator function is provided in the Code Composer IDE.

For 3rd-party C4X Emulators, Evaluation Modules/Starter Kits and DSP boards, please visit the following URL: http://dspvillage.ti.com/docs/third_parties/thirdpartyhome.jhtml

TAB

Tape Automated Bonding entails the attachment of a solder-dipped, rolled copper lead frame to the bond pads of the die. A TAB device offers the following advantages:

- *Increased test capability over non-packaged die options for improved hybrid yields*
- *Reduced weight*
- *Faster signal transfer due to lower package inductance and shorter lead length*
- *Dense packaging (high active silicon to overall size ratio)*

KGD

Known Good Die (KGD) options are offered for use in Multichip Modules and Chip-on-Board (COB) applications. The Temporary Wire Bond (TWB) is currently the verification technology used at TI to support KGD requirements for the TMP/SMJ320C40KGD.

- TWB

    Using the TWB technique, bond wires are attached to the bond pads using modified bonding parameters. This technique allows easy removal of the die after all needed 100% screens and parametric tests have been performed. The die is removed from the temporary package and shipped in a conventional die container. QML KGD devices produced using the TWB technology do not optically meet MIL-STD-883E (Method 2010, paragraph 3.1.1.1.h) metal bond pad visual inspection criterion due to the bond pad marks formed during bonding removal process. However, these devices have been reliably bonded using normal wire bond processes, and pass bond strength evaluation.

ARCHITECTURE

The SMJ320C40's high performance is achieved through the precision and wide dynamic range of the floating-point units, large on-chip memory, a high degree of parallelism and the six-channel DMA coprocessor.

INTERNAL.............. Two blocks of 1Kx32 dual access RAM. Each block can provide two accesses to
MEMORY the CPU or the DMA every cycle. A reserved block of dual access ROM
contains a boot loader.

CACHE.................. Four segments of 32 words each. Operates on the standard least-recently-used algorithm.

DMA..................... On-chip concurrent direct memory access controller. The separate program, data and DMA buses allow for parallel program fetches, data reads and writes, and DMA operations. For example: the CPU can access 2 data values in 1 RAM block and perform an external program fetch in parallel with the DMA coprocessor loading another RAM block, all within a single cycle.

COMMUNICATION.. Six communication ports allow for combined 120-Mbytes/sec (20-Mbytes or
PORTS 4-Mwords/sec per port) bidirectional data transfer operations at 40-ns cycle time. All data transfers are buffered.

DESIGN-IN SUPPORT

<u>TI has the most extensive DSP application support</u>

Product Information Center: (972) 644-5580 (For general information, availability, etc.)
DSP Developer's Village: <u>http://dspvillage.ti.com/docs/dspvillagehome.jhtml</u>
DSP Hotline (Technical questions): <u>http://www-k.ext.ti.com/cgi-bin/webcgi.exe?New,KB=dsp</u>
Military C4x DSP Info: <u>http://www.ti.com/sc/docs/products/military/processr/320c4x.htm</u>
Military DSP Info: <u>http://www.ti.com/sc/docs/products/military/processr/index.htm</u>

Product Information Center

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Military Products – <u>http://www.ti.com/sc/military</u>

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