Demo/Test Codec Systems With TLV320AIC20/21/24/25 EVM

Wendy X. Fang, PhD. — *High Performance Analog Group*

ABSTRACT

A demo/test system has been built as a simple example for using the TLV320AIC20/21/24/25 codecs. The hardware part of the system includes the 'AIC20/21/24/25 EVM boards, an AIC development interface board, and a TMS320C5402™ DSP DSK board. The C54xx software, in assembly and C, is implemented on the 'C5402 DSP. A 2-device/4-channel and a 6-device/12-channel codec system are presented in this application report. Project collateral discussed in this application report can be downloaded from the following URL: http://www.ti.com/lit/zip/SLAA153.

Contents

List of Figures

List of Tables

1 Introduction

By applying the 16-bit 26-ksps dual channel codecs, TLV320AIC20, TLV320AIC21, TLV320AIC24, or TLV320AIC25, this report developes a demo/test system that demonstrates and provides the following:

- The application example
- The basic functions
- The startup software code

TI's TMS320C5402 DSK, and the associated Code Composer Studio (CCS), are utilized as the development platform. The discussion and software/firmware code are applicable for systems that use these codecs and the C54xx interface.

2 Hardware System

The four codec devices addressed in this application report, TLV320AIC20, TLV320AIC21, TLV320AIC24, and TLV320AIC25, share the exact same core, with the differences only in the digital I/O power supply range and the name and number of the analog I/O ports. The differences are summarized in Table 1. For more details on these devices, refer to the corresponding data sheets [1], [2], [3], and [4] listed in the reference section.

Table 1. Summary of AIC20/21/24/25 Differences

DIFFERENCE	TLV320AIC20	TLV320AIC21	TLV320AIC24	TLV320AIC25
Digital I/O Power Supply	2.7 V – 3.6 Vdc	1.1 V – 3.6 Vdc	The same as 'AIC20	The same as 'AIC21
Analog Input Names	MICI+/MICI– LINEI+/LINEI– HNSI+/HNSI– HDSI+/HDSI– CIDI+/CIDI–	The same as 'AIC20	MICI+/MICI– INP1/INM1 INP2/INM2 INP3/INM3 INP4/INM4	The same as 'AIC24
Analog Output Names	LINEO+/LINEO– HNSO+/HNSO– HDSO+/HDSO– SPKO+/SPKO–	The same as 'AIC20	OUTP1/OUTM1 OUTP2/OUTM2 OUTP3/OUTM3	The same as 'AIC24
Number of Analog Output Ports	4	4	3	3

2.1 2-Device/4-Channel Cascade Operation

To build a 2-device/4-channel codec system, the following hardware boards are used for this application report:

- One TLV320AIC20/21/24/25 EVM board, which has two installed 'AIC20 devices
- One TLV320AIC development board, which provides the hardware interface between the Codecs and a DSK or EVM board, such as the 'C5402 DSK, 'C6201 EVM, 'C6211DSK, or 'C6711 DSK
- One TMS320C5402 DSK board (part# TMDS320005402)

Before these boards are connected to form a hardware system, there are some jumpers, straps, or switches that need to be set up on the boards. Such a procedure is called the hardware configuration. Table 2 through Table 5 lists the setting positions for the hardware configuration.

Table 2. Configuration of the AIC20/21/24/25 EVM Board

JUMPER NO.	POSITION	DESCRIPTION
W1	Installed	Connects 3.3-V analog drive power ground to AGND (vs disconnect of the drive ground to AGND)
W2	2~3	Connects the first channel FSD to the second channel's FS (vs connects the FSD to 1 or 0)
W3	Not Installed	(1~2: Connects the first channel FSD high and 2~3: Connects the first channel FSD low)
W4	1~2	Connects the first channel M/S high so that it is a master (vs connects the 1st channel M/S low)
W5	Installed	Connects analog and digital grounds together (vs separate analog and digital grounds on the board)

Table 3. Configuration of the AIC Development Platform Board

JUMPER NO.	POSITION	DESCRIPTION
W1	1~2	Codec EVM system power-up through DSK board (vs through an external power supply)
W2	1~2	MCLK source: DSP's CLKOUT (vs through the on-board 100-MHz oscillator)

Table 4. Configuration of the C5402 DSK Board DIP Switches

SWITCH NO.	NAME	ON/OFF	DESCRIPTION
1	JTAGSEL	OFF	Use external (e.g., XDS510PP emulator)
2	MP/MC	ON	At microcontroller mode
3	CLKMD3	ON	The CLKMD pins are set to 0 1 0, which sets the default DSP CPU clock frequency = 100 MHz (20 MHz × 5)
4	CLKMD2	OFF	
5	CLKMD1	ON	
6	DMSEL	OFF	External memory is onboard
7	USER 1	ON	User S/W defined (0)
8	USER 0	ON	User S/W defined (0)

NOTE: ON = 0 and OFF = 1

Table 5. Configuration of the C5402 DSK Board Straps

STRAP NAME	SETTING	DESCRIPTION
JP1	1 to 2	CPLD program via J1
JP2	2 to 3	Normal boot mode
JP3	2 to 3	Low-impedance output for speaker driver
JP4	Installed	125-mA DAA loop current

NOTE: All strap and jumper settings presented here are the manufacturer default settings.

After the hardware configuration, connect and build the system as shown in Figure 1.

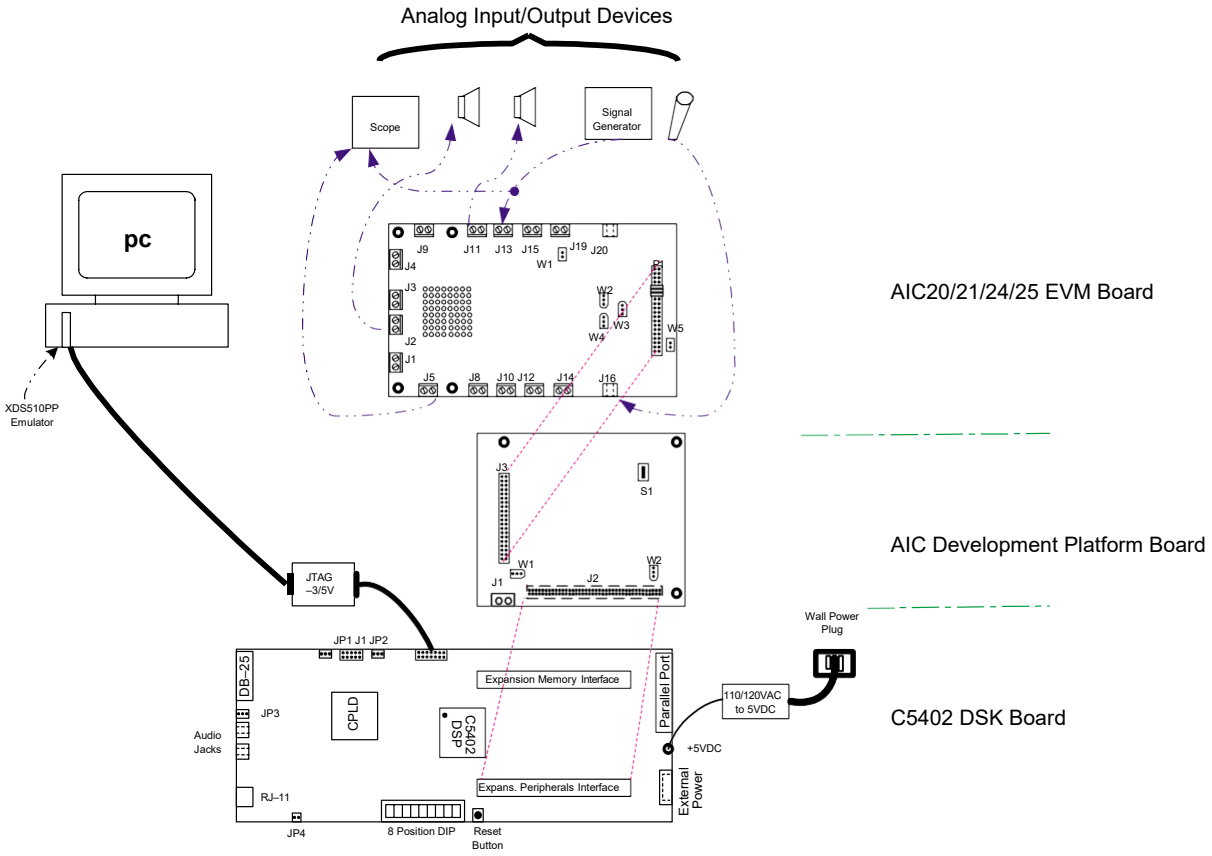


Figure 1. 2-Device/4-Channel AIC20/21/24/25 EVM System and Hardware Connections

Two additional connections are required:

- On the top of the AIC20/21/24/25 EVM board, three more jumpers need to be connected on the P1 connector:
  - Pin#9 with pin#10
  - Pin#11 with pin#12
  - Pin#13 with pin#14
- Some external analog input/output devices, such as a microphone, signal generator, speaker, and oscilloscope need to be connected to the system. Understanding that the actual input/output to a codec channel is programmable, the analog I/O connection in Figure 1 is based on the software configuration which is discussed in Chapter 3.

2.2 6-Device/12-Channel Cascade Operation

By adding two more codec EVM boards on top of the 4-channel system, a 6-device/12-channel EVM system is obtained. The additional hardware connections are shown in Figure 2.

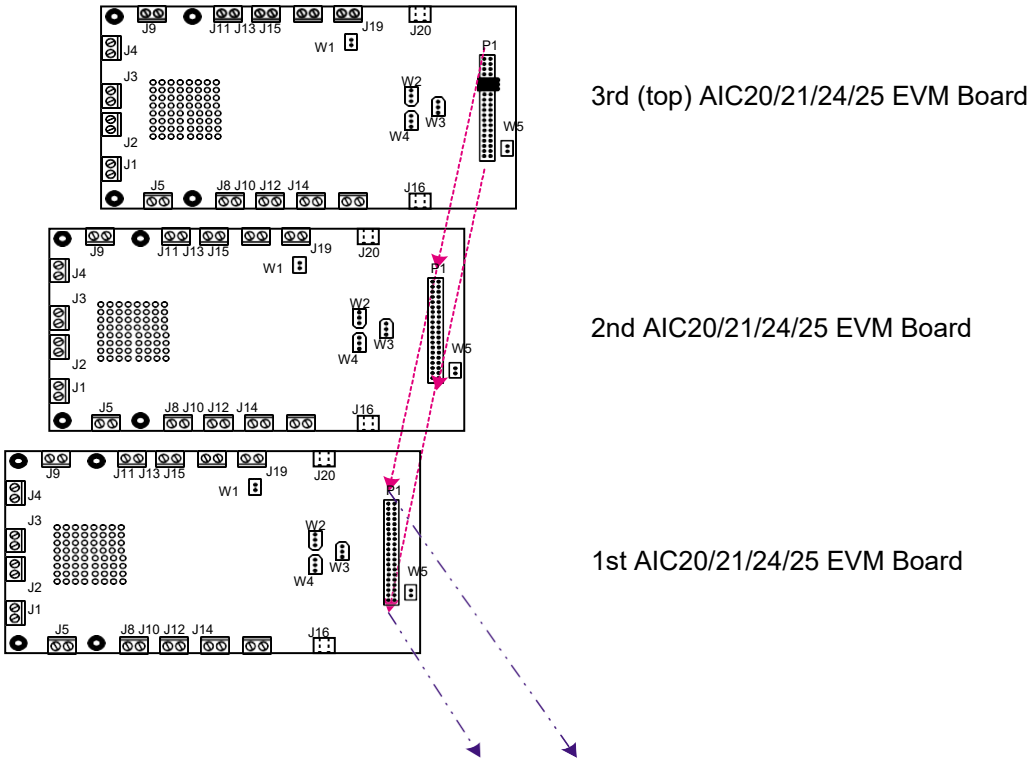


Figure 2. 6-Device/12-Channel System EVM Boards Connections

All discussions on the 4-channel system apply to the 12-channel system, with two additional AIC EVM boards configured. Table 6 lists the configuration of the two EVM boards. Note that all of the codec devices on the boards are in the slave mode.

Table 6. Configuration of the Slave AIC20/21/24/25 EVM Board

JUMPER #	POSITION	DESCRIPTION
W1	Not Installed	Disconnects 3.3-V analog drive power ground to AGND (the two grounds need to be connected only at one point on the first codec EVM board).
W2	2~3	Connects the first channel FSD to the second channel's FS
W3	Not Installed	Don't care
W4	1~2	Connects the first channel M/S low as a slave
W5	Installed	Disconnects analog and digital grounds (the two grounds need to be connected only at one point on the first codec EVM board).

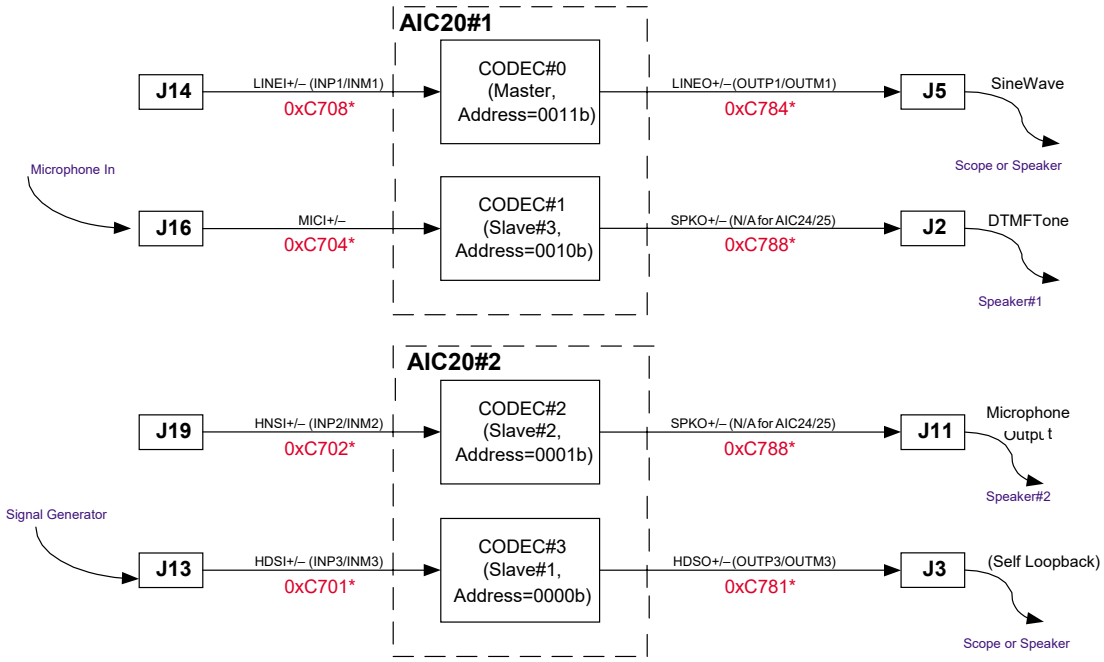
As stated in the previous section, the three jumpers on connector P1 should only appear on the top AIC20/21/24/25 EVM board. In this case, the three jumpers (of P1) on the first AIC EVM board have been removed and moved to P1 on the third (top) AIC EVM board.

3 Software Design

Software configuration sets up the ‘C54xx DSP (MMRs) and all of the codec channels’ control registers. For software configuration of the ‘C54xx DSP, and especially its McBSP(s), refer to reference [5] through reference [7]; and for the definition of the codec’s control registers, refer to references [1], [2], [3], or [4]. The files InitC5402.asm and InitAIC20.asm in the demo/test code package provide configuration examples for the DSP and the AIC20 codec and their interfaces, respectively.

Sample Frequency — As stated in the previous section, MCLK is supplied from the DSP’s CLKOUT. With the DSP’s maximum operating speed of 100 MHz, CLKOUT is set at 50 MHz. By setting M = 20, N = 5, P = 2 (50 M/16/M/N/P = 15625) in the demo/test code, the sample frequency is set to 15.625 KHz.

Analog Input/Output Selection — For each of the codec channels, there are five analog inputs and four (or three for AIC24/25) analog outputs that are accessible through the software configuration. Figure 3 illustrates the selected input/output for each of the codec channels.



* The hex code for configuring the corresponding codec control registers.

Figure 3. Selected Analog Inputs/Outputs of the AIC20/21/24/25 EVM

To test/demo the 2- or 6-AIC20/21/24/25 DSP/codec system though the proper external audio devices, such as a microphone, a speaker, or a scope, follow Figure 3 and connect these external devices to the system.

The actual code for the software configuration can be found in InitAIC20.asm. The complete demo/test software/firmware code can be downloaded from the TI website at:

www.ti.com

The file named AIC20SW_2C.zip is for two AIC20/21/24/25 cascade operation and the file named AIC20SW_6C.zip is for 6-device cascade operation.

4 Demo/Test Procedure

Perform the demo/test with the EVM system according to the following procedure:

1. Power OFF all equipment
2. Set the jumpers/switches on all three layers of boards (DSP, AIC development platform, and AIC20/21/24/25 EVM(s)). Refer to Table 2 through Table 6 of this application report for the positions.
3. Plug the three layers of boards together (note there is no keying between the AIC development platform, also called the AIC mother board, and the AIC20/21/24/25 EVM board connectors, and therefore special precautions are necessary for proper connections). Refer to Figure 1 and Figure 2 for the connections.
4. Connect the JTAG or the parallel cable to the DSK board.
5. Connect the microphone, signal generator, speakers, and scope probes to the system's analog connections, refer to Figure 1 and/or Figure 3.
6. Power up and boot up the PC.
7. At the PC, unzip the file AIC20SW_2C.zip for 2–device system or AIC20SW_6C.zip for a 6–device system and save to proper directories.
8. Connect the ac-to-dc power supply to the DSK board (refer to Figure 1), and power-up the whole EVM system. At the P1 connector at the top of the AIC EVM board, verify the following measurements:
   - 3.3-Vdc at Pins #25 and #27
   - 1.8-Vdc at Pins #29 and #31
   - 3.3-Vdc at Pins #33 and #35
   - 3.3-Vdc at Pins #37 and #39
   - Pins #2, #4, #6, #28, #30 and #32 are digital ground
   - Pins #34, #36, #38 and #40 are analog ground
9. Push the RESET button on the AIC development platform board, refer to Figure 1 for the location (S1), to hardware-reset all of the codecs.
10. Attach the scope's probes at the following test points on the AIC motherboard (development platform):
    - TP8: SCLK
    - TP9: FS (master FS)
    - TP10: DIN (Codec)/DX (DSP)
    - TP11: DOUT (Codec)/DR(DSP)

    And observe the power-up default digital interface conditions and verify the following:
    - FS frequency = MCLK/16/16/8/6 = 4096 Hz
    - SCLK Frequency = FS*16*(# of Codecs)*2 = 520.833 kHz
      (for a 2 AIC20/21/24/25 system — one EVM board)
      or = 1562.5 kHz
      (for a 6 AIC20/21/24/25 system — three EVM boards)

- No DIN since the DSP has not run yet
- A certain DOUT can be observed
- All signals sync to FS

11. At the PC, run CCS, load the *.out file, and run the program
12. The results:
    - You hear a DTMF tone from speaker#1 (J2) generated by the DSP — DTMFTone.c.
    - When talking into the microphone (J16), you hear speaker#2 (J11).
    - Probe J5 and you see a full-scale pure sine wave (about 244 Hz) generated by the DSP — SineGen.c.
    - Input a signal through the signal generator to J13. Observe and compare the original with the codec channel's entire hardware/software loop-back signals through the probes at J13 and J3.

5 References

1. TLV320AIC20, Low Power, Highly-Integrated Programmable 16-Bit 26-KSPS Dual Channel Codec, data manual (SLAS363A)
2. TLV320AIC21, Low Power, Low Voltage, 1.1 V to 3.6 V I/O, Highly-Integrated Programmable 16-Bit 26-KSPS Dual Channel Codec, data manual (SLAS365A)
3. TLV320AIC24, Low Power, Highly-Integrated Programmable 16-Bit 26-KSPS Dual Channel Codec, Data Manual (SLAS366A)
4. TLV320AIC25, Low Power, Low Voltage, 1.1 V to 3.6 V I/O, Highly-Integrated Programmable 16-Bit 26-KSPS Dual Channel Codec, data manual (SLAS367A)
5. TMS320VC5402 Fixed-Point Digital Signal Processor (SPRS079E)
6. TMS320C54x DSP CPU and Peripherals, Reference Set Volume 1 (SPRU131G)
7. TMS320C54x DSP Enhanced Peripherals, Reference Set Volume 5 (SPRU302)
8. TMS320C54x DSP Mnemonic Instruction Set, Reference Set Volume 2 (SPRU172C)
9. TMS320C54x Assembly Language Tools, User's Guide (SPRU102E)
10. TMS320C54x Optimizing C/C++ Compiler, User's Guide (SPRU103F)

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265