Application Report
SLAA690A–February 2016–Revised March 2017

SM72295 For Bi-Directional DC-to-DC Conversion

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ABSTRACT

To address ever tightening fuel economy demands the automotive industry is adopting two battery power systems to facilitate Stop-Start operation in which the internal combustion engine shuts down when stopped or coasting, and automatically restarts when power is applied. Typically a 12-V lead acid battery will be used to power many of the car's traditional systems, but a 48-V Lithium battery will be used to operate the starter. That same 48-V battery will provide a storage reservoir to capture regenerative braking or coast down energy.

This creates a need to move power bi-directionally between the two batteries depending on overall system needs.

This application report will address deploying the SM72295 in a 48:12 bidirectional charger.

Contents

1 SM72295 for 48:12 Bidirectional Charging

Although originally targeted at solar charging applications, the SM72295 has the key features which make it very attractive in a 48:12 bidirectional charger with full digital control:

- Dual high side current sense monitors for measuring inductor current and 48-V battery current
- Both transconductance output current monitor for reduced ground error or buffered monitor for lower drive impedance
- Dual 3-A high and low side gate drivers
- Hardware OVP with open drain logic output and which shuts down driver operation
- Independent high and low side gate driver control facilitates μC based dead time control

2 Example SM72295 48:12 Application

This application report is based on a two phase 48:12 bidirectional charger employing the SM72295 for gate drive & current monitoring, and an F28069 based C2000 controlSTICK for power supply control and monitoring. The design is available on the TIDesigns web site and complete eval board hardware is available to select customers.

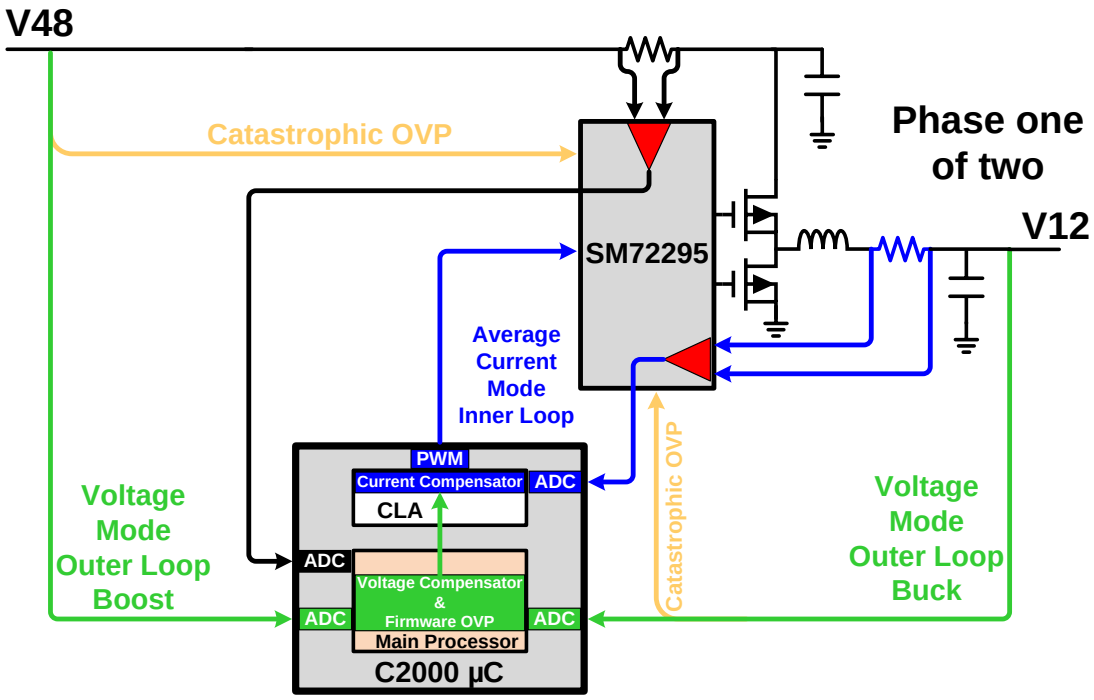

Figure 1. Simplified System Diagram

3 Design Choices

- Two phase interleave with automatic phase adding and shedding
- One SM72295 per phase
- Lead acid batteries

Two phases are enough to demonstrate the multi-phase approach without an excessively large board. The F28069 has adequate resources for expansion to 6-to-8 phases depending on design specifics.

Using one SM72295 per phase enables per phase 48-V and 12-V current sensing, and paralleling the gate drives for faster switching.

For practicality & economy while lab testing the 48-V side battery is assumed to be lead acid as well as the 12-V side.

4 Electrical Specifications

- 48-V power: 40 V to 60 V operating
- 12-V power: 10 V to 15 V operating
- 150-kHz operating frequency
- 28-A inductor current per phase

5 Control Scheme Strategy

This is a two-loop power supply with an average current mode control inner loop and a voltage mode outer loop. Both compensators were developed as continuous systems and converted to discrete time systems using MATLAB.

Cycle-by-cycle inner loop control is implemented in CLA tasks that trigger at ADC sample time which is mid bottom FET on time

The 1-kHz outer loop in implemented with the main processor. Outer loop sample time is an exact integer multiple of the inner loop time.

6 Inner Loop

The inner loop is a numerically programmable current source with 7.5-kHz BW Figure 2. Sample rate is cycle by cycle at 150 kHz with a single pole single zero discrete compensator which runs in the CLA. This loop always controls inductor current so is buck or boost agnostic. Positive numerical input results in buck operation and negative numerical input results in boost operation.

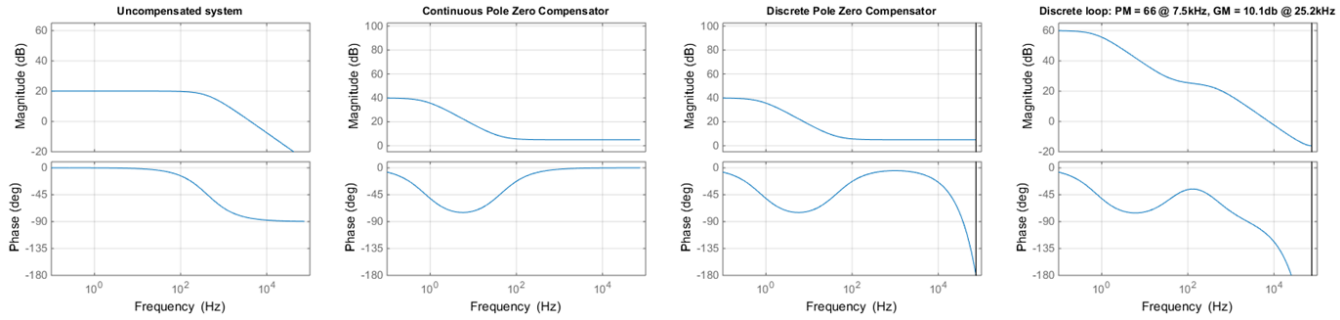

Figure 2. Inner Loop Compensator Simulation

Maximum loop gain is 60 db, with a single pole roll off starting at 764 mHz. The single zero is at 42 Hz, set with a proportional gain that can be used alone by commenting out a single line of CLA code for testing. In spite of the limited loop gain (60 db), the inner loop achieves excellent regulation by operating around a duty factor *zero* point of d =V12 / V48. This duty factor results in approximately zero current. A higher duty factor moves power from V48 to V12 (buck) and a lower duty factor moves power from V12 to V48 (boost). Maximum integrator magnitude is limited around this zero point to prevent excessive integrator wind up. Scaling and calibration correction is done in the outer loop to save CLA machine cycles. The regulation point passed to the CLA in ADC counts, with offsets and gain corrections included. Compensator coefficients are used which assume an error in ADC counts and an output in HRpwm counts. Zero point is also updated in the outer loop.

7 Outer Loop

The outer loop is for voltage mode control of battery float voltage. The sample rate is 1 kHz with a single pole compensator. It is designed with the assumption of a battery load at 12 V and 48 V:

- 1x Odyssey PC925 at 21.9 Ah for 12 V
- 4x Odyssey PC310 at 6 Ah for 48 V

It will work with other batteries, but if the capacity and/or ESR is significantly different that those batteries the compensator coefficients may need to be changed. Loop design assumes that the battery behaves like a huge capacitor with an ESR that leads to an ESR zero well below our desired crossover frequency. That is a significant simplification of the way a battery works, but it is accurate enough to close the loop of this compensator. As shown in Figure 3, the battery ESR zeros are predicted to be around 1mHz and the overall loop crossover is set to 10 mHz. The 1-kHz sample rate will easily support a higher crossover if desired.

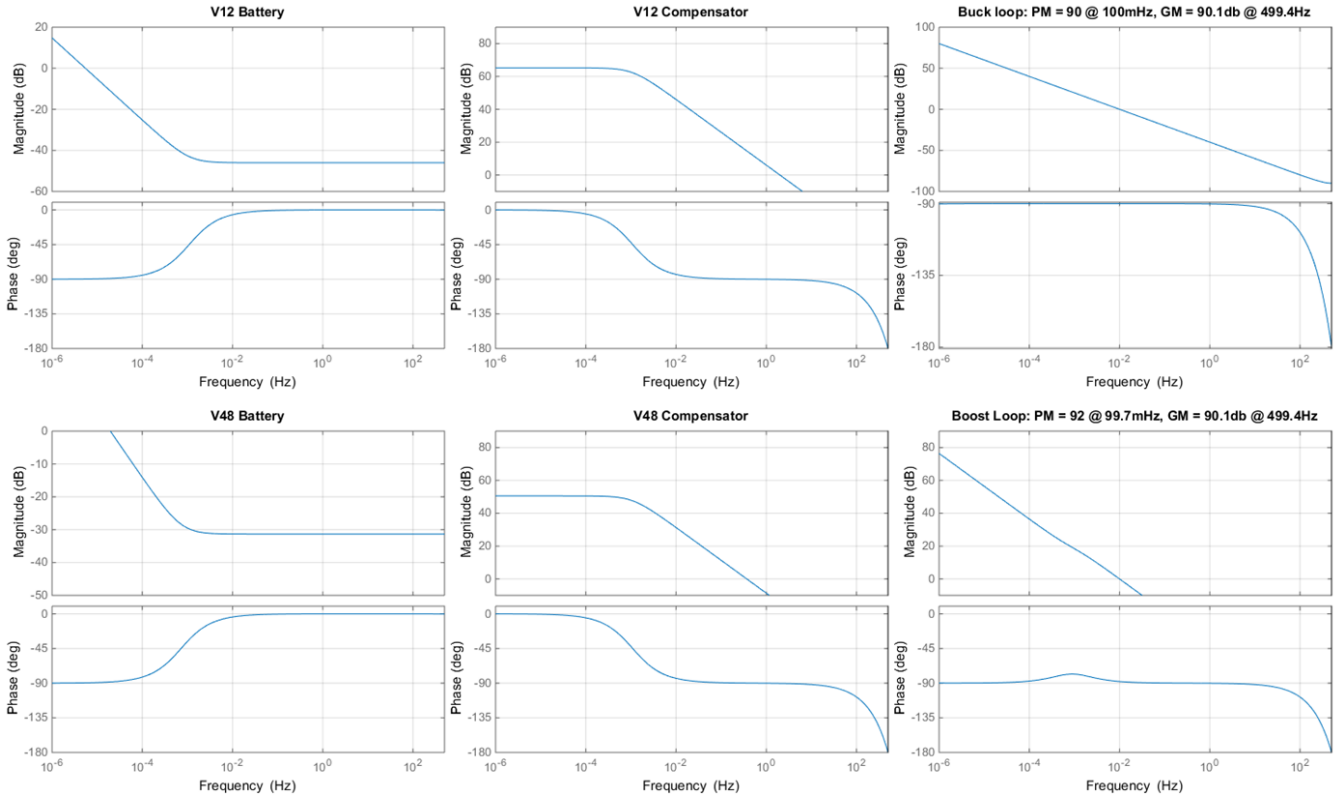

Figure 3. Outer Loop Compensator Simulation

Although the outer loop is designed for battery operation, the loop will close around a resistive load of low enough value cause the loop to cross over at less than about **100Hz**.

8 Inductor Current Sampling

Inductor current is sampled at the midpoint of the bottom FET on-time. By definition this is the average current, so an analog or digital averaging scheme is not required.

Figure 4 shows a plus full scale-to-minus full scale programmed current step.

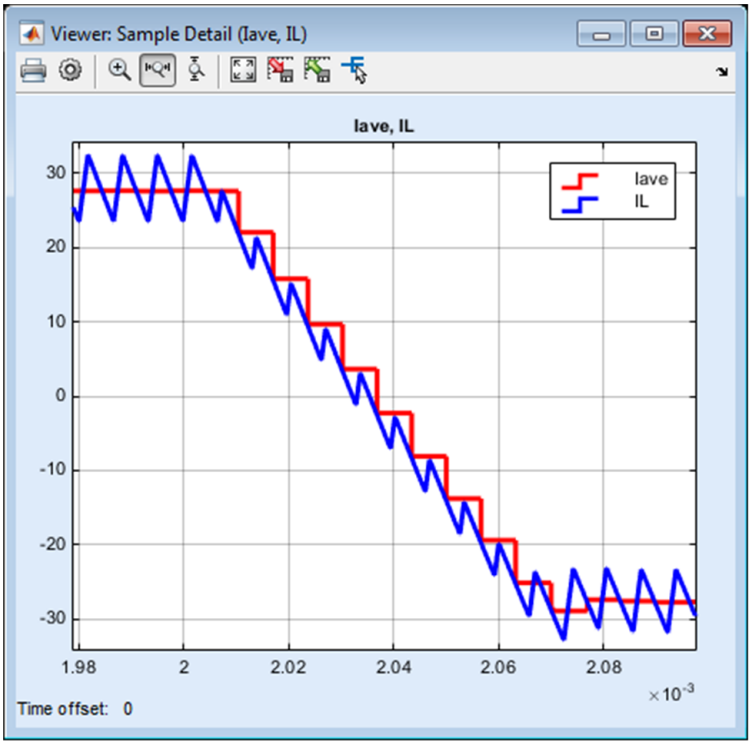

Figure 4. Current Sampling Simulation

The blue trace of Figure 4 is the inductor current waveform in a converter simulation. The red trace is the sampled value as seen by the control compensator. It is evident that bandwidth limiting of the waveform peaks and valleys is not a problem as long is the monitor waveform is accurate when it is sampled mid bottom FET on-time.

The 450-kHz BW of the SM72295 monitor circuitry causes a phase delay in the sampled waveform. That delay is corrected in firmware so that the same point is properly positioned in the sampled waveform. A symptom of mal positioned waveform is poor current accuracy at different line and/or load voltages. This is because once you move away from the bottom FET on time center point, which is average current, the value is influenced by the peaks and valleys which change with voltage.

9 SM72295 Current Sensing

At the core of the sensing circuit is a closed loop transconductance amplifier Figure 5. The loop is closed when the voltage drop across RIN1 is equal to the voltage drop across RSENSE. Current in ROUT equals current in RIN1 so the gain reflected to the voltage across RSENSE is ROUT ÷ RIN1.

The –3-db bandwidth of the circuit working together is about 450 kHz. That is adequate for average current mode operation with inductor current sensing at 150 kHz and probably a little higher. Phase delay caused by the limited BW is later corrected by a firmware setting.

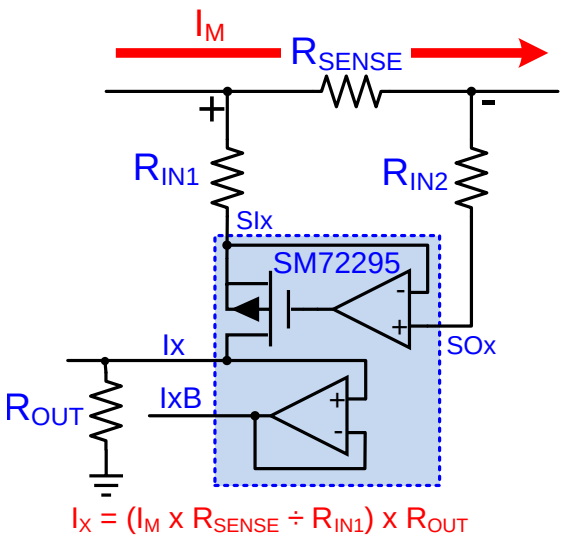

Figure 5. Simplified Current Sense Circuit

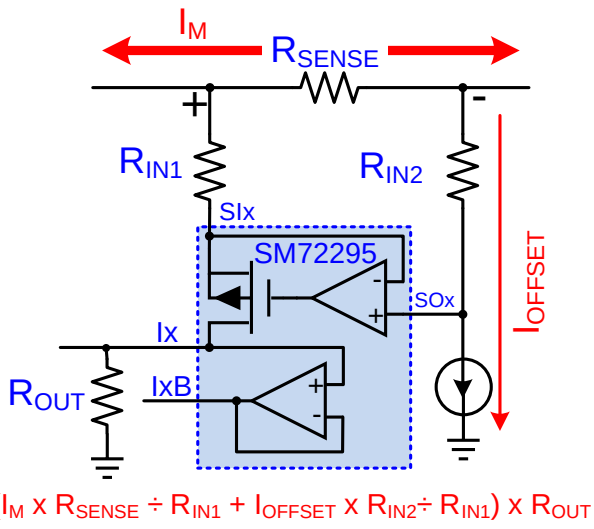

Figure 6. Offset Added for Bidirectional Operation

It is evident in Figure 5 that SM72295 current sensing is unidirectional. However, it can easily be coaxed into bidirectional operation with a simple circuit to add a current offset.

10 Bidirectional Operation

Since the Ix outputs cannot go negative, the SM72295 is limited to unidirectional current monitoring in normal configuration. However, by raising the zero current voltage at Ix Figure 5 to about half of the ADC operating range it is possible to monitor positive or negative currents and then correct for the offset in code.

This is accomplished by introducing a DC offset to the circuit as show in Figure 6. This modification allows the circuit to operate around an offset zero point of about 1.65 V at Ix.

The simplest method of generating an offset current is a resistor to ground. As long as the voltage is known, the offset current is known. This works well, but voltage range at the RSENSE- node cuts into the available dynamic range of current sensing.

A preferred method is a constant current source as shown in Figure 6. The current need not be extremely accurate as long as it is stable over time and temperature. In the end, offsets are calibrated out of the measurements anyway.

11 Common Mode Rejection

With only a 450-kHz BW, the high frequency common mode rejection of the SM72295 is not very strong. Any high frequency common mode noise that shows up on the RSENSE resistor is likely to end up in the current monitor output in some fashion.

This problem can range from barely noticeable up to the point that the monitor is unusable.

For the IL monitor the filter solution begins with accurately canceling the ESL of the current sense resistor. This is done by making the RC time constant equal to the L/R time constant (refer to Figure 7 and Figure 8 show the progression to a filter which cancels RSENSE ESL and provides significant common mode low pass filtering.

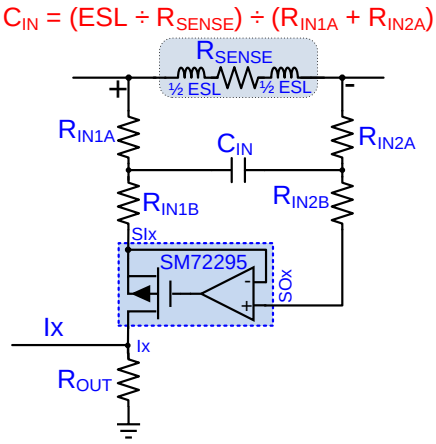

Figure 7. RSENSE Inductance Cancellation

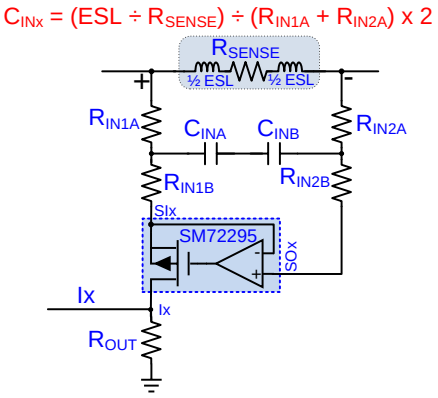

Figure 8. Splitting the Cap Does Not Affect ESL Cancellation

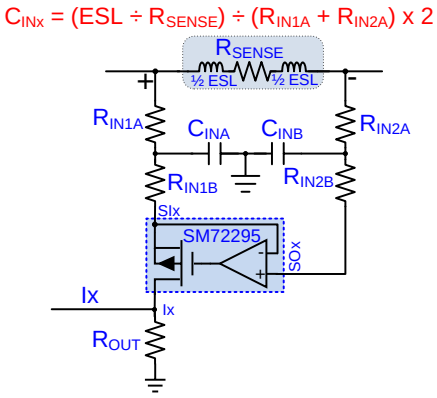

Figure 9. Center Grounded Does Not Affect ESL Cancellation, But Creates a Common Mode Filter

The effect on the waveform and overall accuracy is significant and evident in the simulations of Figure 10, Figure 11 and Figure 12. In practice, the common mode noise can be so severe that the current waveform is unrecognizable.

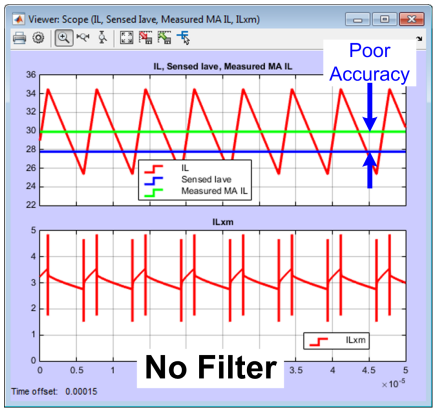

Figure 10. Unfiltered Showing ESL and Common Mode Effects

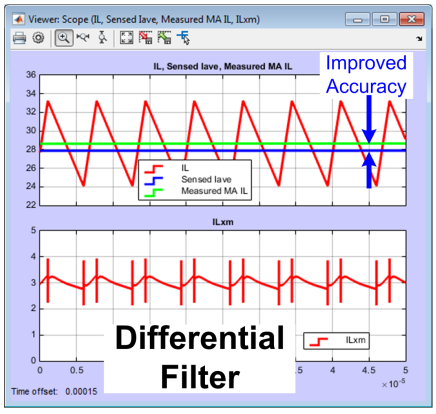

Figure 11. Differential Filter Only: Removes the ESL Effect, But the Common Mode Noise Remains

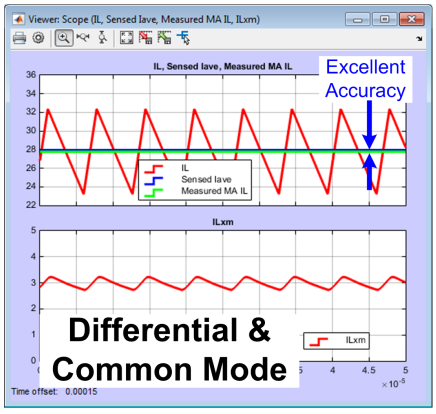

Figure 12. Differential & Common Mode Filter; ESL Effect and Common Mode Noise is Gone

Notice that it is not just wave shape affected. Accuracy of the control loop is improved dramatically with the filter. All three ILxm waveforms look like they are centered on the same voltage, and they are. Inner loop control is making that happen – it is a closed loop. The problem is that the ILxm waveforms have varying levels of accuracy in reproducing the original waveform (including DC level), all the way from very poor on the left, to very good on the right.

On the V48 side there is no need to preserve wave shape or bandwidth. A differential and common mode filter is still required, but the objective is simply to filter it to a DC like level.

12 Final Sensing Circuits

Figure 13 shows the final I48 and IL sensing circuits with current offset and filtering.

Both channels have some additional filtering in the output. On the IL side, this filter is set to 965 kHz and is intended to protect from noise pick up on the IL1m line. It has virtually no effect on the ILxm wave shape.

On the I48 side, the cutoff is 1.45 kHz. This is not only intended to prevent noise pickup, but also add additional filtering to remove ripple from the I48 current representation.

Bipolar transistor current sinks were chosen based on having very high current gain at the low currents of this application.

Offset current accuracy is fairly good, but any remaining error is calibrated out before use.

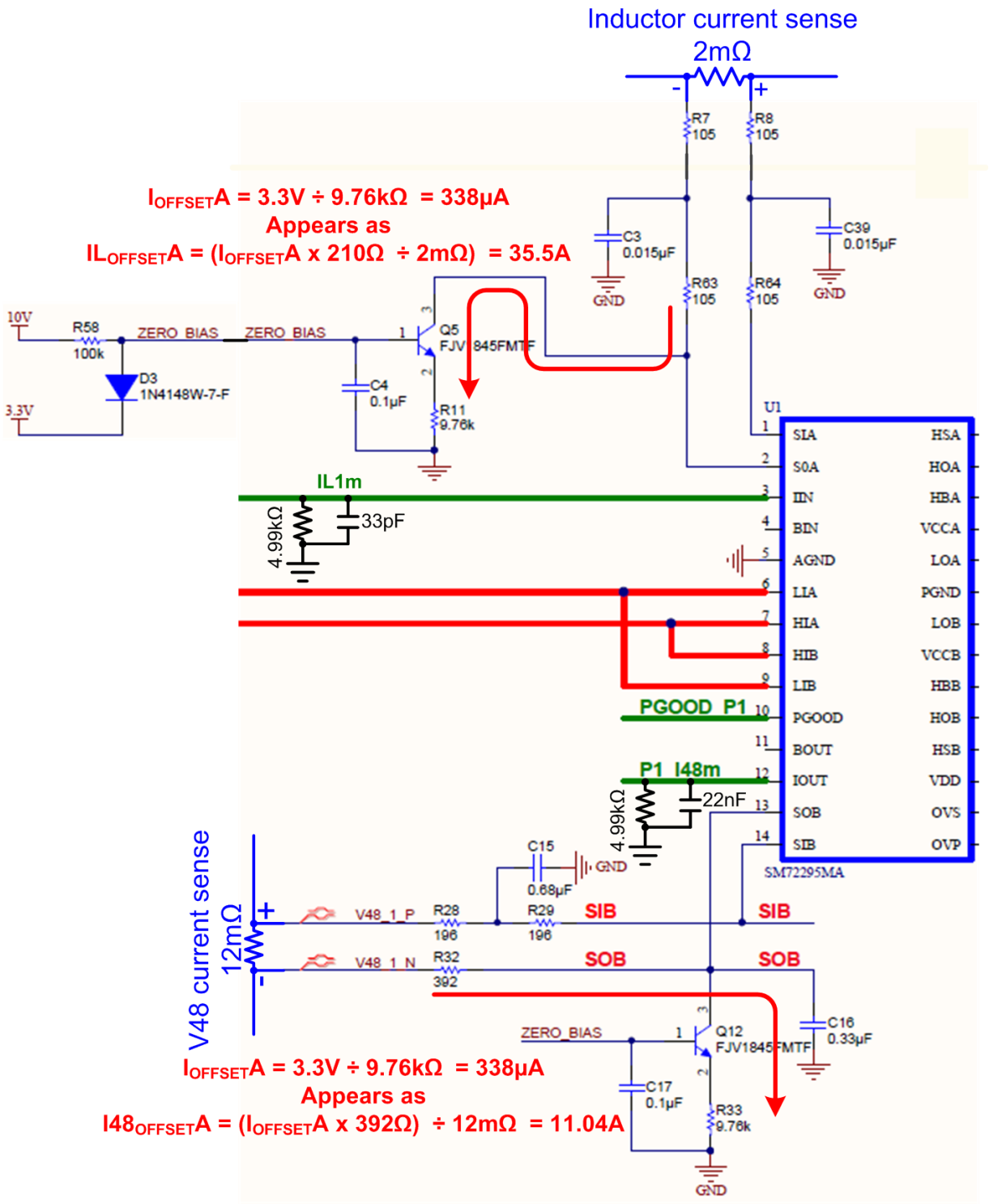

Figure 13. Final Current Sensing Circuits

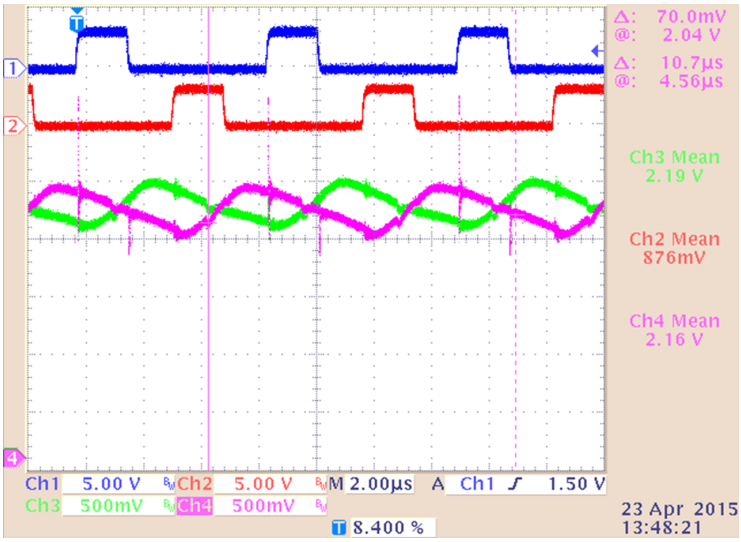

Figure 14. Actual ILxm Waveforms

13 Over Voltage Protection

In an automotive environment an open battery cable is not uncommon. This can be due to corrosion or a loose bolt caused by vibration. It is important to keep charger voltages under control in this circumstance. Primary overvoltage protection is through the intrinsic operation of the inner loop with its firmware boundaries.

Protection starts in the outer loop Figure 15 by limiting the range of HRPWM *zero"*calculation to the battery float voltage. If the battery rises above this voltage, the calculation continues to be done at the float voltage

```
// Limit PWM "zero" point calculation example in SM72295_OuterLoop.c
if ((PowerMode == BUCK) && (O_Loop.V12 > V12_FLOAT))
  CLA_Read_Variables.CMPA_HR_Zero_Sum += (HR_TBPRD - (V12_FLOAT / O_Loop.V48) * HR_TBPRD);      // Limit zero calculation to V12_FLOAT
else
  CLA_Read_Variables.CMPA_HR_Zero_Sum += (HR_TBPRD - (O_Loop.V12 / O_Loop.V48) * HR_TBPRD);    // Sum estimated loop center point

CLA_Read_Variables.CMPA_HR_Zero = CLA_Read_Variables.CMPA_HR_Zero_Sum / ZERO_MA_TAPS;          // Average loop center point for HRPWM
```

Figure 15. Example of Conditional *Zero* Calculation in the Outer Loop for Buck Operation

Over voltage protection is completed by the inner loop Figure 16 integrator limits. This applies a duty factor limit slightly above the duty factor which would result in the battery float voltage. The proportional term is not limited, but the additional duty factor cased by that is small.

In practice, the over voltage is limited to a couple of volts.

```
// CLA TASK (Inner loop - numerically programmable current source) in SM72295_CLA.cla
if (CLA_Read_Variables.UVL12)   // Under voltage error condition set in the CLA ISR
      EPwm1Regs.CMPA.all = HR_CMPA_12_UVL;  // PWM runs in non-sync buck mode. Happens startup and short circuit
else
{
   CLA_Write_Variables.IL1_Error = ADC_IL1 - CLA_Read_Variables.RawIset1;  // IL Error
   // Compensator pole
   CLA_Write_Variables.IL1_Integrator = I_NUM_RAW * CLA_Write_Variables.IL1_Error  + I_DEN_RAW * CLA_Write_Variables.IL1_Integrator ;

   //Impose integrator  limits to prevent wind up ****************************
   if (CLA_Write_Variables.IL1_Integrator > (HR_CONTROL_LIMIT))
        CLA_Write_Variables.IL1_Integrator  = HR_CONTROL_LIMIT;
   else if (CLA_Write_Variables.IL1_Integrator < (-HR_CONTROL_LIMIT))
      CLA_Write_Variables.IL1_Integrator  = -HR_CONTROL_LIMIT;
   //*************************************************************************

   // Set PWM pulse width, combining pole and proportional term (zero)
   EPwm1Regs.CMPA.all = (CLA_Read_Variables.CMPA_HR_Zero + CLA_Write_Variables.IL1_Integrator + CLA_Write_Variables.IL1_Error * I_P_RAW) ;
}
```

Figure 16. Integrator Limits in the Inner Loop

14 Catastrophic Over Voltage Protection

In case of a hardware malfunction, the over voltage condition may no longer be under processor control. In that case, the native over voltage protection of the SM72295 comes into play.

Each SM72295 has one OVP circuit which will shut down the IC if the set point is exceeded. In this application, there are two voltages which must be monitored: V48 & V12. Each SM72295 is designated to monitor one voltage.

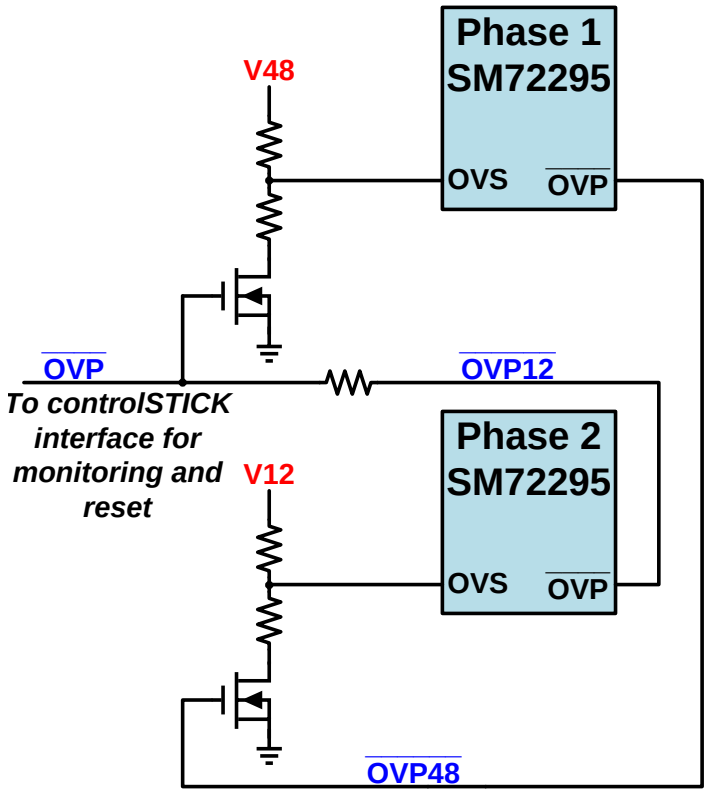

Figure 17. Catastrophic Over Voltage Protection Simplified Diagram

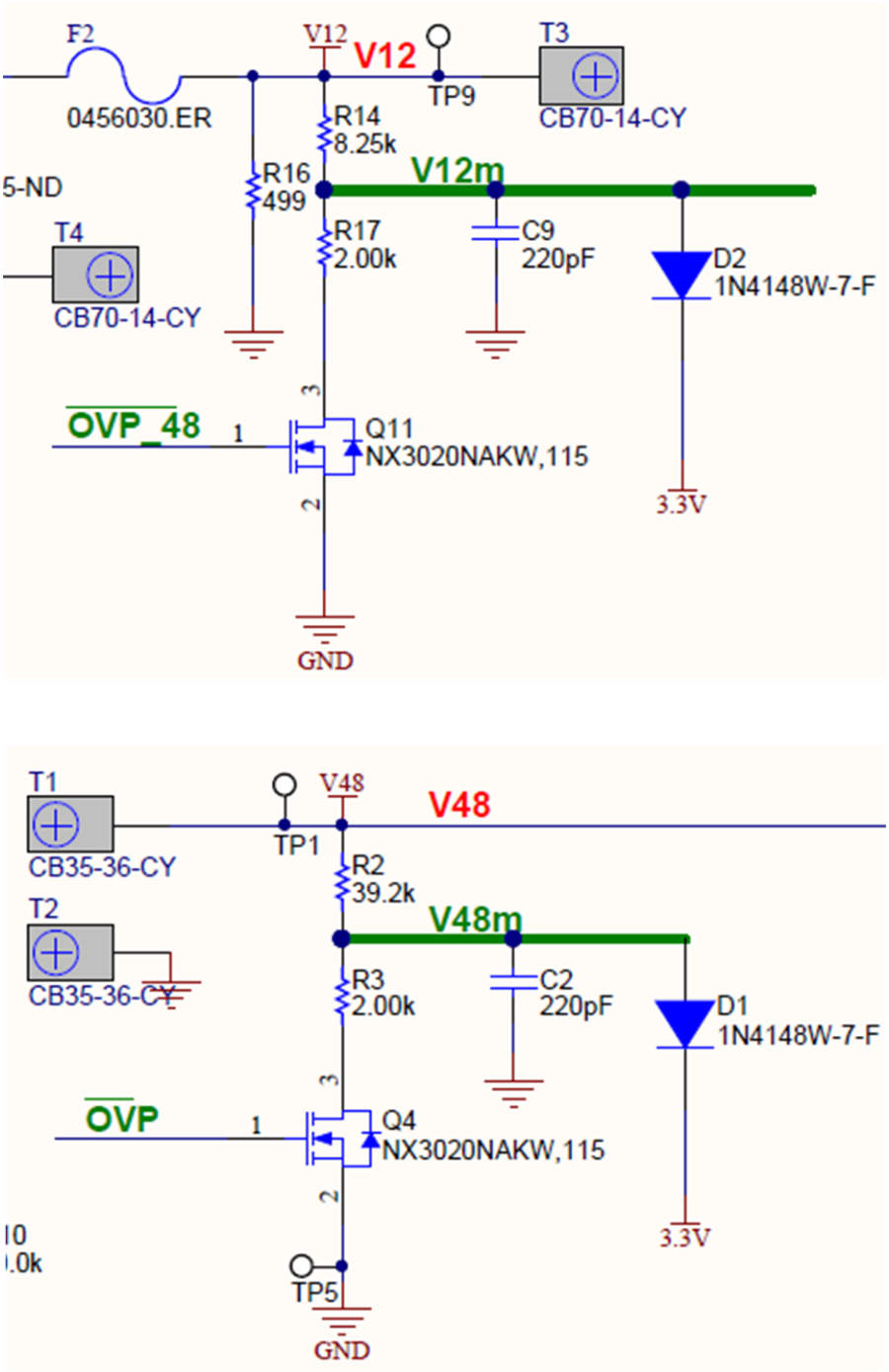

Figure 18. Catastrophic Over Voltage Protection Schematic Detail

However, it is desired that both SM72295 devices shut down if either one detects an over voltage. The circuit of Figure 17 is employed to make this happen. When one OVP is triggered, the voltage divider for the input of the other is opened, which also generates an OVP in that device. This cross coupling creates a hardware latch which once set, can only be reset by the C2000 μC.

Figure 18 provides a little more detail of how this is implemented and how the monitor lines (shared with ADCs) are protected from over voltage.

The assumption is that since a catastrophic OVP can only be caused by equipment failure, there is no need for normal operation to continue after generating one.

15 Complete Schematic

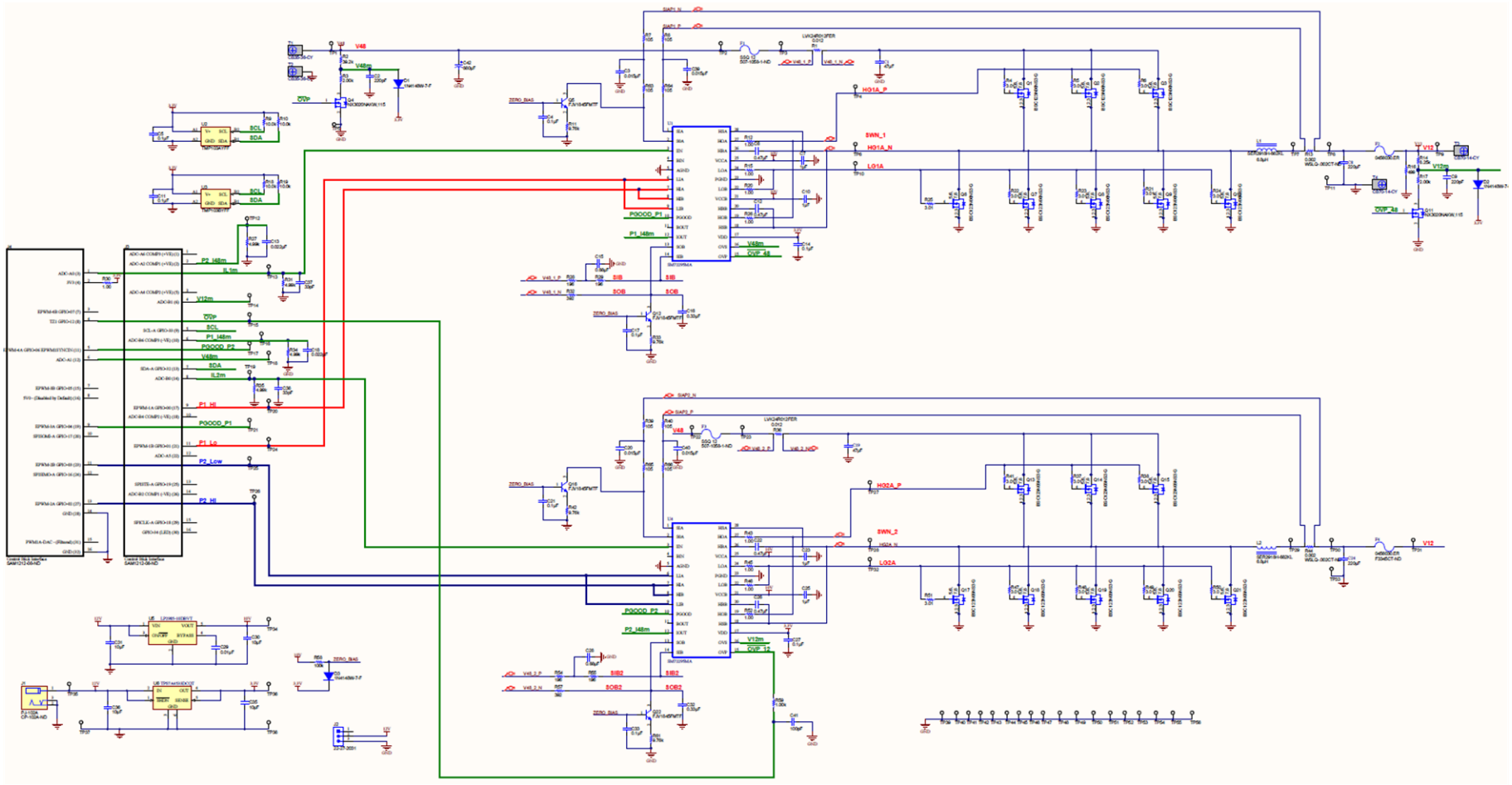

Figure 19. Overall Detailed Schematic Diagram

16 controlSTICK Interface

The controlSTICK attaches to the power supply circuit board via its 4x8 array of header pins. Since there are no commercially available mates to this, it requires two 2x8 header connectors on the PCB

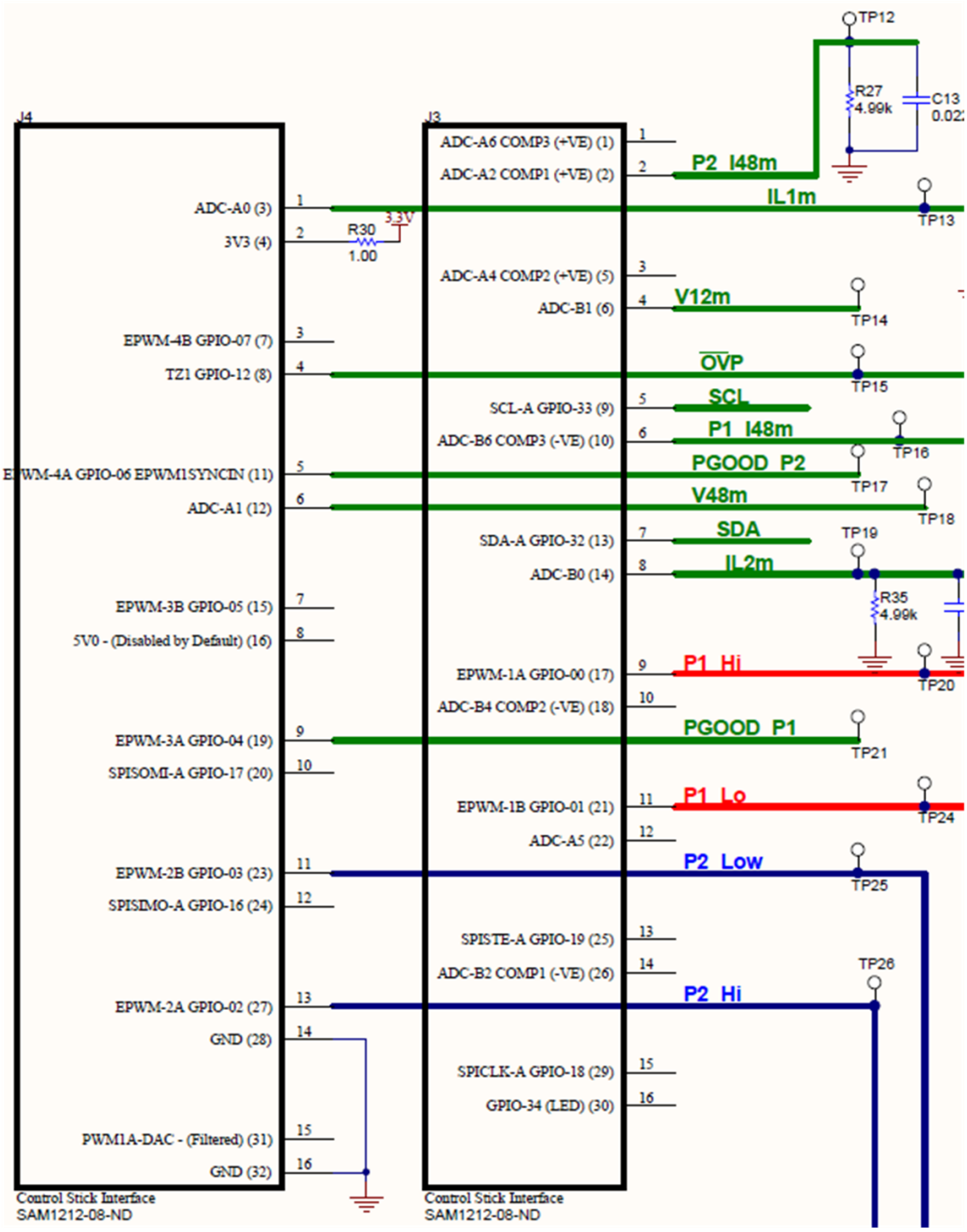

Figure 20. controlSTICK Interface Detail

P2_I48m – Phase 2 V48 current monitor

IL1m – Phase 1 inductor current monitor

V12m – V12 voltage monitor

OVP* – Catastrophic over voltage indicator and clear

SCL – I^2C for temperature sensing

P1_I48m – Phase 1 V48 current monitor

PGOOD_P2 – VDD good to phase 2 SM72295

V48m – V48 voltage monitor

SDA – I^2C for temperature sensing

IL2m – Phase 2 inductor current monitor

P1_Hi – Phase 1 high side PWM

PGOOD_P1 – VDD good to phase 1 SM72295

P1_Lo – Phase 1 low side PWM

P2_Low – Phase 2 low side PWM

P2_Hi – Phase 2 high side PWM

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (February 2016) to A Revision	Page
• Added Author's name to App Report.	1
• resized images and fixed page layout. no data changed.	2

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