Extending JESD204B Link Distance on Low Cost Substrates

ABSTRACT

This application report provides the foundation needed to select the circuit board material and optimize device settings for a JESD204B data link.

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1   Introduction

The goal of this document is to provide the necessary tools and knowledge so that designers can optimize their device settings and board-material choices to achieve good JESD204B link quality and optimal system cost. Ensure good link quality by choosing high end circuit board dielectric material, but this can significantly increase system cost. Good link quality can also be achieved by utilizing serial transmitter pre-emphasis and de-emphasis features in combination with receiver equalization to compensate for the high-frequency loss of lower-cost board materials. This application report evaluates both possibilities using several TI JESD204B evaluation boards, FMC link extender boards of various lengths and materials, and an FPGA link-quality evaluation tool. A successful JESD204B data link was achieved at 10 Gbit/sec over >16" of FR-4 type material.

2   JESD204B Interface

JESD204B links are the latest trend in data-converter digital interfaces. These links take advantage of high-speed serial-digital technology to offer many compelling benefits including improved channel densities and device synchronization. This application note addresses one of the challenges of adopting the new interface: The significantly higher link data rates can limit the link distance on "standard" FR4-type PCB materials. High performance PCB materials can be used to compensate, but they are significantly more expensive. This discusses how to evaluate link quality and illustrates one method of achieving extended transmission distances using standard technology PCB materials.

Understanding this discussion and evaluation will enable a system designer to do the following:

*   Evaluate link quality
*   Optimize transmitter pre-emphasis settings for best link quality
*   Choose appropriate PCB materials
*   Optimize system cost

JESD204B is a JEDEC standard for a high-speed serial data communication interface between data converters and logic devices (for example, FPGAs and DSPs). The JESD204B interface standard provides improvements for board area, FPGA and ASIC pin-count, and latency when compared to traditional LVDS and CMOS interfaces. TI's new generation of ADCs, DACs, clock ICs, and our array of development tools enable quick evaluation, design, and implementation of projects utilizing the JESD204B interface.

2.1   *Baseline Hardware Configuration*

This section will describe the baseline hardware configuration of the ADC12J4000EVM data transmitter plus the TSW14J56EVM data receiver. The ADC12J4000 is a 12-bit, 4-gigasample/second analog-to-digital converter with a JESD204B data interface that operates with one to eight lanes and from 1 to 10 Gbit/second depending on device configuration. The ADC12J4000EVM is a tool used to study the functionality and performance of the ADC12J4000 device.
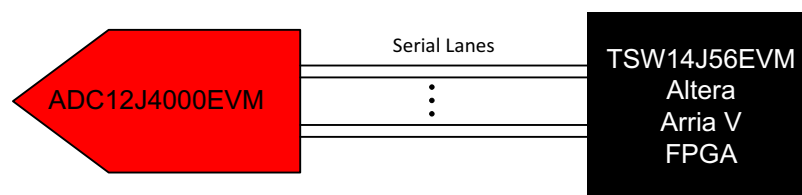
The TSW14J56EVM is a next-generation pattern generator and data-capture card used to evaluate the performance of the TI family of JESD204B high-speed analog-to-digital converters (ADC) and digital-to-analog converters (DAC). ADC or DAC EVMs are connected to the TSW14J56EVM using an FMC (FPGA mezzanine card) interface connection.

As shown in Table 1, the ADC12J4000EVM and TSW14J56EVM have the following signal path details in addition to the board-to-board connection:

Table 1. Baseline Board Signal Path Characteristics

Board	Distance (Inch)	Dielectric Type	Dk @ 10 GHz (Dielectric Constant)	Df @ 10 GHz (Dissipation Factor)
ADC12J4000EVM	4.46	Rogers RO4350B	3.48 ± 0.05	0.0037
TSW14J56EVM	2.61	Panasonic Megtron6 R5775(K)	3.61	0.004
Total length	7.07			

2.2 Link Extender Details

Six different link extenders were designed and fabricated. Three different trace lengths (4", 8", and 16") and two different material types were used to compare standard FR-4 type material to a high-frequency low-loss material. These extenders have male and female FMC connectors so they can connect between an ADC or DAC FMC mezzanine board and the TSW14J56 or other FMC carrier board.

One set of extenders was made of Isola 370HR. This material provides improved thermal performance and low expansion rates in comparison to traditional FR-4 while retaining FR-4 processing compatibility.

The other set of extenders were made of Rogers RO4350B laminate. This material provides tight control of dielectric constant and low energy loss while utilizing the same processing method as standard epoxy/glass.

The dissipation factor (also known as loss tangent) of the 370HR material is approximately 6.7 times higher than that of the RO4350B.

A summary of the extender details is below:

Table 2. Extender Board Signal Path Characteristics

Board	Pair Length (Inch)	Dielectric Type	Dk @ 10 GHz (Dielectric Constant)	Df @ 10 GHz (Dissipation Factor)
4-Inch_370HR	4	Isola 370HR	3.92	0.025
4-Inch_RO4350	4	Rogers RO4350B	3.48 ± 0.05	0.0037
8-Inch_370HR	8	Isola 370HR	3.92	0.025
8-Inch_RO4350	8	Rogers RO4350B	3.48 ± 0.05	0.0037
16-Inch_370HR	16	Isola 370HR	3.92	0.025
16-Inch_RO4350	16	Rogers RO4350B	3.48 ± 0.05	0.0037

3 ADC12J4000 Pre-Emphasis Feature

The ADC12J4000 device can output serial data in link configurations ranging from eight lanes at up to 8 Gbit/second to five or fewer lanes at rates up to 10 Gbit/second. Incorporated into the device is a configurable transmitter pre-emphasis feature to help ensure optimum data quality received under a variety of link conditions. The pre-emphasis feature provides increased emphasis of the higher frequency components in the output waveform to compensate for increased high-frequency attenuation caused by low-cost board dielectric materials and long link distances. The pre-emphasis feature is adjustable in 16 steps to provide flexibility in compensating for this high-frequency loss.

4 TSW14J56 and High Speed Data Converter (HSDC) Pro Eye Quality Analysis

The TSW14J56EVM utilizes an Altera® Arria®® V GZ FPGA device for the receive and transmit functions for the JESD204B link. One of the features of the Arria V GZ device is the On-Chip Signal Quality Monitoring Circuitry (EyeQ). The EyeQ feature is a debug and diagnosis tool that analyzes the received data by measuring the horizontal and vertical eye opening.

The EyeQ feature has been included in an internal development version of the Texas Instruments High Speed Data Converter Pro software. This software includes a menu sub-panel to control and utilize the TSW14J56 Arria V GZ EyeQ features and allow evaluation of link quality. For information on the availability of this software for customer use, contact us using the E2E High Speed Data Converters forum at the following link: https://e2e.ti.com/support/data_converters/high_speed_data_converters/f/68.

The software includes the following features:

• Lane – Selects one of the available lanes for the selected interface mode.
• Time per iteration – Selects how long data is accumulated before generation of the Eye diagram. Increasing this value also increases the Test Time proportionally.
• EQ DC Gain – Adjusts DC gain of FPGA receive hardware block
• EQ AC Gain – Adjusts AC gain of FPGA receive hardware block
• Display Standard Eye – Overlays one of the JESD204B receive eye-mask templates onto the Eye diagram.
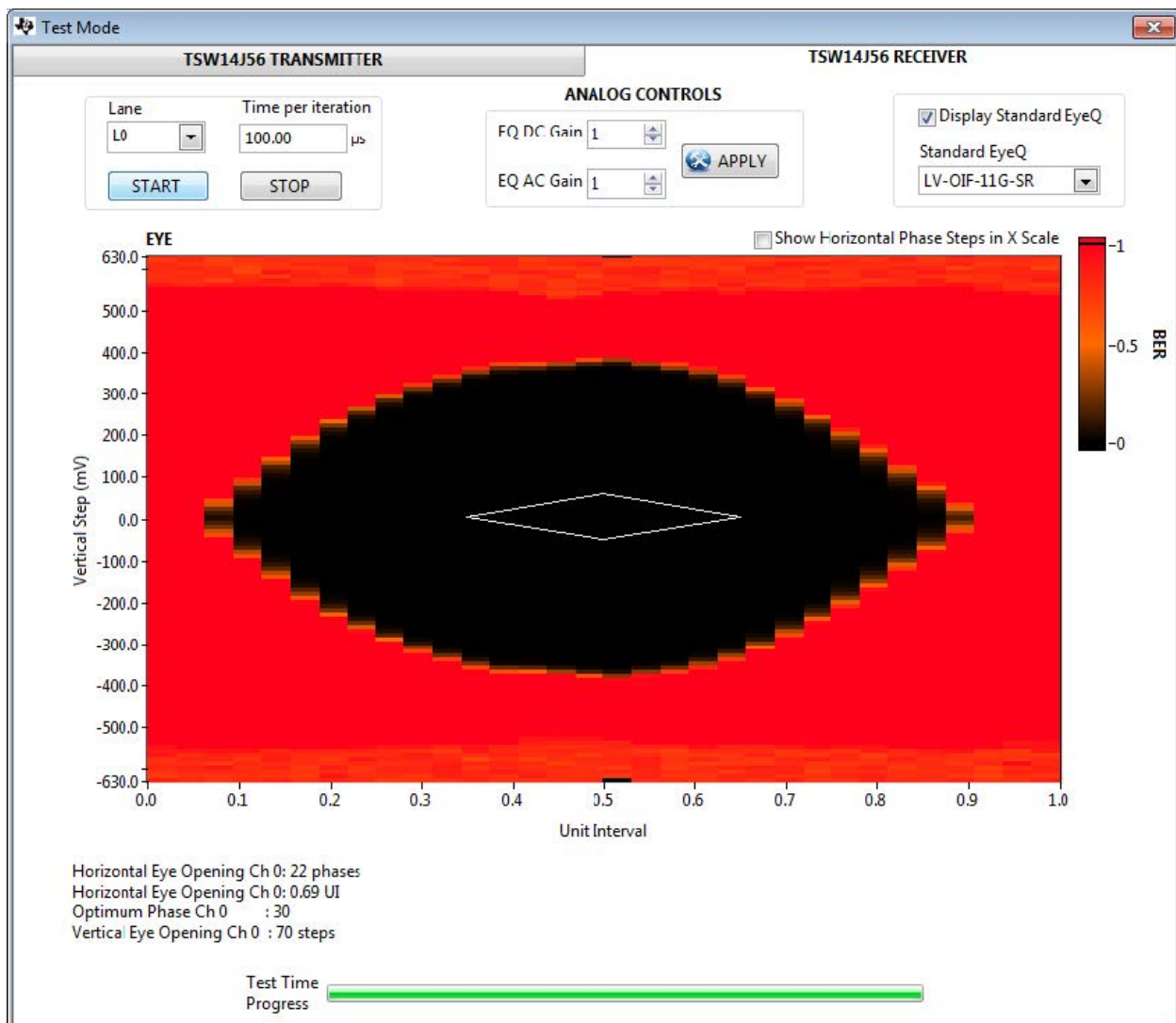
Figure 1. Example Eye Diagram Plot

5 Getting Started

Data is gathered at 8 Gbit/second and 10 Gbit/second line rates, which are the maximum rates available in the ADC12J4000 DDC bypass mode (eight active lanes) and decimate-by-4 DDRP mode (four active lanes). Data is gathered using Lane 0, which is active in both modes evaluated. The EyeQ test result readouts include the following reported parameters:

- Horizontal eye opening (Number of phase steps (0–31) and UI (0–1)
- Vertical eye opening (Number of vertical steps (0–128)

For ease of numerical comparison between the many eye diagrams gathered, the product of horizontal "phase steps" and vertical "steps" has been computed. This value has been termed "EyeProduct". The full summary of results in spreadsheet form and the complete set of EyeQ images is available upon request through the High Speed Data Converters E2E forum at the following link:https://e2e.ti.com/support/data_converters/high_speed_data_converters/f/68.

6 Summary of Results

With the baseline board setup (no extender), the eye quality was very good with even the minimum pre-emphasis setting.
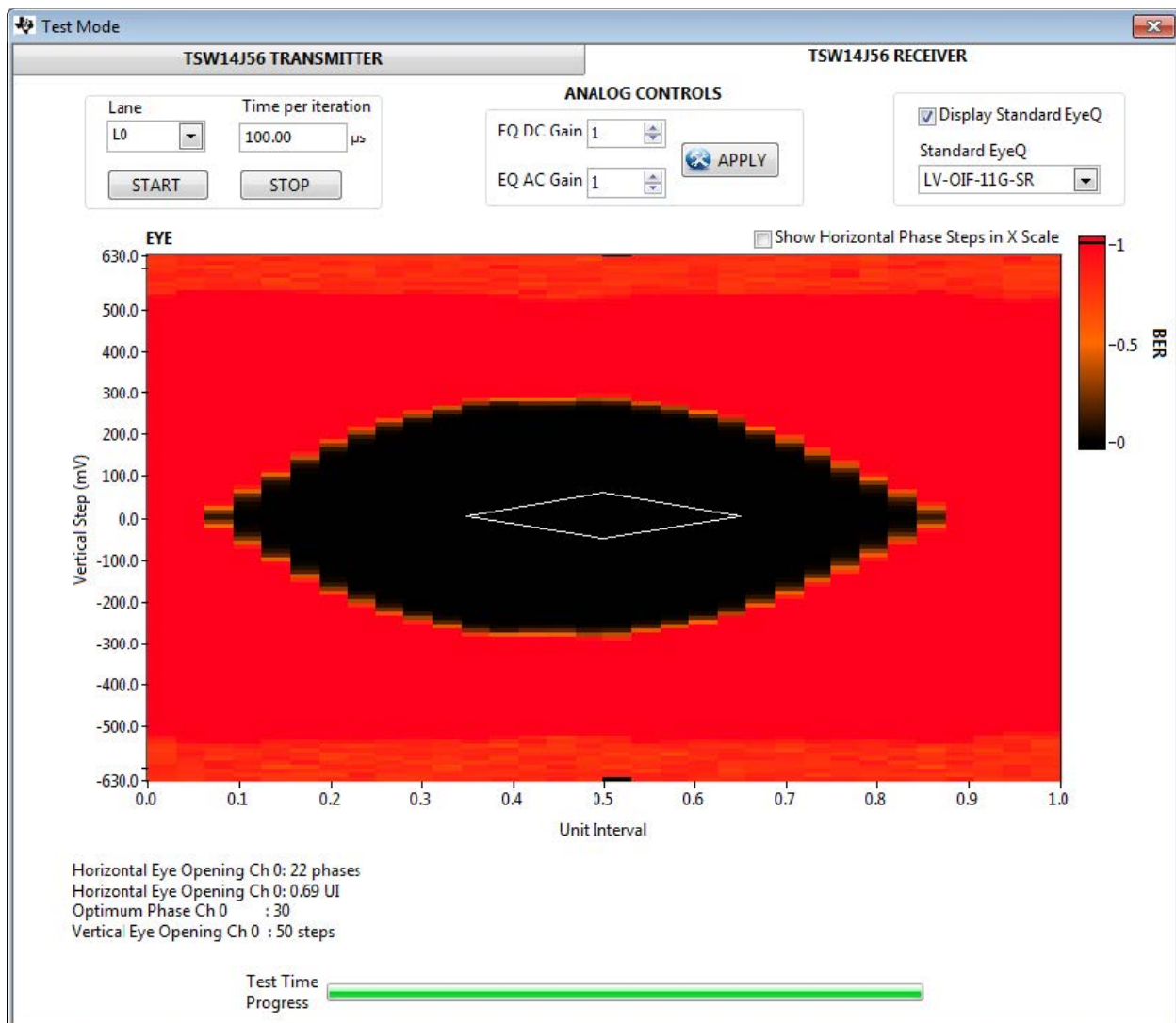
Figure 2. Baseline, 8 Gbit/second, Pre-Emphasis = 0 (min), EyeProduct = 1100
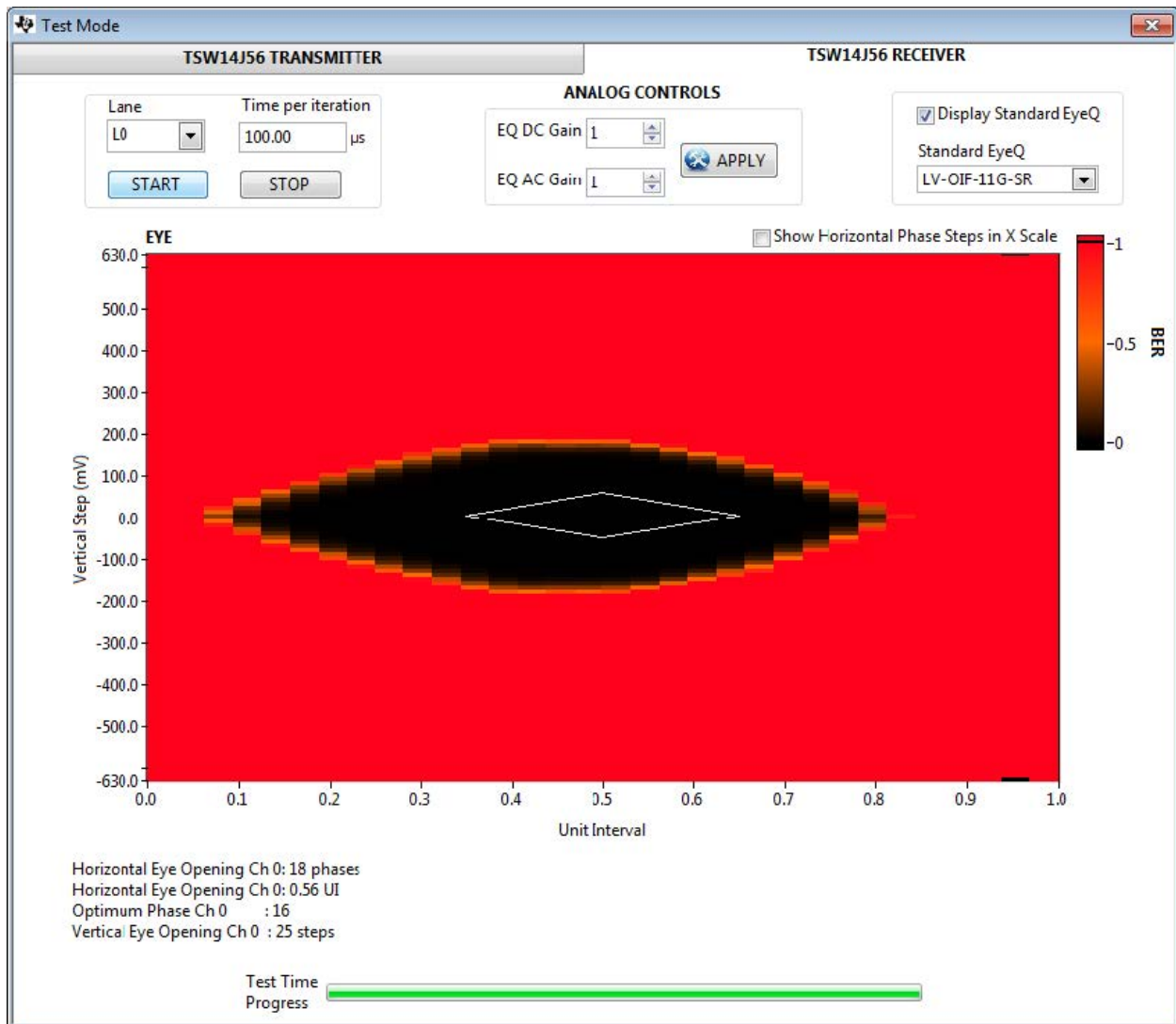
Figure 3. Baseline, 10 Gbit/second, Pre-Emphasis = 0 (min), EyeProduct = 450
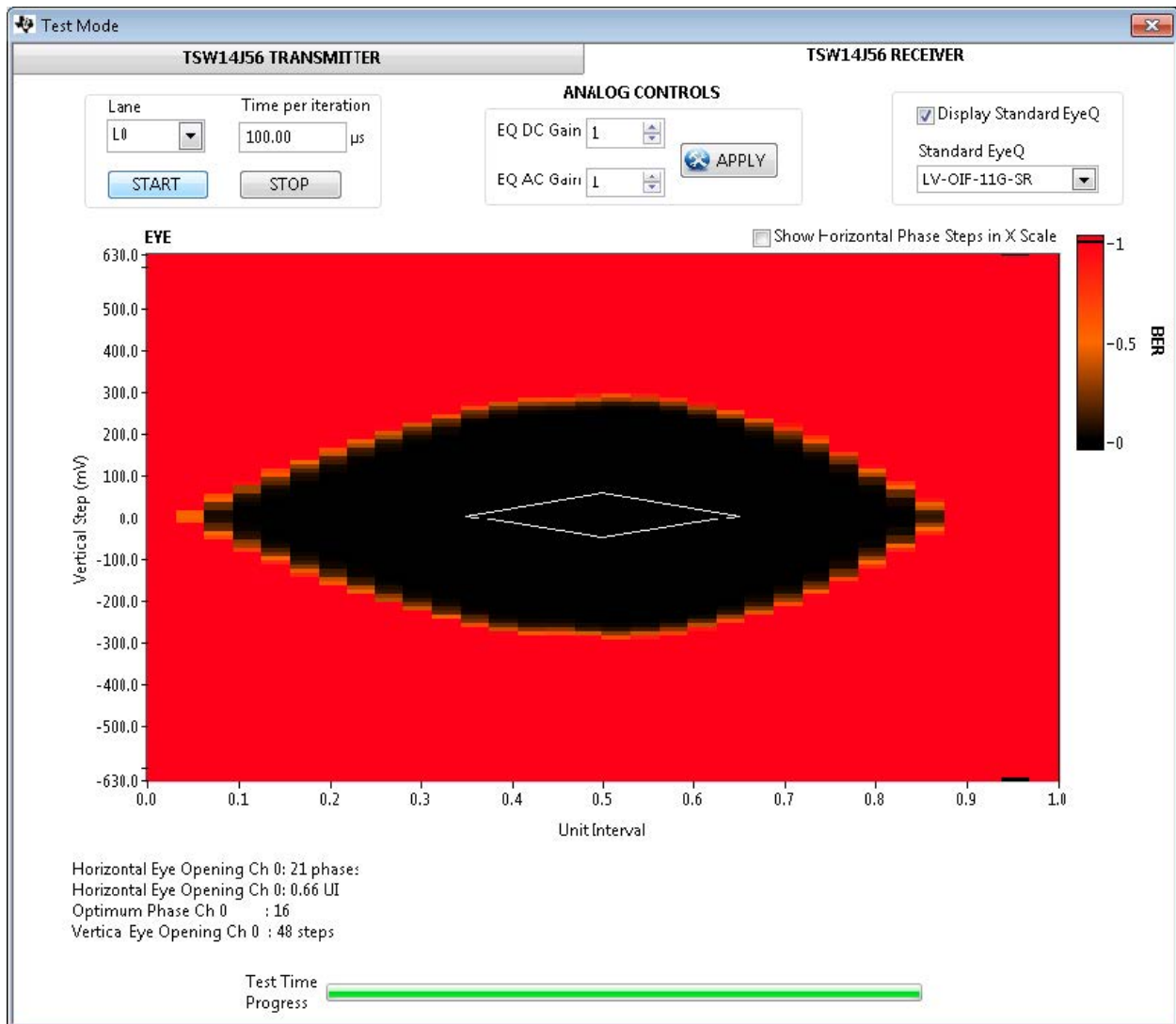
Figure 4. Baseline, 10 Gbit/second, Pre-Emphasis = 4 (default), EyeProduct = 1008

For lossy FR4-based materials and serial rates up to 10 Gbit/second, acceptable eye diagram results can still be achieved by increasing the transmitter pre-emphasis. Even with the longest 16" extender board, the eye quality meets the receiver eye-mask threshold by using the appropriate amount of pre-emphasis, as shown in Figure 5 and Figure 6.
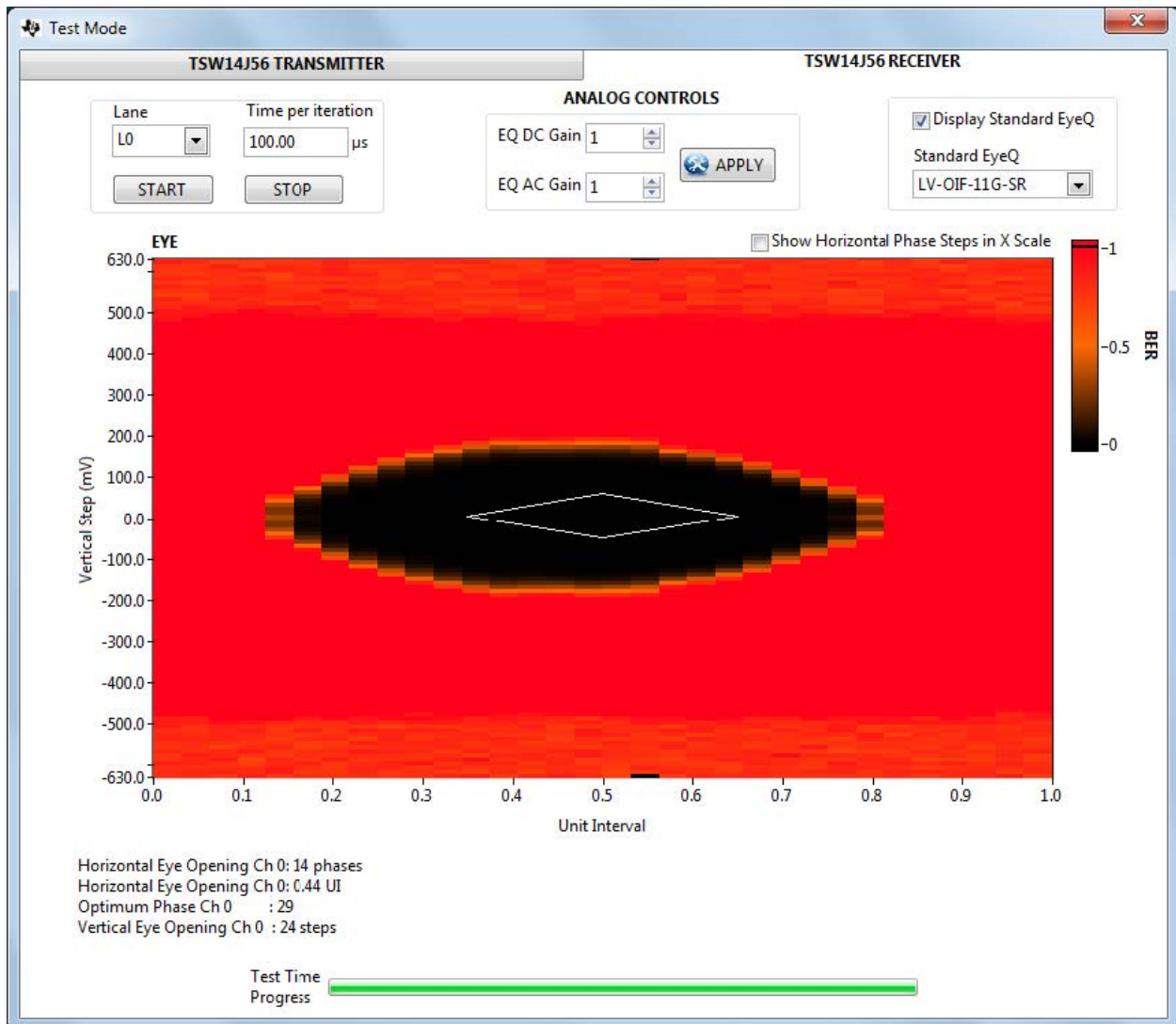
Figure 5. FR4, 8 Gbit/second, 16" Extender, Pre-Emphasis = 10, EyeProduct = 294
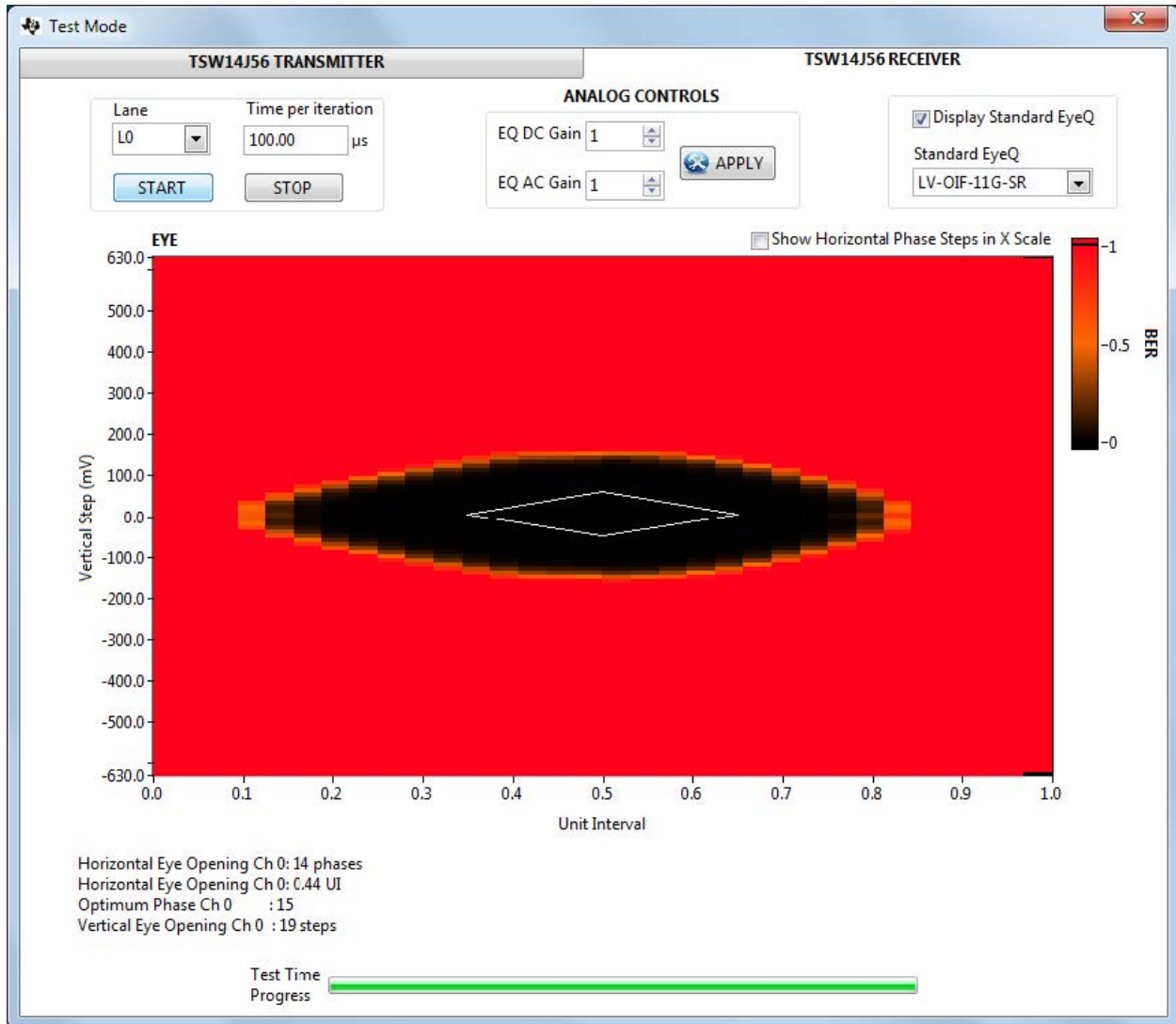
Figure 6. FR4, 10 Gbit/second, 16" Extender, Pre-Emphasis = 15 (max), EyeProduct = 266

Figure 7 shows the eye quality results for the baseline and various extenders at 10 Gbit/second. An EyeProduct value of 250 or higher typically meets the minimum receiver eye-mask requirement with design margin.
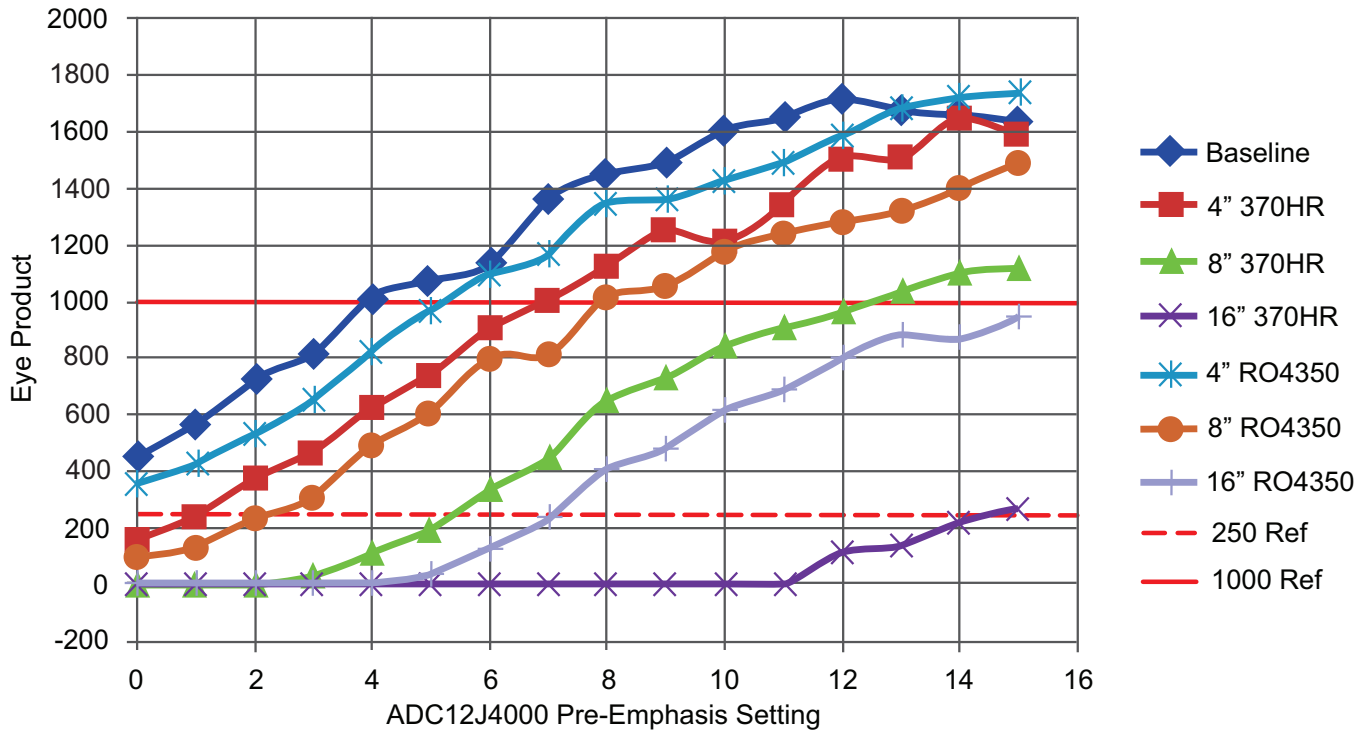
Figure 7. EyeProduct Results at 10 Gbit/second Line Rate

Figure 8 shows the eye quality results for the baseline and extenders at 8 Gbit/second:
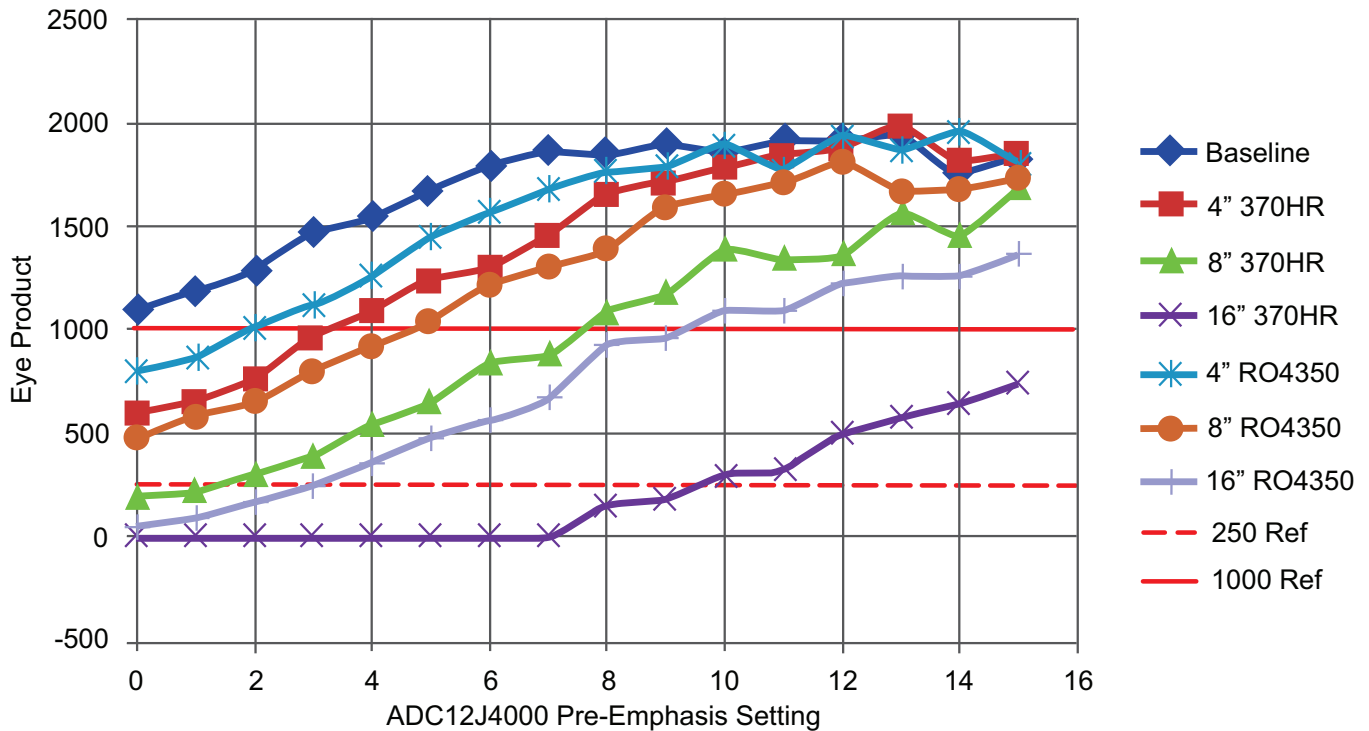
Figure 8. EyeProduct Results at 8 Gbit/second Line Rate

7   References

1. ADC12J4000EVM Evaluation Module (http://www.ti.com/tool/adc12j4000evm)
2. TSW14J56EVM Evaluation Module (http://www.ti.com/tool/tsw14j56evm)
3. Altera: *Using the On-Chip Signal Quality Monitoring Circuitry (EyeQ) Feature in Stratix IV Transceivers* (https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/an/an605.pdf)
4. JEDEC – JESD204 Standard (http://www.jedec.org/standards-documents/results/jesd204b)
5. FMC (VITA 57) Standard (http://www.vita.com/FMC)

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