Simple Power Sequencer Using MSP430™ MCUs

Introduction

Power sequencing is an essential part of many electronic designs including systems with high-performance processing devices such as FPGAs, ASICs, PLDs, DSPs, ADCs, and microcontrollers (MCU). These types of applications require specific voltage rail power-up and power-down sequencing to guarantee reliable operation, better efficiency, and overall system health. The MSP430FR2000 MCU is an ultra-low-power device that provides an elegant and cost-effective solution using only 512 bytes of nonvolatile ferroelectric random access memory (FRAM). The device's extensive low-power modes enable a current draw of 0.5 µA when waiting on a rail power-up signal and 3.5 µA when waiting on a rail power-down signal. The design also takes advantage of the Timer_B peripheral within the MSP430™ MCU to provide a programmable sequencing delay for up to eleven output flags. To get started, download project files and a code example demonstrating this functionality.

Implementation

Several GPIOs on the MSP430FR2000 provide interrupt capabilities that can wake the device from low-power modes. Using this functionality allows the MSP430 MCU to spend most of its time in LPM4, waiting on the appropriate signal to start either a power-up or power-down sequence on the output rails. The MCU then starts the Timer_B peripheral, which provides precise timing for the output signal and controls the output flags through an interrupt-based approach. This interrupt-centric design allows for lower current consumption and more precise timing of the output flags. Figure 1 shows the inputs and outputs of the simple power sequencer example code provided with this document.

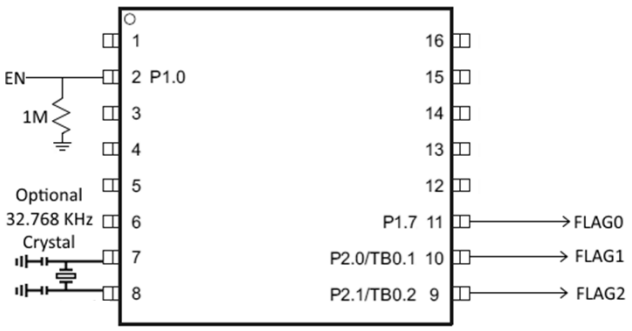

Figure 1. Power Sequencer Inputs and Outputs

TI recommends using an external 32.768-kHz crystal to source Timer_B, but the internal reference oscillator (REFO) can be used with the trade-off of higher current consumption.

After a device reset, the simple power sequencer initializes all GPIO to output driven low. This configuration enables the MSP430 MCU to achieve the lowest possible power consumption. If the power sequencer is using an external crystal, pins 2.6 and 2.7 are not configured as outputs but instead setup for crystal operation. Additionally, P1.0 is configured as an input that will trigger an interrupt on a rising edge.

After initializing the GPIO accordingly, the power sequencer initializes the Timer_B peripheral. This peripheral is used to create the precise time delays between an event on the EN pin and the subsequent response on the FLAGx output. The delay is user configurable and can be easily changed in the example code by modifying the RAIL_DELAY definition at the beginning of code. Note that there is only one RAIL_DELAY variable defining the delay between consecutive output flag level changes. Equation 1 shows how to calculate the value of RAIL_DELAY for your application.

$$RAIL\_DELAY = 32768 \times DELAY \quad (1)$$

The Timer_B peripheral is sourced from the ACLK which is then sourced from either the REFO or the external 32.768kHz crystal. The user can choose whether to use the internal REFO or external crystal by modifying the USE_REFO definition in the example code provided. ACLK is not active in LPM4 on most MSP430 devices. Therefore, the device operates in LPM3 when Timer_B is being used to create the required delays.

Finally, after initializing the GPIO and Timer_B, the power sequencer enters LPM4 with global interrupts enabled. In this state the device is waiting on a rising edge on the EN pin which will kick-off a power-up sequence on the output rails. When the rising edge is seen, the device wakes from LPM4 and enters the pin 1 interrupt service routine. From there, Timer_B starts counting and either the power-up or power-down sequence is selected.

When Timer_B counts to the RAIL_DELAY value, an interrupt is triggered and the TB0.0 interrupt service routine is entered. From there, the current output flag is toggled and the code then points to the next flag or stops the timer if the end of the sequence is reached. There are two sets of flags setup in a linked list

structure. One linked list is for the power-up sequence and the other is for the power-down sequence. Each node in the list contains the port bit that corresponds to the individual flag and a pointer to the next flag in the sequence. The last node in the sequence contains a NULL pointer signifying that the end of sequence was reached. This structure makes adding or removing flags from the sequence simple and quick while maintaining a small code footprint.

Performance

The firmware written for this application was optimized for use on the MSP430FR2000 and was tested with the MSP-TS430PW20 target board. The same code can be modified to work on any MSP430 device with a Timer peripheral. Figure 2 shows an example of the current profile for the example code provided with this document and Table 1 describes the device operation during each power sequencing sate.

There are four basic states throughout operation of the simple power sequencer. Each state operates in either LPM3 or LPM4 with several occurrences where the device enters active mode to service interrupts. The current consumption shown in Figure 2 is based on the specifications in the MSP430FR21xx, MSP430FR2000 Mixed-Signal Microcontrollers data sheet. If using a different device variant, see that device data sheet for more accurate current consumption values.

Additionally, there is a minimum delay between the EN signal and the first flag output determined by the wake-up time from LPM4 + interrupt latency of 6 MCLK cycles. A similar minimum delay exists between consecutive output flags determined by wake-up time from LPM3 + 6 MCLK cycles. For more information on LPM wake-up times, see the device-specific data sheet.

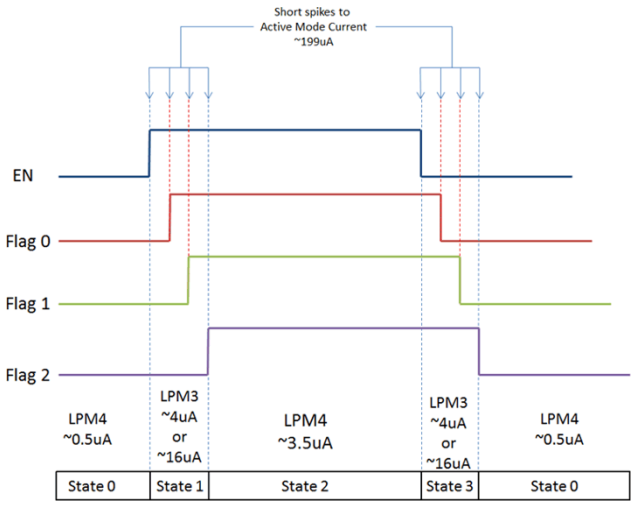

Figure 2. Example Sequence Profile

Table 1. Explanation of Power Sequencing States

State	Description	Cause of Entry	Current Consumption
State 0	Device operates in LPM4 waiting on a rising edge on EN pin	Device power up or Falling edge last flag in power-down sequence	LPM4 including SVS
State 1	Device operates in LPM3 while counting delay for output flag power-up sequence	Rising edge on EN	LPM3 including SVS + REFO (optional) + EN pulldown
State 2	Device operates in LPM4 while holding the output flags high	Rising edge on last flag of power-up sequence	LPM4 including SVS + EN pulldown
State 3	Device operates in LPM3 while counting delay for output flag power-down sequence	Falling edge on EN	LPM3 including SVS + REFO (optional)

Device Recommendations

The device used in this example is part of the MSP430 Value Line Sensing portfolio of low-cost MCUs, designed for sensing and measurement applications. This example can be used with the devices shown in Table 2 with minimal code changes. For more information on the entire Value Line Sensing MCU portfolio, visit www.ti.com/MSP430ValueLine.

Table 2. Device Recommendations

Part Number	Key Features
MSP430FR2000	0.5KB FRAM, 0.5KB RAM, eComp
MSP430FR2100	1KB FRAM, 0.5KB RAM, 10-bit ADC, eComp
MSP430FR2110	2KB FRAM, 1KB RAM, 10-bit ADC, eComp
MSP430FR2111	3.75KB FRAM, 1KB RAM, 10-bit ADC, eComp

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ('TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265