Analog Engineer's Circuit

Programmable, Two-Stage, High-Side Current Source Circuit

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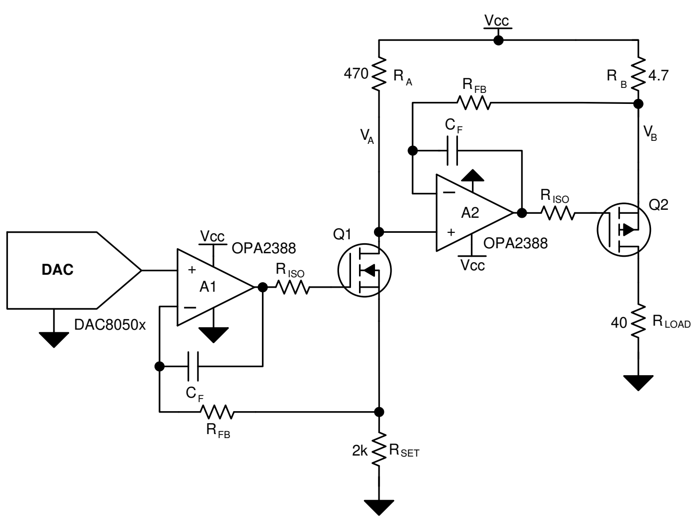
Design Goals

Supply Voltage (V_{CC})	DAC Output Voltage	Output Current	Error	Max Load Resistance	Compliance Voltage
5V	0V–2V	0–100mA	<1% FSR	45Ω	4.5V

Design Description

The programmable high-side current source supplies an adjustable current to a ground reference load. The first op amp stage sets a reference current based on the DAC output voltage. The second op amp stage acts as a current mirror that gains the reference current and regulates the current sourced from the output PMOS to the load. R_{SET}, RA, and RB set the output current based on the DAC voltage. Components C_{COMP}, R_{ISO}, and R_{FB} provide compensation to verify the stability of the circuit. Common end equipment that utilize this circuit include *PLC Analog Output Modules*, *Field Transmitters*, *Digital Multimeters, Printers, Optical Modules, LED Drivers,* and *EPOS.*



Design Notes

1. Choose a DAC with low offset, gain, and drift errors. Use RRIO op amps to maintain low compliance voltage and op amps with low offset should be selected.
2. Minimize the current flow through R_A, Q1, and $R_{SET}$by selecting a large ratio of R_A:R_B to maximize efficiency while also minimizing heating and drift in the first stage.
3. Use high-precision, low-drift resistors for R_{SET}, R_A, and R_B to minimize error caused by resistor mismatch and temperature drift.
4. Minimize the resistance of R_B to maximize compliance voltage.
5. Avoid placing Q2 near thermally sensitive components in layout as the power dissipation causes heating.

Design Steps

1. Set the reference current in the sink stage by selecting R_{SET} based on V_{DAC}. Minimize the reference current as it flows directly to ground and reduced efficiency. Set the reference current to 1mA and calculate R_{SET}.

$$R_{SET} = \frac{V_{DAC,max}}{I_{SET}} = \frac{2V}{1mA} = 2k\Omega$$

2. Select the required gain ratio based on the desired output current and I_{OUT}/I_{SET} = 100mA/1mA = 100, this is the required ratio of R_A:R_B.
3. Calculate the maximum value of R_B from the maximum allowable voltage drop to drive the maximum current through the maximum load.

$$R_B < \frac{V_{CC} - I_{OUT,max} R_{LOAD,max}}{I_{OUT,max}} = \frac{5V - 0.1A \times 45\Omega}{0.1A} = 5\Omega$$

4. The voltage V_A is $V_{CC} – I_{SET}xR_A$ which is equal to the voltage V_B due to the op amp feedback. Select R_A to achieve a voltage drop of <500mV to maintain the desired compliance voltage. A standard resistance of 4.7Ω is chosen.

$$V_A = V_B$$

$$R_A = \frac{V_{CC} - V_A}{I_{SET}} = \frac{470mV}{1mA} = 470\Omega$$

5. Calculate R_B based on R_A and the gain selected in step 2.

$$R_B = \frac{R_A}{100}$$

6. Verify the power dissipation of Q2. The power dissipation of Q2 based on the load is given by:

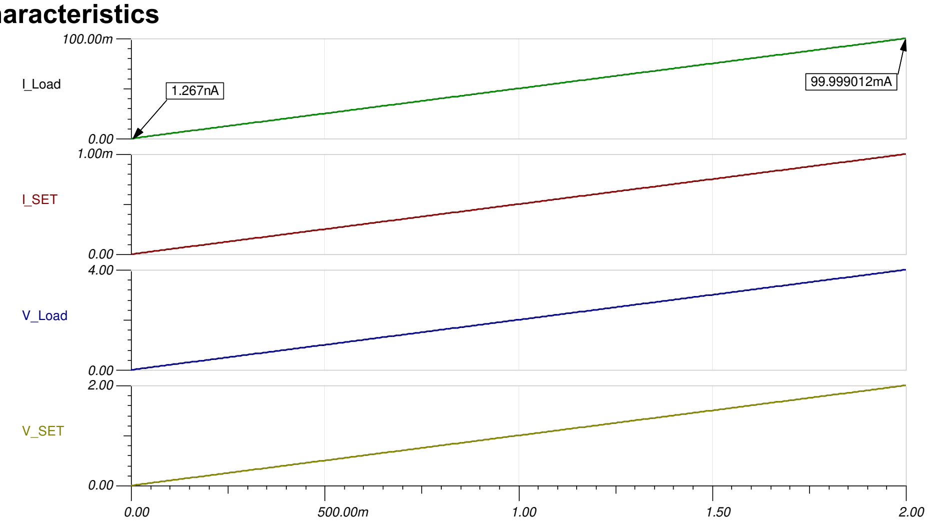
$$P_{Diss,Q2} = V_{CC} \times I_{OUT} - I_{OUT}^2 \times (R_{LOAD} + R_B) = 5V \times 0.1A - 0.1A^2 \times (40\Omega + 4.7\Omega) = 0.053W$$

The maximum power dissipation of Q2 occurs when the load resistance is zero:

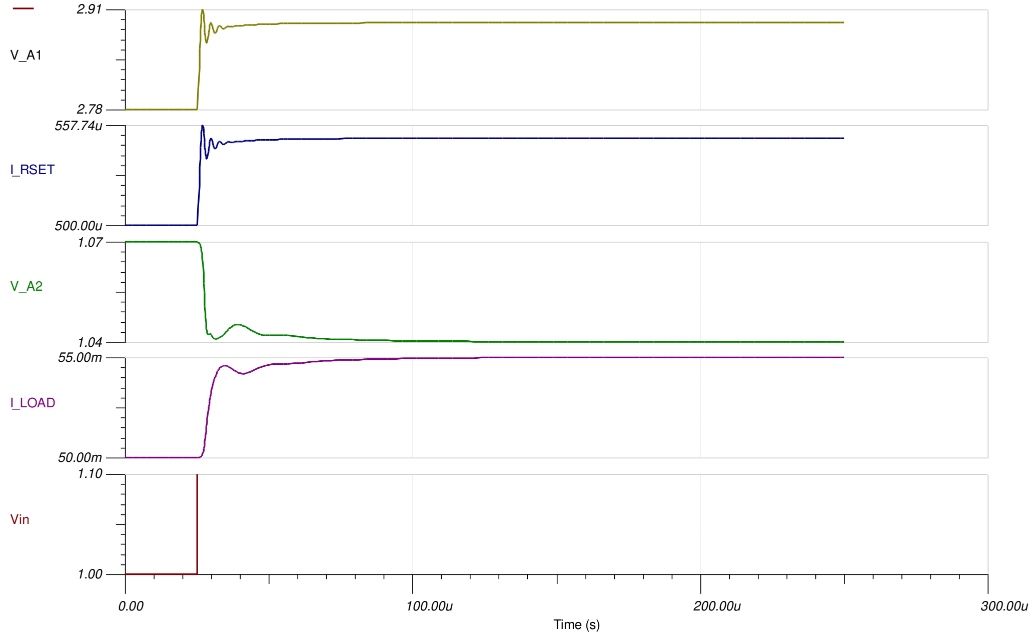
$$P_{Diss,Q2,max} = V_{CC} \times I_{OUT} - I_{OUT}^2 \times R_B = 5V \times 0.1A - 0.1A^2 \times 4.7 = 0.453W$$

Confirm that Q2 is rated for this power dissipation.

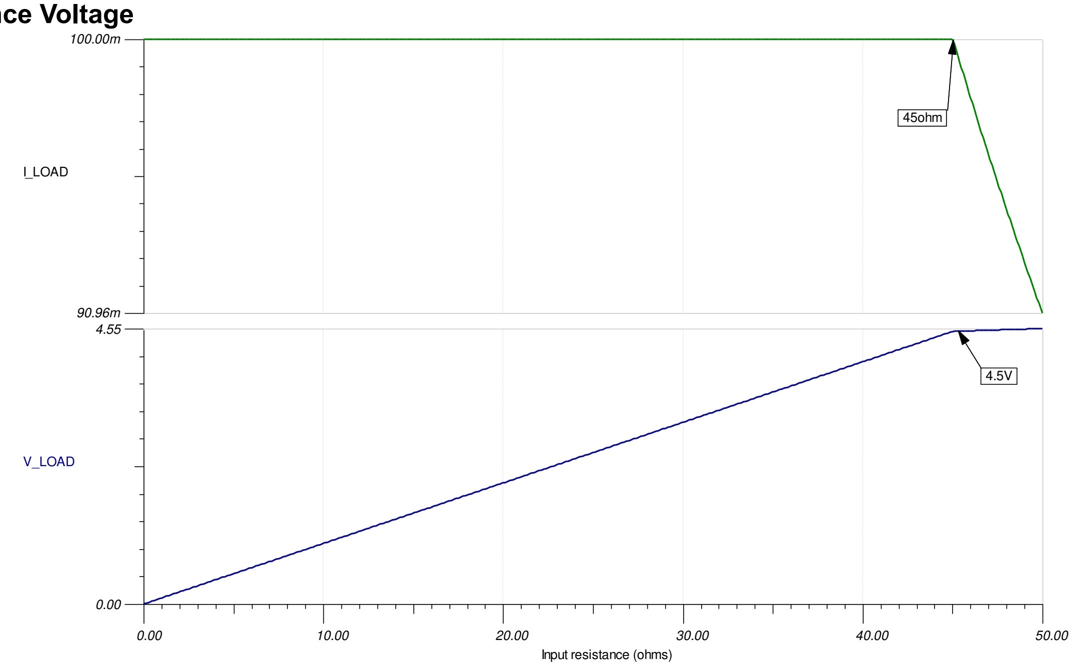
DC Transfer Characteristics



Small-Signal Step Response



Compliance Voltage



High Voltage Supply Modification

This circuit design example uses a low voltage supply for V_{CC}. Some applications, such as 4mA – 20mA current loops, require a high voltage supply to drive large resistive loads. To modify this current source for higher voltage supply, choose a high voltage, rail-to-rail input/output amplifier such as OPA192.

Devices

Device	Key Features	Link	Other Possible Devices
DACs			
DAC80501	16-bit resolution, 1LSB INL, Single-Channel, Voltage Output DAC with 5ppm Internal Reference	True 16-bit, 1-ch, SPI/I2C, voltage-output DAC in WSON package with precision internal reference	Precision DACs (≤10 MSPS)
DAC80508	16-bit resolution, 1LSB INL, Octal-Channel, Voltage Output DAC with 5ppm Internal Reference	True 16-bit, 8-channel, SPI, voltage-output DAC with precision internal reference	Precision DACs (≤10 MSPS)
DAC8775	16-bit resolution, Quad-Channel, ±10V, ±24mA Voltage and Current Output DAC, with Integrated DC/DC Converter	16-Bit Quad-Channel Programmable Current-Output and Voltage-Output Digital-to-Analog Converter (DAC)	Precision DACs (≤10 MSPS)
Amplifiers			
OPA388	Precision, Zero-Drift, Zero-Crossover, Rail-to-Rail Input/Output, 2.5V to 5.5V Supply	Single, 10-MHz, CMOS, zero-drift, zero-crossover, true RRIO precision operational amplifier	Operational amplifiers (op amps)
OPA192	Precision, High-Voltage, Rail-to-Rail Input/Output, 4.5V to 36V Supply	High-Voltage, Rail-to-Rail Input/Output, 5µV, 0.2µV/°C, Precision Operational Amplifier	Operational amplifiers (op amps)
TLV170	Cost Sensitive, Rail-to-Rail Output, 2.7V to 36V Supply	Single, 36V, 1.2MHz, low-power operational amplifier for cost-sensitive applications	Operational amplifiers (op amps)

Links to Key Files

Texas Instruments, *High side V-I converter reference design from 0V to 2V and 0mA to 100mA, 1% full-scale error*, TIPD102 overview

Texas Instruments, *Less Than 1-W, Quad-Channel, Analog Output Module With Adaptive Power Management Reference Design*, TIPD215 overview

Texas Instruments, 8-channel, 16-bit, 200mA current output DAC, reference design

Texas Instruments, source files for SLAA867, software support

Trademarks

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