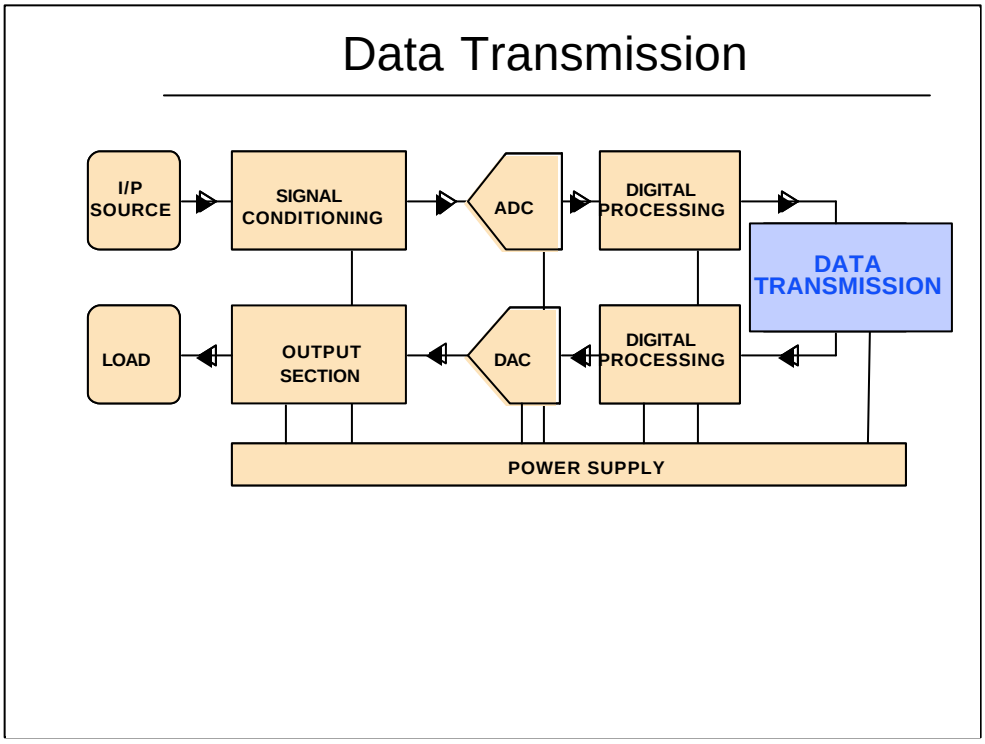
Section 6

Interface Design Solutions
for Harsh Industrial Environments

Agenda

- Data Transmission
  - Speed versus Distance
  - Single-ended versus Differential
- Transmission Line Theory
  - Circuit Representation and Parameters
- Signal Distortion
- Line Impedance and Termination Issues
- Unit Load Concept
- Eye Pattern
- Fault Protection
  - Fail Safe Operations: Internal & External
- Electrostatic Discharge
  - Human Body Model
  - Charged Device Model

This section will examine the challenges of transmitting data through some difficult environments, and give you helpful tools to deal with the issues encountered in these applications.

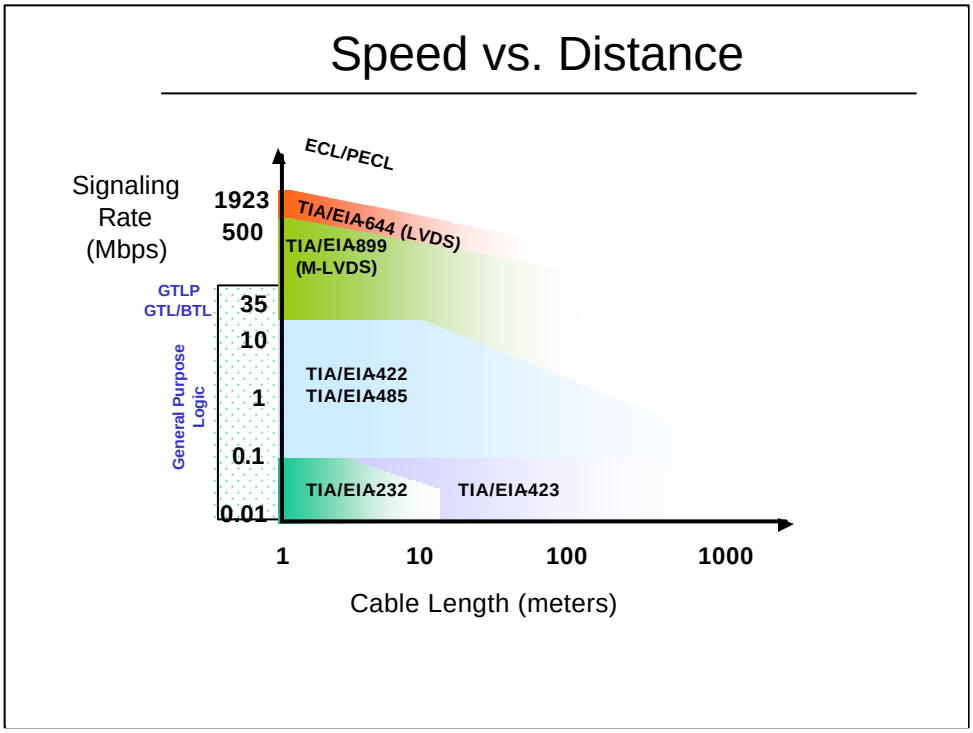


Data transmission standards evolved for two main reasons: the need to transmit data reliably over long distances, and to provide a standard interface to facilitate communication between equipment from different suppliers. Although TTL/Logic signal levels and products can be used, they generally lack the power handling capabilities, robustness and noise margins required for reliable transmission. Indeed, TTL is no longer specified for the newer high speed standards.

In general, the standards concerned with transmitting data over long distances incorporate wider voltage swings, increased robustness and higher power outputs than can be delivered using conventional 'Logic' products. The higher speeds place even more emphasis on proper termination for minimum line reflections on well defined lines, and special care taken to assure adequate noise margin in very noisy environments whether this is directly radiated or by ground shift potentials.

Many specialized data transmission devices have been developed to overcome this problem, and they work by increasing the signal level on a line, thereby improving the noise margin. The techniques involved use single ended or differential (balanced) operation with either voltage mode or current mode drive to the line.

Twisted pair and coax lines are used for single ended drive over longer distances but single- and multi-wire can be used where the data rate is low and line lengths are short. For differential data transmission a twisted pair is normally used.

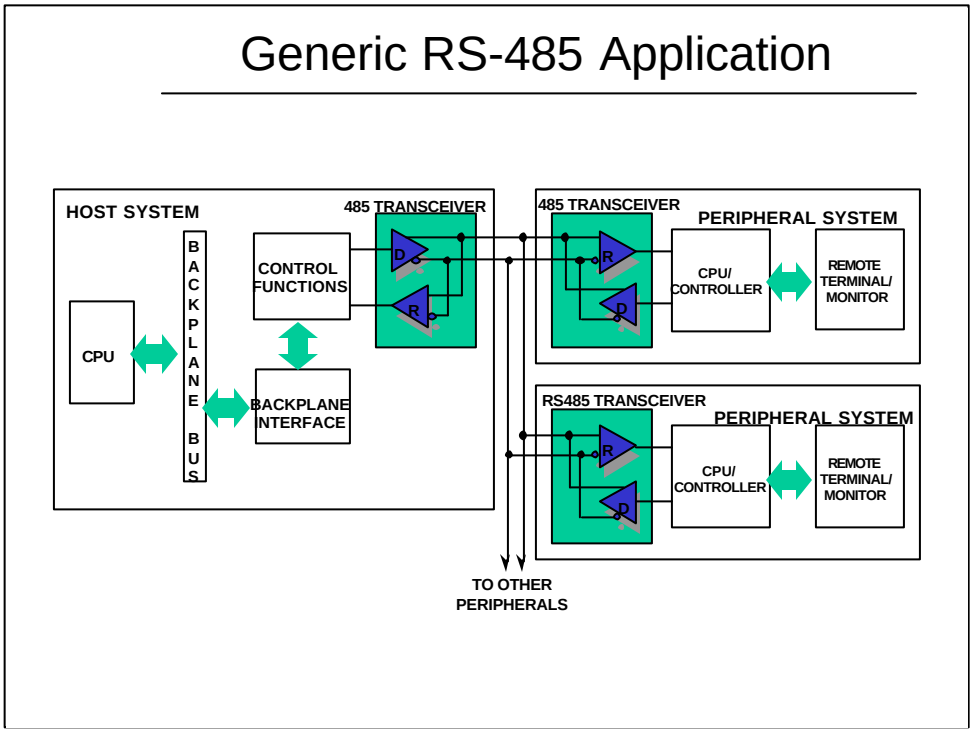


In this figure, we can see the relationship of each transmission standard when comparing data rate and line length.

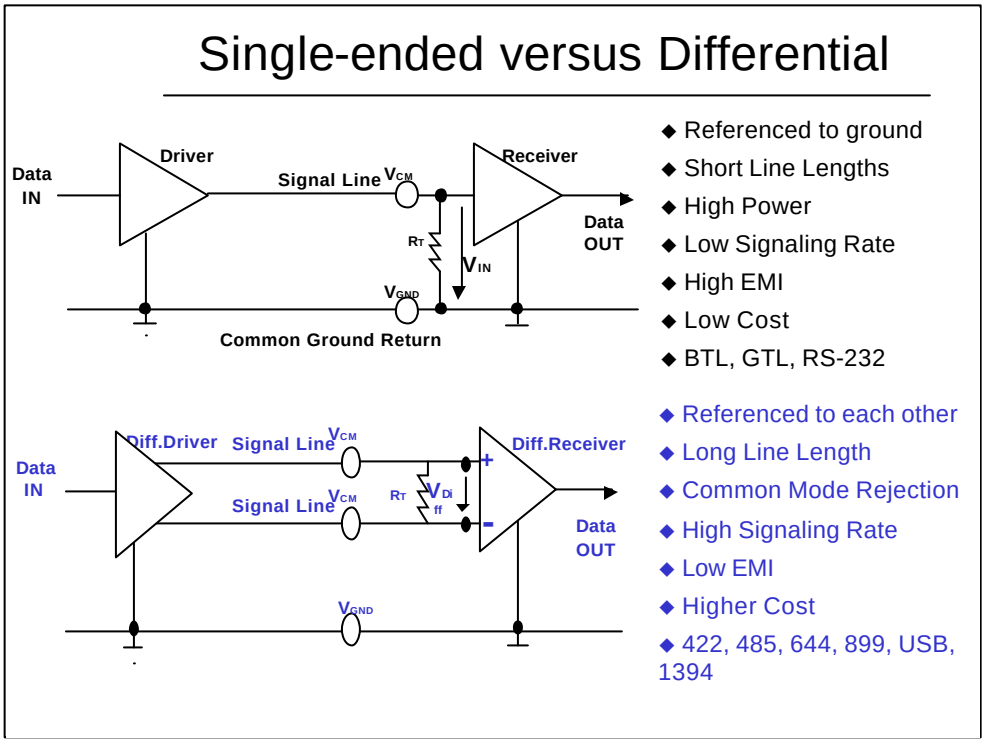
RS-485 can provide plenty of speed for any industrial application and distance of 1.2km to enable communication in a factory setting. For higher signaling rates M-LVDS, a new multi-point standard, is recommended.

If the design does not require multi-point, in other words, it is point-to-point or multi-drop, LVDS can be utilized. It should be noted that M-LVDS and LVDS' maximum signaling rates are 500Mbps and 1923Mbps respectively. For higher signaling rates, it is recommended to use LVDS-like standards, such as ECL or CML. LVDS-like should be preferred due to low-power dissipation, simpler termination networks and in most cases internal termination that will save component and real-estate on your boards.

The application that utilizes RS-485 is not only limited to harsh factory setting, but to e-Meters, Security Systems, Robotics, and Point of Sales terminals due to distance such as in Gas Stations, Actuators and Sensors.



Here, we see a generic 485 application. You have a host system which transfers data to the peripheral system. In this case, we see the multi-point interconnection, various drivers and receivers on the bus line. It can also, of course, apply to multi-drop and point-to-point for the 422 standard.



Numerous integrated circuit devices are available for driving single ended data transmission lines. Some are general purpose and others have been designed to meet specific industrial standards.

The most well-known single-ended transmission is EIA/TIA-232 or 'Recommended Standard' 232 as defined in the ANSI (American National Standard Institution) specification as "The Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange". The standard employs a single ended serial transmission scheme and outlines the set of rules for exchanging data between computer equipment, originally this being a Computer Terminal (DTE) and a modem (DCE).

The standard has evolved over the years with the latest 'E' revision released in July 1991. The standard is now known as EIA/TIA-232-E, with EIA standing for the Electronic Industries Association and TIA for the Telecommunications Industry Association. As with previous revisions of the standard the maximum data rate is defined as 20 k bits per second (kbps) although there are now a number of software applications that now push this data rate above 200 kbps, well outside the standard.

The 'C' revision defined the maximum line length as 15 meters, however this failed to comprehend the type of cable used and consequently the load capacitance on the line driver. Both the 'D' and 'E' revisions addressed this by more correctly defining the line length in terms of load capacitance. The maximum load capacitance is specified as 2500 pF that translates using standard cables to between 15 and 20 meters.

Line length and data rate are limited as the standard employs single ended communication, which is prone to external factors. For longer line lengths and higher data rates a differential balanced line communication link is essential.

Single-ended communication has the advantages of simplicity, and a minimum number of connections, which lead to low costs. However, such a system radiates RFI easily and suffers from poor noise immunity. Coax cables can improve the noise problem, but adds significant cost. Some examples of single-ended interfaces are: TTL, CMOS, BTL, GTL, RS-232 and others.

The ability to transmit data from one location to another without errors requires immunity to noise. At high data rates, on long lines or under noisy conditions, differential data transmission has an advantage because it is more immune to noise interference than single-ended transmission. Voltages induced onto the data lines by ground noise or switching transients appear as common-mode signals at the receiver input. Since the receiver has a differential input it responds only to the differential data signal. Differential drivers and receivers can operate safely within specified common-mode voltage ranges.

Differential line drivers and receivers are designed for general-purpose applications as well as specific standards. The balanced transmission line standard EIA RS-422 was developed in 1975 to interface a host computer's data, timing or control lines to its peripherals. The standard was revised (RS-422A) in December 1978 bringing it in line with its present specification. A RS-422 line allows for only one way communication (simplex) mode. By using a differential twisted pair transmission media (not specified in the standard) and a RS-422 receiver with its minimum 7V common mode voltage capacity it is less susceptible to noise picked up in hostile environments via the long cables allowed by the standard. Each driver can drive up to 10 receivers.

The specification in the standard places no restrictions on minimum or maximum operating data rates but rather on the relationship of transition speed to a unit interval. However, data rates up to 10Mbps are supported and a line length up to 1200 meters is given as a guideline, but not at the maximum data rate.

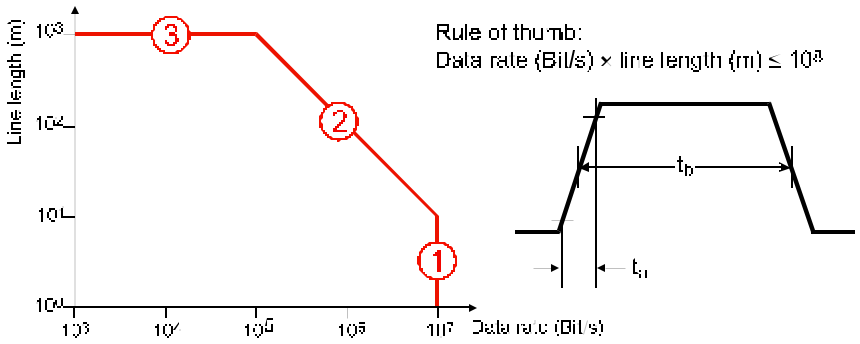
When operating at low data rates (below 200kps) or at any speed where the ratio of the driver's output rise time to the one way propagation delay time of the cable exceeds ten, the cable will not act as a true transmission line and therefore termination is not absolutely necessary. Under all other conditions, the cable loading can no longer be considered as a lumped parameter but must be considered as a transmission line. The characteristic impedance of twisted pair cable is a function of frequency and cable type. Typical twisted pair cable impedances lie in the range 100Ω to 120Ω. A termination resistor with an impedance similar to the cable's characteristics impedance should only be connected at the furthest end of the cable.

The most well-known and popular differential transmission standard is RS-485. RS-485 was primarily an upgrade to the EIA RS-422-A standard utilizing the same signal levels but facilitating half duplex multi-point communication. The standard is less complex than the EIA-232 standard as it only specifies the physical layer of the transmission scheme. Hardware such as the connector is left to the user to define. The standard specifies a balanced transmission line whose maximum line length is undefined but is nominally 1.2 km for 24 AWG cable based on 6 dB signal attenuation. The maximum data rate is also undefined but is specified by the relationship of signal rise time to bit time which is influenced both by the line driver and the line length and the line loading.

In the majority of applications it is the line length that is the limiting factor on data rate due to signal dispersion. This is discussed in later sections.

Differential (balanced) data transmission has the advantages of high common mode noise voltage rejection, reduced line radiation (less RFI), improved speed capabilities, and the ability to drive longer line lengths relative to single ended transmission. Of course, this results in slightly higher costs (sometimes), and requires the use of twisted pair or other types of balanced transmission lines. Some examples of differential transmission standards are RS-422, RS-485, TIA/EIA-644(LVDS), TIA/EIA-899(M-LVDS, USB, 1394 and others.

Maximum Data Rate



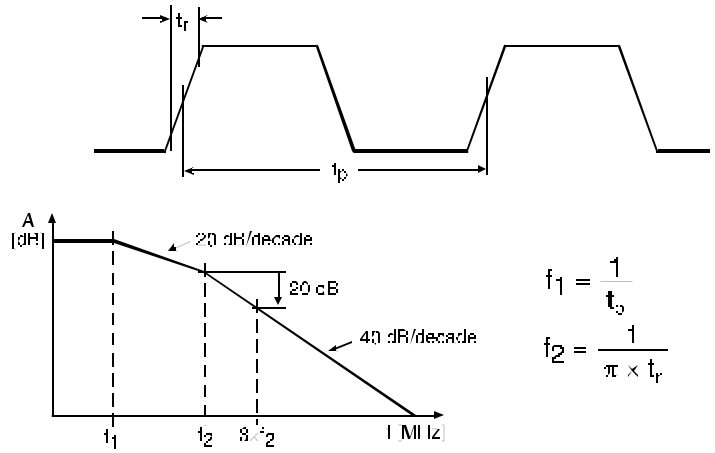
1. Data rate is limited by the rise time of the output signal of the generator (ITU-T V.11: $t_r \leq 0.1 * t_b$; ISO8482: $t_r \leq 0.3 * t_b$)
2. Data rate is limited due to signal distortion caused by losses on the transmission line (e.g. skin effect).
3. Data rate is limited due to the attenuation caused by the ohmic resistance of the wires (a 1000m twisted pair cable with wires of 0.6mm diameter has a resistance of ≈100Ω

The maximum data rate in an interface is determined by various parameters. The standards prescribe a certain rise/fall time of the signal to be transmitted in order to ensure a low signal distortion. The standard ITU-T V.11 allows the rise/fall time to be ≤ 10 % of the bit duration, while the standard ISO 8482 allows a rise/fall time ≤ 30 % of the bit duration. The rise/fall time of the signal is determined by the performance of the generator as well as by the losses of the transmission line. In ITU-T V.11 a diagram is shown (see the above picture) where the maximum data rate in an application can be taken from:

1. The maximum data rate at short lines (where the losses of the transmission line can be neglected) is determined by the capability of the generator. The standard recommends 10 MBit/s, while today's fast interface circuits like the SN76ALS176 can be operated at data rates up to 25 MBit/s.
2. When the line length becomes longer than 10 m, the losses of transmission lines have to be taken into account. Therefore with increasing line length the data rate has to be reduced. A rule of thumb says, that the product of data rate (Bit/s) and line length (m) has to be ≤ 10^8. According to this formula a line length of 100 m would result in a maximum data rate of 1 MBit/s. Note, however, that this formula refers to twisted pair cable of standard quality. High quality cables will allow higher data rates.

3. Finally at long lines the ohmic resistor of the cable and the resulting attenuation of the signal is limiting as well the data rate as well the line length. The maximum line length is determined by an ohmic resistor of the cable which is about equal to the line impedance ($\approx 100\ \Omega$). A twisted pair cable with a diameter 2×0.6 mm and a line length of about 1000 m has an ohmic resistor of $100\ \Omega$.

Spectrum of a Digital Signal



The frequency spectrum of a signal is first determined by the repetition rate of the signal f1. Above this frequency the amplitude of the overtones drops with 20 dB/decade until a frequency f2 which is determined by the rise of the signal t_r:

$$f_2 = \frac{1}{p \cdot t_r}$$

Assuming the bit rate to be 1 MBit/s, and the rise time of the signal to be t_r = 5 ns, the frequencies are as follows:

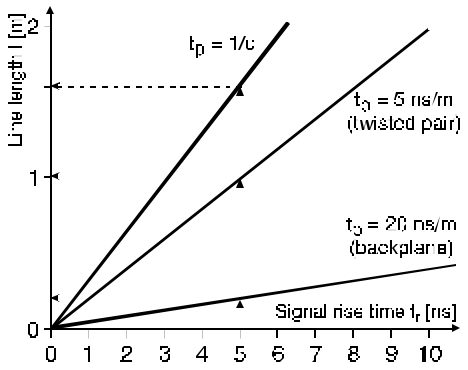
f_1 = 500 kHz (50 % of the bit rate) and f_2 = 64 MHz

If electromagnetic interference of a transmission system is of concern, the designer can improve the compatibility by either reducing the voltage swing, reducing the data rate, or by selecting interface circuits which provide output signals with a slow rise/fall time.

Transmission Line Theory

Rule of Thumb:

The transmission line theory has to be applied when the rise time of the signal is shorter than twice the propagation time.

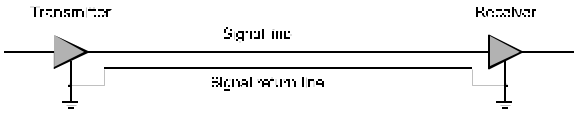


Critical line length

$$l_{max} = \frac{t_r}{2 \times t_p}$$

Transmission lines have to be treated as lines in accordance with transmission line theory when twice the signal propagation time becomes longer than the rise time of the signal - i.e.: when the line reflections no longer fall anymore into the rise time interval. For a given rise time t_r = 5 ns and a typical propagation time of the signal t_p = 5 ns/m, the critical line length in l_{max} = 1 m. In applications where the propagation time of the signal is much longer - e.g. bus lines - the critical line length is even shorter.

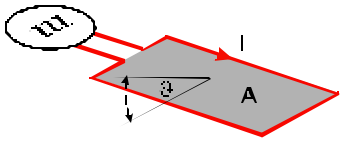
Transmission Line



A transmission line consists of
- a signal line which carries the signal current
- a signal return line (mostly ground) which carries a return current of the same magnitude.

Any DC interconnect between the GND terminals of the two circuits (e.g. safety earth) will not provide a signal return path according to the laws of the transmission line theory.

The Area between the signal line and the return line determines the capability of the circuit to radiate RF and also its susceptibility to EMI.

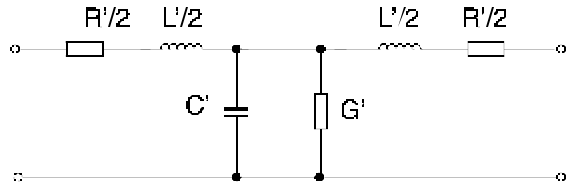


$$E = k \times I \times A \times \frac{1}{r} \times \sin\delta$$

The designer has to keep in mind that a transmission system always has two conductors: the signal line and the signal return line. Both lines have to be designed carefully to ensure the required quality of the interface circuit. Some random signal return path (e.g. via the protective ground wire) is not an adequate signal return line.

Both wires - the signal wire and the signal return wire - act as an antenna which influences the electromagnetic compatibility of the interface circuit. The larger the area between these wires, the larger will be the probability that electromagnetic energy is radiated, which may influence the function of neighboring equipment. Similarly the area between these wires also determines the electromagnetic susceptibility of the interface circuit.

Transmission Line Circuit Diagram



L'	Characteristic inductance per unit length	nH/cm
C'	Characteristic capacitance per unit length	pF/cm
R'	Characteristic resistance per unit length	Ω/cm
G'	Characteristic conductance per unit length	S/cm

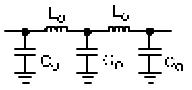
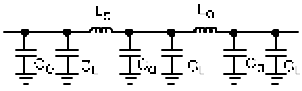
Line Impedance $\vec{Z}_o = \sqrt{\frac{j\omega L' + R'}{j\omega C' + G'}}$

The equivalent circuit of a transmission line consists of an inductance L' - representing the inductance of the transmission line -, a resistor R' - representing the ohmic resistance of the line, a capacitance C' - representing the capacitance of the line - and the conductance G' representing the losses in the capacitance of the line. All these values are length dependent and are therefore specified in unit/length, e.g.: nH/cm, pF/cm, Ω/cm, and S/cm. By setting up a set of differential equations, one can calculate the impedance of a transmission line:

$$Z_o = \sqrt{\frac{jwL'+R'}{jwC+G'}}$$

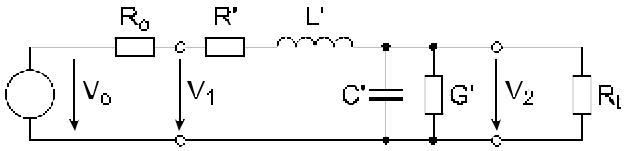
In practice this equation is difficult to handle. First, the line impedance results in a complex number which makes the required calculations time consuming. Second, the line impedance is frequency dependent. This fact becomes uncomfortable in digital circuit, where one has to consider many frequencies simultaneously.

Transmission Line Parameters

		UNLOADED	LUMPED LOADING
			
INDUCTANCE	nH/cm	L_0	L_0
CAPACITANCE	pF/cm	C_0	$C_0 + C_L$
LINE IMPEDANCE	Ω	$Z_0 = \sqrt{\frac{L_0}{C_0}}$	$Z = \sqrt{\frac{L_0}{C_0 + C_L}} = Z_0 \sqrt{\frac{1}{1 + C_L / C_0}}$
PROPAGATION TIME	ns/m	$t_{pd} = \sqrt{L_0 C_0}$	$t_{pd} = \sqrt{L_0 (C_0 + C_L)} = t_{pd} \sqrt{1 + C_L / C_0}$
CUTOFF FREQUENCY	Hz	$f_c = \frac{1}{\pi \sqrt{L_0 C_0}}$	$f_c = \frac{1}{\pi \sqrt{L_0 (C_0 + C_L)}}$

Here is the list of formulas that will be useful for your designs.

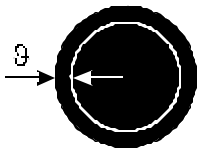
Losses on Transmission Lines



$$V_2 = V_1 \times e^{\frac{-R'}{2 \cdot Z_o}}$$

Due to the skin effect at frequencies above some hundred kHz only the outer layer of the wire conducts. This the loses increase by a factor (f)^0.5

f (MHz)	ϑ (µm)
1	68
100	6.8
10,000	0.68



Owing to the ohmic resistance of the wires R', and to a lower degree the conduction G' of the transmission lines, the amplitude of the signal is degraded with increasing line length. The voltage at the line V_2 can be calculated by using the following formula:

$$V_2 = V_1 \cdot e^{\frac{-R' \cdot l}{2 \cdot Z_o} + \frac{-G' \cdot l \cdot Z_o}{2}}$$

with G' $\rightarrow$ 0 one can simplify the equation:

$$V_2 = V_1 \cdot e^{\frac{-R' \cdot l}{2 \cdot Z_o}}$$

As an example, a transmission line with impedance Z_o = 100 Ω, length l = 1000 m and resistance per unit length R' = 0.1 Ω/m, reduces the voltage at the line end by about 40 %. The formula shown above does not consider the so-called Skin Effect. This causes the current to flow only on the surface of the conductor at higher frequencies. This becomes of importance at frequencies > 100 kHz, therefore above this frequency the resistance of the wire increases even further.

Signal Distortion

With longer lines and high data rates the losses (ohmic resistance, skin effect) have to be considered. These frequency dependent losses slow down the rise time of the signal and thus the maximum data rate.

Note: Signal propagation time not to scale

Beginning of line: t_r = 3 ns
End of line: t_r = 10 ns
Line length: l = 20 m

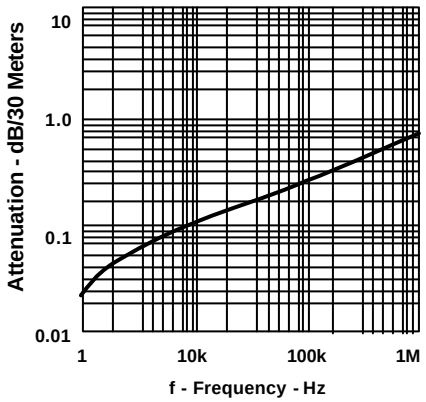
RS422: $t_b \geq 10 \times t_r$
Minimum bit duration = 100 ns
Maximum data rate = 10 MBaud

RS485: $t_b \geq 3 \times t_r$
Minimum bit duration ≤ 1/30 ns
Maximum data rate = 33 MBaud

Beside the distortions caused by the integrated circuits itself, distortion arises from transmission line losses. As discussed, the skin effect makes the transmission line act as a low-pass filter. Such a low pass filter slows down the rise time of signal and by this limits the maximum data rate.

The behavior of a twisted cable has been measured. It was found that when a signal with a rise time t_{rb} = 3 ns was applied at the beginning of the line, the rise time at the end of the line is t_{re} = 10 ns. The standard ITU-T V.11 (EIA-RS422) requires the signal rise time to be 10 % of the rise time. With a signal rise time of 10 ns the maximum data rate will be 10 MBaud. The standard ISO 8482 (EIA-RS485) allows a larger signal distortion and the rise time to be up to 30 % of the signal rise time. Using the same rise time as in the previous example the maximum data rate will be 33 MBaud.

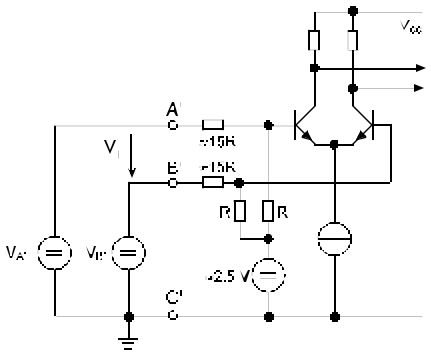
Allowable Attenuation

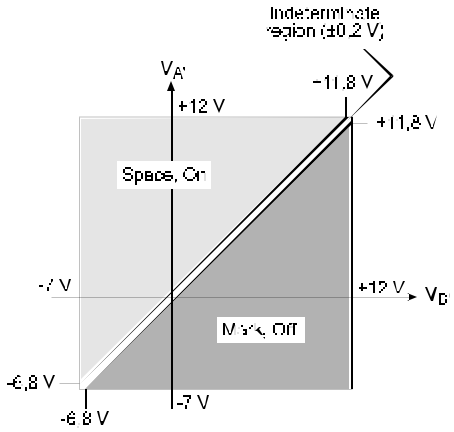


- Rule of thumb is < 6 dB at twice the fundamental frequency needed
- Figures supplied by cable manufacturers
- Curve shows attenuation change versus frequency for a 24-AWG twisted-pair cable

The rule of thumb for allowable attenuation is less than 6 decibels at twice the fundamental frequency needed by the system. These values are provided by cable manufacturers. In this figure, attenuation versus frequency for 24 gauge (AWG) twisted-pair cable is shown. As the frequency increase, the attenuation increases too, due to mostly skin effect. The rule of thumb for allowable attenuation is less than 6 decibels at twice the fundamental frequency needed by the system. These values are provided by cable manufacturers. In this figure, atte nuation versus frequency for 24 gauge (AWG) twisted-pair cable is shown. As the frequency increase, the attenuation increases too, due to mostly skin effect.

Receiver Input Voltage Range





The receiver is built up by using a differential amplifier construction (see the simplified circuit diagram above). To achieve a large common mode range (larger than the supply voltage of the circuit V_{CC} = 5 V) the input voltage is divided by a voltage divider by a factor of ≈ 15. The other end of this resistor divider is connected to an internal reference voltage of about 2.5 V. With an input voltage varying between -7 V and +12 V, the voltage at the input of the differential amplifier (the bases of the two transistors) will vary between about 1.5 and 3.5 V. Such an input voltage will guarantee sufficient margin for a correct operation of the differential amplifier supplied by a supply voltage of 5 V alone.

The sensitivity of the differential amplifier measured at the resistor divider input is 200 mV. Any differential input voltage V_i = 0.2 to 19 V will represent an On voltage, while an differential input voltage V_i = -0.2 to -19 V will represent an Off voltage. The output of the receiver is forced to the corresponding logic states.

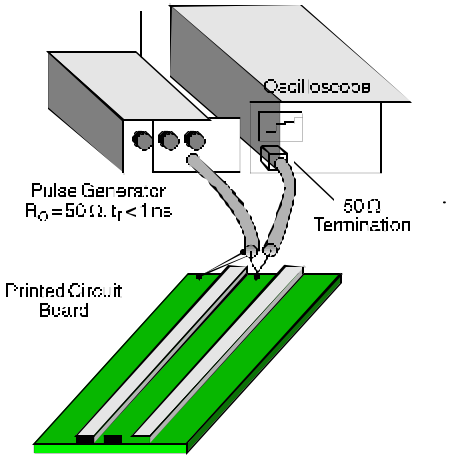
Line Termination

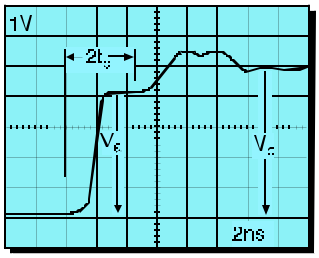
- Does the line have to be terminated?
  - Dependent upon the relationship of
    - Signal transition time, t_t, at the driver output
    - Propagation time, t_{pd}, of the signal down the cable
  - If $2\ t_{pd} \geq t_t\ /5$
    - Line should be treated as a distributed-parameter model and terminated accordingly
    - Otherwise, it can be treated as a lumped-parameter model and termination is unnecessary

There are two main cases when termination must be applied: The first one is with a long line with reflections and the second one is a short line with a low-impedance driver and capacitive load. RS-485 as defined in the standard must be terminated at both ends with 120 ohm resistors that set far end reflection to zero. Although it dissipates some static power, the advantage provided by static end termination outweighs the "side-effects."

The decision whether to terminate or not is dependent upon the relation between the signal transition time at the driver outputs and the propagation time of the signal down the cable. If twice the signal transition time is greater than one fifth of the propagation time, the system must be treated as a distributed model and MUST be terminated. Otherwise, the system can be treated as a lumped model and termination is unnecessary.

Line Impedance Measurement





$$Z_o = \frac{R_o}{V_o/V_a - 1}$$

$$t_p \times Z_o = L'$$

$$t_p / Z_o = C'$$

To correctly design an interface (selection of the generator, termination of the transmission line), knowledge of the impedance of the transmission line in use is necessary. One way to determine the line impedance is by means of an L/C bridge where one measures the inductance of a transmission line shorted at the end (short circuit impedance ≈ inductive layer L') and capacitance with the line open at the end (open circuit impedance » capacitive layer C'). This method, however, mostly requires expensive equipment which often is not available.

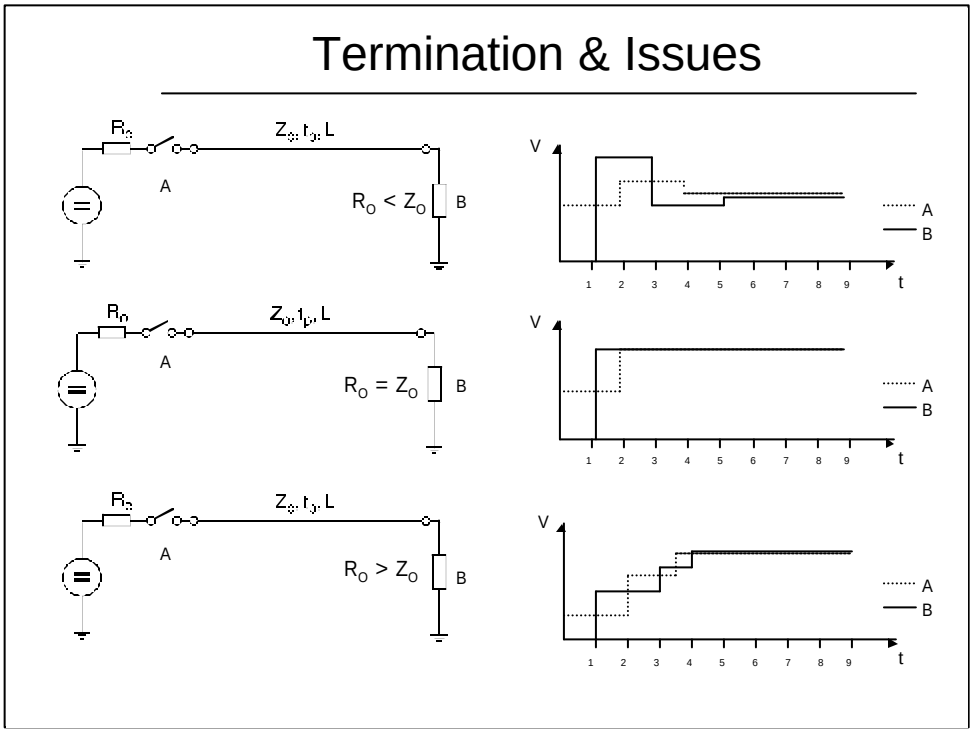
A simpler method is shown in the picture above, where one only needs a fast pulse generator and an oscilloscope. By applying this method one measures the amplitude of the incident wave V_a caused by the voltage divider created by the output impedance of the generator and the line impedance (in this example, a signal and a ground wire in parallel on a printed circuit board) as well as the steady-state voltage V_o. By using the following equation (the voltage divider formula solved to Z_o) one gets the line impedance Z_o:

$$Z_o = \frac{R_o}{\frac{V_o}{V_a} - 1}$$

where Ro is the output impedance of the generator. In this measurement setup the output impedance is made by the two coax cables in parallel, therefore Ro = 25 Ω.

By measuring the propagation time tp one can also determine the inductance and the capacitance per unit length.

$$L' = t_p \cdot Z_o \qquad C' = \frac{t_p}{Z_o}$$



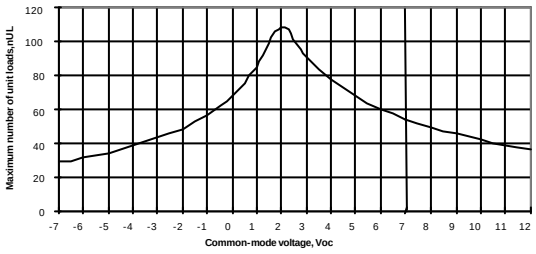
This slide shows various situations in transmission circuits. In the first circuit, a generator with low output impedance compared to characteristic impedance drives a transmission line. The signal overshoots and undershoots until settling, which is referred to as ringing.

The next circuit shows an interface terminated correctly at the line end. Under this condition one finds an undistorted signal (no line reflections.)

The last circuit shows a generator with high output impedance. The signal exponentially converges to final value.

Unit Load Concept

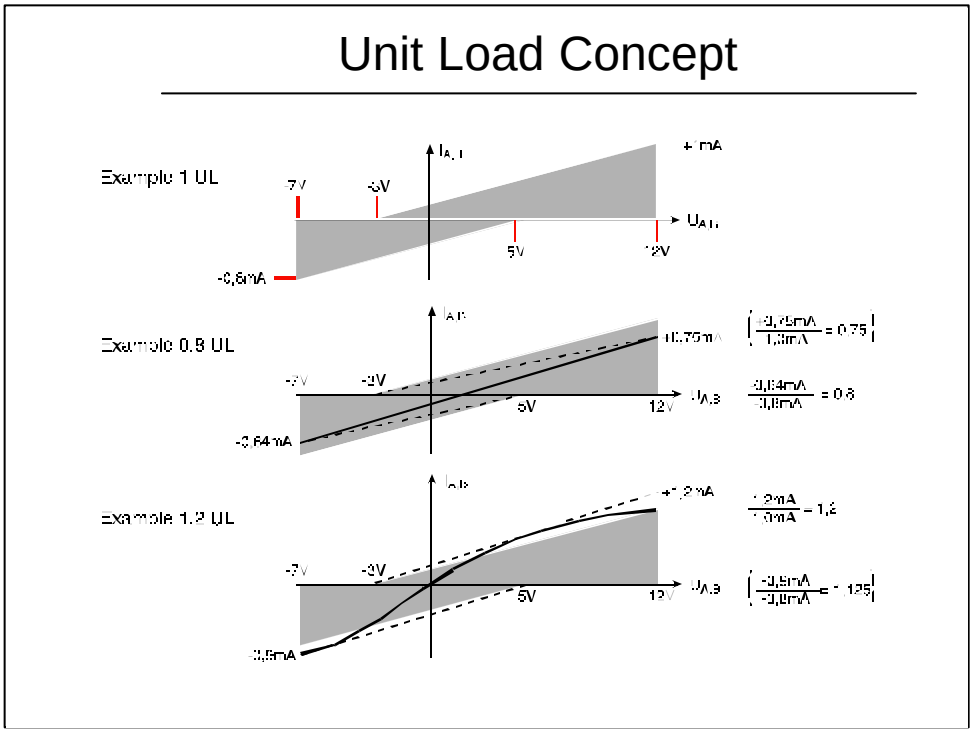
- Unit Load (UL) definition: amount of DC current a device sources or sinks to a bus over the –7 V to 5 V and –3 V to 12 V ranges of common-mode operation
- 485 standard specifies up to 32 ULs
- Number of unit-loads on a bus can be increased by
  - Restricting the common-mode voltage range of the application
  - Using reduced unit-load transceivers like TI's SN65LBC184



Reduced UL transceivers
12 kΩ = 1 UL ≅ 32 xcvrs
24 kΩ = 1/2 UL ≅ 64 xcvrs
48 kΩ = 1/4 UL ≅ 128 xcvrs
96 kΩ = 1/8 UL ≅ 256 xcvrs

The RS-485 standard specifies a hypothetical unit load and the maximum number of receiver/transmitters that can be connected to the bus with this specified load. It is defined by the amount of DC current a device sources or sinks to a bus over -7 to 5 volts and -3 to 12 volts ranges of common-mode operation.

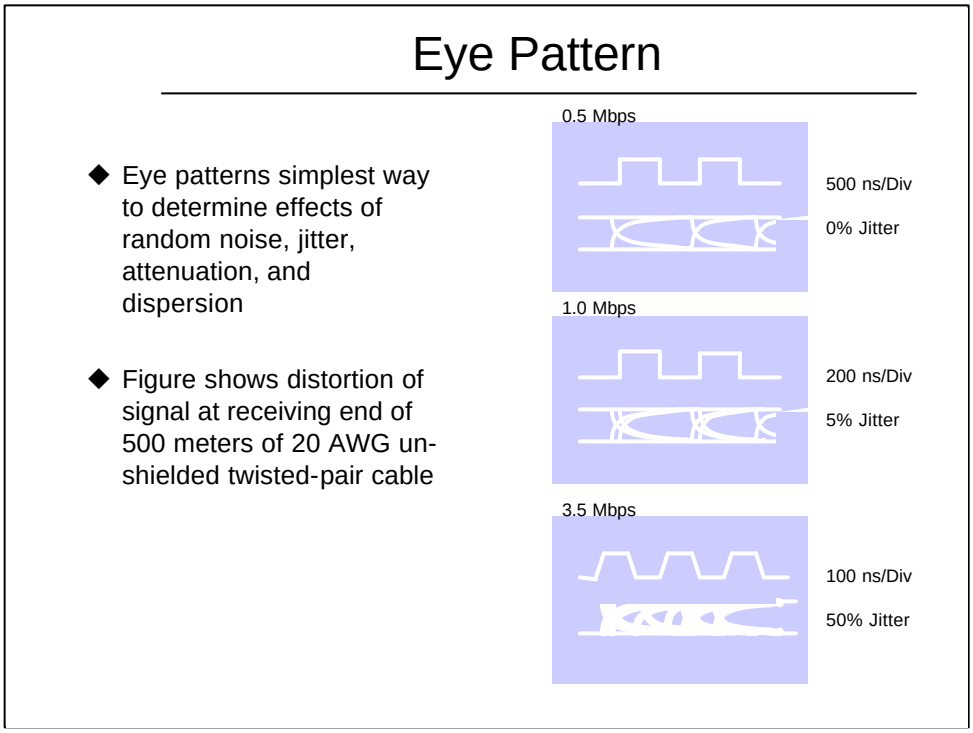
At 12 kilo-ohms, the RS-485 standard specifies up to 32 nodes. However, if the resistance is increased, effectively reducing the DC current sink or source, the number of nodes that can be connected to a bus can be increased. For 1/2 unit load, 64 nodes can be connected. For 1/4 and 1/8 unit loads, 128 and 256 nodes can be connected respectively.



The receiver's input impedance determines the maximum number of circuits that can be connected to a generator. Since semiconductor components like the receivers discussed here have mostly a non-linear characteristic, is it not possible to specify the input impedance of such a circuit by a simple resistor value. Instead a so-called Unit Load has been specified which defines an area in which the curve input characteristic has to fit.

One unit load (UL) is determined — as the picture above shows — by the corners 12 V / 1 mA and -7 V / -0.8 mA. Such a load represents a resistor of 12 kΩ. The input impedance of the receiver may be higher or lower than this value. Many advanced interfaces, for example, show a higher input impedance. The middle example in the picture represents a circuit with 0.8 unit load only. In this case, the maximum number of receivers connected to the interface can be increased according to the lower load of the circuits.

As already mentioned, semiconductor components mostly show a non linear characteristic. To determine the unit load of such a circuit one draws the input characteristic in the unit load diagram and adds a line starting from the point -3 V / 0 mA to positive voltages to be the tangential to the input characteristic. Where this line reaches the input voltage
$V_{A,B}$ = 12 V, one gets the corresponding input current $I_{A,B}$. The ratio between this input current and the input current of 1 UL gives the unit load of the circuit in question. This analysis has to be done for the positive as well as for the negative current. The greater of the two unit loads found determines the final unit load of the circuit. (see the example in the diagram above).



Using a pseudo random pattern generator, the transfer characteristic of a twisted pair cable can be obtained, providing very valuable information about random noise, jitter, attenuation and dispersion. The signal at the beginning (upper trace in the above picture) is a square wave. At the line end the low-pass filter performed by the cable slows down the rise time as well as the amplitude (lower trace). For this experiment, 500 meters of 20 AWG UTP(un-shielded twisted pair) cable is used. Initially, the data rate is set to 500 kBit/s, and jitter is negligible.

However, when the data rate is increased, jitter starts to get problematic at 1Mbps and worse at 3.4Mbps, distorting the signal such that it becomes irrecoverable. At high data rates, the ohmic resistance of the wire has only a minor influence when comparing the peak voltages at the beginning and the end of the line.

The majority of the signal quality degradation is caused by the frequency-dependent losses (skin effect). The voltage swing and the time interval left for recovering the transmitted information is the eye-shaped window in the signal flow. The height of the window gives the effective signal amplitude which has to be detected by the receiver circuit. The width of the eye determines the final time interval in which the information

has to be sampled. This picture shows also that the point of transition between the single bits varies depending on the previous bit sequence. This transition time variation is called jitter. Therefore, in many receiver systems one can find a sophisticated clock recovery circuit to regenerate the original timing (clock) of the information for correct sampling of the data.

Fault Protection

- Consideration should be given to the natural and induced environmental conditions to be encountered during operation
- Factory-controlled applications generally require protection against excessive noise voltages
- Noise immunity afforded by differential transmission scheme and wide common-mode voltage range of 485, may be insufficient
- Protection can be accomplished in a number of ways

Fault Protection is the one of the most critical parameters when designing for Industrial applications. Due to its working environment, natural and induced environmental conditions should be considered, such as transient voltages from motors, cross-talk and others.

The differential transmission scheme and wide common-mode voltage range of RS-485 may provide sufficient noise immunity from these external elements, but there are other dynamics that must be considered. Mostly, the applications are placed in dynamic environments, where the bus line can be cut, shorted to ground or V_{cc}, and protection for these fault conditions can be accomplished in a number of ways.

Fail-Safe Operation

- Fault Conditions
  - Line idle
    - Occurs in any party-line interface system with multiple driver/receivers and with long periods of time when driving devices are inactive
    - During line idle, voltage along the line is left floating (i.e., indeterminate -- neither logic-high nor logic-low state)
    - Receiver can be false triggered into logic-high or logic-low state .
  - Open-Line
    - In any party-line interface system with multiple driver/receivers, unused nodes can be disconnected from the bus.
    - It is also possible to have multichannel receivers with a portion of the channels used and unused channels left open.
    - If receiver inputs are left floating, both pins are pulled internally to the same potential, causing oscillation
  - Shorted-Line
    - Line-fault conditions (a crushed cable) can result in shorted inputs
- Fail-safe
  - Name given to methods which detect floating or disconnected bus conditions and places the receiver outputs into a known and predetermined state

There are three fault conditions that must be considered:

The first condition is idle-line, which occurs when multiple inactive transceivers drive the bus for an extended period of time. In this scenario, the voltage along the line is left floating, thereby the logic state is indeterminate. The receivers connected to the bus may be falsely triggered into high or low logic state.

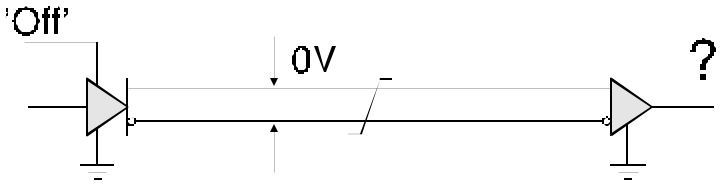
The second condition is open-line, which occurs when receiver inputs are disconnected from the bus. In this case, the input pins are floating, and because the pins are both pulled internally to the same potential, oscillation at the output can happen. Open-line condition can happen when unused nodes are disconnected from the bus or unused channels of multi-channel receiver is left un-connected.

The last condition is shorted-line. This may happen when the cable is shorted to ground or V_{cc}.

Fail-safe is the name of the method which detects these conditions and places the receiver outputs into a known and predetermined state. Please note, there are different type of fail-safe operations. Older parts tend to correct one or two conditions, but newer parts, such as TI's HVD05/06/07 and HVD10/11/12, are designed to correct all three conditions.

Undefined Logic States

With Inactive Generators (3-State)

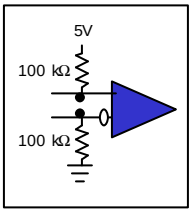


With inactive generators (3-state) the voltage difference on the transmission line becomes zero. Under this condition the receiver output becomes undefined.

In a multi-point interface, when all generators are switched into the inactive high impedance state (3-state) the differential voltage on the transmission line will be zero. A voltage of zero is an undefined state in such an interface. Refer to the input sensitivity of a receiver: $\Delta Vi > 200$ mV. In the corresponding standards the user will only find information that such a situation may occur and must take measures to avoid an undesired reaction of the system.

Open Line Condition: Internal

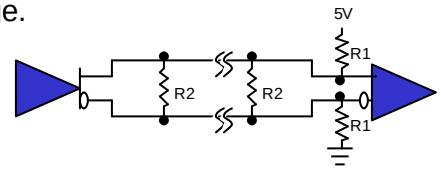
- Extra circuitry within integrated circuitry
  - Pull-up resistor on noninverting receiver input
  - Pull-down resistor on inverting receiver input
  - Resistor ≅ 100 kΩ
- Operation when used on un-terminated line
  - Non-inverting input voltage goes to Vcc
  - Inverting input voltage goes to GND
  - Differential voltage equals Vcc
- Limitations when line is terminated
  - Internal fail-safe is defeated
  - Only effective in relatively short lines and/or low frequencies that do not require a terminating resistor.



The chip includes extra circuitry to detect and correct open-line condition. There are two 100 ohm resistors tied to both inverting and non-inverting receiver inputs. The non-inverting input is pulled-up, and inverting input is pulled-down. When the line is un-terminated, non-inverting input is connected to V_{cc}, and inverting input is connected to ground. In this case, the differential voltage is equal to V_{cc}. However, the the line is terminated, this will be effective only for relatively short lines and/or frequencies, otherwise it is defeated.

Open Line Condition: External

- Purpose
  - Maintain voltage at the receiver inputs above minimum input threshold voltage (200 mV)
  - Known logic state under one or more of three fault conditions.
- R2 represents the terminating resistors and become part of a voltage divider creating steady-state bias voltage.

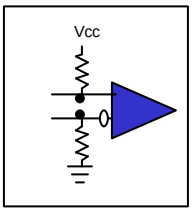


	Ω	Open	Idle	Short	UL	A, dB
R1=	620	Y	Y	N	20.5	0
R2=	120					

Assuming the chip does NOT include any circuitry for fail-safe, the design must include an external resistor network to detect and correct this condition. Here, the purpose is to maintain the voltage at the receiver inputs above the minimum input threshold voltage that is defined to be 200mV by the standard, and to place the output of the receiver to the known logic state under one or more fault conditions.

R2 represents the termination resistors defined by the standards, and it becomes the part of a voltage divider, creating steady-state bias voltage for the receiver. When 620 ohm resistors are placed in the place of R1, open and idle conditions are corrected, but not short-bus. However, this scheme changes the unit load, and the total number of nodes that can be connected to the bus is reduced to 20 without any attenuation.

Shorted-Line Condition: Internal

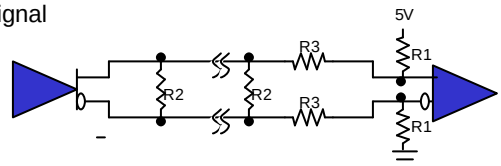


- Extra circuitry within integrated circuitry
  - Pull-up resistor on non-inverting receiver input
  - Pull-down resistor on inverting receiver input
  - Very small current sink: ≈10µA
- Operation when used on shorted line
  - Internal resistor network is isolated from outside
  - Any type of fault at the bus pin whether it be open, terminated or shorted is detected and corrected
- Limitations with Internal Shorted-line Fail-safe
  - Viths are skewed, nominally -100mv
  - Can cause receiver output pulse skew when the input signal is very small

The chip includes extra circuitry to detect and correct shorted, open and idle-line conditions. Again, there is a resistive network internal to the chip tied to inverting and non-inverting receiver input pins. The non-inverting input is pulled-up, and the inverting input is pulled-down. In this scheme, a very small amount of current sinks to the input pins. The internal resistor network is isolated from outside and all three fault conditions are corrected, but input threshold voltages are skewed, nominally -100mV, and the receiver output pulse can be skewed in the presence of a very small signal.

Shorted-Line Condition: External

- Line shorted, then termination resistors shorted, therefore differential input voltage zero.
- Extra resistors in series with receiver's input (R3) provides shorted-line fail-safe protection
- Resistors are added only when using devices with separate driver outputs and receiver inputs.
  - Internally wired transceivers cannot be used (half-duplex)
  - If used, extra resistors would cause extra attenuation of output signal



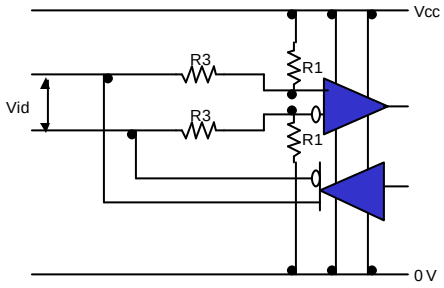
	Ω	Open	Idle	Short	UL	A, db
R1=	2500					
R3=	110	Y	Y	Y	5.6	-0.5
R2=	120					
R1=	27000					
R3=	1000	Y	Y	Y	1.5	-1.0
R2=	120					

Assuming the chip does NOT include any circuitry for a shorted-line condition, the design must include an external resistor network to detect and correct this condition. In this scenario, the line and then the termination resistors are shorted, effectively bringing the differential input voltage to zero. Extra resistors, (R3 = 110 ohms), in series with the receiver's input provides shorted-line fail-safe protection.

It should be noted that the resistors are added only when the device uses separate driver outputs and receiver inputs. Half-duplex, in other words, internally wired transceivers cannot be used, otherwise extra resistors will cause extra attenuation.

Resistor Calculation

- If line becomes shorted, R2 is removed from the circuit
  - $V_{ID} = V_{CC} * 2R3/(2R1 + 2R3)$
- For 485 applications, standard specifies max input voltage threshold (VIT) < 200 mV. So, a known state can be assumed with VID > VIT or VID > 200 mV.
  - $V_{CC} * 2R3/(2R1+2R3) > 200$ mV

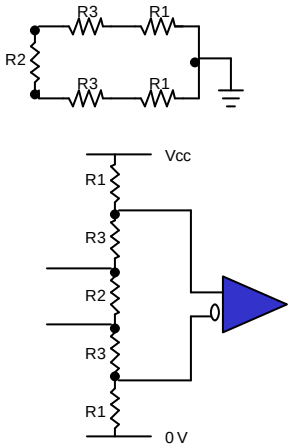


In normal operation, the resistor network consists of total of six different resistors as it was observed in previous slide. When the bus-line is shorted, R2 is removed from the circuit, and the new input differential voltage is $V_{ID} = V_{CC} * 2R3/(2R1 + 2R3)$.

The RS-485 standard defines the maximum input threshold voltage of 200mV, so for a known state this spec must be over 200mV. Using this value, we can easily calculate the values for R1 and R3.

Resistor Calculation

- As seen by driver output
  - $V_{ID} = V_{CC} * (R2 + 2R3)/(2R1 + R2 + 2R3)$
  - **$V_{CC} * (R2 + 2R3)/(2R1 + R2 + 2R3) > 200$ mV**
- As seen by receiver input
  - Should match transmission line's characteristics impedance, Z_O,
  - **$Z_O = 2R2 * (R1 + R3)/(2R1 + R2 + 2R3)$**
- Other design constraints
  - Additional line loading
  - Attenuation caused by R3, R1, and receiver's input resistance



The resistance seen by the driver output can be calculated with the following formula and 200mV spec:

$V_{CC} * (R2 + 2R3)/(2R1 + R2 + 2R3) > 200$ mV

Conversely, the resistance seen by the receiver input can be calculated with the following formula:

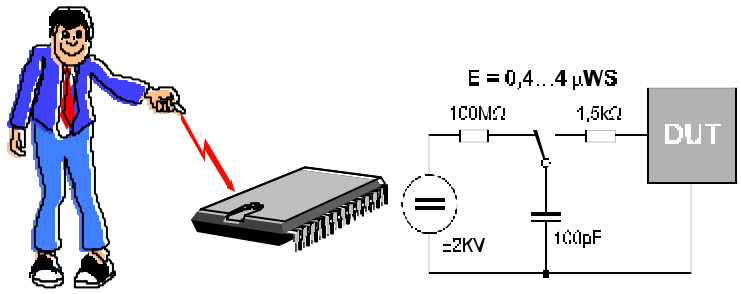
$$Z_O = 2R2 * (R1 + R3)/(2R1 + R2 + 2R3)$$

Here it should be noted that this value should match the transmission line's characteristics impedance.

When designing this resistor network, additional line loading and the attenuation caused by R3, R1, and the receiver's input resistance must be considered.

Electrostatic Discharge

Human Body Model (MIL Std 883)



The Human Body Model simulates the discharge of a human body into an electronic device.

Questions:
- Voltage?
- Capacitance?
- Resistor?
- Rise time (5 … 10ns)?

Note: When it tickles the finger, the voltage is >4000V. The real rise time during an electrostatic discharge is <1ns.

Various test methods have been developed to analyze the immunity of electronic components to damage by an electrostatic discharge. One popular test circuit is the so-called Human Body Model, which simulates the situation where the electric charge stored in a human body is discharged into the device under test.

To simulate that a capacitor C = 100 pF (capacitance of the human body) is charged up to a voltage of V = ±2000 V and is discharged thereafter via a resistor R = 1.5 kΩ into the circuit. Despite the question as to how far this test circuit really simulates the situation mentioned some comments are necessary to explain the different modes of destruction:

1. Short transition time of the discharge: The transition time of the current
   in the circuit under test at the beginning of the discharge is extremely short: t_r < 1 ns. During this short time interval only a small area of the total protection network inside the integrated circuit starts to conduct. This small area in some cases is not capable of dissipating the total power. The silicon melts and the device is destroyed. This phenomenon explains also that if the discharge does not occur in the immediate neighborhood of the circuit but at a certain distance the device will survive: the inductance of the interconnect between the point of discharge and the integrated circuit slows down the rise time. Now the total area of the integrated protection network can conduct and short the current to ground.

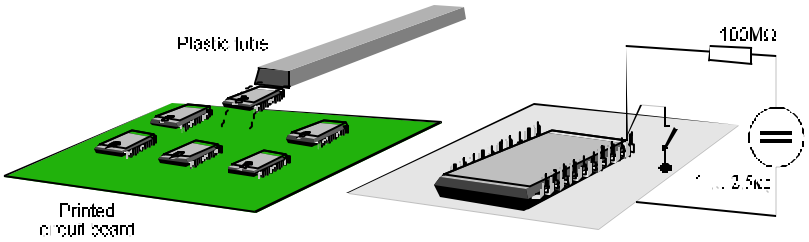
2. High current: The protection network must be able to carry the relative
high currents during the discharge. In the test circuit shown above the peak current is ≈1.5 A.

$$E_a = V_{br} \cdot V \cdot C = 20V \cdot 2000V \cdot 100\,pF = 4mWs$$

3. High energy: The protection network must capable of handling the energy during a discharge. However, the energy is not of concern. Most of the power stored in the capacitor is dissipated in the series resistor. Assuming the breakdown voltage of the device under test to be V_{br} = 20 V (in most applications only the forward voltage of the clamping diode V_f = 1 to 2 V has to be considered), the resulting Energy Ea to be absorbed by the device under test can be calculated as follows.

Electrostatic Discharge

Charged Device Model



The Charged Device Model simulates the discharge of a component charged during handling (e.g. transportation).

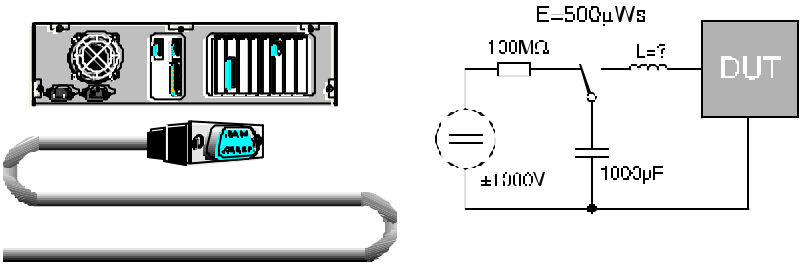
Even after continuous improvement of the capability of protection networks inside integrated circuits, damaged components were still found after assembly on a printed board. A detailed investigation showed that this destruction could be explained by the following situation: In an automatic assembly equipment during assembly the integrated circuit in question slides through the plastic tube (the container during transportation and storage) and is charged up. When the circuit lands on the printed circuit board the capacitance of the device is discharged again. By this discharge, the circuit may be destroyed.

To test the immunity against discharge the device under test is placed on a metal plate (see the above figure). The circuit is charged up to a voltage V = 1.5 to 2 kV. Thereafter the pin of the device to be investigated is shorted to the metal plate. It has been demonstrated that integrated circuits which withstand a test with a voltage V = 1.5 to 2 kV, are not degraded during the assembly cycle. Circuits which withstand a lower voltage, may be degraded.

It should be noted that no correlation has yet been found between the test results of the human body model test and the charged device model test. Circuits which show a good performance in one test environment, may fail in the other one.

Real World ESD Test

Connection of a charged cable



A cable with a length of 10 m (C = 1000 pF) is connected to an electronic equipment. The energy stored in the capacitance of the cable is discharged into the electronic components of the interface circuitry.

All the tests shown above by far do not show the rough treatment which may happen to interface circuits. A typical situation is the following: A modem needs to be connected to a personal computer. The modem is placed at one end of the room, the computer at the other end, with 10 m between these two equipments. The man who installs the cable walks through the room over carpet, which as is well-known, generates high electrostatic charge. By keeping one end of the cable in his hand, the cable may be charged up to a voltage V = 1000 V. When the cable is now connected to the equipment, the capacitance of the cable C = 1000 pF is discharged into the interface circuits. The energy to be absorbed under this condition is far higher than that found in the previous test standards.

Interface Products

TIA/EIA-485 (RS-485)	**Universal Serial Bus (USB)**
TIA/EIA-422 (RS-422)	**Gigabit Transceivers (SERDES)**
TIA/EIA-232 (RS-232)	**Appletalk/GeoPort**
CAN (ISO11898)	**IBM360/370**
SCSI	**IEEE-488 (GPIB)**
LVDS	**IEEE-802.3 (Ethernet)**
LVDM	**IEEE-896.1 (BTL)**
M-LVDS	**SCSI Parallel Interface (SPI)**
IEEE 1394	**MBus**
Infrared Data Access (IrDA)	**FlatLink**
Peripheral Component Interconnect (PCI)	**PanelBus**

Application Notes:

- 422 and 485 Standards Overview and System Configurations (SLLA070A)
- A Statistical Survey of Common- Mode Noise (SLLA057)
- Comparing Bus Solutions (SLLA06)
- Interface Circuits for TIA/EIA -485 (SLLA036A)

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